Fabricating a Slit Array for Laser-Based Angle-Resolved Photoemission Spectroscopy

Caroline Hughes
Mentor: Daniel Dessau
University of Colorado, Boulder *

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Abstract

The data obtained by the laser-based angle-resolved photoemission spectroscopy (ARPES) system in Dan Dessau's lab depends on a small wire array inside the machine. The current model of the slit array ages with time and could be improved. One method of preventing aging of the outer layer of the slit array includes changing the fabrication process and material with which its made. This new slit array includes a nano-fabricated Si structure, coated in Pt with a layer of graphene on top. This paper explores the process of fabricating this new method of achieving an array pattern in Laser ARPES.

1 Introduction

Superconductors are materials that conduct electricity perfectly, with no resistance, below a certain temperature. The first superconductor was discovered in 1911 by H. K. Onnes after he became the first to liquidize helium at approximately 4 K. [1] Onnes was interested in the resistances of different materials at this temperature which, at the time, was the coldest on earth. One contemporary theory stated that electron movement was responsible for conductivity, meaning that lower temperatures could result in less electron mobility, resulting in no conductivity and nearly infinite resistivity. However, after one test of resistivity, Onnes's results read "Mercury practically zero." [1] This marked the discovery of the first low-T_C superconductor.

The first high-T_C superconductor was not discovered until K. A. Muller and J. G. Bednorz from IBM discovered that Barium, Lanthanum-Copper-Oxide (Ba-La-Cu-O) ceramics with T_C 35 K and higher in 1986. [2] The discovery of the first high-temperature superconductors won the Nobel Prize in Physics in 1987 [3] and sparked a

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new field of high-temperature superconductor research because, although the existence of these superconductors is known, the theory behind them is not.

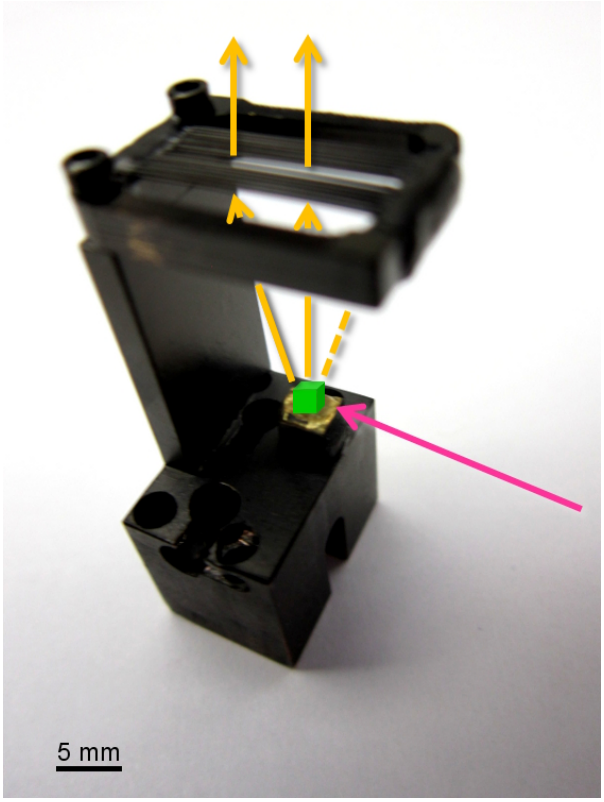


Figure 1: This is a photograph of the current system inside ARPES with cartoons added to depict the photons (pink) striking the sample (green) which emits electrons (yellow).

1.1 Modern Superconductor Research

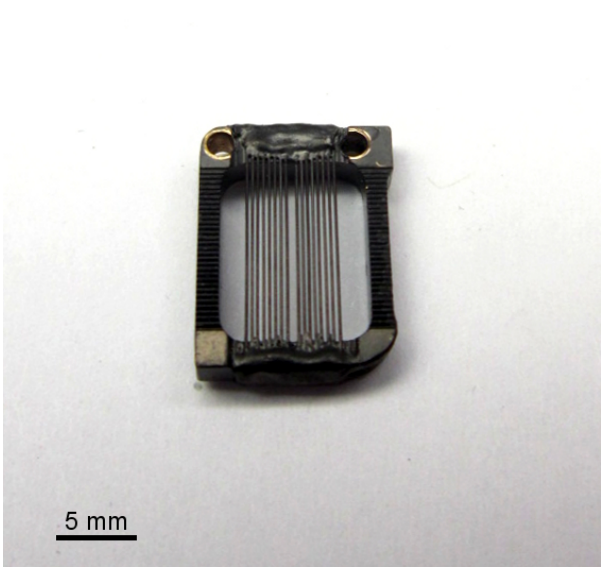
The Dessau Group tests the properties of known high-T_C superconductors, $Bi_2Sr_2CaCu_2O_{8+\delta}$, in particular, to determine what about the superconductors gives them superconducting properties. [4] The most commonly-used method of testing superconductors is with a synchrotron because it can be used at higher energy. However, laser-based ARPES has several advantages over these large synchrotrons. The entire ARPES system can be stored in one room in a lab. This significantly reduces the cost of, and increases the accessibility to, a laser ARPES system. [5] There are also advantages in the quality of results achieved with laser ARPES. Lower energy increases sensitivity and improves momentum resolution, improving the quality of binding-energy-vs.-momentum plots over those for data taken by synchrotrons. [4]

Laser ARPES works using the photoelectric effect, in which photons excite electrons in a metal to a higher energy state. Einstein discovered in 1905 that the electron can escape if the initial energy overcomes the work function, or the binding energy, at the surface of the metal. [6] The same phenomenon takes place inside the ARPES system, as shown in Figure 1, when a pulse of photons strikes the sample, which emits electrons. The energies of the photons and the electrons are related by:

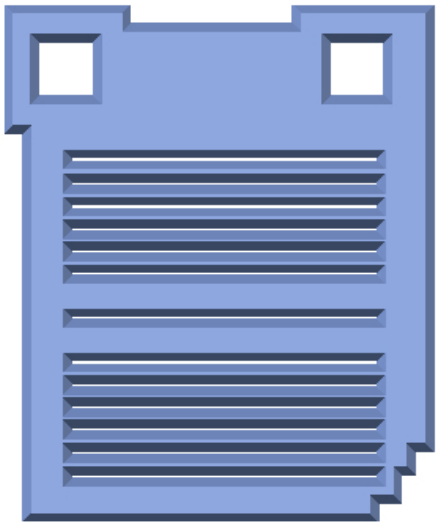
$$E_{final} = h\nu - E_{initial} - \phi \qquad (1)$$

Where $h\nu$ is the energy of the photon, ϕ is the work function of the material, $E_{initial}$ is the kinetic energy of the electron inside the solid, and E_{final} is the energy with which the electron is ejected from the metal [7]. Koralek and Dessau describe in a 2006 feature that the angle at which an electron is emitted depends on its initial momenta. [7] This creates the need for a slit array to resolve these angles into position.

The slit array is used to isolate certain electrons emitted from the sample. Any electrons that hit the slit array are deflected and are not included in the data studied. The current design, as shown in Figure 2a for the slit array, is made by Justin Griffith in the Dessau Lab from metal stretched over the outer frame. The structure is then sprayed with dag, a graphite material with



(a) This is the slit array design currently installed in the ARPES system.



(b) This is an AUTOCad model of the proposed slit array design that is the end result of the fabrication process.

Figure 2: Here is a comparison between the current and improved slit array designs.

some adhesion layer to keep it on the metal structure. The problem with the dag coat is that as the electrons pass through the slit array, they age the dag, creating uneven surfaces between the slits. Any bumps on the structure create a concentration of an electric field around these points and skews data from ARPES. The only way to fix this problem is to open the ARPES system, remove the slit array, respray it with dag and return it to the chamber. With all of the effort and money put into constructing the ARPES system, it is worth fabricating a slit array design that does not have these flaws.

The biggest change between the design of the current slit array and the new slit array, as shown in Figure 2b, is in the materials used to fabricate each. The new slit array is made from a Si(100) wafer to provide structure to the slit array, Pt, and graphene grown on top of Pt. These materials and this method of fabrication should greatly improve the current design.

2 Background

2.1 Graphene

Graphene, a monolayer of graphite, was first discovered using adhesive tape to peel layer after layer off of graphite until only graphene was left. [8] Now, single layers of graphene can be grown via chemical vapor deposition (CVD) of a mixture of methane (CH_4) and hydrogen onto copper (Cu) foils at temperatures up to 1,000°C. [9] Like dag, CVD will coat the slit array with a thin layer of graphite, but without the disadvantage of adhesion. The Schibli Lab, also in the Physics department, grows graphene on Cu using CVD. Graphene is typically grown on Cu, but the ARPES system in the Dessau group is very sensitive to any small change in electric or magnetic field. This means that it is much better to grow this graphene on Pt rather than Cu to decrease the chance of a negative impact of the new design on the

ARPES system as a whole. Graphene can be grown on Pt sputtered onto a Si/SiO_2 wafer using ethylene (C_2H_4) gas, another carbon-hydrogen combination. [10] In order to grow graphene on Pt, a new growth chamber specifically for the growth of graphene on Pt must be installed in the Schibli Lab to prevent contamination of the chamber used for graphene-growth on Cu with Pt.

2.2 Nanofabrication

Several different wet and dry etches were considered for the fabrication of the Si wafer into the shape desired for the slit array.[1] Dry etches can be very anisotropic, independently of crystal structure, with vertical etch profiles. [11] Although this seems like a good option for fabricating a very precise slit array, there are several problems with this method. One is that facilities available for reactive ion etches (RIE), a type of dry etch, are only capable of shallow etches and the wafer etched for the slit array was 380 μm. If possible, vertical sidewalls could cause problems inside ARPES. Electrons that pass through the slit could hit the sidewalls, changing the angle at which they're resolved.

Many wet etches are isotropic, or non-directional. An isotropic buffered hydrofluoric (HF) acid etch, more commonly known as a buffered oxide etch (BOE) will be used in a step necessary to complete the final etch of the Si wafer. Wet etches can also be used to achieve anisotropic etch profiles of Si wafers. A potassium hydroxide (KOH) etch is the best way to achieve an anisotropic wet etch of Si, however, the anisotropy of the etch depends on the crystal orientation of the wafer. For instance, etching a Si(100)[2] wafer along its (111) planes results in an etch profile such as that shown in Figure 3a. KOH etches Si(100) faster along the (100) planes than along the (111) planes because the (111) planes have a high bond density preventing them from etching [12]

This type of etch was chosen to fabricate the slit array because electrons that enter the slit array through the narrower slits, as shown in Figure 3b, will not be deflected by the slit array. After the KOH etch, Pt can be evaporated onto the silicon to prepare for graphene growth.

3 Process

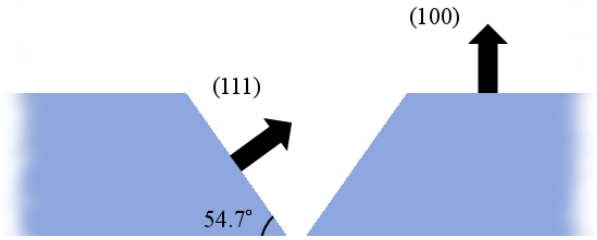
3.1 Nanolithography of Si Wafers

This process consists of four important materials: The chromium (Cr) mask, positive photoresist (PR), thermally-grown silicon dioxide (SiO_2), and the Si wafer. The Si(100) wafer, purchased from University Wafer, will provide structure to the slit array. It will be the only material from the entire etching process that will also be included in the final product. All of the other materials and processes serve the purpose of etching the wafer into the desired shape for the slit array. Infographic representations of the entire etching process, with the exclusion of designing and etching the Cr mask, are available in Figure A.1 in Appendix A.

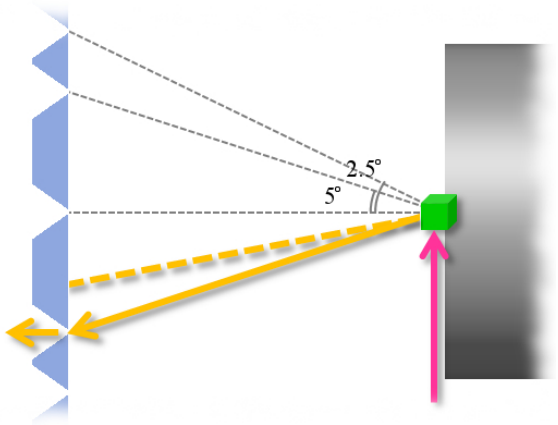
The SiO_2 mask is made from a layer of SiO_2 thermally grown on top of the Si wafer. A positive pattern is then etched in the SiO_2 mask, meaning that it is the same as the pattern that will be etched in the Si wafer with KOH etchant. There will be holes etched

[1] The Si(100) wafer was etched into the final slit array pattern at the Colorado Nanofabrication Lab (CNL), a member of the National Nanotechnology Infrastructure Network (NNIN), located in the Engineering Center on campus.

[2] (100) refers to the fact that the (100) crystal planes are parallel with the flat surface of the wafer.



(a) This is the ideal etch geometry of a Si(100) wafer showing the (111) planes at a 54.7° angle with the (100) planes. The arrows drawn are normal to the surfaces of the planes.



(b) This is a photograph of the current system inside ARPES with cartoons added to depict the photons (pink) striking the sample (green) which emits electrons (yellow). The electron that is deflected by the slit array (dotted yellow) is not included in the data.

Figure 3: Both of these factors impact the design of the Cr mask.

through the Si wafer where there are holes in the SiO_2 mask, while the Si wafer will remain unetched where the SiO_2 protects it from the KOH.

Before the uniform thermally-grown layer of SiO_2 can be used as a mask, it must first be etched into the correct pattern to act as a positive mask patterned. The layer of SiO_2 will be etched using a BOE. This etch will be completed using positive PR and will work the same way that the KOH etch of Si(100) worked where the pattern etched in the SiO_2 will be the same as that exposed in the PR, which depends on the pattern of the Cr mask.

3.1.1 Photomask Design

Designing the photomask is the first step of any etching process. If the wafer is covered with positive PR prior to etching, the etched wafer will have the same pattern as that on the photomask. If the wafer is coated with negative PR, the wafer will have a resulting pattern inverse of that of the photomask.

The anisotropy of the (100)-Si wafer etch was crucial to the design of the Cr mask. The KOH etch of Si(100) stops on the (111) planes, which are at an angle of 54.7° to the (100) planes. This means that a two-dimensional rectangular feature on the Cr mask will appear as a three-dimensional pyramidal structure, with a narrow slit on the bottom (unpolished) side of the wafer and a larger slit on the top (polished) side of the mask, as shown in Figure 3a, when etched. The finished slit array will be installed in the ARPES system so that the electrons pass through the narrow slits first, as shown in Figure 3b. This etch profile was taken into account when designing the Cr mask so that the bottom of the etch would be the size required for the side of the slit array. The width of the larger portion of the slit was calculated with the equation:

$$W = w + \frac{2 * h}{tan(54.7°)} \tag{2}$$

Where W is the width of the feature dimension on the mask, w is the width of the feature dimension at the bottom of the mask, h is the wafer thickness, and

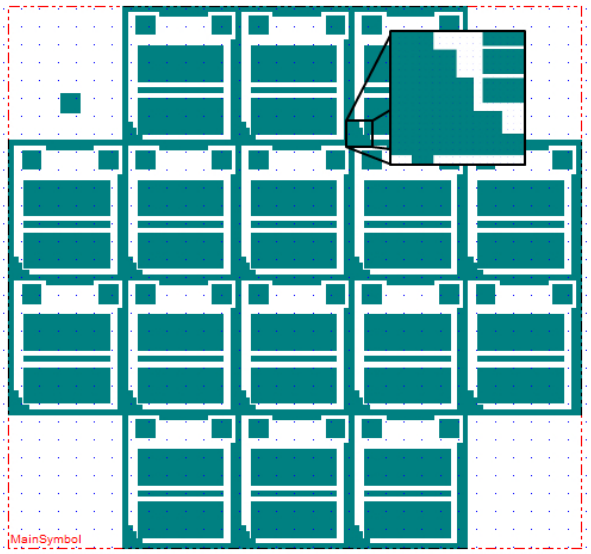
$tan(54.7°)$ is given by the angle between the (111) and (100) planes, shown in Figure 3a, that determines the relationship between the vertical and horizontal etching of the Si(100) wafer. For example, the slits used in this wafer design were 50 μm. By this equation, in order to achieve a lower level dimension of 50 μm, the upper dimension patterned on the mask should be 588 μm.

The widths of these slits determined how many slits could be included on the slit array pattern so that the slits did not overlap. Since the slit array is used for angle resolved photoemission spectroscopy, the separation between the slits is angular as shown in Figure 4. The minimum separation of the slits was 2.5°, allowing for 11 total slits on the slit array. The two slits on either side of the center slit were removed so that the center of the slit array was apparent when analyzing data taken by ARPES.

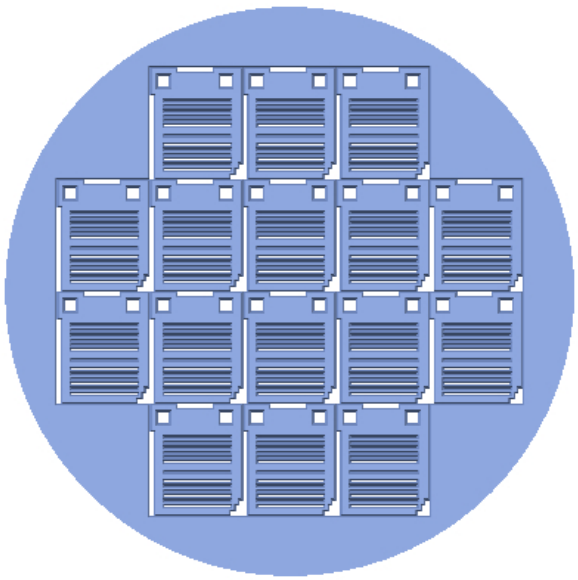
Multiple copies of the slit array design can be fabricated on the same wafer as a more efficient use of space. Although it was designed in AUTOCad, the pattern was converted to a CleWin file, as shown in Figure 4a, the same as that used by the Heidelberg Mask Generator in CNL. Theoretically, if the etch comes out exactly as planned, it should resemble Figure 4b. The spaces between the slit arrays are etched nearly all the way through the wafer. Scribing the wafer and then cleaving it along these lines will finish the process.

3.1.2 SiO_2 Growth

SiO_2 was grown on three blank Si wafers using CNL's Tynal Oxidation Furnace, as shown in Figure A.1a. This layer will be etched and used as a "hard" SiO_2 mask on top of the Si(100) wafer. The SiO_2 mask is hard because it was thermally grown onto the Si(100) wafer. The thickness of SiO_2 required to withstand a KOH etch of a Si(100) wafer is given by the equation:



(a) Although it looks like there are not 11 different slits on each pattern, the zoomed-in view shows they are just too small to be seen.



(b) This is what the wafer should look like at the completion of the KOH etch.

Figure 4: Here is a comparison between the pattern used to create the Cr mask and the theoretical design of the etched wafer.

$$h_{SiO_2} = \frac{h_{Si(100)} * e_{KOH,SiO_2}}{e_{KOH,Si(100)}} \quad (3)$$

Where h_{SiO_2} is the thickness of the SiO_2 layer, h_{Si} is the thickness of the Si(100) wafer, e_{KOH,SiO_2} is the etch rate of SiO_2 by KOH, and $e_{KOH,Si(100)}$ is the etch rate of Si(100) by KOH. The Si(100) wafer was 380-µm thick, as ordered from University Wafer and the etch rates of SiO_2 and Si(100) by KOH at 70°C were 24 µm/hour and less than 100 nm/hour respectively. [13] This means that the desired thickness of the SiO_2 layer is approximately 1.583 µm. The actual thickness of SiO_2 grown on the wafer was approximately 1.869 µm at a temperature of 1,150°C for a duration of 7 hours.[3] [14] The extra thickness was intended to ensure that the SiO_2 remained on the Si(100) wafer for the duration of the 16 hours it would take to etch all the way through the wafer, as shown in Equation 5.

3.1.3 Preparing for Etching

The BOE of the SiO_2 layer transfers the mirror image of the pattern on the Cr mask onto this SiO_2 layer. Several steps, including spinning PR onto the wafer, as shown in Figure A.1b, and exposing and developing the PR, are required in order to prepare the SiO_2 layer for the BOE.

Both the front (polished) and back (unpolished) sides of the wafer were coated with positive PR, AZ 4210, using PR spinners. Using positive PR meant that the BOE would not etch where the wafer is coated with PR. Only the front of the wafer would be etched, but the back also had to be coated in PR to prevent it from etching. The back of the wafer was coated in PR first because the finish on the front of the wafer was more important than that on its back. Before it was coated in PR, the back of the wafer was cleaned on a spinner with distilled water to remove any dust that might be on the wafer, acetone to strip any chemicals that might be on the wafer from its surface, and finally with isopropanol to clean the acetone from the wafer, and air-dried. The mask was then pre-dried on a hotplate at 110°C for two minutes to remove any residual water droplets from the wafer surface. Next, the PR was spun onto the wafer at 6,000 rotations per minute for 30 seconds. Since the wafer was 3 inches in diameter, it took two syringes of PR to coat the entire wafer prior to starting the spinner. Finally, the wafer was prebaked on a hotplate at 100°C for 90 seconds to harden the PR on the wafer. The same steps were repeated to apply PR to the front of the wafer.

Once the PR was applied to the wafer, the wafer was aligned with the Cr mask, as shown in Figure A.1c, and the pattern was transferred onto the wafer using UV light. The PR was removed where it was exposed to the light and remained on the SiO_2 layer where it was not, as shown in Figure A.1d. This was then developed with solution AZ 400 for 1 minute and 15 seconds. During this portion of the process, the excess PR was actually removed from the SiO_2 layer. Now the Si(100) wafer was finally ready to be etched.

3.1.4 BOE and KOH etch

The etch time it took to BOE the SiO_2 was given by the equation:

$$t_{BOE} = \frac{h_{SiO_2grown}}{e_{BOE,SiO_2}} \quad (4)$$

Where t_{BOE} is the duration of the BOE, h_{SiO_2grown} is the thickness of the SiO_2 layer grown onto the Si(100) wafer, and

[3]Information from CNL is available through the user Website only.

e_{BOE,SiO_2} is the etch rate of SiO_2 by BOE, 97 nm/minute. [15] This resulted in a predicted etch time of approximately 19 minutes. After 19 minutes, the wafer was checked under a microscope with a red filter as not to expose the PR remaining on the wafer. At this point, the SiO_2 layer could be etched longer if necessary. Once the BOE was complete, as shown in Figure A.1f, the PR that was not exposed to the UV light and removed from the wafer was washed off of the wafer by the same process with which the wafer was cleaned prior to the pre-dry.

Finally, the Si(100) wafer was etched with KOH at 70°C for 16 hours, as shown in Figure A.1g, by the equation:

$$t_{KOH} = \frac{h_{Si(100)}}{e_{KOH,Si(100)}} \tag{5}$$

Where t_{KOH} is the duration of the BOE, $h_{Si(100)}$ is the thickness of the Si(100) wafer, and $e_{KOH,Si(100)}$ is the etch rate of SiO_2 by KOH, 24 μm/minute. [13] The substrate was put into a beaker of KOH submerged in a hot bath of water. The bath had to be refilled every 8 hours to ensure that there was enough water to keep the KOH at a constant temperature. In an improved procedure, the Si(100) wafer was removed from the KOH every few hours and examined to determine how the etch effected the wafer in correlation with time. These results are available in Appendix B.

3.2 Graphene Growth Chamber Construction

Graphene was intended to be grown on the Pt-coated Si wafers in the Schibli Lab, also a part of the University of Colorado, Boulder Physics Department. The Schibli Lab focuses on growing graphene on Cu. However, the ARPES chamber required graphene growth on Pt. To prevent contaminating the Cu chamber with Pt, a new chamber was constructed for the specific purpose of the growth of graphene on Pt.

This new Pt chamber, used for the growth of graphene on Pt, was constructed to replicate the Cu chamber, used for the growth of graphene on Cu, currently in place in the Schibli Lab. It was important that the Pt chamber matched the Cu chamber very closely so that it could replace this chamber in the Schibli Lab set-up. Both chambers consist of two quartz tubes, an inner quartz tube that fits inside an outer quartz tube. There is one stainless steel quick flange (KF) on either end of the outer quartz tube where it will be connected into the Schibli Lab's graphene growth system.

Both the outer and inner quartz tubes were cut using the glass cutter in the JILA machine shop so that the entire chamber, with KFs on either end of the outer tube, would match the dimensions of the Cu chamber in the Schibli Lab. The 25-KF on the right end of the outer quartz tube and the 50-KF on the left end of the outer quartz tube were machined to an outer diameter

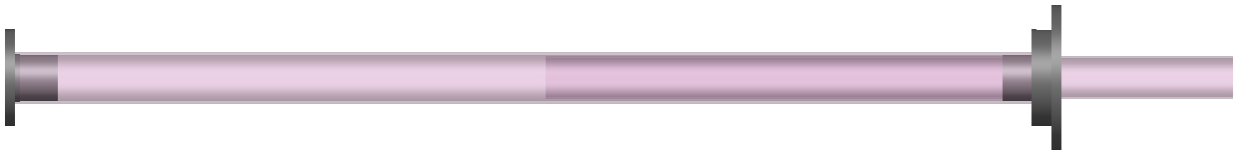


Figure 5: This is a model of the completed graphene-growth chamber with the quartz tube is shown in pink and the KFs shown in gray.

of 23.95 mm, just smaller than the 24-mm outer diameter of the outer quartz tube so that there would be just enough space to slide the quartz tube over each KF to create a tight Torr seal for the chamber. Furthermore, since the inner tube slid into the outer tube through the 50-KF, the inner diameter of the 50-KF was thinned so that it is just smaller than the outer diameter of the inner quartz tube. Both stainless steel KFs were cut very slowly with a lathe in the Physics machine shop and cleaned in JILA before being sealed to the outer quartz tube in the Dessau Lab.

4 Results

During the first KOH etch attempt, the timer on the outlet controlling the temperature of the KOH bath turned off. This meant that some unknown portion of the etch was completed at room temperature rather than at 70°C. Since the etch rate halves with every temperature drop and the durations of the etch completed at these temperatures was unknown, the thickness of the etched portion of the wafer was also unknown. As a result, the time needed to complete the etch was now unknown. When the KOH etch bath was turned back on, the sample was left in the KOH solution for too long and disintegrated so much that only its outer edge remained. To prevent this in the future, the thickness of the sample could have been measured, allowing for the calculation of a new etch time, before it was put back in the KOH solution.

For the second etch attempt, the solution bath was connected to an outlet without a timer to ensure that it remained hot for the duration of the etch. Throughout different steps of the process, images were taken from a microscope to show how different features looked after different steps in the etching process. Images of different portions of the pattern at different points in the can be found in Appendix B.

The upper right-hand corner of the upper right-hand screw hole shows off the isotropy in the BOE of SiO_2. This is most visible in Figures B.1b and B.1c, where there appears to be a double line outlining the screw hole. If the BOE had completely vertical sidewalls, as shown in Figures A.1e and A.1f and was assumed when designing the slit array, this double line effect would not have occurred. This makes sense since a BOE is non-directional [citation], and etches every direction of the SiO_2 layer at an equal rate. Such an isotropic etch makes transferring the straight lines on the Cr mask onto the Si(100) wafer impossible, and results in crooked lines in the KOH etch such as those in Figures B.2e and B.2f.

5 Further Work

5.1 Fixing Current Problems

There are two major problems that must be addressed before Pt can be deposited on the slit array: the rounded outer corners created by the KOH etch and the isotropic profile of the BOE. One way to prevent rounded corners in the final design is to grow Si_3N_4 on the Si(100) wafer rather than SiO2, as suggested by Ian Haygood, a technician at CNL. Si_3N_4 adheres better to Si(100) and is not etched as quickly as SiO_2 is by KOH. Improved coverage of the Si(100) mask during the KOH will prevent as severely rounded corners.

The simplest way to prevent isotropy during the BOE would be to use a different etch altogether. Reactive Ion Etching (RIE) results in a very straight vertical etch profile. [11] An RIE was not an option for the Si(100) because the RIE facilities at CNL

can only be used for shallow etches, but the SiO_2 etch is just the right thickness where an RIE should work very well. This will ensure that the Si3N4 mask will be as close as possible to the desired pattern of the slit array.

5.2 What's next?

After the fabrication of the Si(100) structure for the slit array is complete, Pt will be evaporated onto the substrate at the National Institute of Standards and Technology (NIST) to prepare it for graphene growth. Then the Pt graphene growth chamber will be installed in the Schibli Lab and graphene will be grown onto the Pt on the Si(100) wafer. Once the fabrication of the new slit array is complete, it will be installed in the Laser ARPES system in the Dessau Lab and used to examine samples. The same samples should be examined with both the new and old slit arrays to determine if the new design is in fact an improvement on the old.

6 Acknowledgments

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A Etching Process

(a) Both the front (top) and back (bottom) of the Si(100) wafer were coated with SiO_2 in the Tynal Oxidation Furnace at CNL.

(b) Positive PR, AZ 4210, was spun onto the back and then the front of the wafer on top of the thermally-grown layers of SiO_2.

(c) This shows the mask aligned over the PR in preparation for exposure.

(d) The exposed PR was removed during development and protected the mask during the BOE of SiO_2.

(e) The SiO_2 was etched where it was not protected by the PR.

(f) The BOE created the hard SiO_2 mask that protected the Si(100) during the KOH etch.

(g) Both the SiO_2 and Si(100) wafer were etched by the KOH solution.

(h) The final result of the process was the complete etch of the Si(100) wafer.

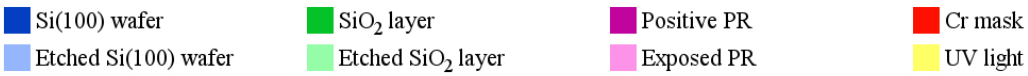
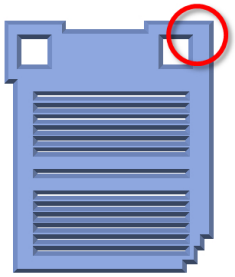


Figure A.1

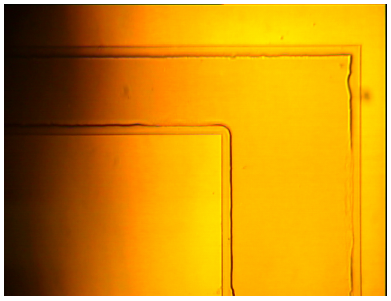
B Results

There are some features consistent in all of the locations examined at each time examined. One is the red color in all of the images of the sample after the BOE before the PR has been removed. This is because there is a red filter on the microscope that prevents any white light from the microscope from exposing the PR on the wafer. After this PR is cleaned off of the wafer, the samples are viewed under white light.

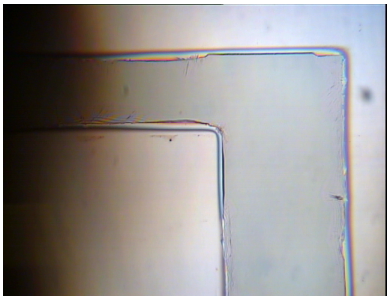
The rough surface of the KOH-etched samples is the part that was etched away. The smooth surfaces are the parts that are covered with SiO_2 and were not removed. These surfaces change color between 3, 8, and 10 hours of KOH etching. This is because the KOH also etches the SiO_2 layer (although much more slowly than it etches the Si(100) wafer) and SiO_2 changes color with thickness, as observed during CNL's nanofabrication course.



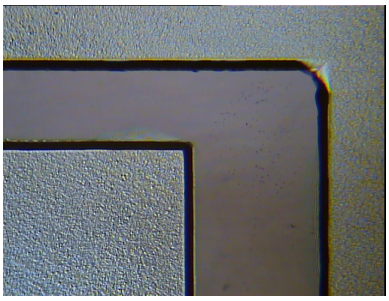
(a) This is the portion of the etch examined in the following images.



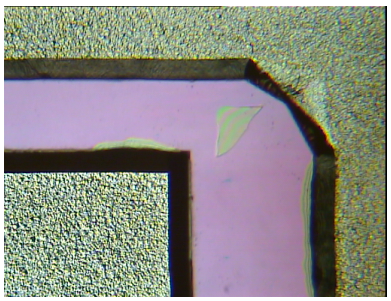
(b) This is the wafer after the BOE but before the PR was removed.



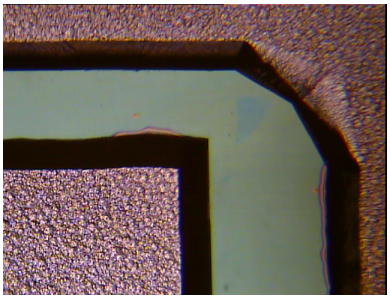
(c) This is the wafer after the BOE and after the PR was removed. It is now more obvious that the lines that should be straight are crooked after the BOE.



(d) After 3 hours in the KOH etch the outer corner is beginning to round but still has a definite square shape.

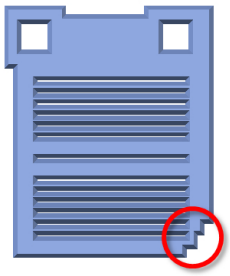


(e) After 8 hours in the KOH the outer corner is beginning to lose its square shape.

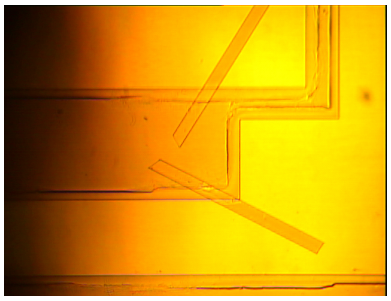


(f) After 10 hours in the KOH the outer corner is nearly completely rounded.

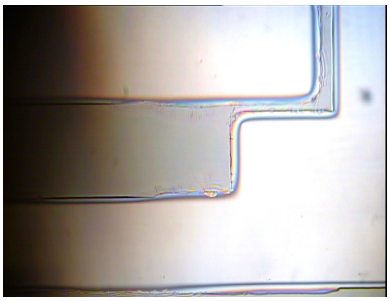
Figure B.1



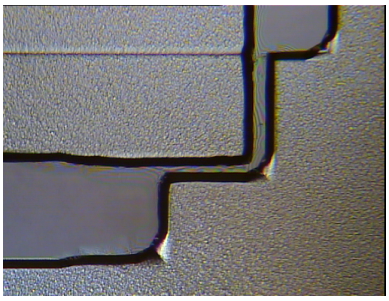
(a) This is the portion of the etch examined in the following images.



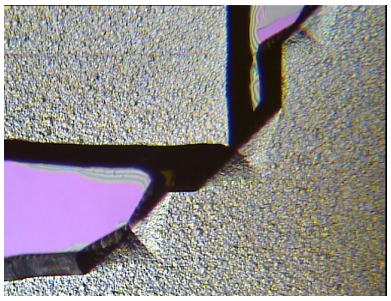
(b) This is the wafer after the BOE but before the PR was removed. Broken pieces of PR are stuck to the wafer in the wrong places.



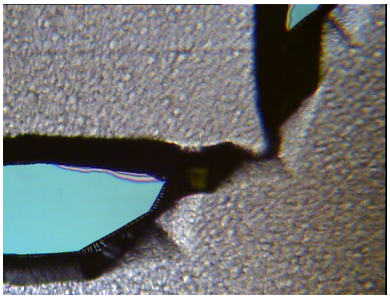
(c) This is the wafer after the BOE and after the PR was removed. The broken pieces of PR are now gone.



(d) After 3 hours in the KOH etch the outer corners are still recognizable.



(e) After 8 hours in the KOH etch the outer corners are more rounded than square.



(f) After 10 hours in the KOH etch the pixelated corner feature is almost combined with the slit region.

Figure B.2