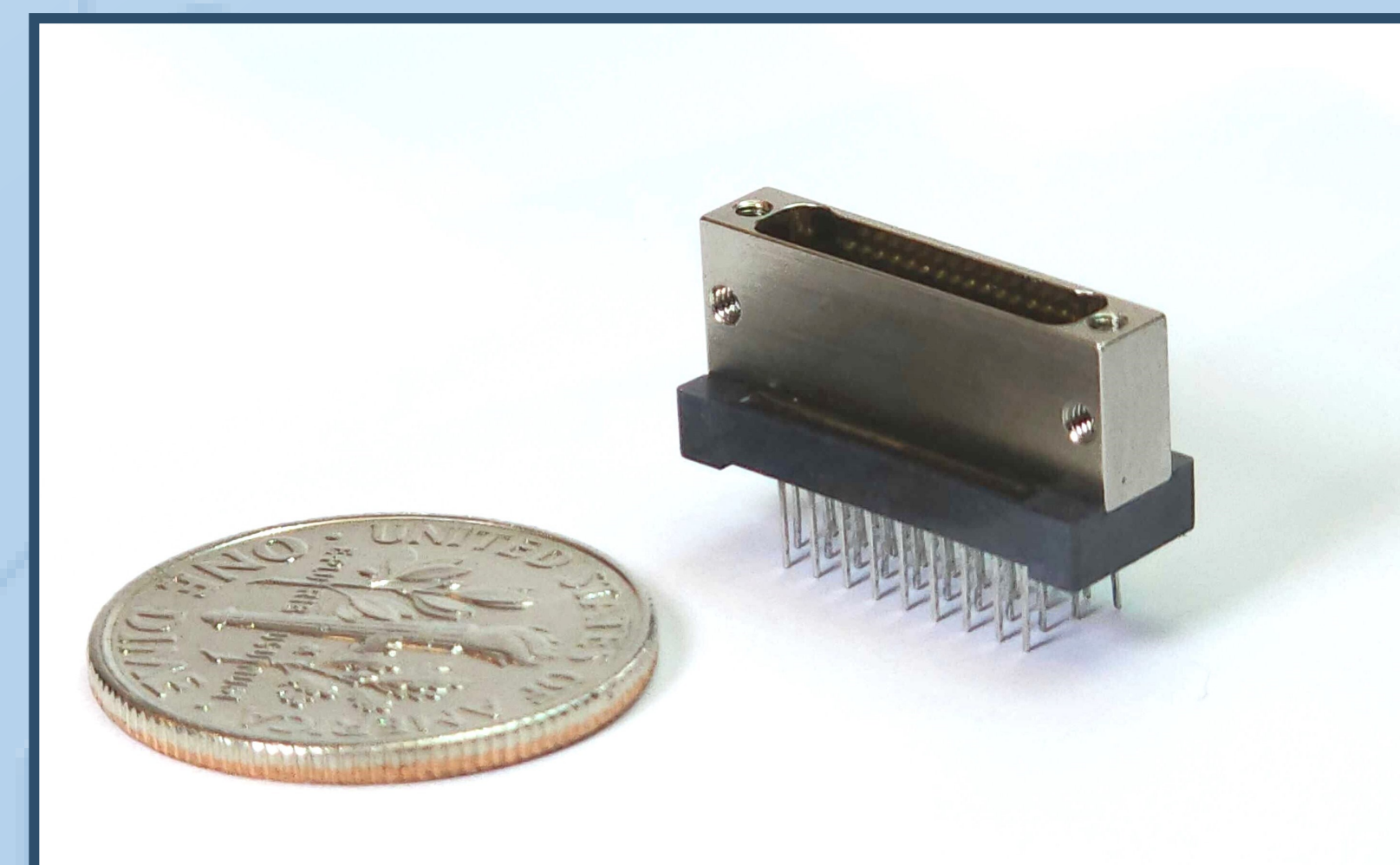


# NANONICS CONNECTOR REWORK

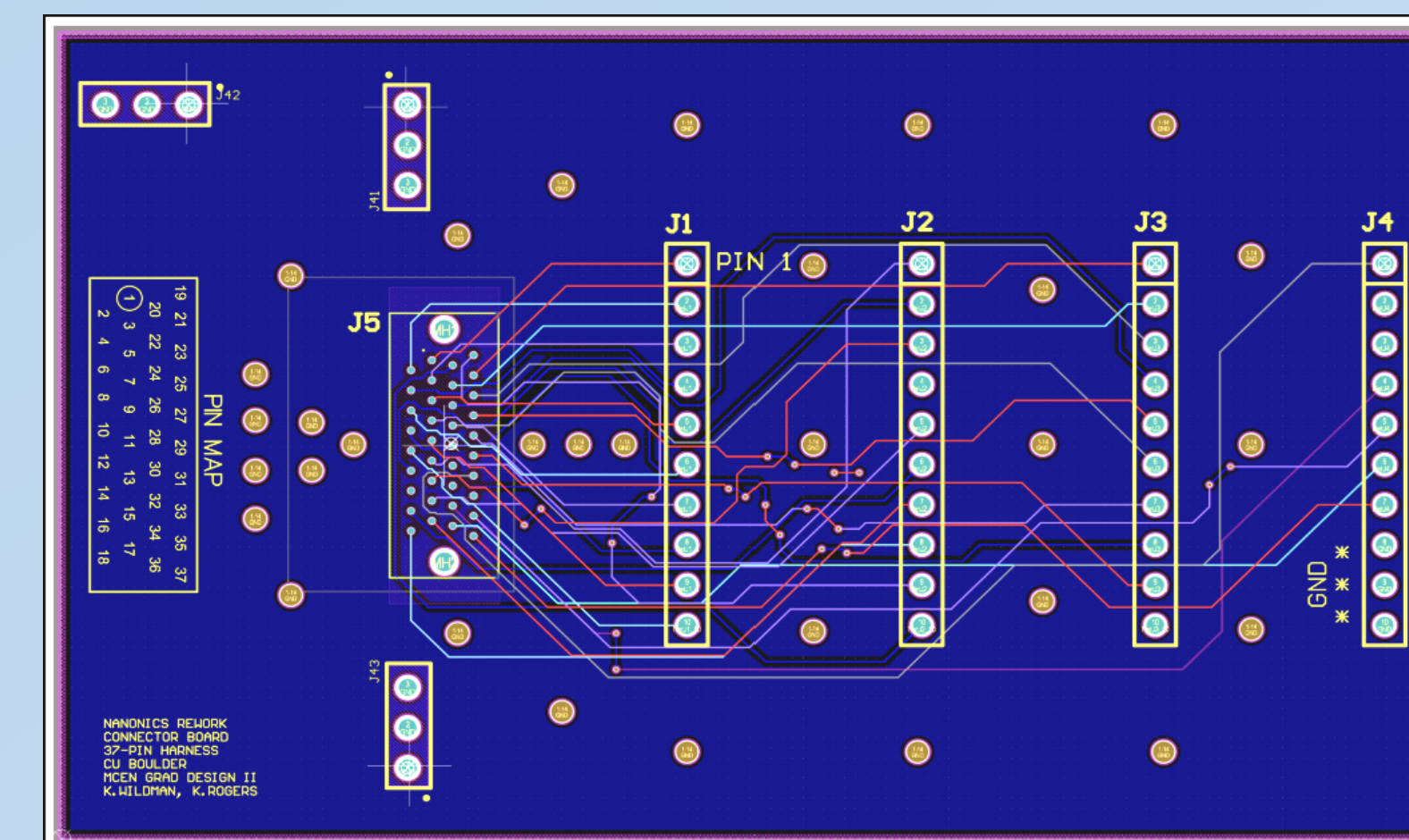
## DEVELOPMENT OF TECHNICIAN'S PROCEDURE TO PHYSICALLY REMOVE D-SUB TYPE CONNECTOR FROM AEROSPACE-GRADE PWBs FOR REUSE OF BOARD IN R&D PROJECTS

Advisors: James Harris, Joshua Crawford, Matthew Francisco, Becky Komarek, Greg Whiting

Kelli Wildman & Kyle Rogers



37-PIN NANONICS CONNECTOR WITH DIME FOR SCALE



CUSTOM PCB WITH 14 LAYERS TO TEST REWORK PROCESS

### INTRODUCTION & PROBLEM STATEMENT

Sandia National Labs specializes in scientific and engineering applications for promoting national security and advancing technology in space, defense, and other innovation areas. The "Nanonics" series of connectors used in these applications have high pin counts and are very delicate and utilized on complicated, densely-populated PWBAs ("Printed Wire Board Assembly", a.k.a. "PCBA" or "printed circuit board assembly").

### PROJECT MISSION

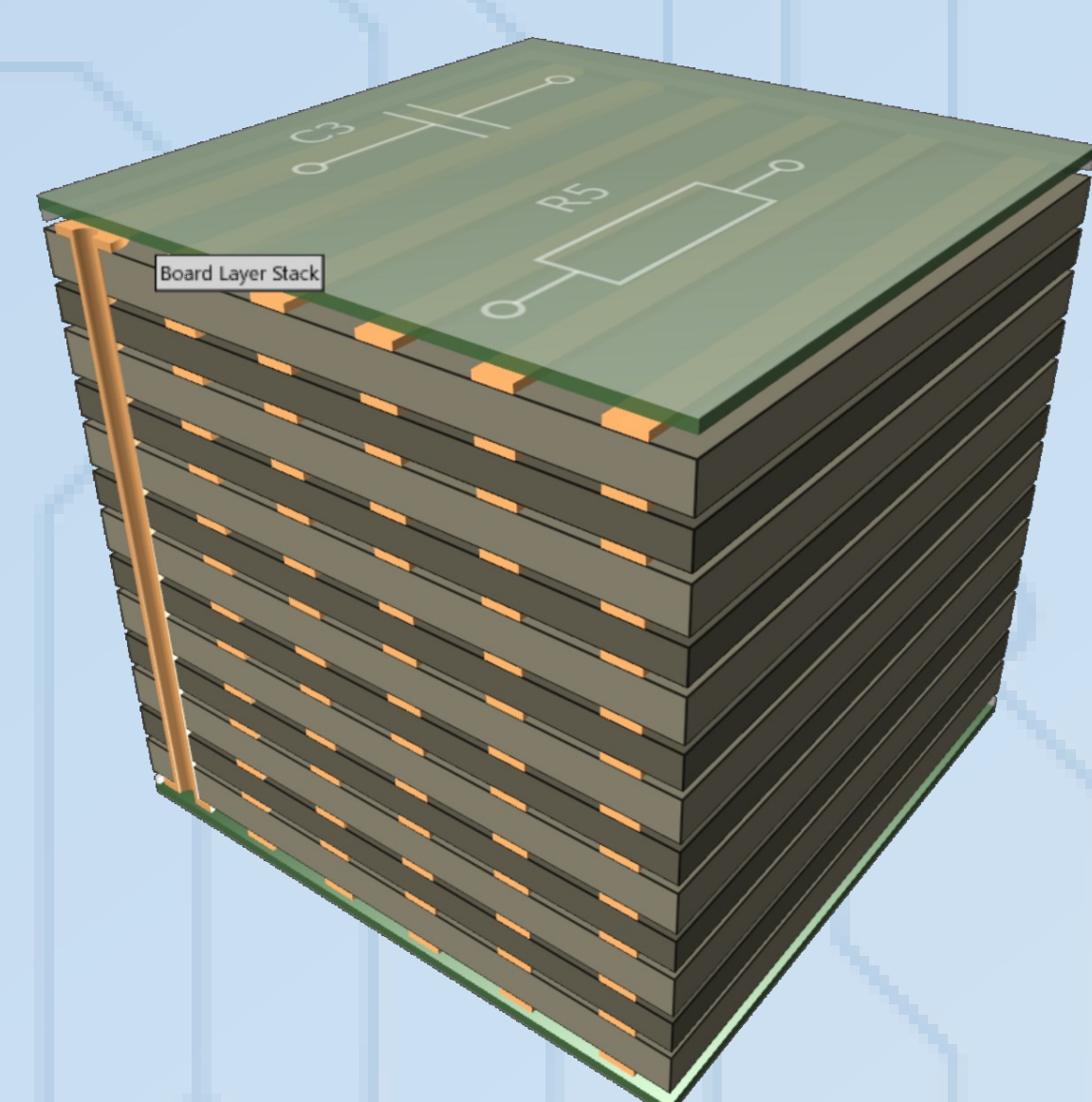
Remove a Nanonics-style connector with high pin count from a PCB with between 12-16 layers. Upon successful connector removal, the PCB can be reused with a new connector replacement. The rework must be done in a manner that meets aerospace-grade inspection that passes IPC Standards (Class III Specifications).

### DELIVERABLE(S)

Create a procedure document detailing the successful process for use by a lab technician

### PROJECT CHALLENGES

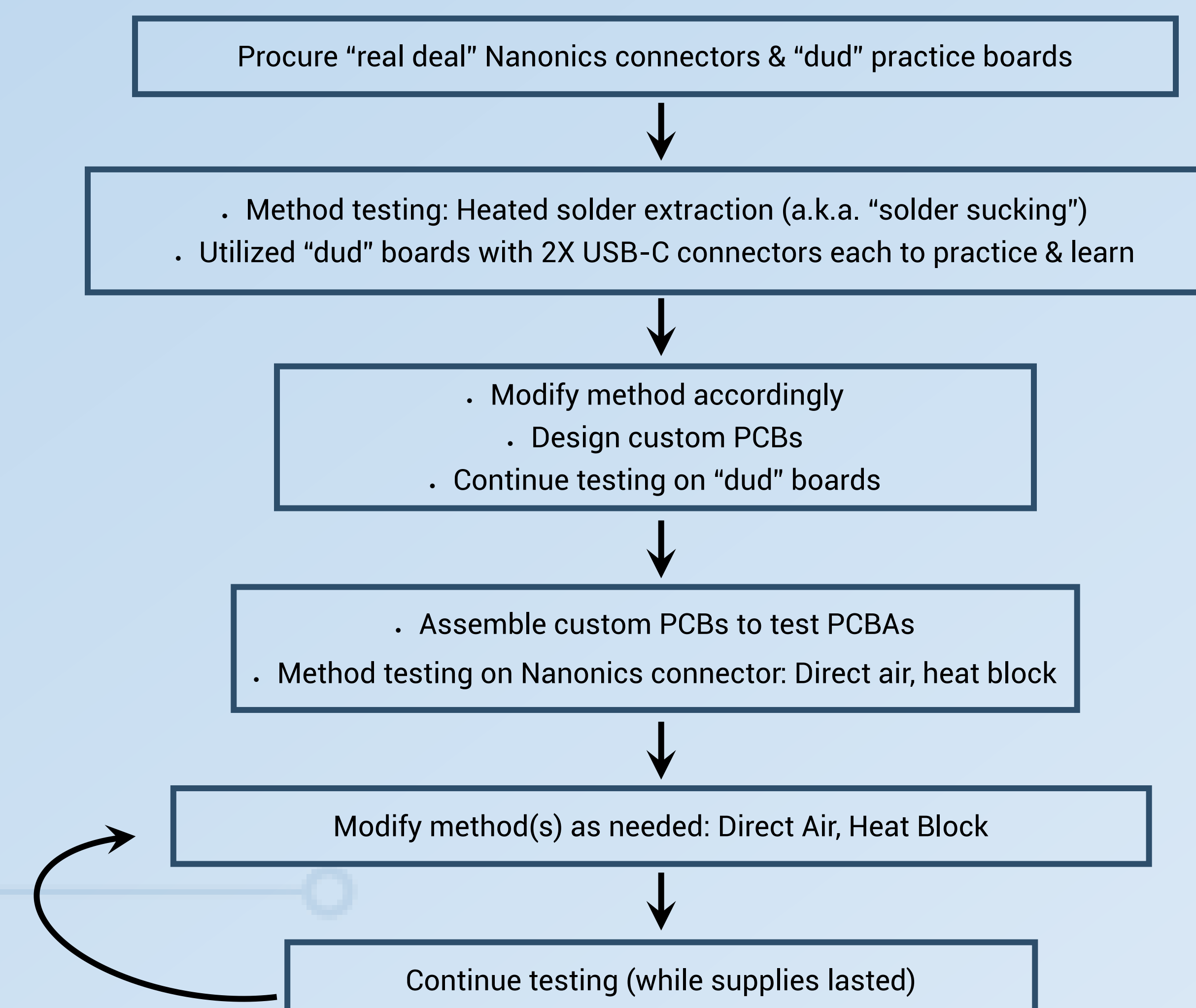
PCBAs are double-sided and densely populated by components. Layouts, photos, or sample declassified PCBAs could not be provided for reference for use.



ALTium DESIGNER  
LAYER STACK VISUALIZATION FOR A 14-LAYER PCB

- Connectors & PCBs typically have high expense costs to procure and long lead times.
- Specific materials required:
  - 63/37 leaded solder, no lead-free solder
  - "Kester 186" liquid flux
- Many Nanonics connectors are now obsolete
- Many layers per PCB = large internal copper planes. Large copper planes = significant heat sinks

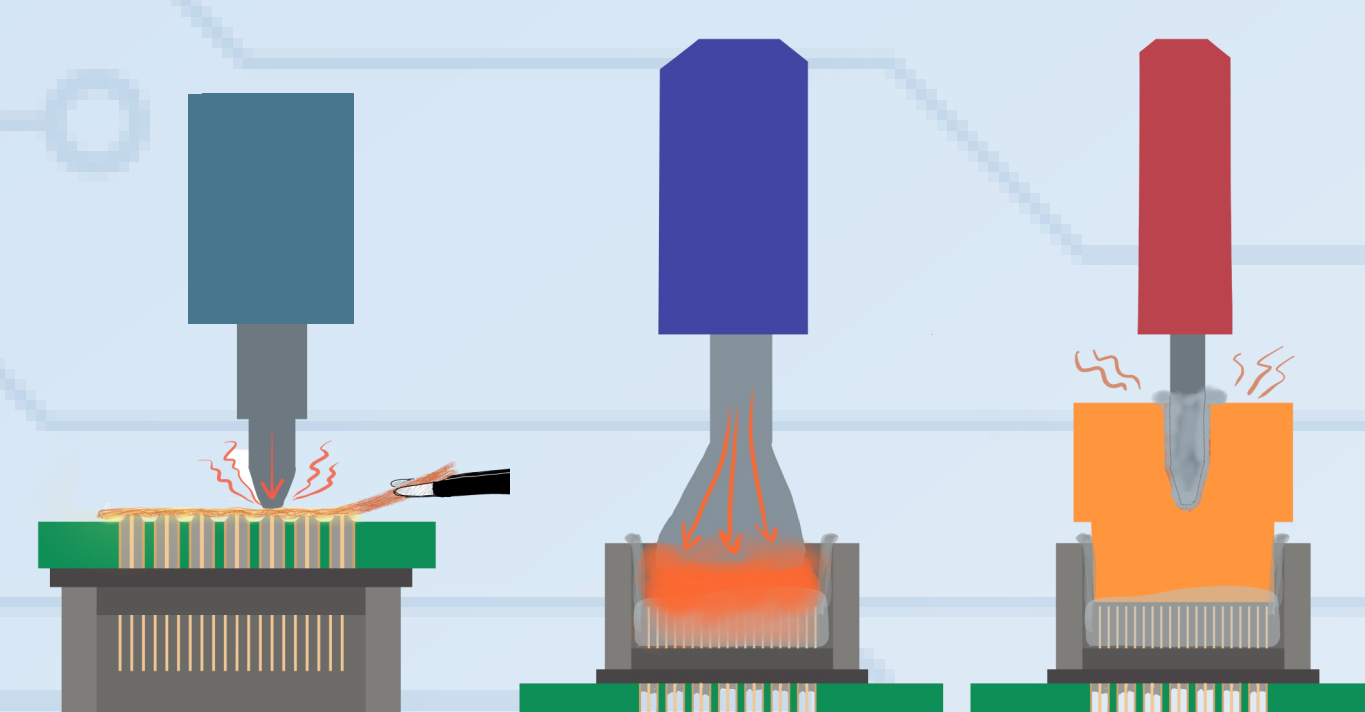
### PROTOTYPING PROCESS



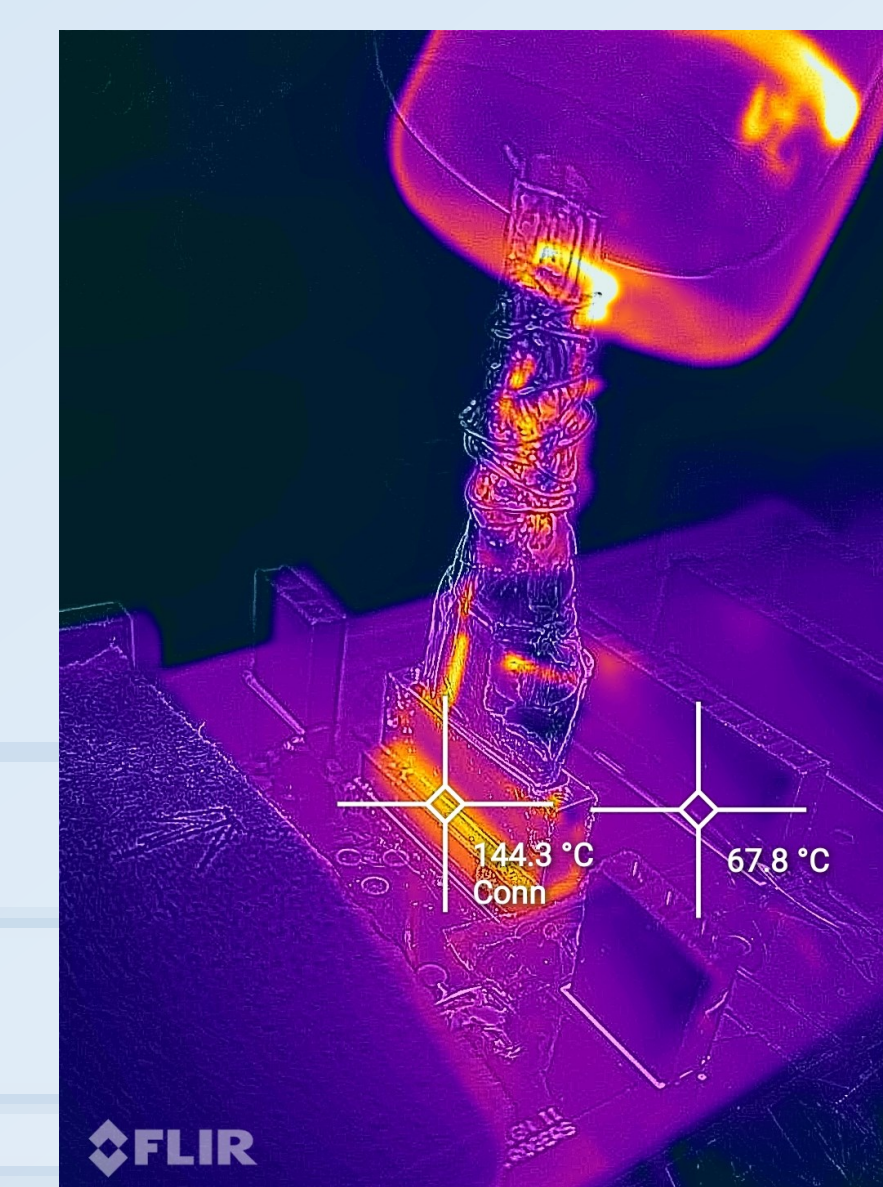
### METHODS TESTED

Methods included one or a combination of the following:

- Conduction via soldering iron through custom copper block
- Convection via soldering pins inside the connector
- "Solder sandwich" - solder wick with flux infused
- Heated solder sucker extraction
- Preheater plate (low temp)



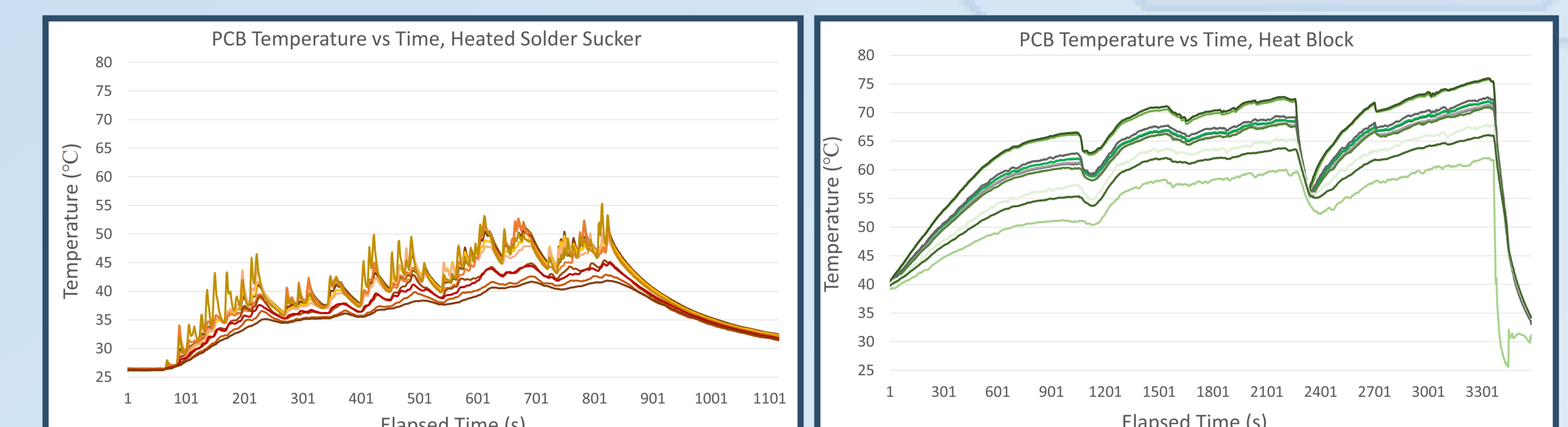
[LEFT]: PRIMARY METHODS TESTED: VACUUM, HOT AIR, & Cu BLOCK



[RIGHT]: THERMAL IMAGING OF DIRECT AIR METHOD

### THERMAL MONITORING

A key factor in procedure development was the goal to keep heat isolated at the connector itself and reduce heat creep into nearby components, due to lack of knowledge of Sandia's PCBA components and board layouts. Data collection & monitoring of internal PCB temperatures during the rework process was done with both K-Type thermocouples and FLIR thermal images, shown in graphs below:

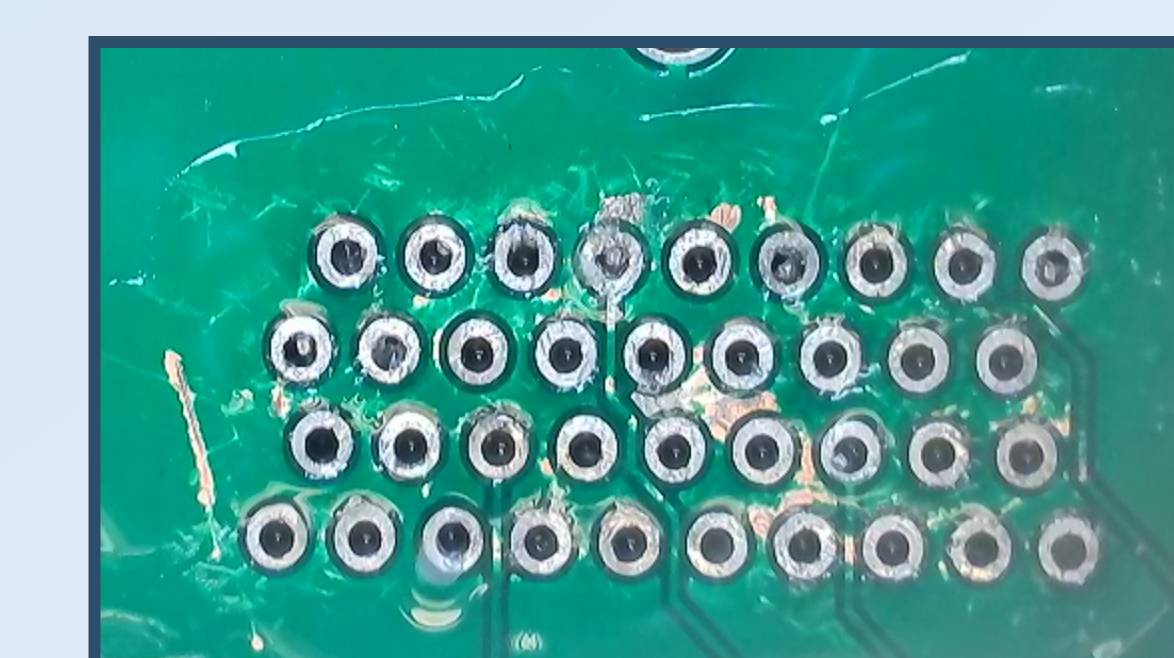


### FINDINGS

After testing an assortment of heat transfer methods, in general the successful criteria focused on removing a majority of the solder from pins and heating the contacts in the connector directly rather than the region it is mounted (as in a typical method for rework).

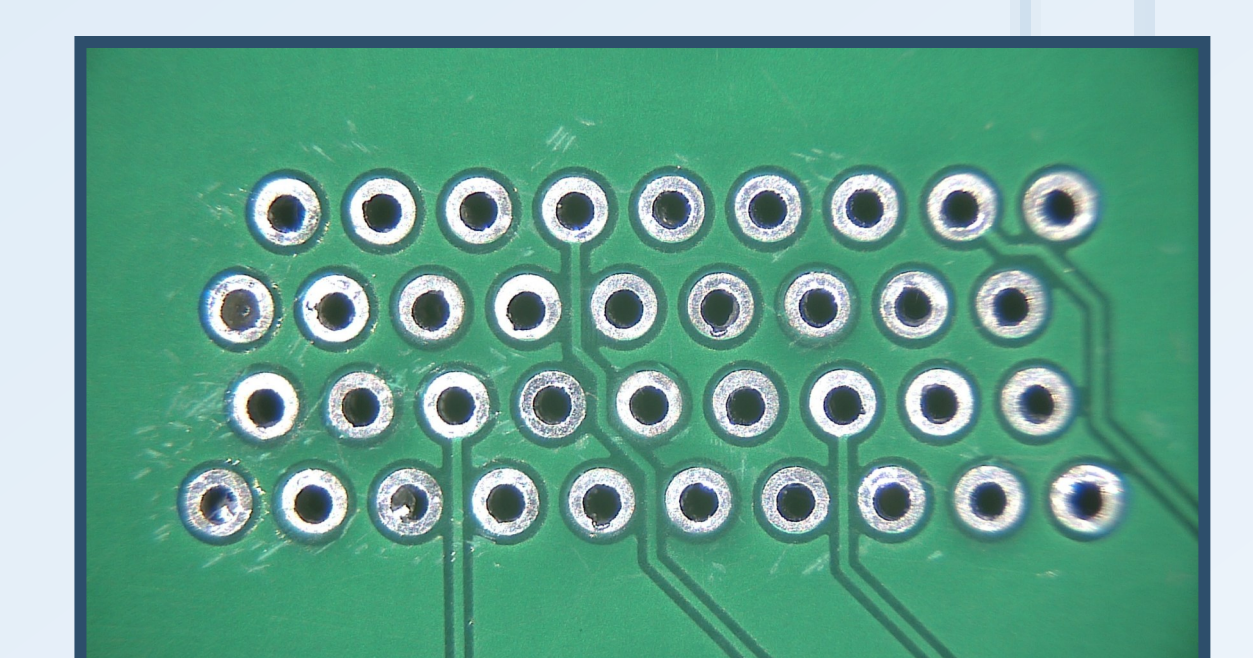
The method that appears to work the most successfully is a combination of vacuum extraction of solder around pins, preheating the board to below melting temperature of the solder, and conduction of heat into the connector via the copper block with assistance of a thermal compound or generous amounts of flux. With these methods combined, we were successful in removal of a Nanonics connector that passes IPC inspection specifications.

Fail ✗



FAILURE: SIGNIFICANT SCRATCHING OF SOLDER MASK, EXPOSED COPPER, DAMAGED SOLDER PADS

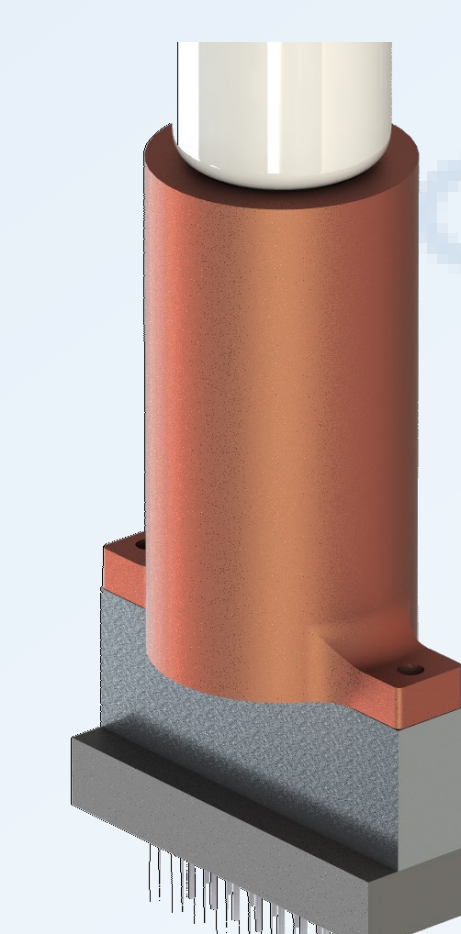
Pass ✓



PASS: SOLDER PADS UNDAMAGED, JUST NEEDS A BIT MORE CLEANUP. NO DEEP SCRATCHES IN SOLDER MASK, AND NO EXPOSED COPPER

### FUTURE STEPS

A final document will be provided to Sandia National Labs as a guide to create a finalized, formal rework procedure that will be used in the lab. A CAD model of a well-fitting copper soldering iron "adapter" block will be provided for future fabrication purposes.



Special Thanks:

The Last Gameboard  
CU Boulder ITLL Electronics Lab

National Institute of  
Standards and Technology (NIST)

Dr. Eric Bogatin (CU Boulder)

Our friends, families, and bosses for  
their incredible patience and support!



NIST