Fabio Somenzi

Curriculum Vitae

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Biography: Fabio Somenzi received the Dr. Eng. degree in Electronic Engineering from Politecnico di Torino, Italy, in 1980, filing a thesis on automatic test pattern generation for sequential circuits. He was with SGS-Thomson Microelectronics from 1982 to 1989 as responsible for computer-aided digital design.

From 1984 to 1987 he taught digital logic design at the Computer Science Department of the University of Milano, Italy. In 1987 he visited the Electrical Engineering and Computer Science Department of the University of California, Berkeley. Since 1989 he has been an with the Department of Electrical and Computer Engineering of the University of Colorado, Boulder, where he is currently a Full Professor.

Personal Data: born in Salerno, Italy, on September 17, 1957.
Italian Citizen. U.S. Permanent Resident.

Education: Dr. Eng. Degree in Electronic Engineering (summa cum laude) Politecnico di Torino, Italy, 1980.

Professional Experience:

2001–present: Professor, Department of Electrical and Computer Engineering University of Colorado.

1993–2001: Associate Professor, Department of Electrical and Computer Engineering University of Colorado.

1989–1993: Assistant Professor, Department of Electrical and Computer Engineering University of Colorado.

1987: Visiting Industrial Fellow, Electrical Engineering and Computer Science Department, University of California, Berkeley.

1984–1987: Adjunct Professor, Computer Science Department, Università di Milano, Italy.

1982–1989: SGS-Thomson Microelectronics, Agrate Brianza (MI), Italy. Responsible for computer aids for digital design.

1981: Served in Italian Army.

Awards:

- D'Ovidio Award as outstanding graduate of Politecnico di Torino for the academic year 1979–1980.
- Best Paper Award. Design Automation Conference, June 2000.

Professional Activities:

- Associate Editor for IEEE Transactions on Computer-Aided Design (1994–1998).
- Coordinating editor for Journal of Formal Methods in System Design (2005–present).
- Reviewer for:
  - IEEE Transactions on Computer-Aided Design;
  - IEEE Transaction of Computers;
  - Journal of Formal Methods in System Design;
  - Linear Algebra and its Applications;
  - Journal of Parallel and Distributed Computing;
  - Journal of Electronic Testing Theory and Applications;
  - IEEE Design and Test;
  - IEEE Design Automation Conference;
  - IFIP VLSI Conference;
  - European Test Conference.
- Member of the Program Committee of:
  - International Conference on Computer Aided Verification (1994, 1995, 1998–2004, 2006, 2007, 2008, 2009 (Co-chair 2003)).
  - IEEE International Conference on Computer Aided Design (1989, 1992–1995, 1998, 2001–2002, 2006, 2008).
  - ACM/IEEE Design Automation Conference (1995–1997, 2007, 2008).
  - IEEE European Conference on Design Automation (1990, 1992–1994, 2001, 2003).
  - IEEE International Conference on Computer Design (1992, 1993, 1994, 1999, 2000).
  - Formal Methods in Computer-Aided Design (2006).
  - IEEE European Design for Testability Workshop (1987).
  - MCNC International Workshop on Logic Synthesis (1989–2001 (Program Chair 1995, Executive Committee 1998, General Chair 1999)).
  - IFIP International Workshop on Logic and Architecture Synthesis (1990).
  - International Symposium on Low Power Electronics and Design (1996, 2000).

– International Conference on Application of Concurrency to System Design (1998).
– Computer Aided Design and Test Decision Diagrams - Concepts and Applications (1999, 2001).
– International SPIN Workshop on Model Checking of Software (2001).
– IEEE Asia-Pacific Design Automation Conference (2003).
– International Workshop on Bounded Model Checking (2004, 2005).
– IBM Verification Conference (2006).
– Workshop on Verification and Debugging (2006, co-organizer).

Ph.D. Thesis Advisor:

- H. Cho, "Reachability Analyses and Their Applications in Test Generation and Logic Optimization for Sequential Circuits," 1993.
- J.-K. Rho, "Finite State Models for the Optimization and Verification of Digital Systems," 1993.
- R. I. Bahar, "Methods for Timing Analysis and Logic Synthesis to Decrease Power Dissipation of VLSI Circuits," 1995.
- W. Lee, "Approximate Model Checking," 1998.
- K. Ravi, "Adaptive Techniques to Improve State Space Search in Formal Verification," 1999.
- M. Escobar, "Efficient Solution of Satisfiability Problems in CAD Applications," 1999.
- B. Kumthekar, "Layout Conscious Logic Optimization Techniques for Power and Delay Reduction in FPGAs," 2000.
- I.-H. Moon, "Efficient Reachability Algorithms in Symbolic Model Checking," 2000.
- R. P. Bloem, "Search Techniques and Automata for Symbolic Model Checking," 2001.
- HoonSang Jin "Efficient Algorithms for Finding All Satisfying Assignments of a Propositional Formula," 2005.
- Mohammad Awedh, "Proving properties for Bounded Model Checking" 2006.
- Bing Li, "Satisfiability-based Abstraction Refinement in Symbolic Model Checking," 2006.
- David Ward, "Exploiting High-Level Design Control and Data Structures for Hardware Verification," 2007.
- Kuntal Nanshi, "Proving Properties of Digital Systems with Abstraction-Guided Simulation," 2009.

M.S. Student Advisor:

- Sankaranarayanan Gurumurthy
- Huthasana Kalyanam
- David Morgan
- Saloni Shah
- Tara Weber

Current Ph.D. Student Advisor:

- Hyojung Han
- Hyondeuk Kim
- Elias Shihadeh
- Saqib Sohail

Research Interests. Fabio Somenzi has published two books and over 180 papers on the verification, synthesis, optimization, simulation, and testing of digital systems.

References

[1] S. Sohail and F. Somenzi. A two-stage algorithm for LTL games. In *Ninth International Conference on Formal Methods in Computer-Aided Design (FMCAD 2009)*, pages 77–84, Austin, TX, November 2009.

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[3] H. Kim and F. Somenzi. Efficient term-ITE conversion for satisfiability modulo theories. In *Twelfth International Conference on Theory and Applications of Satisfiability Testing (SAT 2009)*, pages 195–208, Swansea, UK, June 2009. Springer-Verlag. LNCS 5584.

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[7] S. Sohail, F. Somenzi, and K. Ravi. A hybrid algorithm for LTL games. In *Verification, Model Checking and Abstract Interpretation*, pages 309–323, San Francisco, CA, January 2008. LNCS 4905.

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