QUASI-OPTICAL CLASS-E POWER AMPLIFIERS

by

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Quasi-Optical Class-E Power Amplifiers

Thesis directed by Professor Zoya Popović

ABSTRACT

The class-E amplifier has a maximum theoretical efficiency of 100 %, compared to, for example, ideal class-A (50 %) and class-B (78 %) amplifiers. Invented in 1975 by Alan Sokal [1], the class-E amplifier has been used at MHz frequencies using lumped elements to enforce class-E operation, achieving efficiencies approaching 100 % [1]. Meanwhile, at microwave and mm-wave frequencies (0.3-300 GHz), traditional power amplifiers provide moderate output power levels at relatively low operating efficiencies (20-50 %), generating heat and lowering battery life in mobile equipment. Class-C and Class-F amplifiers achieve higher efficiencies than class A or class B, but the class-E amplifier promises *maximum* efficiency performance. In this thesis, the class-E switched-mode circuit conditions are satisfied using distributed transmission lines, and high efficiency operation is experimentally achieved at microwave frequencies. For example, using the Siemens CLY5 MESFET at 0.5 GHz, 83 % drain efficiency (η_d), 80 % power-added efficiency (PAE), and 0.55 W output power (P_{out}) are measured, and using the Fujitsu FLK052WG MESFET at 5 GHz, $\eta_d = 81\,\%$, PAE=72 %, and $P_{out} = 0.61$ W are measured.

Free-space quasi-optical power-combining techniques offer a practical method for combining the output power of a large number of devices. In this thesis the quasi-optical power-combining concept is successfully applied to the transmission-line class-E amplifier. Measurements show 2.4 W of total output power at 5.05 GHz, with a DC-to-RF conversion efficiency of 74 % and a power-added efficiency of 64 % for a four-element power-combined class-E amplifier using Fujitsu FLK052WG MESFETs. It is believed that this is the highest reported frequency of switched-mode class-E operation, the first class-E amplifier using transmission lines instead of lumped elements, and the highest efficiency free-space power amplifier structure to date.

DEDICATION

To My Family, Friends and Electric Guitar

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CHAPTER 1

INTRODUCTION AND BACKGROUND

1.1 Introduction

The millimeter-wave region corresponds to frequencies between 30 GHz and 300 GHz. This frequency range has a wide variety of applications in communication, radar, radiometry, remote sensing, radio astronomy, plasma diagnostics, and spectroscopy [2]–[5]. Due to the shorter wavelengths, millimeter-wave systems are generally more compact than their microwave counterparts. They also provide broader bandwidths for communication systems and higher resolution for radar and imaging systems. In addition, the atmospheric attenuation at these frequencies is significantly lower than that of infrared and optical wavelengths, which is important for many of the applications listed above [2]. Millimeter waves travel through clouds, fog, dust, and smoke, which allows for radar systems that work well even under these adverse conditions. In contrast, microwave systems lack the required resolution and optical systems suffer from severe attenuation and scattering.

Presently, tube sources such as klystrons or travelling-wave tubes are necessary to generate high power levels at millimeter-wave frequencies [6]–[8]. However, these sources are expensive, have limited lifetimes, and require large, high-voltage DC power supplies. On the other hand, solid-state devices are relatively inexpensive, have longer lifetimes, and only require smaller, low-voltage power supplies [9],[10]. Furthermore, as will be explored in this thesis, solid-state devices are capable of generating moderate power levels with high efficiency, which both maximizes output power for a given power supply, and also minimizes heat sinking requirements in a system. It would be advantageous to use solid-state devices to attain medium and high power levels at both microwave and millimeter-wave frequencies, while maintaining high-efficiency operation.

Since the output power of a single solid-state device is significantly lower than that of a tube source, and falls off approximately as the square of frequency [11], the output generated by a large number of such devices must be combined to generate high power at millimeter-wave frequencies. A review of microwave and millimeter-wave power-combining techniques may be found in [12],[13]. Both the complexity of coherently combining the power of hundreds of devices and the associated losses prohibit the use of conventional passive circuit combiners. Waveguide power combiners have also been studied [14], but at higher frequencies, the machining tolerances and the losses due to the waveguide walls become prohibitive as well. These obstacles have motivated most of the recent research work in free-space power-combining techniques. The basic idea behind this area of research is to coherently combine the output power of a large number, perhaps hundreds or even thousands, of solid-state devices in free space. Since the medium in which the power is combined is free space, which is lossless and dispersion-free, these methods are similar to optical techniques. However, since the wavelength is comparable to the size of the structures at microwave and millimeter-wave frequencies, diffraction plays an important role. Therefore, the approaches used in free-space power-combining are referred to as "quasi-optical" techniques. Several excellent review articles discuss the variety of quasi-optical power-combining techniques studied to date [15],[16]. A special issue of the IEEE Transactions on Microwave Theory and Techniques has been dedicated to this subject [17]. A significant amount of information on the background of quasi optics was also presented by Bundy [18], some of which is repeated here for completeness.

1.2 Background

Quasi-optical power-combining techniques can essentially be categorized into three distinct areas: (1) wave-beam resonators, (2) active antenna arrays, and (3) active grids. Fig. 1.1 illustrates the basic differences between these three classes. In wave-beam resonators, Fig. 1.1 (a), the output power of several independently-biased and tuned oscillators is combined in a free-space Fabry-Perot resonant cavity. This type

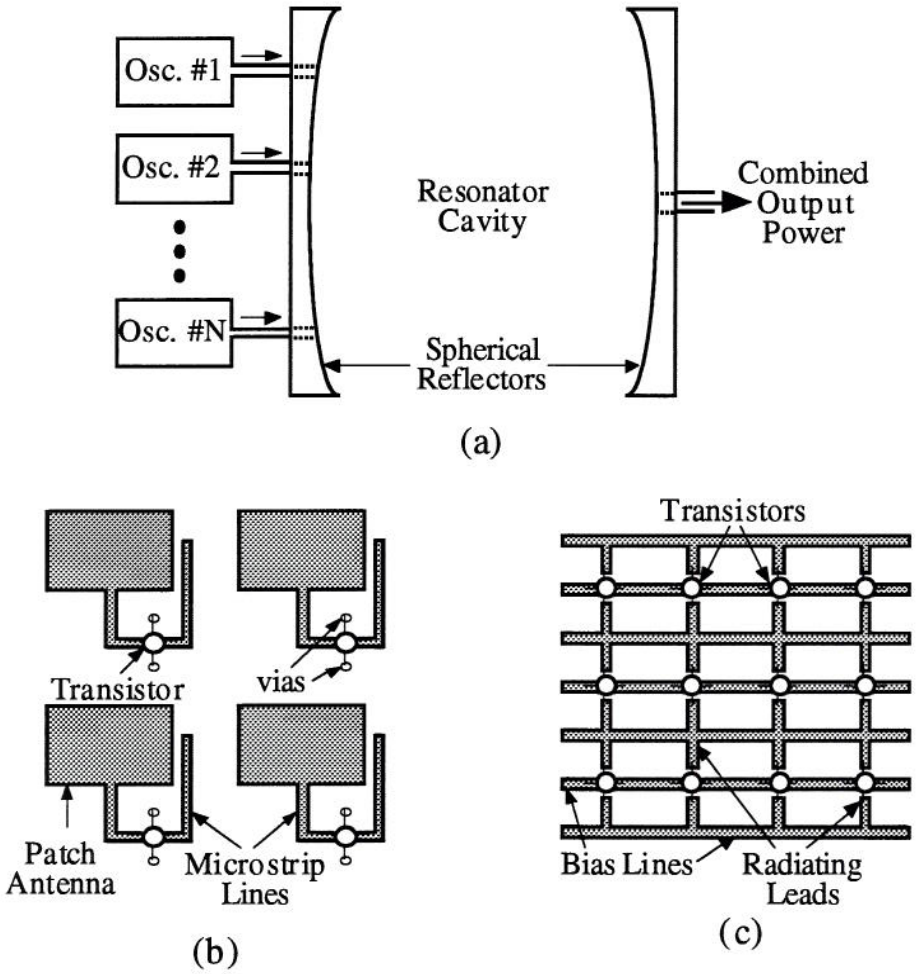


Figure 1.1. The classification of quasi-optical power-combining techniques. (a) In wave-beam resonators, the power from a number of individual oscillator elements is combined in a confocal resonator cavity, where the fields have a Gaussian distribution. (b) In active antenna arrays, a conventional array of antenna elements, each driven by an active device, radiates power into free space. (c) In active grids, a printed grating with a period much smaller than a free-space wavelength is loaded with active devices, and therefore the grid acts more as a distributed impedance surface than an array of individual elements.

of resonator was first demonstrated by Wandinger and Nalbandian in [19]. A slightly different configuration was studied by Mink [20]. This 1986 paper is credited with generating the significant amount of research interest in quasi-optical power combining seen today. Additional work in oscillators utilizing open-cavity resonators may be found in [21]–[25]. An active antenna array consists of a standard antenna array in which the individual elements are driven by active devices, Fig. 1.1 (b). A number of both amplifier [26]–[37] and oscillator [38]–[50] arrays have been demonstrated, using a variety of different antennas and devices. In these active antennas, the inter-element spacing is on the order of a half-wavelength. An active grid, on the other hand, consists of a periodic metal pattern loaded with active devices, where the spacing between individual elements is a smaller fraction of a free-space wavelength, Fig. 1.1 (c). A number of both grid oscillators [51]–[57] and grid amplifiers [58]–[60] have been demonstrated. In all three of these power-combining techniques, a wide variety of solid-state devices can be used, including two-terminal devices such as Gunn, IMPATT, or tunnelling diodes, and three-terminal devices, such as metal semiconductor field effect transistors (MESFETs), high electron mobility transistors (HEMTs), or heterojunction bipolar transistors (HBTs).

The first grid oscillator was demonstrated at Caltech by Popović, Kim, and Rutledge in 1988 [61]. This structure consists of a 5×5 array of GaAs MESFETs loading a periodic metal pattern printed on a grounded dielectric substrate, as shown in Fig. 1.2. The gate and drain terminals of the device are connected to radiating leads, and the sources are connected through the substrate to the back-side metallization using vias. A coherent oscillation frequency of 9.7 GHz with a few hundred mW of power was observed when this grid was biased.

A second scheme was developed in which all of the device terminals are coplanar, eliminating the need for vias [62]. In this structure, a series of parallel, horizontal metal bars are periodically loaded with MESFETs, as shown in Fig. 1.3. The gate and drain leads of the devices are connected to the vertical radiating elements between the bars, and the source leads are soldered directly onto the bars. These parallel plates reinforce

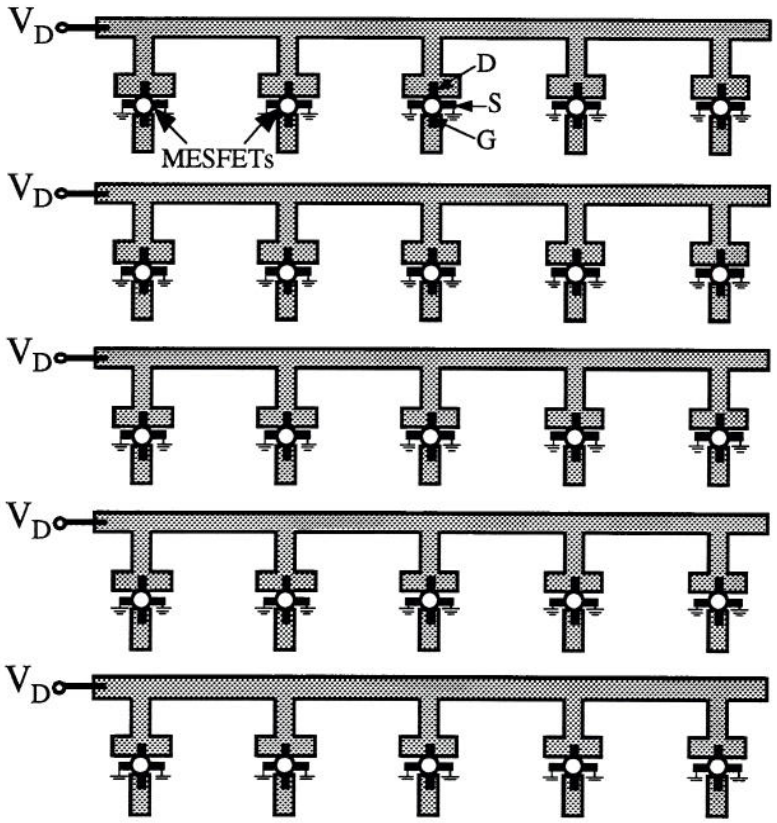


Figure 1.2. The first grid oscillator, in which a 5×5 array of MESFETs load a periodic structure [61]. The gate and drain terminals are connected to the vertical leads and the source is connected to the ground plane on the back side of the substrate through vias. The horizontal line provides the drain bias and the gates are self-biased.

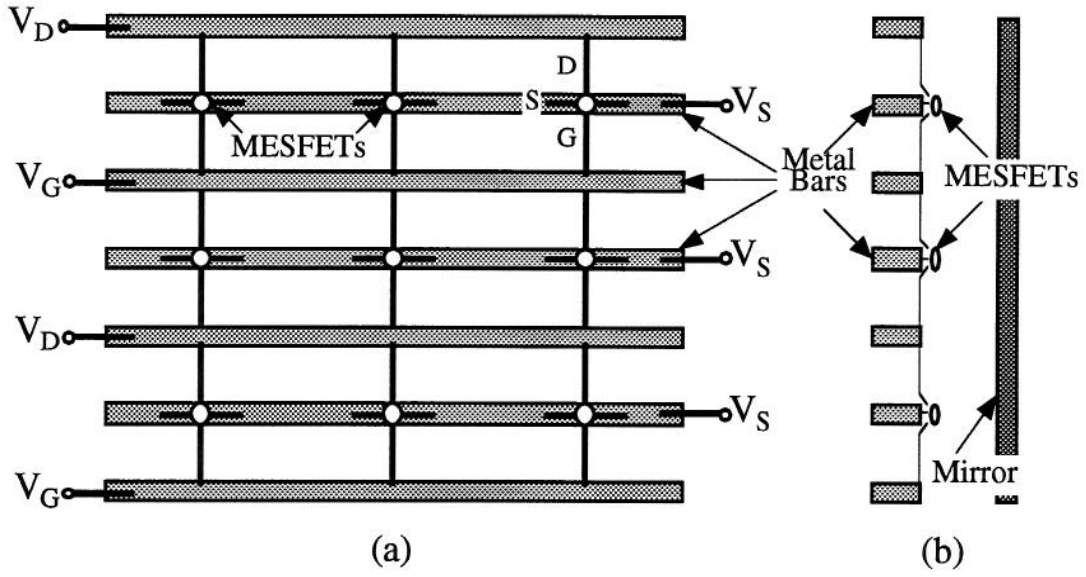


Figure 1.3. The (a) front view and (b) side view of the bar-grid oscillator presented in [62]. The MESFETs are soldered directly onto horizontal metal bars, which provide both bias and heat-sinking for the devices.

the desired TEM boundary conditions, and simultaneously provide the bias and the heat sink for the devices. This bar-grid oscillator operated at 3.0 GHz.

Since the primary goal is to develop a high-power source at millimeter-wave frequencies using solid-state devices, a design compatible with monolithic fabrication techniques is desired. This led to the planar grid oscillator shown in Fig. 1.4, where the metal bars of the bar-grid oscillator are replaced by printed strips on a dielectric substrate, and all of the device terminals are on the same planar surface [51]. In this case, the drains and gates are connected to the vertical radiating leads and the sources are connected directly to the horizontal bias lines. A 10×10 array was fabricated and an oscillation frequency of 5.0 GHz was observed. A number of other grid oscillators similar in nature have been studied as well [52]–[57], achieving up to 10 W of output power [57].

The key element in a typical planar grid oscillator is a periodic metal pattern loaded with an array of solid-state devices, such as the one shown in Fig. 1.4. When the devices are biased, the electrical noise generates a small signal, which builds up into an oscillation. Under the proper bias conditions and with the feedback provided through

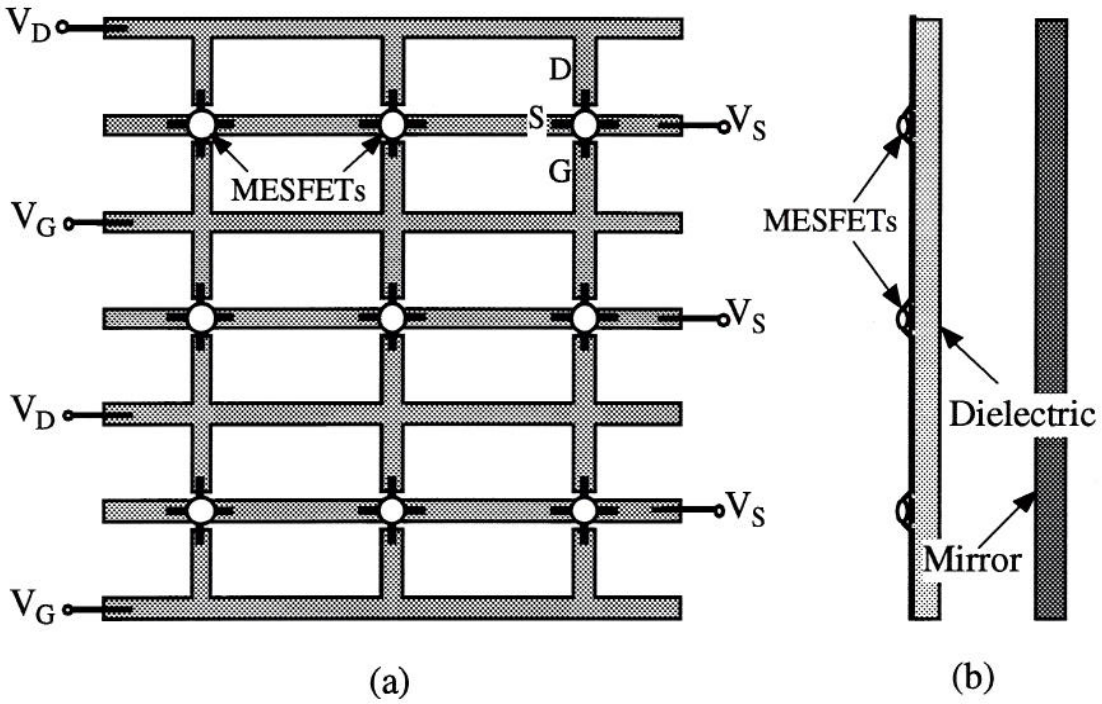


Figure 1.4. The (a) front view and (b) side view of a typical planar grid oscillator, consisting of a printed periodic metal pattern loaded with solid-state devices. Under the proper conditions, the devices lock together and oscillate in phase, radiating power in the broadside direction. The mirror provides unidirectional output power and may also be used to mechanically tune the frequency of oscillation.

the dielectric and the mirror, the devices lock together and oscillate in phase, radiating power in the broadside direction.

Numerous approaches have been taken to analyze periodic quasi-optical structures such as grid oscillators, many of which are outlined in Scott Bundy's Ph.D. thesis [18]. In his thesis, Bundy uses the Moment Method to numerically determine the impedances seen by an active device embedded within a grid oscillator. These impedances are then used to find the oscillation frequency of a grid oscillator design. Bundy and Shiroma also developed a method of analyzing a complete quasi-optical system [63]. Both of these methods have demonstrated their usefulness experimentally, and are currently in use and under further development at the University of Colorado at Boulder.

A significant amount of work has also been done on more conventional oscillator arrays [38]–[47]. These structures consist of an array of oscillator elements, each connected to their own antenna. Different coupling and feedback mechanisms are used, ranging from situations in which tight coupling is provided through transmission-line circuitry [64],[65], to cases where the weaker free-space coupling is the predominant mechanism [66],[67]. This work has been studied at several universities, and many interesting aspects of these arrays have been researched, such as injection locking [68]–[70] and beamsteering [71]–[74].

Numerous methods have been applied to quasi-optical amplifiers, both for low-noise receiving and for high power generation. The more classical approach involves a conventional array of active amplifiers, each with their own separate receiving and transmitting elements, forming a free-space amplifier [26]–[37] . In this case, lens focussing techniques can be employed to increase the efficiency of the amplifier and overcome the losses due to diffraction, as demonstrated in [75]–[76]. A second approach utilizing the active grid philosophy has also shown success [58]–[60]. The grid amplifier in [59] has a planar structure somewhat similar to the grid oscillator geometry shown in Fig. 1.4, but with the single MESFET transistors replaced by HBT differential amplifier pairs.

In this thesis, the classical array approach is taken to demonstrate high efficiency

quasi-optical power amplification. Efficiency is important in quasi-optical amplifiers and oscillators because heat must flow laterally across these two-dimensional structures, and must be extracted at their perimeter, since a quasi-optical beam must flow through the surface. The difficulties posed by excess heat production in a quasi-optical power amplifier are seen in Hubert et al [34], and problems arising from excess heat generation in a power oscillator are seen in [57]. Hubert's experiences demonstrate that minimizing the generation of excess heat is clearly desirable. Since each amplifier cell is on the order of a substrate wavelength in transverse dimension, enough real estate is available for harmonic waveshaping circuitry necessary for high-efficiency power amplification. Stabilization is difficult in quasi-optical power amplifiers, both because radiating structures have highly reactive impedances off of their design frequencies, and also because input and output antennas often couple to one another parasitically. For these reasons, stable amplification is difficult to achieve without degrading the gain and power conversion efficiency of the amplifier. Grid amplifiers, where each unit cell is a small fraction of a wavelength in transverse dimension, offer the possibility of very high power densities, but matching and stabilization circuitry must be kept physically small, and therefore tradeoffs must be made to fit each amplifying element into a unit cell. Also, in the array approach used in this work, a single unit cell can be prototyped to demonstrate the feasibility of a particular topology; in the grid approach, an entire array must be populated and powered up to test a new topology. Furthermore, each separate piece of a quasi-optical array amplifier can be designed and tested separately; in Chapter 6, for example, a 5 GHz class-E microstrip amplifier is designed and tested in a 50-Ω coaxial environment. Then a 50-Ω antenna and a bias network are also separately designed and tested. When these pieces are put together to form the quasi-optical class-E power amplifier, it works without any further adjustment. A lower-frequency oscillation occurs (at 1.5 GHz), but this is suppressed using resistors and capacitors. The electrical location and values for these lumped elements is determined from known impedances in the circuit, and does not degrade the efficiency or gain of the amplifier at 5 GHz.

Besides oscillators and amplifiers, other quasi-optical components have been

demonstrated as well. Several grid mixers have been fabricated [77]–[81]. The grid mixer presented in [80] consists of a planar array of Schottky diodes. When two different plane waves are incident on the grid (an RF and an LO signal), the mixer diodes generate a signal at the difference frequency, and this low-frequency IF signal is seen across the entire mixer grid. Phase-shifter grids have been studied in [82]–[84]. In [83], an array of Schottky diodes is used to change the phase of the surface's reflection coefficient by varying the DC bias on the devices. Two of these phase-shifter grids were also used for beamsteering [82],[84]. Multiplier grids have been demonstrated as well [85]–[88]. In this case, the diode array generates a plane wave at a harmonic frequency of the incident plane wave. Grid switches have also been presented [89]–[91]. In [91], the forward bias on an array of *pin* diodes is used to vary the reflectance and transmittance of this variable impedance surface. With such a wide variety of quasi-optical components present in the literature, the demonstration of a full system based on a number of quasi-optical arrays should be possible in the near future.

Since quasi-optical power amplification is in an early stage of development, and since quasi optics is a method of combining already existing devices and circuits, a review of recent results in single-device amplification is appropriate. Recent developments in device technology have resulted in the following single-transistor performances: 72 % power-added efficiency (PAE) with 1 W of output power at 12 GHz [92], 47 % PAE with 0.5 W of output power at 20 GHz [93], 29 % PAE with 1 W of output power at 40 GHz [94], 24 % PAE with 0.27 W of output power at 60 GHz [95], and 33 % PAE with 0.06 W of output power at 94 GHz [96]. Furthermore, device technology is improving at a rapid pace, and it is expected to continue to do so. It is not the intent of this thesis to compete with single-transistor amplifier results; the point is to *build upon these results.* The promise of quasi-optical power combining is to preserve the gain and efficiency of single transistor amplifiers, but to achieve power levels many times as large.

Numerous classes of amplification have evolved during the past several decades for both low-frequency and radio-frequency operation, including class A, B, C, D, E, F, G, H, and S, among others. In [97], Raab gives an excellent review of the classes of

amplification, and compares the relative strengths and weaknesses of each class. Useful analysis and design methods for microwave class-A and class-B power amplifiers are derived in [98]. Each class of operation presents a set of tradeoffs between efficiency, bandwidth, output power, and gain to the circuit designer. For example, an experimental study of class-C vs. class-B operation is presented in [99].

Load lines for the most common classes of amplification are superimposed on a MESFET's I_{ds}-V_{ds} curves in Fig. 1.5. Class A and class B operate mostly in the active region of a transistor, which results in maximum gain and linearity at the expense of efficiency. Classes D, E, and F operate in the switched-mode region of the transistor's I_{ds}-V_{ds} curves, close to the $V_{ds} = 0$ and $I_{ds} = 0$ axes (where the device dissipation $V_{ds}I_{ds}$ is minimized). This results in maximum efficiency operation, at the expense of gain and linearity. Class C operates somewhere in between the two extremes, resulting in a tradeoff between efficiency, linearity, and output power. All of the classes shown in Fig. 1.5 are suitable for microwave operation, except for class D because of the phenomenon of switching loss, where the stored capacitive energy in the transistor is dissipated during each switching cycle. Microwave class-E and class-F amplifiers minimize switching loss by using reactive tuning at harmonic frequencies to recover the energy stored in the device's parasitic reactances during each switching cycle.

The idea of harmonic tuning of RF power amplifiers has been around since at least 1958 [100], and some work was done in 1967 as well [101]. In both of these works, a short circuit is presented to the output of the transistor (or vacuum tube) at even harmonics, and an open circuit is presented at all of the odd harmonic frequencies. This results in a square-wave voltage waveform, and a raised half-rectified sinusoidal current waveform. In the ideal case, the product of the voltage and current waveforms is zero at all times, which results in 100 % efficiency operation because no power is dissipated in the active device. In [97], Raab coins the term "class F" to denote this type of harmonically-tuned amplifier operation. During the 1980s this class of amplifier was rediscovered, and numerous researchers have successfully applied the class F concept to microwave solid-state power amplifiers [102]–[115]. Of particular interest are [113] and [114], in which

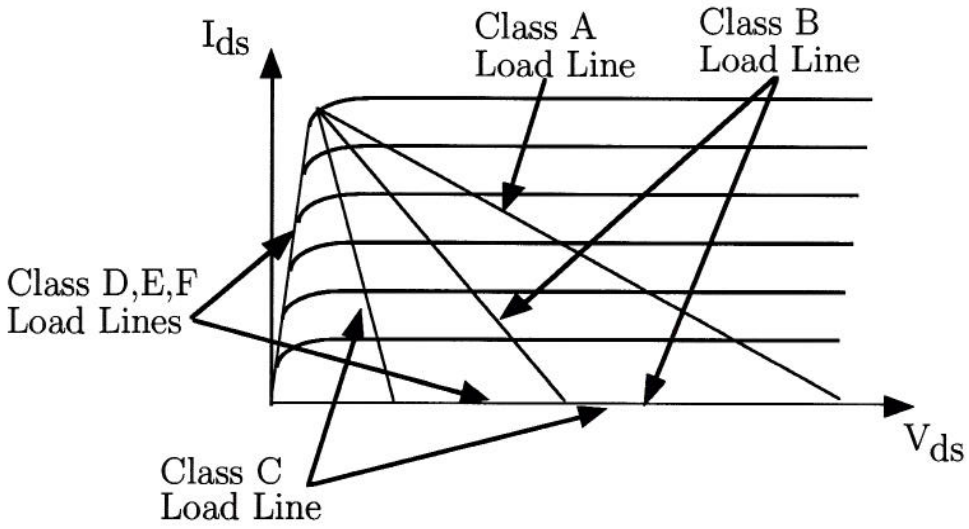


Figure 1.5. Load lines for the most common classes of power amplification, superimposed on the I_{ds}-V_{ds} curves for a MESFET. The more linear classes of operation (A,B) operate largely in the active region of the transistor, while the more efficient classes of operation (D,E,F) operate in the switched-mode region. Class C falls somewhere in between the two extremes.

second-harmonic *source* (input) matching is shown to result in higher efficiency class-F operation. Also, in [115], a two-transistor amplifier is presented in which each transistor injects the other with additional second harmonic current, resulting in an increase of efficiency over the conventional class-F amplifier. Recently a class-F *oscillator* was presented [116], in which feedback was added to a class-F amplifier.

The class-E amplifier, invented in 1975 by the Sokals [1], is particularly interesting for high frequency, high-efficiency power generation, and this class of operation is investigated in this thesis. Class-E amplifier operation is well known at MHz frequencies using lumped elements (capacitors, inductors), but no examples of microwave class-E operation have been found in the literature to date. In particular, the transmission-line class-E amplifier is believed to be newly presented in this thesis. Some interesting related work is the class-E multiplier [117],[118], and the class-E rectifier [119]. The high frequency active-antenna rectifier is of interest because it makes microwave *power transmission* possible. An example of a so-called "rectenna" is presented in [120]. The class-E amplifier exhibits similarities in operation to the class-F amplifier, and often

these two classes of operation overlap (an amplifier can exhibit aspects of both class-E and F operation). The dual of the original class-E circuit is presented in [121]; however, this circuit is more applicable to low-frequency, high-current applications than to microwave ones.

Numerous authors have analyzed various aspects of low-frequency (MHz) class-E operation. Of particular use is an early paper by Raab [122], in which he first makes the assumption of sinusoidal current flow in the output of the class-E circuit. This approximation is used in the derivations of this thesis (in Chapter 4) as well. However, the design equations derived in Chapter 4 are more concise than those presented by Raab and others. Also, the series-L/shunt-C and the series/shunt transmission-line topologies have not been found in the literature to date, and design equations are presented for those topologies (which are of particular interest for microwave operation). The simple expression for DC-RF conversion efficiency derived in Chapter 4 has not been seen elsewhere. Also, closed-form analytical solution of the class-E circuit with nonlinear output capacitance has not been seen in the literature. Finally, although the original class-E amplifier topology has been solved exactly, it has never before been solved directly and analytically in the time domain, as it is in Appendix A. In [123], Laplace transform techniques are used to solve the class-E circuit exactly, while in [124], numerical techniques are used.

Envelope restoration is a method by which heavily saturated amplifiers (such as the class-E amplifer) can be amplitude-modulated with a high degree of linearity. Envelope restoration applied to the class-E circuit is found in [125]. It is believed that this principle can be applied to microwave class-E amplifiers as well. Another concept of importance is the Doherty amplifier, which has been in use for decades in vacuum-tube transmitters. Using the Doherty amplifier technique, high efficiency can be maintained over a large dynamic range, and therefore it is also useful for linear amplitude modulation. The Doherty amplifier technique has recently been applied to MESFETs [126]. Also of interest is the Cascode amplifier configuration, which is presented in [127], for example.

1.3 Organization of the Thesis

This thesis discusses quasi-optical VCOs and power amplifiers, and in particular introduces the microwave class-E amplifier concept, and integrates the class-E concept into a quasi-optical structure. Some of the motivation for using free-space power-combining techniques, as well as previous work in quasi optics and high efficiency power amplification were given earlier in this chapter.

Chapter 2 describes a quasi-optical voltage-controlled oscillator (VCO), where a surface loaded with varactor diodes was used to tune the frequency of a grid oscillator loaded with MESFETs. The quasi-optical VCO was the first demonstration of a quasi-optical component consisting of more than one planar surface. This early work motivated the search for high power, high efficiency quasi-optical methods for generating power at millimeter wavelengths. Since a power amplifier is a fundamental building block for oscillator design, as well as a necessary system component, high-efficiency power amplification is pursued next.

In Chapter 3, a quasi-optical class-A power amplifier is presented. The amplifier is saturated in a free-space environment, and 24 elements are power-combined in free space. The structure is shown to be electrically robust and flexible. For example, the input wave can be linearly polarized, with a circularly-polarized output wave. However, the power-added efficiency of this amplifier is only 20 %, so a method for higher-efficiency power amplification is investigated.

In Chapter 4, the class-E high-efficiency amplifier concept is introduced, applied to microwave and millimeter wave frequencies. Analysis is performed on the class-E circuit, with an eye to high-frequency effects such as transistor capacitive nonlinearities and transmission-line effects.

Experimental verification of the transmission-line class-E amplifier is given in Chapter 5. The Siemens CLY5 MESFET is used in a microstrip circuit environment to demonstrate the class-E concept at microwave frequencies, and to show that the analysis presented in Chapter 4 is valid.

In Chapter 6, the concepts of quasi-optical power combining and the transmission-line class-E circuit are combined into a quasi-optical class-E power amplifier. High power and high efficiency are demonstrated in a quasi-optical amplifier structure.

Finally, Chapter 7 gives a summary of the thesis with concluding remarks and suggestions for future work. Since quasi-optical power-combining and transmission-line class-E amplifiers are new areas of research, there is a wide variety of possible topics for further study.

CHAPTER 2

THE QUASI-OPTICAL VCO

2.1 Introduction

In this chapter, quasi-optical grid voltage controlled oscillators (VCOs) are presented. These VCOs are the first demonstration of a quasi-optical system consisting of several periodic arrays loaded with solid-state devices. A quasi-optical VCO consists of an array of oscillators, a variable capacitance array, and a mirror. The mirror provides feedback for locked power combining of a large number of MESFET oscillators that load a two-dimensional metal grid on a dielectric substrate. The frequency can be electrically tuned either with gate bias or with another array loaded with varactor diodes. When the varactor bias voltage is changed, the capacitance of the diodes changes, which in turn modulates the frequency of the output power-combined wave. Two types of arrays are presented, one consisting of short dipoles, and the other of bow-tie elements. As expected, the bow-tie VCO has better performance than the dipole VCO, due to its broadband impedance. A 10 % tuning bandwidth with less than 2 dB power change was measured in the case of a bow-tie VCO. The results in this chapter were first presented in [128].

2.2 Dipole and Bow-tie MESFET VCOs

The quasi-optical voltage-controlled oscillator shown in Fig. 2.1 consists of a transistor oscillator grid and a varactor diode tuning grid. The oscillator grid is an array of transistors (Fujitsu FSC11 GaAs MESFETs) arranged on a metallic grid structure, such as the one shown in Fig. 2.2(a), etched on a 0.5 mm thick Roger's Duroid substrate with $\epsilon_r = 2.2$. Each MESFET is connected to a radiating element on the grid, and the spacing between the transistors is a fraction of a free-space wavelength. For the oscillators presented in this paper, the period is 15 mm and they consist of 7 by 7 arrays

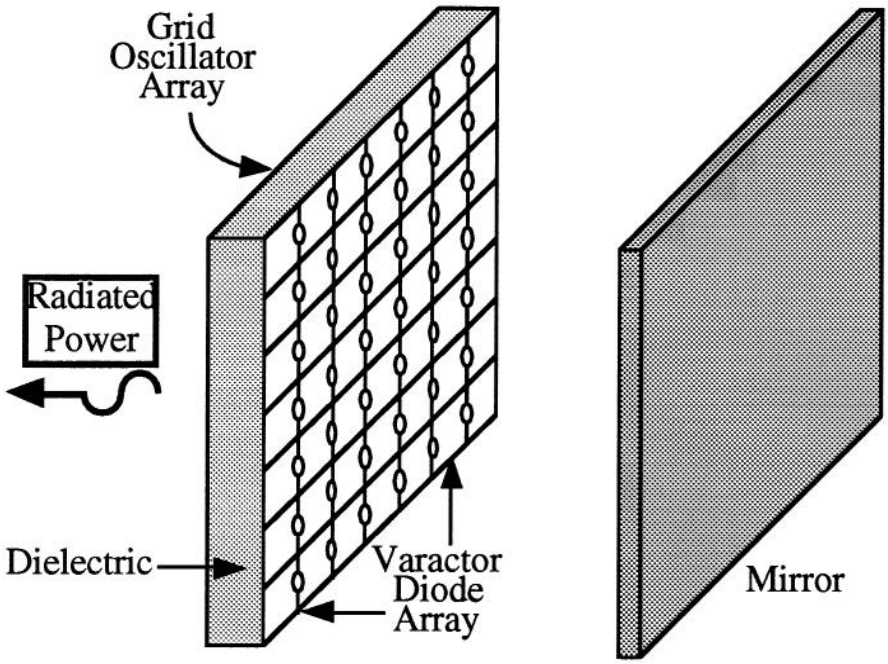


Figure 2.1. A quasi-optical voltage controlled oscillator system. A grid loaded with oscillating transistors is backed with a grid loaded with varactor diodes. When the capacitance of the diodes is bias tuned, the frequency of the locked oscillation changes. The mirror helps the self-injection locking of the individual oscillators.

of devices. All of the MESFETs in the grid are biased in parallel.

Previous work has shown that the frequency of such an oscillator may be changed mechanically by adjusting the position of the mirror [51], [62], [53]. However, mechanical tuning is impractical. It is more advantageous to be able to adjust the frequency electrically, particularly for modulation purposes. Electrical frequency tuning can be done by modulating the DC bias of the MESFETs. Another way to tune the oscillation frequency is shown in Fig. 2.1. A metallic grid structure similar to the transistor grid is loaded with reverse-biased varactor diodes. We used Metelics MSV34 varactors that have a specified ratio of $C_{max}/C_{min} = 4$. Low frequency measurements of the diode capacitance gave capacitances between 1.7 pF (at 0V) and 0.7 pF (at 30V). This diode grid is placed between the oscillator grid and the mirror. The diode reactance changes as the DC bias is adjusted and hence the transistors see a different equivalent impedance. This does not directly affect the bias point of the MESFETs. Electrical frequency tuning using both gate bias and varactor bias will be discussed in this paper.

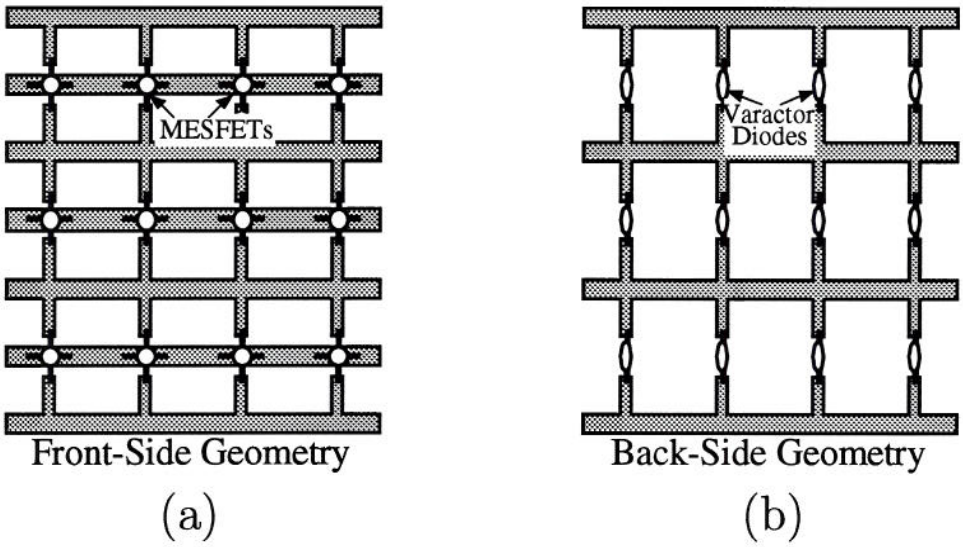


Figure 2.2. The dipole (a) MESFET and (b) diode grid structures. The vertical leads radiate, and the horizontal leads are the bias lines.

The oscillation frequency and output power depend on transistor and diode characteristics, grid structure, thickness and permittivity of the dielectric spacers, and mirror position. To a large extent, the metal grid geometry determines the frequency of

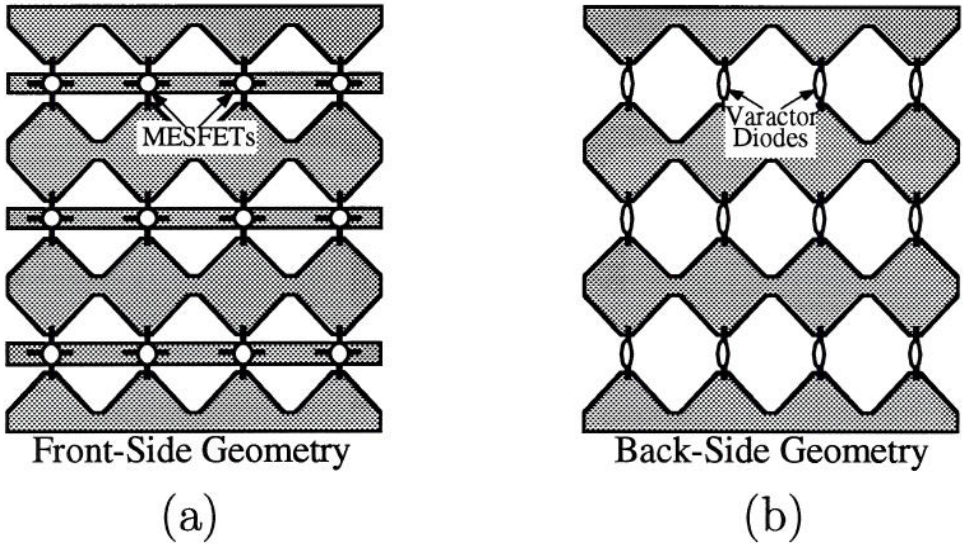


Figure 2.3. The bow-tie (a) MESFET and (b) diode grid structures. The horizontal leads on the MESFET grid are source bias lines.

oscillation. One type of grid structure is an array of short dipoles connected to the gate and drain leads of the transistors, as shown in Fig. 2.2(a). The driving point impedance of a dipole has a strong frequency dependence. A broadband radiating structure may prove to increase the tuning range. The bow-tie grid in Fig. 2.3(a) has broadband properties [129],[130], and was built for comparison with the dipole grid. The structure is self-complementary if the array is infinite. This can be seen by first looking at a single feed point assuming there are no generators connected to the other feed points. For this case, the structure is clearly self-complementary and the bandwidth is infinite for an infinite structure [131],[132]. By applying superposition, this conclusion extends to the impedances seen by all generators connected to the array feed points. In the transistor grid in Fig. 2.3(a), the source bias lines and the dielectric substrate perturb the self-complementarity.

The transistor dipole grid was designed using the theory outlined in [51] for the available MESFETs and dielectric substrate. In an infinite grid with all the devices locked in phase, symmetry allows us to represent the grid as an equivalent waveguide unit cell with magnetic walls on the sides and electric walls on the top and bottom. The propagating mode is TEM, and the evanescent modes present reactances at the device

terminals. Those reactances are found by the EMF method [133]. The embedding circuit for a device in the grid consists of lead inductances in the gate and the drain, a complex impedance in the source, a 377Ω transmission line representing free space, and a short representing the mirror. The entire grid is in this way reduced to a two-port equivalent. The measured small-signal transistor s-parameters were used, and the saturation taken into account by reducing $|s_{21}|$ by 2 dB [134]. The reflection coefficient looking into the oscillator from the 377Ω load is then examined as a function of frequency. When the amplitude of this reflection coefficient is greater than unity and the phase crosses zero, the oscillation frequency is found. For the dipole grid presented in this work, on a 0.5-mm thick dielectric with $\epsilon_r = 2.2$, an oscillation frequency around 3 GHz was found for a grid period of 15 mm and grid leads 1 mm wide. The exact frequency depends on the mirror position and bias. The varactor grid was designed to have the same metal geometry, so that when the two grids are aligned, the unit cell boundary conditions are preserved. The bow-tie grids were made to have the same period as the dipole grids.

Experiments were carried out for mirror tuning, bias tuning, and varactor diode tuning. The varactor diode grid shown in Fig. 2.1 was only present during the diode tuning measurements and was absent in the case of mirror tuning and bias tuning. In all of the results presented below, the frequency tuning range was limited by either the transistors unlocking, the oscillation ceasing altogether, or the limited capacitance range of the varactors.

2.2.1 Mirror and Bias Tuning

For comparison purposes, mechanical tuning using the mirror was performed for each of the oscillator grids. In both cases, less than $\Delta f = 10$ MHz of frequency tuning was observed, while the received power varied by ΔP =30 dB (at broadside) with mirror position. The model described in the previous section shows that the mirror tuning range is smaller when the dielectric is electrically thinner, as in our case. Simulations show a tuning range of less than 100 MHz (3%), which is more than in the experiment, possibly due to diffraction loss that is not taken into account in the model. However,

when the dielectric constant of the substrate is increased to $\epsilon_r = 10$ in the model, the frequency of oscillation jumps to 4 GHz, and the tuning bandwidth increases to 12%.

Since the transistors are three terminal devices, the bias point is set by both the gate-to-source and the drain-to-source voltages. The drain bias affects both the output power and frequency, but the change in power is much less than in the case of mirror tuning. Drain bias tuning data for the dipole grid oscillating at 2.95 GHz and the bow-tie grid oscillating at 3.18 GHz are shown in Table 2.1. In both cases the output power increased as V_{DS} increased, as expected. The frequency of the dipole grid decreased with increasing drain bias while the opposite was observed for the bow-tie grid. For both grids, the output power is less dependent on gate bias than it is on drain bias. Gate bias tuning data for the dipole grid oscillating at 2.10 GHz and the bow-tie grid oscillating at 3.50 GHz are shown in Table 2.2. These oscillation frequencies are different in the cases of maximum drain and gate bias tuning, because the two biases do not tune the grids optimally at the same operating points. As shown in Fig. 2.4, the oscillation frequency increases approximately linearly with gate bias. The corresponding change in output power is small.

Table 2.1: Drain bias tuning data for the dipole and bow-tie grid oscillators.

Grid	ΔV_{DS}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
Dipole	1.5 Volts	42 MHz	1.4 %	5.5 dB
Bowtie	1.5 Volts	10 MHz	0.3 %	5.7 dB

Table 2.2: Gate bias tuning data for the dipole and bow-tie grid oscillators.

Grid	ΔV_{GS}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
Dipole	1.2 Volts	87 MHz	4.1 %	4.7 dB
Bowtie	1.7 Volts	55 MHz	1.6 %	2.5 dB

2.2.2 Varactor Tuning

In the oscillator system of Fig. 2.1, by varying the reverse bias on the varactors, the capacitance of the diodes, and therefore the frequency of oscillation, is changed. If varactor diodes are placed on the same side of the substrate as the FETs, the biasing

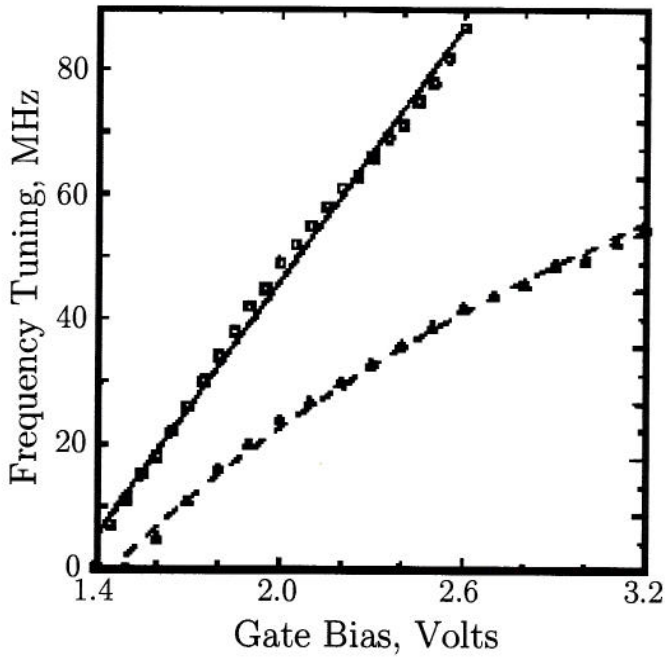


Figure 2.4. Gate bias tuning measured for the dipole and bow-tie grids. The grids locked respectively at 2.1 and 3.2 GHz. The solid line shows the dipole, and the dashed line the bow-tie behavior.

becomes complicated. If only a few varactors are placed on the back side of the transistor grid substrate, no measurable effect is observed on the frequency tuning. To keep biasing and fabrication simple, in the VCOs presented here, the varactor diodes form a separate grid placed back-to-back with the FET grid. In order to preserve the unit cell waveguide boundary conditions, the varactor grids are made to have the same period as the MESFET grids and the diodes are aligned with the transistors. Since the varactor structure is in the near field of the transistors, the original transmission-line circuit model is no longer applicable.

The behavior of the VCO is sensitive to the electrical thickness of the dielectric between the two loaded grids. The maximum amount of frequency tuning for both the dipole and bow-tie arrays was observed when the transistor and diode grids were placed directly back-to-back, with a 1-mm thick dielectric of $\epsilon_r = 2.2$ between them. In this case, each transistor is primarily affected by its own diode, and it is difficult to get all of the MESFETs to remain locked. The dipole grid locked at 2.8 GHz, and

the bow-tie grid at 6.0 GHz in this case. Tuning data are shown in Table 2.3, and the measured frequency tuning curves for these oscillators are shown in Fig. 2.5. A 9.9% tuning bandwidth around 4.9 GHz with less than 2 dB change in power was measured on an earlier 4 by 6 bow-tie array with a smaller period. In all cases, the polarization on the radiated wave was vertical and not affected by adding the varactor grids. These results indicate the feasibility of a planar broadband voltage controlled oscillator using a separate grid of varactor diodes as the tuning element.

In the previous measurements, the bow-tie and dipole oscillator frequencies and powers were different. Using a dielectric spacer 3.5 mm thick and with $\epsilon_r = 2.2$ between the grids, comparable output power levels were obtained at $V_{DS} = 2$V. For $V_{GS} = -1.6$V, the dipole grid locked at 2.6 GHz, and the bow-tie grid locked at 3.7 GHz for $V_{GS} = -2$V. It is seen in Table 2.4 that the bow-tie grid exhibits a wider frequency tuning range.

Table 2.3. Varactor diode tuning data for the oscillators with the transistor and diode grids back-to-back. Results for three different grids are shown.

Grid	ΔV_{Diode}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
7 × 7 Dipole	23.0 Volts	200 MHz	7.1 %	24.6 dB
7 × 7 Bowtie	30.0 Volts	616 MHz	10.3 %	12.0 dB
4 × 6 Bowtie	30.0 Volts	486 MHz	9.9 %	2.0 dB

Table 2.4. Varactor diode tuning data for the oscillators with two dielectric spacers between the transistor and diode grids.

Grid	ΔV_{Diode}	Δ Freq	$\frac{\Delta F}{F}$	Δ Power
7 × 7 Dipole	17.0 Volts	43 MHz	1.7 %	5.1 dB
7 × 7 Bowtie	30.0 Volts	154 MHz	4.2 %	14.1 dB

2.3 Conclusion

A quasi-optical voltage-controlled oscillator combining a large number of devices has been presented. A planar grid of frequency-locked MESFETs connected to radiating elements constitutes the heart of the system. Another planar grid of varactor

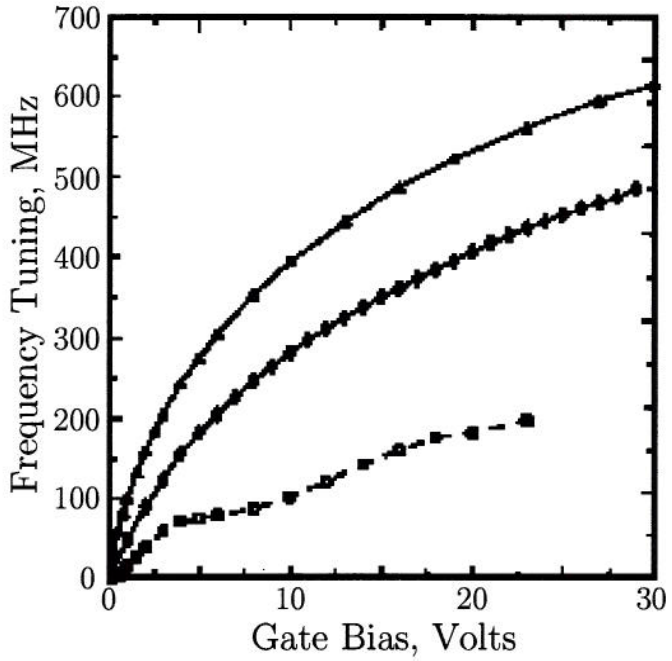


Figure 2.5. Varactor diode frequency tuning of three different oscillator grids with the transistor and diode grids back-to-back. The top curve represents the 7×7 bow-tie grid, the bottom curve represents the 7×7 dipole grid, and the middle curve represents the 4×6 bow-tie grid.

diodes is used to frequency tune the oscillator and the power radiated from the oscillating transistors is combined in free space producing the desired electromagnetic wave. Factors such as the radiating structure and coupling between the transistors and diodes play an important role in the frequency tuning range. A broadband structure such as the bow-tie array and near-field coupling through dielectric spacers are necessary to attain optimum performance from the system. The demonstrated 10% 2-dB tuning range shows the possibility of a constant power, broadband, frequency tunable oscillator using the basic system configuration presented here.

An oscillator alone may not be able to simultaneously provide enough output power and bandwidth for a particular application. A broadband or low phase-noise quasi-optical grid oscillator could be cascaded with a high power quasi-optical amplifier. Such a device is presented in the next chapter.

CHAPTER 3

THE PATCH/PATCH FREE-SPACE MESFET AMPLIFIER

3.1 Introduction

In this chapter, a quasioptical power combining transmission amplifier for increasing the power level available from solid-state circuits is presented, as shown in Fig. 3.1. Receiving and transmitting arrays of patch antennas, input/output isolation, MESFET's, bias and matching circuitry are contained on a single substrate, making monolithic millimeter-wave integration possible. The flexibility of selecting input polarization with respect to the output while maintaining amplifier stability is demonstrated. A 24-MESFET patch antenna amplifier array with 0.7 W of total output power at 10 GHz, with 10.3 dB of gain and 21 % power-added efficiency, is presented. The amplifier shown in Fig. 3.1 has an array of patch antennas on input and output sides of the substrate. Each common-source MESFET amplifier is coupled and matched to its input and output patch elements with microstrip lines. A substrate via connects the output of each amplifier to its radiating patch printed on the opposite side of the substrate. Alternating ground planes effectively isolate input and output sections of the amplifying structure. The ground planes are connected by vias periodically spaced at quarter-wavelength intervals. High impedance gate and drain bias lines run through the voltage nulls of the patches on input and output surfaces, respectively.

3.2 Single-MESFET, dual-patch amplifier element

A 10 GHz prototype amplifier element using Avantek ATF13484 GaAs MESFET's was built on a 0.508-mm-thick substrate with $\epsilon_r = 2.2$. To save space, minimize parasitics, and maximize circuit bandwidth, a single transmission-line matching section was used. The patch antennas were designed using an analysis and synthesis program [135], and are fed at their radiating edges. The use of a frequency-dependent one-port

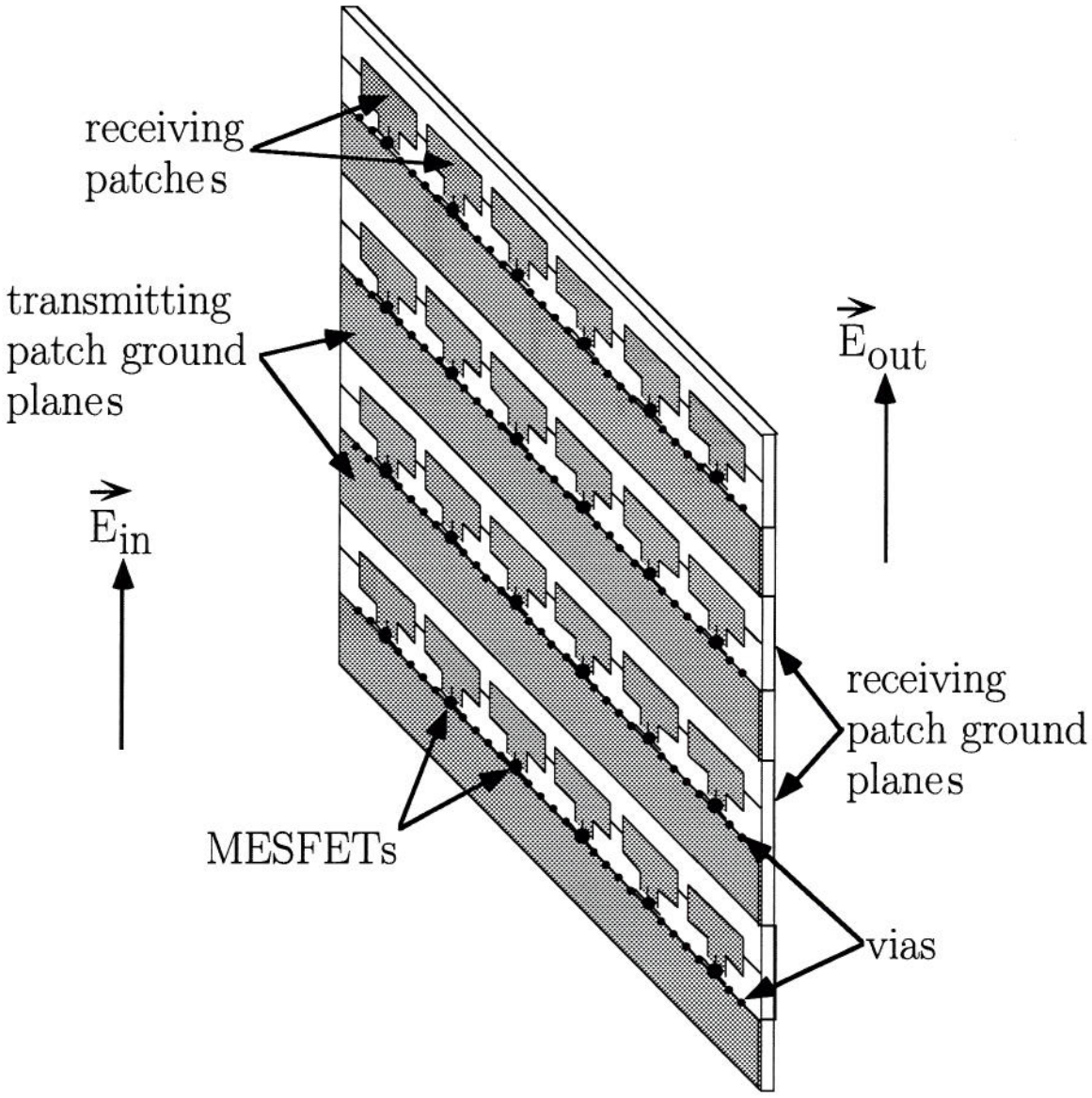


Figure 3.1: Free-space MESFET transmission wave amplifier.

equivalent circuit for the patch is essential to ensure stability of the amplifier over the frequency range in which the MESFET has gain. A bilateral design at 10 GHz was performed with a 100-Ω stabilizing resistor between the gate and source of the MESFET. The DC and RF voltages across the gate-to-source terminals are smallest in magnitude, so that efficiency is maximized and heat dissipation minimized. This design is stable and the maximum simulated gain is 8.4 dB at a low-current bias point. The final design of a single-MESFET dual-patch amplifier is shown in Fig. 3.2. The chip resistor is soldered directly between the transistor gate and source leads.

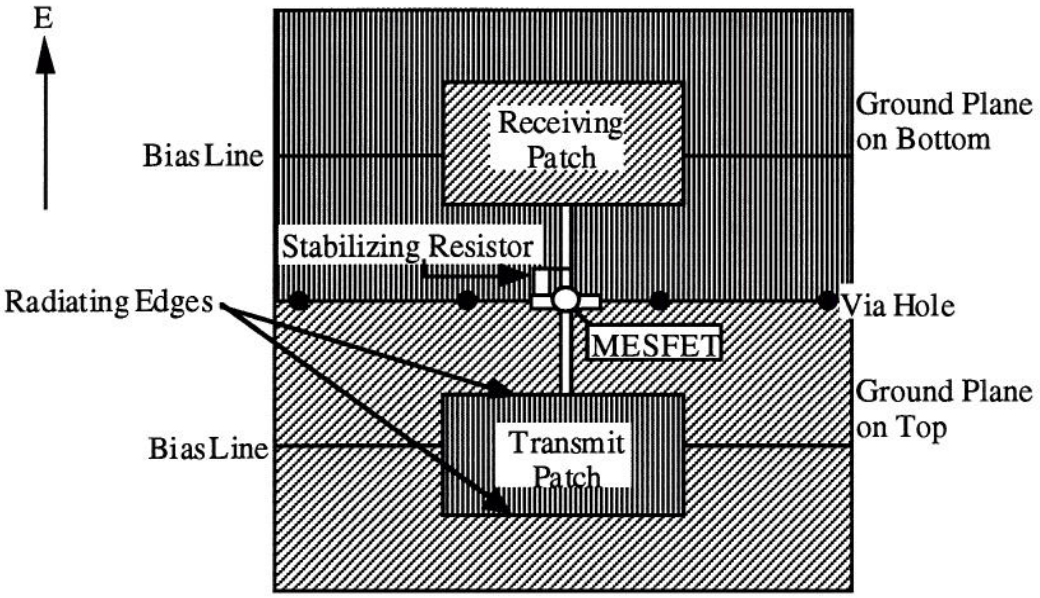


Figure 3.2. Single-MESFET dual-patch free-space amplifier with resistive loading for stability.

A free-space measurement technique similar to that in [58] determines the gain contributed by the MESFET's, as well as the frequency response of the array. Our technique uses a known frequency-dependent gain value of the patch element and the theoretical directivity of a uniform amplitude, equiphase array. Fig. 3.3 shows the experimental setup in which an absorbing screen at the array plane prevents diffraction path measurement error. Standard gain horns G_1 and G_2 are connected to an HP83640A synthesized sweeper and HP71500A/HP70820A microwave transition analyzer, respectively. First the path loss between the horn antennas is measured. The

free-space transmission amplifier is then placed between the horns, and the path loss is again measured. The ratio between these two measured powers is then given by

$$P' = \frac{P}{P_0} = G_{in} G_{out} G_{FET} \frac{(r_1 + r_2)^2}{r_1^2 r_2^2} (\frac{\lambda}{4\pi})^2, \tag{3.1}$$

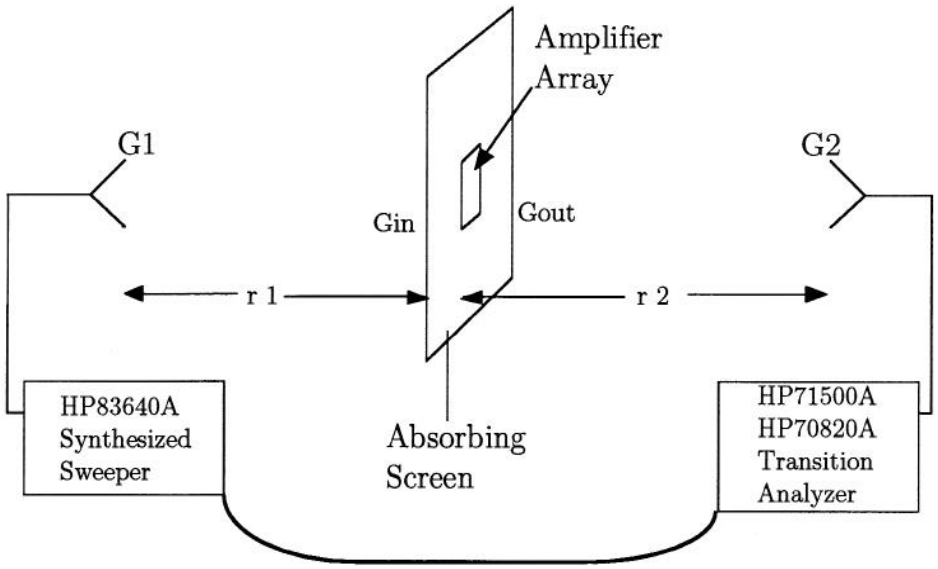


Figure 3.3. Experimental setup for measuring transistor-added gain for the free-space patch antenna amplifier.

where G_{in} and G_{out} are the effective input and output antenna gains of the amplifier array, respectively, G_{FET} is the gain added by the MESFET's, and r_1 and r_2 are the distances from the horn antennas to the array. Distances r_1 and r_2 are selected to be equal and in the far field of both the amplifier array and the horns.

Once P' is measured, the only unknown parameter in the above equation is G_{FET}, which is expected to be the same regardless of array size. The transistor-added gain of the single-MESFET dual-patch amplifier was measured from 9 to 11 GHz using the method outlined above, and the results are plotted in Fig. 3.4. When the FET's are not biased, there should be little power transmitted through the amplifier, as the alternating ground planes provide good input-to-output isolation. When the FET's are biased ($V_{ds} = 2.5$V, $I_{ds} = 20$mA), a maximum gain of 7.1 dB is measured at 10 GHz at the low-current bias point. The crosspolarization ratio for the output of the amplifier is 23.4 dB. In Fig. 3.4, the patch antenna's frequency-dependent gain is taken into

account. The frequency dependence of the patch antenna was calculated using a pc-baced program [135].

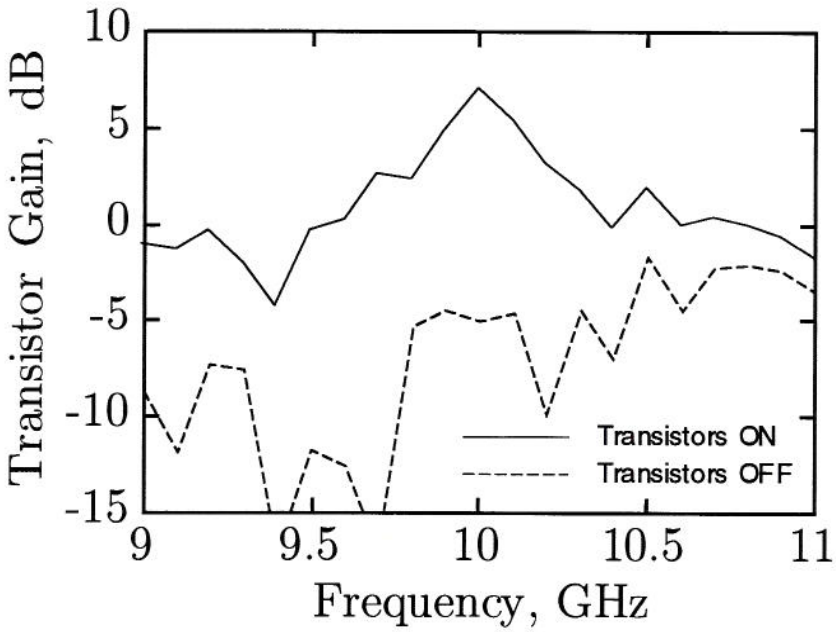


Figure 3.4. Measured gain versus frequency for the single-MESFET linearly polarized wave amplifier. The frequency dependence of the patch antennas are taken into account in the graph.

The structure of the patch antenna amplifier array allows for flexibility in the polarities of both the input and output waves. A single patch antenna amplifier element was designed to receive a linearly polarized wave, and transmit a circularly polarized wave, as shown in Fig. 3.5. The transmitting square patch is fed on two adjacent sides with 300-Ω edge impedance and a 90° separation in phase between the two feeds. The drain of the MESFET is biased through a via to the back of the square patch at a voltage null. A maximum transistor-added gain of 6.8 dB and an output axial ratio within 0.3 dB were measured at 10 GHz, at the low-current bias point (V_{ds} = 2.5V, I_{ds} = 20mA).

3.3 Patch antenna amplifier array

The single patch antenna amplifier element was placed into a 4x6 array, so that the power of 24 MESFET's could be combined in free space as shown in Fig. 3.1. The

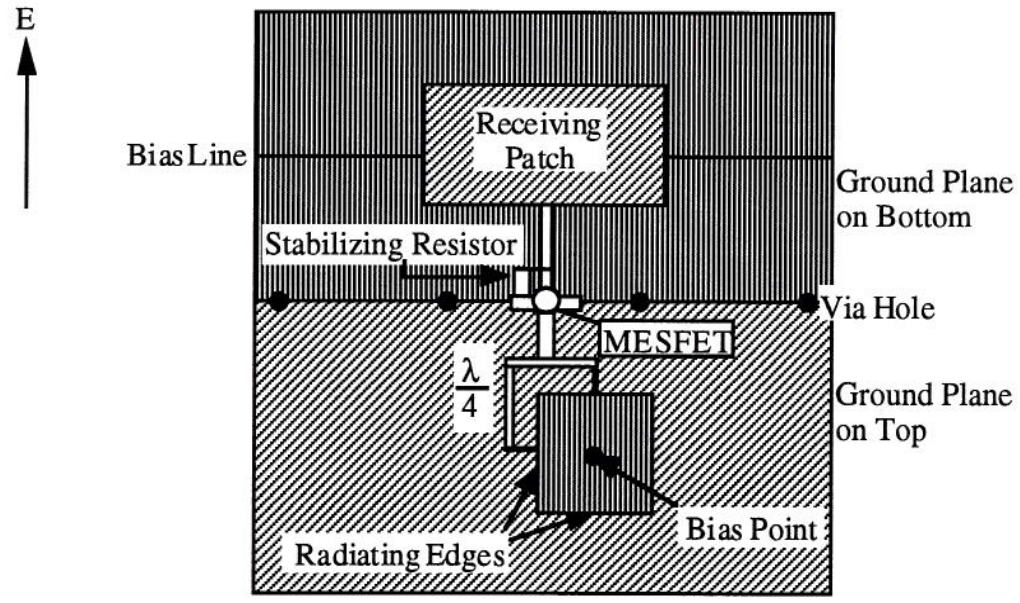


Figure 3.5. Single-MESFET dual-patch free-space amplifier with resistive loading for stability and with linearly polarized input and circularly polarized output wave.

horizontal spacing between elements is $\frac{2\lambda}{3}$ and the vertical spacing is $\frac{4\lambda}{3}$. It is assumed that this spacing is large enough so that the individual amplifiers do not significantly couple to each other.

The polarization-preserving 24-MESFET patch array was designed for maximum gain and stability at a lower bias point (20mA, 2.5V per device). The s-parameters at a higher bias point (40mA, 4V) are practically identical, except for an increase in $|S_{21}|$. Since, to a first approximation, only this parameter changes (decreases) when a MESFET is saturated, the design for a saturated class-A amplifier at the high bias point should be the same as the low-bias point linear design. The array is built on a $\epsilon_r = 2.17$, 0.5-mm Duroid substrate with Avantek low-cost general-purpose ATF13484 MESFETs.

First a single cell was measured between two polarization-aligned 16-dB gain horn antennas, placed in the far field of the active antenna. The horns were connected to a HP71500A Transistion Analyzer, used to measure the power saturation curves for several bias points, shown in Fig. 3.6. Then the array was placed in the setup. A TWT amplifier provides a total input power to the array of 64mW (2.7mW/device). The

on/off ratio was 10dB. With a constant input power and total array drain current of 1 A, the output power was measured for several drain-bias voltage points, and the results are given in Table 3.1. For obtaining the values in Table 3.1, a patch gain of 5.5 dB was used, which was measured using the Friis transmission formula on a microstrip-fed patch antenna in the lab with dimensions identical to the patch antennas in the array. The small-signal gain was measured to be 7.1 dB for the single cell in the previous section at the low-power bias point (20mA, 2.5V). At the high-power bias point (40mA, 4V), the single cell now demonstrated a small-signal gain of almost 12 dB.

In Fig. 3.6, saturation curves are plotted for a unit cell. The entire array results are superimposed on the curves. The average power per element in the array is slightly lower than that of a single element tested alone, which means that the array combining is lower than in an ideal uniform array. For this low-cost class-A amplifier, an output power of 0.7 W with 21 % power-added efficiency was measured at 10 GHz for a DC power of 3 Watts.

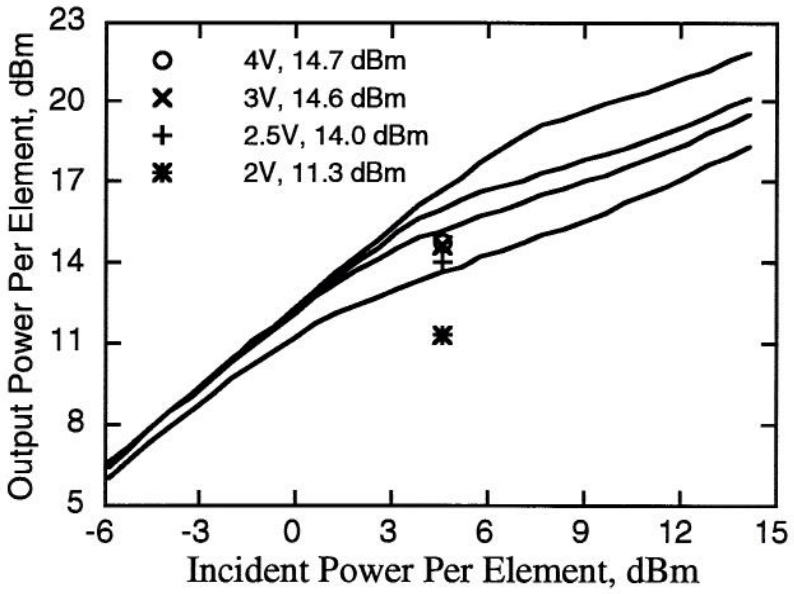


Figure 3.6: Saturation curves for the 4x6 free-space amplifier.

Table 3.1: Summary of results for the saturated 4x6 free-space amplifier.

Vds for Id = 1 Amp	Gain (dB)	Output Power (W)	Drain Efficiency	Power-Added Efficiency
2.0	8.6	0.3	16%	13%
2.5	9.7	0.6	24%	22%
3.0	10.3	0.7	23%	21%
4.0	10.4	0.7	18%	16%

3.4 Conclusions

Free space provides for nearly ideal power combining; superposition in space allows large numbers of active devices to be power-combined without the losses inherent in a guided transmission-line medium. A free-space class-A amplifier which combines the power of 24 Avantek 13484 MESFETs has been presented. Each transistor provides approximately 40 mW individually; in the free-space array, 24 elements provide a total power of about 0.7 Watts at 10 GHz. In this chapter it has been shown that the quasi-optical power-combining structure preserves not only the gain of the individual elements, but also the power output *and efficiency* of each individual element. Also, this structure provides flexibility in the polarization of the input and output waves, because they are isolated using a meandering ground plane, not using orthogonality as all other power-combining amplifiers have used to date. In chapter 6, the principles demonstrated in this chapter will be used at a higher efficiency and output power level, using the nonlinear class-E amplifier approach, rather than the more traditional class-A approach used here.

CHAPTER 4

ANALYSIS OF THE CLASS-E CIRCUIT

4.1 Introduction

A 75% efficient amplifier can deliver three times the power that a 50% efficient amplifier can deliver, using the same devices, if the output power is limited by the heat dissipated by the transistors. The class-E switched-mode amplifier topology is investigated in this chapter with high efficiency in mind (a brief overview of the different classes of amplification is given in Chapter 1). Figure 4.1 shows the topology first proposed by Sokal and Sokal in 1975 [1]. The class-E amplifier is a resonant switched-mode circuit in which the switch turns on at zero voltage and zero derivative of voltage, and in which the product of the switch voltage and current is zero. The active device, in this case a MESFET, acts as a switch, and the surrounding circuitry needs to be properly designed to give class-E operation. At low RF frequencies, such circuits have shown to exhibit efficiencies as high as 96% [1]. Ideally, the efficiency is limited only by the drain-to-source saturation resistance of the transistor and the lossy properties of its parasitic elements. Device parasitic reactances are included in the tuned circuit design and do not degrade the circuit performance. The capacitance C_s in the circuit in Figure 4.1 may be the intrinsic output capacitance of the transistor, while part of the inductance L may be the lead inductance of a packaged MESFET transistor, for example. Earlier work has hinted at the possibility of including the device output capacitance in the class-E circuit, but using the device's output capacitance *solely* for the switch capacitance in the class-E circuit has not been found in the literature.

4.2 Simplified analysis of the original class-E circuit

There are several assumptions made in the simplified analysis of the class-E circuit presented here (see Figure 4.1). A 50% duty cycle is used in this analysis; the

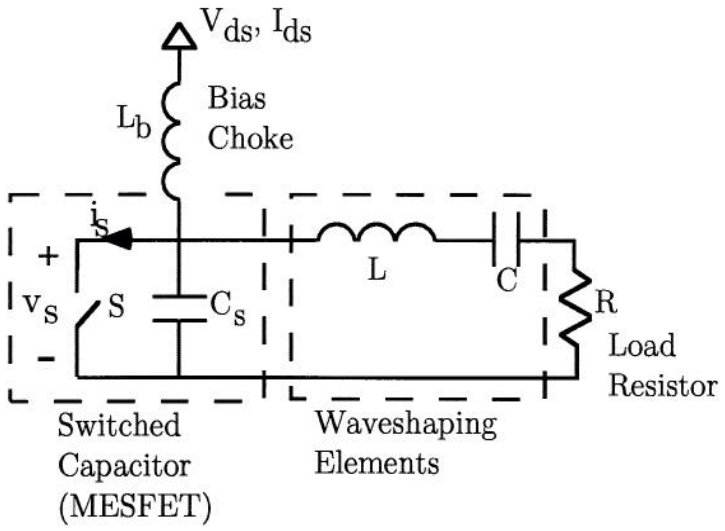


Figure 4.1: The original class-E high-efficiency circuit.

transistor switch is ON half of the period, and OFF the other half. This is shown in [122] to be the optimal case. It is assumed that the switching element has zero on-resistance and infinite off-resistance. For a properly designed gate-drive circuit, the off resistance will be very large, but care must be taken to ensure that the on-resistance of a practical GaAs FET is much smaller than the impedance that it drives when it is turned on. The shunt capacitor C_s for a maximum-frequency design consists solely of the output capacitance of the transistor and is assumed to be linear in this analysis. In practice, the capacitance C_s is often nonlinear; its capacitance changes as a function of the voltage applied across it. The effects of this nonlinearity are addressed; it has been found that an equivalent linear capacitance can approximate the nonlinear real capacitance in the circuit for a first-order design. L_b acts as an ideal bias choke (open circuit at RF). For DC biasing, the voltage V_{ds} appears across the MESFET drain-source terminals, but not across the output port R. There are no losses in the idealized circuit except into the load R. Therefore, all of the input power $V_{ds}I_{ds}$ ends up dissipated in R (100% efficiency operation). The external load network L-C-R has a high Q-factor and resonates slightly below the switching frequency f_s, so that the voltage across the output port R is constrained to be a sinusoid. Another effect of the high-Q filter section L-C is to constrain the current into L to also be approximately a sinusoid at the

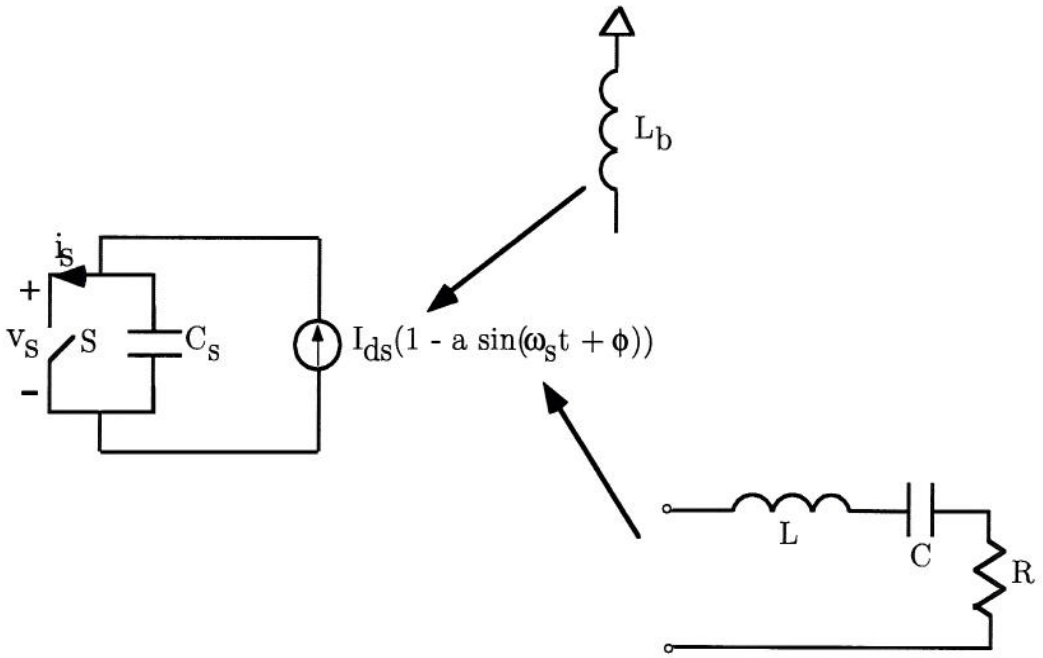


Figure 4.2: Class-E circuit assuming sinusoidal load current.

switching frequency. These assumptions simplify the basic explanation of the class-E circuit significantly and allow tractable equations to describe its operation [122]. The exact solution of this circuit in the time domain, still assuming ideal (lossless) elements and linear C_s, requires the solution of a time-varying third-order system of ordinary differential equations. This exact solution is given in Appendix A.

The assumptions used in the analysis in this chapter are illustrated in Fig. 4.2. The current flowing into the choke inductor L_b is assumed to be constant (I_{ds}), and the current flowing into the filter load network is assumed to be sinusoidal at the switching frequency. An equivalent current is placed across the switched capacitor, which consists of constant (DC) and sinusoidal (RF) components. The class-E amplifier is thus reduced to a time-varying first-order system.

It is seen in Fig. 4.2 that the switch can be either ON or OFF. When the switch is turned ON, there is no voltage across the switch, but a piece of sinusoidal current (with a DC component) flows through it. At the instant of switch turn-on, the current through the switch is zero, but at the instant of switch turn-off, a discontinuous jump in current appears across the switch as the flow of current is transferred from the switch

to the capacitor (see Fig. 4.3). This jump in current will cause losses to appear across any parasitic inductance between the switch and the capacitor. In the case presented here, where C_s is the internal parasitic capacitance of a transistor, this inductance is minimized. If an external shunt capacitance is used (the usual case), then any parasitic inductance between the transistor and the shunt capacitor causes an energy of $\frac{1}{2}Li^2$ to be lost every switching period due to the current jump in the parasitic inductance. It has been shown [136] [137] that at least one discontinuity in switch voltage or switch current is necessary for nonzero output power of such a circuit. So the minimum possible number of discontinuities (as found in the definition of the class-E circuit) is 1, and since capacitive switching losses dominate at microwave frequencies, it is best to constrain this discontinuity to appear across the switch current.

When the switch turns OFF, the sinusoidal current continues to flow, but now it flows through the shunt capacitive part of the switch, as shown in Figure 4.2. During the OFF interval,

$$C_s \frac{\mathrm{d}v_s}{dt} = I_{ds}(1 - a\sin(\omega_s t + \phi)). \tag{4.1}$$

Integrate:

$$v_s(t) = \frac{I_{ds}}{C_s}\int_0^t (1 - a\sin(\omega_s t' + \phi))\, dt'. \tag{4.2}$$

The integral implicitly assumes that $v_{C_s}(0) = 0$, which is one of the three boundary conditions which will be imposed upon $v_{C_s}(t)$. Thus

$$v_s(t) = \frac{I_{ds}}{\omega_s C_s}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)). \tag{4.3}$$

The other two conditions for class-E operation are

$$v_s\left(\frac{T_s}{2}\right) = 0, \tag{4.4}$$

$$\frac{\mathrm{d}v_s}{dt}\left(\frac{T_s}{2}\right) = 0. \tag{4.5}$$

The first condition avoids shorting the capacitor C_s when there is voltage across it during switching, and the second condition ensures a "soft" turn-on condition for the switching device. These two additional constraints determine a and ϕ uniquely:

$$a = \sqrt{1 + \frac{\pi^2}{4}} \simeq 1.862, \tag{4.6}$$

$$\phi = -\arctan\frac{2}{\pi} \simeq -32.48°. \tag{4.7}$$

Note that these are constants for *any* high-Q class-E circuit with a capacitor in shunt with the switch (any microwave class-E circuit, for example). Now the voltage and current across the switch are known:

$$(0 \leq (\omega_s t) \leq \pi): \quad v_s(t) = \frac{I_{ds}}{\omega_s C_s}((\omega_s t) + a(\cos((\omega_s t) + \phi) - \cos\phi)), \tag{4.8}$$

$$(\pi \leq (\omega_s t) \leq 2\pi): \quad v_s(t) = 0. \tag{4.9}$$

$$(0 \leq (\omega_s t) \leq \pi): \quad i_s(t) = 0, \tag{4.10}$$

$$(\pi \leq (\omega_s t) \leq 2\pi): \quad i_s(t) = I_{ds}(1 - a\sin(\omega_s t + \phi)). \tag{4.11}$$

The switch voltage and current time waveforms are plotted in Fig. 4.3.

It is of interest to find the relationship between V_{ds} and I_{ds}, or in other words, how much current is drawn for a given supply voltage or vice-versa. V_{ds} is the DC component of $v_s(t)$, the voltage across the switch, capacitor and load network. Take the time average of the switch voltage:

$$V_{ds} = \frac{1}{T_s}\int_0^{\frac{T_s}{2}} v_s(t)\,dt = \frac{1}{\pi}\frac{I_{ds}}{\omega_s C_s}, \tag{4.12}$$

$$I_{ds} = \pi\omega_s C_s V_{ds}. \tag{4.13}$$

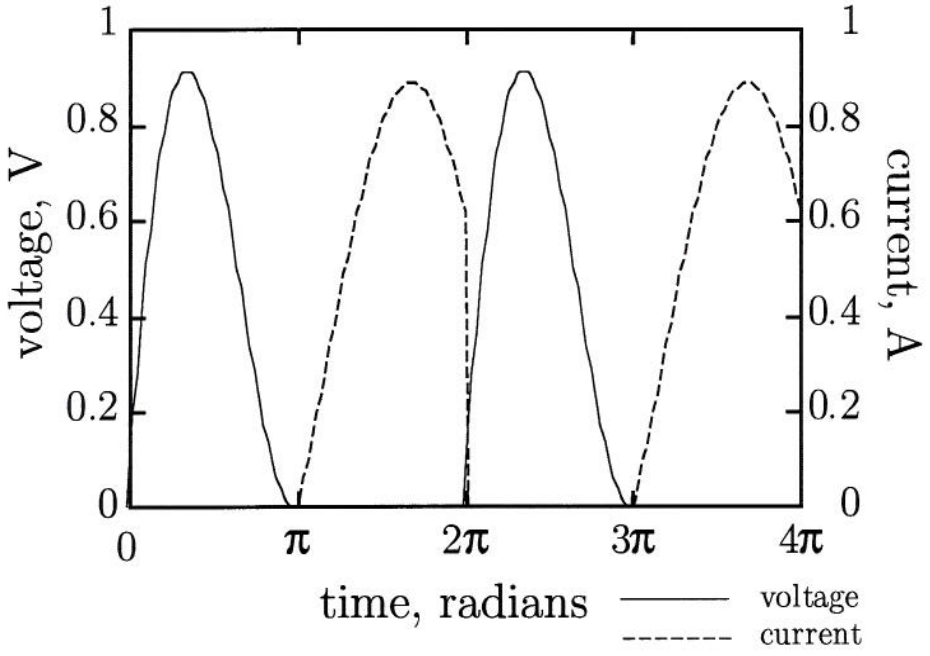


Figure 4.3. Theoretical class-E switch voltage and current time waveforms, assuming sinusoidal load network current.

This rather simple result has important implications for a practical microwave class-E circuit, assuming that the minimum value of C_s must necessarily be the parasitic capacitance of a microwave device, for example C_{ds} of a MESFET. For example, at a specified frequency, a device with an output capacitance C_s must operate at some supply voltage V_{ds}, which must be well above the transistor's knee voltage. Since ω_s, C_s, and V_{ds} are now specified, the device must be able handle the required maximum current, which is $(1+a)I_{ds} \simeq 2.86 I_{ds}$! If the device cannot handle this current, then it is *impossible* to make an ideal class-E circuit with the particular device at that frequency. In fact, an approximate maximum frequency of class-E operation can be found for a given device:

$$f_{max} = \frac{I_{ds}}{2\pi^2 C_s V_{ds}} = \frac{I_{max}}{C_s V_{ds}} \frac{1}{2\pi^2(1+a)} \simeq \frac{I_{max}}{56.5 C_s V_{ds}}. \tag{4.14}$$

For higher drain bias voltage, the maximum frequency of operation decreases. Consider, for example, the Siemens CLY5 MESFET. For this transistor, $I_{max} \simeq 1200\,\text{mA}$ and $C_s \simeq 2.6\,\text{pF}$. For this transistor at a DC drain voltage of $V_{ds} = 6\,\text{V}$, $f_{max} \simeq 1.4\,\text{GHz}$.

At $V_{ds} = 3\,\mathrm{V}$, $f_{max} \simeq 2.4\,\mathrm{GHz}$. Above these frequencies, this device can not be used for an *ideal* class-E circuit, although an approximation to class-E operation may be obtained at higher frequencies with some degradation in maximum achievable efficiency [138]. Experimental verification of the concept of maximum frequency of class-E operation is given in the next chapter, using the CLY5 at 0.5, 1, and 2 GHz.

The above discussion also implies that a given technology (MESFET, HEMT, HBT) using a given fabrication process will yield some maximum class-E output power as a function of frequency.

Finding the DC component of $v_s(t)$ yields an expression relating the DC parameters of the class-E circuit (V_{ds} and I_{ds}). Finding the fundamental-frequency component of $v_s(t)$ will yield information about the RF complex impedances in the circuit. These will then be used to find design equations for the load network element values. The higher harmonic frequency components present in the switch voltage will not be considered for this first-order analysis, however the load network is assumed to be a near-infinite impedance at the higher harmonics, and therefore the currents flowing into the load network at the higher harmonics should be near zero. The fundamental component of load current, i_{net_1}, is known, but the fundamental component of load voltage, v_{s_1}, must be found using Fourier series, since $v_s(t)$ is a periodic function. Thus, we have

$$v_s(t) = \sum_{n=-\infty}^{\infty} K_n e^{jn\omega_s t}, \tag{4.15}$$

$$K_n = \frac{1}{T_s} \int_0^{\frac{T_s}{2}} v_s(t) e^{-jn\omega_s t}\, dt, \tag{4.16}$$

$$K_1 = \frac{I_{ds}}{\omega_s C_s T_s} \int_0^{\frac{T_s}{2}} (\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)) e^{-j\omega_s t}\, dt. \tag{4.17}$$

The integral is taken over only the first half of the period because $v_s(t)$ is zero over the second half of the period. The calculations are somewhat tedious, so only the results are given here.

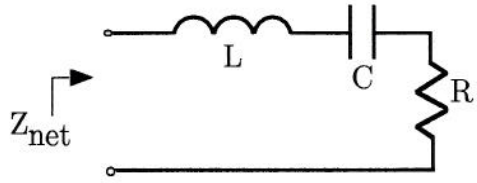


Figure 4.4: External load network seen by the switched capacitor at RF frequencies.

$$v_{s_1} = a_0 I_{ds} \sin(\omega_s t + \phi_0) \tag{4.18}$$

$$i_{net_1} = a I_{ds} \sin(\omega_s t + \phi), \tag{4.19}$$

where the constants a and ϕ were found earlier, and where

$$a_0 = \frac{2|K_1|}{I_{ds}} = \frac{1}{\omega_s C_s}\sqrt{\frac{\pi^2}{16} + \frac{4}{\pi^2} - \frac{3}{4}}, \tag{4.20}$$

$$\phi_0 = \frac{\pi}{2} + \angle K_1 = \frac{\pi}{2} + \arctan(\frac{2\pi}{8 - \pi^2}). \tag{4.21}$$

The phasor impedance of the external load network can now be found:

$$Z_{net_1} = \frac{a_0}{a} e^{j(\phi_0 - \phi)} \simeq \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ}. \tag{4.22}$$

Notice that the required load angle for class-E operation with a capacitor in shunt with the switch is a constant, *regardless of the rest of the topology.* The magnitude is directly proportional to the impedance of the capacitor shunting the switch at the switching frequency. To ensure class-E operation, all that is needed is a specific fundamental impedance of Z_{net_1}, and open-circuit conditions at all of the higher harmonic frequencies (a filter can do this).

Now the specific external load network topology comes into the picture (Figure 4.4). All that is important for this step is the impedance of this particular topology at the switching frequency f_s (this network satisfies the condition of large input impedance at the higher harmonic frequencies):

$$Z_{net_1} = j\omega_s L + \frac{1}{j\omega_s C} + R. \tag{4.23}$$

Equating the two expressions for Z_{net_1}, one complex equation in the two unknowns C_s and C is obtained. Equating real and imaginary parts of the equation, expressions for C_s and C are found:

$$C_s = \frac{1}{2\pi f_s R(\frac{\pi^2}{4}+1)(\frac{\pi}{2})} \simeq \frac{1}{2\pi f_s R 5.447}, \tag{4.24}$$

$$C = C_s\left(\frac{(\frac{\pi^2}{4}+1)(\frac{\pi}{2})}{Q_L}\right)\left(1+\frac{\frac{\pi^3}{16}-\frac{\pi}{4}}{Q_L-(\frac{\pi^3}{16}-\frac{\pi}{4})}\right) \simeq C_s\left(\frac{5.447}{Q_L}\right)\left(1+\frac{1.153}{Q_L-1.153}\right), \tag{4.25}$$

where Q_L is *defined as*

$$Q_L = \frac{\omega_s L}{R}. \tag{4.26}$$

These equations for C_s and C were introduced in the above form for comparison with the original equations presented in [1]. The expression for C_s found here is identical to the expression given there. However, the expression given there for C is

$$C \simeq C_s\left(\frac{5.447}{Q_L}\right)\left(1+\frac{1.42}{Q_L-2.08}\right). \tag{4.27}$$

The quantities 1.42 and 2.08 were determined from experimental measurements in [1]. The assumption used in the analysis given here is that Q_L is large; the experimental measurements were most likely made with a small value of Q_L (one example circuit given in [1] has $Q_L = 6$). Therefore, the results presented here are more accurate than those presented in [1] for high-Q_L operation.

To design a class-E amplifier using this topology, first ω_s, L, and R are chosen. These parameters determine Q_L. Then C_s and C are evaluated using the above expressions. However, this topology has limited usefulness for microwave circuits, because frequency, load impedance, and switch capacitance cannot be independently chosen. For a saturated microwave amplifier, the load impedance is often set at 50Ω, and usually one starts out with a particular transistor in mind, which has a certain output capacitance C_s. Then the frequency of operation ω_s is chosen. For the above topology, these

three quantities cannot be independently chosen. Therefore another topology, which is much more convenient to use for a microwave class-E amplifier, is presented in the next section.

4.3 The series-L/shunt-C lumped-element class-E circuit

The series-L/shunt-C lumped-element class-E circuit is shown in figure 4.5. L_b and C_b act as a bias tee, but are assumed not to affect the RF operation of the circuit appreciably. At the switching frequency, only L, C, and R contribute to the RF impedance seen by the switched capacitor (Figure 4.6). This impedance is

$$Z_{net_1} = j\omega_s L + \frac{R}{1 + j\omega_s CR}. \tag{4.28}$$

As before, the desired load network impedance at the switching frequency is

$$Z_{net_1} = \frac{k_0}{\omega_s C_s} e^{j\theta_0}, \tag{4.29}$$

$$k_0 = \omega_s C_s \frac{a_0}{a} \simeq 0.28015, \tag{4.30}$$

$$\theta_0 = \phi_0 - \phi \simeq 49.0524°. \tag{4.31}$$

Equating the two expressions for Z_{net_1}, one complex equation in two unknowns (L and C) is obtained. Equating real and imaginary parts of the equation, expressions for L and C are found:

$$L = \frac{k_0}{\omega_s^2 C_s} \left(\sin\theta_0 + \cos\theta_0 \sqrt{\frac{\omega_s C_s R}{k_0 \cos\theta_0} - 1} \right), \tag{4.32}$$

$$C = \frac{1}{\omega_s R} \sqrt{\frac{\omega_s C_s R}{k_0 \cos\theta_0} - 1}. \tag{4.33}$$

For this topology, the load resistor, operating frequency, and switch capacitance can be independently chosen, unlike the original class-E circuit analyzed above. Therefore, a transistor such as the Siemens CLY5 could, for example, be chosen for a class-E

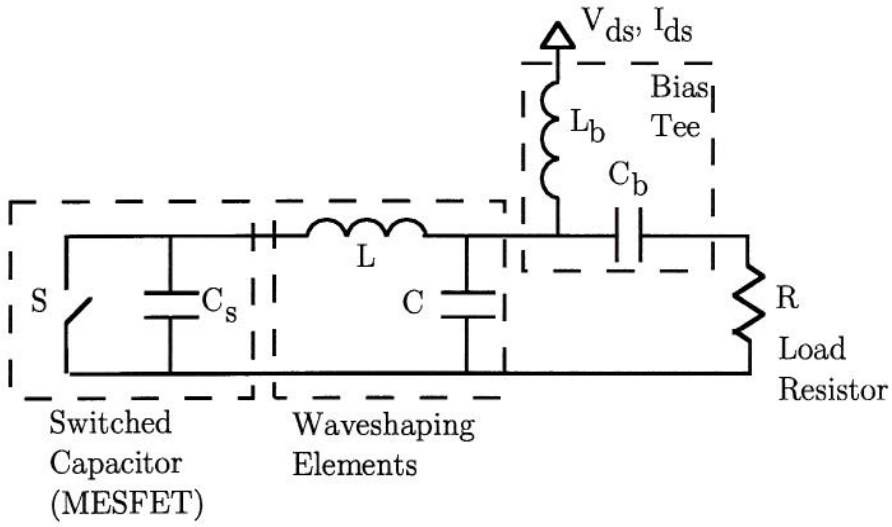


Figure 4.5: The series-L/shunt-C lumped-element class-E circuit.

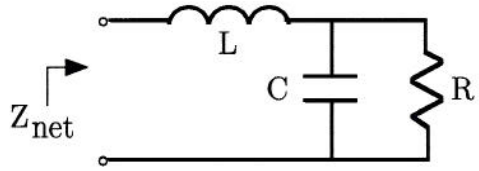


Figure 4.6. External load network of the series-L/shunt-C class-E circuit seen by the switched capacitor at the switching frequency.

circuit at 1 GHz with a load impedance of 50Ω. For the original topology analyzed previously, an additional impedance transformer would have to be included to get the load impedance to 50Ω.

4.4 The series/shunt transmission-line class-E circuit

At microwave and millimeter-wave frequencies, transmission lines are often preferred over lumped elements because lumped elements are much lossier and more difficult to fabricate. Figure 4.7 shows the series/shunt transmission-line class-E circuit. As above, L_b and C_b act as a bias tee, but are assumed not to affect the RF operation of the circuit appreciably. The transmission lines may be microstrip, coplanar waveguide, or any other guiding medium. This circuit is similar in operation to the series L/shunt C lumped-element class-E circuit presented above. Both transmission lines are assumed to be between 0° and 90° long. Therefore, the shunt open-circuited transmission line looks like a capacitor at the switching frequency, and the series section of line looks

inductive.

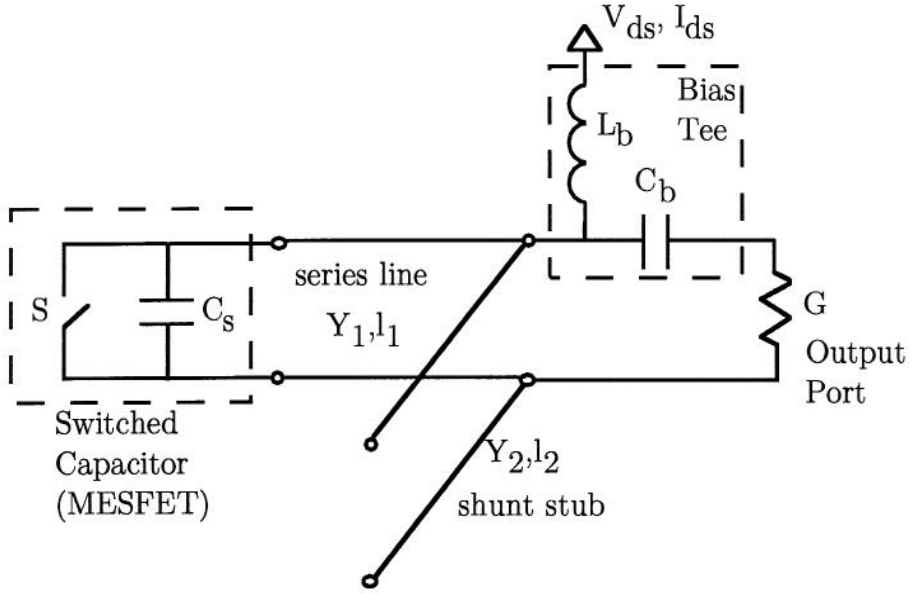


Figure 4.7: The series/shunt transmission-line class-E circuit.

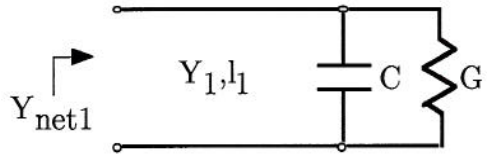


Figure 4.8. Equivalent circuit of the load network for the series/shunt transmission-line class-E circuit at the switching frequency. The open-circuited shunt stub has been replaced by an equivalent capacitor C.

It is assumed that $|Z_{net}| < R$, or $\frac{0.281}{\omega_s C_s} < R$. To first order, the series/shunt transmission lines step the large-signal transistor output impedance up to R. However, for maximum efficiency, the class-E conditions are applied (admittance is used here for simplicity):

$$Y_{net1} = \frac{\omega_s C_s}{k_0} e^{-j\theta_0}, \tag{4.34}$$

where k_0 and θ_0 were derived earlier.

Once again, at RF frequencies, the bias tee does not contribute to the load network impedance. The shunt section of transmission line looks capacitive at the switching frequency, and can be replaced by an equivalent capacitor C (its length is less

than 90°). The modified circuit is shown in figure 4.8. At the switching frequency,

$$Y_{net1} = Y_1 \frac{G + j\omega_s C + jY_1 \tan(\beta_1 l_1)}{Y_1 - \omega_s C \tan(\beta_1 l_1) + jG \tan(\beta_1 l_1)}. \tag{4.35}$$

Equating real and imaginary parts of the two expressions for Y_{net1}, two equations are found for the two unknowns C and $\tan(\beta_1 l_1)$:

$$\omega_s C_s \cos\theta_0((Y_1 - \omega_s C \tan(\beta_1 l_1))^2 + (G \tan(\beta_1 l_1))^2) - \tag{4.36}$$
$$k_0 Y_1(G(Y_1 - \omega_s C \tan(\beta_1 l_1)) + G \tan(\beta_1 l_1)(\omega_s C + Y_1 \tan(\beta_1 l_1))) = 0,$$

$$\omega_s C_s \sin\theta_0((Y_1 - \omega_s C \tan(\beta_1 l_1))^2 + (G \tan(\beta_1 l_1))^2) + \tag{4.37}$$
$$k_0 Y_1((\omega_s C + Y_1 \tan(\beta_1 l_1))(Y_1 - \omega_s C \tan(\beta_1 l_1)) - G^2 \tan(\beta_1 l_1)) = 0.$$

These two equations may be solved numerically. A good initial guess is $C = C_s$ and $\tan(\beta_1 l_1) = 1$. C and C_s are of the same order of magnitude, and the series transmission line is between 0° and 90°; picking a starting length of 45° corresponds to $\tan(\beta_1 l_1) = 1$.

After C and $\tan(\beta_1 l_1)$ are found using numerical solution, the electrical length of the transmission lines can be determined.

$$(0° < \beta_1 l_1 < 90°) \quad \beta_1 l_1 = \arctan(\tan(\beta_1 l_1)), \tag{4.38}$$

$$(0° < \beta_2 l_2 < 90°) \quad \beta_2 l_2 = \arctan(\frac{\omega_s C}{Y_2}). \tag{4.39}$$

Transmission-line lengths l_1 and l_2 are usually determined using experimental load-pull techniques or harmonic-balance circuit simulations, without insight into the operation of the circuit. The design formulas presented here give a first-order high-efficiency output match for a microwave transistor, and give insight into the operation of high-efficiency microwave amplification. Experiments and harmonic-balance circuit simulations presented in Chapter 5 and Chapter 6 validate this approach. For most

practical cases, when the lengths l_1 and l_2 are reasonably close to 45°, the load network presents a high impedance to the switched capacitor at the second harmonic. It is even possible to adjust the characteristic impedances of the two lines such that their lengths turn out to be exactly 45° at the fundamental frequency of operation. Later in this chapter, it will be shown that two harmonics are sufficient to generate an approximate class-E switch voltage waveform (see Figure 4.11, for example).

4.5 Explicit enforcement of harmonic open-circuit conditions using transmission lines

In the previous section, a single-stub class-E transmission line topology was presented. At the switching frequency, the correct impedance is presented to the transistor. At the higher harmonic frequencies, no explicit constraints are placed on the load impedance; it is assumed that the load impedance is large for the higher harmonics. It has been found that the above circuit works in class-E mode for practical cases, but there is some harmonic content in the output signal, and therefore a small loss in efficiency due to imperfect harmonic termination. In this section, some methods for overcoming these limitations are presented.

First, it is known that the second harmonic of switch voltage is of primary importance in the operation of a class-E amplifier (this will be discussed later). The design method for the single section series/shunt transmission-line class-E circuit presented in the previous section assumed that some known impedance of transmission line (like 50Ω) would be used for the series and shunt sections of the class-E circuit. Then the only design parameters were the lengths of the lines, and it is hoped that the second-harmonic impedance of the load network is large. However, there are two more degrees of freedom if the impedance of the lines is left as a variable. For example, if the lengths of the two lines is set to 45°, then the equations in the previous section can be used to find the correct impedance transmission lines to enforce the class-E conditions at the fundamental switching frequency. If this is done, then both transmission lines are a quarter-wavelength (90°) long at the second harmonic, which explicitly enforces a

perfect open circuit at the switched capacitor at the second harmonic. This method is useful for many practical cases, although there may be some situations where another method for explicit open-circuit harmonic termination may be required. For example, in some situations, a limited range of transmission-line characteristic impedances are available.

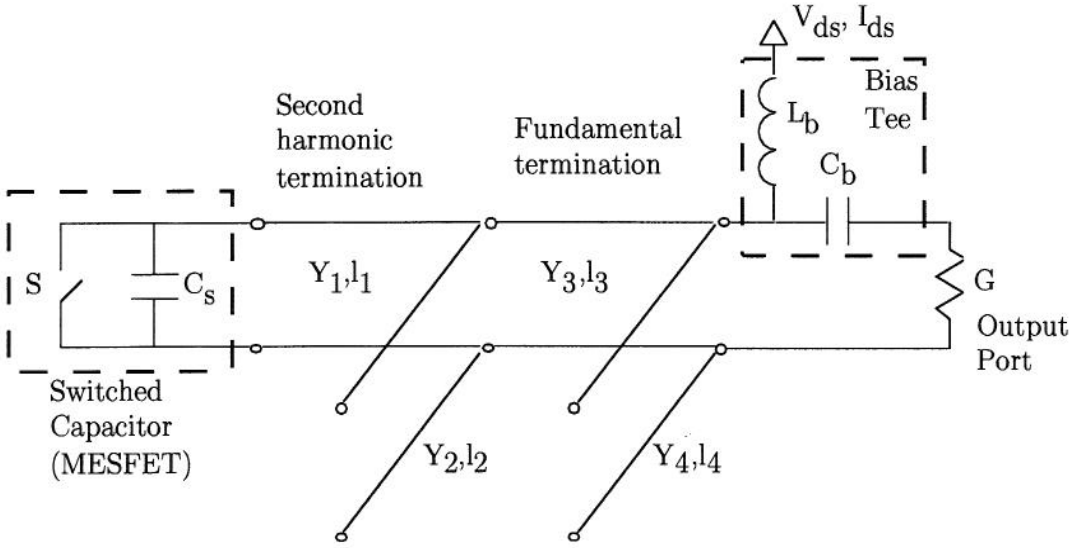


Figure 4.9. Class-E transmission line circuit with a second-harmonic open-circuit termination at the output port.

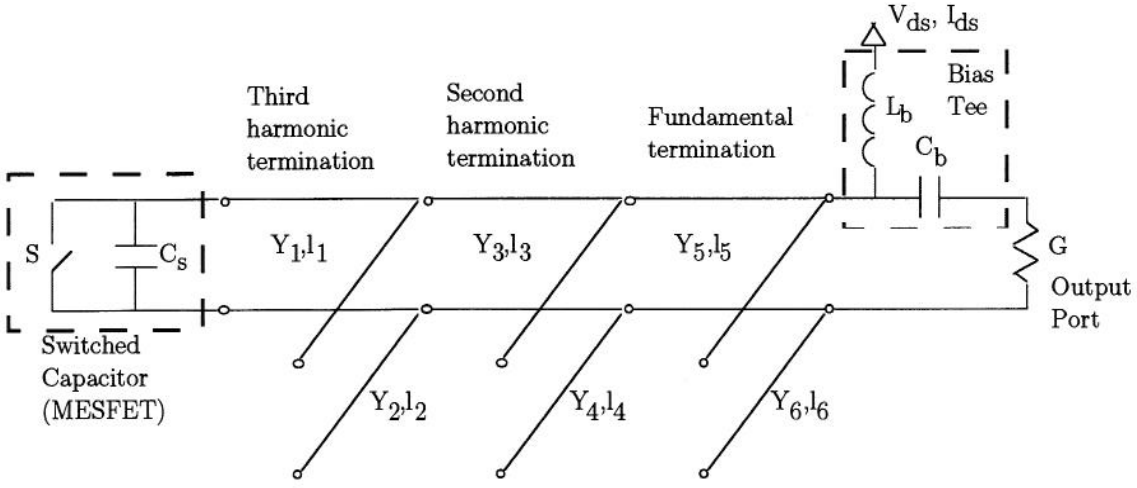


Figure 4.10. Class-E transmission-line circuit with second- and third-harmonic open-circuit terminations at the transistor output port.

In figure 4.9, a new transmission-line topology is shown. The first set of lines, l_1 and l_2, enforce an open-circuit condition at the second harmonic frequency. Line

l_2 is 45° long at the fundamental frequency, which makes it 90° long at the second harmonic frequency; since it is open-circuited at one end, a short circuit will appear at the point where it intersects line l_1 and line l_3 at the second harmonic. Line l_1 is also 90° long at the second harmonic frequency, and transforms this short circuit to an open circuit. This open-circuit condition occurs regardless of the values of lines l_3 and l_4. At the first harmonic frequency, lines l_3 and l_4 act as a single stub match, such that the output impedance (usually 50Ω) is transformed to the correct impedance at the transistor output port. This impedance is the one found previously:

$$Z_{net1} = \frac{k_0}{\omega_s C_s} e^{j\theta_0}. \tag{4.40}$$

In practice, the lengths of lines l_3 and l_4 can be found on a linear circuit simulator package. Ideally, the signal produced at the output of this circuit will not have *any* second harmonic component.

The concept of explicit open-circuit enforcement can be extended to three harmonics, as shown in figure 4.10. In this modified circuit, lines l_1 and l_2 are both 30° long at the fundamental frequency, which makes them both 90° long at the third harmonic frequency. Once again, line l_2 creates a short circuit where it intersects with lines l_1 and l_3, and line l_1 transforms this short circuit to an open circuit at the transistor. Line l_4 is 45° long at the fundamental frequency, and creates a short circuit where it intersects lines l_3 and l_5. Line l_3, however, is *shorter* than 45° at the fundamental frequency. It is shortened to compensate for the effects of lines l_1 and l_2 at the second harmonic. Then, lines l_5 and l_6 are adjusted until the correct fundamental-frequency impedance is seen at the output of the transistor. Ideally, this circuit will not produce *any* second *or* third harmonic component at the output port.

It is not obvious that l_3 can simply be made shorter to compensate for the effects of lines l_1 and l_2 at the second harmonic. In practice, it has been found that it can be done. For example, for the case when all line impedances are 50Ω, the length of line l_3 is approximately 8° (Lines l_1 and l_2 are 30°, and line l_4 is 45°).

4.6 Harmonic content of switch voltage

The simplified analysis of the class-E circuit given above assumes a sinusoidal output signal at the load resistor R. In practice, some residual higher harmonic components will be present at the output of the circuit, depending upon the particular choice of load network topology and specific design values for the elements. In this section, the switch voltage $v_s(t)$ found above is analyzed using Fourier series, and expressions for the magnitude and phase of the harmonics of switch voltage are given. These general results can then be transformed through any specific load network to find explicit expressions for the harmonic content at the output of the class-E amplifier. Furthermore, it will be seen that a good approximation to class-E operation may be obtained with only two harmonics of the switch voltage waveform.

An expression for switch voltage $v_s(t)$ was derived earlier, and is repeated here:

$$(0 \leq (\omega_s t) \leq \pi): \quad v_s(t) = \frac{I_{ds}}{\omega_s C_s}((\omega_s t) + a(\cos((\omega_s t) + \phi) - \cos\phi)), \tag{4.41}$$

$$(\pi \leq (\omega_s t) \leq 2\pi): \quad v_s(t) = 0. \tag{4.42}$$

As before, the Fourier series is defined as

$$v_s(t) = \sum_{n=-\infty}^{\infty} K_n e^{jn\omega_s t}, \tag{4.43}$$

$$K_n = \frac{1}{T_s}\int_0^{T_s} v_s(t) e^{-jn\omega_s t}\, dt, \tag{4.44}$$

$$K_n = \frac{I_{ds}}{2\pi\omega_s C_s}\int_0^{\pi} ((\omega_s t) + a(\cos((\omega_s t) + \phi) - \cos\phi)) e^{-jn(\omega_s t)}\, d(\omega_s t). \tag{4.45}$$

Once again, the integration is only performed over the first half of the period, when $v_s(t)$ is nonzero, and $(\omega_s t)$ is used as the integration variable. The results are:

$$v_{sn}(t) = a_n I_{ds} \sin(\omega_s t + \phi_n), \tag{4.46}$$

$$a_n = \frac{2|K_n|}{I_{ds}}, \tag{4.47}$$

$$\phi_n = \frac{\pi}{2} + \angle K_n. \tag{4.48}$$

$$(n \text{ odd}, n \neq 1): \quad K_n = \frac{I_{ds}}{\pi\omega_s C_s}\left(-\frac{1}{n^2}\right), \tag{4.49}$$

$$(n \text{ even}, n \neq 0): \quad K_n = \frac{I_{ds}}{\pi\omega_s C_s}\left(\frac{2n + j\pi}{2n(1-n^2)}\right). \tag{4.50}$$

The special cases $(n = 1)$ and $(n = 0)$ were separately dealt with earlier; the results are repeated here:

$$(n = 1): \quad K_1 = \frac{I_{ds}}{\pi\omega_s C_s}\left(\frac{\pi^2}{8} - 1 - \frac{j\pi}{4}\right), \tag{4.51}$$

$$(n = 0): \quad V_{ds} = \frac{I_{ds}}{\pi\omega_s C_s}. \tag{4.52}$$

These expressions may be used to find the magnitude and phase of any number of harmonics of the ideal class-E switch voltage waveform. In Figure 4.11, for example, the first two harmonics of the switch voltage waveform are plotted along with the ideal waveform. It can be seen that only two harmonics of switch voltage give a reasonably close approximation to class-E operation. Therefore, the transmission-line class-E topologies presented earlier in this chapter are validated; they satisfy the class-E conditions at a finite number of harmonics.

4.7 Analysis of the effects of small switch ON-resistance

Although the class-E circuit has a maximum theoretical efficiency of 100 %, in practice microwave amplifiers fall short of this ideal case. For microwave class-E amplifiers using low-loss reactive elements (such as microstrip transmission lines), the primary loss occurs within the transistor itself. During the transistor OFF-state it looks primarily reactive (the intrinsic device looks like a capacitor at its output port, as

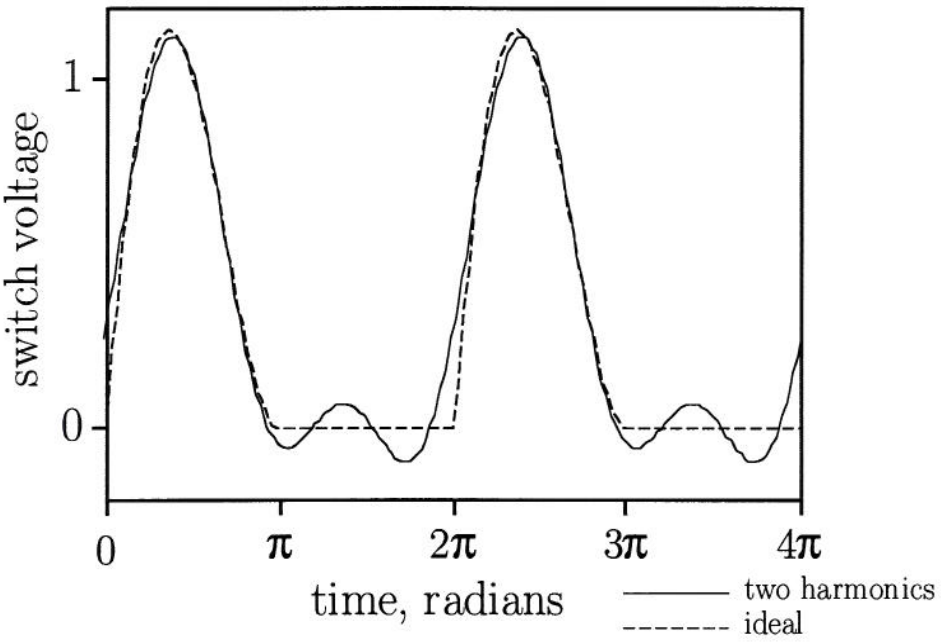


Figure 4.11. Two harmonics of the ideal switch voltage (solid line), plotted along with the ideal class-E switch voltage waveform (dashed line). It is seen that satisfying the class-E impedances at only two harmonics can give a reasonably close approximation to class-E operation.

shown in Figure 4.12). During the ON-state, the transistor looks like a small resistor, usually on the order of a few ohms (Figure 4.13). It is this ON-state resistance, which may be estimated from the MESFET's I-V curves, which is primarily responsible for its nonideal lossy behavior. In this section, the effects of this ON-state resistance R_s will be investigated. The transistor output port model used here is modified from the model proposed by Sokal and Redl [139].

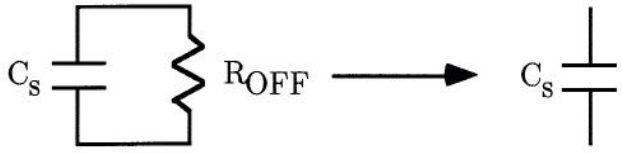


Figure 4.12. The intrinsic transistor output port during the OFF-state. It is assumed that the transistor output capacitance C_s dominates over its OFF-state resistance R_{OFF} during this half of the switching cycle $\left(R_{OFF} \gg \frac{1}{\omega_s C_s}\right)$. The transistor is represented by an OFF-state capacitance C_s.

As before, a sinusoidal load network current is assumed. During the switch ON-state, Ohm's law yields the switch voltage:

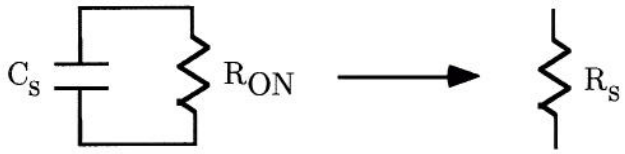


Figure 4.13. The intrinsic transistor output port during the ON-state. It is assumed that the transistor ON-state resistance R_{ON} dominates over its output capacitance C_s during this half of the switching cycle $\left(R_{ON} \ll \frac{1}{\omega_s C_s}\right)$. The transistor is therefore represented by an ON-state switching resistance R_s.

$$\left(\frac{T_s}{2} \leq t \leq T_s\right) \quad v_s(t) = R_s I_{ds}(1 - a_r \sin(\omega_s t + \phi_r)). \tag{4.53}$$

The boundary conditions for class-E operation are modified; the switch voltage may not be exactly zero at $t = 0$ and $t = \frac{T_s}{2}$, although the derivative of switch voltage is still constrained to be zero at $t = \frac{T_s}{2}$:

$$v_s(0) = v_s(T_s) = R_s I_{ds}(1 - a_r \sin \phi_r), \tag{4.54}$$

$$v_s\left(\frac{T_s}{2}\right) = R_s I_{ds}(1 + a_r \sin \phi_r), \tag{4.55}$$

$$\frac{dv_s}{dt}\left(\frac{T_s}{2}\right) = 0. \tag{4.56}$$

During the switch OFF-state,

$$\frac{dv_s}{dt} = \frac{I_{ds}}{C_s}(1 - a_r \sin(\omega_s t + \phi_r)). \tag{4.57}$$

Integrate:

$$v_s(t) = \frac{I_{ds}}{C_s}\int_0^t (1 - a_r \sin(\omega_s t' + \phi_r))dt' + R_s I_{ds}(1 - a_r \sin \phi_r), \tag{4.58}$$

where $v_s(0) = R_s I_{ds}(1 - a_r \sin \phi_r)$ to satisfy the $t = 0$ boundary condition determined by the switch ON-state previously. Evaluating the integral, it is found that

$$v_s(t) = \frac{I_{ds}}{\omega_s C_s}(\omega_s t + a_r(\cos(\omega_s t + \phi_r) - \cos \phi_r)) + R_s I_{ds}(1 - a_r \sin \phi_r). \tag{4.59}$$

Applying the two remaining boundary conditions, modified expressions for a_r and ϕ_r are found:

$$a_r \sin \phi_r = -1, \tag{4.60}$$

$$a_r \cos \phi_r = \frac{\pi}{2} + \omega_s C_s R_s, \tag{4.61}$$

$$a_r = \sqrt{1 + \left(\frac{\pi}{2} + \omega_s C_s R_s\right)^2}, \tag{4.62}$$

$$\phi_r = -\arctan\left(\frac{1}{\frac{\pi}{2} + \omega_s C_s R_s}\right). \tag{4.63}$$

When $\omega_s C_s R_s \ll \frac{\pi}{2}$, a_r and ϕ_r reduce to the constants found previously. Applying these expressions to the boundary conditions for $v_s(t)$, we get

$$v_s(0) = 2R_s I_{ds}, \tag{4.64}$$

$$v_s\left(\frac{T_s}{2}\right) = 0. \tag{4.65}$$

So the switch voltage is equal to zero at $t = \frac{T_s}{2}$, although it is clearly nonzero at $t = 0$. Now $v_s(t)$ is known over the entire period:

$$\left(0 \le t \le \frac{T_s}{2}\right): \quad v_s(t) = \frac{I_{ds}}{\omega_s C_s}(\omega_s t + a_r(\cos(\omega_s t + \phi_r) - \cos \phi_r)) + 2R_s I_{ds}, \tag{4.66}$$

$$\left(\frac{T_s}{2} \le t \le T_s\right): \quad v_s(t) = R_s I_{ds}(1 - a_r \sin(\omega_s t + \phi_r)). \tag{4.67}$$

To find the relationship between V_{ds} and I_{ds}, the DC component of $v_s(t)$ is evaluated:

$$V_{ds} = \frac{1}{T_s}\int_0^{T_s} v_s(t)dt. \tag{4.68}$$

Inserting the expressions for $v_s(t)$ into the above and simplifying, it is found that

$$\frac{V_{ds}}{I_{ds}} = \frac{1}{\pi\omega_s C_s} + 2R_s + \pi\omega_s C_s R_s^2. \tag{4.69}$$

To find the DC to RF conversion efficiency, a ratio of output (RF) power to input (DC) power must be found:

$$\eta = \frac{P_{outr}}{P_{inr}} = \frac{P_{outr}}{P_{out0}} \frac{P_{in0}}{P_{inr}}, \tag{4.70}$$

where P_{in0} and P_{out0} are the input and output power for the ideal class-E circuit ($P_{in0} = P_{out0}$), and P_{inr} and P_{outr} are the input and output powers for the class-E circuit analyzed in this section. The input (DC) power is determined by $V_{ds}I_{ds}$. The output (RF) power is proportional to a_r^2, the square of the magnitude of current flowing into the load network at the switching frequency.

$$\frac{P_{outr}}{P_{out0}} = \frac{a_r^2}{a_0^2}, \tag{4.71}$$

$$\frac{P_{in0}}{P_{inr}} = \frac{V_{g0}I_{g0}}{V_{g1}I_{g1}}. \tag{4.72}$$

Assuming a unit current is applied to both cases ($I_{g0} = I_{g1}$), an expression is found for DC to RF conversion efficiency (η_d):

$$\eta_d = \frac{1 + (\frac{\pi}{2} + \omega_s C_s R_s)^2}{(1 + \frac{\pi^2}{4})(1 + \pi\omega_s C_s R_s)^2}. \tag{4.73}$$

This expression for drain efficiency is plotted in Fig. 4.14 as a function of the product $\omega_s C_s R_s$. It can be seen in the plot that the product $\omega_s C_s R_s$ is indeed much less than one for a practical high-efficiency class-E circuit, validating the approximation made at the beginning of this section (see Figure 4.13). The efficiency analysis derived here is meant to be used in class-E circuits with efficiencies greater than approximately 60 %.

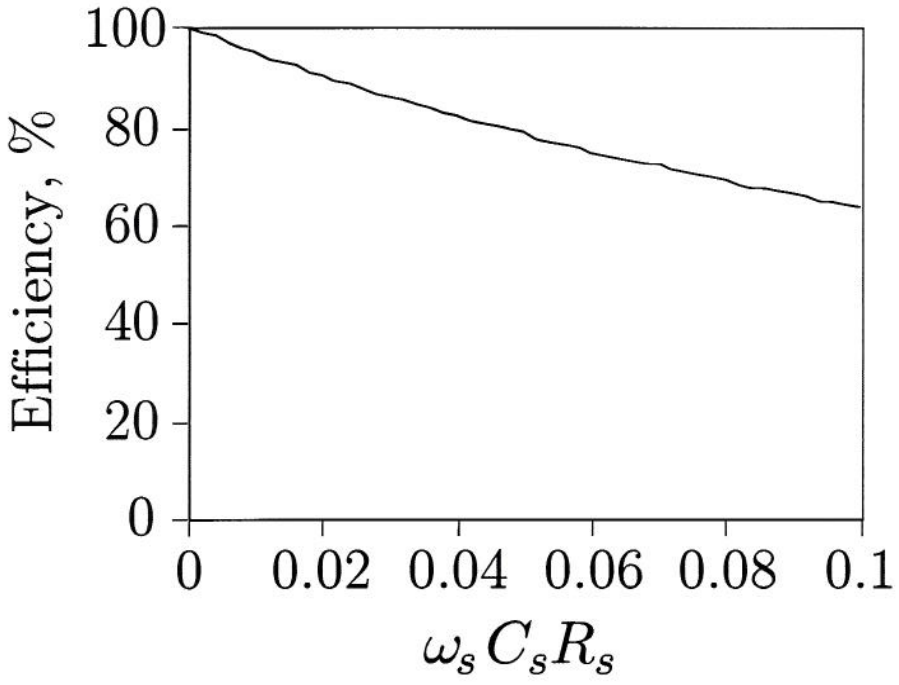


Figure 4.14. Drain efficiency as a function of the product $\omega_s C_s R_s$ for the class-E circuit, assuming sinusoidal load network current and assuming that the transistor looks capacitive during its OFF-state, and resistive during its ON-state.

For example, for the Siemens CLY5 MESFET considered previously, assume $C_s = 2.6pF$ and $R_s = 4\Omega$ under large-signal sinusoidal gate-source excitation. Using the above formula, the drain efficiency is calculated for this device at 0.5, 1.0, and 2.0 GHz. At 0.5 GHz, a drain efficiency of 85% is found. At 1.0 GHz, the efficiency drops to 73%. At 2.0 GHz, the expected drain efficiency is only 56%. These numbers are compared with experimental results in Chapter 5. Thus the analysis presented in this chapter demonstrates that the ON-state device output resistance is a primary source of power loss in the class-E circuit.

4.8 Analysis of the effects of nonlinear switch capacitance

Microwave devices, such as the Heterojunction Bipolar Transistor (HBT), exhibit nonlinearities in their parasitic output capacitance. The capacitor in parallel with the switch in a class-E circuit becomes nonlinear, which distorts the switch voltage waveform and affects the operation of the amplifier. In this section it is shown how

nonlinearities in the output capacitance of a transistor can be taken into account analytically, and closed-form expressions for the class-E circuit are found for some specific capacitance nonlinearities.

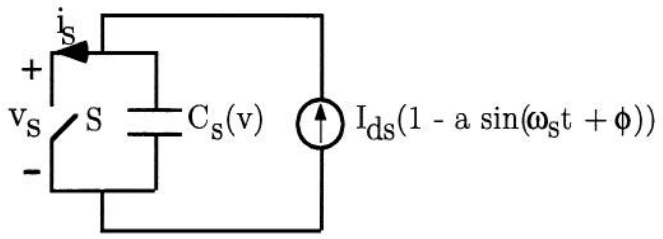


Figure 4.15. Class E circuit assuming sinusoidal load current with nonlinear switch capacitance $C_s(v)$.

To take nonlinearity of the switch capacitor C_s into account, the basic assumptions used in the previous analysis must be revisited. For example, the assumption of zero on-resistance and zero off-conductance will still be used for this first-order solution. The waveshaping elements still act as before, filtering the switch voltage and causing the output voltage and current across R to be sinusoidal. Also, as before, the total current flowing into the switched capacitor will be assumed to be sinusoidal, with arbitrary magnitude and phase, but with a known frequency and a DC offset equal to the supply current, I_{ds}. This is shown in Fig. 4.15. The shape of the switch voltage will differ from the linear case. The effects of this distortion are investigated here.

Modified design equations for load network elements will be found for a specific case of nonlinear capacitance, as well as a modified relationship between DC parameters I_{ds} and V_{ds}. The capacitance of a linear capacitor is defined by $C = \frac{Q}{V}$. Nonlinear capacitance parameters typically given in data sheets or in nonlinear circuit models use the definition $C(v) = \frac{dq}{dv}$ for nonlinear (voltage-dependent) capacitances present in a semiconductor device. This nonlinear capacitance can be determined using a small-signal (s-parameter) measurement, and this definition will be used here.

Rearrangement of the nonlinear capacitance definition yields

$$i = \frac{dq}{dt} = C(v)\frac{dv}{dt}. \tag{4.74}$$

Assume a capacitance-voltage characteristic

$$C_p(v_s) = C_m(1 + \frac{v_s}{V_m})^p. \tag{4.75}$$

For example, for a Gallium Arsenide Heterojunction Bipolar Transistor (HBT), $p \simeq -\frac{1}{3}$. The analysis from here parallels the linear case:

$$C_p(v_s)\frac{dv_s}{dt} = I_{ds}(1 - a\sin(\omega_s t + \phi)), \tag{4.76}$$

$$C_m(1 + \frac{v_s}{V_m})^p\frac{dv_s}{dt} = I_{ds}(1 - a\sin(\omega_s t + \phi)), \tag{4.77}$$

$$\int_0^{v_s}(1 + \frac{v'}{V_m})^p\,dv' = \frac{I_{ds}}{C_m}\int_0^t(1 - a\sin(\omega_s t' + \phi))\,dt'. \tag{4.78}$$

The above integral, as before, implicitly assumes that $v_s(0) = 0$. The three boundary conditions for class-E operation are the same as for the linear case. Two special cases result from solving for $v_s(t)$:

$$(p = -1) \qquad v_s(t) = V_m(e^{(\frac{I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)))} - 1), \tag{4.79}$$

$$(p \neq -1) \quad v_s(t) = V_m\left(\left(\frac{(1+p)I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)) + 1\right)^{\frac{1}{p+1}} - 1\right). \tag{4.80}$$

Notice that $(p = 0)$ gives the linear capacitance result, with $C_m = C_s$. The remaining two boundary conditions for class-E operation are

$$v_s\left(\frac{T_s}{2}\right) = 0, \tag{4.81}$$

$$\frac{dv_s}{dt}\left(\frac{T_s}{2}\right) = 0. \tag{4.82}$$

Adding the two above constraints, as before, a and ϕ are uniquely determined. Interestingly, it is found that a and ϕ for this nonlinear switched capacitor are the *same as for the linear case,* and they are *still constants regardless of* p.

$$a = \sqrt{1 + \frac{\pi^2}{4}} \simeq 1.862, \tag{4.83}$$

$$\phi = -\arctan\frac{2}{\pi} \simeq -32.48°. \tag{4.84}$$

Now the voltage and current flowing into the load network are known for arbitrary capacitor exponent p, and are summarized below:

$$(p = 0) \qquad v_s(t) = \frac{I_{ds}}{\omega_s C_s}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)), \tag{4.85}$$

$$(p = -1) \qquad v_s(t) = V_m(e^{(\frac{I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)))} - 1), \tag{4.86}$$

$$(p \neq -1) \quad v_s(t) = V_m\left(\left(\frac{(1+p)I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)) + 1\right)^{\frac{1}{p+1}} - 1\right), \tag{4.87}$$

$$(p_{any}) \qquad i_{net}(t) = I_{ds}(a\sin(\omega_s t + \phi) - 1). \tag{4.88}$$

Notice that the $(p \neq -1)$ equation reduces to the linear case, with $C_s = C_m$, when p is set to zero. Also, for any p, the nonlinear equations reduce to the linear case $(p = 0)$ for a sufficiently low supply current I_{ds}. For example, when $|p| \leq 1$, and $\left(\frac{I_{ds}}{\omega_s C_m V_m}\right) \ll 1$, the equation for v_s approaches the linear equation $(p = 0)$.

4.9 Relation between V_{ds} and I_{ds} for nonlinear C_s

The relationship between V_{ds} and I_{ds} involves the integral of the switch voltage over half of a period. This integral is not straightforward, but can be solved for the cases $(p = -\frac{1}{2})$ and $(p = -\frac{2}{3})$. Here the case $(p = -\frac{1}{2})$ is considered, which corresponds to

$$C_s(v) = \frac{C_m}{\sqrt{1 + \frac{v_s}{V_m}}}. \tag{4.89}$$

The DC component of the switch voltage $v_s(t)$ is the supply voltage V_{ds}:

$$\left(p = -\frac{1}{2}\right)\ V_{ds} = \frac{V_m}{T_s}\int_0^{\frac{T_s}{2}} \left(\left(\frac{I_{ds}}{2\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t + \phi) - \cos\phi)) + 1\right)^2 - 1\right) dt. \tag{4.90}$$

Solving the above integral, and rearranging the result, a relationship between I_{ds} and V_{ds} is found:

$$\left(\left(\frac{I_{ds}}{\omega_s C_m V_m}\right)\left(\frac{5\pi^3}{192} - \frac{3\pi}{16}\right) + 1\right) I_{ds} = \pi\omega_s C_m V_{ds}. \tag{4.91}$$

For low operating current, when $\left(\frac{I_{ds}}{\omega_s C_m V_m}\right) \ll \left(\frac{5\pi^3}{192} - \frac{3\pi}{16}\right)$, the linear result $I_{ds} = \pi\omega_s C_m V_{ds}$ is obtained, and the supply voltage V_{ds} is in proportion to I_{ds}. For large operating currents, when $\left(\frac{I_{ds}}{\omega_s C_m V_m}\right) \gg \left(\frac{5\pi^3}{192} - \frac{3\pi}{16}\right)$, the supply voltage V_{ds} increases as the square of the supply current I_{ds}.

4.10 Equivalent linear capacitance for nonlinear Cs

To define an "equivalent linear capacitance" for a given nonlinear capacitor at a given power level for class-E operation, charge flow equations are used. By the definition of nonlinear capacitance used here, $dq = C_p(v)\,dv$. Integrating both sides from the start of the switch OFF period to the time of maximum switch voltage yields

$$Q_{max} = \int_0^{v_{pmax}} C_p(v)\,dv. \tag{4.92}$$

Notice that Q_{max} does not depend upon the capacitance $C_p(v)$; it is determined by the current $I_{ds}(1-a\sin(\omega_s t+\phi))$ (a and ϕ do not depend upon $C_p(v)$). The maximum capacitor voltage, v_{pmax}, *will* depend upon $C_p(v)$. For the linear case,

$$Q_{max} = C_s V_{0max}. \tag{4.93}$$

Since the total charge Q_{max} is equal in both the linear and nonlinear cases, the two expressions can be equated, yielding an expression for an "equivalent linear capacitance" for the nonlinear case, based upon charge equivalence arguments:

$$C_s = \frac{1}{V_{0max}} \int_0^{V_{pmax}} C_p(v)\, dv. \tag{4.94}$$

For the special case $C_p(v) = C_m \left(1 + \frac{v}{V_m}\right)^p$ considered here, evaluation of the above yields

$$(p \neq -1) \qquad C_s = \frac{C_m V_m}{V_{0max}(p+1)} \left(\left(1 + \frac{V_{pmax}}{V_m}\right)^{p+1} - 1 \right). \tag{4.95}$$

The special case $(p = -1)$ is not encountered in practice, and will not be considered here.

It is necessary to find expressions for V_{0max} and V_{pmax}, the maximum capacitor voltage during the switch "OFF" state. It is known that the capacitor voltage rises monotonically from 0 to its maximum voltage when current flows into it, and then decreases monotonically back to zero when current flows out of it. Therefore, the time of maximum switch voltage is when the *current* is zero, which is *independent of the capacitor nonlinearity*:

$$\frac{t_{max}}{T_s} = \frac{1}{\pi} \arctan\left(\frac{2}{\pi}\right) \simeq 0.1805. \tag{4.96}$$

Inserting the time of maximum switch voltage into the expression for $v_p(t)$, an expression for V_{pmax} is found:

$$\frac{V_{pmax}}{V_m} = \left(\frac{2(1+p) I_{ds}}{\omega_s C_m V_m} \arctan\left(\frac{2}{\pi}\right) + 1 \right)^{\frac{1}{p+1}} - 1. \tag{4.97}$$

Setting $(p = 0)$ in the above expression gives an expression for V_{0max} as well. Inserting V_{0max} and V_{pmax} into the above expression for equivalent linear capacitance C_s and simplifying, it is found that

$$|Z_{C_s}| = \pi \frac{V_{ds}}{I_{ds}} \tag{4.98}$$

$$C_s = \frac{I_{ds}}{\pi \omega_s V_{ds}}. \tag{4.99}$$

Once an expression is found relating V_{ds} and I_{ds} for a given nonlinear capacitor, an equivalent capacitance C_s can be defined. For example, in section 4.9, a relationship between V_{ds} and I_{ds} was found for the case ($p = -\frac{1}{2}$). Inserting that result into the above,

$$\left(p = -\frac{1}{2}\right) \qquad C_s = \frac{C_m}{1 + \frac{I_{ds}}{\omega_s C_m V_m}\left(\frac{5\pi^3}{192} - \frac{3\pi}{16}\right)}. \tag{4.100}$$

This "equivalent linear capacitor" is useful for DC arguments only; unfortunately, it cannot be used in the equations derived earlier to find load network elements. It only relates DC currents and voltages in the class-E circuit. Due to the capacitor nonlinearity, the RF voltages and currents are not related to the DC parameters the same way they are related in the linear case. However, using the equivalent linear capacitance expression above, the same supply voltage, supply current, and operating power level will occur. For example, in Figure 4.16, the switch voltage waveform is plotted for a linear output capacitance ($p = 0$), and for a nonlinear output capacitance ($p = -\frac{1}{2}$). The supply voltage and supply current are the same in both cases, but the peak voltage stress placed upon the switch is 28 % higher for the nonlinear case. Thus it can be seen that nonlinear output capacitance places higher peak stresses upon a transistor for the same output power level.

4.11 Modified load network design equations for nonlinear C_s

To find modified load network design equations for the case of nonlinear output capacitance, the same Fourier series approach as before can be applied to $v_s(t)$, to find the fundamental frequency component of the switch voltage for the nonlinear capacitor case of the class-E circuit. As before, the network is an open circuit for all higher harmonic frequencies (no power will flow into R, except at the fundamental frequency), and the phasor voltages for v_{s1} and i_{net1} can be found, leading to modified design equations. As before,

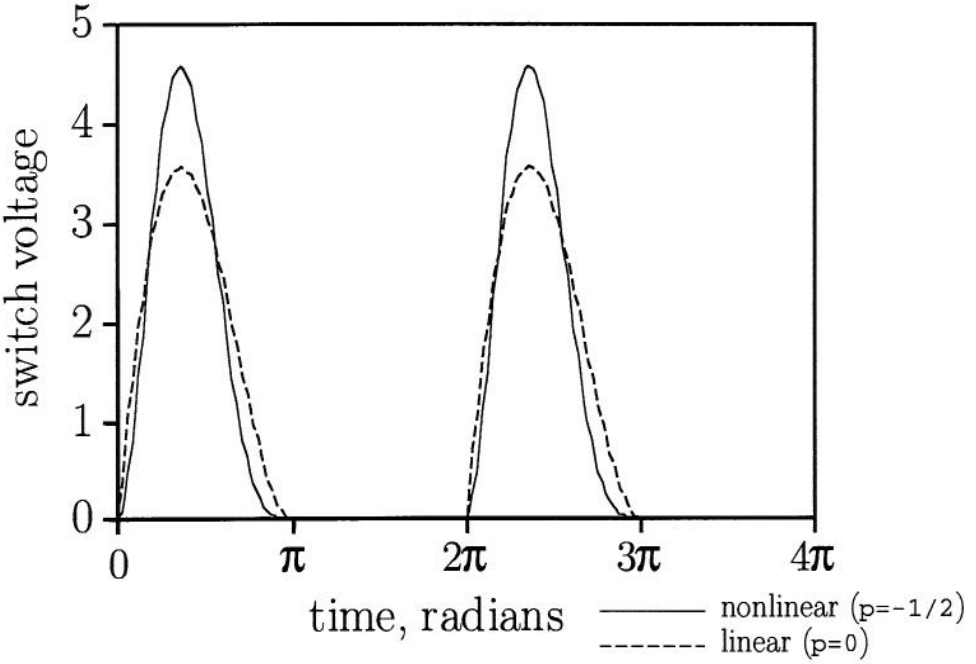


Figure 4.16. Ideal class-E switch voltage waveform, for a nonlinear output capacitance with (p=-1/2) (solid line), plotted along with the ideal class-E switch voltage waveform for a linear output capacitance (dashed line). The linear output capacitance was replaced with an "equivalent" nonlinear output capacitance, so that the same supply voltage and operating power level occurs in both cases. The supply voltage is 1 V in both cases. The peak voltage stress placed upon the switch is 28 % higher for the nonlinear case.

$$v_p(t) = \sum_{n=-\infty}^{\infty} K_n e^{jn\omega_s t}, \tag{4.101}$$

$$K_n = \frac{1}{T_s}\int_0^{\frac{T_s}{2}} v_p(t) e^{-jn\omega_s t}\, dt, \tag{4.102}$$

$$(p=-1) \qquad K_1 = \frac{V_m}{T_s}\int_0^{\frac{T_s}{2}} (e^{\left(\frac{I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t+\phi)-\cos\phi))\right)} - 1)e^{-j\omega_s t}\, dt, \tag{4.103}$$

$$(p \neq -1)$$
$$K_1 = \frac{V_m}{T_s}\int_0^{\frac{T_s}{2}} \left(\left(\frac{(1+p)I_{ds}}{\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t+\phi)-\cos\phi)) + 1\right)^{\frac{1}{p+1}} - 1\right) e^{-j\omega_s t}\, dt. \tag{4.104}$$

Again, the integral is taken over only half of the period because the switch voltage is zero over the second half. For the special case ($p = 0$), the rest of the analysis has already been performed (the linear C_s case). The above integrals are difficult to solve analytically, except for a few special cases, such as $\left(p = -\frac{1}{2}\right)$ and $\left(p = -\frac{2}{3}\right)$. The analysis will proceed for the special case $\left(p = -\frac{1}{2}\right)$, which corresponds to

$$C_s(v_s) = \frac{C_m}{\sqrt{1+\frac{v_s}{V_m}}}, \tag{4.105}$$

$$\left(p = -\frac{1}{2}\right)$$
$$K_1 = \frac{V_m}{T_s}\int_0^{\frac{T_s}{2}} \left(\left(\frac{I_{ds}}{2\omega_s C_m V_m}(\omega_s t + a(\cos(\omega_s t+\phi)-\cos\phi)\right) + 1)^2 - 1\right) e^{-j\omega_s t}\, dt. \tag{4.106}$$

The calculations are very tedious, and only the results are presented:

$$v_{s1} = a_2 I_{ds}\sin(\omega_s t + \phi_2), \tag{4.107}$$

where

$$a_2 = \frac{2|K_1|}{I_{ds}} = \frac{1}{\omega_s C_m}\sqrt{\left(-\frac{2}{\pi}+\frac{\pi}{4}+\frac{I_{ds}}{\omega_s C_m V_m}\frac{1}{24}\right)^2+\left(-\frac{1}{2}+\frac{I_{ds}}{\omega_s C_m V_m}\left(\frac{2}{3\pi}-\frac{5\pi}{48}\right)\right)^2}, \tag{4.108}$$

$$\phi_2 = \frac{\pi}{2}+\angle K_1 = \frac{\pi}{2}+\arctan\left(\frac{-\frac{1}{2}+\frac{I_{ds}}{\omega_s C_m V_m}\left(\frac{2}{3\pi}-\frac{5\pi}{48}\right)}{-\frac{2}{\pi}+\frac{\pi}{4}+\frac{I_{ds}}{\omega_s C_m V_m}\frac{1}{24}}\right). \tag{4.109}$$

The phasor impedance of the external load network is

$$Z_{net1} = \frac{a_2}{a}e^{j(\phi_2-\phi)}. \tag{4.110}$$

This complex impedance is now equated to the load network impedance at the fundamental switching frequency to solve for load network element values. The design equations derived in the previous sections for the different topologies are identical, except that k_0 and θ_0 are modified in those expressions; now k_2 and θ_2 are used instead.

$$k_2 = \omega_s C_m \frac{a_2}{a}, \tag{4.111}$$

$$\theta_2 = \phi_2 - \phi. \tag{4.112}$$

CHAPTER 5

EXPERIMENTAL VERIFICATION OF THE CLASS-E APPROACH

5.1 Introduction

In Chapter 4, the microwave class-E circuit was presented, and various aspects of its operation and properties were analyzed. In this chapter, experimental verification of the class-E approach is provided, using the Siemens CLY5 MESFET in a microstrip transmission-line environment, at 0.5, 1, and 2 GHz. The series/shunt transmission-line class-E circuit is implemented, and the equations derived in Chapter 4 are used for the designs in this chapter. Experimental results are compared to analysis and harmonic-balance computer circuit simulations. Table 5.1 summarizes the experimental results from this chapter, and compares the measured drain efficiencies and output powers to the analytical equations presented in Chapter 4. Further explanation for the individual cases are given below.

Table 5.1. Summary of results for the 0.5, 1, and 2 GHz microstrip class-E amplifiers using the Siemens CLY5 MESFET.

Frequency	**0.5 GHz**	**1.0 GHz**	**2.0 GHz**
$\text{Gain}_{\text{meas}}$	15.3 dB	14.7 dB	9.1 dB
PAE_{meas}	80 %	73 %	54 %
$\eta_{\text{d pred}}$	85 %	73 %	56 %
$\eta_{\text{d meas}}$	83 %	75 %	62 %
$P_{\text{out pred}}$	0.77 W	1.35 W	2.07 W
$P_{\text{out meas}}$	0.55 W	0.94 W	0.53 W

5.2 Experimental class-E circuit at 0.5 GHz

A 0.5 GHz class-E circuit using the above series/shunt transmission-line topology was designed, fabricated and tested. The Siemens CLY5 MESFET was used in a microstrip transmission-line circuit. The layout of the circuit is shown in Fig. 5.1, and

its equivalent transmission-line circuit is shown in Fig. 5.2. The equations derived in Chapter 4 were used for the first-pass design of the single-stub high-efficiency output circuit, using an approximate switch capacitance of 2.4 pF (from C_{ds} of a Materka non-linear transistor model of this device provided by Compact Software). The first-pass design of the input matching circuit was done using s-parameters for the CLY5 with the above output circuit attached to the drain of the device on a linear circuit simulator. The bias to the device was provided through quarter-wavelength capacitively shorted stubs, attached to points in the circuit where only fundamental-frequency sinusoidal voltages would be expected. The microstrip lines were all 50Ω (about 2.3 mm wide), and the substrate was 2.54 mm thick Duroid, with $\epsilon_r = 10.5$. The final microstrip line lengths are labeled in Fig. 5.1.

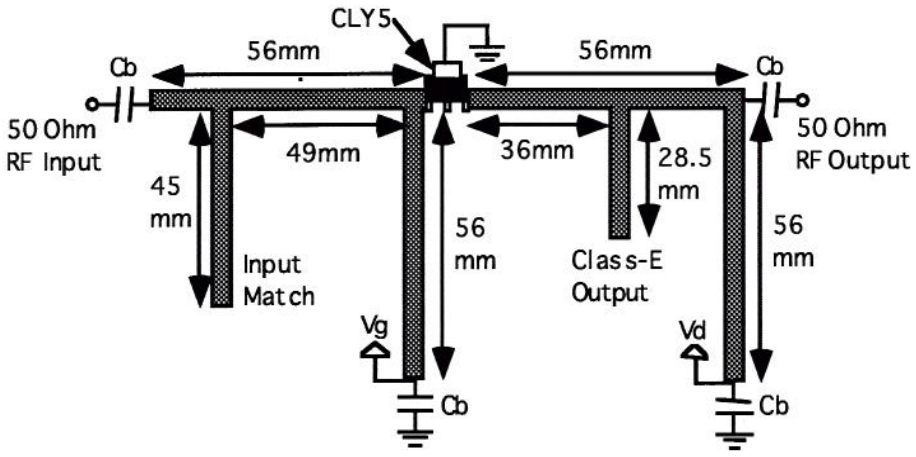


Figure 5.1. Microstrip layout of the 0.5 GHz class-E circuit, using the CLY5. Bias was brought in through quarter-wave shorted stubs. A Duroid substrate was used, with a thickness of 2.54 mm and $\epsilon_r = 10.5$.

In the lab, the device was heavily saturated, and the input and output circuits were adjusted experimentally until the maximum power-added-efficiency was obtained. A maximum power-added efficiency of 80 % was measured at 0.5 GHz at an output power of 550 mW and a gain of 15.3 dB. The drain efficiency was 83 %. After this performance was experimentally obtained (similar to a load-pull measurement), a series inductance was included in the transistor switch model; this inductance appears between

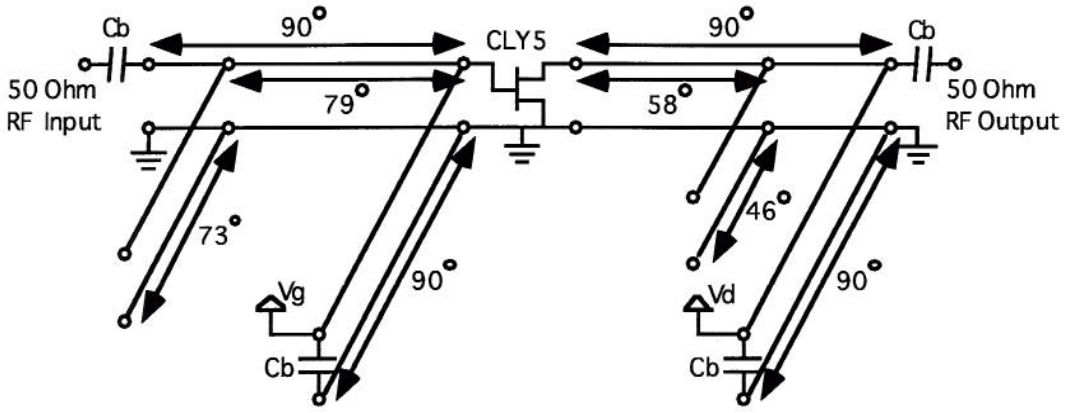


Figure 5.2: Equivalent circuit of the 0.5 GHz class-E circuit, using the CLY5.

the switched capacitor and the series transmission line in Fig. 4.7, and can be compensated for by shortening the series section of line. From the same Materka model used above, this inductance was estimated to be 1.7 nH. On a linear circuit simulator, the load network impedance seen by the switched capacitor at the fundamental frequency was determined, using the experimentally determined transmission-line lengths of the class-E circuit, and the lead inductance estimated from the Materka model. The load network impedance of the experimentally-adjusted circuit, assuming a lead inductance of 1.7 nH, is

$$Z_{net1} = 34.3e^{j51^\circ}\Omega.$$

It was found earlier that the impedance of the load network at the fundamental frequency of operation for the ideal class-E circuit is

$$Z_{net1} = \frac{0.28015}{\omega_s C_s} e^{j49.0524^\circ}\Omega.$$

The experimentally determined load angle is close to that expected for the ideal class-E circuit. Equating the magnitude of the measured load network impedance to that expected for an ideal class-E circuit yields $C_s = 2.6\,\text{pF}$, which is close to the value found in the Materka model. Therefore, it was discovered that a lead inductance of 1.7 nH must be included into the class-E circuit switch model to obtain an optimum class-E design using the Siemens CLY5 MESFET. This modified transistor output port model was used in the later designs.

The magnitudes of s_{11} and s_{21} were measured under small-signal and large-signal conditions, shown in Fig. 5.3. The input match shifted in frequency under large-signal gate drive; the circuit's input match was adjusted under large-signal conditions for this reason. Also, the magnitude of s_{21} was saturated by 4.7 dB at 0.5 GHz under large-signal gate drive. At this power level the amplifier operated at the maximum power-added efficiency of 80 %. The output power, drain efficiency and power-added-efficiency are plotted as a function of frequency in Fig. 5.4. The efficiency is high over a relatively broad frequency range. For example, the power-added-efficiency remains above 75 % over a 10 % bandwidth, and it remains above 50 % over a 26 % bandwidth. The output power, drain efficiency, and power-added-efficiency are plotted as a function of input power level in Fig. 5.5. The efficiency is high over a broad input power range; however, the output power is mostly constant over this range. Therefore, this class-E circuit is unsuitable for amplitude modulation of the input signal at maximum efficiency operation, although it is well-suited for frequency modulation because the amplitude is relatively constant when the frequency is varied.

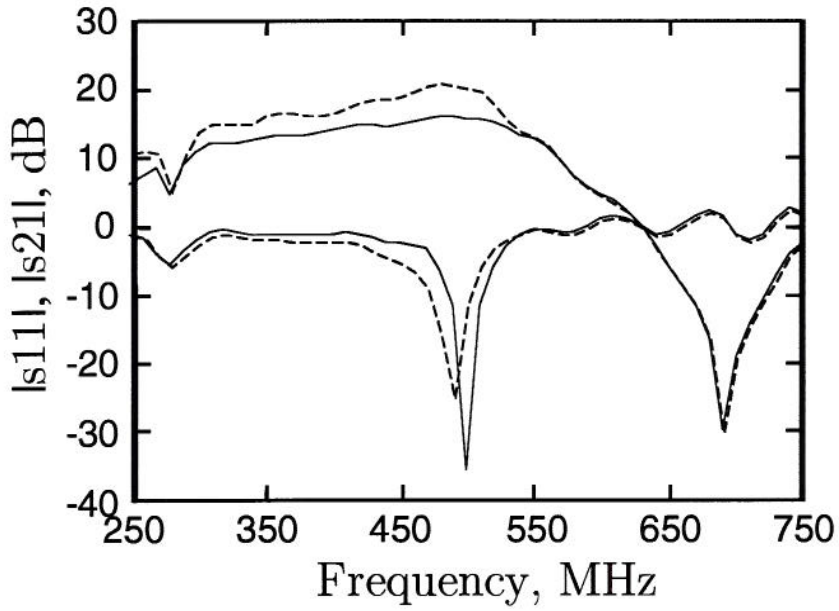


Figure 5.3. Magnitude of s11 and s21 for the 0.5 GHz CLY5 class-E amplifier under small-signal (dashed lines) and large-signal (solid lines) conditions.

In chapter 4, an expression was found relating the DC supply voltage and supply

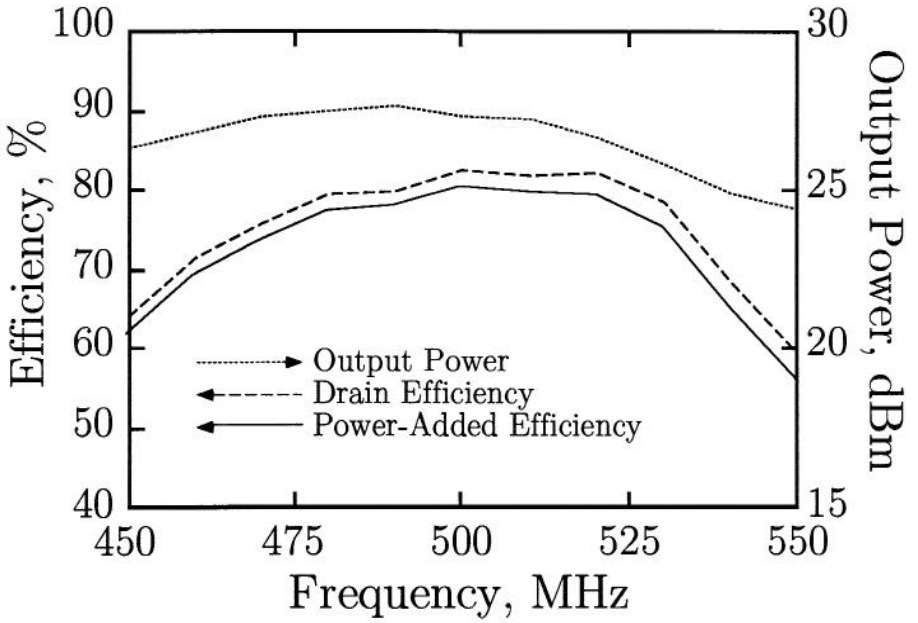


Figure 5.4. Output power (dotted line), power-added efficiency (solid line) and drain efficiency (dashed line) of the 0.5 GHz CLY5 class-E amplifier as a function of frequency under large-signal gate drive conditions.

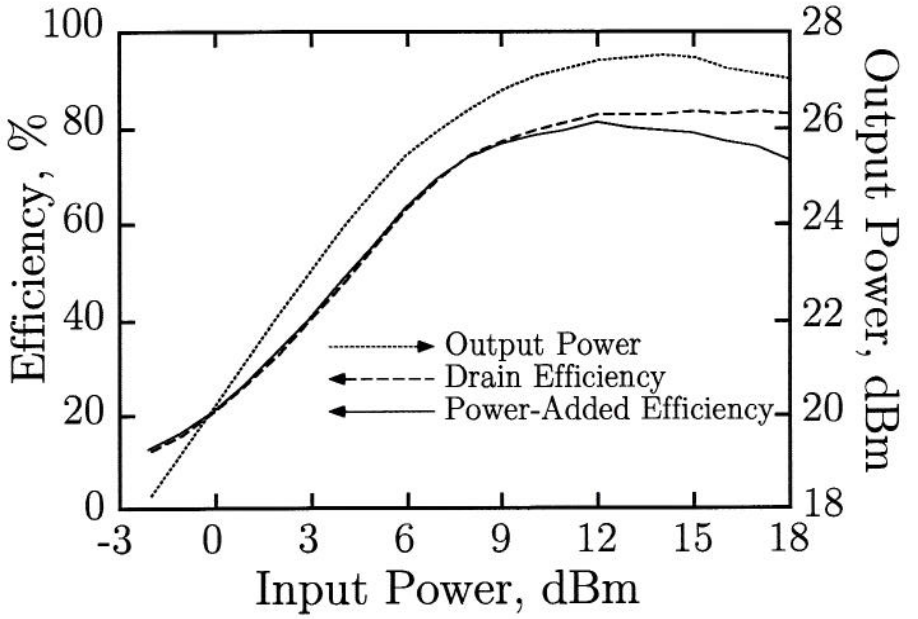


Figure 5.5. Output power (dotted line), power-added-efficiency (solid line), and drain efficiency (dashed line) as a function of gate input drive level for the 0.5 GHz CLY5 class-E amplifier.

current for the class-E circuit:

$$I_g = \pi\omega_s C_s V_g.$$

Multiplying the above expression by V_g, an expression for operating power level is found:

$$P_{DC} = \pi\omega_s C_s V_g^2.$$

For the circuit presented above, $V_g = 6\,\mathrm{V}$, $C_s = 2.6\,\mathrm{pF}$, and the frequency is 0.5 GHz. According to the above expression, therefore, $P_{DC} = 924\,\mathrm{mW}$. The measured DC power is 666 mW. The discrepancy between the expected and the measured DC power levels may be due to the equivalent ON-state resistance of the MESFET, which is primarily responsible for the non-ideal efficiency of 80 % for the amplifier. Some of the supply voltage V_g is dropped through this resistance, which also causes the supply current to drop in proportion to the supply voltage. Thus the real circuit operates at a lower power level than is expected from an ideal class-E circuit.

5.3 Measurement of the CLY5 MESFET drain-source voltage

The Hewlett-Packard HP71500A/HP70820A Transition Analyzer is capable of reconstructing a time waveform of a periodic microwave signal. To verify that the 0.5 GHz amplifier (Fig. 5.1) operates in class-E mode, the Transition Analyzer was used to measure the drain-source voltage of the MESFET. The measured voltage is shown in Fig. 5.6.

To probe the MESFET's drain-source voltage, a 400-Ω chip resistor was soldered from the MESFET drain lead to a 50-Ω microstrip transmission line, which was then coupled to the 50-Ω coaxial input port of the Transition Analyzer. Electrically, a 450-Ω resistance was presented to the MESFET across its drain and source terminals. Harmonic-balance circuit simulations showed that this resistance would not affect the amplifier's operation appreciably. The MESFET's drain-source voltage was then divided between the 400-Ω chip resistor and the 50-Ω Transition Analyzer input port, a frequency-independent ratio of 9:1. The measured waveform is only approximate; the chip resistors and the MESFET both have parasitic inductances which affect the

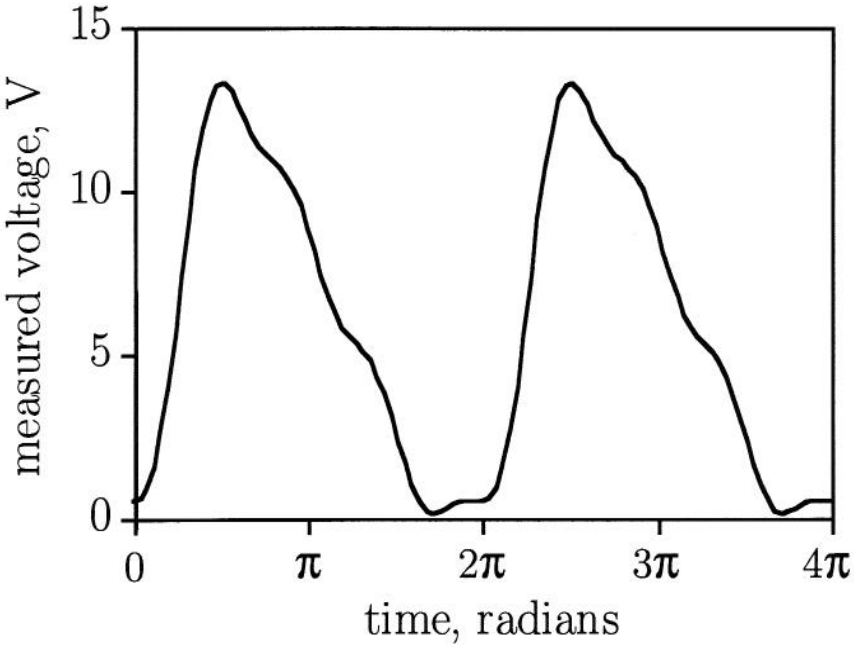


Figure 5.6. Measured drain-source voltage of the CLY5 MESFET operating in class-E mode in the 0.5 GHz amplifier presented in section 5.2.

measurement. However, the waveform shown in Fig. 5.6 shows the general class-E properties described in Chapter 4; the slope of the switch voltage is steeper when it rises than when it falls back to zero (see Fig. 5.15 for comparison).

5.4 Experimental class-E circuit at 1 GHz

The microstrip layout of the 1 GHz class-E circuit using the Siemens CLY5 is shown in Fig. 5.7, and its equivalent circuit is shown in Fig. 5.8. From the above experiment, the simple switched-capacitor MESFET output port model was extended to include a series inductance. For the 1 GHz circuit design, a switch capacitance of 2.6 pF and a series inductance of 1.7 nH were used to design the output circuit, such that the correct class-E load network impedance would be seen by the switched capacitor inside the MESFET. No adjustment was done on the output circuit this time; only the input circuit was adjusted for minimum return loss. Bias tees were used to provide DC power to the MESFET. A Duroid substrate was used, with a thickness of 0.787 mm and $\epsilon_r = 2.2$. The dimensions of the microstrip lines are labeled in Fig. 5.7.

A maximum power-added efficiency of 73 % was measured at 1 GHz with 935 mW

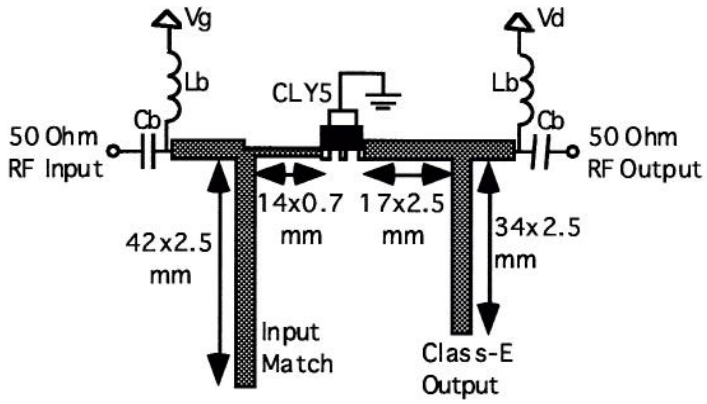


Figure 5.7. Microstrip layout of the 1 GHz class-E circuit, using the CLY5. External bias tees were used to power the circuit. A Duroid substrate was used, with a thickness of 0.787 mm and $\epsilon_r = 2.2$.

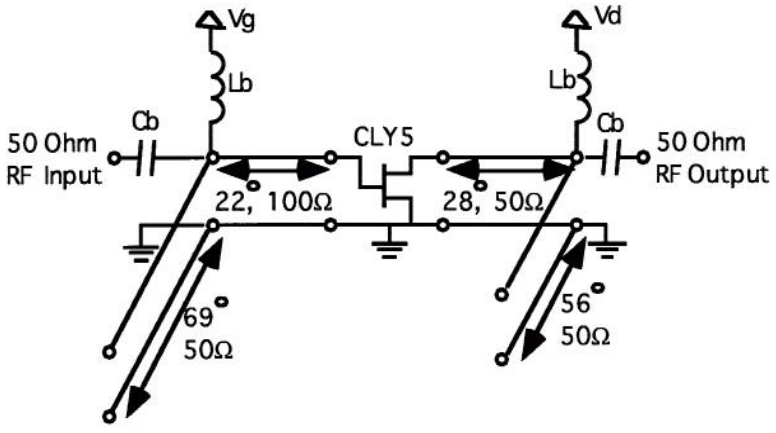


Figure 5.8: Equivalent circuit of the 1 GHz class-E circuit, using the CLY5.

of output power and 14.7 dB of gain. The drain efficiency was 75 %. Output power, drain efficiency and power-added-efficiency are plotted as a function of frequency in Fig. 5.9. The power-added efficiency is greater than 65 % over a 12 % bandwidth. Output power, drain efficiency and power-added-efficiency are also plotted as a function of input power level in Fig. 5.10. Again, this circuit is suitable for frequency modulation but not for amplitude modulation.

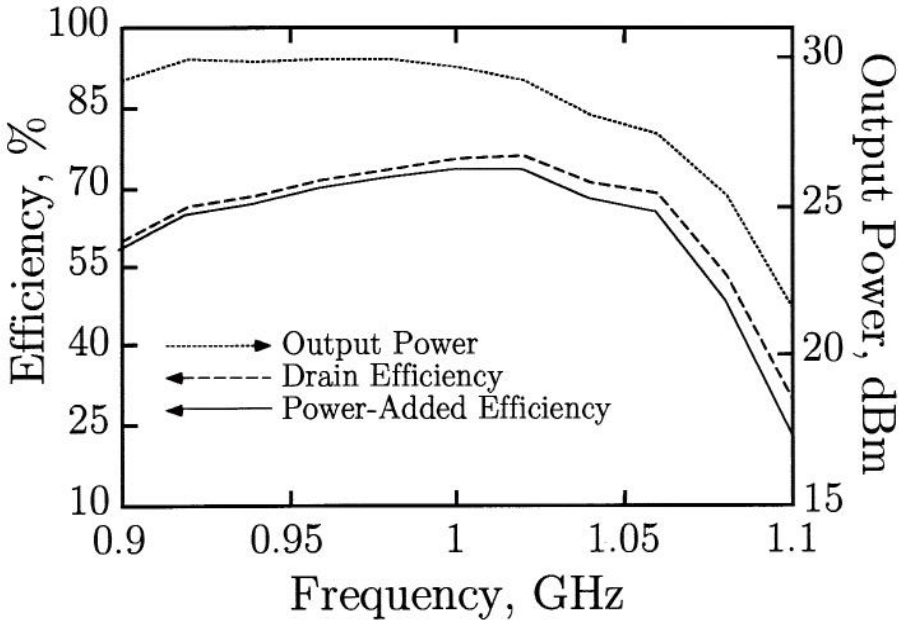


Figure 5.9. Output power (dotted line), power-added-efficiency (solid line), and drain efficiency (dashed line) of the 1 GHz CLY5 class-E amplifier as a function of frequency under large-signal gate drive conditions.

The DC power level of the ideal class-E circuit is proportional to the switching frequency if the supply voltage and switch capacitance are held constant:

$$P_{DC} = \pi \omega_s C_s V_g^2.$$

For the 0.5 GHz CLY5 class-E circuit, the DC power level was 666 mW. For this 1 GHz CLY5 class-E circuit, the DC power level is 1244 mW. The ratio between the two power levels is 1.87; in the ideal case, the ratio should be 2.

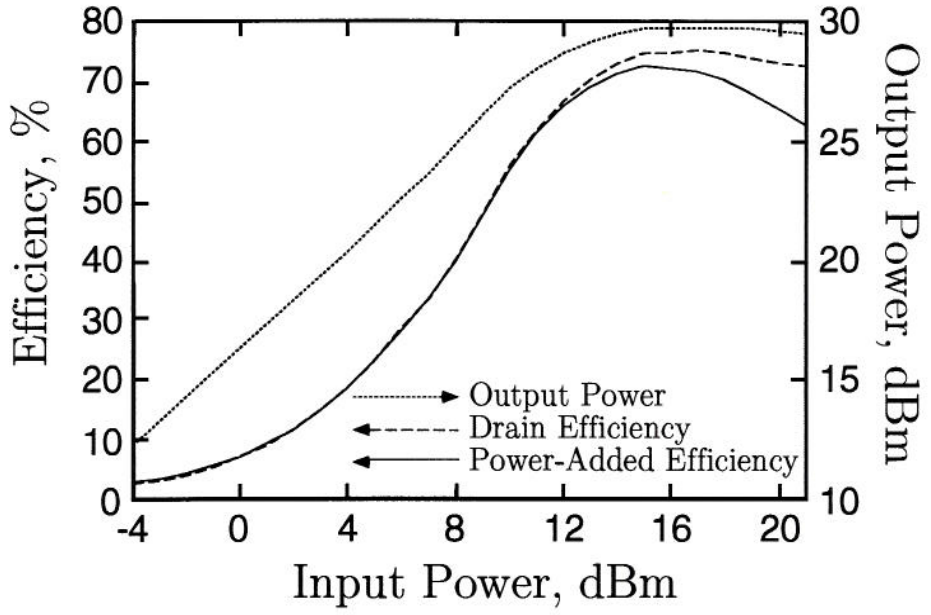


Figure 5.10. Output power (dotted line), power-added-efficiency (solid line), and drain efficiency (dashed line) as a function of gate input drive level for the 1 GHz CLY5 class-E amplifier.

5.5 Experimental class-E circuit at 2 GHz

The microstrip layout of the 2 GHz class-E circuit using the Siemens CLY5 is shown in Fig. 5.11, and its equivalent circuit is shown in Fig. 5.12. A switch capacitance of 2.6 pF and a series inductance of 1.7 nH were used to design the output circuit, such that the correct class-E load network impedance would be seen by the switched capacitor inside the MESFET. At this frequency, no additional series transmission-line was needed between the series inductance and the shunt transmission-line stub. Also, no adjustment was done on the output circuit; only the input circuit was adjusted for minimum return loss. Bias tees were used to provide DC power to the MESFET. A Duroid substrate was used, with a thickness of 0.787 mm and $\epsilon_r = 2.2$. The dimensions of the microstrip lines are labeled in Fig. 5.11.

A maximum power-added efficiency of 54 % was measured at 2 GHz with 530 mW of output power and 9.1 dB of gain. The drain efficiency was 62 %. The broadband sweeper available for this measurement only provided enough power to moderately saturate the transistor (to about 30 % efficiency). A high-power narrowband amplifier

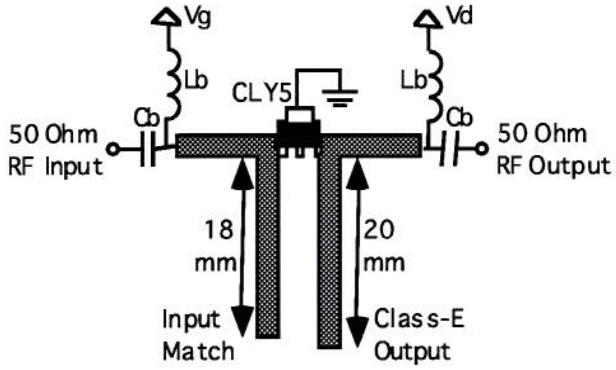


Figure 5.11. Microstrip layout of the 2 GHz class-E circuit, using the CLY5. External bias tees were used to power the circuit. A Duroid substrate was used, with a thickness of 0.787 mm and $\epsilon_r = 2.2$.

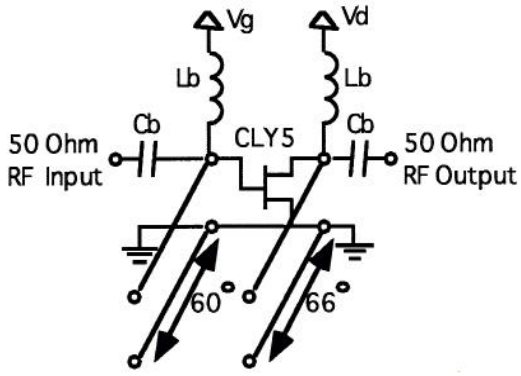


Figure 5.12: Equivalent circuit of the 2 GHz class-E circuit, using the CLY5.

was used to saturate the class-E circuit to find output power and efficiency as a function of input power. Efficiency as a function of frequency was not measured due to the narrowband nature of the preamplifier. Output power, drain efficiency and power-added-efficiency are plotted as a function of input power level in Fig. 5.13.

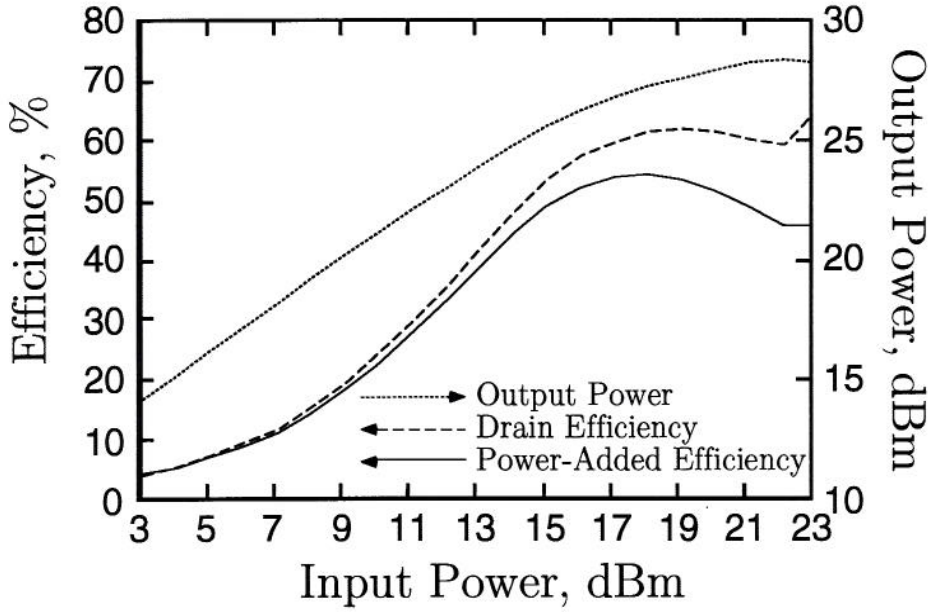


Figure 5.13. Output power (dotted line), power-added-efficiency (solid line), and drain efficiency (dashed line) as a function of gate input drive level for the 2 GHz CLY5 class-E amplifier.

In chapter 4, a maximum frequency of class-E operation was found for a given transistor's output capacitance and maximum current-carrying capability, I_{max}. The expression is repeated here:

$$f_{max} = \frac{I_g}{2\pi^2 C_s V_g} = \frac{I_{max}}{2\pi^2(1+a)C_s V_g} \simeq \frac{I_{max}}{56.5 C_s V_g},$$

where $a \simeq 1.8621$. For the class-E circuits considered here, the supply voltage is 6 V, and the output capacitance was found to be about 2.6 pF. From the transistor I_{ds}-V_{ds} curves given in the manufacturer's data sheets, the maximum drain current for the Siemens CLY5 is approximately 1.2 A (when the gate voltage is slightly positive). This yields a maximum frequency of "ideal" class-E operation of approximately 1.4 GHz. Therefore, the 2 GHz class-E circuit presented here operates in a "suboptimum" class-E mode. The class-E circuit demands a higher peak drain current than the MESFET can provide.

This may explain why the output power level is much lower than expected at this frequency, and why the efficiency drops so suddenly between the switching frequencies of 1 GHz and 2 GHz. Despite this problem, it is advantageous to operate the 2 GHz class-E circuit at 6 V rather than a lower supply voltage. This is because the gain of the MESFET decreases rapidly at lower drain voltages, and the gain is already low enough that the input power is a significant fraction of the output power (which affects power-added-efficiency directly).

5.6 Harmonic balance circuit simulations using an ideal switch model

The output circuits of the transmission-line class-E amplifiers presented in this chapter are represented by the general circuit shown in Fig. 5.14. The CLY5 MESFET's output port is represented by an ideal switch, with parasitics R_s, C_s, and L_s shown in the figure. Ideally, only the lengths of lines l_3 and l_4 should change to reflect the class-E impedance conditions at 0.5, 1, and 2 GHz. Of course, the switch model is simplified, since in practice the transistor has more complicated mechanisms governing its exact operation. To verify the validity of using this approximate MESFET output port model, harmonic-balance circuit simulations were performed on the three class-E circuits (five harmonics were used in the analysis).

Unfortunately, an ideal switch model was not available on the harmonic balance circuit simulation software. Therefore, an approximate switch was created by modifying the Materka nonlinear MESFET transistor model on Compact Software's Harmonica program [140]. All parameters in the model were set to 0 (all parasitic capacitances and inductances, for example), except for the following: $I_{dss} = 100$ Amps, $V_{po} = -5$ Volts, $V_{gmn} = -10$ Volts, $E = 0.01$, and $SL = \frac{1}{R_s}$, where R_s is the parasitic switch ON-state resistance. A sinusoidal voltage was then fed to the gate of the modified Materka MESFET model at the switching frequency, such that the sinusoid's DC component was -5 Volts, and its amplitude was 10 Volts peak-to-peak. The Materka model then behaved like the ideal switch in Fig. 5.14, with a duty cycle of 50 %. The parasitics C_s and L_s were added externally to the switch.

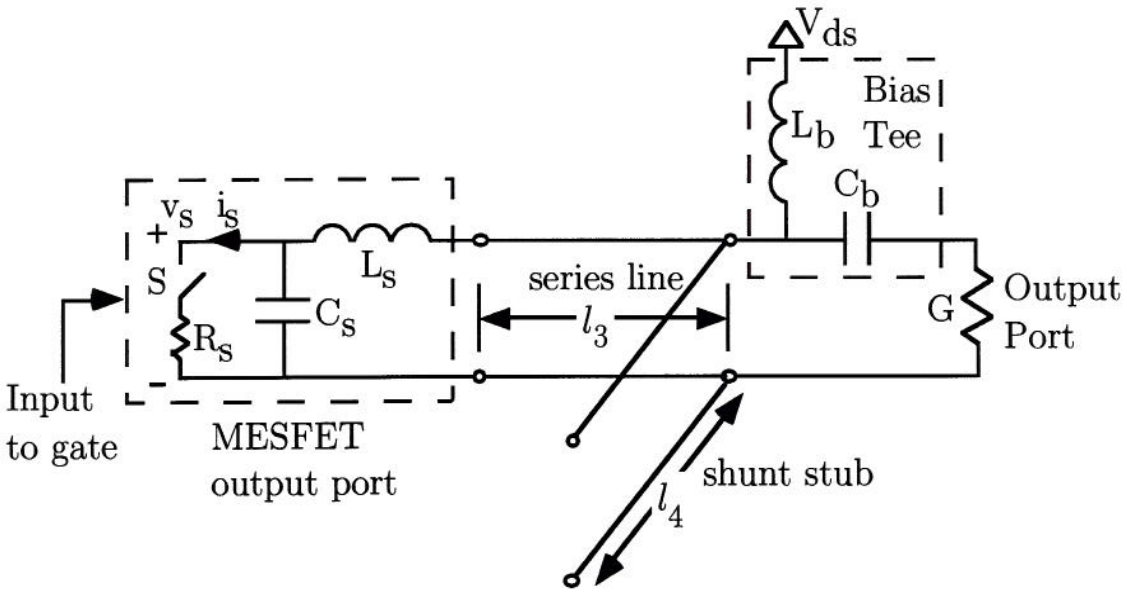


Figure 5.14. General class-E transmission-line amplifier with the MESFET output port represented by an ideal switch model, including switch parasitics.

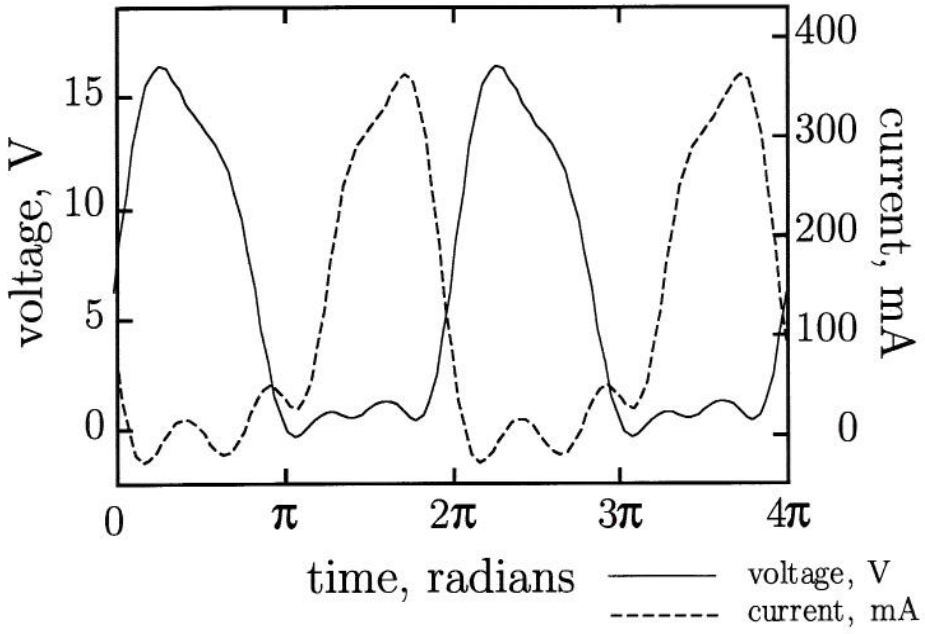


Figure 5.15. Harmonic balance circuit simulation of the 0.5 GHz class-E amplifier, showing the switch voltage and current time waveforms.

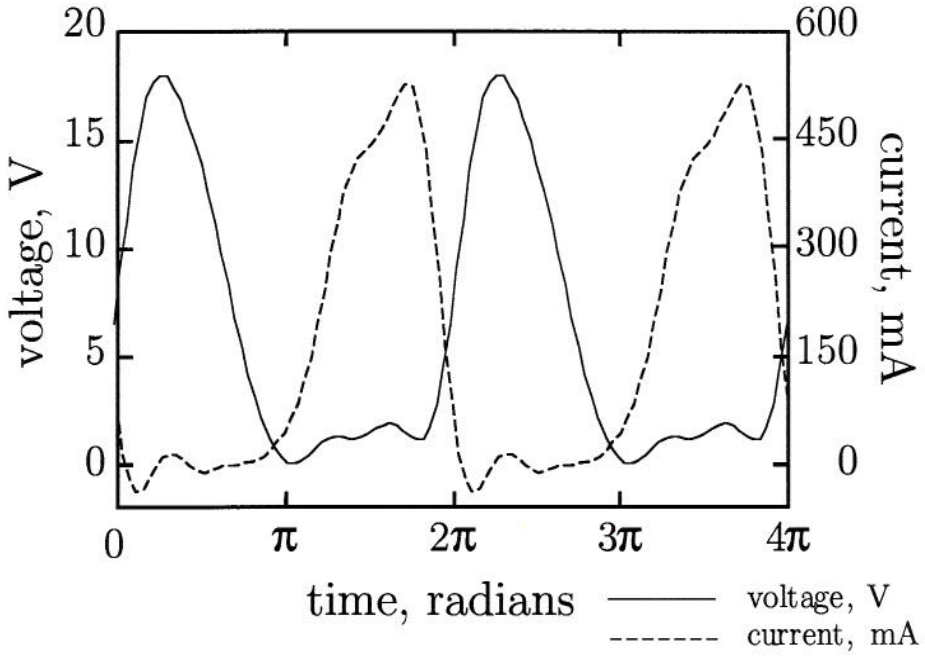


Figure 5.16. Harmonic balance circuit simulation of the 1 GHz class-E amplifier, showing the switch voltage and current time waveforms.

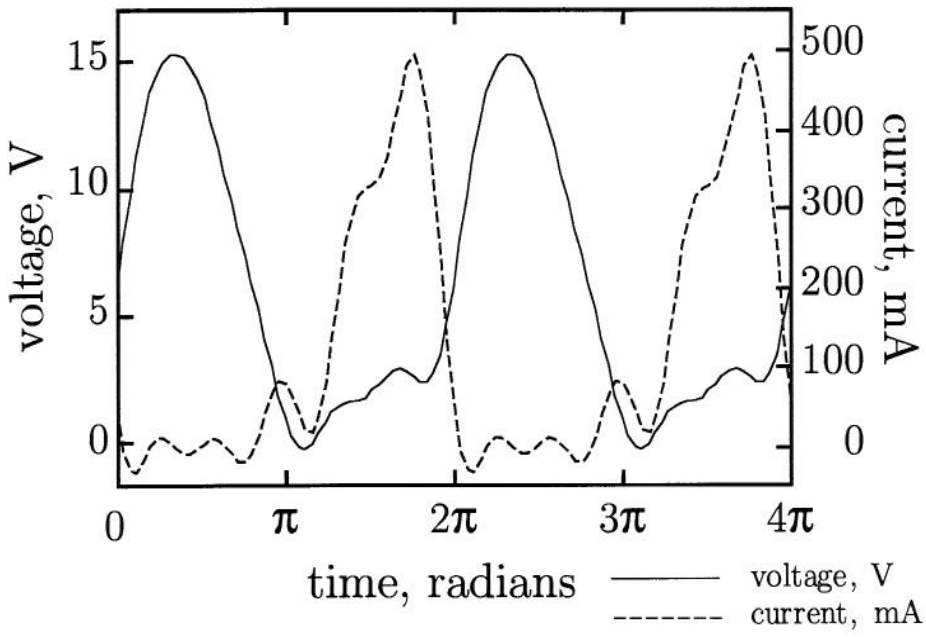


Figure 5.17. Harmonic balance circuit simulation of the 2 GHz class-E amplifier, showing the switch voltage and current time waveforms.

The exact dimensions of the three experimental circuits were used for lines l_3 and l_4, including the microstrip TEE-junction between l_3 and l_4, and the microstrip open-end capacitance for the shunt stub l_4. Then the switch parameters R_s, C_s, and L_s were adjusted until the expected class-E waveforms were observed, and the simulated drain efficiencies matched the measured results. The simulated switch voltages and currents are shown in Fig. 5.15, Fig. 5.16, and Fig. 5.17, for the 0.5, 1, and 2 GHz cases, respectively. The corresponding values of R_s, C_s, and L_s are tabulated in Table 5.2. The "expected" switch resistance R_s is found from the slope of the "knee" of the transistor's I-V curve. This switch resistance corresponds to an infinite transistor gain. Since the gain of the transistor decreases as the operating frequency increases, the simulated switch resistance increases for the higher-frequency class-E designs. The simulated switch capacitance changes slowly as a function of frequency, but it remains reasonably close to the expected value. The switch inductance L_s is larger than that expected from the Materka model, but this could be due to an extra inductance in the source of the CLY5. It is seen that the switch voltages and currents demonstrate the characteristics of class-E operation (compare with Fig. 4.3), thus verifying that the transmission-line class-E amplifier concept is valid, although the class-E conditions are only approximately satisfied. The output power levels predicted from these harmonic-balance circuit simulations using the ideal switch model are compared with measurement in Table 5.3.

Table 5.2. Comparison of analytically expected and numerically determined class-E switch resistance, capacitance, and inductance for the CLY5 MESFET.

Switch	Expected	Simulated 0.5 GHz	Simulated 1 GHz	Simulated 2 GHz
C_s	2.6 pF	3.3 pF	2.6 pF	2 pF
L_s	1.7 nH	3 nH	3 nH	3 nH
R_s	1.8Ω	2.6Ω	3.3Ω	6.1Ω

5.7 Conclusion

A transmission-line microwave class-E circuit has been introduced, along with design equations for the transmission-line lengths and impedances. Three circuits were

Table 5.3. Comparison between power levels predicted using harmonic balance simulations of the ideal circuit in Fig.5.14 and measured output power levels.

Frequency	Harmonic Balance P_{out}	Measured P_{out}
0.5 GHz	28.8 dBm	27.4 dBm
1 GHz	30.0 dBm	29.7 dBm
2 GHz	28.1 dBm	27.3 dBm

designed, fabricated, and measured using the Siemens CLY5 MESFET in a microstrip environment, at 0.5, 1, and 2 GHz. Experiments and harmonic-balance circuit simulations verified the simplified analysis presented previously, demonstrating a simple design method for matching the output of a MESFET for power and efficiency in class-E mode in a microwave transmission-line circuit for the first time. It was found that the MESFET's internal output capacitance and lead inductance are of primary importance for the design of a microwave class-E circuit. This work was done to verify the class-E theory from Chapter 4, and as a precursor to the quasi-optical class-E power amplifier which is presented in Chapter 6.

CHAPTER 6

THE QUASI-OPTICAL CLASS-E POWER AMPLIFIER

6.1 Introduction

In chapter 3, the free-space class-A power amplifier was introduced. In chapters 4 and 5, theory and experiments demonstrated the microwave class-E amplifier concept. In this chapter, the transmission-line class-E amplifier is integrated into a quasi-optical power-combining structure, demonstrating the first quasi-optical class-E power amplifier to date. Although the amplifier operates at microwave frequencies (5 GHz), it is believed that the class-E amplifier concept is applicable at millimeter-wave frequencies as well.

A modular approach was taken in designing the structure. The antennas, bias network, and class-E amplifier were all designed, built and measured separately. Then the pieces were put together to form the final amplifier, shown in Fig. 6.1. The final amplifier was not experimentally adjusted between fabrication and measurement, and the best performance was observed at 5.05 GHz, where an output power of 2.4 W was measured, with a corresponding drain efficiency of 74 %, a power-added efficiency of 64 %, and a compressed gain of 8.8 dB. These numbers represent the total power delivered to the output antennas in the amplifier, and do not take antenna losses into account. The measured powers and efficiencies also do not take into account potential lens nonidealities in a practical quasi-optical system. However, the intent of this work is to demonstrate the feasibility of a quasi-optical class-E power amplifier element; system integration is beyond the scope of this thesis.

6.2 Two microstrip 5 GHz class-E power amplifiers

In chapter 5, three experimental class-E circuits were presented, using the Siemens CLY5 MESFET at 0.5, 1, and 2 GHz. The CLY5 is designed for use up to 2.5 GHz,

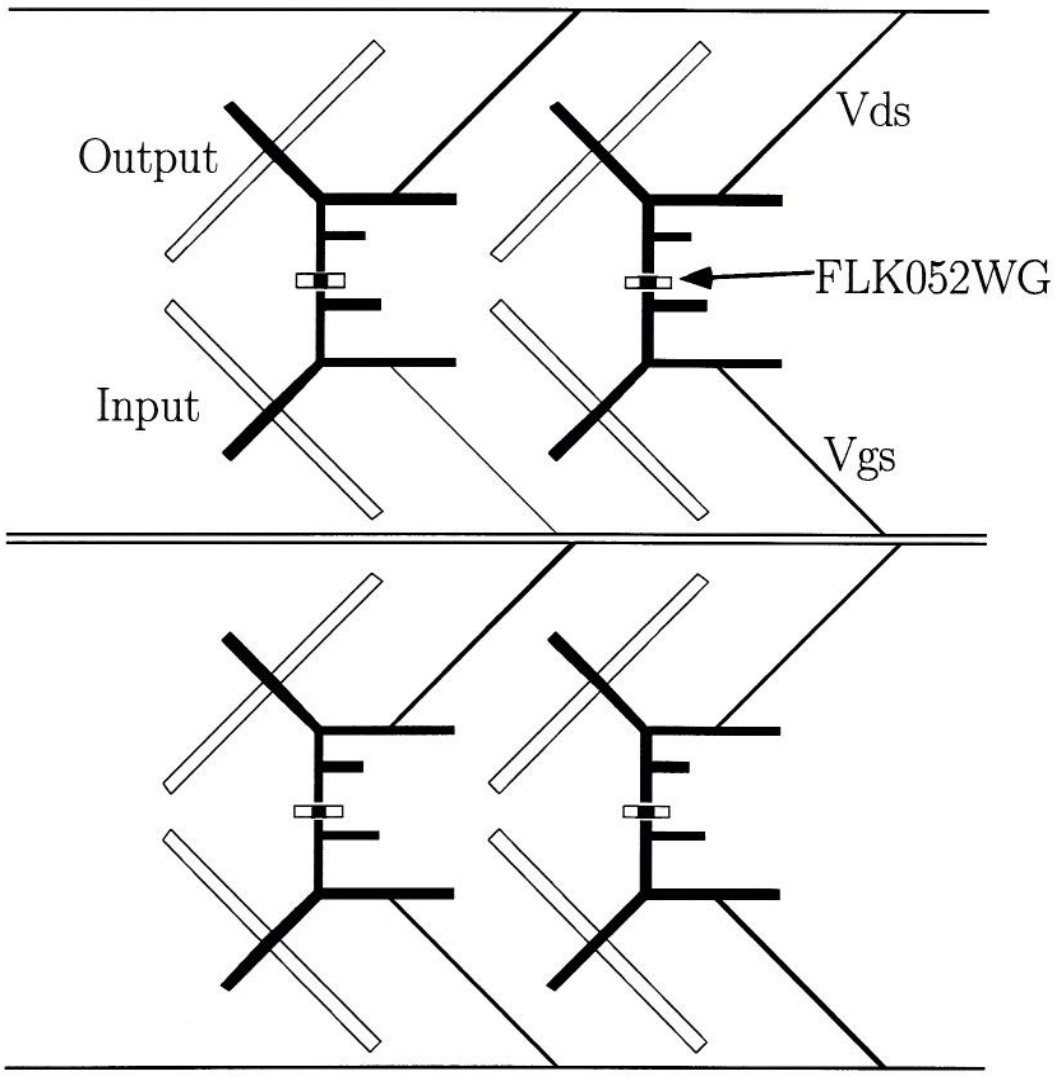


Figure 6.1. The quasi-optical class-E power amplifier. This 4-element power-combining structure demonstrated 2.4 W of output power at 5.05 GHz, with 8.8 dB compressed gain, 74 % drain efficiency, and 64 % power-added efficiency. Antiresonant 50Ω orthogonal slot antennas couple the power between the amplifier and free-space, and half-wave microstrip lines provide bias to the Fujitsu FLK052WGs' gate and drain terminals.

and it works best for high-efficiency class-E operation at 1 GHz and below. For a quasi-optical class-E amplifier, a higher frequency of operation is desired. Therefore, higher frequency power MESFETs were sought. Two packaged MESFETs were considered for the quasi-optical class-E power amplifier, the Fujitsu FLK052WG and the FLK202MH-14. Both of these devices are designed for Ku-Band (12-15 GHz) power amplification. At these frequencies, these MESFETs operate at approximately 30 % power-added efficiency. Using these devices at a lower frequency, such as 5 GHz, allows for the harmonic waveshaping required for class-E operation, analogous to using the 2.5 GHz CLY5 down at 0.5 and 1 GHz.

For an initial design of the two class-E amplifiers, the output capacitance and inductance C_s and L_s of the devices were estimated using s-parameters given in the data sheets and knowledge of the expected approximate output power of the amplifiers at 5 GHz. The output power of the class-E amplifier is proportional to the capacitance across the switch in the circuit (C_s). s-parameters were also used to design a single-stub input matching circuit for the two devices. These dimensions were used as a starting point for the experimental circuits, then the dimensions were experimentally adjusted until maximum power-added efficiency was obtained. The bias point and input power levels were also experimentally adjusted. The topology of these two class-E amplifiers was the same as the topology used for the amplifiers in chapter 5. The final amplifiers are shown in Fig. 6.2 and Fig. 6.3.

The FLK052WG class-E amplifier demonstrated an output power of 0.61 W, a compressed gain of 9.8 dB, a drain efficiency of 81 %, and a power-added efficiency of 72 % at 5 GHz. The input power was +18 dBm (63 mW). The FLK202MH-14 class-E amplifier demonstrated an output power of 1.8 W, a compressed gain of 7.6 dB, a drain efficiency of 73 %, and a power-added efficiency of 60 % at 5.1 GHz. The input power was +25 dBm (316 mW). Although the FLK202MH-14 amplifier delivers a higher output power into 50Ω, it operates at a lower efficiency, and it requires five times as much input power to operate in class-E mode. The high input power requirement is a concern, especially since the quasi-optical amplifier is fed in a free space setup from

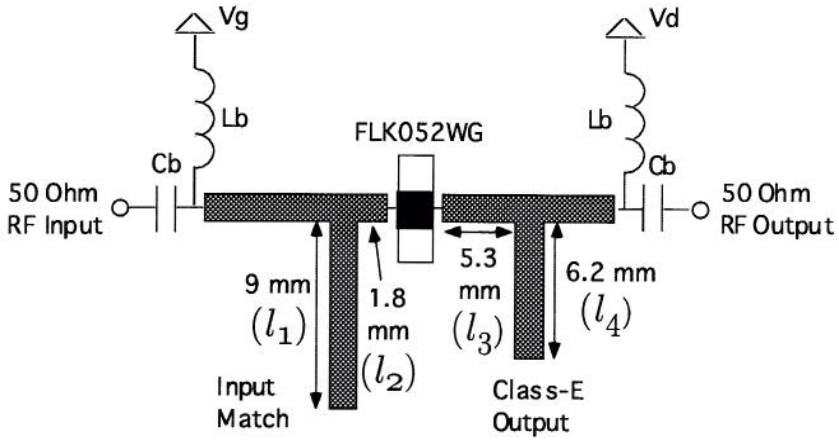


Figure 6.2. The FLK052WG class-E power amplifier in microstrip. This amplifier delivered 0.61 W into 50Ω, with a compressed gain of 9.8 dB, a drain efficiency of 81 %, and a power-added efficiency of 72 % at 5.0 GHz. The substrate was Duroid with ϵ_r = 2.2, h=0.508 mm, and all lines were 50Ω (1.6 mm wide).

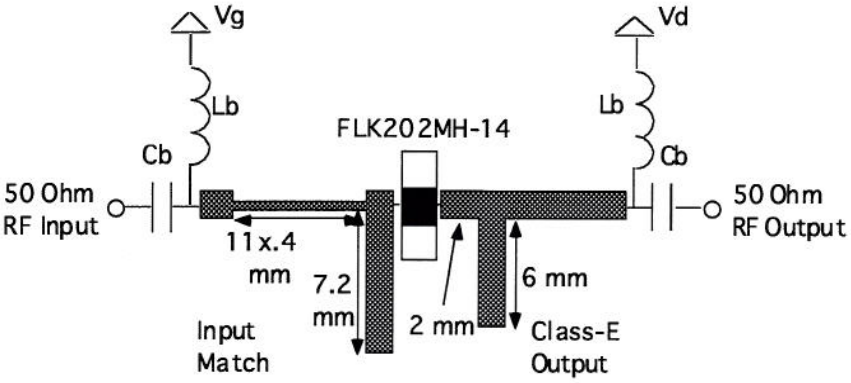


Figure 6.3. The FLK202MH-14 class-E power amplifier in microstrip. This amplifier delivered 1.8 W into 50Ω, with a compressed gain of 7.6 dB, a drain efficiency of 73 %, and a power-added efficiency of 60 % at 5.1 GHz. The substrate was Duroid with ϵ_r = 2.2, h=0.508 mm, and all lines were 50Ω (1.6 mm wide), except as noted.

a point in the far field of the array. Therefore, it was decided to used the Fujitsu FLK052WG MESFET for a 5 GHz quasi-optical class-E power amplifier.

The output power, drain efficiency, and power-added efficiency were measured as a function of input power level and frequency for the FLK052WG class-E amplifier. The power sweep is plotted in Fig. 6.4, and the frequency sweep is plotted in Fig. 6.5. The power-added efficiency is greater than 70 % over a 5 % bandwidth, and it is greater than 60 % over a 10 % bandwidth.

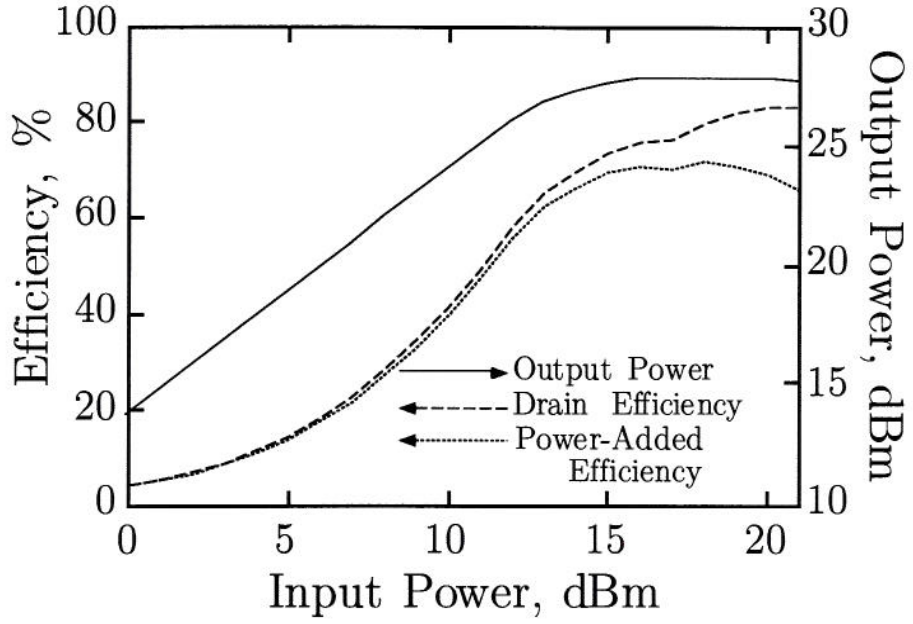


Figure 6.4. Power sweep for the FLK052WG class-E amplifier. Output power, drain efficiency, and power-added efficiency are plotted as a function of input power level.

It was desired to verify that the FLK052WG amplifier operates in class-E mode. Class-E operation is defined by the characteristics of the voltage waveform across the switch (as described in Chapter 4), in this case the voltage across the intrinsic MESFET's drain-source terminals. Unfortunately, measuring the voltage *inside* the MESFET package was not possible with the standard microwave equipment available for this project. Harmonic balance circuit simulations, however, can provide insight into the circuit's operation, as was shown in Chapter 5.

The circuit shown in Fig. 6.6 represents the output circuit for the FLK052WG class-E amplifier. The exact transmission-line dimensions from the actual circuit were

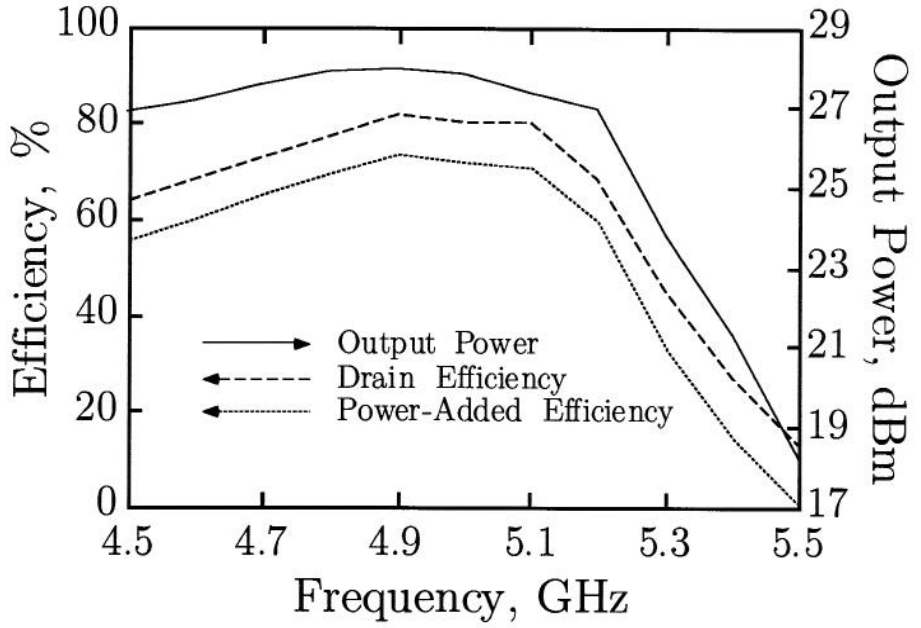


Figure 6.5. Frequency sweep for the FLK052WG class-E amplifier. Output power, drain efficiency, and power-added efficiency are plotted as a function of frequency of operation.

used in Compact Software's Harmonica (harmonic balance) circuit simulator. L_b and C_b were assumed to act as an ideal bias tee (a real bias tee was used in the measurement). The output port impedance is 50Ω. As in Chapters 4 and 5, the transistor's output port was assumed to look like an ideal switch with an ON-state resistance R_s, output capacitance C_s, and output inductance L_s. C_s and L_s were adjusted in the harmonic balance simulations until the voltage and current waveforms across the switch looked like the ideal class-E waveforms. R_s was adjusted until the simulated DC-RF conversion efficiency matched the measured efficiency. According to the simulations, $C_s = 0.4\,\text{pF}$, $L_s = 0.5\,\text{nH}$, and $R_s = 3.3\Omega$ for the 5 GHz Fujitsu FLK052WG class-E amplifier. The simulated class-E switch voltage and current waveforms are shown in Fig. 6.7. The simulated output power level was 29.7 dBm, while the measured output power level was 27.9 dBm.

After the two 5 GHz class-E circuits were fabricated and measured, a nonlinear Materka MESFET model became available for the FLK052WG (from Compact Software). This model was used on a harmonic-balance circuit simulator to compare with

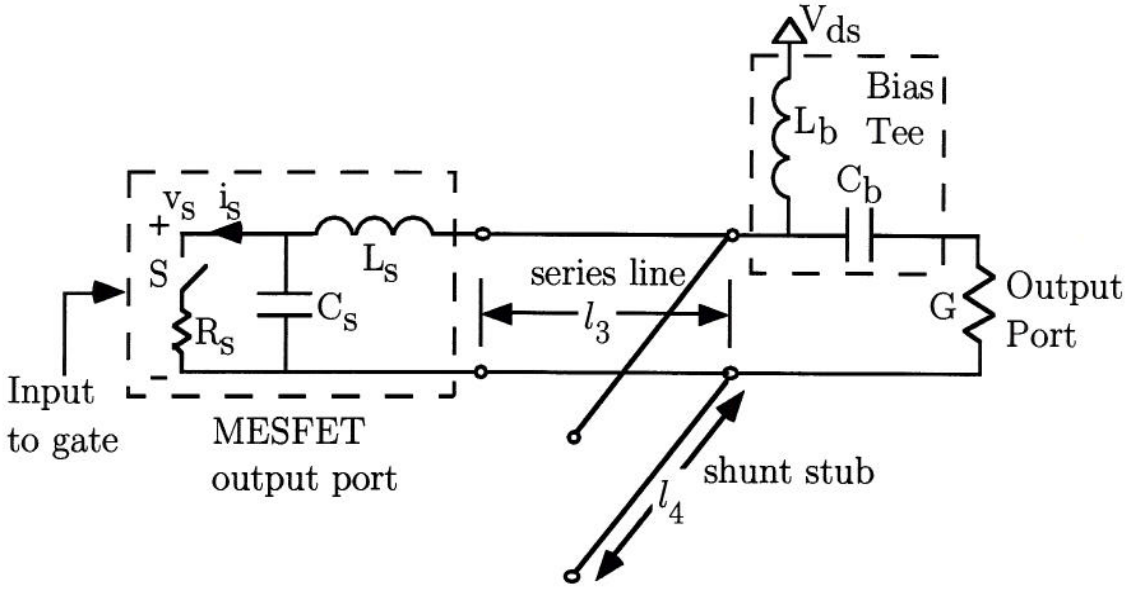


Figure 6.6. Output circuit for the FLK052WG class-E amplifier. Both transmission lines are 50Ω, and their lengths are the same as shown in Fig. 6.2. C_s, L_s, and R_s were determined using harmonic balance circuit simulation, and the voltage and current across the switch ($v_s(t)$ and $i_s(t)$) are shown in Fig. 6.7.

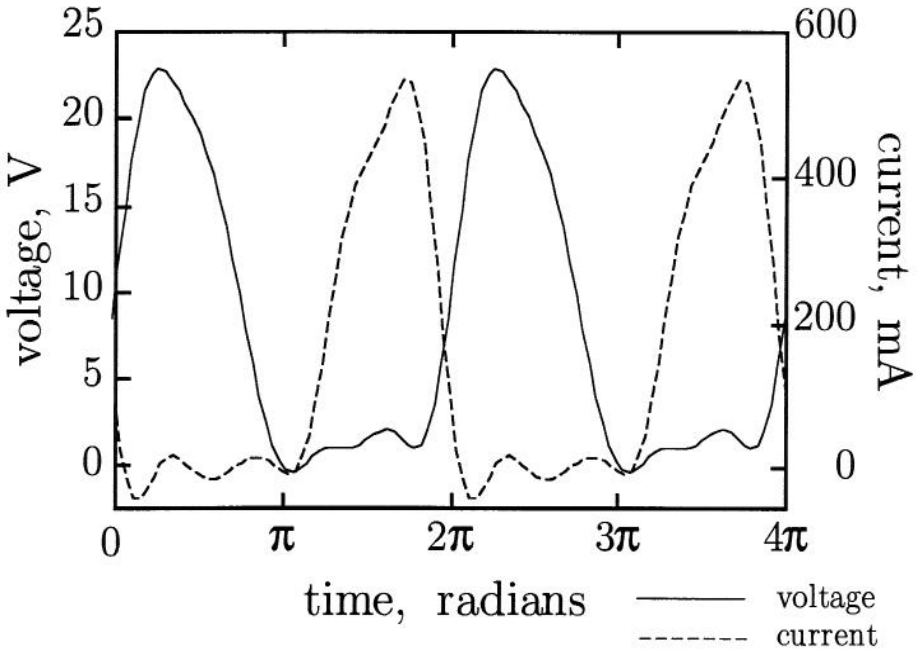


Figure 6.7. Simulated voltage and current time waveforms ($v_s(t)$ and $i_s(t)$) for the FLK052WG class-E output circuit shown in Fig. 6.6. The waveforms have the characteristic class-E shape.

the experimental results. Initially, the dimensions of the experimental circuit were used in the simulation. The simulated results were not close to measurement, however; in the simulation, the input was mismatched, and the gain, output power, and efficiency were very low. Since the measured circuit was experimentally optimized for power-added efficiency, it was decided to optimize the circuit on the simulator for power-added efficiency as well, and to compare the two cases. The results of the experimental and numerical optimizations are shown in Table 6.1. The simulation and experiment differ significantly, which leads to the conclusion that the nonlinear Materka MESFET model does not adequately predict heavily compressed (switched-mode) class-E amplifier operation. It is believed that the harmonic-balance circuit simulator is not at fault, since the ideal switch model used above (see Fig. 6.6) predicts the class-E amplifier's output section adequately, including characteristic class-E switch voltage and current waveforms for the FLK052WG circuit, as shown in Fig. 6.7. Unfortunately, the ideal switch model cannot be used to design the input match of a class-E amplifier, and does not allow prediction of gain, power-added efficiency, or final amplifier power and efficiency bandwidths. Therefore, it is concluded that better nonlinear MESFET models are needed to allow accurate simulation of heavily compressed (switched-mode) microwave class-E amplifiers.

Table 6.1. Comparison of experimentally optimized 5 GHz FLK052WG class-E amplifier with optimization using a harmonic balance circuit simulator (with the Materka MESFET model). The simulation and experiment differ significantly. Lengths l_1 through l_4 are labelled in Fig. 6.2.

Optimization	η_d	PAE	Pout	Gain	l_1	l_2	l_3	l_4
Experiment	81 %	72 %	27.8 dBm	9.8 dB	9.0 mm	1.8 mm	5.3 mm	6.2 mm
Simulation	44 %	35 %	23.8 dBm	5.8 dB	6.5 mm	0 mm	4.8 mm	6.4 mm

6.3 The antiresonant slot antenna and bias network

The microstrip-fed antiresonant slot antenna, shown in Fig. 6.8, was chosen to couple the 5 GHz FLK052WG class-E amplifier to free space because of its broadband nature and its 50Ω input impedance. The slot antenna was designed using the CAD

tool WireZeus (described in [141]), then it was fabricated, measured and adjusted for optimum input return loss at 5 GHz. An open-circuited 50Ω microstrip line runs a quarter wavelength beyond the slot antenna, which causes the 50Ω microstrip feed line to be coupled to the antiresonant slot antenna in the ground plane of the structure. A coax-to-microstrip connector was attached to the structure, and a 2:1 voltage standing-wave ratio (VSWR) bandwidth of greater than 20 % was measured. The cross-polarization ratio was approximately 23 dB at 5 GHz. A half wavelength open-circuited microstrip line was used to provide bias to the amplifier, by attaching a thin wire to the voltage null at the center of the line. The dimensions of the final radiating structure, including the bias network, are shown in Fig. 6.8.

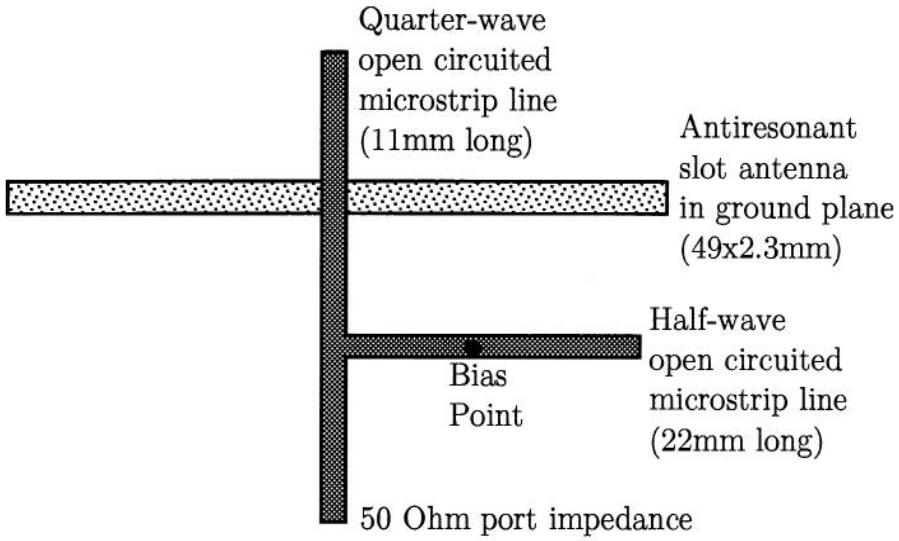
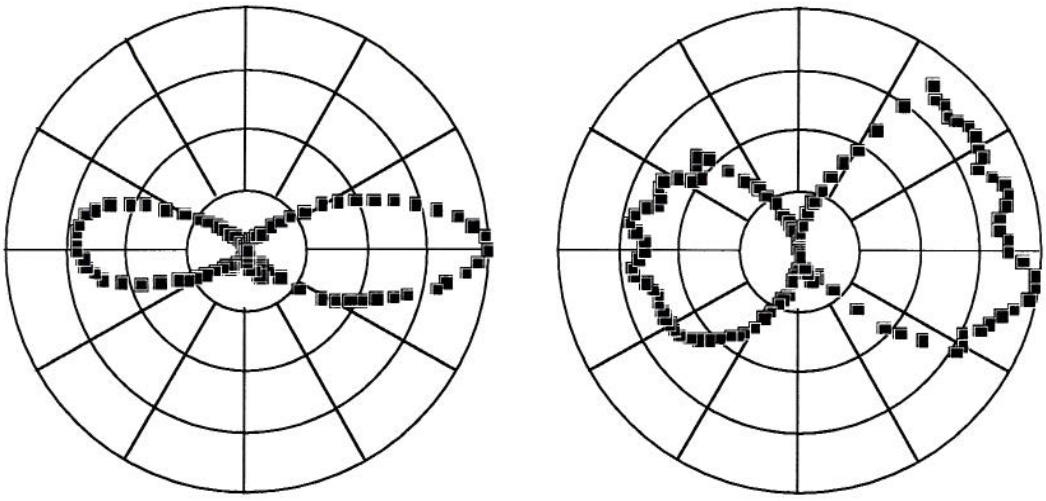


Figure 6.8. 50Ω antiresonant microstrip-fed slot antenna used for the 5 GHz quasi-optical class-E amplifier. This antenna demonstrated a 2:1 VSWR bandwidth greater than 20 % . A half-wave bias line is used to provide bias to the MESFET's gate and drain terminals. All microstrip lines are 50Ω (1.6 mm wide), and the substrate is Duroid with a thickness of 0.508 mm and $\epsilon_r = 2.2$.

The measured radiation patterns for the microstrip-fed 50-Ω antiresonant slot antenna are shown in Fig. 6.9. The antenna radiates approximately 1.5 dB more power into the dielectric/air side of the structure, as can be seen in the H- and E-plane pattern measurements.



(a) H-Plane Pattern (b) E-Plane Pattern

Figure 6.9. Radiation patterns for the 50-Ω antiresonant microstrip-fed slot antenna at 5 GHz. The H-plane pattern is shown in (a), and the E-plane pattern is shown in (b).

6.4 The quasi-optical class-E power amplifier

The 4-element quasi-optical class-E power amplifier is shown in Fig. 6.1. The FLK052WG 5 GHz class-E amplifier, the antiresonant 50Ω slot antenna, and the bias network were all integrated into the quasi-optical structure. The class-E amplifier sees 50Ω at the fundamental frequency of operation at both its input and output ports. At the second harmonic frequency, the input impedance of the antiresonant slot antenna is unimportant, since the open-circuit condition at the output port of the FLK052WG is preserved independent of the load impedance at the second harmonic (as discussed in Chapter 4). The input and output antennas are orthogonally polarized to one another to minimize coupling between them, and the fields contained in the microstrip lines are primarily in a direction orthogonal to both input and output radiated fields. Although the slot antennas radiate and receive in both directions from the array surface, external polarizers can be used in a quasi-optical system to make the amplifier receive and radiate in a preferred direction.

To calibrate the free-space amplifier measurement, a "through" structure was fabricated, which was identical to the amplifier array, except that the class-E amplifiers

in the structure were replaced with 50Ω lines. First the through structure was placed between two horn antennas, and the power received in the second horn relative to the power delivered to the first horn was measured (see Fig. 6.10). Since the through structure was in the middle between the two horn antennas, approximately half of the power loss was assumed to be due to the input side of the structure, and other half of the power loss was assumed to be due to the output side of the structure. A correction was made to compensate for the difference in power radiated from the two sides of the slot antennas. Then the quasi-optical class-E power amplifier was placed in the system, and enough power was delivered to the first horn to drive the input of the amplifier into compression. 10 W of power was delivered to the first horn, and 316 mW of power was received by the amplifier. 2.24 W of output power was generated by the quasi-optical class-E power amplifier. This method of calibration resulted in measurements of output power and efficiency which were repeatable to within a few percent, which is believed to be more accurate than the method used to calibrate the amplifier presented in Chapter 3 (where the Friis transmission formula was used to calibrate power levels in the system)

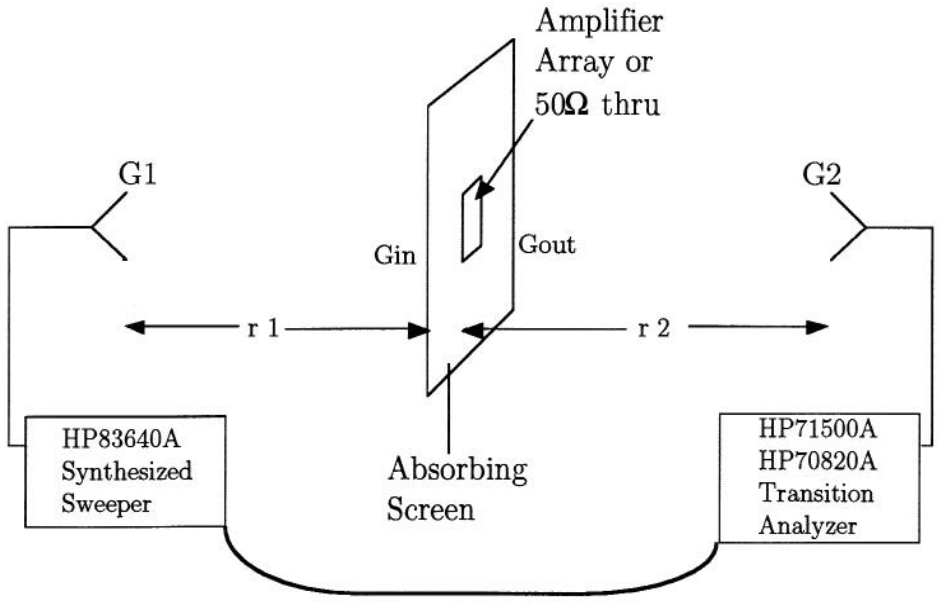


Figure 6.10. Measurement setup for the 5 GHz quasi-optical class-E power amplifier. First a passive structure is placed into the system (with 50-Ω lines connecting the input and output antennas), and a calibration power level is measured. Then the amplifier array is placed in the system, and the gain and power levels are determined.

A single cell of the quasi-optical class-E amplifier was measured in free space, and it demonstrated 0.67 W of output power at 5 GHz, with a drain efficiency of 80 %, a power-added efficiency of 71 %, and a compressed gain of 9.3 dB. Then the 2x2 quasi-optical array was measured in free space, and it demonstrated 2.24 W of output power at 5 GHz, with a drain efficiency of 67 %, a power-added efficiency of 58 %, and a compressed gain of 8.5 dB. Dividing the output power per element in the 2x2 array by the output power of the single cell, a power-combining efficiency of 84 % is found. A power sweep was performed on the single cell quasi-optical class-E amplifier, and it is shown in Fig. 6.11. The results of the 2x2 quasi-optical class-E power amplifier are superimposed on the graph; the output power in this case is plotted *per element* for direct comparison with the single cell results.

The 2x2 quasi-optical class-E amplifier was then calibrated over a 10 % frequency range, and the output power, drain efficiency, and power-added efficiency were plotted as a function of frequency, shown in Fig. 6.12. The efficiency is above 50 % over a 3.5 % bandwidth, and it is above 30 % over a 6 % bandwidth. The best performance was observed at 5.05 GHz, where an output power of 2.4 W was measured, with a corresponding drain efficiency of 74 % and a power-added efficiency of 64 %. The compressed gain at 5.05 GHz was 8.8 dB.

Earlier in this chapter, two 50Ω microstrip class-E amplifiers were presented, one using the Fujitsu FLK052WG MESFET, and the other using the Fujitsu FLK202MH-14 MESFET. The intrinsic semiconductor chips inside of these two MESFETs are identical, except that the FLK202MH-14 is four times as large as the FLK052WG. It is known that the output power of a MESFET does not grow as quickly as its physical size, and this is clearly the case here: the FLK052WG class-E amplifier delivers 0.61 W of output power into 50Ω, while the FLK202MH-14 delivers 1.8 W. Considering that the FLK202MH-14 is physically four times as large as the FLK052WG, the output power might be expected to be four times as large as well, or 2.44 W. If the FLK202MH-14 is considered as four FLK052WGs in parallel, then a power-combining efficiency can be defined. In this case, the power-combining efficiency is 74 %. Using the quasi-optical

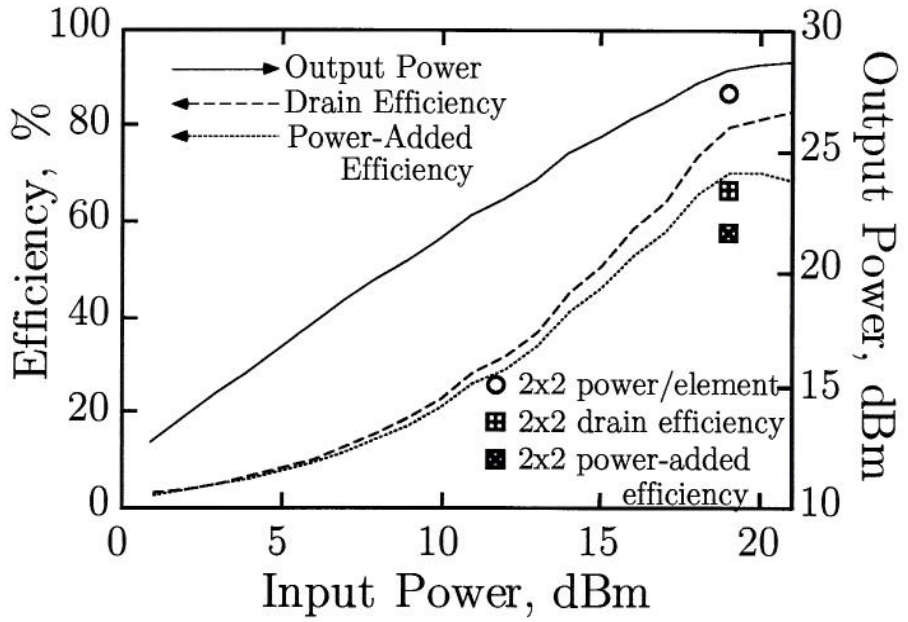


Figure 6.11. Power sweep curve for the single cell quasi-optical class-E power amplifier element. Output power, drain efficiency, and power-added efficiency are plotted as a function of input power level. The results of the 2x2 quasi-optical class-E power amplifier are superimposed on the graph; the output power in this case is plotted *per element.*

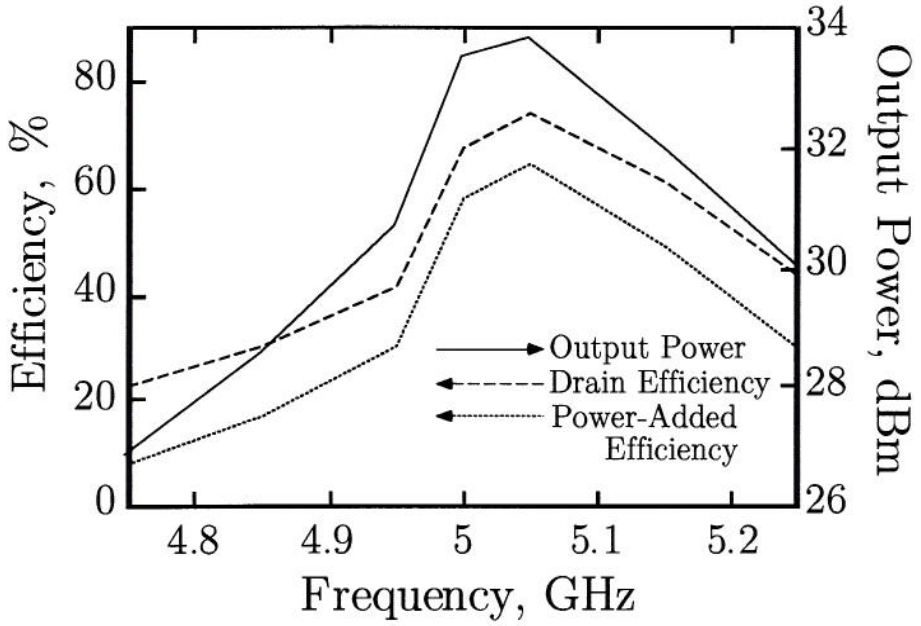


Figure 6.12. Frequency sweep curve for the 2x2 quasi-optical class-E power amplifier array. Output power, drain efficiency, and power-added efficiency are plotted as a function of operating frequency. The input power level is +25 dBm at 5 GHz.

techniques demonstrated in this chapter, a higher power-combining efficiency of 84% has been demonstrated, which validates the use of quasi-optical combining techniques. This advantage is expected to become more significant when larger numbers of elements are power combined.

When the quasi-optical class-E power amplifier was first tested, an oscillation at 1.6 GHz was observed. Numerous attempts were made at stabilization, until finally a 50Ω resistor and a 56 pF DC blocking capacitor in series were soldered directly between the gate and drain terminal of each FLK052WG MESFET. An analysis of the input match to the FLK052WG class-E amplifiers showed that the FLK052WG's input impedance was only $3.5 - j5.3\Omega$ under heavily compressed class-E operation at 5 GHz. Since the input impedance of the MESFET was so low at the frequency of operation, the 50Ω impedance placed across its gate and source terminals caused an insignificant degradation in the class-E amplifier's input match and gain at 5 GHz. However, the 1.6 GHz oscillation ceased, and the amplifier became stable. The 56 pF blocking capacitor kept the DC gate-source bias from dissipating any power into the 50Ω resistor. It is possible that coupling between the input and output slot antennas caused the 1.6 GHz oscillation to occur.

6.5 Conclusions

In this chapter, a class-E power amplifier active antenna element has been demonstrated for the first time. Quasi-optical power combining can add the power of a large number of transistors while maintaining high efficiency operation. Since heat sinking is an important issue for high power quasi-optical power amplifiers (due to their two-dimensional nature), high efficiency power generation is crucial in a successful quasi-optical system.

CHAPTER 7

SUMMARY OF RESULTS AND SUGGESTIONS FOR FUTURE WORK

7.1 Summary of Results

This thesis has for the first time presented a *high efficiency* quasi-optical power amplifier, integrating a class-E transmission-line amplifier into a free-space structure. High efficiency is of interest to the quasi optical community, because of the two-dimensional nature of quasi-optical active surfaces and the difficulties which arise in heat sinking these structures without interfering with wave propagation through them. In Chapter 1 of this thesis, some of the preliminary work in quasi-optics and in quasi-optical amplification was reviewed.

In Chapter 2, some preliminary work done on a quasi-optical voltage-controlled oscillator (VCO) was described, which revealed the need for an accurate way to electrically characterize these structures, and also the need to find ways of predicting and designing for high power and efficiency in a quasi-optical system. This preliminary study motivated the rest of the work in this thesis, since high efficiency power amplification is a prerequisite for high-efficiency oscillator design, and is a necessary component placed after oscillator sources in most systems.

In Chapter 3 the quasi-optical class-A power amplifier was introduced. Although the efficiency of this structure was relatively low (on the order of 20%), it demonstrated the feasibility of stable quasi-optical power amplification. The meandering ground planes in the structure electrically isolate the two sides of the amplifier, and allow arbitrary polarization of input and output waves. This was demonstrated with a single cell amplifier which had a linearly polarized input wave and a circularly polarized output wave. Although broadband matching was used to couple the transistor to the patch antenna, the narrowband nature of the patches limited the bandwidth of the

amplifier. Also, via holes were an integral part of the structure, and were used to electrically connect the meandering ground planes on either side of the structure, as well as to connect the drain leads of the MESFETs to the back side of the amplifier. Via holes are problematic at millimeter-wave frequencies, due to their unknown parasitic reactances and the mechanical problems which occur when substrates are made electrically thin at very small wavelengths.

In Chapter 4 the microwave class-E amplifier was presented. The original class-E topology was analyzed exactly in Appendix A, and although the results were numerically very accurate, the resulting equations were so long and complicated that design and insight using the exact results was not feasible. Therefore in Chapter 4, several simplifying assumptions were made about high frequency class-E amplification, which resulted in insightful results and allowed first-order designs of microwave and millimeter-wave class-E amplifiers to be derived. Closed-form design equations were found for several different class-E topologies, including (for the first time) a transmission-line version suitable for very high frequency class-E circuits, since transmission lines have much lower loss than lumped elements at microwave and millimeter-wave frequencies. The method used in Chapter 4 may be applied to other class-E topologies, and may even be used to design radiating structures (antennas) which satisfy the class-E conditions at a finite number of harmonics (two harmonics are sufficient for approximate class-E operation). An approximate expression for DC-RF conversion efficiency was developed under the assumption that the transistor's ON-state resistance was the primary source of loss in the class-E circuit. The voltage across the device output port (the switch voltage) was analyzed using Fourier series, and closed-form expressions for switch voltage harmonic magnitude and phase were found. It was found that the class-E switch voltage consists primarily of first and second harmonic frequency components. Finally, the effects of nonlinear switch (device output port) capacitance was analyzed. The distorted switch voltage was plotted, and modified class-E design equations were found.

In Chapter 5 the concept of the transmission-line class-E amplifier was experimentally verified. The Siemens CLY5 MESFET was used in three experimental class-E

amplifiers at 0.5, 1, and 2 GHz using microstrip transmission lines. The approximate design equations developed in Chapter 4 were used for the initial design of the 0.5 GHz amplifier, which was then experimentally adjusted in the lab for maximum power-added efficiency. The transistor switch model was then adjusted to correspond to the experimental transmission line lengths, and this modified model was used to design the 1 and 2 GHz amplifiers. Thus the design equations presented in Chapter 4 were validated. Then the ideal switch model and the experimentally determined transmission line lengths were used to simulate the amplifier output circuits on a harmonic balance simulator, to verify that the three circuits operated in class-E mode. The characteristic class-E switch waveforms were seen for all three circuits.

In Chapter 6, the quasi-optical class-E power amplifier was presented. First, two 5 GHz class-E amplifiers were measured in a 50Ω coaxial system, to determine which one would be more suitable for integration into a quasi-optical structure. Once one of these amplifiers was chosen, an antiresonant 50Ω microstrip-fed antenna was designed, fabricated, and measured, also in a 50Ω system. A bias network was included into the microstrip-fed antenna structure. Then the separate pieces were combined into a single quasi-optical amplifying element, and the quasi-optical class-E power amplifier was measured in free space, after the amplifier was stabilized using lumped elements without degrading gain and efficiency. A different calibration procedure was used for this project than for the amplifier presented in Chapter 3. In the patch/patch amplifier, the Friis transmission formula was used to calculate the gain added by the amplifier in the free-space system. For the quasi-optical class-E power amplifer, a 50Ω "through" line was integrated into a second quasi-optical structure, to compare to the amplifier directly. This resulted in more accurate power and efficiency measurements. Also, this structure required no vias through the substrate, since the slot antennas were placed in the ground planes of the microstrip lines directly. The MESFET packaged devices were soldered into the structure's ground plane, which facilitated heat sinking.

7.2 Suggestions for Future Work

Quasi-optical power combining is a relatively young and broad research topic, and quasi-optical power amplification is in its early infancy. Several possibilities for future work are given in this section, although this is in no way a comprehensive list of the different aspects of quasi-optical power amplification which may be pursued.

7.2.1 New class-E circuit topologies

In Chapter 4, the original class-E circuit topology was analyzed, along with several other circuit topologies which had never before been presented in the literature. Of particular interest were the transmission-line class-E load networks which offer low loss reactance at microwave frequencies. These new class-E circuit topologies are by no means the only ones possible, and research into interesting new configurations may yield performance enhancements over existing topologies. It would also be useful to design radiating structures (antennas) which would satisfy the load impedances necessary for class-E operation for a given transistor directly. This would be especially useful for quasi-optical power generation, where space is at a premium, and matching network complexity between transistor and antenna are best minimized.

7.2.2 Effects of finite harmonic content in the class-E circuit

In Chapter 4 the Fourier series of the switch voltage in the class-E amplifer was derived. When only two harmonics of switch voltage were plotted, it was seen that the waveform differed only slightly from the exact (infinite-harmonic) switch voltage waveform. However, the switch voltage is no longer exactly zero when there is current present across the switch, so that the maximum theoretical efficiency attainable in a two-harmonic class-E circuit is no longer 100 %. It would be useful to derive the maximum efficiency attainable in a class-E circuit with either two or three harmonics of switching frequency present in the switch voltage. It is useful at microwave and millimeter-wave frequencies to be able to design for a finite number of harmonics.

7.2.3 Linearity and modulation of the class-E amplifier

For many applications, it is necessary to transmit information in addition to being able to generate high power levels efficiently. Many of today's communication systems use modulation schemes which simultaneously require broad bandwidth, frequency modulation, and amplitude modulation. The class-E amplifier is capable of large bandwidth and excellent frequency modulation characteristics, but since the amplifier is so heavily compressed, amplitude modulation at the input to the amplifier is almost entirely lost (the output power is not a function of the input power level under heavy compression). However, if amplitude information is separated from frequency information in an incoming signal, a technique known as envelope restoration may be used effectively in a class-E amplifier. The frequency information is fed to the input of the amplifier, and the amplitude information is put onto the supply voltage. Since the output power of a high-efficiency power amplifier closely follows the DC power, the amplitude information placed on the supply voltage is directly transferred to the output signal. This technique can be used to modulate the quasi-optical class-E amplifier with a high degree of linearity.

7.2.4 Effects of input drive on the class-E amplifier

In a standard microwave power amplifier, it is usually assumed that both the input and the output of the circuit contain pure sinusoidal signals. At the output ports of a transistor, nonlinearity occurs during saturation, and harmonic waveshaping is utilized for high efficiency operation. The signal delivered to a 50Ω port, however, is sinusoidal.

The input waveform is assumed to be sinusoidal, and if the input port of the transistor is not driven too hard, and if its impedance is not strongly nonlinear, then the signal at the input to the transistor remains a sinusoid. The advantages of this standard approach to power amplifier input drive is that only one harmonic needs to be taken into account in the amplifier's input port analysis, making the design relatively simple, and allowing standard phasor analysis of the input matching circuit. In addition, restricting

the input signal to the fundamental frequency allows for broadband circuit operation.

Under high levels of saturation, the sinusoid incident upon the input of a microwave power amplifier begins to distort, for example due to the parasitic diode and nonlinear capacitance present at the input of a MESFET. The top of the sinusoid begins to flatten, and the bottom of the sinusoid becomes sharper, causing the input signal to look much like an inverted triangular waveform. This effect has been observed in harmonic balance circuit simulations of the class-E amplifier circuit under heavy compression.

Presently it is unknown whether this effect can be exploited for advantageous effects, or whether the effect should simply be avoided. Possibly, second and third harmonic resonators at the input of a power amplifier circuit could either enhance or minimize this effect. Understanding this phenomenon could prove to be important in the design of high-efficiency power amplifiers. Also, MESFET designers could work towards using this effect to advantage in new transistor fabrication processes.

For heavily compressed high efficiency operation, the ideal input signal to the gate of a transistor is a square wave. During the upper half of the square wave, the transistor is turned "ON", and during the lower half of the square wave, the transistor is turned "OFF". Because the transition between the transistor "ON" and "OFF"-states is so abrupt, the efficiency of a switched-mode (heavily compressed) circuit is maximized. Harmonic balance simulations have shown that 5-15 % improvement in DC-RF conversion efficiency can be realized by using a square wave at the gate of a MESFET rather than a sinusoid. There are some drawbacks to using a square-wave input signal in a practical microwave amplifier, however. Higher harmonics present at the input of an amplifier make the system more complex, and stronger nonlinearity in the circuit make it more difficult to analyze accurately. A square wave signal at the input of an amplifier requires significant third and fifth harmonic components to be present at the gate of the transistor, which inherently makes the circuit more narrowband than with simpler sinusoidal drive. Also, other problems such as subharmonic oscillation may be exacerbated by the stronger nonlinearity of the system. However, the improvement

in efficiency possible using square-wave input drive may be worth the extra effort in situations where high efficiency power generation is critical.

7.2.5 Losses in the class-E circuit – further efficiency analysis

In Chapter 4, the efficiency of the class-E circuit was found for the case of small switch ON-state resistance. This is believed to be the dominant loss mechanism in the class-E amplifier. An OFF-state resistance may provide more accurate efficiency calculations if taken into account. Also, in some cases the losses in the load network reactive elements (such as transmission-line losses) may become of importance, expecially for the analysis of power amplifiers approaching 100 % efficiency. Analysis of losses at the input to the switching transistor would allow calculation of overall power-added efficiency.

7.2.6 Transistor capacitance nonlinearity in the class-E amplifier

A special case of transistor output capacitance nonlinearity was analyzed in Chapter 4. For this special case, modified switch voltage and design equations were derived. Analysis of more general cases of output capacitance nonlinearities would yield more accurate design equations and more insight into the effects of device nonlinearity. This would be particularly useful for devices such as the Heterojunction Bipolar Transistor (HBT), in which the output capacitance is strongly nonlinear.

7.2.7 Broadband class-E amplifier operation

The experimental class-E amplifiers presented in Chapter 5 and Chapter 6 demonstrated high efficiency over relatively large bandwidths, using standard single-stub input matching circuits and single-stub class-E load networks. Broadband input and output circuit topologies (using quarter-wave matching sections, for example) would maximize the operating bandwidth of a high-frequency class-E amplifier.

7.2.8 More accurate nonlinear transistor models for simulation

In Chapter 5 and Chapter 6, experimental class-E amplifiers were simulated using a standard nonlinear MESFET model (the Materka model) on a harmonic balance circuit simulator. The simulations differed from experiment significantly. However,

using an ideal switch model on the harmonic balance simulator yielded the correct class-E switch voltage and current waveforms, and correlated well with experiment. Unfortunately, the ideal switch model does not take the gain or input match of the device into account, and the switch parasitics (R_s, C_s, and L_s) were deduced from the experimental class-E amplifier dimensions. More accurate nonlinear transistor models are needed to accurately simulate heavily compressed (switched-mode) high-efficiency quasi-optical power amplifiers.

7.2.9 The quasi-optical class-E multiplier

In a class-E multiplier, the input of the transistor is driven at a fundamental frequency, and an output class-E circuit responds to a higher harmonic frequency. In a quasi-optical class-E multiplier, the receiving side of the structure (the input antennas) would be tuned to the fundamental frequency of operation, and the output radiating antennas would be tuned to the desired harmonic frequency. Conceivably, a single antenna could act as a receiver at the fundamental frequency, and re-transmit at the desired harmonic.

7.2.10 The quasi-optical class-E oscillator

The maximum power available from a feedback oscillator is equal to the maximum power which can be added to the system by an active device. Therefore, the maximum DC-RF conversion efficiency possible from an oscillator is equal to the maximum power-added efficiency possible in an amplifier using the same device. To make a class-E oscillator, first a class-E amplifier is designed. At the point of maximum power-added efficiency, the compressed large-signal gain of the amplifier is determined, and the relative phase between the input and output signals is also found. A feedback network is then added between the output and input of the class-E amplifier, with the proper phase and amplitude relationship to operate the feedback class-E oscillator at the optimum compression point, and to cause the system to oscillate at the desired operating frequency. For a quasi-optical class-E oscillator, the necessary feedback path between the output and input of the class-E amplifier is achieved using coupling between input

and output antennas and quasi-optical interaction within the system.

7.2.11 The quasi-optical class-F amplifier

The class-F amplifier uses harmonic waveshaping in its output circuit in similar fashion to the class-E circuit. Class-F operation demonstrates relatively high linearity in its input-to-output power gain characteristic, while still providing high efficiency. The class-E amplifier presented in this thesis requires envelope restoration to provide the amplitude linearity required for modern digital modulation schemes. Although the class-E circuit promises to provide broader bandwidth operation than the class-F circuit, the added complexity of implementing an envelope restoration circuit adds cost to a system and is in many cases undesirable. Therefore, it is believed that class-F operation in a quasi-optical amplifier may prove advantageous over class-E operation in some circumstances. Ideally, some compromise between class-E and class-F operation (class E/F) may provide an optimum balance between bandwidth and linearity in a high efficiency quasi-optical power amplifier.

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APPENDIX A

EXACT SOLUTION OF THE ORIGINAL CLASS-E CIRCUIT

The original class-E circuit is shown in Figure A.1. To solve this idealized circuit exactly (without any high-Q assumption), a time-varying third-order set of differential equations must be solved. When the switch is in its ON-state, a second-order differential equation describes the circuit. When the switch is in its OFF-state, a third-order differential equation describes the circuit. The boundary conditions on the voltages and currents between the switch ON and OFF states combine the two equations into one time-varying third-order system. The waveforms are most nonlinear at the switch, and become mostly sinusoidal at the output resistor. It is easiest to begin with an equation for the voltage across the switch during the switch OFF-state (since the boundary conditions for class-E operation are defined for this voltage), but during the ON-state, this voltage is zero, so the voltage across the network capacitor C is used. Later, to combine the boundaries between the switch states, the switch voltage during the switch OFF-state is used to find the voltage across C.

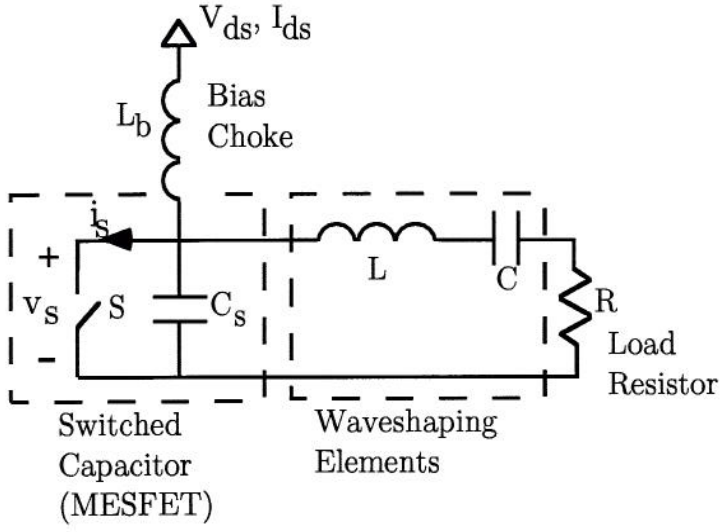

Figure A.1: Class-E high-efficiency circuit.

$$(0 \le t \le \frac{T_s}{2}) \quad \frac{\mathrm{d}^3 v_s}{dt^3} + \frac{R}{L}\frac{\mathrm{d}^2 v_s}{dt^2} + \frac{1}{L}(\frac{1}{C_s} + \frac{1}{C})\frac{\mathrm{d}v_s}{dt} = \frac{I_g}{C_s C L},$$

$$(\frac{T_s}{2} \le t \le T_s) \quad \frac{\mathrm{d}^2 v_C}{dt^2} + \frac{R}{L}\frac{\mathrm{d}v_C}{dt} + \frac{v_C}{LC} = 0.$$

The boundary conditions imposed upon $v_s(t)$ which define class-E operation are:

$$v_s(0) = 0,$$

$$v_s(\frac{T_s}{2}) = 0,$$

$$\frac{\mathrm{d}v_s}{dt}(\frac{T_s}{2}) = 0.$$

The basic solution for this class-E circuit is given below. Again, the voltage across the switch is given for the first half of the cycle, and the voltage across the second capacitor C is given during the second half of the switch cycle. Differentiation and integration of these expressions yields all of the currents and voltages in the circuit at all times.

$$(0 \le t \le \frac{T_s}{2}): \quad v_s(t) = K_1 + \frac{I_g t}{C_s + C} + K_2 e^{\frac{-tR}{2L}} \sin(t\sqrt{\frac{C_s + C}{C_s C L} - (\frac{R}{2L})^2}) +$$

$$K_3 e^{\frac{-tR}{2L}} \cos(t\sqrt{\frac{C_s + C}{C_s C L} - (\frac{R}{2L})^2}),$$

$$(\frac{T_s}{2} \le t \le T_s): \quad v_C(t) = A_1 e^{\frac{-tR}{2L}} \sin(t\sqrt{\frac{1}{CL} - (\frac{R}{2L})^2}) + A_2 e^{\frac{-tR}{2L}} \cos(t\sqrt{\frac{1}{CL} - (\frac{R}{2L})^2}).$$

Trancendental equations are derived which constrain the load network elements; these can be solved numerically for C_s and C. The results of the simplified analysis presented in Chapter 4 are used to find first-order element values, which can then be used as a starting point in the numerical solution of these equations. The equations derived here are exact, without the high-Q assumption used in Chapter 4.

$$A_2 = LC_s(\frac{RI_g}{2L(C_s + C)} + \sqrt{\frac{C_s + C}{C_s C L} - (\frac{R}{2L})^2} e^{\frac{-RT_s}{4L}}((-K_2\sqrt{\frac{C_s + C}{C_s C L} - (\frac{R}{2L})^2} + \frac{K_3 R}{2L})$$

$$\sin(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})-(\frac{K_2R}{2L}+K_3\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})\cos(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}))),$$

$$e^{\frac{-RT_s}{4L}}(A_1\sin(\frac{T_s}{2}\sqrt{\frac{1}{CL}-(\frac{R}{2L})^2})+A_2\cos(\frac{T_s}{2}\sqrt{\frac{1}{CL}-(\frac{R}{2L})^2}))=$$

$$LC_s(-\frac{R}{L}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}K_2+K_3((\frac{R}{2L})^2-\frac{C_s+C}{C_sCL}+(\frac{R}{2L})^2))+$$

$$RC_s(\frac{I_g}{C_s+C}+K_2\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}-K_3\frac{R}{2L})-RI_g.$$

The constants K_1, K_2, K_3, A_1, and A_2 are complicated functions of the circuit parameters (the circuit element values and the switching period):

$$K_1=\frac{I_g}{C_s+C}\frac{K_{1n}}{K_{1d}},$$

$$K_{1n}=\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}\cot(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})-\frac{RT_s}{4L}-1,$$

$$K_{1d}=\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}e^{\frac{-RT_s}{4L}}(\sin(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})+$$

$$\cos(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})\cot(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}))-$$

$$\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2}\cot(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})+\frac{R}{2L},$$

$$K_2=K_1(\cot(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})-e^{\frac{RT_s}{4L}}\csc(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})-$$

$$\frac{I_gT_s}{2(C_s+C)}e^{\frac{RT_s}{4L}}\csc(\frac{T_s}{2}\sqrt{\frac{C_s+C}{C_sCL}-(\frac{R}{2L})^2})),$$

$$K_3=-K_1,$$

$$A_1=\frac{A_{1n}}{A_{1d}},$$

$$A_{1n}=\frac{I_g}{C_2}(2L\sqrt{\frac{1}{CL}-(\frac{R}{2L})^2}\sin(\frac{T_s}{2}\sqrt{\frac{1}{CL}-(\frac{R}{2L})^2})\frac{1}{R}+\cos(\frac{T_s}{2}\sqrt{\frac{1}{CL}-(\frac{R}{2L})^2}))-Be^{\frac{RT_s}{4L}},$$

$$A_{1d} = (\frac{R}{2L} + 2L(\frac{1}{CL} - (\frac{R}{2L})^2)\frac{1}{R})\sin(\frac{T_s}{2}\sqrt{\frac{1}{CL} - (\frac{R}{2L})^2}),$$

$$A_2 = \frac{2L}{R}(A_1\sqrt{\frac{1}{CL} - (\frac{R}{2L})^2} - \frac{I_g}{C}),$$

$$B = \frac{I_g}{C} - \frac{C_s}{C}(\frac{I_g}{C_s + C} + K_2\sqrt{\frac{C_s + C}{C_s CL} - (\frac{R}{2L})^2} - \frac{K_3 R}{2L}).$$