Characterization and Design of a Low-Power Wireless Power Delivery System

by

Erez Avigdor Falkenstein

B.S., University of Colorado, 2010

M.S., University of Colorado, 2010

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

2011

This thesis entitled:

Characterization and Design of a Low-Power Wireless Power Delivery System

written by Erez Avigdor Falkenstein

has been approved for the Department of Electrical and Computer Engineering

_____

Zoya Popović

_____

Dejan S. Filipović

Date _____

The final copy of this thesis has been examined by the signatories, and we

Find that both the content and the form meet acceptable presentation standards

Of scholarly work in the above mentioned discipline.

Falkenstein, Erez Avigdor (Ph.D., Electrical Engineering)

Characterization and Design of a Low-Power Wireless Power Delivery System

Thesis directed by Professor Zoya Popović

This thesis focuses on a design methodology for low-power non-directional far-field wireless powering. The power receiver consists of one or more antennae which receive plane waves transmitted by the powering source, and deliver the RF power to a rectifying element. The resulting DC power is optimally transferred to the electronic application via a power management circuit. The powering is independent of the electronic application which can include wireless transmission of sensor data.

The design and implementation of an integrated rectifier-antenna at low incident power densities (from 25-200μW/cm^2) is presented. Nonlinear source-pull measurements and harmonic balance simulations are used for finding the optimal rectifying device RF and DC impedances for efficient rectification. Experimental results show that an antenna design with a specific complex impedance reaches the highest rectification efficiency. Several examples of the design methodology are shown. In specific, characterization of a linearly polarized rectifying patch antenna at frequency of 1.96 GHz is detailed, with an optimal RF impedance of $137 + j149\,\Omega$ and an optimal DC load of 365Ω resulting in RF to DC conversion efficiency of 63% (simulated) for the rectifier alone and 54% (measured) for the total rectifying antenna. A compact design (eliminating SMA connector) of a dual-polarized rectifier antenna integrated with two rectifiers, one for each polarization is detailed. The complications and issues of combining the powers from the two polarizations are addressed. A analysis of required RF and DC isolation in multiple-rectifier integrated rectifier-antenna is developed and confirmed. Measurement results of a

2.45 GHz integrated rectifier antenna show conversion efficiency of 56% and very small dependance on rotation angle between powering polarization and receiving rectifier antenna (ratio of maximum to minimum power as the antenna is rotated of 1.09).

Dedication

This thesis is dedicated to the memory of my inspiring father,

Eliezer O. Falkenstein (1938 - 1991).

Personal

Acknowledgments

I am truly grateful to my father for the engineering interest that he cultivated in me. My father, a holocaust survivor, an engineer [1, 2, 3, 4] and a friend of mine ("haver-sheli"), died December 13 th 1991. As a young child, I was encouraged by him to ask questions and be curious. Every mechanical or electrical toy I got form my parents also came with my fathers explanation of the concepts that made it operate. Words cannot convey my gratitude to my mother and sisters for always being supportive. I wish to thank my entire extended family for their support.

I owe my appreciation to the former and current research group members who have made graduate school a great experience: Dr. Jonathan Chisum, Rob Scheeler, Frank Trang, Mike Roberg, Asmita Dani, Jennifer Imperial, Xavier Palomer, Brad Lindseth, Dan Kuester (K pup), Scoot schafer, Dr. Evan Cullens, Dr. Negar Ehsan, Dr. Charles R. Dietlein, Dr. Mike Elsbury, Dr. John Hoversten, Dr. Miloš Janković, Dr. Nicola Kinzie, Dr. Qianli Mu, Dr. Mabel Ramírez, Dr. Néstor López, Dr. Luke Sankey and Dr. Leonardo Ranzani (The nard dog).

To Laura, who deserves applause for her patience dealing with me throughout the last few years of school; thank you for ignoring my faults and encouraging my merits. Last, but not the least, I'd like to thank our dog, Louie, who after long days at school, always greets me with lots of happiness.

Professional Acknowledgments

I am profoundly grateful to Professor Zoya Popović. Without her, all of the work in this thesis would of not been possible. She has provided guidance, motivation, opportunity and has developed an amazing research group.

I cannot express my appreciation to Daniel Costinett from the Power Electronics group, who has always been willing to help with any problem, regardless of relevance to his own research or time constraints.

I am very grateful to the countless others how have provided guidance and advice throughout the research leading to this thesis including, professor Regan A. Zane, Dr. Thurein Paing, Dr. Joseph Hagerty and all of the microwave and RF group members for many helpful discussions.

Last, but certainly not the least, I would like to thank my committee, Prof' Zoya Popović, Prof' Edward F. Kuester, Prof' Dejan S. Filipović, Prof' Regan A. Zane, Prof' Richard T. Mihran and Prof' Penina Axelrad, for taking the time to teach me and listen to me.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

Thought is a strenuous art - few practice it, and then only at rare times.

—David Ben-Gurion

Contents

1.1 MOTIVATION

1.1.1 Introduction

Many electronic devices operate in conditions where it is costly, inconvenient or impossible to replace a battery, or deliver wired power. As a result there has been an increased demand for wireless sensors for data gathering and transmission. Often

the data is gathered at locations with accessibility issues, sensors need to be covert and where the sensor maintenance is not trivial. Some examples are implanted sensors for medical diagnostics and therapy [5], structural monitoring sensors [6], sensors inside hazardous manufacturing or other hazardous environments, sensors for health monitoring of patients or in assisted living environments [7], aircraft health monitoring [8], sensors for covert operations, etc. For any low power sensor that operates at a low duty cycle, and in an environment with low levels of light or vibration, RF wireless powering offers the potential for maintenance-free operation.

1.1.2 Background Survey

In the past, wireless power beaming with directive antennas has been demonstrated for various applications such as solar power satellite (SPS) where power would be collected on large solar panels and beamed to earth or power transfer from one part of a satellite to another as illustrated in Fig 1.1. [9, 10, 11, 12, 13]. In

(a) (b)

Figure 1.1: Microwave power transmission experiment in space on a small satellite and on the International Space Station.

most of this work, directive antennas were used with high power densities, on the order of a few $10^4 \mu W/cm^2$ with efficiencies ranging from 20% to 80%. In 1975 Jet Propulsion Laboratory (JPL) and Raytheon demonstrated power transfer on gourd to validate this concept [14]. In this experiment power was transferred over

1.6 km. The transmitted power was 450 kW and the DC power recovered by a the rectifying antenna with an area of 24 m^2 was 30 kW. The proposed SPS in [10], is a satellite placed in geostationary orbit and generating very high power levels, on the order of 5 GW. The power would be generated by solar cells and be transmitted at a frequency of 2.45 GHz to the rectifying antenna on the ground, a photograph of the proposed rectifying antenna is seen in Fig. 1.2. The rectifying antenna array is composed of 256 sub-arrays, each composed form 9 elements totaling at 2304 elements.

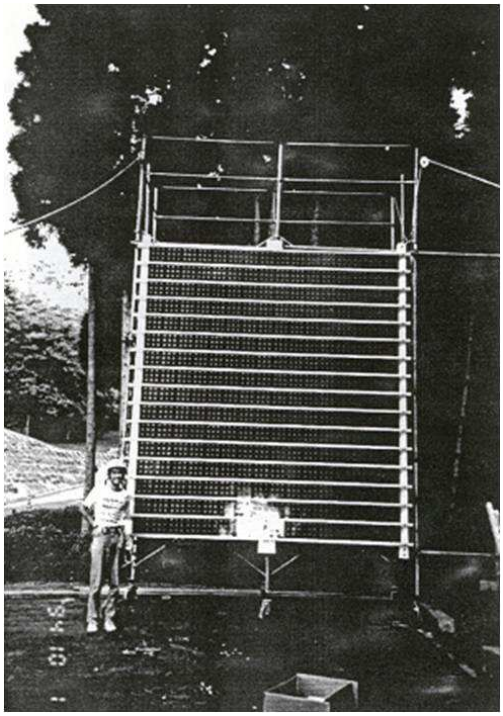


Figure 1.2: The rectifying antenna array used in Shinohara's field experiment at a frequency of 2.45 GHz. The size is 3.2 m × 3.6 m.

In [15], a large dipole array (8 by 6) with a 5 $\mu W/cm^2$ incident power density was coupled to a single rectifier with a corporate feed. This is the first low-power density rectifying antenna work reported in the literature, the power densities are a factor of 10000 times less than the previous work. Since a corporate feed is used, the incident power to the rectifying diode is the power collected by all

array elements and is on the order of 20 mW. According to [15], that is the power level where efficiency is maximized for the diode used in that work. Combining the power from all elements of the array increases the power to the rectifier, but the non-directive properties of the single element rectifying antenna are lost. In [16], 64 spiral antenna elements with integrated Schottky diodes with connected DC lines, seen in Fig. 1.3, were used to receive and rectify very low power densities in the $\mu W/cm^2$ range. In this work, each antenna element is connected to a rectifying diode, keeping the non-directive properties of each element. In addition, the power is collected from any arbitrary polarization incident on the rectifying antenna array.

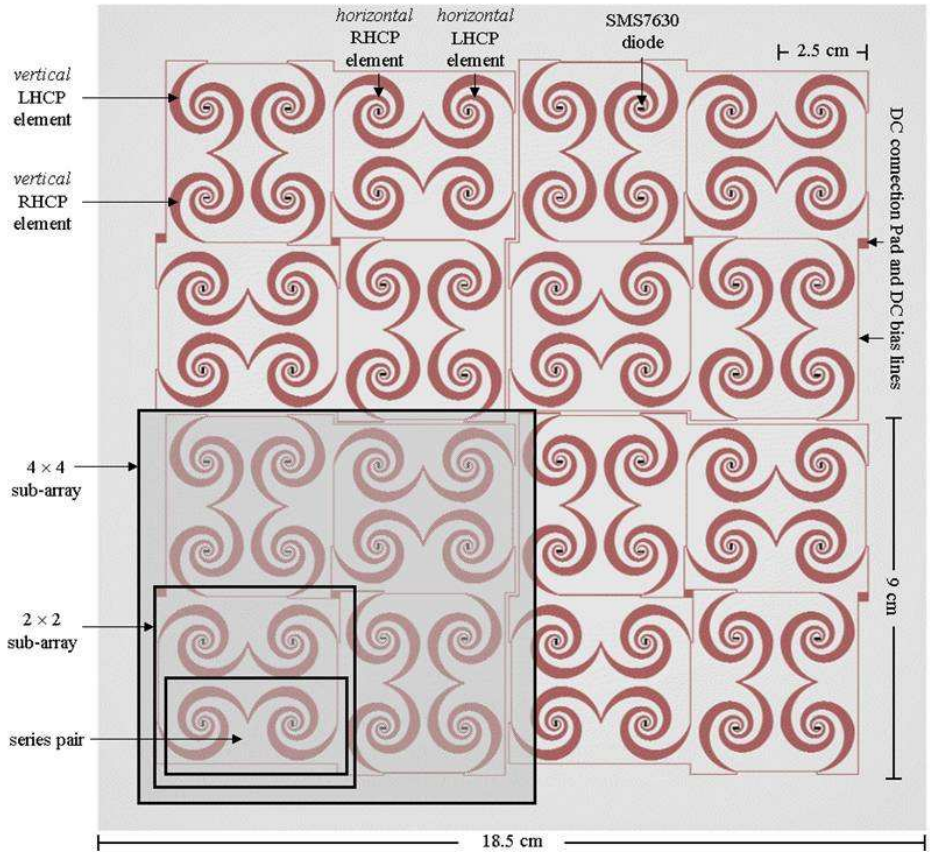


Figure 1.3: Layout of the 64-element array. Received RF power is rectified at each spiral locally and the combined dc power for all elements is extracted using two dc collection lines at the edges of the array (not shown).

Wirelessly powered devices include RFIDs, these devices are widely used for supply chain management and inventory control. The RFIDs are powered by the interrogating radio-frequency wave, typically in the UHF frequency range [17] [18]. Usually, the RFID distances are short and the device operates only when the interrogating wave delivers sufficient power density to the usually inefficient RFID antenna. Since the wavelength used for powering is larger or on the order of the powering range, the antennas on the power transmitter and RFID tag are in each other's near fields, and the energy is transferred via either capacitive or inductive coupling. In recent years, the field of active RFID has been evolving. Active RFID tags have a built in power supply, such as a battery, as well as electronics that perform specialized tasks independent of the interrogating signal. Since the tags have a power supply that needs charging, the fields of active RFID and far-field wireless powering are merging [19, 20]. However, the approach in this thesis differs from active RFID in that the powering is done independent from the interrogation signal.

In addition to RFIDs, other near-field powered RF devices include toothbrushes, implants [5], resonantly powered devices [21] and recently, different phone and tablet-computer chargers [22]. The principle of operation is of a power transformer, where by magnetic induction, the power is transferred form the primary coil to the secondary coil. In [22] the efficiency is increased by using resonant structured for the transmit and receive coils at the same frequency. A photograph of a 60 W light-bulb powered from a 2 m distance is shown in 1.4.

1.1.3 Low-Power Non-Directional Wireless Powering

In this work, we investigate single integrated antenna-rectifier elements with incident power densities in the 25-200 μW/cm^2 range. This thesis focuses on a design methodology for low-power non-directional far-field wireless powering. In the block

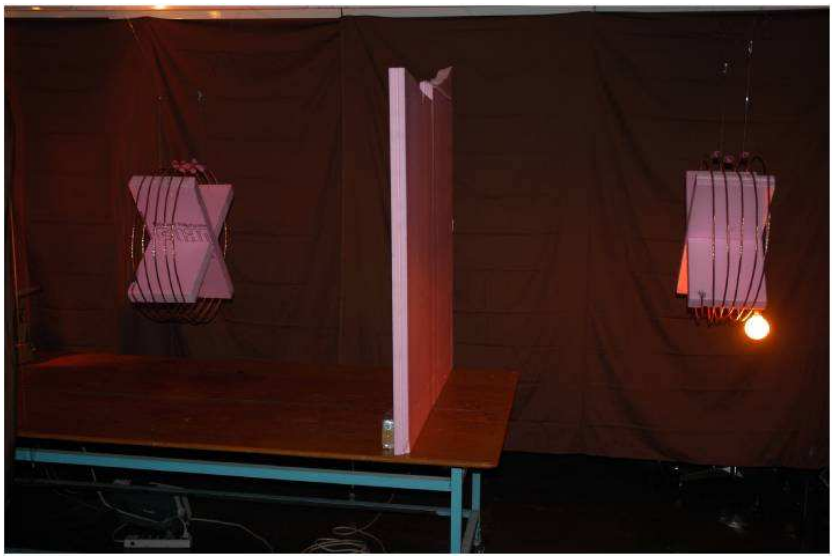


Figure 1.4: 60 W light-bulb being lit from 2 m away. Note the "obstruction" in the center. The loop radius is 25 cm and the frequency is 9.9 MHz.

diagram in Fig. 1.5, the power receiver consists of one or more antennae which receive plane waves transmitted by the powering source, and deliver the RF power to a rectifying element. The resulting DC power is optimally transferred to the electronic application via a power management circuit. The powering is independent of the electronic application which can include wireless transmission of sensor data [7].

Table 1.1 gives an overview of example far-field power receiving devices described in the literature. It is important to note that the efficiencies are listed as reported in the papers, but they cannot be directly compared due to the different power levels and perhaps more critically, different efficiency definitions. For example, most work, does not include the antenna efficiency or coupling efficiency from antenna to the rectifier. The power incident on the rectifier is measured in a circuit with no antenna or estimated from simulation. In some cases, the incident power density is also provided. In [23, 24, 25, 26, 30] power levels incident on the diode are in 100mW range with 40% to 82% rectification efficiency. In [30], the rectifier was directly connected to a generator, with no antenna. In [27], the 42% efficiency is measured

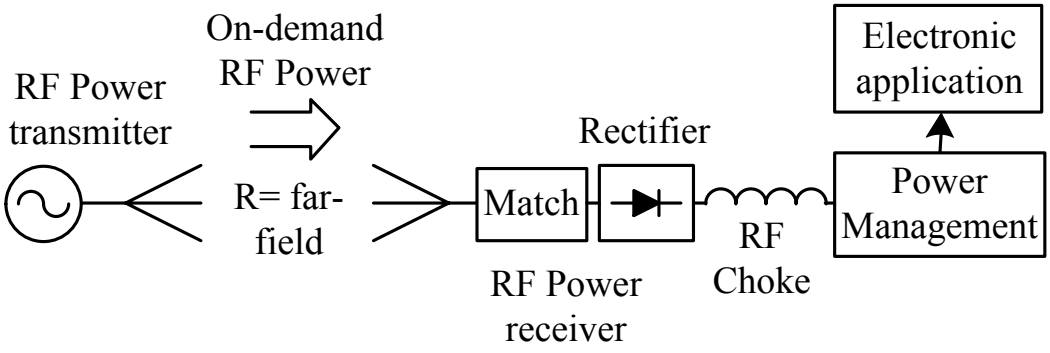


Figure 1.5: Block diagram of a wireless powering system. An RF power transmitter transmits a plane wave incident on a rectenna element or array (RF power receiver). Following rectification is a DC stage with power management. In this paper, we consider a narrowband low power non directional power transmitter. The electronic application for this study is a wireless sensor platform. The power density at the receiver is between 25 to 200μW/cm^2.

Table 1.1: Overview of integrated rectifier antennas and rectifiers described in the literature.

Ref	f (GHz)	$P_{RF,in}$	Antenna	η
[23]	5.8	50mW	LP dipole omni-dir	82%
[24]	5.8	105mW	LP dipole omni-dir	67%
[25]	2.45	316mW	LP 4 element patch array	65%
[26]	2.45	100mW	LP Patch on $FR4$	40%
[27]	2.45	0.1mW	LP miniaturized patch	42%
[15]	2.45	20mW (5 μW/cm^2)	48 element LP dipole array	50%
[28]	2.45	1mW	LP Patch	50-80%
[29]	2.45	10mW (150 μW/cm^2)	LP Patch	52%
[30]	5.8	40mW	LP printed grounded ant	59.5%
[16]	$2-18$	62 μW/cm^2	64 dual CP spiral elements	20%*
This	1.96	25-200 μW/cm^2	LP Patch	54%*
Work	2.45	25-200 μW/cm^2	Dual LP Patch	58%*

* η-Rectification efficiency; includes antenna efficiency,mismatch and coupling.

as the ratio of the DC power and the estimated input power to the diode of 0.1 mW for a fairly large antenna area whose total dimensions not given in the paper. In [15], a 48-element dipole array with a corporate feed was coupled to a single diode, allowing high input power to the diode at low power densities ($5\mu W/cm^2$), but loosing the individual rectifier antenna pattern properties and thus, with a strong dependence on antenna orientation due to high antenna array gain. In [28], the diode impedance is optimized at the fundamental frequency with harmonic balance non-linear simulations for 1mW of power incident on the diode, however then the diode is matched to a $50-\Omega$ antenna. The efficiency calculation was done by estimating antenna gain when the antenna is not connected to the rectifier, so at least a part of the antenna efficiency is taken into account by simulations. [29] reports rectification as well as overall integrated rectifier antenna efficiency also found from simulated unloaded antenna gain for 10mW estimated incident power on a 4-diode rectifier. The rectifier is integrated with the antenna on the same substrate and the overall device is compact. [16] presents 64 DC-connected dual-circularly polarized broadband spirals with diodes directly connected at the feeds and with very low incident power density and with at most 20% efficiency calculated from incident power density and total antenna area.

This work reports both single and dual linearly-polarized patch antennas with total efficiencies over 50%, including antenna, coupling, rectification and DC network losses.For $25-200\mu W/cm^2$ to the best of my knowledge, the efficiencies reported here are the highest demonstrated for the power levels of interest. Because of the multiple efficiency definitions present in the literature, it is difficult to compare the efficiency numbers directly. Clarifying and standardizing the efficiency definitions is important for practical applications of RF energy harvesting, and an attempt of defining the most conservative approach is given in Section 5.2.2.

1.1.4 Thesis Outline

This thesis details research performed on non-linear rectifier circuit analysis, experimental validation, and application to wireless powering for wireless sensor platforms. The thesis is organized as follows:

- Chapter. 2 discusses wireless sensor platform architecture and integration and has the goal to explain the requirements for the integrated rectifier and antenna which act as the far-field RF power front end receiver. In specific, low-power circuit approaches to the power management and control portions of the sensor are discussed. This work was done in collaboration with Prof. Regan Zane's group and the Colorado Power Electronics Center (CoPEC) at the University of Colorado.

- Chapter. 3 develops an analysis of nonlinear rectifiers and derives the conditions necessary for high efficiency rectification. The theory is done assuming diode rectifying devices, but is also applicable to transistor rectifiers. Time-domain waveforms across the rectifying element are derived and the relationship between their shape and RF-DC conversion efficiency is discussed in detail.

- Chapter. 4 presents methods for experimental-based rectifier modeling and non-linear frequency-domain simulations of microwave rectifiers, and the agreement between them. The close correlation between the two, which follows trends from Chapter. 3, provides confidence in the non-linear simulation for future designs.

- Chapter. 5, the integration between rectifiers and antennas for wireless powering is addressed and a method developed that results in maximized efficiency. The method is demonstrated in simulation and experiment on

the example of a patch antenna and Schottky-diode single-ended rectifier. Calibration, circuit validation, impedance matching to nonlinear impedances, DC collection circuit design and integrated rectifier-antenna characterization is presented in detail.

- Chapter. 6 extends the method from Chapter. 5 to a dual-polarized patch antenna and presents a comprehensive analysis of required RF and DC isolation in multiple-rectifier rectennas.

- Finally, Chapter. 7 summarizes the thesis contributions and gives some directions and preliminary results for future research in this interesting area of microwave engineering.

Chapter 2

Wirelessly Powered Sensor Platforms

When you have two alternatives, the first thing you have to do is to look for the third that you didn't think about, that doesn't exist.

—Shimon Peres

Contents

2.1 Introduction

Wireless sensors ar becoming common for many applications, due to the availability of very low power transceivers (e.g. Texas Instruments CC2500 or Nordic Semiconductors nRF24L01) and microcontrollers (e.g. Texas Instruments MSP430). Usually the wireless transmission is done in the ISM bands, most commonly 900 MHz and 2.45 GHz, moving towards the 5.8 GHz band. Wireless sensor platforms are integrate sensors, power harvesting and low power controllers and transceivers in to one unit. The integration and co-design of the platform as a system allows optimal configuration and overall lower power consumption as is described in the rest of the chapter.

Many of the sensors are used in different applications where changing a battery my be hard, expensive or impossible. In addition to examples from Chapter 1 applications include; habitat and environmental monitoring [31], volcano monitoring [32], structural monitoring [33, 34, 35], health monitoring of patients [7]. A major limitation of wireless sensors is the limited battery life. One solution is increasing the battery capacity, but that comes at the expense of size, weight and cost [36]. Energy harvesting is a solution that could be long lasting and inexpensive in the long run. Exploiting energy sources that exist in the operating space of the sensors, raises the possibility of very long lifetime. Since power harvesting for sensor platforms is done on a small scale, the platform must be efficient at low powers (efficient at power conversion and low overhead control power) [37]. A wireless sensor platform block diagram is shown in Fig. 2.1 Extensive research has been conducted on a large scale of harvesting solar, wind ,geothermal energy and electromagnetic beaming [38, 39]. For sensor platforms that require powering on a much smaller scale, the problems and issues are very different, and previous large-scale energy harvesting approaches are not applicable [40].

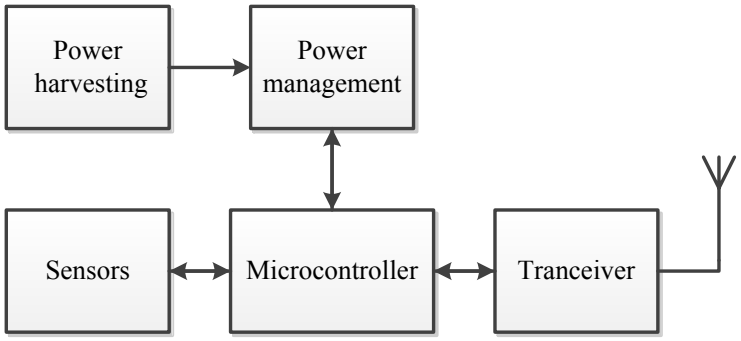


Figure 2.1: Basic sensor platform block diagram. The power harvesting could be one of many sources (solar, electromagnetic, wind, etc). The power management is responsible for maintaining the correct voltages to all components of the platform and storing the harvested energy. One or more sensors are connected to the microcontroller and provide measurement data as demanded. The transceiver transmits data packets of the sensed data and can receive control commands from base station. The microcontroller provides all timing and control signals to all of the components of the platform.

2.2 Energy Sources for Wireless Sensors

There are many potential sources of stray energy to be harvested such as solar, wind, heat, mechanical vibration, acoustic and electromagnetic.

Solar energy is available in many environments and convenient to use. If the sensor node is exposed to sun light for a big portion of the time this is a good source. Many sensor nodes were developed for solar harvesting for different applications [41, 42, 43]. The power density from photo-voltaic is $15\,\mathrm{mW/cm^2}$ while exposed to the sun [41]. The power circuitry for optimally loading a photo-voltaic could become complicated when the illumination conditions change, as a result, the overhead control power could become significant. Fig. 2.2 is an example of a small ($27 \times 67\,\mathrm{mm}$) solar panel powering a Cymbet energy harvesting platform [44].

Wind is a renewable energy source that is widely researched on a large scale. Research is focused mostly on large turbines for connection to the main power

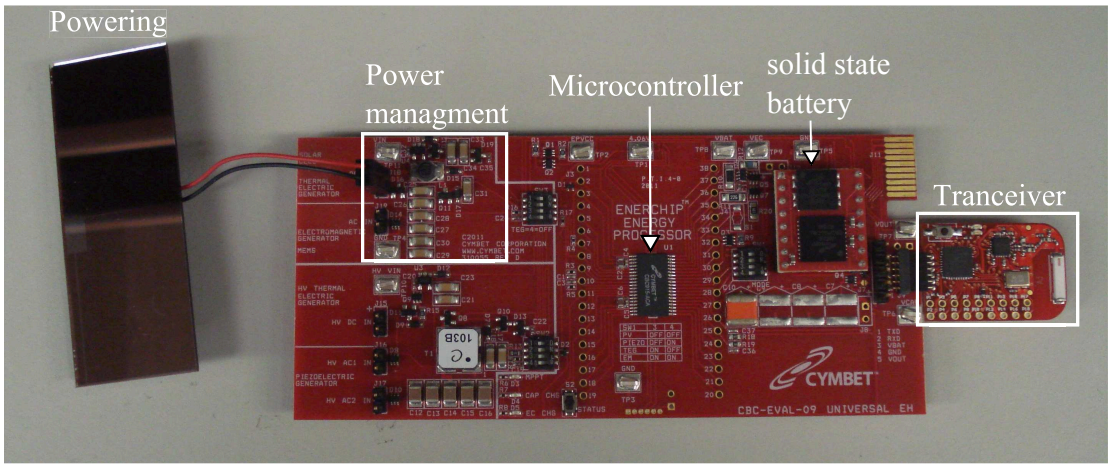


Figure 2.2: ($27 \times 67\,\text{mm}$) solar panel powering a Cymbet CBC-EVAL-09 energy harvesting platform while measuring temperature. The same board has capability to harvest power from thermal, vibration and electromagnetic energy as well. This board is an evaluation board with many test points, a board with the same capability can be much smaller as seen later this chapter.

grid [45]. Research of small scale wind harvesting is not widely reported in the literature but, some research has been done in the field and reported in [46, 47, 48].

The main disadvantages with wind power is the difficulty to predict the wind ahead of time, constantly changing wind strength, unreliability due to may mechanical moving parts as seen in Fig. 2.3 and noise due to the moving parts [40]. For applications where turbines are used regardless of power harvesting such as in [46], wind may be the best solution. Otherwise, for small scale power harvesting, reliability issues rule out wind harvesting.

Thermal energy or the use of thermal gradient for conversion to electric energy is done using thermocouples. Thermocouples are devices where an output voltage is proportional to the temperature difference between the two materials forming it. Such thermocouples have been arrayed to create large potential differences. Thermoelectric power generators have been proposed to generate electricity from body heat or any environment where there is a temperature gradient [49]. Prototypes of wireless sensors placed on a human body and powered by the temperature

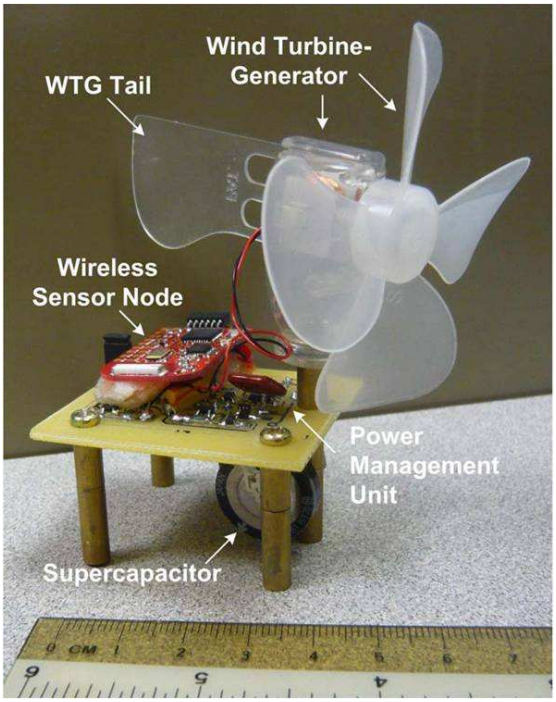


Figure 2.3: photograph of prototype of sensor node powered by wind energy harvesting developed by Yen Kheng Tan.

difference have been demonstrated in [50].

Mechanical vibrations are observed in a very wide spectrum of frequencies. The conversion of vibration to electric power is optimal if the frequency of vibration matches the eigenfrequency of the mechanical to electric power converter [51]. In some environments with high vibration such as suspended bridges or running shoes [51, 52, 53], this is a good source of energy although it could be hard to get a stable constant source of vibrations.

This work focuses on improving efficiency of delivering power wirelessly to a low-power wireless sensor platform with an electrically small antenna, at most one wavelength on the side. "Low power" in this work refers to less than $200\,\mu\mathrm{W/cm^2}$ of incident power density of an electromagnetic wave in the radio frequency range of the spectrum [16]. Specific frequencies are considered that either are in unlicensed (ISM) bands, such as 2.45 and 5.8 GHz, or frequencies where power is radiated

for other applications and can potentially be scavenged, e.g. the 1.96 GHz cellular band and S & X radar bands. Far-field powering implies plane wave propagation between antennae at longer range, can be done without line of sight, and is less sensitive to the orientation and position relative to the transmitting antenna. Few applications have taken advantage of this technology for harvesting energy at sub-milliwatt power levels attributed to the challenges associated with optimizing the interface between the power reception device, and typical low-power sensor loads to achieve high overall efficiency. This work addresses a method for improved far-field powering efficiency at low incident power densities by integrated design of the power reception device and power management circuit. It differs from radio frequency identification (RFID) devices in that the powering is independent of signal transmission and is done at different time scales, power levels and frequencies.

2.3 Approach

A block diagram for the prototype described in this work is shown in Fig. 2.4. An antenna integrated with a rectifier receives arbitrarily polarized radiation at levels at or below 200 μW/cm^2. The DC output is managed by a digitally controlled power converter in such a way that it always presents an optimal DC load to the energy storage device, which provides power to the microcontroller, sensor and data transceiver. The sensor data is input to a commercial low-power wireless transceiver operating in the 2.4 GHz ISM band. The data transmission is the most power-consuming task and is not done continuously, which is acceptable for most applications. If there is not enough stored energy, the data cannot be transmitted and there is danger of damaging the storage device. Therefore, the available rectified RF power and the available energy stored are monitored in a closed-loop system allowing for adaptive adjustment of the data transmission duty

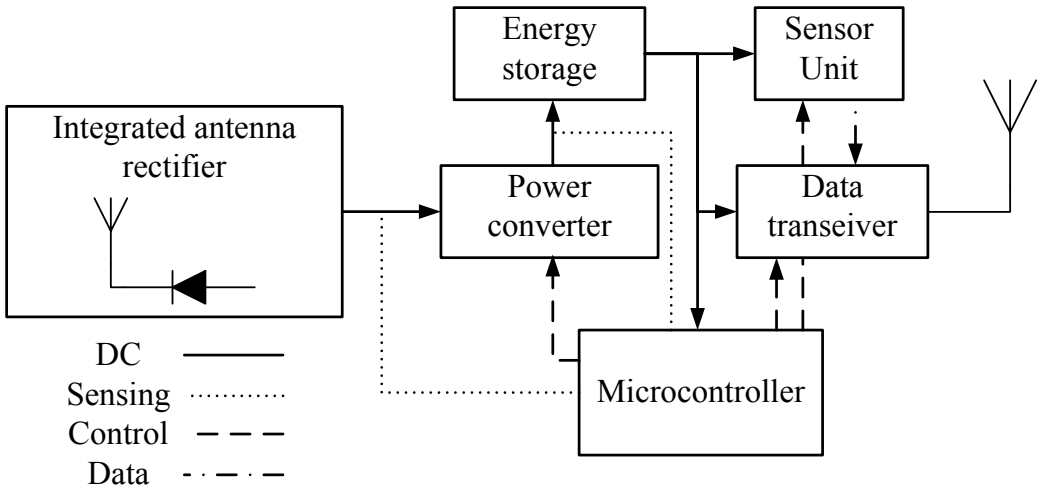


Figure 2.4: . Block diagram of far-field RF-powered wireless sensor. The available rectified RF power and the available energy stored are monitored (shown in dotted lines) allowing for adaptive adjustment of the data transmission duty cycle. The low-power microcontroller provides control to the power management circuit, wireless transceiver and sensor. The power is collected in the far field of one or more ISM transmitters at 5.8 GHz or 2.45 GHz, independently of data transmission.

cycle.

2.4 RF Power Reception

An integrated antenna rectifier (often termed "rectenna") is designed to receive arbitrary polarized radiation at low incident power densities. Integrated rectifier antennas for reception have been demonstrated earlier with high RF-DC conversion efficiency, e.g. [23], but for significantly higher incident power densities and with linear polarization. Discussion of issues, design methodology, simulations and experiments are detailed in Chapter 3 and 4. In an unknown multipath environment, the polarization is random, and it has been shown that rectifying two orthogonal polarizations independently and adding the resulting DC power increases overall efficiency [16, 54]. Issues and methods of combining power from both polarizations are discussed in Chapter 6. A photograph of an example dual-linearly polarized

patch antenna at 5.8 GHz fabricated on a Rogers 4350b substrate [55] is shown in Fig. 2.5. Two Skyworks Schottky diodes [56] are connected to the centers of the radiating edges at the high-impedance points. Each diode rectifies power received in one polarization, and is in the voltage null for the orthogonal polarization, providing polarization diversity.

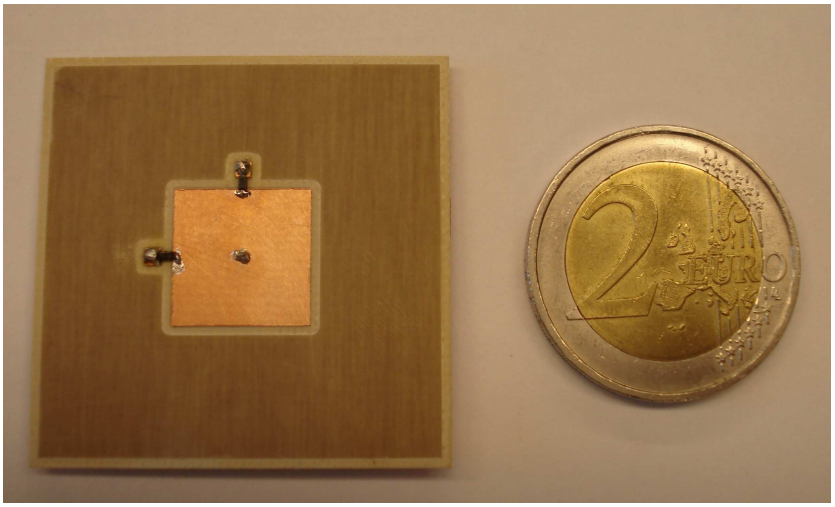


Figure 2.5: Photo of integrated antenna rectifier for 5.8 GHz dual polarization reception and rectification. The antenna is fabricated on a Rogers 4350b substrate, and the diodes are soldered to the high-impedance points. The two DC connections are taken from the diode terminals and through an isolated via in the voltage null of the patch, which is 1.3cm squared in size.

2.5 Power Management

As seen in Fig. 2.4, the power management, sensing and transmission load are controlled by a single Texas Instruments MSP430F2132 low-power microcontroller. In contrast to previous work, the co-design of converter and sensing/transmission load, as well as the integrated antenna rectifier and power management, is presented here. This integration allows the microcontroller to dynamically control converter operation to maximize the harvested power P_h and to control the average load power P_l to match P_l to P_h. The power flow of the system is shown in Fig. 2.6.

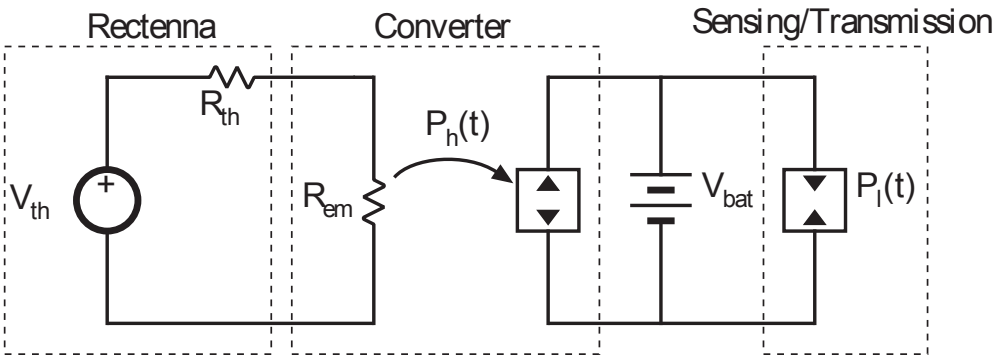


Figure 2.6: Averaged model of the converter, integrated antenna rectifier, and load.

The converter ideally acts as a lossless resistor R_{em} at the input port and transfers input power to the battery at the output port. when presenting the optimal integrated rectifier antenna load, this operation results in maximum input power P_h from the integrated antenna rectifier. With changing incident RF power densities, if R_{em} of the converter input port is maintained equal to the integrated antenna rectifier optimal DC load at that density, the optimal conditions are kept.

The power converter implementation, shown in Fig. 2.7, is an asynchronous DCM boost converter, whose output is a Seiko MS412FE battery with a nominal voltage of 2.5V (other batteries with different capacity and votage could be used, for example Cymbet EnerChip CBC050-M8C [57]). The battery decouples the converter from the load by storing or providing any energy resulting from a temporary mismatch between P_l and P_h. The converter is controlled by the MSP430 microcontroller through a gate drive signal that has both a high-frequency period and duty cycle, T_{HF} and D, and a low-frequency period and duty cycle, T_{LF} and k, which are altered in order to extract the maximum power from the integrated antenna rectifier.

When operated in DCM, as is guaranteed at the low power levels present in this application, the boost converter input port has the desired resistive average

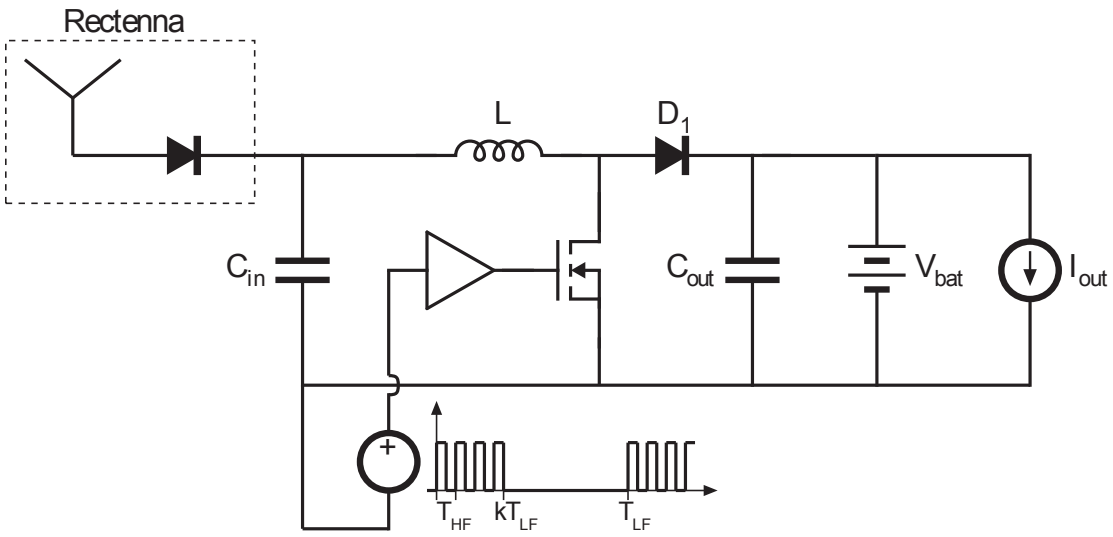


Figure 2.7: Circuit diagram of the converter portion of the power management module. I_{out} represents the load on the battery presented by the control, sensing, and transmission circuitry.

behavior with value

$$R_{em} = \frac{4L}{DT_{HF}k} \tag{2.1}$$

which is valid under the assumption $V_{bat} \gg V_{in}$ [7]. This averaging is valid for frequencies well below T_{LF}, and assumes input capacitance C_{in} large enough to maintain negligible voltage ripple across one low-frequency period. Important waveforms of converter operation are shown in Fig. 2.8. The high frequency period T_{HF} is chosen based on a tradeoff between the increased control oscillator current I_{osc} required at high frequencies and reduced converter efficiency due to the discharge of C_{in} during kT_{LF}. Inductance is optimized offline, based on a sweep of all possible timing parameters and estimated losses in the converter, with results of the sweep and measured efficiency shown in Fig. 2.9 for a $100\,\mu H$ inductor.

Compared to previous circuits, e.g. [7, 58], this implementation has increased control losses due to the use of a microcontroller. However, in previous demonstrations a microcontroller was a part of the sensing/transmission load, which was

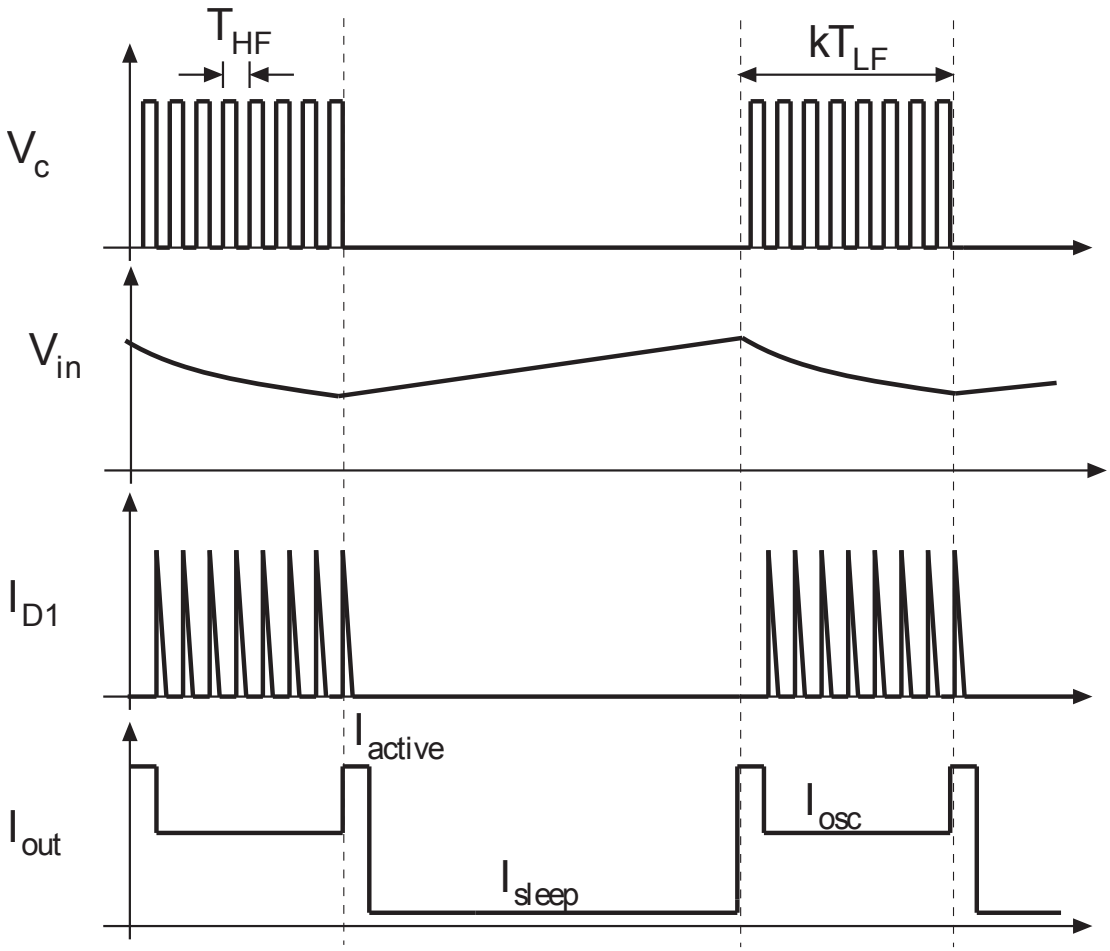


Figure 2.8: MOSFET switching waveform Vc, Converter input voltage V_{in} (with exaggerated ripple), diode current I_{D1}, and battery load current I_{ctl} caused by the generation the gate drive signals.

not integrated and thus not included in loss calculations. Significant conduction losses in the inductor are also present due to its small size and relatively high equivalent series resistance (ESR). The resulting circuit has higher integration, with a single Texas Instruments MSP430F2132 low-power microcontroller, controlling the converter, sensing, and transmission, with board area about 1/5 the size of that demonstrated previously.

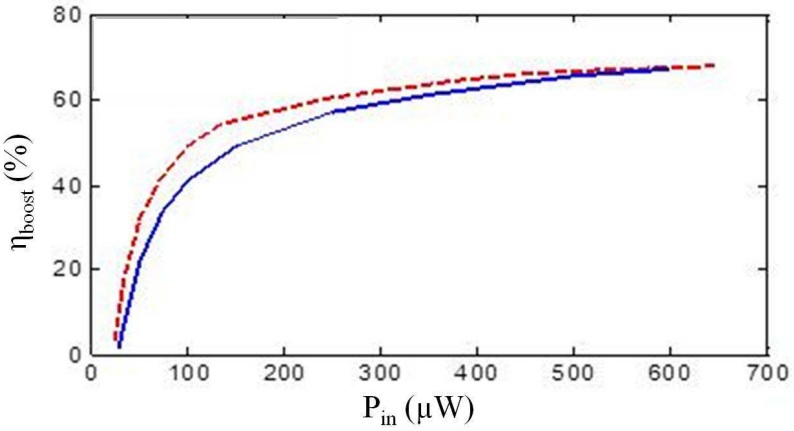


Figure 2.9: Measured and predicted efficiency of circuit as a function of available input DC power.

2.6 Load Management

Referring to Fig. 2.6, the goal of the load management control is to match the average power consumed by sensing and transmission of data to the average power harvested from the converter circuit. If the device is not actively sensing or transmitting, the processor is allowed to go into a sleep mode, waking only into active mode briefly on the rising and falling edges of the low-frequency interval, as shown in Fig. 2.8. When the device is sensing, however, the processor remains in active mode after the kT_{LF} interval for a period of time long enough to sample input and output voltages as well as any application-specific sensors, then transmits the data. The average current taken from the $2.5\,V$ battery during one sensing and transmission cycle is integrated to obtain the energy per transmission,

$$W_{trans} = 20.5\,\mu J \tag{2.2}$$

as in [58].

Because the input port acts as a known resistance, R_{em}, input voltage sensing is sufficient to allow estimation of input power, and the transmission period T_{sense}

is set to match the power consumed during transmission to the harvested power:

$$P_h = \eta_{boost}\left(\frac{V_{in}^2}{R_{em}}\right) \approx \frac{W_{trans}}{T_{sense}} \tag{2.3}$$

To account for mismatch between P_l and P_h, a battery monitoring routine checks the battery voltage to determine the state of charge and can enable/disable both transmission and converter operation if the battery is at risk of overcharging or discharging completely. For battery voltage below $2.2\,V$ (90% discharged), all transmission is disabled. If the measured input power is below $25\,\mu W$, the converter is disabled, the controller enters the sleep mode with $2.5\,\mu W$ power consumption, and the Rem load on the integrated rectifier antenna is no longer maintained. For battery voltage above $2.85\,V$, the converter is shut down so that no further power is sent to the battery and transmission is allowed to continue at the highest duty cycle until the battery voltage drops below $2.8\,V$. When the entire circuit is tested in an anechoic chamber as a function of incident power density, the results shown in Table. 2.1 were measured. The transmission duty cycle adaptively decreases with RF power decrease.

Table 2.1: Adaptive transmission test results using 5.8 GHz patch integrated rectifier antenna. Negative I_{bat} indicates net power flow into the battery.

	V_bat $[V]$	S_{RF} $[\mu\mathrm{W/cm^2}]$	$V_{Rectenna}$ $[V]$	T_{sence}^{-1} $[Hz]$	I_{bat} $[\mu A]$
Regular operation conditions	2.5	150	0.826	5	-63.1
		105	0.697	1.5	-57.2
		50	0.505	1.5	-23.4
		30	0.342	0.4	-10
		12.5	0.182	-	-0.4
Overcharge	3	50	0.801	20	132
Discharge	2	50	0.501	-	-43.5

A photograph of the fabricated circuit board including the boost converter,

control circuitry and temperature sensor is shown in Fig. 2.10.

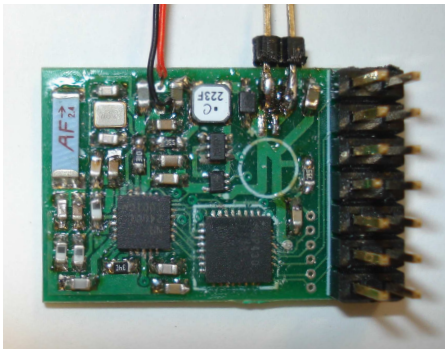


Figure 2.10: The 2.1x1.7 cm circuit contains both power management and sensor/transmitter circuitry.

The transmission current diagram is shown in Fig 2.11, with a sleep current of less than $1\,\mu A$ at $2.5\,V$. The wireless sensor platform is capable of transmitting bursts of 2 Mbps of data with less than 8 mA.

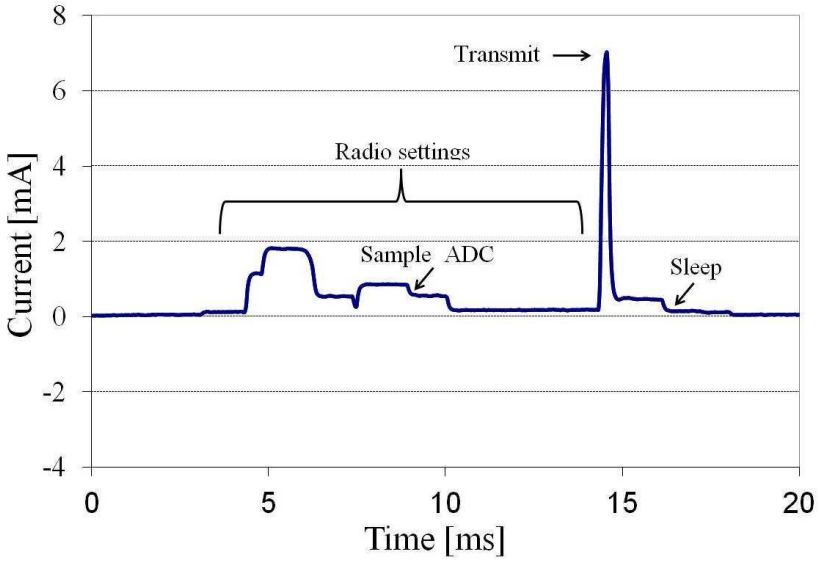


Figure 2.11: Measured total current consumption of the circuit described in Fig. 2.4 and shown in Fig. 2.10.

2.7 Summary

In this chapter, the integration of a wirelessly powered wireless sensor platform is discussed. The architecture is focused on low-power low duty cycle data transmission and is used to explain the requirements for the integrated rectifier and antenna which act as the far-field RF power front end receiver. In specific, low-power circuit approaches to the power management and control portions of the sensor are overviewed. The discussion of the sensor as a system shows how the theory and experiments in this thesis enable low-power maintenance-free wireless sensors. The work presented here was done in collaboration with Prof. Regan Zane's group and the Colorado Power Electronics Center (CoPEC) at the University of Colorado. The contributions from this thesis in the context of sensor platform integration are presented in the following publications: [58, 59, 60, 61]

Chapter 3

Microwave Rectifier Analysis

Anyone who has never made a mistake has never tried anything new.

—Albert Einstein

Contents

3.1 Introduction

For microwave rectifiers at low input power levels (a few mW) the full-wave rectifier approach is not efficient and a single-diode rectifier should be considered [62, 63].

As the input power is lowered, the forward bias voltage (which is constant) becomes more significant in relation to the input RF voltage. Since the forward bias voltage is constant, the power loss within the diode increases in relation to the total power as the input power lowers. A single-diode rectifier allows turning the diode on only once during each cycle and dissipating power only during that forward bias period. The diode is a nonlinear device that provides harmonic content to the system. In order to create a rectifier with high RF-to-DC conversion efficiency the following conditions must be met: (a) low reflections at the fundamental frequency, maximizing power transfer to the diode; (b) harmonic terminations reducing voltage and current overlap; (c) the DC load maximizing the DC power (0 order harmonic).

The rectifying element used in this work is a Schottky diode. The conversion of RF-to-DC power is the result of a nonlinearity provided by the Schottky diode. In this chapter, the theoretical rectification concepts are discussed, starting with a simplified diode model and building up in complexity to a model that closely predicts the device behavior and explains power conversion and dissipation within the diode. The non-ideal elements of the diode are evaluated to give a frame for diode selection according to Spice model parameters. Some 1.96 GHz and 2.45 GHz Agilent ADS simulation results are provided to illustrate the analysis concepts. Similarities to the waveforms of high efficiency amplifiers are addressed and some topologies of amplifier/rectifier classes are discussed.

3.2 Time-Domain Analysis

Time-domain voltage waveforms as a function of input RF voltage and DC load and the diode I-V curve give quantitative insight into efficiency improvement possibilities. In [23], time-domain analysis was used to determine rectifying diode impedance

maximizing power transfer to the diode but neglecting harmonic conditioning to further efficient rectification.

Consider the simplified model of a rectifying diode shown in Fig. 3.1, where the junction is an ideal switch with a constant voltage drop as described by the ideal IV curve in Fig. 3.2. Notice that while the switch is open the voltage across the diode is equal to the input voltage and no current is flowing through the diode, hence, no power is dissipated in the diode. When the switch is closed, the voltage across the the diode is the forward bias voltage and current can flow through the diode. In this period, power is dissipated in the diode since current and voltage exist simultaneously. In the ideal case where $V_f = 0$, the rectifier would be 100% efficient since there is no overlap of voltage and current through the rectifying device. On the other hand, using the model described in Fig. 3.3 where during the forward bias period a voltage (V_f) exists and there is a current through the diode (I_d), there is some loss. The current can be written as:

$$I_d = \begin{cases} I_d = 0 & \text{diode off} \\ I_d = V_{RF}/R_j & \text{diode on} \end{cases} \tag{3.1}$$

Using the diode model of Fig. 3.3, high RF-to-DC conversion efficiency is reached by minimizing the portion of the cycle during which the diode is forward biased, and therefor, reducing loss in the diode. For this simplified theoretical model, efficiencies in the high 90's (depending on the forward bias voltage) can be reached, and the model gives insight in to the balance of dissipated power and output DC power.

Fig. 3.4 shows an example input voltage waveform V_{RF} across the diode terminals, as well as the voltage V_d resulting from the interaction with the nonlinear elements of the diode model from Fig. 3.2. The resulting V_d is a clipped sinusoid at the forward bias voltage V_f and follows the the input wave during the reverse bias period from θ_1 to $(2\pi - \theta_1)$, where $2\theta_1$ is the forward bias period. V_d has a

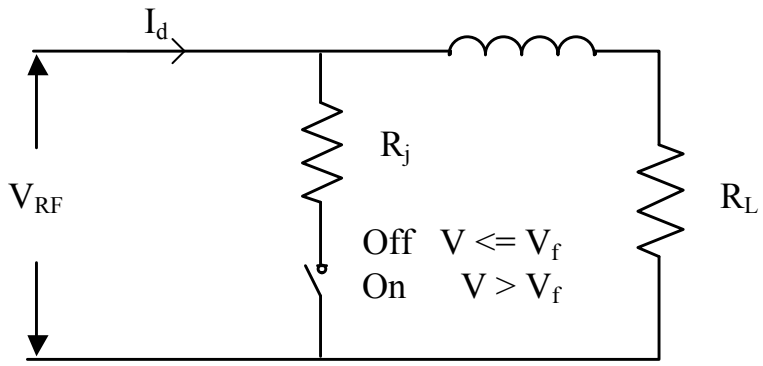


Figure 3.1: Circuit model of an ideal diode with constant forward bias voltage connected to an RF choke and a DC load. R_j is a small on resistance, in the ideal case it is a perfect short, in a more realistic model it is a few Ω to a few tens of Ω.

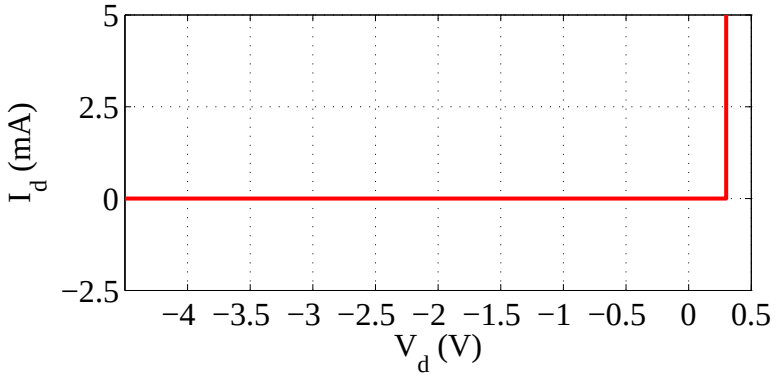


Figure 3.2: I-V curve for an ideal diode with constant forward bias voltage ($R_j = 0\Omega$).

DC component that is always higher than $-V_f$, since the input is connected to the same node as the diode and the DC load, the signals add, and the input sinusoid is offset by that DC voltage value. The DC current flows through the RF choke and load. Therefore, the load resistance changes the DC level and controls the level that the input signal is added to. This gives the ability to control the portion of the period of forward bias by adjusting the DC load, as can be seen in the waveforms

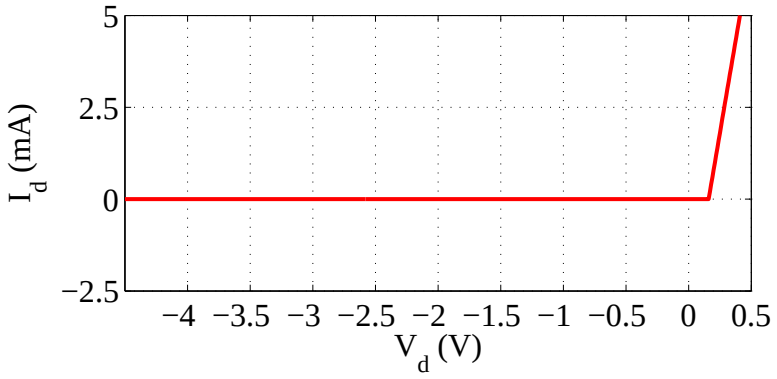


Figure 3.3: I-V curve for an ideal switch diode model with constant resistance $R_j = 50\Omega$.

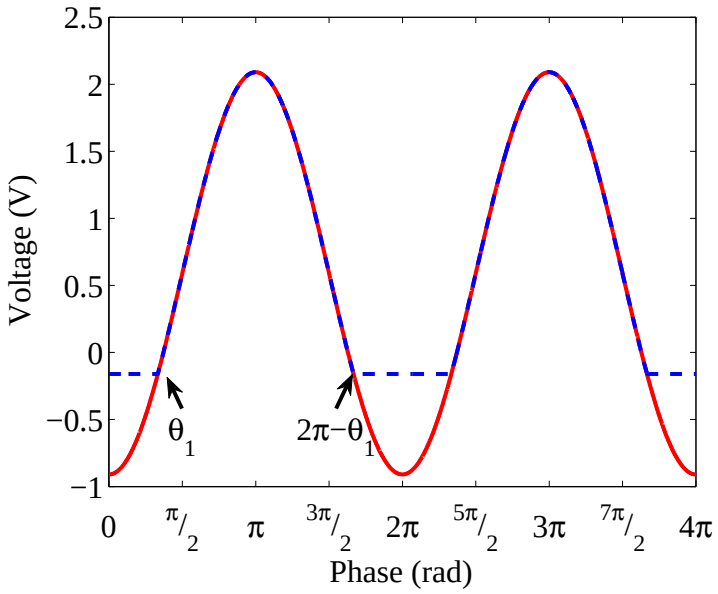


Figure 3.4: Generator Voltage waveform (red) and the resulting voltage waveform across the diode V_d from Fig. 3.1 (blue) following the IV curve in . 3.2 . The points of transition from forward bias to reverse and vice verse are labeled (θ_1) and ($2\pi - \theta_1$). Notice that the forward bias voltage is a non zero value.

in Fig. 3.5 and the corresponding values in Table. 3.1. Assuming no reflections, the total power is the sum of the power on the DC load and the power lost in the diode, and the powers can be found as follows.

The generator waveform is

$$V_{gen} = -V_{d1}\cos(\theta) \tag{3.2}$$

Where V_{d1} is the voltage amplitude.

The resulting waveform across the diode is

$$V_d = \begin{cases} V_{d0} - V_{d1}\cos(\theta) & \text{diode off} \\ -V_f & \text{diode on} \end{cases} \tag{3.3}$$

where the value for V_{d0} is found by observing V_d at the transition from forward to reverse bias, found by setting both parts of (3.3) equal and solving for the phase θ_1:

$$\begin{aligned} -V_f &= V_{d0} - V_{d1}\cos\theta_1 \\ V_{d0} &= \frac{V_f}{V_{d1}\cos\theta_1} \end{aligned} \tag{3.4}$$

From (3.4) (3.3) (3.2), the DC voltage can be calculated as

$$\begin{aligned} V_{DC} &= \frac{1}{2\pi}\left[\int_0^{\theta_1} -V_f\,\mathrm{d}\theta + \int_{\theta_1}^{2\pi-\theta_1} [V_{d0} - V_{d1}\cos(\theta)]\,\mathrm{d}\theta + \int_{2\pi-\theta_1}^{2\pi} -V_f\,\mathrm{d}\theta\right] \\ &= -V_f\frac{\theta_1}{\pi} + V_{d0}\left(1 - \frac{\theta_1}{\pi}\right) + \frac{V_{d1}}{\pi} sin\,(\theta_1) \end{aligned} \tag{3.5}$$

The DC load can be found by the ratio of the DC voltage (3.5) to the DC current

$$\begin{aligned} I_{DC} &= \frac{1}{2\pi}\left[\int_0^{\theta_1} \frac{V_{d0} - V_{d1}\cos(\theta)}{R_j}\,\mathrm{d}\theta + \int_{theta_1}^{2\pi-\theta_1} 0\,\mathrm{d}\theta + \int_{2\pi-\theta_1}^{2\pi} \frac{V_{d0} - V_{d1}\cos(\theta)}{R_j}\,\mathrm{d}\theta\right] \\ &= \frac{1}{R_j\pi}\left[V_{d0}\theta_1 - V_{d1}\sin(\theta_1)\right] \end{aligned} \tag{3.6}$$

resulting in

$$R_L = \frac{V_{DC}}{I_{DC}} \tag{3.7}$$

Similarly, the diode impedance at the fundamental frequency can be found as the ratio of the voltage and current Fourier coefficients at that frequency, as follows

$$V(f_0) = a_{v1} + jb_{v1}, \tag{3.8}$$

where

$$\begin{aligned} a_{v1} &= \frac{1}{\pi}\left[\int_0^{2\pi} V_d(\theta)\cos(\theta)\,\mathrm{d}\theta\right] \\ b_{v1} &= \frac{1}{\pi}\left[\int_0^{2\pi} V_d(\theta)\sin(\theta)\,\mathrm{d}\theta\right]. \end{aligned} \tag{3.9}$$

Solving for a_{v1} and b_{v1}, we obtain

$$\begin{aligned} a_{v1} &= \frac{1}{\pi}\left[\int_0^{\theta_1} -V_f\cos(\theta)\,\mathrm{d}\theta + \int_{\theta_1}^{2\pi-\theta_1} V_{d0}\cos(\theta)\,\mathrm{d}\theta\right. \\ &\quad \left. - \int_{\theta_1}^{2\pi-\theta_1} V_{d1}\cos(\theta)^2\,\mathrm{d}\theta - \int_{2\pi-\theta_1}^{2\pi} V_f\cos(\theta)\,\mathrm{d}\theta\right] \\ &= \frac{1}{\pi}\left[-2V_f\sin(\theta_1) - 2V_{d0}\sin(\theta_1) - V_{d1}(\pi-\theta_1) + V_{d1}\sin(\theta_1)\cos(\theta_1)\right] \end{aligned} \tag{3.10}$$

$$\begin{aligned} b_{v1} &= \frac{1}{\pi}\left[\int_0^{\theta_1} -V_f\sin(\theta)\,\mathrm{d}\theta + \int_{\theta_1}^{2\pi-\theta_1} V_{d0}\sin(\theta)\,\mathrm{d}\theta\right. \\ &\quad \left. - \int_{\theta_1}^{2\pi-\theta_1} V_{d1}\cos(\theta)\sin(\theta)\,\mathrm{d}\theta - \int_{2\pi-\theta_1}^{2\pi} V_f\sin(\theta)\,\mathrm{d}\theta\right] = 0 \end{aligned} \tag{3.11}$$

since V_d is an even function.

The current expansion is similarly

$$I(f_0) = a_{i1} + jb_{i1} \tag{3.12}$$

$$\begin{aligned} a_{i1} &= \frac{1}{\pi}\left[\int_0^{\theta_1} \frac{V_{d0}\cos(\theta) - V_{d1}\cos^2(\theta)}{R_j}\,\mathrm{d}\theta + \int_{2\pi-\theta_1}^{2\pi} \frac{V_{d0}\cos(\theta) - V_{d1}\cos^2(\theta)}{R_j}\,\mathrm{d}\theta\right] \\ &= \frac{1}{R_j\pi}\left[-2V_{d0}\sin(\theta_1) + V_{d1}\frac{\theta_1}{2}\right] \end{aligned} \tag{3.13}$$

$b_{i1} = 0$. Using the definitions (3.3)- (3.13), the DC load, diode impedance at the fundamental and efficiency can be examined as a function of θ_1 as shown in Fig. 3.5

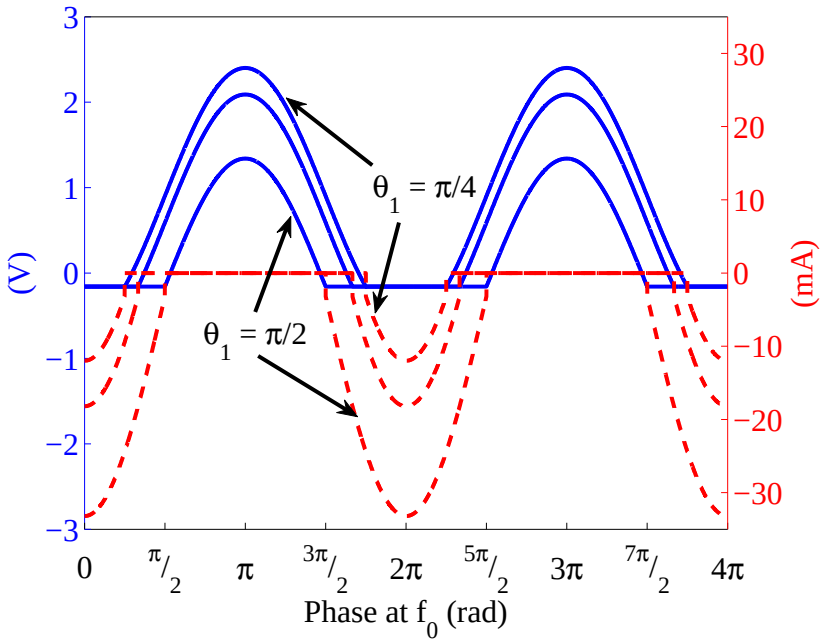


Figure 3.5: Diode voltage V_d (blue) and current through the diode I_d (dashed red), for conduction angle $\theta_1 = \pi/2$, $\pi/3$ and $\pi/4$.

Fig. 3.6 shows the dependance of θ_1 on the DC load. The values are for the diode model characterized by Fig. 3.3. Since the values for the DC load are very high for low values of θ_1 they are not practical because high values of a DC load are hard to emulate with a boost converter [64].

The dissipated power in the diode and DC output increase as the angle of forward bias increases. Fig. 3.7 shows these trends for the same model used in Fig. 3.3. It is interesting to note that the ratio of the powers changes throughout the changes in θ_1 indicating that the efficiency is changing as well. The maximum DC output does not necessarily represent the maximum efficiency point. For this model the amplitude of the input voltage was kept constant, since the diode fundamental impedance changes as a function of the forward bias angle, the input power to the model is not constant. Therefor, the efficiency (3.14) is the parameter of interest

Table 3.1: Summary of DC load and diode impedance at the fundamental frequency for the waveforms from Fig. 3.5

θ_1	$RL(\Omega)$	$R_d(\Omega)$
$\pi/4$	433	163
$\pi/3$	174	79
$\pi/2$	29	22

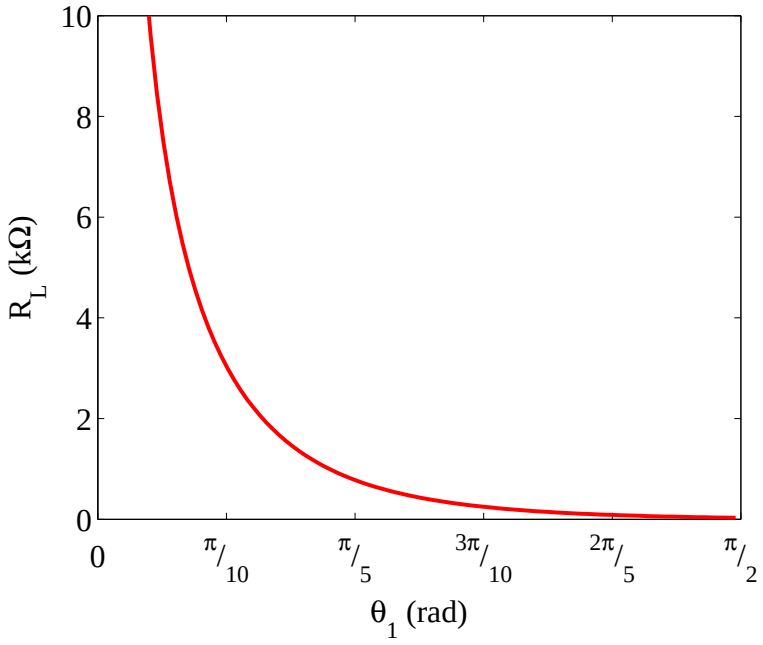


Figure 3.6: Dependance of the forward bias period $2\theta_1$ on the DC load resistance while keeping the voltage amplitude constant. Notice that reaching very small values of θ_1 is not practical since the DC load climbs to values of many $k\Omega$'s rapidly.

and it can be calculated as the ratio of DC power to the total power:

$$\eta = \frac{P_{DC}}{P_{DC} + P_{dissipated}} \tag{3.14}$$

Since the input used to calculate the efficiency is a voltage across the diode, this calculation does not include matching and coupling losses.

As can be seen in Fig. 3.8, the efficiency increases as the forward bias period $2\theta_1$ gets smaller. Although the efficiency is increasing, the output power is decreasing as the angle gets smaller as seen in Fig. 3.14. This is because the fundamental

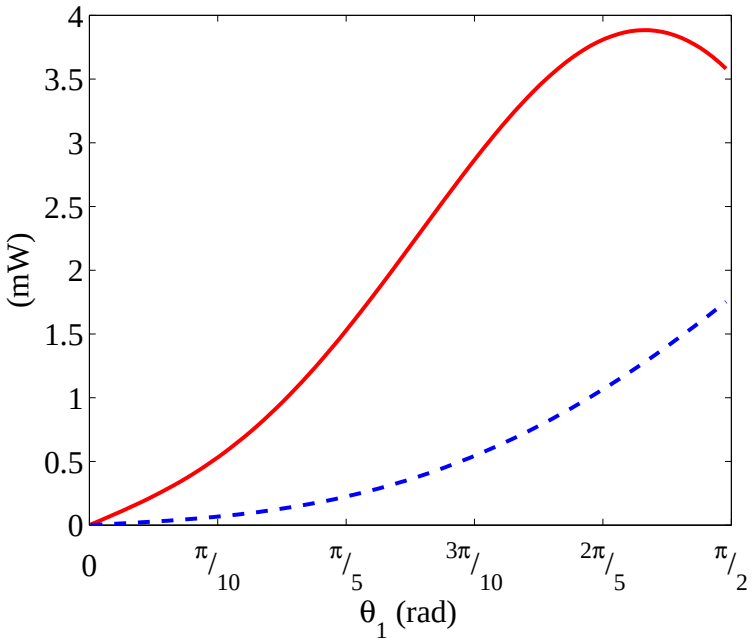


Figure 3.7: red - DC power on the DC load, Blue - power dissipated in the diode. The powers are for a constant input voltage amplitude while sweeping the DC load to adjust the forward bias angle $theta_1$.

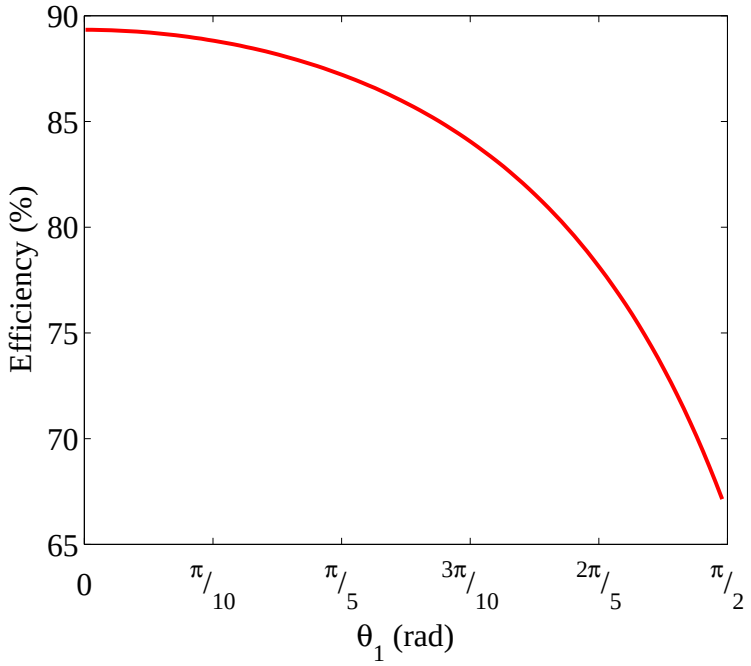


Figure 3.8: Rectification efficiency for the circuit in Fig 3.1 as a function of the forward bias period calculated using (3.14).

impedance increases with the DC load (Fig. 3.9) and the input power decreases according to (3.15) for a constant input voltage:

$$P_{RF} = \frac{1}{2}|V_g|^2 + \frac{1}{4R_d} \tag{3.15}$$

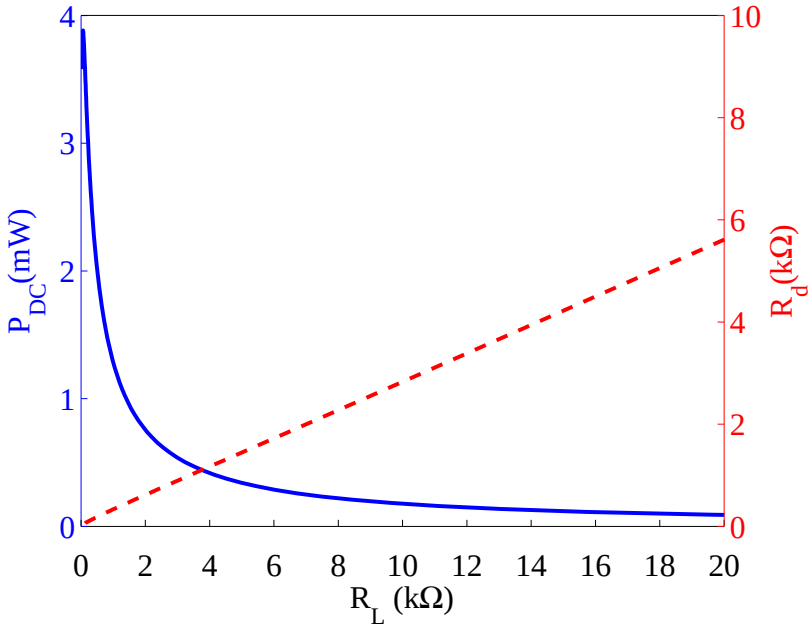


Figure 3.9: Output DC power (blue) and diode impedance at the fundamental frequency (red) as a function of the DC load R_L

From Fig. 3.9 it can be seen that the DC load has a direct impact on the diode impedance. This is a design advantage since the lower fundamental frequency impedances, 10 to 200Ω are impedances that are practical to match to. a higher impedance would make the matching a very challenging task. This region in the shown in Fig. 3.10 a zoomed in version of Fig 3.9 showing the relevant impedances of the region.

The discussion above and Fig. 3.5 to Fig. 3.10 give insight to the importance of controlling θ_1 in order to achieve maximum RF-to-DC conversion efficiency. Fig. 3.8 shows an improvement in efficiency as the conduction angle θ_1 is minimized. For a realistic diode model, the diode must be forward biased for a long enough period

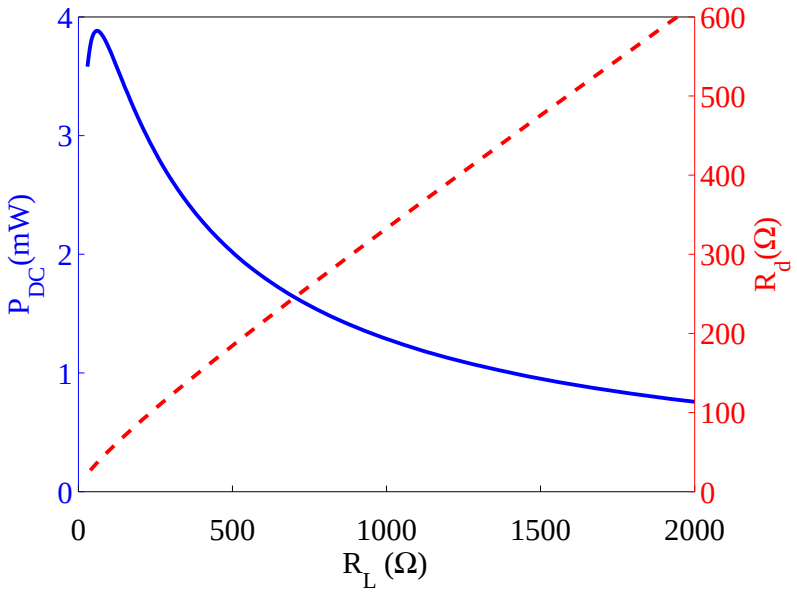


Figure 3.10: Zoomed in version of Fig. 3.9 showing that the practical impedances in terms of impedance matching are in the region of high DC power.

to create all of the harmonic power needed while minimizing the loss. Any diode will have in addition to the nonlinear resistance, a constant series resistance, series lead inductance, package capacitance and finally a nonlinear junction capacitance as seen in the circuit schematic in Fig. 3.11.

The package parasitics L_p and C_p are constant and can be addressed by using a simple matching network that would cancel their effect on the circuit. Fig. 3.12 shows the nonlinear circuit used in simulation for the rest of this chapter. Assuming the source (the antenna) is perfectly matched to the rectifier and DC load combination, the circuit from Fig. 3.12 is reduced to Fig. 3.13.

In an attempt to make a realistic diode model, the junction resistance is modeled using the IV curve of the diode at DC conditions Fig. 3.14. The IV curve is obtained from IV simulations using the model from [65]. Closer inspection of the model in Fig. 3.13 gives insight to the nonlinear behavior of the diode. The junction impedance is a parallel combination of the nonlinear resistance as shown in Fig. 3.15 and the nonlinear capacitance as shown in Fig. 3.17.

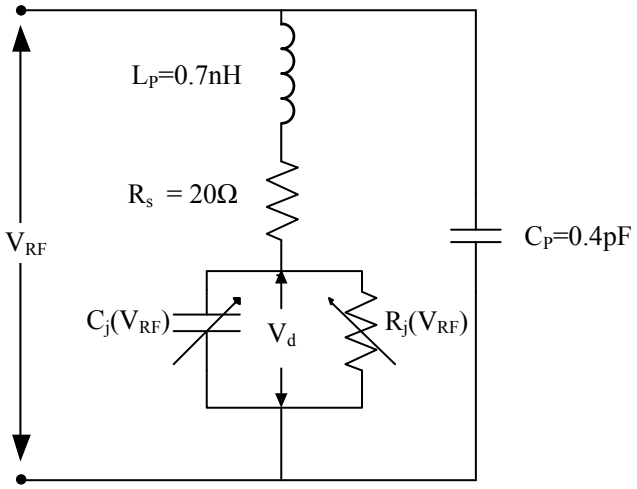


Figure 3.11: Detailed circuit model for the Skyworks SMS-7630-79 Schottky diode including package parasitics and nonlinear junction characteristics.

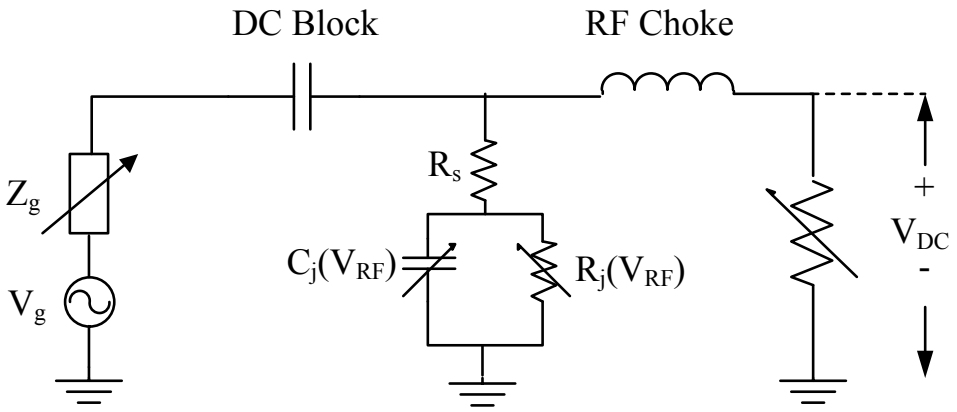


Figure 3.12: Circuit schematic using the detailed nonlinear resistance, nonlinear capacitance and series resistor as the rectifying element.

The capacitance is modeled according to (3.22). The diode capacitance is a sum of the depletion capacitance and of the diffusion capacitance. The depletion capacitance of the junction is caused by the junction potential barrier [66]. As the bias voltage of the diode is changes to reverse bias, electrons and holes are

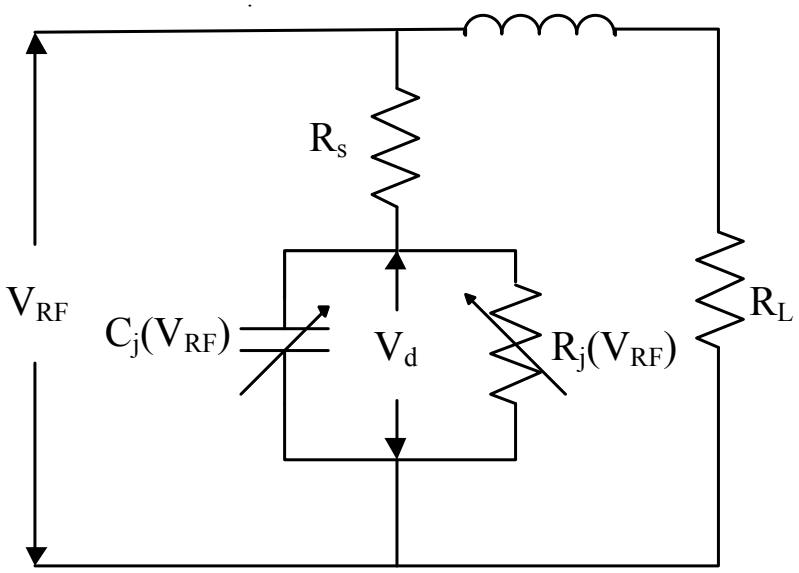


Figure 3.13: Simplified diode model. R_s is the series resistance of the diode, R_j and C_j are the junction resistance and capacitance as a function of V_d. R_L is the DC load connected to the diode through a low-pass filter.

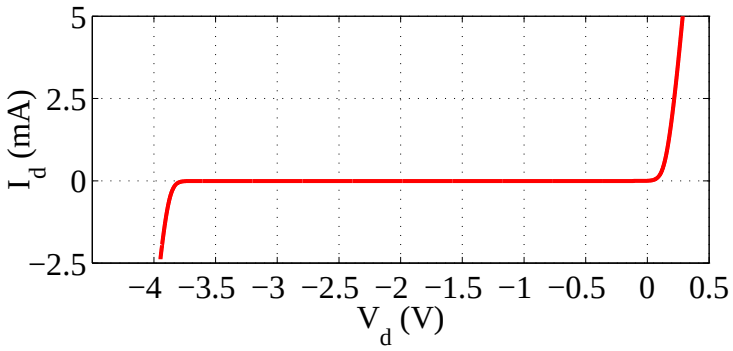


Figure 3.14: I-V curve for the SMS-7630-79 diode obtained from simulations using the manufacturer Spice model.

"pulled" away from the barrier region, this results in changes to the barrier width and charge quantity in the region. This change in width and the concentration of positive and negative charges on each side of the region is similar to a structure of a parallel plate capacitor [67] with a voltage controlled distance between the plates. Similar to the capacitance value of a parallel plate capacitor in(3.16)

$$C = \frac{\epsilon A}{d} \tag{3.16}$$

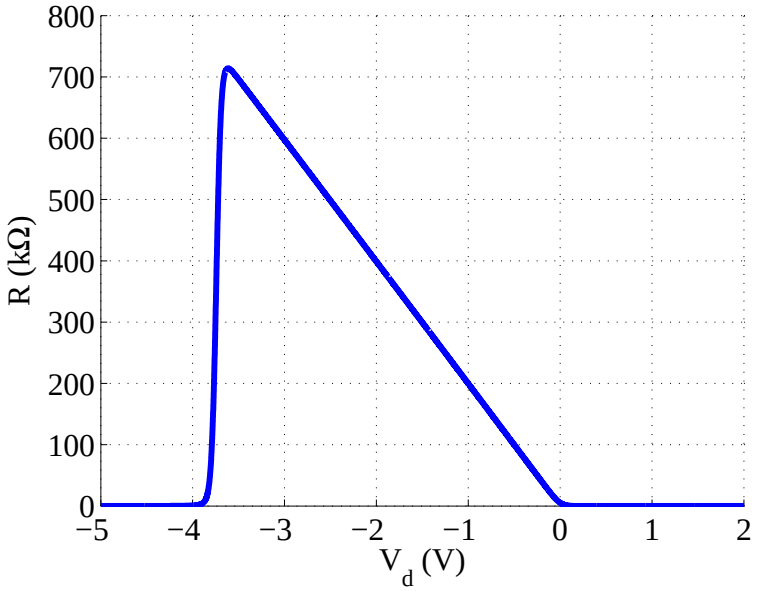


Figure 3.15: Diode junction resistance as a function of voltage. The data is extracted in Agilent ADS form SPICE model parameters at DC for the Skyworks SMS-7630-79 Schottky diode.

where, the region width is d and the cross section of the diode is A, the junction depletion capacitance changes with bias voltage, as the reverse bias changes towards forward bias and the width of the barrier region reduces the capacitance of the junction increases. This is held true up to the point of forward bias. (3.22) is an approximation for the capacitance that holds for uniform doping profile of the diode

$$N(x) = N_o \tag{3.17}$$

where

N_o is the surface doping in $\left(\frac{\text{charges}}{\text{cm}^3}\right)$

x depth through active layer in (μm)

and leads to a zero bias capacitance of

$$C_{j0} = A\left(\frac{q\epsilon N_o}{2V_f}\right)^{0.5} \tag{3.18}$$

where

A area (m^2)

q electron charge (e)

ϵ permittivity $\left(\frac{\mathrm{F}}{\mathrm{m}}\right)$

Many foundries however do not use uniform doping. In [68] a explicit formula relating Schottky diode capacitance (C_{j0}) to the bias voltage (V) and Gaussian doping profile (k) is developed. A Gaussian doping profile is convenient since by changing k, various profiles can be considered.

$$N(x) = N_o e^{-kx^2} \tag{3.19}$$

where

k Gaussian coefficient, and for each value of k, the junction capacitance is given by

$$C_j(V) = \frac{A\left(\frac{q\epsilon N_o}{2V_f}\right)^{0.5} A_1}{\left(1 - \frac{V}{V_f + A_2}\right)^{0.5+A_3}} \tag{3.20}$$

where A_1, A_2 and A_3 are functions of the Gaussian characteristic (k), the derivation can be found in [68]. For k = 1-100 a polynomial fit to A_1, A_2 and A_3 as a function of (k) yields

$$\begin{aligned} A_1 &= 1 - 2e^{-4}k + 1e^{-6}k^2 - 1e^{-8}k^3 \\ A_2 &= 1.24 - 2e^{-2}k - 4e^{-4}k^2 + 5e^{-6}k^3 \\ A_3 &= 6.5e^{-3}k - 2e^{-4}k^2 + 6e^{-6}k^3 \end{aligned} \tag{3.21}$$

Fig. 3.16 shows capacitance curves for three different doping curves; the capacitance for doping profile $k = 0$ is the highest. In the analysis in Fig. 3.5 to Fig. 3.20 the effect of worst case of doping profile in terms of junction capacitance, on the waveforms and RF-to-DC conversion efficiency is examined. The dimensions of the

diode have a big effect on the capacitance as well, the analysis below uses values for the Skyworks $SMS-7630-79$ Schottky diode.

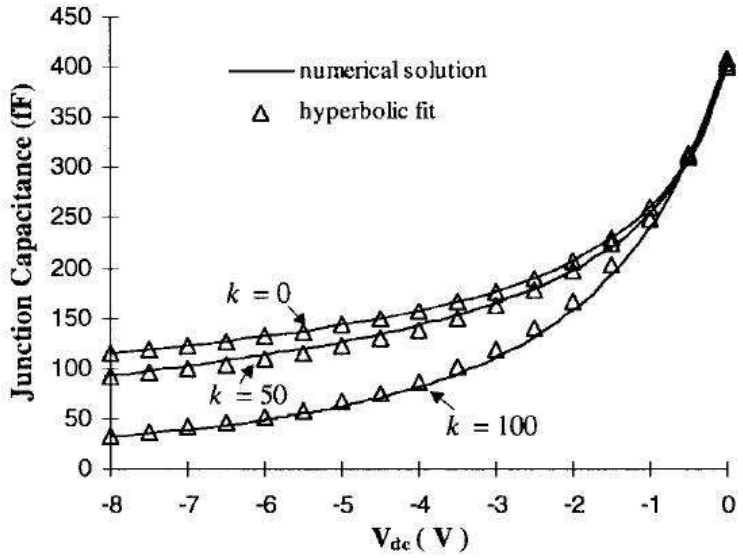


Figure 3.16: Junction capacitance versus bias voltage for three Gaussian doping profiles ($k = 0, k = 50, k = 100$) for Shottky diode with area of $150\mu\text{m}^2$ used in the analysis by Salameh and Linton.

Using the circuit model in Fig. 3.13 where the nonlinear resistor is identical to the one in the previous analysis as described by Fig. 3.1 and the nonlinear capacitance is described as Fig. 3.17, analysis of efficiency and the dependance on θ_1 and R_L is done.

$$C_j(V) = \frac{C_{j0}}{\left(1 - \frac{V}{V_j}\right)^{0.4}} \tag{3.22}$$

For $SMS-7630-79$ Schottky diode, the grading coefficient is $m = 0.4$, which is different from the typical square root dependance usually seen for a P-N junction. The grading coefficient depends on the nature of the junction change, when it changes abruptly from P to N, then $m = 0.5$, and when the P region changes linearly in to the N region then $m = 0.33$. Fig 3.17 shows example capacitance approximation values for Skyworks SMS-7630-79 [56] at reverse bias voltages.

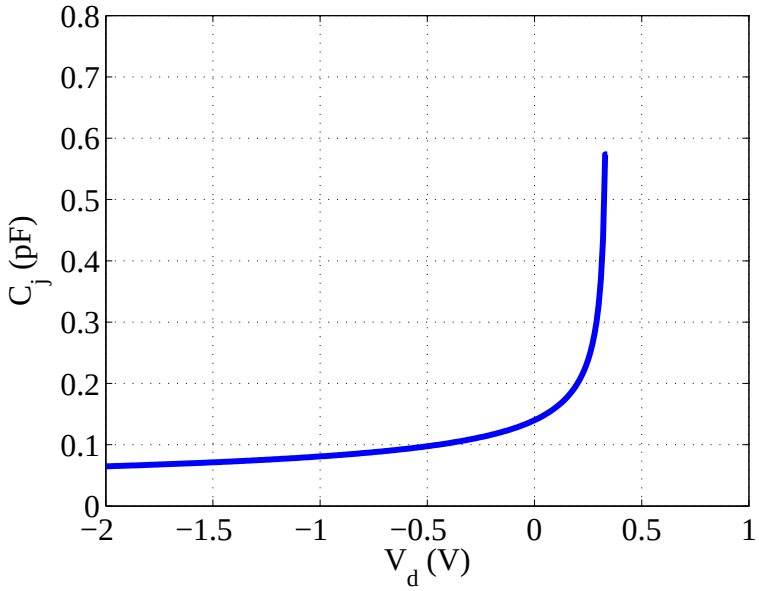


Figure 3.17: $SMS-7630-79$ Schottky diode junction capacitance as a function of voltage using (3.22). This is a simplified approximation to the junction capacitance not including the diffusion capacitance effect.

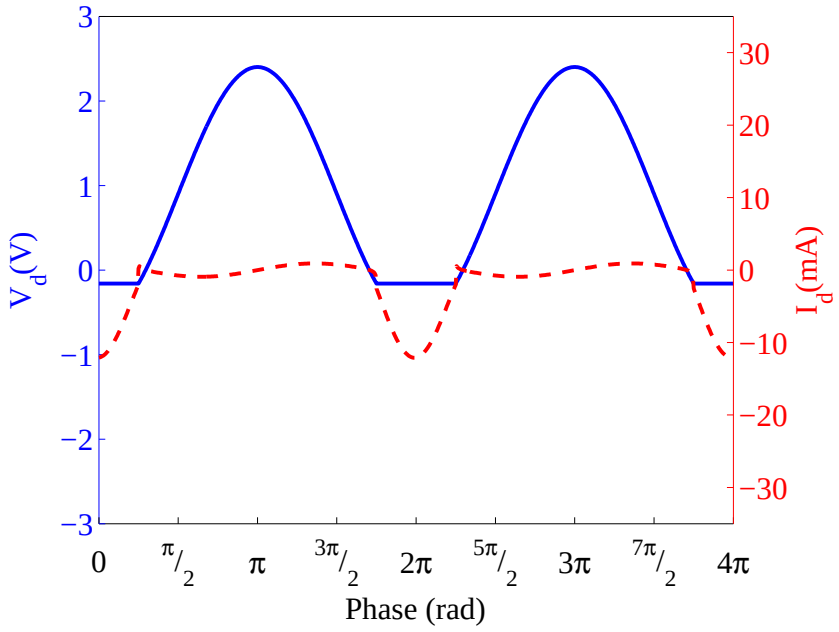
Schottky diodes are majority carrier devices and as such, the junction capacitance is dominated by depletion capacitance. Parasitic diffusion capacitance caused by minority carrier injection mostly for high currents exist at forward bias. The parasitic diffusion capacitance can be estimated by

$$C_{diff}(V) = \tau \cdot \frac{\partial}{\partial V} I_d. \tag{3.23}$$

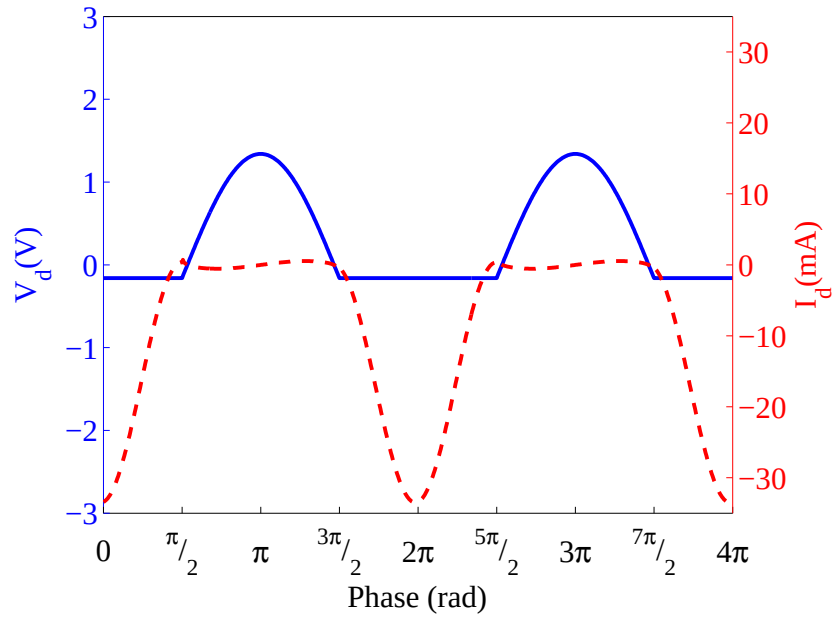
where τ is the carrier transit time.

Simulations show it has very small effect on the waveforms hence it can be neglected in this analysis [69].

Fig. 3.18 shows the current waveform for an added capacitance of $C_{j0} = 0.14\,\text{pF}$. The nonlinear capacitance adds loss to the system and decreases the efficiency. The high values of the capacitance around the forward bias voltage create a low impedance at that part of the period, since the capacitance is in parallel with the resistive part of the junction, the low impedance dominates and a higher current flows which in turn increases the loss. Notice that the current is non-zero



(a)



(b)

Figure 3.18: diode voltage V_d (blue) and current through the diode I_d (red) for different values of (θ_1), $\pi/4$ (a) and $\pi/2$ (b) for a diode model including junction capacitance (3.22)

throughout the whole reverse bias period and hence adds loss through that period that was not existent using a diode model with no capacitance as seen in Fig. 3.5.

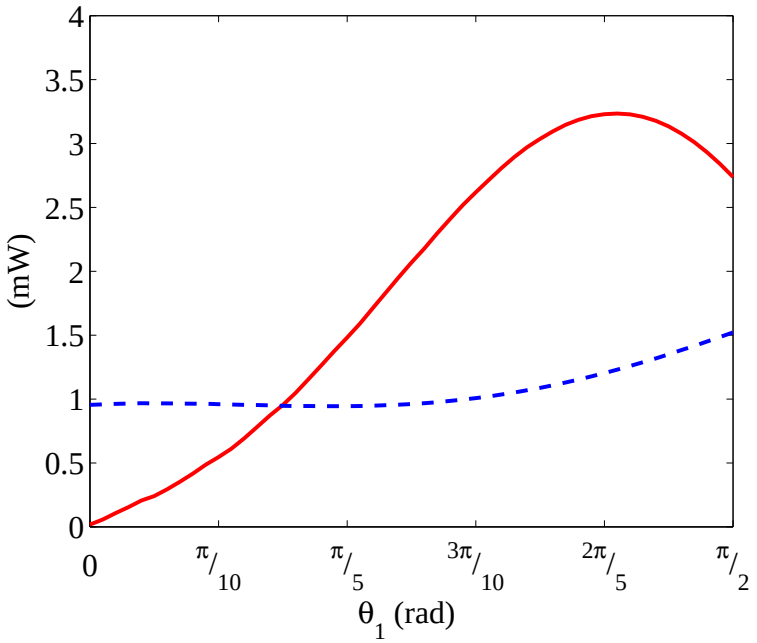


Figure 3.19: red - DC power on the DC load, Blue - power dissipated in the diode. The powers are for a constant input voltage amplitude while sweeping the DC load to adjust the forward bias angle θ_1. In contrast to Fig. 3.7 the model used to evaluate the powers pesented in the plot include the effects of the paracitic nonlinear junction capacitance.

Fig. 3.19 shows that the parasitic nonlinear capacitance adds loss for all values of θ_1. The added loss due to current flowing through the parasitic capacitance is much larger for small values of θ_1. Since the loss is high in comparison to the DC output power for small values of θ_1, the efficiency is low at those θ_1 values.

Fig. 3.20 shows in contrast to Fig. 3.8 that the value of θ_1 for maximum efficiency is not as small as possible. The selection of θ_1 for maximum efficiency is a balance between DC power created in the diode and the power dissipated in the diode. The smaller C_{j0} which leads to smaller overall junction capacitance, the smaller the value of θ_1 for maximum efficiency.

All of the analysis up to here has assumed a cosine voltage wave across the

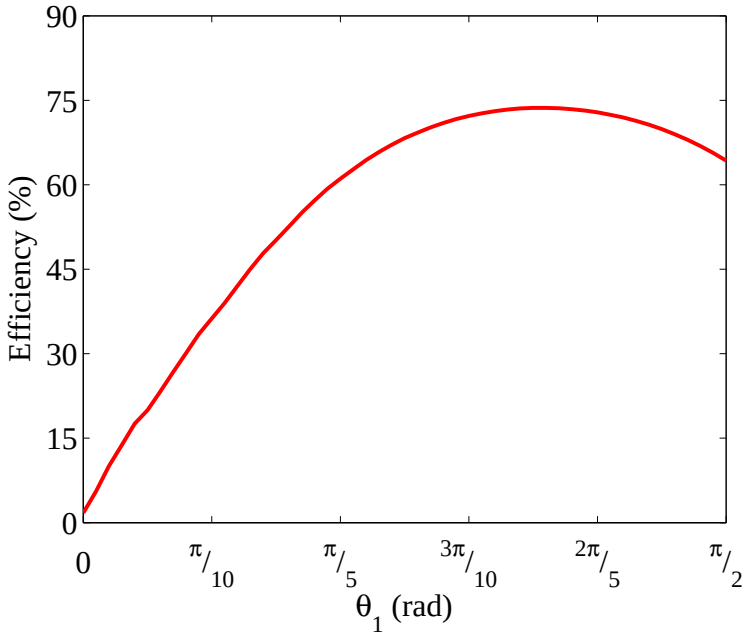


Figure 3.20: Rectification efficiency for the circuit in Fig. 3.13 as a function of the forward bias period calculated using 3.14.

diode. The RF generator in a wireless powering application is the receiving antenna and can be modeled as a voltage source with an internal impedance as in Fig. 3.12. For a given antenna the internal impedance is a constant at the fundamental frequency. The diode impedance is changing in time within the period according to the biasing conditions. The voltage generated by the source is the total voltage on both the internal impedance and the diode. Since the diode is a complex impedance there is a phase shift ϕ between the source and the diode as seen in Fig. 3.21. The dashed lines indicate the DC voltage across the load and the DC voltage across the nonlinear part of the diode model. The generator voltage can be expressed as:

$$V = -V_0 + V_1 \cos \omega t \tag{3.24}$$

The voltage across the nonlinear elements of the diode can be expressed as:

$$-V_d = V_{d0} - V_f \cos \theta_1 \tag{3.25}$$

$$\text{where}(\omega t - \phi = \theta_1)$$

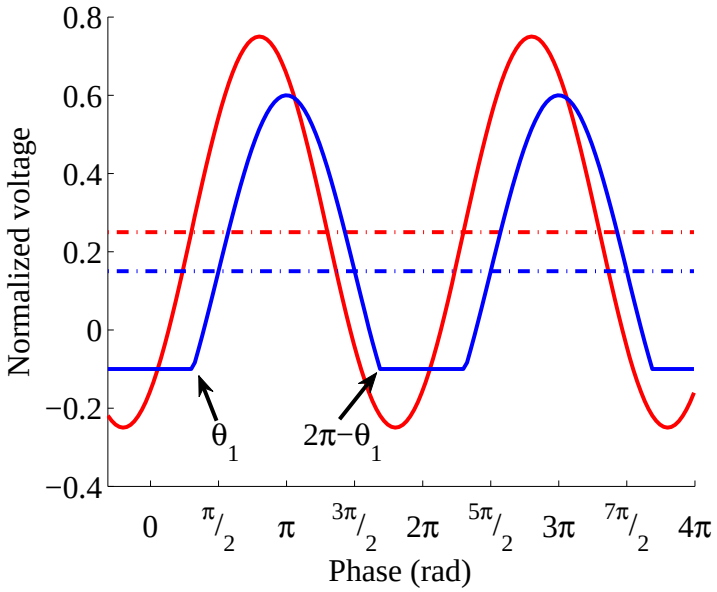


Figure 3.21: Example voltage waveforms: input voltage V across diode (red) and voltage V_d across nonlinear portion of the diode model (blue). The dashed red line shows the DC components of the input waveform and the blue is the DC component of the voltage across the nonlinear portion of the diode while it is reverse biased.

where V_{d0} is the DC component and V_{d1} is the fundamental amplitude during the reverse bias period, V_f is the forward bias voltage, $2\theta_1$ is the forward-bias period, and ϕ is the phase shift with respect to the input voltage.

In [70] time-domain analysis is done where the capacitance is defined as a monotonic increasing function of V_d and is expanded as follows

$$C_j = C_0 + C_1 \cos(\omega t - \phi) + C_2 \cos(2\omega t - 2\phi) + ... \tag{3.26}$$

Using (3.26) ϕ is derived in detail in [70] and found to be

$$\phi = \arctan\left[\omega R_s \left(C_0 - \frac{C_1 \cos\theta_1}{1 + \frac{V_f}{V_0}}\right) + C_2\right]. \tag{3.27}$$

At the transition points between forward and reverse bias, The relationship in 3.25 leads to

$$\cos\theta_1 = \frac{V_f + V_{d0}}{V_{d1}} \tag{3.28}$$

and minimizing θ_1 implies an increase in V_{d0} assuming the other parameters do not change. The DC voltage on the load is in reverse polarity to the forward bias voltage V_f. Since the magnitude of the reverse breakdown voltage V_{br} is much larger than the forward bias voltage V_f, the DC voltage can be larger than V_f. The limit on increasing the DC voltage during the reverse bias period is the the reverse breakdown voltage V_{br}. The sum of the fundamental amplitude V_{d1} and the DC component V_{d0} should be smaller than V_{br} in order to prevent an additional source of harmonic generation and additional power dissipation in the diode. This means that for improved efficiency, the diode should be in forward bias as little as possible during each cycle, however, it still needs some amount of forward bias to provide the nonlinearity. as described in the previous analysis that includes junction capacitance. This is in agreement with the earlier statement that power is mostly dissipated in the diode during forward bias period. The assumptions made while minimizing θ_1 in (3.28) are valid since V_f is a constant that is determined by the diode used and V_{d1} is determined primarily by the RF impedance presented to the source at the fundamental frequency.

$$V_{DC} = \frac{1}{2\pi}\left[\int_0^{2\theta_1} -V_f \,\mathrm{d}\theta + \int_{2\theta_1}^{2\pi} V_{d0} - V_{d1}\cos(\theta)\,\mathrm{d}\theta\right]$$

$$V_{DC} = -V_f\frac{\theta_1}{\pi} + V_{d0}\left(1-\frac{\theta_1}{\pi}\right) + \frac{V_{d1}}{\pi} sin\,(\theta_1) \tag{3.29}$$

Examining the The DC component of the junction voltage waveform from Fig. 3.21, the expression in 3.29 can be derived. While θ_1 is approaching 0 and V_{DC} is approaching V_{d0} the junction voltage is formed to be a pure sinusoid around V_{d0}. This indicates the need for harmonic termination in order to create a high efficiency rectifier.

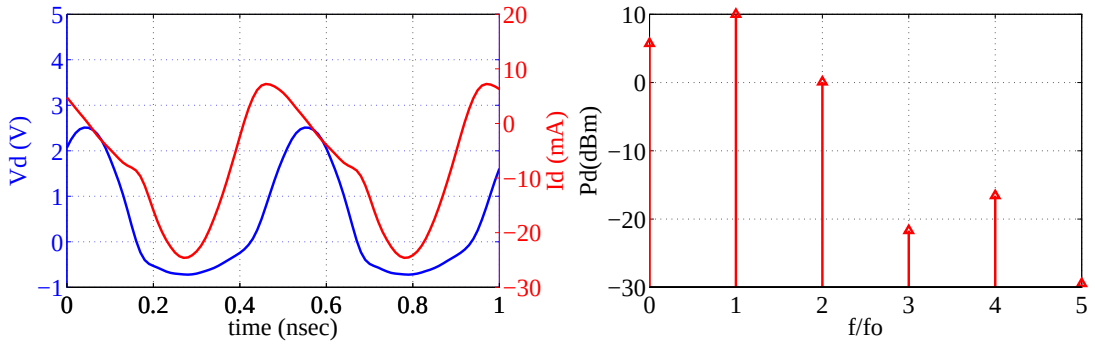
In the model in Fig. 3.13, the junction can be replaced by its Norton equivalent current source. The antenna is an open circuit for DC currents and is the source of

the waveform to the diode. hence, the DC current can only flow from the Norton current source to the DC load RL and thus a larger R_L implies a larger DC output voltage and higher efficiency within the limits described above. For a larger value of R_L, the blue waveform in Fig. 3.21 shifts upwards, and the diode is forward biased during a smaller portion of the period, thus increasing the DC rectified voltage and increasing the efficiency. It is interesting to note that this is opposite to reduced-conduction angle efficient power amplifiers, where the DC bias voltage is reduced for higher efficiency [71], which will be discussed in the next section.

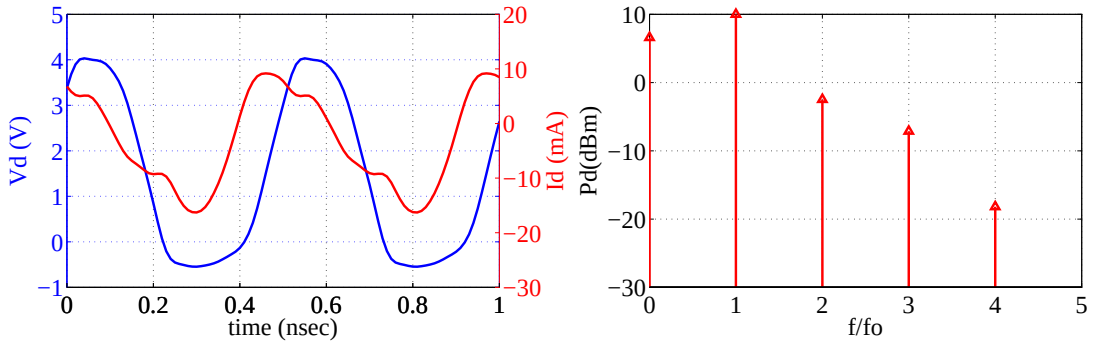
Harmonic balance simulations using Agilent ADS were performed with a varying DC load for a constant input RF power of 10 dBm. Fig. 3.22(a) and (b) shows the diode voltage and current waveforms for $R_L = 60\,\Omega$ and $460\,\Omega$. The spectral content of the voltage shows that for the optimal load, the ratio of the DC rectified voltage (V_{d0}) and the fundamental voltage amplitude (V_{d1}) is small and $V_{d0} + V_{d1} \simeq V_{br}$. The efficiencies corresponding to the two loads are 41% and 52%, respectively.

As in the case of power amplifiers, harmonic terminations can be used to improve efficiency. Fig. 3.22(c) is the result for a high impedance presented at all even harmonics, resulting in a 65% efficiency. For this increase in efficiency, the optimal load is reduced to $360\,\Omega$ to avoid voltage breakdown.

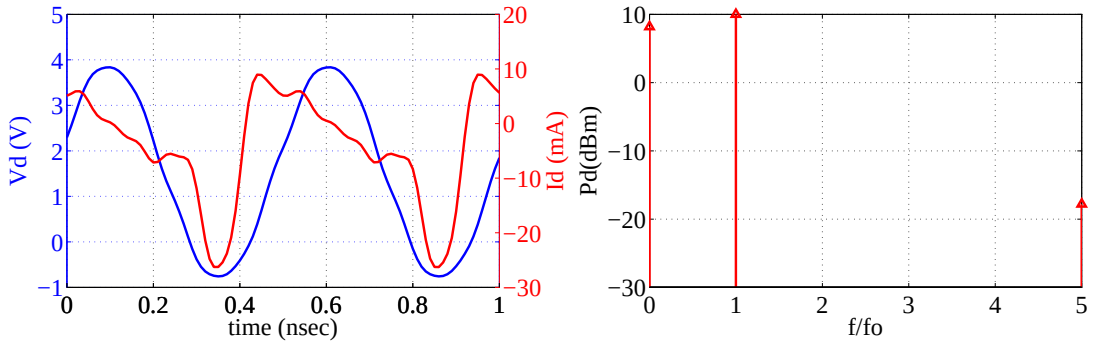
The harmonic content of the dissipated power is similar in all cases but the distribution of power between the harmonics can differ. In the optimal case all the harmonic content will be in the DC term. When the input power is swept, the load can be adjusted to maintain $V_{d0} + V_{d1} \leq V_{br}$, and maintain the correct conduction angle the efficiency can be maintained. As the input power decreases further than a few dBm, the efficiency will drop, since the diode will not get in to deep forward bias region and its series impedance is high during the current flow through it, as summarized in Table 3.2. For the simulated case, the best efficiency of 70% is achieved for $P_{in} = 5\,\text{dBm}$ for $R_L = 1210\,\Omega$.



(a)



(b)



(c)

Figure 3.22: Simulated time-domain voltage and current waveforms and corresponding voltage spectra for (a) $R_L = 60\,\Omega$; (b) $R_L = 460\,\Omega$; and (c) terminated even harmonics and $R_L = 360\,\Omega$ for an input power of 10 dBm. Note that the best efficiency is obtained for the harmonically terminated case when the time-domain waveform is closest to a pure sinusoid.

Table 3.2: Efficiency simulation rectifier results for sevral input powers. R_L is the optimal load

P_{in} (dBm)	R_L (Ω)	P_{out} (dBm)	η (%)
10	360	8.18	65
5	1210	3.42	70
0	1260	-1.99	63

3.3 Harmonic Analysis

Any periodic signal can be expressed as a sum of sine and cosine signals [72, 73] as:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left[a_n \cos(n\omega t) + b_n \sin(n\omega t)\right]$$

where:

$$a_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \cos(n\omega t)\, \mathrm{d}t$$

and

$$b_n = \frac{1}{\pi} \int_{-\pi}^{\pi} f(t) \sin(n\omega t)\, \mathrm{d}t \tag{3.30}$$

In circuits incorporating nonlinear elements such as diodes, the voltage and current time-domain waveforms are clipped at the threshold voltage point. These clipped waveforms in the time-domain contain harmonics in the frequency domain. In the case of a nonlinear system such as a rectifier, higher frequencies are generated by the non-linearity [74]. Applying correct impedances at the specific harmonic frequencies, will modify the voltage and current at those harmonics and in turn, the overall shape of the waveforms [75, 76]. The impedances presented to the diode at the frequencies of the harmonics are referred to as harmonic terminations. In order to prevent power dissipation at the harmonics, the magnitude of the reflection is set to unity $|\Gamma = 1|$, and the phase of the reflections is used to control the waveform shapes. All circuits at every configuration have an impedances that varies with frequency. The impedances at the higher harmonics are not always part of the design. For linear circuits the harmonic impedances do not matter, since there

will be on content at the frequencies higher than the input signal. For circuits that include nonlinear elements such as diodes or transistors, higher frequency components at integer multiples of the input signal are generated. Since there are higher frequencies than the fundamental present, the impedances at those frequencies effect the waveforms and the response of the circuit [71, 75]. By correct design of impedances at the frequencies of the harmonics, specific reflections can terminate the current or voltage at each harmonic frequency. A termination of a low impedance (close to short), will create a reflection of $\Gamma = -1$ and would eliminate the voltage component while allowing current at that frequency. On the other hand, a termination in a high impedance (close to an open), will generate a reflection of $\Gamma = 1$ and eliminate the current while allowing voltage. In both cases the termination eliminates power dissipation at that frequency since current and voltage do not coexist.

3.3.1 Amplifier and Rectifier Classes

The ability to present different impedances at different harmonics gives the ability to form the waveforms in ways that enhance the performance. Amplifier designers have been using this technique as early as 1932 [77]. Different amplifier topologies of shaping the voltage and current waveforms have been suggested in order to maximize output power, linearity and/or efficiency. Most of the theoretical work assumes all harmonics are terminated but, for practical circuits, only a finite number of harmonics is considered. A comprehensive analysis for a finite number of harmonics in amplifier design is discussed in [78]. Much of the amplifier efficiency analysis is similar to that of rectifier, since the main effect on efficiency is offsetting the voltage and current time waveformes across the nonlinear device terminals. In [79] a class-E amplifier analysis is modified for rectifiers, and in [80] rectifier classes E,F, $E^{-}1$ and $F^{-}1$ are analyzed and compared. In this work, a class-C

reduced-conduction angle rectifier is presented. In this class, the device is in cutoff for over half of the cycle. The advantage of class-C is high efficiency, but with high distortion at the output and reduced output power [71]. Since the conduction angle is small, the current peaks to high values in a short time, hence class C rectifier configuration gives high efficiency but at low power.

In the remainder of this chapter several harmonically terminated classes of power amplifiers are overviewed and their applicability to rectifiers is discussed

Class F is an amplifier topology where the odd harmonics are terminated with $\Gamma = 1$ (open) and the even harmonics are terminated in $\Gamma = -1$ (short). Infinite harmonic terminations would create a voltage waveform that has only odd harmonic content and is a square wave in the time domain. On the other hand, the current has only even harmonic content and is a clipped sinusoid in the time domain. The figure below is generated in Agilent ADS harmonic balance simulation with an ideal switch as the nonlinear device. The 2nd, 4th and 6th harmonics are terminated with quarter-wave open stubs that present shorts at the plane of the switch and 3rd, 5th and 7th harmonic quarter-wave stubs that present opens the switch plane. Initial simulations of the rectifier while applying Class F finite (7 harmonics) harmonic conditions, shown in Fig. 3.27, look promising with efficiencies η_{RF-DC} well into the high nineties but, further investigation reveals compatibility problems for this topology with integrated rectifier antennas. The simulated input impedances for the switch model are over $1k\Omega$, which would make matching in microstrip extremely hard or impossible. Another problem is the need for a dutycycle of the waveform to be 50%, As the DC voltage builds up on the DC load, it adds with the incoming wave from the generator. The addition of the two signals shifts the voltage across the rectifier, and as a result, the duty cycle varies from 50% and the waveform shapes differ from the theoretical class-F shapes. The sensitivity to duty cycle change, forces the use of a small DC load in order to ensure a small DC voltage

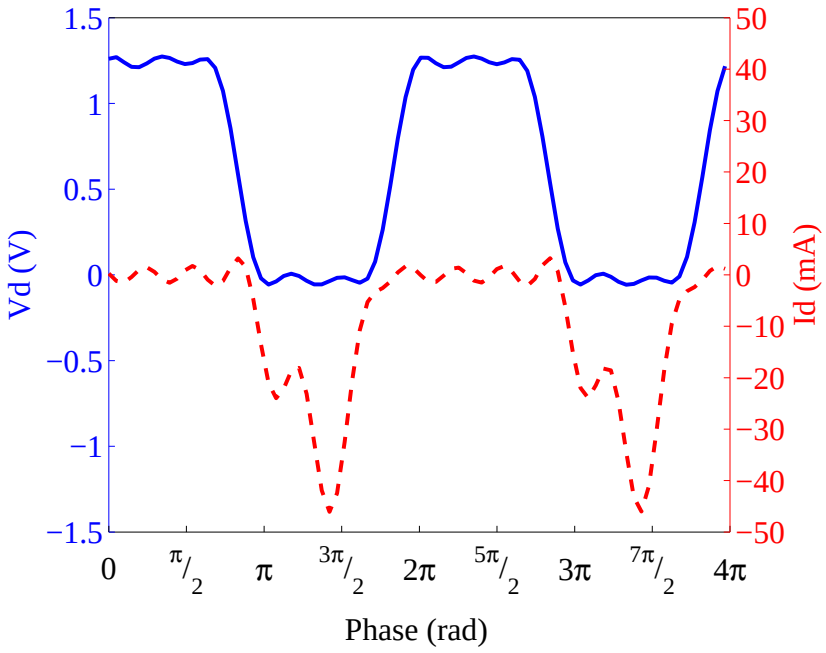


Figure 3.23: Voltage (blue) and current (dashed red) time-domain waveforms corresponding to class-F harmonic terminations. Obtained from harmonic balance simulations in Agilent ADS using an ideal switch with R_{on}=1 Ω and R_{off}=5 MΩ with the switch transition at V_d=0 and a DC load of 190Ω. The harmonic conditions are created using six $\lambda/4$ stubs for harmonic terminations, shorts at even harmonics and opens at odd harmonics.

offset. Further, the class-F rectifier topology is very sensitive to parasitic reactance. Any addition of small capacitance in parallel with the switch, creates big variations from the ideal case waveforms and drops efficiency. The parasitic capacitance is effectively connected in parallel to the harmonic terminations, and thus the open terminations have very small to no effect in the parallel combination. Finally, applying the class-F finite (7 harmonic) terminations to a more realistic Skyworks diode Spice model [56] result in waveforms that dissipate over 80% of the RF power in the diode, as seen in Fig. 3.24.

Class-F^{-1} is an attractive topology since, as in class F, it offsets the current and voltage waveforms across the nonlinear device, theoretically reaching 100% efficiency. The F^{-1} mode has a duty cycle of 50% and a clipped sinusoid voltage

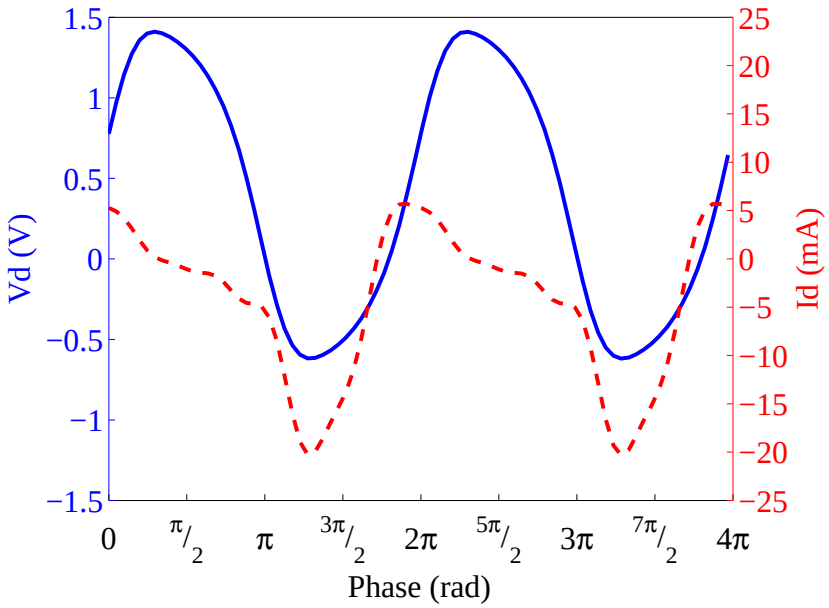


Figure 3.24: Voltage (blue) and current (dashed red) time-domain waveforms, obtained from harmonic balance simulation in ADS using a Skyworks schottky diode Spice model. The input power is 10 dBm at a frequency of 2.45 GHz. The harmonic conditions where created using six harmonic terminations, with the same stubs used in the previous class-F simulation with the ideal switch.

while the current is square. The class F^{-1} conditions are achieved by terminating all odd harmonics in shorts and all even in opens. Amplifier design experiments show that class-F^{-1} can preform better than class-F [81, 82]. This gives reason to explore the topology in rectifiers as well. Agilent ADS harmonic balance using an ideal switch were performed at f=2.45 GHz enforcing shorted odd harmonics and open even harmonics with six stubs. The resulting waveforms are presented in Fig. 3.25. Although the current waveform differs quite a bit from a square wave (due to the limited number of harmonic terminations), an efficiency of 92% is simulated assuming perfect match at the fundamental frequency and an optimal DC load of 35 Ω. Additional simulations, where the ideal switch is replaced by the Skyworks Spice model [56] were conducted. For the Skyworks $SMS-7630-79$ Schottky diode model case, it is interesting to see that the DC load for best rectification efficiency is much higher (215Ω) than for the ideal switch model case.

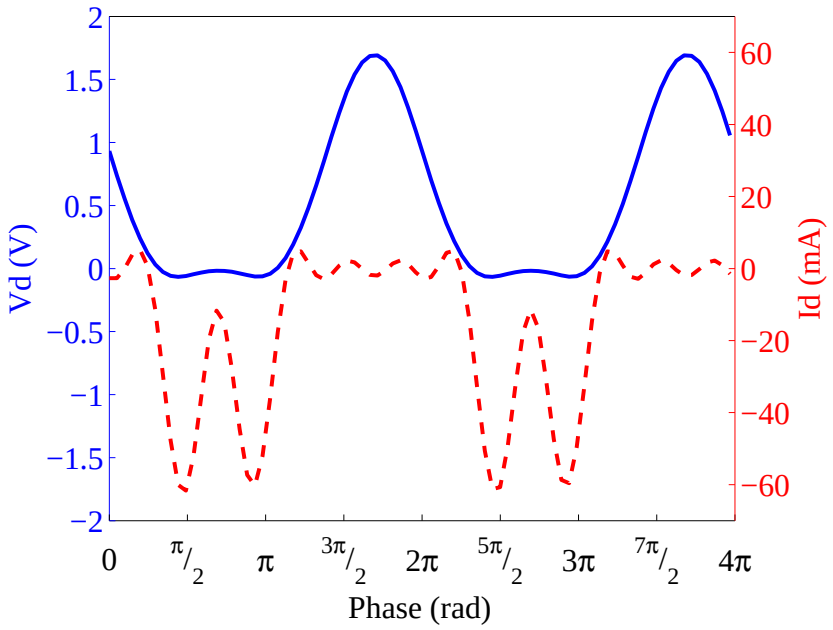


Figure 3.25: Voltage (blue) and current (dashed red) time-domain waveforms corresponding to class-F^{-1} harmonic terminations. Obtained from harmonic balance simulations in Agilent ADS using an ideal switch with R_{on}=1 Ω and R_{off}=5 MΩ with the switch transition at V_d=0 and a DC load of 190Ω. The harmonic conditions are created using six $\lambda/4$ stubs for harmonic terminations, shorts at odd harmonics and opens at even harmonics.

The waveforms from this simulation are shown in Fig. 3.26 and the RF-to-DC efficiency is 51%. As with the class-F termination case, the high DC voltage at the output forces the driving signal from the generator to have an offset and changes the duty cycle so the diode conduction angle is smaller than half the period and hence, the waveforms differ from the theoretical ones. The same argument of the device junction capacitance as in the class-F case applies to the harmonics terminated in opens.

Class-C is a class that has been used in power amplifiers since the beginning of the last century [77, 83]. For this class, the current waveform takes the form of a train of short pulses, witch have a low DC component but also a low fundamental frequency component [71], as shown in Fig. 3.27. This makes this topology extremely nonlinear which could be an unattractive property for power amplifier design, but

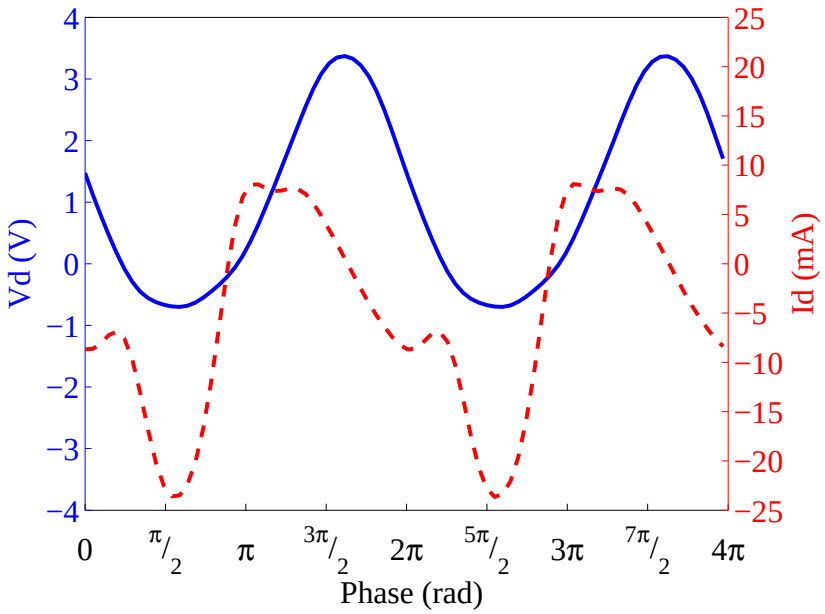


Figure 3.26: Voltage (blue) and current (dashed red) time-domain waveforms, obtained from harmonic balance simulation in ADS using a Skyworks schottky diode Spice model. The input power is 10 dBm at a frequency of 2.45 GHz. The harmonic conditions where created using six harmonic terminations, with the same stubs used in the previous class-F^{-1} simulation with the ideal switch.

it has many attractive rectifier benefits. Since the current pulses have a low DC component, the power dissipation in the series resistance of the diode is small. The current pulses are formed by allowing the diode to be forward biased for a very small fraction of the full cycle. This is controlled by the DC voltage that is in turn controlled by the DC load, as mentioned in section 3.2. An advantage over the other rectifier classes discussed above, is that the increase in DC voltage value and the change of duty cycle of the waveforms pushes the waveforms into deeper class-C mode. On the other hand, using this topology, a diode with relatively high breakdown voltage should be selected so that the high voltages do not reach breakdown, $V_{DC} + V_{in} < V_{br}$. An implementation of class-C can be generated by providing shorts to all harmonics beyond the fundamental frequency. An example circuit is shown in Fig. 3.28, where the 2nd to 7th harmonics are terminated in shorts. Starting from the 2nd harmonic on the left side of the circuit and moving to

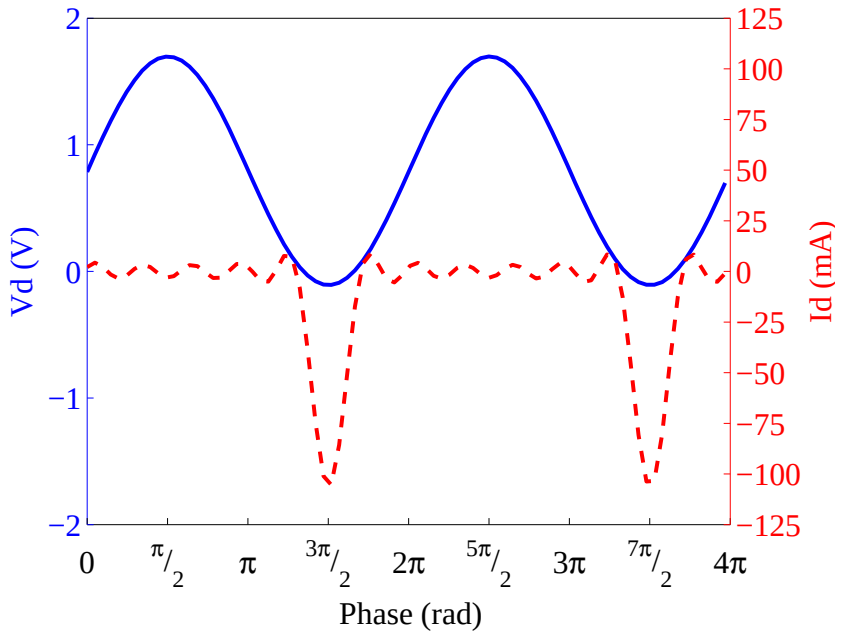


Figure 3.27: Voltage (blue) and current (dashed red) time-domain waveforms corresponding to class-C harmonic terminations. Obtained from harmonic balance simulations in Agilent ADS using an ideal switch with R_{on}=1 Ω and R_{off}=5 MΩ with the switch transition at V_d=0 and a DC load of 190Ω. The harmonic conditions are created using six $\lambda/4$ stubs for harmonic terminations, shorting the harmonics.

3rd, 4th and 5th towards the right. Finally, the 6th (15° @ f_0) and 7th (12.8° @ f_0) are the two stubs at the diode plane. The stubs are placed at distances that insure short terminations at the diode plane for each of there corresponding frequencies. Notice that in this circuit, the DC path is not part of the harmonic terminations. There are many different ways to implement these harmonic terminations, this is one example that was used for simulations in this section. The short harmonic terminations and the waveform offset by the DC voltage creates conditions so that the diode is forward biased for a short portion of the period, and no harmonic power can be dissipated in the diode Fig. 3.27.

Another advantage to this topology of rectifier is that a quarter-wave long stub at the fundamental frequency terminated with a shunt capacitor will provide an open at the fundamental and shorts to all even harmonics (as long as the capacitor

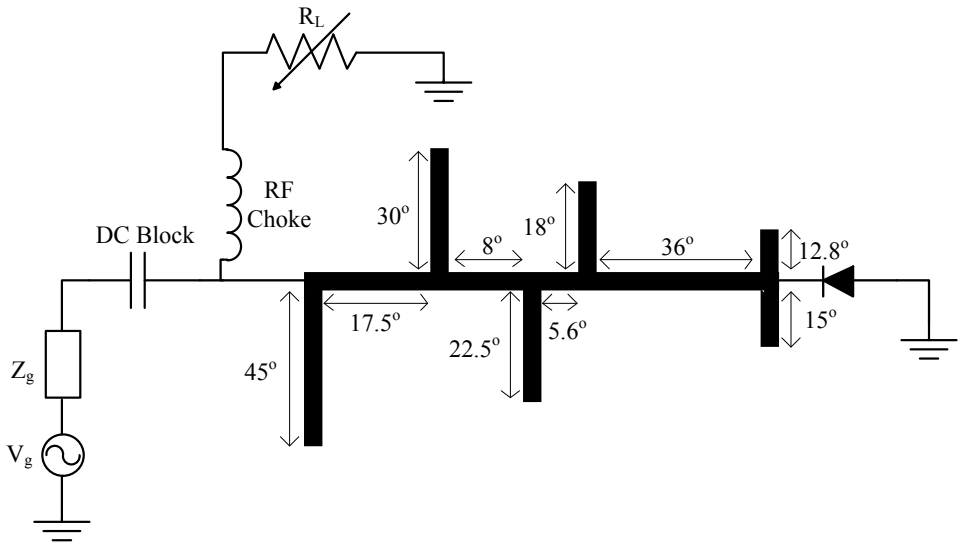


Figure 3.28: Microstrip circuit example of a harmonic terminated class C rectifier. The terminated harmonics are 2nd to 7th. Each stub is a $\lambda/4$ length at its harmonic frequency. The design is done using the diode plane as the reference plane. Starting with the higher harmonic stubs at the reference plane and adding the lower harmonic stubs at a distance that transforms there impedance to a short at the diode plane. All lengths in the figure are in electrical degrees at the fundamental frequency. The fundamental is assumed to be matched.

still provides a short). The single quarter-wave long stub is used for many harmonic terminations, while also providing a path for DC. The reuse of the same stub leads to reduction in the size of the circuit. Applying the terminations used to generate the waveforms seen in Fig. 3.27 to the Skyworks $SMS-7630-79$ Schottky diode Spice model [56], simulated results in Fig. 3.29 are obtained.

The voltage waveform of the Skyworks $SMS-7630-79$ Schottky diode Spice model [56] keeps the same shape as the ideal switch model, the current differs from the ideal switch, but still keeps the high current periodic pulse form. Although the RF-to-DC efficiency drops down to 65% is is still the highest efficiency of the topologies above when using the Spice model which includes the nonlinear capacitance and packaging parasitics.

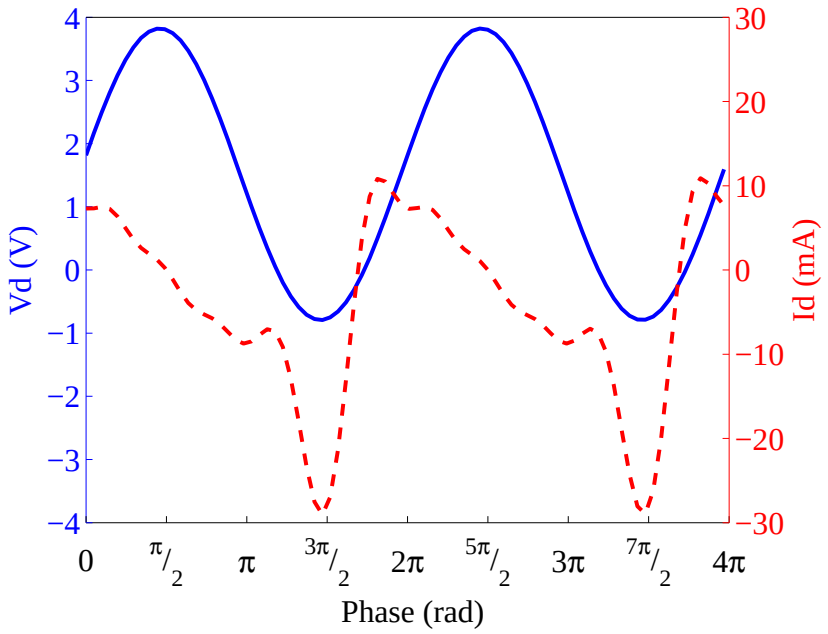


Figure 3.29: Voltage (blue) and current (dashed red) time-domain waveforms, obtained from harmonic balance simulation in ADS using a Skyworks schottky diode Spice model. The input power is 10 dBm at a frequency of 2.45 GHz. The harmonic conditions where created using six harmonic terminations, with the same stubs used in the previous class-C simulation with the ideal switch.

3.4 Summary

In summary, this chapter develops an analysis of nonlinear rectifiers and derives the conditions necessary for high efficiency rectification. Both time-domain and frequency-domain Fourier analysis are presented assuming diode rectifying devices, with ideal as well as non-ideal diode models. Time-domain waveforms across the rectifying element are derived and the relationship between their shape and RF-DC conversion efficiency is discussed in detail. For best efficiency, it is shown that harmonic frequencies of the incident RF wave need to be appropriately terminated at the diode terminals in order to accomplish required wave-shaping resulting from the time-domain analysis. An interesting relationship between harmonically-terminated and reduced-conduction angle power amplifiers and rectifiers is presented, and the analogy used to demonstrate efficiency improvements that harmonic terminations

can result in for rectifiers. Although the theory is focused on single-ended diode rectifiers, it can be extended to transistor rectifiers for higher power applications.

The contributions in this chapter are detailed in the following publications: [84, 85]

Chapter 4

Rectifying Element Simulations and Measurements

Miracles sometimes occur, but one has to work terribly hard for them.

—Chaim Weizmann

Contents

4.1 Introduction

The goal of this chapter is to present a method for measuring and predicting the nonlinear diode impedance that will transfer all of the incident power to the diode, and to accurately define and measure the conditions that maximizes rectification efficiency. The optimal complex impedance presented to a rectifying element for best rectification efficiency depends on frequency, incident RF power level and the DC load:

$$\eta_{RF-DC} = \frac{P_{DC}}{P_{RF,in}} = \eta(f, P_{RF,in}, R_{L,DC}). \tag{4.1}$$

The DC rectified power will be maximized for a specific load. A network analyzer could be used to measure the impedance of the diode, provided enough power range is available at the network analyzer port, proper calibration is performed, impedance tuners are integrated into the system and a controlled DC load is added. However, these additions are not straightforward and there is no real advantage for using a network vector analyzer over only source-pull with tuners.

4.2 Rectifying diode impedance

Matching the RF generator to the rectifier is a difficult task since the rectifier has a input impedance that is a function of several variables: frequency, power, DC load and harmonic terminations. The main contributor to the diode impedance is the junction nonlinear resistance $R_j(V_d)$. The junction nonlinear capacitance $C_j(V_d)$ is in parallel with the junction resistance $R_j(V_d)$ and gains influence as the frequency increases. The remaining linear components are; the series resistance

R_s, in with the series package inductance L_p, both in parallel with the package capacitance C_p, see section 3.2.

$$Z_{diode}(\omega, V) = \left(\left(\left(j\omega C_j(V_d) + \frac{1}{R_j(V_d)} \right)^{-1} + R_s + L_s \right)^{-1} + j\omega C_p \right)^{-1} \tag{4.2}$$

Since $C_j(V_d)$ and $R_j(V_d)$ are extremely nonlinear and their functions change with frequency and power level, (4.2) can only be used to predict the diode impedance under small signal conditions. For large signal impedances at different power levels and frequencies, harmonic balance nonlinear simulations are used. The harmonic balance simulation uses a diode model [65, 56] that is extracted through experiment at various frequencies and powers. The experimental procedure is not straightforward as in the case of linear circuits, where a circuit can be connected to a vector network analyzer. However, there are several problems which make a vector network analyzer measurement inadequate for rectifier design:

(1) The diode impedance can be found only for a specific RF pre-matching condition at the diode terminals;

(2) Rectified power trends for varying RF load conditions cannot be obtained;

(3) For different incident power levels, the match to the diode varies, and so the exact power across the diode is not known;

(4) It is not straightforward to include both a power amplifier and a variable DC load in a vector network analyzer. Thus, a modified load-pull technique is used here to fully characterize the rectifier element.

In order to determine the optimal diode impedance for rectification, a Focus Microwave load-pull system is used in a modified source-pull RF to DC configuration, as shown in Fig. 4.1,

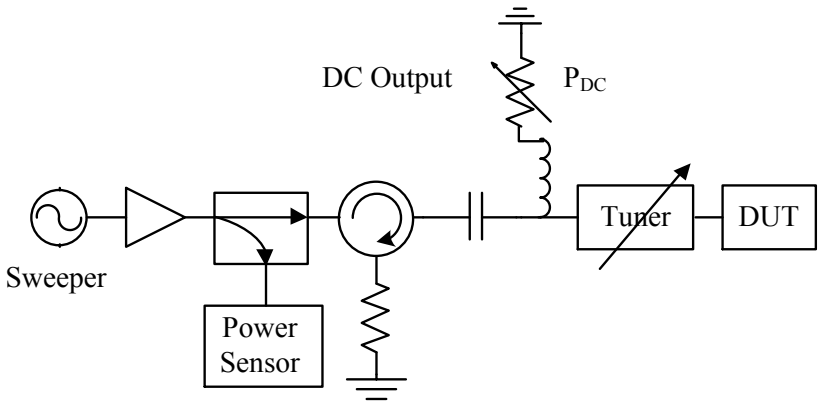


Figure 4.1: Block diagram of the source-pull RF-DC measurement. The rectified voltage is measured across a DC load resistor while the RF power to the diode (DUT) and the impedance presented at the diode input are varied.

where the source impedance, looking in to the device under test (DUT), is swept with a computer-controlled tuner. The tuner used in this work is a Focus Microwave single stub tuner, while giving the ability to sweep the fundamental frequency impedance but, with no control of impedances at the harmonic frequencies. A photograph of the test bench is shown in Fig. 4.2. The harmonic terminations vary arbitrarily if no terminations are presented by the test structure that the diode is mounted on. Multi tuner and/or active harmonic load pull systems are available commercially, but are extremely expensive and complex [86]. A simple fixed harmonic termination source-pull is possible by presenting terminations on the diode test structure. For each different harmonic terminations set, a new test structure must be fabricated and a separate source-pull measurement performed [87]. TRL calibration standards bring the reference plane to the diode, and the input power is varied while directly measuring DC power into a variable DC load [88]. Fig. 4.3 shows a photograph of TRL standards fabricated on a Rogers 4003c substrate covering frequency rage 700 MHz to 3 GHz.

First, rough measurements in a 50 Ω environment are used to predict the range of impedances for which the rectifier yields high efficiency. As can be seen in Fig. 4.4

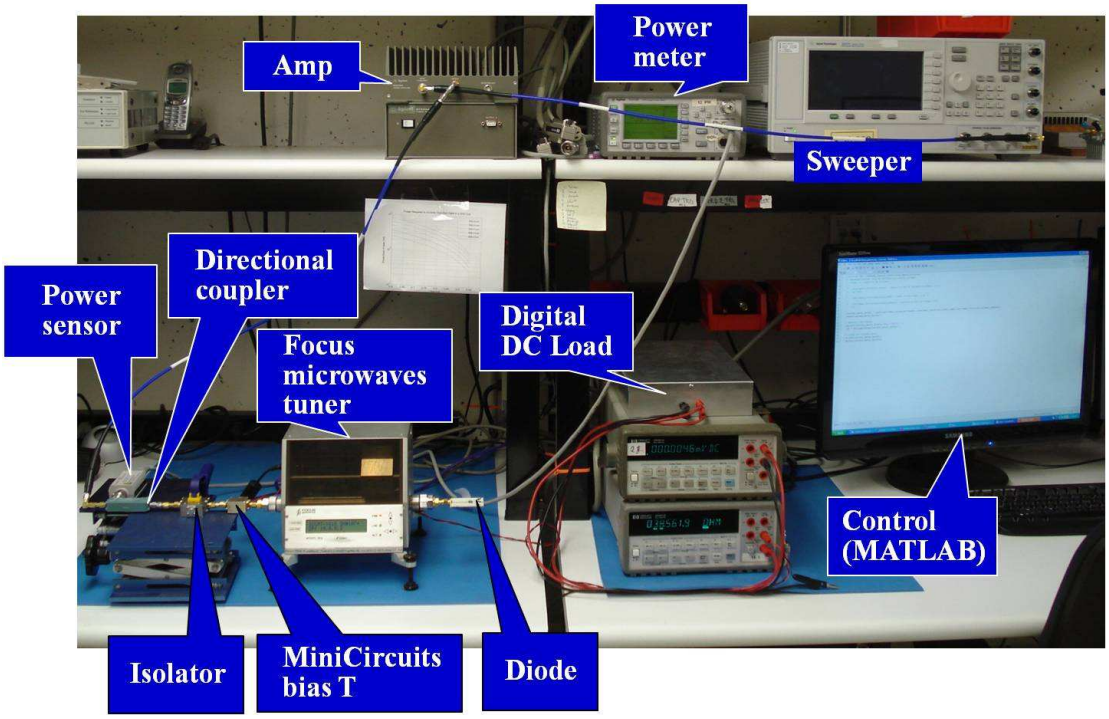
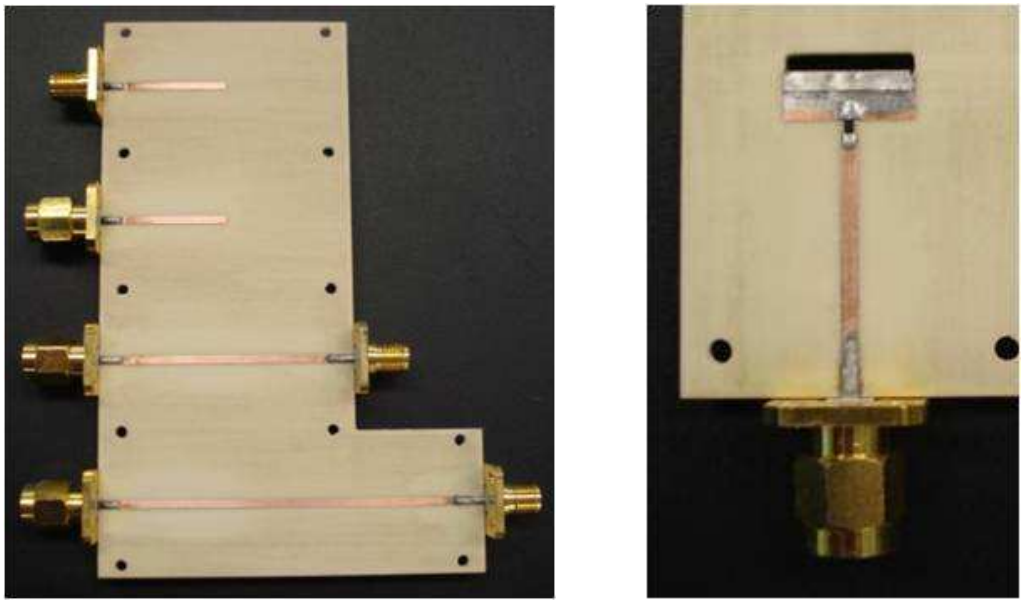


Figure 4.2: Photograph of the source-pull RF-DC measurement. The rectified voltage is measured across a variable DC load resistor while the RF power to the diode (DUT) and the impedance presented at the diode input are varied. This is repeated for several values of the DC load resistor.

the measurement resolution is higher closer to the center of the Smith chart.

Once this is estimated, a pre-matching circuit is designed to bring the impedance close to the range where reflections are low Fig. 4.5. Using a $\lambda/4$ impedance transformer constructed from a 80Ω line, the 50Ω environment is transformed to a 128Ω environment at the test plane. Note that 120Ω will therefore be chosen as the characteristic impedance. This enhances the measurement accuracy, but requires careful calibration.

Therefore the TRL standards in Fig. 4.3 are implemented with $80-\Omega$ lines. In order to obtain accurate diode characterization, the substrate permittivity and thickness are chosen so that a $80\,\Omega$ microstrip line is close in width to the diode leads. For example, in the $80\,\Omega$ TRL kit shown in Fig. 4.3, used to characterize diodes in a plastic packages, a Rogers 4000c substrate with $\epsilon_r = 3.55$ and 0.762 mm



(a) (b)

Figure 4.3: (a) TRL calibration and (b) test circuit used in the source-pull. The test circuit is narrowband and designed to move the impedance of the diode towards the middle of the Smith chart at the design frequency.

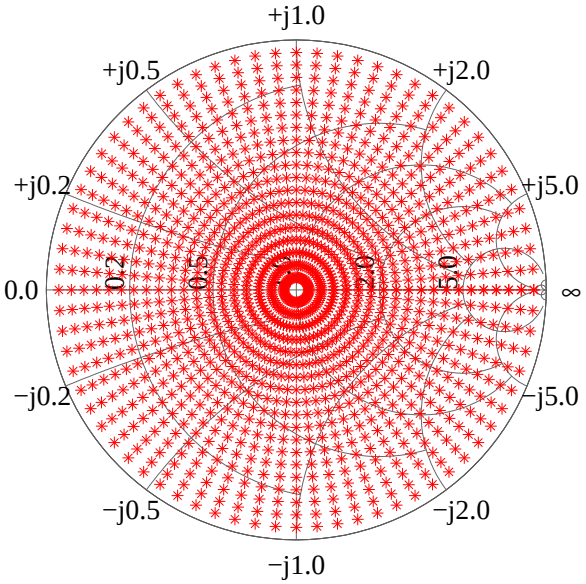


Figure 4.4: Distribution of source-pull measurement points in a $50-\Omega$ environment ($Z_0 = 50\,\Omega$).

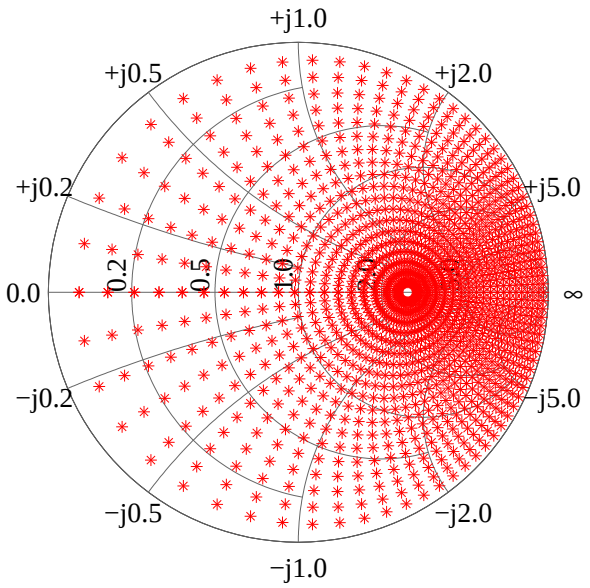


Figure 4.5: Distribution of source-pull measurement points in a $50-\Omega$ environment ($Z_0 = 50\Omega$) transformed by a $\lambda/4$ long $80-\Omega$ line.

(30 mil) thick, resulting in a 0.7 mm wide $80\ -\Omega$ line [55].

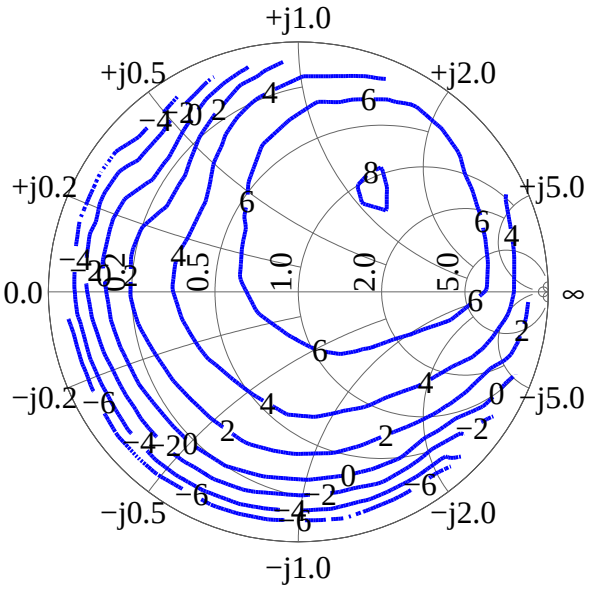


Figure 4.6: Measured rectified power contours for 10 dBm input power. Optimal load $R_L = 460\,\Omega$ at 1.96 GHz. The Smith chart is normalized to $120\,\Omega$.

To obtain the impedance that needs to be presented to the diode for most efficient rectification, the input RF power is varied through a calibrated power amplifier. The voltage across the DC load is measured while the input RF power, input impedance, and DC load resistance are varied at a given frequency. An example of the results of source-pull measurement is shown in Fig. 4.6.

The results of the source pull measurements are of high importance not only to the design of the integrated rectifier antenna and RF circuitry but, also to the design of the DC - CD power converter that provides the DC load to the integrated rectifier antenna, discussed in more detail in Chapter. 2.

The optimal load for rectification efficiency is extracted from the measured data and displayed in Fig. 4.7.

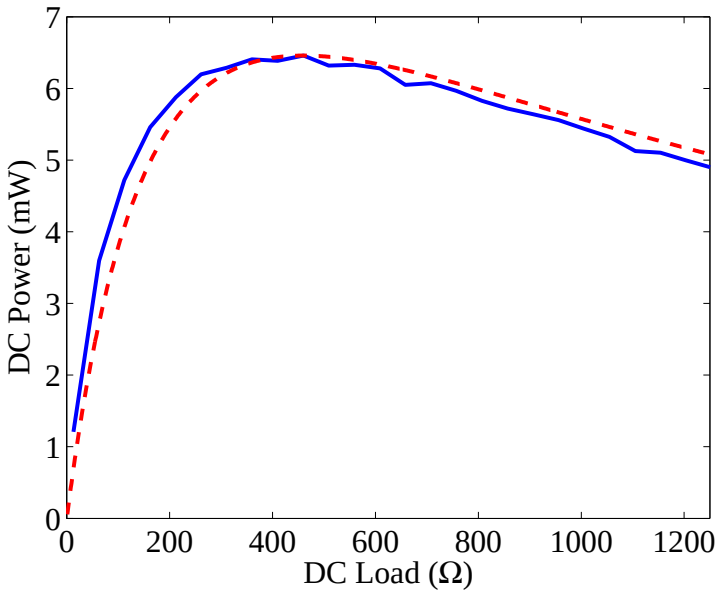


Figure 4.7: Measured DC power for 10 dBm incident power at 1.96 GHz for optimal RF impedance for each load (blue). Load sweep of a Thevenin equivalent voltage source and resistor (red). The Thevenin values were calculated using the data from the maximum output power point on the measured curve.

Each point on the blue curve corresponding to a DC load, is a maximum DC power point from a source-pull measurement sweeping the whole Smith chart. The curve of maximum power is obtained by adjusting the RF fundamental frequency

impedance at each DC load. The resulting curve has the characteristics of a Thevenin equivalent circuit [10, 89], required for power converter design [58, 90], as illustrated in Fig. 4.8.

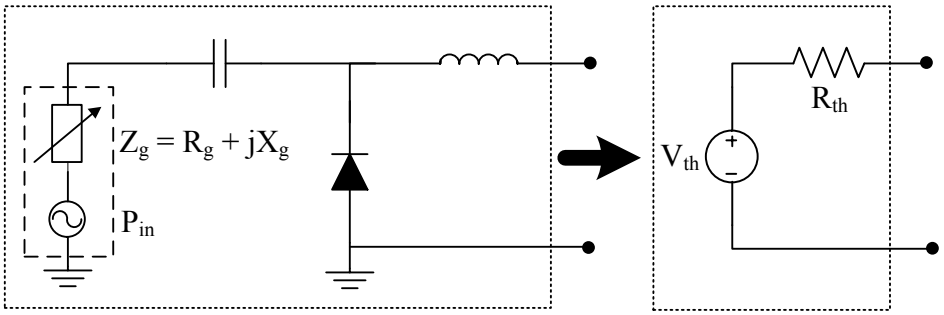


Figure 4.8: Schematic circuit description of the Thevenin equivalent of the rectifier circuit.

4.3 Harmonic Balance Simulations

The source pull measurements give useful design data, but are time consuming, and need to be repeated for different configurations of the diodes, harmonic terminations and different frequencies. To establish a nonlinear simulation which is validated by measurements, a Spice diode model [65] using manufacturer's data is used in harmonic balance simulations in Agilent ADS, as shown in Fig. 4.9. The simulation circuit is slightly different from the measurement circuit, The RF choke and DC load are connected directly to the node the diode is connected to. In the measurement setup, the DC load was connected before the tuner, still in the 50 Ω environment. The location of the RF choke and DC load are not important, as long as the RF impedance to the diode is not impacted by it. The location of the RF choke and DC load can become significant if the structure is designed with as a distributed circuit and provides different harmonic impedances.

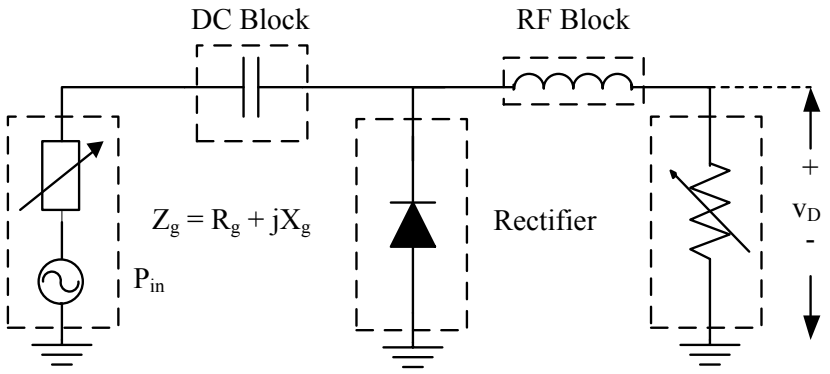


Figure 4.9: Block diagram of Agilent ADS harmonic balance simulations corresponding to the source-pull measurement of Fig. 4.1. Notice that in this case, the DC load is in a transformed RF impedance environment, not 50Ω environment as in Fig. 4.1. The location of the DC load connection in not important, as long as the RF impedance it presents is an open, the the RF impedance presented to the diode is unchanged.

Harmonic balance is a frequency domain method for nonlinear circuit analysis [91, 92]. In this method, the circuit is exited at the fundamental frequency, the simulator iteratively satisfies Kirchoff's laws at all nodes of the circuit, at the fundamental frequency and all harmonics defined by the user. At a given input frequency, and for each input power and DC load, the magnitude of the reflection coefficient at the port is varied from 0 to 0.95, as a compromise between accuracy and computational complexity. For each value of reflection coefficient magnitude, the angle is swept from 0° to 360° in steps of 5°, as shown with the blue points in Fig. 4.10. In this way, constant output DC power contours, shown in red, are obtained for a particular input RF power at a given frequency.

Fig. 4.11 shows results obtained by simulations for the mismatch between the source pulled diode impedance and a 120 Ω characteristic impedance. The TRL trace transforms the tuners characteristic 50 Ω impedance to 128 Ω. The 120 Ω impedance is chosen since, it is close to the center of the Smith chart and places the plotted data in the center of the plot, as described in Section. 4.2. The

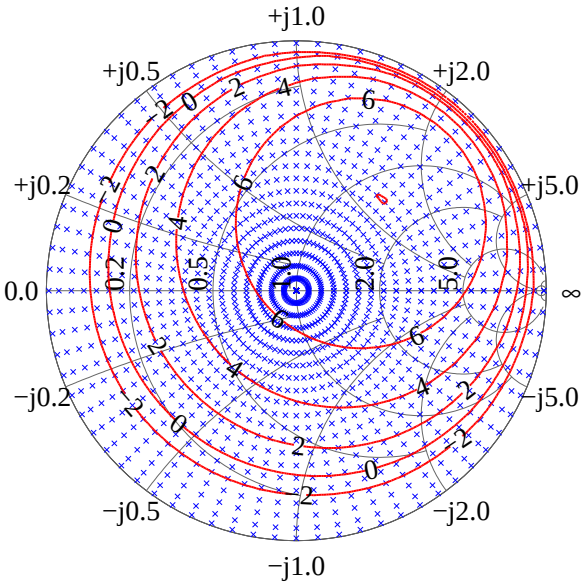


Figure 4.10: Simulated constant rectified power contours at 2 dB increments at 1.96 GHz for a 460 Ω DC load resistance. The results are for a 10 dBm input power for a single Skyworks SMS7630-79 Schottky diode connected to an 80 Ω input line. The maximal rectified power is 7.7 dBm. In this case, the RF-to-DC conversion efficiency is 58%.The Smith chart is normalized to 120 Ω.

contours describe constant DC rectified power (in dBm) for a range of mismatched amplitudes and phases. Note that the same DC power output can be obtained for two RF reflection coefficients, but the maximum output power is obtained within a magnitude range of 0.1 and a phase range of a few degrees.

4.4 Comparison of Harmonic Balance and Source-Pull

Harmonic balance simulations are compared to source pull data for several cases. Examples shown in Fig. 4.12 and Fig. 4.13 are for different DC loads, frequencies and input powers. The measured and simulated contours track well over a range of DC loads from 10 to 1250 Ω and for input power levels of 0 and 10 dBm and at the cellular phone frequency 1.96 GHz as well as ISM frequency of 2.45 GHz for the

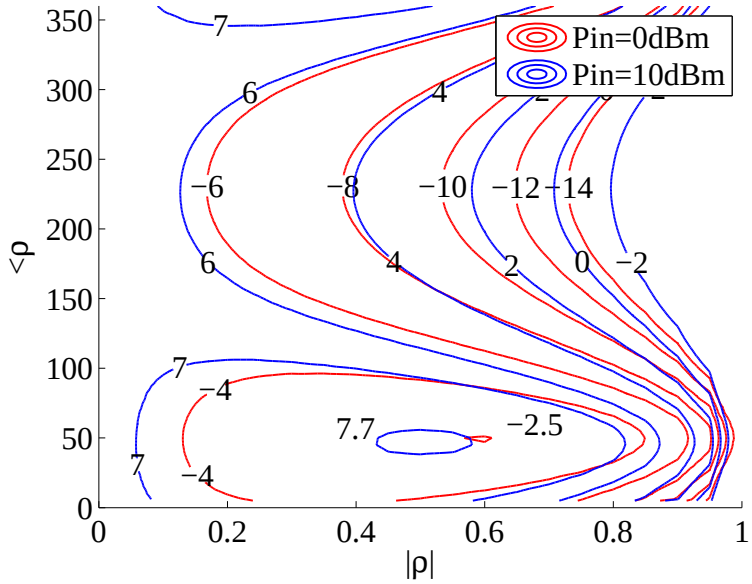


Figure 4.11: Simulated contours of constant DC power for a range of magnitude and phase mismatch between diode impedance and reference impedance, for two values of input power (red and blue traces). The plot shows that the same rectified power can be obtained for multiple values of diode impedance mismatch relative to a 120 Ω characteristic impedance.

same diode(Skyworks SMS7630-79 Schottky diode). Fig. 4.12b shows the case for the optimal DC load at 1.96 GHz. The optimal rectification impedance is used for antenna input impedance design at a given frequency and incident power density.

The initial characterization work and model definitions were done at 1.96 GHz. Source-pull measurements were performed at 2.45 GHz as well, and demonstrating good agrement with simulations as seen in Fig. 4.12. The agreement between simulation and measurement show that the diode model can be used for design with confidence, the model and simulations agree for a variety of different DC loads and frequencies, but not the maximum DC power. Measurements have shown higher output power than the simulations. The impedance is predicted accurately. In all cases investigated in this thesis, the measured power was higher than the predicted by Agilent ADS simulations. In addition, the design is based on the input power and the output power level show the correct trend, even though the

output powers may be 1.5 dB off at the maximum DC power point. Away from the maximum DC power point the simulation and measurement DC powers track well. The power and small impedance differences are summarized in Table 4.1

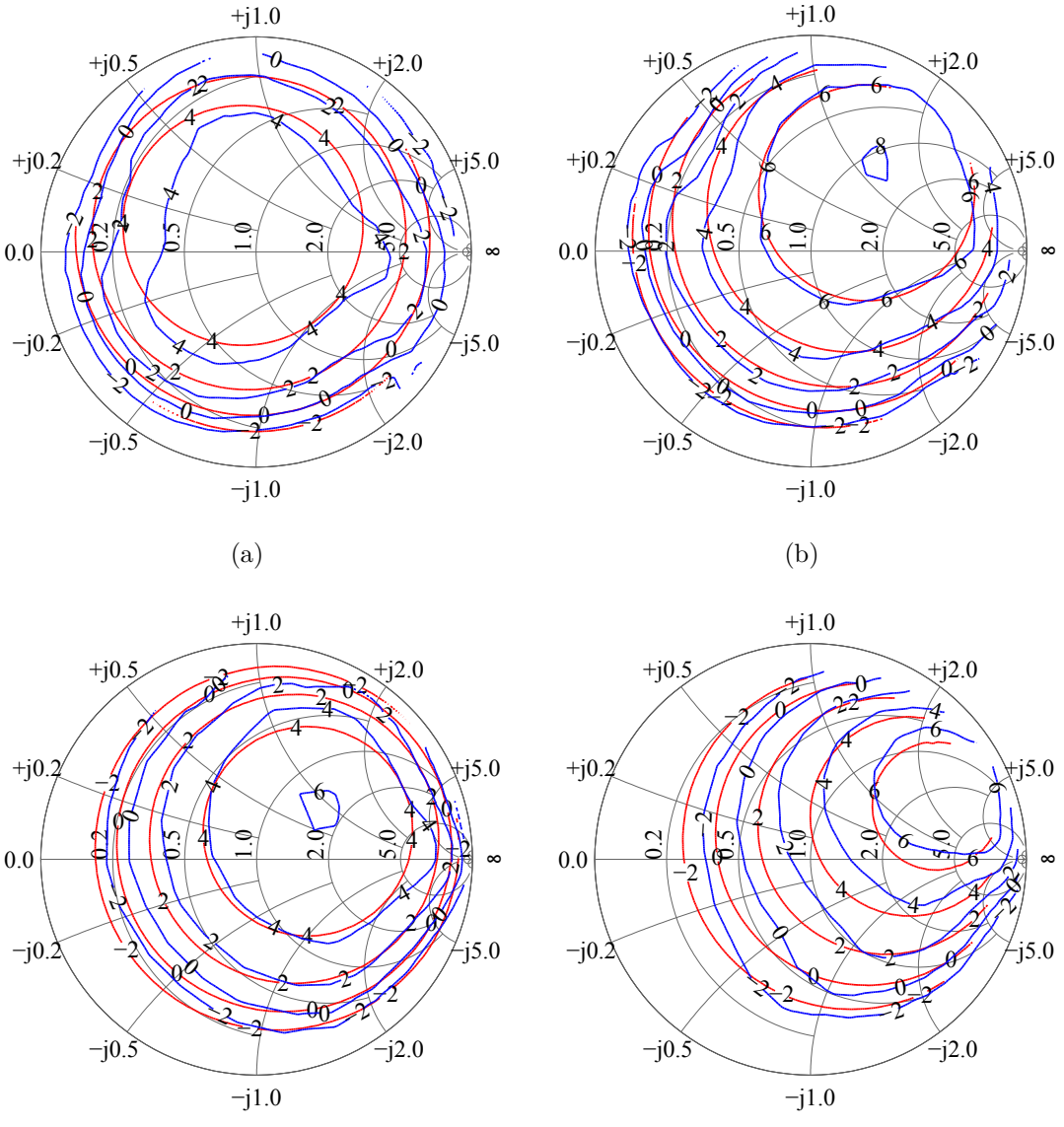


Figure 4.12: Simulated (blue) and measured (red) rectified power contours for 10 dBm input power. $R_L = 60\,\Omega$ (a) and optimal load $R_L = 460\,\Omega$ (b) are at 1.96 GHz. $R_L = 60\,\Omega$ (c) and optimal load $R_L = 485\,\Omega$ (d) are at 2.45 GHz.The Smith charts are normalized to $120\,\Omega$.

The measurements have been repeated for 0 dBm as seen in Fig. 4.12, again

showing agreement with simulations. The model and simulator can be used for predicting the rectified DC power, over a large range of input power, frequency, DC load and input impedances.

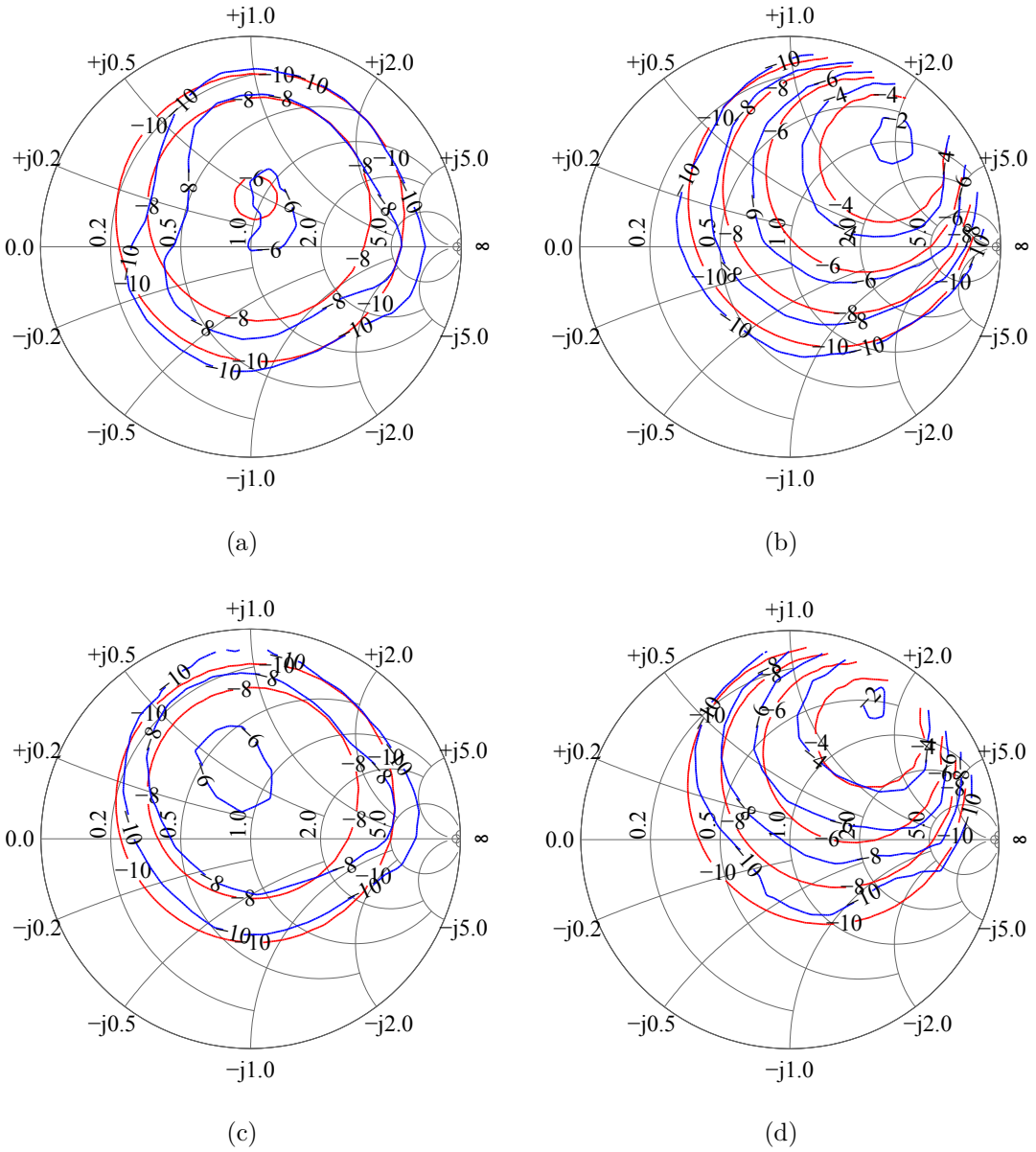


Figure 4.13: Simulated (blue) and measured (red) rectified power contours for 0 dBm input power. $R_L = 63\,\Omega$ (a) and $R_L = 1050\,\Omega$ (b) are at 1.96 GHz. $R_L = 60\,\Omega$ (c) and optimal load $R_L = 1165\,\Omega$ (d) are at 2.45 GHz. The Smith charts are normalized to $120\,\Omega$.

Table 4.1: Summary of measured and simulated rectified power for optimal RF and DC impedance at the diode terminals seen in Fig. 4.12 and Fig. 4.13

f (GHz)	$P_{in,RF}$ (dBm)	R_{DC} (Ω)	P_{DC} (dBm)		$Z_{RF}@f_0$ (Ω)		η_{RF-DC} (%)	
			Meas	Sim	Meas	Sim	Meas	Sim
1.96	10	460	8.1	7.2	137+j149	146+j151	64.5	52.4
		60	5.6	5.5	109+j33	97+j51	36.3	35.5
	0	1050	-1.64	-2.15	94+j253	110+j235	68.5	61.0
		60	-5.84	-5.93	142+j52	108+j60	26.1	25.5
2.45	10	485	7.7	6.8	178+147	114+134	58.8	47.9
		60	5.6	4.04	87+31	90+43	36.3	25.4
	0	1165	-1.85	-2.56	73+j203	80+j200	65.0	55.5
		60	-5.6	-6.08	79+j81	98+j64	27.5	24.7

4.5 Harmonic Balance Simulation and Large Signal Scattering Parameters Analysis

As seen by the simulations in Section 3.3.1 the waveforms deviate from the ideal waveform significantly. By comparing the rectifier and amplifier classes of waveforms, it is clear that the class C (reduced conduction angle) topology deviates the least, as seen in Fig. 3.27 and Fig. 3.29. The voltage waveforms are identical in both figures, while the current waveforms, although not identical, share many characteristics. Large Signal Scattering Parameters (LSSP) simulations can give insight to the reasoning of this finding.

4.5.1 Large Signal Scattering Parameters

The LSSP feature of Agilent ADS computes S-parameters for nonlinear circuits using harmonic balance techniques for each input power level and frequency point.

Since LSSPs are for nonlinear circuits, they are power dependant. As in the case of small signal S-parameters, LSSPs are defined as the ratio of reflected to incident waves [93]:

$$S_{ij} = \frac{B_i}{A_j}, \tag{4.3}$$

where the incident are reflected waves are defined as:

$$A_j = \frac{V_j + Z_{0j} I_j}{2\sqrt{R_{0j}}}, \qquad B_j = \frac{V_i - Z_{0i}^{*} I_i}{2\sqrt{R_{0i}}} \tag{4.4}$$

and:

V_i and V_j are the voltage Fourier coefficients, and I_i and I_j are the current Fourier coefficients for the fundamental frequency at the ports i and j. Z_{0i} and Z_{0j} are the reference impedances of the ports i and j and R_{0i} and R_{0j} are the real parts of Z_{0i} and Z_{0j}.

For a two port system, $port_2$ is terminated with the complex conjugate of its reference impedance. Then using a source at $port_1$ whose impedance is the conjugate impedance of that port, a signal is applied at power level P_1. Next, using harmonic balance, the currents and voltages at $port_1$ and $port_2$ are calculated. The information is used to calculate S_{11} and S_{21}. Next, for calculating S_{22} and S_{12}, $port_1$ is terminated with the conjugate of its reference impedance and a power P_2 is applied at $port_2$ where $P_2 = |S_{21}|^2 P_1$ using a source with $port_2$ conjugate impedance. Again, using harmonic balance, the voltages and current are found and S_{22} and S_{12} are calculated [93, 94].

4.5.2 Simulation Results

The circuit in Fig. 4.14 is simulated using Agilent ADS LSSP simulation. Simulation results are shown in Fig. 4.15, for the Skyworks SMS-7630-79 diode [56].

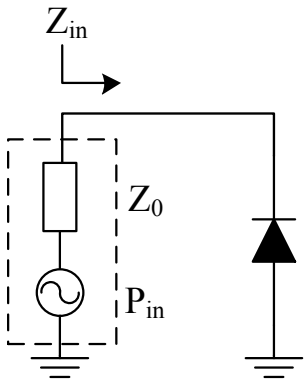


Figure 4.14: circuit used to simulate input impedance of the diode as a function of input power at 2.45 GHz. The harmonic balance technique using 25 harmonics is used to find the voltages and currents at every node.

For an input power sweep from -30 dBm to 30 dBm at 2.45 GHz using 25 harmonics for analysis, the 10 first harmonic impedances are plotted. The complex input impedance at each frequency is calculated from the S-parameters using

$$Z_{in} = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{4.5}$$

The results are plotted in Fig 4.15, where the real part of the impedance is in red and the imaginary in blue. The real part of the fundamental frequency is dashed red and the imaginary is dotted blue, the rest of the harmonics are plotted in solid lines (both real and imaginary components get closer to zero as the order of the harmonics increase). Notice that the both components of the impedance change in a very nonlinear way as a function of input power. Further investigation leads to examining the capacitance of the diode. Subtracting R_s from the diode impedance results in the parallel combination of R_j and C_j. Separation of the parallel combination yields the junction capacitance and resistance separately. The capacitance is changing with the input power, as seen in Fig. 4.16. It is interesting to see that for low powers (up to -20 dBm) the capacitance stays constant for

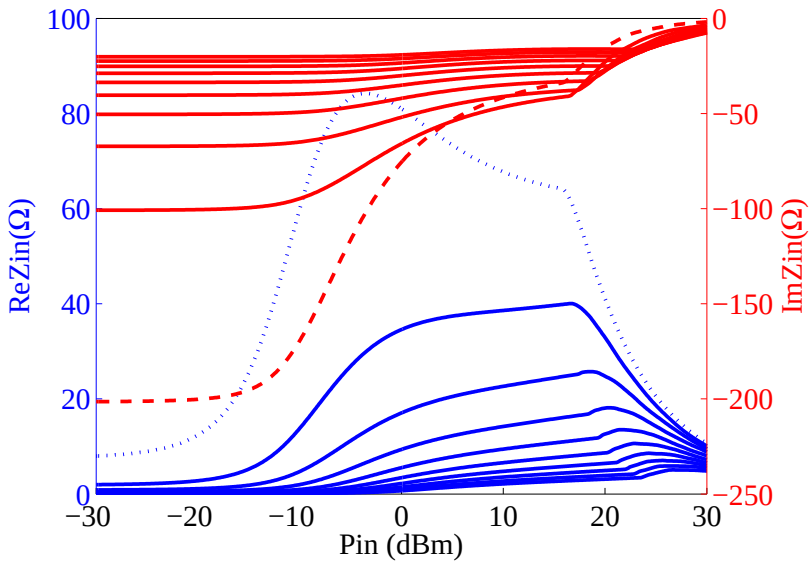


Figure 4.15: Simulated input impedance of the diode as a function of input power at 2.45 GHz. Blue - real part of the diode impedance, dotted - fundamental , solid - harmonics. Blue - imaginary part of the diode impedance, dashed - fundamental , solid - harmonics. Based on measurements, we trust the model on to 10 dBm.

the fundamental and the harmonics at 0.32 pF, at higher powers, the capacitance exhibits strong nonlinear behavior, different for each driving frequency.

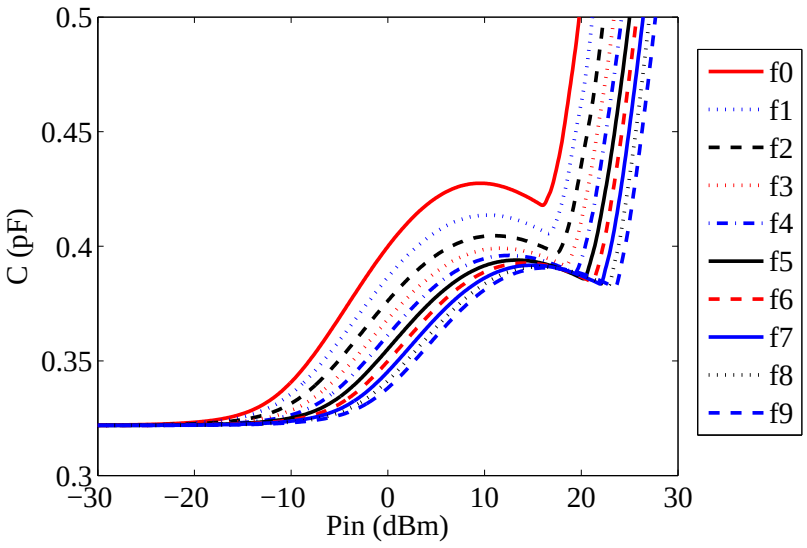


Figure 4.16: Input capacitance of the diode as a function of input power at 2.45 GHz and the first nine harmonics. For each curve the circuit is exited by one frequency at a time over the range of powers.

In the shunt diode configuration of the rectifier, the diode capacitance is in parallel with any harmonic impedance presented to the diode. In a parallel combination, the lower impedance is the dominant and as so, any high impedance presented at the harmonics to the diode is not significant. This means that all open terminations of the harmonics are in parallel to a capacitor. The capacitive impedance gets lower as the frequency increases, and hence the parallel harmonic open termination, has very small effect on the total impedance, and therefore on shaping the waveforms. The magnitude of the diode impedances changes with incident power and frequency as shown in Fig. 4.17. As the input power increases,

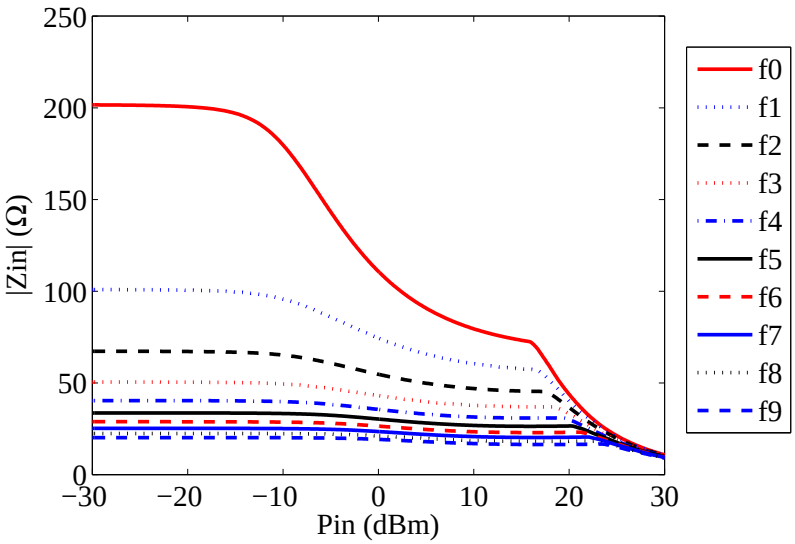


Figure 4.17: Magnitude of the input impedance of the diode as a function of input power at $f_0 = 2.45\,\text{GHz}$ and the first ten harmonics.

the impedance magnitude decreases and makes the open terminations insignificant. The open terminations lose effect as the frequency and power increase. Since the class-F and class-F^{-1} rectifier topologies have open terminations at every other harmonic, they are not suited well for operation with the diode. Any topology that is based on short terminations such as the reduced conduction angle class-C topology will work well with a diode that exhibits this nonlinear capacitance

behavior.

Source-pull measurements where the input power was above 10 dBm at the diode plane, resulted in damage to the diode. The diode does not complectly burnout, but its rectification performance degrades. The damage to the diode was observed also in measurement and characterization of the integrated rectifier antenna, when power densities were such that the input power to the diode was above 10 dBm. The damage to the diode is due to voltages above the breakdown voltage and high currents through the diode as a result of the high incident power. Due to these observations, the model for Skyworks SMS-7630-79 Schottky diode can only be trusted up to an input power level of 10 dBm. The simulation results seen in Fig. 4.15 to Fig. 4.17 should also be trusted only up to that input power.

4.6 Summary

This chapter presents methods for experimental-based rectifier modeling and non-linear frequency-domain simulations of microwave rectifiers using harmonic balance. The goal of the work shown in this chapter is to extend the theory and analysis presented in Chapter. 3 to design-oriented simulations and experimental validations of the nonlinear models. The simulations are performed using harmonic balance in commercial circuit simulators (Agilent ADS), while the experimental validity of the diode nonlinear model is demonstrated with a modified source-pull power-amplifier method developed specifically for rectifiers. The close agreement between the two, which follows trends from Chapter. 3, provides confidence in the non-linear simulation for future designs. The validation is specifically performed for diodes used in this work, but also demonstrates a method by which the model validity can be determined more generally.

The contributions of this work are reported in the following publications: [85, 84]

Chapter 5

Antenna and Rectifier; design, integration and Measurement

The highest activity a human being can attain is learning for understanding, because to understand is to be free.

—Benedict de Spinoza

Contents

5.1 Antenna Design For Integration With Rectifiers

For many integrated rectifier antenna designers, e.g. [95, 96], the design involves matching to a 50 Ω antenna load. Rectifiers, are often designed with an input match of 50 Ω as well [96, 63]. The intermediate 50 Ω impedance, makes the rectifier portion of the system testing simple. The rectifier integration with the antenna then seems as a natural and straightforward process. However for integrated rectifier antennas, the intermediate 50 Ω impedance is meaningless, since there is no need for integration or connection to any 50 Ω system. Avoiding the 50 Ω match allows for less matching circuitry, and thus reduces loss and compact design. As discussed in earlier chapters, the diode impedance is mostly capacitive and creates a large magnitude of Γ with respect to 50 Ω. Therefore, any matching circuit to 50 Ω will have high insertion loss [97]. The available power at the antenna port would go through an unnecessary attenuation before it reaches the rectifier. The match to 50 Ω adds a design constraint that can be avoided. The method developed here attempts to design the matching to the experimentally-determined optimal diode impedance by antenna input impedance co-design.

This chapter is devoted to detailing the co-design procedure on the example of a narrowband 1.96 GHz cell-phone frequency patch antenna integrated with a

Schottky diode. The steps of the procedure are: (A) antenna design for complex impedance feed point and validation of antenna impedance performance; and (B) validation of integrated antenna, matching circuit and bias line performance and finally, integrated rectifier antenna performance test.

5.1.1 Antenna Feed Point Design

Antenna full-wave simulations (Ansoft HFSS) are used with the goal of obtaining the highest radiation efficiency, desired radiation pattern and determining the feed with a complex impedance presented to the diode for best conversion efficiency, as determined by HB simulations or source-pull measurements. Most antenna simulations refer to the magnitude of the reflection coefficient, while in the integrated rectifier antenna design process, both the real and imaginary part of the impedance are of interest. Rather than matching to the standard $50\,\Omega$, the design attempts to obtain a match to the optimal diode complex impedance. Fig. 5.1 shows the geometry of a patch antenna in which several feed points (labeled 1-7), the different feed points are simulated and measured in order to determine the sensitivity of the complex impedance to patch feed location and parasitic reactance associated with the connector. Fig. 5.2 shows the simulated and measured complex impedances for patch geometry from Fig. 5.1. The dashed line is the result of a simulation where a 50Ω coaxial feed is excited with a waveport, while the solid line, which closely matches the experimental data, includes the full 3-D SMA connector model in the simulation. From these results, it is clear that the complex impedance of the antenna is extremely sensitive to the feed structure and parasitics associated with the feed connector, even at this relatively low frequency [98, 99, 100]. Notice also that the reactance is much more sensitive than the resistance, and thus a plot of $|S_{11}|$ (or return loss) would not show this sensitivity. The use of a connector in this simulation allows a modular approach to design and measurement, the response of

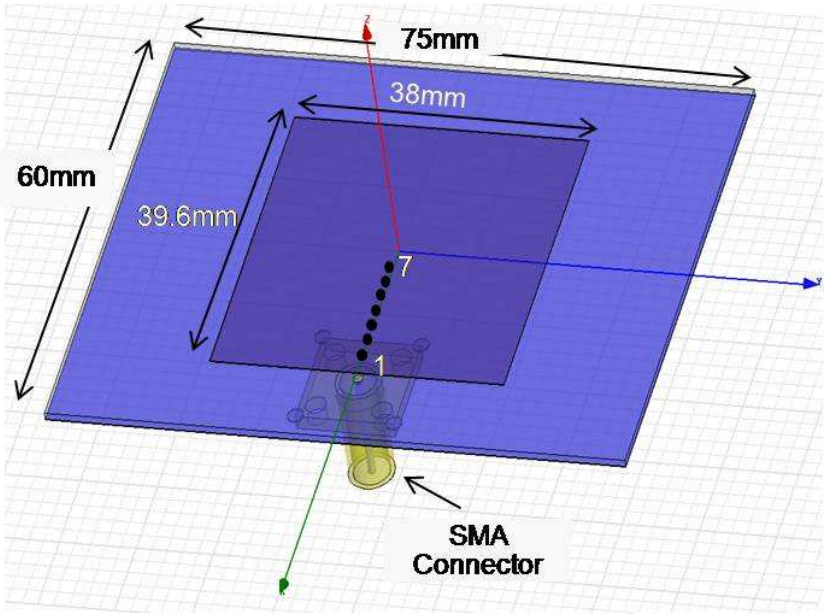


Figure 5.1: Geometry of patch antenna with 3D detailed SMA connector implemented in Ansoft HFSS. The antenna was simulated with 7 different feed point locations. For validation, the same geometry was fabricated. The feed points are located along the center axis that is parallel to the non-radiating edge of the antenna. Feed number 1 is at the radiating edge feed number 7 is 6 mm away from the center, the rest of the feed locations are evenly spaced between them.

the connector modifies the impedance to the connecting external circuits and must be taken into account. Once the design is finalized and validated, a more compact and integrated approach excluding connectors between the antenna and matching circuitry is implemented. An example is discussed in Chapter 6.

5.1.2 Antenna, Matching and DC Line Design Validation

The impedance range shown in Fig. 5.2 does not reach exactly the optimal diode impedance. There is an additional degree of freedom in choosing the antenna feed point, and in the design presented here, a point 14mm off the center of the patch is used. It is chosen so that the matching network to the diode is simple. In addition, simulation and measurement have excellent agreement at that point. Note that

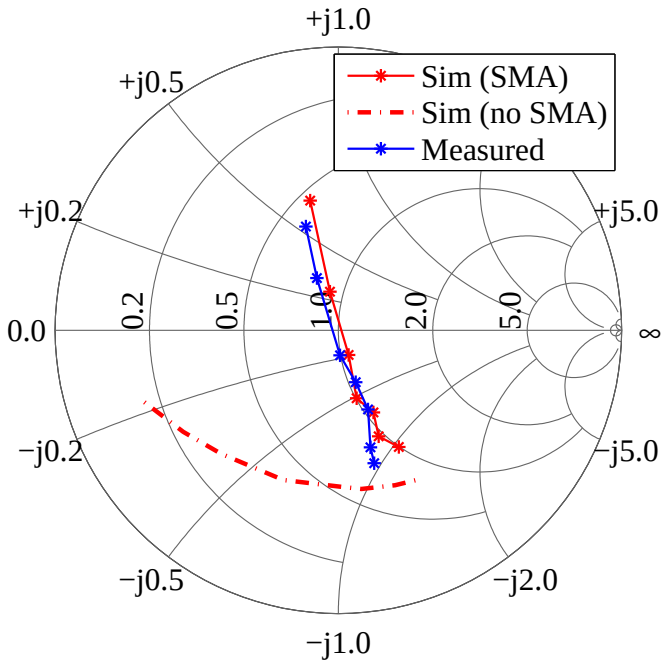


Figure 5.2: Simulated and measured results of the antenna complex impedance. The dashed line shows the simulation without the full SMA connector implemented in HFSS. The Smith chart is normalized to 120 Ω.

for different antenna designs and diodes, it might be possible to eliminate the matching circuit altogether.

The next step in the design procedure is validation of the full passive part of the integrated rectifier antenna, including the matching circuit and DC output line. A series of steps are taken to validate the performance of the passive part of the integrated rectifier antenna, prior to adding the diode. First, a trace from a connector to the calibration reference plane where the diode will be connected is inserted (this trace is not needed after validation and can be removed). This TRL-calibrated measurement validates that the exact source-pull determined diode impedance is obtained with the fabricated antenna and matching circuit as seen in Fig. 5.3.

The match between the antenna and the diode can be obtained in many ways. In this example, the method of a stepped impedance line is used. Fig. 5.4 describes

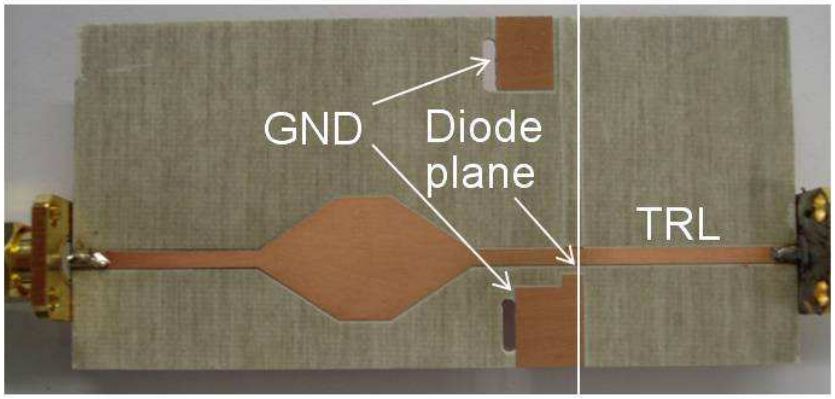


Figure 5.3: Photograph of impedance validation circuit. The SMA connector on the left that is assumed to be connected to the complex impedance feed of the antenna. The stepped impedance circuit is matching the antenna impedance to the diode impedance at the fundamental frequency. The impedance is validated by measurement at the diode. The TRL calibration portion of the circuit on the right can be removed after validation.

the match progression. The antenna impedance including the connector impedance

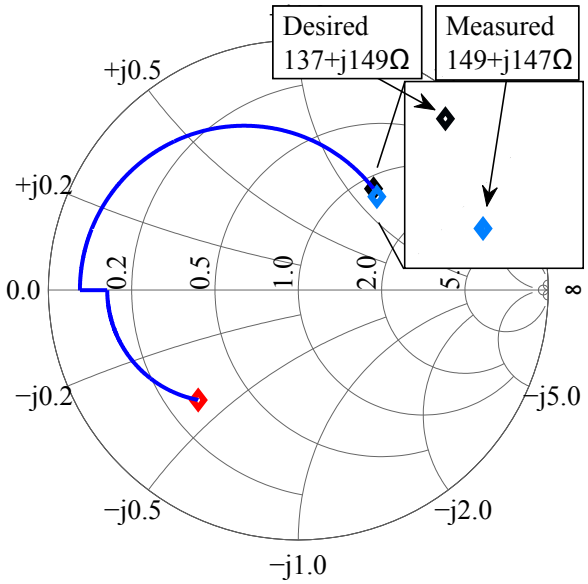
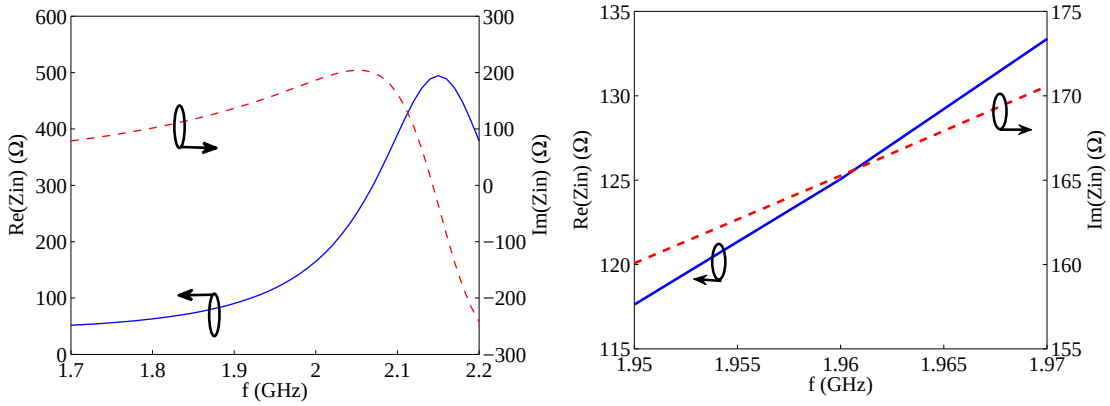


Figure 5.4: Measured impedance presented at the diode reference plane is within a few ohms from the desired complex impedance. The red data point shows the antenna impedance at the feed point. The blue trace shows the transformation due to the matching circuit. The curves connecting the measured points show the matching procedure. The Smith chart is normalized to 120 Ω.

is labeled by the red diamond. The first microstrip trace form the right in Fig. 5.3 is a 50 Ω line that transforms the impedance to a real impedance. The diamond-shaped thick line is a $\lambda/4$ transformer that transforms the impedance to the correct $|\Gamma|$. Finally, an additional 50 Ω line changes the phase of Γ and transforms the impedance to the desired diode impedance. The blue trace in Fig. 5.4 describes this progression.

Patch antennas are narrow band by nature, on the order of 5% depending on definition of band-width, substrate and thickness [101, 102]. Since the antenna and matching circuitry are narrow band, it is important to make sure that the match will work if any of them are a bit detuned in any direction. If the two are narrow band and detuned in opposite directions, the performance will degrade very quickly. For that reason, in this case the match is tested over a band from 1.7 GHz to 2.2 GHz. Fig. 5.5 shows the real and imaginary components of the input impedance looking in at the diode reference plane for a fixed load. In order to

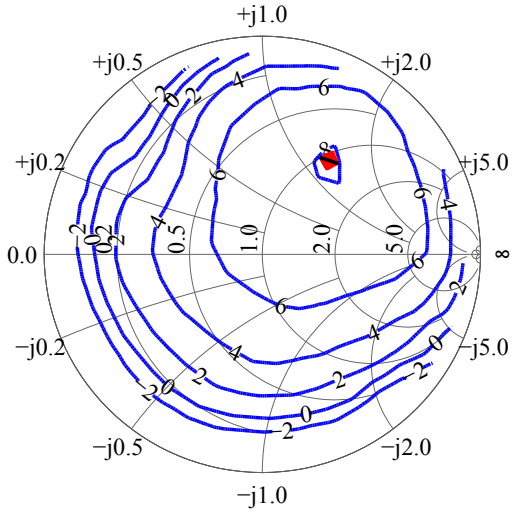


(a) (b)

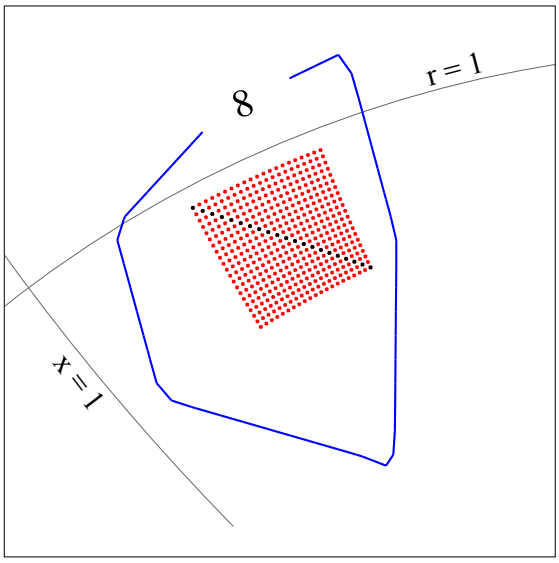
Figure 5.5: Real and imaginary parts of the input impedance at the diode plane (a) a close up of the same impedance data in the band of interest (b).

assure the diode will be presented with a impedance that is acceptable for small frequency variations, the resulting impedances are overlayed with the source-pull constant DC power contours as seen in Fig. 5.6. As can be seen in the close up in

Fig. 5.6b, all impedance combinations are well within the maximum power contour, and assure maximum rectification efficiency.



(a)

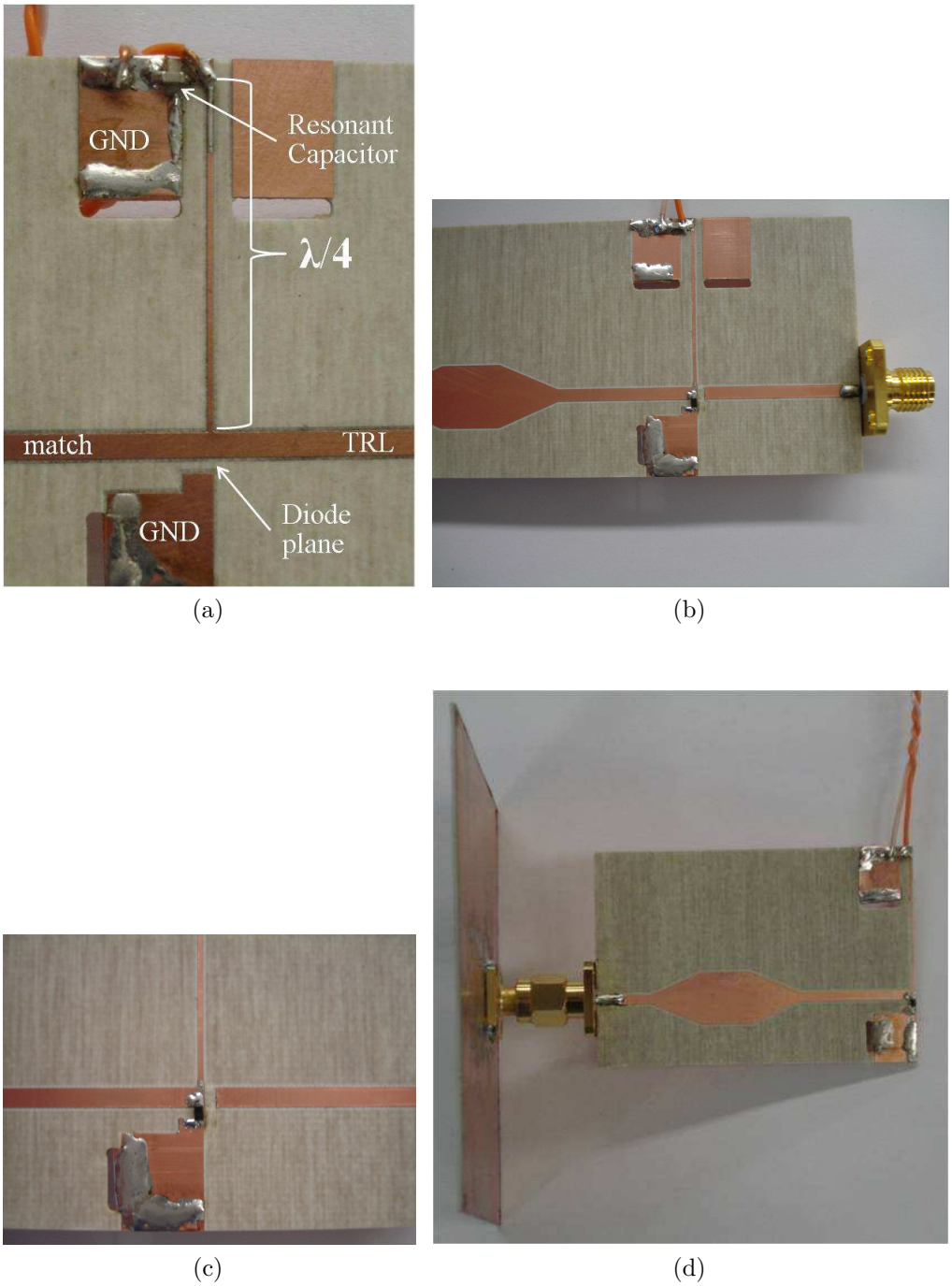


(b)

Figure 5.6: (a) Measured source pull contours at 1.96 GHz in blue for Skyworks SMS-7630-79 Schottky diode at an input power of 10 dBm. The black symbols are the complex impedances combinations from 1.7 GHz to 2.2 GHz shown in Fig. 5.5b and the Red are all possible combinations of each point of the real part of the impedance with each of the imaginary parts within that band. (b) a close up of the maximum DC power contour with the impedance combinations. The Smith chart is normalized to 120 Ω.

The next step is to add the DC collection line, without disturbing the fundamental frequency impedance match. The DC line which consists of a quarter-wave microstrip section and shunt resonant surface mount capacitor shown in Fig. 5.7a. The resonant capacitor presents a short which is transformed through the quarter-wave long transformer and presents an open at the fundamental frequency to the diode plane. While not effecting the RF impedances, the quarter-wave transformer provides a DC path to the DC load. Other ways of extracting the DC are available, such as different lumped element bias Tees, or fully distributed configurations. This configuration is dependant on a combination of a lumped element and distributed circuitry, and is very repeatable in fabrication. The combination of distributed and lumped elements gives a reasonable size circuit which is simple to assemble. Another reason to use the resonant capacitor is that it shorts higher harmonics and as such, in combination with the quarter-wave at fundamental, provides shorts at the even harmonics. The quarter-wave line at the fundamental becomes a half-wave at the second harmonic and a integer multiple of a half-wave line at all even harmonics. As the frequency increases, it moves farther from the resonant frequency of the capacitor, and the termination moves away from a perfect short.

The TRL calibrated measurement allows validation that the fundamental impedance does not change regardless of the load connected past the resonant capacitor. Finally, after validation, the TRL trace is cut and a diode is soldered between the diode plane and ground as seen in Fig. 5.7b with a closeup of the soldered diode in Fig. 5.7c. After testing, the substrate that the TRL trace is on can be trimmed and a more compact circuit is obtained as seen in Fig. 5.7d. The specific matching circuit is shown in Fig. 5.8, the measurement results are shown in Fig. 5.4 with the red data point being the antenna feed point impedance. The blue trace is a set of transformations for a multiple-section transmission line match to the desired impedance ($137 + \mathrm{j}149\,\Omega$), as shown in the inset. The measured



(a) (b)

(c) (d)

Figure 5.7: Photographs of the validation circuits for the antenna, matching, DC collection circuit and full integrated rectifier antenna. (a) DC collection circuit added to matching circuit. (b) TRL trace cut at the reference plane for measuring the impedance presented to the diode. (c) Closeup of the cut TRL line and the diode soldered in place. (d) The full integrated rectifier antenna after trimming the excess substrate from the validation portion of the circuit.

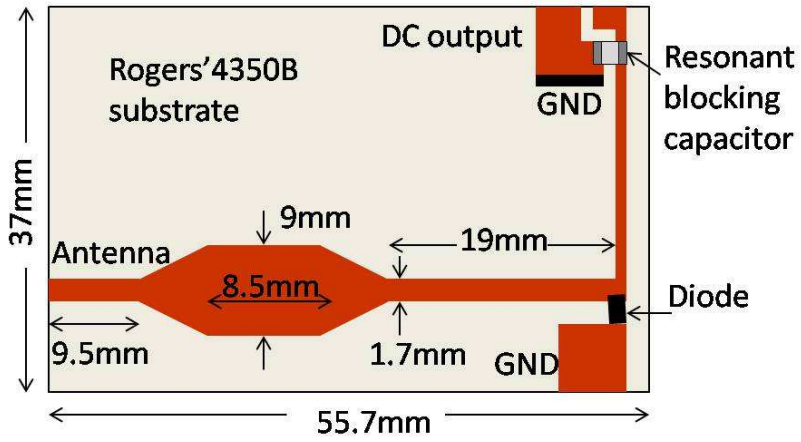


Figure 5.8: Layout of the matching circuit used to transform the antenna complex impedance to the optimal diode complex impedance.

impedance is within a few Ω from the desired one.

5.2 Integrated Rectifier Antenna Characterization

In order to validate that best rectification is obtained for the match closest to the optimum, three integrated rectifier-antennas were tested. The antenna and matching circuit are connectorized for measurement purposes and allow validation of each part. Additional line length between the antenna and matching circuit moves the diode match from the optimal A1 to suboptimal A2 and A3 as seen in Fig. 5.9. The impedances were chosen to be on DC power contours separated by approximately 2 dB; the exact powers are given in Table 5.1.

All three test integrated rectifier antennas A1 to A3, use the same antenna, matching circuit and DC circuit, but have different length adapters added to change the matching to the diode, reducing uncertainty due to parasitics and fabrication tolerances as seen in Fig. 5.10. For each case, the integrated rectifier antenna was fully characterized, and the efficiencies compared.

Table 5.1: DC output power from source pull measurement at 1.96 GHz, input power of 10 dBm and DC load of 460 Ω for the three matching conditions of integrated rectifier antennas A1 to A3.

Antenna	DC power (dBm)
A1	8
A2	5.6
A3	4.5

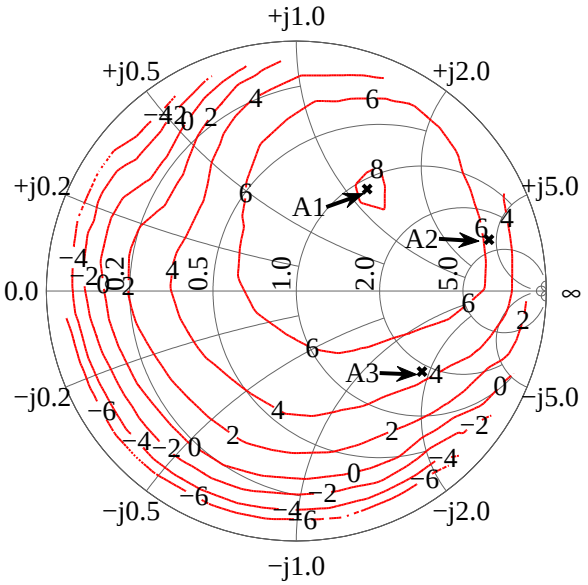
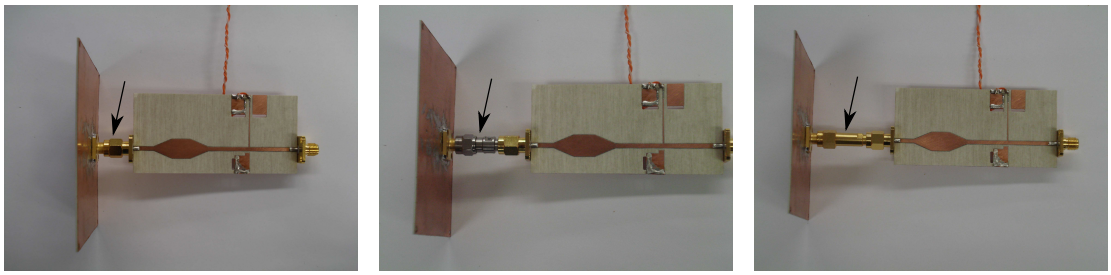


Figure 5.9: Measured diode load-pull contours for rectified DC power with superimposed impedances that antennas A1-A3 are matched to (black symbols). This data is for the optimal DC load for antenna A1, and sub-optimal load for A2 and A3. The Smith chart is normalized to 120 Ω.

5.2.1 Measurements and Calibration

Antennas A1 through A3 were characterized in a calibrated setup as illustrated in Fig. 5.11. The source is an HP83650A synthesizer feeding a 40 dB gain power amplifier (maximum power 30 W), allowing far field measurements to be performed for a range of incident power densities on the integrated rectifier antenna at normal incidence. The calibration procedure is performed with two equal calibrated AEL



(a) (b) (c)

Figure 5.10: Photographs of the integrated rectifier antenna with three different matches. (a) integrated rectifier antenna A1, the diode is presented with the optimal fundamental frequency impedance. (b) By adding a line section between the antenna and matching circuit the diode is presented with a sub-optimal impedance, A2 and (c) a longer adaptors between the antenna and rectifying circuit moves the impedance farther away from the optimal, A3.

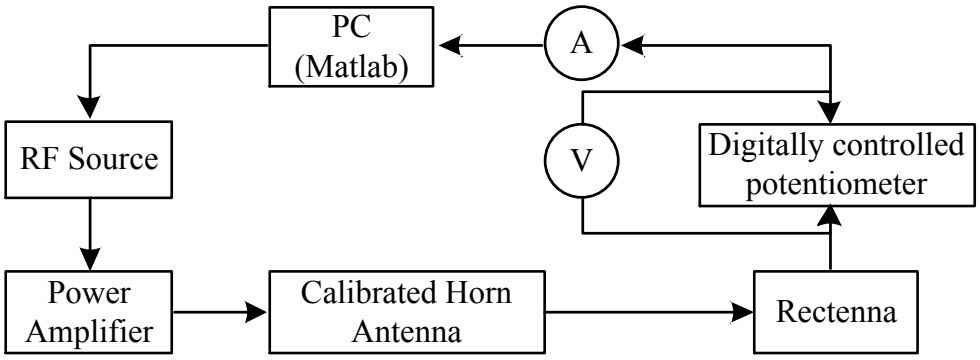


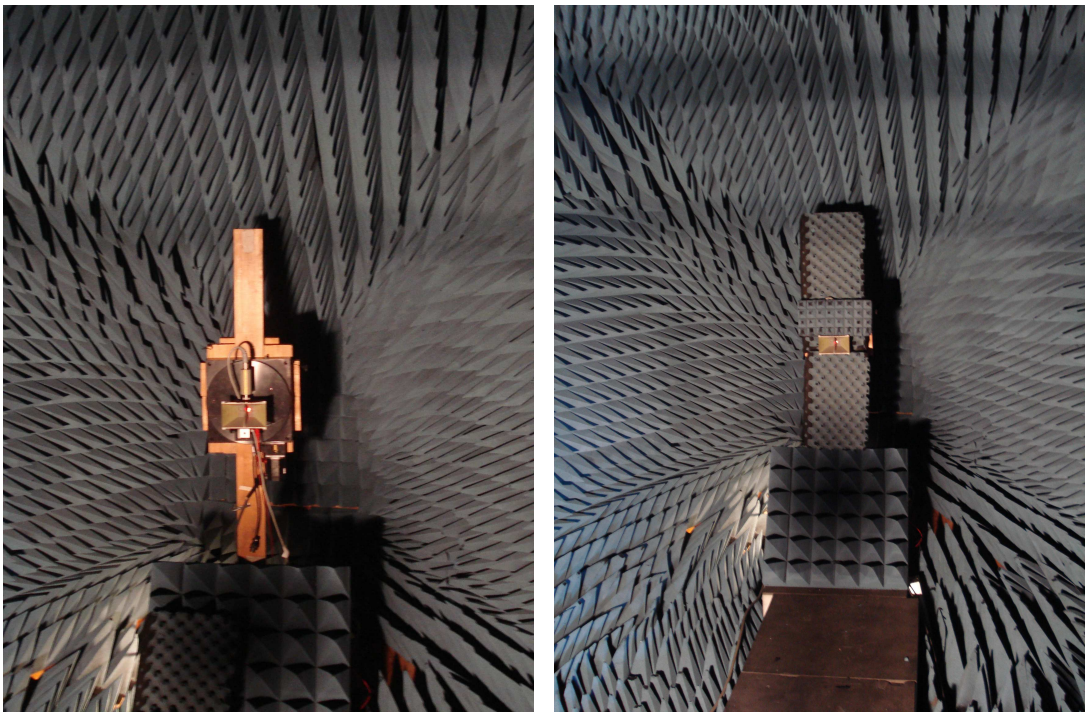
Figure 5.11: Block diagram of measurement setup for obtaining calibrated rectified power levels and efficiencies over a range of normally incident power densities and DC loads.

H-1498 broadband horn $G(1.96\,\text{GHz}) = 3.7\,\text{dBi}$ antennas. The power density at the plane of the integrated rectifier antenna is found from:

$$S(\theta = 0°, \phi = 90°) = \frac{4\pi P_{CAL}}{G_{CAL}\lambda^2} \tag{5.1}$$

where G_{CAL} is the gain of the receiving calibrated horn antenna and P_{CAL} is the RF power measured at the receiving horn output when the aperture is at the reference plane. Fig. 5.12 shows the alignment of the horn antenna on the

wooden rack. Notice the red dot in the center of the antenna, the alignment of the antennas is done using a level with a laser pointer to make sure the antenna are aligned properly (facing each other and are co-polarized as in (5.1). After the power densities are calibrated, the horn and power meter are removed, and next, the integrated rectifier antenna is placed at the reference plane. The rectified power is measured over precisely controlled DC load values, for incident power densities from 25 to 200 μW/cm^2. The measurements are performed in an anechoic chamber shown in Fig. 5.12.



(a) (b)

Figure 5.12: Photographs of the calibrated AEL H-1498 broadband horn $G(1.96GHz) = 3.7$ dBi antenna mounted on wooden mount (a). the mount is equipped with two step motors allowing rotation of the antenna under test in to axis. After alignment, the mount and measuring equipment are covered with RF absorber material (b), and the antenna is ready for RF measurements.

The whole characterization procedure is controlled by computer using MATLAB. Fig 5.11 shows in detail the setup after power density calibration where the

integrated rectifier antenna is placed at the reference plane. The DC load is swept in steps of $5\,\Omega$ while recording the voltage and current through the load at each step.

5.2.2 Efficiency Definition

The efficiency is found from

$$\eta_{RF-DC} = \frac{P_{DC}}{P_{RF,in}} = \eta(f, P_{RF,in}, R_{L,DC}). \tag{5.2}$$

By assuming that the effective area of the integrated rectifier antenna is the largest possible, i.e. equal to the geometric area, A_G:

$$\eta_{RF-DC} = \frac{V_{DC}^2}{R_L} \cdot \frac{1}{S(\theta = 0°, \phi = 90°) \cdot A_G} \tag{5.3}$$

The denominator in (5.3) over-estimates the RF power delivered to the diode, therefore the efficiencies reported here are conservative lower bounds, and are precisely calibrated for normally co-polarized incident powering waves. Other efficiency definitions have been reported in the literature. For example in [29, 103] P_{in} is the RF power delivered to the diode based on the Friis formula (5.4)

$$\eta'_{RF-DC} = \frac{V_{DC}^2}{R_L} \cdot \frac{1}{G_t G_r P_t (\frac{\lambda}{4\pi r})^2} \tag{5.4}$$

were P_t, G_t and r are the transited co-polarized power gain and distance of the transmitter, separately. G_r is found from measurement or simulation of an equivalent antenna without the rectifier. Thus, this definition does not take into account the non-linear loading of the antenna by the feed, coupling between the rectifier and antenna, mismatch and ohmic losses. Small errors in r, G_r, P_t, G_r have a large effect.

Another definition in the literature, for example [27], uses measured power density at the integrated rectifier antenna plane and estimates the effective area of the antenna obtained through gain measurement or simulation:

$$\eta''_{RF-DC} = \frac{V_{DC}^2}{R_L} \cdot \frac{1}{S \cdot A_{eff}} \tag{5.5}$$

As in (5.4) the antenna gain is found for a fixed (usually 50-Ω) load, and does not take in to account gain changes due to non-linear rectifier loading. A comparison of (5.3) to (5.5) for a specific integrated rectifier antenna is given in section 5.2.3.

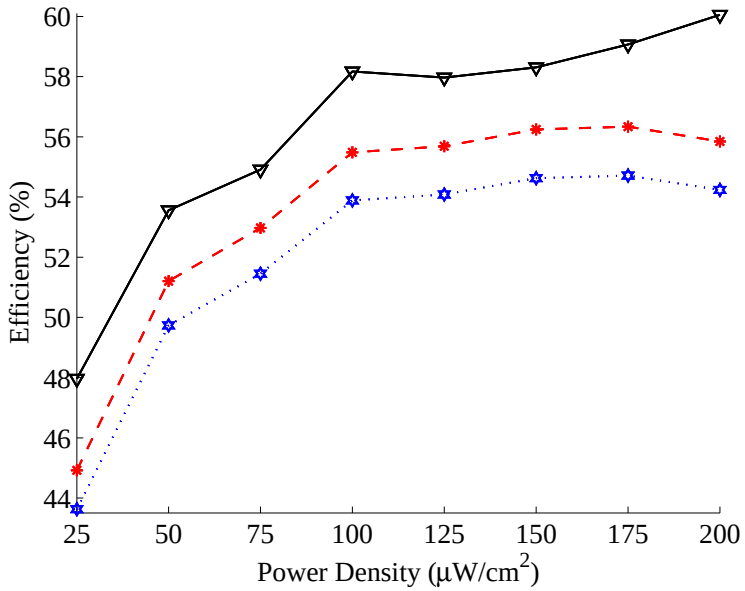


Figure 5.13: Measured efficiency using (5.3)-Blue, (5.5)-Red and (5.4)-Black. The RF power in(5.5) is found by multiplying the power density by the effective area of the antenna obtained from HFSS simulations with a fixed 50Ω port impedance. The input power in (5.4) is obtained from measured power from a reference patch antenna with same geometry as the integrated rectifier antenna but matched to 50Ω and connected to a power meter.

The efficiency definition (5.3) reported in this work gives measured values for A1 between 43%-54% for power densities of 25 to 200 μW/cm^2 as shown in blue in Fig 5.13. Comparing to results obtained from (5.4)-(5.5) with the same measured data shows that (5.3) cannot over estimate the total RF-DC efficiency. An error

source for the efficiency definition in (5.3) could be inaccurate gain of the reference antenna used for power density measurement. The horn antenna used is an AEL H-1498 broadband horn, with gain calibrated by NIST. The gain was verified by a measurement with two identical AEL H-1498 broadband horn antennas in the anechoic chamber. The resulting gain was within 0.5 dB from the nist data at 2.45 GHz. Any error in antenna gain will affect the calibrated pwoer density and therefore, the efficiency defined by (5.3).For example, the efficiency reported for A1 at a power density of 200 μW/cm^2 (54%) would range from 48% to 60% with a gain error of $\pm$0.5 dB and the efficiency error would change linearly with gain error.

5.2.3 Results

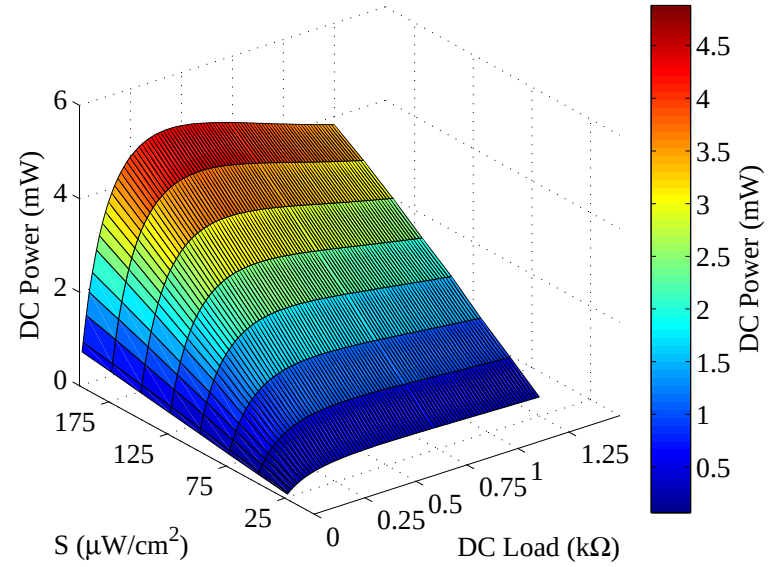
Fig. 5.14a shows measured rectified power for the optimally matched integrated rectifier antenna A1. For A1, the optimal DC load at a power density of 200 μW/cm^2 is 460 Ω, and changes by up to 30 Ω for lower power densities. The corresponding lower bounds on peak conversion efficiencies calculated from (5.3) are shown in Table 5.2.

Table 5.2: Measured optimal efficiencies for the 3 antennas

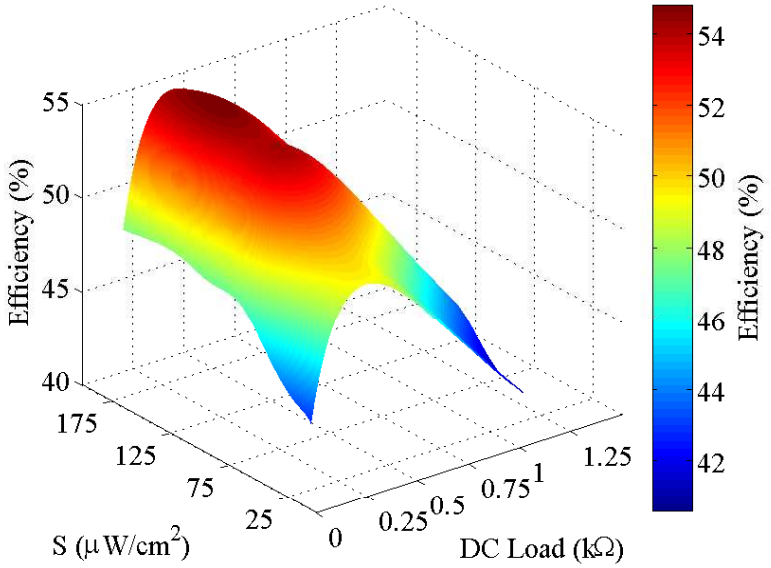
Antenna	A1	A2	A3
η(200 μW/cm^2) (%)	54.2	36.5	28.0
η(25 μW/cm^2) (%)	43.6	30.9	23.4

Fig. 5.14b shows the RF to DC conversion efficiency for the varying DC load and power levels. Notice, that the efficiency stays above 53% over the range of power densities of 75 to 200 μW/cm^2 and constant DC load of 460 Ω. The efficiency surface takes a very different shape than the DC output power surface shape; small output power deviations translates to large changes in the efficiency. This is

important in order to accurately determine the range of power densities and DC loading that the integrated rectifier antenna is suited for.



(a)



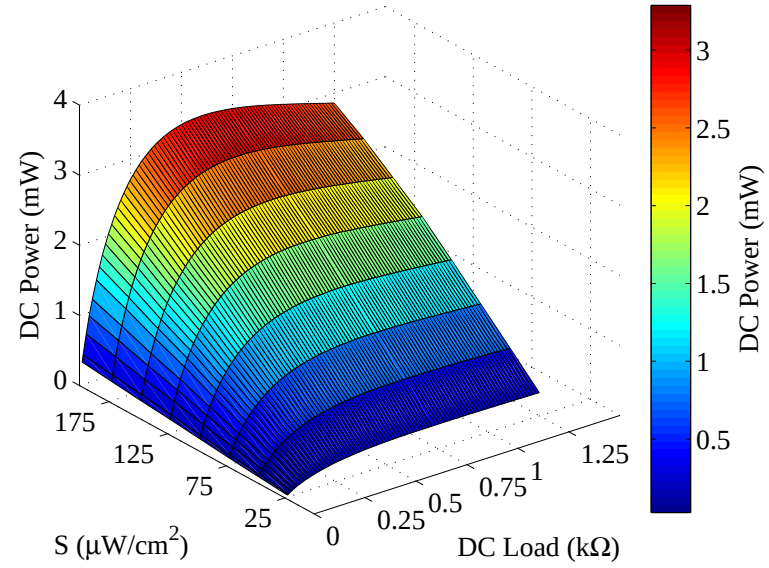
(b)

Figure 5.14: (a) Measured co-polarized rectified power for Antenna A1 at broadside for power densities 25 to 200 μW/cm^2. Every intersection of the black grid lines and black curves is a measured data point.(b) RF to DC conversion efficiency calculated from measured data in (a).

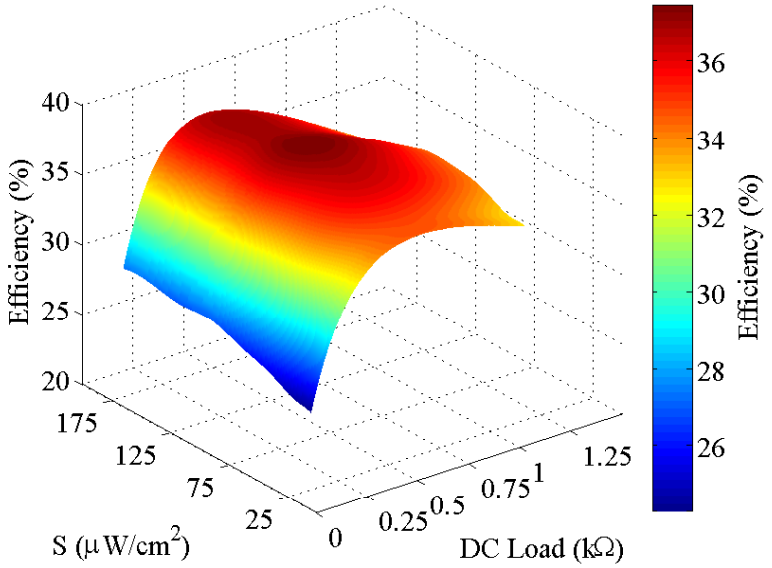
For the integrated rectifier antenna A2, the impedance looking in towards the antenna at the diode plane is $460 + j520\,\Omega$. The DC power source pull measurement at that impedance was 5.6 dBm at 10 dBm input power. Fig. 5.15 shows the measured power and efficiency. Notice that the gradient is smaller than in Fig 5.14 although, the overall efficiency is lower and the peak efficiency is at a higher DC load. The match to the diode is not as good as the in the case of the optimal A1, and part of the available power is reflected. Because some of the power is reflected, the incident power to the diode is lower. A higher DC load is needed in order to get the DC voltage up and shift the waveform to the optimal conduction angle, as explained in Section. 3.2. The broader range of high efficiency values in comparison to A1, is due to the lower incident power, which prevents the diode from reaching its breakdown voltage at higher DC loads, and hence, the second nonlinearity that induces loss is not introduced as in the case of A1. The mismatch to the diode at integrated rectifier antenna A3 is the greatest mismatch tested; the impedance measured at the diode plane was $220 - j220\,\Omega$. The measured DC power form source-pull at that impedance is 4.5 dBm. As expected, the output DC power from this rectifier antenna combination is the lowest of the ones tested (A1 to A3), and can be seen in Fig. 5.16a.

A result not expected in this test is the lower optimal DC load for this rectifier antenna integration, as can be seen in Fig 5.16. In this case, the incident power to the diode is low (high reflection), and at lower power, the voltage may not be high enough to forward bias the diode. In addition, the nonlinear behavior of the diode has an effect on the optimal DC load. In contradiction to previous results, the optimal DC load is lower than the optimal DC loads for A1 and A2. Fig. 5.17 gives insight to the unexpected shift to a lower DC load seen in Fig. 5.16.

The impedances selected for the test integrated rectifier antennas A1 to A3 were chosen according to the data presented in Fig. 5.9, where the source pull data was



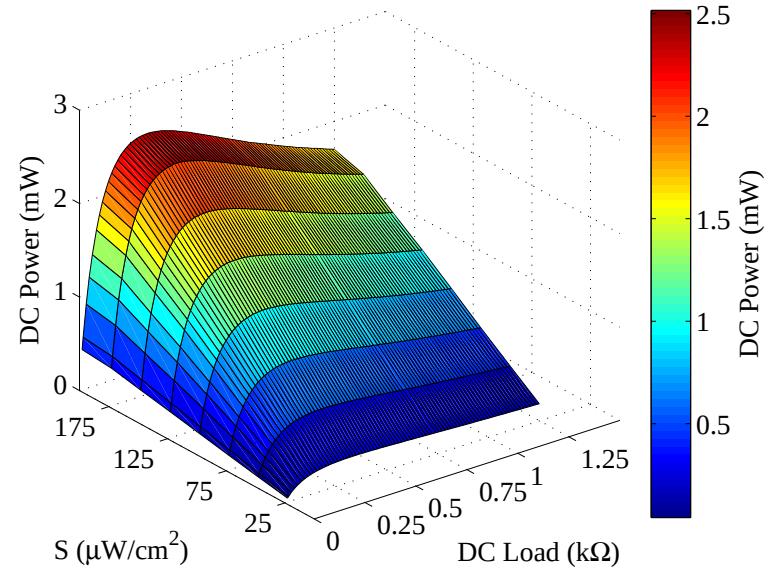
(a)



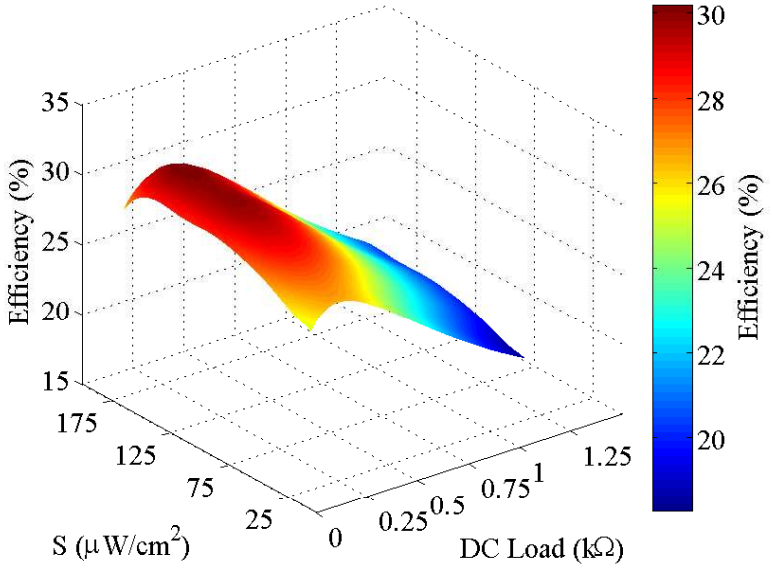
(b)

Figure 5.15: (a) (a) Measured co-polarized rectified power for Antenna A2 at broadside for power densities 25 to 200 μW/cm^2. Every intersection of the black grid lines and black curves is a measured data point.(b) RF to DC conversion efficiency calculated from measured data in (a)..

for a fixed DC load of 460 Ω. Examining Fig. 5.17 it is clear that while changing the DC load, the constant DC power contours scale in a non-linear manner. Notice the



(a)



(b)

Figure 5.16: (a) Measured co-polarized rectified power for Antenna A3 at broadside for power densities 25 to 200 μW/cm^2. Every intersection of the black grid lines and black curves is a measured data point.(b) RF to DC conversion efficiency calculated from measured data in (a).

order of powers in Fig. 5.17b where, the DC powers in order of largest to smallest are A1, A2 and A3. At the a higher DC load, the same trend of the order of DC

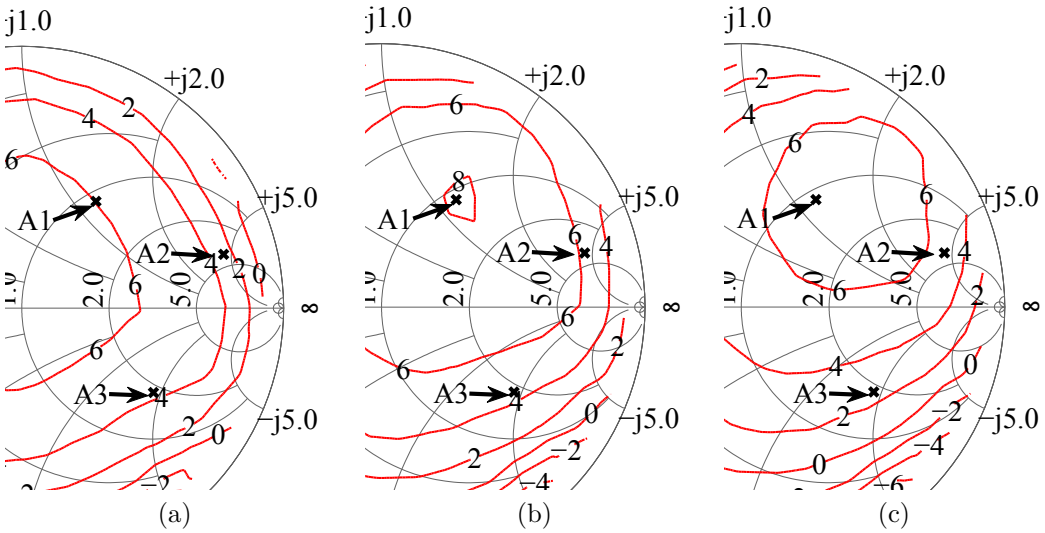


Figure 5.17: Source pull constant DC contours overlayed with the impedance of each of the test antennas A1 to A3 (a) A low DC load of 112 Ω.(b) Optimal DC load of 460 Ω. (c) High DC load of 1200 Ω. The Smith chart is normalized to 120 Ω.

powers is kept, seen in Fig. 5.17c. On the other hand, in Fig. 5.17a, the order is not kept, where the power at A1 is still the highest but, second is A3 and finally the smallest is A2. This non linear scaling with change of DC load and change of constant DC contour shapes, explain the unexpected shifts in the optimal DC load observed in Fig. 5.18.

A summary of test results for the three integrated rectifier antennas A1 to A3, at power densities 200 μW/cm^2 and 25 μW/cm^2, is shown in Fig. 5.18. The shifts in optimal loads is clearly seen at the higher power density.

These results confirm that the optimal match between the antenna and rectifier yields considerably higher efficiencies than the sub-optimal match cases. Fig. 5.19 shows the rectified output efficiencies for antennas A1 and sub-optimally matched antennas A2 and A3 at a range of power densities 25 to 200 μW/cm^2. As the impedance deviates from the optimum, the rectified power decreases significantly. The optimally complex-impedance matched integrated rectifier antenna gives the highest rectified power. Note that the optimal DC load shifts, as expected from the

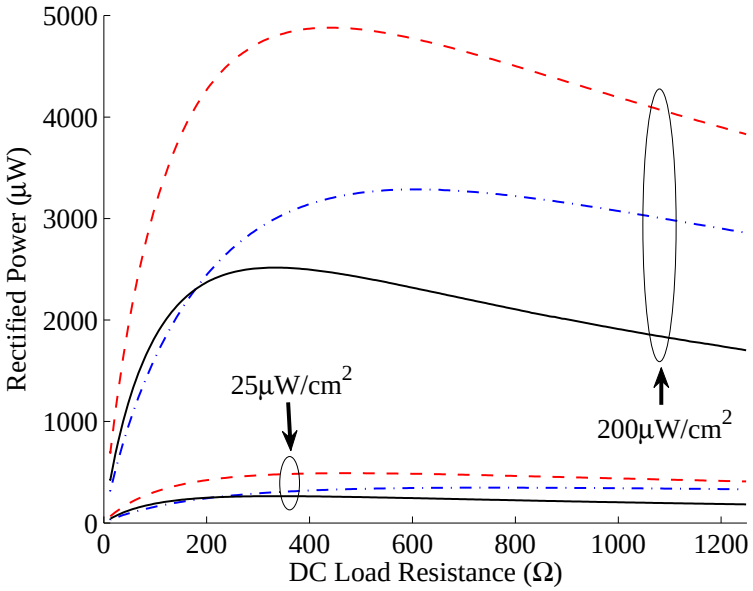
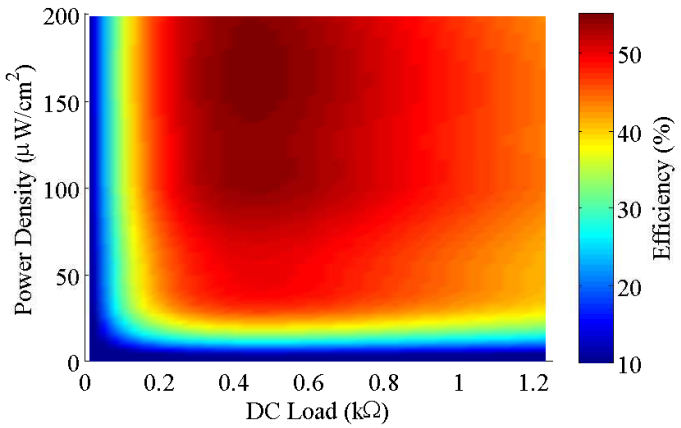


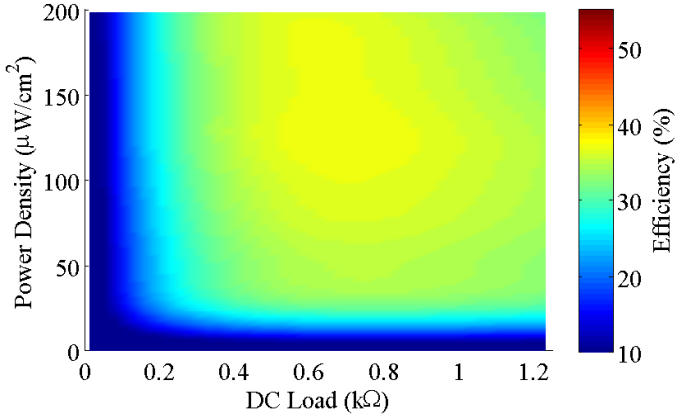
Figure 5.18: Rectifier antennas A1(Red dashed) A2(Blue dash-dot) and A3(Black solid) at power densities of 25 and 200 μW/cm^2.

source-pull measurements. For practical applications it is important to notice that the value of DC load decreases with increasing incident power, as seen in Fig. 5.20, and discussed in Section 3.2

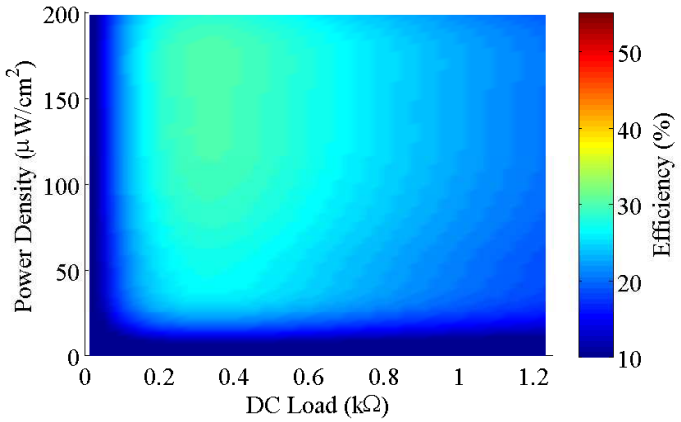
The optimal loads for each of the integrated rectifier antennas A1 to A3, at power densities 25 to 200 μW/cm^2 are shown in Fig. 5.20. The three integrated rectifier antenna optimal loads match the source pull measurement data, notice, that the load differs only by approximately 30Ω form the lowest the highest power densities in order to keep the rectifier operating at the optimum efficiency. This is useful for the DC-DC power converter design [64, 60, 61]. The range of loads that it needs to present is small and a simple lookup table [58] or a maximum power point tracking algorithm [90, 54] can be used to configure the load presented by the DC-DC converter.



(a)



(b)



(c)

Figure 5.19: Measured efficiencies for the three test integrated rectifier antennas (A1 to A3) plotted on the same efficiency scale for power densities 25 to 200 μW/cm^2 at broadside. (a) Antenna A1 (b) Antenna A2 and (c) Antenna A3.

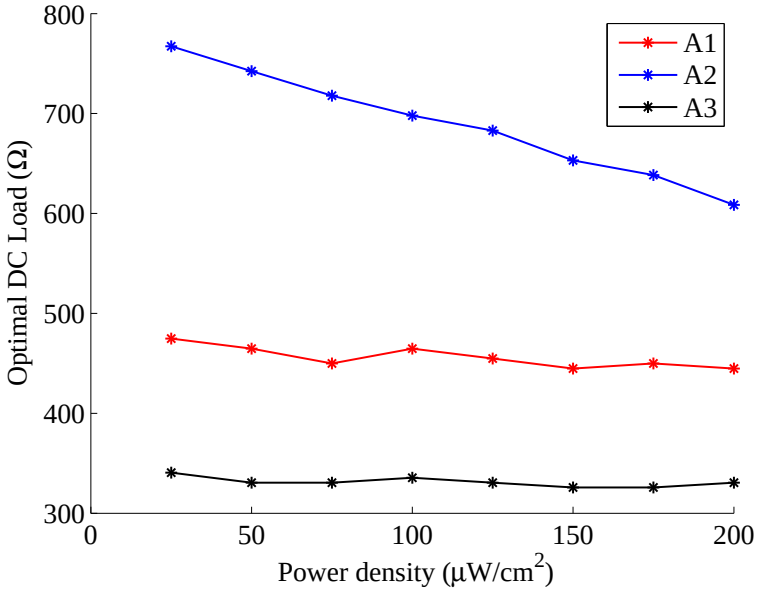


Figure 5.20: Measured integrated rectifier antenna optimal DC load sensitivity to incident RF power, for the three antennas.

5.3 Integrated Rectifier Antenna Patterns Measured at DC

5.3.1 Introduction

A wirelessly-powered sensor has an integrated rectifier antenna which receives power radiated from a transmitter in the far field, and couples it in to a rectifier. As a result of the variety of locations that sensors can be placed at, and the different orientation of the sensor relative to the power transmitter, it is important to characterize the performance of the integrated rectifier antenna from different angles and different incident power densities. DC power pattern characterization has been done by direct measurement of the DC output power at the different orientations [104, 16]. In other work, e.g.[105, 106, 107] the RF power pattern of the antenna alone is characterized which gives insight in to the performance of the integrated rectifier antenna at different angles but, neglects the dependance of the

rectifier on input power. A more accurate estimation proposed here, is to multiply the RF power pattern with the integrated rectifier antenna efficiency, obtained both from simulation and measurement at broadside for different power densities, resulting in an efficiency as a function of the input power. Simulations are done in Agilent Advanced Design System (ADS) for the rectifier and Ansoft HFSS for the antenna. The efficiency drops rapidly at lower input powers consistent with other published results [23, 58]. The nonlinearity of the rectification process can be used to explain and predict the difference between patterns of integrated rectifier antenna compared to antenna radiation pattern alone.

5.3.2 Rectifier Antenna Efficiency

In Section, all further references to efficiency of an integrated rectifier antenna will be according to the definition in (5.3). Measurement results of a 1.96 GHz patch integrated rectifier antenna are presented in Fig. 5.21, These results are compared with separate simulations for the rectifying circuit and the antenna done in ADS and HFSS, respectively. For this plot, the efficiency for each input power to the rectifier is multiplied by the antenna efficiency in order to get the total rectifier-antenna efficiency.

5.3.3 RF & DC Antenna Power Patterns

Before the antenna is connected to the nonlinear rectifier, its power pattern can be characterized with a fixed matched load (power meter). For this work an antenna with identical geometry was fabricated and matched to 50Ω. The E & H patterns of the antenna were measured in an anechoic chamber. As seen in Fig 5.22 there is very good agrement between HFSS simulations and measurements for wide angles off broadside. The difference in traces at 90° off broadside are due to the mount for the antenna and power sensor. At broadside all metal of the mount is behind the

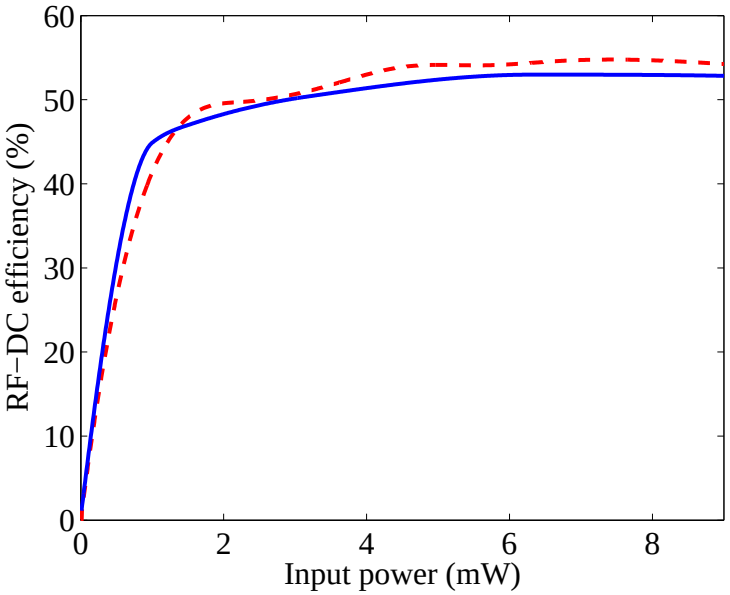
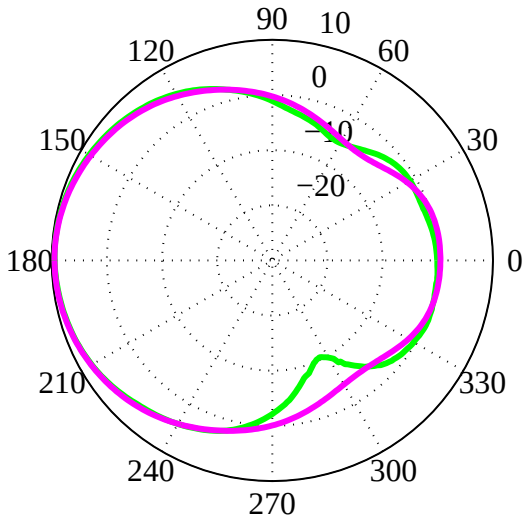


Figure 5.21: Measured integrated rectifier antenna efficiency (dashed red). ADS diode rectifier simulation efficiency multiplied by the HFSS simulated antenna radiation efficiency (blue).

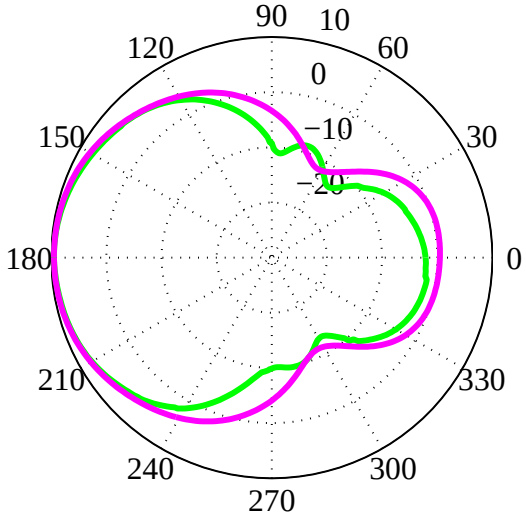
ground plane of the antenna, thus as the antenna rotates more metal is exposed and can cause interference.

Once the antenna RF pattern is characterized and the rectifier efficiency for the power range of interest is obtained from measurement or calculation, the DC pattern can be constructed. Note that, it is important to obtain efficiencies at much lower power than expected at broadside for each power density. The power supplied to the rectifier from the antenna could drop significantly as the orientation of the antenna and the source change (this would vary for different antennas) and the correct efficiency for that power must be used for the DC power pattern. An example comparison is showed in Fig 5.23 where the normalized RF antenna pattern is shown together with predicted and measured rectifier-antenna DC patterns.

It is interesting that the DC pattern is approximately 3dB below the RF power



(a)



(b)

Figure 5.22: (a) E-plane normalized power pattern (b) H-plane normalized power pattern. For both (a) and (b) the green trace is measured pattern for a 50Ω matched patch and the magenta is HFSS simulation.

pattern. This is excellent agreement to maximum measured efficiency at broadside of 54% of this integrated rectifier antenna at power density of $200\mu W/cm^2$. As can be seen from Fig 5.24 the prediction of DC power patterns can be scaled to other

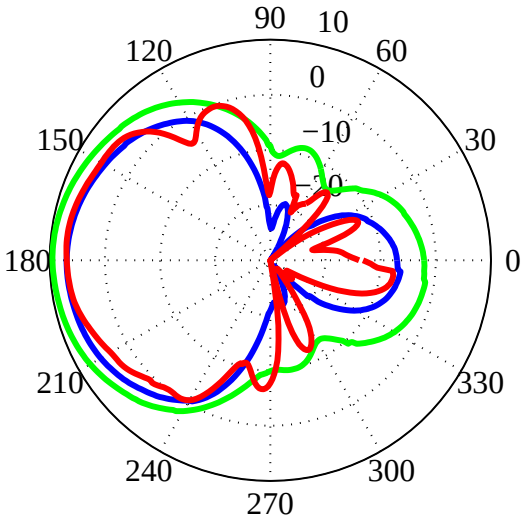
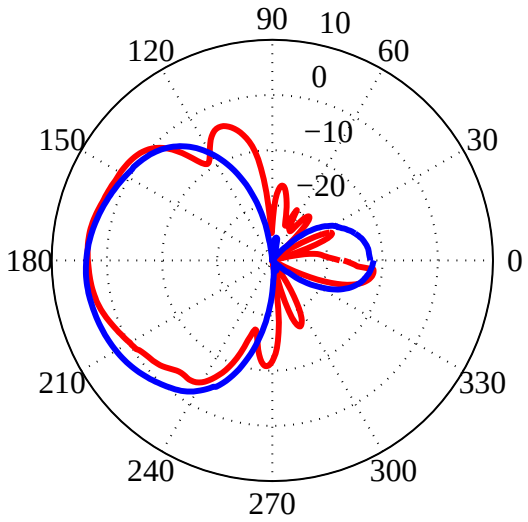


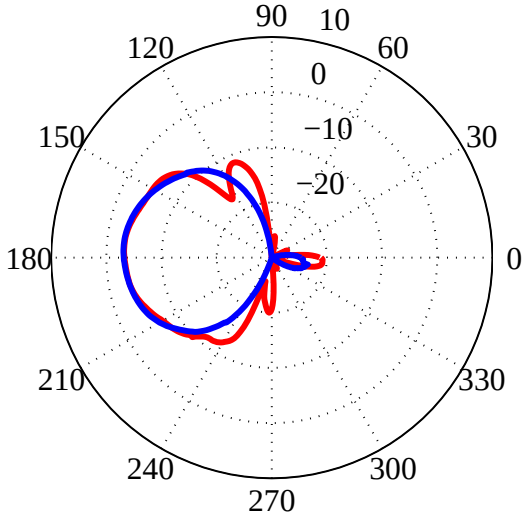
Figure 5.23: Normalized measured 50Ω patch antenna pattern (green). Predicted DC power pattern for a power density of 200 μW/cm^2 (blue). Measured rectifier-antenna pattern at power density of 200 μW/cm^2 (red).

power densities. As mentioned before, there are some variations at angles that are approximately 90° off broadside due to mounting.

The DC performance of a integrated rectifier antenna is a non-linear function of not only θ and ϕ but also of the efficiency η. It is clear from the measurement that characterizing a integrated rectifier antenna with its RF power pattern alone does not accurately predict performance. The method presented in this section integrates the rectification efficiency in to pattern calculations and is shown to be an accurate predictor of the integrated rectifier antenna performance. The omni-directional characterization is important for determining the power budget of a wireless powered sensor.



(a)



(b)

Figure 5.24: DC power pattern for incident power densities of $100\mu W/cm^2$ (a) and $25\mu W/cm^2$ (b). Blue: Predicted DC power pattern. Red: Measured integrated rectifier-antenna DC power pattern.

5.4 Summary

In this chapter, the integration between rectifiers and antennas for wireless powering is addressed and a method developed that results in maximized efficiency. The

method is demonstrated in simulation and experiment on the example of a patch antenna and Schottky-diode single-ended rectifier. It is shown that the order of steps taken in rectifier-antenna integration is critical, and should follow as discussed below:

(1) Characterize rectifying device (diode in this case) by harmonic balance simulations or modified source-pull measurements to determine the optimal device complex impedance range for maximizing rectification efficiency over a given range of incident RF power levels. This modeling results in both RF and DC impedances for efficient rectification over a range of input powers.

(2) Use the obtained RF impedance as a starting point for antenna design, in addition to other antenna-specific requirements, such as shape, size, mounting environment, etc. The antenna design for a complex input impedance might require an additional non-50 Ω matching network.

(3) Design DC collection circuit for a given antenna and rectifier combination to maximize DC-RF isolation.

(4) Design calibration standards to validate the passive part of the integrated rectifier-antenna. After validation, remove validation and calibration circuitry.

(5) Characterize the rectifier-antenna. The output of the characterization is a DC Thevenin equivalent representation of the rectifier-antenna which can be used to determine efficiency and to design the power management circuit for the wirelessly powered sensor platform described in Chapter. 2.

The characterization in step 5 above required development of a free-space calibration procedure, described in this chapter. The RF-DC conversion efficiency of an integrated rectifier and antenna is not a straightforward parameter to measure, and several efficiency definitions are overviewed. In this chapter, a conservative

definition which determines the lower bound on efficiency and is straightforward to measure in a standardized way, is defined and discussed.

The contributions from this chapter are reported in the following publications: [108, 84, 109]

Chapter 6

Dual Polarization Integrated Rectifier Antenna

A consensus means that everyone agrees to say collectively what no one believes individually.

—Abba Eban

Contents

6.1 Introduction

The incident powering wave will in general arrive to the rectenna at different polarizations, depending on the radiating source and propagation environment [110, 111, 112]. Since the orientation of the integrated rectifier antenna is not always known, the dependency on alignment of the source to the receiver should ideally be eliminated. In the case of a linearly polarized source, a linearly polarized receiver antenna will receive a power

$$P_{Rec} = \eta P_{inc} PLF = \eta P_{inc} |\cos \psi_p|^2, \tag{6.1}$$

where, the polarization loss vector (PLF) takes in to account the polarization misalignment w.r.t. the transmit antenna [113] as described in Fig. 6.1 . If a linearly polarized source is used, a circularly polarized receiving antenna will receive 3 dB for a line of sight link. In a multipath propagation environment for a verticaly polarized antenna the electric field at the receiving antenna will on average contain equal power in the two orthogonal polarizations. therefore, if a

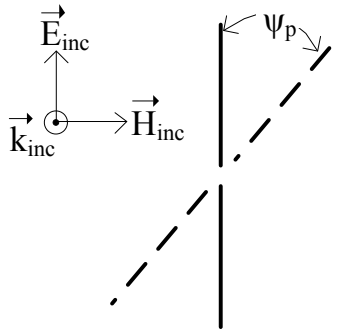


Figure 6.1: PLF for transmitting and receiving linear wire antennas .

dual orthogonal linear polarization antenna is used all of the power of the wave will be received. This chapter goes through the design considerations, as well as

experimental data, in order to be able to rectify RF power regardless of rotation angle of the integrated rectifier antenna.

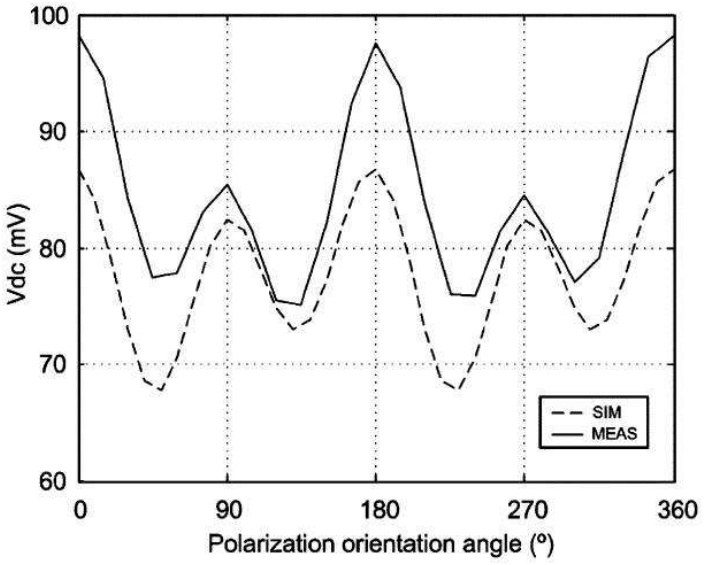
6.1.1 Background

The need for a dual-polarized receiving element is recognized by many of the integrated rectifier antenna designs in the literature. In [54, 27, 114] dual linear square patches are used with a rectifier for each of the polarizations where the DC output of the rectifiers are combined and share a single node. Examples of DC output variations of different antenna orientations is shown in Fig. 6.2. Georgiadis's [114] DC output voltage is shown in Fig. 6.2a, and Paing's [54] integrated rectifier antenna DC output power is shown in Fig. 6.2b.

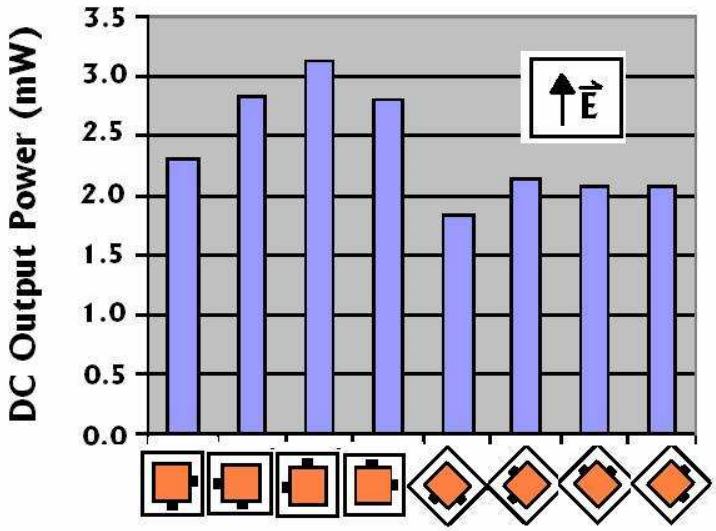
In [115] a circular polarization patch is used, in this case, one port is terminated in 50 Ω while the other is used for power reception, so the rectifier antenna needs to be configured according to the incoming wave. A crossed dipole is used in [116], where the DC output of the two rectifiers are connected to the same node and DC load. The rest of the chapter will concentrate on simulations and experiments showing the advantages of isolating the DC path for each of the polarizations and feeding two different DC-DC converters in order to provide the optimal conditions to each of the rectifiers.

6.1.2 This work

The methodology developed in the previous chapters is used to design an integrated patch rectifier antenna at a frequency of 2.45 GHz. In contrast to the design in Chapter 5, the size and volume of the antenna are taken into account, and a stack of substrates is used with via connections between the two, eliminating the SMA connectors used in the 1.96 GHz design. The substrate stack seen in Fig. 6.3 consists of 30 mil thick Rogers 5880 with $\epsilon_r = 2.2$ [117] for the patch antenna



(a)



(b)

Figure 6.2: Dc output voltage variation for different integrated rectifier antenna orientation angles relative to the input signal polarization($f = 2.45\,\mathrm{GHz}, \mathrm{R_L} = 6.2\,\mathrm{k\Omega}$).(a). Measured histogram of DC power levels for an incident power level of $170\,\mu\mathrm{W/cm^2}$ for different orientations of the dual-polarized integrated rectifier antenna element, corresponding to different incident polarizations. The incident RF power is linearly polarized. (b).

element substrate and 30 mil thick Rogers 4350b with $\epsilon_r = 3.66$ [55] for the rectifier substrate, with a shared ground plane. The Rogers 5880 was chosen for the antenna

because of its low loss tangent of 0.0004. The low loss tangent results in high radiation efficiency (95% simulated in HFSS). The rectifier circuit was built on Rogers 4350*b*, which is rigid and easy to work with, and has a dielectric constant of $\epsilon_r = 3.66$ which reduces the circuitry dimensions in comparison to free space or Rogers 5880.

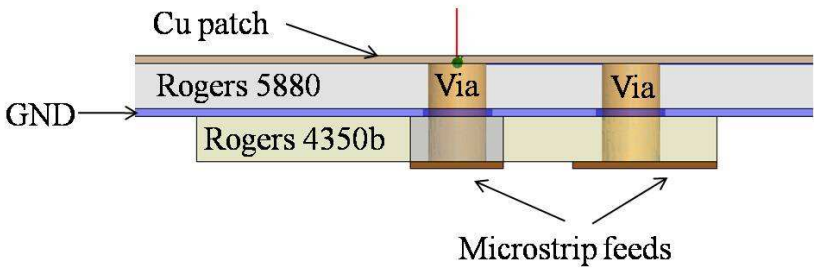


Figure 6.3: Layer description of the substrate and copper stack-up used for a dual-polarized integrated rectifier antenna at 2.45 GHz.

The simulations for this design were done in two separated parts, the antenna feed and part of the microstrip line going to the rectifier, were simulated in a full 3D simulator (HFSS), and the matching circuit and nonlinear device (diode), were simulated in Agilent ADS using harmonic balance techniques. The point where the circuit is split for the two simulations is at the 50-Ω line between the antenna feed via and the rectifier 50-Ω microstrip input line. At that point, there are no geometry transitions, thus splitting the circuit at that point will have limited effects on performance and simulations can be cascaded.

6.2 Dual Linear Polarization Patch Integrated Rectifier Antenna

A circuit providing short harmonic terminations to the even harmonics and the 3rd and 5th harmonics was designed on 30 mil thick Rogers 4350*b* $\epsilon_r = 3.66$ [55]. In order to minimize the total area of the circuit, the $\lambda/4$ DC feed line @ the

fundamental frequency, is meandered, resulting in a total size of the dual rectifier circuitry of 20 mm × 20 mm.

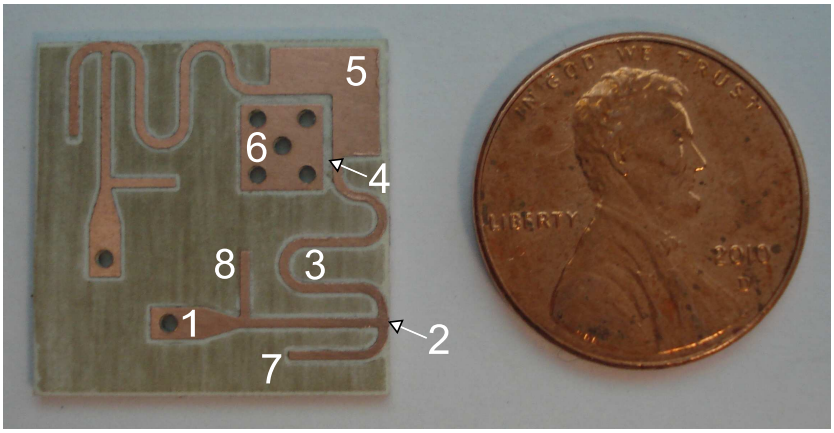


Figure 6.4: Photograph of the dual rectifier circuit fabricated on Rogers 4350*b*. (1) via to antenna feed, (2) diode location, (3) quarter-wave long DC feed line. The line is meandered in order to make the overall dimensions of the circuit smaller (4), Resonant capacitor location, (5) DC output, (6) GND, (7) 3rd harmonic stub, (8) 5th harmonic stub. (6) and (5) are common to both rectifiers on the circuit.

The Smith chart in Fig. 6.5 shows S_{11} of one of the rectifier circuit from Fig. 6.4 from 2.45 GHz to 12.25 GHz. Port 1 in the simulation is the diode plane (2 in Fig. 6.4) and the other ports are terminated in 50 Ω. The terminations at the other ports do not effect the harmonic impedances seen form port 1. An identical rectifier circuit was fabricated with a TRL line connected to the diode plane as seen in Fig. 6.10a. The S_{11} is measured from 2.45 GHz to 12.5 GHz so it includes the first five harmonics. The results are plotted in Fig. 6.6. The harmonic impedances are located at the low impedance region of the Smith chart, the 2nd, 3rd and 4th harmonic impedances are capacitive while the 5th is inductive. The diode package has some parasitic inductance (0.7 nH) according to the manufacturer, the inductance is distributed between the two diode package leads [56]. Including the inductance with the measured data shifts the impedances as seen in Fig. 6.7. The harmonic terminations are wanted at the diode junction it self, as so the package parasitics must be included in the harmonic termination design. This is in contrast

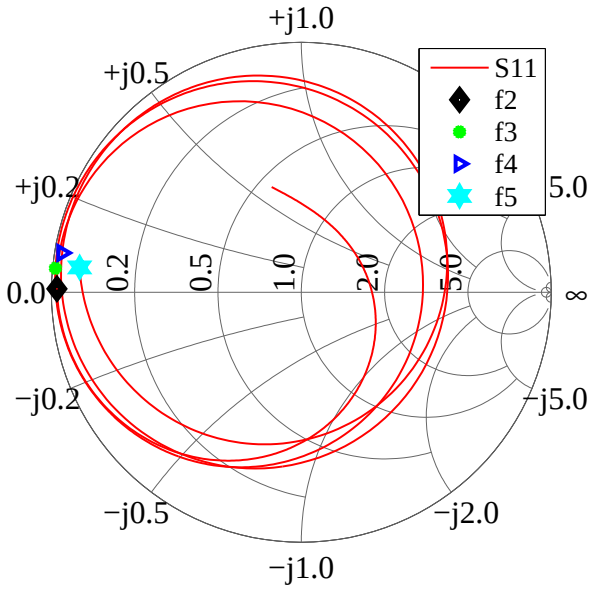


Figure 6.5: Simulated S_{11} from 1 GHz to 12.25 GHz of a single rectifier circuit while the three ports are terminated with 50 Ω and port 1 is at the diode plane. The diamond markers are at the 2nd to 5th harmonics of the fundamental. The scattering parameters and the Smith chart is referenced to 50 Ω.

to the fundamental frequency impedance that is simulated and measured to a reference plane at the package of the diode.

As seen in Fig. 6.7 the package inductance shifts the harmonic impedances, the higher the harmonic the larger the shift, as expected. The 5th harmonic is shifted away from a short and is inductive ($5.7 + j25\,\Omega$), since the power generated by the nonlinearity decreases at the higher harmonics, the weight of each harmonic termination decreases as well. The accuracy of the harmonic terminations at the 2nd and 3rd harmonics are much more significant to the overall RF-to-DC conversion efficiency than at 5th and 6th harmonics. In simulation, the difference in efficiencies between a perfect short and $5.7 + j25\,\Omega$ termination is 0.02 %, hence the design is not modified.

In order to find the optimal feed impedance to the rectifier, an ADS harmonic balance source pull simulation is performed using the manufacturer diode model

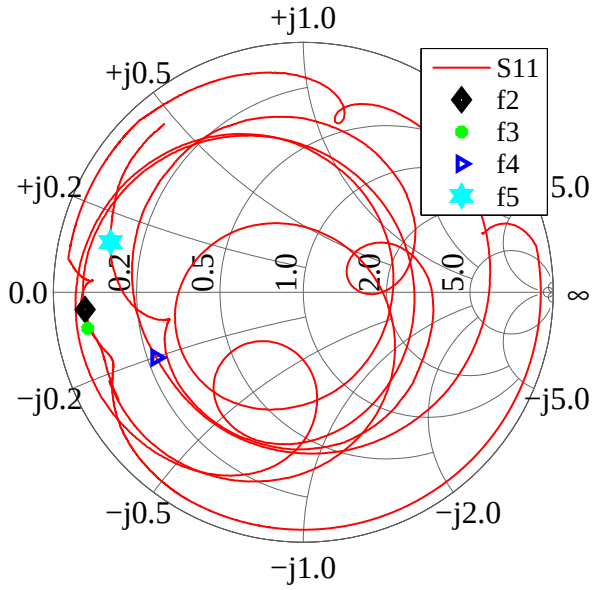


Figure 6.6: Measured S_{11} from 2.45 GHz to 12.5 GHz of a single rectifier circuit while port 1 is at the diode plane port 2 is connected to the antenna feed and port 3 (The DC port) is open. The diamond markers are at the 2nd to 5th harmonics of the fundamental. The scattering parameters and the Smith chart is referenced to 50 Ω.

for Skyworks SMS-7630-79 [56] and the rectifier layout. The input of the layout in simulation is the wide side of the microstrip tapered line (1 in Fig. 6.4). The characteristic impedance at that point is 50 Ω ($W = 1.66$ mm on 30 mil thick Rogers 4350b). Additional length or other matching circuitry will be added (if needed) in a later point of the design to match to an antenna feed point impedance. The harmonic balance simulations have been carried out at input powers varying from 0 dBm to 10 dBm, while keeping the DC load constant at 360 Ω. The input impedance of $16.9 + j5.8$ Ω is found to be the optimal value for input power of 10 dBm, as seen in Fig. 6.8. The efficiency of the rectifier is above 50 % for the whole power span, while keeping input match and DC load constant. Above 10 dBm which is the maximum power expected, it drops rapidly. From Section 3.2 it is known that the efficiency slope drops rapidly and, the diode could be damaged at higher powers if breakdown voltage of the diode is reached. The efficiency is

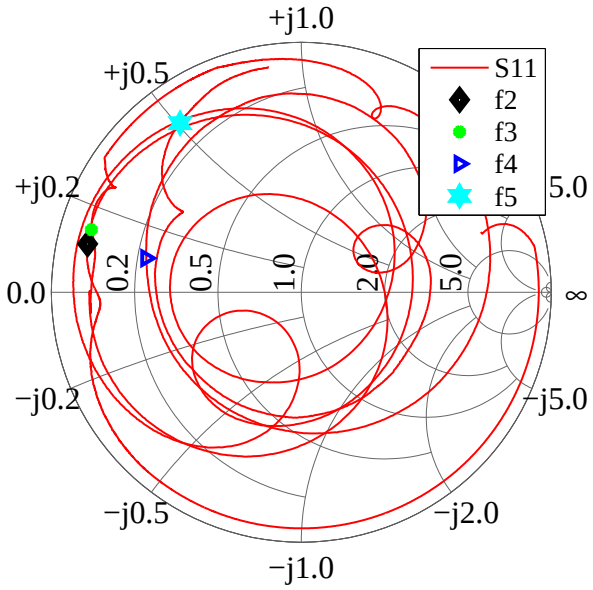


Figure 6.7: Measured S_{11} including package inductance from 2.45 GHz to 12.5 GHz of a single rectifier circuit while port 1 is at the diode plane port 2 is connected to the antenna feed and port 3 (The DC port) is open. The diamond markers are at the 2nd to 5th harmonics of the fundamental. The scattering parameters and the Smith chart is referenced to 50 Ω.

maximized for the maximum expected power of the design and drops gradually for a decrease in power.

6.2.1 Single DC Load

The optimal simulated input impedance of the rectifier circuit is $16.9 + j5.8\,\Omega$ as seen in Fig. 6.8. Fig. 6.9 shows the simulated antenna input impedance for a square patch where the feed point is varies from 2 mm to 20 mm away from the patch center. The rectifier input impedance is directly on the trace seen in Fig. 6.9, between the, 3 mm and 4 mm feed points. A fine sweep of points between those antenna feed points, found 3.6 mm to match the rectifier feed impedance (the impedance reference point for both the rectifier and the antenna feed are from the connecting port looking in to the component, hence, no conjugation is needed for the match). Verification of the antenna input impedance is done by measurement,

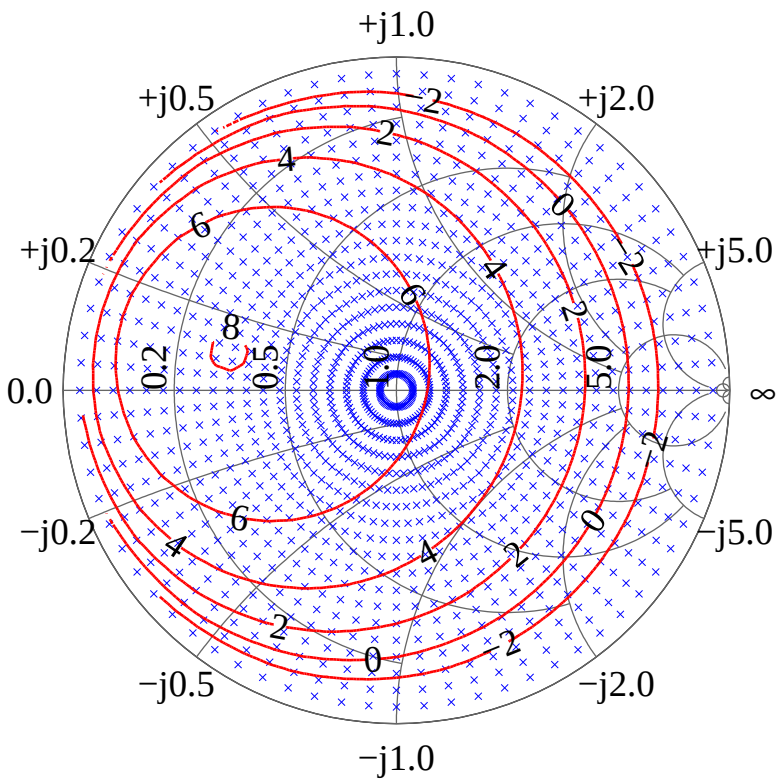


Figure 6.8: Simulated source-pull contours of constant DC power (in red) where the power is given in dBm. The input power to the rectifier is 10 dBm. The characteristic impedance of the chart is 50 Ω and the simulated tuner impedances are shown by blue x's.

with a TRL calibration, as seen in Fig. 6.10a. Simulation and measurement show excellent agreement, with $|\Gamma| < 0.05$ between the two values.

Since the rectifier and patch antenna input impedances match, no additional line or matching circuit is needed. Any addition of circuitry would increase the insertion loss between the antenna feed and diode, which would add to the degradation of overall efficiency. After verification of the impedances, the TRL trace is removed and a rectifier is connected to the antenna. The integrated rectifier antenna is placed in an anechoic chamber and tested at power densities of 25 to 200 μW/cm^2, as described in detail in Section. 5.2.

The integrated rectifier antenna was tested for both vertical and horizontal

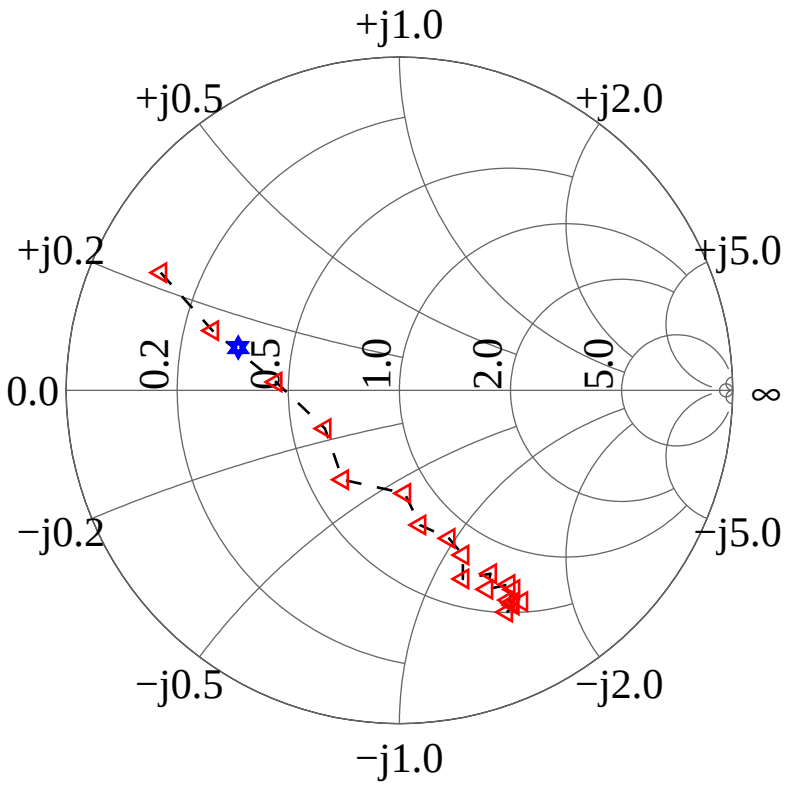
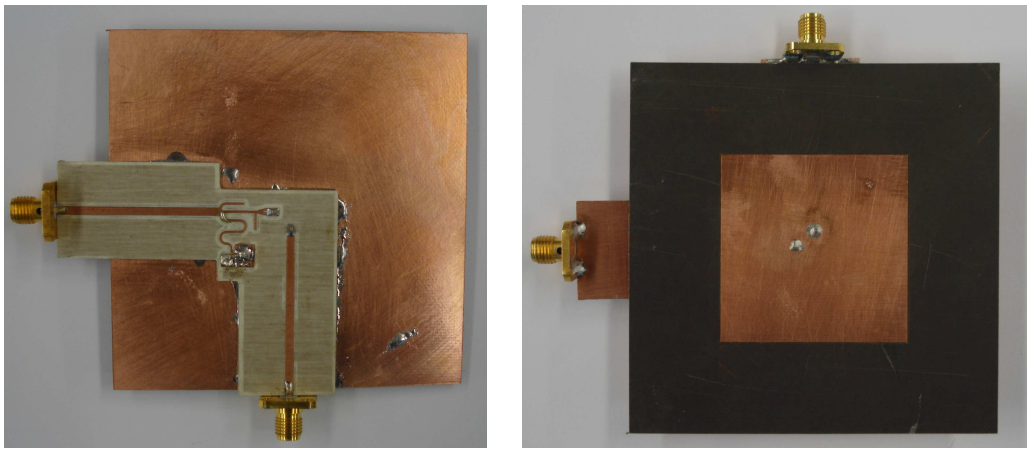


Figure 6.9: Input impedance at 2.45 GHz of a square patch antenna on a Rogers 5880 substrate, the patch size is 40.3×40.3 . The red triangles are simulated points moving the feed away from the center of the patch from 2 mm to 20 mm at 1 mm intervals, The blue star is a measured impedance. The measurement was done using TRL calibration at 3.6 mm bringing the reference plane to the antenna feed.

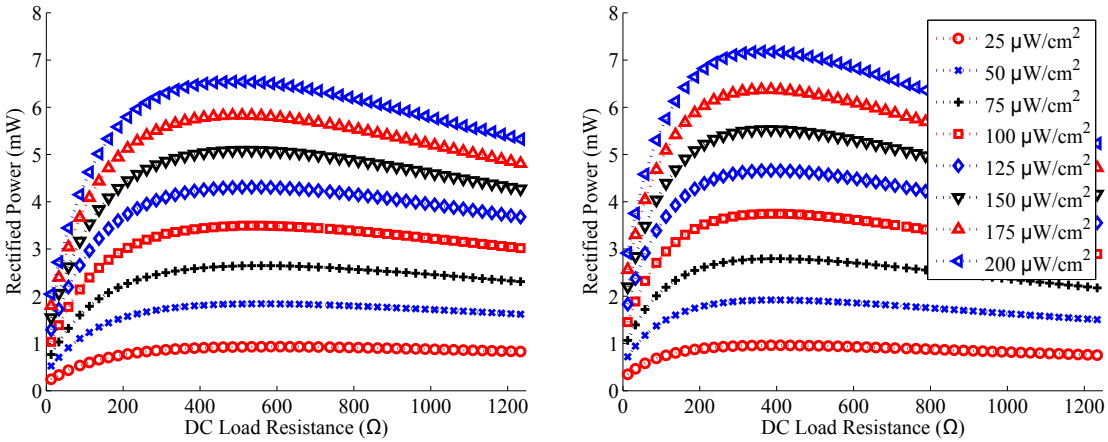
incident wave polarizations. The linear-polarized transmitting horn (AEL H-1498 broadband horn) was aligned with the edge of the patch for the first test (denoted as pol1), and then rotated by 90° to align it with the orthogonal edge (denoted as pol2). Fig. 6.11 are the measured power density sweeps versus DC load. Notice that the two polarizations have very close but not identical curves, the peak power of pol1 is 6538 μW Fig. 6.11a and the peak power of pol2 Fig. 6.11b is 7180 μW. These results are promising in terms of peak efficiency (57%) for these low power levels. However, they show sensitivity to polarization which was not expected.

Since the goal is to have a integrated antenna that has no output power or efficiency dependency on the rotation angle, measurements of the DC power as the



(a) (b)

Figure 6.10: (a) Photograph of the ground plane side of a patch antenna with TRL calibration traces up to the via feed point (vertical trace) and an additional trace up to the diode plane of the rectifier loaded with the antenna (horizontal trace). Photograph of the front side of the patch used for impedance verification (b).



(a) (b)

Figure 6.11: Measured rectified power for eight incident power density levels versus DC load for pol1 (a) and pol2 (b) co-polarized with the linear-polarized transmitting antenna.

antenna is rotated are conducted. An estimation of DC output power is based on the power versus load sweeps conducted under the two polarization conditions, for a given constant load. The data from Fig. 6.11a is converted into a lookup table, where for each input power and load, the result is a DC power. The input power is

estimated from the power density multiplied by the geometric area of the antenna and the $\cos^2\psi$ off the alignment. The same lookup table is constructed from pol2 data. Fig. 6.12 shows the values of the power estimated for each polarization, as

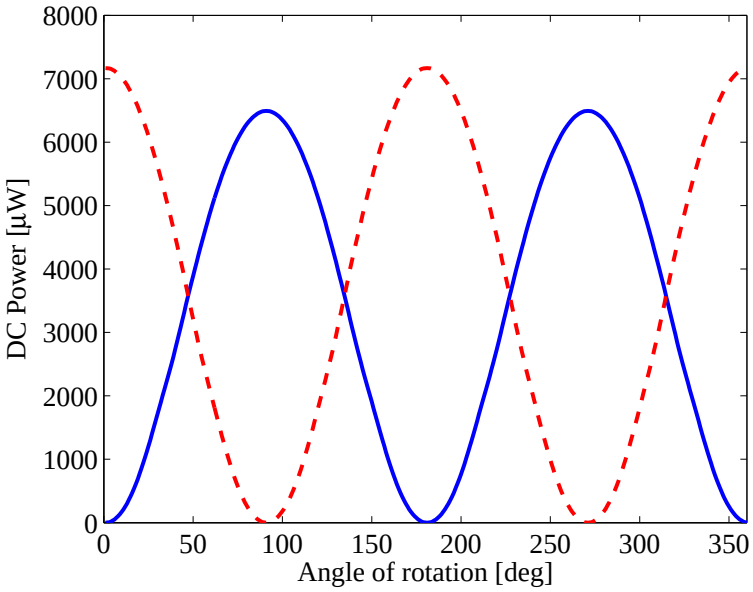


Figure 6.12: Estimated power contribution from each polarization on a 400Ω load. Blue solid is pol1 and dashed red is pol2.

the integrated rectifier antenna is rotated 360°. Notice that the power follows the $\cos^2\psi$ function as expected, with peaks at the co-polarized angles, and minima, very close to zero, at the cross-polarization angles [118]. Since the two diodes are connected through the bias lines to the same node, a measurement of these powers cannot be conducted separately. The total measured power is the addition of the contribution from both polarizations. Fig. 6.13 shows the addition of the powers from the two polarizations from Fig. 6.12 and the measured power on a 400 Ω load at a power density of 200 μW/cm^2. Examining Fig. 6.13, it is obvious that the two polarization are not independent. The estimated trace and the measured trace show same range of DC powers but the trends of peaks and minima are not aligned. A closer look at the configuration of integration of the two rectifiers reveals two problems: (1) the two rectifiers share the same DC load Fig. 6.14, and (2) the feed

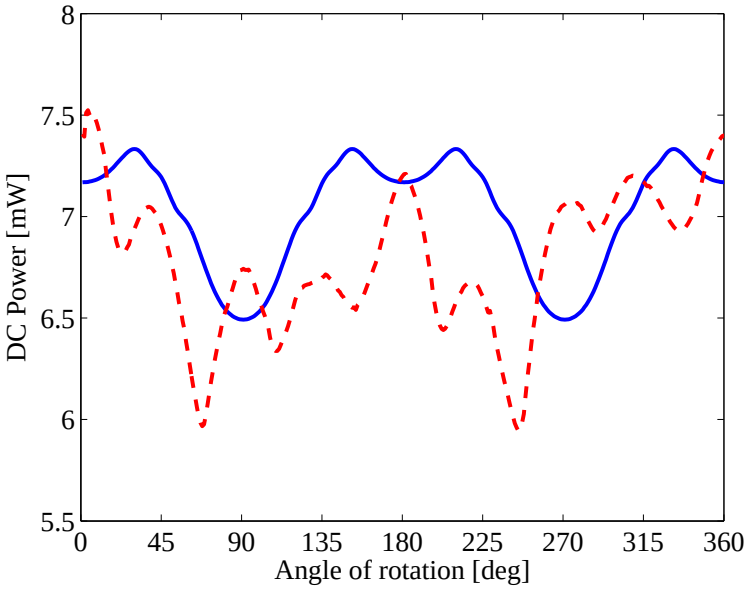


Figure 6.13: Blue is total power of pol1 and pol2 estimation and red is the measured power to a 400 Ω load at a power density of 200 μW/cm^2.

point of the antenna is close to the center of the patch.

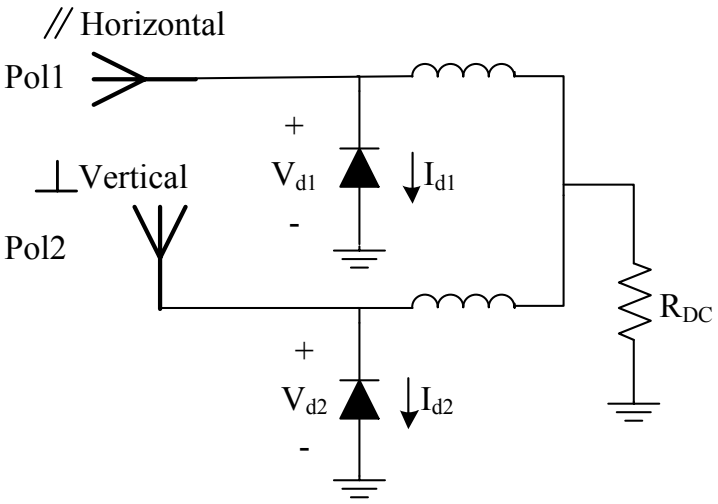


Figure 6.14: Circuit description of a integrated patch antenna rectifier with a common DC load for both polarizations.

The repeatability problem with this design is seen in the differences of powers

between pol1 and pol2, which is a result of providing slightly different input impedances to the rectifiers. The change in the antenna input impedance for a given displacement of the feed point, closer to the center the patch, is greater than the change in impedance for the same displacement close to the edge of the patch, as seen in Fig. 6.9. In the Smith chart, the feed point impedances (red markers) are for feeds separated by 1 mm, and the impedances are much closer to each other as the probe approaches the radiating edge of the patch [119]. This leads to a design with an antenna feed closer to the radiating edge of the patch. Small fabrication tolerances will have less effect on the input impedance, and the two rectifiers will be provided with input matches that are closer to each other than in the previous case.

Having the two rectifiers share the same DC load forces the same DC voltage on both diodes. Section 3.2, discusses how the DC voltage offset of the incident voltage on the diode and the control of conduction angle impact the DC power output and efficiency. A harmonic balance simulation in Agilent ADS can be used to examine the effects of combining the DC outputs of two rectifiers in the same DC load. The schematic in Fig. 6.15 is the circuit used in the simulation. The variable power splitter between the two branches of the circuit simulates the polarization misalignment and potential for power differences between the branches of the circuit. An even split represents a $\psi_p = 45°$, where the power received by both polarizations is equal.

Fig. 6.16 shows the resulting waveforms when the power splitter is set to an even split, i.e. the integrated rectifier antenna is oriented at an angle of 45° to the linear polarized powering antenna. As expected, the voltages and currents are identical for both branches of the circuit and behave as expected from Section 3.2. As the rotation angle moves away from 45° toward 90°, the power difference between the two ports increases [120]. To simulate the effect of polarization mismatch

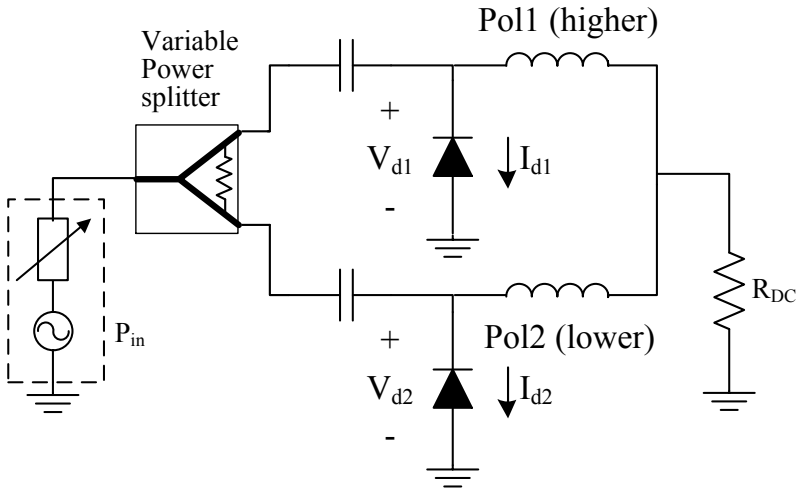


Figure 6.15: Circuit schematic used in the harmonic balance simulation to simulate the time domain waveforms on the diodes in a dual polarization rectifier antenna with a single DC load. The generator simulates the dual polarized antenna and the variable power splitter simulates the polarization power split. The Pol1 branch is used to simulate the rectifier receiving the higher power and Pol2 the lower power.

the power split between branches pol1, and pol2 were set to be $P_2 = P_1 - 3\,\mathrm{dB}$. Fig. 6.17 shows the voltage and current across the diodes in both rectifiers. Since the DC component of both voltage waveforms is equal, the lower powered rectifier diode is not in deep forward bias, which translates to a small current peak and low RF-to-DC conversion efficiency. Notice that the current waveforms of the two diodes track well, except for the high current peak during the forward bias period. This translates into approximately equal power dissipation, while the output DC power is much lower for the pol2 branch. The DC component of the voltage is determined primarily by the DC current through the load produced from the pol1 branch of the circuit. The amplitude swing on the pol2 voltage waveform must be higher than the DC voltage value, in order to forward bias the diode for any part of the period. If conditions are such that the power difference between branches is very large and produces a high DC voltage from the co-polarized branch, while the

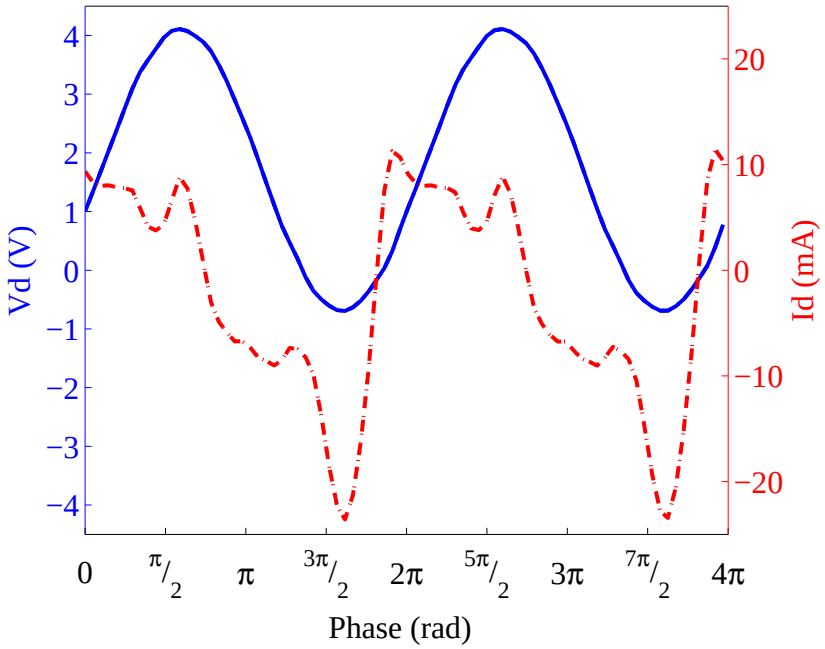


Figure 6.16: Voltage (blue solid) and current (red dashed) waveforms across the diodes. The voltage and current waveforms are identical on both diodes, for $\psi_p = 45°$, i.e. pol1 = pol2.

amplitude of the other branch is reduced, the diode will not be forward biased at all. This large mismatch is simulated by changing the power splitter in Fig. 6.15 to $P_2 = P_1 - 10\,\text{dB}$, with results plotted in Fig. 6.18. In the case of a 10 dB input power difference between the two rectifiers, the pol2 branch is dissipating power and not contributing to the RF-to-DC conversion. In Fig. 6.18 it can be seen that the pol1 branch has the waveforms of a reduced conduction angle rectifier, a sinusoid voltage that passes the forward bias voltage for a short period of time and a current that peaks during that forward bias period. The voltage waveform on the second branch, is a sinusoid with the same DC value as the first branch, but its amplitude does not reach the forward bias voltage of the diode at any point during the period. The current is a sinusoid as well and is phase shifted in relation to the voltage, which is a result of the capacitive diode impedance.

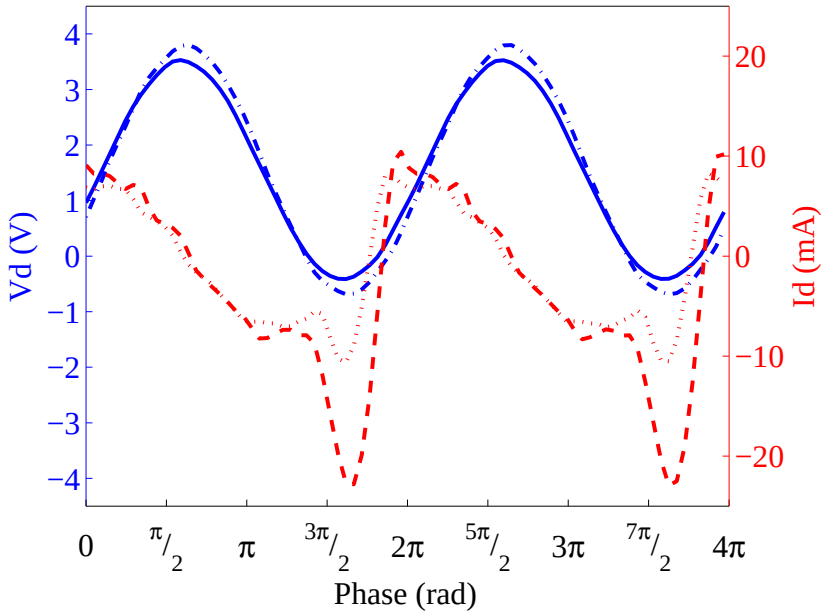


Figure 6.17: Simulated pol1 voltage (dashed blue) and current (red dashed), pol2 voltage (solid blue) and current (dotted red) waveforms across the diodes. The waveforms of pol1 are very similar to the expected reduced conduction angle rectifier waveform, indicating good RF-to-DC conversion efficiency through that branch of the circuit. On the other hand, the waveforms of Pol2 show the diode is not deep enough into forward bias, and the resulting RF-to-DC conversion efficiency is reduced.

6.2.2 Split DC Load

In an attempt to solve the problems of the previous integrated dual-polarization rectifier antenna, a new design approach is taken, where: (a) the antenna feed is moved toward the edge of the patch (less sensitivity to fabrication tolerances), and (b) isolating the DC nodes corresponding to the two polarizations by splitting the DC path to two separated DC loads. The same rectifier that was used in the previous section, Section. 6.2, with an input impedance of $16.4 + j5.9\,\Omega$, can be matched to a point further towards the edge of the patch. Examining the input impedance trace of the patch in Fig. 6.9, and adding a length of $50\,\Omega$ line (12.5 mm or 62° at 2.45 GHz), transforms the impedance along a constant VSWR circle to $42 + j49\,\Omega$. This impedance matches with a feed point 9 mm away from the center

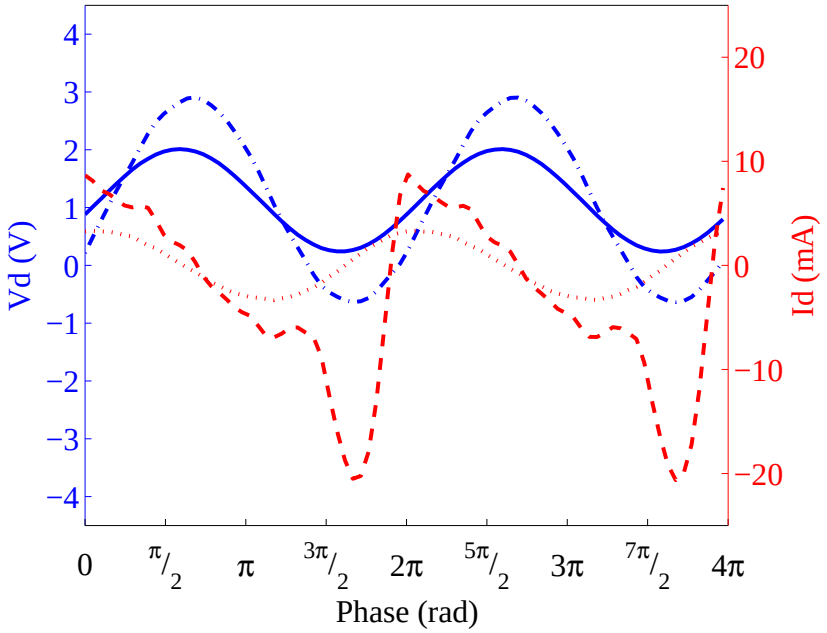


Figure 6.18: Simulated pol1 voltage (dashed blue) and current (red dashed), pol2 voltage (solid blue) and current (dotted red) waveforms across the diode. as in the previous simulated conditions, the rectifier that has the high power is operating with the expected reduced conduction angle intended for this rectifier. The second rectifier does not reach voltages that allow forward bias of the diode, reducing the RF-to-DC conversion efficiency.

of the patch for the given substrate at 2.45 GHz. A harmonic balance simulation with the addition length of line results in constant DC power contours as plotted in Fig. 6.20. Fig. 6.19 is a photograph of the rectifier built with the additional 62°

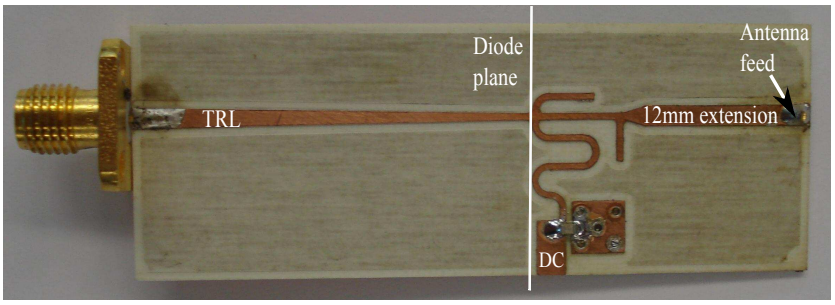


Figure 6.19: Photograph of the rectifier with the 12.5mm impedance matching length and a TRL trace for impedance measurement at the diode plane.

50 Ω line for impedance matching. Two rectifiers were fabricated and connected to the antenna, the DC ports of each polarization were connected to separated DC

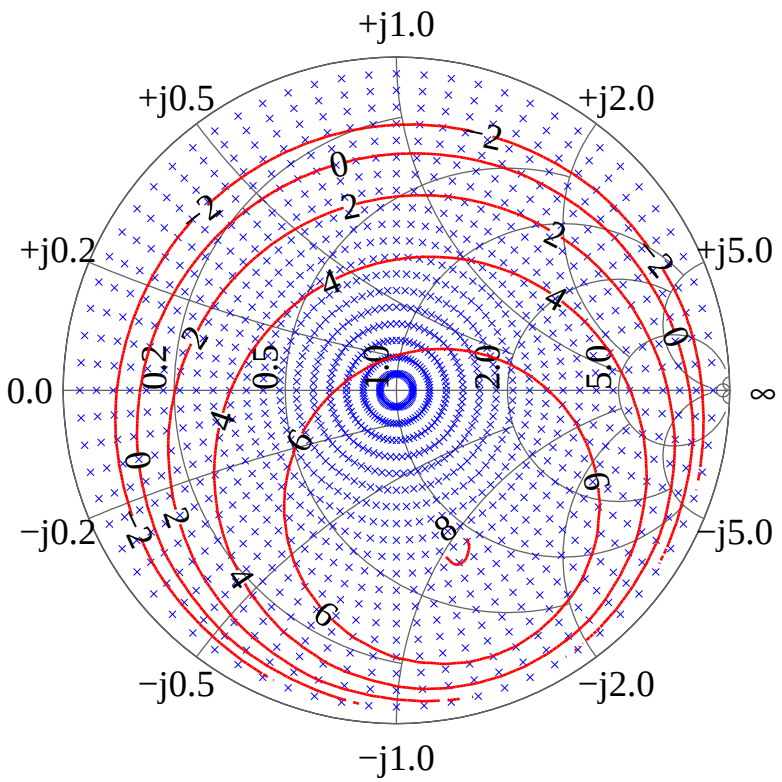


Figure 6.20: The Smith chart has all tuner impedances that were simulated labeled with blue X's and contours of constant DC power in red where the power is given in dBm. The input power to the rectifier is 10 dBm. The Smith chart is normalized to 50 Ω.

loads where the power was monitored on each one separately, as seen in Fig. 6.21. The separation to two DC loads would allow each rectifier to have a different DC voltage across it, and in that way keep optimal conditions (conduction angle and peak voltages) for RF-to-DC conversion. In a practical powering application, it does not make sense to split the power to two loads, but isolation is straightforward by connecting the two DC outputs from the integrated rectifier antenna to two DC-DC boost converters, and connecting the converter outputs to a single load. The separated DC-DC converters each present a real impedance to the rectifier output and hence the use of two DC loads for testing is equivalent [64, 58].

The integrated antenna rectifier described above was fabricated and tested in

an anechoic chamber, as described in Section. 5.2, with the addition of a second DC load and voltage and current meters, to record the DC power.

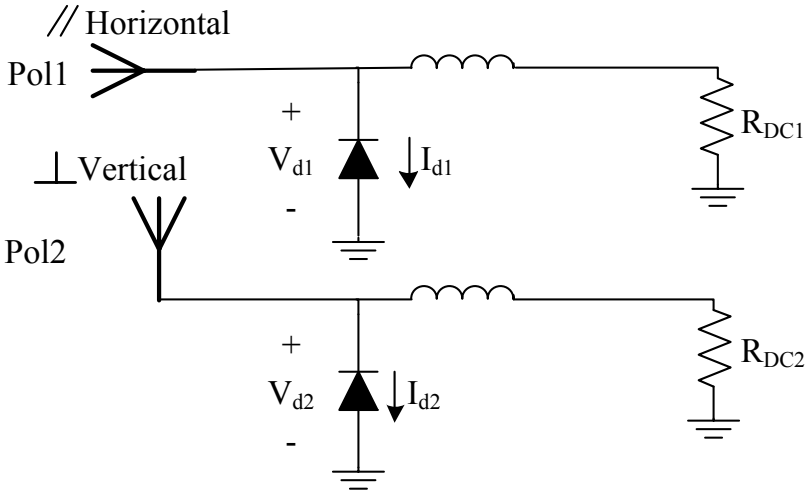
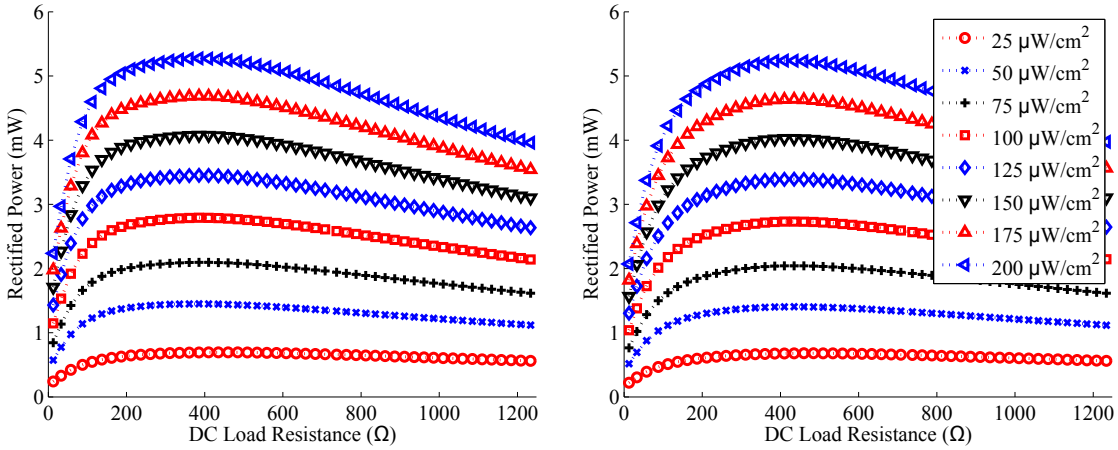


Figure 6.21: Circuit description of the separated DC loads of a integrated patch antenna rectifier.



(a) (b)

Figure 6.22: Measured rectified power versus DC load at incident power densities of 25 to 200 μW/cm^2 for pol1 (a) and pol2 (b), both co-polarized with the transmitting antenna. Each of the measurements was taken with the second DC port unloaded.

First inspection of the results in Fig. 6.26 are encouraging: both antenna

orientations in Fig. 6.26, show very similar curves. Although the repeatability issue seems to be solved, the RF-to-DC efficiency, is lower than before (41% Versus 57%). The efficiency reduction is attributed to an error in fabrication (discovered at a later time), where the feed point via of the antenna was drilled 9 mm away form the edge of the patch instead of 9 mm away from the center. This error connects the rectifier to an input impedance of $32 + j66\,\Omega$ which, lays on the constant DC 6 dBm power contour in place of the 8 dBm, as seen in Fig. 6.20. In spite

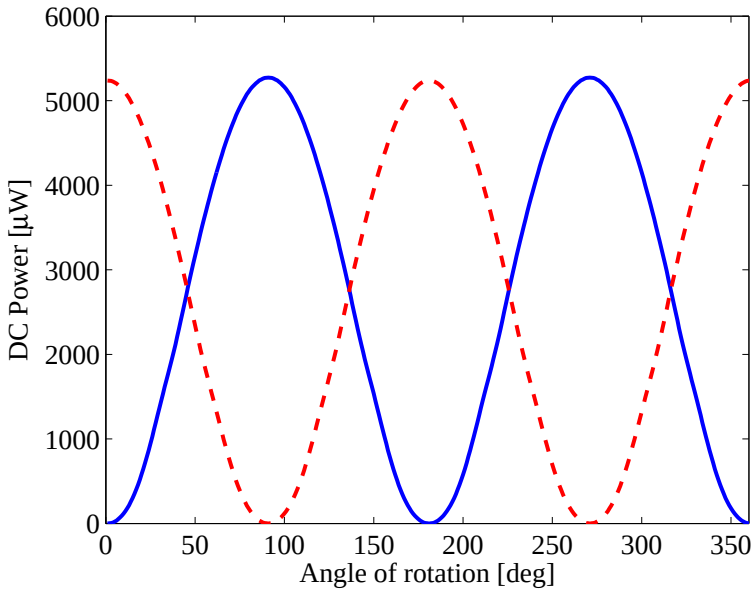


Figure 6.23: Predicted power contribution from each polarization on a 400Ω load. Blue solid pol1, and dashed red pol2.

of the fabrication error, much can be learned from the measurements results of this integrated rectifier antenna. Following the same procedure as described in Section 6.2.1, a lookup table was constructed from the measured data to estimate the power contribution of each polarization. In contrast to the result in shown in Fig. 6.12, the contributions from the two polarizations seen in Fig. 6.23 are nearly identical. The addition of the DC powers is plotted in Fig. 6.24. Once again, the prediction and the measured results do not agree. Notice that the local maxima of the measured trace are at $45° + n \times 90°$ where: $n = 1, 2, ...$ intervals, meaning that

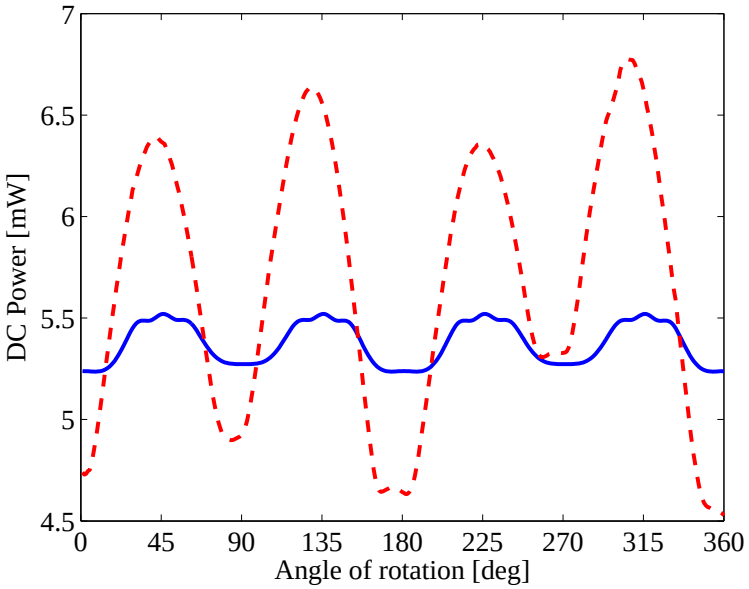


Figure 6.24: Measured power on the two ports as the rectifier antenna is rotated 360° at a power density of 200 μW/cm^2 (red). The predicted dependence (blue) based on assumed DC-separated branches estimations and red dashed is measured over the DC loads.

the vertically polarized incident wave is split equally between the two polarizations at the receiving antenna. The local minima are at $n \times 90°$ where: $n = 1, 2, ...$ intervals, meaning all of the power is going through one polarization on the receive side. These observations point to the conclusion that the two rectifiers are not completely isolated. The design works well when the power to both rectifiers is identical, but the RF-to-DC conversion efficiency degrades for unbalanced pol1 and pol2 branches, as discussed Section. 6.2. A closer look at the current design seen in Fig. 6.21, reveals that, while the two rectifiers do not share the same DC load, they are DC connected though the patch antenna. The connection implies that one rectifier imposes its DC voltage on the other, leading to unnecessary power dissipation. This problem could be solved by different antenna design, for example, a cross dipole [116] or adding a resonant DC blocking capacitor between the antenna feed and the rectifier as in Fig. 6.25.

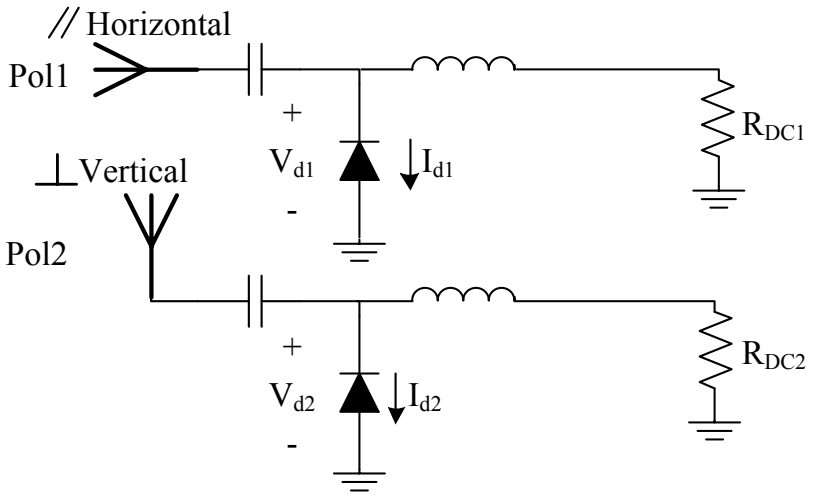
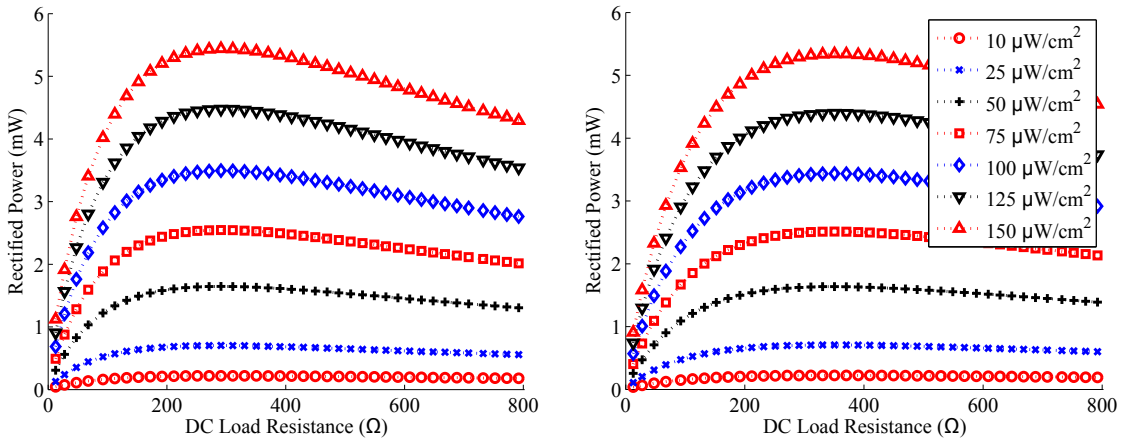


Figure 6.25: Circuit description of the isolated DC path and separated DC loads of a integrated patch antenna rectifier.

An integrated rectifier antenna incorporating the resonant capacitors between the antenna feeds and the rectifiers, was fabricated and tested. The measured data



(a) (b)

Figure 6.26: Measured rectified power versus DC load at incident power densities of 25 to 150 μW/cm^2 for pol1 (a) and pol2 (b), both co-polarized with the transmitting antenna. Each of the measurements was taken with the second DC port unloaded.

in Fig. 6.26a and in Fig. 6.26b are almost identical, pointing to good polarization

isolation. In addition to the good isolation between the polarizations, there is true isolation between the rectifiers and diodes in this circuit. Since the rectifiers are isolated from each other, any leakage power form one polarization to the other will not interfere with the rectifier operation, and the optimal conduction angle can be found by adjusting the separated DC loads. A DC isolation between the two rectifiers allows return to feed points closer to the center of the antenna, since each rectifier is loaded only by it's own diode. With careful attention to fabrication and via placements good repeatability is achieved and a reduced size matching circuit is used, as seen in Fig. 6.31c. As with the previous two integrated rectifier antennas, lookup tables for each of the tested polarizations were constructed to estimate the DC power as a function of the antenna rotation angle.

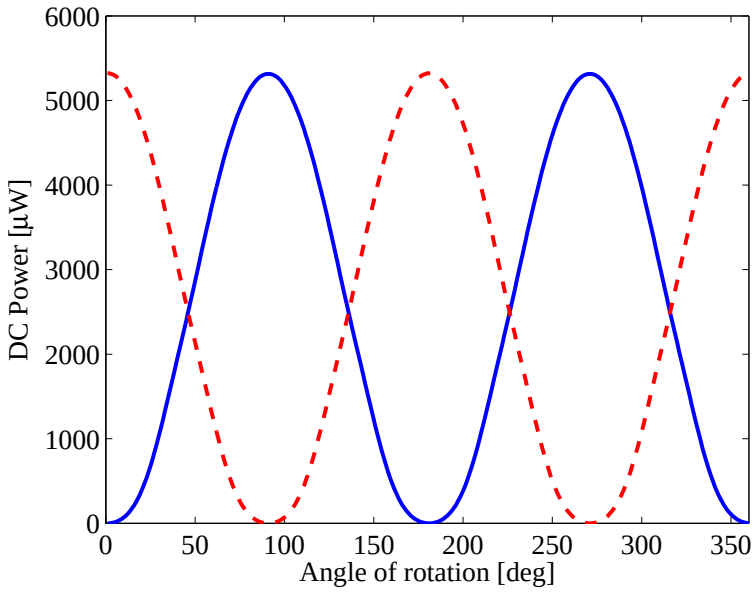


Figure 6.27: Estimated power contribution from each polarization on a 400Ω load at a power density of 150 μW/cm^2. Blue solid is pol1 and dashed red is pol2.

The prediction of the output DC power is plotted in Fig. 6.27 for each rectifier. The measured output DC power data is presented in Fig 6.28. The measurement and prediction have excellent agreement over the all rotation angles. Notice that at the cross-polarization angles (where the power is close to zero) the gradient of the

curve is changing slower than at the co-polarized (maximum power peaks) regions, since the rectifier efficiency drops at lower incident powers.

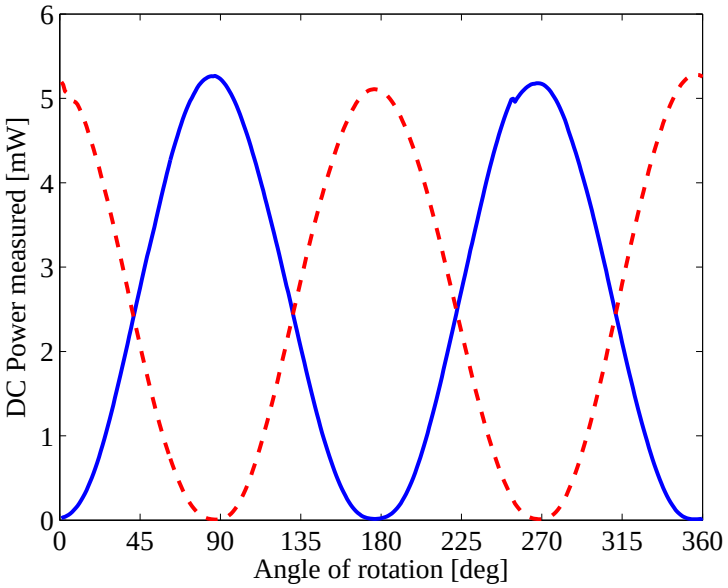


Figure 6.28: Measured power contribution from each polarization on a 400Ω load at a power density of 150 μW/cm^2. Blue solid is pol1 and dashed red is pol2.

Finally, the predicted powers for both polarizations are added and compared with the sum of the measured powers in Fig. 6.29 and Fig. 6.30. In an ideal case where the rectifier efficiency was constant over all input powers and the two polarizations are perfectly balanced according to (6.1), the total output power would have no ripple and would be a horizontal line in the plot. The small oscillations seen in the total power in Fig. 6.29, are due to the efficiency curve of the rectifier. At $45° + n90°$ where $n = 1, 2, ...$ intervals, the power is split evenly between the two rectifiers, with equal RF-to-DC efficiencies. As the antenna is rotated,the power in one of the polarizations is increases, and hence the efficiency increases as well. In the other branch, the power is drops and as does the efficiency, but at a steeper rate. The higher powered branch will dominate the total RF-to-DC conversion efficiency. In Fig 6.30, the data from Fig. 6.29 is plotted on a finer scale and the maxima and minima points are seen much clearer. The lower peak at 180° is probably due to a

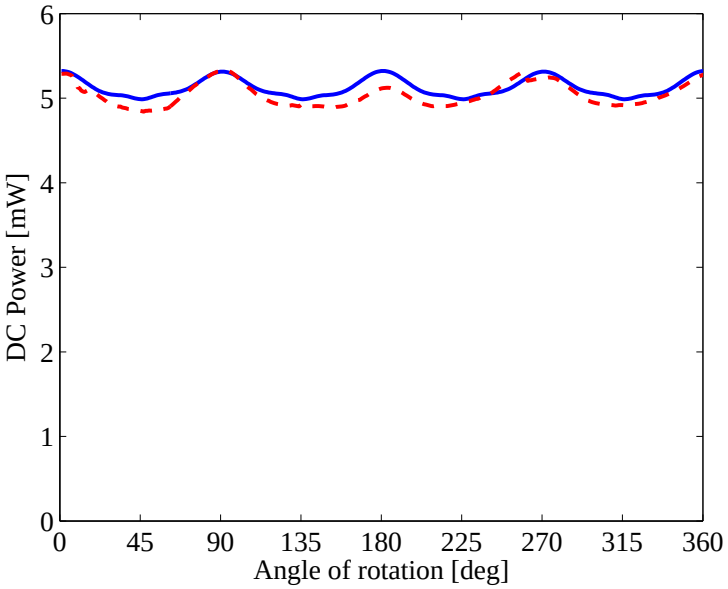


Figure 6.29: Power on the two ports as the rectifier antenna is rotated by 360° in a power density of 150 μW/cm^2. Blue estimated based on the separated co-polarized estimations and red dashed is measured over the DC loads.

slight misalignment in the antenna placement on the stepper motor in the anechoic chamber that resulted in a rotation that is not exactly around the antenna axis and as a result misaligned with the transmit antenna.

This result is the first integrated rectifier antenna that is not circularly polarized and exhibits this flat of a response with respect to rotation, to the best of the author's knowledge. There is not much published data about the behavior of integrated rectifier antenna when they are polarization mismatched. A meaningful figure of merit for polarization misalignment is the ratio of maximum to minimum rectified power as the integrated rectifier antenna is rotated w.r.t. a linearly polarized transmitter. An ideal antenna would give the ratio of 1. Table. 6.1 shows this DC axial ratio (DCAR) for the integrated rectifier antenna shown in Fig 6.31 The antenna presented here, results in a ratio of 1.09, In comparison, [7] yields 1.72 and [27] and [114] yield 2.98 and 1.6, respectively.

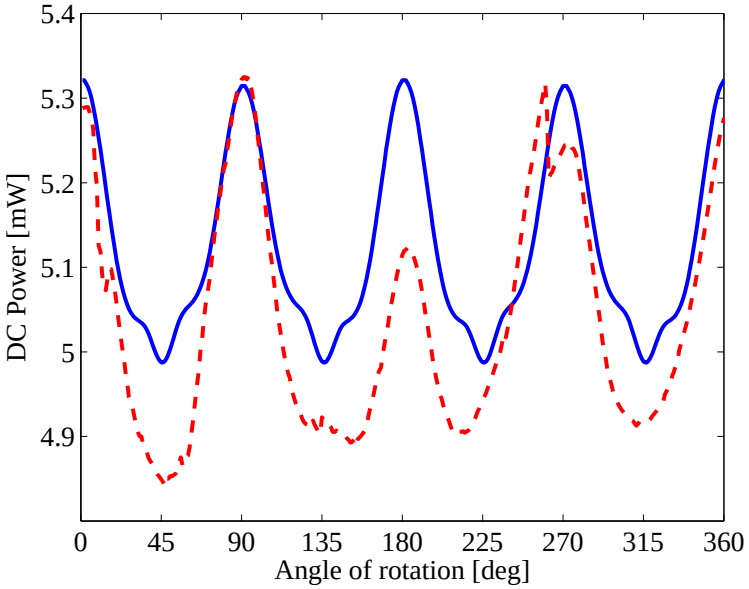


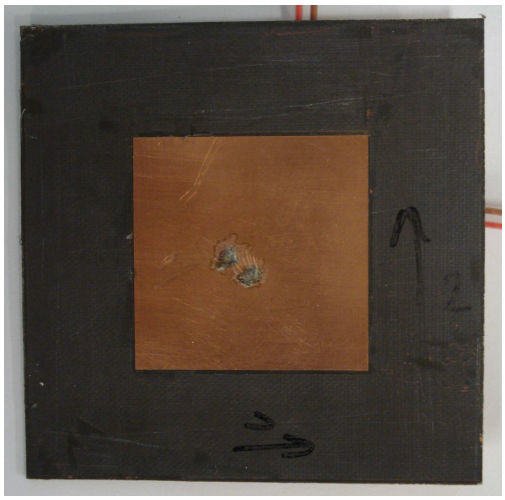
Figure 6.30: Power on the two ports as the rectifier antenna is rotated by 360° in a power density of 150 μW/cm^2. Blue estimated based on the separated co-polarized estimations and red dashed is measured over the DC loads. The power scale has been changed to much finer in order to be able to see the small differences between the two traces.

Table 6.1: DCAR overview described in the literature.

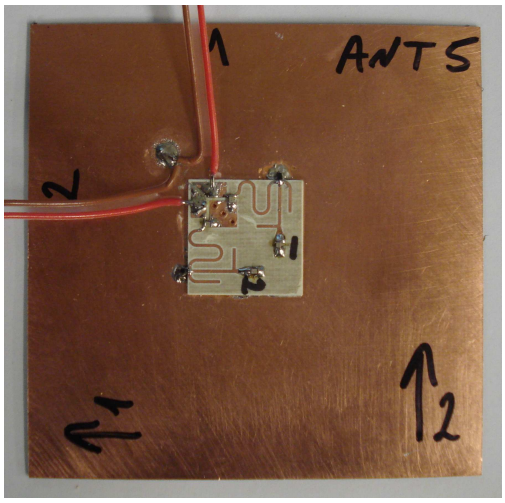
Ref	f (GHz)	antenna type	DCAR
This work	2.45	Patch	1.09
[7]	2.45	Patch	1.72
[27]	2.45	Cross slot patch	2.98
[114]	2.45	Cross slot patch	1.6

6.3 Summary

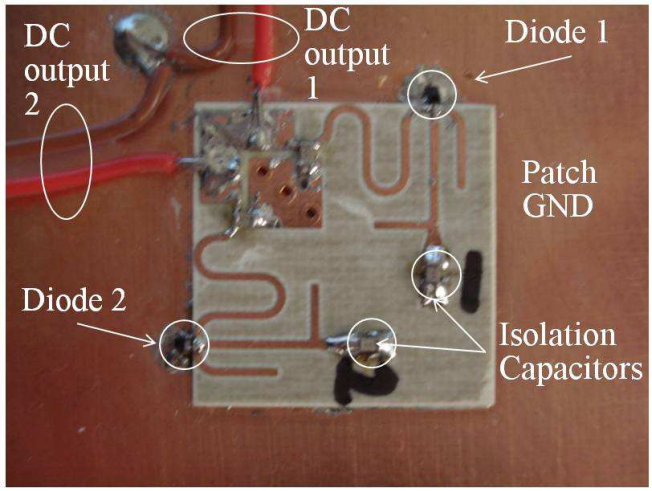
This chapter extends the method from Chapter. 5 to a dual-polarized patch antenna integrated with two rectifiers, one for each polarization. A comprehensive analysis of required RF and DC isolation in multiple-rectifier integrated rectifier-antenna is developed and confirmed with a series of experimental rectifier-antenna results. A dual-polarized integrated rectifier-antenna has been shown by a number of authors



(a)



(b)



(c)

Figure 6.31: Photographs of front side (a) ground plane and the two rectifiers (b) closeup of the two rectifiers(c), of the DC isolated dual polarized integrated rectifier antenna.

to improve the variation of efficiency as a function of antenna orientation in a multipath channel, but to the best of the author's knowledge, there has been no report on the required RF-RF, RF-DC and DC-DC isolation between the various components of a dual-polarization multi-rectifier topology. The conclusion from the simulations and experiments is that isolation between rectifiers is important at both RF and DC in order to achieve high overall rectification efficiency. This implies

that the architecture of a low-power wireless sensor with improved orientation sensitivity for wireless powering will require a separate power management circuit (emulated resistance from Chapter. 2) for each rectifier, and that the DC loads of the rectifiers should have high isolation between them.

Chapter 7

Summary and Contributions

Contents

7.1 Thesis summary and outlook

This thesis establishes the required methodology for design and implementation of integrated rectifier antennas with optimized efficiency for far-field low-power

non-directive wireless power reception. The research has shown that efficiencies greater than 50 % can be obtained for power density levels in the 100 μW range, using the most conservative efficiency definition. Although, to the best of the authorŠs knowledge, the demonstrated efficiencies are the highest reported for the power levels and frequencies of interest, there remain several areas of possible improvements, as discussed in the next section of this chapter. In addition, there are a number of applications which dictate different antenna topologies and will require system considerations beyond the wireless sensor platform.

Alternative designs in the future can explore:

- Different rectifier topologies and devices (Section. 7.2.1);
- Various antenna types depending on the environment, size constraints, circuit integration, etc. and corresponding integration with rectifiers (Section. 7.2.2);
- Power management circuit, storage, low-power transceiver integration (Section. 7.2.3);
- System integration which includes transmitter considerations (Section. 7.2.4);
- - Different propagation environments (Section. 7.2.5).

It should also be noted that, although most of the work in this thesis was funded by the National Science Foundation for integration with heterogeneously integrated transceivers, and the Rehabilitation Engineering Research Center for the Advancement of Cognitive Technologies RERC-ACT for assistive technology [54], there has been a significant interest from various companies for specific applications and designs:

(1) During the research described in this thesis, we have worked with PowerCast, a company that enables wireless power solutions [121], to enable low-profile

915 MHz efficient rectifier-antennas, and one of the antenna candidates will be described in Section. 7.2.2.

(2) Sierra Nevada Corporation (formerly MicroSat Corporation) [122] has requested a system for scavenging power from cellular phone towers, funded by DARPA. For this task, a square patch array was developed at a frequency of 1.96 GHz, described further in Section. 7.2.2. In addition, the SNC space division has included a small rectifier-antenna array printed on a flexible substrate as a part of a space-born payload on a satellite, currently still in orbit. The goal is to determine how much power the rectifier antenna array can harvest from the satellite transmit antenna sidelobes.

(3) Masco Corporation, a construction company which own a number of other companies with products ranging from windows to faucets (masco.com), has shown interest in developing low power sensor platforms for their green low-energy home products [123]. The main products that would benefit from low-level wireless powering are light-level sensors, temperature sensors, occupancy (CO_2) sensors, mold sensors, and flow sensors for HVAC systems. The feedback from such sensors can be used to control the house environment and lead to a reduction in energy consumption and improved living conditions. As part of the work for Masco, a study of available power densities at different frequencies was conducted in typical home and office environments and concluded that the average amount of RF power densities is not sufficient to power a sensor and that a dedicated power source should be used in order to power the platforms. A design based on the platform in [59, 58] was used with a dipole integrated rectifier-antenna array to power a Masco light switch, and the details are described in a technical report to the company and are briefly discussed in Sections. 7.2.2, 7.2.3 and 7.2.5.

(4) The Coleman Institute [124] is interested in improving lives for people with disabilities and has funded work for developing a prototype wireless powering ŞdrawerŤ that would enable universal simple generic powering of wireless assistive and other devices, without the need for specific wall-plug powering units, described in Section. 7.2.5.

(5) Cymbet, a leading manufacturer of thin-film batteries [125] has licensed IP from the University of Colorado and is now developing products which include our power management designs with various powering sources such as piezo-electrics, photovoltaics, etc. Recently, Cymbet has decided to include RF energy harvesting, and the integrated rectifier antennas described in detail in Chapter 6 have been delivered to Cymbet and have been shown to work well with their energy harvesting evaluation board [44].

7.2 Future Work

7.2.1 Rectifier Topologies and Devices

The thesis focuses on simulation and experiments on a single diode rectifier. Other rectifier configurations can also be considered [126, 27], and two examples are shown in Fig. 7.1. The source-pull measurements were repeated for these configurations and are summarized and compared to the single diode rectifier in Table 7.1. From this measured data, verified with simulations, a single diode gives the best efficiency for the input power levels of interest, which in turn correspond to the 25-200 μW/cm^2 incident power density for the example patch antenna from Chapter. 5. In (b) and (c), the losses are increased, it takes more power to turn both diodes on, and the diodes are most likely different resulting in different bias conditions. It is likely that for high power levels, with well-matched diodes, two-diode rectifiers would

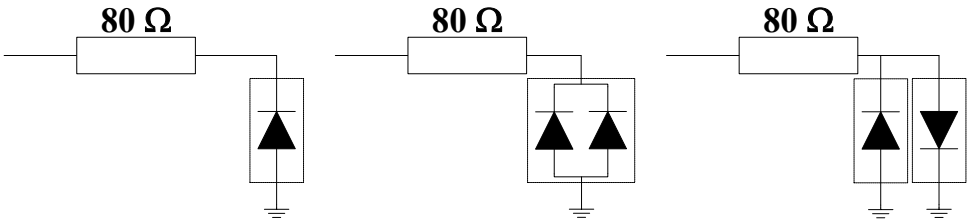


Figure 7.1: Three diode rectifier topologies were measured and simulated using the same method: (a) single SMS-7630-79 Schottky diode, described in detail throughout the paper; (b) SMS-7621-74, two-diode package and (c) two anti-parallel SMS-7630-79 diodes.

result in higher efficiency. On the other hand, for low power densities where the RF voltage is not high enough to forward bias the diode, pre-biasing the diode using power from the energy storage will result in rectification at lower powers, but with a price of reduced efficiency and increase in circuit complexity. A good topic for future research would be to investigate particular losses for which the overall powering efficiency will increase. The amount of benefits will depend on the pdf of power levels and the type of diode.

Table 7.1: Summary of Measured Maximum Rectified Power for Optimal RF and DC Impedance at the Diode Terminals

P_{in}	Configuration	$P_{DC,max}$	$Z_{RF,opt}$	$R_{DC,opt}$
0 dBm	A	-1.64 dBm	120+j240 Ω	1050 Ω
	B	-2.24 dBm	33+j126 Ω	1000 Ω
	C	-2.23 dBm	53+j108 Ω	880 Ω
10 dBm	A	8.1 dBm	137+j149 Ω	460 Ω
	B	7.2 dBm	33+j126 Ω	1005 Ω
	C	4.8 dBm	60+j25 Ω	1030 Ω

Although RF-to-DC efficiencies of the integrated rectifier-antennas presented in this thesis are high in comparison to previous work at these sizes and power densities, further improvement may be possible. Diode selection is critical, and

although for the ISM bands presented here the silicon Schottky diodes worked well, other technologies such as GaAs and GaN (gallium nitride) might prove to be a better choice for higher frequencies or powers. GaN high electron mobility transistors (HEMTs) are known for there favorable electric characteristics for high efficiency power electronics. The high breakdown voltage, low on resistance and fast switching speeds are attractive for rectifier design as well [127]. The higher breakdown voltage allows for devices that are smaller than Si devices for the same power levels. Smaller devices lead to less junction parasitic capacitance, which is one of the main contributes for power dissipation within the rectifying device. Nevertheless, no matter what device technology is chosen, the same method as the one demonstrated on Si Schottky diodes in this thesis can be applied and will guarantee high efficiency. In addition, it is possible to extend the theory presented in this thesis to three-terminal transistor rectifiers, which are more complex since they require a gate drive, but might prove to be good rectifiers for higher power levels.

7.2.2 Antenna and array considerations

In the previous chapters, mainly patch antenna element integration with rectifiers was presented. A patch antenna has the advantage of being backed by a ground plane, and for wireless powering applications, this implies that it can be placed on any surface, and electronics can be packaged on the common ground plane. However, a patch does not radiate well in the ground plane direction, and there are cases where omni-directional reception in one plane is required. The antenna for a specific application should be selected so that the aperture is as efficient is possible. In cases where the relative orientation between the rectifying antenna and the powering source (or sources)is known, the gain of the antenna should be maximized in the source direction. Fig. 7.2a shows an example dipole antenna with an integrated

rectifier, and Fig. 7.2b a folded slot printed on a flexible substrate [58, 128]. The goal for the printed dipole design is to reduce the dipole length as much as possible, while enabling match to the diode optimal rectification impedance. The shape of the metal on the 60-mil thick FR4 substrate provides reactive loading along the antenna resulting in a dipole size of 100 mm × 13 mm (work done for PowerCast). In order to match to the optimal diode impedance, a series inductor was added at the feedpoint. The folded slot antenna can be made on a flexible substrate without a metal ground plane, where ICs for power management can be integrated in the slot ground. The slot antenna prototype in the figure has a roughly 100 Ω input impedance at 5.8 GHz, and the measured data for both linear polarizations is shown in the figure. The slot can also be backed by a ground, resulting in a doubled efficiency.

(a) (b)

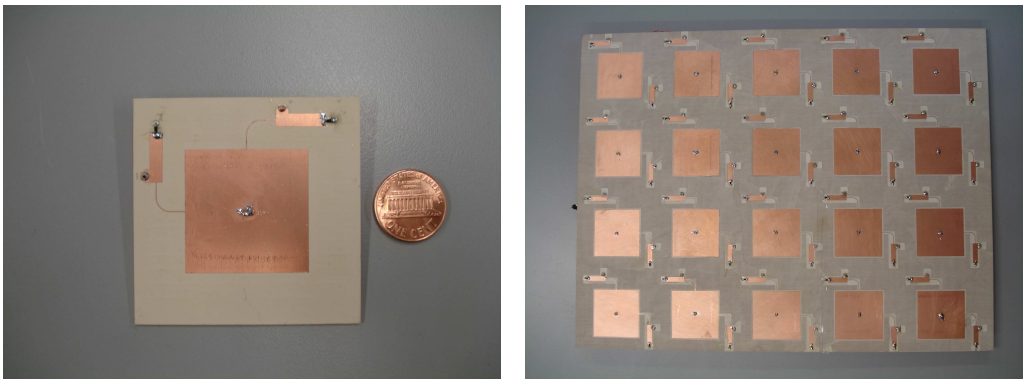
Figure 7.2: (a) 2.4 GHz dipole integrated directly with a diode. (b) Printed dipole at 915 MHz is reactively loaded to reduce the length to 100 mm, with a surface-mount inductor in the feed allowing for improved matching to the rectifier. (c) Printed 5.8 GHz folded slot on a flexible substrate and its measured rectified power. (d) Dual polarized patch antenna with Schottky diodes directly connected for small footprint at 5.8 GHz.

Arrays of antennas have been employed for directive beaming, e.g. [15], where a corporately fed array was connected to a single diode for improved rectification

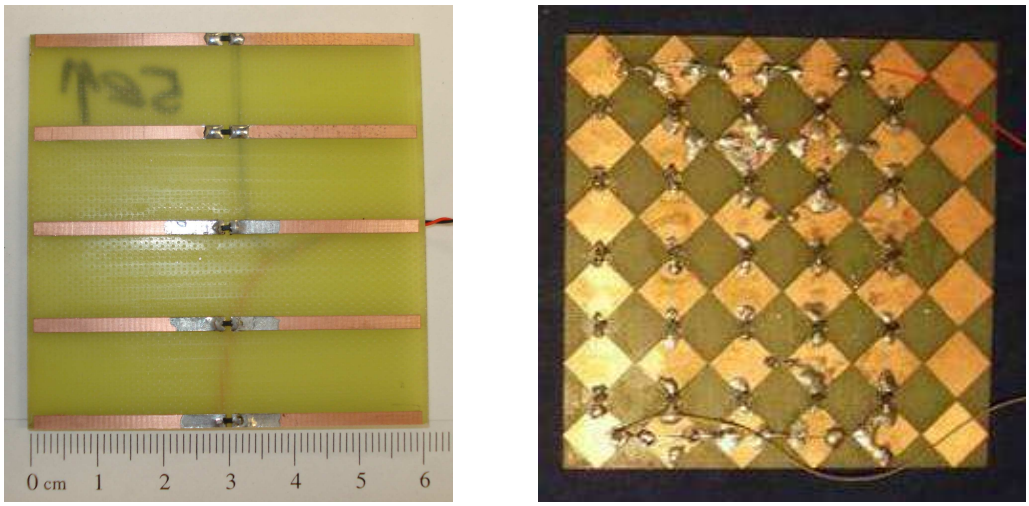
efficiency. This approach is only efficient when the transmit and receive antennas are aligned for highest gain. In a distributed wireless sensor powering application, where often the sensor position is not known, a directional antenna is not an advantage. Fig. 7.3a shows a single 1.96 GHz element patch and Fig. 7.3b shows a patch array used for scavenging power from a cell-phone base-station tower. Each element of the array contains a rectifier, and the resulting DC power is combined. In this way, the directivity of the entire array is the same as that of a single patch, though the edge elements will have a slightly different pattern than the center elements. This fact was shown earlier in [16] and confirmed by results with an 20-element patch array with a power management circuit based on commercial components and described in [64]. A similar array (with no diode matching) of dipole antennas is shown in Fig. 7.3c, designed for 2.4 GHz. Here the dipoles are coupled, resulting in broader band performance. Fig. 7.3d shows a broadband self-complementary non-resonant array of printed bow-tie antennas with integrated dual-polarization diodes, which allows easy scaling to larger size arrays, and can operate at high or low power densities, but does not provide an optimal impedance match to each rectifier since the impedance at each feed point is real and around 189 Ω.

7.2.3 Integration with power management, storage and control

At the low power levels, the limiting factor for efficiency is the low-cost hybrid power management circuit, though IC versions have shown to have much better low-power efficiencies [61]. An example of a low power integrated power management circuit from [61] is shown in Fig. 7.4. Combining of the sensing, transmission, and power converter circuits leads to a small size, low-complexity, highly integrated application circuit and similar approaches in other silicon processes are expected to



(a) (b)



(c) (d)

Figure 7.3: Single patch element 30 mil thick Rogers 4350*b* substrate at 1.96 GHz from the Sierra Nevada Corporation patch array (a). Patch array on 30 mil thick Rogers 4350*b* substrate used for Sierra Nevada Corporation Demo, size 300 mm × 240 mm at 1.96 GHz (b). Dipole array on 60 mil thick FR4 substrate used for Masco Demo, size 60 mm × 60 mm at 2.45 GHz, (c). Bow-tie integrated rectifier-antenna array. The squares are 1 cm on the side, and there are 16 Skyworks diodes in the array(d).

result in very efficient power management ICs for various harvesting applications.

The dual polarized rectifying antenna detailed in Chapter. 6, drives the need for further work on converter architecture. A converter with two isolated inputs is needed. Rather than having two Boost converters in parallel and each one of them having it's own control circuitry, a design reducing the control to a single

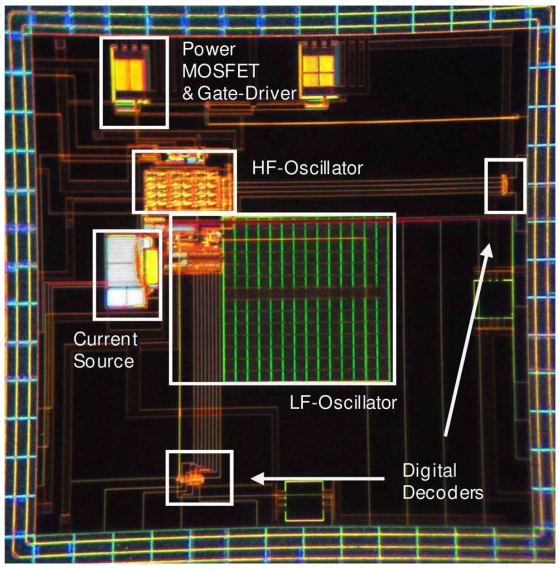


Figure 7.4: Microscope image of energy scavenger IC fabricated in 5 V, 0.35 μm CMOS process. Various circuit components are labeled. The dimensions of the chip are 2 mm $\times$ 2 mm.

microcontroller that keeps each converter branch at its peak efficiency, could result in lower overhead control power. A study comparing overall efficiency (integrated rectifier antenna and DC-DC converter) of the RF and DC isolated dual polarization antenna to the non isolated integrated rectifier antenna wold lead to optimized converter and control design.

The energy collected from integrated rectifier antennas must be converted to a form that can be stored for later use. In remote sensor systems or portable device applications that use energy harvesting a small rechargeable battery or storage capacitor is often employed to store the collected energy the system needs for operation. The drawbacks to each of these storage methods are numerous in that even rechargeable batteries wear out after a few hundred charge/discharge cycles and need to be replaced. Super-capacitors on the other hand tend to change characteristics over time, as well as self discharge rapidly by as much as 20% per day, causing much of the converted energy to be wasted. Both IPS [129] and Cymbet [125] offer a solution with solid-state batteries; Cymbet offers the EnerChip

solid state battery on silicon as the energy storage element in the system to eliminate the need for replacement since it can support in excess of 5000 cycles and has a minimal self-discharge of less than 3% per month [57]. This data should be taken in to account for long lifetime sensor, as those embedded in concrete for structural monitoring. On the other hand, IPS offers THINERGY Micro-Energy Cells (MECs) solid-state on thin metal foil, rechargeable, energy storage. These paper-thin MECs are flexible and provide long cycle life with good power performance. Able to operate in temperatures ranging from $-40\,C^{\circ}$ to $+85\,C^{\circ}$, these ultra-thin MECs offer low self discharge rates, low cell resistance and high power [129].

Although solid-stage batteries have shown a big improvement in self discharge and trickle charge capability over other battery technologies, they are still sensitive to discharge below their threshold voltage.

As part of the higher degree of integration, the storage element could be integrated with the antenna. The thin-film battery can be used as the conductor for the patch antenna. Fig. 7.5 shows the first prototype which tested this idea, to the best of our knowledge. In this example, an Infinite Power Solutions thin-film battery is glued on to FR4 substrate and used as an antenna. The patch antenna-battery was characterized and showed only a slight frequency shift in resonance compared to a standard patch antenna on the same substrate, most likely due to the multi-layer nature of the battery. Such integration will allow further size minimization of the energy storage element and power receiving antenna.

Further integrations and size minimization can be reached with controller transceiver integration. An example for such an integration is, the CC1010 from Texas Instruments. The CC1010, is a true single-chip UHF transceiver with an integrated high performance 8051 microcontroller with 32 kB of Flash program memory. The RF transceiver can be programmed for operation in the 300 to 1000 MHz range, and is designed for very low power wireless applications [130].

Figure 7.5: Photo of a 2.8 GHz patch antenna made from a battery and 60 mil FR4 substrate. Battery dimensions are 25 mm × 25 mm.

7.2.4 Wireless powering system and transmitter considerations

An entire wireless powering system consists of the power receiver, which is the main topic of this thesis, and of power transmitters located in the far field of the receiver. A general powering scenario is shown in the sketch of Fig. 7.6, where a powering transmitter operating in an ISM band and compliant with FCC rules (to be discussed later) sends non-directional RF waves towards sensors that can be embedded in structures or behind obstacles. Since RF waves propagate around corners and through most materials (metal excluded), this enables powering of multiple sensors simultaneously. The sensors are embedded in a self-powered platform which manages the received RF power in order to transmit data when sufficient power is available. Note that more than one powering transmitter can be used in this scenario, either using the same narrow bandwidth (essentially single frequency), or using multiple frequencies or wider spectrum over which the integrated rectifier antennas operate efficiently. It has been shown that using

multiple frequencies for powering increases the efficiency for all cases of incidence angles and relative time of arrivals [16]. It is also of interest to consider modulating the transmitter to optimize efficiency. Finally, the transmitters themselves should be efficient, but since there are no linearity requirements, efficiencies above 80 % should be possible in the 2 GHz band with a few watts of power using GaN transistors [127]. Integration of a full system with studies of relative positioning of multiple transmitters and sensors is an interesting and practical area of future work.

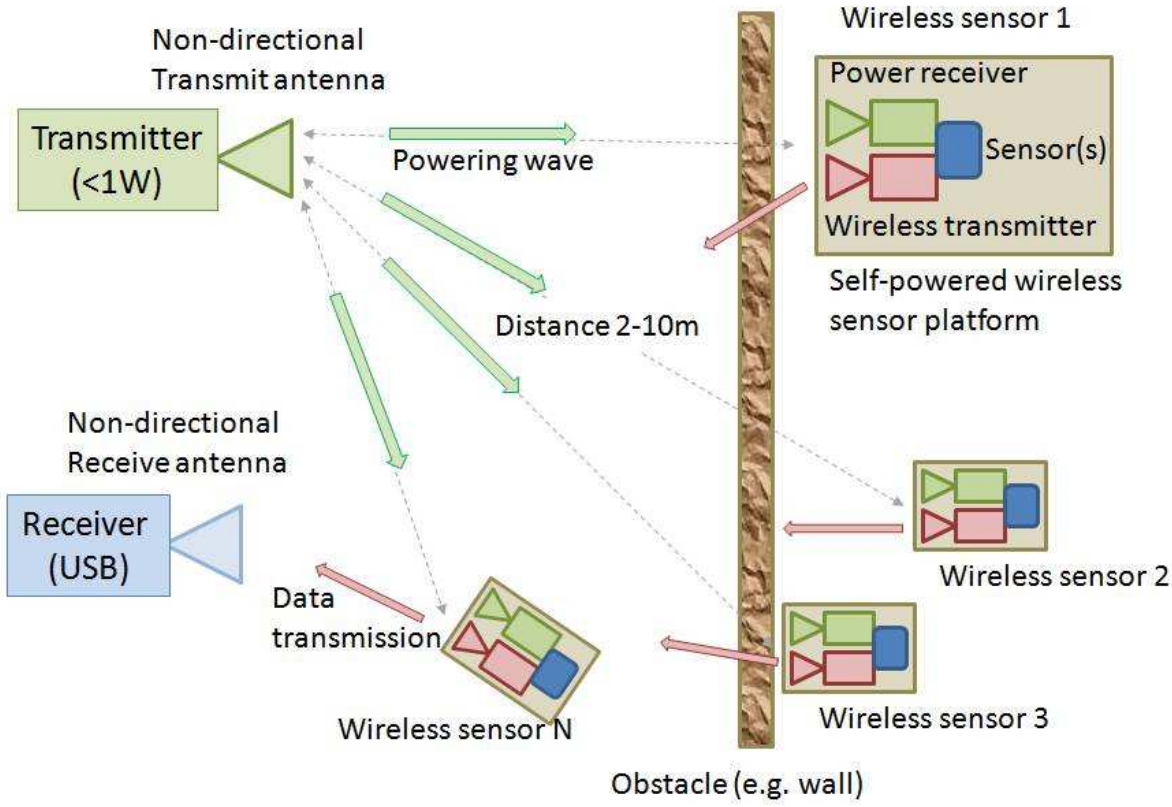


Figure 7.6: Multi-sensor, multi-transmitter, general powering scenario

7.2.5 Propagation environment considerations

This thesis deals with line-of-sight and/or multipath channel power transmission from a far-field transmitter. However, a similar approach can be used for envi-

ronments where waves other than uniform plane waves carry power. An example of an over-moded rectangular waveguide cavity, referred to as the "power box" is shown in Fig. 7.7. This device was designed for powering a number of devices

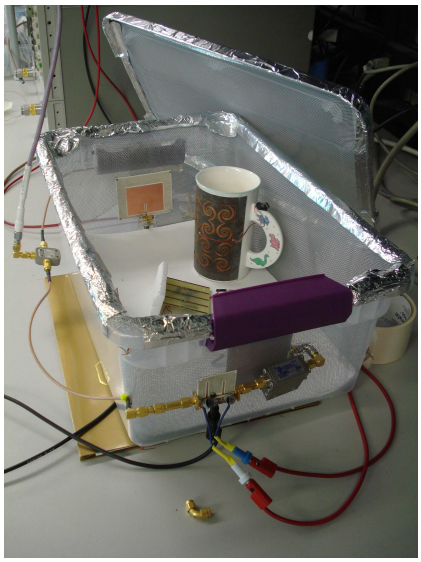
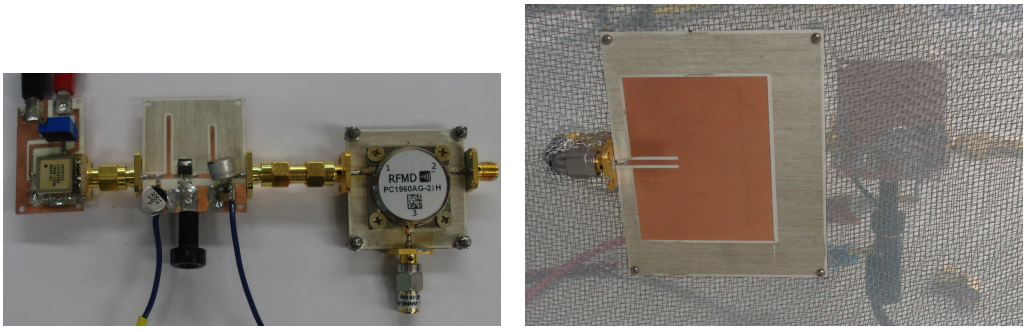


Figure 7.7: Photo of a charging box at 1.96 GHz, the box has two radiators oriented orthogonally to each other. The metal screening is used as a reflector that keeps all radiation within the box while the lid is closed. The reflections within the box make the orientation of the rectifier antenna irrelevant and power is harvested at all locations.

simultaneously by a complex field due to a number of modes excited in the loaded cavity. Two transmitting probes designed as patch antennas and fed by 1.96 GHz transmitters are placed on opposite walls of the box implemented from a metal mesh with -3 dB transmission at the powering frequency. The patches are fed through surface-mount circulators by $1-W$ PAs with 77% power-added efficiency at 1.96 GHz, Fig. 7.8. Preliminary measurements, with a power management and monitoring circuit antenna situated outside of the box and transmitting data, show that the box effectively powers several devices simultaneously. Future work in this area requires further studies of optimal mode distribution, resonator design and feeding, allowable device placement, number of devices, etc. in order to make this device practical. An example of a low cost < 1 W transmitter assembled from

off-the-shelf components is given in Appendix.I.

Similar non-plane wave environments are found in HVAC pipes, where flow and vibration sensors can be placed for building monitoring. In this case, standard size pipes are overmoded waveguides at most microwave frequencies, and guided waves can be used to power the sensors. This would be another interesting area for future work, since monitoring room occupancy and flow in HVAC pipes can lead to significant savings in energy, as most rooms are designed for maximal occupancy but are rarely fully occupied. Finally, it should be noted that the work shown in this thesis is directly applicable to directive power beaming. The difference would likely be the type of diode, and the fact that either a larger corporate-fed array or single high-gain antenna, would be connected to the rectifier. In this case, more complicated rectifier topologies, such as the ones described at the beginning of this section, would be practical since the higher power densities would allow for efficient rectification by multiple diode rectifiers.



(a) (b)

Figure 7.8: The powering chain composed of a VCO, amplifier and circulator (a). The patch antenna inside the charging box that connects to the powering chain (b).

7.3 Thesis contributions

The contributions of the work presented here can be summarized as follows:

- Chapter. 2 discusses wireless sensor platform architecture and integration and explains the requirements for the integrated rectifier and antenna which act as the far-field RF power front end receiver. The architecture is focused on low-power low duty cycle data transmission and is used to explain the requirements for the integrated rectifier and antenna. In specific, low-power circuit approaches to the power management and control portions of the sensor are discussed. The discussion of the sensor as a system shows how the theory and experiments in this thesis enable low-power maintenance-free wireless sensors. This work was done in collaboration with Prof. Regan ZaneŠs group and the Colorado Power Electronics Center (CoPEC) at the University of Colorado, and is reported in [58, 59, 60, 61].

- Chapter. 3 develops an analysis of nonlinear rectifiers and derives the conditions necessary for high efficiency rectification. Both time-domain and frequency-domain Fourier analysis are presented assuming diode rectifying devices, with ideal as well as non-ideal diode models. Time-domain waveforms across the rectifying element are derived and the relationship between their shape and RF-DC conversion efficiency is discussed in detail. For best efficiency, it is shown that harmonic frequencies of the incident RF wave need to be appropriately terminated at the diode terminals in order to accomplish required wave-shaping resulting from the time-domain analysis. The results are reported in [84, 85], and add a new paper for MTT Trans expanded from IMS.

- Chapter. 4 presents methods for experimental-based rectifier modeling and non-linear frequency-domain harmonic balance simulations of microwave rectifiers, and the agreement between them. The close correlation between the two, which follows trends from Chapter. 3, provides confidence in the

non-linear simulation for future designs. This chapter extends the theory and analysis to design-oriented simulations and experimental validations of the nonlinear models and is reported in [85, 84].

- In Chapter. 5, the integration between rectifiers and antennas for wireless powering is addressed and a method developed that results in maximized efficiency. The method is demonstrated in simulation and experiment on the example of a patch antenna and Schottky-diode single-ended rectifier. Calibration, circuit validation, impedance matching to nonlinear impedances, DC collection circuit design and integrated rectifier-antenna characterization is presented in detail. It is shown that the order of steps taken in rectifier-antenna integration is critical, and these results are reported in [108, 84, 109].

- Chapter. 6 extends the method from Chapter. 5 to a dual-polarized patch antenna and presents a comprehensive analysis of required RF and DC isolation in multiple-rectifier (one for each polarization) integrated rectifier-antennas. A comprehensive analysis of required RF and DC isolation in multiple-rectifier integrated rectifier-antenna is developed and confirmed. Isolation between rectifiers is important at both RF and DC in order to achieve high overall rectification efficiency. A publication of these results is planned for the near future.

In conclusion, the area of far-field wireless powering is a promising solution for low-power low-duty cycle, maintenance-free wireless sensors with increased lifetimes. This thesis develops several design methods for optimizing efficiency of power-reception circuitry and demonstrates the method on several experimental models. However, a lot remains to be done, and this chapter presents some of the possible future research directions in this interesting area of microwave engineering.

Bibliography

[1] E. Falkenstein, *The effect of plastic deformation on the bainite transformation near the Bs temperature*. Illinois Institute of Technology, 1970. vi

[2] E. Ripling and E. Falkenstein, "Measuring kr-curves for thin sheets," in *ASTM STP 527, American Society for Testing and Materials*, pp. 36–47, 1973. vi

[3] E. Ripling and E. Falkenstein, "Flow and fracture properties of aluminum alloys potentially useful for small arms cartridge cases.," in *Defense Technical Information Center OAI-PMH Repository (United States)*, 1973. vi

[4] Z. Y. I. Amnon Kritzman, Z. Y. I. Eliezer Falkenstein, H. I. Moshe Ish-Shalom, H. I. Alla Buch, and H. I. Menuha Beer, "Optical fiber sensing device for analysis," 09 1991. vi

[5] U. Lee, K. D. Song, Y. Park, V. K. Varadan, and S. H. Choi, "Perspective in nanoneural electronic implants with wireless power-feed and sensory control," *Journal of Nanotechnology in Engineering and Medicine*, vol. 1, no. 2, p. 021007, 2010. 2, 5

[6] J. Bernhard, K. Hietpas, E. George, D. Kuchima, and H. Reis, "An interdisciplinary effort to develop a wireless embedded sensor system to monitor and assess corrosion in the tendons of prestressed concrete girders," in *Wireless Communication Technology, 2003. IEEE Topical Conference on*, pp. 241 – 243, 2003. 2

[7] T. Paing, J. Morroni, A. Dolgov, J. Shin, J. Brannan, R. Zane, and Z. Popovic, "Wirelessly-powered wireless sensor platform," in *Microwave Conference, 2007. European*, pp. 999 –1002, 2007. 2, 6, 12, 20, 140, 141

[8] C. Walsh, S. Rondineau, M. Jankovic, G. Zhao, and Z. Popovic, "A conformal 10 GHz rectenna for wireless powering of piezoelectric sensor electronics," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, p. 4 pp., 2005. 2

[9] W. Brown, "The history of power transmission by radio waves," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, pp. 1230 – 1242, Sept. 1984. 2

[10] N. Shinohara and H. Matsumoto, "Experimental study of large rectenna array for microwave energy transmission," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 261 –268, Mar. 1998. 2, 3, 70

[11] J. McSpadden, F. Little, M. Duke, and A. Ignatiev, "An in-space wireless energy transmission experiment," in *Energy Conversion Engineering Conference, 1996. IECEC 96. Proceedings of the 31st Intersociety*, vol. 1, pp. 468 –473 vol.1, Aug. 1996. 2

[12] L. Epp, A. Khan, H. Smith, and R. Smith, "A compact dual-polarized 8.51-ghz rectenna for high-voltage (50 v) actuator applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, pp. 111 –120, Jan. 2000. 2

[13] Y. Fujino, T. Ito, M. Fujita, N. Kaya, H. Matsumoto, K. Kawabata, H. Sawada, and T. Onodera, "A driving test of a small dc motor with a rectenna array," *Communications, IEICE Transactions on*, vol. E77-B, pp. 526 –528, Apr. 1994. 2

[14] R. Dickinson, "Performance of a high-power, 2.388-ghz receiving array in wireless power transmission over 1.54 km," in *Microwave Symposium, 1976 IEEE-MTT-S International*, pp. 139 –141, june 1976. 2

[15] W. Brown, "An experimental low power density rectenna," in *Microwave Symposium Digest, 1991., IEEE MTT-S International*, pp. 197 –200 vol.1, July 1991. 3, 4, 7, 8, 150

[16] J. Hagerty, F. Helmbrecht, W. McCalpin, R. Zane, and Z. Popovic, "Recycling ambient microwave energy with broad-band rectenna arrays," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 3, pp. 1014 – 1024, 2004. 4, 7, 8, 15, 17, 106, 151, 156

[17] K. Finkenzeller, "Rfid handbook - fundamentals and applications in contactless smart cards and identification," 2003. 5

[18] D. M. Dobkin, "The rf in rfid: Passive uhf rfid in practice," 2007. 5

[19] U. Olgun, C.-C. Chen, and J. Volakis, "Wireless power harvesting with planar rectennas for 2.45 ghz rfids," in *Electromagnetic Theory (EMTS), 2010 URSI International Symposium on*, pp. 329 –331, aug. 2010. 5

[20] A. Douyere, F. Alicalapa, J.-D. Lan Sun Luk, and A. Celeste, "Losses analysis and performance improvement of a rectenna for rfid systems," in *Electronics, Circuits and Systems, 2008. ICECS 2008. 15th IEEE International Conference on*, pp. 1083 –1086, 31 2008-sept. 3 2008. 5

[21] V. Rizzoli, D. Masotti, N. Arbizzani, and A. Costanzo, "Cad procedure for predicting the energy received by wireless scavenging systems in the near- and far-field regions," in *Microwave Symposium Digest (MTT), 2010 IEEE MTT-S International*, pp. 1768 –1771, May 2010. 5

[22] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Soljacic, "Wireless power transfer via strongly coupled magnetic resonances.," *Science*, vol. 317, no. 5834, pp. 83–86, 2007. 5

[23] J. McSpadden, L. Fan, and K. Chang, "Design and experiments of a high-

conversion-efficiency 5.8-ghz rectenna," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 2053 –2060, Dec. 1998. 6, 7, 17, 27, 107

[24] B. Strassner and K. Chang, "5.8 ghz circular polarized rectenna for microwave power transmission," in *Energy Conversion Engineering Conference and Exhibit, 2000. (IECEC) 35th Intersociety*, vol. 2, pp. 1458 –1468 vol.2, 2000. 6, 7

[25] J. Zbitou, M. Latrach, and S. Toutain, "Hybrid rectenna and monolithic integrated zero-bias microwave rectifier," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 1, pp. 147 –152, 2006. 6, 7

[26] J. Akkermans, M. van Beurden, G. Doodeman, and H. Visser, "Analytical models for low-power rectenna design," *Antennas and Wireless Propagation Letters, IEEE*, vol. 4, pp. 187 – 190, 2005. 6, 7

[27] G. Vera, A. Georgiadis, A. Collado, and S. Via, "Design of a 2.45 ghz rectenna for electromagnetic (em) energy scavenging," in *Radio and Wireless Symposium (RWS), 2010 IEEE*, pp. 61 –64, 2010. 6, 7, 97, 116, 140, 141, 147

[28] J. Heikkinen, P. Salonen, and M. Kivikoski, "Planar rectennas for 2.45 ghz wireless power transfer," in *Radio and Wireless Conference, 2000. RAWCON 2000. 2000 IEEE*, pp. 63 –66, 2000. 7, 8

[29] H. Takhedmit, B. Merabet, L. Cirio, B. Allard, F. Costa, C. Vollaire, and O. Picon, "A 2.45-ghz low cost and efficient rectenna," in *Antennas and Propagation (EuCAP), 2010 Proceedings of the Fourth European Conference on*, pp. 1 –5, 2010. 7, 8, 96

[30] Y. Hiramatsu, T. Yamamoto, K. Fujimori, M. Sanagi, and S. Nogi, "The design of mw-class compact size rectenna using sharp directional antenna," in *Microwave Conference, 2009. EuMC 2009. European*, pp. 1243 –1246, 29 2009-oct. 1 2009. 6, 7

[31] A. Mainwaring, D. Culler, J. Polastre, R. Szewczyk, and J. Anderson, "Wireless sensor networks for habitat monitoring," in *Proceedings of the 1st ACM international workshop on Wireless sensor networks and applications*, WSNA '02, (New York, NY, USA), pp. 88–97, ACM, 2002. 12

[32] K. Lorincz, M. Welsh, O. Marcillo, J. Johnson, M. Ruiz, and J. Lees, "Deploying a wireless sensor network on an active volcano," in *IEEE Internet Computing*, pp. 18–25, 2006. 12

[33] C. Walsh, S. Rondineau, M. Jankovic, G. Zhao, and Z. Popovic, "A conformal 10 ghz rectenna for wireless powering of piezoelectric sensor electronics," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, p. 4 pp., 2005. 12

[34] R.-G. Lee, K.-C. Chen, S.-S. Chiang, C.-C. Lai, H.-S. Liu, and M.-S. Wei, "A backup routing with wireless sensor network for bridge monitoring system," in *Communication Networks and Services Research Conference, 2006. CNSR 2006. Proceedings of the 4th Annual*, pp. 5 pp. –161, may 2006. 12

[35] F. Flammini, A. Gaglione, F. Ottello, A. Pappalardo, C. Pragliola, and A. Tedesco, "Towards wireless sensor networks for railway infrastructure monitoring," in *Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS), 2010*, pp. 1 –6, oct. 2010. 12

[36] S. Sudevalayam and P. Kulkarni, "Energy harvesting sensor nodes: Survey and implications," *Communications Surveys Tutorials, IEEE*, vol. 13, pp. 443 –461, quarter 2011. 12

[37] P. Glatz, L. Hormann, C. Steger, and R. Weiss, "Designing sustainable wireless sensor networks with efficient energy harvesting systems," in *Wireless Communications and Networking Conference (WCNC), 2011 IEEE*, pp. 2018 –2023, march 2011. 12

[38] Y. K. Tan and S. Panda, "Optimized wind energy harvesting system using resistance emulator and active rectifier for wireless sensor nodes," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 38 –50, jan. 2011. 12

[39] S. Sasaki and K. Tanaka, "Wireless power transmission technologies for solar power satellite," in *Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications (IMWS), 2011 IEEE MTT-S International*, pp. 3 –6, may 2011. 12

[40] Y. K. Tan and S. K. Panda, "Review of energy harvesting technologies for sustainable wireless sensor network," *Sustainable Wireless Sensor Networks*, no. February, pp. 15–44, 2003. 12, 14

[41] V. Raghunathan, A. Kansal, J. Hsu, J. Friedman, and M. Srivastava, "Design considerations for solar energy harvesting wireless embedded systems," in *Information Processing in Sensor Networks, 2005. IPSN 2005. Fourth International Symposium on*, pp. 457 – 462, april 2005. 13

[42] G. Yi, S. Guiling, L. Weixiang, and P. Yong, "Wireless sensor node design based on solar energy supply," in *Power Electronics and Intelligent Transportation System (PEITS), 2009 2nd International Conference on*, vol. 3, pp. 203 –207, dec. 2009. 13

[43] F. Simjee and P. Chou, "Efficient charging of supercapacitors for extended lifetime of wireless sensor nodes," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 1526 –1536, may 2008. 13

[44] Cymbet Corporation, "CBC-EVAL-09, EnerChip EP Universal Energy Harvester Eval Kit." online, January 2011. http://www.cymbet.com/pdfs/DS-72-13.pdf. 13, 147

[45] S. Muyeen, R. Takahashi, T. Murata, and J. Tamura, "A variable speed wind turbine control strategy to meet wind farm grid code requirements," *Power Systems, IEEE Transactions on*, vol. 25, pp. 331 –340, feb. 2010. 14

[46] M. Weimer, T. Paing, and R. Zane, "Remote area wind energy harvesting for low-power autonomous sensors," in *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pp. 1 – 5, june 2006. 14

[47] R. Myers, M. Vickers, H. Kim, and S. Priya, "Small scale windmill," *Applied Physics Letters*, vol. 90, pp. 054106 –054106–3, jan 2007. 14

[48] Y. K. Tan and S. Panda, "Self-autonomous wireless sensor nodes with wind energy harvesting for remote sensing of wind-driven wildfire spread," *Instrumentation and Measurement, IEEE Transactions on*, vol. 60, pp. 1367 –1377, april 2011. 14

[49] J. Xie, C. Lee, and H. Feng, "Design, fabrication, and characterization of cmos mems-based thermoelectric power generators," *Microelectromechanical Systems, Journal of*, vol. 19, pp. 317 –324, april 2010. 14

[50] H. Bottner, J. Nurnus, A. Gavrikov, G. Kuhner, M. Jagle, C. Kunzel, D. Eberhard, G. Plescher, A. Schubert, and K.-H. Schlereth, "New thermoelectric components using microsystem technologies," *Microelectromechanical Systems, Journal of*, vol. 13, pp. 414 – 420, june 2004. 15

[51] S. Pobering and N. Schwesinger, "Power supply for wireless sensor systems," in *Sensors, 2008 IEEE*, pp. 685 –688, oct. 2008. 15

[52] G. Orecchini, L. Yang, M. Tentzeris, and L. Roselli, "Smart shoe; an autonomous inkjet-printed rfid system scavenging walking energy," in *Antennas and Propagation (APSURSI), 2011 IEEE International Symposium on*, pp. 1417 –1420, july 2011. 15

[53] T. Starner, "Human-powered wearable computing," *IBM Systems Journal*, vol. 35, no. 3.4, pp. 618 –629, 1996. 15

[54] T. Paing, J. Morroni, A. Dolgov, J. Shin, J. Brannan, R. Zane, and Z. Popovic, "Wirelessly-powered wireless sensor platform," in *Wireless Technologies, 2007 European Conference on*, pp. 241 –244, 2007. 17, 104, 116, 145

[55] Rogers corporation, "RO4000 Series High Frequency Circuit Materials." online, Publication 92-004, May 2010.

http://www.rogerscorp.com/documents/726/acm/RO4000-Laminates—Data-sheet.aspx. 18, 68, 117, 118

[56] Skyworks, "SMS7630 series, Mixer and Detector Schottky Diodes." online, accessed 2/21/09, January 2010. http://www.skyworksinc.com/uploads/documents/200041U.pdf. 18, 42, 54, 55, 59, 64, 77, 119, 121

[57] Cymbet Corporation, "Rechargeable Solid State Energy Storage: $50\mu Ah$,$3.8V$." online, January 2009. http://www.cymbet.com/pdfs/DS-72-01.pdf. 19, 154

[58] D. Costinett, E. Falkenstein, R. Zane, and Z. Popovic, "Rf-powered variable duty cycle wireless sensor," in *Microwave Conference (EuMC), 2010 European*, pp. 41 –44, 2010. 20, 22, 25, 70, 104, 107, 133, 146, 150, 159

[59] E. Falkenstein, D. Costinett, R. Zane, and Z. Popovic, "Far-field rf-powered variable duty cycle wireless sensor platform," *Circuits and Systems II, IEEE Transactions on*, vol. Accepted, Submitted August 2011. 25, 146, 159

[60] T. Paing, E. Falkenstein, R. Zane, and Z. Popovic, "Custom ic for ultra-low power rf energy harvesting," in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pp. 1239 –1245, 2009. 25, 104, 159

[61] T. Paing, E. Falkenstein, R. Zane, and Z. Popovic, "Custom ic for ultralow power rf energy scavenging," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 1620 –1626, june 2011. 25, 104, 151, 159

[62] L. Clare and S. Burrow, "Half-wave rectifiers offer advantages for vibration energy harvesters," *Electronics Letters*, vol. 46, pp. 1623 –1624, 25 2010. 26

[63] S. Imai, S. Tamaru, K. Fujimori, M. Sanagi, and S. Nogi, "Efficiency and harmonics generation in microwave to dc conversion circuits of half-wave and

full-wave rectifier types," in *Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications (IMWS), 2011 IEEE MTT-S International*, pp. 15 –18, may 2011. 26, 83

[64] A. Dolgov, R. Zane, and Z. Popovic, "Power management system for online low power rf energy harvesting optimization," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 57, no. 7, pp. 1802 –1811, 2010. 33, 104, 133, 151

[65] Modelithics, Inc., "Surface Mount Schottky Diode Model, Skyworks SMS7621-079 Schottky Diode, SC79 Package." Modelithics COMPLETE v7.0 Help File, Rev. 050302, 2005. 37, 64, 70

[66] W. Yuan, J. Song, C. Zhongjian, and J. Lijiu, "Full parasitic capacitance model of diode-class esd protection structures for mix-signal and rf ics," in *Electron Devices and Solid-State Circuits, 2005 IEEE Conference on*, pp. 515 – 518, dec. 2005. 38

[67] R. W. Vogel, "Microwave on-wafer characterization and modelling of schottky barrier diodes," in *Microwave Conference, 1990. 20th European*, vol. 1, pp. 766 –771, sept. 1990. 39

[68] D. Salameh and D. Linton, "Study of the relation between doping profile and diode cv characteristics," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 47, pp. 506 –509, apr 1999. 41

[69] S. Pendharkar, C. Winterhalter, and K. Shenai, "A behavioral circuit simulation model for high-power gaas schottky diodes," *Electron Devices, IEEE Transactions on*, vol. 42, pp. 1847 – 1854, oct 1995. 43

[70] T.-W. Yoo and K. Chang, "Theoretical and experimental development of 10 and 35 ghz rectennas," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 40, pp. 1259 –1266, June 1992. 47

[71] S. Cripps, "Rf power amplifiers for wireless communications," 2006. 49, 52, 53, 56

[72] A. W. A.V. Oppenheim, "Signals and systems, englewood cliffs, new jersey, 1983," *Cytometry*, vol. 6, no. 4, pp. 392–392, 1985. 51

[73] A. V. Oppenheim, R. W. Schafer, and J. R. Buck, *Discrete Time Signal Processing*, vol. 1999. Prentice Hall. 51

[74] D. Prince, "Mathematical treatment of rectification phenomena," *Proceedings of the Institute of Radio Engineers*, vol. 10, pp. 393 – 398, oct. 1922. 51

[75] N. Sokal, "Rf power amplifiers, classes a through s-how they operate, and when to use each," in *Electronics Industries Forum of New England, 1997. Professional Program Proceedings*, pp. 179 –252, may 1997. 51, 52

[76] H. Roder, "A simple method of harmonic analysis for use in radio engineering practice," *Proceedings of the Institute of Radio Engineers*, vol. 19, pp. 1481 – 1487, aug. 1931. 51

[77] J. Hallman, L.B., "A fourier analysis of radio-frequency power amplifier wave forms," *Proceedings of the Institute of Radio Engineers*, vol. 20, pp. 1640 – 1659, oct. 1932. 52, 56

[78] F. Raab, "Class-e, class-c, and class-f power amplifiers based upon a finite number of harmonics," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, pp. 1462 –1468, aug 2001. 52

[79] W. Nitz, W. Bowman, F. Dickens, F. Magalhaes, W. Strauss, W. Suiter, and N. Ziesse, "A new family of resonant rectifier circuits for high frequency dc-dc converter applications," in *Applied Power Electronics Conference and Exposition, 1988. APEC '88. Conference Proceedings 1988., Third Annual IEEE*, pp. 12 –22, feb 1988. 52

[80] J. A. Hagerty, "Nonlinear circuits and antennas for microwave energy conversion," *Thesis*, pp. 1–165, 2003. 52

[81] S. Goto, T. Kunii, A. Ohta, A. Inoue, Y. Hosokawa, R. Hattori, and Y. Mitsui, "Effect of bias condition and input harmonic termination on high efficiency inverse class-f amplifiers," in *Microwave Conference, 2001. 31st European*, pp. 1 –4, sept. 2001. 55

[82] A. Inoue, T. Heima, A. Ohta, R. Hattori, and Y. Mitsui, "Analysis of class-f and inverse class-f amplifiers," in *Microwave Symposium Digest. 2000 IEEE MTT-S International*, vol. 2, pp. 775 –778 vol.2, 2000. 55

[83] F. Terman and J. Ferns, "The calculation of class c amplifier and harmonic generator performance of screen-grid and similar tubes," *Proceedings of the Institute of Radio Engineers*, vol. 22, pp. 359 –373, march 1934. 56

[84] E. Falkenstein, M. Roberg, and Z. Popovic, "Low-power wireless power delivery," *Microwave Theory and Techniques, IEEE Transactions on*, vol. Under review, Submitted October 2011. 61, 81, 113, 159, 160

[85] M. Roberg, E. Falkenstien, and Z. Popovic, "High-efficiency harmonically-terminated half-wave microwave rectifiers," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, To be submitted. 61, 81, 159, 160

[86] V. Camarchia, V. Teppati, S. Corbellini, and M. Pirola, "Microwave measurements part ii non-linear measurements," *Instrumentation Measurement Magazine, IEEE*, vol. 10, pp. 34 –39, june 2007. 65

[87] J. Hoversten, M. Roberg, and Z. Popovicť and, "Harmonic load pull of high-power microwave devices using fundamental-only load pull tuners," in *Microwave Measurements Conference (ARFTG), 2010 75th ARFTG*, pp. 1 –4, may 2010. 65

[88] G. Engen and C. Hoer, "Thru-reflect-line: An improved technique for cali-

brating the dual six-port automatic network analyzer," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 27, pp. 987 – 993, dec 1979. 65

[89] N. Shinohara and H. Matsumoto, "Dependence of dc output of a rectenna array on the method of interconnection of its array elements," *Electrical Engineering in Japan*, vol. 125, no. 1, pp. 9–17, 1998. 70

[90] T. Paing, J. Shin, R. Zane, and Z. Popovic, "Resistor emulation approach to low-power rf energy harvesting," *Power Electronics, IEEE Transactions on*, vol. 23, pp. 1494 –1501, may 2008. 70, 104

[91] S. Maas, *Nonlinear microwave and RF circuits*. Microwave Library, Artech House, 2003. 71

[92] E. Holzman and R. Robertson, *Solid-State Microwave Power Oscillator Design*. Artech House Microwave Library, Books on Demand, 1992. 71

[93] G. Xuebang, "Large-signal s-parameters simulation of microwave power circuits," in *Microwave and Millimeter Wave Technology Proceedings, 1998. ICMMT '98. 1998 International Conference on*, pp. 1061 –1063, 1998. 77

[94] Agilent Technologies, "Large-Signal S-Parameters Simulation," September 2006. http://cp.literature.agilent.com/litweb/pdf/ads2006/pdf/cktsimlssp.pdf. 77

[95] D. H. Li and K. Li, "A novel high-efficiency rectenna for 35ghz wireless power transmission," in *Microwave and Millimeter Wave Technology, 2004. ICMMT 4th International Conference on, Proceedings*, pp. 114 – 117, 2004. 83

[96] H. Takhedmit, B. Merabet, L. Cirio, B. Allard, F. Costa, C. Vollaire, and O. Picon, "A 2.45-ghz dual-diode rf-to-dc rectifier for rectenna applications," in *Microwave Conference (EuMC), 2010 European*, pp. 37 –40, sept. 2010. 83

[97] R. Beatty, "Insertion loss concepts," *Proceedings of the IEEE*, vol. 52, pp. 663 – 671, june 1964. 83

[98] D. Pinchera and M. Migliore, "A technique for the extraction of the connector response in adaptive parasitic antenna arrays," in *Microwave Conference, 2009. EuMC 2009. European*, pp. 1334 –1337, 29 2009-oct. 1 2009. 84

[99] M. Manteghi, "Analytical calculation of impedance matching for probe-fed microstrip patch antennas," *Antennas and Propagation, IEEE Transactions on*, vol. 57, pp. 3972 –3975, dec. 2009. 84

[100] P. Haskins and J. Dahele, "Capacitive coupling to patch antenna by means of modified coaxial connectors," *Electronics Letters*, vol. 34, pp. 2187 –2188, nov 1998. 84

[101] T. Masri, M. K. A. Rahim, M. H. Jamaluddin, and A. Asrokin, "Bandwidth enhancement of a narrowband rectangular microstrip antenna on a spiral fan-shape electromagnetic band-gap (ebg) patch structure," in *RF and Microwave Conference, 2006. RFM 2006. International*, pp. 225 –227, sept. 2006. 88

[102] A. Mohammad, H. Subhi, A. Ahmad, and S. Juma, "Bandwidth enhancement of stacked rectangular microstrip patch antenna," in *Antennas, Propagation EM Theory, 2006. ISAPE '06. 7th International Symposium on*, pp. 1 –13, oct. 2006. 88

[103] H.-K. Chiou and I.-S. Chen, "High-efficiency dual-band on-chip rectenna for 35- and 94-ghz wireless power transmission in 0.13-*muhboxm* cmos technology," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, pp. 3598 –3606, dec. 2010. 96

[104] H. Takhedmit, B. Merabet, L. Cirio, B. Allard, F. Costa, C. Vollaire, and O. Picon, "A 2.45-ghz low cost and efficient rectenna," in *Antennas and Propagation (EuCAP), 2010 Proceedings of the Fourth European Conference on*, pp. 1 –5, 2010. 106

[105] C.-H. Chin, Q. Xue, and C. H. Chan, "Design of a 5.8-ghz rectenna incorporating a new patch antenna," *Antennas and Wireless Propagation Letters, IEEE*, 2005. 106

[106] H.-K. Chiou and I.-S. Chen, "High-efficiency dual-band on-chip rectenna for 35- and 94-ghz wireless power transmission in 0.13-*muhboxm* cmos technology," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 58, no. 12, pp. 3598 –3606, 2010. 106

[107] Y. Hiramatsu, T. Yamamoto, K. Fujimori, M. Sanagi, and S. Nogi, "The design of mw-class compact size rectenna using sharp directional antenna," in *Microwave Conference, 2009. EuMC 2009. European*, 29 2009. 106

[108] E. Falkenstein and Z. Popovic, "Dc power pattern of rectifier-antennas," in *General Assembly and Scientific Symposium, 2011 XXXth URSI*, pp. 1 –4, aug. 2011. 113, 160

[109] E. Falkenstein and Z. Popovic, "Rectifying antenna design method for wireless powering applications," in *Proceedings of the USNC/URSI National Radio Science Meeting*, (Boulder, USA), Jan. 2010. 113, 160

[110] A. Manikas and J. Ng, "Crossed-dipole arrays for asynchronous ds-cdma systems," *Antennas and Propagation, IEEE Transactions on*, vol. 52, pp. 122 – 131, jan. 2004. 115

[111] T. Manabe, K. Sato, H. Masuzawa, K. Taira, T. Ihara, Y. Kasashima, and K. Yamaki, "Polarization dependence of multipath propagation and high-speed transmission characteristics of indoor millimeter-wave channel at 60 ghz," *Vehicular Technology, IEEE Transactions on*, vol. 44, pp. 268 –274, may 1995. 115

[112] D. Cox, R. Murray, H. Arnold, A. Norris, and M. Wazowicz, "Cross-polarization coupling measured for 800 mhz radio transmission in and around houses and large buildings," *Antennas and Propagation, IEEE Transactions on*, vol. 34, pp. 83 – 87, jan 1986. 115

[113] C. A. Balanis, *Antenna theory : analysis and design / Constantine A. Balanis.* J. Wiley, New York ; Brisbane :, 1982. 115

[114] A. Georgiadis, G. Andia, and A. Collado, "Rectenna design and optimization using reciprocity theory and harmonic balance analysis for electromagnetic (em) energy harvesting," *Antennas and Wireless Propagation Letters, IEEE*, vol. 9, pp. 444 –446, 2010. 116, 140, 141

[115] Z. Harouni, L. Cirio, L. Osman, A. Gharsallah, and O. Picon, "A dual circularly polarized 2.45-ghz rectenna for wireless power transmission," *Antennas and Wireless Propagation Letters, IEEE*, vol. 10, pp. 306 –309, 2011. 116

[116] D.-G. Youn, K.-H. Kim, Y.-C. Rhee, S.-T. Kim, and C.-C. Shin, "Experimental development of 2.45ghz rectenna using fss and dual-polarization," in *Microwave Conference, 2000. 30th European*, pp. 1 –4, oct. 2000. 116, 136

[117] Rogers corporation, "RT/duroid 5870/5880 High Frequency Laminates." online, Publication 92-101, March 2011. http://www.rogerscorp.com/documents/606/acm/RT-duroid-5870-5880-Data-Sheet.aspx. 116

[118] K. Woelder and J. Granholm, "Cross-polarization and sidelobe suppression in dual linear polarization antenna arrays," *Antennas and Propagation, IEEE Transactions on*, vol. 45, pp. 1727 –1740, dec 1997. 126

[119] T. Au and K. Luk, "Effect of parasitic element on the characteristics of microstrip antenna," *Antennas and Propagation, IEEE Transactions on*, vol. 39, pp. 1247 –1251, aug 1991. 128

[120] J. Granholm and K. Woelders, "Dual polarization stacked microstrip patch antenna array with very low cross-polarization," *Antennas and Propagation, IEEE Transactions on*, vol. 49, pp. 1393 –1402, oct 2001. 128

[121] Powercast Corporation, "Powercast Corporation Home page." online, accessed 1/08/11, January 2009. http://www.powercastco.com/. 145

[122] Sierra Nevada Corporation, "Sierra Nevada Corporation Home page." online, accessed 1/08/11, January 2011. http://www.spacedev.com/colorado.php. 146

[123] Masco Home Services, Inc, "Environments For Living Home." online, accessed 1/08/11, January 2011. http://www.environmentsforliving.com/EFLPublicSite/index.jsp. 146

[124] Coleman Institute for Cognitive Disabilities, "Coleman Institute for Cognitive Disabilities, University of Colorado." online, accessed 1/08/11, January 2005. http://www.colemaninstitute.org/. 147

[125] Cymbet Corporation, "Cymbet Corporation home page." online, January 2011. http://www.cymbet.com. 147, 153

[126] U. Olgun, C.-C. Chen, and J. Volakis, "Wireless power harvesting with planar rectennas for 2.45 ghz rfids," in *Electromagnetic Theory (EMTS), 2010 URSI International Symposium on*, pp. 329 –331, 2010. 147

[127] M. Roberg, E. Falkenstien, and Z. Popovic, "High-efficiency harmonically-terminated half-wave microwave rectifiers," in *Microwave Symposium Digest (MTT), 2012 IEEE MTT-S International*, To be submitted. 149, 156

[128] K. Bossert, E. Falkenstein, and Z. Popovic, "Slot rectifier antennas for low-power applications," in *Proceedings of the USNC/URSI National Radio Science Meeting*, (Boulder, USA), Jan. 2010. 150

[129] Infinite Power Solutions, Inc, "THINERGY Micro-Energy Cells." online, January 2010. http://www.infinitepowersolutions.com/products/thinergy. 153, 154

[130] Texas Instruments Incorporated, "Single Chip Very Low Power RF Transceiver with 8051-Compatible Microcontroller." online, January 2009. http://www.ti.com/lit/ds/symlink/cc1010.pdf. 154

[131] Crystek Corporation, "Crystek Oscillator, VCO, CVCO55BE-1650-2150." online, accessed 2/21/09, January 2008. http://www.alliedelec.com/Images/Products/Datasheets/BM/CRYSTEK/393-0038.PDF. 178

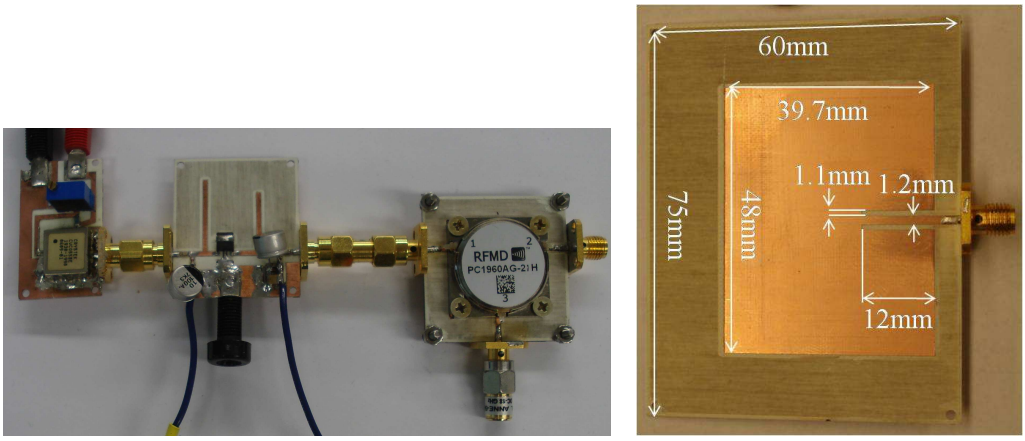
[132] RF MICRO DEVICES, "RFMD, FPD3000SOT89 Low noise high linearity packaged pHEMT." online, accessed 2/21/09, January 2007. http://www.rfmd.com/CS/Documents/FPD3000SOT89DS.pdf. 179

[133] RF MICRO DEVICES, "RFMD, 1930MHz to 1990MHz single junction drop-in circulator." online, accessed 2/21/09, January 2006. http://www.rfmd.com/CS/Documents/PC1960AG-21HDS.pdf. 179

Appendix I

Efficient Low Cost Transmitter

An example of a low cost transmitter made with mostly off-the-shelf parts is given in below for 1.96 GHz, similar parts are available for the 2.45 GHz ISM band. Assuming two general DC power supplies, the transmitter consists of an oscillator, amplifier, circulator and an antenna 7.9. The specifications are as follows:



(a) (b)

Figure 7.9: The powering chain composed of a VCO, amplifier and circulator (a) and patch antenna(b).

- VCO - CVCO55BE-1650-2150 with 5 dBm output power (26$) [131]

- Amplifier - RFMD FPD3000SOT89 low-noise high-linearity packaged pHEMPT presented with input impedance of $4 - j0.4\,\Omega$ and an output impedance of $13.2 - j2.5\Omega$. The circuit is fabricated on Rogers $4350b$ 30 mil thick. (15$) [132]

- Circulator - PC1960AG-21H 1930 MHz TO 1990 MHz single junction drop in circulator. (100$) [133]

- Antenna - a patch antenna with indented feed was designed using ADS Momentum and is fabricated on Rogers 4350b.

Sample measured data of the amplifier is given in Fig. 7.10.

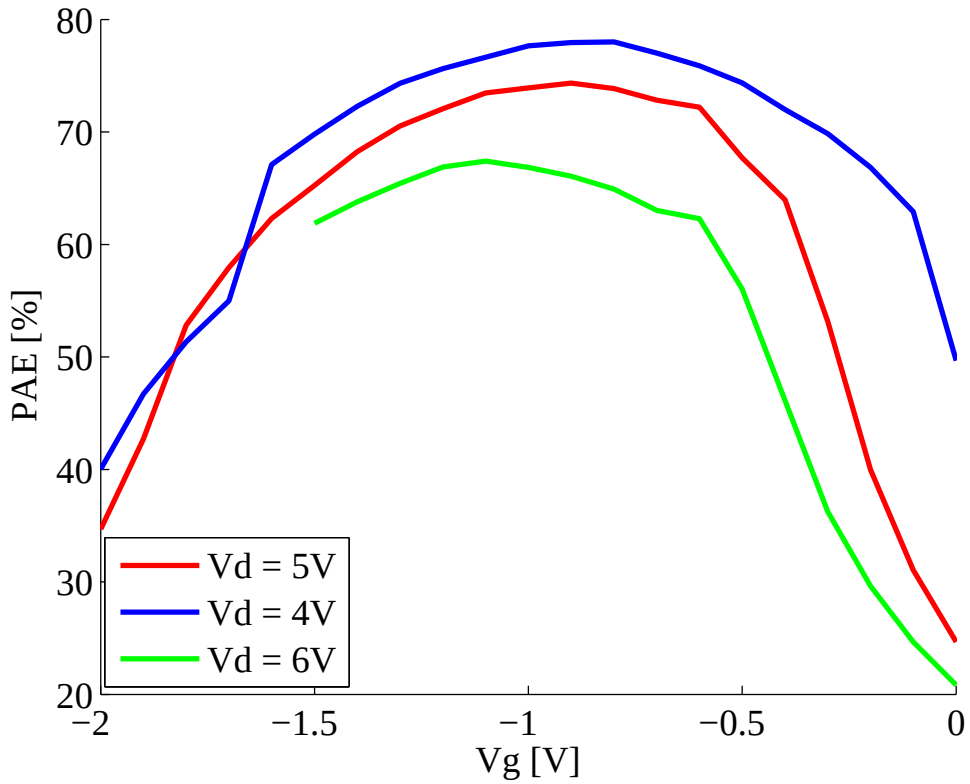


Figure 7.10: Measured Power added efficiency for the amplifier described above for different biasing voltages at 1.96GHz and input power of 18 dBm.