

DESIGN AND IMPLEMENTATION OF MICROWAVE VCOs FOR CHIP-SCALE
ATOMIC CLOCKS

by

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Local Oscillators in Chip-Scale Atomic Clocks

Thesis directed by Professor Zoya Popović

This work is focused on the design and implementation of miniature, low-power, and low-phase-noise voltage-controlled oscillators for miniature atomic clocks. The aim is to enable new high-performance atomic clocks with a small fraction of the size and power consumption of existing commercial clocks. Such devices have applications in handheld GPS receivers as well as military and commercial communications and wherever stable and battery-operated time synchronization of autonomous devices is required. A new design approach combining harmonic balance and the two-port method for optimizing the loaded Q factor of oscillators is shown to result in a design with the best combination of small size, low phase noise, and low power consumption among those previously reported in literature or commercially-available.

This thesis presents the first reported integration of microwave oscillators with the MEMS-based physics package of a chip-scale atomic clock. Two prototype chip-scale atomic clocks have been demonstrated in collaboration with NIST and show the viability of battery-operated atomic frequency references with a size on the order of one cubic centimeter.

Another contribution of this thesis is the demonstration and accurate simulation of a new type of lock to the atomic hyperfine resonance, resulting in improved phase noise, improved short-term stability, and a faster lock to the

atomic hyperfine transition. This is also the first demonstration of oscillator self-injection locking through an atomic medium. The method is based on the generation of a high-contrast, coherent-population-trapping signal at 6.8 GHz with the use of atomic 4-wave mixing. This signal is then used to injection lock the oscillator at its second harmonic, permitting the above benefits as well as improved vibration sensitivity and good separation of the 6.8-GHz incoming and 3.4-GHz outgoing frequencies of the oscillator.

Dedication

To my parents.

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Soli Deo Gloria

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Chapter 1

1. Introduction and Background

1.1 Introduction

Atomic clocks can be thought of as electronic oscillators that maintain a very stable frequency by locking the oscillator frequency to stable and precise transitions between atomic energy levels. The first atomic clock was made in 1949 at the National Bureau of Standards (now NIST), and was based on the ammonia molecule(1). Since then, use of alkali atoms such as cesium and rubidium has become predominant in commercial(2),(3),(4) devices and research(5) continues today on these practical systems. Cesium-based frequency standards have been designed to have good stability and excellent accuracy. In fact, since 1967, the fundamental unit of time, the second, has been defined as the duration of 9,192,631,770 periods of the radiation corresponding

to the transition between the two hyperfine levels of the ground state of the cesium-133 atom(6).

The first small commercial atomic clocks(7), (8), (9) were based on techniques that required the microwave excitation of atoms directly. For high performance, the atoms were confined in a microwave cavity, which was large because of the microwave wavelength and, to some degree, to achieve high Q factors at the atomic resonant frequency. Most of the power consumption of such devices was used to run the rubidium lamp and for heating the atomic cell and other components. The advent of diode lasers with high modulation bandwidth made it possible to miniaturize atomic clocks by applying the microwave field as a modulation on the light field generated by the laser, thus eliminating the bulky cavity. This resulted in examples such as the commercially-available Kernco rubidium frequency standard(2) with size less than 300 cubic centimeters and power consumption at 3.5 W. It was believed that extreme miniaturization of atomic clocks was possible if microelectromechanical (MEMS) fabrication techniques could be used with advanced atomic interrogation techniques(10). The use of MEMS techniques allowed more than a factor of one hundred reduction in the size and power requirements for atomic clocks, mostly due to the creation of miniature atomic cells(11) that required less power for heating. This, combined with the mass production capabilities of wafer-level fabrication, has made possible many new applications for atomic clock technology. Several possible applications are given in(12),(13),(14),(15) including:

- Jam-resistant GPS receivers with fast acquisition time
- Accurate timekeeping and guidance in GPS-denied situations
- Friend-or-foe identification
- Improved secure communications such as frequency hopping
- Other systems requiring autonomous time synchronization

Because the technology was no longer limited by the size or power consumption of the atomic cell, more stringent requirements were placed on the microwave source. A new microwave oscillator was required to modulate the laser and to exhibit an unprecedented combination of small size, extremely low power consumption, and very low phase noise. This thesis presents the design, implementation, and performance of such oscillators, both as stand-alone components and in prototype chip-scale atomic clocks, proving the viability of the technology. In addition, a new method for stabilizing a microwave oscillator to an atomic clock transition is presented. The method is based on injection locking and atomic 4-wave mixing and provides a fast lock to the atomic resonance, resulting in improved phase noise, short-term stability, and vibration sensitivity.

1.2 Thesis Organization

This thesis is divided into seven chapters as outlined below:

- Section 1.3 reviews the Coherent Population Trapping (CPT) method and how this development enables the technology of chip-scale atomic clocks.
- Section 1.4 introduces the requirements for a local oscillator that is to be used in chip-scale atomic clocks. It is broken into several subsections devoted to size, power consumption, thermal drift, and phase noise.
- Section 1.5 describes the state of the art in oscillator design and how the subject of this thesis compares to existing methods and components.
- Chapter 2 develops the circuit selection process and the theoretical and experimental evaluation of chosen components.
- Chapter 3 describes the design of the oscillator at a circuit level. The unique benefits of a two-port feedback design are compared with more standard techniques of oscillator design.
- Chapter 4 presents the power consumption, phase noise, thermal frequency shift, and vibration sensitivity performance of the LO. This chapter concludes with examples of locking to an atomic “clock transition” in table-top experiments.
- Chapter 5 introduces the integration of the oscillator with the physics package and the control electronics in prototype chip-scale atomic clocks.

- Chapter 6 develops a new method for locking an oscillator to the atomic resonance, and presents experiments with the oscillator presented in previous chapters.
- Chapter 7 summarizes the contributions of this thesis and provides discussion of ongoing work and suggestions of future work.

1.3 Coherent Population Trapping in Atomic Clocks

When measured over long periods of time (minutes to years) atomic frequency references have been the most stable oscillators to date (16), (17), (18). Most early atomic clocks were very large in volume (on the order of 1 m^3), but there are some recent examples of smaller (on the order of 100 cm^3) commercially-available atomic clocks based on optical pumping (9), (19), (20), (4) and based on coherent population trapping (CPT) (2). This section describes briefly the atomic energy level structure, shows the benefits of CPT versus other techniques, and leads into the requirements for the local oscillator.

1.3.1 Atomic Energy Transitions

Alkali atoms tend to be used in atomic clocks because the outer shell has only one valence electron that is somewhat shielded from complex interactions with other electrons and the nucleus by the inner shells of electrons that are completely filled. The gas phase is preferred over solids since the energy levels are less perturbed by the environment. Finally, commercial diode lasers are

available for Rb, so for the remainder of this thesis, we will be concerned with isotope 87 of the Rubidium atom (^{87}Rb).

Figure 1 shows a part of the energy level diagram of ^{87}Rb . The lowest two energy levels in the coarse structure of the 5th shell are denoted 5S and 5P. The 5S state has angular momentum quantum number $L=0$ and the P state has angular momentum quantum number $L=1$. The levels are split into several sublevels (F1-F...). An electron can change level by absorbing or emitting a photon with an energy proportional to frequency by Planck's constant.

The coarse structure is split into a fine structure by the interaction of the electron's spin with the magnetic field due to the electron's orbital motion about the nucleus. This causes the P state to be split into the $P_{3/2}$ state and the $P_{1/2}$ state, named such because of the total angular momentum quantum number $J = |L \pm S|$ where $S=1/2$ is the quantum number of an electron. Notice that the lowest state ($5S_{1/2}$) has no fine structure splitting. In a classical analogy, this is because in the ground state, the electron has no orbital angular momentum ($L=0$), so there is no magnetic field for the electron spin to interact with. The two ground-state to excited-state transitions are shown in Figure 1 and are known as the D1 line and the D2 line, with associated optical wavelengths 795 nm and 780 nm, respectively.

The fine structure is again split into a hyperfine structure by the interaction of the spin of the electron with the spin of the nucleus. For ^{87}Rb , the quantum number for the spin of the nucleus is $I=3/2$. This is combined with J to form levels F , which are described by the integer combination between $I+J$ and $I-$

J, determined by the quantum mechanical rules of vector addition of angular momentum. Therefore, for the ground state hyperfine splitting, there are two levels, corresponding to $F = 1$ and $F = 2$. These levels are separated by 2.826598×10^{-5} eV, or 6.834683 GHz.

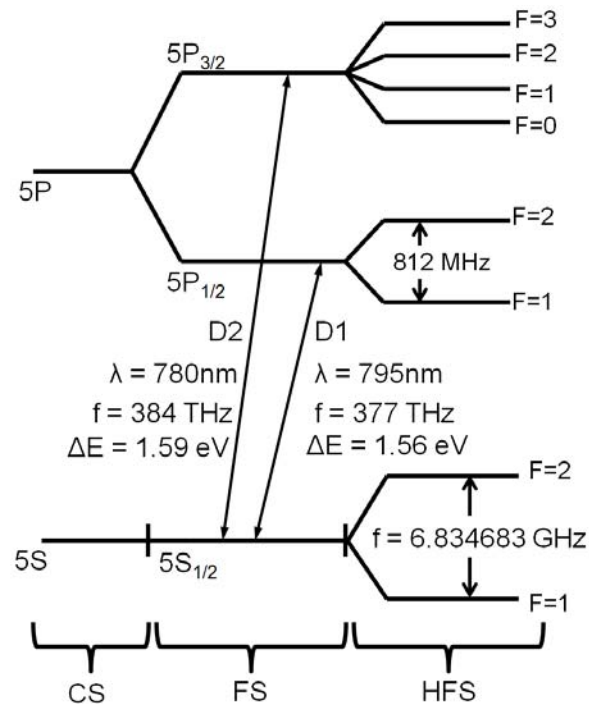


Figure 1 – Energy level diagram of the 5th electron shell of ⁸⁷Rb, showing only the ground-state and first excited-state transitions, including the fine-structure splitting between $5P_{3/2}$ and $5P_{1/2}$ and the hyperfine-structure splitting between different F values. CS stands for coarse splitting, HS for fine splitting, and HFS for hyperfine splitting.

Finally, as shown in Figure 2, the hyperfine structure is again split by the presence of externally-applied magnetic fields. The number of levels within each hyperfine level is determined by the integer number between (and including) F

and $-F$. To first order, the levels $m_F=0$ are insensitive to external magnetic fields and so these levels are used in atomic clocks. The transitions between an excited state and the ground state $F=1, m_F=0$ and $F=2, m_F=0$ levels are typically known as the “clock transitions”.

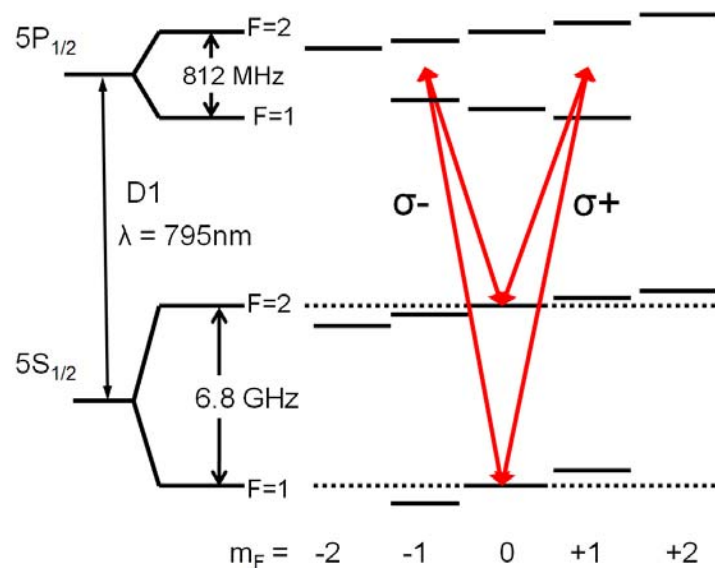


Figure 2 – Energy level diagram of the 5th shell of ^{87}Rb showing the magnetically-separated Zeeman levels. The optical transitions used in CPT atomic clocks use two photons to drive the transition between $F=2, m_F=0$ and $F=1, m_F=0$. These can be driven by either right- ($\sigma+$) or left- ($\sigma-$) circularly polarized light.

1.3.2 Optical Pumping

Past versions of miniature atomic clocks have used optical pumping (21) as the primary method for locking to the atomic clock transition since the method can result in microwave Q factors as high as 10^8 and those systems can reach fractional frequency instabilities on the order of $10^{-12}/\tau^{1/2}$. In that method, light (typically from a rubidium discharge lamp) is filtered (using ^{85}Rb) leaving light that causes a transition from a ground state to the excited state in ^{87}Rb (Figure 3 is using the D1 line). This excites atoms from state $|1\rangle$ to state $|2\rangle$. The atoms then decay quickly, and at approximately equal rate $\Gamma/2$, into either of the two ground states. However, because of the presence of the pumping light field, atoms accumulate in state $|2\rangle$. When this happens, the cell appears transparent because the atoms are no longer absorbing light. A microwave field from an oscillator, tuned to the ground-state hyperfine splitting frequency, is then applied and the atoms are pumped from state $|2\rangle$ to state $|1\rangle$. This is detected by a decrease in transmission of light through the cell. For high precision, these systems normally use a microwave cavity, which is typically several centimeters in length, to match the microwave wavelength. They also use a rubidium lamp, which must be heated to high temperatures. Furthermore, the lamp has a broad spectrum which requires an additional atomic vapor cell containing ^{85}Rb to absorb light falling on the $|2\rangle$ - $|3\rangle$ transition.

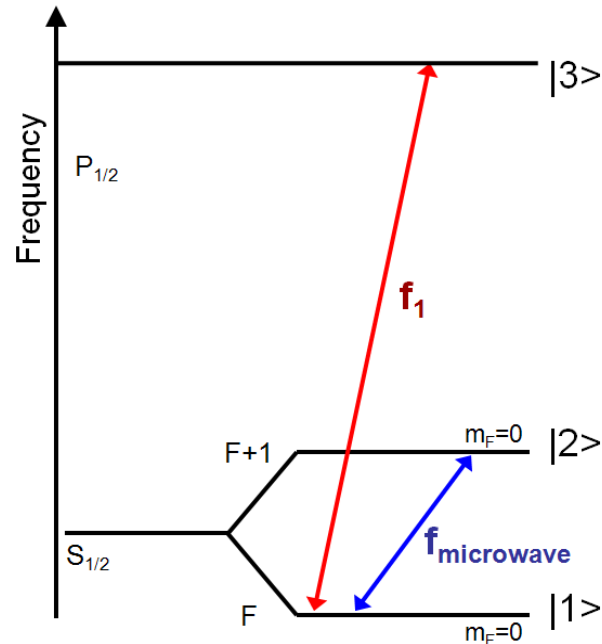


Figure 3 – Optical pumping energy level diagram. A microwave cavity is often used to probe the microwave resonance.

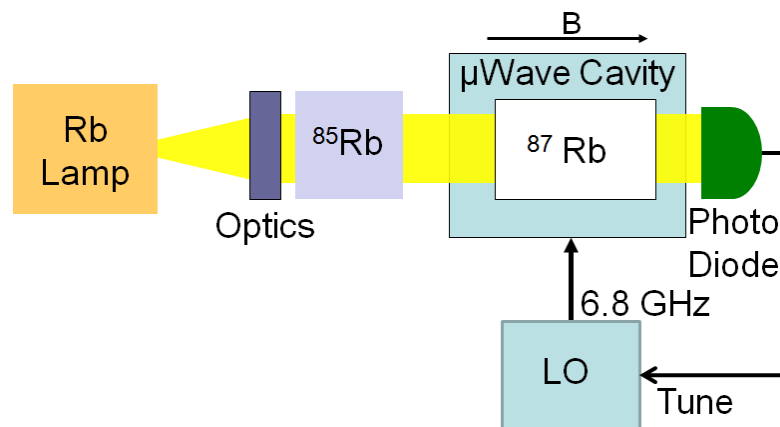


Figure 4 – Schematic used for optical pumping. The optics focus and polarize the light from the Rb lamp. The power consumption is dominated by the Rb lamp and by heating for temperature control of the system. The size is limited mostly by the Rb lamp and the microwave cavity.

1.3.3 Coherent Population Trapping

The first observation of coherent population trapping was made in 1976 by Alzetta (22) and was theoretically explained in the same year (23). For a review on CPT, see reference (24). In summary, the phenomenon can be seen as a destructive quantum interference that occurs when two light fields are applied, and each is resonant with an electric dipole transition of the atom. The configuration most applicable to our discussion is the Λ -system, named for the two light fields, depicted in Figure 5, that form the shape of the Greek letter Λ . In this method, one light beam with wavelength λ_1 is tuned to the transition between state $|3\rangle$ and state $|1\rangle$ and another light beam with wavelength λ_2 is tuned between state $|3\rangle$ and state $|2\rangle$. This causes a pumping that is similar to the optical pumping description of the previous section, but this time into a superposition of the two ground states that is coherent with the difference frequency of the light fields. The probability that the atom is in either state $|1\rangle$ or state $|2\rangle$ oscillates with a frequency that is equal to, but out of phase with, the beat frequency between the two optical fields. For simplification purposes, we can change the basis $\{|1\rangle, |2\rangle, |3\rangle\}$ into a new basis $\{|C\rangle, |NC\rangle, |3\rangle\}$ where $|C\rangle$ is the superposition of states $|1\rangle$ and $|2\rangle$ that is coupled to the light and $|NC\rangle$ is the superposition that is not coupled. These states are related as shown in formulas (1-1) and (1-2) below.

$$|C\rangle(t) \propto \Omega_1|1\rangle + \Omega_2 e^{-i\omega t + i\varphi}|2\rangle \quad (1-1)$$

$$|NC\rangle(t) \propto \Omega_2|1\rangle - \Omega_1 e^{-i\omega t + i\varphi}|2\rangle \quad (1-2)$$

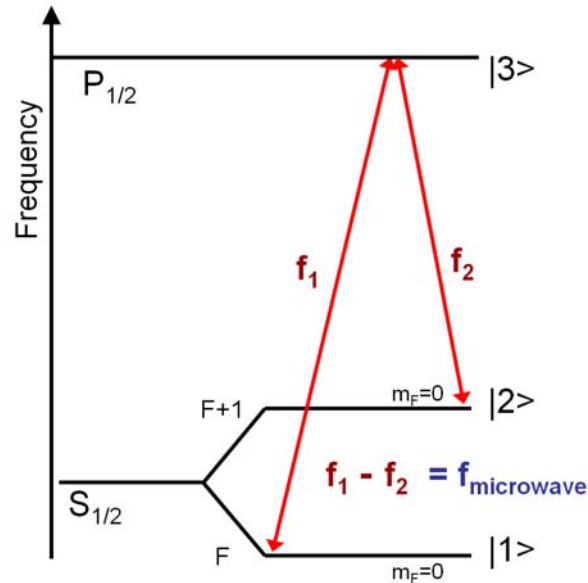


Figure 5 – Energy level diagram showing coherent population trapping. The microwave resonance is driven by the beat frequency between the two light fields.

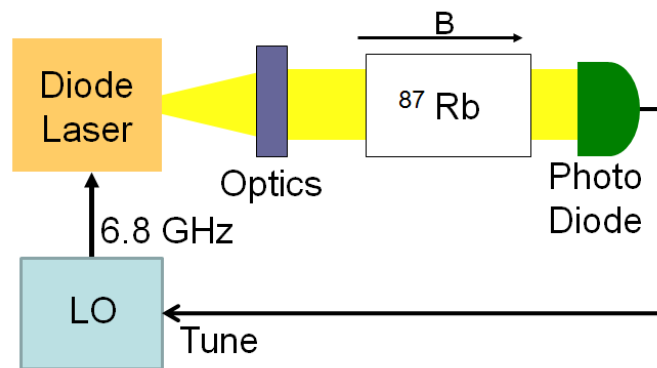


Figure 6 – Schematic diagram showing a CPT-based atomic clock. The optics focus and polarize the light. The Local Oscillator (LO) modulates the diode laser current directly, eliminating the need for the microwave cavity. This, combined with the use of a diode laser and MEMS fabrication techniques, enables an extremely small design.

Here, Ω_1 and Ω_2 are the Rabi frequencies, which are proportional to the intensity of the light. They determine the rate at which the atoms flop between the ground states and the excited state, and so they describe the strength of the interaction with the light. These two states are time-dependent and have a frequency ω (the ground-state hyperfine splitting frequency), and a phase φ . It can be shown that the probability of the light fields exciting an atom from the state $|NC\rangle$ is zero if the difference frequency of the light fields is tuned to the hyperfine splitting frequency and if the phase of the difference frequency is equal to the phase of state $|NC\rangle$. Therefore, this state $|NC\rangle$ is called the dark state because the atoms no longer absorb and re-emit light (i.e. they cease to fluoresce, appearing dark.) Because the orthogonal state $|C\rangle$ can be excited, the atoms are pumped into state $|NC\rangle$ much like in optical pumping experiments. Interestingly, this phenomenon depends more on the relative stability of the frequency difference between the light fields than on the frequency stability of the light fields themselves. The width of the CPT resonance is inversely proportional to the lifetime of the coherence created in the ground state. However, because the long-lived ground state hyperfine levels decay at a rate of thousands of years, the width is practically determined by atomic collisions with cell walls, collisions with other atoms, changes in magnetic fields, transit time of the atoms through the laser fields, and changes in the phase stability of the frequency difference of the light fields. In practice, atomic resonator Q factors on the order of 10^6 are obtained in small (~ 1 mm) cells.

1.3.4 Use of the LO in CPT

As mentioned above, the quality of the CPT resonance depends largely on the stability of the frequency difference between the light fields. Different techniques have been used to create these two light fields, including phase locking of two diode lasers(25), external modulation of one laser(26), or modulation of the current of a diode laser(27), (28). The first two methods involve large and/or high-power techniques. The latter technique is particularly well suited to the design of ultra-miniature atomic clocks since low-power diode lasers can be modulated with low microwave powers. Diodes with somewhat poor spectral purity can be used since the more important difference frequency is equal to the modulation frequency, which can originate from a stable microwave oscillator. In this method, as shown in Figure 6, a local oscillator (LO) is used to modulate the frequency of a diode laser by modulating the current directly. When the laser diode frequency is tuned (with current and/or temperature changes) to the optical resonant frequency (i.e. the D1 line of ^{87}Rb) an increase in absorption is detected as a decrease in photodetector current. When the frequency of the LO is simultaneously tuned to the hyperfine splitting frequency, the two light fields in Figure 5 are created and coherent population trapping occurs. This results in a pumping of the atoms into the dark state and an increase in light transmission through the atomic cell, observed as an increase in the DC current from a photo diode. Electronic feedback is then used to stabilize the LO using some tuning mechanism.

It is also possible to modulate the laser at half of the hyperfine frequency. This allows for laser diodes with lower modulation efficiency and the two first-order sidebands from the laser are used, since they are separated by the hyperfine splitting frequency. The carrier frequency is detuned from the atomic resonance and can be further suppressed with filtering or by a judicious choice of modulation power.

1.4 Requirements for the Local Oscillator

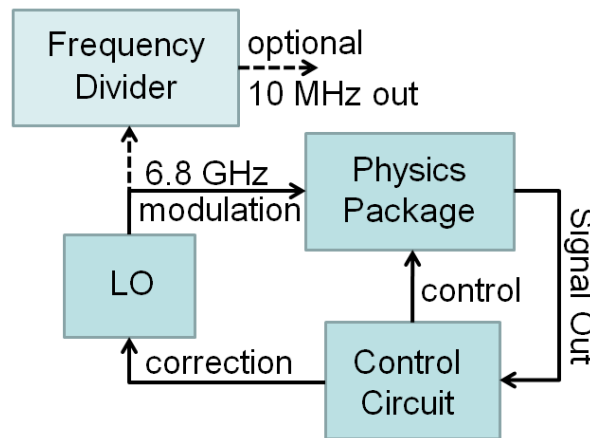


Figure 7 – Schematic showing the three main components of a chip-scale atomic clock. The output from the LO modulates the VCSEL in the physics package. The photodetector output signal is sent from the physics package to the locking electronics, which stabilizes the LO and provides thermal stabilization and other control to the physics. An optional frequency divider can be used to divide the LO frequency down to a standard reference frequency, such as 10 MHz.

The overall locking schematic used in this thesis is shown in Figure 7. The three main components of this atomic clock are the physics package (containing laser, atoms, photodetector, and optical components), the local oscillator (LO), and the control circuitry that provides thermal control and frequency stabilization. An optional frequency divider can be added to divide the LO frequency to a more standard reference frequency, such as 10 MHz. The input to the LO is a DC bias voltage and the output (3.417 GHz for half the ^{87}Rb hyperfine frequency) modulates the diode laser. The output of the physics package is a current that is proportional to the light intensity received on a photo diode. The control circuitry converts this to a voltage that is used to stabilize the LO (using voltage tunability). Thus, from a microwave engineer's perspective, the physics package is a very high Q resonant circuit that can be used to stabilize an oscillator. The requirements for an LO used in a CSAC are summarized below.

1.4.1 Size

Since the size of a chip-scale atomic clock is no longer limited by the microwave cavity of traditional optically-pumped clocks, the size of the LO can be a limiting factor on the overall volume of a clock. Many oscillators use high Q-factor resonators to achieve low phase noise. Resonant cavities and dielectric resonator oscillators often reach Q factors on the order of 10^4 and cryogenic cooling can further increase this to 10^5 or more. Unfortunately, the size of these devices is prohibitive. It is expected that chip-scale atomic clocks can reach sizes

as small as 1 cm^3 (29), already smaller than most microwave resonators at 3.4 GHz. Only a small fraction of the total size can be reserved for the LO, resulting in a challenging design goal that required a new approach.

1.4.2 Power

Using the CPT method, the LO is required to modulate the diode laser with sufficient modulation index to put a large fraction of the optical power into the first-order sidebands of the laser. Preliminary experiments at NIST showed that this required approximately -6dBm of output power at 3.4 GHz (for ^{87}Rb) to modulate the current of a vertical-cavity, surface-emitting laser (VCSEL) that was not impedance matched to the source. It was expected that lower power would be required for a laser that is optimally mounted with an appropriate impedance-matching circuit.

The future DC power consumption of the entire chip-scale clock was expected to be approximately 30 mW, so the LO was initially allotted 10 mW of DC power consumption. This permitted a low-efficiency design, allowing for more focus on low phase noise. However, transistor oscillators typically exhibit lower phase noise at higher bias currents. The challenge in the design was to reduce the bias power while ensuring low phase noise.

1.4.3 Tunability

The LO must produce a frequency compatible with the atomic ground state hyperfine transition. The exact frequency of this transition depends on many factors such as the buffer gas pressure inside the atomic cell, the type of wall coatings used, and the intensity of the light inside the cell. Therefore, until a cell is fabricated, it is not possible to determine the precise frequency. Nonetheless, it is likely that the actual frequency will be within a few tens of kHz above the frequency of a free atom. For ^{87}Rb , the free-atom frequency is 6.834682612 GHz. Partly because the modulation efficiency of the VCSELs (from Ulm Germany) is low at this frequency, it was decided to modulate the laser at exactly half the buffer gas shifted frequency. The LO must be able to tune to this frequency, despite changes in environment, device aging, and part tolerances. However, the frequency tuning range should be small in order to electronically lock to the atomic transition with the precision required for high stability. A large tuning range would increase the effect of electronic noise at the LO output and would increase the number of bits required for a DAC on the control electronics board to reach a resolution consistent with the overall stability requirement of 10^{-11} at one hour integration time. It is therefore desired that the tuning range be as small as possible while allowing for part tolerances, aging, and thermal frequency drift. To enable this, some post-production tuning method is desired for coarse tuning.

1.4.4 Modulation Method

For lock-in detection and feedback, the LO frequency is required to be electronically modulated at a low rate, typically between 100 Hz and 10 kHz, with a modulation depth near the atomic linewidth.(30) This could be accomplished by use of a voltage tuning port on the LO. A linear tuning coefficient of the LO would improve detection and locking by the control electronics, but is not required.

1.4.5 Frequency Drift

A minimal requirement on the drift of the LO is determined by the fact that the LO must not come out of lock with the atoms. This means that the LO frequency must not drift by more than the linewidth of the CPT resonance during the locking time. For a typical resonance linewidth of $\Delta f=1$ kHz and a locking time of $\Delta t=1$ ms (for a typical modulation of a few kHz), there is a limit of $(\Delta f/f)/\Delta t = 10^{-4}/s$ on the drift of the LO. This is an easily achieved goal. However, the requirement is more stringent when considering the overall stability of the locked system. To achieve overall stability comparable to commercial atomic clocks, the goal is 10^{-11} at long integration times (>3600 s).(29) If a one-stage integration servo is used to lock the LO to the atomic resonance, the overall frequency drift is $\Delta f = T_{\text{lock}}(df/dt)$ where T_{lock} is the locking time and df/dt is the LO drift rate. Again, for a lock time of 1 ms, the limit on the LO drift becomes $10^{-8}/s$. Most likely, the drift will be caused by

temperature fluctuations. If the thermal frequency sensitivity of the LO is 10 ppm/K, this results in an environmental requirement of 1 mK/s. The thermal frequency sensitivity requirement is challenging since size and power requirements limit the number of components and thermal control of the LO would consume too much power.

1.4.6 Phase Noise and Resonator Q Factor

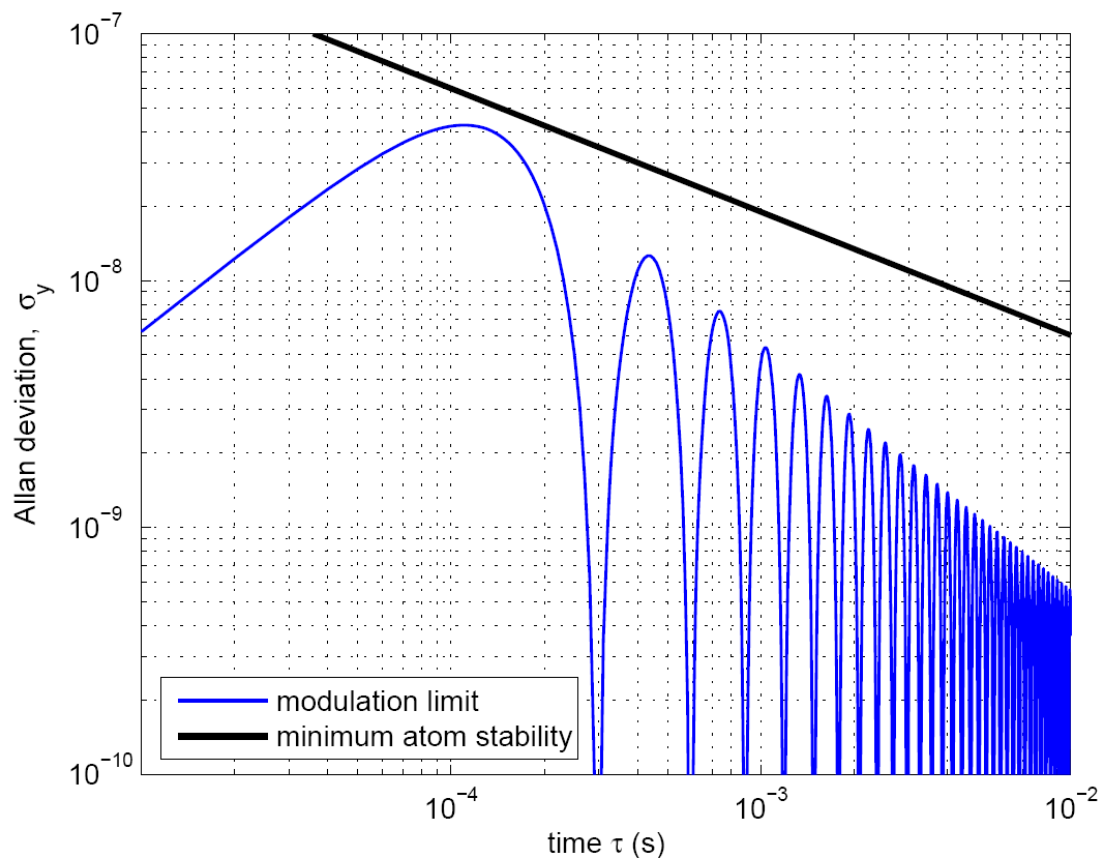


Figure 8 – Allan deviation limits in terms of minimally required atom stability (black) and due to the effect of sinusoidal modulation of the LO frequency with a 3 kHz modulation depth (blue). At small time offsets, the modulation limit becomes more significant.

One of the possible limitations for the frequency stability of an atomic clock of our type has been discovered by Audoin (31) and arises as a result of noise aliasing during the modulation and phase sensitive detection of the LO. This limit can be approximated as

$$\sigma_y(\tau) = \sqrt{\frac{(2f)^2 S_{\phi}^{LO}(2f)}{4\tau f_0}}, \quad (1-3)$$

where $S_{\phi}^{LO}(2f)$ is the phase noise at twice the modulation frequency, f , τ is the measurement time in the Allan deviation measurement, and f_0 is the frequency of the LO. It is not practical to set a modulation frequency greater than the linewidth of the atomic resonance. Therefore a typical upper limit is chosen as $f_m = 1$ kHz. To achieve $1 \cdot 10^{-11}$ at one hour offset time and for the typical $\tau^{-1/2}$ Allan deviation slope, the LO phase noise limit is $S_{\phi}^{LO}(2f) < -64$ dBc/Hz, a requirement that is less stringent than the others listed below.

Another possible limit arises directly from the sinusoidal modulation of the LO mentioned above (32). This modulation results in a noticeable, narrowband peak in the LO phase noise. This peak can be represented as

$$S_y^{LO}(f) = \frac{1}{2} \left(\frac{\Delta f_0}{f_0} \right)^2 \delta(f - f_m), \quad (1-4)$$

where δ is the Dirac delta function, $S_y^{LO}(f)$ is the power spectral density of frequency (not phase) deviations, Δf_0 is the change in the LO frequency, f_0 , due to modulation. Cutler and Searle (33) derived the equation

$$\sigma_y^2(\tau) = 2 \int_0^{\infty} S_y^{LO}(f) \left(\frac{\sin^4(\pi f \tau)}{(\pi f \tau)^2} \right) df, \quad (1-5)$$

which shows the Allan variance (square of Allan deviation) due to a sinusoidal modulation in the frequency domain. Substituting the well known relationship

$$S_y^{LO}(f) = \left(\frac{f}{f_0}\right)^2 S_\varphi^{LO}(f), \quad (1-6)$$

into (1-5) we have

$$\sigma_y^2(\tau) = 2 \int_0^\infty \left(\frac{f}{f_0}\right)^2 S_\varphi^{LO}(f) \left(\frac{\sin^4(\pi f \tau)}{(\pi f \tau)^2}\right) df. \quad (1-7)$$

Substituting a phase noise of -27 dBc/Hz, which is a typical (measured) phase noise peak due to LO modulation, we have the performance limitation shown in Figure 8. This poses a possible limitation near the lock time of the LO, especially as this time is pushed shorter and closer to 10^{-4} s. Comparing this limitation to the minimum required atom stability, shown in Figure 8, we see that for short lock times, the LO must be modulated with a lower modulation depth if the atomic system is better than the absolute minimum and if we want to be everywhere maximized in terms of locked system stability.

The system stability also depends strongly on the design of the control servo. It was decided to use a 1-stage integrating servo because of its simplicity to implement in a small design and because it was determined that a 1-stage integrator would be sufficient to achieve lock if the lock time occurs well before the $\tau^{1/2}$ slope due to LO noise (f^{-4} slope due to random walk in frequency on a phase noise plot)(30). Rather than attempt to minimally meet the DARPA-imposed specification of 10^{-11} at 1 hr integration time, we decided to achieve a lock that does not degrade the atomic performance. For this, we found an analytical representation of Allan deviation based on phase noise, by integrating

equation (1-7) for noise that follows power-law formulation (described below).

The Allan deviation is then the square root of

$$\begin{aligned}
 \sigma_y^2(\tau) = & a_0 \left[36f + \frac{3 \sin(4\pi\tau f) - 24 \sin(2\pi\tau f)}{\pi\tau} \right] \dots \\
 & + a_1 [36 + 36 \ln(f)] \\
 & + a_2 \left[96\pi\tau \sin(2\pi\tau f) - 48\pi\tau \sin(4\pi\tau f) - \frac{36 - 48 \cos(2\pi\tau f) + 12 \cos(4\pi\tau f)}{f} \right] \\
 & + a_3 \left[\frac{96\pi\tau \sin(2\pi\tau f) + 24\pi\tau \sin(4\pi\tau f)}{f} - \frac{18 - 24 \cos(2\pi\tau f) + 6 \cos(4\pi\tau f)}{f^2} - \right. \\
 & \quad \left. 96\pi^2\tau^2 \cos(4\pi\tau f) \right] \\
 & + a_4 \left[\frac{-12 + 16 \cos(2\pi\tau f) - 4 \cos(4\pi\tau f)}{f^3} - \frac{16\pi\tau \sin(2\pi\tau f) - 8\pi\tau \sin(4\pi\tau f)}{f^2} - \right. \\
 & \quad \left. \frac{32\pi^2\tau^2 \cos(2\pi\tau f) - 32\pi^2\tau^2 \cos(4\pi\tau f)}{f} - 64\pi^3\tau^3 \sin(2\pi\tau f) + \right. \\
 & \quad \left. 128\pi^3\tau^3 \sin(4\pi\tau f) \right] \tag{1-8}
 \end{aligned}$$

where a_0 , a_1 , a_2 , a_3 , and a_4 are the 1-Hz intercepts of white phase noise, flicker phase noise, white frequency noise, flicker frequency noise, and random walk frequency noise, respectively. The solution must then be evaluated as a definite integral between some limits $f = f_{\max}$ and $f = f_{\min}$. Equation (1-8) is valid only for the power law formulation of phase noise (a sum of different noise types as represented by their slopes on a log-log phase noise plot.)

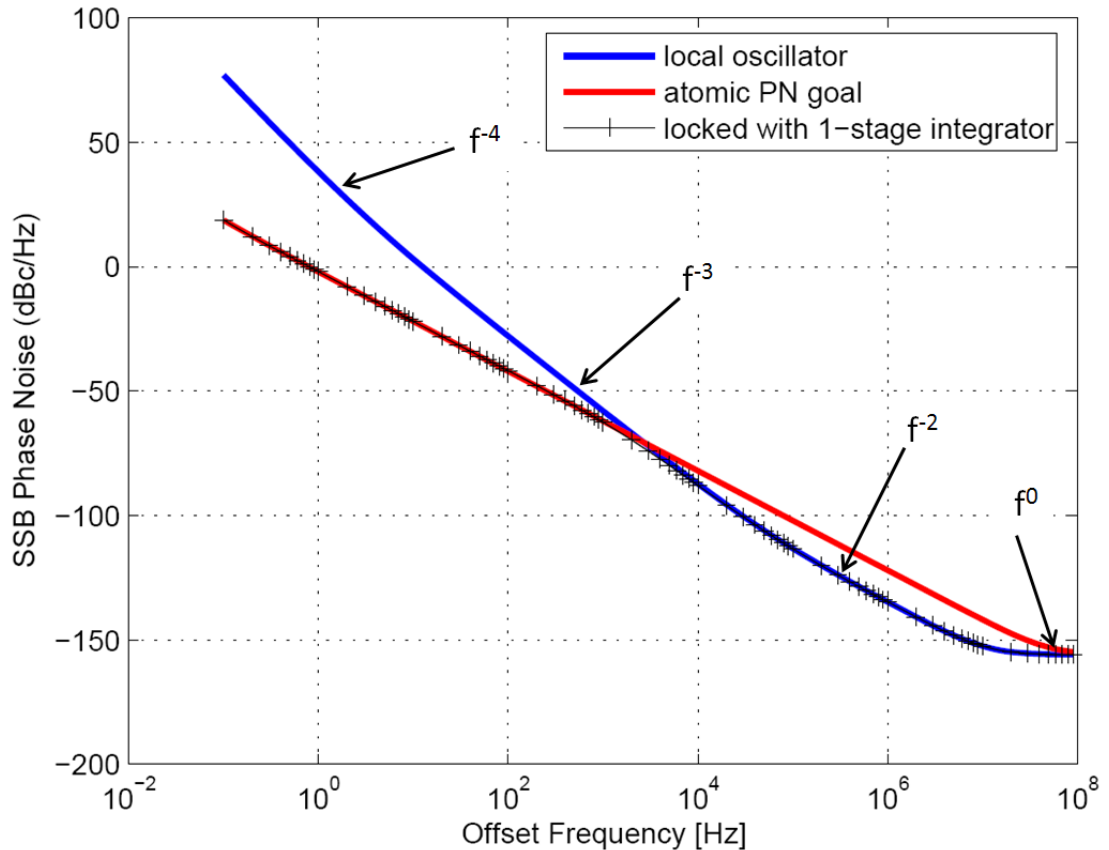


Figure 9 – Phase noise representation of a local oscillator and the atomic phase noise required to reach an Allan deviation of $2 \cdot 10^{-10}$ at one second integration time (based on 3 times the performance of the DARPA-specified goal of $1 \cdot 10^{-11}$ at one hour). The 1-stage integrating servo lock is shown in black. Phase noise slopes f^n with $n = -2, -3, -4$ are shown for comparison to Allan deviation slopes $\tau^{1/2}$ to $\tau^{-1/2}$ in Figure 10.

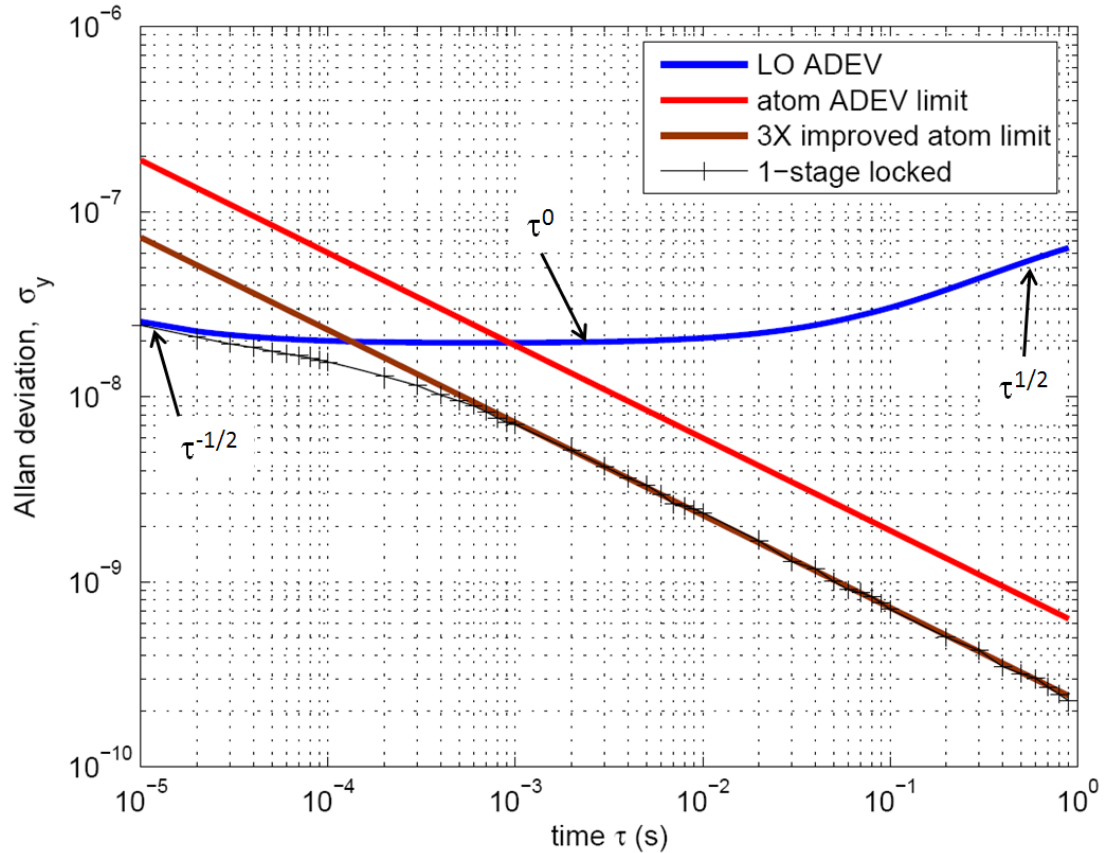


Figure 10 – Allan deviation requirements based on reaching 10^{-11} at one hour integration time (red), a factor of 3 improvement (brown), and a lock (black) to the LO phase noise (blue) based on the oscillator shown in Figure 9.

To determine the minimum phase noise requirement, we considered the power law formulation of phase noise as shown in Figure 9 and solved for the resulting Allan deviation representation, in Figure 10, for times near the lock time. The slopes correspond to the different noise types shown in both figures. In the formulation of phase noise requirements, the location of the intersections of these slopes is very important. Of particular importance are the phase noise

slopes f^4 , f^3 , and f^2 , corresponding to Allan deviation slopes $\tau^{1/2}$, τ^0 , and $\tau^{-1/2}$, respectively. The servo lock is described by

$$\begin{aligned} S_y^{out}(f) &= \frac{1}{(1+G)^2} S_y^{LO}(f) + \frac{G^2}{(1+G)^2} S_y^{at}(f) \dots \\ &= \frac{f^2 T_{lock}^2}{(1+fT_{lock})^2} S_y^{LO}(f) + \frac{1}{(1+fT_{lock})^2} S_y^{at}(f), \end{aligned} \quad (1-9)$$

where $S_y^{out}(f)$ is the frequency spectral density of the locked system, $S_y^{LO}(f)$ is the free running LO frequency noise, and $S_y^{at}(f)$ is the atomic frequency noise. If the $\tau^{1/2}$ slope in Figure 10 is close to the lock time (1 ms in our consideration), the 1-stage integrating servo lock will not be able to completely track to the atoms. If the locked system noise is worse than the LO noise when reaching the LO slope $\tau^{1/2}$, the corrected slope will follow parallel, but not integrate down to the atom stability as $\tau > T_{lock}$. The f^3 flicker frequency noise is important because it largely determines the level of the τ^0 slope in the Allan deviation, which occurs at the lock time. Therefore, choosing a device with a low flicker noise corner is important (see section 2.2.2). For the purpose of determining LO limitations, we assume a transistor with a typical but high flicker corner at 50 kHz, resulting in a flicker frequency level shown in Figure 9. Finally, the f^2 noise is important because it increases the level of the noise that has slope f^3 . Figure 9 and Figure 10 show the results of achieving a lock to atom noise that is a factor of 3 lower than the minimum requirement. This lock time is 1 ms and achieves a lock with no degradation in overall system noise improvement. For this result, the phase noise requirement is as shown in Figure 9. At 100 Hz offset frequency, the phase

noise is shown as -25 dBc/Hz. The phase noise has a flicker noise corner at 50 kHz (lower is desirable), and an oscillator loaded Q of

$$Q_L = \frac{f_0}{2f_L} = 100, \quad (1-10)$$

where f_L is the transition frequency between noise with slope f^0 and noise with slope f^2 . This loaded Q translates to a resonator unloaded Q_U of 200, in the case of a perfectly-loaded, critically-coupled oscillator design.

1.5 State-of-the-Art in Oscillator Design

Table I – Comparison of State-of-the-Art Oscillator Designs				
Resonator Type	Frequency	Phase Noise	Size	DC Power
Sapphire(34)	9 GHz	-160 dBc/Hz @1kHz	>1000 cm ²	many W
FBAR(35)	2 GHz	-112 dBc/Hz @10kHz	0.5 cm ²	115 mW
FBAR(36)	3.4 GHz	-53 dBc/Hz @300Hz	0.5 cm ²	10 mW
This Work(37)	3.4 GHz	-98 dBc/Hz@10kHz	0.5 cm ²	2.8 mW
Other μ -coax(38)	3.4 GHz	-99 dBc/Hz @10kHz	2 cm ²	124 mW
Microstrip(39)	1.8 GHz	-97 dBc/Hz @10kHz	8 cm ²	85 mW
CMOS(40)	5 GHz	-72 dBc/Hz @10kHz	<0.1cm ²	17 mW

Table 1 summarizes the state of the art in microwave oscillator design with respect to phase noise, size, and power consumption. Dielectric resonator oscillators provide some of the best phase noise, with cryogenically-cooled sapphire DROs providing record phase noise(34). However, they tend to be larger than 100 cm³ (not including cryogenics) and consume many Watts of

power. Transmission line oscillators such as microstrip resonators are also too large since the free-space wavelength at 3.4 GHz is 8.8 cm and meandering techniques and high dielectric constant materials are unlikely to bring the size limit below requirements. CMOS and other integrated oscillators based on lumped element (L-C) resonators can be extremely small but suffer in phase noise because of the low Q factor of the resonators (on the order of 10) and because of the high flicker noise corner of CMOS active devices. Therefore, resonators smaller than a few cubic millimeters but with Q factors better than 100 are considered. In this category are field-bulk-acoustic resonators (FBAR) and dielectrically-loaded quarter wave coaxial transmission lines (μ -coax). FBAR oscillators have higher Q factors but can have large thermal drift, while μ -coax resonators can have a somewhat selectable temperature coefficient and can be manually tuned by removing material from the outer conductor. This thesis presents μ -coax based LOs that are shown to have phase noise comparable to the phase noise of the best research-level FBAR oscillators but with smaller size, power consumption, and temperature coefficients. In addition, we compare this work to a commercial design that also uses a μ -coax resonator.

Chapter 2

2. Component Modeling for VCO Design

An oscillator meeting the requirements of small size, and low power and phase noise requires careful design at the component level. Where possible, manufacturer-provided device models are used. However, in the case of the resonator, the tuning varactor, and the VCSEL load, measurements are required to obtain complete information due to the lack of adequate models at microwave frequencies. A low phase noise design implies the need for a high Q resonator and a low noise transistor. Large-signal noise measurements were made to obtain an accurate model for the noise figure and flicker noise of the transistor,

in conditions close to the operating point of the oscillator. To reduce power and size, the measured VCSEL load was initially incorporated as part of the oscillator design.

2.1 Resonator Selection and Modeling

The resonator was the most important component for defining frequency of operation and overall Q factor of an oscillator. In the work described here, selection was made based on the requirements of section 1.5, specifically the need for a small, high-Q resonator. Lumped-element (L-C) resonators can be made extremely small at microwave frequencies but typically have Q factors less than 10, mostly due to low-Q inductors(41)(42). Surface-mount, high-Q inductors are available but are large, can suffer from microphonics (vibration-induced noise) and poor part tolerances(43). MEMS-based resonators that are currently in the research phase(44) can be extremely small and can exhibit microwave Q factors greater than 10,000(45). However, it is difficult or impossible to couple useful power to the resonators and therefore no oscillators using these resonators have been successfully demonstrated. Other interesting candidates include thin-film bulk acoustic resonators (FBAR) and high-overtone bulk acoustic resonators (HBAR). These devices can have Q factors in excess of 500 for FBAR(46) and more than 10,000 for HBAR(47). However, such resonators can have undesirably high thermal frequency drift (48) and large vibration sensitivity(49).

Dielectric resonator oscillators (DRO) offer the best phase-noise performance for this application at 3.4 GHz since the loaded Q is between 100 and 500. Unfortunately, the size of the dielectric puck would exceed the 1 cm² specification. Recent advances in manufacturing have allowed the high dielectric materials, used in dielectric resonators, to be adapted to coaxial resonators, dramatically reducing their size and improving temperature stability. Additionally, increased containment of the field inside the shielded resonator can allow more stable and more predictable frequency operation. These resonators, sometimes called TEM-mode dielectric resonators, can be purchased as one-port quarter-wave transmission lines with the non-connected end shorted or as half-wave transmission lines with the non-connected end open. The inner and outer metallic conductors are typically either copper or silver-plated, with silver providing the highest Q and cost. The rigid construction largely reduces problems with microphonics as compared to surface-mount inductors or crystal-based resonators(50). For these micro-coaxial resonators, good part tolerances result in a high degree of frequency selectivity (0.5%). Additionally, up to 10% tuning can be accomplished, one time, without significant degradation in the Q factor, by physical removal of resonator material at the tab end (51). Figure 11 shows the two commonly-used methods of changing the resonant frequency of a micro-coaxial resonator. An increase in resonant frequency is accomplished by removal of the material on the tab side of the resonator, effectively shortening the overall length. A decrease in resonant frequency can be accomplished by removing metal from the shorted side of the

resonator. However, the latter method perturbs the currents at the short and will more rapidly cause a decrease in Q . We therefore ordered the resonators slightly longer than optimal to allow for manual tuning at the tab end.

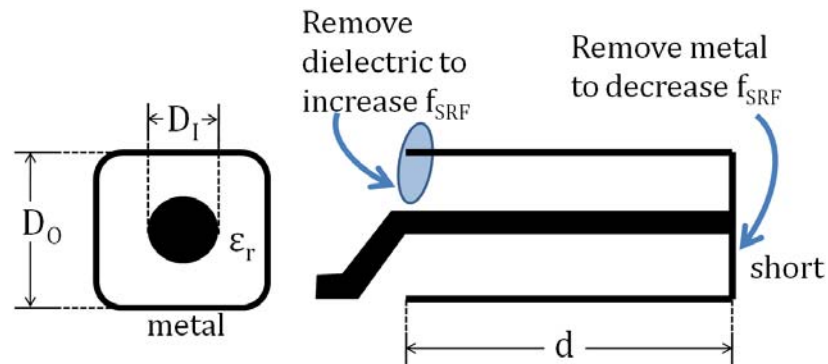


Figure 11 – Diagram showing the construction and tuning methods of a ceramic-loaded coaxial resonator. The height and width of the square structure is D_0 , the inside diameter of the round center conductor is D_i , the length is d , and the relative permittivity of the ceramic is ϵ_r . Approximately 10% tuning to a higher frequency can be accomplished by removing material from the tab end. Small tuning to a lower frequency can be accomplished by removal of conductor material from the shorted end, at the expense of degraded Q factor.

2.1.1 Resonator Operation

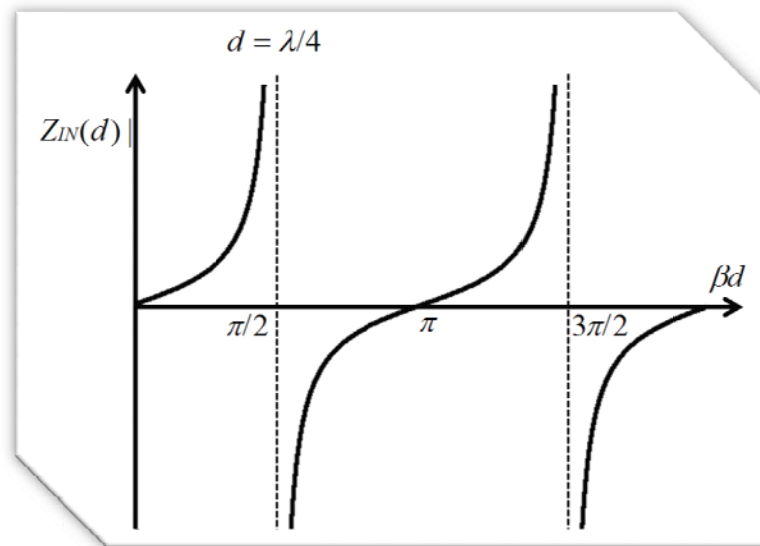


Figure 12 – Well-known graph of the input impedance of a short-circuited transmission line. Below self-resonance ($\beta d = \pi/2$), the component appears inductive. Slightly above self-resonance, the component appears capacitive.

The input impedance for a short-circuited coaxial transmission line is shown in Figure 12, according to the equation

$$Z_{IN}(d) = jZ_0 \tan(\beta d). \quad (2-2)$$

When $0 < \beta d < \pi/2$ the impedance is inductive and when $\pi/2 < \beta d < \pi$ the impedance is capacitive. At frequencies lower than the self-resonant frequencies ($\beta d = n\pi/2, n = 1, 3, 5, \dots$) the resonator appears inductive. As a result, the typical use of a micro-coaxial resonator is as high-Q, temperature-stable and vibration-stable inductor. When coupled with a high-Q series capacitor, it forms a series L-C resonant circuit. Near the self-resonant frequency (ω_{srf}), quarter wave

resonators behave like parallel-resonant circuits. A method similar to (52) is used to derive an equivalent parallel RLC circuit of the $\lambda/4$ shorted resonator, near the first resonance.

The input admittance of a short-circuit $d = \lambda/4$ lossy transmission line is given by

$$Y_{IN}(d) = Y_0 \coth(\alpha d + i\beta d) = Y_0 \frac{1 + j \tan \beta d \tanh \alpha d}{\tanh \alpha d + j \tan \beta d}. \quad (2-1)$$

In the case of low losses ($\alpha \ll 1$) the approximation

$$\tanh \alpha d \approx \alpha d = \frac{\alpha \lambda}{4} \quad (2-2)$$

can be made. In the neighborhood of the first resonance, $\omega = \omega_{srf} + \Delta\omega$, and the following substitution can be made:

$$\beta d = \frac{\pi}{2} + \frac{\pi \Delta\omega}{2\omega_{srf}}, \text{ where}$$

$$\beta = \frac{2\pi}{\lambda} = \frac{\omega}{v_p}$$

and v_p is the phase velocity in the line.

Therefore, near the first resonance,

$$\tan \beta d = \tan\left(\frac{\pi}{2} + \frac{\pi \Delta\omega}{2\omega_{srf}}\right) = \frac{-1}{\tan \frac{\pi \Delta\omega}{2\omega_{srf}}} \approx \frac{-2\omega_{srf}}{\pi \Delta\omega} \quad (2-3)$$

Substituting (2-2) and (2-3) into (2-1), we have

$$Y_{IN} \approx Y_0 \frac{j \frac{\pi \Delta\omega}{2\omega_{srf}} + \frac{\alpha \lambda}{4}}{j \frac{\alpha \lambda}{4} \frac{\pi \Delta\omega}{2\omega_{srf}} + 1}. \quad (2-4)$$

Assuming $\alpha\Delta\omega \ll 1$, the following results:

$$Y_{IN} \approx Y_0 \left(\frac{\alpha\lambda}{4} + j \frac{\pi\Delta\omega}{2\omega_{srf}} \right) \quad (2-5)$$

Now considering the equivalent parallel RLC circuit shown in Figure 13, an expression for the input admittance is

$$Y_0 = G + \frac{1}{j\omega L} + j\omega C. \quad (2-6)$$

Near resonance and using the expansion for small $\Delta\omega/\omega_r$

$$\frac{1}{1+x} \approx 1 - x + \dots$$

yielding

$$\frac{1}{\omega_{srf} + \Delta\omega_{srf}} \approx \frac{1}{\omega_{srf}} - \frac{\Delta\omega}{\omega_{srf}^2}.$$

Substituting into (2-6) the admittance is

$$Y_{IN} = G + \frac{1}{j\omega_{srf} L} + j \frac{\Delta\omega}{\omega_{srf}^2 L} + j\omega_{srf} C + j\alpha C \quad (2-7)$$

At resonance, eq. (2-7) becomes

$$Y_{IN} = G + j \frac{\Delta\omega}{\omega_{srf}^2 L} + j\alpha C \quad (2-8)$$

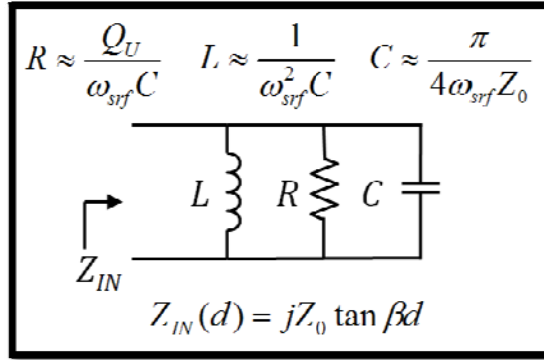


Figure 13 – Equivalent lumped-element RLC circuit for a quarter wave, shorted transmission line. The terms used to approximate R, L, and C are shown.

Near resonant frequency, the middle term in (2-8) becomes negligibly small and, upon comparing (2-8) and (2-5), the following expressions result for the equivalent parallel RLC circuit:

$$R = \frac{4Z_0}{\alpha\lambda} \quad (2-9)$$

$$C = \frac{\pi}{4\omega_{srf} Z_0} \quad (2-10)$$

$$L = \frac{1}{\omega_{srf}^2 C} \quad (2-11)$$

At resonance, the input impedance is purely real and equal to R.

The unloaded Q of the parallel RLC is often quoted and can be used to determine

$$R: Q_U = \omega_{srf} RC = \frac{\pi}{\alpha\lambda},$$

meaning R can be expressed as

$$R = \frac{Q_U}{\omega_{srf} C}. \quad (2-12)$$

For a coaxial resonator, typically the manufacturer specifies the relative permittivity of the ceramic, the dimensions of the part, an approximate value for the unloaded Q, and the self-resonant frequency. A good approximation for the characteristic impedance of a coaxial transmission line with a square outer conductor has been found as(53)

$$Z_0 = \frac{\eta_0}{2\pi\sqrt{\epsilon_r}} \ln(R_{eff} \frac{D_o}{D_i}) \quad (2-13)$$

Where $R_{eff} \approx 1.079$ when the ratio of D_i/D_o becomes less than 1/2 and where η_0 is the characteristic impedance of free space. From the manufacturer-specified values for Q_U , ϵ_r , D_i , and D_o , the characteristic impedance, and the equivalent RLC circuit model were found by use of equations (2-10) through (2-13).

2.1.2 Resonator Specification

For widest tuning bandwidth, the manufacturer recommends a first resonance approximately 15% higher than the desired operating frequency. The main reason for this suggestion is the reduced tuning range due to the tangential increase in inductance shown in Figure 12. When a varactor is used to decrease the capacitance of the series L-C resonant circuit, the operating frequency is increased. However, this tuning ability is restricted due to the steeper increase in effective series inductance near first resonance.

Rather than large tuning range, our goals required a high Q design for low phase noise and a narrow tuning range due to limitations in precision from

digital frequency tuning circuitry. Near first resonance, the resonator presents a higher Q because of the increased series inductance (and a proportionately lower increase in series resistance). However, a careful design is needed in this region of operation due to a larger thermal frequency drift resulting from a larger change in equivalent inductance based on changes in resonant frequency. Operation near first resonance implies low Z_0 and high dielectric permittivity. Three options of dielectric permittivity were offered by the manufacturer (20.5 ± 1 , 37.4 ± 1 , 85.0 ± 3) with decreasing Q_u and size as ϵ_r increases. We chose $\epsilon_r = 37.4$ to provide an expected Q_u as large as 200 and since, at the minimum square profile ($D_0 = 2\text{mm}$), the length of a quarter wave resonator is not significantly larger than the profile.

Equations (2-10) through (2-13) were used to develop an equivalent circuit model, which was then optimized for desired performance. Figure 13 shows the implementation of an equivalent parallel-resonant circuit. The part dimensions and dielectric constant resulted in a characteristic impedance of 9.6 ohms, consistent with that reported by other manufacturers of similar parts(54),(55). Based on communications with the manufacturer, a conservative estimate of unloaded Q was used as $Q_u = 150$ (56). The resonator load of 25 ohms was selected as a typical load presented by the base of the transistor when simulated in the expected operating conditions. While many of the parameters of the resonator can be specified on a continuous range, only discrete values of the coupling capacitor were possible. The coupling capacitor serves the dual purpose of setting the series resonant frequency while achieving critical

coupling for optimum loaded Q . With the use of manufacturer-provided microwave capacitor models, the resonator was simulated with different values of coupling capacitor while varying ϵ_r , and ω_{srf} . As shown in Figure 14, the apparent optimum choice was a 0.2 pF capacitor from Panasonic. Series resistive losses from the capacitor were determined sufficiently low to ignore. With this capacitor, the self-resonant frequency ω_{SRF} was adjusted to provide an operating frequency slightly lower than the desired 3.417 GHz, allowing for some post-production tuning.

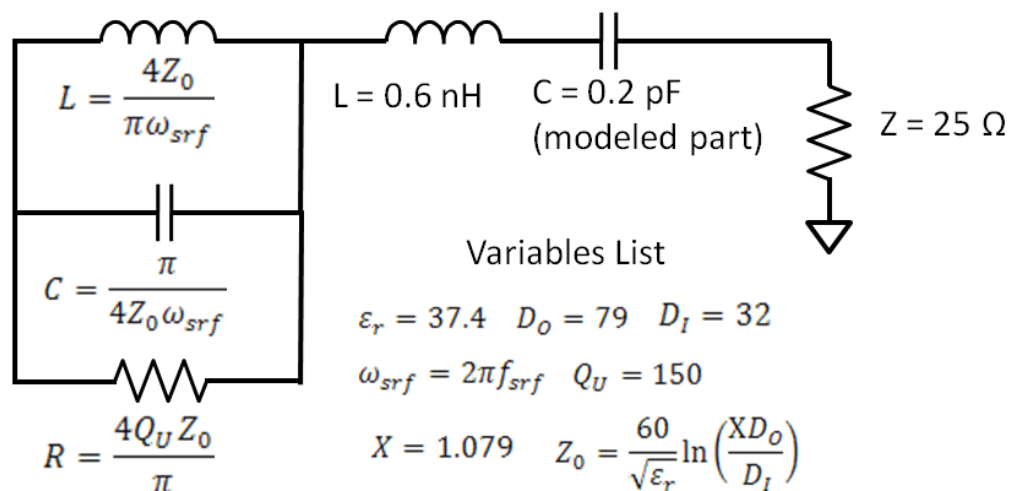


Figure 14 – Equivalent RLC circuit used to model the resonator near first resonance. The equations used to determine component values are shown. A 0.6 nH inductor is added to model tab inductance. The coupling capacitor parasitic effects are considered with a microwave-circuit model provided by the manufacturer. The load impedance is set at 25 ohms, which is a nominal value for the input impedance of the transistor in the oscillator circuit configuration, discussed in chapter 3.

With little available space and power, active thermal compensation techniques were not considered. Instead, we made an effort to balance the temperature-dependent phase shifts of the two most sensitive components—the resonator and the transistor. A temperature-dependent transistor model was used to simulate the change in phase shift across the transistor when operated at 25 °C and at 35 °C. This value was compared to the simulated thermal change in frequency for the resonator, given the manufacturer’s specification that the thermal coefficient of the self-resonant frequency is +7 ppm/°C. A simulated change in ω_{SRF} by +7 ppm resulted in a +6.5 ppm change in the resonant frequency of the circuit in Figure 14. This value tends to compensate for the transistor-caused thermal phase shift. With resonant frequency, Q, size, and thermal drift all meeting goals, the resonators were ordered based on a self-resonant frequency of 3.525 GHz.

In addition to the parallel-resonant equivalent circuit, we developed a transmission line model to aid in simulations covering frequency ranges both near and far from the resonant frequency. A free transmission line modeling program(57), was used to simulate the resonator as a coaxial resonator with a round center connector and a square outer shield. The dimensions and dielectric constant were entered and the reported characteristic impedance was $Z_0=9.6\Omega$, consistent with our calculations. Agilent’s ADS software was then used to model the device as a round coaxial transmission line with the same dielectric permittivity and outer dimensions. The diameter of the inner conductor was, however, reduced to 0.0296 inches in order to provide the characteristic

impedance of 9.6Ω . Finally, we used an optimization routine to adjust the length, loss tangent, and metal conductivity of the model to match the magnitude and phase response of the parallel-RLC model near resonance. Achieving near-perfect overlap, as shown in Figure 15, we used this transmission line model in the initial design of the oscillator, until measured data could be collected.

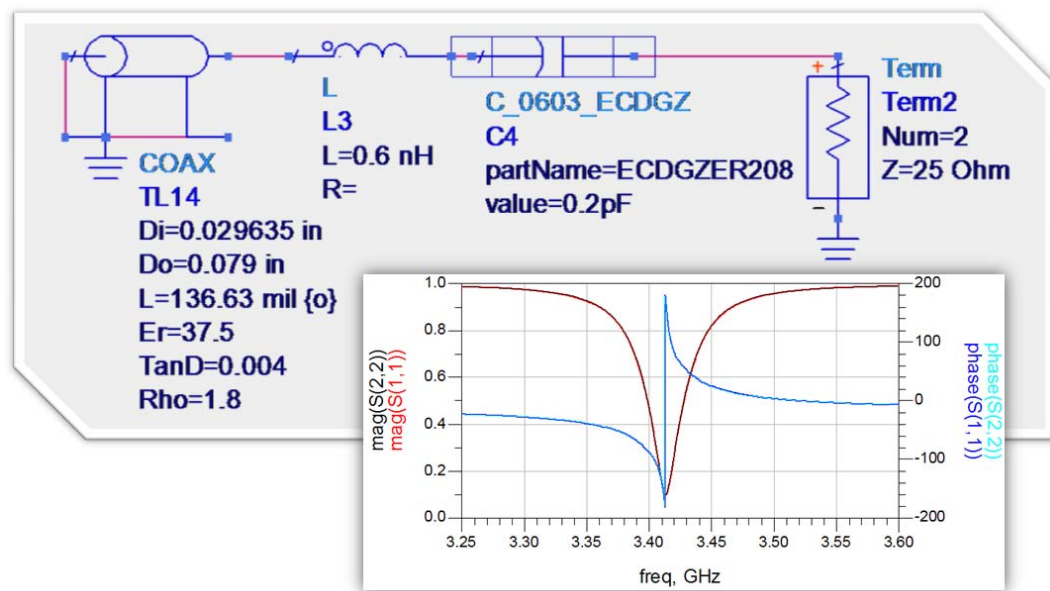


Figure 15 – The final resonator used in Agilent’s ADS software. The loss tangent and conductivity of the coaxial transmission line model were varied by an optimization routine such that the simulated magnitude and phase overlaps with the simulated results from the RLC model shown in Figure 14.

2.1.3 Resonator Measurements

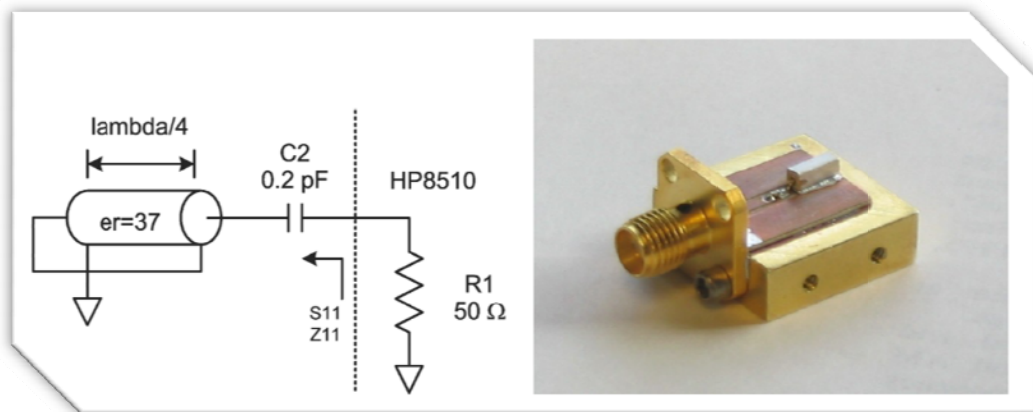


Figure 16 – Resonator schematic and photo showing the method used to measure the self-resonant frequency and Q.

Figure 16 shows a photo and schematic of the resonator mounted in a test fixture used to determine the unloaded Q and operating frequency. The series coupling capacitor is the high-Q 0.2 pF ceramic chip capacitor modeled in Figure 14. A standard coaxial SOLT calibration set was used to set the reference plane at the connector and a negative phase delay was added to back out the extra length of the 50-Ω CPW transmission line. The measured S_{11} data were then inserted in place of the equivalent circuit of Figure 15. We calculated the input impedance Z_{11} from S_{11} to give a close approximation of the unloaded impedance response of the resonator, apart from the 50-Ω load of the network analyzer. As shown in Figure 17, the operating frequency in the expected loaded case is 3.418 GHz. The unloaded Q was calculated from Z_{11} with the use of the magnitude and phase relationships

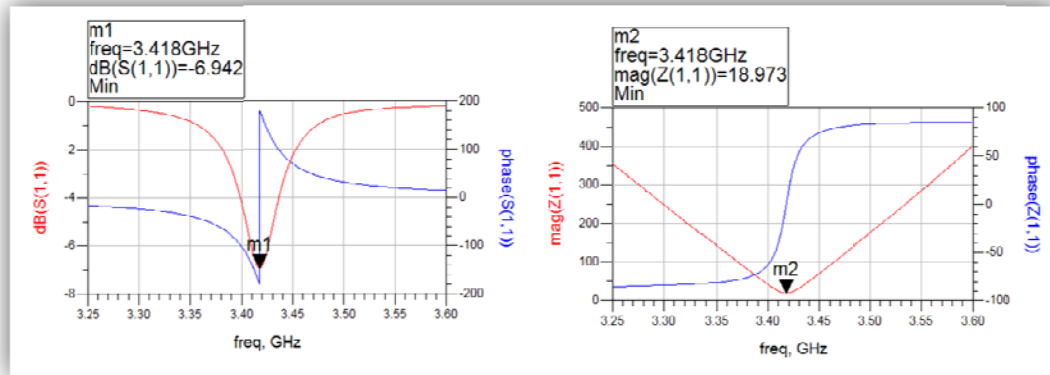


Figure 17 – Measured data from the test set in Figure 16 are plotted from the *.S1P file showing near critical coupling and a self resonant frequency only a few MHz higher than expected. The magnitude and phase of the Z parameters are used to determine unloaded Q factor, which is near 200.

$$Q_L = \frac{\omega_0}{BW} \quad \text{and} \quad Q_U = \frac{\omega}{2} \frac{\partial \phi}{\partial \omega}$$

where BW is the half-power bandwidth of the resonator, or the difference between the frequencies where $|Z_{11}| = \sqrt{2}R$, where R is the equivalent series resistance at resonance.

Thus, the measured, unloaded Q was found to be 193 and the resonant frequency of the loaded device *in situ* was 3.418 GHz. These measured values were later used to modify the circuit models shown in Figure 14 and Figure 15.

The 5-MHz difference between measured and predicted resonant frequencies was believed to be the result of changes within part tolerances. To verify this assumption, a Monte Carlo analysis was performed with the following manufacturer-specified tolerances: $D_0 = 79 \pm 3$, $D_1 = 32 \pm 3$, $\epsilon_r = 37.4 \pm 1$, and $f_{srf} =$

3.525 GHz \pm 0.5%. The results, given in Figure 18, show that frequency shifts as large as 55 MHz can be expected. Therefore, a resonator should be specified with SRF near $f_{srf} = 3.465$ GHz and post-production tuning should be expected if the voltage tuning range is desired small. However, in the interest of time and because some manual tuning of frequency is possible, we used the resonator as is, with some manual tuning expected.

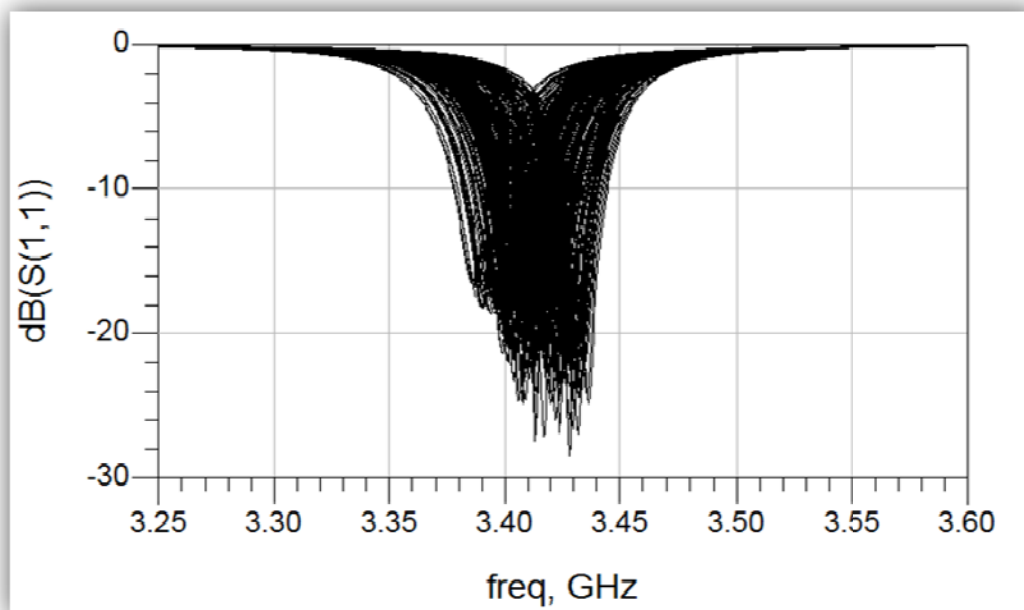


Figure 18 – Monte Carlo simulation (using Agilent’s ADS software) showing more than 50 MHz variation in series-resonant frequency based on manufacturer-specified tolerances.

2.2 Transistor Selection

2.2.1 General Considerations

Available dielectric resonator oscillators at 3.4 GHz typically use a Gallium Arsenide (GaAs) field effect transistor (FET) as the active device. Silicon Germanium (SiGe) has become a popular option for oscillator design as well. However, silicon bipolar devices still perform the best with regard to flicker noise. Flicker noise affects the phase noise very close to the carrier with an increase in close-in phase noise slope by 10 dB. For atomic clocks, low phase noise close to the carrier (100-1000 Hz) is important. Within this range, the phase noise is affected by the flicker corner frequency of the device. (For a further explanation, see section 1.4.6.) SiGe and GaAs FETs typically have flicker corner frequencies near 50 kHz and 1 MHz, respectively. Silicon bipolar junction transistors (BJT) typically have flicker corner frequencies between 5 kHz and 15 kHz. A new class of high frequency ($f_T=25$ GHz device process) silicon BJT devices has become available that is enabling oscillator designs to 10 GHz.

Two factors determine how much gain the active device should have: the loss of the resonator and the desired amount of compression of the closed-loop oscillator. For a critically-coupled resonator, where half the power is dissipated in the load and half the power is in the resonator, the loss is 3 dB. Low levels of compression may seem to be ideal due to the greater accuracy of linear models in this regime. However, an oscillator is in part stabilized by the self-limiting nature of gain compression. Therefore a few dB of compression is desirable to

ensure oscillation occurs over a variety of temperatures and part tolerances. When gain compression is more than 3-5 dB, the flicker noise increases significantly from the small-signal value. Therefore, an open loop gain of approximately 6 dB, requiring adjustment for actual resonator losses, is a reasonable starting point.

Oscillators are generally designed to operate at high power levels, because this increases the power above the noise floor level, resulting in overall phase noise improvement according to Leeson's equation (2-15)(58). However, our stringent low power requirement mandates operation near the lower limits of operation for modern BJTs. To reduce the shot noise associated with device current, we used a low collector current near 1 mA with a bias voltage near the device upper limit of 4 V. Because a transistor's unity gain frequency f_T decreases as collector current decreases, a high f_T is desirable. The BFP405 and the BFP420 BJT from Infineon Technologies have f_T of 6-8 GHz for 1 mA collector current, roughly twice our desired operating frequency(59). This is sufficient to achieve sufficient loop gain to permit oscillation but is low enough to prevent the transistor from strong compression and to reduce oscillations at higher harmonics. Additionally, the devices have large collector areas, permitting a high maximum collector current ($I_C = 12$ mA and 35 mA), which reduces noise due to current crowding, especially at lower operating currents.

2.2.2 Flicker Noise Measurements

One of the parameters that can aid in predicting the final oscillator phase noise(58),(33) is the transistor noise figure, F , which is given in most manufacturers' data sheets, but is specified at small-signal levels. In oscillators, transistors operate in large-signal mode, usually 2-3 dB in compression. In (60), it is experimentally shown that many amplifiers exhibit an increase in noise figure of several dB as the input signal increases, and this large-signal noise figure is given in terms of the broadband (far from carrier) single-sideband PM noise by

$$L(f) = N_{th} + F - P_{in} \quad (2-14)$$

where N_{th} is the thermal noise and is equal to -177 dBm at room temperature, P_{in} is the signal power in dBm and $L(f)$ is the wideband PM noise floor of the amplifier in dBc/Hz. When the large signal F is measured along with the flicker noise corner frequency (f_c), a better prediction of the oscillator phase noise can be found using Leeson's formula, restated here from section 1.5.6(58):

$$L(f_m) = 10 \log_{10} \left[\left(\frac{FkT}{2P_{in}} \right) \left(1 + \frac{f_0^2}{(2f_m Q_L)^2} \right) \left(1 + \frac{f_c}{f_m} \right) \right] \quad (2-15)$$

where f_0 is the carrier frequency, $L(f_m)$ is the ratio of the phase noise power to the oscillator carrier power in a 1 Hz bandwidth, f_m is the carrier frequency offset, f_c is the noise edge of the $1/f$ noise of the oscillator, and F is the large signal noise figure.

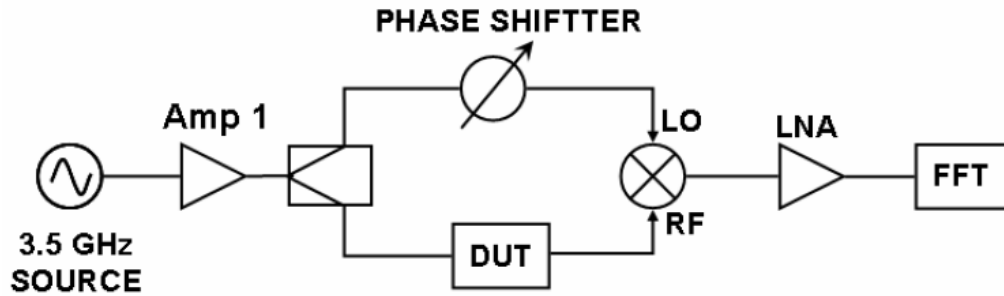


Figure 19 – Block diagram of the additive phase noise measurement system used to measure transistor noise at 3.5 GHz.

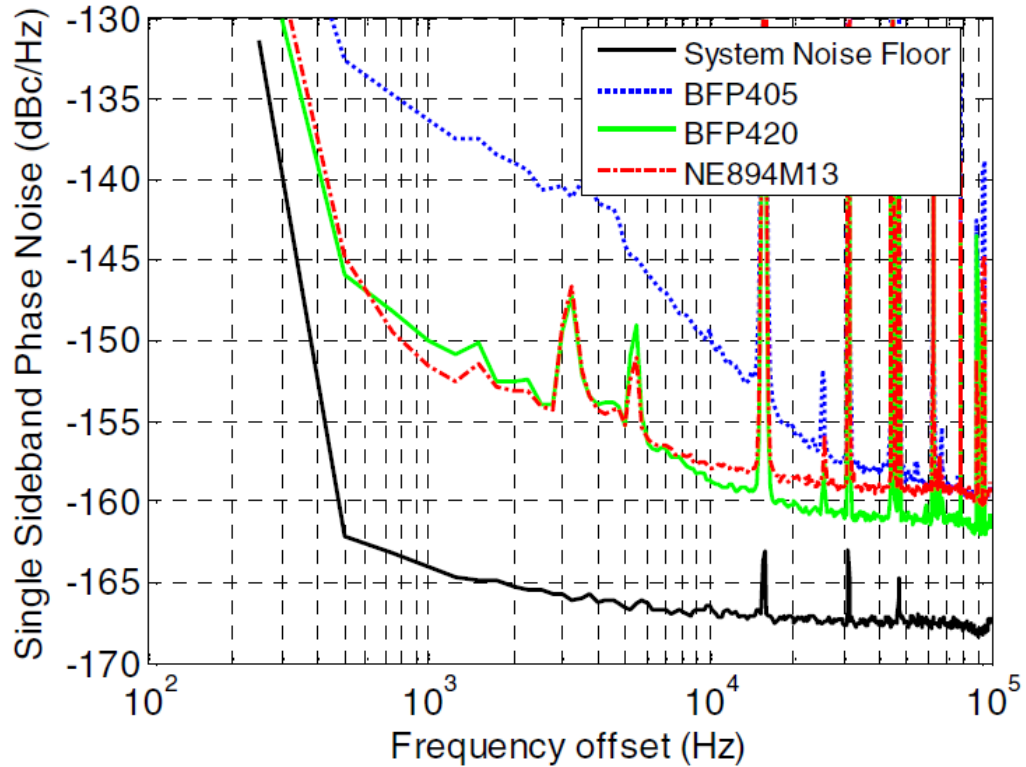


Figure 20 – Additive phase noise measurements made by Milos Jankovic (61) for three BJTs (Infineon's BFP405 and BFP420 and CEL's NE894) at a collector bias of 2.5 V and for an input power of 10 dBm.

A large-signal additive phase noise measurement of three Si BJTs in amplifier circuits with gain similar to that of the device in the oscillator was used to characterize the devices. As this measurement was performed after the design and construction of the oscillators mentioned here, it was not used as part of the selection process but rather serves as a tool to analyze the phase noise of the oscillator and as a guide toward the improvement of the design(61). To ensure that the noise contribution of the additive phase noise measurement system shown in Figure 19 is much lower than the PM noise of the transistor under test, a very clean source at 3.5 GHz is developed. The output of a 100-MHz oven-controlled crystal oscillator is amplified and then up-converted using a low phase-noise comb generating nonlinear transmission line (NLTL) multiplier. The 500-MHz signal component is filtered, amplified and multiplied through another NLTL which generates the required 3.5-GHz source signal in Figure 19. The phase shifter establishes phase quadrature between the two signals at the mixer inputs. The amplified mixer output is detected and on a Stanford Research Systems SR760 FFT spectrum analyzer. Post-processing then converts this to additive phase noise of the DUT. The system provides a noise floor of -168 dBc/Hz at 100 kHz offset from the carrier. Once the additive phase noise $L(f)$ of a transistor is measured, using equation (2-14), the large-signal noise figure of the device is determined. The measurement also gives information about the flicker ($1/f$) noise of the transistor in the amplifier circuit.

The results are given in Figure 19 for three different bipolar transistors connected to 50-ohm input-output lines, with grounded emitters and with 20-k Ω

base bias resistors. The measurement system noise floor is sufficiently low for measurement validity. The last data point, at 100 kHz offset, is considered to be the thermal noise level $L(f)$ and the large-signal noise figure of the transistor is calculated as $177+P_{in}+L(f)$. The data show comparable noise figures for all three silicon devices, though the BFP420 provides the lowest at $F=5.5$ dB. Additionally, the low flicker corner and close-in additive phase noise of the BFP420 validates this transistor as an appropriate choice for a low-noise oscillator design operating at very low power levels.

2.3 Varactor Characterization

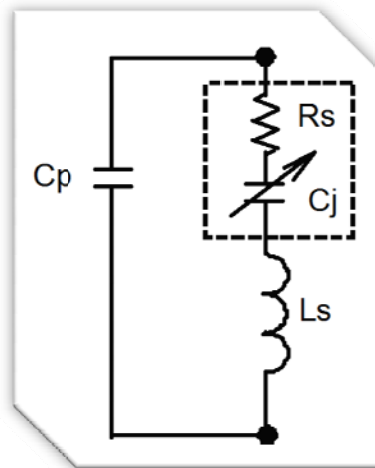


Figure 21 –Varactor diode model in reverse bias, showing parasitic inductance L_s and package capacitance C_p . Series resistance (R_s) and junction capacitance (C_j) vary with frequency and bias voltage.

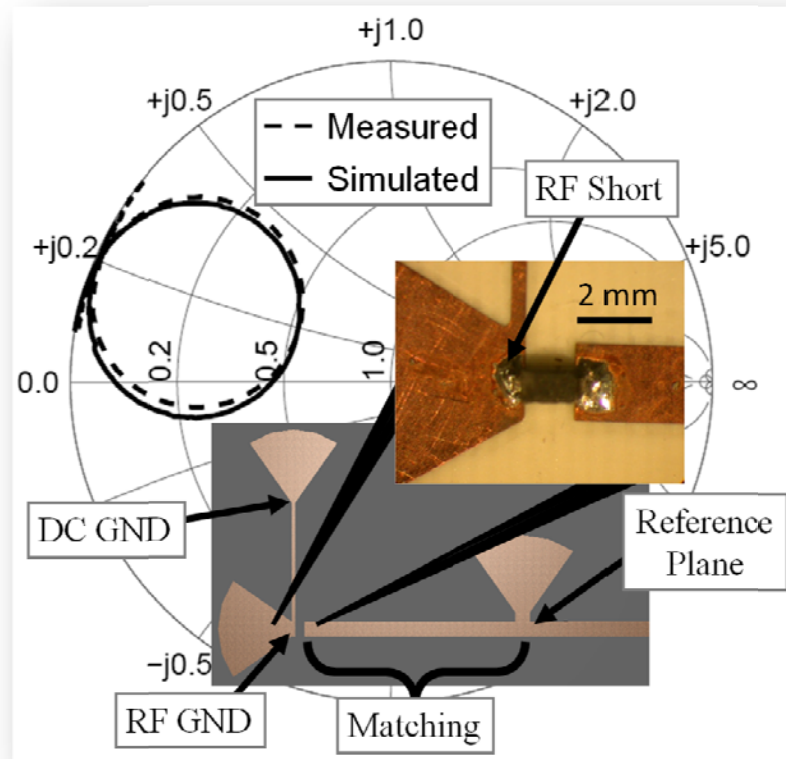


Figure 22 –Photograph of a 1SV280 varactor diode from Toshiba showing its location in a test circuit. In the background are simulated (solid) and measured (dashed) impedances of the varactor diode connected to a $50\ \Omega$ matching line. The R_s and C_j from Figure 21 are fitted to modify measured data at 3.4 GHz, shown on the plot.

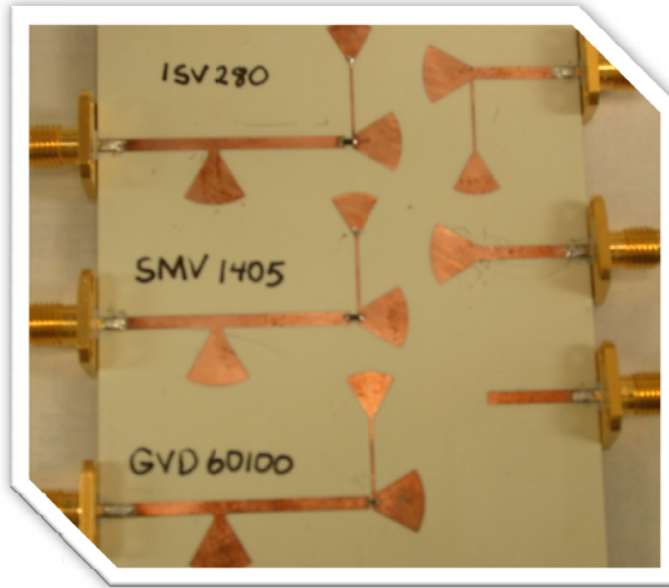


Figure 23 –Photograph of test circuits used to find equivalent circuit models for three varactors. The board also allows impedance measurements for the bias tee, radial stub, and matching circuit.

The typical equivalent circuit model for a reverse-biased varactor is shown in Figure 21. C_j represents the series junction capacitance, R_s is the parasitic series resistance that models package dielectric and conductor losses. The parallel parasitic capacitance, C_p is mostly from packaging effects. Bond wires to the chip and package leads contribute to an equivalent series inductance, L_s . The manufacturer typically specifies the varactor Q, from which the equivalent series resistance can be found using the formula

$$Q = \frac{1}{\omega C_j R_s} \quad (2-16)$$

The manufacturer-supplied values for junction capacitance and Q are specified at low frequency, typically 50 MHz and often at only one reverse bias

voltage, typically 4 V. At microwave frequencies, additional parasitic package and conductor losses often lead to an R_s that is a few times greater than the low-frequency model. R_s also varies as the diode depletion region increases with greater bias voltage, reducing the effective path length through the semiconductor bulk material. Additionally, the variation of C_j with reverse bias is determined mainly by the grading coefficient, M , of the PN junction. M can be found from a datasheet, but often has a wide tolerance specification, resulting in some variation in C_j that reflects process variations from die to die. A varactor model, derived from measurements, is therefore needed to more accurately predict the VCO's tuning range, oscillator frequency, and phase noise. This was obtained with the use of impedance measurements at 3.4 GHz, while sweeping the bias voltage.

The accuracy of S-parameter measurements using a calibrated network analyzer is typically ± 0.05 dB and a typical varactor series resistance is only one or two ohms. Therefore, the directly-measured impedance will be on the edge of the Smith chart and small variations in R_s will be difficult to observe. This results in significant errors if the varactor impedance is measured directly. Instead, we simulated and constructed an impedance match at the frequency of interest from the low-frequency, manufacturer's equivalent circuit to 50 ohms. In this configuration, shown in Figure 22, small changes in R_s result in large variations in measured data near the center of the Smith chart. The actual varactor was inserted at the location shown in Figure 22 and a Thru-Reflect-Line (TRL) network analyzer calibration was used to set the reference plane at the end of

the matching circuit. This matching circuit was designed using microstrip transmission lines and radial stubs and simulated with Agilent's ADS software between 3 GHz and 4 GHz. For increased simulation speed and accuracy, we modified Stauffer's technique(62) to eliminate the need for vias for RF and DC ground. Our circuit shown in Figure 22 provides DC ground at the end of a planar microstrip bias tee, and RF ground is achieved with a radial stub at the anode. DC bias voltage was inserted with an external bias tee, located before the SMA connector on the test board.

Although planar microstrip simulations are typically accurate, S-parameters of the radial stubs and the planar bias tee were measured using the test board shown in Figure 23 and then inserted into the simulations. It was verified that either the measured S-parameters or the simulated transmission-line models can be used to simulate the matching and bias circuits.

Finally, an optimization was performed to modify the values of C_j and R_s so that the simulated curves, typified in Figure 22, matched the measured curves as closely as possible at all points. This was accomplished by setting the simulation optimization goal to minimize the magnitude of the difference between the S_{11} measured and S_{11} simulated curves. The error between the measured S_{11} curve and the resulting simulated curve is apparently due to a difference in phase delay of less than 1° , which is likely an error in setting the location of the reference plane. Following this approach, a series resistance greater than 2Ω at 3.4 GHz was found for each of the varactors tested, more than a factor of 2 increase over the optimistic circuit model.

2.4 VCSEL Characterization

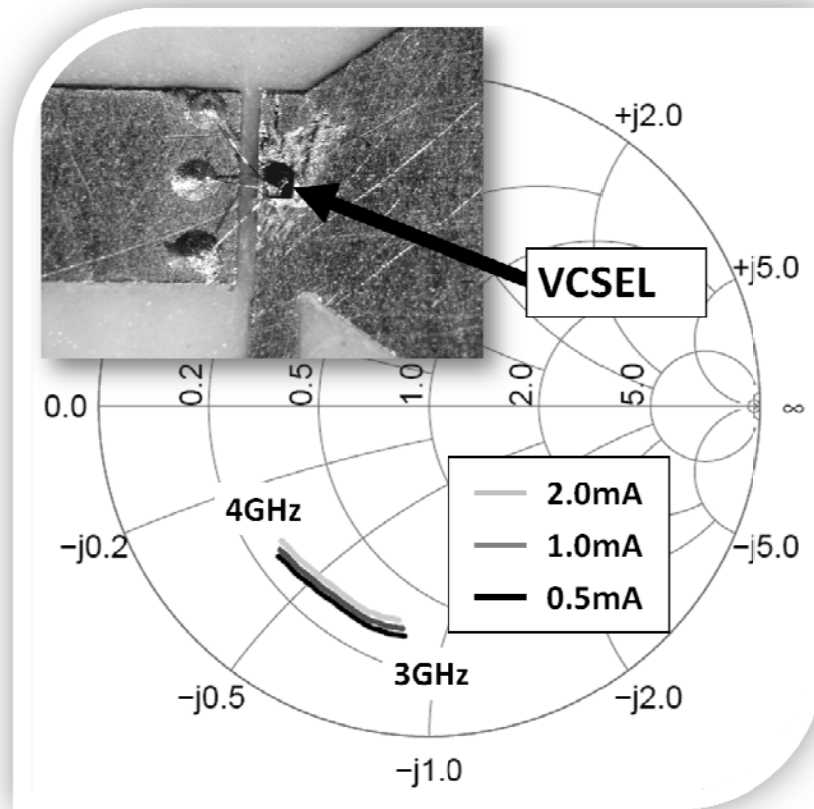


Figure 24 –Photograph of VCSEL wirebonded to its test circuit and measured input impedance for three values of bias current.

The load for the oscillator output is a vertical-cavity, surface-emitting laser (VCSEL) that is tuned to the appropriate optical absorption frequency for the alkali atom species (795nm for Rb87). For best impedance matching, the RF load presented by the VCSEL was measured under several bias conditions. The VCSEL was mounted in a microstrip circuit shown in the inset of Figure 24. The circuit was calibrated with TRL standards and the reference plane set at the end of the microstrip line where the wire bonds connect. Figure 24 shows the

resulting measured RF impedance of a 795nm VCSEL at different bias conditions over a frequency range of 3 GHz to 4 GHz. The data show little change over the typical current bias levels and the nominal impedance at 3.4 GHz is $16-j31.6\Omega$.

2.5 Other Components

Small-sized 0402 components were used where possible to provide a better approximation of lumped-element components and to keep the overall size of the oscillator small. The bias network was constructed with surface-mount inductors used near the first parallel self-resonant frequency. To include parasitic effects, full microwave circuit models were used in simulations. The operation of a bias inductor is to appear as an open circuit at 3.4 GHz. The second, package series resonance does not occur until much higher frequencies, typically at least twice the parallel resonant frequency. The result is that a given inductor may be used as a bias inductor to approximately $1.5f_{\text{res}}$ where f_{res} is the self resonant frequency given in manufacturers' datasheets.

The capacitors were chosen to have high quality factors (low series resistance losses). This is particularly important for the resonator coupling capacitor since it forms part of the resonator and is in series with the equivalent inductance of the high-Q coaxial resonator mentioned in section 2.1. Ceramic chip capacitors have Q factors often above 400 at S-band frequencies. We chose Panasonic's ECD series high-Q microwave chip capacitors, offering Q factors greater than 300 at microwave frequencies.

Chapter 3

3. Oscillator Circuit Design and Modeling

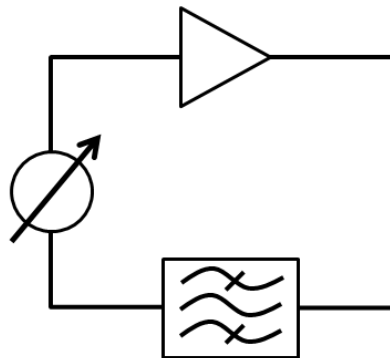


Figure 25 – Diagram showing an oscillator as a simple frequency-selective feedback loop with gain and an adjustable phase shift.

In the simplest representation, an oscillator, shown in Figure 25, consists of a gain block, a frequency selective filter, and a phase shift. Oscillations start from noise at the frequency specified by the filter due to the greater-than-unity small-signal gain of the feedback path around the loop at this frequency. For oscillations to be maintained, the total loop phase shift must be an integer multiple of 360° . Self-limiting of the gain can occur with the use of automatic gain control (AGC) circuitry, but typically occurs as a result of self-limiting in the active device as it moves into a region of gain compression. This nonlinear effect can almost always be neglected in the initial design of an oscillator, while the frequency of operation is determined. However, phase noise is typically only determined after the use of nonlinear techniques such as harmonic balance analysis. In our design, we have implemented the little-known technique of transmission analysis with virtual ground (63) to optimize the phase slope, and hence the loaded Q, of the oscillator. Our analysis also displays other important circuit properties such as the shape and nature of the loop gain, allowing for useful insight for post-production frequency tuning while maintaining proper phase and phase slope conditions. We compare the results achieved with the transmission analysis to those found using harmonic balance and the negative resistance method. As will be shown, much of the circuit-level design was performed as an iterative process, comparing the more intuitive results from transmission analysis to the more accurate nonlinear harmonic balance analysis. Due to the complex interactions among circuit components, the sections below

were not followed in a stepwise fashion but were instead considered as parts of the whole picture.

3.1 Resonator Topology

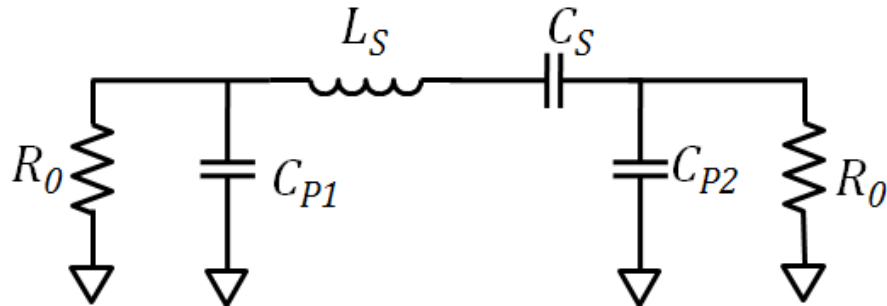


Figure 26 – The loaded resonator shown with two potential shunt capacitors.

The selection and characterization of the resonator was shown in section 2.1. There are several ways to implement this resonator in a circuit, but these can be reduced to two primary categories: a reflection topology and a feedback topology. We have chosen to use the reflection topology, connected at the base of the transistor, for reasons shown in section 3.2. However, the transformation employed in section 3.4 enables the resonator to be viewed in a feedback topology for purposes of that analysis. Therefore, we now take a look at the two-port implementation of the resonator.

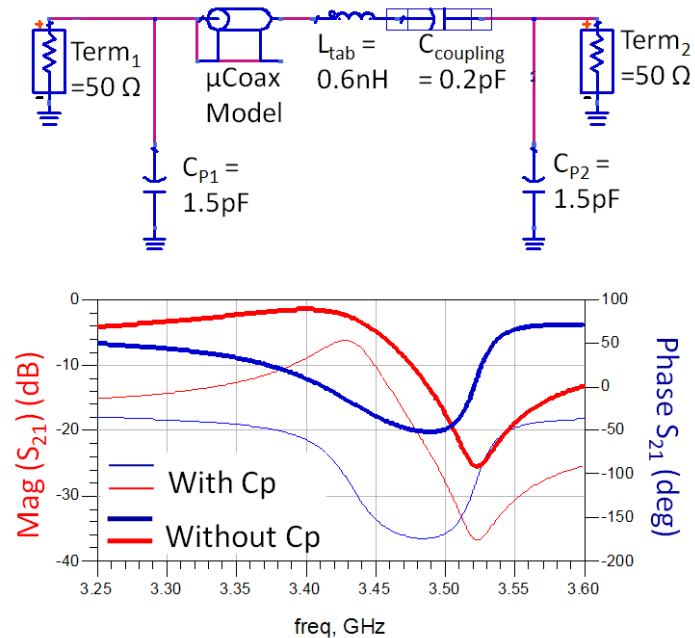


Figure 27 – The effect of the shunt capacitors on the phase slope and total phase shift. The coupling capacitors can improve resonator Q and they introduce a negative phase shift.

Showing the simplified circuit as a series L-C resonator, we consider the topology in Figure 26. The shunt capacitors are added for three purposes. First, they can be used to transform the impedance at the input or output port to the remaining part of the circuit, enabling optimal loop gain transmission and the adjustment of overall gain margin for optimal gain compression. Secondly, the shunt capacitors add a negative phase shift from port 1 to port 2, providing a useful adjustment for overall phase shift in the loop. Finally, these components can be used to increase the loaded Q of the circuit as observed by an increase in the slope of the phase response.

Although this circuit is best optimized with the use of a CAD simulator, it is useful to show the effect of the various components. For the circuit shown in Figure 26, the loaded Q can be derived as

$$Q_L = \frac{X_L}{2R_0} \left(1 + \left(\frac{R_0}{X_P} \right)^2 \right) \quad (3.1)$$

from the energy-based definition of Q and by transforming the shunt R and C into equivalent series components. Here, R_0 is the reference (load) resistance, X_L is the inductor reactance, and X_P is the shunt capacitor reactance, assuming equal values. As can be seen in eq. (3.1), increasing the shunt capacitor values is an effective way to increase the Q_L of the resonator.

Considering the transmission analysis shown in Figure 27, using the actual component models, we observe the three above-mentioned effects of increasing the shunt capacitors. The parallel self-resonant frequency can also be observed as a decrease in transmission and a positive phase slope. In this configuration, this “anti-resonance” is not useful since the positive phase slope would result in a counter-clockwise rotation on the Nyquist plot, counter to the proper encircling of the (1,0) point that is required for oscillation. For more on this, see section 3.4. Notice the significant decrease in phase shift caused by the shunt capacitors. At microwave frequencies in the S-band, typical BJTs exhibit S_{21} phase shifts between +50 and +80 degrees, when terminated in matched loads (63). For transistors with lower f_T , this phase shift can be lower. Therefore, in order to keep the negative phase shift contribution appropriately small, capacitor C_{P2} can be removed. This simplifies the circuit since there will

be no additional phase shifters required. The removal of C_{P2} causes no significant detrimental effect in our circuit because, at 3.4 GHz, the internal base-emitter capacitance of the BJT will take the place of C_{P2} , as shown in the next section. Additionally, microwave capacitors typically have an output impedance that is considerably higher than the input impedance (which is usually matched near 50 ohms). Therefore the matching effects of C_{P1} will be more useful than those of C_{P2} .

3.2 Circuit Topology

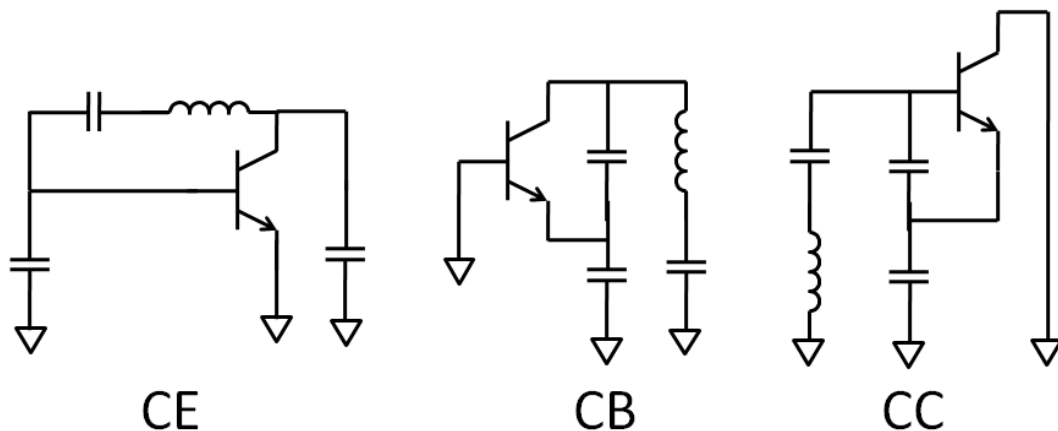


Figure 28 – The three main oscillator configurations (common-emitter, common-base, and common-collector), where the resonator is modeled as a series L-C circuit.

Ignoring DC biasing and output coupling components, we can represent our circuit topology options as three circuits, shown in Figure 28. These circuits are called common-base (CB), common-collector (CC), and common-emitter

(CE), based on the location of the ground reference point. CC topologies typically present a large negative resistance at the base over a large range of frequencies. Instability is therefore a potential problem since the phase shift in the loop might easily have multiple zero crossings. Due to nonlinear operation, unwanted changes in bias point can lead to large sensitivity to thermal variations, sharply nonlinear tuning characteristics, and squegging (a change in oscillation frequency and even sporadic existence of oscillations)(64),(65). CC designs typically form the load with a transistor, creating a complex amplifier. Considering the dangers of very nonlinear action and our need to maintain a low and specific output power with minimum components, this topology was rejected. CB topologies are typically used in the microwave regime due to their exemplary gain at microwave frequencies and ready analysis using negative-resistance techniques, which are most common for RF and microwave oscillators. The Colpitts design of a CB oscillator typically has negative real-part impedance at its emitter between $f_T/5$ up to f_{max} , depending on the base-to-ground parasitic inductance(64). Often, an additional inductor is placed at the base of a CB oscillator to increase the negative resistance(52). Due to the potentially large negative resistance observed at the input of a common-base device, CB oscillators can make excellent microwave oscillators but can also be susceptible to spurious modes. CE topologies like the Pierce oscillator typically present excellent out-of-band stability(64),(66), (67), presenting open-circuit stability (and stability with high output mismatches) at frequencies typically above $f_T/3$. They can also be kept stable at lower frequencies, where the higher

gain of active components can cause spurious oscillations in most oscillator topologies. As shown in section 3.4, we transform our circuit from a CB topology to a CE topology for transmission analysis. This will enable some of the benefits of both topologies in our CB design.

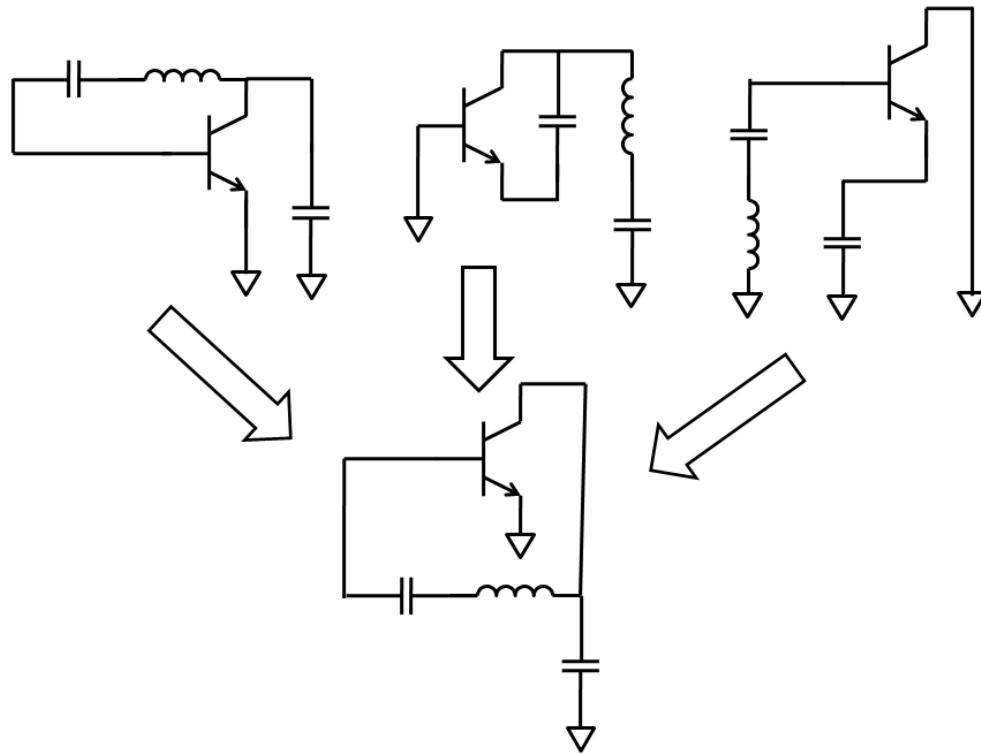


Figure 29 – The three configurations are shown without the shunt capacitor C_{P2} and can be seen as essentially the same topology, depending on the location of the ground reference.

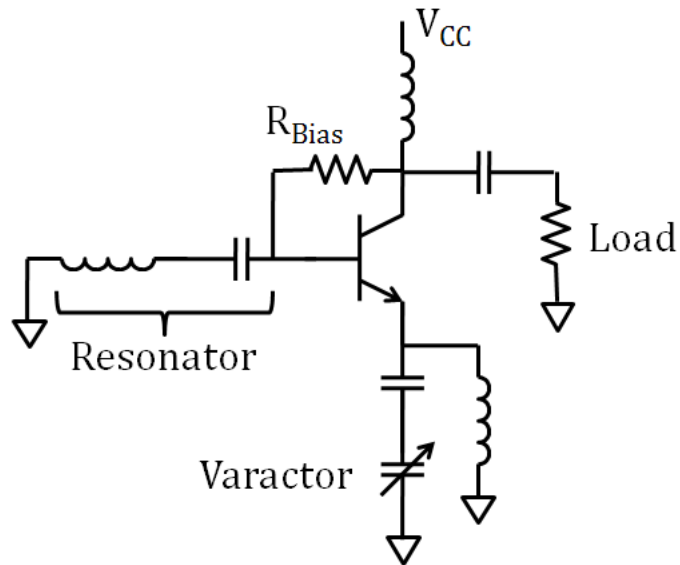


Figure 30 – The chosen oscillator topology. The resonator is an equivalent series L-C type, bias is accomplished with a base-collector resistor, the varactor is lightly coupled through a series capacitor to reduce tuning range and to increase Q. The output power is coupled from the collector.

Removing the shunt capacitor C_{P2} from our design, the three topologies can be represented as in Figure 29. The CE configuration is most practical since it enables an output from the collector, a convenient way of separating the resonator from the active device, and a simple and reliable bias scheme. Additionally, the configuration provides a convenient location for the varactor in the feedback network – in series with the emitter capacitor. In this location, the varactor can be lightly coupled to the circuit, providing a small voltage-variable phase shift while not storing a significantly large portion of RF current. This provides a high-Q design (the effective series resistance losses in the varactor

are reduced) and minimizes AM to FM noise conversion that can result from the primary action of varactors.

The seminal work of Lee and Hajimiri (68) has shown that $1/f$ phase noise in oscillators is added in a linear time-varying fashion according to the location of the peak currents of the oscillation. It was determined that Colpitts-type oscillators are ideal because the collector current flows typically during a short interval coincident with the most benign moments (the peaks of the tank voltage). The correspondingly excellent phase noise properties cause this to be our choice of topology. A Colpitts-type topology, known as a Clapp oscillator, (69) has superior frequency stability due to the insertion of a frequency-determining capacitance shown in Figure 30 in series with the inductor. This enables the phase shift to be determined primarily by the shunt capacitor(s) and the frequency can be set by the series L-C combination. This is the topology we employ.

The resultant basic circuit topology is shown in Figure 30. For virtual ground analysis (section 1.4) it is good to have a topology that is easily converted to an active gain element that is separated from a feedback network. Our topology is readily suited to this analysis, allowing visualization of such things as loop gain, loop phase angle, and stopband stability. We chose a topology that does not have a significant change in bias conditions as the circuit is transformed from a CB to a CE configuration. This allows us to use the nonlinear transistor model instead of the bias-dependent s-parameter representation, speeding the design and enabling quick comparison with

nonlinear harmonic balance simulations. The transistor is biased with a resistor for simplicity, low power consumption, and low part count. While the thermal noise of this resistor was a concern, the shot noise due to collector current is typically more significant (70),(71). To reduce this current, the oscillator was biased to operate at a high voltage and at the minimum current required to provide proper output power. The resonator coupling capacitor also served as a DC block from the bias voltage. An inductor was connected from the emitter to ground to pass DC and to provide a component to tune the loop phase shift in the positive direction, if needed. The output coupling capacitance and the collector bias inductance can be used to transform the output to the proper VCSEL load impedance, channeling the output power more effectively.

3.3 A Review of the Negative Resistance Technique

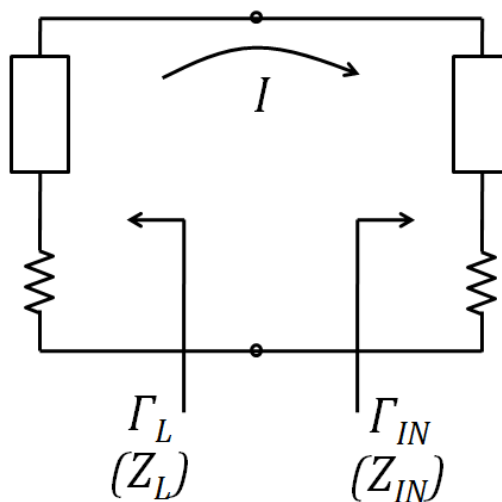


Figure 31 – The simple negative resistance oscillator typically used as a starting point for oscillator designs. When $Z_{IN} = -Z_L$, the circuit oscillates.

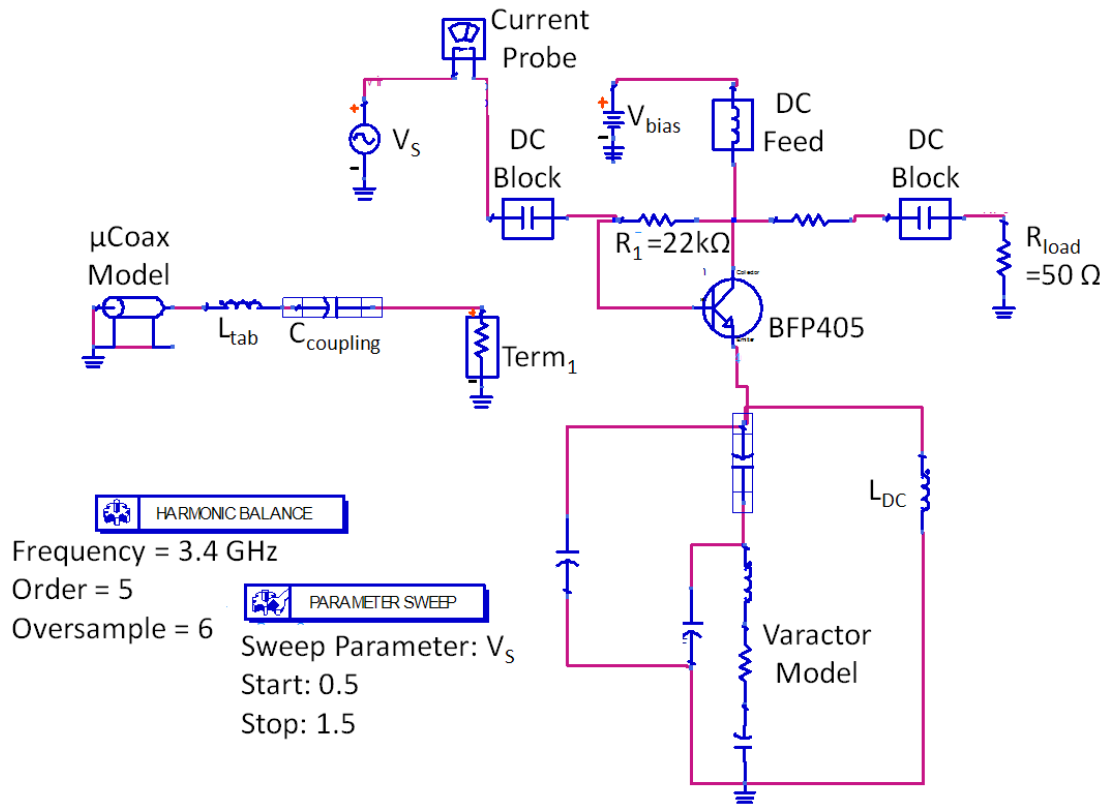
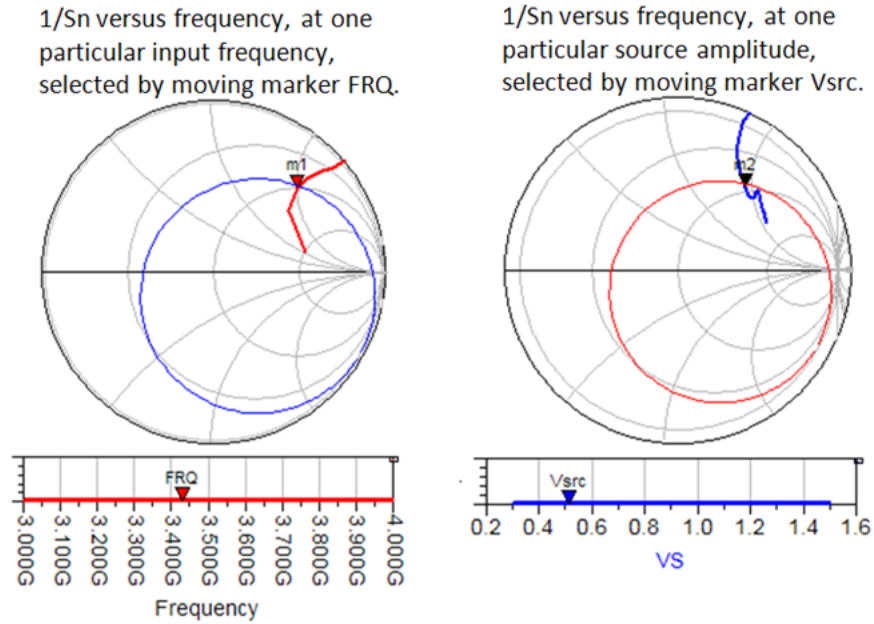


Figure 32 – The oscillator configured for negative-resistance analysis. A harmonic balance simulator is used to simulate the nonlinear circuit while varying the input voltage on the transistor base, specified by V_S . The resulting device impedance line and load impedance line are shown in Figure 33.



Definition of Large-Signal S-Parameters:

$$V_1 = VS[1]$$

Select the first harmonics of voltage and current. (For a high Q resonator we can neglect higher harmonics.)

$$I_1 = I_{probe}[1]$$

$$Z_0 = 50$$

With V_1 , I_1 from above we define large-signal incident and reflected waves.

$$a_1 = V_1 + Z_0 I_1$$

$$b_1 = V_1 - Z_0 I_1$$

We can now define the large-signal reflection coefficient S_n .

$$S_n = b_1 / a_1$$

Figure 33 – The results of the negative-resistance analysis from Figure 32. These can be compared to the results from the TAVG method and the HB method in Figure 35 and Figure 38, respectively. Good agreement in terms of frequency and stability are shown.

An overview of the negative resistance technique can be found in references (52),(69),(72), (73). We merely state the most significant points here for later comparison to the transmission analysis method. Although two-port methods (74) have been developed, negative resistance analysis is typically viewed as a one-port method. It is based on the separation of the passive components (typically including a resonator) and the active components that generate RF power. In the same manner that resistors dissipate power, a negative resistance can be used to describe power generation at the operating frequency. Figure 31 shows an oscillator represented by the connection of active and passive components. The active impedance is represented by

$$Z_{IN}(I, j\omega) = R_{IN}(I, j\omega) + jX_{IN}(I, j\omega) \quad (3.2)$$

and is dependent on both RF amplitude and frequency. The passive impedance is represented by

$$Z_L(j\omega) = R_L + jX_L(j\omega) \quad (3.3)$$

R_L is typically only a weak function of frequency and so is omitted here. The reactance X_L , however, is a fast-varying function of frequency, especially for a high-Q resonant structure. Using Kirchhoff's voltage law, it is seen that oscillation occurs when $Z_L(j\omega) + Z_{IN}(I, j\omega) = 0$. Typically, the resistive components $R_L(j\omega) + R_{IN}(I, j\omega) = 0$ are used to determine the existence of oscillation by ensuring that the active device is biased in such a way as to provide a significantly large negative resistance. The frequency of operation is determined by the reactive components such that $X_L(j\omega) + X_{IN}(I, j\omega) = 0$. This is mostly a function of the quickly-varying passive reactance, but phase shifts in the active

components will also contribute. The stability of the oscillation is then found using the Kurokawa condition (75)

$$\left. \frac{\partial R_{IN}(I)}{\partial I} \right|_{I=I_0} \left. \frac{dX_L(\omega)}{d\omega} \right|_{\omega=\omega_0} - \left. \frac{\partial X_{IN}(I)}{\partial I} \right|_{I=I_0} \left. \frac{dR_L(\omega)}{d\omega} \right|_{\omega=\omega_0} \quad (3.4)$$

Using the negative resistance technique, Kurokawa developed a widely-used graphical analysis for evaluating the oscillation frequency and stability of a negative resistance oscillator(76). This technique, shown with our oscillator as an example, plots the impedances of Figure 32 as reflection coefficients, Γ . The active device line is plotted as $1/\Gamma_{IN}$ and the intersection of this line, shown in Figure 33, with the load line Γ_L occurs at the frequency of oscillation specified by the load line and at the amplitude specified by the device line.

Our circuit, shown in Figure 30, is readily configured for negative resistance analysis. The load line in Figure 33 is plotted directly as the reflection seen looking toward the resonator. The device line is plotted as the reflection seen in the other direction when driven by an adjustable voltage source. The amplitude and frequency dependent device line is shown separately as a frequency-dependent line, chosen at a given amplitude and an amplitude-dependent line, chosen at a given frequency. The equations shown in Figure 33 were used to calculate the large signal reflection coefficients for the analysis. We have chosen two circuit operating points for comparison to the transmission analysis and harmonic balance analysis of sections 3.4 and 3.5. The first is for a configuration that leads to poor phase noise and the latter is for a configuration that leads to near-optimal phase noise. As predicted by Kurokawa (76), better

phase noise is achieved when the device line and the load line intersect near right angles. The operating frequency and power compare well with that shown in the nonlinear harmonic balance analysis of section 1.5.

Though frequency and signal power are found with this method, there remain some challenges posed for the designer. For example, the odd change in device line direction as a function of frequency is left unexplained with little means for correction. The main problem with this method is that the feedback action of the oscillator is not shown, leaving the designer with little intuition regarding the effect of individual circuit components on the overall design. To ensure oscillation, the use of this technique typically suggests setting the negative resistance at least 3 times the magnitude of the load resistance (52), relying on the gain compression to stabilize the circuit at a frequency close to the desired one. This often results in high noise levels due to strong gain compression or, alternatively, the circuit may not oscillate, leaving the designer without a good understanding what can be changed to correct the design. To achieve an accurate estimate of the operating frequency, nonlinear s-parameters should be used, requiring a harmonic balance analysis, which is not available in several circuit simulators. Finally, there is some confusion in the literature regarding the definition of loaded Q for this technique and the corresponding predictions of phase noise. This is because when oscillation occurs, the negative resistance cancels the positive resistance in the circuit. Strictly speaking, no resistance means no losses and infinite Q. This is, of course, nonsensical when using Q to determine phase noise as is classically done using Leeson's equation

(58),(33). Hamilton (77) presents a noise analysis of negative-resistance oscillators and gives apparently strict equations. However, others (78),(79) state that this analysis does not permit strict prediction of phase noise.

3.4 Transmission Analysis with Virtual Ground

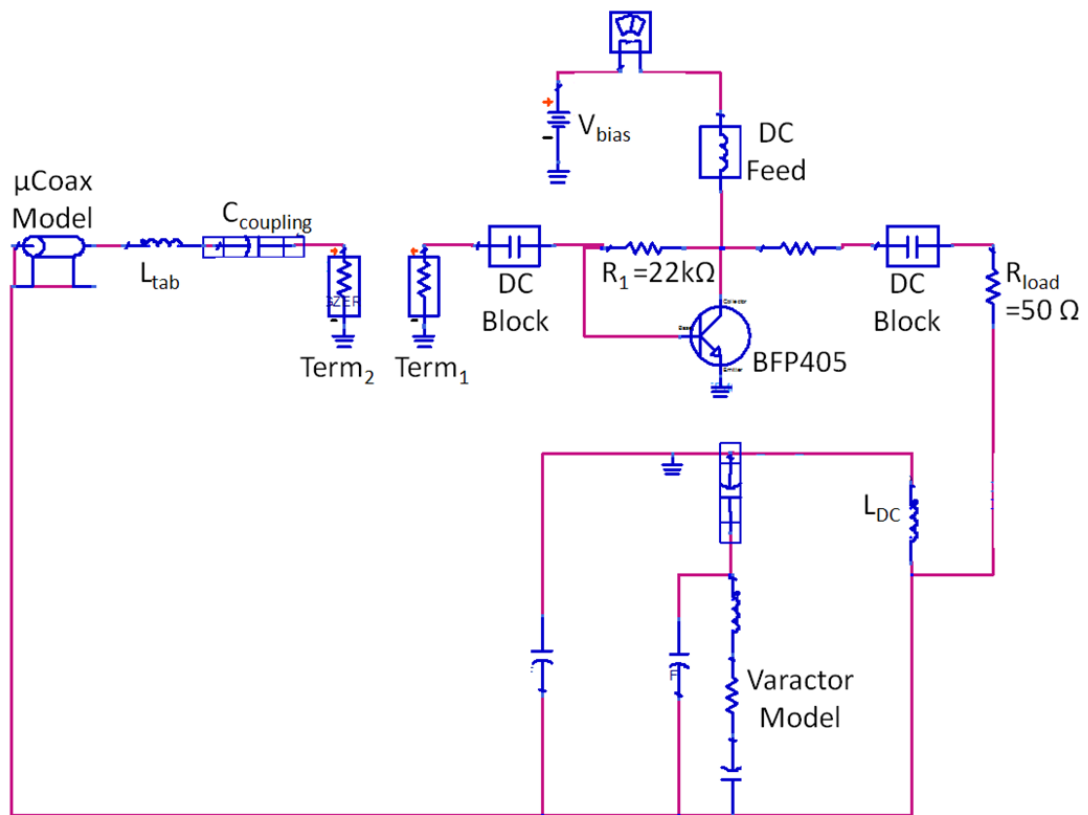


Figure 34 – The circuit used to implement the TAVG analysis on our oscillator design. Maintaining bias conditions after the insertion of a virtual ground permitted use of the transistor model instead of a bias-dependent S-parameter block. Good matching at both sides of the break point resulted in a transmission analysis that largely preserved the action of the oscillator loop.

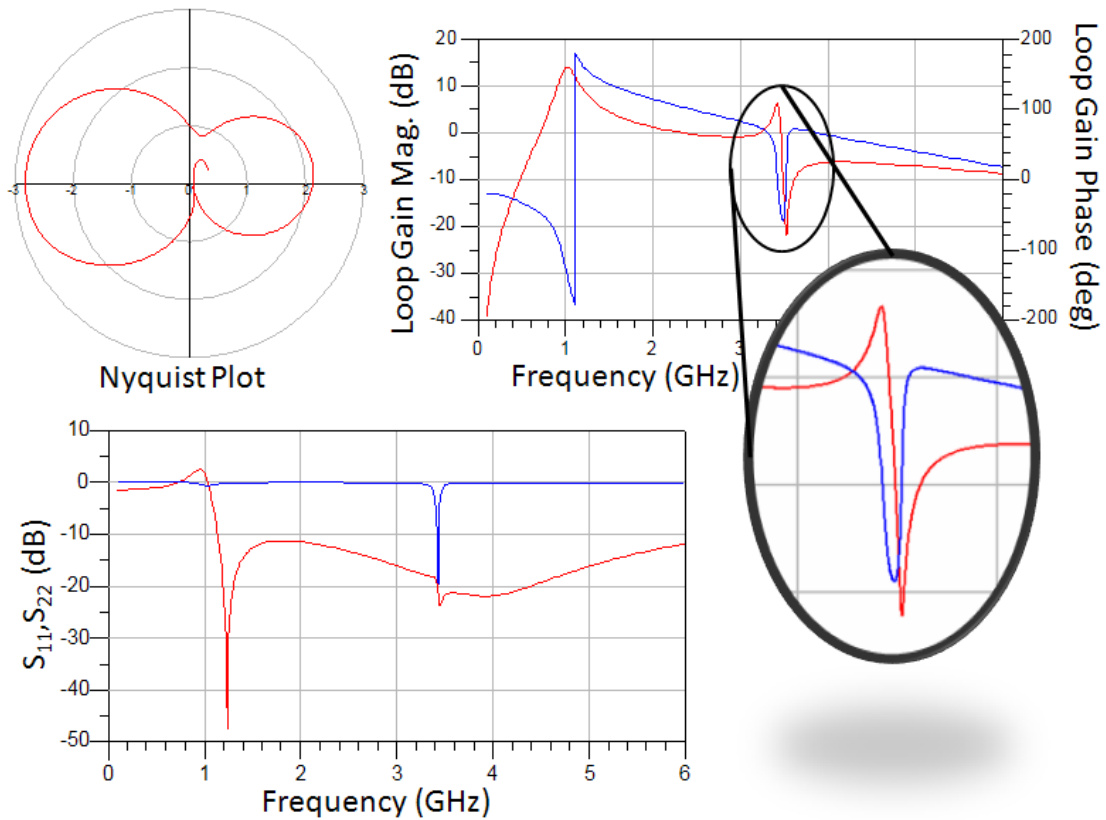


Figure 35 – The results of the transmission analysis with virtual gain from Figure 34. These can be compared to the results from the negative resistance method and the HB method in Figure 33 and Figure 38, respectively. Good agreement in terms of frequency and stability are shown. The Nyquist plot shows clockwise encirclement of the (1,0) point, indicating oscillation is likely. The steep slope of the phase of the loop gain indicates a high-Q design. A good match is shown at the input and output terminals in the opened loop.

Often, when designing for a frequency as precise as that required for CSAC applications, the measured oscillation frequency will be slightly incorrect. In this case, it is desirable to have a design method that shows the shape and nature of the feedback loop and its dependence on circuit components so that the oscillator can be methodically tuned, rather than having the designer guess. To achieve such an insight, we implemented a two-port method of analysis called Transmission Analysis with Virtual Ground (TAVG)(63). This analysis makes use of the essential equivalence of the circuits shown in Figure 29. The primary difference in these circuits is the location of the ground reference point. In circuit simulators, it is possible to change the reference point without affecting the simulation in the ideal case where DC biasing is preserved. However, for circuits that are on the order of a wavelength in size, the introduced reference nodes may be separated by a significant delay. To some extent, this delay can be simulated by the insertion of time delay in the simulation. Our oscillator is well suited for transmission analysis because of its small size. Therefore, time delay was only added in the simulation when integrating the LO with the physics package increased the overall circuit size.

The oscillator was analyzed as shown in Figure 34. The new reference point was chosen as the emitter of the BJT, because this is the location that is common to both controlling and controlled currents, allowing the oscillator to be divided into a CE gain block separated by a feedback network. The load resistor is considered part of the oscillator and its role in the feedback network becomes clear with TAVG. Typically, using the TAVG approach, the transistor must be

replaced by the equivalent s-parameter block at a given bias. However, our circuit topology maintains the DC bias, enabling quick tuning of bias levels and quick transition between the topologies for Harmonic Balance analysis and TAVG.

Once the reference point was determined, a break point was chosen to analyze the transmission properties of the oscillator. The goal is to preserve as much as possible the reflection and transmission properties of the connected point in the loop while being able to observe the overall transmission. Two methods have been proposed in the literature. Alechno (63) recommends the simulation of a cascade of open-loop oscillators that are identical. This method is somewhat undesirable because it increases simulation time and compounds errors in the circuit, it still has one improperly-modeled interaction at the break point, and it is not an elegant method. Harada (72) has left the port mismatch intact and derived equation (3.5) to account for the introduced reflections. This equation is, however, less valid as $|S_{12}|$ becomes large.

$$LoopGain = \frac{S_{21}}{1 - S_{11}S_{22}} \quad (3.5)$$

In general, we have chosen to implement a conjugate match at the input (term 1 in Figure 34) by setting the impedance of term 1 equal to the conjugate of the reflection coefficient seen looking into the gain block. The second terminal, term 2, is then given the same impedance as that seen looking into the resonator block. This preserves one reflection that is ideally the same as in the one-port topology. The first terminal is used to inject power into the loop with as little

reflection as possible, thus preserving the proper transmission properties. The choice of break point could be either the input or the output of the transistor. We chose the input location because we were able to design both ports to be near real values at this location. As seen in the S11 plot in Figure 35, ports 1 and 2 are well matched near 40 ohms.

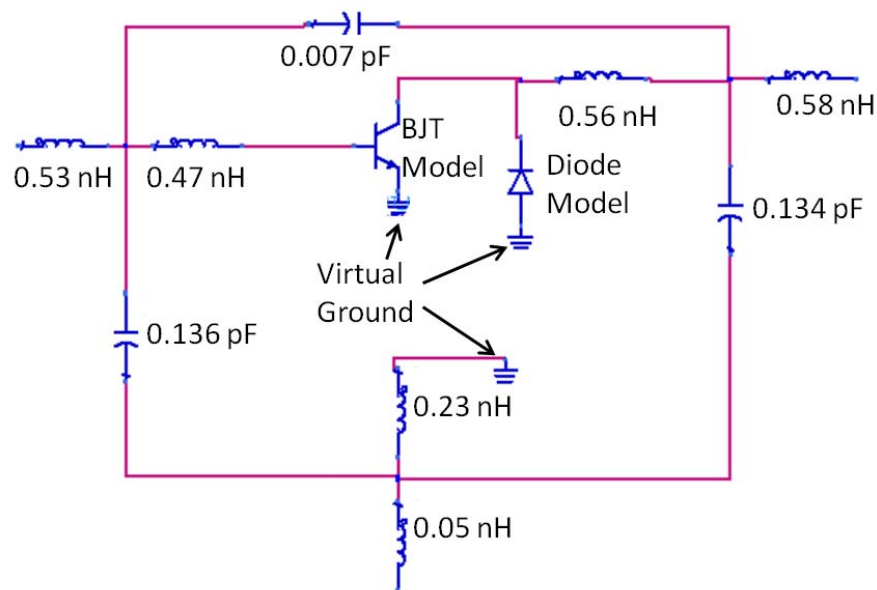


Figure 36 – The active device is shown here with the virtual ground applied at a location inside the package equivalent circuit. This technique can be used to reduce the bilateral action of the transistor, mostly due to the base-collector parasitic capacitance.

Using any of the above methods to break the loop requires a near unilateral amplifier in order to observe a correct loop gain. In our case, $|S_{12}|$ was small for our operating conditions (relatively high voltage and low current bias.) Nevertheless, we were able to reduce this reverse transmission by removing the

package parasitic model from the transistor model as shown in Figure 36. It may also be useful to remove the internal base-collector parasitic capacitance and the internal emitter inductance. To accomplish this, the designer should find the equations used to determine these parasitic values in the device model. In our case, the equivalent base-collector capacitance was of the same order of magnitude as the package parasitic value, and the device was close to unilateral. Since these values are modeled as distributed elements connected to other distributed elements, this final method should be used only in the case of a strongly bilateral device.

The results of the simulation shown in Figure 34 are shown in Figure 35. We observe a zero phase crossing at 3.425GHz and a gain margin of 6 dB. This gain margin was shown sufficient to start oscillation in both harmonic balance analysis and measurements. The phase slope was also optimized to increase overall loaded Q and to decrease phase noise. A combination of components were varied to improve the phase slope, with the match and frequency selection mostly determined by the resonator coupling capacitor and the phase slope and total phase shift mostly determined by the emitter coupling capacitors. Using this analysis, it is seen that a reduction in the series emitter-connected capacitor will cause the phase to be less negative and will increase the gain margin, driving the device harder into compression. This is not desirable because the greater compression can result in increased $1/f$ device noise (73). Similarly, an increase in loop phase shift due to larger emitter coupling capacitors will cause the oscillator to operate near the region of lesser phase slope, and a corresponding

increase in phase noise is observed in harmonic balance analyses. The tuning effects of the varactor model are also easily seen in the analysis. Decreasing bias voltage causes an increase in varactor capacitance, reducing the overall phase shift, and tuning the oscillation frequency lower. In initial designs, series coupling of the varactor was chosen using this method such that this tune range was approximately 3 MHz. If the capacitor is made too small, the phase shift does not cross zero at resonance and no oscillation occurs. This is confirmed with harmonic balance in that the same value of capacitances that reduce the gain margin below approximately 1, or that reduce the phase shift such that it no longer crosses 0 degrees, also yield no oscillation frequency in harmonic balance analyses.

Finally, the Nyquist condition can be plotted as shown in Figure 35. This shows the three conditions required for oscillation. Gain greater than one at zero phase shift is seen by the loop gain being greater than one in the polar plot. Clockwise encirclement of the (1,0) point is required to achieve a right-plane pole in the loop gain. These criteria are also shown in the loop gain plot of Figure 35 as a zero phase crossing with gain greater than one and a negative phase slope.

3.5 Harmonic Balance Implementation

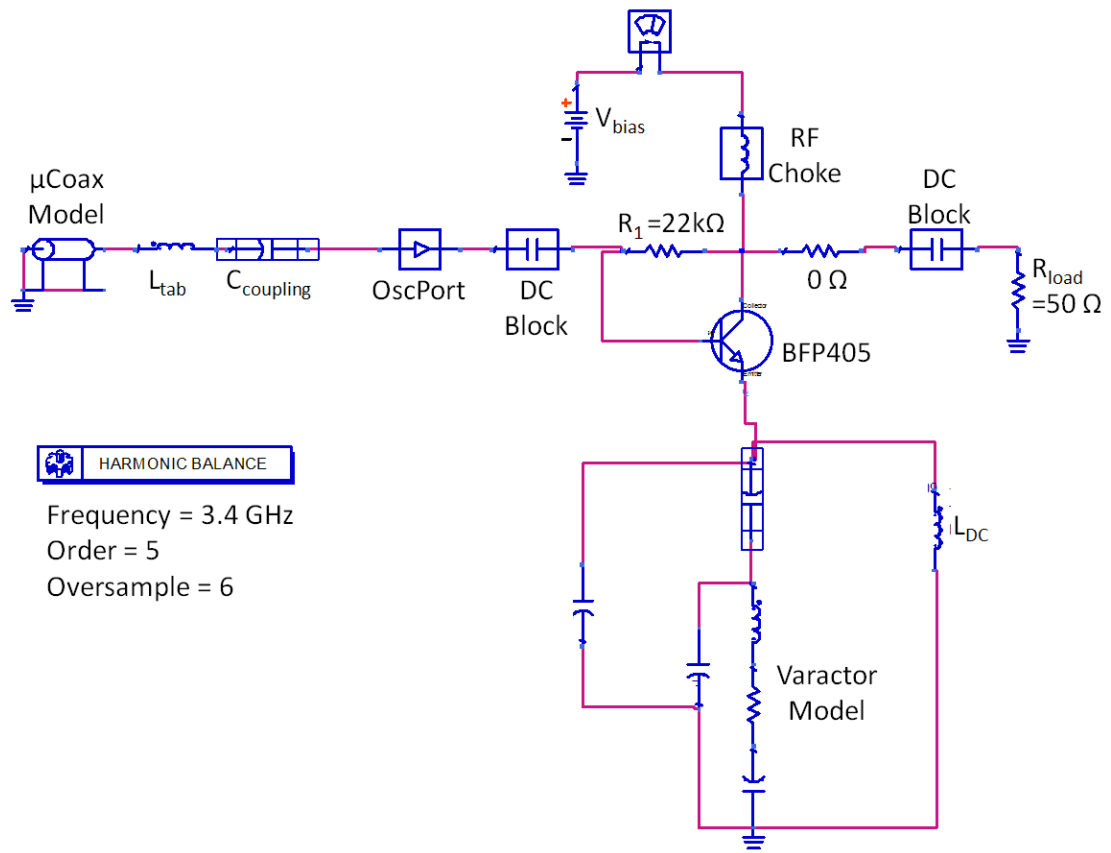


Figure 37 – The circuit used for harmonic balance analysis. The simulation order was set to 5 and the fundamental oversample was set to 6. Models are used for the resonator, varactor, transistor, and coupling capacitors.

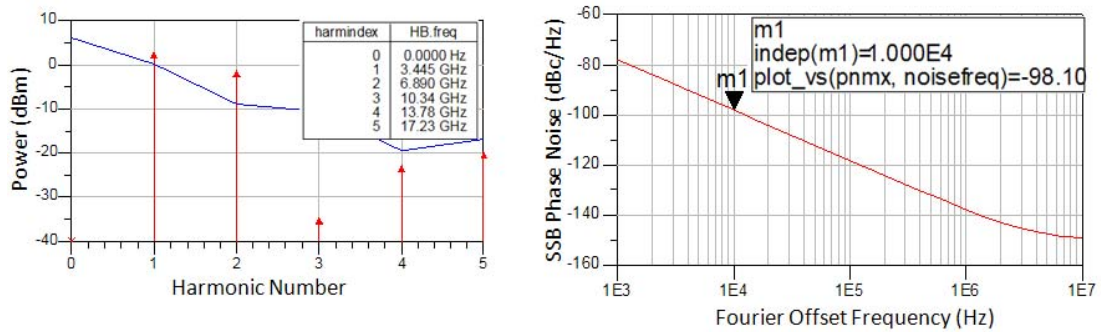


Figure 38 – The results of harmonic balance analysis. Output power at the fundamental is set to 2 dBm. A large second harmonic is observed. The phase noise at 10 kHz is low at -98 dBc/Hz at a 10 kHz offset.

Harmonic Balance (HB) analysis is a nonlinear solution method that solves multiple frequency equations concurrently, while varying the operating point power levels. An introduction to the HB method can be found in (70),(69). Recently, the introduction of Krylov subspace methods, proposed by Freund and Golub (80) has significantly reduced the computer simulation time required to solve the network matrices, especially for large or highly nonlinear circuits. The main output characteristics given by a HB analysis are:

- Oscillation frequency
- Complex node voltages and mesh currents at harmonic frequencies
- Time-domain waveforms of node voltages and mesh currents
- Average power dissipated in circuit elements
- Power levels of harmonics
- Phase noise (for a suitably capable simulator)

Our analysis, shown in Figure 37, makes use of the nonlinear simulator component OscPort in ADS. This component checks for the loop gain condition by becoming an isolator at the fundamental frequency while short-circuiting the harmonics.

For the simulation to be accurate, the number of harmonics (order) should be set such that the highest frequency simulated is within the allowed range of component device models. Otherwise, this value should be set as high as possible to allow accurate determination of the phases and amplitudes of the first few harmonics. Comparing circuit simulations while varying harmonic levels, we set the order to 5, noting little change in the first three harmonics when it is set to 4 or 6. The oversampling parameter was set at 6, an intentionally high value in order to be able to observe voltages and currents with rich harmonic content, due to the large nonlinearity of the oscillator in compression. The more nonlinear is the circuit, the higher should be the oversample, but at the expense of longer simulation time. We observed the convergence of HB simulations and determined that an oversample of 6 gave excellent convergence with an acceptable simulation time.

Our results, shown in Figure 38, show an oscillator optimized for phase noise with a designed output power of 2 dBm. The high second harmonic could be problematic if radiated to the atoms in close proximity. This is because coherent population trapping of the atoms could be destroyed by this harmonic, which is at the hyperfine ground state splitting frequency. However, we did not observe this to be problematic in practice, partly due to the shielding of the

oscillator and also due to the poor modulation efficiency of the VCSEL at this frequency. The phase noise plot in Figure 38 does not show a flicker noise corner due to the absence of a $1/f$ noise model for the BFP405 transistor. It was assumed that this noise corner occurs near 10 kHz, as is typical for Si BJTs. Comparing these results with those achieved using the other techniques, we see good agreement. The frequency obtained with HB is lower than that simulated using TAVG. This can be expected due to the differences between the nonlinear analysis and the linear technique.

Chapter 4

4. Oscillator Fabrication and Characterization

4.1 Oscillator Layout and Construction

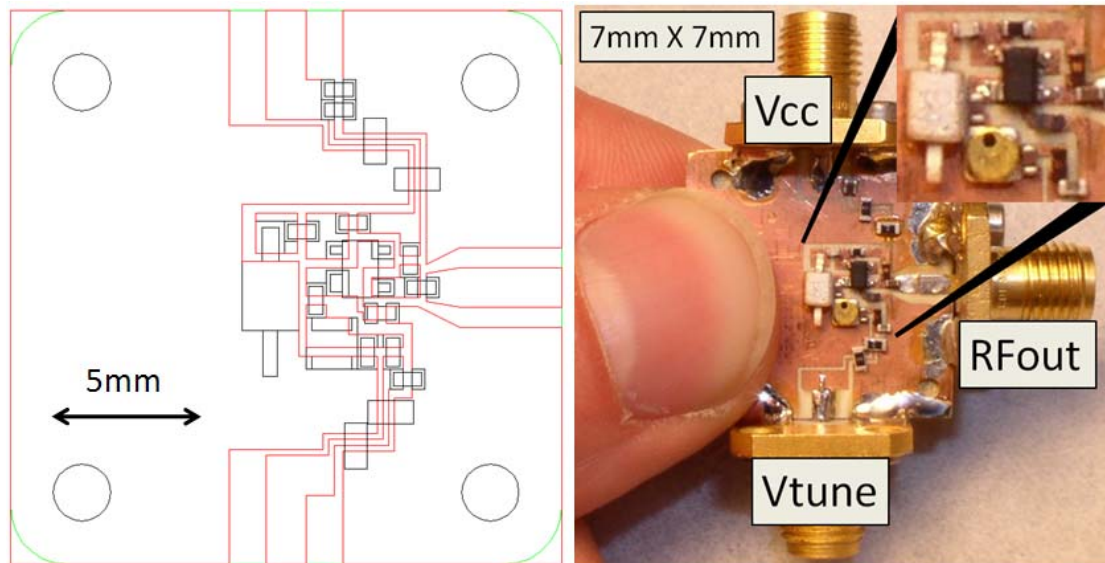


Figure 39 – The layout (left) and completed circuit (right) of the VCO. The VCO occupies 0.5 cm^2 of board space. Power supply decoupling capacitors are mounted to reduce noise and surface-mount zero-ohm jumpers are placed across the DC connections to maintain ground continuity. A coplanar design permits surface-mountable components, a CPW transmission line output, and reduced thermal conductivity due to the absence of vias. The back side of the board is metalized to reduce field coupling to the surroundings.

The layout, shown in Figure 39, is designed as a coplanar structure, with 1-oz metallization on the top and bottom of a Rogers 4350 substrate, which has a relative permittivity of 3.48 and a loss tangent of 0.0032 at the design frequency. The output is a 50-ohm grounded coplanar waveguide (CPW). When integrated with the physics package of a CSAC, as will be described in the next chapter in

more detail, the CPW is extended to reach the VCSEL laser diode. For characterization, a CPW transition to an edge-mountable SMA connector is implemented. The back-side ground is used to help prevent fields coupling from changing the operating characteristics and to permit mounting on several structures, such as the brass test fixture shown in Figure 39. This allows for the necessary CSAC locking and thermal control circuitry to be integrated on the bottom layer, with vias potentially carrying voltages to the VCO and to MEMS heaters on the rubidium cell and VCSEL.

The VCO has two inputs, a DC bias port and a DC voltage tune port. The power supply noise on the bias line is filtered with two capacitors (typically 1 nF and 0.1 μ F) to ground, and an RF block is provided by a 12 nH inductor operated near the high-impedance parallel resonant region. This inductor is mounted as close as possible to the VCO in order to eliminate 6-GHz bias-line instabilities. The tune voltage is connected to the cathode of an abrupt-junction varactor and is similarly filtered with a capacitor to ground near the varactor. Due to the 1 kHz to 10 kHz modulation applied to the tune port for locking the VCO to the atomic resonance, the capacitor is removed or reduced to 1 nF in the version integrated with the physics package, as shown in the next chapter.

The test circuit, shown in Figure 39, is milled from a single piece of brass to allow a solid mount, a good heat sink, and a brass lid for electrically shielding the LO during phase noise measurements.

The footprint of the VCO is 0.5 cm². All components are commercially-available to provide a repeatable and inexpensive design. The tight layout

increases the effectiveness of the transmission analysis with virtual ground, presented in chapter 3, since the ground node is considered to be lumped in that analysis. The largest component is the resonator, with a size of 2 mm X 2 mm X 3.5 mm and sets a size limit for the VCO, since other components can be reduced further in size by smaller surface-mount components or as an integrated circuit with an external resonator. Other components are chosen as size 0402 (40 mils by 20 mils) and are surface-mountable for ease of placement and re-working to fine-tune operating frequency and phase noise, based on the transmission analysis with virtual ground technique.

4.2 Power Consumption and Output

Bias (V)	DC Power (mW)	RF Output (dBm)
1.90	7.6	2
1.50	4.5	-2
1.30	2.8	-5
1.20	2.1	-6
1.00	0.7	-16

For optimal performance, the VCSEL should be driven by a specific amount of RF signal, with a minimal amount of DC power and simultaneous low phase noise. The power necessary to optimally modulate the Ulm VCSEL in the

rubidium-based CSAC was measured to be approximately -6 dBm, when delivered into a 50-ohm load(81). The required power for an impedance-matched VCSEL is therefore less than -6 dBm, but for testing purposes, the oscillator shown in Figure 39 was designed to deliver power into 50 ohms. When operated in tabletop experiments (section 4.7), we measured the output power between -5 dBm and -6 dBm for optimal VCSEL modulation. Table II shows the measured DC input power corresponding to measured RF output power levels. The desired output power of -6 dBm requires approximately 2.1 mW of DC power at 1.2 V. The low efficiency of approximately 10% is an acceptable trade-off to achieve low phase noise. The VCO begins operation at 1.0 V and at a current that, according to the datasheet, yields a transistor f_T value that is 6.8 GHz, which is twice the frequency of operation. Section 2.2 discussed this requirement and the chosen transistor satisfies desired specifications.

For the power measurements, a 9 dB attenuator was attached at the RF output of the test board shown in Figure 39. This provided a stable 50-ohm termination while the output of the attenuator was fed to a calibrated RF power meter. The voltage and current were simultaneously measured to determine DC power consumption.

The output power can be increased by reducing the resistance connecting base to collector in the schematic shown in Figure 37. This was done, as shown in section 4.6, to improve phase noise. In this case, the simulation-based design procedure was repeated with the new component values to provide a more reliable estimate of frequency and phase noise.

4.3 Thermal Sensitivity

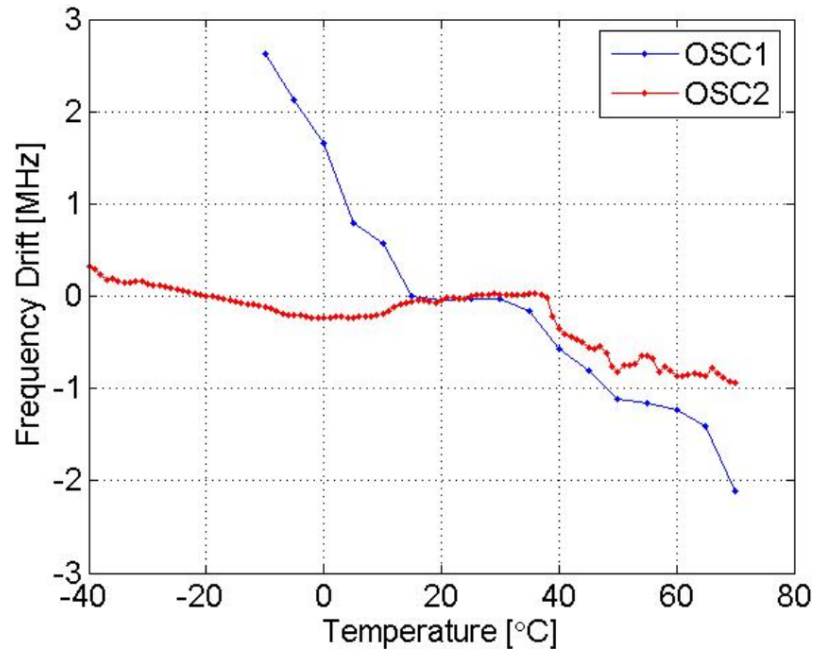


Figure 40 – Measured frequency drift with temperature. With no thermal feedback control, the drift in both oscillators is minimized near room temperature. This measurement was performed by Milos Jankovic while at Rockwell Collins.

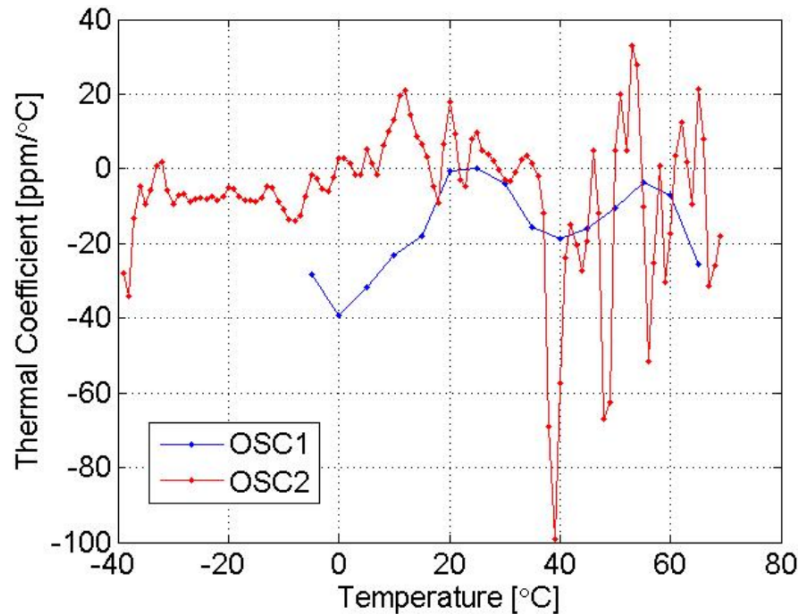


Figure 41 – Measured thermal coefficient of frequency drift in ppm/°C. The oscillators are most stable near room temperatures. The drift increases significantly near 40 °C.

Initial measurements of thermal stability were obtained by bolting a power resistor to the brass test set block of Figure 39, and adding thermally conductive grease. A feedback control circuit was used to stabilize the temperature based on a voltage measured across a thermistor affixed to the brass test set. The set voltage (and hence the temperature) was changed by a potentiometer. The temperature was adjusted by 10 °C and the frequency was read on a spectrum analyzer after several seconds, when it appeared to stabilize on a frequency. This method was intended merely to determine an estimate of the frequency tuning versus temperature. Above 50 °C, we observed significant drift, making the measurement particularly inaccurate. At frequencies near

room temperature, repeated measurements showed fractional frequency shifts less than 10 ppm/°C in magnitude. This might be due to thermal drifts in the COG-type capacitors used in the design, particularly the series coupling capacitor that forms part of the resonator. These capacitors are specified 0 ± 30 ppm/°C near room temperature but have wide tolerances away from room temperature.

For a more accurate measurement, the VCO was cycled in a temperature-controlled chamber from -10 °C to 70 °C at 5° increments and allowed to stabilize at each temperature step. The frequency at each step was measured with a frequency counter and the results are shown in Figure 40 as OSC1. The calculated thermal frequency instability versus temperature is shown in Figure 41, in ppm/°C. At room temperature, the oscillator has thermal frequency instability of approximately 0 ppm/°C. The expected operating temperature range of the CSAC is 0° C to 50° C(82)(83). Over this range, the total frequency shift due to temperature is 2.9 MHz, representing an average thermal drift of -17 ppm/°C with a peak of -40 ppm/°C at 0°C. This thermal drift range was a primary consideration when setting the voltage tune range of the VCO to 3 MHz. A second oscillator with the same layout and similar lumped-element component values was measured in a thermal chamber at Rockwell Collins. For this measurement, the VCO (OSC2) was slowly cycled between -40 °C and +70 °C in a temperature chamber. The frequency, read on a frequency counter, was monitored with a computer program. The results are shown in Figure 40 and Figure 41 for every one degree increment. Figure 40 shows the normalized frequency change in MHz as temperature is varied. Figure 41 shows the rate of

frequency change per degree Celsius at every temperature point. Near and below room temperature, the oscillator shows thermal frequency drift near 0 ± 20 ppm/ $^{\circ}\text{C}$, with the rate worsening at higher temperatures. Over the range of -40 $^{\circ}\text{C}$ to 25 $^{\circ}\text{C}$, the oscillator exhibits less than 1 MHz of frequency change, representing an average thermal drift less than ± 10 ppm/ $^{\circ}\text{C}$. Above 30 $^{\circ}\text{C}$, the performance degrades.

4.4 Vibration Sensitivity

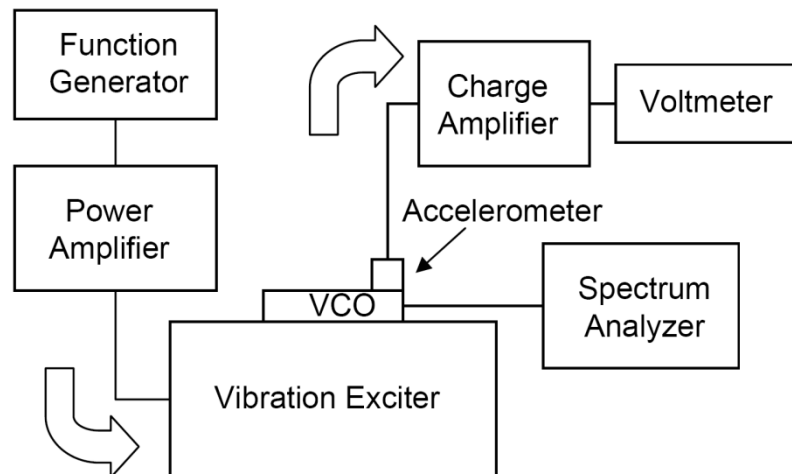


Figure 42 – Setup used by Milos Jankovic for the VCO vibration sensitivity measurements at Rockwell Collins.

The schematic for the vibration sensitivity tests is shown in Figure 42. In this measurement, the oscillator is tightly connected to the vibration fixture. A sinusoidal modulation frequency from a function generator is amplified and sent to the vibration fixture to vibrate the. An accelerometer is placed on top of the oscillator to measure the acceleration F_G . The current from the accelerometer is

measured on a voltmeter after a transimpedance amplifier stage. The spectrum analyzer is used to observe modulation sidebands around the carrier; the power levels of the main carrier and the sidebands are measured and compared as in equation (4-1).

$$P_{dBc} = 20 \log \left(\frac{\Delta f}{2 f_m} \right) \quad (4-1)$$

where P_{dBc} is the power level difference between the main carrier and a sideband, Δf is the frequency deviation solved for, and f_m is the modulation frequency. The sensitivity is then converted to parts-per-billion per g (ppB/g) using equation (4-2)

$$sensitivity = 10^9 \cdot \left(\frac{\Delta f}{F_G f_0} \right) \quad (4-2)$$

Using this method, the sidebands were typically lower in power than the noise around the carrier for vibration frequencies less than 10 kHz. The measurements were performed at 10 kHz because of this, and because 10 kHz is a standard modulation frequency for vibration testing. The vibration sensitivity was measured at 200 ppB/g and 350 ppB/g for two oscillators. These results are superior to typical DRO performance and to typical crystal oscillator without active stabilization or vibration damping(84).

4.5 Frequency Selection and Tuning

The VCO must be capable of tuning precisely to the hyperfine resonance frequency used for chip-scale atomic clocks(29),(11). However, as mentioned in

section 1.5.3, the voltage tuning range must remain small to permit precise frequency control. Therefore, it was expected that tuning would be accomplished, at least in preliminary designs, by manually replacing the components. The intuition gained by use of transmission analysis with virtual ground is valuable in determining which components to vary in order to tune the frequency without significantly increasing phase noise. The tuning range was initially set at 3 MHz based on measured thermal frequency drift and simulated part tolerance changes. The usefulness of this range is verified by the thermal sensitivity measurements of section 4.3. The simulations proved accurate enough to reliably result in first-try oscillator designs within a few tens of MHz of the correct frequency. Frequency tuning less than 10 MHz was accomplished by manually tuning the resonator as described in section 2.1. For larger frequency steps, component values were changed. Decreasing the emitter-to-ground capacitance and decreasing the resonator coupling capacitance both increase the resonant frequency. Changing the resonator coupling capacitance will also change the slope of the phase near resonance, typically resulting in degraded phase noise. However, changing the emitter-to-ground capacitance causes an overall phase shift without changing the shape of the transfer function, thus preserving the Q. This emitter-to-ground capacitance is made of a parallel combination of a capacitor and an abrupt varactor diode that is lightly coupled to the circuit with a series capacitor. A small increase in frequency is therefore observed by increasing the bias voltage (lowering the capacitance) of the varactor. Larger changes in frequency are accomplished by changing the

parallel-connected capacitor. The voltage frequency tuning is nonlinear due to the choice of an abrupt varactor diode. Hyperabrupt diodes are more linear but have a degraded Q due to increased series resistance. The voltage tuning sensitivity of the oscillator shown in Figure 39 is approximately 500 kHz/V near low tuning voltages (1-3V) and reduces to 100 kHz/V near high voltages (5-10 V).

4.6 Phase Noise

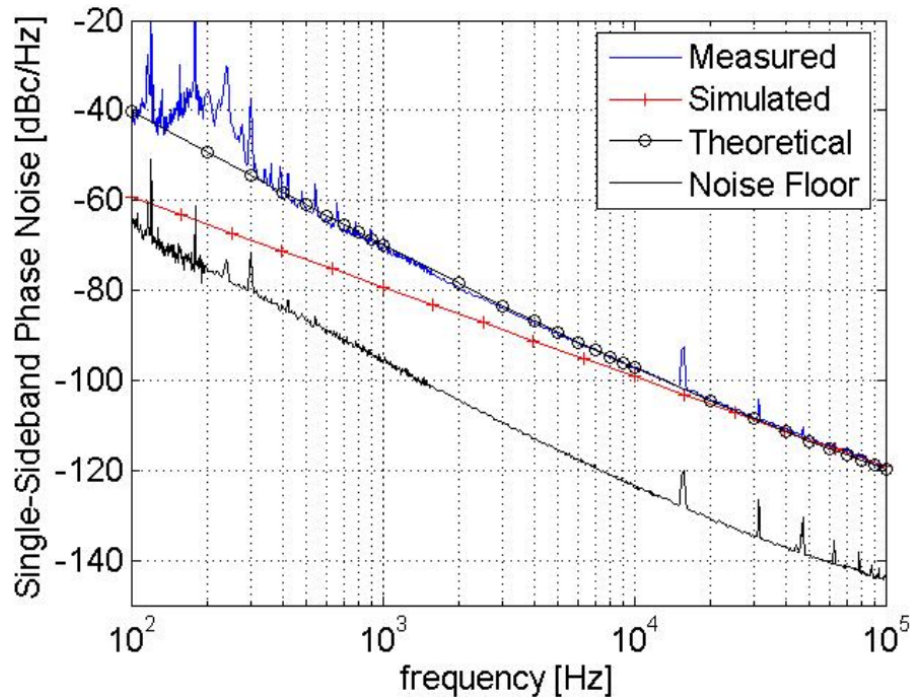


Figure 43 – Phase noise performance of an optimized VCO consuming less than 3 mW DC power. Simulated and theoretical values are shown for comparison. The noise floor of the measurement system is shown.

The phase noise of the 3.4 GHz VCO was measured out to a 100-kHz offset, using the discriminator method(85), with a 125-ns low-loss coaxial delay line. This measurement was verified by evaluating a commercial DRO and comparing to the DRO phase noise obtained from the manufacturer, who used an Agilent E5500 phase noise measurement system. Our discriminator measurement system has a noise floor, shown in Figure 43, more than 20 dB lower than the measurements.

As shown in Figure 43, the phase noise measured at a 10-kHz offset is -97 dBc/Hz. The close-in phase noise is better than -35 dBc/Hz at a 100-Hz offset. These results represent our best phase noise performance at 3 mW power consumption. To achieve optimal phase noise, we tuned the overall loop phase shift as shown in section 3.4. Higher base to ground capacitance decreased the overall phase shown in simulation in Figure 35. This phase shift moved the operating point (zero-crossing of phase) across regions of low phase slope near the upper and lower extremities around resonance and into a region of maximum phase slope (and maximum Q) near the middle of the negative phase slope region. As the operating position was adjusted in this manner, we observed degradation in phase noise when tuned to lower frequencies, becoming -70 dBc/Hz at 10-kHz offset near the low frequency extreme. For frequencies lower than this, the loop gain was insufficient to sustain oscillations and we observed no oscillation. Tuning in the other direction (by reducing the base-to-ground capacitance) resulted in increasing frequency, passing through a

region of low phase noise, and then into a region of low phase noise. When the phase was tuned consistent with passing the local minimum of Figure 35, another oscillation was observed around 7 GHz. Simulations show that, due to the increased gain that also occurs when decreasing the base-to-ground capacitance, the zero crossing of phase near 7 GHz occurs at a location with loop gain greater than 1.

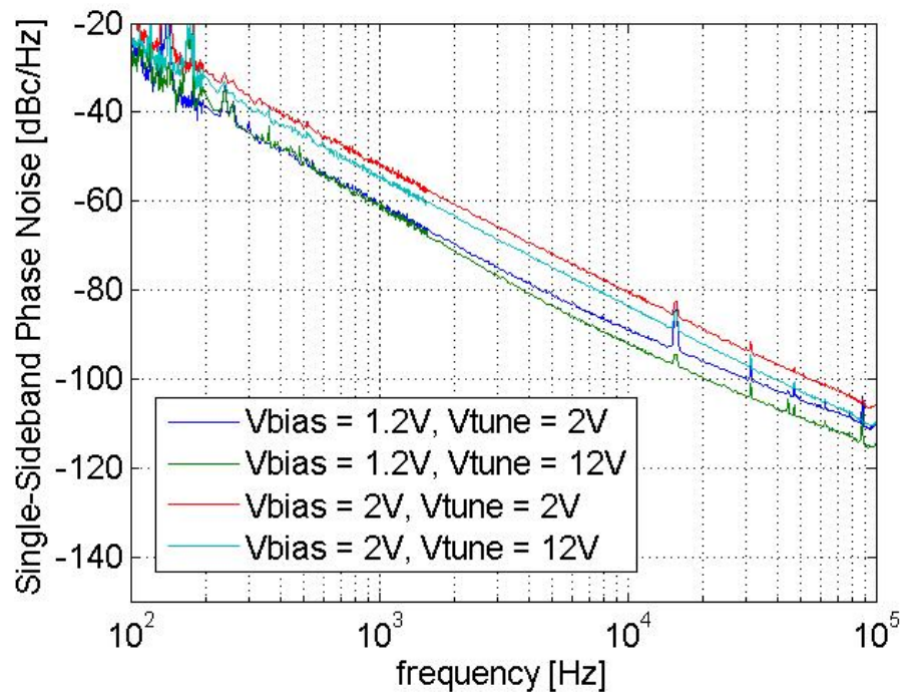


Figure 44 – Phase noise plotted as varactor bias (V_{tune}) is varied from 2 V to 12 V. The results are shown at two different VCO DC bias (V_{bias}) levels.

The effect of tuning on phase noise performance is shown for a non-optimized oscillator in Figure 44. Increased varactor bias represents a small decrease in base-to-ground capacitance. The phase noise change is shown for two different oscillator DC bias levels and for varactor bias of 2 V and 12 V.

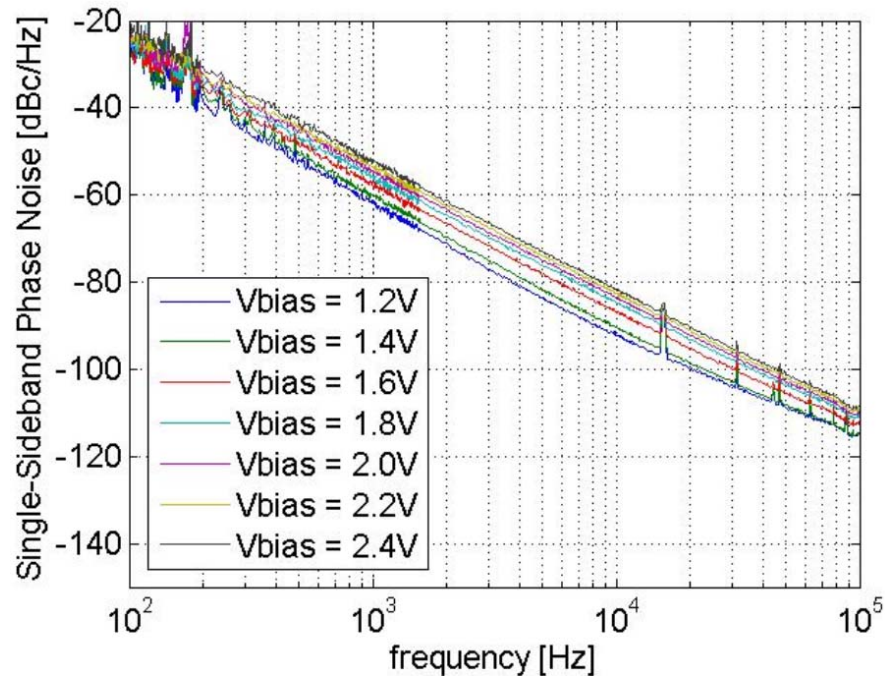


Figure 45 – Phase noise plotted as VCO DC bias (V_{bias}) is changed from the design voltage of 1.3 V to 2.4 V.

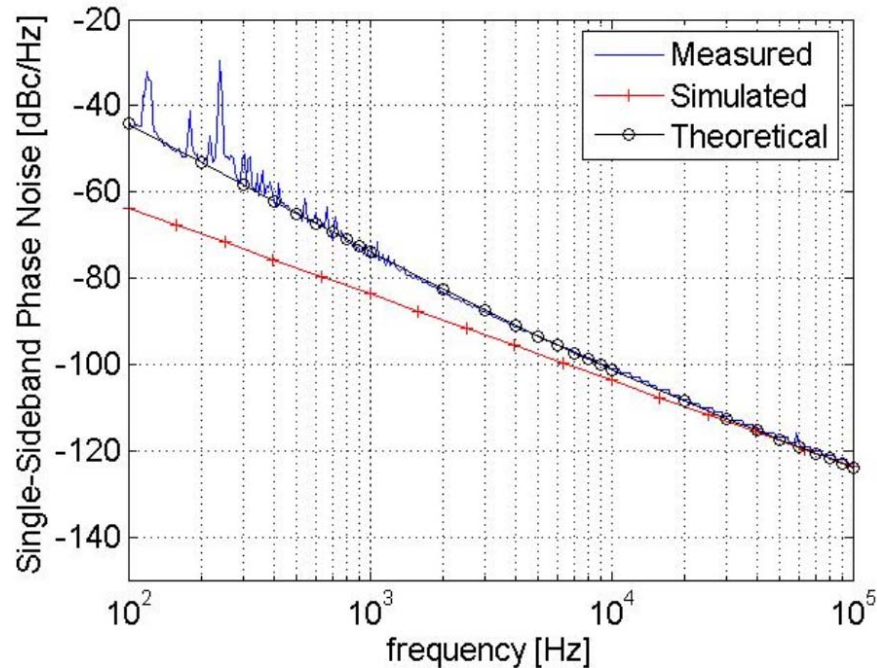


Figure 46 – Phase noise observed, simulated, and predicted for an optimized VCO at an increased power level due to a bias voltage increase to 2.3 V and a reduced base-collector bias resistor of 12 k Ω .

Tuning bias power also tunes the zero crossing of phase because of the change in phase shift through the transistor. This effect is shown in Figure 45 for a constant varactor bias and for VCO bias varied from 1.2 V to 2.4 V. However, increasing the bias power also increases the power available at the input of the gain stage. This can result in an improved phase noise performance as described by Leeson's equation (2-15). When we increased the VCO bias voltage to 2.3 V, redesigned for zero phase crossing, and tuned for optimal phase slope, we observed an improved phase noise performance as shown in Figure 46. Using the simulated input power available at the transistor and the large signal noise figure and flicker corner found in section 2.2.2, the theoretical

performance shown in Figure 43 and Figure 46 was obtained. This predicts the increase in phase slope from -20 dB per decade to -30 dB per decade due to the device flicker noise. The prediction from computer simulation, however, becomes inaccurate for small offset frequencies due to the absence of a flicker noise model in the transistor simulation model.

The optimized results presented here are an improvement over other small-sized, low phase noise oscillators currently available at the time of this work, as shown in table I of section 1.6. State-of-the-art free-running MMIC oscillators typically have low power but a modest phase noise of approximately -80 dBc at 10-kHz offset(86). A notable exception combines an off-chip FBAR resonator with integrated CMOS(87). This is not tunable and the low power was quoted for the oscillator core only. Considering a recent design (35), FBAR-resonator oscillators may prove suitable for CSAC applications if DC power consumption is reduced and thermal frequency drift is compensated.

4.7 Locking to Tabletop Atomic Setup

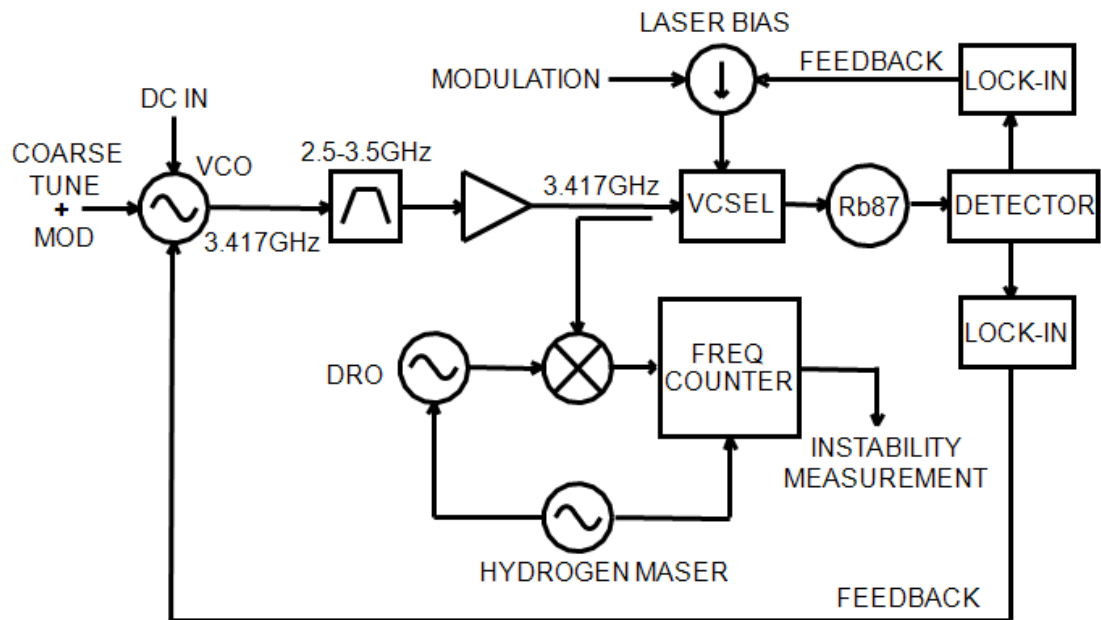


Figure 47 – Diagram of the setup used to lock the VCO to the atomic resonance of Rb atoms and to measure the resulting instability.

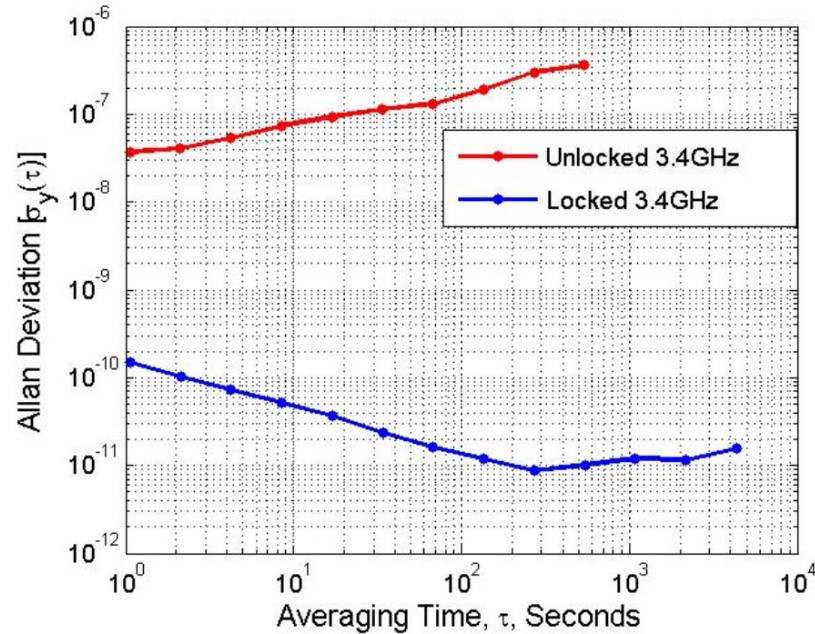


Figure 48 – Measured frequency instability of the VCO locked to the atomic resonance of Rb atoms in a tabletop experiment. The data show a significant improvement over the instability requirement, reaching 10^{-11} before 200 seconds.

To demonstrate sufficient quality for application in chip-scale atomic clocks, the VCO was locked to the CPT resonance of rubidium atoms. The setup was designed to somewhat mimic that used by chip-scale atomic clocks. The diagram of the setup is shown in Figure 47 and incorporates a VCSEL laser diode at the optical absorption frequency of rubidium, an amplifier to recover power lost from attenuators and cables, a 1 cm³ glass cell containing gaseous Rb atoms with nitrogen buffer gas at 1 torr, a photodetector, and the lock-in amplifiers necessary to adjust the VCSEL current and oscillator tune voltage. The inner schematic with the phase-locked DRO, frequency counter, and maser is the setup

used to measure the fractional frequency instability of the oscillator both when free-running and when locked to the resonance of the atoms, as shown in Figure 48. In this measurement, a frequency-disciplined DRO is mixed with the RF output of the VCO and the beat frequency is measured by a frequency counter. The reference for the counter and the stable DRO is a 5 MHz reference from a hydrogen maser ($\sigma_y(\tau) \cong 2 \times 10^{-13}/\tau^{1/2}$).

The atomic experiment provided a CPT linewidth of 4 kHz. The Avalon VCSEL provided a laser beamwidth of 2.5 mm radius and the optical intensity was $860 \mu\text{W}/\text{cm}^2$ in the cell. Optical absorption in the cell was approximately 25% at 33.5 °C cell temperature. The laser temperature was well stabilized but the Rb cell was only marginally stabilized. Thermal fluctuations in the lab could therefore result in some long-term frequency drifts.

The LO was locked by modulating at a frequency of 4.4 kHz and with a similar modulation depth. The LO lock-in amplifier time constant was set to 100 μs and a third-order filter was used, resulting in an 18 dB/octave lock to the atoms. A loop servo filter was used after the lock-in amplifier and was set as a pure integrator with negligible proportional gain.

The measured fractional frequency instability of the locked oscillator is reported in Figure 48. It is evident that the VCO has been locked to the atomic resonance by the large improvement in stability, reaching the value of 10^{-11} at approximately 200 seconds for the 3.4 GHz LO, equal to the DARPA requirement for the chip-scale atomic clock for fractional frequency instability of 10^{-11} at one hour (3600 s) integration time. In this and similar measurements, the instability

worsened as time progressed, due in part to long-term thermal drifts in the atomic system. Similar long-term drifts were observed when using a synthesizer in place of the LO.

Chapter 5

5. Integration of the VCO into Miniature Atomic Clocks

5.1 Overview of the Integrated CSAC

The local oscillator discussed in this thesis and the NIST atomic physics package have been optimized as separate systems using conventional electronics. One of the remaining challenges was the assembly of a fully integrated clock, where limited space and a multitude of signals can result in coupling of components and degraded performance of the system as a whole. This chapter gives an overview of the components that compose the first integrated NIST CSAC (SP1), including an overview of the physics package (PP), control electronics, frequency divider board, and the local oscillator (LO). The

integration of the LO with the PP is discussed. We show the changes made for a second, improved prototype (SP2). The measured results for the prototypes are discussed, including the best reported short-term stability, at the time of our experiment, for an integrated miniature LO and PP. Finally, the limitations of the system and possible improvements are suggested.

The CSAC prototypes consist of three subsystems, the local oscillator, the physics package, and control electronics, as shown in the block diagram in Figure 49. All of these subsystems are integrated into one unit of volume approximately 22.5 cm³. The inputs are three DC voltages supplying a total power of approximately 400 mW. The output is a signal of frequency 3.417 GHz with a fractional frequency instability below 1×10^{-9} between 15 s and 4.5 hours of integration. A fourth subsystem of volume 3.4 cm³ transforms this signal into a 10.00 MHz signal with similar stability, requiring an additional 30 mW of power.

The voltage-controlled local oscillator generates an output of 3.417 GHz, which is sent to the physics package (PP). The latter makes a comparison with the frequency of the atoms, and generates an output signal that depends on the frequency difference between the two. A servo loop implemented in the control electronics (CE) then tunes the LO frequency to coincide with the atomic resonance frequency.

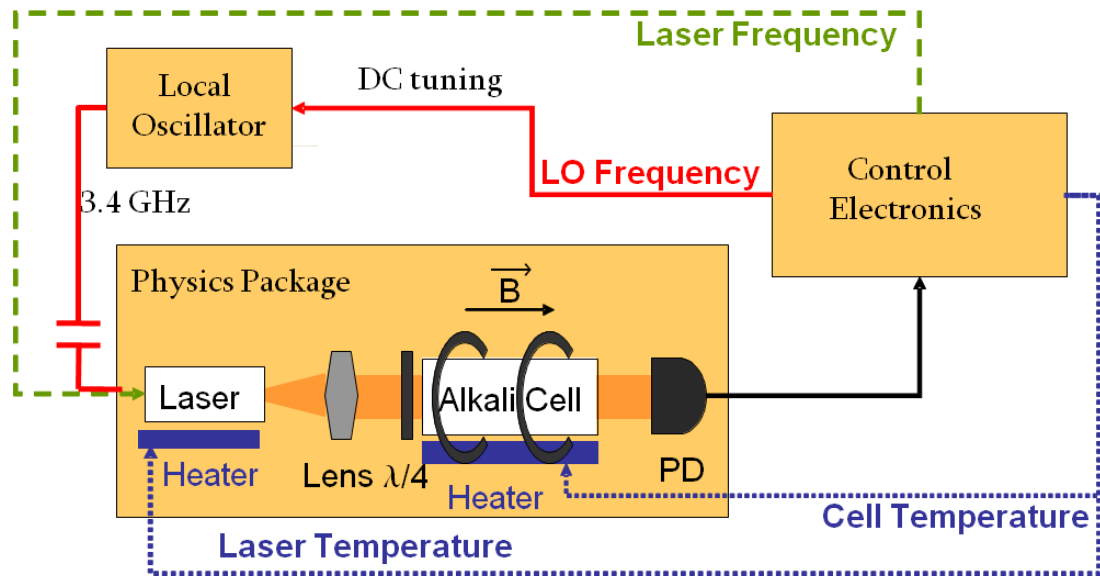


Figure 49 – Schematic of CSAC components, physics package, local oscillator, and control electronics, as well as the four feedback loops for laser and cell temperatures, laser frequency and LO frequency.

5.2 The First NIST-CU Integrated CSAC

5.2.1 The Physics Package

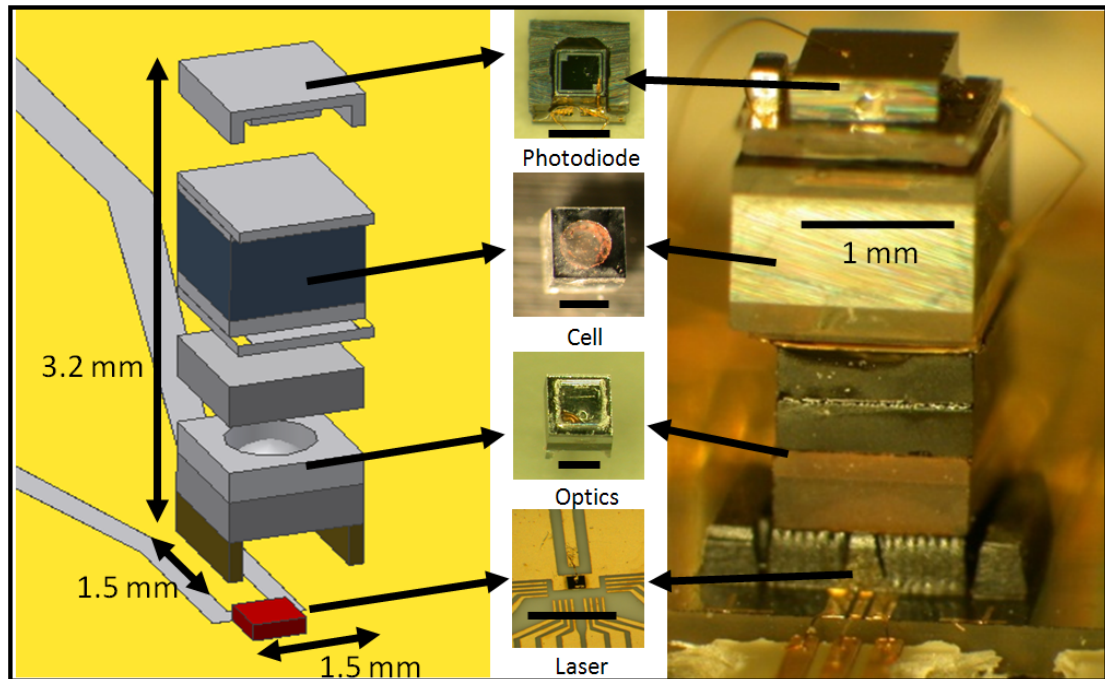


Figure 50 – Diagram and photograph of the NIST physics package, from (88). The vertical integration makes wafer-level fabrication possible. This device, based on Rb atoms, had a volume of approximately 0.1 cm^3 and was able to support a short-term fractional frequency instability of 4.5×10^{-11} at one second.

The NIST physics package is based on a micro-machined atomic confinement cell (11) and all-optical excitation of the atoms using a vertical-cavity surface-emitting laser (VCSEL)(89). With this type of system, NIST demonstrated the first functioning microfabricated atomic clock physics package(89), as well as a physics package with a short-term instability below 10^{-11} .

¹⁰ at one second integration time(90). The system is operated in a standard CPT configuration (91) and the design of the physics package is similar to the one described in (92), where we demonstrated a CSAC at the component level.

The architecture of the physics package follows the vertical integration design developed by researchers at NIST, which makes it compatible with wafer-level assembly technology(92). Figure 50 shows a diagram and a photograph of the physics package. The package is built on a 6×4×0.5 mm quartz baseplate. The vertical cavity surface emitting laser (VCSEL) chip is placed on top of a thin-film resistive heater (resistance 70 Ω), with insulating thin layer between the two, and is wire-bonded to a co-planar waveguide (CPW) line deposited on the baseplate. A 100 kΩ SMD thermistor (0.3×0.3×0.6 mm) used for laser temperature control is mounted next to the laser. A 0.5 mm thick Kapton spacer with a rectangular vertical opening for the VCSEL chip encloses the laser and supports the structure above the VCSEL chip. A 0.5-mm thick AR-coated polarizer is glued on top of the spacer. The polarizer's axis is aligned along the linear polarization of the strongest polarization mode of the VCSEL. The polarizer is covered with an 80 μm thick quarter waveplate, which converts the linearly polarized light transmitted through the polarizer into circularly polarized light. The polarizer eliminates a second, orthogonal polarization mode and leads to an increase in CPT resonance contrast by a factor of 3. However, power fluctuations between the two polarization modes in the laser can result in increased light intensity noise after the polarizer, which can degrade the performance of the clock.

To improve the long-term frequency stability, a set of two neutral density filters (0.5 mm thickness) reduces the laser intensity to approximately $200 \mu\text{W}/\text{cm}^2$. On top of the neutral density filters sits the Rb vapor cell sandwiched between two sets of transparent Indium Tin-Oxide (ITO) heaters. Each heater is a 0.125 mm thick Pyrex plate with a thin ITO film deposited between two bus bars of deposited gold. Each heater set has two such heaters on top of each other, with the current used for heating passing the heaters in opposite direction in order to minimize the magnetic field created by the current.

The vapor cell is manufactured according to the techniques described by Knappe *et al.* (93). It has a $1\times 1\times 1$ mm cavity filled with isotopically enriched ^{87}Rb and a combination of Ar and Ne acting as buffer gasses. The partial pressures of Ar and Ne are chosen to minimize the temperature-dependent shift of the clock frequency(21)(94).

A photodiode is mounted on top of the second heater set. Since the electrodes of the photodiode are on the active side, it is soldered to the gold contacts of a 0.125-mm thick glass plate. Another 100-k Ω thermistor is mounted next to the photodiode, for Rb cell temperature stabilization. Since the photocurrent produced by the photodiode is only a few microamperes, the first stage of photodiode amplification is placed on the physics board as close to the physics package as possible. This positioning also reduces the noise at the power-line frequency of 60 Hz.

The physics package is capped with a rectangular magnetic shield. The shield is made of folded 0.5 mm thick foil of magnetic shielding material. A

permanent magnet is glued inside the shield above the physics package. The permanent magnet creates a static magnetic field of 50 μT parallel to the light direction of propagation. The magnetic field lifts the degeneracy of Zeeman sublevels of each ground state component and isolates the clock transition from the magnetically sensitive ones. (For an explanation, see section 1.3.1.) The quartz baseplate is mounted into a specially machined 6x4 mm slot in the PC board with gold traces that are bonded to the quartz baseplate of the physics package.

A number of diagnostic signals can be monitored to ensure that the CSAC is functioning as expected. These signals (below at left) and the processes they monitor (below at right) are as follows:

- | | | |
|---------------------------|---|----------------------------------------|
| • Laser current | → | Laser aging |
| • Photodetector voltage | → | Laser aging, cell aging, laser lock |
| • Cell temperature | → | Cell aging, cell temperature lock |
| • Laser temperature | → | Laser aging, laser temperature lock |
| • Cell heater current | → | Cell aging, ambient temperature |
| • Laser heater current | → | Laser aging, laser lock, ambient temp. |
| • Laser lock error signal | → | Laser lock integrity |

5.2.2 The Integrated Local Oscillator

The design process described in chapter 3 was used for the LO in the prototype CSACs, resulting in a similar oscillator, with several notable exceptions described in this section. The LO was integrated on the same substrate as the PP and is shown in Figure 51.

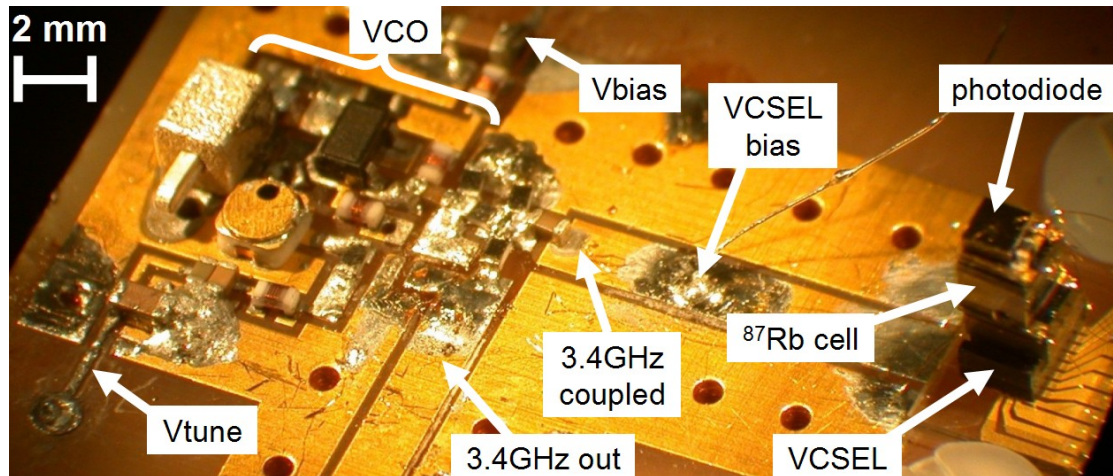


Figure 51 – Photograph showing the local oscillator integrated with the physics package. Separate coupled outputs are sent to modulate the VCSEL and to provide a reference for the frequency divider board (not shown). RF losses due to the VCSEL bias line, 6 dB attenuator, and long bondwires to the VCSEL required an increase in LO power consumption to 8.4 mW.

Integrating the LO and PP can be challenging considering the experimentally-determined requirements: 1.) the 3.4173 GHz frequency should be able to be maintained with a precision better than 340 mHz for one-hour integration times using feedback from control electronics; 2.) the VCSEL should be optimally modulated with approximately -6 dBm of RF power; 3.) more than -25 dBm of useful RF power should be coupled out of the circuit to a frequency divider board; and 4.) low thermal losses are desired for the integrated board.

Although the oscillator was initially designed to have a tuning range of 3 MHz to allow for part tolerances and drift, this range needed to be decreased due to the limited dynamic range of the 12-bit DAC that was used to control the

voltage on the LO tune port. For a 12-bit DAC and a locking time of 1 ms, the tunability must be less than 266 kHz/V to achieve the required stability of 10^{-11} at one hour. Considering that the integrated LO exhibited long term frequency drift generally less than 200 kHz, the tuning range was reduced to this value by reducing the capacitance that series-coupled the varactor to the LO circuit. This modification was completed after the physics package was mounted on the physics board, next to the LO. Separate AC-coupled LO outputs were provided, one to modulate the VCSEL, the other to provide the stabilized 3.417-GHz to the frequency division stage.

A copper shield, shown in Figure 52, was placed around the LO to reduce the effects of frequency variations due to external coupled and radiated fields. Increased shielding was accomplished by soldering the copper shield to the ground plane and by filling holes in the ground plane with solder. Because the proximity of the copper shield affected the resonant frequency, phase-shifting capacitors were used for manual re-tuning, as described in chapter 3, and a tuning screw was mounted in the shield and above the resonator. To provide proper power levels and impedance matching to the VCSEL and to the frequency divider board, a lumped-element coupling circuit was designed but was replaced by a 6 dB lumped-element attenuator because unpredictable transmission line and bondwire lengths led to an uncertain RF impedance of the VCSEL. To overcome the attenuation losses, the LO power consumption was increased from the design in (37) to 8.4 mW by increasing the bias voltage to 3.3 V.

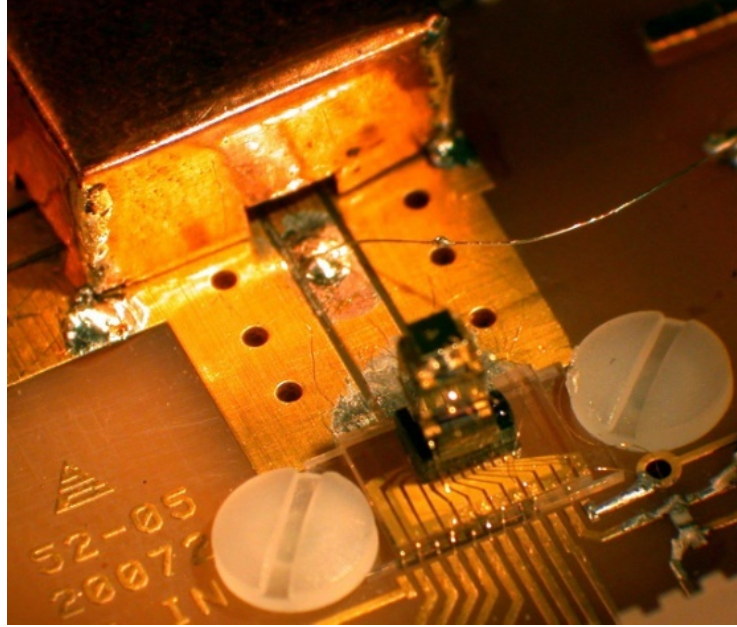


Figure 52 – Photograph of the integrated LO and PP showing the electric shield placed around the LO. The frequency shift caused by this shield resulted in a need to tune the LO frequency by a significant amount (30 MHz), leading to degraded phase noise performance.

With this LO, an output power of -6 dBm was delivered to the 50-ohm coplanar waveguide leading to the VCSEL. This RF power is sufficient to modulate the VCSEL at its optimum modulation index. In addition, a signal with a power level of -20 dBm is delivered as an output to the frequency divider, which divides the RF output frequency to provide the 10 MHz output. By mechanical tuning of the resonator, using both the method described in chapter 2 and the tuning screw, it was possible to tune the LO onto the resonance while maintaining voltage tunability less than 200 kHz/V. However, future designs

will require a 16-bit DAC and separate methods for automatic coarse tuning and fine tuning of the LO frequency.

The FR-4 substrate shown in Figure 51 is larger than would be necessary for a finalized design but allows access to test points and to LO components for frequency tuning and modifications. The LO volume is 0.4 cm^3 , almost half of the total desirable CSAC volume. The physics package fills approximately 0.5 cm^3 (including the magnetic shield) and, apart from thermal power consumption, consumes only 2 mW. Together, this integrated board forms a system that meets the short-term stability specification, using large control electronics, with an Allan deviation of $2.5 \times 10^{-10} / \tau^{1/2}$ for short integration times. Inputs to the board are DC bias and tune voltages for the LO, DC current bias for the vertical-cavity surface-emitting laser (VCSEL), and currents to resistive heaters on the physics package. The outputs are a stabilized 3.4173 GHz reference frequency, photodetector signal for locking the laser's optical frequency to the atomic resonance, and voltages for temperature stabilization of the rubidium vapor cell and the VCSEL. Electronics for temperature control and for locking the VCO to the atomic resonance are external but could in principle be integrated on the remaining board space or on the reverse side of the board.

5.2.3 The Control Electronics



Figure 53 – Photograph of the CSAC control electronics board. This board was placed on the back side of the integrated LO-PP physics board.

The control electronics are primarily designed by Dr. John Kitching at NIST and are based on a digital microprocessor chip Silicon Laboratories C8051F006. A multiplexed 12-bit analog-to-digital converter (ADC) and four 12 bit digital-to-analog converters (DACs; two internal, two external) form the interface between the microprocessor and the analog control board. A photograph of the control electronics board is shown in Figure 53. The board is designed to stack with the physics board of the same size. The two temperature servos use the signals from the thermistors to control the cell and VCSEL temperatures with a proportional-integral (PI) loop. The two frequency servos use phase sensitive detection to lock the VCSEL to the Rb optical transition and the LO to the Rb microwave resonance. In order to do this, the laser current and

LO tune voltage are square-wave modulated at 510 Hz and 1.5 kHz, respectively. The photodetector signal is then filtered by two band-pass filters around these frequencies. Afterwards, the signals are multiplied with the reference signal and low-pass filtered. The filtered signals are digitized by the ADC and software-implemented, user-selected proportional and integral gains provide outputs that are used to lock the frequencies to the zero-crossings of the demodulated signals. One of these outputs is sent to the operational amplifier controlling the frequency of the LO. This locks the LO frequency to one half of the Rb CPT resonance frequency. A phase shift is included through a digital positive or negative delay of the reference signal. In order to implement the four servos, 8 op-amps are required in addition to a number of passive components and an 18 MHz clock chip. A graphical user interface running on a computer is used to communicate with the microprocessor chip and all loops can be monitored and changed in this way. The computer can then be disconnected and the CSAC will run independently.

The control board has a size of $2.5 \text{ cm} \times 4.5 \text{ cm} \times 0.5 \text{ cm} = 5.6 \text{ cm}^3$ and requires 152 mW at 3.3 V. One major limitation originates with the use of 12 bit DACs. In order for the control loops to be able to compensate for large changes in the control parameter, they must have correspondingly rather coarse resolution. With the DACs set for a large enough tuning range, the change of the output corresponding to one significant bit can cause large frequency changes of the clock frequency. For the VCSEL temperature control, a passive preset circuit is therefore implemented, which provides a nominal current into the VCSEL

heater. This nominal current can be modified over a small range by the output of one of the DACs.

The temperature controllers allow measurements of the laser and cell temperatures on the order of 30 mK, limited by the resolution of the 12-bit DACs. To achieve optimal performance, the laser temperature is stabilized in the vicinity of 350 K, and the cell temperature in the vicinity of 360 K. To control frequency shifts due to temperature variations of the temperature-compensated cell used in the clock, such temperature measurement is adequate; a change of 30 mK corresponds to fractional frequency instability of 1×10^{-11} (93). For frequency shifts due to temperature changes of the laser, the temperature measurement limits the clock performance to 2×10^{-11} level. This temperature stability is also determined by the 12-bit resolution of the control voltages that determine the currents through the laser and cell heaters.

The LO servo loop was the most difficult to implement. The dynamic range must be large enough so that the LO does not drift out of this range (several megahertz over 24 hours). This limits the minimum step size for the LO frequency to roughly 45 Hz (or $1 \times 10^{-9}/\tau^{1/2}$). A plot of the Allan deviation of the complete CSAC is included in Figure 57 (red circles). The short-term frequency instability is $1 \times 10^{-9}/\tau^{1/2}$. This is much worse than the measured instability of the system that uses large electronics. One reason is that in order to tune the LO onto CPT resonance with a maximum 5 V tune voltage and to reach sufficient modulation efficiency of the VCSEL at the same time, the VCSEL needed to be

operated very close to its lasing threshold. At this point the FM and polarization noise are large, and the signal-to noise ratio of the CPT resonance is degraded.

5.2.4 The Frequency Divider Board

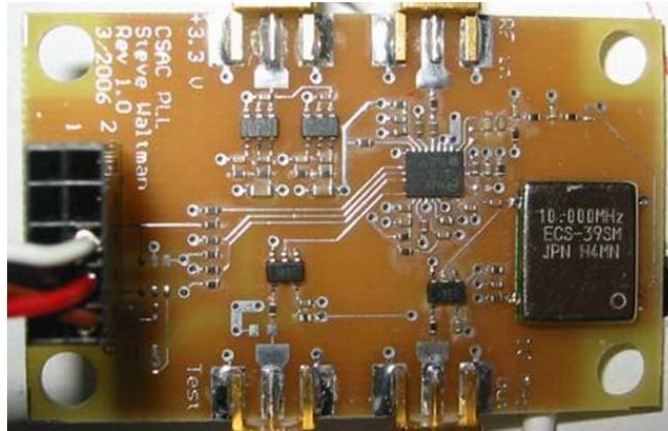


Figure 54 –Photograph of the CSAC frequency divider board. Inputs are DC bias and stabilized RF at 3.4173 GHz and the outputs are two stabilized 10 MHz frequencies and a diagnostic port.

The frequency divider, designed by Steve Waltman, uses a commercial PLL chip LMX2471 to divide the input frequency of 3.417 GHz by a fraction of a number N to reach $10 \text{ MHz} \pm 10 \mu\text{Hz}$. It then phase-stabilizes a TCXO to this frequency. In this way, the modulation sidebands on the LO frequency can be easily eliminated. The divider board has a volume of $2.5 \text{ cm} \times 4.5 \text{ cm} \times 0.3 \text{ cm} = 3.4 \text{ cm}^3$ and requires 30 mW of power, of which 15 mW are consumed by the TCXO. No degradation of the frequency stability of the CSAC could be measured when counting the 10 MHz rather than the 3.417 GHz. Figure 54 displays a

photograph of the divider board. A computer interface allows the user to program the divider. After programming, the computer interface can be disconnected.

5.3 The Second NIST-CU Integrated CSAC

5.3.1 Changes Made

This section describes the changes made between the first (SP1) and the second (SP2) prototypes of the CSAC.

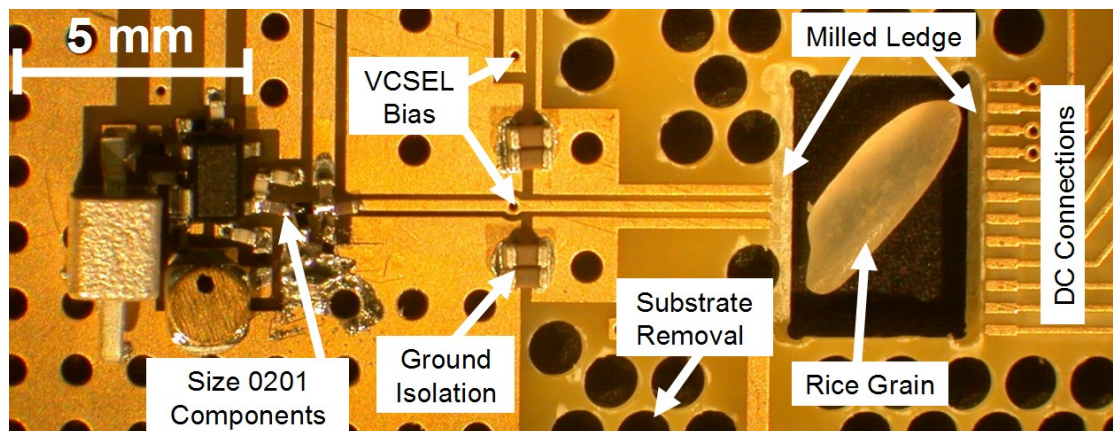


Figure 55 –Photograph of the improved integrated physics board. The physics package is not shown but is replaced by a grain of rice for size scaling, giving a better view of the board layout. Thermal power losses were reduced by the removal of unnecessary substrate material and by the thinning of circuit traces near the physics package.

For SP2, the physics package remained essentially the same as SP1, though higher reliability was achieved by eliminating all electrically-conductive

epoxy, except for the thermistor connections. Also, the electrical connections of the photodetector mount were redesigned to enable wire-bonding. The volume of the structure is roughly 10 mm^3 , and it is enclosed in a magnetic shield of volume 0.47 cm^3 .

The most significant change for the LO was a reduction in size of the passive components of the LO from size 0402 to size 0201 packages. This resulted in a circuit footprint of 0.25 cm^2 , a reduction by a factor of two compared to previous designs. In addition to the benefit of overall size reduction, more accurate design simulations could be carried out since these rely on circuit theory approximations rather than full microwave fields simulations. Since the longest length is less than one-tenth of a wavelength with this design, circuit simulations can be used with acceptable accuracy. Additionally, the component parasitics are lower for size 0201 components.

Several improvements were made to the physics board and the resulting integration of the LO and PP. These were implemented to provide reduced noise and reduced thermal power losses. A picture of the resulting physics board is shown in Figure 55. To reduce noise from the 60 Hz mains, the LO signal and ground were AC-coupled to the laser input with capacitors, eliminating ground loops. This also added some additional protection for the laser against stray voltage spikes. Unwanted RF output coupling to the laser bias line was reduced by adding a high-impedance laser bias line that was connected with series inductors on the board back side. Very short ($<0.25 \text{ mm}$) wire bonds connect

the CPW transmission line to the VCSEL current leads on the quartz baseplate to minimize the RF power lost and mismatch due to wirebond inductance.

Mechanical modifications to the physics board resulted in a measured 20% reduction of heat losses through the conductors and the bulk FR-4 substrate. The thermally-conductive CPW transmission line was made less wide, with fields simulations showing negligible parasitic effects over the short distance between the LO and the PP. The quartz baseplate that supports the PP was inserted into a specially-machined 6x4 mm slot in the PC board. Besides the thinly-milled ledge that supports the baseplate, wire bonds are the only solid contacts to the physics package. The PC board thickness was reduced to 0.5 mm, and holes were drilled where possible to reduce the thermal conductivity of the FR-4 substrate.

The physics board was soldered onto the electronics board and the finished CSAC prototype unit (Figure 56, left) was placed inside a thermally stabilized box (Figure 56, right) that provides outputs for all diagnostic signals and connections to the four power supplies (3.3 V for control electronics, LO bias, and laser, 4.5 V for laser and cell heaters, and 4.8 V for LO tune). At the same time it allows for additional RF shielding and can be temperature controlled. A connector on the box allows communication interface signals to be transmitted from the CSAC to a computer for control and monitoring of the CSAC, if desired. Eleven analog signals are also exported for integrity monitoring of the CSAC. This prototype (SP2) was shipped to the Navy's Space and Naval

Warfare Systems Command (SPAWAR) for additional measurements, which are described in the next section.

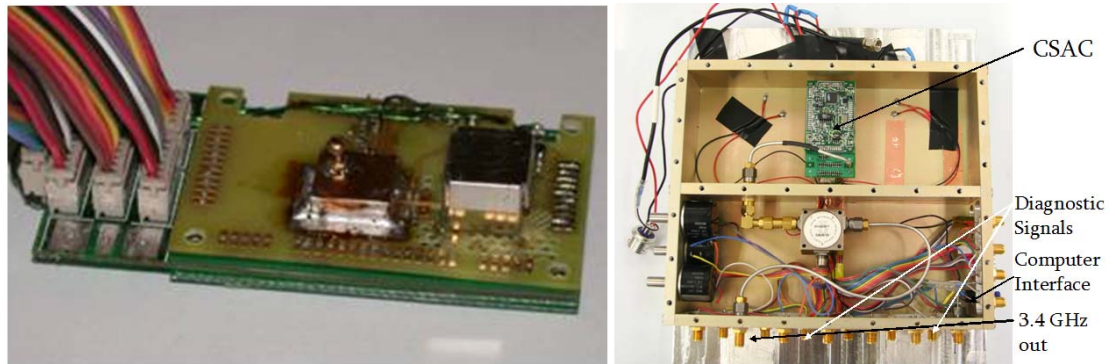


Figure 56 –Photograph of the integrated CSAC (left) and the CSAC enclosed in a thermally-stabilized, electrically-shielding interface box (right). The CSAC is a fully-integrated system including physics package (shown under a magnetic shield), a local oscillator (shown under an electric shield), and control electronics (green board on bottom). The interface box provides outputs for diagnostic signals, and a computer interface. This package was shipped to SPAWAR for further evaluation.

5.4 Measurements and Discussion

As Figure 57 shows, the frequency stability of the integrated LO-PP system is 2.5×10^{-10} at one second, when locked with rack-mounted electronics. At the time, that was the best short-term frequency stability demonstrated with a low-power local oscillator (< 10 mW) and a physics package. It can be seen from the figure as well that a fractional frequency instability below 10^{-10} can be achieved between 15 s and 4.5 hours. In order to reach this, the ambient

temperature of the CSAC must be stabilized precisely, since the integrated package has a temperature coefficient of -45 Hz/K. This is mainly caused by small temperature gradients between the thermistor and the VCSEL(95) that change with the ambient temperature. An approach to reduce this dependence has been published in(95).

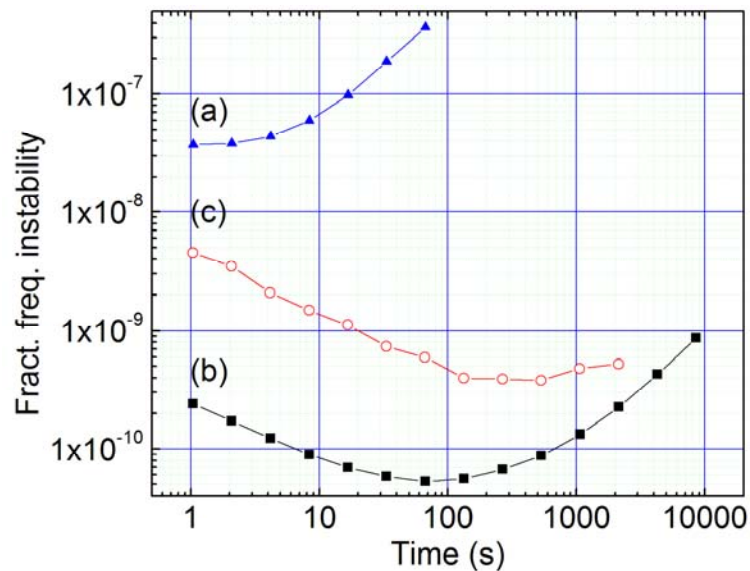


Figure 57 –Summary of the CSAC SP2 frequency instability. (a) The output of the free-running local oscillator, (b) when locked using large electronics, and (c) when locked with small electronics in a fully-integrated system. Figure generated by Dr. J. Kitching for the final DARPA CSAC report.

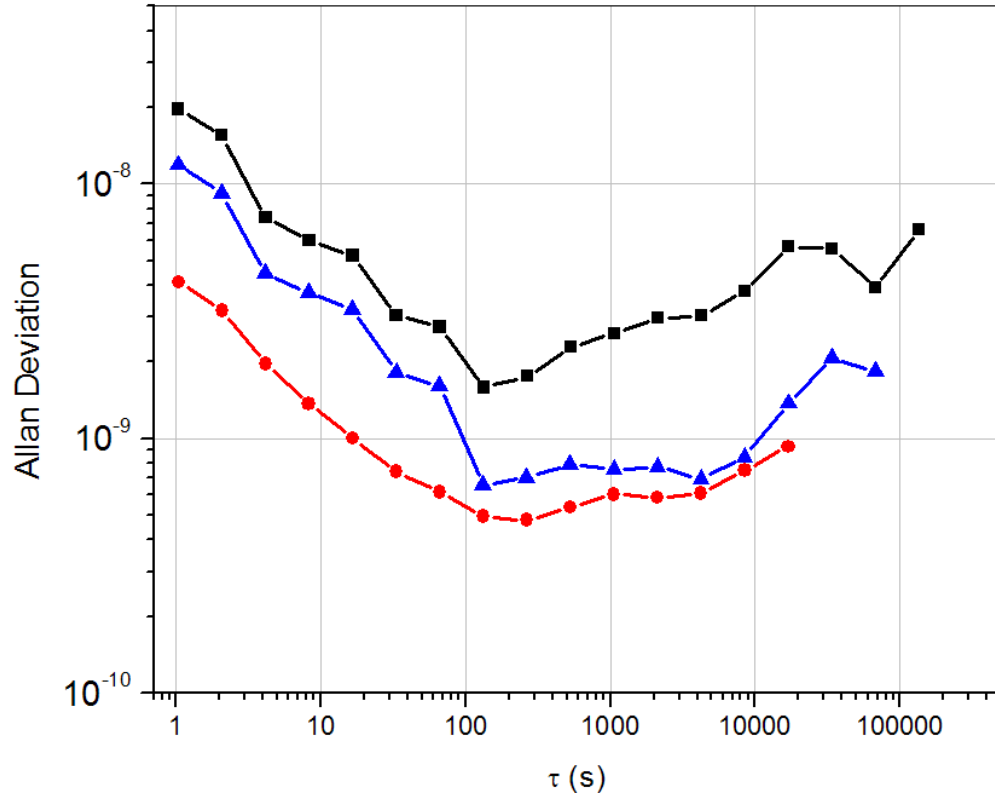


Figure 58 –Allan deviation of the CSAC at NIST (red circles), when operating at SPAWAR initially (black squares) and at SPAWAR after improvements (blue triangles).

One of the two CSACs (SP2) was delivered to SPAWAR and was operated between September 2006 and January 2007. Figure 58 shows some typical Allan deviations when operating at NIST (red circles), when operating at SPAWAR initially (black squares) and at SPAWAR after using a new (lower-noise) power supply and inside a temperature controlled oven (blue triangles). The short-term stability of the CSAC at SPAWAR seems very consistent at $1 \times 10^{-8}/\tau^{1/2}$. The improvements at long times are likely due to improved thermal control. The external temperature control is not operated by SPAWAR. The temperature

stability of the laser appears to become significant and limits the CSAC frequency at intermediate time periods of one hour. As shown in Figure 59, ambient temperature fluctuations appear to change the CSAC frequency and 24-hour fluctuations can be seen on the output frequency (reduced on weekends). The frequency of the CSAC at longer times is determined by a slow frequency drift of roughly $-2 \times 10^{-9}/\text{day}$.

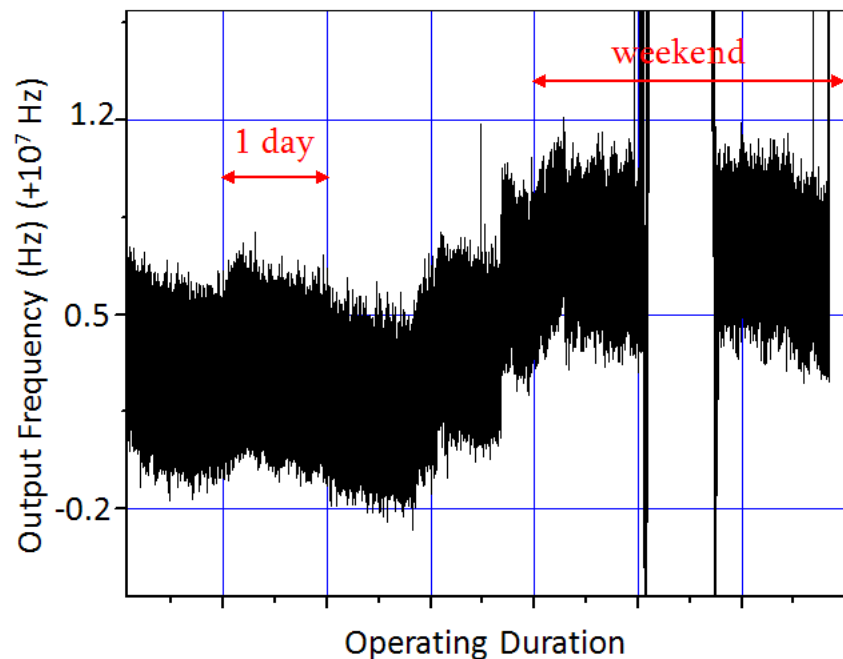


Figure 59 –CSAC output frequency at 10 MHz as a function of time over a period of one week, running at SPAWAR. A long-term frequency drift of $-2 \times 10^{-9}/\text{day}$ seems to be present. We speculate that this is a result of laser aging: the laser output power can change over time resulting in an altered light shift of the atomic resonance. Measurement performed by M. Nicholson at SPAWAR.

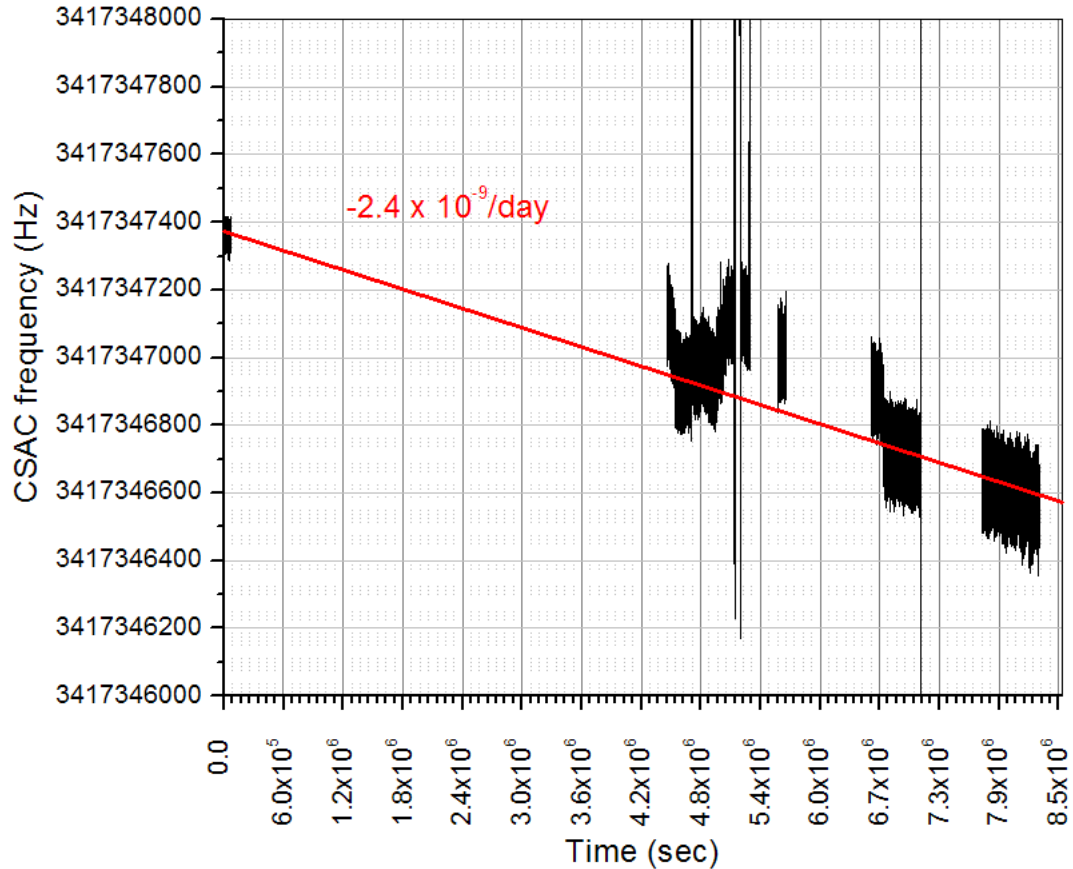


Figure 60 –CSAC output frequency as a function of time over a period of three months. Measurements performed by V. Gerginov and A. Brannon at NIST.

Figure 60 shows the output frequency of the CSAC over a period of 3 months. The long-term frequency of the cells is expected to be below 2×10^{-11} /day(93). We suspect the drift of the device to be caused by aging of the VCSEL, which might be reduced when implementing advanced locking techniques(93)(96).

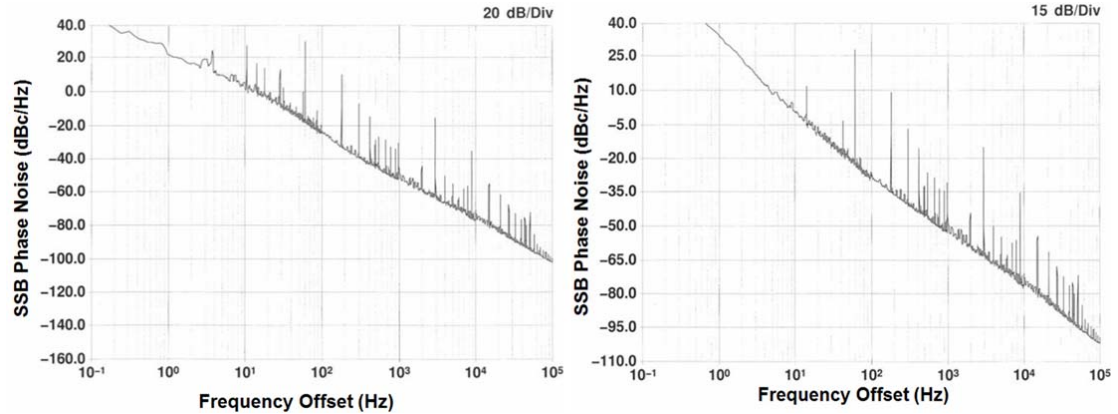


Figure 61 –Measured single-sideband phase noise of the CSAC output at 3.4 GHz when locked (left) and when unlocked (right), where the LO is free-running.

A single sideband (SSB) phase noise plot of the CSAC output can be seen in Figure 61. It is expected that the phase noise of the device is determined by the LO phase noise at frequencies larger than the locking bandwidth of the LO servo controller (~ 1 kHz), and by the atoms at frequencies shorter than the locking bandwidth. Figure 61 (left) shows the effect of locking to the atoms, where the free-running LO phase noise (shown in Figure 61, right) is improved at offsets less than 1 kHz. Using a LO with better free-running phase noise should improve the overall performance.

The performance of the CSAC in terms of size and power consumption is summarized in Table III. Most of the power is consumed by the control electronics board and heat dissipation in the physics package. The largest components are the control electronics and the frequency divider boards, both of which can be considerably miniaturized with integrated circuit design.

Table III – Summary of the CSAC Deliverable Performance

Component	Size (cm ³)	Freq. Stab. @ 1s	Power Cons.(mW)
Physics Package	0.7	1×10^{-10}	130
Local Oscillator	0.5	4×10^{-7}	<10
Control Electronics	5.6	4×10^{-9}	152
Frequency Divider	3.4	$\ll 4 \times 10^{-9}$	30
Total	22.5	4×10^{-9}	322

5.5 Discussion of System Limitations

5.5.1 Short-Term Fractional Frequency Instability

The short-term fractional frequency instability of the fully integrated clock is at $4 \times 10^{-9}/\tau^{1/2}$ level, compared with the $2.5 \times 10^{-10}/\tau^{1/2}$ supported by the combined LO-PP board before the integration with control electronics. Several reasons for performance degradation after the integration have been identified, and are listed below.

- Step size of LO frequency control. The minimum step size of the LO frequency control loop corresponded to a 50 Hz change of the LO frequency, leading to fractional frequency instability that was limited to $5 \times 10^{-10}/s$ level. Increasing to 16 the number of bits of DAC that controls the LO should improve this.

- Phase of the LO frequency loop. The LO is locked by comparing the photodetector output for each half-period of the LO frequency modulation. The feedback loop compares the two values, and applies correction to the LO to make the difference a constant value (zero value locks the LO exactly on top of the CPT resonance). The resolution of the 12-bit ADC limits this correction to 1.3 Hz, or 4×10^{-10} . Increasing to 16 the number of bits of the ADC should improve this.
- Coupled noise to the VCSEL current. The modulation frequency at 1.5 kHz, used for LO frequency control, was present in the injection current of the VCSEL, causing laser frequency noise at 1.5 kHz. This noise was transferred in the LO frequency control loop, causing instabilities in the LO frequency control. Improved shielding between the two boards and a greater awareness of the positions of signal traces should improve this.
- Time-jitter errors. The microprocessor sampled the LO frequency modulation period of 1.5 kHz at non-uniform time intervals. The corresponding phase error caused the LO frequency to be detuned from the maximum of the CPT signal. Using two or more dedicated processors to avoid delay problems might improve this. There may be other implementations of lock-in detectors that are less susceptible to this problem.
- The LO was very sensitive to RF reflections both from the laser and from other components in physical proximity. The control electronics were attached below the LO at a distance of less than 1mm, providing easy

coupling to the many square-wave signals on the board. Additionally, the LO exhibited frequency pulling effects due to changes in the load (VCSEL) impedance(97), as shown in Figure 62, and changes in the position of reflective elements in the vicinity of the LO. Since the distance between the LO output and the VCSEL was approximately 0.25 wavelengths at 3.4 GHz, and since there were significant reflections from the VCSEL, it was possible to have an extra mode of oscillation in the vicinity of the desired frequency. This low-Q spurious oscillation added noise to the laser and made proper modulation difficult. In order to stabilize the output of the LO, the injection current of the VCSEL was reduced, which improved the impedance matching between the LO and the VCSEL and eliminated the multi-mode oscillation. However, the lower injection current caused the VCSEL to operate closer to its threshold, where it was in general more noisy. Although the copper shielding reduced the LO frequency sensitivity, further improvement should be made with the addition of an output buffer stage. With DC power consumption less than 3 mW, a simple one-stage buffer amplifier resulted in a simulated improvement in frequency pulling effects by a factor of 65. Greater improvement can be made by reducing the power coupling between the LO and the buffer stage. Further shielding might be obtained using stripline in a multilayer circuit board and by shielding the entire package.

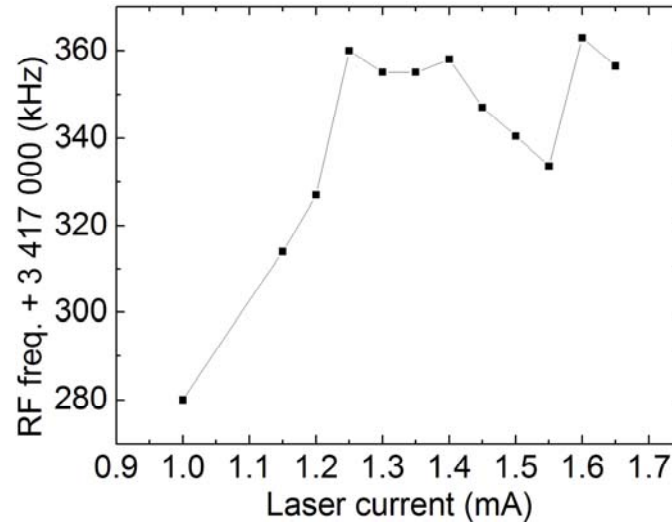


Figure 62 –Measured output frequency of the LO due to VCSEL impedance changes.

5.5.2 Long-Term Fractional Frequency Instability

The long-term fractional frequency instability of the integrated CSAC averages down as $1/\tau^{1/2}$ up to 100 s (see Figure 58). The important parameters that degrade the long-term performance of the system are listed below:

- Laser temperature instability. The 12-bit resolution limits the accuracy of laser temperature measurements to 20-30 mK. To measure such influence, the clock frequency was measured as a function of the laser temperature setpoint. A change in one least significant bit of the laser temperature setpoint produces a clock frequency shift of 2.6 Hz, or 8×10^{-10} . As the temperature of the laser changes, the laser injection current changes to compensate for the drift of the laser frequency. For VCSELs, the laser intensity is strongly coupled to the injection current, and the

corresponding change of the laser intensity causes the clock frequency to shift due to the AC Stark shift. Two methods (95)(96) have been proposed at NIST and show considerable improvement in laser temperature stabilization.

- Cell temperature stability. The 12-bit resolution of the ADC limits the accuracy of the cell temperature measurements to 20-30 mK. To measure this influence, the clock frequency was measured as a function of the cell temperature setpoint. One least significant bit change of the cell temperature setpoint produced a clock frequency shift of -0.2 Hz, or 6×10^{-11} . The reason for a shift of the clock frequency with cell temperature is the change in Rb and buffer gas pressures inside the cell. The change in the buffer gas pressure leads to a shift of the clock frequency due to collisions. A method to correct this (97) has been proposed at NIST and stabilizes the cell temperature accurately to approximately 4 mK.
- Ambient temperature. The temperature gradients between a thermistor and the component being stabilized change with the ambient temperature. This causes the temperature of the stabilized component to drift with the ambient temperature. A change of the laser or cell temperature leads to clock frequency drift. Another effect is a change in currents used to heat the laser and the cell. They change the magnetic field inside the cell, and through a second-order Zeeman effect, this leads to a shift in the clock frequency. The clock frequency versus the ambient

temperature was measured to be 45 Hz/K, or $1.3 \times 10^{-8}/\text{K}$. The CSAC was enclosed in a box with ambient temperature control which stabilized the temperature of the entire package to 100 mK, reducing the long-term drift of the clock frequency to $\sim 1 \times 10^{-9}$. As can be seen from Figure 57, the actual CSAC performance is consistent with such ambient temperature control. The three methods (97)(95)(96) mentioned above provide significantly improved frequency stability in the presence of ambient temperature fluctuations.

- Cell or VCSEL aging. The cell is manufactured according to the procedure described in (93) and is not expected to drift over long times, but this remains to be tested with multiple cells and over long times (many years). The VCSEL is operated near its maximum operating temperature and its output intensity might change due to aging, causing clock frequency drifts via the AC Stark shift. The performance of the CSAC has been monitored for a period of three months (See Figure 60) and shows a gradual decrease of the clock frequency. The two methods(95)(96) mentioned for laser temperature stability, also correct for VCSEL aging. However, because cell aging may be due to chemical changes inside the cell, no direct compensation methods are known. If the cell aging is predictable over time, a microprocessor-implemented calibration could provide some compensation for this effect. Alternatively, cell aging effects result in drifts only at very long time scales (weeks) and may be of little concern.

Chapter 6

6. Self-Injection Locking by use of Atomic Four-Wave Mixing

6.1 Introduction

Current CPT-based clocks use either active or passive locking techniques. In the case of a passive frequency reference, the output of a local oscillator (LO) is used to modulate the laser diode and the LO frequency is tuned onto the resonance by use of lock-in detection, which requires modulating the LO. Phase-locking techniques based on a detected increase in the microwave signal have also been shown (98). Passive systems are limited in both locking range and correction bandwidth, requiring the LO to be precisely tunable, to have minimal drift, and to have minimal high-frequency fluctuations. These specifications usually imply a high-power, large LO. Active locking (98),(99) eliminates the LO

and much of the locking electronics by modulating the laser with an amplified microwave beat note, which is generated by the atoms and is detected by a fast photodiode. However, these systems are sensitive to phase shifts in the oscillating loop and can be difficult to lock since the resonance is observed merely as an increase in an existing signal, often by less than 10 %. Also, increased complications in the locking dynamics can lead to instability and several possible resonances (99).

Problems with the long-term instability of chip-scale clocks are largely due to temperature fluctuations and aging of the VCSEL (95),(97),(96). The short-term frequency instability can be limited by the LO, which is itself limited in performance by stringent size and power consumption requirements. In particular, the phase noise of the LO at twice the modulation frequency has been shown to limit performance (31). In this chapter, a simple, robust, and potentially low-power lock to the atomic hyperfine transition is presented. The approach requires no modulation of the LO and results in a design that can be easier to implement than recent active designs, has a larger locking range and correction bandwidth than passive methods, and presents improved phase noise and short-term instability versus comparable examples using both methods.

6.2 Self-Injection Locking Method

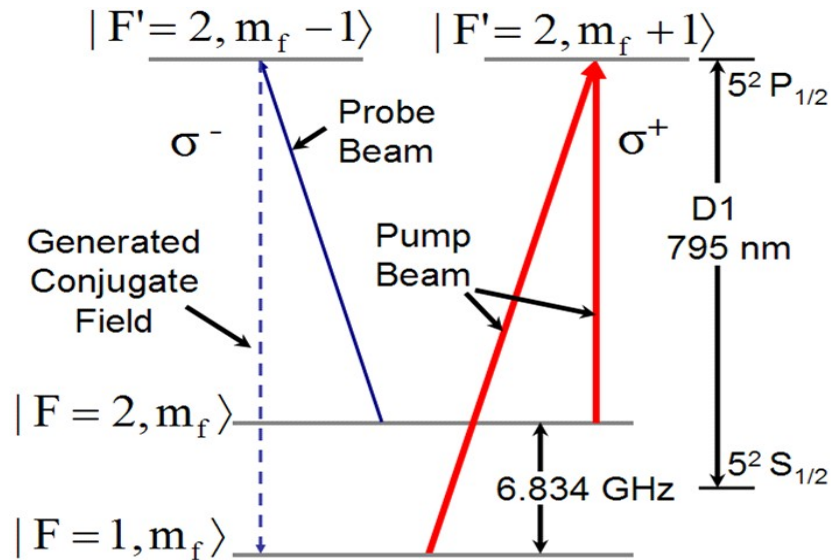


Figure 63 -Depiction of the level scheme used in CPT four-wave mixing experiments. The light field that is represented by the dotted line is generated with four-wave mixing. A clock is created by use of the ground state sublevels where $m_F=0$, while a magnetometer can be created by use of the magnetically-sensitive sublevels $|m_F| = 1, 2$.

The RF output signal from a compact local oscillator is sent to an optical system described in more detail below. This optical system acts as a narrowband RF filter and frequency doubler; it generates as its output a phase-coherent RF signal at twice the input frequency. This signal is used to self-injection lock the LO at the second harmonic, stabilizing its frequency. First we discuss the generation of the signal in the atoms.

Figure 63 shows the atomic energy level diagram that can be used to describe four-wave mixing with a CPT system. Here, the ^{87}Rb atom is used as an

example. The ^{87}Rb atoms are excited by the pump beam, a 795-nm circularly-polarized laser beam containing two optical components separated by 6.8 GHz. Each optical component is resonant with a transition between a ground-state component and the excited state. This results in coherent population trapping, or pumping of the atoms into a superposition of the two ground states. This superposition is uncoupled from the two light fields. When this occurs, a decrease in photon absorption is detected by a photodiode as an increase in total transmitted light. Because the spectral difference of the two optical components is a precise microwave frequency, one observes a very narrow resonance with an effective microwave Q factor typically greater than 1 million. However, the low contrast of the signal (<1% to 10%) is often a practical limitation. It has recently been shown (100) that a large improvement in contrast can be achieved with use of a four-wave mixing process that generates a new, phase-conjugated light field when CPT resonance occurs. In this process, a non-modulated probe beam is tuned to the $F = 2, F' = 2$ transition. This beam is identical to the pump beam in wavelength and spatial orientation but has opposite circular polarization. Due to the nonlinearities of the CPT process, a fourth phase-conjugated light field, separated from the probe by 6.8 GHz, is generated by the atoms. In (100) all the light fields except the generated field are removed and the signal is detected against a near-zero background. In our technique, we remove only the pump beam with a $\lambda/4$ waveplate and a polarizer. Both the probe beam and the generated field impinge on a fast photodiode. The output, at approximately 6.834 GHz, is precisely equal to the frequency difference between

the ground state hyperfine components. This signal is used to stabilize the LO. Whereas the process in (100) results in a large contrast in a DC photodetector signal, the technique described here results in a large microwave contrast observed by a fast photodiode.

The primary advantage over the conventional techniques is that, rather than observing a small increase in an existing signal, this signal is observed only when the LO is tuned in the vicinity of the CPT resonance. This signal could be used to directly modulate the pump laser, forming an active system similar to (99). However, several stages of amplification would be required to achieve the -6 dBm of power required to modulate the diode laser. Additionally, it has been shown (99) that signal power fluctuations in similar active frequency references can cause instability due to power-sensitive phase shifts. Here, we use a low-power LO to modulate the laser with a relatively stable power and the generated signal is used to injection-lock the LO, stabilizing its frequency. Although the injected signal is at twice the frequency of the LO output signal, this harmonic injection locking occurs effectively with injected powers as low as -70 dBm. The LO output power remains largely unaffected by changes in injection-locking power, eliminating some of the problems caused by the unstable loop power in active self-locked systems.

6.3 Experimental Setup

6.3.1 Setup Overview

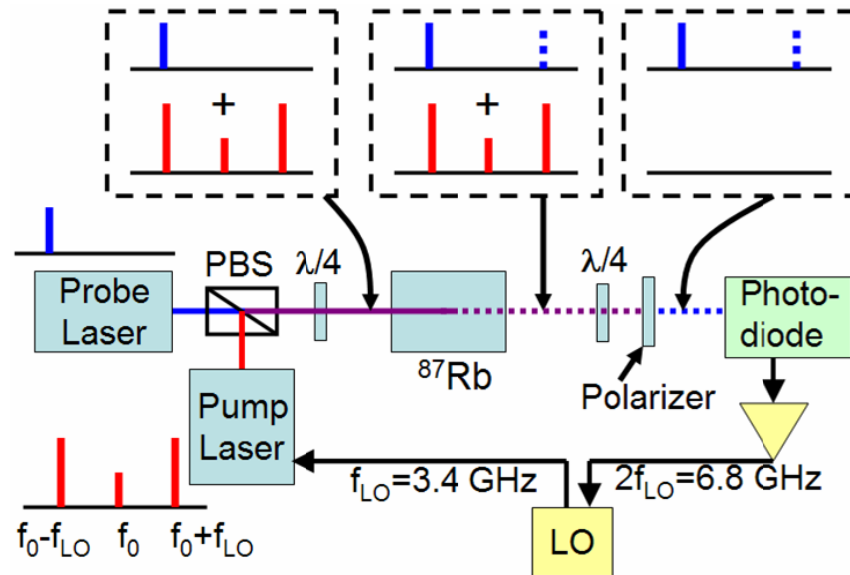


Figure 64 –Diagram of the experimental setup. The pump laser is modulated by the LO such that the two first-order sidebands are separated by 6.8 GHz. Additional filtering of the pump carrier wavelength is not needed. The probe laser is tuned to the same (795-nm) wavelength as the pump but has orthogonal polarization. $\lambda/4$ waveplates result in circular polarizations of the beams. When the LO is tuned to the CPT resonant frequency, a phase-coherent 6.8-GHz frequency is observed at the output of a fast photodiode. This is used directly (without frequency division) to injection-lock the LO.

Figure 64 shows the setup used as a proof-of-principle experiment. The pump and probe lasers are VCSELs tuned to the 795 nm D1 line of ^{87}Rb . The pump laser is modulated with the 3.417 GHz, 0 dBm output of a miniature LO

like that designed in (37) and that consumes less than 10 mW. The modulation produces sidebands in the optical spectrum, with the two first-order sidebands separated by 6.8 GHz. This light is then circularly-polarized by a $\lambda/4$ waveplate and passes through a 1 cm diameter glass cell containing ^{87}Rb atoms with a 50 Torr buffer gas pressure in a ratio of 1.44 argon to nitrogen. The incident optical intensity on the cell is approximately $50 \mu\text{W}/\text{mm}^2$ for the pump. Then, a second but non-modulated probe beam is spatially aligned with the pump beam and its polarization is aligned perpendicular to the pump beam polarization. The probe has intensity, incident on the cell, of approximately $5 \mu\text{W}/\text{mm}^2$. It interacts with the atoms that are pumped with the first beam, resulting in the generation of a phase-conjugated signal with the same polarization as the probe beam but separated from the probe in frequency by 6.834 GHz. The two beams are then linearly polarized by another $\lambda/4$ waveplate and the pump beam is removed with a polarizer. The combined probe and generated light field impinge on the fast photodiode, resulting in a 6.834-GHz oscillating current that yields -90 dBm when output from the photodiode into 50Ω . This signal is then amplified by 10 dB to 50 dB and is fed directly into the output of the LO, which locks to the signal by second-harmonic microwave injection locking. We have observed that the LO output power remains stable over a wide range of injection-locking power, and levels less than -70 dBm are strong enough to lock the LO.

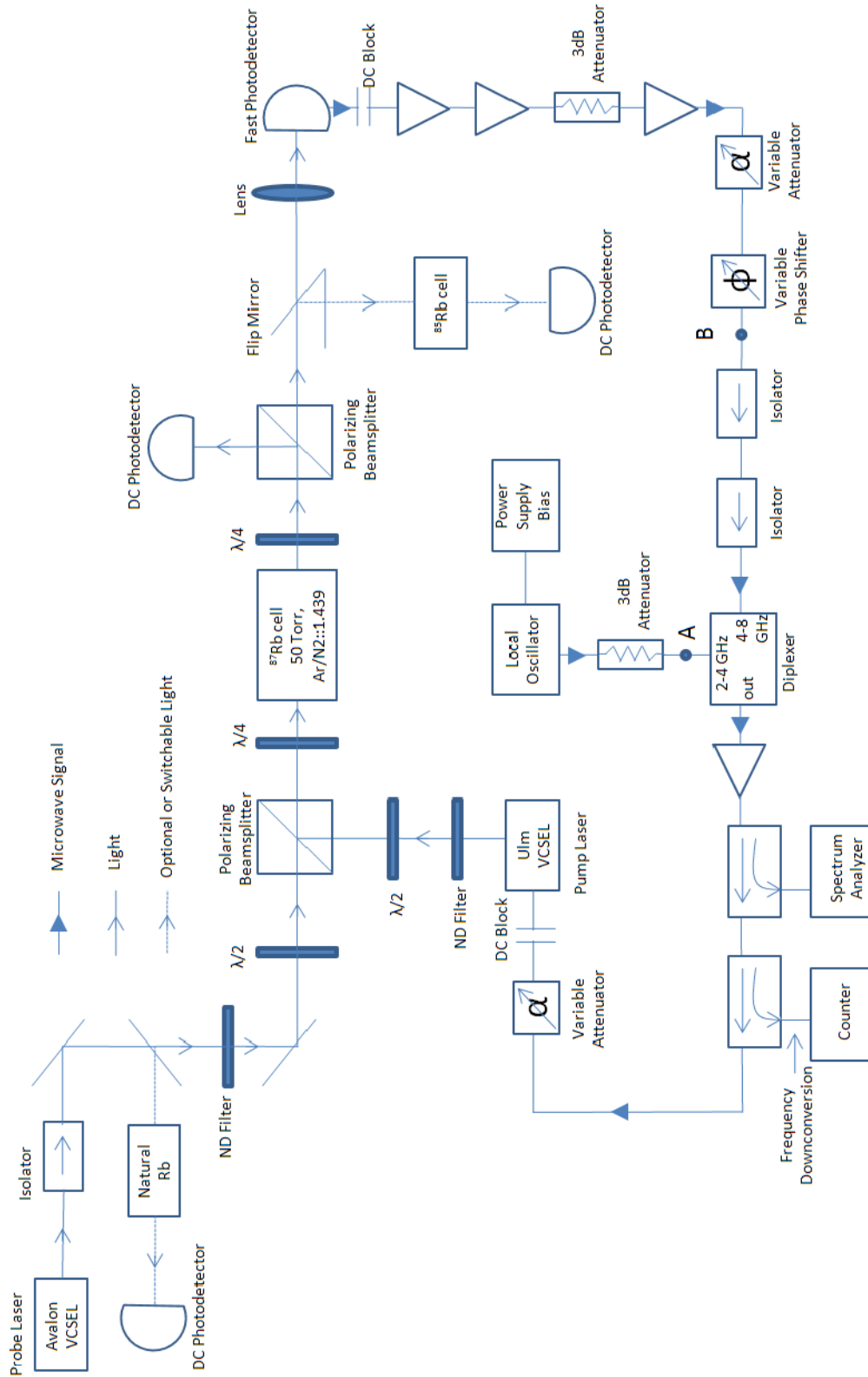


Figure 65 –Schematic diagram of the experimental setup used in this chapter. The diplexer and isolators are not needed but are used here to additionally separate the 3.4 GHz output from the 6.8 GHz injected input.

6.3.2 Setup Overview

Figure 65 shows the detailed schematic diagram of the system used for the material in this chapter. The optical part of the setup is essentially as described above in Figure 64. The pump laser is a proton-implanted VCSEL, manufactured by Ulm, and is modulated at 3.417 GHz. The probe laser is an Avalon VCSEL with an etched mesa structure. The probe laser does not need to be modulated and can therefore be a more spectrally-stable laser. To prevent distortions due to reflections, the pump beam passes through an optical isolator. The polarizations of the pump and probe beams are made orthogonal with $\lambda/2$ waveplates. The probe laser is stabilized by locking to the D1 line of ^{85}Rb , since this was shown to give the highest contrast in the 4-wave signal(100). This stabilization was implemented primarily to prevent long-term drift of the laser; no significant improvement in short-term stability was observed. A polarizing beamsplitter removes the pump beam after the ^{87}Rb cell and directs it to a DC photodetector for implementing stabilization of the pump laser. The combined probe beam and the 4-wave mixed beam are focused onto a fast photodetector, which outputs the high-contrast 6.8 GHz signal. The flip mirror enables rapid switching between a 4-wave injection locking system and a 4-wave DC high-contrast system similar to the one reported in (100). The system can be configured for DC servo-locking by changing the polarization of the pump beam such that it passes through the second polarizing beamsplitter.

In the RF part of the system, the 6.8 GHz signal is amplified, with 3 dB attenuators used to improve isolation between amplifiers. A variable phase

shifter provides the ability to tune in an optimal phase for injection locking and a variable attenuator enables adjustment of the strength of the injected signal. This signal enters the output of the LO through a diplexer, which permits good separation of this input injected signal and the LO output at 3.4 GHz. It should be noted that we observed injection-locking with roughly equal results by substituting a simple power combiner in place of the diplexer. However, the system was used as shown to permit better separation of the LO fundamental and second harmonic frequencies, permitting appropriate comparison to theory. Likewise, the isolators provide good separation from the incoming signal and any possible output of the LO. The 3.4 GHz from the LO is amplified to compensate for cable and component losses and power is coupled off for measuring the output spectrum and quality. A variable attenuator is adjusted for optimal power before modulating the current of the pump laser.

An additional means of frequency stabilization was discovered by noticing that the phase shift in the loop changes dramatically as the frequency is tuned, a result of the very high Q of the atomic system. By connecting a mixer as a phase detector between locations A and B in Figure 65, a voltage proportional to the phase shift is found. This voltage is then amplified, low-pass filtered and injected with proper phase into the tune port of the LO. This method was effective for reducing the frequency instability at time offsets greater than 1 s.

6.3.3 Fast Photodetector

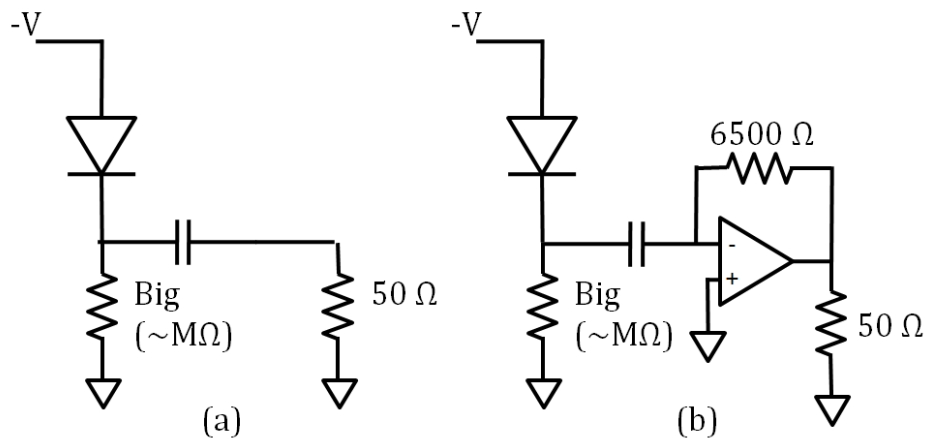


Figure 66 –Schematic of the non-amplified New Focus fast photodetector (a) and the photodiode-transimpedance (TIA) amplifier pair (b). The Johnson noise of the TIA's 6500 Ω transimpedance limits schematic (b) to no significant improvement over the device in schematic (a).

A NewFocus fast photodetector is biased as in Figure 66(a). For this component, the two noise sources are described as shot noise and thermal Johnson noise. The shot noise is found as in equation (6-1) where I_{DC} is the DC current through the photodetector, e is the electron charge, R is the parallel combination of the 50 Ω resistor and the 50 Ω resistance of the output, and B is the noise bandwidth, which is 1 Hz in our calculations.

$$v_{shot,rms} = i_{shot} R = R\sqrt{2eI_{DC}B} \quad (6-1)$$

$$v_{Johnson,rms} = \sqrt{kTBR} \quad (6-2)$$

The Johnson noise is found in equation (6-2) where k is Boltzmann's constant, T is the temperature in Kelvins, and R is the resistive noise source. The "4" in the typical Johnson noise equation is removed in the case of Figure 66(a) because of the voltage noise division between the 50 Ω load resistance and the 50 Ω output resistance. From these equations, we see that the Johnson noise is dominant and the geometric mean of the two noise sources gives $4.55 \cdot 10^{-10}$ V/Hz^{1/2}, which when squared and divided by the load resistance gives -174 dBm, the standard noise power from a room temperature 50 Ω source. The RMS signal current in a 1 Hz bandwidth (calculated from the photodiode efficiency and the measured light intensities from the probe beam of 1.1 μ W and the 4-wave beam of 7.1 nW) is 0.12 μ A_{rms}, which gives -91 dBm of power and a SNR of 83 dB. When subtracting 3 dB (since phase noise power is half the total noise power) and subtracting 2 dB due to the noise figure of a typical microwave amplifier, we should expect a SNR of 78 dB.

In an attempt to improve the SNR, a transimpedance amplifier (TIA) was added to the output of a fast photodiode as shown in Figure 67. The TIA is the TGA4815 from TriQuint, which has a particularly high transimpedance gain of 6500 Ω and a low input noise current of 9pA/Hz^{1/2}. The test fixture of Figure 67 is constructed to permit short wirebonds at both the input and the output of the TIA. One end of the double-ended output is terminated in 50 Ω and the other is used as the output. DC connections are connected to the wires shown and consist of ground, bias, receive signal indicator, and photodiode bias. This

component was used as the fast photodetector in the system described by Figure 65.

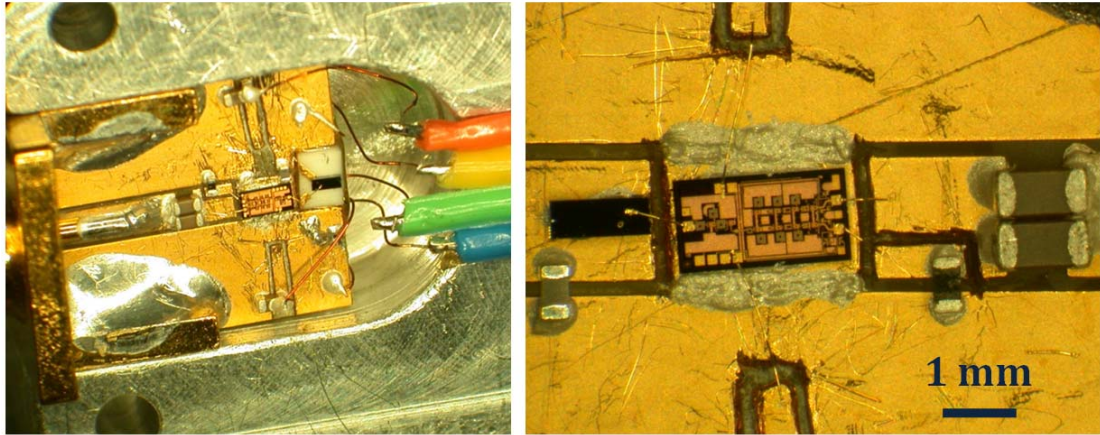


Figure 67 –Photograph of the PD-TIA pair used as the fast photodetector that detects the 6.8 GHz beat note generated by atomic 4-wave mixing. The in-situ mounting (left) shows the mounting block with screw holes, the RF output to the left, and the DC inputs to the right. The close-up (right) shows the short wirebond from the PD to the TIA and the differential output of the TIA to the right, one side of which is directed immediately to a 50 Ω dummy load.

A noise analysis of the photodiode-TIA pair reveals why the resulting SNR was not improved. Figure 66(b) shows a schematic of the receiver. There are three noise sources: the diode shot noise, the Johnson noise of the 6500 Ω impedance, and the input-referred amplifier current noise. In this case, the amplifier noise dominates with $v_{\text{noise}} = i_{\text{noise}} * R = 58.5 \text{ nV/Hz}^{1/2}$. This noise power, dissipated across the 50 Ω load, results in a noise power of -132 dBm. The 0.12 μA_{rms} input is amplified by 6500 Ω and yields a signal power of -49 dBm, or a SNR of -80 dB, after subtracting 3 dB for phase noise only.

6.4 Simulations of Self-Injection Locking

6.4.1 Theory and MATLAB Simulations

Self-injection locking of microwave oscillators has recently been described in terms of stability of the system(101) and the phase noise performance (102). This theory states that phase noise of the self-locked system is improved (for parallel-resonant oscillators) over the range of $-90^\circ < \Delta\theta_{loop} < 90^\circ$, and integer multiples of this range, where $\Delta\theta_{loop}$ is the steady-state phase shift in the external feedback loop. Outside this range, the feedback will degrade the phase noise performance. Choosing the loop phase that permits the best phase noise improvement ($\Delta\theta_{loop} = 2m\pi$, integer m) expression (6-3) is used to describe the expected improvement in phase noise. In this expression, $\omega_{3dB} = \omega_0/2Q$ is half the 3-dB bandwidth of the free-running oscillator, ρ is the ratio of injected current to oscillator output current, $\Delta\theta$ is the steady-state loop phase shift, and ω_m is the offset frequency from the carrier.

$$\left| j + \rho \left(\frac{\omega_{3dB}}{\omega_m} \right) \cos \Delta\theta - \rho \left(\frac{\omega_{3dB}}{\omega_m} \right) (\cos \Delta\theta) H(\omega_0 + \omega_m) \right|^2 \quad (6-3)$$

$$H(\omega_m) = \frac{j\omega \left(\frac{\omega_r}{Q_r} \right)}{\left(\omega_r^2 - \omega^2 + j\omega \left(\frac{\omega_r}{Q_r} \right) \right)} \quad (6-4)$$

To model the self-injection locking due to feedback from our 4-wave atomic system, we simplify the system as a microwave resonator with a high Q. The transfer function, H, is chosen as shown in equation (6-4), where ω_r/Q_r is

the FWHM 3dB bandwidth of the resonator. Based on the measured phase noise of the free-running oscillator, the oscillator's loaded Q is determined to be 20. The resultant phase noise improvement and its dependence on resonator Q and injection strength ρ is shown in Figure 68.

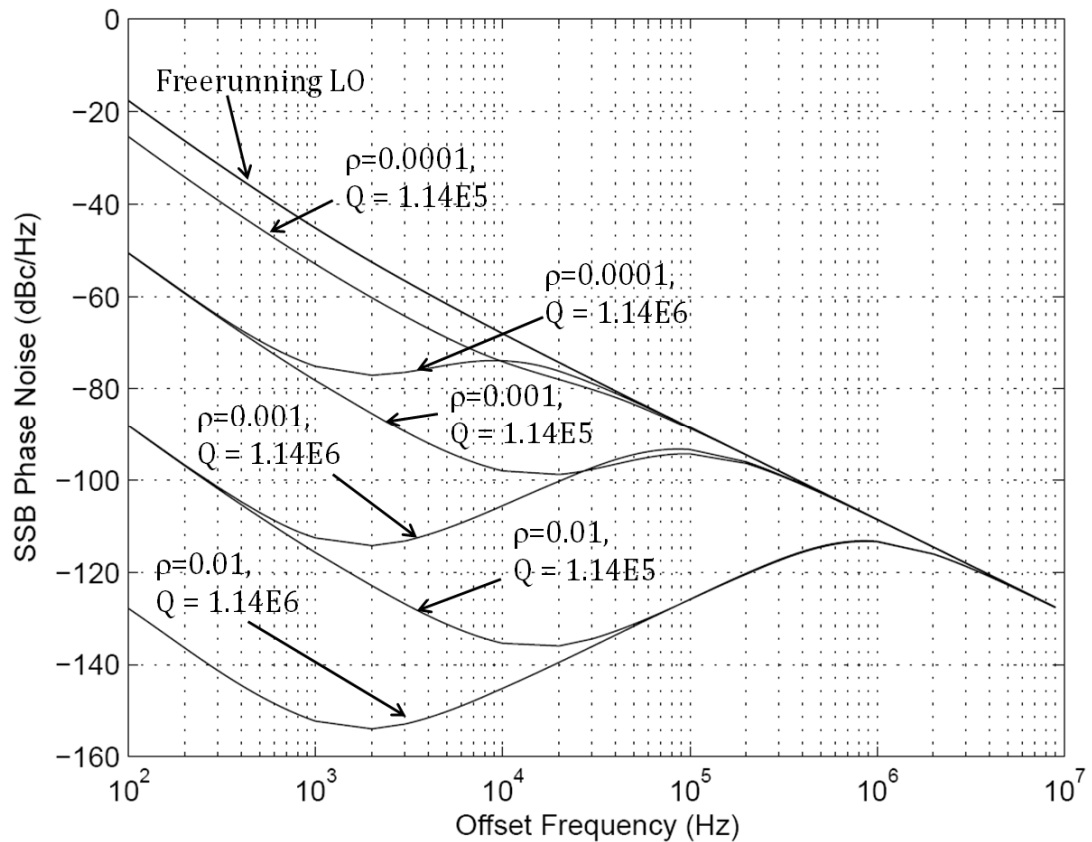


Figure 68 –Comparison of simulation of expressions (6-3) and (6-4) as the feedback resonator Q is varied from the measured value of 1.4 million to 0.114 million and as the ratio of injected current to oscillator output current is varied from $\rho=0.0001$ to 0.01.

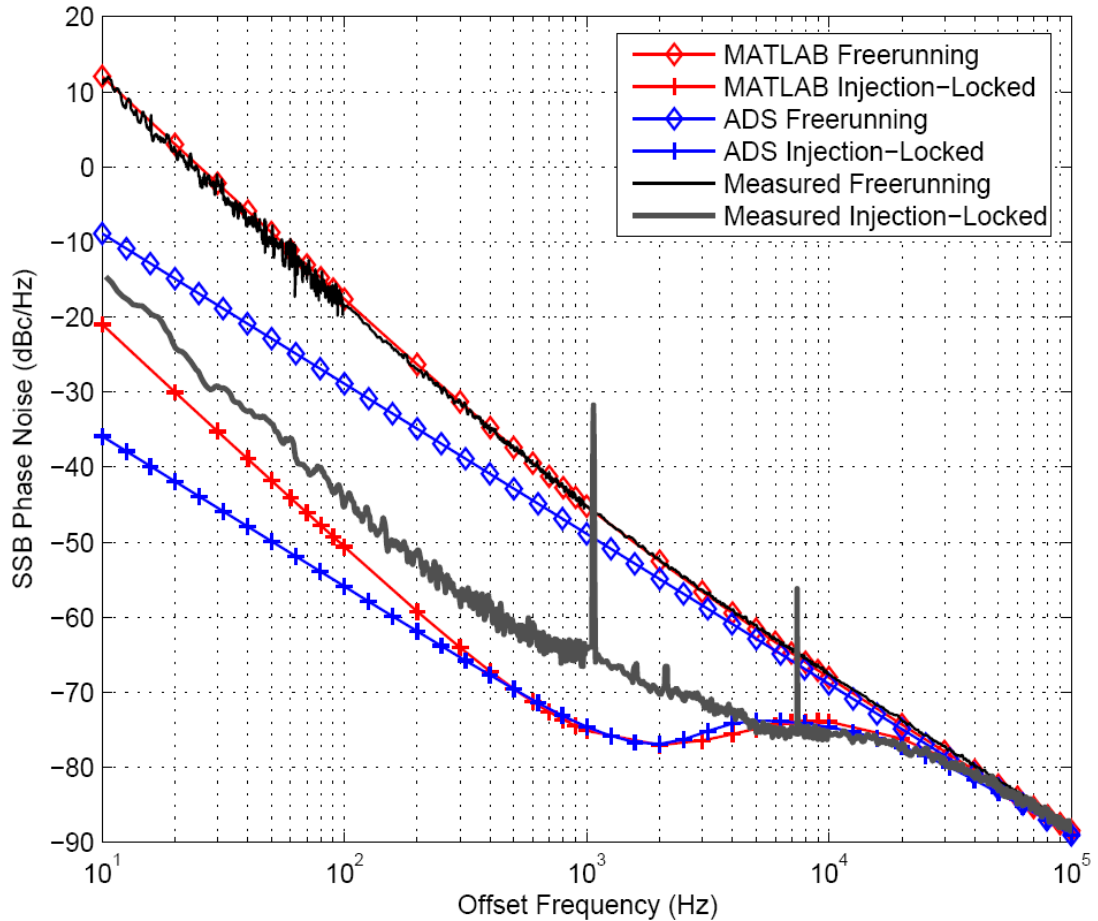


Figure 69 –Comparison of the self-injection locking theory to a circuit simulation and to measured data. The theory and the measured data represent a feedback current ratio of $\rho=0.0001$, a resonator (atomic) Q of 1.14 million and a free-running oscillator Q of 20. The ADS model used circuit element models but did not incorporate a flicker noise model for the transistor. The ADS model was scaled only in terms of simulated injected power.

For the model of the atomic self-injection locked system, the parameter ρ is chosen as -80 dB in terms of power ratios, or 0.0001 in terms of current ratios and Q_r is chosen as 1.14×10^6 , based on the measured FWHM bandwidth of 3 kHz. The result of this model, compared to measurements and an ADS circuit simulation, is shown in Figure 69. We observe a calculated improvement of more than 30 dB, very closely matching both the shape and the levels of the measured data, with no scaling of the simulated or measured data. The measured data were obtained by inserting the injection signal at the oscillator's second harmonic, with a power ratio of -80 dB. This was near the minimum limit for practical injection locking of the oscillator but was necessary to reduce the injection locking bandwidth to a range that permitted observation of the correction at offset frequencies less than 100 kHz. To provide a more accurate depiction of the theoretical phase noise improvement, the flicker noise of the oscillator was added to the simulation.

The measured data were obtained using the system diagrammed in Figure 65, with an introduced variable phase shift that experimentally maximized the phase noise improvement. Though the injected signal was at the oscillator's second harmonic, very good agreement with the fundamental-frequency self-locking theory was obtained. Typical harmonic-frequency injection locking has been shown to improve the phase noise of the fundamental frequency by the same amount that the harmonic was improved. However, since it is generally considered that the injection locking process occurs by internal nonlinear mixing of the incoming signal that converts it to a fundamental-

frequency injection signal, it is surprising that the predicted correction is observed with the same -80 dB power ratio that is observed at the second harmonic. One would expect some internal conversion loss associated with this process. One possible explanation is that the oscillator's resonator can also pass frequencies in the loop at the second harmonic, resulting in a relatively high signal output that is only 5 or 6 dB below the fundamental frequency.

The shape of the predicted phase noise is observed to follow the same curve of the measured phase noise, particularly near the end of the injection locking bandwidth. However, there is some deviation where the phase noise decreases with a -20 dB per decade slope. It is believed that this is the phase noise due to the atomic system for a few reasons. First, this slope is characteristic of atomic phase noise more than a few Hz away from the carrier frequency, corresponding to the $\tau^{-1/2}$ slope observed in the time-domain Allan deviation measurements. Secondly, as injected power was increased, the noise at greater than 5 kHz offset frequencies lowered to match the -20 dB per decade slope and the noise originally at this slope remained unchanged. Finally, within the injection locking bandwidth, a near-constant measured phase noise improvement is generally observed, (25 dB improvement in Figure 69) as is shown by the increased slope of both the corrected and uncorrected phase noise at frequency offsets less than the oscillator flicker corner.

6.4.2 ADS Circuit Simulations

This section presents, to the author's knowledge, the only circuit-level simulation of self-injection locking using a commercial microwave circuit simulator. A tool in Agilent's Advanced Design System (ADS) software known as Circuit Envelope, intended for simulating complex-modulated waveforms software, was employed (103). Traditional Spice simulations require impractical memory and processor resources because the circuit must be sampled at a few times the highest harmonic frequency of interest. In addition, this sampling must occur over a significant number of cycles to model the modulation effects. Harmonic Balance techniques efficiently solve circuits in the frequency domain that have a limited number of steady-state sinusoids. However, complicated modulation schemes often have a large number of tones that are impractical to simulate with Harmonic Balance alone. Circuit Envelope simulations improve on these techniques by allowing a Harmonic Balance solution at the fundamental frequency and harmonics and then simulating the modulation effects as a baseband time-varying complex envelope around the carrier frequencies. The bandwidth must only be large enough to capture the modulation envelope.

One key element in the simulation is the use of Circuit Envelope to simulate the evolution of the output frequencies and the modulated phase noise as the circuit progresses from a free-running oscillator to a self-injected oscillator. For this simulation, the step size is set to the inverse of the

modulation bandwidth or 1/100 kHz. The duration of the time evolution was set to twice the inverse of the resolution bandwidth.

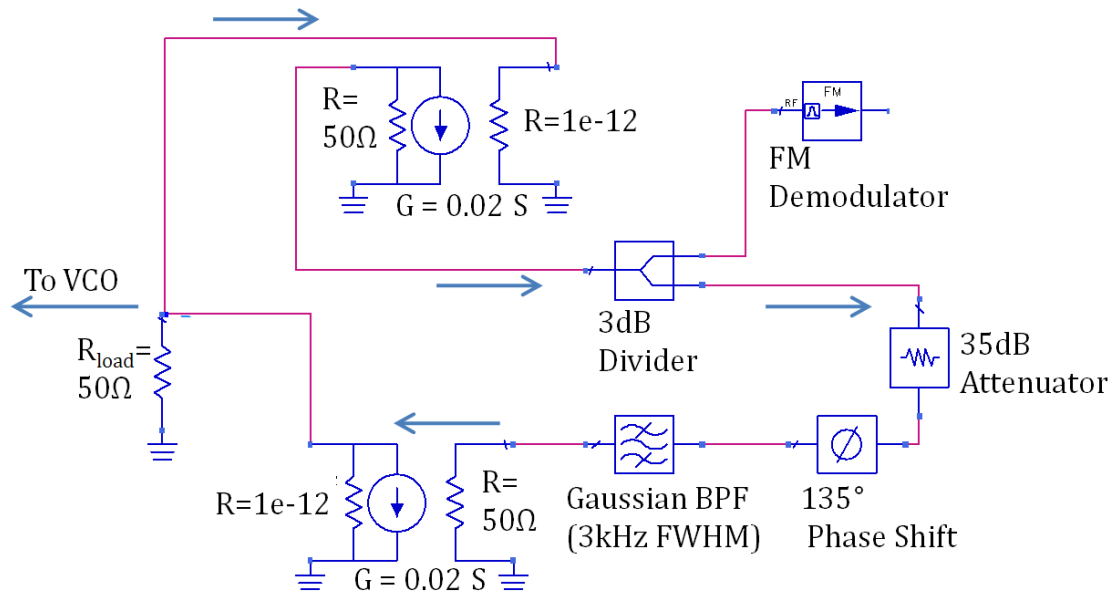


Figure 70 –Schematic of the feedback circuit used to simulate self-injection locking due to the atomic 4-wave resonance. The atomic system is evaluated as a similar microwave system at the fundamental frequency of the oscillator. The atomic resonance is considered as a high-Q bandpass filter. An adjustable phase shift is set to provide the optimal feedback (and phase noise correction) to the LO. The attenuator sets the power ratio of the injected signal to the oscillator output. The voltage-controlled current sources allow injected power into and out of the loop without loading the oscillator or invalidating the initial harmonic balance solution. The FM demodulator permits observation of the changes in frequency as the circuit envelop simulation proceeds in time.

In order to simulate the self-injection locking, the circuit shown in Figure 70 is connected to the output of the oscillator circuit. With ordinary sources and loads, the removal of power from the circuit or the injection of power into the circuit requires some loading of the circuit, which significantly alters the frequency-based solution of the Harmonic Balance analysis. In our case, this results in either an inaccurate solution or the inability to solve the circuit using the Circuit Envelope simulator. The voltage-controlled current sources (VCCS) in Figure 70 are used to recreate the power leaving the feedback circuit and the power returning from the circuit without loading the original oscillator circuit. For this 50Ω system, the transimpedance of the VCCS is set to 0.02. The resistances near the oscillator output are set to a very high number to prevent loading of the circuit.

The variable phase shifter is first tuned to a value that ensures the strongest injection locking and phase stabilization of the oscillator (an integer multiple of 2π). Then, the Gaussian bandpass filter is inserted with a center frequency equal to that of the free-running oscillator (based on an initial Harmonic Balance solution). Finally, the injection signal strength is adjusted with the variable attenuator.

In order to simulate the injection-locking effects, it is necessary to allow the Harmonic Balance engine to arrive at a free-running solution before attaching the feedback circuit. This is accomplished by use of a time-based value for the transimpedance of either of the VCCS in Figure 70. For the first 1 ms, the VCCS is off while the circuit evolves to its steady state operation, then the VCCS

transimpedance is set to 0.02 S, turning on the loop. Circuit Envelope then simulates the evolution of frequency and power changes in the oscillator for the next 1 ms. Finally, the simulator is set to evaluate phase noise at the end of the simulation.

The measurements show the overall improvement and shape of the phase noise and agree well in this manner versus measurements and theory. Additionally, the simulations agree closely with the theory regarding the stable range of injection locking. However, there are some significant differences at this point. Firstly, the injection locking observed occurs with only a 35 dB reduction in injection power as opposed to the 80 dB reduction in theory and measurements. It is likely that this is at least partly related to the internal impedance mismatches between the oscillator output and a 50 Ω system. Finally, the transistor model used in the oscillator circuit does not include a flicker noise model, resulting in the departure from measurements at small offset frequencies. The introduction of a flicker noise model should remove this difference, as it did with the simulation of theory in Figure 69.

The simulation is also able to model the frequency deviations from the initial Harmonic Balance solution with the use of the FM demodulator shown in Figure 70. This device outputs a voltage that is proportional to the frequency difference from the initial solution. Additionally, the output spectrum can be calculated and is shown in Figure 71 with the noise improvement visible out to 10 kHz, as the phase noise simulations also show.

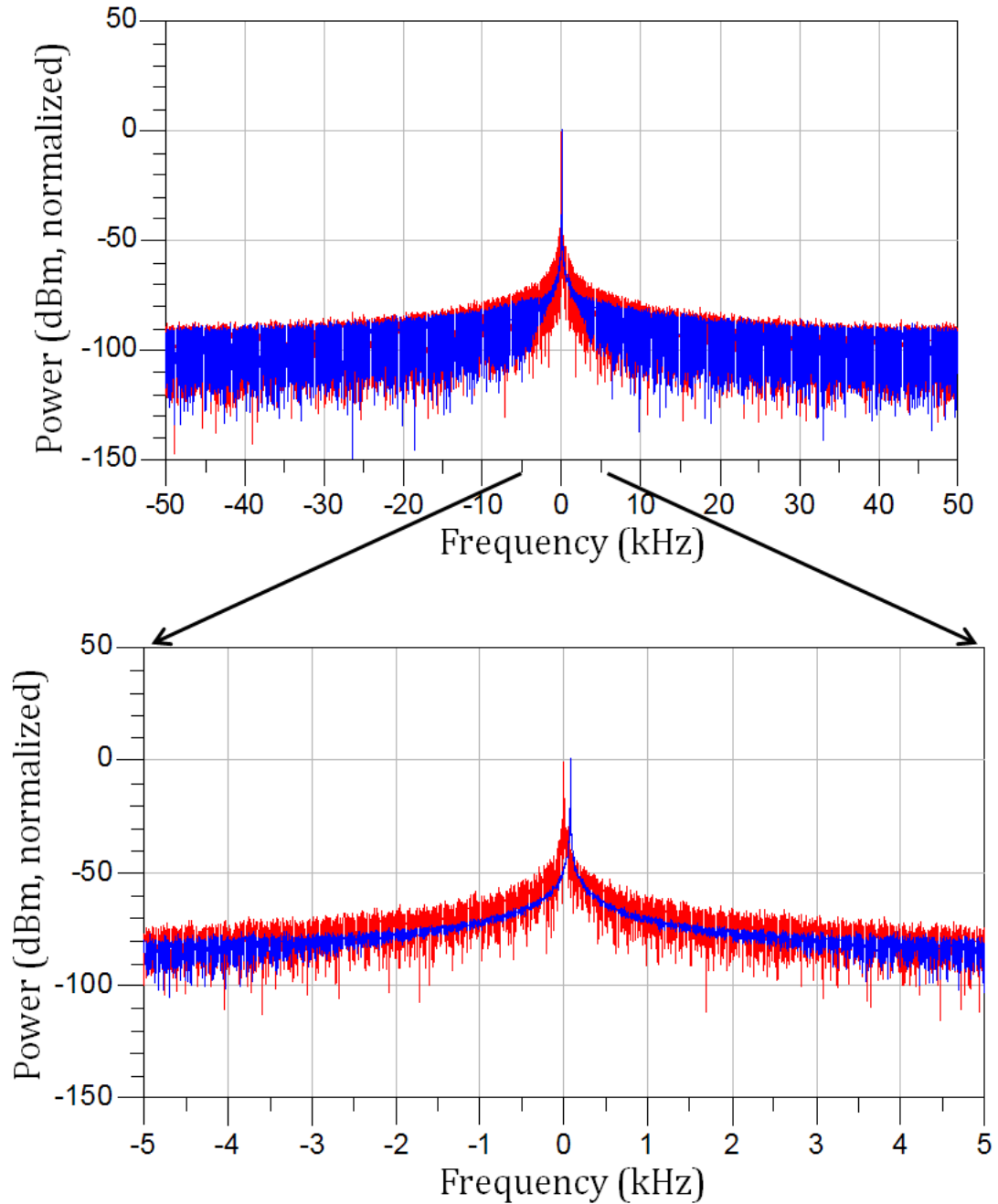


Figure 71 –Frequency spectrum of the oscillator before self-injection locking (red) and after self-injection locking (blue). The improvement between 0 kHz and 10 kHz is observed and the close-up (bottom) shows a 100 Hz frequency shift due to self-injection locking.

6.5 Results

6.5.1 Locking Bandwidth vs. Injected Power

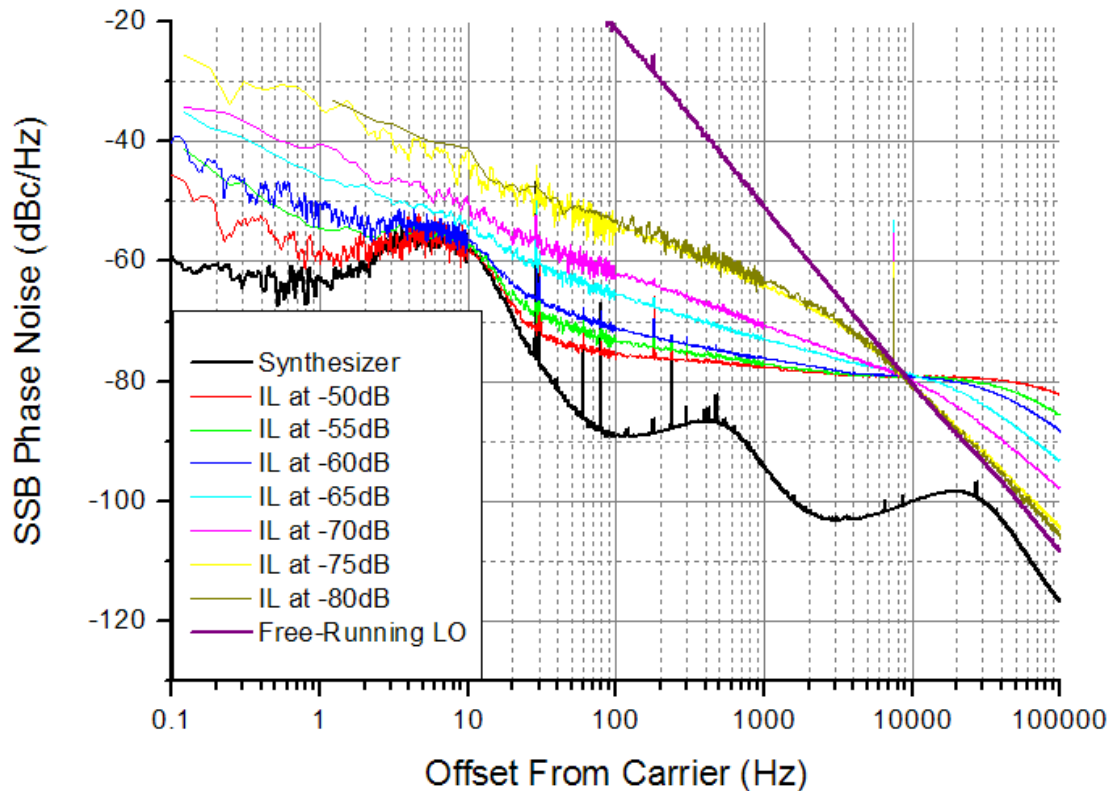


Figure 72 –Phase noise measurements of the low-Q LO locked to the 4-wave mixing signal that is generated by a synthesizer. At low injected powers, the resulting LO output appears similar to the free-running LO. At high injected powers, the LO output more closely matches the synthesizer phase noise. The -80 dBc/Hz limitation due to the noise of the transimpedance amplifier is observed. The noise spike near 7 kHz offset is an artifact of the phase noise measurement system and does not affect the measurements shown.

Figure 72 shows the phase noise at 3.417 GHz with varying injected power ratios. The injected signal originates from a spectrum analyzer that is exciting the 4-wave signal from the atoms. Because of the flicker noise of the photodetector, the -79 dB SNR at 1 Hz bandwidth is observed as an apparent, but frequency-limited noise floor. It is seen that injection locking occurs with as little as 80 dB below the second harmonic LO output power. With an injected power ratio of -80 dB, it is seen that the locking bandwidth is approximately 10 kHz and becomes significantly wider as power is increased. With increased injected power, the noise conforms more strongly to the noise of the synthesizer-created 4-wave signal. It should be observed that, as power is increased, the noise of the oscillator is degraded at large offset frequencies as the oscillator locks to the noise floor from the Johnson noise of the transimpedance amplifier. The noise spike near 7.3 kHz is an artifact from the phase noise measurement system. Other noise spikes are power line noise and unidentified noise from equipment.

6.5.2 Comparison of Best Measurements

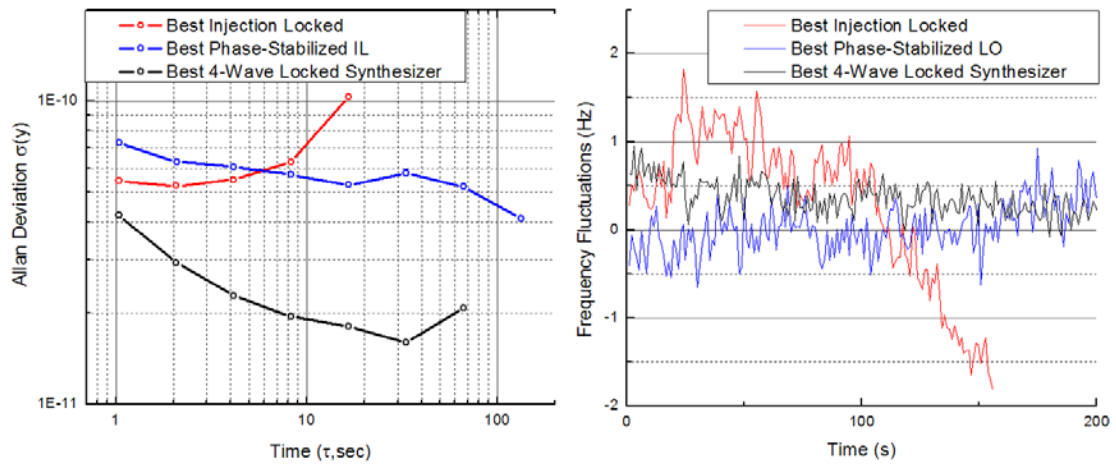


Figure 73 –Frequency fluctuations (right) and Allan deviation (left) of the best example of self-injection locked LO compared to the best measurement of the phase-stabilized self-injection locked LO and the best observed measurement of the synthesizer locked to the DC 4-wave generated output of the atoms. A frequency drift is observed with this and every other observed example of non-phase-stabilized self-injection locking to the atoms. This appears to be significantly corrected in the phase-stabilized case. The typical drift near 20 or 30 Hz, due to the atomic system drift, is observed in the synthesizer-driven case.

Figure 73 shows the Allan deviation of the best short-term result of injection locking compared to the best phase-stabilized injection locking, and the best synthesizer that was stabilized to the 4-wave signal. The system was as diagrammed in Figure 65, but an attempt was made to optimize the system for each of the locking methods. Mostly, the changes involved different locking times and servo loop time constants. Also, the 4-wave servo-locking of the

synthesizer was accomplished by blocking the pump beam with a ^{85}Rb cell as shown in Figure 65, resulting in a high-contrast DC CPT signal. In the same manner, the LO was locked to this high-contrast DC signal. The phase stabilization was implemented as described in section 6.3.2.

The self-locked LO is shown to have a 1-second Allan deviation at 5.5×10^{-11} and drifts before 10 seconds, due to the typical phase drift of the LO (due to temperature fluctuations and bias and tune voltage supply battery drain). The synthesizer shows drift near 30 s, common with this system and similar systems(95), (100) due mostly to temperature fluctuations of lasers and Rb cell. Additional phase stabilization of the self-injection locked LO resulted in improvement in long-term drift, with drifting occurring after 100 s.

6.5.3 Long-Term Measurements

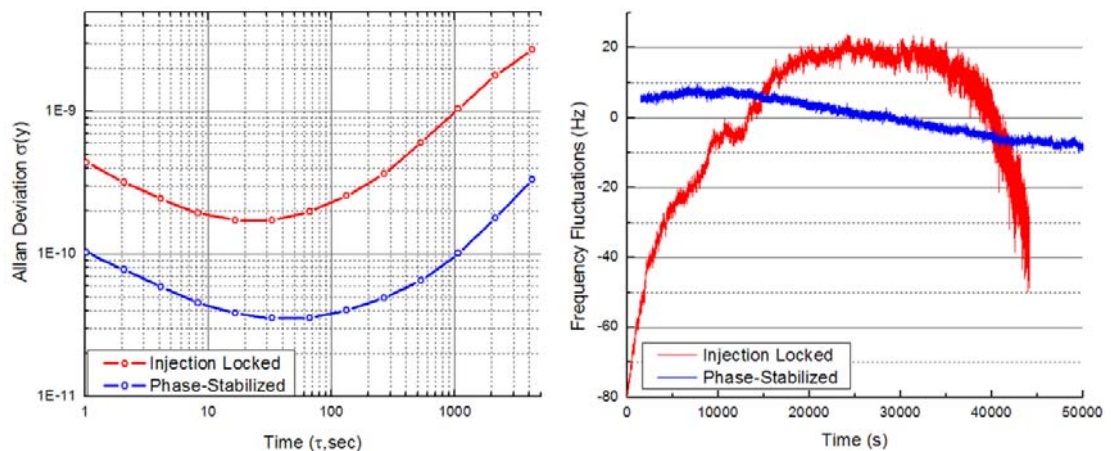


Figure 74 –Frequency drift (right) and Allan deviation (left) of an overnight comparison of non-phase-stabilized self-injection locking and phase-stabilized self-injection locking. The atomic setup remained the same for this comparison.

We observe a greater long-term drift in the non-phase-stabilized case and the frequency stability appears to degrade gradually over time. For these measurements, the LO was temperature stabilized to permit a continuous lock in the non-phase-stabilized case.

Figure 74 shows the results of overnight measurements of the self-injection locked oscillator and the phase-stabilized self-injection locked oscillator. To obtain these measurements, the oscillator was temperature stabilized with a Peltier element and a temperature controller. Additionally, the LO bias was converted to a power supply to reduce bias drift. However, the tune voltage remained on battery power. Without these corrections, we did not observe overnight measurements of the non-phase-stabilized injection locked LO.

Two primary differences are observed. First, the overall frequency drift of the phase-stabilized LO is lower than the simply self-injection locked LO. Additionally, the frequency-domain measurements of the free-running self-injection locked LO is seen to degrade gradually and significantly over time.

6.5.4 Direct Comparison of Techniques: ADEV

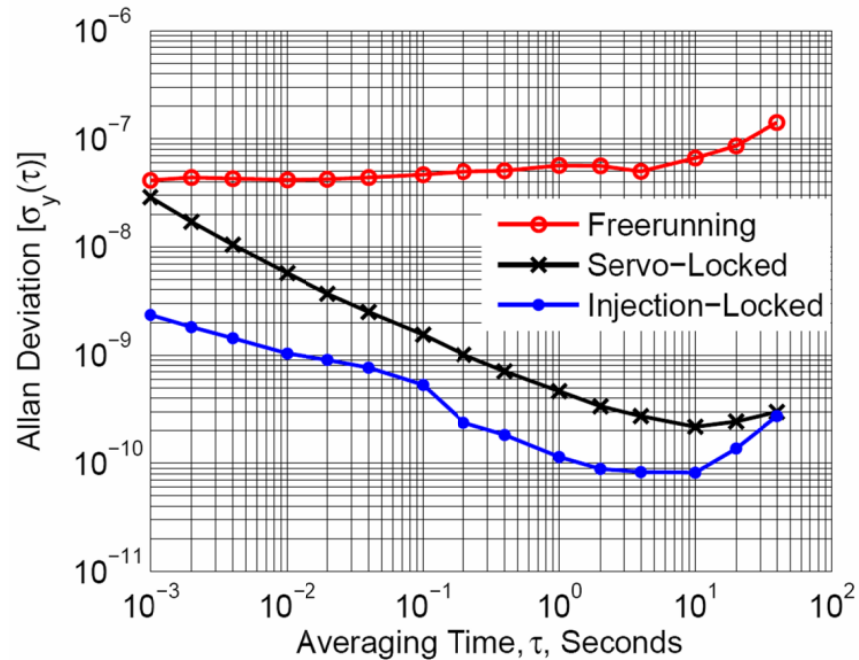


Figure 75 –Frequency instabilities using the different methods. Injection locking is shown to improve the short-term Allan deviation. The servo-locking correction time is shown at approximately 1 ms, and the injection-locking method provides much faster correction. Frequency drift at times greater than 10 s is observed in each method.

Figure 75 shows the time-domain data that were measured under the same conditions (in fact, simultaneously) as the phase noise data in section 6.5.5, Figure 76 below. Notice that the typical servo lock begins improving the fractional frequency instability at 1 ms. The slope follows $1/\tau^{1/2}$, due to the white frequency noise of the atoms, until a drift, which is assumed due to vapor cell temperature changes, is observed after 10 seconds. When the system is

configured for four-wave mixing and injection locking, the signal shows significant improvement in short-term instability. With good temperature stabilization, it is expected that this method will improve the overall stability of ultra-miniature atomic frequency references.

6.5.5 Direct Comparison of Techniques: PN

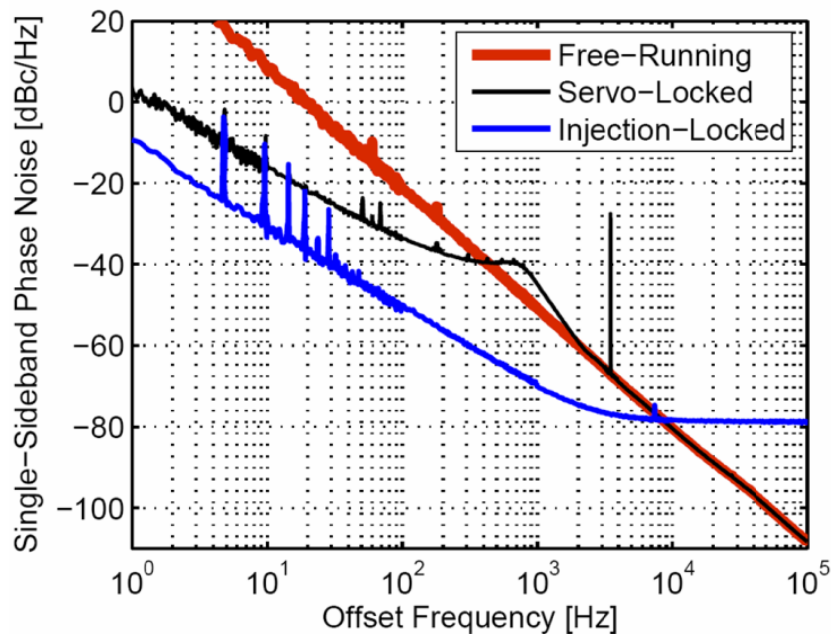


Figure 76 –Phase noise plots comparing the unlocked LO to typical servo control and to the self-injection locking method. Injection locking is shown to improve the close-in phase noise and removes the noise spike at 3.49 kHz, since modulation is not necessary.

Figure 76 shows phase noise measurements of the output of the LO at 3.417 GHz. To obtain these measurements, the LO frequency was down-

converted to 17.3 MHz by mixing against the output of a low noise synthesizer that was stabilized to a hydrogen maser reference. A commercially-available phase noise test set was then used to compare the 17.3-MHz signal against a low-phase-noise, oven-controlled quartz crystal reference. Lock-in amplification and detection (servo-locking) improved the phase noise by more than 40 dB at one Hertz offset, and the noise becomes worse than the free-running LO only around the locking bandwidth near 1 kHz. Here, the phase noise plateau characteristic of lock-in detection is observed, and so is the phase noise spike at 3.49 kHz, due to the required modulation. At frequency offsets larger than the locking bandwidth, we observe that the servo-locked LO matches the free-running LO in performance, as expected.

While keeping the LO bias and tune voltages the same, and while maintaining the same laser intensities and physical setup, the LO was injection-locked to the generated four-wave mixed output of the atoms. This method did not require modulation or lock-in servo electronics for the LO, and we observed a phase noise improvement of 10 dB at 1 Hz offset and 30 dB at 1 kHz offset. The slope of the noise data follows 20 dB per decade until hitting a noise floor at -79 dBc/Hz. This floor seems to be due to the injection locking of the LO to the noise floor of the amplified signal from the photodetector. It is consistent with the 1-Hz bandwidth signal-to-(phase)noise ratio of -79 dB, measured at the output of the amplified photodetector. For frequencies greater than the injection-locking bandwidth, this noise appears to roll off to the original noise floor of the LO, as expected. Using a spectrum analyzer, we observed a locking bandwidth greater

than 20 MHz, depending on injection-locking power. The phase noise at large offsets can be improved by increasing the signal-to-noise ratio from the photodiode or by reducing the injection-locking power. However, this latter method reduces the locking bandwidth. Maintaining a high-bandwidth lock should permit stabilization of the LO during fast perturbations and over a wide range of frequency drifts.

6.5.6 Vibration Sensitivity

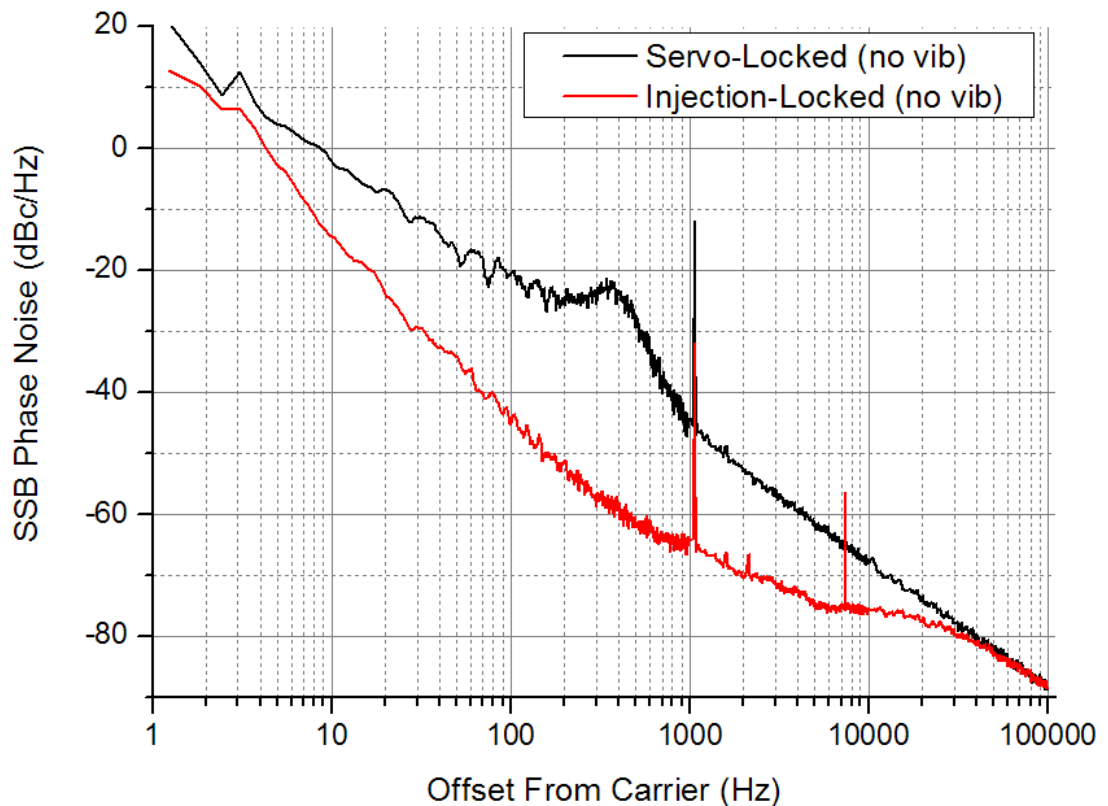


Figure 77 –Phase noise comparison of the servo-locked LO compared to the self-injection locked LO in the case that no vibration is applied. Frequency modulation of the LO is applied at 1.065 kHz in order to implement servo-

locking. To ensure a fair comparison, this modulation is also applied to the self-injection locked LO, though it is not needed. The phase noise spike near 7 kHz is an artifact of the phase noise measurement system and does not affect the results shown. The phase noise bump at 1.065 kHz due to servo-locking is shown. An improvement of the phase noise due to FM modulation is observed for the self-injection locked example. This improvement is the same as the overall difference between the two cases at this frequency.

Figure 77 shows the LO self-injection locked with a 6.834 GHz signal that is 80 dB lower than the LO second harmonic. This permits a locking range near 10 kHz and a lock that is weak enough to observe significant vibration-induced noise. The self-injection locked LO is compared to DC CPT servo-locking to the 4-wave signal. For this DC lock, the LO is modulated at 1.065 kHz for and this modulation is also present on the LO when injection locked, to provide an equal comparison. For these tests, the LO is mounted solidly to the lid of a small metal box and a mechanical shaker is affixed to the box. An accelerometer is also bolted to the lid of the box to measure the frequency and intensity of the vibration. For each comparison, the vibration is kept constant and the only system change is the flip mirror shown in Figure 65 is flipped to divert the output beam from the atoms to the fast photodetector for injection locking and alternatively to the DC photodetector for servo-locking to the 4-wave output signal.

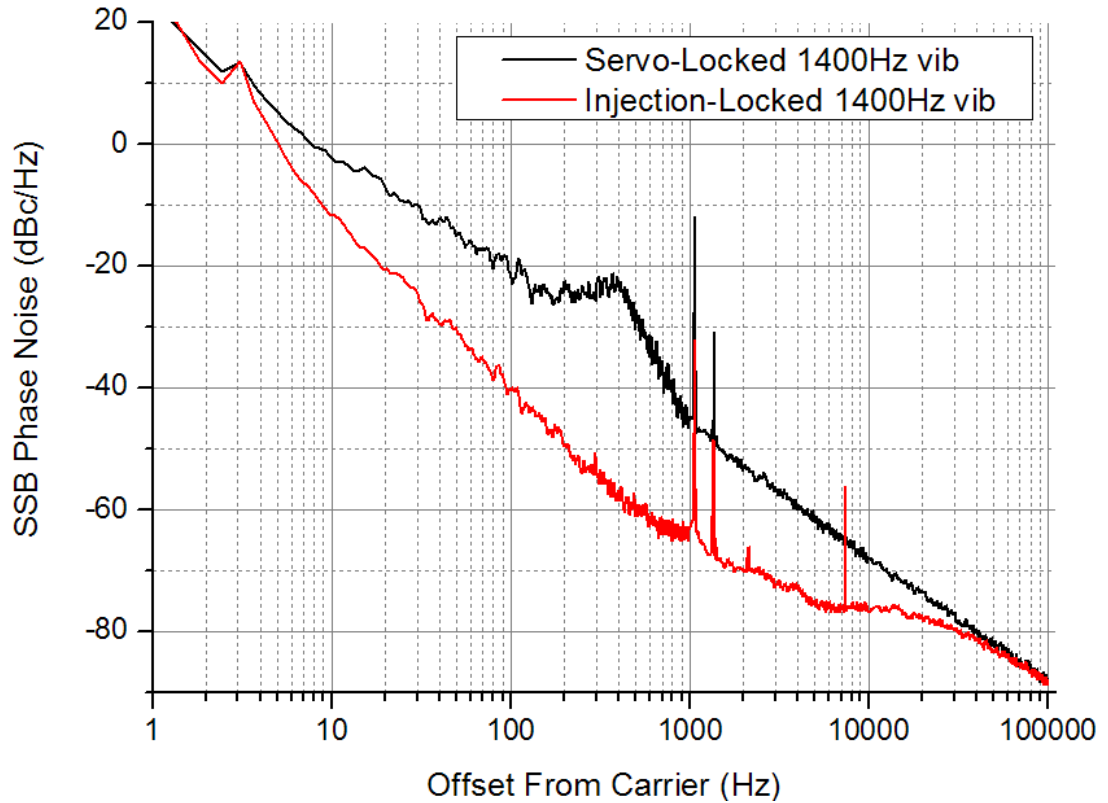


Figure 78 –Phase noise comparison of the servo-locked LO compared to the self-injection locked LO in the case that 1.4 kHz vibration is applied. An improvement of the phase noise due to vibration-induced phase noise is observed for the self-injection locked example. This improvement is the same as the overall difference between the two cases at this frequency.

Figure 78 shows the results of vibration at 1.4 kHz and Figure 79 shows the results of vibration at 575 Hz. The phase noise spike near 7 kHz is an artifact of the phase noise measurement system. In both cases, the modulation causes a phase noise spike at the vibration frequency. The difference in the intensity of this noise spike is equal to the difference between the non-modulated phase noise of the servo-locked oscillator and the injection locked oscillator. However,

as shown in Figure 79, the modulation at 575 Hz begins to degrade the servo-locked oscillator for offset frequencies less than the modulation frequency, resulting in a more significant noise difference at those frequencies.

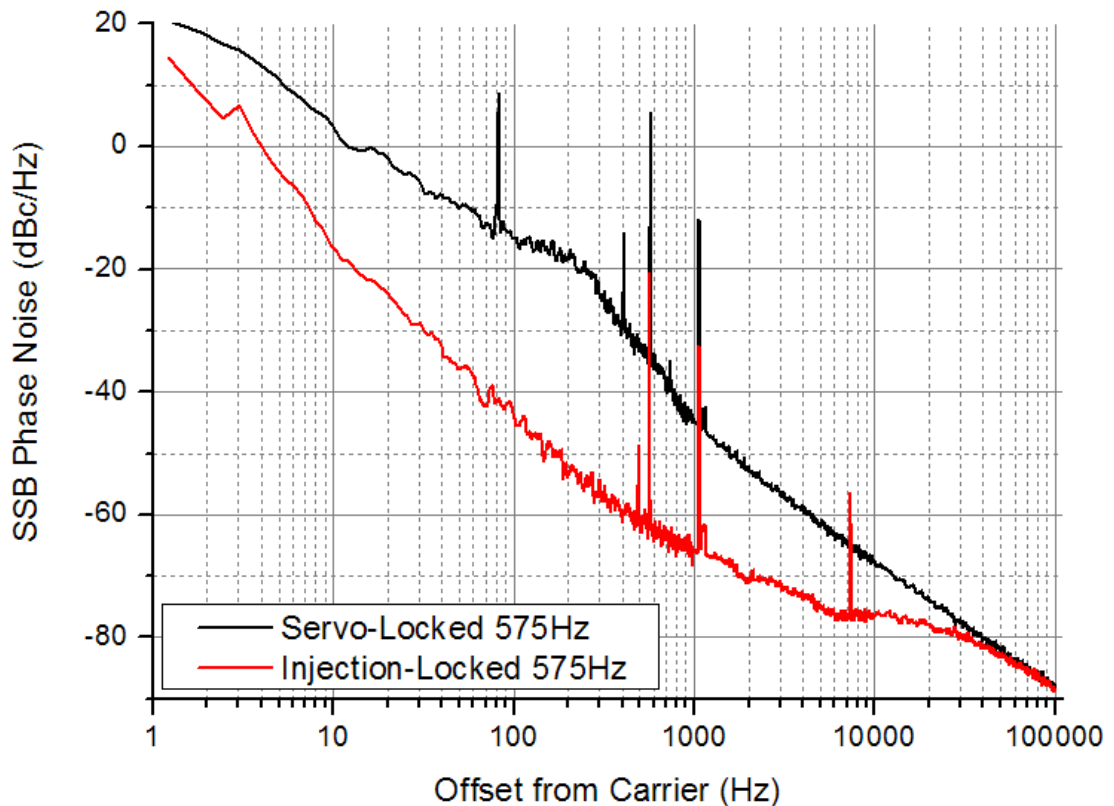


Figure 79 –Phase noise comparison of the servo-locked LO compared to the self-injection locked LO in the case that 570 Hz vibration is applied. In addition to the phase-noise spikes at the vibration frequency, there are spikes that appear to be associated with the oscillator being pushed out of lock. An improvement of the phase noise spikes due to vibration-induced phase noise is observed for the self-injection locked example. This improvement is the same as the overall difference between the two cases at this frequency.

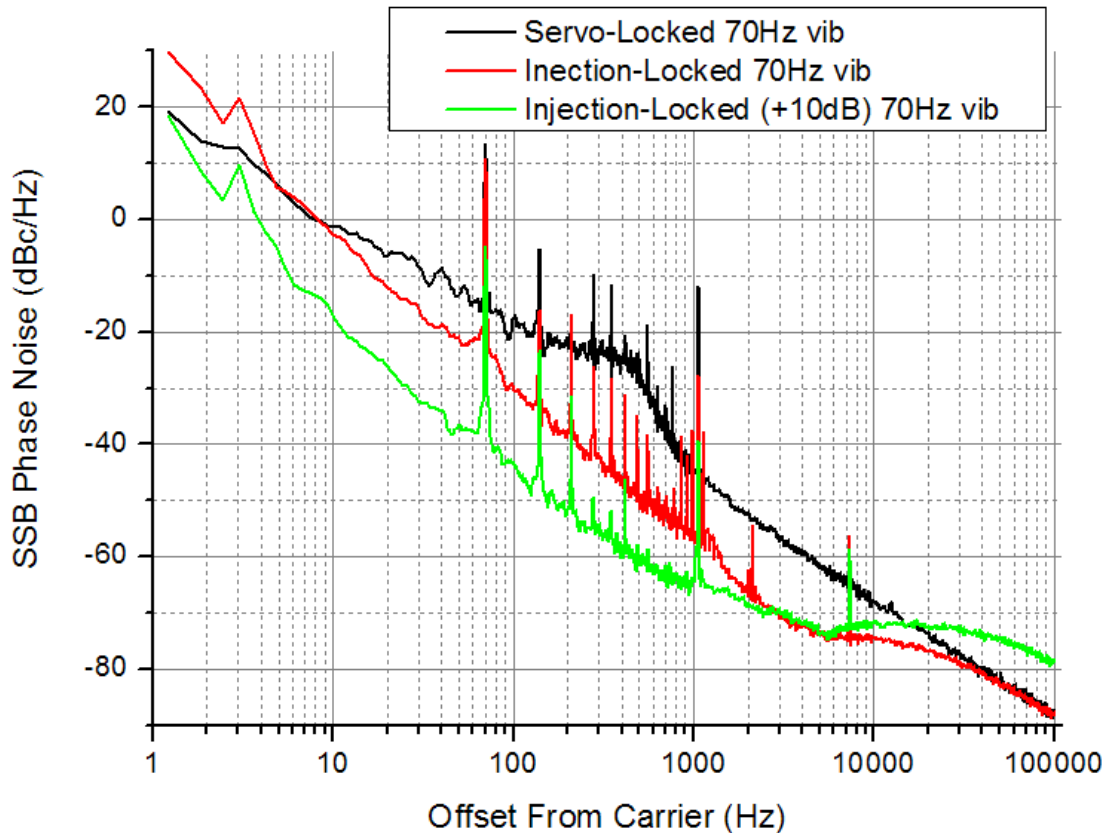


Figure 80 –Phase noise comparison of the servo-locked LO compared to the self-injection locked LO in the case that a 70 Hz vibration is applied. In addition to the phase-noise spikes at the vibration frequency, there are spikes that appear to be associated with both oscillators being pushed significantly away from lock. An improvement of the phase noise spikes due to vibration-induced phase noise is observed for the self-injection locked example. This improvement is generally the same as the overall difference between the two cases at this frequency. A 10 dB increase in the injected signal power significantly improves the results in the self-injection locked example.

Figure 80 shows the result of modulating the LO at 70 Hz, resulting in significant phase noise degradation at small offset frequencies, for both the injection locked LO and the servo-locked LO. This degradation is observed in terms of an overall increase in close-in phase noise as well as the introduction of multiple spikes in both locked cases. In the injection-locked case, significant improvement was obtained with the increase in injection signal strength by 10 dB. In the servo-locked case, the lock was already as strong as we could experimentally determine, by varying the lock-in time constants and correction filtering.

6.6 Advantages

This method achieves a simple, fast and robust lock to the CPT signal, resulting in improved close-in phase noise and short-term frequency instability versus typical servo-locking when used in similar systems. The components consume little power (several mW for the LO, less for the lasers and potentially less for the RF amplifier), showing promise for use in low power atomic frequency references. Since the LO in this experiment occupies less than 0.5 cm² on a substrate, and the VCSEL diodes and photodiode are much smaller, the system is well suited for miniature frequency references.

This method can be adapted for use in miniature atomic magnetometers by use of the magnetically sensitive sublevels $m_F = \pm 1$ instead of the clock transition $m_F = 0$ to set the oscillation frequency. An adjustable phase shift in the microwave loop will switch the oscillation frequency between the clock and

magnetic transitions, allowing for fast accuracy calibration by comparing the magnetically sensitive frequency to the magnetically insensitive one.

Since this injection-locking is achieved at the second harmonic, no power-consuming frequency conversion is required. Also, because electromagnetic radiation at the hyperfine splitting frequency (6.834 GHz for ^{87}Rb) can destroy the CPT pumping of the atoms, operating at half this frequency can allow the LO to be placed very close to the atoms with no harmful effect. The microwave amplifier can be built for low power consumption since its output power remains small.

There are possible benefits in addition to improved close-in phase noise. For example, the removal of modulation of the LO reduces the requirement of low phase noise at twice the modulation frequency, which was due to a unique aliasing effect (31). Finally, some improvement in vibration sensitivity has been observed.

6.7 Limitations

As shown in Figure 73, Figure 74, and Figure 75, the LO and atom drift lead to system drift. The freerunning LO drift is reduced by the atomic stability but some external stabilization will be necessary. This can be accomplished with phase sensitive detection of the phase shift through the injection loop. However, the signal that is sent to the LO tune port must be filtered, requiring external circuitry and reducing some of the benefits of the simplicity of the injection-locked system.

In the case of self-injection locking, the physics package becomes more complicated. The implementation of the system requires an additional laser that needs temperature and current stabilization, a $\lambda/2$ waveplate and two polarizing beamsplitters. A more expensive fast photodetector is required. The light must be focused tightly on the photodetector, possibly resulting in increased vibration sensitivity due to any vibration-induced position changes of the focus point. Finally, the best 4-wave signal strength occurs when the probe beam is locked to the D1 line of 85Rb, requiring an additional atomic cell.

Chapter 7

7. Conclusion

7.1 Conclusion

The last few years have seen the technology of chip-scale atomic clocks grow from an idea(10) to prototypes(104),(105). I anticipate that the next year or two will see the successful commercial development of atomic clocks that have a small fraction of the size and power consumption of existing clocks, with no degradation in stability. Such devices will find applications in many high-end technology applications such as anti-jam GPS, GPS with a faster lock to the military P(Y) code, various communications systems, and other areas where a stable, miniature, and battery-operated frequency reference is desired. At the time of writing this thesis, a number of companies including Honeywell, Symmetricom, Geometrics, Sarnoff Research Labs, Teledyne, Rockwell Collins,

and Agilent, are actively working on developing and possibly commercializing this technology.

The goal of the work presented in this thesis is to make possible the operation of these chip-scale atomic clocks due to the design and implementation of small, low-power, low-phase noise, tunable oscillators that are capable of driving and maintaining a lock to the atomic clock resonance. The design process presented in this thesis required unconventional oscillator design and development of some new methods. At the component level, this involved careful modeling of circuit components, including part selection for temperature compensation and the design of a new method for determining the equivalent circuit model of a varactor diode at microwave frequencies. At the circuit level, the adoption of the two-port method with virtual ground analysis combined with harmonic balance analysis permitted the design of a VCO that is precise in terms of frequency, output power and harmonics, that has predictable phase noise, and that yields intuition into all aspects of the circuit behavior as component values change. The result is a 3.4 GHz oscillator with the best simultaneous size, phase noise, and DC power consumption previously found in literature or commercially available. Extensive measurements validated the usefulness of the oscillator for future commercial chip-scale atomic clocks in terms of frequency stability, temperature drift, vibration sensitivity, and power usage and output. For phase noise analysis, two phase noise measurement systems were designed, one based on phase-locking to a more stable source and

the other with the ability to measure at multiple frequencies and with the potential for automated measurement.

The implementation of this oscillator in the atomic system began with proof-of-concept experiments on optical tables with various macro and miniature atomic clocks. This evaluation culminated with, to the author's knowledge, the first integration of a miniature, low power local oscillator with the miniature physics package of a chip-scale atomic clock. The short term fractional frequency stability of the integrated system (largely a result of the local oscillator) proved adequate for achieving the overall long-term stability goals, if the atomic system can be made to integrate down with the typical $\tau^{-1/2}$ slope. The second integrated system was improved in several aspects, including the heat losses, size, and 60-Hz noise reduction. This second system was then integrated with the control electronics developed by researchers at NIST, and was developed into, to the author's knowledge, the first prototype of a chip-scale atomic clock.

During the course of this work, a new way to lock to the atomic clock resonance was discovered. In this new system, the recent discovery of high contrast DC detection of CPT resonances due to atomic four-wave mixing is converted to a high-contrast microwave detection of this signal. The four-wave mixing process creates an effective microwave filter with a bandwidth on the order of 1 kHz and 80 dB off-resonant signal suppression. Self-injection locking the oscillator to this signal can result in a shorter locking time, increased short-term stability, improved close-in phase noise, and reduced spurious signals as

compared to current techniques used in miniature atomic clocks. New simulations of self-injection locking to this type of system agree well with measured data and confirm that this process is similar to self-injection locking through a microwave resonator with an effective Q factor near 10^6 . It is anticipated that uses for this type of locking will be found in miniature atomic clocks due to its simplicity and low power implementation. It might also prove useful in atomic magnetometers for which fast measurements are desired, as well as fast calibration of the measurement accuracy.

7.2 Contributions

The technical contributions of this thesis can be summarized as follows:

1. Design methodology for low phase noise, low power VCOs, in particular:

- The implementation of the two-port method for optimization of the loaded Q-factor in high-frequency, low-power, and low-phase noise oscillators. The 3.4 GHz oscillator has the best simultaneous size, phase noise, DC power consumption, and thermal stability in literature or commercially available at the time of publication. The combination of harmonic balance techniques and the two-port method permits the design of VCOs that are precise in terms of frequency, output power and harmonics, that have predictable phase noise, and that yield intuition into most aspects of the circuit behavior as component values change.

- An improved, planar, method of obtaining a model for a varactor diode at microwave frequencies for use with other component models in microwave oscillator design.

2. Demonstration of an integrated VCO and chip-scale physics package, in particular:

- The first reported oscillator that is successfully integrated with a miniature physics package. Later, control electronics were integrated, forming a prototype chip-scale atomic clock.
- Measurements-based determination of the requirements of a local oscillator for chip-scale atomic clocks, including the observation of a previously neglected limit arising directly from the modulation of the LO.

3. A new method for atomic clock locking, in particular:

- The self-injection locking of an oscillator to a CPT atomic resonance generated by atomic 4-wave mixing. The method can result in a shorter locking time, increased short-term stability, improved close-in phase noise, and reduced spurious signals as compared to current techniques used in miniature atomic clocks.
- Two techniques for modeling atomic self-injection locking, one using a commercial circuit simulator, the other using an existing theory of microwave self-injection locking.

7.3 Future Directions

In the process of this work, certain improvements have been identified both at the circuit design level and the overall clock locking approach. Some of the main and short-term issues can be summarized as follows.

In terms of improving the VCO circuit, a higher Q resonator such as FBAR and HBAR devices could be employed in future devices that could reach greater stability levels as the performance of the physics package of atomic clocks improves(106). In one case, FBAR resonators have already been employed (36) In addition, the oscillator output could be followed by a low power buffer amplifier to improve the load-pulling effects on LO frequency that we observed due to changes in VCSEL impedance and other loads connected to the output. Finally, future devices will likely explore the use of integrated components, particularly the control electronics board, which is the largest system in the NIST prototypes. The oscillator circuit can also be developed as an integrated circuit with an external resonator. This would reduce the oscillator size to a limit of roughly 2 mm X 2 mm X 4 mm, smaller than current physics packages.

A more thorough characterization of the atomic four-wave system would help define theoretical and practical system limitations. Due to the observations in Section 6.5.6, it is the author's opinion that the vibration sensitivity of a clock, driven by an LO that is similar to the one presented in this thesis, can be significantly improved using four-wave mixing and injection locking versus typically servo-locking methods. An integrated, self-injection locked local oscillator-physics package combination would permit observation of possible

limitations that might exist. Finally, determining whether the self-injection locking technique will prove useful for magnetometry would be an interesting study. With the introduction of a switchable phase shift, it should be possible to rapidly alternate between clock and magnetometer transitions, perhaps permitting a very quick calibration for inexpensive, miniature magnetometers that are both accurate and precise.

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