Dual-Band and Broadband RF Power Amplifiers for Concurrent Signal Transmission

by

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B.S., New Jersey Institute of Technology, 2016

M.S., University of Colorado, 2018

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

May 2021

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Broadband power amplifiers are becoming increasingly important for communications and radar phased array applications. Amplifying concurrent signals allows for increased data throughput with carrier aggregation and improved radar tracking performance, among other benefits. However, non-concurrent broadband amplifier design is limited in performance by fundamental matching limitations, and suffers further in the concurrent mode due to signal mixing.

To reduce the cost of phased arrays, a low-cost GaN-on-Si technology is first investigated on which broadband power amplifiers are designed and fabricated. Various passive structures are simulated to validate process stack-up simplifications, along with the design and characterization of a narrowband proof-of-concept X-band power amplifier. Fundamental limitations are summarized and utilized to develop a design procedure for multi-stage power amplifiers with increased gain for phased array applications. This procedure is confirmed with a fabricated matching network. These results are then used in dual-band and broadband power amplifiers designs, which are fabricated with commercially available GaAs and GaN technologies. Hybrid and MMIC implementations in both cover 2-18 GHz in aggregate.

The power amplifier characterization focuses on comparing each implementation in the non-concurrent and concurrent mode to understand the effect each power amplifier has on signal amplification. A new broadband power amplifier architecture is developed to improve the performance of broadband power amplifier amplifying concurrent signals. Results indicate that a PA with this architecture can achieve similar power and efficiency as compared to a standard broadband PA, whereas linearity can be improved and/or simplified using this approach.

Dedication

Dla mojej rodziny.

Acknowledgements

Just as this thesis is a collection of the research I have performed, it is also a reflection of my interactions with colleagues, friends, and family that have supported me along the way. First and foremost deserving of praise is my advisor, Zoya Popović, as a constant role model and mentor. Without her I would not have developed the drive and curiosity that is vital to research, had the flexibility to investigate my interests without worrying about funding, and had the pleasure to work with such a wonderful group. In particular, Akim Babenko, Eric Berry, Patrick Bluem, Tommaso Cappello, Devon Donahue, Allison Duh, Maxwell Duffy, José Estrada, Gabriel Botello, Dan Fishler, Seth Johannes, Michael Litchfield, Daniel Martin, Laila Marzall, Connor Nogales, Prathamesh Pednekar, Mauricio Pinto, Nina Popović, Sushia Rahimizadeh, Megan Robinson, Aman Samaiyar, Matthew Schoomaker, Dakotah Simpson, Tim Sonnenberg, Rob Streeter, and Shane Verploegh have all been positive influences professionally and a pleasure to have become friends with. Other faculty at the university, including Taylor Barton, Dejan Filipović, Edward Kuester, and Gregor Lasser, are all exceptional and additional sources of expertise and motivation beneficial to me. Outside the university, I have learned a great deal from my colleagues at the MIT Lincoln Laboratory: Chang-Lee Chen, Christopher Galbraith, Jeffrey Herd, Ryan Johnson, Jeffrey Knecht, and Joseph Varghese. My friends, Alexander Denton, Kate Enenbach, Jacob Friedlein, Michael Grayson, Guillermo Nevett, and Charles Rackson, contributed to maintaining my sanity during the hard parts and helped enjoy the good parts even more. Finally, and most importantly, I must thank my family, Barbara Zurek, Roman Zurek, and Olivia Zurek, and my partner, Shireen Warnock, for their selfless support along the way.

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Introduction

This thesis addresses the trade-off between high efficiency and broad bandwidth of a radio-frequency (RF) power amplifier (PA). As is shown in Chapter 3, both properties cannot be simultaneously maximized, and two main approaches to avoid this limitation are considered: (1) focusing on only two narrow bands, instead of a broad bandwidth, amplified by a single (dual-band) PA; and (2) combining two narrow-band PAs into a single broadband PA.

When these approaches are implemented and used to amplify a single (non-concurrent) continuous-wave (CW) signal, similar performance (gain, output power, efficiency, and linearity) can be obtained as compared to a narrow-band PA counterpart. However, when multiple simultaneous (concurrent) signals are amplified, output power and gain are decreased for the dual-band and "standard" broadband PAs due to the transistor's fixed total output power, and due to signal mixing generating intermodulation (IMD) power. This also lowers the efficiency and linearity of both PAs; however, the decrease in linearity for concurrent signals can largely be avoided if the second PA architecture from above is utilized.

By improving concurrent PA performance, modern phased-arrays can be enhanced in applications such as communications systems and radar, as phased arrays contain many PAs. This introductory chapter motivates and provides background information of the work in context of these applications in Section 1.1, and summarizes the work of each chapter in Section 1.2.

1.1 Background and Motivation

PAs are found in a wide variety of systems utilizing phased arrays, such as: radar [5–7], satellites [8, 9], cellular base stations [10, 11], and mobile phones [12, 13]. Advanced phased arrays are necessary in 5G cellular communications [14,15], in addition to radar and satellite, applications. This section summarizes the components of an advanced phased array, with particular emphasis on the PA and the signals it amplifies.

1.1.1 Phased Arrays

Phased array technology has evolved through several stages over the past century [5]. Passive phased arrays feature a single up/down-conversion and amplification chain, with analog beamforming distributing a signal to phase shifters prior to each antenna element. By controlling the phase along the path of each element, the main antenna beam of the array can be steered electronically. However, early phase shifters had significant losses, negatively affecting the sensitivity of passive phased arrays.

Active phased arrays contain amplification blocks between each phase shifter and antenna element, reducing path loss, and increasing sensitivity. Minimally, the amplification chain consists of a PA for transmit, low-noise amplifier (LNA) for receive, switch, and phase shifter, and together is usually referred to as the transmit/receive (T/R) module. A single up/down-conversion block is still employed, unlike more current subarray digital phased arrays. These arrays add digital beamforming prior to several digital receiver/exciter (DREX) blocks at the subarray level, each of which contain a digital-to-analog converter (DAC), analog-to-digital converter (ADC), mixer, and a local oscillator (LO), to perform up/down conversion. Like active phased arrays, the subarray output feeds into an analog beamforming network. This approach allows for multiple simultaneous beams at the same frequency over a limited scan sector, and the capability for sophisticated spatial processing techniques [5].

Modern phased arrays are increasingly moving towards DREXs at the element level, rather

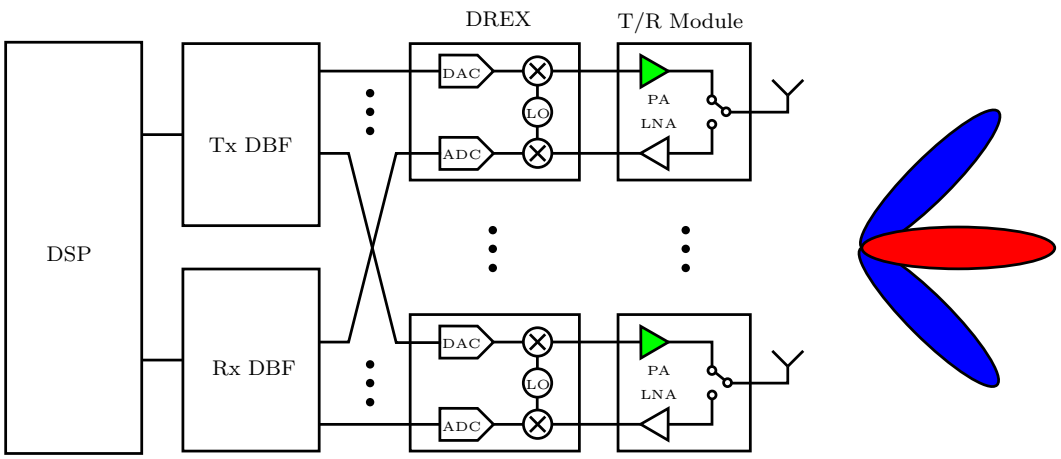


Figure 1.1: Element-level digital phased array block diagram showing the digital signal processing unit, transmit/receive digital beamforming networks, digital receiver/exciters, transmit/receive modules, and antennas. Depicted also is a representative multi-beam antenna pattern, with different colors representing different frequencies. This thesis focuses on the power amplifier, highlighted in green.

than the subarray level [15,16]. A block diagram of this element-level digital phased array is shown in Fig. 1.1. It consists of a single digital signal processor, transmit (Tx) and receive (Rx) digital beamforming (DBF) networks, and at each element: a DREX, T/R module, and antenna. T/R modules no longer require phase shifters due to digital signal processing (DSP) controlling the angles of multiple beams independently, with a representative pattern also illustrated in the figure.

There are several advantages to this element-level approach, a notable one being that any number of beams can be generated with DSP, allowing for hypothesis testing of multiple scenarios in radar applications. The cost, size, and power consumption considerations that have prevented element-level DREXs in the past are being improved to enable demonstrations of element-level digital phased arrays for satellite [9], mobile [13], (multiple-input multiple-output) MIMO [11], and radar [7] applications. In typical radars, the DREX elements account for about a quarter of the total cost [5]. The phased array, on the other hand, usually accounts for about half of the total radar cost, with the T/R modules being about half of the phased array cost. The work of Chapter 2 demonstrates a relatively low-cost gallium-nitride on silicon (GaN-on-Si) technology being developed by the Massachusetts Institute of Technology (MIT) Lincoln Laboratory to reduce

this T/R module cost. The approach also enables low-cost element-level digital phased arrays through future wafer-scale DREX and T/R module integration [17, 18], with a photograph of a wafer and reticle shown in Fig. 1.2. Other commercial technologies used for T/R modules, including gallium-nitride on silicon-carbide (GaN-SiC) [19], gallium-arsenide (GaAs) [20], silicon-germanium (SiGe) [21], and complementary metal-oxide semiconductor (CMOS) [22], either suffer from a lack of performance or increased cost as compared to GaN-on-Si.

Because with both subarray and element-level digital phased arrays multiple simultaneous beams can be generated, with appropriately broadband RF components these beams can be generated at multiple frequencies, as depicted in Fig. 1.1 with different colors. Linear amplification of multiple signals present within a broad RF bandwidth finds many uses in radar [23, 24] and communications [25, 26] applications. For example, multi-band radar [27] offers advantages such as improved tracking range due to better tolerance to atmospheric effects, inherent resistance to jamming and interference, wider choice of waveforms for more accurate range and Doppler measurements, and improved target recognition with sufficient separation between bands. Communications such as 5G often employ modulation schemes with carrier aggregation to increase data transfer

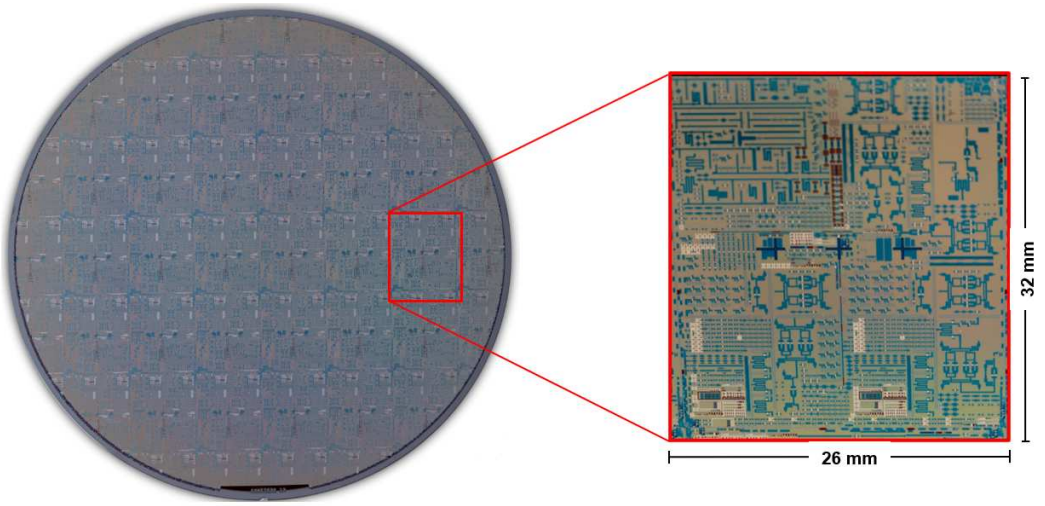


Figure 1.2: Photograph of MIT Laboratory GaN-on-Si 200 mm diameter wafer. Repeated across the wafer is a 26 mm x 32 mm reticle containing passive structures such as transmission lines, various transistors, PAs, LNAs, switches, and a T/R module.

rates [28, 29]. To enhance these phased array platforms, broadband antennas (not considered in this thesis) and T/R modules are necessary.

Circuit design of broadband PAs will be considered in-depth from Chapter 3 onwards. Shown in Section 1.1.3, the PA has a significant impact on power and thermal constraints, and is generally the most power-consuming and heat-generating component of a T/R module to design. Therefore, the other components are not considered in this thesis, except for a brief consideration of a simple switch demonstrated in Section 6.2.1. To better understand PA specifications and challenges, signal characteristics are reviewed in the following section.

1.1.2 Signals

The well-known orthogonal frequency-division multiplexing (OFDM) digital communications signal is summarized in this section. Similar signals are used throughout the remainder of this thesis to demonstrate PA functionality. Radar signals are not considered as many tend to be proprietary; regardless, they have comparable properties to an OFDM signal, giving similar PA responses. OFDM encodes several channels of information onto several corresponding frequencies, all contained within some bandwidth [30, 31]. It is implemented in several standards, such as IEEE 802.11a [32], cellular 4G LTE, [33], and cellular 5G [34], which determine the signal's characteristics. In this section, the 802.11a standard is used with a relatively simple process [1] as an example, with 4G LTE and 5G signals used in later chapters.

1.1.2.1 OFDM Digital Signal Encoding

To create an OFDM signal, a binary digital bitstream is first encoded with an error-correcting code [35] to minimize errors over a noisy channel. The Shannon-Hartley theorem defines the maximum data transfer rate over a noisy channel as:

$$C = B \log_2 \left(1 + \frac{S}{N}\right), \tag{1.1}$$

where C is the channel capacity (bits/s), B is the channel bandwidth (Hz), S is the average

received signal power (W) in the bandwidth, and N is the average noise power and interference (W) in the bandwidth. The ratio S/N defines the signal-to-noise ratio (SNR) of the channel, with the error-correcting code effectively increasing SNR. The two main types of error-correcting codes are block codes and convolutional codes [35], and in principle operate by adding redundancy. For example, if each bit of the bitstream is duplicated three times in succession during transmission, the receiver would examine sets of three bits and take the majority occurrence. This forms a simple $1/3$ code, making the initial bitstream three times as long. Modern codes are much more efficient in a variety of ways, with turbo codes [35, 36] combining convolutional and block codes to be the first to approach the Shannon limit (1.1). They are often used in cellular communications.

Encoded data is typically also interleaved to account for noisy channels with memory. This memory effect manifests itself as burst error, with bit errors all occurring in finite groups rather than being randomly spaced. Interleaving rearranges encoded data such that after decoding, errors are more likely to be randomly spaced [36]. Most error-correcting codes assume, and perform better, with such spacing.

1.1.2.2 OFDM Constellation Mapping

Interleaved data is next grouped in sections of n bits corresponding to the digital modulation scheme used. The 802.11a standard utilizes binary phase-shift keying (BPSK) ($n = 1$), quadrature phase-shift keying (QPSK) ($n = 2$), 16 quadrature-amplitude modulation (QAM) ($n = 4$), and 64-QAM ($n = 6$) schemes, depending on the user's SNR [37]. These bits are then mapped, or modulated, by the schemes onto a constellation point, shown in Fig. 1.3 with in-phase (I) and quadrature-phase (Q) axes. These axes represent two orthogonal signal carriers which can be generated with a shared LO feeding one mixer directly, and feeding another mixer through a 90° delay line. The I and Q components of the constellation point are generated by two clocked DAC components and fed into the mixer to modulate the carrier at the clocked frequency [31].

BPSK modulates the phase of a carrier frequency by 180° corresponding to whether a constellation point represents a bit of 0 or 1, and so does not contain a quadrature-phase component.

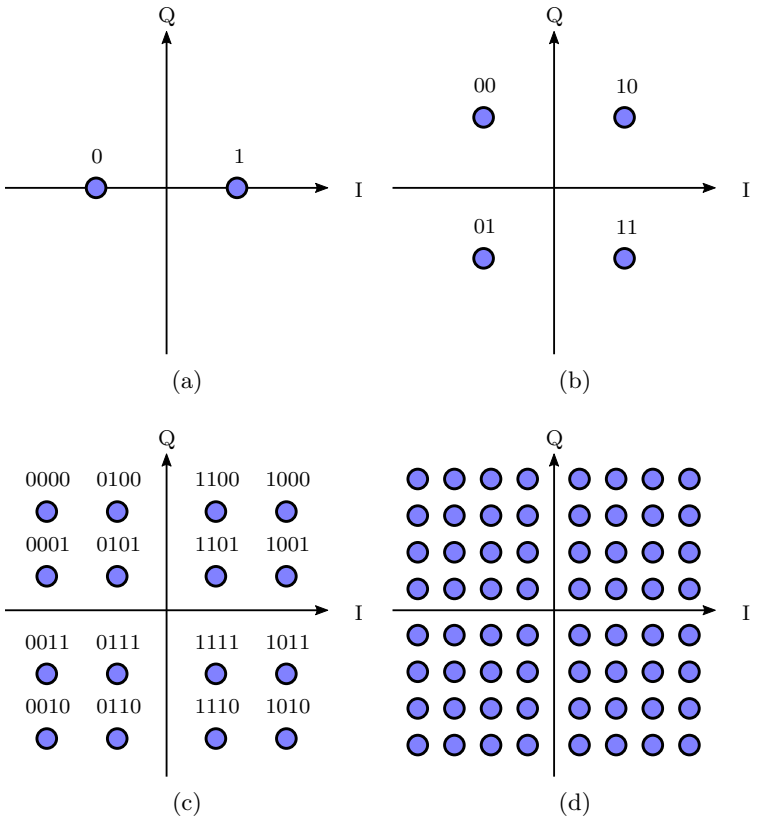


Figure 1.3: Constellations of (a) BPSK, (b) QPSK, (c) 16-QAM, and (d) 64-QAM modulation schemes. Note that Gray coding is implemented, with points next to one another having only one bit different between them.

QPSK modulates the phase of a carrier by 90° corresponding to whether bits are 00, 01, 11, or 10 (signifying Gray coding to minimize bit error). Therefore, the DACs of both can be implemented with a single dual-polarity voltage source. 16-QAM and 64-QAM schemes, on the other hand, modulate the phase and amplitude of a carrier. Therefore, the DACs will need two and four voltage levels, respectively, all with dual polarity.

1.1.2.3 OFDM Waveform Generation

In 802.11a, 48 data sub-carriers are utilized, meaning that 48 unique groups of n data bits are mapped per OFDM symbol onto 48 distinct frequencies. In phased array applications, this modulation in the RF domain becomes increasingly impractical with many antenna elements, as

each element would need at least a multiplexer and two DACs with voltage supplies *per frequency*. Therefore, this modulation process is typically implemented with DSP. Each scheme maps a group of n bits to a complex number corresponding to its particular constellation point. In addition to these 48 data sub-carriers, 4 pilot sub-carriers are also used, for a total of 52 sub-carriers. These 52 complex numbers are loaded into 64 fast-Fourier transform (FFT) frequency bins and converted into the time domain with a discrete inverse fast-Fourier transform (IFFT) function.

To remove the high-frequency content of this discrete-time signal, a digital low-pass finite impulse response (FIR) filter is applied [37]. The real (I) and imaginary (Q) parts of this analog time-domain signal are clocked separately by two multi-level DACs at 20 MHz, corresponding to a sub-carrier spacing of 312.5 kHz (20 MHz / 64). These two paths can now feed the two orthogonal frequency carriers described previously, and together could constitute a simple DREX. Due to the orthogonal nature of the signal, spacing each sub-carrier by 312.5 kHz places the nulls of each sinc function at the peaks of the others. This prevents inter-symbol interference (ISI) [1, 31] and is illustrated in Fig. 1.4.

The final 0.8 μs of each 3.2 μs (1 / 312.5 kHz) waveform is repeated at the beginning, forming the final 4 μs OFDM symbol. This 0.8 μs guard interval containing the cyclic prefix is important to include as it minimizes the effect of multi-path on a noisy channel [31]. An example OFDM signal is shown in Fig. 1.5, with (a) plotting the frequency-domain and (b) plotting the time-domain of

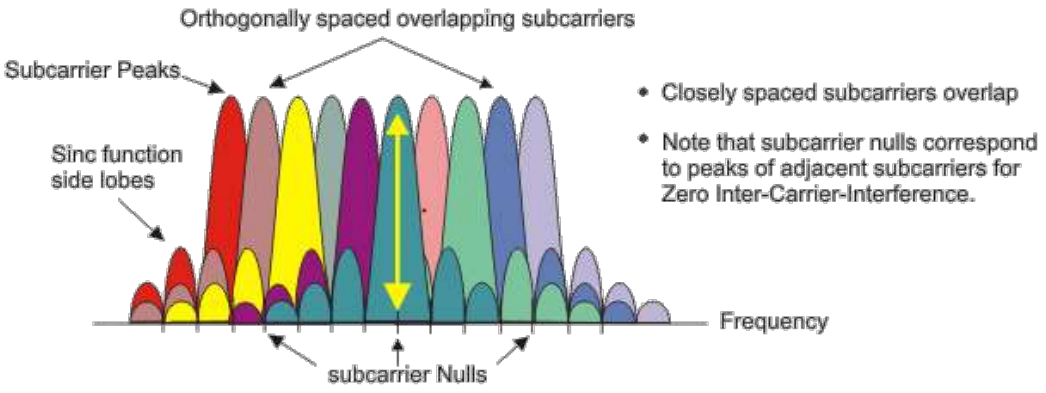


Figure 1.4: Orthogonally-spaced sinc functions places the peak of one at the nulls of the others, preventing interference, and is key for OFDM [1].

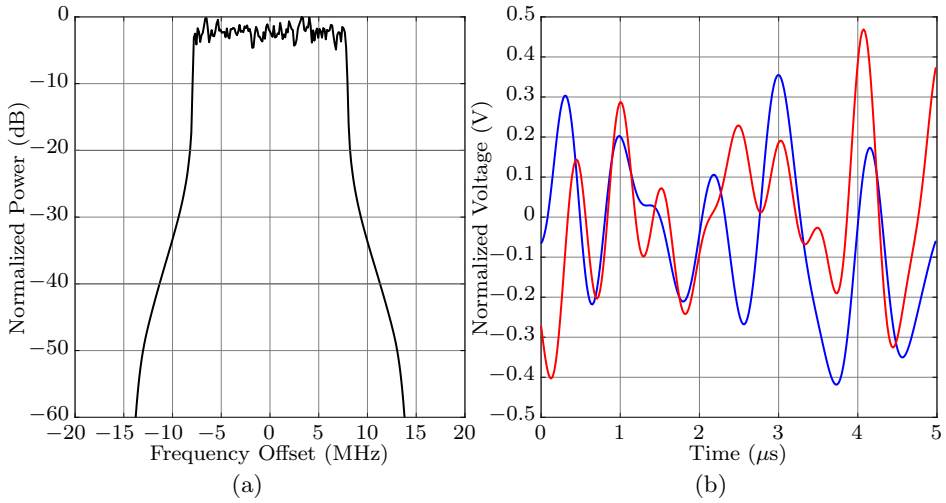


Figure 1.5: An example 20 MHz OFDM signal in the (a) frequency domain and (b) time domain. The real (I) portion of the signal is in blue, and the imaginary (Q) portion is in red.

the signal. To decode a received 4 μs signal, the entire process is reversed to obtain the transmitted digital bitstream. The algorithms used to encode and interleave the data typically must be known *a priori* by both users. It is noted that an advantage of OFDM is transmission at a slower symbol rate, reducing the analog circuit complexity and clock speed. This circuitry, though, must be able to perform the FFT function faster than the symbol rate.

A major disadvantage of OFDM is related to its signal's large crest factor C and PAPR values [31], related by:

$$PAPR = \frac{|x_{peak}|^2}{x_{rms}^2} = C^2, \tag{1.2}$$

where $x = \sqrt{I^2 + Q^2}$ corresponds to the voltages output by the DACs. This is considered further in Section 1.1.3.

1.1.2.4 OFDM Transmission

With a $^3/_4$ convolutional coding rate and 64-QAM, the 802.11a standard can achieve at most a $(6\,\text{bits} \cdot {}^3/_4 \cdot 48)\,/\,(4\,\mu s) = 54\,\text{Mbits/s}$ data rate over a 20 MHz channel. For comparison with the Shannon limit (1.1), a channel with 60 dB SNR can transfer at most approximately 399 Mbits/s. However, if a user experiences a degraded SNR, it may be advantageous to use a

smaller n modulation scheme to decrease bit-error rate (BER) due to tight constellation points being affected by noise and nonlinearities (such as those from a PA), effectively lowering the SNR and channel capacity per (1.1) [37].

To maximize the data transfer rate of any OFDM standard, one may consider increasing the modulation order, *e.g.* 256-QAM. However, for constant energy per bit to noise power spectral density ratio E_b/N_0 (a metric used to compare the BER of different modulation schemes), 256-QAM has a higher BER than lower orders for similar reasons a degraded SNR increases constellation ISI [37]. Increasing the channel bandwidth instead directly increases (1.1), but requires appropriately broadband systems. Alternatively, combining multiple widely-spaced channels with carrier aggregation also increases data rates [28,29]. This thesis demonstrates several PAs that can be used in broadband systems to achieve this, with the next section reviewing basic PA characterization concepts. PA design is covered from Chapter 3 onwards.

As will become clear in the next section, a PA transmitting a signal with a large PAPR value will have a much lower average efficiency than if it were transmitting a CW signal. Because of the many advantages of OFDM, however, this disadvantage is often accepted. Various PA architectures for efficiency enhancement, such as the Doherty or supply-modulation, help in increasing the efficiency at lower output powers, and therefore the average efficiency [38]. This thesis does not consider such techniques, but would be natural in future work.

1.1.3 RF Power Amplifiers

A PA is typically the final of a series of amplification stages for an RF signal, and is often called a high-power amplifier (HPA) because it typically produces the most RF and consumes the most direct current (dc) power. Assuming the PA is connected to $50\,\Omega$ loads, its input envelope voltage (also known as the peak value of the RF voltage) $v_{in}(t) = x(t)$ (V) is related to its input RF power by:

$$P_{in}(t) = 10 \cdot \log_{10}\left(1000 \cdot \frac{1}{2} \cdot \frac{|x(t)|^2}{50}\right) (\text{dBm}), \tag{1.3}$$

with t representing each discrete sampled point in time by the DAC. A similar equation for output envelope voltage $v_{out} = y(t)$ (V) and output RF power $P_{out}(t)$ (dBm) can be written, and from these, gain can be defined as:

$$\text{Gain}(t)(\text{dB}) = P_{out}(t)(\text{dBm}) - P_{in}(t)(\text{dBm}). \tag{1.4}$$

RF power amplification is performed by converting dc power. The efficiency of a PA can be described by its drain efficiency $\eta_D = {}^{P_{out}}/_{P_{dc}}$ or, considered throughout this thesis, power-added efficiency (PAE):

$$\text{PAE}(t) = 100 \cdot \frac{P_{out}(t) - P_{in}(t)}{P_{dc}(t)}(\%), \tag{1.5}$$

where $P_{dc}(t) = I_{DD}(t) \cdot V_{DD}(t)$. For a CW signal at a particular power, $x(t)$ and $y(t)$ are constant in time, leading to constant P_{in}, P_{out}, and gain. Therefore, $I_{DD}(t)$ is constant in time, and without supply modulation, $V_{DD}(t)$ and P_{dc} are also constant in time. The envelope voltage of an 802.11a modulated signal changes at 20 MHz, and so it will not have constant P_{in}, P_{out}, and gain values. Therefore, $I_{DD}(t)$ will also not be constant in time, and the average and maximum values of PAE can be calculated over some time period.

Equation (1.5) demonstrates the need for a high-efficiency final PA over a range of output powers. For example, a 50 % PAE 10 W P_{out} single-ended (one transistor) single-stage (of amplification) final PA with 10 dB gain draws 18 W P_{dc} and produces 8 W of heat. A similar single-ended driver PA preceding this might have 50 % PAE, 1 W output power, and 10 dB gain, drawing only 1.8 W P_{dc} and producing 0.8 W of heat. About 91 % of this total dc power is consumed by the final PA. On the other hand, a 30 % PAE 10 W P_{out} final PA with 10 dB gain draws 30 W P_{dc} and produces 20 W of heat. This significant additional heat generation degrades the gain of the PA, and in phased arrays, scales with the number of elements transmitting across the aperture. Increasing the efficiency of the PA greatly simplifies the problem of phased array heat dissipation.

High-efficiency PA design techniques are commonly implemented to reduce P_{dc}. Three main

categories include: 1) reducing the conduction angle to reduce voltage and current overlap (classes AB, B, and C); 2) waveform shaping by harmonic terminations, in addition to reduced conduction angle (class F); and 3) operating the transistor as a switch (classes D and E) [2]. All introduce harmonics, making any efficient PA inherently nonlinear. With PAs that have an octave of bandwidth or more, however, harmonic terminations become increasingly difficult to implement as higher fundamental frequencies can be the harmonics of lower fundamental frequencies, requiring additional matching network considerations. Additionally, as the RF bandwidth of a PA increases, the efficiency decreases [39], as will be explored in Chapter 3.

A PA block diagram is shown in Fig. 1.6. The main components include the input-matching network (IMN), output-matching network (OMN), gate bias-tee, drain bias-tee, and active device. A field-effect transistor (FET), specifically a high electron-mobility transistor (HEMT) in this thesis, is often used for the active device in high-power microwave applications [2]. Because most HEMTs are depletion mode devices, a negative dc gate voltage must be applied to deplete the channel, preventing current flow. With a fixed drain voltage, the pinch-off gate voltage at which the drain current begins to increase is used for class B PAs. The RF voltage modulates the dc gate voltage, making the transistor conduct above pinch-off; for CW signals this is half the time. Class AB PAs are biased above, and class C below, this pinch-off value. With the transistor not continuously conducting, the half-wave rectified current waveforms of class B PAs have harmonic frequency content that can be calculated with the Fourier transform.

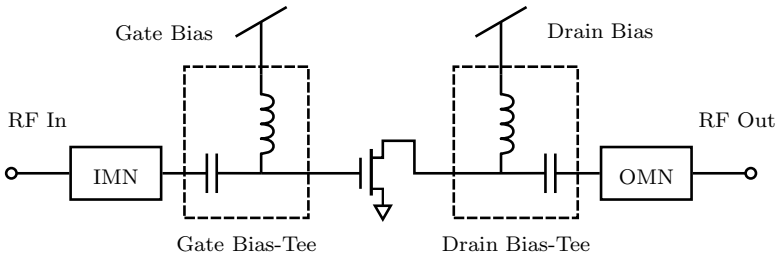


Figure 1.6: Simple PA block diagram containing IMN, OMN, gate bias-tee, drain bias-tee, and transistor.

1.1.3.1 Signal Distortion

Various metrics are used to define the linearity of a PA, indicating how much signal distortion is expected. For CW signals, the drive-up curves are considered and shown in Fig. 1.7, plotting gain and efficiency as a function of output power. For a well-designed common class-AB amplifier, the gain would be linear in back-off (lower power values) before decreasing in compression (higher power values). The P1dB output power point is often quoted, which occurs for the output power with gain decreased by 1 dB from its linear value. To maintain linearity, hence minimizing signal distortion, one could choose to keep output power and gain in the linear region. However, efficiency typically grows rapidly before peaking around the P1dB or P3dB points, requiring a CW signal to be amplified in the nonlinear region for maximum efficiency. Because of the nonlinearities, fundamental frequency harmonics begin to appear in the output spectrum as well, which in many applications would need to be removed with a low-pass (LPF) or band-pass filter (BPF) [40]. Also plotted is the probability-density function (PDF) of a high PAPR signal, noting how the PA amplifying this signal experiences relatively low efficiency most of the time. Efficiency-enhancement techniques [38] focus on improving this efficiency in back-off, along with signal processing techniques such as crest-factor reduction (CFR).

Two-tone measurements are used to partially characterize the linearity of a PA amplifying a modulated signal. By inputting two CW signals at $f_c \pm \Delta$:

$$\frac{1}{2}\cos\Big(2\pi\big(f_c+\Delta\big)t\Big)+\frac{1}{2}\cos\Big(2\pi\big(f_c-\Delta\big)t\Big)=\cos\big(2\pi f_c t\big)\cos\big(2\pi\Delta t\big), \tag{1.6}$$

the resulting amplitude-modulated signal oscillates at f_c, with its envelope oscillating at Δ. Because of the Δ envelope, the RF power has a 3.01 dB PAPR, decreasing the average PAE of the PA closer to what the modulated signal would produce, unlike a CW test signal. In addition, 3^{rd} order IMD products will be generated at $f_c \pm 2\Delta$, limiting output power. The difference between the fundamental $f_c \pm \Delta$ tones and the $f_c \pm 2\Delta$ IMD products is the commonly quoted two-tone measurement value, and it will be considered in Chapters 4 and 5 for concurrent signals. For a

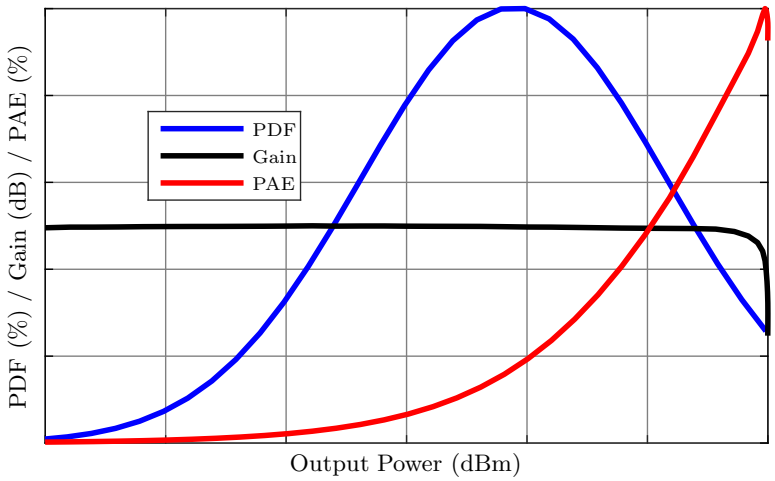


Figure 1.7: Typical PA performance over output power, along with an overlaid probability density function of a typical OFDM signal [2].

non-concurrent 20 MHz 802.11a signal, for example, $\Delta = 10$ MHz would be chosen for the two-tone PA characterization at some RF carrier frequency because this two-tone test signal has the same envelope frequency as the desired modulated signal.

Linearity for a modulated signal, *e.g.* OFDM, can also be directly quantified both in-band and out-of-band. Communications systems often stagger frequency channels adjacent to one another [25,26]. For example, consider an 802.11a signal occupying the spectrum between $f_c - \Delta$ and $f_c + \Delta$. Assuming no guard band between channels, another signal may be present between $f_c + \Delta$ and $f_c + 2\Delta$, and so on, and so it is desired to minimize leakage power in those bands, as in Fig. 1.8(a). The total power present within each band can be calculated, and the adjacent-channel power ratio (ACPR), or sometimes called the adjacent-channel leakage ratio (ACLR), can be defined from their ratios as:

$$ACPR = 10 \cdot \log_{10}\left(\frac{P_{adjacent}}{P_{channel}}\right) \text{(dBc)}, \tag{1.7}$$

where $P_{adjacent}$ can be for any other channel. However, a single value of ACPR is typically taken as the larger of the two directly-adjacent channels, and will be assumed throughout this thesis. This is an example of an out-of-band linearity metric.

For communications standards such as OFDM which employ constellation mapping, error-vector magnitude (EVM) can also be defined [41], illustrated in Fig. 1.8(b). A received constellation point $I_{rx} + j\,Q_{rx}$ maps to some complex value on the IQ axes and can be compared to the original transmitted point $I_{tx} + j\,Q_{tx}$, for all N points, with:

$$EVM = 100 \cdot \sqrt{\frac{\frac{1}{N}\sum_{n=1}^{N}\left(\left(I_{tx}[n] - I_{rx}[n]\right)^2 + \left(Q_{tx}[n] - Q_{rx}[n]\right)^2\right)}{\frac{1}{N}\sum_{n=1}^{N}\left(I_{tx}[n]^2 + Q_{tx}[n]^2\right)}}(\%) \tag{1.8}$$

In this case, EVM is using the transmitted signal in the denominator for normalization. Other values, such as average and peak constellation power, can also be used. This is an example of an in-band linearity metric.

BER can also be quoted, but is not often in PA applications because much of the metric depends on coding techniques not directly affected by the PA. It compares the transmitted and received bitstreams to determine the fraction of incorrect bits. Considering the PA by itself as the communications channel, an EVM of approximately 10 % might result in zero BER for an OFDM burst of 10 symbols. High values of the distortion metrics in this section may be mitigated with digital pre-distortion (DPD), detailed next.

1.1.3.2 Digital Pre-Distortion

Because it is typically desired for a PA to operate efficiently, some nonlinearities must be present, as described in the previous section. A common way to improve the linearity of an efficient amplifier is with DPD, a technique which relies on generating a mathematical model of the nonlinear properties of a PA [42]. An input signal is first passed through the inverse model, digitally, before being amplified by the PA the model was based on.

To generate a nonlinear model of a PA, the 1-D memory polynomial model can used:

$$z(t) = \sum_{m=0}^{M}\sum_{k=0}^{K} c_{mk}x(t-m)|x(t-m)|^k, \tag{1.9}$$

where $x(t)$ is the original baseband signal to transmit, c_{mk} are the correction coefficients, $z(t)$ is the

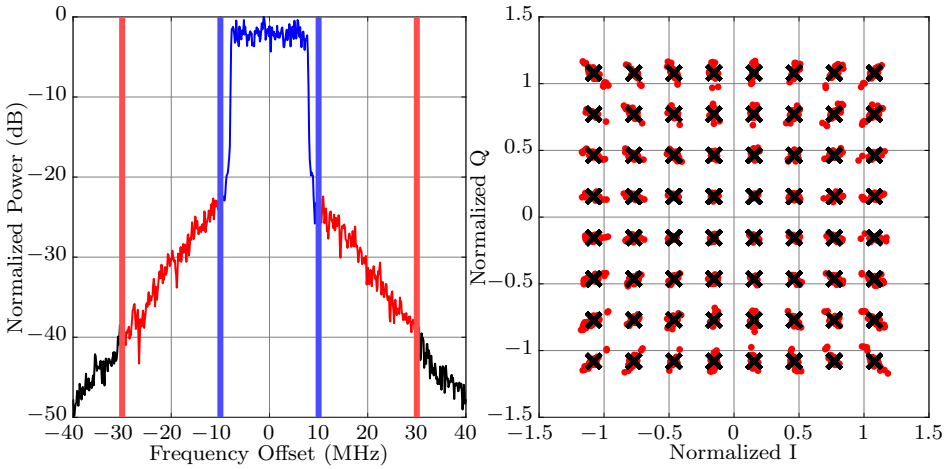


Figure 1.8: The (a) ACPR and (b) EVM of an example 20 MHz OFDM signal. The powers of the (blue) main channel and (red) adjacent channels can be used to calculate ACPR. The transmitted constellation points are shown in black crosses, with the received constellation points shown as red dots, used to calculate EVM.

pre-distorter output, M is the memory order, and K is the non-linearity order. The complex-valued time-domain OFDM signal from Section 1.1.2 would be applied as $x(t)$ to generate a desired $z(t)$ which would be up-converted and amplified.

To generate this model, some shorter OFDM test signal would first be generated and amplified by a PA. By swapping the input and output signals in (1.9), $x(t)$ being the PA output and $z(t)$ being the PA input, the c_{mk} coefficients can be found for a range of M (typically 1–3) and K (typically 5–7). The values of M and K that generate the best linearity improvement using the metrics of Section 1.1.3.1 are typically used, noting that to prevent aliasing, the instantaneous RF bandwidth of the baseband circuitry must be able to support a bandwidth of at least $(B \cdot K)$, B being the OFDM signal bandwidth. For example, a 20 MHz OFDM signal with nonlinearity order $K = 7$ used in DPD must be read by an instrument with at least 140 MHz instantaneous bandwidth.

Finally, amplitude modulation/amplitude modulation (AM/AM) and amplitude modulation/phase modulation (AM/PM) plots are also helpful in defining linearity for modulated signals. Similar to drive-up curves, these plot the normalized voltage amplitude and phase baseband points. The x-axis of both is $|x(t)|/|x|_{max}$, with a similar equation for the y-axis of the AM/AM plot, instead

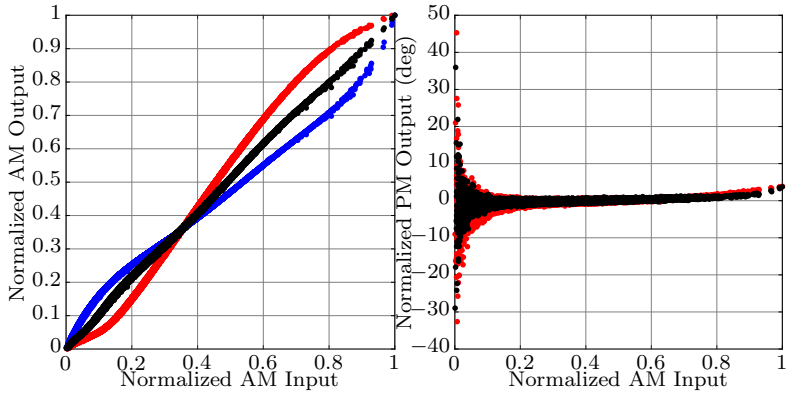


Figure 1.9: Plots of (a) AM/AM and (b) AM/PM of an example 20 MHz OFDM signal. The (red) original and (black) pre-distorted characteristics are shown, along with those of the (blue) pre-distorter itself.

using the output $y(t)$ in the calculation. The AM/PM figure plots the angle of $y(t) - x(t)$ on the y-axis. An example AM/AM plot is shown in Fig. 1.9(a), and an AM/PM plot in Fig. 1.9(b). These are especially useful when performing DPD. In Fig. 1.9(a), the signal before and after DPD is shown, along with the response of the pre-distortion. Notably, the shape of the pre-distortion is symmetric about $y = x$ as compared to the signal without DPD.

1.2 Thesis Contents

This thesis focuses on the design of various broadband RF power amplifiers, including a new architecture for broadband operation. The characterization of PAs with non-concurrent and concurrent signals leads to a better understanding of their operation for advanced phased array applications in a low-cost implementation. The content of each chapter is summarized as follows:

Chapter 2: A GaN-on-Si semiconductor technology with a goal of integrating RF GaN and digital CMOS circuitry for low-cost phased array systems is summarized. Developed by the MIT Lincoln Laboratory, the dielectric stack-up of this process is characterized with full-wave electromagnetic (EM) simulations to develop a planar process-design kit (PDK). Various passive structures, such as coplanar waveguide (CPW) transmission lines and capacitors, are modeled

and used to design various harmonically-terminated 10 GHz PAs. Small-signal and dc-IV data is used to model the transistors, which do not have a large-signal nonlinear model. As the process matured, a microstrip-based PA with nonlinear model comparisons is shown. This technology is being developed to reduce the cost of future phased arrays, and because they will likely benefit from concurrent signal amplification, its characterization is essential. However, because this technology is still under-development, commercial semiconductor technologies are used in the remainder of this thesis to fabricate broadband PAs. The next chapter addresses the fundamental challenges associated with broadband network design.

Chapter 3: Fundamental limitations of narrowband and broadband networks are considered. A narrowband relationship between the scattering parameters of any passive lossy network is derived. A well-known method of narrowband network synthesis is summarized, and a general method to perform non-conjugate double matching of two-port networks is developed and implemented two ways: (1) numerically towards an algorithm used to design the dual-band microwave monolithic integrated circuit (MMIC) PA of Chapter 4; and (2) analytically to design a PA matching network in Chapter 5.

Chapter 4: Two dual-band RF PAs, one GaN-SiC hybrid at 2.1 and 3.7 GHz and the other GaAs MMIC at 9 and 16 GHz, are described. The different design process of each is summarized, along with including a comparison between simulated and measured CW performance. Concurrent modulated signals are used to further characterize the hybrid and demonstrate its performance in the concurrent mode of operation. Concurrent CW signals are used to characterize the cross-band gain and performance limitations of the MMIC, which the architecture of the following chapter addresses.

Chapter 5: Several different broadband PA architectures are considered. A previous one-stage S-band PA from another work is summarized, along with the design procedure of a simulated two-stage C-band PA using the results of Chapter 3. An architecture for improving the linearity, while maintaining high-efficiency, of a broadband PA is also presented and analyzed. Two implementations, in hybrid 1.8–4 GHz GaN-SiC and MMIC 8–18 GHz GaN-SiC technologies, are

presented. The first is characterized with non- concurrent and concurrent signals, with the second briefly considered in the following chapter.

Chapter 6: A summary of this thesis is presented, along with a path towards further development of these efforts as future work. Additionally, for broadband T/R modules, broadband LOs are also required. The appendix describes circuits for this purpose.

Chapter 2

Low-Cost Phased Array Technology

2.1 GaN-on-Si for Low-Cost Phased Arrays

As mentioned in the previous chapter, of the total cost of a military phased array radar, approximately half comes from the phased array itself, with half of the phased array cost coming from the T/R module [5]. A portion also comes from the RF boards and cabling due to the amount required for a full system. The multi-function phased array (MPAR) program [5, 6] seeks to reduce these costs by building the phased array in a tile configuration, reducing the cost per area of the phased array by more than five times compared to the more traditional brick (or slat) configuration. The T/R module, often implemented with GaAs in the past, with higher powers requiring GaN-on-SiC technology, still comprises a significant portion of the cost.

Because GaN is established as a high-voltage semiconductor with broad applications, including those at microwave and millimeter-wave frequencies, it is used at the front-end of systems like MPAR due to its high-power density allowing for relatively small MMIC areas as compared to other technologies [43]. At frequencies above UHF, MMIC passive and active circuit components with a GaN active layer are typically fabricated on a SiC substrate. However, SiC is expensive, is not easily integrated with CMOS, and wafers tend to be 100 mm in diameter. To overcome this, GaN MMICs on Si substrates are being developed to improve device performance [44–46], integrate with CMOS [47], and be fabricated on larger substrates (*e.g.* 200 mm diameter) to improve yield [17]. In addition, growing GaN directly on low-cost Si wafers with Au-free processes [17, 18] leverages the high-volume capabilities of existing CMOS foundries, increasing yield and reducing cost.

This chapter explores the GaN-on-Si process under development at the MIT Lincoln Laboratory as a technology to fabricate T/R modules for future wafer-scale integration with CMOS electronics such as the DREX. Such integration has already been demonstrated, *e.g.* [17, 47]. The process is described first, then passive and active components designed with it are presented. Due to various manufacturing difficulties, measurement results are not available for the passive components at the time of writing this thesis.

2.1.1 GaN-on-Si Process Characterization

A stack-up of the MIT Lincoln Laboratory GaN-on-Si technology process is shown in Fig. 2.1, where a GaN active layer is epitaxially grown on a high-resistivity Si substrate with three metal layers and no through-vias. AlGaN is used as a barrier layer (not shown). The fabrication process includes passives (*e.g.* capacitors, resistors, transmission lines) and HEMTs of varying gate lengths (from 120 to 200 nm), periphery, gate-source spacing, and gate-drain spacing. Metal structures are written using lithography. Due to the complex stack-up with high aspect ratios and non-planar layers, numerical analysis required for accurate circuit design presents a number of challenges. The thicknesses of the eight layers range from 90 nm to 1.065 mm, while the guided wavelength at X-band is on the order of 15 mm. Appropriate port excitation and model de-embedding also needs to be considered. Here, several CPW circuit components are designed and simulated using both finite-element method (FEM) based Ansys HFSS and method-of-moments (MoM) based Sonnet Software. The goal is to establish which method agrees better with measurements and is therefore better suited for designs.

To show the usefulness of the process, a portion of the T/R module (*e.g.* PA) is designed. This circuit requires passive components such as capacitors (dc block), resistors (stabilization), and transmission lines for the matching and biasing circuits. Since the initial process did not allow back-side processing, CPW transmission lines were a natural choice. Later improvements of the process allowed for through-vias, enabling a microstrip-based design detailed in Section 2.3.2. CPW transmission lines can be evaluated using the conformal mapping method described in [48], which

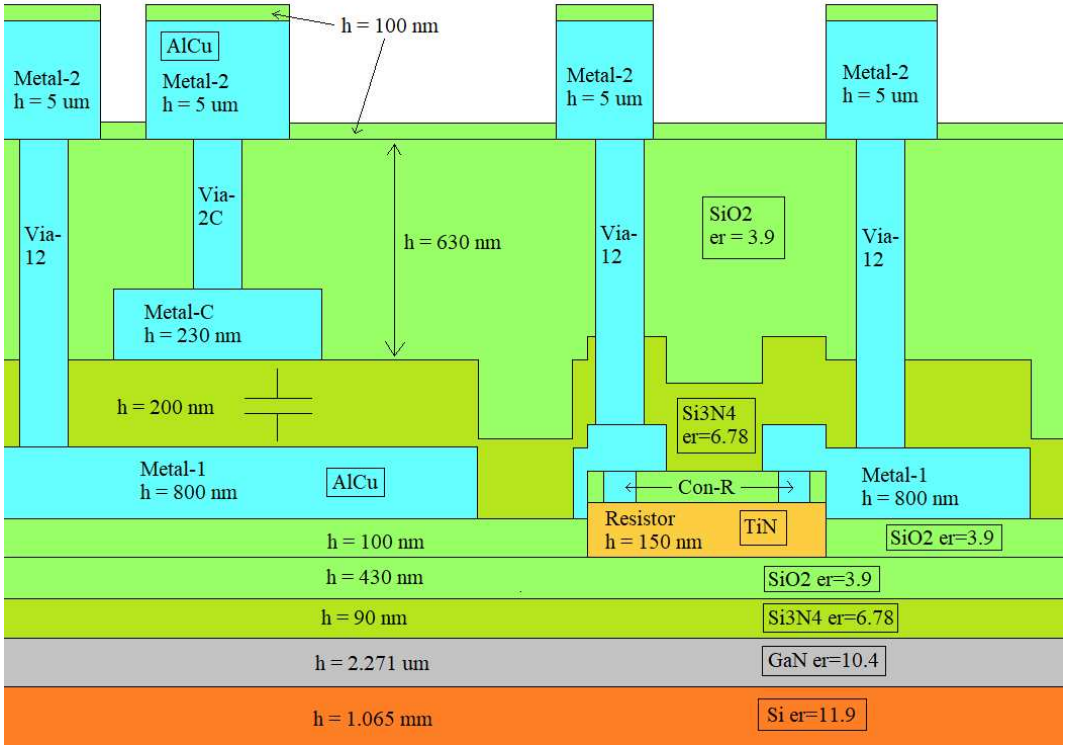


Figure 2.1: GaN-on-Si process stack-up (not to scale). CPW lines are made in the Metal-2 layer. Underpasses are made using the Metal-1 layer. Capacitors are made using Metal-C and Metal-1 layers. The various dielectrics and their permittivities are shown in green, metals in blue, GaN in purple, and the Si substrate in orange. HEMT metal layers are omitted since this work focuses on passive circuit components.

results in the characteristic impedance given by:

$$Z_{0cp} = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K'(k_1)}{K(k_1)}, \tag{2.1}$$

where K is the complete elliptic integral of the first kind (K' is its complement), k_1 is its argument, and ϵ_{re} is the effective dielectric constant. The constant ϵ_{re} can be determined as the weighted sum of each dielectric layer's filling factor and relative permittivity. This approach is used as a starting point in design, *e.g.*, for a gap width of 34 μm and conductor line width of 40 μm, $Z_{0cp} = 50\,\Omega$. However, when simulated using HFSS, a gap width of 25 μm produces a 50 Ω line due to the influence of the conductor thickness, pointing to the need for detailed electromagnetic simulations.

Referring to Fig. 2.1, along with the Metal-2 layer used for the CPW lines, the Metal-1 layer

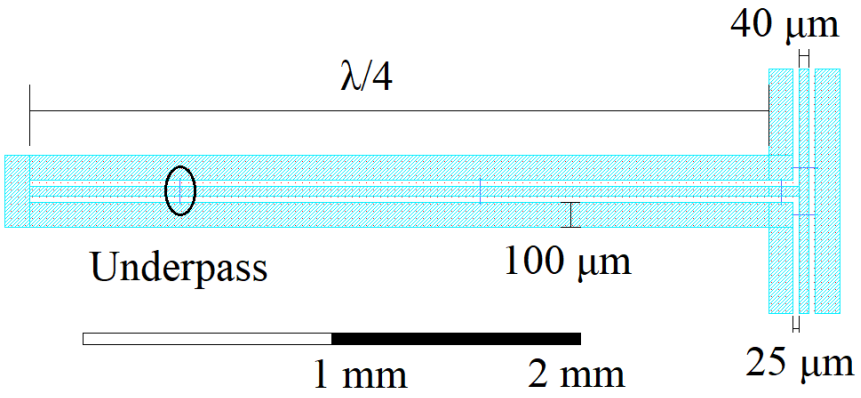


Figure 2.2: ADS layout of a 50 Ω CPW line with $\lambda/4$ shunt shorted stub and $\lambda/10$ spaced underpasses (at 10 GHz), currently in fabrication. Labeled line width, gap width, and ground width are the same everywhere in this layout.

is used to create underpasses to connect the CPW reference planes and for capacitor electrodes in conjunction with the Metal-C layer. An example ADS layout of a portion of a 50 Ω line with a $\lambda/4$ shunt shorted stub is shown in Fig. 2.2. Because of the fringing fields associated with the inductive nature of the short, this line is modeled in ADS as having a length extension of 10 μm [48].

2.1.2 Simulation Simplifications

Two dominant numerical methods for electromagnetic (EM) analysis are FEM and MoM. Here, commercial implementations of these by Ansys (HFSS) and Sonnet Software (Sonnet) are used and compared. For a full stack-up model, Sonnet requires memory on the order of 30 GB for more complex circuit geometries such as capacitors and meandered lines, whereas HFSS requires 13 GB. This is because the MoM method needs metal meshing everywhere, memory requirements scale as the square of the number of meshed elements [49]. Complex geometries often require many elements to accurately capture EM interactions. However, because Sonnet only meshes metal, it is unaffected by the aspect ratio of the dielectric layers, unlike HFSS. Any FEM method subdivides the entire volume into smaller volumes, such as tetrahedrons, to solve the defining partial differential equations subject to boundary conditions. Mesh compensation can be performing at each dielectric layer to partially reduce computing requirements.

For excitation and de-embedding lumped ports are used in HFSS so that the radiation boundary can be properly set up a distance $\lambda/10$ away at the design frequency. In Sonnet, push-pull ports are utilized to connect to the PEC sidewalls. The shorted stub of Fig. 2.2, *e.g.*, requires 8.35 hours to solve in Sonnet and 2.82 in HFSS with a full stack-up using a computer with 16 GB of RAM and an Intel i7 3.4 GHz processor.

To reduce simulation times, the stack-up of Fig. 2.1 is simplified by combining the two dielectric layers between Metal-2 and Metal-1 into a single homogeneous effective dielectric with a relative permittivity of 4.55 (1 % below weighted average). Similarly with the layers at Metal-1 and below, but not including Si, a second effective dielectric layer with relative permittivity 6.1 is included in the simulations (29 % below weighted average). The Si thickness was reduced from 1.065 mm to 600 μm. The equivalent dielectric simulations are shown to be within 0.1 dB in terms of loss compared to the full stack-up simulations up to 30 GHz. However, the simulation time is reduced by about 95 % for complicated geometries, justifying this simplification.

2.2 GaN-on-Si Passive Components

Several passive components are investigated, then combined together to create various matching networks for PA designs, as described in the following sections.

2.2.1 Straight Transmission Line Sections

For transmission line design, loss and characteristic impedance are evaluated for 30, 50, and 75 Ω $\lambda/4$ long lines at 10 GHz. Underpasses are added at varying intervals with necessary adjustments to produce different characteristic impedance transmission lines, summarized in Table 2.2.1, where the effective relative permittivity ϵ_{re} is adjusted to maintain $\lambda/4$ length. For the 50 Ω line with $\lambda/10$ underpass spacing, plots of loss and $|S_{11}|$ for $Z_L = 15\,\Omega$ are included in Fig. 2.3, 15 Ω chosen to highlight simulation differences.

Sonnet gives a resonant spike around 28 GHz due to the PEC boundaries imposed by the simulation method. The disagreement between the two simulations is about 0.5 dB in $|S_{11}|$, 0.2 dB/mm

Table 2.1: Varying Impedance Transmission Line Dimensions

ϵ_{re} HFSS	ϵ_{re} Sonnet	Underpass Spacing	Z_0	HFSS Line Width	HFSS Gap Width
4.96	5.06	none	50 Ω	40 μm	23 μm
5.61	5.38	$\sim \lambda/20$	50 Ω	40 μm	28 μm
5.20	5.18	$\sim \lambda/10$	50 Ω	40 μm	25 μm
5.11	5.01	$\sim \lambda/4$	50 Ω	40 μm	24 μm
4.83	5.05	$\sim \lambda/10$	30 Ω	74 μm	8 μm
4.83	4.95	$\sim \lambda/10$	75 Ω	16 μm	37 μm

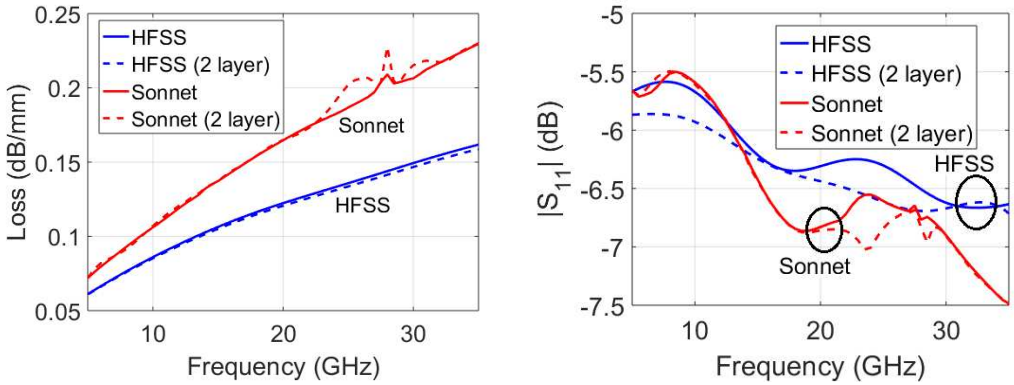
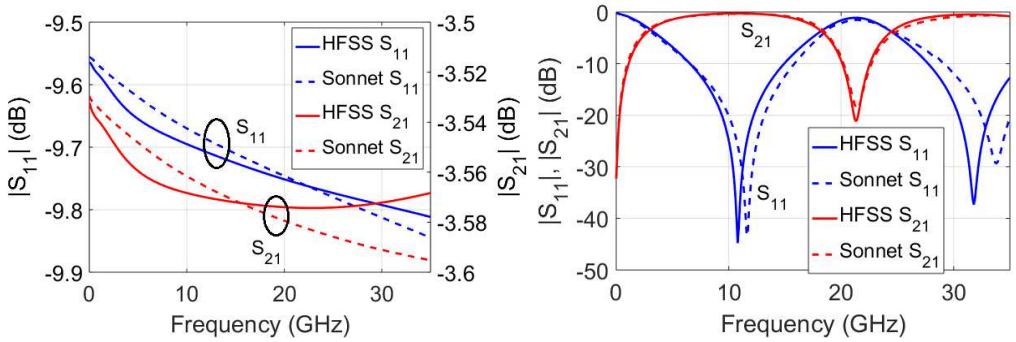


Figure 2.3: Simulated (a) loss (dB/mm) and (b) $|S_{11}|$ comparison between HFSS (gap = 25 μm) and Sonnet (gap = 21 μm) of a 50 Ω line with $\lambda/10$ underpass spacing at 10 GHz. Load terminations are (a) 50 Ω load and (b) 15 Ω load.

in loss, with a nearly identical phase response (not plotted). It is found that each underpass adds about one effective degree of electrical line length. The ground plane width is also varied from 50 μm to 150 μm, with 100 μm chosen as the smallest distance that preserves the CPW mode.

2.2.2 CPW Junctions and Stubs

In addition to straight sections of lines, shorted stubs, open stubs, and tee junctions are needed in circuit design. The 50 Ω tee junction from Fig. 2.2 is simulated, separately from the entire circuit, in HFSS and Sonnet, reference planes 145 μm from the tee-junction center. Results



(a) (b)

Figure 2.4: Comparison of S-parameters of: (a) 50 Ω tee junction and (b) 50 Ω quarter-wave shorted stub at 10 GHz, obtained by FEM (HFSS) and MoM (Sonnet) simulations.

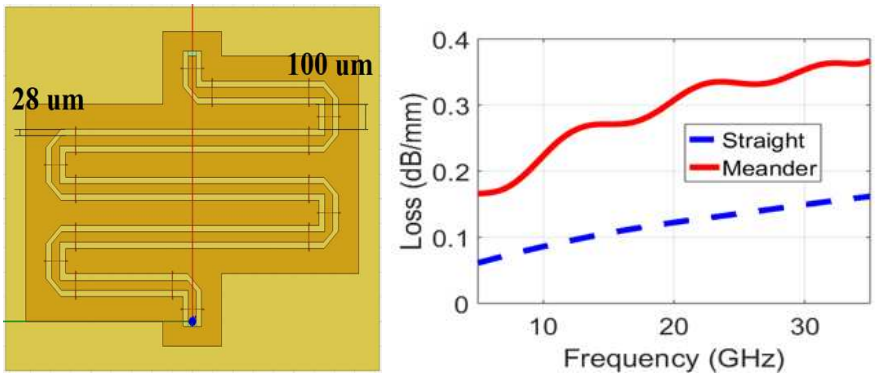
are shown in Fig. 2.4(a). The entire 50 Ω $\lambda/4$ CPW shunt shorted stub of Fig. 2.2 is simulated in HFSS and Sonnet, with results shown in Fig. 2.4(b). S-parameters demonstrate relatively good agreement between HFSS and Sonnet.

2.2.3 Meandered CPW Lines

Footprint miniaturization was studied on a four-turn half-wavelength meandered line with 100 μm ground plane width between lines requiring a 28 μm gap width to maintain 50 Ω characteristic impedance. An ADS layout of this structure is shown in Fig. 2.5(a), along with a loss comparison to an un-meandered line in Fig. 2.5(b). It is about 20 % shorter than the straight line due to EM coupling, and has about 0.2 dB/mm increased loss. As width between meandered line segments increases, the total meandered line length approaches $\lambda/2$ at 10 GHz, as expected. The odd CPW mode is confirmed to not be present by observing the fields.

2.2.4 Lumped Capacitors

Between the Metal-C and Metal-1 layers, using the stack-up of Fig. 2.1, parallel-plate capacitors with expected 0.3 fF/μm^2 can be designed. An HFSS simulated 60 μm x 80 μm dc blocking capacitor, *e.g.*, has a capacitance of 1.55 pF at dc (1.44 pF calculated) and 1.46 pF at 10 GHz. Sonnet simulations result in a dc capacitance of 1.58 pF for the same capacitor. HFSS models of series and shunt capacitors are shown in Figs. 2.6(a) and 2.6(a), respectively.



(a) (b)

Figure 2.5: (a) HFSS layout of a $\lambda/2$ 50 Ω CPW meandered line at 10 GHz; and (b) loss comparisons between this line and a straight line.

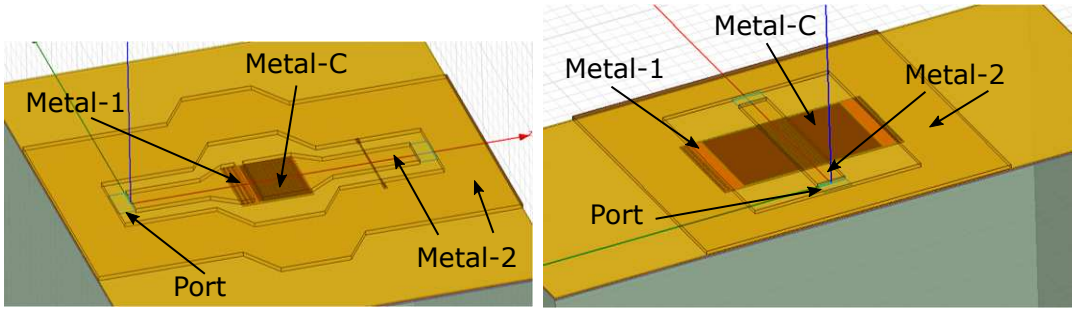


Figure 2.6: HFSS (a) series and (b) shunt 50 Ω capacitor models.

2.2.5 Bias-Tees

Using the junction, meandered line, and capacitor elements designed in the preceding sections, bias-tees are modeled in HFSS. Designed for X-band, the gate bias-tee, Fig. 2.7(a), provides a good match at 10 GHz for the RF and RF/dc ports while being highly reflective at the dc port, as shown in Fig. 2.7(b). Fig. 2.7(c) demonstrates a minimal RF loss of less than 1 dB. Similarly for the drain bias-tee, Fig. 2.7(d), the response is centered around 20 GHz to allow for impedance matching of the fundamental, second, and third harmonic frequencies, as Figs. 2.7(e) and 2.7(f) illustrate. Varying the port 3 impedance for both circuits results in a 10 GHz S-parameter change of less than 0.5 dB.

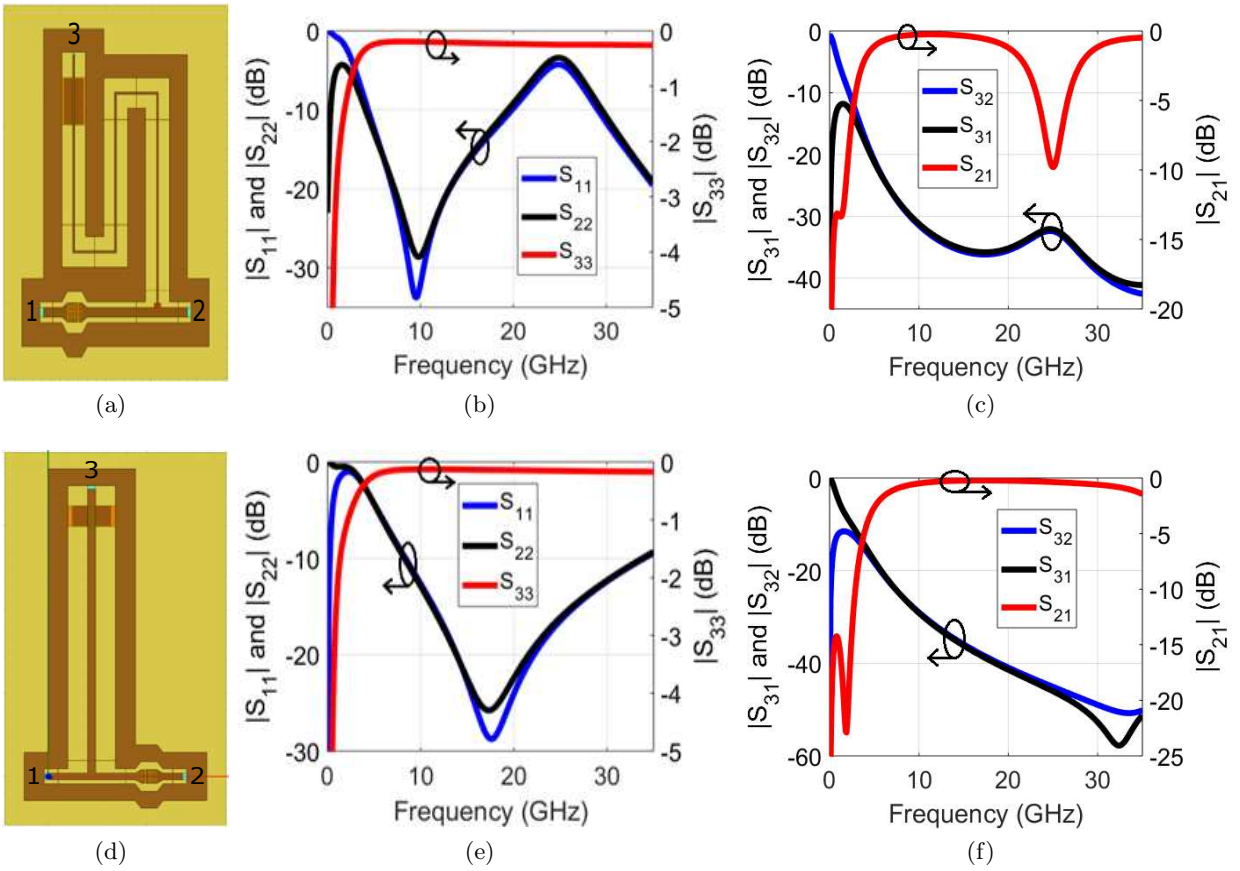


Figure 2.7: Bias-tee layouts. The (a) gate bias-tee, (b) reflection response, and (c) transmission response are centered at 10 GHz. The (d) drain bias-tee, (e) reflection response, and (f) transmission response are centered near 20 GHz to allow for harmonic impedance tuning.

2.3 GaN-on-Si Active Components

With the components of the previous sections, the GaN-on-Si matching network building blocks are characterized. For a PA, the transistor should also be modeled; however, in this work a nonlinear model was not initially available. Typically these are used to design the large-signal behavior of a PA, and are created from a combination of s-parameter, pulsed dc-IV, and load-pull measurements. Therefore, the next sections describe using static s-parameter and dc-IV data to characterize transistors in the GaN-on-Si process. This information is used to design a variety of PAs, with the final Section 2.3.2 comparing measured results to a newly available nonlinear model.

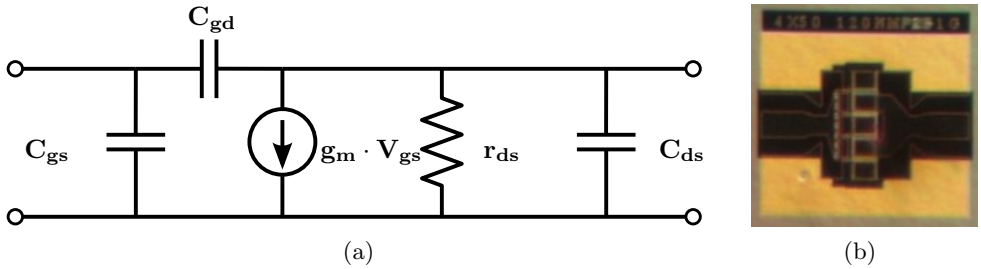
2.3.1 Transistor Modeling

The simplest high-frequency intrinsic circuit of a common-source FET is given in Fig. 2.8(a) [2]. Various GaN-on-Si HEMTs, an example photograph of one given in Fig. 2.8(b), can be measured at various bias conditions, extracting s-parameter values for each state to create models from [50]. For a particular transistor size, gate bias voltage, and drain bias voltage, the circuit parameters of Fig. 2.8(a) can be extracted. These can be used, along with an R_{opt} value from measured dc-IV data, to determine an appropriate fundamental impedance to present at the drain terminal of the transistor. Harmonics can be made reflective to increase efficiency [51], and a conjugate-match can be presented at the gate terminal for maximal power transfer.

With this method, several PAs are simulated, each having a different harmonic impedance, to perform discrete harmonic load-pull characterizations of the transistors. An ADS layout of one is shown in Fig. 2.9. Unfortunately, due to manufacturing difficulties, the components up to this point have not been fabricated. The next section describes an X-band microstrip PA designed in an updated technology with backside processing.

2.3.2 X-Band Power Amplifier

Various PAs with GaN-on-Si technology have been demonstrated in literature. For example, hybrid designs at 880 MHz [52] and 5.6–5.9 GHz [53] report 4 W or more of output power with greater than 40 % drain efficiency using a MACOM process. MMICs have been demonstrated with



(a) (b)

Figure 2.8: (a) Simple high-frequency intrinsic equivalent circuit of a HEMT. (b) Photo of 4×50 μm transistor fabricated in the GaN-on-Si process.

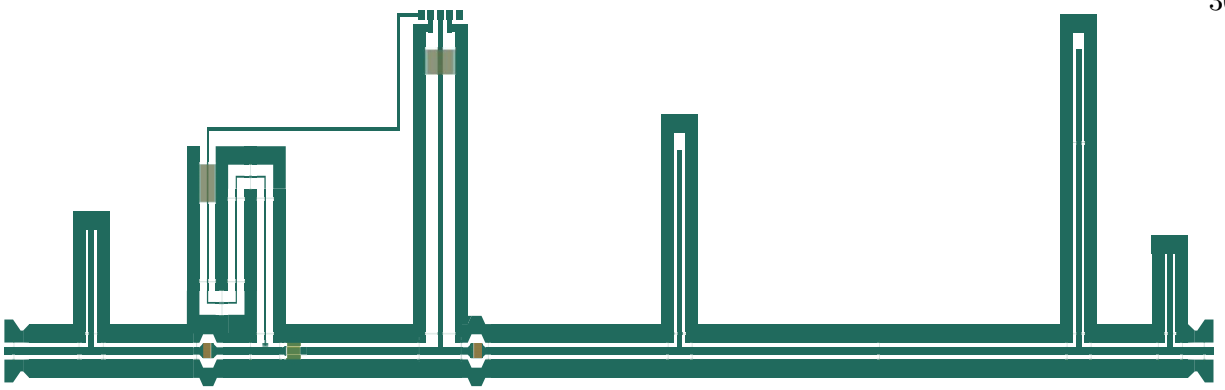


Figure 2.9: Layout of an example CPW X-band GaN-on-Si PA measuring 9.7 mm×2.1 mm.

the same process [45] at 2.5 GHz achieving 50 W of output power, 17 dB of gain, and 64 % drain efficiency. The Ubidyne process is used for a digitally-driven MMIC PA with 1.8 W of output power with a digital 2.25 Gb/s drive signal [54]. The Ommic process is also used to design a MMIC PA in the 27–34 GHz range with 30 % PAE and 5.6 W of output power [44]. This section focuses on the design of a proof-of-concept X-band PA with the MIT Lincoln Laboratory GaN-on-Si process.

2.3.2.1 Simulation and Design Considerations

Cadence AWR Microwave Office software is used for the PA design. Because its Axiem EM solver is based on MoM, the full dielectric stack-up is used and converted to a multi-layer planar PDK in AWR. A $\lambda/4$ transmission line at 10 GHz with the same physical dimensions as an HFSS model is simulated, and the PDK is modified until the response is similar. Because it is the thickest layer, Si had the largest effect; its relative permittivity was increased from 11.9 to 13.5. Other values remained unchanged. For non-EM simulations, a single-layer microstrip substrate that corresponds to this model at 10 GHz is generated. Final values different from the physical stack-up include a relative permittivity of 11.82, dielectric height of 115.136 μm, and loss tangent of 0.00702.

For this design, a 2×100 μm transistor is chosen for gain and desired output power at 10 GHz. In general, larger transistors have less gain at a given frequency. This transistor has two gate fingers, each of which are 100 μm wide. The periphery (in this case $2\times100 = 200\,\mu$m) is a useful figure to

keep in mind for power considerations: experimental results suggested transistors in this GaN-on-Si process had a power density of about 1–3 W/mm. For 30 dBm desired output power, this would require 1.6 mm of periphery, as a conservative estimate, with eight-way power combining and assuming 2 dB combiner loss.

The measured s-parameters for this transistor at $V_{DD} = 20\,V$ are used to generate an updated circuit representation of Fig. 2.8 in Fig. 2.10. Connected to an input-matching network (IMN) and output-matching network (OMN), the small-signal s-parameters of the resulting PA are easily calculated. For large-signal power calculations, additional data is required. Because measured dc-IV data was only available for the $2 \times 20\,\mu$m device, drain currents were scaled by a factor of five to approximate the $2 \times 100\,\mu$m device. This data is plotted in Fig. 2.11 alongside the fitted load-line representing a class-A bias; data past 20 V was not available. The inverse of the slope of the load-line represents the R_{opt} load of the transistor for maximum output power as [55]:

$$R_{opt} = \frac{V_{dc} - V_{knee}}{I_{max}/2} = \frac{V_{dc} - V_{knee}}{I_{dc}} = \frac{20 - 3.5}{0.021} = 785.7\,\Omega. \tag{2.2}$$

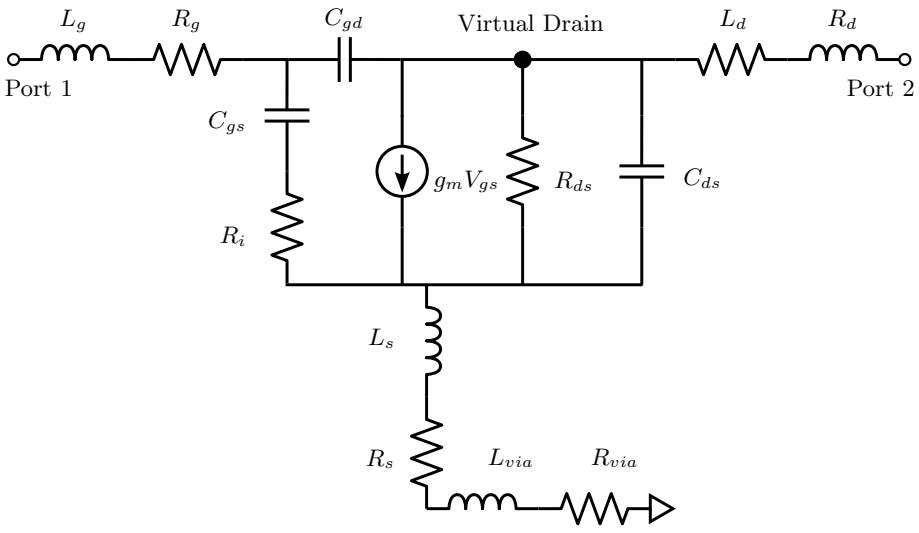


Figure 2.10: High-frequency circuit model of the GaN-on-Si $2 \times 100\,\mu$m transistor at $V_{DD} = 20\,V$. Values include: $L_g = 0.02\,$nH, $R_g = 1.5\,\Omega$, $L_d = 0.03\,$nH, $R_d = 0.05\,\Omega$, $C_{gs} = 0.15\,$pF, $R_i = 0.37\,\Omega$, $R_i = 0.37\,\Omega$, $g_m = 0.044\,S$, $R_{ds} = 796.8\,\Omega$, $C_{ds} = 0.03\,$pF, $L_s = 0.01\,$nH, $R_s = 1.7\,\Omega$, and $C_{gd} = 0.03\,$pF.

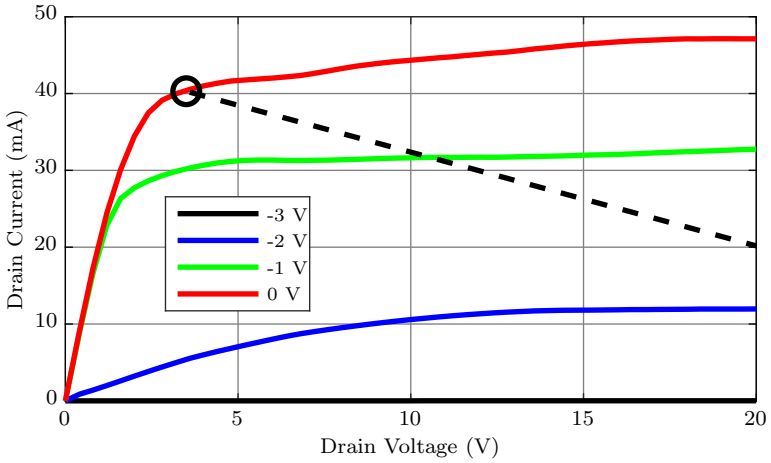


Figure 2.11: Measured dc-IV data for the $2\times100\,\mu$m transistor, scaled from the $2\times20\,\mu$m transistor, for different values of V_g. Plotted also is the fitted load-line used to calculate R_{opt}.

This is the value that is presented to the virtual drain, *i.e.* the node of the current source in Fig. 2.10, for maximum output power. However, the various parasitics in the model require that the output matching network present some other impedance at the accessible port-2 location, while also having minimal loss. This port-2 impedance can be related to R_{opt} through the circuit components of Fig. 2.10 and used to determine the output power the transistor generates [55]. To determine the power delivered to the load, the operating power gain G_P of the OMN can be used [56], and for a $50\,\Omega$ load, this becomes:

$$G_P = \frac{|S_{21}|^2}{1-|S_{11}|^2}. \tag{2.3}$$

However, this equation must be updated for eight-way power combining when excited in the even-mode [57]:

$$S_{21} = \frac{8}{\sqrt{8}} S'_{91}, \tag{2.4}$$

$$S_{11} = S'_{11} + S'_{21} + S'_{31} + S'_{4,} + S'_{51} + S'_{61} + S'_{71} + S'_{81}, \tag{2.5}$$

where ports $1'$–$8'$ are the combining ports and port $9'$ is the common output port of the OMN. A similar procedure can be performed on the IMN and transistors to determine the large-signal gain.

With tools in place to simulate the small and large-signal performance of a GaN-on-Si PA, matching network topologies are considered next. It is found that a port-2 impedance of $240.3 + j356.7\,\Omega$ results in maximum power amplification. Various narrowband topologies are considered, and it is found that to simultaneously provide a good match with low loss, the reactance should be resonated out with an inductor. At 10 GHz, this corresponds to an inductance of 5.68 nH, which can be achieved by an 75.8° 90 Ω line. However, due to space constraints, this line must be meandered. The total meandered length is increased to 6.3 mm to implement a 1.18 nH inductance at each transistor drain, shown in Fig. 2.12, as a trade-off between match, insertion loss, and size. Inductors might be a reasonable alternative if a low-enough Q factor and high-enough self-resonant frequency can be obtained.

Transmission line segments are used to perform the power combining with approximately real impedances. A shunt tuning and a dc blocking capacitor is used near the output port to complete the match. The bias lines are similarly meandered with high-impedance lines meeting current handling guidelines, and contain shunt capacitors (with series resistors) for stability purposes. A nearly equivalent procedure is repeated for the IMN. In this case, a series resistor is added in the bias line, along with parallel symmetric RC circuits at each gate, for stability. The gates are also connected together with resistors for odd-mode stability [58]. The final circuit layout is in Fig. 2.13.

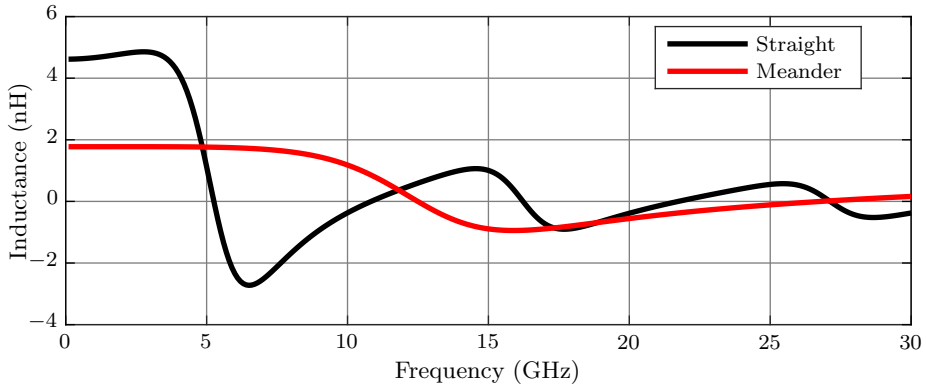


Figure 2.12: Inductance of the line at the drain of each transistor when (black) straight and (red) meandered. The first zero cross-over point occurs at 5.258 GHz for the straight line and 12.49 GHz for the meandered line. The inductance of the meandered line at 10 GHz is 1.18 nH.

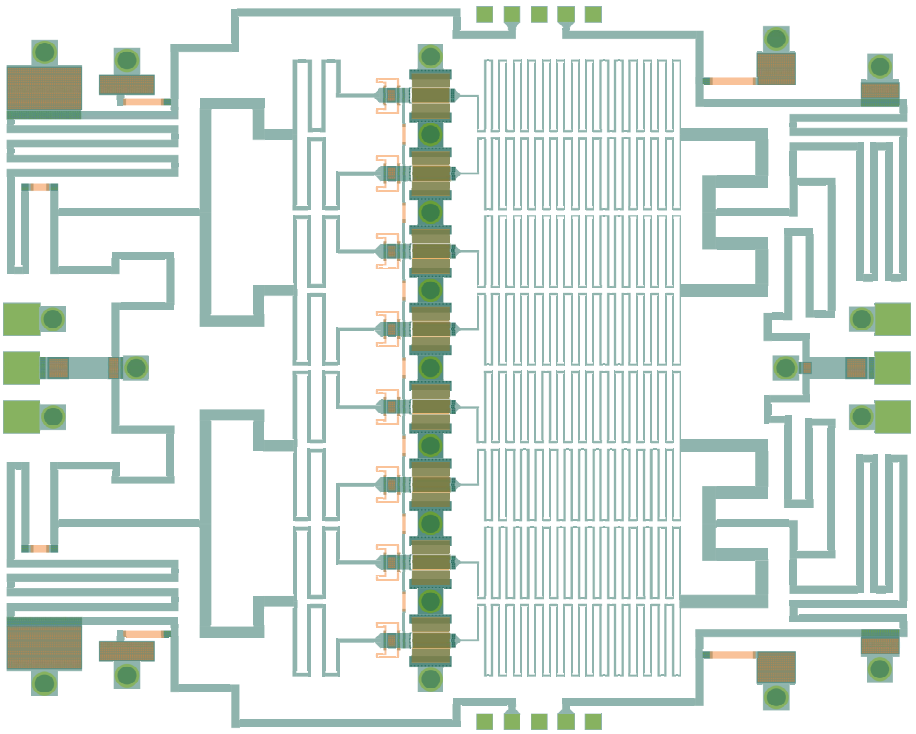


Figure 2.13: Layout of the final GaN-on-Si X-band PA measuring 2.5×2 mm^2.

Stability is confirmed by simulating the stability-factor (K), Nyquist stability criterion, and loop-gain analysis over process variations, shown in Fig. 2.14. Conditions for stability include $K > 1$, $B1 = 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 > 0$, Nyquist not encircling the -1 point, and loop-gain not encircling the +1 point. Process variation considerations consist of increasing g_m by 30 %, decreasing C_{gs} by 30 %, and increasing C_{gd} by 30 % to account for a worst-case scenario [58].

2.3.2.2 Measured and Simulated Results

The small-signal input/output reflection response of the PA is shown in Fig. 2.15. The large-signal drive-up curves at 10 GHz are shown in Fig. 2.16(a) with simulations from a nonlinear model that was not available during the design process. The saturated response over frequency is shown in Fig. 2.16(b). The highest measured saturated output power at $V_{dd} = 20\,V$ was 23 dBm, corresponding to 3 dB of gain and 3 % PAE at 10 GHz. Despite the fact that output power was about 7 dB less than desired, small-signal agreement with the simulated nonlinear model, and large-signal

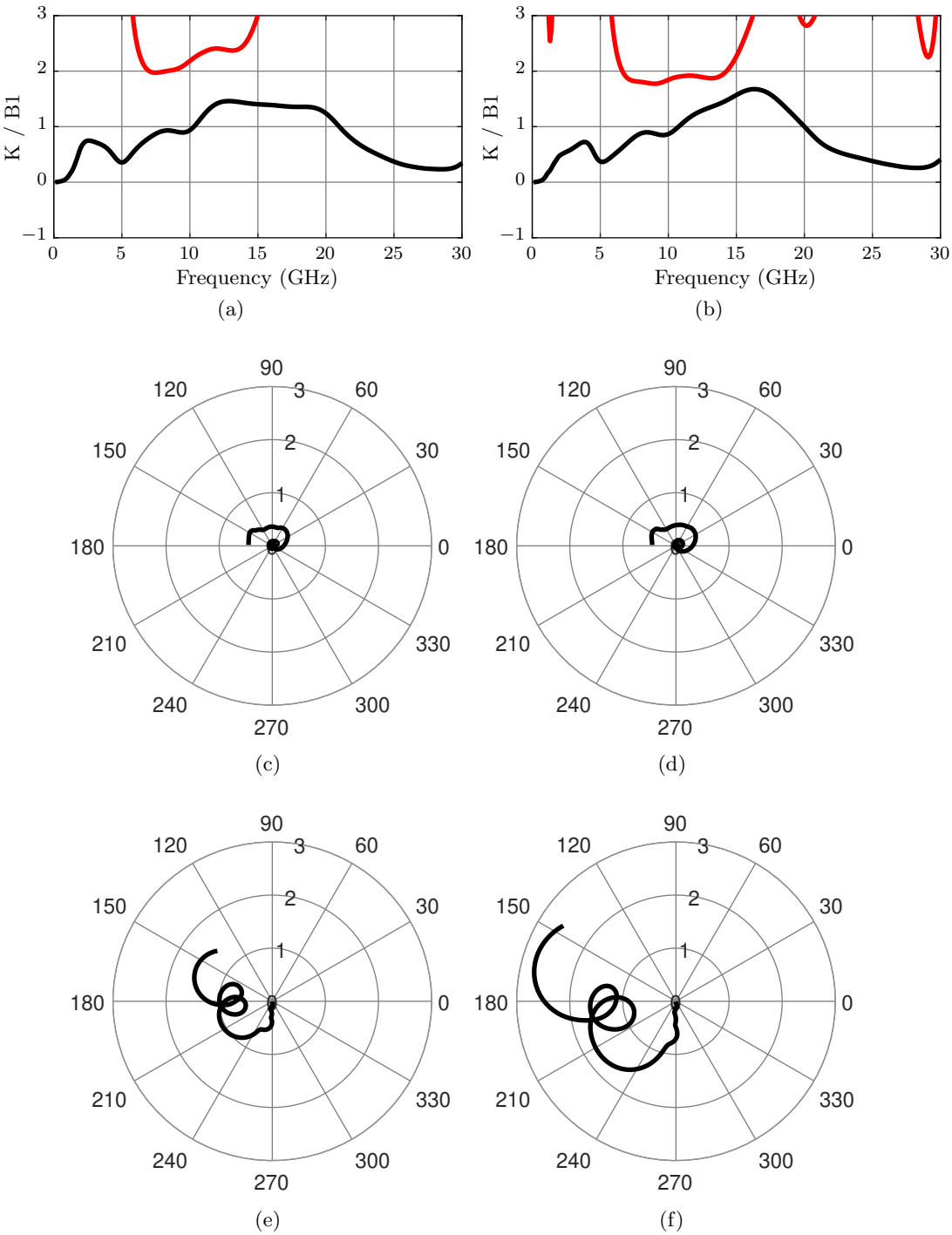


Figure 2.14: Simulated stability considerations include (left column) nominal process and (right column) 30 % process variations. The (top row) stability-factor (K) is plotted in red, along with its supplementary value B1 in black. The (middle row) Nyquist stability criterion and (bottom row) loop-gain plots are also shown, all indicating stable performance.

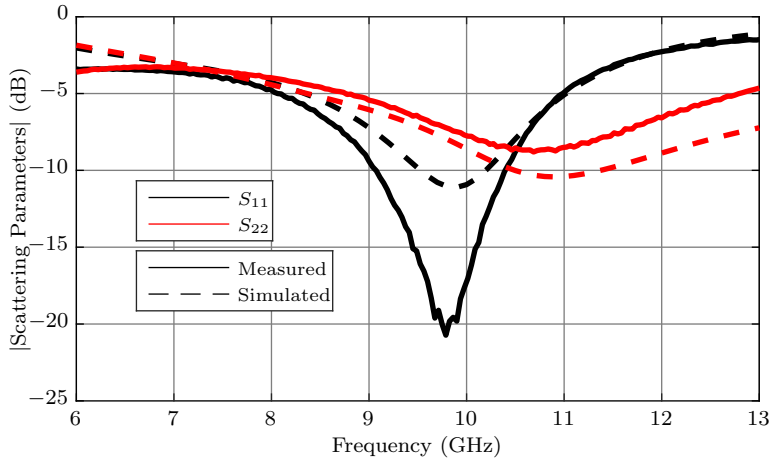


Figure 2.15: The (solid) measured and (dashed) simulated small-signal input/output reflection response of the GaN-on-Si X-band PA.

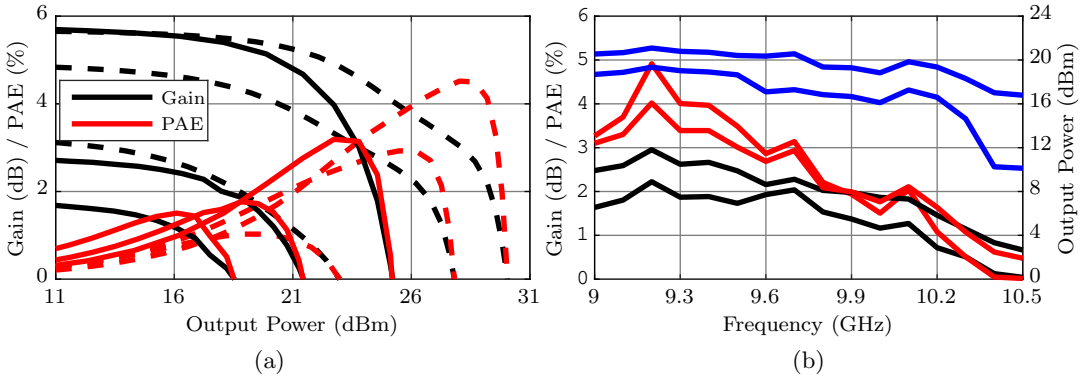


Figure 2.16: (a) Simulated (dashed) and measured (solid) drive-up curves at 10 GHz for $V_{dd} = 5$, 10, and 20 V. (b) Saturated performance over frequency of the GaN-on-Si PA: output power (blue), PAE (red), and gain (black) for $V_{dd} = 5$ and 10 V.

trends, indicate that the simplifications taken in developing the PDK were appropriate. Additionally, nonlinear models are not normally fitted for best fit at larger $|\Gamma|$ values, so some disagreement is expected.

For future designs, load-pull simulations with the nonlinear model are performed. The highest achievable performance occurs at a load-pull impedance of $79 + j140\,\Omega$ and a source-pull impedance of $29.1 + j60\,\Omega$. Drive-up curves at 10 GHz for a single $2 \times 100\,\mu m$ transistor are shown in Fig. 2.17. At saturation, 25.9 dBm, corresponding to 40.5 % of PAE and 8.9 dB of gain, is achieved. With

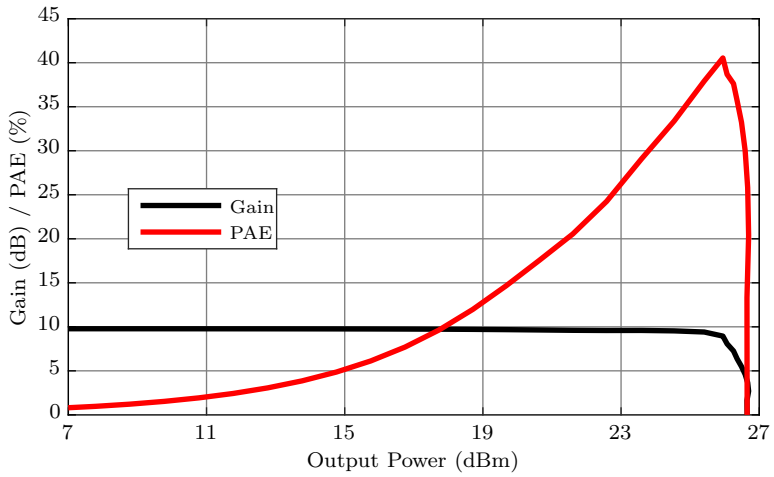


Figure 2.17: Simulated drive-up curves with ideal load-pull ($79 + j140\,\Omega$) and source-pull ($29.1 + j60\,\Omega$) terminations, chosen for highest PAE.

eight-way power combining, this corresponds to 34.9 dBm, demonstrating that $> 1\,W$ output power is possible even with significant combining loss. Future work involves designing this PA.

2.4 Conclusion

A GaN-on-Si technology under development at the MIT Lincoln Laboratory is presented in this chapter. The dielectric stackup is simulated and simplified with both FEM (HFSS) and MoM (Sonnet) computational numerical tools. Various passive components were simulated and combined to create matching and biasing networks. Transistors were analyzed using only s-parameter and dc-IV data, with a PA design shown incorporating these passive component matching networks. Measured data indicated simplifications were appropriate and indicated future designs are likely to perform better. Original contributions in this chapter include the following:

- Design, characterization, and validation of a GaN-on-Si process lacking back-side processing with HFSS and Sonnet simulations [18].
- Design of the first X-band PA with the GaN-on-Si process with back-side processing, using the process characterization and without a nonlinear model.
- Measurement and post-fabrication simulation comparisons of the X-band PA.

Despite promising results, and due to the present-day limitations of this GaN-on-Si process and its limited availability, the remainder of the work in this thesis will focus around commercially available GaN-on-SiC and GaAs technology. Additionally, the proof-of-concept narrowband X-band PA design is extended to broadband network design, considered in later chapters. As a starting point for these designs, fundamental matching limitations are the focus of the next chapter.

Chapter 3

Impedance Matching Techniques

This chapter considers the fundamental properties of matching networks to apply towards PA design. The work of the previous chapter considered a narrowband single-stage PA to demonstrate the functionality of the GaN-on-Si process. However, this PA had limited gain, and with advanced phased arrays requiring more gain over a broad bandwidth, broadband multi-stage PAs are necessary. Though these PAs contain one or more inter-stage matching networks (ISMNs), in addition to the IMN and OMN, the analysis and design of the ISMN is often not detailed in literature.

Some design methods, such as the simplified real-frequency technique (RFT), analytically optimize and flatten the response of lossless matching networks over a broad frequency range [59], including double-matching for ISMN design [60]. However, this approach assumes a lossless conjugate matching network, whereas PAs require a non-conjugate match at the output device terminal. The RFT method is extended to lossy junction matching networks in [61, 62], but conditions for the phase of the matching network scattering parameters are not considered. In addition, traditional two-port matching networks are assumed to be lossless and designed to provide a conjugate match [56, 63]. However, the PA transistor in general delivers maximum power into a non-conjugately matched load [64]. The next section considers a general narrowband multi-stage PA two-port matching network, applicable to the IMN, ISMN, or OMN, and applies it towards broadband network design.

3.1 Non-Conjugate Double-Matching

This section considers an arbitrary passive two-port network connected to two arbitrary complex loads at the two ports. In the most general case, the desired reflection coefficients at each port are considered as arbitrary. A solution for these reflection coefficients involves determining the scattering parameters of the two-port network.

3.1.1 Passivity

A network $\mathbf{S}$ is lossless if its total output power equals its total input power, and passive if its input impedances contain only non-negative real parts over all other passive port impedance terminations. Typically, if a passive circuit is fabricated with non-magnetic materials, it is reciprocal but not symmetric nor lossless. Reciprocal matrices consider networks $\mathbf{S}$ such that $S_{ij} = S_{ji}$, while symmetric matrices consider networks $\mathbf{S}$ such that $\mathbf{S} = \mathbf{S}^{\mathrm{T}}$. Though lossless cases are useful approximations for low-loss networks, in general, a passive network must satisfy:

$$\mathbf{I} - \mathbf{S}^{+}\mathbf{S} = \mathbf{A} \succeq 0, \tag{3.1}$$

where $\mathbf{S}^{+}$ is the conjugate transpose of $\mathbf{S}$ [63]. Because $\mathbf{A}$ is a Hermitian matrix, it has purely real eigenvalues λ, and so (3.1) requires $\lambda \geq 0$. With $\mathbf{S}$ parameters of a two-port network expressed as $S_{ij}\,(m_{ij},\, \theta_{ij}) = m_{ij}\, e^{j\,\theta_{ij}}$, the characteristic equation of $\mathbf{A}$ is determined as:

$$\lambda^2 - \lambda(B_1 + B_2) + (B_1 B_2 - B_3) = 0, \tag{3.2a}$$

$$B_1 = 1 - (m_{11}^2 + m_{12}^2) \tag{3.2b}$$

$$B_2 = 1 - (m_{22}^2 + m_{12}^2), \tag{3.2c}$$

$$B_3 = m_{12}^2(m_{11}^2 + m_{22}^2 + 2m_{11}m_{22}\cos\phi), \tag{3.2d}$$

$$\phi = \theta_{11} + \theta_{22} - 2\theta_{12}. \tag{3.2e}$$

Solving (3.2) for the eigenvalues λ yields:

$$\lambda = \frac{B_1 + B_2}{2} \pm \sqrt{(\frac{B_1 - B_2}{2})^2 + B_3} \geq 0, \tag{3.3}$$

with the argument of the square root function guaranteed non-negative. Finding and evaluating the critical points of (3.2d) yields $B_3 \geq 0$, confirming purely real λ. If $B_1 + B_2 < 0$, then at least one eigenvalue will always be negative, which cannot be the case for a passive network. Therefore, $B_1 + B_2 \geq 0$. To ensure the solution (3.3) with the negative sign yields a non-negative λ, $B_1 B_2 \geq B_3 \geq 0$. Furthermore, because $B_1 B_2 \geq 0$, $B_1 \geq 0$ and $B_2 \geq 0$, yielding the well-known power conservation conditions also found in [63]:

$$0 \leq m_{11}^2 + m_{12}^2 \leq 1, \tag{3.4a}$$

$$0 \leq m_{22}^2 + m_{12}^2 \leq 1. \tag{3.4b}$$

The phase relationship between S_{ij} can be determined from $B_1 B_2 \geq B_3$. Expanding and re-arranging yields:

$$2m_{12}^2(1 + m_{11}m_{22}\cos\phi) \leq (1 - m_{11}^2)(1 - m_{22}^2) + m_{12}^4, \tag{3.5}$$

which generalizes the well-known lossless phase condition [63] to lossy networks. If $m_{11} \neq 0$, $m_{22} \neq 0$, and $m_{12} \neq 0$, (3.5) is more clearly expressed as:

$$-1 \leq \cos\phi \leq \frac{(1 - m_{11}^2)(1 - m_{22}^2) - m_{12}^2(2 - m_{12}^2)}{2m_{11}m_{22}m_{12}^2}. \tag{3.6}$$

Note that ϕ is arbitrary if $m_{11} = 0$, $m_{22} = 0$, or $m_{12} = 0$. If all are non-negative, such as when $m_{12}^2 = 0.8$ and $m_{11}^2 = m_{22}^2 = 0.01$, ϕ may still be arbitrary if:

$$1 \leq \frac{(1 - m_{11}^2)(1 - m_{22}^2) - m_{12}^2(2 - m_{12}^2)}{2m_{11}m_{22}m_{12}^2} = f_a. \tag{3.7}$$

When (3.7) is true, the resulting arbitrary-phase network is passive, independent of the phases θ_{ij}, allowing additional degrees of design freedom, which is useful for broadband matching. If (3.7) is

not satisfied, the resulting constrained-phase network is passive only for some values of θ_{ij}. The single-frequency analysis above is a starting point for broadband matching network design; the narrowband lowest-loss case degrades over bandwidth.

3.1.2 Matching Problem Definitions

Consider the double-matching problem of Fig. 3.1, where two known but arbitrary one-port $\mathbf{S}^1$ and $\mathbf{S}^2$ networks are connected between an unknown two-port $\mathbf{S}$ network. The presented reflection coefficients by $\mathbf{S}$ are fixed, arbitrary, and the solution involves finding $\mathbf{S}$. For a desired Γ_1' and Γ_2', and given Γ_1 and Γ_2, simultaneous non-conjugate low-loss match, it follows that [56]:

$$\Gamma_1' = S_{11} + \frac{S_{12}^2 \Gamma_2}{1 - S_{22}\Gamma_2}, \tag{3.8a}$$

$$\Gamma_2' = S_{22} + \frac{S_{12}^2 \Gamma_1}{1 - S_{11}\Gamma_1}. \tag{3.8b}$$

The trivial case, when all reflection coefficients are zero, leads to a solution were $S_{11} = S_{22} = 0$ and $S_{12} = S_{21} = 1$. This suggests that the two loads can be directly connected. Similarly, it is useless to set $S_{12} = S_{21} = 0$ such that $S_{11} = \Gamma_1' = \Gamma_{desired,1}$ and $S_{22} = \Gamma_2' = \Gamma_{desired,2}$, as this prevents any power transfer through $\mathbf{S}$. Three specific sets of constraints are examined: (1) symmetric, reciprocal, and lossless networks; (2) reciprocal and lossless networks; and (3) reciprocal and lossy networks.

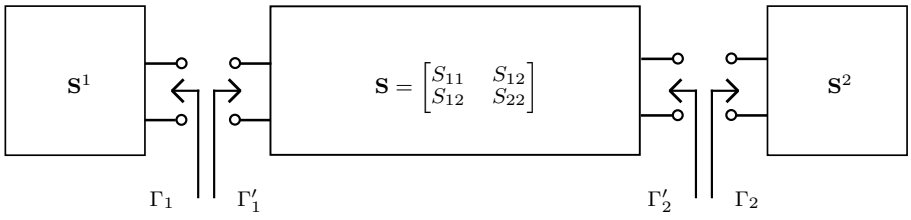


Figure 3.1: Simultaneous non-conjugate double matching schematic, *i.e.* $\Gamma_1 \neq \Gamma_1'^*$ and $\Gamma_2 \neq \Gamma_2'^*$. An unknown two-port network $\mathbf{S}$ is connected between given one-port networks $\mathbf{S}^1$ and $\mathbf{S}^2$ with transmission lines of negligible length. Solving for the $\mathbf{S}$ parameters gives a solution $\mathbf{S}$ with minimal loss such that Γ_1' and Γ_2' are desired complex reflection coefficients.

3.1.3 Symmetric, Reciprocal, and Lossless Networks

For a symmetric and reciprocal network, $S_{11} = S_{22}$ and $S_{12} = S_{21}$. Using (3.1), power conservation for the lossless case is expressed as:

$$|S_{11}|^2 + |S_{12}|^2 = 1. \tag{3.9}$$

It also follows that a relation between the angles can be expressed as:

$$\angle S_{11} - \angle S_{12} = \frac{\pi}{2} + \pi n, \tag{3.10}$$

where n is any integer. Therefore, S_{12} can be related entirely to the value of S_{11} as:

$$S_{11} = m e^{j\theta_1} \tag{3.11}$$

$$S_{12} = \pm j\sqrt{1 - m^2} e^{j\theta_1}. \tag{3.12}$$

Equations (3.11) and (3.12) can be used with (3.8a) and (3.8b) to solve for the two respective equations:

$$m_1 = \frac{\Gamma_1' + \Gamma_2 e^{j2\theta_1}}{(1 + \Gamma_1'\Gamma_2)e^{j\theta_1}} \tag{3.13}$$

$$m_2 = \frac{\Gamma_2' + \Gamma_1 e^{j2\theta_1}}{(1 + \Gamma_2'\Gamma_1)e^{j\theta_1}}, \tag{3.14}$$

where $\Gamma_1' = \Gamma_{1,desired}$, $\Gamma_2' = \Gamma_{2,desired}$. For a simultaneous match it is required that $m_1 = m_2$. When true, the required constraints on the reflection coefficients are found to be:

$$\frac{1}{\Gamma_1} - \Gamma_1' = \frac{1}{\Gamma_2} - \Gamma_2' \tag{3.15}$$

$$\Gamma_1\Gamma_1' = \Gamma_2\Gamma_2', \tag{3.16}$$

These set of equations lead to a forced relationship between S_{11} and S_{12} for a symmetrical, lossless, and reciprocal network. Two classes are defined: when $\Gamma_1 = \Gamma_2$ and when $\Gamma_1 \neq \Gamma_2$.

3.1.3.1 Class One: $\Gamma_1 = \Gamma_2$ (General)

In the first class, $\Gamma_1' = \Gamma_2'$ due to (3.16). Therefore:

$$m_1 = m_2 = m = \frac{\Gamma_1' + \Gamma_1 e^{j2\theta_1}}{(1 + \Gamma_1'\Gamma_1)e^{j\theta_1}}, \tag{3.17}$$

and $\mathbf{S}$ is now fully described in terms of only θ_1. However, m must be purely real, which introduces the additional constraint of $Im\{m\} = 0$, leading to:

$$A_1 \sin(\theta_1 + \angle\Gamma_1) = A_1' \sin(\theta_1 - \angle\Gamma_1'), \tag{3.18}$$

where

$$A_1 = \frac{|\Gamma_1|}{1 - |\Gamma_1|^2} \tag{3.19}$$

$$A_1' = \frac{|\Gamma_1'|}{1 - |\Gamma_1'|^2}. \tag{3.20}$$

The harmonic addition theorem can be used to solve for θ_1 in (3.18) as:

$$\sqrt{a^2 + b^2} \cos\left(\theta_1 + \arctan\left(\frac{b}{a}\right)\right) = 0, \tag{3.21}$$

where

$$a = A_1' \sin(\angle\Gamma_1') + A_1 \sin(\angle\Gamma_1) \tag{3.22}$$

$$b = A_1' \cos(\angle\Gamma_1') - A_1 \cos(\angle\Gamma_1). \tag{3.23}$$

The two ways to solve (3.21) include either setting the coefficient of the cosine term to zero or choosing θ_1 such that the cosine term goes to zero when the coefficient is not zero. The latter is achieved when:

$$\theta_1 = \frac{\pi}{2} - \arctan(\frac{b}{a}) + \pi n, \tag{3.24}$$

for any integer n. Equation (3.24) can be plugged into (3.17), demonstrating that a symmetrical, lossless, and reciprocal network can simultaneously transform any two symmetrical loads into any two symmetrical non-conjugate ones. However, there are at most two solutions.

The former way to solve (3.21) is achieved with either a conjugate match (considered in-depth below) or when Γ_1 and Γ_1' are purely reactive. Considering the purely reactive class subset, θ_1 is arbitrary (leading to possibly many solutions) and:

$$m = \frac{cos\left(\theta_1 + \frac{\angle\Gamma_1 - \angle\Gamma_1'}{2}\right)}{cos\left(\frac{\angle\Gamma_1 + \angle\Gamma_1'}{2}\right)}. \tag{3.25}$$

Therefore, for any set of purely reactive reflection coefficients, θ_1 can be chosen such that $|m| \leq 1$. The solution, however, may be trivial. For the conjugate match class subset, $\Gamma_1' = \Gamma_1^*$, and (3.17) becomes:

$$m = 2A_1 cos(\theta_1 + \angle\Gamma_1). \tag{3.26}$$

It is seen that the conjugate-match case is always realizable and that there are many solutions.

The trivial case subset of (3.17) is obtained when $|\Gamma_1'| = |\Gamma_1|$ and $\theta_1 = \frac{1}{2}(\angle\Gamma_1' - \angle\Gamma_1 + \pi) + \pi n$ for any integer n. For example, when $m = 0$, a $\frac{\lambda}{4}$ transmission line will match two identical capacitors. Other cases involving a complex impedance will not result in the trivial case.

3.1.3.2 Class Two: $\Gamma_1 \neq \Gamma_2$ (Pure Reactance)

Considering the second class when $\Gamma_1 \neq \Gamma_2$, $\Gamma_1\Gamma_1' = 1$ and $\Gamma_2\Gamma_2' = 1$ because of (3.15) and (3.16). This leads to $|\Gamma_1| = |\Gamma_1'| = |\Gamma_2| = |\Gamma_2'| = 1$, $\Gamma_1 = \Gamma_1'^*$, and $\Gamma_2 = \Gamma_2'^*$. Therefore this second class is a pure reactance matching problem, extending the first class by allowing dissimilar reactive loads, but now requiring a conjugate match. By plugging in the constraints on the reflection coefficients, setting (3.13) and (3.14) equal to each other, and solving for the real and imaginary

parts, relationships between $\angle\Gamma_1$, $\angle\Gamma_2$, and θ_1 are found. From these, two solution sub-classes are defined. The first one is for $\Gamma_1 = -1$ and $\Gamma_2 = 1$, which leads to a solution of $\theta_1 = 0$ and arbitrary m. This shows that a zero impedance (short circuit) can always be matched to an infinite impedance (open circuit), whether $m = 1$ (useless case), $m = 0$ and a quarter-wave transformer is used, or another network is used for other values of m. The second subclass is for:

$$\theta_1 = \frac{\pi - \angle\Gamma_1 - \angle\Gamma_2}{2} + \pi n. \tag{3.27}$$

For example, if $\mathbf{S}^1$ and $\mathbf{S}^2$ are a capacitor and inductor with equal impedance magnitudes, respectively, then it can be shown that a realizable network, which presents a conjugate match to both sides, requires $\theta_1 = \pm\frac{\pi}{2}$ and an arbitrary m. Again, this shows that these two reactances can always be matched to each other, whether $m = 1$ by adding a parallel inductor to $\mathbf{S}^1$ and parallel capacitor to $\mathbf{S}^2$ (useless case, no longer symmetric), $m = 0$ and the two are directly connected, or another network is used for other values of m. For purely reactive loads, there still exists a single degree of freedom, but now it is m instead of θ_1.

Even though the second solution class is not practical as practical loads always have some resistance, it provides useful insight into how to match reactive loads. This could provide a useful starting point for when resistances are very low, *e.g.*, matching high-power transistors. In practice, though, a symmetrical, lossless, and reciprocal network can only provide a solution when $\Gamma_1 = \Gamma_2$. It is not necessary, however, to present a conjugate match, which will then introduce reflection loss. This type of network could be used as a PA ISMN to provide the appropriate load to the drain of the driver while accepting whatever gate impedance is presented to the power stage.

3.1.4 Reciprocal and Lossless Networks

For a reciprocal network, $S_{12} = S_{21}$. Then, using (3.1), it can be shown that $|S_{11}| = |S_{22}|$ for a non-symmetric but lossless network, and thus (3.9) holds. The relation between the angles, however, must be updated to:

$$\frac{\angle S_{11}(f)}{2} - \angle S_{12}(f) + \frac{\angle S_{22}(f)}{2} = \frac{\pi}{2} + \pi n, \tag{3.28}$$

where n is any integer. Using (3.11) and (3.28), S_{12} can be related entirely to the values of S_{11} and S_{22} as:

$$S_{22} = me^{j\theta_2} \tag{3.29}$$

$$S_{12} = \pm j\sqrt{1-m^2}e^{j\frac{\theta_1+\theta_2}{2}}, \tag{3.30}$$

together known as the Belevitch representation [59,65]. Equations (3.11), (3.29), and (3.30) can be used with (3.8a) and (3.8b) to solve for the two respective equations:

$$m_1 = \frac{\Gamma_1' + \Gamma_2 e^{j(\theta_1+\theta_2)}}{e^{j\theta_1} + \Gamma_1'\Gamma_2 e^{j\theta_2}} \tag{3.31}$$

$$m_2 = \frac{\Gamma_2' + \Gamma_1 e^{j(\theta_1+\theta_2)}}{e^{j\theta_2} + \Gamma_2'\Gamma_1 e^{j\theta_1}}, \tag{3.32}$$

again where $\Gamma_1' = \Gamma_{1,desired}$ and $\Gamma_2' = \Gamma_{2,desired}$. Equations (3.31) and (3.32) must first be made to be purely real with the following constraints, respectively:

$$A_1' sin(\theta_1 - \angle\Gamma_1') = A_2 sin(\theta_2 + \angle\Gamma_2) \tag{3.33}$$

$$A_2' sin(\theta_2 - \angle\Gamma_2') = A_1 sin(\theta_1 + \angle\Gamma_1), \tag{3.34}$$

where

$$A_2 = \frac{|\Gamma_2|}{1-|\Gamma_2|^2} \tag{3.35}$$

$$A_2' = \frac{|\Gamma_2'|}{1-|\Gamma_2'|^2} \tag{3.36}$$

Equations (3.33) and (3.34) can be solved simultaneously to decouple θ_1 and θ_2, obtaining the two implicit equations:

$$\arcsin\left(\frac{A_1'}{A_2}\sin\left(\theta_1 - \angle\Gamma_1'\right)\right) - \arcsin\left(\frac{A_1}{A_2'}\sin\left(\theta_1 + \angle\Gamma_1\right)\right) = \angle\Gamma_2 + \angle\Gamma_2' \tag{3.37}$$

$$\arcsin\left(\frac{A_2'}{A_1}\sin\left(\theta_2 - \angle\Gamma_2'\right)\right) - \arcsin\left(\frac{A_2}{A_1'}\sin\left(\theta_2 + \angle\Gamma_2\right)\right) = \angle\Gamma_1 + \angle\Gamma_1' \tag{3.38}$$

If there is a solution for these two equations, then the resulting θ_1 and θ_2 can be used to calculate m_1 and m_2 from (3.31) and (3.32). However, no additional degrees of freedom are available to set $m_1 = m_2$. Therefore it is shown that only certain reflection coefficients can be used with a lossless and reciprocal network. If a solution exists, there is only a single set of scattering parameters that will satisfy the equation. Regardless, because of how restrictive this case is, it is not practical to implement.

For the conjugate-match case, (3.33) and (3.34) become the same equation, which can be rearranged as:

$$\theta_2 = \arcsin\left(\frac{A_1}{A_2}\sin\left(\theta_1 + \angle\Gamma_1\right)\right) - \angle\Gamma_2. \tag{3.39}$$

Now, (3.31) and (3.32) can be set equal to each other and solved using the remaining variable θ_1. Note that θ_1 can always be chosen such that the magnitude of the argument of arcsin is less than or equal to one. This shows that a network solution always exists for a simultaneous conjugate match to two non-symmetrical loads, and that there could be many solutions. A similar conclusion is obtained in [56]. However, that work does not explicitly give equations for $\mathbf{S}$ in terms of reflection coefficients and still requires stability to be checked with K and Δ_S. This work inherently guarantees stability if all $|\Gamma| < 1$. However, because of the restrictive nature of the aforementioned solutions here, for general reflection coefficients, it is shown that a sacrifice must be made in terms of loss or desired reflection coefficient.

3.1.5 Reciprocal and Lossy Networks

For a reciprocal ($S_{21} = S_{12}$) network, (3.4) and (3.5) must hold for the network to be passive. For such a network to be a simultaneous non-conjugate solution, (3.8a) and (3.8b) must be simultaneously true. Solving for S_{12}^2 gives the relationship:

$$S_{22} = S_{11} \cdot \frac{\Gamma_1(\Gamma_2\Gamma_2' - 1)}{\Gamma_2(\Gamma_1\Gamma_1' - 1)} + \frac{\Gamma_1\Gamma_1' - \Gamma_2\Gamma_2'}{\Gamma_2(\Gamma_1\Gamma_1' - 1)} \tag{3.40}$$

as a constraint that ensures a simultaneous solution. For the desired Γ_1' and Γ_2', inserting (3.40) into (3.8b) yields:

$$S_{12} = \pm\sqrt{S_{11}S_{22} - S_{11}\Gamma_2' - \frac{S_{22}}{\Gamma_1} + \frac{\Gamma_2'}{\Gamma_1}}. \tag{3.41}$$

Now $\mathbf{S}$ is completely expressed in terms of $S_{11}\,(m_{11},\ \theta_{11})$ and the given Γ's in Fig. 3.1. When $S_{11}\,(m_{11},\ \theta_{11})$ is chosen such that all passivity constraints are satisfied, the power loss (or power gain) $L_P\,(\text{dB}) = -G_P\,(\text{dB})$ [56] of an ISMN that presents desired Γ_1' and Γ_2' is evaluated using (3.40) and (3.41):

$$L_P = -10\log\left(\frac{1 - |\Gamma_2|^2}{1 - |\Gamma_1'|^2}\frac{|S_{12}|^2}{|1 - S_{22}\Gamma_2|^2}\right). \tag{3.42}$$

Equation (3.42) can be numerically minimized by choice of $S_{11}\,(m_{11},\ \theta_{11})$ with two degrees of freedom, and constrained by (3.4), (3.5), (3.40), and (3.41) to solve the simultaneous non-conjugate matching problem in Fig. 3.1. With all $|\Gamma| \leq 1$, this solution inherently guarantees network passivity, unlike the approach in [56]. It is noted that similar relations are obtained from a power-conservation point-of-view in [66], albeit with added constraints for K and Δ_S assuming a simultaneous conjugate match. Further, it can be shown that only conjugate-match solutions are lossless, which is left as an exercise for the reader.

The results of this section are used for a practical PA design process in Section 5.1.2. By finding the drain and gate impedances of the first and second-stage transistors of a two-stage PA,

and determining the appropriate load and source-pull impedances for these two terminals, a non-conjugate double-matching problem is established. This problem is then solved with broadband matching networks, described in the following section.

3.2 Broadband Networks

This section deals with the fundamental matching limitations of a broadband matching network given by the Bode-Fano criterion and how it applies to PA design. It also describes a branch-search algorithm to synthesize such a broadband network as an alternative to the real-frequency technique.

3.2.1 Bode-Fano Criterion

A lossless two-port matching network N'' connected to a parallel RC load presents a reflection coefficient $\Gamma(\omega)$, shown in Fig. 3.2 (a). Bode [67] showed that $\Gamma(\omega)$ is constrained by:

$$\int_0^\infty \ln \frac{1}{|\Gamma(\omega)|} \mathrm{d}\omega < \frac{\pi}{RC}. \tag{3.43}$$

Assuming a brick-wall response as the optimal $\Gamma(\omega)$ function, the minimum upper-bound on $|\Gamma(\omega)| = \Gamma_{min}$ can be described as:

$$\ln \Gamma_{min} = -\frac{1}{RC}\frac{\pi}{b\omega_0}, \tag{3.44}$$

with fractional bandwidth b and center angular frequency ω_0. Because R, C, b, and ω_0 must be positive, Γ_{min} and b are bounded between $[0, 1]$ and $[0, \infty]$, respectively. N'' can be any physically realizable network, consisting of only reactive elements [68], that corresponds to the Γ_{min} brick-wall response. No other physical network can have a smaller Γ_{min} value over this bandwidth.

Fano [69] demonstrated that because some characteristics of N' are independent of N'', characteristics of the cascade can be determined from just the known N'. The work of Bode was limited to N' containing a single reactive element. Fano's extension determined that an analytical solution

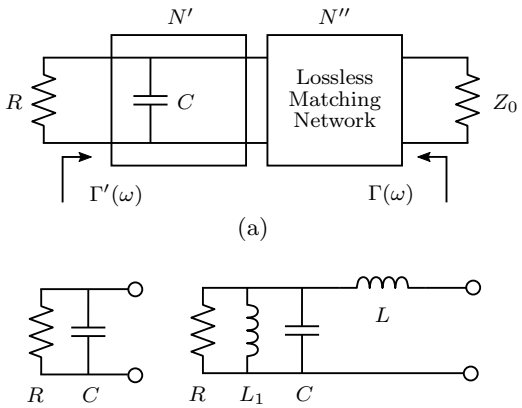


Figure 3.2: (a) The Bode criterion gives a bandwidth relationship between $\Gamma(\omega)$ and N' networks consisting of a single reactive element (shunt C here). Fano extended this to two reactive elements and showed the theory for an arbitrary number of reactive elements, reformulating the criterion for $\Gamma'(\omega)$. Network approximations of the (b) transistor with parasitics and (c) transistor, parasitics, and bias-network.

for Γ_{min} exists if N' contains at most two non-degenerate elements, but offers the mathematics for a numerical approach if N' contains more than two elements.

Fano's procedure is modified by Kerr [70] to avoid a low-pass to band-pass transformation, which also suggests a way to examine an arbitrary load. If the load is physically realizable, Darlington [68] demonstrated that it can be described by the input to a network, comprised only of reactive elements, connected to a resistive termination. Therefore, if some arbitrary load can be described reasonably well by this type of circuit equivalent over at least the frequency bandwidth of interest, then Fano's conclusion could be applied numerically to determine the matching limitations for the load.

For the parallel RC load example, one can consider the reactive component (shunt C), as one network N', which can consist of many reactive elements. This network is connected to the resistive component of the load (shunt R), and the lossless matching network N''. The N'' network is connected to another resistive load, typically $Z_0 = 50\,\Omega$, and it can be shown that the value of Z_0 does not affect the quality or bandwidth of $\Gamma'(\omega)$ in Fig. 3.2 (a). $\Gamma'(\omega)$ can be used in (3.43) instead of $\Gamma(\omega)$, which has implications for PA design. This conclusion is commonly referred to as the Bode-Fano criterion.

3.2.2 Application to Power Amplifier Design

In this section, the Bode-Fano criterion is applied to sub bands and to the entire frequency range, with and without the bias networks of a PA. Equation (3.43) results in a conjugate match for $\Gamma'(\omega)$; however, in PA design, large-signal impedances such as those obtained from load-pull are not conjugately-matched. Furthermore, quality of match $\Gamma'(\omega)$ becomes dependent on the spacings of the load-pull contours, as [39, 71] summarize. These works determine the optimal conjugate load-pull impedances within the bandwidth of interest (impedance trajectory) and approximate it with a one or two-element N' network to apply (3.43). For more general conclusions, *e.g.* modeling parasitics as well, one could represent the impedance trajectory as an arbitrary load. This is valid only if the load is physically realizable as R and N', with N' containing only reactive elements [68].

As an example, consider the 7 W Qorvo T2G-6000528-Q3 transistor in a hybrid PA, with series source impedance $\mathrm{R} = 0.8\Omega$ and $\mathrm{L} = 0.17\,\mathrm{nH}$, between 1.8 and 4 GHz. For the physically realizable arbitrary load (5-element N') describing the impedance trajectory, Kerr's approach [70] is used to evaluate (3.43). However, the resulting system of nonlinear polynomial equations does not seem to have a solution. This suggests that the Bode-Fano criterion cannot always be used to describe an arbitrary load and limits N' to two reactive elements, as Fano [69] suggested.

As a compromise, the impedance trajectory of the device output can be approximately described with a parallel $\mathrm{R} = 45\,\Omega$ and $\mathrm{C} = 0.85\,\mathrm{pF}$ network (which includes packaging parasitics), corresponding to $\Gamma_{min} = -52\,\mathrm{dB}$ and shown in Fig. 3.2 (b). Realistic bias-tees and stability networks are added, consisting of a microstrip line interface with the transistor, Modelithics capacitor model as the dc block, and a meandered line as the RF choke. Source and load-pull simulations confirm that performance remains similar. The updated impedance trajectory can now be described by the inductively tuned low-pass structure [70] consisting of a parallel $\mathrm{R} = 50\,\Omega$, $\mathrm{L}_1 = 2.7\,\mathrm{nH}$, and $\mathrm{C} = 1.3\,\mathrm{pF}$, connected to a series $\mathrm{L} = 0.3\,\mathrm{nH}$, shown in Fig. 3.2 (c). The impedance trajectories and the conjugate load-pull impedances are shown in Fig. 3.3. The fitted lines for the RC/RLC loads from Fig. 3.2 overlap with PAE contours, but match degrades with a bias-tee, as Table 3.1 shows.

Table 3.1: Summary of Γ_{min} with and without Bias-Tees

Freq. (GHz)	No Tee [dB]	Tee [dB]	Tee (degen) [dB]
1.8–4	-52	-123	-30
1.8–2.8	-104	-276	-67
3–4	-121	-289	-107

In the non-degenerate case [69] of Fig. 3.2(c) (when the first element of N'' is *not* a series inductance), an improved $\Gamma_{min} = -123\,\text{dB}$ results. In the degenerate case when the first element *is* a series inductance, a degraded $\Gamma_{min} = -30\,\text{dB}$ results. In PA applications, the degenerate case is typically used, as other options either prevent dc bias (series C or shunt L) or limit higher-frequency performance (shunt C). Results for the 1.8–4 GHz band, and two smaller sub bands, are summarized in Table 3.1, for the transistor without and with a bias-tee, and with a bias-tee

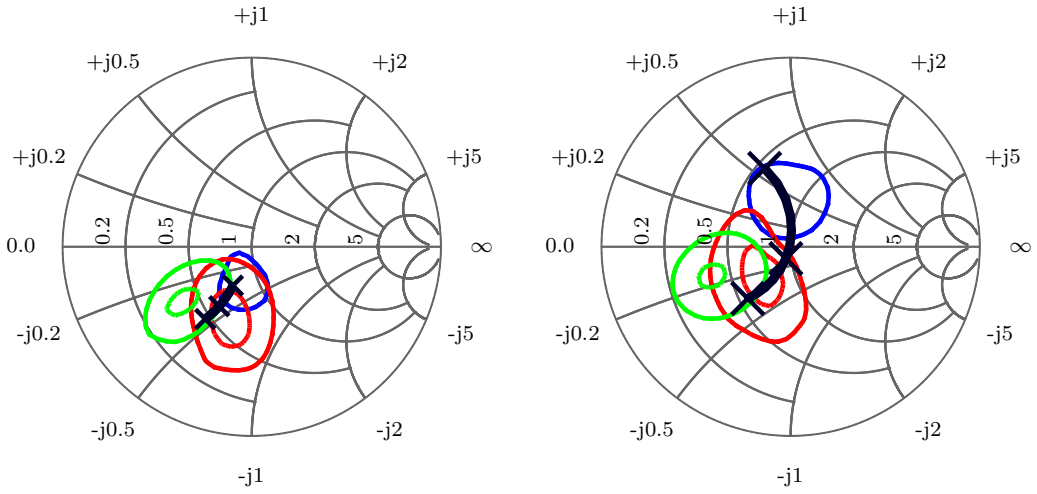


Figure 3.3: Simulated conjugate load-pull constant PAE contours for the 7 W Qorvo T2G-6000528-Q3 transistor (a) without and (b) with a bias-tee. The black line represents the fitted *RC* or *RLC* load trajectory, respectively, with markers at 1.8, 3, and 4 GHz. These markers also correspond to the blue, red, and green contours. Outer contours are at (a) 64 and (b) 60 % PAE, while inner contours are at (a) 71 and (b) 67 % PAE. There is no inner contour at 1.8 GHz because its 2nd harmonic is terminated with the 3.6 GHz fundamental impedance.

network connected directly to a degenerate series inductance. To overcome the Γ_{min} limitation, one can sacrifice bandwidth in order to improve the performance of a PA [39], as the improved sub band Γ_{min} of Table 3.1 demonstrates. This leads to a broadband PA architecture where two narrowband (30–40% fractional bandwidth) PAs, with offset center frequencies, are combined at the input and output with diplexers, as described in Section 5.2.

3.2.3 Branch Search Algorithm

To synthesize broadband matching networks for multi-stage power amplifiers, the simplified RFT method is a well-known option [59]. This method analytically optimizes and flattens the response of lossless matching networks over frequency, where the ISMN design is a type of double-matching problem [60]. However, this approach assumes a lossless conjugate match, whereas efficient PAs require a non-conjugate match at the drain and gate device terminals.

Another method to synthesize broadband matching networks is to utilize stepped-impedance lines [72, 73]. This approach is discussed in more detail in Section 5.1.1 and shown to work well in hybrid implementations. However, stepped-impedance lines may be more difficult to realize in MMIC implementations. Therefore, alternate broadband matching networks are required.

When designing PAs, and especially MMIC PAs, matching networks typically contain series transmission lines and shunt capacitors and inductors (implemented as shorted stubs). The network parameters of these elements can be found in [74], which describes each element in terms of its physical parameters such as length, width (for transmission lines), and capacitance (for capacitors). By arranging in order the desired elements for a network topology, the overall network can be described by the multiplication of each element's ABCD matrix. The resulting matrix then can be transformed into its scattering matrix representation, giving the network performance in terms of its constitutive geometry components over frequency. Reflection coefficients Γ_1' and Γ_2' can be determined from this network and given Γ_1 and Γ_2.

One can determine the gate and/or drain impedances, along with the load-pull impedances, for any PA matching network. Because Section 3.1.5 demonstrated that a simultaneous non-

conjugate lossless solution does not exist, a wide range of loss and match quality trade-offs can be made. In this section, this problem is solved numerically but Section 5.1.2 describes a more analytical approach for PA design. Topological considerations form the basis for a numerical solution to allow for solutions covering a broad bandwidth.

First, several objective functions are defined to indicate how well a problem is solved. Two nonlinear functions can be written using (3.8a), (3.8b), and desired reflection coefficients, as:

$$f_1 = |\Gamma'_1 - \Gamma'_{1,desired}|^2 \tag{3.45}$$

$$f_2 = |\Gamma'_2 - \Gamma'_{2,desired}|^2. \tag{3.46}$$

With this least squares approach, when f_1 and f_2 both equal zero, Γ'_1 and Γ'_2 will equal $\Gamma'_{1,desired}$ and $\Gamma'_{2,desired}$, respectively. An additional nonlinear objective function is defined to correspond to the loss of the network:

$$f_3 = |G - G_{desired}|^2, \tag{3.47}$$

again utilizing a least squares approach, where G can represent either G_T, G_A, or G_P. A desired minimization objective function is now defined as:

$$M = \sum_{n=1}^{3} f_n. \tag{3.48}$$

The minimization function (3.48), with constraints (3.4) and (3.5), form a numerical problem that can be efficiently computed. Due to its ease of setup, use, and integration with circuit simulators, MATLAB's *fmincon* function is used to minimize (3.48).

For a given network, (3.48) is used to determine how well the network satisfies desired performance targets over the frequency range and physical parameter constraints. Different weights can be assigned to different frequencies, such as when designing a dual-band power amplifier's matching

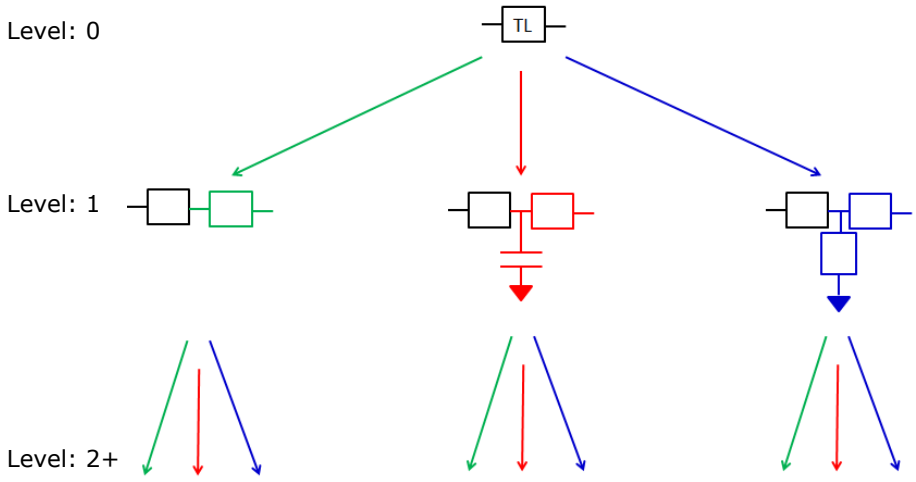


Figure 3.4: Diagram of the branch search algorithm. Three cascaded add-on elements include: (1, green) transmission line; (2, red) shunt capacitor and transmission line; and (3, blue) shunt inductor (shorted stub) and transmission line. The number of the level indicates how many add-on elements are included in the matching network; level n contains 3^n distinct topologies.

networks. Because physical transmission lines have an associated loss per unit length, overall size is also desired to be minimized. Therefore the following tree search algorithm is used:

(0) Beginning with a single transmission line, its objective function is minimized and recorded.

(1) Then, one of three possible add-on elements is cascaded to form three new topologies. These elements include: (1, green) transmission line; (2, red) shunt capacitor and transmission line; and (3, blue) shunt inductor and transmission line. Again, the objective function of each topology is minimized and recorded.

(2+) The algorithm is repeated, descending into higher-order levels until either performance targets are met or desired network complexity is exceeded. The number of the level indicates how many add-on elements are included. A diagram of this process is shown in Fig 3.4.

This algorithm is used to design the two-stage dual-band single-ended PA of Section 4.2. The gate and drain impedances of the first and second-stage transistors, along with the load-pull impedances of both, are first found before using the algorithm to design the IMN, ISMN, and OMN.

3.3 Conclusion

A mathematical analysis of lossy matching networks is detailed. Methods to synthesize narrowband and broadband networks are presented, alongside fundamental limitations to broadband design. Original contributions in this chapter include the following:

- Demonstrating for the first time in literature, to the best of the authors' knowledge, the phase relationship between scattering parameter phases of lossy networks for the double-matching problem [75].
- Developing an analytical ISMN design method for a PA [75].
- Developing a numerical ISMN design method for a PA.
- Analyzing the Bode-Fano criterion in terms of an arbitrary load and demonstrating its applicability to PA design [76].

Though the results of this chapter are used for PA design in Sections 4.2, 5.1.2, and 5.3, they are general and applicable to any design. The next chapter discusses dual-band PAs, with the following chapter focusing on broadband PAs. The contents of Chapter 3 are helpful in guiding the different design processes.

Chapter 4

Dual-band RF Power Amplifiers

Carrier aggregation in 5G communication standards requires simultaneous amplification of signals in multiple channels [25, 26], as depicted in Fig. 4.1. For reduced circuit size compared to multiple amplifiers, and greater efficiency compared to broadband designs, multi-band PAs, *e.g.* [77–79], as well as tunable PAs, *e.g.* [77, 80, 81] are an attractive option,. In these PAs, the active device is matched at two or more fundamental frequencies and their harmonics, using typical CW PA performance enhancement techniques. The case of several simultaneous modulated signals is considered in [82, 83].

Many of the efficiency improvement techniques developed for CW PAs, such as reduced conduction angle [82], harmonic terminations [78, 83], and using the transistor as a switch have been applied to dual-band PAs. In some tunable PAs, varactors are used in the matching networks, requiring an additional reverse-bias supply [80]. In the non-concurrent mode, switches can be used to toggle between two different single-frequency PAs, increasing performance at the expense of size and complexity [81].

Harmonic terminations in multi-band PAs requires simultaneous matching to many impedance values. In [78] a 7-element LC ladder network is used to terminate the first two harmonics of a class-F dual-band PA. These are then transformed to microstrip lines to be realized as a MMIC. Composite right/left-handed transmission lines are used by [83] to similarly terminate the first two harmonics of a class-F dual-band PA with two such transmission lines, simultaneously at two frequencies.

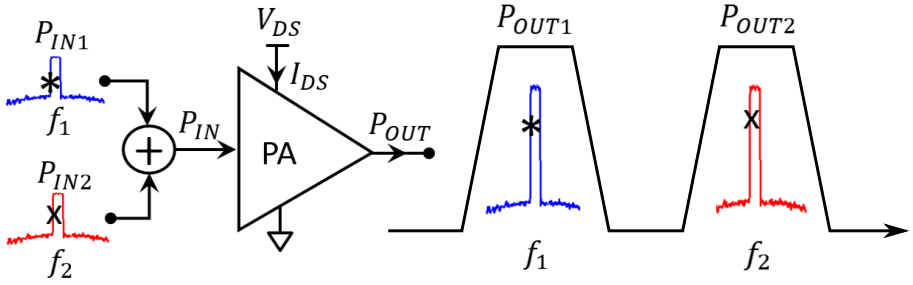


Figure 4.1: Concept block-diagram of the dual-band PA for concurrent signal amplification. Signals modulated onto two broadly separated carriers at f_1 and f_2 are concurrently amplified with high efficiency with a single load.

For applications such as phased array radar and communications, dual-band hybrid amplifiers have been published at sub-6 GHz, *e.g.* [77], and higher frequencies as MMIC implementations, but often not characterized in the concurrent mode. Many of these are single-stage PAs with limited gain, and so driver stages would be required to achieve practical levels of gain, degrading efficiency and linearity. For example, the dual-band PAs in [77, 84, 85] consist of a single-stage, while a two-stage Ka/Q dual-band PA is demonstrated in [86]. The work in [87] presents a two-stage dual-band PA covering 6-18 GHz; however, different transistors are used for different bands. The first part of this chapter describes and characterizes a single-stage 2.1/3.7 GHz PA, with the second part considering a two-stage 9/16 GHz PA, both in the non-concurrent and concurrent modes.

4.1 S-Band Power Amplifier

This section details the design and characterization of a dual-band power amplifier in S-band. CW signals are used to test the amplifier in the non-concurrent mode, followed by multiple simultaneous modulated signals to test the concurrent mode of operation.

4.1.1 S-Band Dual-Band Hybrid PA Design

Widely-spaced center frequencies of $f_1 = 2.1$ and $f_2 = 3.7$ GHz are chosen for the hybrid design and depicted in Fig. 4.1, with frequencies outside these two bandwidths not amplified. The goal is to generate and combine these two frequencies at the input of a single PA, amplify the concurrent

signals, and measure the output spectrum of the PA containing the two signals, with both CW and modulated signals considered. The design procedure focuses on terminating the f_1 and f_2 impedances as a trade-off between PAE and P_{out}.

Simulated load-pull power-added efficiency (PAE) and P_{out} contours for the 0.25 μm 15 W 28 V Qorvo GaN HEMT device (T2G6001528-SG), using the Modelithics nonlinear model, at the fundamental frequencies of the two bands, Fig. 4.2, are used as a starting point for dual-band output matching network design. This transistor is chosen because it can operate from dc–6 GHz with about 17 W output power and 15 dB linear gain. Target design load impedances of $Z_L(f_1) = 9.99 + j4.78\,\Omega$ and $Z_L(f_2) = 11.78 - j4.51\,\Omega$ are chosen as a trade-off between maximal PAE and P_{out} values (marked in plot), resulting in predicted PAE = 70/ 58 % and P_{out} = 41.5/ 39.2 dBm at the lower/ upper bands. A similar procedure is used from simulated source pull contours to determine target source impedances. Note the sensitivity to impedance of the PAE contours, which are closely spaced for low impedance values.

Because the IMN affects the drain impedance, and the OMN affects the gate impedance, each matching network requires at least eight tuning variables to achieve the four complex impedance points (each having a real and imaginary value) determined from the load and source-pull simulations: $Z_{sp,f1}$, $Z_{sp,f2}$, $Z_{lp,f1}$, and $Z_{lp,f2}$. Stepped-impedance line, shorted-stub, open-stub, and combination-based topologies were considered to achieve these values. For simplicity, and integration with the bias line (detailed later), the stepped-impedance single-stub topology of [78] is chosen

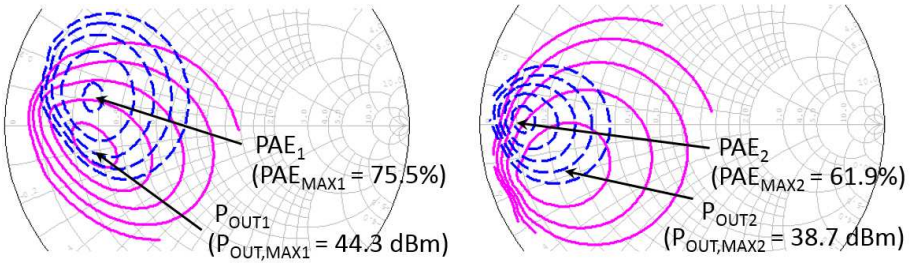
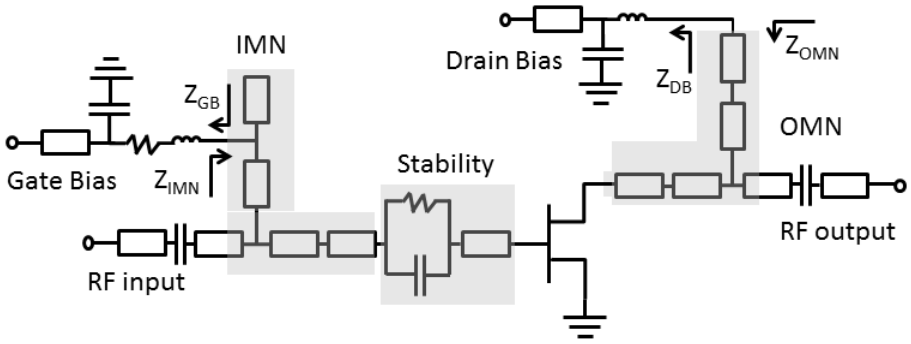


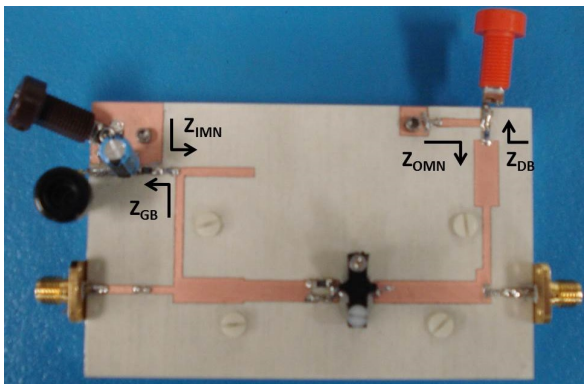
Figure 4.2: Fundamental load-pull of the Qorvo GaN 15 W GaN-on-SiC HEMT at 2.1 GHz (left) and 3.7 GHz (right). PAE contours (dashed blue lines) are shown in steps of 5 percentage points whereas P_{out} contours (solid red lines) are indicated in steps of 1 dB.

to present these impedances to the device. A circuit schematic is shown in Fig. 4.3(a).

Bias lines are designed with a 6 nH inductor with Q = 154 and self-resonant frequency (SFR) of 6 GHz, as larger inductances have lower SRFs, negatively affecting the higher band. These are placed along each stub of the matching network to ensure a high RF impedance, along with shunt 82 pF capacitors by the dc supply for stability. The bias line inductor and its parallel parasitic capacitance, in combination with the shunt capacitor and its series parasitic inductance, are designed together as a band-reject filter, with the center frequency between the two frequencies designed to present an approximate open circuit. Looking into the gate bias network, simulations give $|Z_{GB}| = 176/1350\,\Omega > |Z_{IMN}| = 9.72/188\,\Omega$ at the two carrier frequencies. Similarly, $|Z_{DB}| = 130/494\,\Omega > |Z_{OMN}| = 97.5/190\,\Omega$, referring to the photograph of the final PA in Fig. 4.3(b).



(a)



(b)

Figure 4.3: The hybrid dual-band S-band PA (a) circuit schematic and (b) photograph. The PA measures 106 x 114 mm^2.

Considering both small and large-signal performance, a dual-band PA on a 30 mil Rogers 4350B substrate with $\epsilon_r = 3.33$ is designed to operate efficiently at 2.1 and 3.7 GHz. Because the device has less gain at higher frequencies, the PA is designed to operate 1 dB in compression at the upper frequency to maintain an acceptable amount of gain. At the lower frequency, the devices operates 3 dB in compression to maximize efficiency.

The final simulated impedances at the two carrier frequencies are $Z_L(f_1) = 14.61 + j6.45\,\Omega$ and $Z_L(f_2) = 10.95 - j7.72\,\Omega$, with second harmonic impedances of $Z_L(2f_1) = 3.09 + j17.41\,\Omega$ and $Z_L(2f_2) = 37.06 - j9.00\,\Omega$. According to [51], PA efficiency increases as the second harmonic moves away from the center of the Smith chart towards a short or open. The second harmonic impedance at $f_1 = 2.1$ GHz lies in the region of the Smith chart 18 points above nominal efficiency for a Class-A PA, near the upper limit, while that of $f_2 = 3.7$ GHz lies 6 points above, chosen to maintain appropriate output power. Stability is verified with linear and nonlinear models of the HEMT over multiple gate bias voltages. A stability network consisting of a parallel 18 Ω resistor and 4.7 pF capacitor is included in the gate circuit. The complete fabricated circuit is shown in Fig. 4.3(b).

4.1.2 S-Band Dual-Band Hybrid PA CW Characterization

The PA is first characterized in the non-concurrent CW mode of operation. The device is biased at 28 V and 19 mA for a deep-AB class of operation. The maximal PAE frequency points are shifted 4.8 % from 2.1 to 2.2 GHz, and 5.4 % from 3.7 to 3.9 GHz, seen in the measured broadband frequency response in Fig. 4.4. This shift can be attributed to the sensitivity of the PAE load-pull contours to fabrication tolerances.

Plots of simulated and measured saturated gain, P_{out}, and PAE at the two peak-PAE frequencies are shown in Fig. 4.5. The drop in PAE at 3.9 GHz can be attributed to the gain discrepancy near compression between simulations and measurements due to limited output power of the driver in the upper band. Table 4.1 compares results found in the literature and this work.

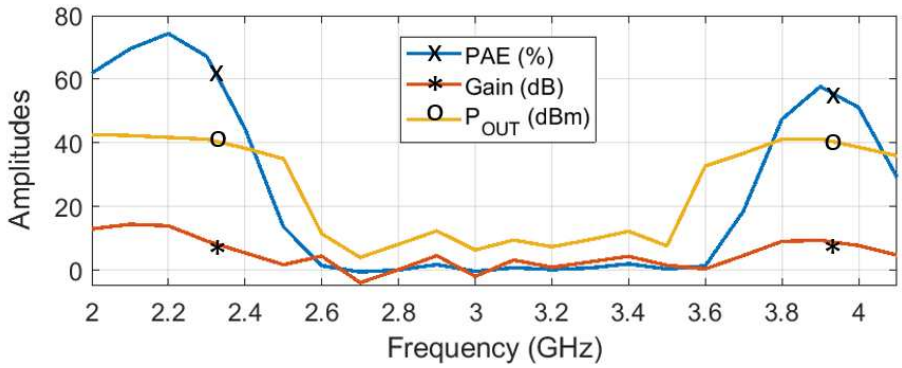
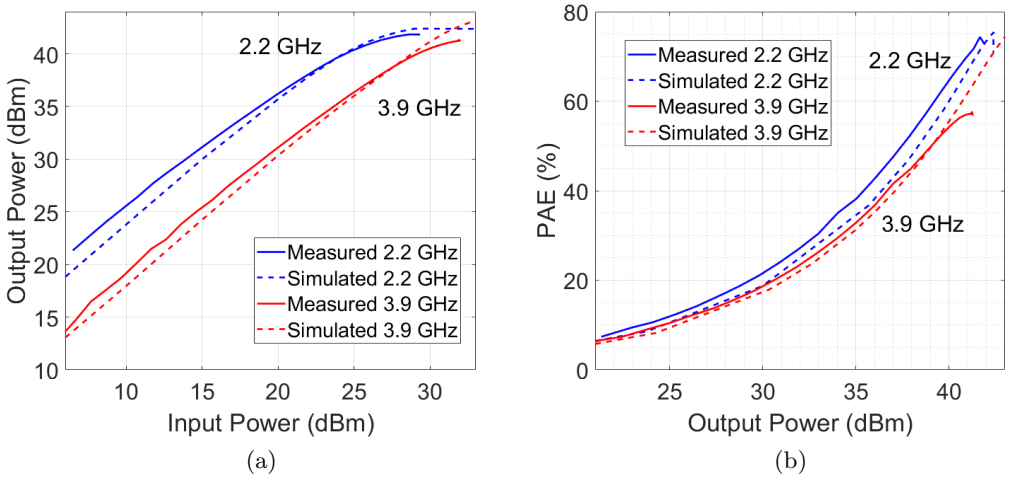


Figure 4.4: Measured CW performance of the PA over frequency. Peak efficiencies are observed at 2.2 and 3.9 GHz.



(a) (b)

Figure 4.5: Static characterization of the dual-band PA in terms of (a) output power and (b) PAE. Simulated (dashed lines) and measured values (solid lines) show good agreement.

4.1.3 Concurrent Modulated Signal PA Characterization at S-Band

The PA is next evaluated with two different multitone signals with 10 MHz bandwidth and 6 dB PAPR. Two synchronized National Instruments VSTs (PXIe-5646 and PXIe-5645), with bandwidths of 200 and 80 MHz, generate two broadly spaced signals at 2.2 and 3.9 GHz, with peak-envelope powers of 28 and 32 dBm at the PA input, respectively. These two signals are summed using a broadband combiner to generate an appropriate multi-tone signal. A linear wideband driver is used to increase signal power to drive the PA, without introducing significant intermodulation products. The driver output is attenuated and split with another broadband divider to

Table 4.1: Summary of Dual-Band PA Performance

Ref.	Freq. (GHz)	PAE (%)	P_{OUT} (dBm)	Gain (dB)
[77]	5/12	58/51	28/26.7	12/10.3
[78]	0.8/1.85	69.4/68.9	42.7/41.8	19.8/16.7
[79]	1.8/2.4	60/58	41/40	12/11
[80]	0.68/1.84	61.3/52.7	41/41.9	11/10
[81]	1.8/2.3	60.1/56.5	40.9/39.8	12/8
[82]	1.7/2.14	78/77.1	40.5/39.8	12.5/11.8
[88]	1.9/2.6	62.9/56.2	44.5/44	15/12
[89]	3.5/5.5	40.4/39.9	36.7/37.1	9.7/6.4
This work	**2.2/3.9**	**74.4/57.7**	**41.7/41.2**	**13.9/9.37**

feed the two VSTs. Pulsed characterization is performed with the PA biased at $V_{DS,Q} = 28\,\text{V}$ and $I_{DS,Q} = 19\,\text{mA}$. This setup is shown in Fig. 4.6.

Fig. 4.7 shows the narrowband gain of the PA. An AM gaussian pulse of $10\,\mu\text{s}$ duration and $100\,\mu\text{s}$ repetition period is used to sweep the input and output powers of the PA in the lower band. Simultaneously, an AM rectangular pulse of variable constant amplitude is used as the input in the higher band in order to quantify the gain degradation due to concurrent operation, Fig. 4.7(a) upper-right inset. The pulse shape is then switched between the two bands, Fig. 4.7(b) lower-right inset. When the PA is operated in non-concurrent mode, the gain is maximized. The back-off gain of the upper band increases when a second signal is injected; this effect is most likely due to a higher bias current and thus trans-conductance introduced by the concurrent signal.

Figs. 4.8(a) and 4.8(b) highlight the gain dispersion of each band of the PA when driven with two different 10 MHz 6 dB PAPR signals, with and without DPD, with representative signals depicted in the upper-right and lower-right insets, respectively. Significant cross modulation is manifested by widely scattered points, which are confined by the boundaries obtained with the narrowband characterization of Fig. 4.7. We verified experimentally that the PA characteristics are not sensitive to the phase difference between the two input signals but only to their amplitudes.

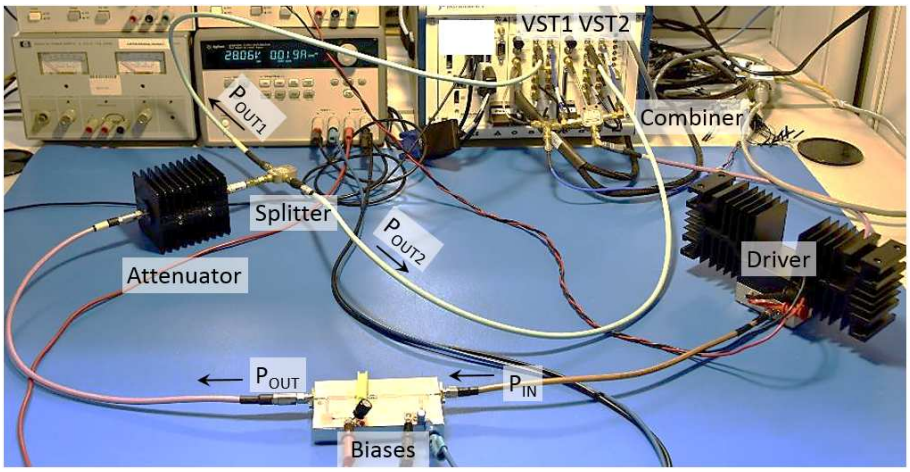


Figure 4.6: Setup for the dynamic characterization of the dual-band PA in concurrent mode. Two VSTs are employed to generate two broadly-spaced concurrent signals which are combined and injected in the PA. The output of the PA is then split and sampled around the two carrier frequencies by the VSTs.

This allows a bi-dimensional memory polynomial (2-D MP) model in which the output is only dependent on the amplitudes of the two input signals [42]. It is worth mentioning that when one of the two signals is disabled, the 2-D MP reduces to a well-known 1-D MP model. This corresponds

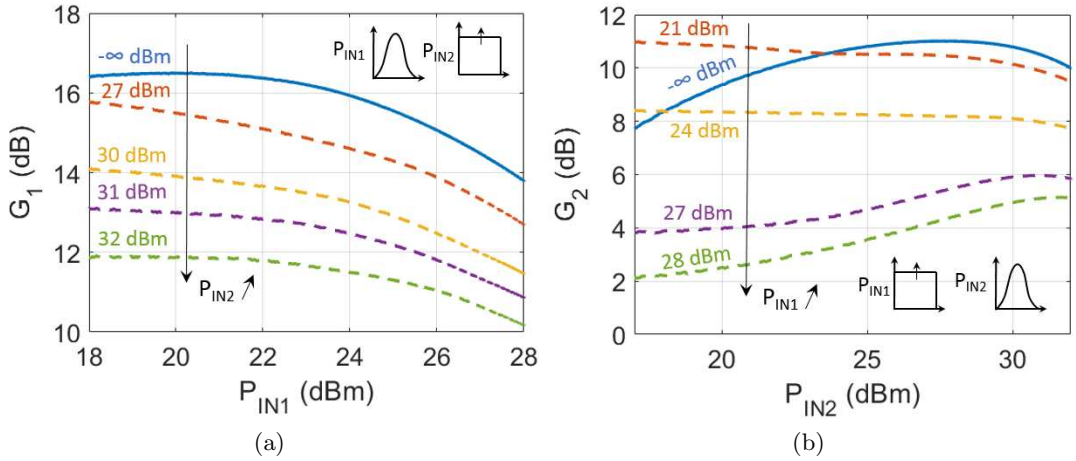


Figure 4.7: Experimental variable-amplitude Gaussian-pulsed characterization of the (a) lower band of the PA operated concurrently with a rectangular pulse at the upper band, and (b) upper band of the PA operated concurrently with a rectangular pulse at the lower band. For constant input powers at the non-swept frequency, the input power and gain is swept and measured at the other frequency, demonstrating a gain degradation induced by the concurrent signal. The insets at the (a) upper right and (b) lower right depict the input signals.

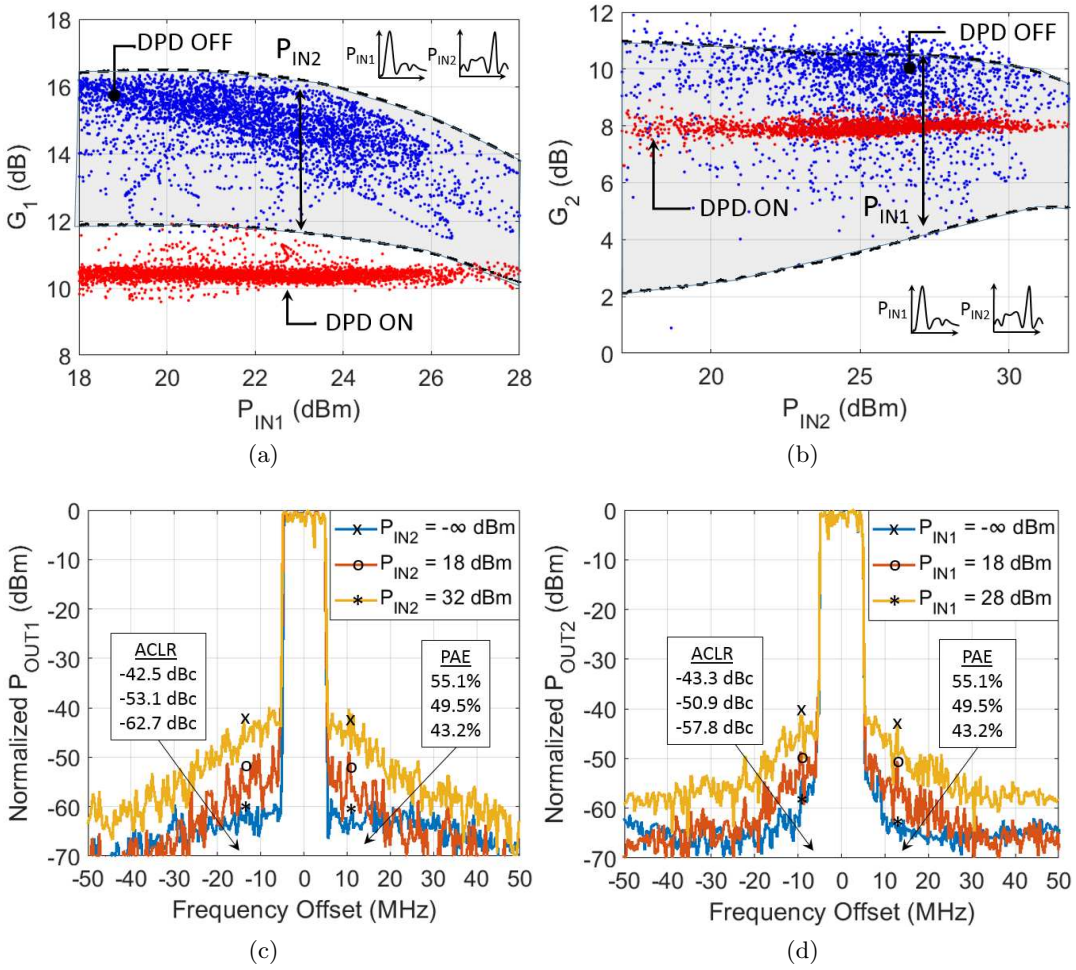


Figure 4.8: Experimental results of the PA fed with concurrent modulated 10 MHz 6 dB PAPR signals at 2.2 and 3.9 GHz illustrating (a) gain dispersion of the lower-frequency band and (b) gain dispersion of the upper-frequency band, with and without DPD. Representative signals are shown in the insets at the upper right and lower right, respectively. The (c) lower-band output spectra and (d) upper-band output spectra of the linearized PA at various maximum input powers of the other band, along with the ACLR and PAE for each input power, is shown.

to the case of non-concurrent gain from Fig. 4.7. We employ a 2-D MP model for pre-distortion with an indirect learning approach; a nonlinearity order of 7 and memory order of 1 are selected for the DPD model.

Linearized gains of the dual-band PA are measured to be 10.2 dB and 8.0 dB at 2.2 and 3.9 GHz, respectively. Figs. 4.8(c) and 4.8(d) show the two concurrent output spectra for the two bands at various maximum input powers in the opposite band. As the input power of the opposite

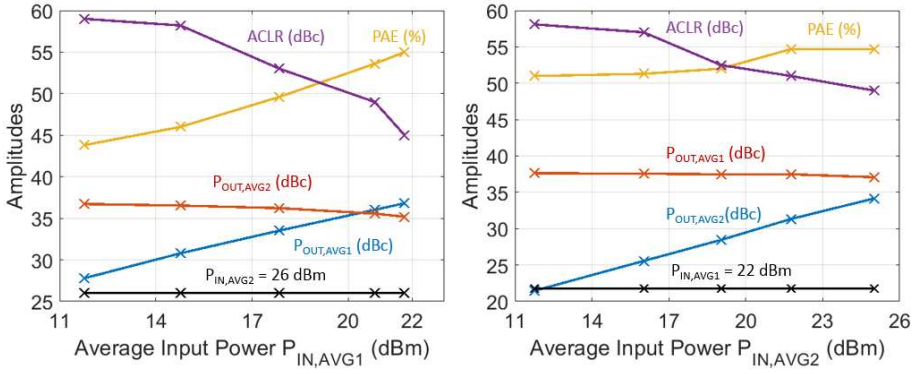


Figure 4.9: Measured performance of the dual-band PA in concurrent mode at different input powers with modulated signals and DPD. The PA efficiency peaks at about 55% for the lower (left) and higher band (right) when driven with nominal input powers $P_{in,1} = 28\,\text{dBm}$ and $P_{in,2} = 32\,\text{dBm}$. An opposite trend is observed for the ACLR metric. Note that graph axes do not correspond with the other.

band is backed-off, we observe a more confined spectrum, likely due to better linearization at lower levels of cross-modulation. As shown in the insets of these figures, the PAE is maximized at the nominal input drive (*i.e.* $P_{in,1} = 28\,\text{dBm}$ and $P_{in,2} = 32\,\text{dBm}$) and peaks at 55% while the ACLR is -42.5/ -43.3 dBc. We note that this high PAE value is mainly due to a lower PAPR of the resulting total output signal (4.42 dB at the maximum input powers). As the opposite signal power is backed-off, an efficiency degradation is observed while ACLR improves, as seen in Figs. 4.9(a) and 4.9(b). This figure also plots PAE, P_{out}, and P_{in} for both bands as a function of input power at the lower and upper bands, respectively.

These figures characterizing the concurrent performance of the PA demonstrate the effects two two signals have on one another. It is shown that applying both signals at the same time results in lower gain and higher ACLR for each as compared to their non-concurrent case. By utilizing DPD, ACLR and gain dispersion can be improved. The next sections considers a similar analysis performed on an X/Ku-band dual-band MMIC PA, with additional consideration given to IMD products.

4.2 X/Ku-Band Power Amplifier

In a phased array application, especially at increasingly high frequencies, the efficiency of each element is important because the number of elements per unit area increases. Therefore, heat dissipation is an important factor to consider, and hence, efficiency should be optimized during the design procedure. Additionally, multiple stages of amplification are typically required to achieve the necessary gain for phased array applications.

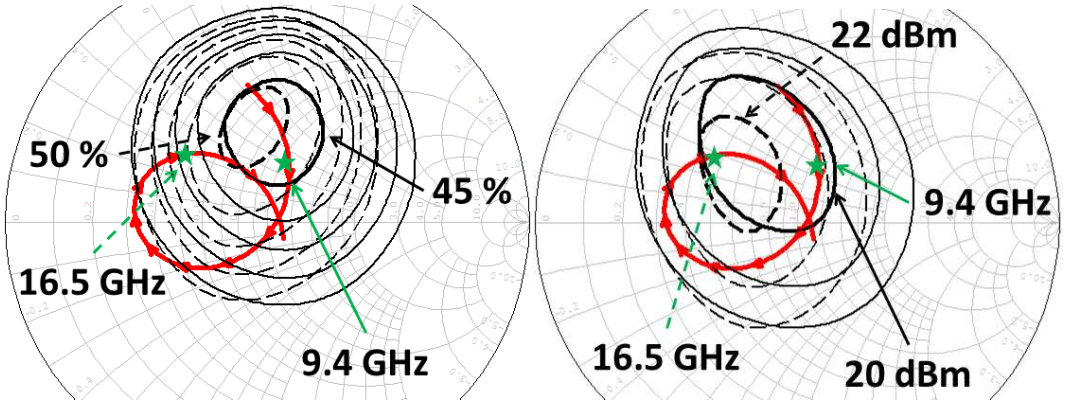
This section details the design of a two-stage X/Ku-band MMIC PA and its characterization in the non-concurrent and concurrent modes for phased array applications such as radar, which commonly operates in these bands. The goal is to scale the frequencies of the PA from the previous section, to maintain a similar f_2/f_1 ratio, in an integrated implementation. Hybrid implementations are difficult to fabricate at these higher frequencies due to limited fabrication tolerances.

4.2.1 X/Ku-Band Dual-Band MMIC PA Design

The WIN Semiconductor PIH 150-nm pHEMT enhancement-mode GaAs process is chosen in this design for its maturity and reliability. For gain, this design incorporates two stages, and the second stage is sized such that it can deliver at least P_{out} = 20 dBm (4 x 100 μm). The first stage sized for a 1:4 staging ratio (2 x 50 μm) for efficiency [58].

A deep Class-AB mode of operation (10% of I_{max}) is chosen as a trade-off between efficiency and P_{out}. In order to achieve a high-efficiency when either one or both signals are present, the IMN, ISMN, and OMN have to provide an appropriate match with low loss. Broadband and low-loss gate and drain bias tees are included in the load and source pull simulations. Fig. 4.10 shows the load-pull contours of the output stage at the two frequencies. Using the branch search algorithm of Section 3.2.3, the IMN, ISMN, and OMN are designed for the load and source-pull impedances at 9.5 and 16.5 GHz. The resulting OMN impedance is shown in red, demonstrating a poor match in the intra-band region.

Note the spacing of the power and efficiency contours and the corresponding dip in the intra-



(a) (b)

Figure 4.10: Simulated (a) PAE and (b) P_{out} load-pull contours for the output matching network, at the reference plane after the biasing network. Solid black circles are for 9.4 GHz and dashed for 16.5 GHz. Step size for PAE is 5 % and 1 dB for P_{out}. The red curve shows simulated impedances from 8 to 18 GHz presented by the output matching network, with 9.4 GHz ($\Gamma = 0.08 + j0.20$) and 16.5 GHz ($\Gamma = -0.35 + j0.25$) marked.

band region, as discussed in detail in the remainder of the paper. An analogous procedure is used for determining required impedances at the input, and between stages. The matching networks are designed using linear simulations with a topology consisting of three sections of transmission line, with a capacitive shunt element and inductive shunt element, as depicted in Fig. 4.11. Full-wave electromagnetic and harmonic-balance simulations are performed to give final circuit performance.

Stability for this PA with two widely spaced frequency bands is confirmed in multiple ways. From DC through the third harmonic, it is ensured that $K > 1$. The NI-AWR linear Nyquist stability criterion is also used. For both of these tests, the input and output terminations of the power amplifier are swept, while the bias source termination is also varied over reasonable values to account for a real supply. Next, using the foundry's nonlinear model at the chosen bias level of $V_d = 4\,V$ and $V_g = 0.45\,V$ for both stages, corresponding to a drain current of 5.54 and 21.7 mA for the first and second stage respectively, for both devices, a linear model of the transistor is extracted. With this model, g_m and C_{gd} are increased by 30 % while C_{gs} is decreased by 30 % to model a worst-case stability condition from a process variation point of view [58]. Finally, the linear model is used to perform a loop-gain analysis over port terminations and bias impedances to confirm stability; the stability networks are indicated in Fig. 4.11.

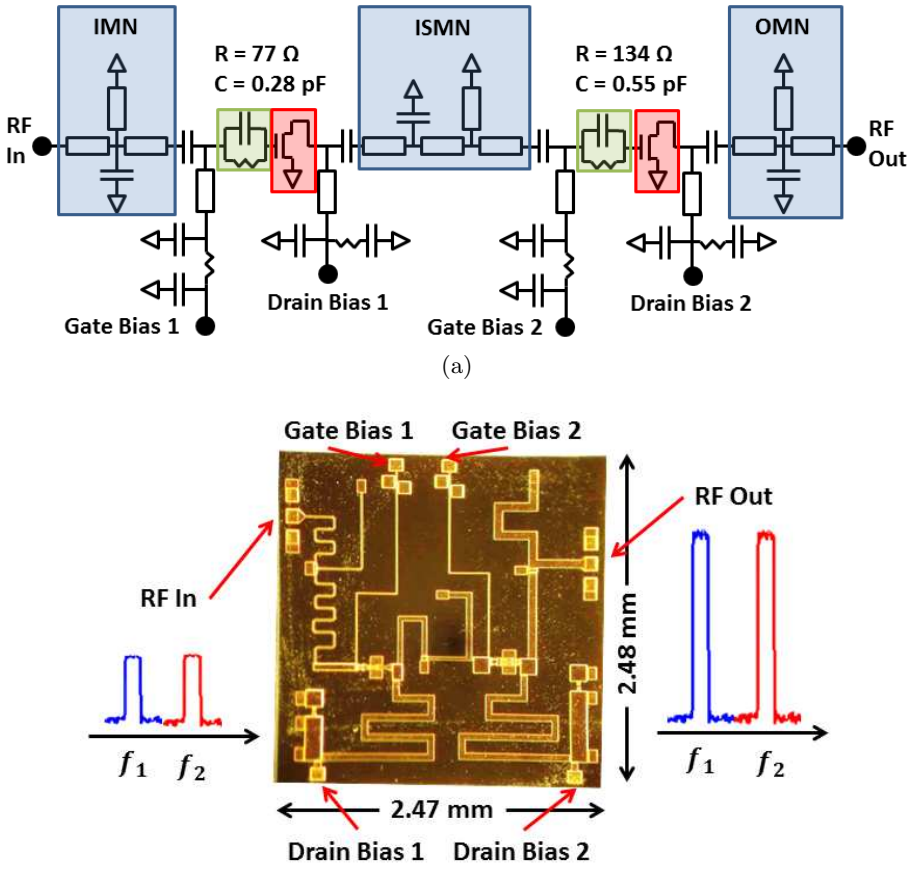


Figure 4.11: Power amplifier (a) circuit diagram and (b) MMIC photograph. The same matching network and bias topology is used throughout the circuit. Concurrent signals are input at carrier frequencies $f_1 = 9\,\text{GHz}$ and $f_2 = 16.1\,\text{GHz}$.

4.2.2 X/Ku-Band Dual-Band MMIC PA CW Characterization

An on-chip TRL kit is used with an Agilent E8364C PNA for calibration. The MMIC is mounted onto a CuMo carrier using conductive silver epoxy, with four 1 nF single-layer capacitors, and probed. Small-signal measurements are recorded and shown in Fig. 4.12. This figure also shows simulated small-signal measurements for comparison, demonstrating good agreement and a slight downward frequency shift of 400 MHz for both bands (about 4.3/ 2.4 %), likely due to matching elements, such as capacitors, being sensitive to process variations. Small-signal measurements are confirmed with a scalar setup for power measurements, by backing off the power.

The large-signal measurement frequency sweep is shown in Fig. 4.13. This shows the maxi-

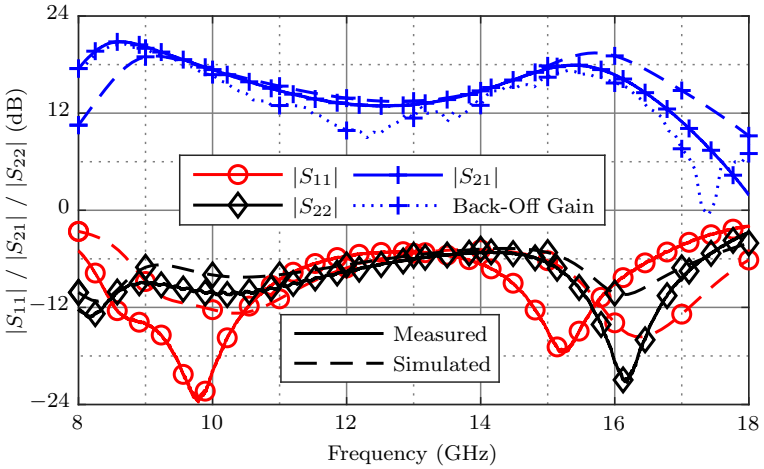


Figure 4.12: Small-signal simulated and measured S-parameters over frequency. Measurements are done with a PNA, and also with a scalar power measurement setup ("Back-Off Gain"), confirming agreement.

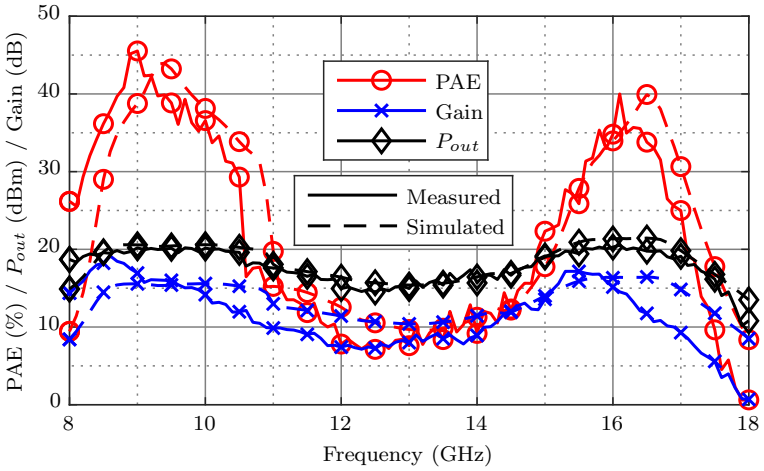


Figure 4.13: Simulated and measured CW performance of the PA over frequency. Recorded values are peak PAE with corresponding P_{out} and gain. Peak simulated/measured PAE values are observed at 9.4/9.0 and 16.5/16.1 GHz.

mum saturated power-added efficiency (PAE) at each frequency, alongside the corresponding P_{out} and gain. A power sweep is performed comparing the two frequencies with highest efficiency in both the simulated and measured cases in Fig. 4.14. A comparison to current state-of-the-art designs is given in Table. 4.2.

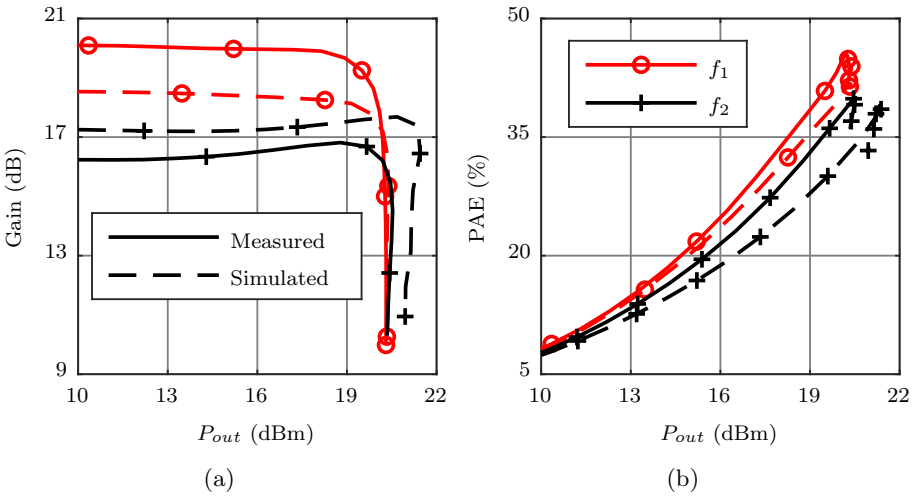


Figure 4.14: Simulated ($f_1 = 9.4\,\text{GHz}$ and $f_2 = 16.5\,\text{GHz}$) and measured ($f_1 = 9.0\,\text{GHz}$ and $f_2 = 16.1\,\text{GHz}$) CW (a) gain and (b) PAE of the PA over P_{in} for both f_1 and f_2.

Table 4.2: Summary of Dual-Band CW PA Performance

Ref.	Freq. (GHz)	PAE (%)	P_{out} (dBm)	Gain (dB)
[77]	5/12	58/51	28/26.7	9.5/7.7
[84]	7.7/14.9	24/29	34.6/34.6	11/7
[85]	6/16	55/53	26/25.5	8/7.5
[86]	29.5/47	38/40	22.5/22.7	17.5/15.5
[87]	5/12	58/51	28/26.7	N/A
This work	9/16.1	45.5/40	20.2/20.5	16.9/14.5

4.2.3 Concurrent CW Characterization at X and Ku-Bands

To measure PA performance in the concurrent mode, the power in the two bands is measured with separate power meters. A scalar test bench that accomplishes this task using power splitters and BPFs, is shown in the block diagram in Fig. 4.15.

Because 9 and 16.1 GHz are 7.1 GHz apart, two sources must be used to generate the concurrent signal. A driver is cascaded with one source to generate enough power, while harmonics are eliminated with a BPF. A calibration is performed from the probe input and the coupler output

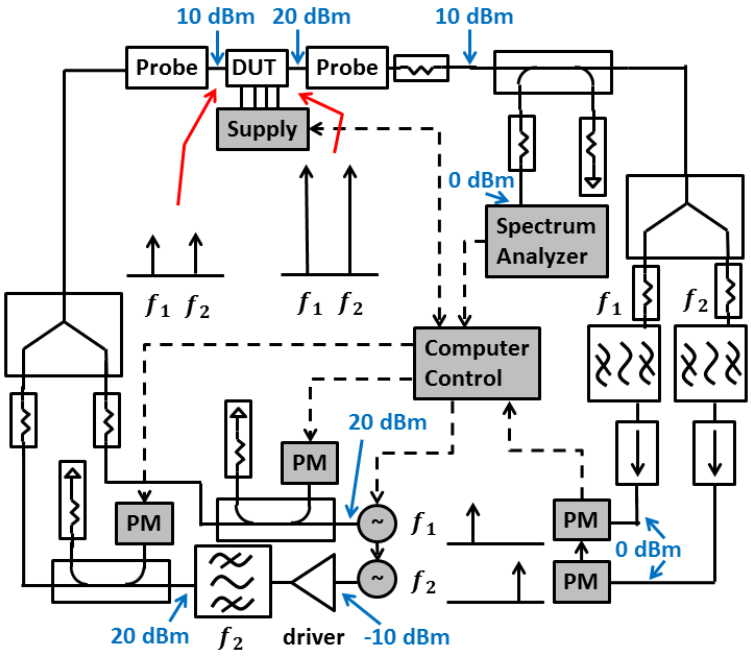


Figure 4.15: Setup block-diagram used to make concurrent CW measurements. Two sources provide tones which are each measured through a coupler. These are combined and input to the PA. The signal is then split and the two tones isolated before being measured with a power meter.

along these two paths to measure P_{in}. These CW signals are combined with a resistive power combiner and additional attenuators for matching, measured to be -15 dB or better at the input. Immediately at the output an attenuator is present to present a measured output match of -15 dB or better. The output signal is coupled to a spectrum analyzer while the thru signal is split. The split signal travels through a BPF, which has an attenuator and isolator at either end to ensure a good match, before being measured by a power meter. Because one filter operates from 8–13.9 GHz, and the other from 14.8–18.5 GHz, this setup ensures that only in-band power is measured.

The concurrent mode of operation is analyzed and results summarized in Fig. 4.16. Relative input power levels are defined from the CW $P_{in}(f)$ value corresponding to the maximum PAE(f). At f_1/f_2 this is measured as approximately 3/6 dBm. In the legend of Fig. 4.16, A and B correspond to a 6 dB back-off value while C and D correspond to the nominal $P_{in}(f)$ (0 dB back-off). When two CW tones are present, four power measurements can be made: $P_{in}(f_1)$, $P_{in}(f_2)$, $P_{out}(f_1)$, and $P_{out}(f_2)$. Therefore, a self (f_n/f_n) and cross (f_n/f_m) measurement can be defined for gain (B and D) and P_{out} (A and C) over P_{in}.

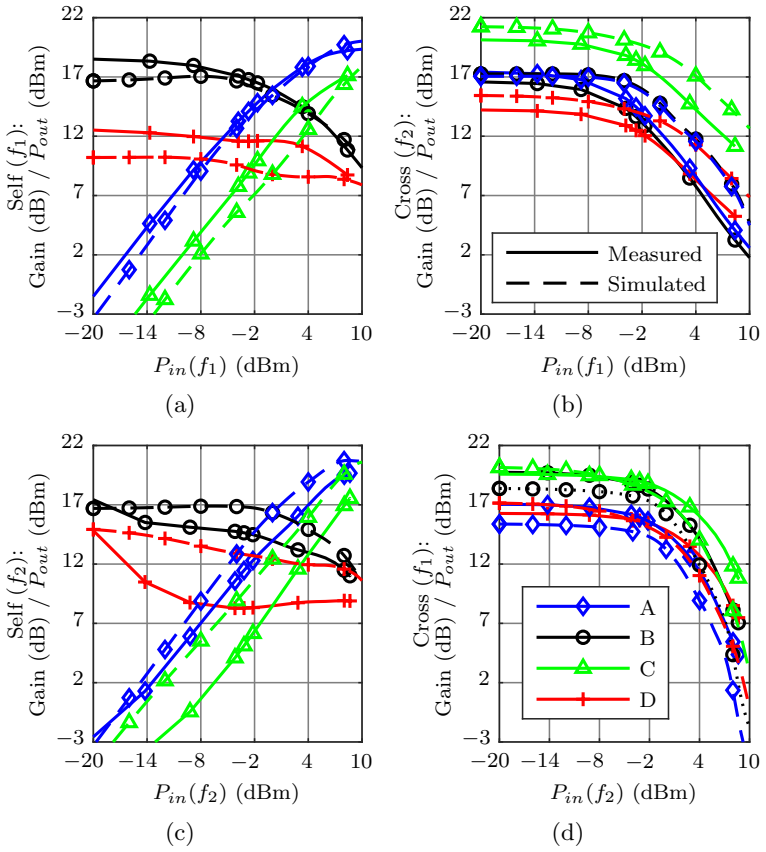


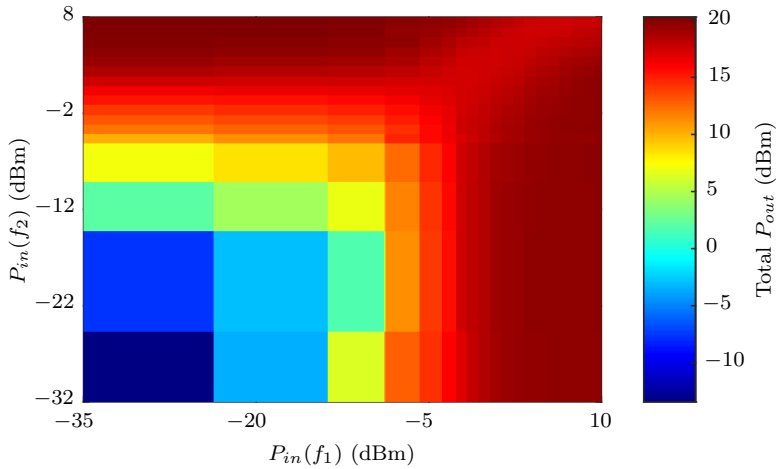
Figure 4.16: Simulated ($f_1 = 9.4\,\text{GHz}$ and $f_2 = 16.5\,\text{GHz}$) and measured ($f_1 = 9.0\,\text{GHz}$ and $f_2 = 16.1\,\text{GHz}$) concurrent mode self and cross-gain and P_{out} of the PA over several P_{in}. The legend in (d) corresponds to: A – P_{out}, 6 dB backoff; B – gain, 6 dB backoff; C – P_{out}, 0 dB backoff; and D – gain, 0 dB backoff. The top row (a) and (b) shows self results over $P_{in}(f_1)$ for a constant $P_{in}(f_2)$. Similarly, the bottom row (c) and (d) shows cross results over $P_{in}(f_2)$.

The results of Fig. 4.16 show that as cross-P_{in} increases, self-gain, self-P_{out}, and cross-gain decrease while cross-P_{out} increases. As this happens, neither signal is able to dominate in the amplification, and because the amplifier is limited in the total P_{out} it can produce, concurrent-mode gain and P_{out} must reduce accordingly. Some discrepancies between measurements and simulations may be due to the nonlinear model not correctly predicting concurrent operation.

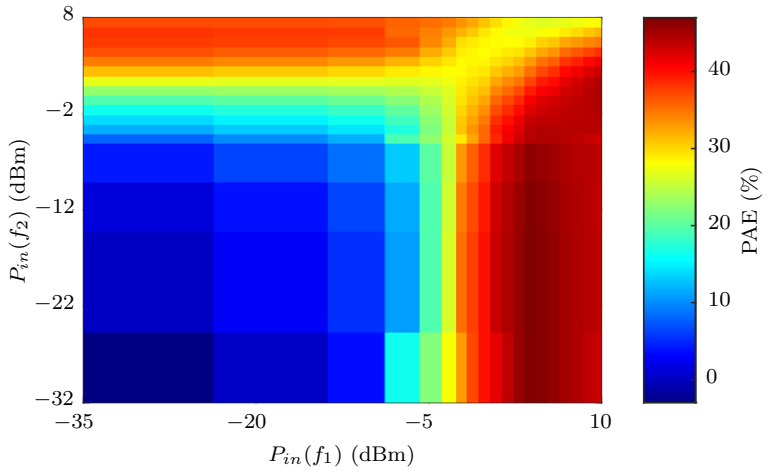
Because one cannot isolate the PAE of just one band or the other during concurrent operation, a three-dimensional figure could be used to illustrate the simultaneous effect of both bands on PAE. A similar analysis can be performed for P_{out}. Measured data is summarized as a heat map in Fig. 4.17, where PAE is defined as:

$$PAE = \frac{P_{out,1} + P_{out,2} - P_{in,1} - P_{in,2}}{P_{DC}}. \tag{4.1}$$

The heat map degenerates to the CW case at the two axes where the other band is turned off. As additional power is added in the other band, sliding away from the axis illustrates the effect on PA performance. For example, the maximum total output power and PAE decrease with simultaneous input power increase from the two bands. The heat map illustrates a saddle point in the PAE region, where P_{out} in both bands is about equal. This PAE value, however, is lower than



(a)



(b)

Figure 4.17: Heat map illustrating the measured $f_1 = 9.0\,\text{GHz}$ and $f_2 = 16.1\,\text{GHz}$ concurrent mode of operation of (a) Total P_{out} and (b) PAE over P_{in}.

the maximum value for either band in the non-concurrent mode. The corresponding saddle point in the P_{out} plot also shows a slightly lower value than in the non-concurrent mode. This saddle point corresponds to operating most strongly in the concurrent mode.

At this saddle point, with the same P_{out} in each band, the amplifier simulated and measured performance is shown in Fig. 4.18. These curves follow the ones for the non-concurrent mode. As compared to simulation, it is noted that the gain of the lower band is higher and the upper band lower, possibly due to either process variations (because the upper band sees decreased performance due to slight matching issues) or the nonlinear model not correctly predicting concurrent operation (because of the results of Fig. 4.16). In this figure at the maximum PAE point, $P_{in}(f_1)$ and $P_{in}(f_2)$ are about 5 dB lower than their respective non-concurrent values.

Using the calibrated spectrum analyzer setup of Section 5.4 to measure the fundamental, harmonic, and IMD power content of the PA output, the concurrent mode of operation is analyzed. Results for various input powers are shown in Fig. 4.19. As seen, some input power values results in positive gain for the $f_2 - f_1$ IMD product, with other values also relatively high.

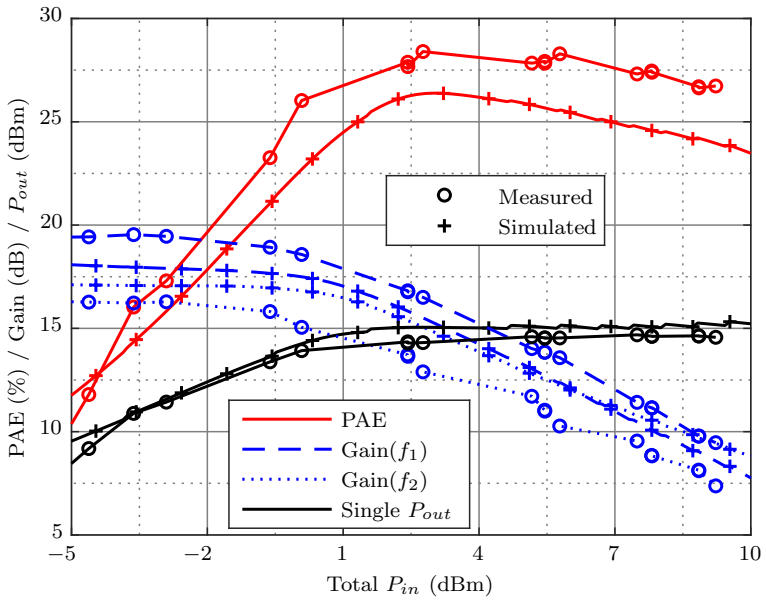


Figure 4.18: Simulated ($f_1 = 9.4$ GHz and $f_2 = 16.5$ GHz) and measured ($f_1 = 9.0$ GHz and $f_2 = 16.1$ GHz) amplifier performance when both bands output equal power.

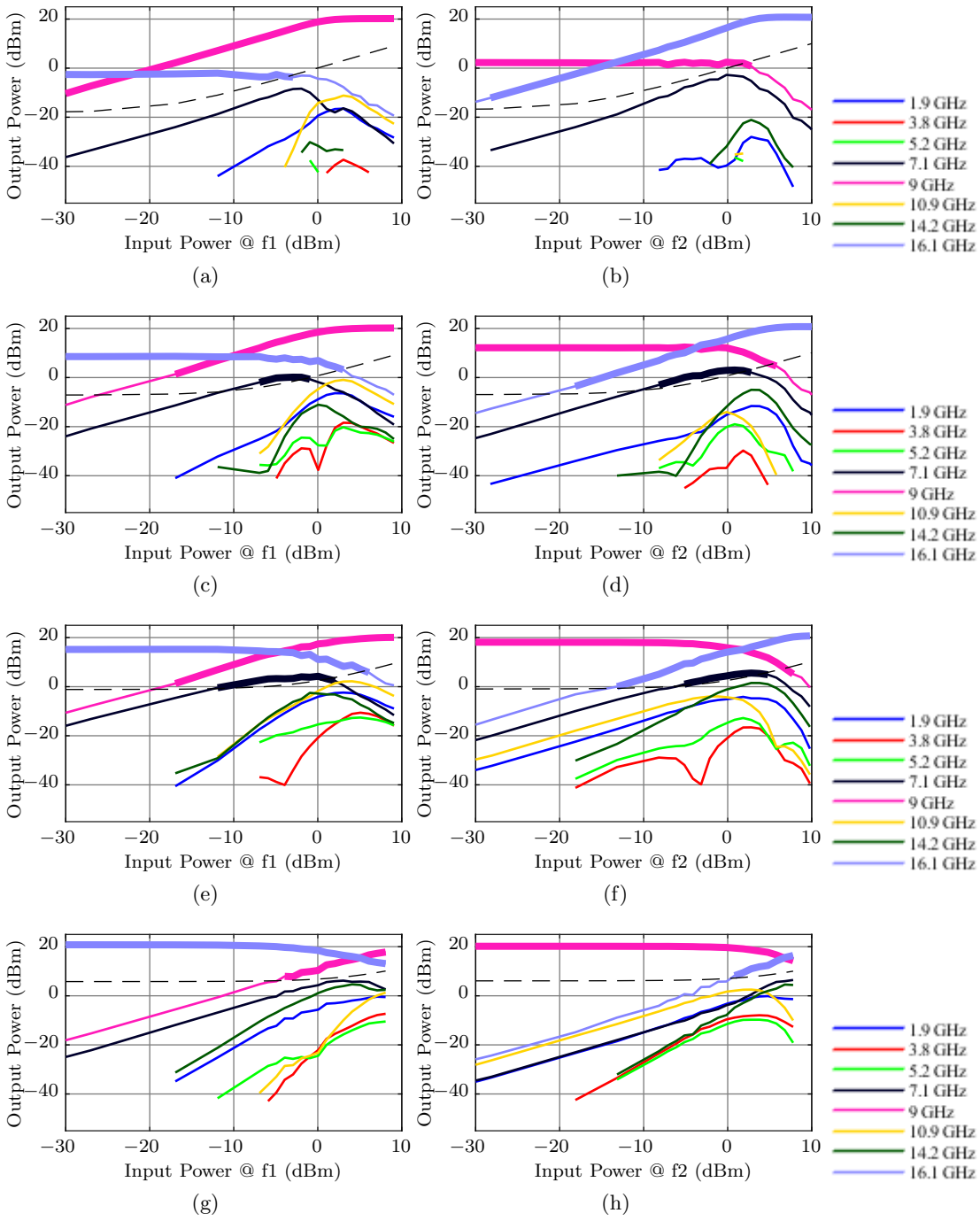


Figure 4.19: Measured concurrent CW ($f_1 = 9.0\,\text{GHz}$ and $f_2 = 16.1\,\text{GHz}$) drive-up spectra of the PA over P_{in}. The left column plots the f_1 self-measurements for constant input powers at f_2, and vice versa for the right column. The input power at either frequency are (first row) -17.6 dBm, (second) -7.0 dBm, (third) -1.0 dBm, and (fourth) 5.9 dBm. Bold lines indicate positive gain.

4.3 Conclusion

Two dual-band PAs were presented and characterized in the non-concurrent and concurrent mode of operation. Hybrid and MMIC implementations were used due to the different center frequencies of the two designs. Both characterizations demonstrated a dependence between the two frequencies in the concurrent mode, and degraded performance (gain, efficiency, output power, and linearity) as compared to the non-concurrent mode. Original contributions in this chapter include the following:

- The design and characterization of a 2.2/3.9 GHz single-stage hybrid GaN PA under non-concurrent CW and concurrent modulated signals [90].
- The design and characterization of a 9.0/16.1 GHz two-stage MMIC GaAs PA under non-concurrent and concurrent CW signals [20].

The next chapter describes two "standard" broadband PAs with similar non-concurrent and concurrent behavior. A comparison between them and another broadband PA with an alternate architecture is presented, showing that the alternate architecture significantly reduces the IMD content while maintaining performance.

Chapter 5

Broadband RF Power Amplifiers

Linear amplification of multiple signals present within a broad RF bandwidth finds many uses in radar [23, 24] and communications [25, 26] applications. For example, modern multi-band radar [27] offers advantages such as improved tracking range due to better tolerance to atmospheric effects, inherent resistance to jamming and interference, wider choice of waveforms for more accurate range and Doppler measurements, and improved target recognition with sufficient separation between bands. Communications often employ modulation schemes with carrier aggregation to increase data transfer rates [28, 29].

Two key challenges exist when amplifying such signals: (1) achieving broadband amplification with high power-added efficiency (PAE); and (2) maintaining linearity for multiple simultaneous (concurrent) signals. A well-known method of addressing these challenges is to use a bank of narrowband PAs, each designed for a different frequency range, connected through a network of switches [91–93]. This has the advantages of ease of design, fabrication, reconfigurability, isolation, and high PA efficiency. However, semiconductor switches tend to have an insertion loss of 2 - 3 dB [94, 95], while MEMS- based switches have switching speed, reliability and power handling constraints [96]. An alternative is a reconfigurable PA, *e.g.* [97, 98], which incurs loss and requires control signals for reconfiguration. The disadvantage of these two PA types is that they do not support inter-band carrier aggregation [26].

To overcome the narrow bandwidth of these two approaches broadband PAs can be designed, with commonly used architectures including the distributed, traveling-wave, feedback, and balanced

configurations [99]. The first three can achieve decades of bandwidth [100, 101], while balanced PAs achieve around an octave [102]. Single-ended PAs have been designed to cover an octave or more [3,103], using methods such as stepped impedance lines [10,104,105], transferring from F^{-1} to F modes of operation [106], or resonating output transistor capacitance [107]. Octave [3], over two octaves [73], or decade (with distributed topology) [108] bandwidth PAs have been demonstrated. More complicated topologies with multiple amplifiers include LMBA with octave bandwidth and high efficiency, [109, 110]. However, linearity of concurrent signals becomes a major concern as signal mixing occurs within the active nonlinear device, decreasing efficiency, output power, and gain, and creating IMD products which impact linearity.

A comprehensive description of broadband PAs amplifying widely-spaced concurrent signals is given in [111]. Linearization techniques using two-dimensional digital pre-distortion (DPD) algorithms have been developed [42, 112, 113] to account for signal mixing. This was applied in dual-band [90] and broadband [3] PAs and trades complexity in the RF domain for complexity in baseband. This chapter considers non-concurrent and concurrent signal amplification by broadband PAs. In particular, the above performance characteristics are compared between two types of broadband amplifier architectures: (1) a more standard single-ended design; and (2) a diplexed design for improving the linearity while maintaining high-efficiency.

5.1 Broadband Power Amplifiers

This section considers two "standard" single-ended broadband power amplifiers: (1) a 10 W S-band one-stage power amplifier; and (2) a 10Ẇ C-band two-stage power amplifier. Both are designed with similar topologies based on stepped-impedance lines.

5.1.1 S-Band Power Amplifier

The amplifier from [3] is briefly described here for completeness, with a photograph shown in Fig. 5.1. Measurement comparisons between this more "standard" broadband amplifier, and the diplexed amplifier, are shown in Section 5.4.

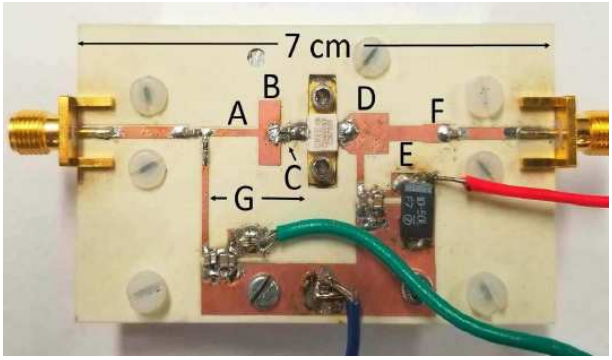


Figure 5.1: Fabricated 2–4 GHz power amplifier based on a Cree (Wolfspeed) CGH40010F GaN on SiC HEMT with stepped-impedance matching line segments of A–66 Ω, B–15 Ω, C–gate stability network, D–21 Ω, E–41 Ω, F–36 Ω, G–1.5 cm. The substrate is a 0.762 mm Rogers 4835 [3].

To design this 2–4 GHz amplifier, frequencies up to the third harmonic are simulated and terminated to improve efficiency. After performing load-pull simulations on the 10 W Cree (Wolfspeed) CGH40010F GaN on SiC HEMT transistor, short transmission line segments, used to approximate lumped elements, are used to perform a broadband match. This stepped-impedance line approach, along with constraining the number of elements on the IMN and OMN, gives a final design achieving measured $P_{out} \geq 40$ dBm and $\eta_D \geq 45\,\%$. The saturated performance over frequency is shown in Fig. 5.2, indicating agreement between measured and simulated data.

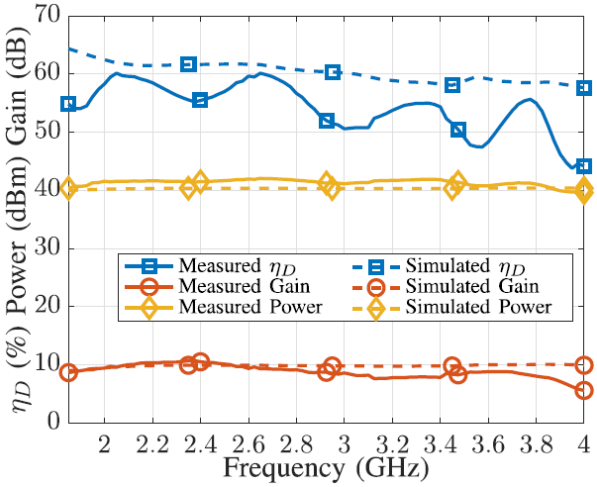


Figure 5.2: Amplifier large-signal performance at saturation over frequency depicting (solid) measured and (dashed) simulated results [3].

Communications and radar applications, however, often require significantly more gain at the RF front-end than this amplifier provides. Therefore, the non-conjugate double-matching results of Section 3.1 are utilized to demonstrate how to design a two-stage broadband power amplifier with increased gain in the next section.

5.1.2 C-Band Power Amplifier

To visualize an example solution set of Fig. 3.1, an ISMN of a two-stage C-band PA is designed. An ideal IMN for the Qorvo 6 W TGF2023-2-01 transistor (1st stage), and an OMN for the Qorvo 12 W TGF2023-2-02 transistor (2nd stage), are found with load-pull simulations. Input powers are chosen to compress the 2nd stage about 2 dB more. The resulting first-stage drain and second-stage gate Γ points across C-band are plotted in Fig. 5.3 (a), with $\Gamma_1 = 0.68\angle$-122° and $\Gamma_2 = 0.89\angle 148°$ at the 5.8 GHz (ISM band). Load/source-pull simulations indicate that $\Gamma_1' = 0.49\angle 130°$ and $\Gamma_2' = 0.88\angle$-165° result in desired PA performance at 5.8 GHz. These pairs are relatively close to, but not actual conjugate matches. Note that Γ_1' and Γ_2' non-physically rotate counterclockwise with frequency, as per Foster's reactance theorem [114].

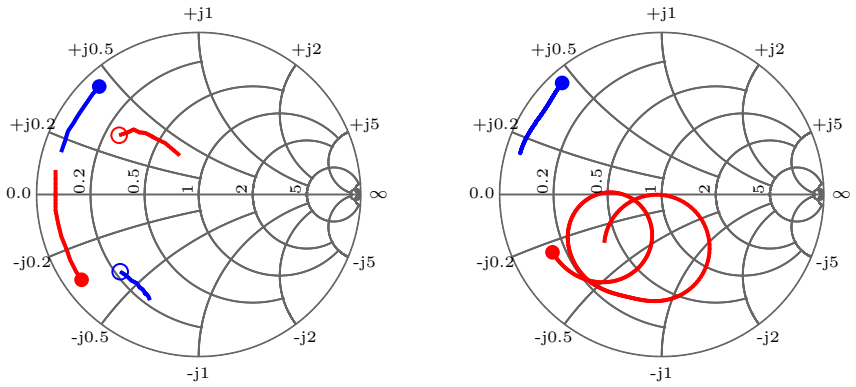


Figure 5.3: 4–8 GHz Γ trajectories (a) obtained by load-pull simulations of the transistors at the output of the 1st stage (Γ_1', open circle, red), input of the 2nd stage (Γ_2', filled circle, red) and plotted together with the drain (Γ_1, open circle, blue) and gate reflection coefficients (Γ_2, filled circle, blue) of the 1st and 2nd stages, respectively. (b) Source-pull and gate reflection coefficients of the 2nd stage in the final power amplifier design. The circles are placed at the highest frequency.

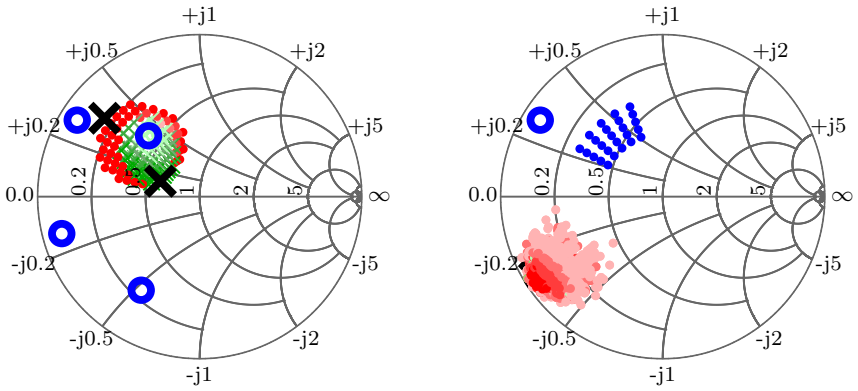


Figure 5.4: (a) Γ-prioritized solutions showing S_{11} of (green) arbitrary-phase and (red) constrained-phase passive networks at 5.8 GHz, darker shading indicating lower loss. Γ values are shown in blue circles. The lowest-loss constrained (4.8 dB) and arbitrary (6.9 dB) phase solutions are indicated by black crosses. (b) L_P-prioritized solutions showing Γ'_2 of constrained-phase solutions at 5.8 GHz, darker red shading indicating lower loss. The lowest-loss constrained (0.2 dB) and arbitrary (1.6 dB) phase solutions are nearly the conjugate of Γ_2 (blue circle). The neighborhood of considered Γ'_1 points are shown as blue dots. Only networks with $L_P \leq 4.0$ dB are shown.

To obtain a matching network design, either Γ or L_P is prioritized. For the former, **S** solutions for all exact Γ points are found. If passive solutions exist, it is possible that none have low loss. For the example PA, a discretized set of all passive Γ-prioritized **S** networks are found. The passive solution regions of S_{11} are plotted in Fig. 5.4 (a). It is interesting that the arbitrary-phase solutions are enclosed by constrained-phase ones. The L_P shading of each point demonstrates smooth contours, with the lowest-loss constrained (4.8 dB @ $0.76\angle 141°$) and arbitrary (6.9 dB @ $0.26\angle 159°$) phase **S** solutions being close to the edge of passivity, as may be expected. *These results confirm that significant loss might be present in the best solution, even if* Γ *pairs are nearly a conjugate match.*

When finding L_P-prioritized solutions **S** for the chosen $\Gamma'_{1,2}$, the other $\Gamma'_{2,1}$ is arbitrary. In the example PA, the size of the Γ'_1 neighborhood is determined from the 1st-stage load-pull contours. For each Γ'_1 point, a discretized set of all passive L_P-prioritized **S** networks are found, and for each of the $16 \cdot 10^6$ networks, Γ'_2 and L_P are calculated. The resulting Γ'_2, for passive networks, are shown in Fig. 5.4 (b). Note that the far-fewer scattered arbitrary-phase network solutions are

not plotted. Observing the solution set suggests that low-loss **S** solutions generally fall around a single peak, with only low-loss ($L_P \leq 4.0\,\text{dB}$) ISMN solutions plotted. The lowest-loss constrained (0.2 dB) and arbitrary (1.6 dB) phase **S** solutions are close to each other ($0.93\angle\text{-}148^\circ$) and to the conjugate of Γ_2.

The ISMN for the two-stage PA with L_P-prioritization is designed using the following procedure to find the **S** parameters of all MNs:

(1) Design IMN/ OMN for a single-ended PA with the 2nd-stage 12 W transistor. Find the Γ_2 gate impedance.

(2) Design IMN/ OMN for a single-ended PA with the 1st-stage 6 W transistor. Find the Γ_1 drain impedance.

(3) With the 1st-stage Γ_1' load-pull point, Γ_1 drain impedance, and 2nd-stage Γ_2 gate impedance, find the L_P-prioritized constrained-phase ISMN **S** solution.

(4) This network presents some non-conjugate (but close) impedance to the 2nd-stage gate Γ_2. Perform updated 2nd-stage load-pull simulations with the cascade to better capture appropriate 2nd-stage input power.

The load and source-pull simulations of the two transistors become dependent through the ISMN solution with the least loss. The staging ratio (here 1:2) of the transistors also plays a critical role [58]. With a smaller ratio, acceptable ISMN loss (or degraded match) can be obtained to avoid over-compressing the 2nd stage. On the other hand, a higher ratio requires a low-loss ISMN to ensure 2nd-stage saturation.

To cover a broad frequency range, and because some ISMN loss can be tolerated due to the staging ratio, the previous procedure is repeated for arbitrary-phase solutions over frequency. However, the resulting lower limit of L_P is non-physical over a broad bandwidth because Γ_1' and Γ_2' are non-physical. This result is still useful, though, in defining the best-possible center-frequency network characteristics. Broadband stepped-impedance lines [4] are used for the ISMN design and

tuned to minimize Γ_1' and L_P residuals with the arbitrary-phase networks over frequency. The approximate synthesized ISMN topology is first efficiently determined with linear circuit simulations before full-wave EM harmonic-balance simulations. The final stable C-band two-stage PA performance in Fig. 5.5 shows 20–24 dB gain, 38–42 dBm output power, and 37–56 % PAE.

Final Γ_2 and Γ_2' trajectories are shown in Fig. 5.3 (b). The large differences compared to Fig. 5.3 (a) illustrate the effect of the initial non-physical Γ_2'. The final ISMN circuit is fabricated and a photograph is shown in Fig. 5.6 (a). Measured and EM-simulated power loss curves are shown in Fig. 5.6 (b), demonstrating agreement, with differences exaggerated by non-zero Γ_2 in L_P. Increased loss at band edges is partially due to the gate mismatch seen in Fig. 5.3 (b), and due to double-matching limitations over a broad bandwidth. For comparison, the procedure is repeated for constrained-phase networks, with the power loss of both network types plotted in Fig. 5.6 (b).

The final ISMN loss is always larger than the constrained-phase minimum, but lower than the arbitrary-phase minimum over some frequency range. The maximum f_a from (3.7) of the measured (f_a=−0.73) and simulated (f_a=−0.87) ISMN show that both are of constrained-phase type over 4–8 GHz. It can further be shown that only conjugate-match solutions are lossless, while ensuring passivity for arbitrary Γ results in loss. The method can be extended to harmonics for high-efficiency PA topologies. Instead of designing a single-ended broadband PA, the next section describes how combining two relatively narrowband PAs can be used to improve performance.

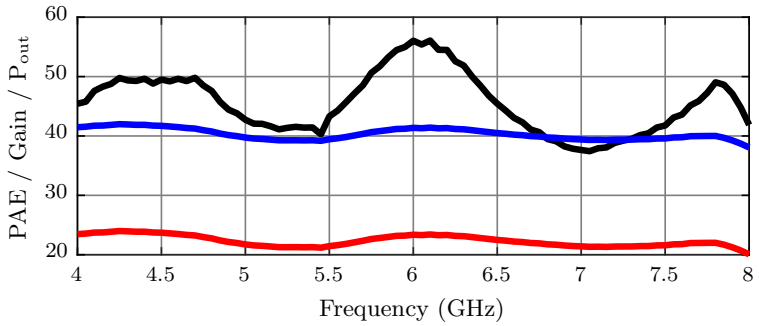
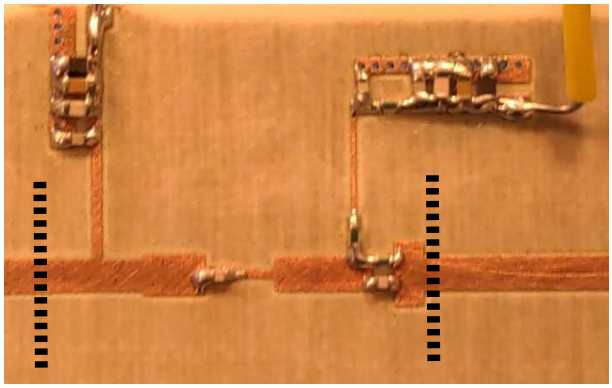
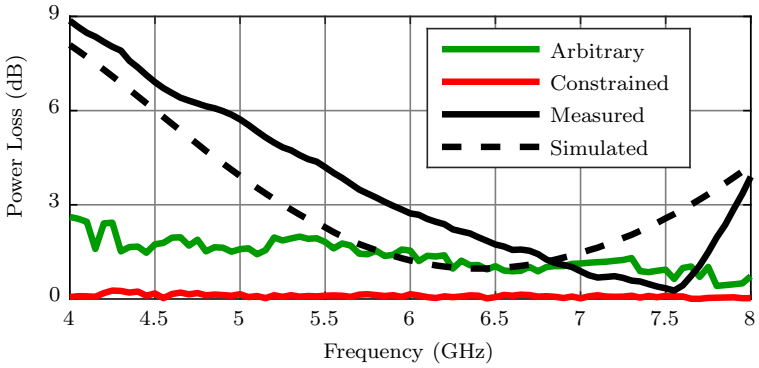


Figure 5.5: Simulated final power amplifier gain (red, dB), output power (blue, dBm), and power-added efficiency (black, %) as a function of frequency for $P_{\text{in}} = 18$ dBm. The input and output return loss are both better than 10 dB.



(a)



(b)

Figure 5.6: (a) Photograph of the fabricated inter-stage matching network on 30 mil Rogers 4305B, with dashed lines indicating TRL calibration planes. The circuit itself measures 18.5 mm × 15.5 mm. (b) Measured vs. simulated power loss of final network. Also shown are the arbitrary and constrained-phase network minimums, noting that these are only valid per frequency point and not over the bandwidth as a whole.

5.2 Diplexed Power Amplifier Architecture

An approach of combining two relatively narrowband frequency-offset PAs with correspondingly designed diplexer to maintain a wide bandwidth [4] with a single RF input/ output is illustrated in Fig. 5.7, which is in principle scalable to wider bandwidths by increasing the number of PA paths. Compared to a more standard broadband PA, this approach has the added benefit of improved linearity for concurrent signals because of the isolation introduced by the diplexers. Analog or digital pre-distortion (DPD) can still be used to further improve linearity. Compared to a switched multi-band PA, this approach has reduced active part count, and most significantly allows for amplification of multiple simultaneous widely-spaced signals.

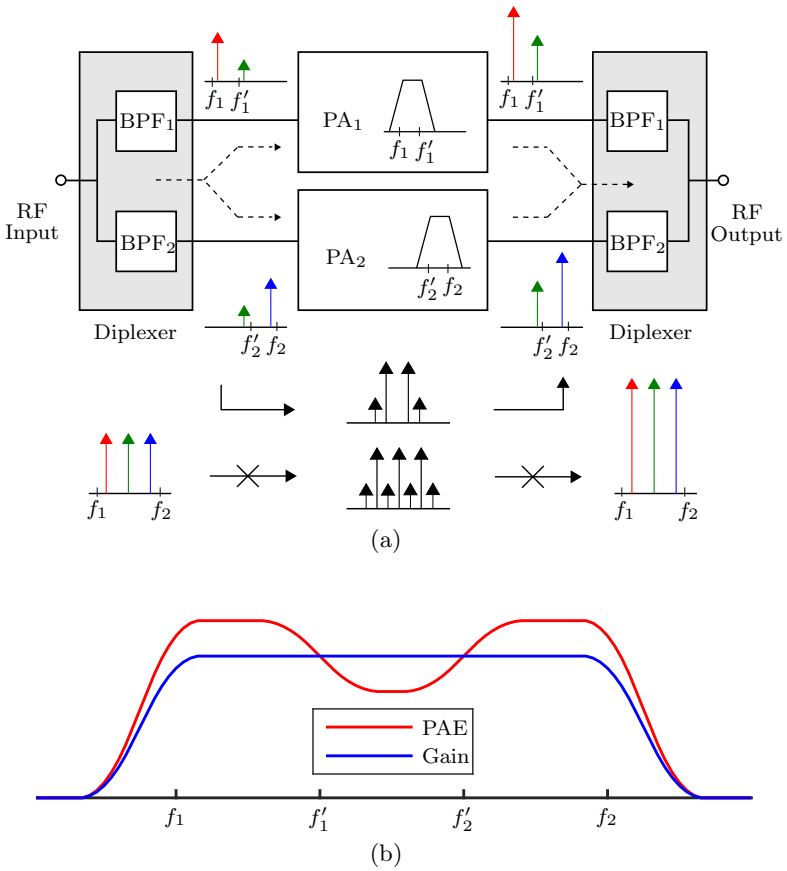


Figure 5.7: (a) Diplexing approach for broadband (f_1 to f_2) power amplifier operation. The f_1 to f_1' (BPF$_1$) and f_2' to f_2 (BPF$_2$) filters are combined to create identical diplexers at the input and output. For concurrent signals, amplifier linearity is improved, while maintaining output power and efficiency. (b) Sketch of PAE and gain over frequency for the diplexed amplifier. The output power follows the flat gain profile, characteristic of this topology.

A similar crossover technique is implemented in audio applications [115], though at much lower frequencies. Implementations at RF frequencies require different considerations, detailed in this chapter. Other related work in [116] considers a similar architecture, but does not present measured results nor considers the transition band of a diplexer with a realistic roll-off response. A systemic design process is not presented, and as a result, flat output power is not achieved through the transition band. Additional work in [117] uses a negative-component signal processor in the digital domain for splitting the two RF paths. Band splitting was also used in envelope modulators for envelope-tracking amplifiers up to 5 MHz in [118], and extended to 10 MHz [119]. This section describes the diplexing approach in detail: (1) filter design; (2) individual PA design; and (3) integration. Typically this process is iterative, as each component affects the others.

5.2.1 Filter Design

Three distinct frequency regions are considered in the diplexed design: the lower, transition, and upper bands. Considering the filter design, a diplexer is required with minimal insertion loss in the lower and upper bands, along with maintaining low combining loss and good input match throughout the transition band. The combining loss can be described by [57]:

$$IL = -10 \log \frac{|S_{12} + S_{13}|^2}{2}. \tag{5.1}$$

The diplexer with the above characteristics is referred to as a "branching" or an "invulnerable" filter [117] and can be designed with a BPF on the two branches, each having the same 3 dB cutoff frequency. Diplexer design is also influenced by PA and signal considerations. For example, if only one band is used, to prevent leakage RF power from turning on the transistor in the other branch, and thus creating undesired current draw and reducing efficiency, nulls are introduced in the out-of-band response of each branch of the diplexer to increase the isolation between the two split/ combined ports.

Two single-ended Butterworth BPF prototypes can be designed for the lower and upper bands, which also introduce transmission nulls in their out-of-band regions, and combine to create a diplexer without the need for junction compensation elements [120]. However, this implementation tends to be large. Therefore, small BPFs are designed as a shunt stub along a transmission line [121], with an additional open stub for tuning [122]. Based on a dual-band BPF response with this approach [123], the two BPFs are combined without any compensation elements.

The center frequencies are chosen as a trade-off between branch PA performances. Two intermediate frequencies f_1' and f_2' correspond to the inside edges of frequency bands B_1 and B_2 of the diplexer and the branch PAs. The lower-band PA and $|S_{21}|$ of the diplexer provide amplification from f_1 to f_1', while the upper-band PA and diplexer $|S_{31}|$ operate from f_2' to f_2. The fractional bandwidths FBW_1 and FBW_2 of the branch PAs are therefore easily defined, and for the transition band B_{tr} between them, the FBW_{tr} of f_1' to f_2' can be expressed as:

$$FBW_{tr} = 2\frac{f_2\frac{2-FBW_2}{2+FBW_2} - f_1\frac{2+FBW_1}{2-FBW_1}}{f_2\frac{2-FBW_2}{2+FBW_2} + f_1\frac{2+FBW_1}{2-FBW_1}}. \tag{5.2}$$

For $FBW_{tr} = 0$ and $FBW_1 = FBW_2 = FBW$, the greatest FBW a branch PA needs is:

$$FBW = 2\frac{(\sqrt{f_2} - \sqrt{f_1})^2}{f_2 - f_1}. \tag{5.3}$$

Though a real diplexer must have a non-zero B_{tr}, (5.3) gives a target bandwidth for each branch PA, to maintain reasonable performance in the transition band. For example, if a total octave bandwidth is desired, each PA can have $FBW \approx 34.3\,\%$, assuming $B_{tr} = 0$. As will become clear later, it is typically desired to have a low-order filter for less sensitivity at the filter edges, smaller size, and limited loss. Finally, from a layout point of view, it is simplest to design the splitting/combining ports of the diplexer to be aligned for later combination with the PAs.

5.2.2 Individual PA Design

Initially, the two PAs are designed separately at the lower and upper bands, while also targeting minimal performance degradation in the transition band. Both transistors are class-B biased because if a single narrowband signal is present in either band, overall efficiency is degraded with current draw from both transistors. Additionally, the diplexer nulls help reduce current draw due to RF leakage between the two paths.

Once the three frequency regions are chosen and a diplexer is designed, little adjustment is needed in the diplexer. However, the process of determining the frequency regions is technology-dependent and can be iterative, using considerations from the previous section as a starting point. For example, LDMOS technology could be used in the lower-frequency PA, with GaN technology implemented in the upper-frequency PA. This work considers both PAs implemented with GaN.

A primary consideration in the initial design is in-band performance, while maximizing output power in the transition band is a secondary target. However, it is not necessary to obtain the best performance in the transition band initially, since it will change once the full circuit is completed.

5.2.3 Component Integration

To derive the power gain to port 1 from port 2 of a three-port network with load Γ_i at port i, the average power delivered to port 2 of the network and power delivered to the port-1 load must be found. To begin, the port-2 input power is:

$$P_{in,2} = \frac{|V_S|^2}{8Z_0}\frac{|1-\Gamma_2|^2}{|1-\Gamma_2\Gamma_{in,2}|^2}(1-|\Gamma_{in,2}|^2), \tag{5.4}$$

where the input impedance $\Gamma_{in,2}$ can be determined as in [124]. Solving next for V_1^- from the three equations defining the scattering parameters yields:

$$V_1^- = V_2^+\frac{S_{12}+A\Gamma_3}{1-S_{11}\Gamma_1+B\Gamma_3}, \tag{5.5a}$$

$$A = S_{13}S_{32} - S_{12}S_{33}, \tag{5.5b}$$

$$B = -S_{33} + \Gamma_1(S_{11}S_{33} - S_{13}S_{31}), \tag{5.5c}$$

$$V_2^+ = \frac{V_S}{2}\frac{1-\Gamma_2}{1-\Gamma_2\Gamma_{in,2}}. \tag{5.5d}$$

Equations (5.5) can be inserted into the equation for power delivered to port 1,

$$P_{L,1} = \frac{|V_1^-|^2}{2Z_0}(1-|\Gamma_1|^2), \tag{5.6}$$

resulting in an expression for the the power gain between ports 2 and 1:

$$G_{P,12} = \frac{P_{L,1}}{P_{in,2}} = \frac{1-|\Gamma_1|^2}{1-|\Gamma_{in,2}|^2}\frac{|S_{12}+A\Gamma_3|^2}{|1-S_{11}\Gamma_1+B\Gamma_3|^2}. \tag{5.7}$$

Consider two PAs, with attributes $P_{out,n}$, $P_{in,n}$, and $P_{DC,n}$ for $n=[1,2]$, connected to the combining ports two and three of an output diplexer. Let $\Gamma_1=0$ to represent the system load, and let Γ_2 and Γ_3 represent the output impedances of the PAs. Therefore:

$$G_{P,12} = \frac{|S_{12}+\Gamma_3(S_{13}S_{32}-S_{12}S_{33})|^2}{(1-|\Gamma_{in,2}|^2)|1-S_{33}\Gamma_3|^2}, \tag{5.8}$$

$$\Gamma_{in,2} = S_{22} + \frac{S_{23}S_{32}\Gamma_3}{1 - S_{33}\Gamma_3}. \tag{5.9}$$

and similarly for $G_{P,13}$. The overall output power is:

$$P'_{out} = P_{out,1}G_{P,12} + P_{out,2}G_{P,13}. \tag{5.10}$$

Similarly, the PAs can be connected at the input with an input diplexer at ports two and three, resulting in an overall input power of:

$$P'_{in} = \frac{P_{in,1}}{G_{P,21}} = \frac{P_{in,2}}{G_{P,31}}, \tag{5.11}$$

noting that $G_{P,ij} = G_{P,ji}$ as both diplexers are identical and reciprocal. Transducer gain is not used in this case because it is nearly identical to power gain, as the input of the diplexer should be well-matched over both frequency bands and the $\Gamma_{in,1}$ term of the equivalent form of (5.7) for the input diplexer is close to zero.

The dc component of the drain current $I_{D,n}$ of a PA can be modeled as a function of the input power:

$$I_{D,n} = f_n(P_{in,n}). \tag{5.12}$$

Assuming that functions f_n for the PAs are known, (5.11) and (5.12) can be used to determine the drain current $I'_{D,1}$ within the full circuit as:

$$I'_{D,1} = f_1(P'_{in} \cdot G_{P,21}), \tag{5.13}$$

and similarly for $I'_{D,2}$. Therefore, with a shared drain voltage supply V_{DD}, the overall PAE can now be defined as:

$$PAE = 100\frac{P'_{out} - P'_{in}}{V_{DD}(I'_{D,1} + I'_{D,2})}[\%], \tag{5.14}$$

which is valid for all frequency bands of the full PA. Depending on the out-of-band performance of G_P, significant additional drain current could be drawn, lowering PAE. To demonstrate the effect of proper insertion loss and biasing with a single CW signal in the lower band, assume $G_{P,12} = G_{P,13} = |S_{21}|^2 = |S_{31}|^2 = 0.9$ (0.9 dB insertion loss), $P_{out,1} = 10\,\text{W}$, $P_{out,2} = 0\,\text{W}$, $P_{in,1} = 1\,\text{W}$, $P_{in,2} = 0\,\text{W}$, and $P_{DC,1} = 18\,\text{W}$, so that the one branch PA has 50 % PAE and 10 dB gain. For a 28 V shared drain bias, (5.14) becomes:

$$PAE = 100\frac{7.89}{18 + 28I_{drain,2}}[\%]. \tag{5.15}$$

Starting with a 50 % baseline PAE, the full PA has an overall gain of 9.1 dB and 43.8 % PAE if class-B biased with perfect diplexer isolation. If biased in class-AB with 100 mA drain current, the overall PAE degrades further to 37.9 %. With no insertion loss and only 10 mA current draw, the gain remains 10 dB but PAE degrades to 49.2 %. Qualitatively, this suggests that insertion loss is most relevant, while proper biasing and diplexer nulls still play an important role in maintaining PAE.

With an ideal diplexer, considering just the lower band, $S_{13} = S_{31} = 0$. Therefore, (5.8) can be simplified to:

$$G_{P,12} = \frac{|S_{12}|^2}{1 - |\Gamma_{in,2}|^2}. \tag{5.16}$$

Furthermore, an ideal diplexer also has $S_{22} = 0$ and $S_{23} = 0$ in the lower band, resulting in $|\Gamma_{in,2}|^2 = 0$. This leads to $G_P = |S_{12}|^2$. Similarly in the upper band, $G_P = |S_{13}|^2$, and so the assumptions previously made hold true, *regardless of the output impedance of either PA*. However, in the transition band, G_P is affected by the output impedance of each PA. Therefore, by ensuring the output match of each PA is low, insertion loss can be minimized.

For a flat overall output power over the lower or upper band, the individual PAs must have a corresponding flat output power. However, in the transition band, there is additional flexibility. Considering (5.10) as a function over frequency, to maintain a flat response over all frequency

bands, its derivative must be zero:

$$\frac{\partial P'_{out}}{\partial f} = P_{out,1}\frac{\partial G_{P,12}}{\partial f} + \frac{\partial P_{out,1}}{\partial f}G_{P,12} + P_{out,2}\frac{\partial G_{P,13}}{\partial f} + \frac{\partial P_{out,2}}{\partial f}G_{P,13} = 0. \tag{5.17}$$

If both PAs have equal and flat output powers in the transition band, in addition to their respective bands, (5.17) becomes:

$$\frac{\partial G_{P,12}}{\partial f} = -\frac{\partial G_{P,13}}{\partial f}, \tag{5.18}$$

which is true for a symmetric diplexer. However, this difficult PA requirement is not necessary because G_P in (5.8) is a function of the output impedance of each PA. Therefore, that output impedance can be used as a tuning variable in (5.17) to maintain flat output power in the transition band without requiring a flat individual PA response. This result is one of the differences between this work and that of [117], where additional signal pre-processing is required at the PA input.

5.3 S-Band Diplexed Power Amplifier

A center frequency of 2.9 GHz is chosen for this design with the goal of maximizing bandwidth. The 7 W Qorvo T2G-6000528-Q3 GaN packaged device, which operates from dc to 6 GHz, is selected with $P_{out} = 38$ dBm. The transistor is mounted on an aluminum heat-sink and the PCB is fabricated on a 0.762 mm thick Rogers 4350B substrate, with the final PA shown in Fig. 5.8.

5.3.1 Diplexer Design

For the design of the input and output diplexer divider/combiner, BPFs are first designed with center frequencies of 2.1 and 3.6 GHz, found as geometric means between band edges and the center frequency. As the theory in Section 5.2.1 indicates, shunt short and open stubs are used for filtering and tuning, respectively. Combined, these form an initial diplexer design, where the open stub is tuned to maintain low reflection and combining loss across $f_1 = 1.6$ GHz to $f_2 = 4.3$ GHz.

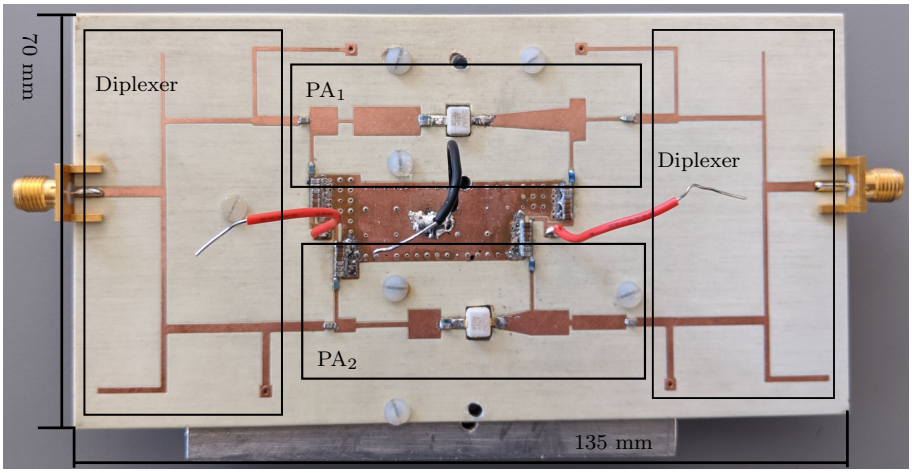


Figure 5.8: Fabricated hybrid power amplifier on a 0.762 mm thick Rogers 4350B substrate operating from 1.8 to 4 GHz [4].

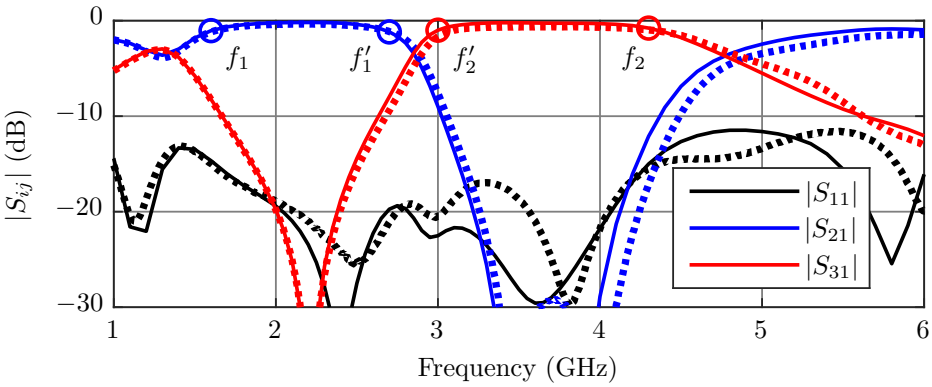


Figure 5.9: Microstrip diplexer (solid) electromagnetically simulated and (dotted) measured results. The same diplexer is used to combine the two branch power amplifiers. Frequencies f_1, f_1' and f_2', f_2 used in the design process to obtain match in the transition band are labeled [4].

After iterating with the PAs, the final diplexer has $|S_{21}|$ covering $f_1 = 1.6\,\text{GHz}$ to $f_1' = 2.7\,\text{GHz}$ of B_1, while $|S_{31}|$ covers $f_2' = 3\,\text{GHz}$ to $f_2 = 4.3\,\text{GHz}$ of B_2. A photo of the fabricated diplexer within the full PA is shown in Fig. 5.8. The passive sub-circuit was measured separately and the results are plotted in Fig. 5.9. The diplexer maintains a measured insertion loss of 0.36–1.43 dB and better than a 15 dB reflection loss from f_1 to f_2. From frequencies where the insertion loss is 1 dB above the minimum loss in each band, the transition band of the diplexer is between $f_1' = 2.7\,\text{GHz}$ and $f_2' = 3\,\text{GHz}$.

5.3.2 Individual PA Design

While operating in one of the pass-bands B_1 or B_2, ideally, the other transistor will be turned off so that it does not draw power, keeping overall efficiency similar to that of a single-ended PA. Therefore, the transistors are biased near pinch-off in class B at 0.1 % of I_{max}, where V_{gate} = -3 V, with an associated minimal (0.3 percentage point) reduction in power-added efficiency (PAE) due to the other transistor's current draw.

Using stepped impedance lines, two 50-Ω element PAs operating in the pass-bands $B_1 = 1.8 - 2.8$ GHz and $B_2 = 2.8 - 4$ GHz are designed. Modelithics models are used for each of the lumped and active components. The transistor is simulated with a 0.17 nH source inductance and 0.8 Ω source resistance to account for mounting parasitics. Harmonic-balance and full-wave electromagnetic simulations are performed, with simulated and measured results in Fig. 5.10 for the two bands. Note that the gate bias had to be reduced to -3.4 V/ 0.4 mA from the nominal -3 V/ 3.6 mA predicted by the nonlinear model, to exhibit a class-B gain. The two PAs maintain an average measured PAE over their respective bands of 55.3/ 49.4 % with an average output power and gain of 37.2/ 38.5 dBm and 10.0/ 8.9 dB, respectively.

5.3.3 Full PA Design

The two RF paths are split and combined with the same diplexer designed for 50-Ω ports. Corresponding bias lines from the two individual PAs are connected together for a single gate, and a single drain, dc bias connection point. The following procedure is used for the full PA design:

A. Design the two branch PAs with around 30% fractional bandwidths. In the implemented circuit, the lower-band PA covers $f_1 = 1.8$ GHz to $f_1' = 2.8$ GHz of B_1, while the upper-band PA covers $f_2' = 2.8$ GHz to $f_2 = 4$ GHz of B_2. The matching networks are designed as stepped-impedance lines [3] for the load-pulled impedances, and harmonics terminated approximately in an open impedance to improve efficiency. The transistors are biased near pinch-off in class-B at 0.1 % of I_{max}, where V_{gate} = -3 V, with an associated minimal (0.3

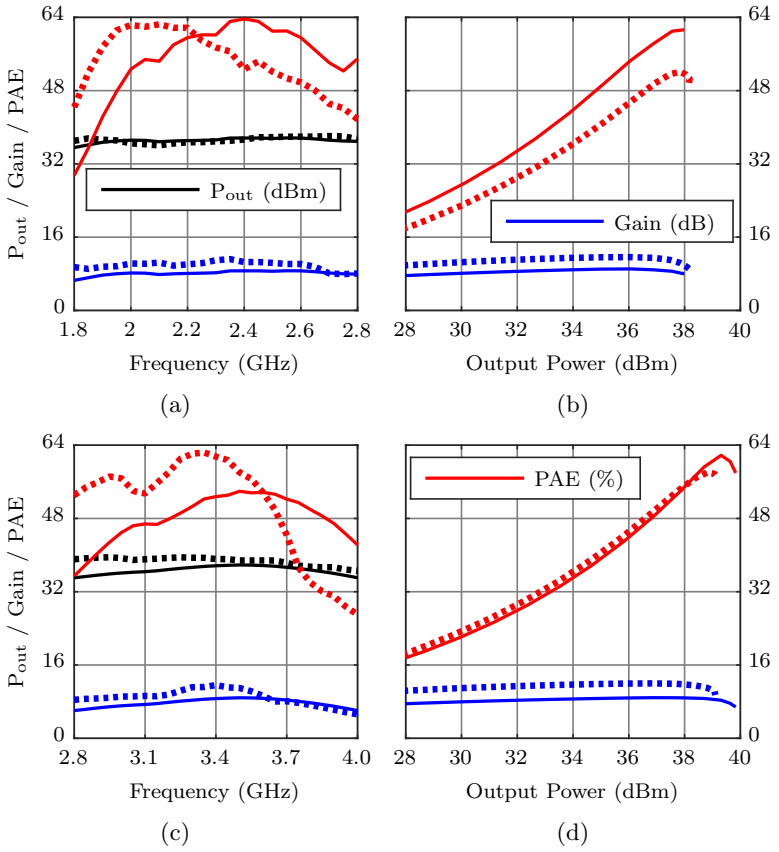


Figure 5.10: Lower (a, b) and upper-band (c, d) power amplifier simulated (solid) and measured (dotted) large-signal parameters, where (b) is measured at 2.5 GHz and (d) at 3.5 GHz. Both amplifiers are biased at -3.4 V/ 0.4 mA.

percentage point) reduction in PAE due to the other transistor's current draw.

B. Perform the diplexer layout so that the two combining ports are aligned and spaced appropriately to fit the PAs.

C. Adjust the PA designs to account for the layout of the diplexer. Modelithics models are used for each of the lumped and active components. The transistor is simulated with a 0.17 nH source inductance and 0.8 Ω source resistance to account for mounting parasitics. Perform the layout of the PAs including full-wave electromagnetic (EM) simulations.

D. Perform full-wave simulations of the final diplexer.

E. Perform full-wave simulations and tuning of the final matching networks.

Measurement and simulation results for the final PA are shown in Fig. 5.11. Averaged over the band, an average measured PAE of 43.7 % and corresponding average output power and gain of 38 dBm and 8.8 dB, respectively, are achieved. Measured large-signal results in Figs. 5.12 and 5.13 compare the performance of the branch PAs with that of the full circuit. The two PAs maintain an average measured PAE, over their respective bands, of 55.3/ 49.4 % with an average output power and gain of 37.2. 38.5 dBm and 10.0/ 8.9 dB, respectively. Note that the gate bias had to be reduced to -3.3 V/ 2.3 mA from -3 V/ 7.2 mA predicted by the non-linear device model, to maintain class-B operation. Because each element PA has PAE maximized within its corresponding band, there is a degradation in performance out-of-band, contributing to the drop in efficiency between B_1 and B_2. One could design the element PAs to be more efficient in the transition region with flat PAE, but maximal efficiency would drop. The relationship between the contiguous diplexers and element PAs is chosen to maintain constant gain and output power across the band.

As expected, the maximum output power of the full circuit is slightly less than that of the branch PAs due to the combining loss of the diplexer. This loss also contributes to the degradation in PAE. The measured PAE of the full PA, averaged over the band, is 43.7 % and the corresponding average output power and gain are 38 dBm and 8.8 dB, respectively. Because each branch PA has

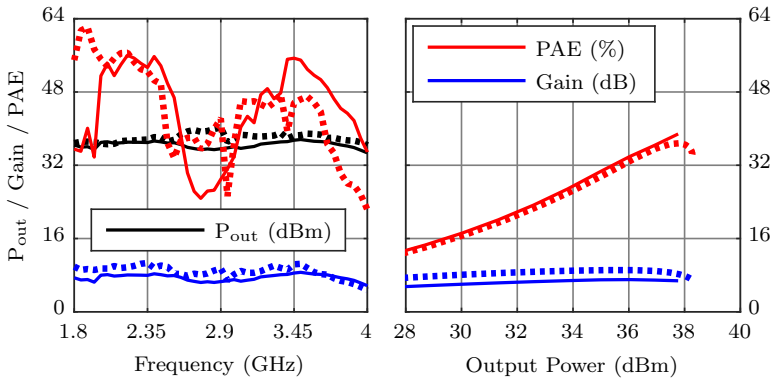


Figure 5.11: Simulated (solid) and measured (dotted) large-signal parameters over frequency (a) and power at 3 GHz (b) of the full circuit depicted in Fig. 5.7(b). The power amplifier is biased at -3.3 V/ 2.3 mA.

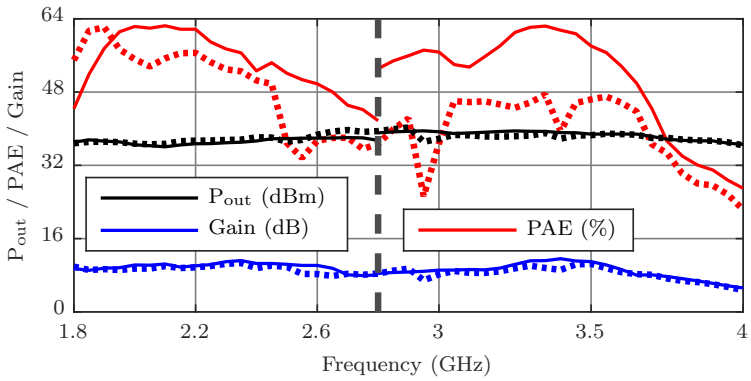


Figure 5.12: Measured (solid) lower and upper-band, alongside (dashed) full, power amplifier large-signal saturated performance. All amplifiers are class-B biased.

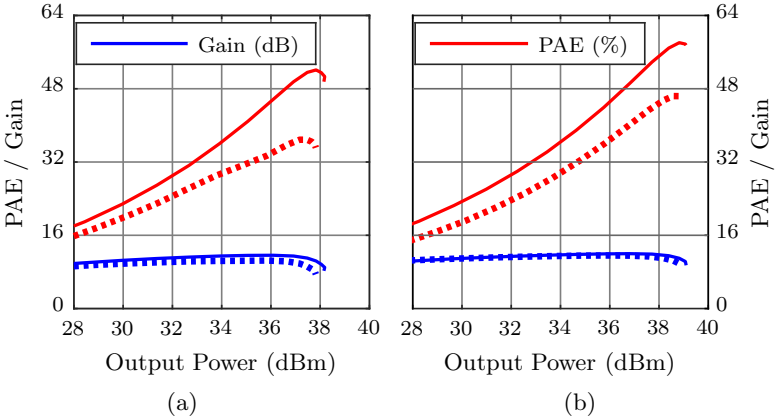


Figure 5.13: Measured (left, solid) lower and (right, solid) upper-band, alongside (both, dashed) full, power amplifier drive-up performance at 2.5 and 3.5 GHz, respectively. All amplifiers are class-B biased.

PAE maximized within its corresponding band, there is a degradation in out-of-band performance, contributing to the drop in efficiency between B_1 and B_2. The relationship between the contiguous diplexers and branch PAs is chosen to maintain constant gain and output power across the band, per (5.17). An alternative trade-off design is with the branch PAs more efficient in the transition region with flat PAE, at the expense of maximal efficiency, as suggested by the Bode-Fano criterion discussion in Section 3.2.1.

Table 5.1 compares this work to similar broadband PAs. Although nonlinear simulations predict measurement trends, a frequency shift between the two contributes to performance degradation.

Table 5.1: Summary of Broadband CW PA Performance

Ref.	Freq. (GHz)	PAE (%)	P_{out} (dBm)	Gain (dB)
[104]	2–4	48–62	40–42	9–10
[10]	1.9–4.2	40–61	40–40.8	11–12
[105]	0.85–5.4	45–55	43.5–45	8–9.5
[106]	1.3–3.3	55–78	40–40.4	10–13
[107]	1.9–4.3	48–62	40–41.8	9–11
This work	1.8–4	22.3–62	36.4–40.3	4.7–10.7

Some possible reasons, resulting from previous experience with this device, include degradation of the device at higher frequencies and manufacturing tolerances. Additionally, the operating point is in class B, whereas most transistor nonlinear models are validated for class A or AB, and therefore some disagreement is expected.

For a fair comparison, a broadband PA is designed with the same Qorvo transistor and same bias, following closely that in [104], with simple device replacement. Comparisons between the diplexed and broadband PA full-wave electromagnetic simulations show that average values of PAE, output power, and gain are 48/49 %, 39/39 dBm, 8/8 dB. This suggests linearity can be improved without sacrificing performance as compared to a standard broadband PA.

5.3.4 Concurrent Modulated Signal Characterization

The non-linearity seen in Fig. 5.11 will result in spectral regrowth when a modulated signal is amplified. To correct this, simple digital pre-distortion (DPD) can be implemented by using a 1-D memory polynomial model (1.9). Additional distortion of concurrent signals is introduced due to intermodulation between the two bands. When a single-ended broadband PA amplifies concurrent signals, this cross-modulation distortion can be corrected using a more complex 2-D memory polynomial model [42]:

$$
\begin{aligned}
z_1(n) &= \sum_{m=0}^{M}\sum_{i=0}^{K}\sum_{j=0}^{i} c_{1,mij}x_1(n-m) \\
&\quad \times |x_1(n-m)|^{i-j}|x_2(n-m)|^{j} \\
z_2(n) &= \sum_{m=0}^{M}\sum_{i=0}^{K}\sum_{j=0}^{i} c_{2,mij}x_2(n-m) \\
&\quad \times |x_2(n-m)|^{i-j}|x_1(n-m)|^{j}.
\end{aligned}
\tag{5.19}
$$

where the two baseband outputs, $z_1(n)$ and $z_2(n)$, of the predistorters are separately computed by two equations for inputs $x_1(n)$ and $x_2(n)$. The digital complexity of the resulting 2-D memory polynomial in (5.19) scales as $N \times N = N^2$ [42]. The quadratic dependence can generate large memory requirements in the digital baseband, making the 2-D model less attractive.

The goal of the diplexed architecture is to inherently reduce concurrent signal cross-modulation distortion in the RF domain with diplexers, and so the 2-D DPD model cannot be used. However, DPD with a 1-D memory polynomial model can be used in baseband to further reduce signal distortion. We separately model the two branches with 1-D memory polynomials, thus reducing the digital memory complexity from N^2 to $2N$, making practical implementations simpler.

This method is validated experimentally. A 5G-like signal is generated in MATLAB, consisting of a 5 MHz bandwidth, 20 frames, 30 kHz sub-carrier spacing, 132 sub-carriers, 256 FFT length, oversampling rate of 7, and a cyclic prefix length of 18. A random bitstream is modulated onto 64 QAM symbols to generate this OFDM signal, which is low-pass digitally filtered. Two such uncorrelated signals are upconverted to 2.5 and 3.5 GHz carriers with two triggered VSTs (NI PXIe-5645, 80 MHz and NI PXIe-5646, 200 MHz), sampled at 53.76 Ms/sec.

After a circulator in each path, the outputs of the VSTs are combined and amplified by a broadband linear instrumentation driver amplifier (MiniCircuits ZHL-16W-43). The input path is calibrated to the output of the driver, where the DUT is attached. The output path is power calibrated from the DUT, through an attenuator and coupler to a spectrum analyzer, followed by a splitter to the downconverters in the VSTs. The measured gain dispersion of two signals for the diplexed PA is plotted in Fig. 5.14. Center frequencies are chosen, as before, at 2.5 and 3.5 GHz. Both signals are generated to have peak powers of about 30 dBm at the DUT input calibration

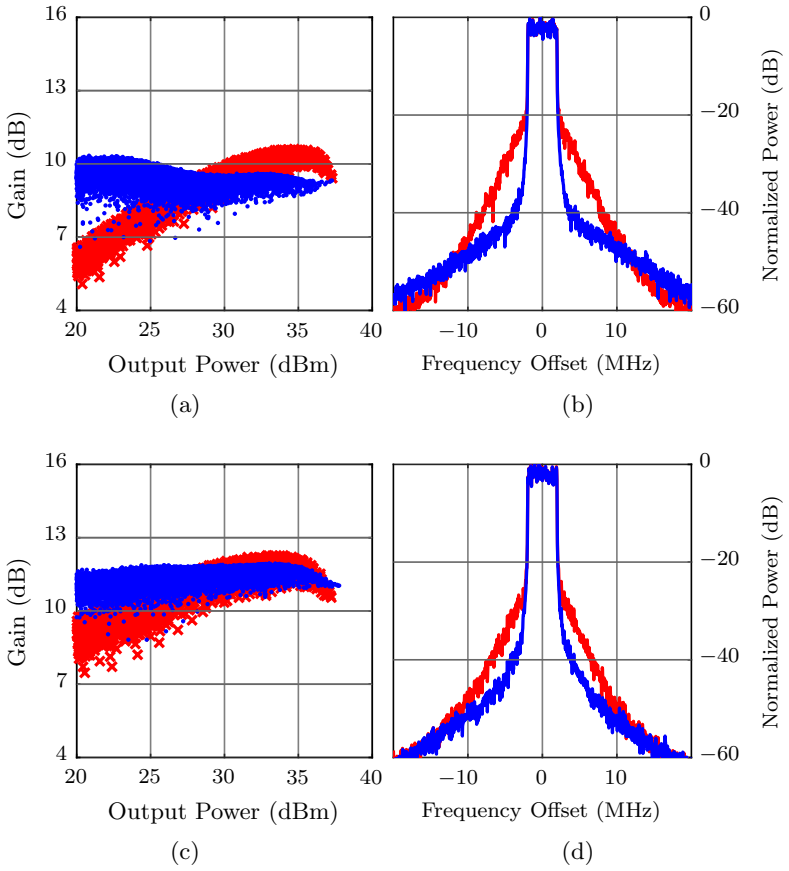


Figure 5.14: Measured (left) gain dispersion and (right) output spectra for the class-B biased diplexed power amplifier (red) before and (blue) after digital pre-distortion. The top row plots 2.5 GHz while the bottom row plots 3.5 GHz. The amplifier is fed with two 5G-like modulated 5 MHz multitone signals with individual peak power and PAPR values of 28/ 26.8 dBm and 10.0/ 9.8 dB at 2.5 and 3.5 GHz, respectively, corresponding to total peak input power and PAPR values of 30.5 dBm and 10.6 dB.

point. After time-aligning the output signal, the gain dispersion is obtained. Also from this data, the frequency spectra is calculated by applying an FFT function, the results of which are also plotted in Fig. 5.14, demonstrating spectral regrowth.

To linearize the diplexed PA, a 1-D memory polynomial is found with a similar 5G-like test signal consisting of 10 frames [42]. The chosen memory polynomial has a memory length of 3 and non-linearity order of 6 for all measurements to give the lowest adjacent-channel power ratio (ACPR) values. The original 20-frame 5G-like signals are digitally pre-distorted using the measured memory polynomial to produce new gain dispersion and frequency spectra output in

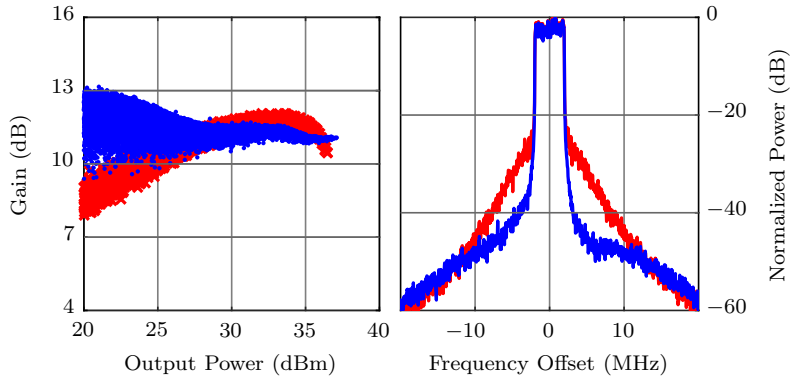


Figure 5.15: Measured (a) gain dispersion and (b) output spectra for the class-B biased diplexed power amplifier (red) before and (blue) after digital pre-distortion. A center frequency of 3.0 GHz is chosen to operate in the transition band with an input non-concurrent 5G-like modulated 5 MHz multitone signal with peak power and PAPR values of 26.1 dBm and 9.1 dB, respectively.

Fig. 5.14. These results demonstrate a lower/upper ACPR improvement with DPD at 2.5 GHz from -23.4/ -24.2 to -34.5/ -34.0 dB and an EVM improvement from 17.7 to 3.7 %. At 3.5 GHz, there is a lower/upper ACPR improvement from -28.0/ -28.2 to -34.2/ -34.3 dB and an EVM improvement from 9.7 to 3.6 %. The BER is zero with DPD in both cases.

PA performance in the transition region is confirmed with a similar non-concurrent modulated 5G-like signal centered at 3 GHz. Gain dispersion and frequency spectra of the corresponding output is shown in Fig. 5.15. These results demonstrate a lower/upper ACPR improvement with DPD from -26.1/ -26.4 to -34.8/ -36.2 dB, and an EVM improvement from 12.4 to 5.5 %. The BER is zero with DPD.

5.4 Broadband and Diplexed Comparison

This section compares the non-concurrent and concurrent CW large-signal performance of the “standard” broadband amplifier from [3] and the diplexed amplifier of this work.

5.4.1 Non-Concurrent Mode Comparison

In the non-concurrent CW mode, each test is conducted with a single CW tone input. Fig. 5.16 plots the gain, output power, and PAE of both PAs over 1.8–4 GHz. As expected, both maintain relatively flat output power and gain. The drive-up performance at the 3 GHz transition band is shown in Fig. 5.17 and compared to the "standard" PA. As expected, the diplexed architecture saturates earlier in the transition band. Note that the "standard" PA uses a Cree device rated at a slightly higher power (10 W) than the Qorvo device (7 W).

5.4.2 Concurrent Mode Comparison

In the concurrent CW mode, each test is conducted with two simultaneous tone inputs at 2.5 and 3.5 GHz for the "standard" broadband PA and the diplexed PA to obtain two-dimensional drive-up curves. In this case, in addition to the harmonic content, intermodulation (IMD) products are present. For equal output power values at 2.5 and 3.5 GHz, Fig. 5.18 plots the PAE and gains, where the two gain curves correspond to individual gains of the 2.5 and 3.5 GHz tones. The diplexed PA saturates later than the "standard" PA in this case.

The locations of the maximum concurrent PAE points for the two PAs are summarized in Table 5.2, with similar performance. Note that the diplexed architecture achieves more output power (40.3 dBm) in the concurrent than in the non-concurrent mode, due to the power combining of two PAs. In addition, its total gain (8.4 dB) is greater than that of the "standard" PA (6.8 dB).

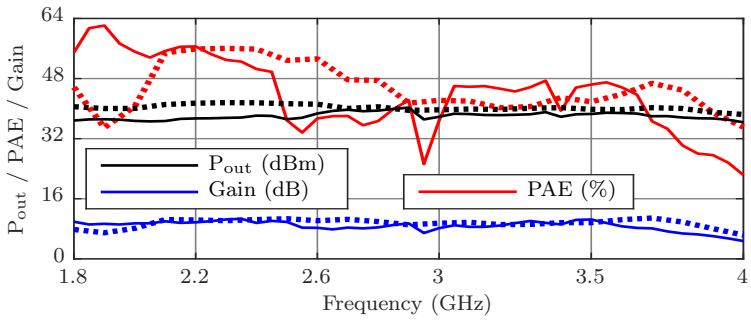


Figure 5.16: Measured non-concurrent large-signal performance over frequency of the (dashed) "standard" and (solid) diplexed broadband power amplifiers. Both amplifiers are class-B biased.

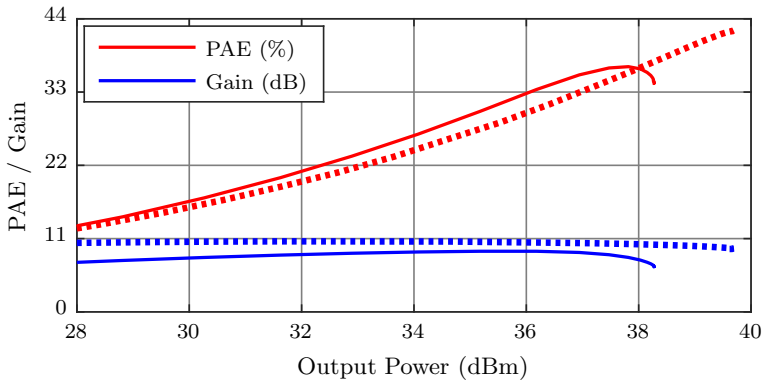


Figure 5.17: Measured non-concurrent large-signal drive-up performance of the (dashed) "standard" and (solid) diplexed broadband power amplifiers at 3 GHz. Both amplifiers are class-B biased.

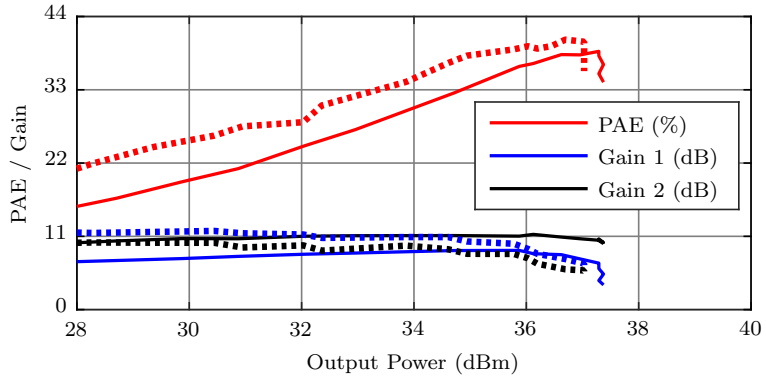


Figure 5.18: Measured concurrent 2.5 and 3.5 GHz large-signal performance over frequency of the (dashed) "standard" and (solid) diplexed broadband power amplifiers. Input powers are chosen such that the fundamental output powers are equal. This output power is plotted with corresponding (blue) 2.5 GHz and (black) 3.5 GHz gain curves, alongside (red) total PAE. Both amplifiers are class-B biased.

Table 5.2: Summary of Maximum Concurrent PAE Locations

PA	Gain_1 (dB)	Gain_2 (dB)	$P_{out,1,2}$ (dBm)	PAE (%)
"Standard"	7.6	6.1	36.7	40.5
Diplexed	7.0	10.4	37.3	38.8

Fixing the output power, P_{cross} at one (cross) frequency, corresponding to Table 5.2, the concurrent drive-up curves of the other (self) frequency can be obtained. This, alongside other concurrent power conditions, are depicted in Fig. 5.19 in solid and faded lines, respectively. In

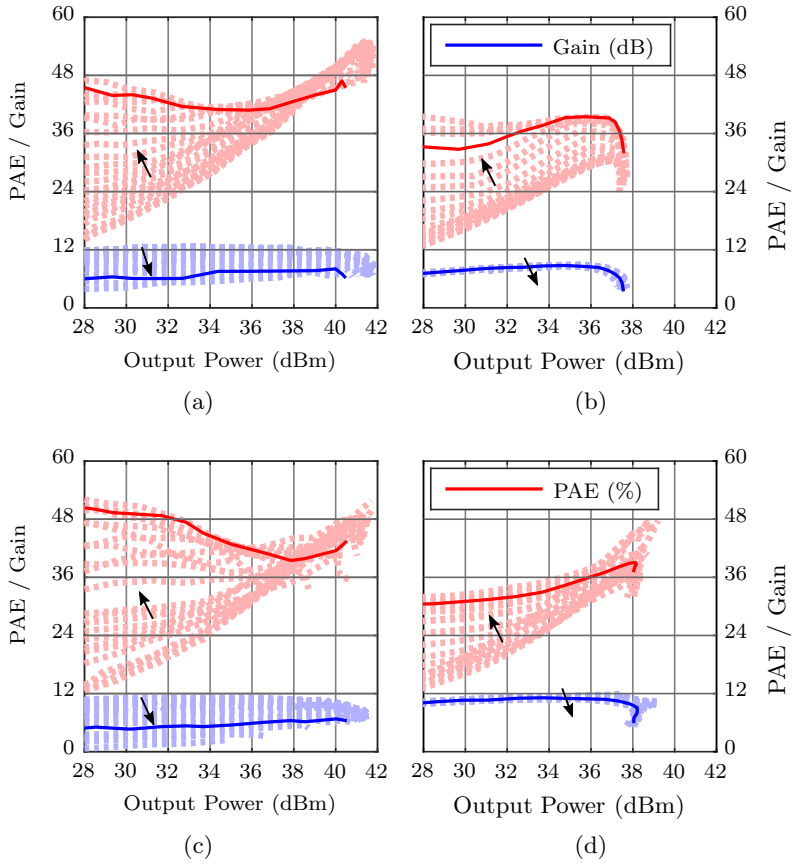


Figure 5.19: Measured concurrent drive-up performance of the (left) "standard" and (right) diplexed broadband power amplifiers, both class-B biased. The top row sweeps 2.5 GHz output power with a fixed 3.5 GHz P_{cross} value, plotting (blue) gain and (red) overall PAE. Solid lines correspond to the saturated concurrent performance of Table II, with faded dashed lines corresponding to lower and higher output power conditions, arrow pointing in the direction of increasing P_{cross}. Similarly, the bottom row sweeps 3.5 GHz output power for a fixed 2.5 GHz P_{cross}.

general, the PAE increases and gain decreases as P_{cross} is increased (direction of arrow). However, the gain variation and maximum output power degradation are much less in the diplexed PA than in the "standard" one.

The entire two-dimensional drive-up curves of the output spectrum are considered in context of IMD products. The relative power of each IMD product is calculated by:

$$\Delta P_{\text{IMD}} = P_{\text{fund,max}} - P_{\text{IMD,max}}, \tag{5.20}$$

where $P_{\text{fund,max}}$ is the maximum of the greater of the two fundamental tones, and $P_{\text{IMD,max}}$ is the maximum power of each IMD product occurring for any power. The highest values are summarized

in Table 5.3, demonstrating that the diplexed architecture contains significantly less IMD power than the "standard" architecture. The values shown in bold in the table correspond to common IMD products for the two PAs.

The drive-up curves of the highest tones identified in Table 5.3 are plotted in Fig. 5.20. In general, the IMD power increases as P_{cross} is increased (direction of arrow), but with about 20 dB less power in the diplexed PA than in the "standard" one. This can be explained as follows. In the "standard" architecture, maximum concurrent output power is limited by additional IMD content, which in turn lowers the fundamental power. Appropriate matching could mitigate this problem [111], but this approach requires accurate nonlinear models, which often are not available or validated for this purpose. In the diplexed architecture, on the other hand, there are effectively no IMD products, but output power is limited by combining loss.

Harmonics are not considered in Fig. 5.20 or Table 5.3 even though they have higher powers than the IMD products. A wideband spectrum under 2.5 and 3.5 GHz fundamental frequency excitation is shown in Fig. 5.21, which contains harmonics and IMD products for the two tones. Note that the IMD product values do not correspond to Table 5.3 because plotted values are not necessarily the highest in the two-dimensional drive-up curves. This figure illustrates in a different way that the diplexed PA has less IMD content, but more harmonic content, than the "standard" PA because its branch PAs are effectively operating in the non-concurrent mode.

Table 5.3: Comparison of Largest IMD Products

"Standard"		Diplexed	
ΔP_{IMD} (dBc)	IMD (GHz)	ΔP_{IMD} (dBc)	IMD (GHz)
-11.6	$2f_1 - f_2 = \mathbf{1.5}$	-22.6	$2f_2 - f_1 = \mathbf{4.5}$
-13.4	$f_2 - f_1 = \mathbf{1.0}$	-27.3	$2(f_2 - f_1) = \mathbf{2.0}$
-14.7	$2f_2 - f_1 = \mathbf{4.5}$	-27.5	$2f_1 - f_2 = \mathbf{1.5}$
-20.2	$f_1 + f_2 = 6.0$	-27.8	$f_2 - f_1 = \mathbf{1.0}$
-20.9	$2(f_2 - f_1) = \mathbf{2.0}$	-28.8	$2f_1 + f_2 = 8.5$

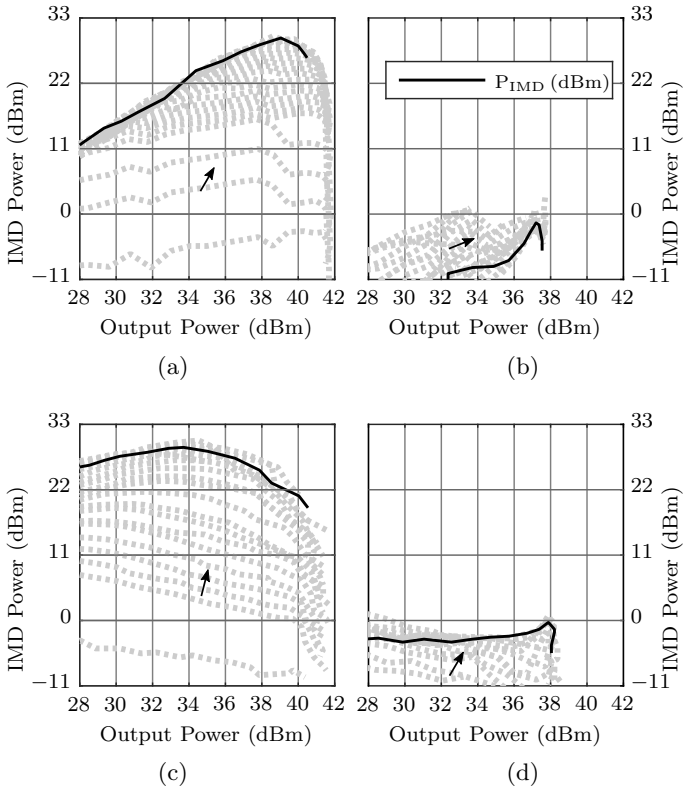


Figure 5.20: Largest measured concurrent IMD product drive-up performance of the (left) "standard" and (right) diplexed broadband power amplifiers, both class-B biased. The top row sweeps 2.5 GHz fundamental output power with a fixed 3.5 GHz fundamental P_{cross} value, plotting the $2f_1 - f_2 = 1.5$ GHz IMD product. Solid lines correspond to the saturated concurrent performance of Table II, with faded dashed lines corresponding to lower and higher output power conditions, arrow pointing in the direction of increasing cross power. Similarly, the bottom row sweeps 3.5 GHz fundamental output power for the $2f_2 - f_1 = 4.5$ GHz IMD product.

5.5 Conclusion

An analysis of a diplexing architecture for broadband PA design is presented in this section. By diplexing concurrent signals into two paths consisting of relatively narrowband but efficient PAs, overall efficiency, gain, power, and linearity remain high. Linearity of concurrent signals is improved further with a simple implementation of DPD. The advantages of this architecture become clear when comparing concurrent signal IMD products with a more "standard" broadband PA.

Two "standard" broadband PAs were analyzed, one incorporating an analytical ISMN design procedure. An alternative broadband PA architecture is demonstrated, showing that the implementation results in far few IMD products in the concurrent mode of operation as compared to the

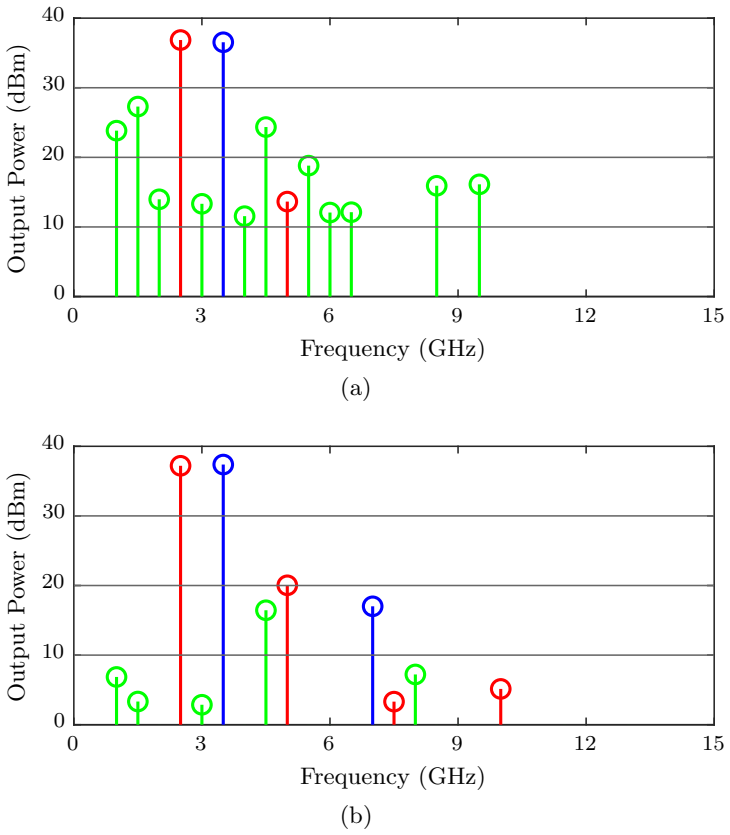


Figure 5.21: Measured CW concurrent wideband output spectra of the (a) "standard" and (b) diplexed broadband power amplifiers corresponding to the conditions in Table II. Red lines correspond to 2.5 GHz and its harmonics, blue lines to 3.5 GHz and its harmonics, and green lines to intermodulation products. Both amplifiers are class-B biased.

"standard" PA. This architecture is demonstrated to also amplify concurrent modulated signals with DPD. Original contributions in this chapter include the following:

- Validating the analytical ISMN design with a fabricated implementation [75].
- Reporting for the first time in literature an alternative broadband PA architecture for increased linearity with concurrent signals [4, 76].
- Demonstrating the alternative broadband PA architecture achieves increased linearity and similar performance with concurrent signals compared to a "standard" broadband PA [4,76].

The design methods in this and previous chapters provides insight into dual-band and broadband PA design. Depending on whether concurrent signals are being amplified, non-traditional architectures may be considered for improved linearity.

Chapter 6

Conclusion

6.1 Summary and Contributions

This thesis considers the trade-off between high efficiency and broad bandwidth of an RF PA. Chapter 3 demonstrates that both properties cannot be simultaneously maximized. Two main approaches to avoid this limitation include: (1) focusing on dual-band PAs in Chapter 4; and (2) focusing on broadband PAs in Chapter 5. These amplifiers, along with concurrent signals, will be useful in enhancing modern phased-arrays in applications such as communications systems and radar. Technology being developed towards reducing the cost of phased arrays is considered in Chapter 2. In any phased array application, LOs are required to generate RF frequencies. Appendix A presents circuits for generating broadband LO gain for applications such as broadband phased arrays.

When these results are used to implement dual-band and broadband PAs which can amplify a non-concurrent CW signal, similar gain, output power, efficiency, and linearity characteristics can be obtained as compared to a narrow-band PA counterpart. However, when concurrent signals are amplified, output power and gain are decreased for the dual-band and "standard" broadband PAs, as investigated in Chapters 4 and 5. This also lowers the efficiency and linearity of both PAs; however, the decrease in linearity for concurrent signals can largely be avoided if the diplexed PA architecture is used. This section summarizes the contents and contributions of each chapter.

6.1.1 Chapter 2: Low-Cost Phased Array Technology

A GaN-on-Si technology being developed by the MIT Lincoln Laboratory was presented. The dielectric stackup was simulated and simplified in HFSS and Sonnet. Various passive components were simulated and combined to create matching networks. Transistors were analyzed using only s-parameter and dc-IV data, with a PA design shown incorporating these passive component matching networks. Measured data indicated simplifications were appropriate and indicated future designs are likely to perform better. Original contributions in this chapter include the following: (1) design, characterization, and validation of a GaN-on-Si process with HFSS and Sonnet simulations [18]; and (2) design and measurements of the first X-band PA with this GaN-on-Si process using the process characterization and without a nonlinear model typically used.

6.1.2 Chapter 3: Impedance Matching Techniques

A mathematical analysis of lossy matching networks is presented. Methods to synthesize narrowband and broadband networks were presented, alongside fundamental limitations to broadband design. Original contributions in this chapter include the following: (1) demonstrating for the first time in literature the phase relationship between scattering parameter phases of lossy networks in [75]; (2) developing an analytical ISMN design method for a PA in [75]; (3) developing a numerical ISMN design method for a PA; (4) analyzing the Bode-Fano criterion in terms of an arbitrary load and demonstrating its applicability to PA design in [76].

6.1.3 Chapter 4: Dual-Band RF Power Amplifiers

Two dual-band PAs in hybrid and MMIC implementations are presented and characterized in the non-concurrent and concurrent mode of operation. Both characterizations demonstrated a dependence between the two frequencies in the concurrent mode, and degraded performance (gain, efficiency, output power, and linearity) as compared to the non-concurrent mode. Original contributions in this chapter include the following: (1) the design and characterization of a 2.2/3.9 GHz single-stage hybrid GaN PA under non-concurrent CW and concurrent modulated signals presented

in [90]; and (2) the design and characterization of a 9.0/16.1 GHz two-stage MMIC GaAs PA under non-concurrent and concurrent CW signals presented in [20].

6.1.4 Chapter 5: Broadband RF Power Amplifiers

An analysis of a diplexing architecture for broadband PA design is presented in this section. By diplexing concurrent signals into two paths consisting of relatively narrowband but efficient PAs, overall efficiency, gain, power, and linearity remain high. Linearity of concurrent signals is improved further with a simple implementation of DPD. The advantages of this architecture become clear when comparing concurrent signal IMD products with a more "standard" broadband PA.

Two "standard" broadband PAs were analyzed, one incorporating an analytical ISMN design procedure. An alternative broadband PA architecture is demonstrated, showing that the implementation results in far few IMD products in the concurrent mode of operation as compared to the "standard" PA. This architecture is demonstrated to also amplify concurrent modulated signals with DPD. Original contributions in this chapter include the following: (1) validating the analytical ISMN design with a fabricated implementation in [75]; (2) reporting for the first time in literature an alternative broadband PA architecture for increased linearity with concurrent signals in [4, 76]; (3) demonstrating that the alternative broadband PA architecture achieves increased linearity and similar performance, as compared to a "standard" broadband PA, with concurrent signals in [4, 76].

6.2 Future Work

There are several areas from the work of this thesis that are candidates for further investigation. Architectures to improve the functionality of phased arrays are discussed, followed by considerations of the diplexed power amplifier.

6.2.1 RF Front-End Feedback Network

One limitation of the phased array architecture in Fig. 1.1 is that it does not allow for in-band full-duplex, or simultaneous transmit and receive (STAR), operation. STAR enables increased

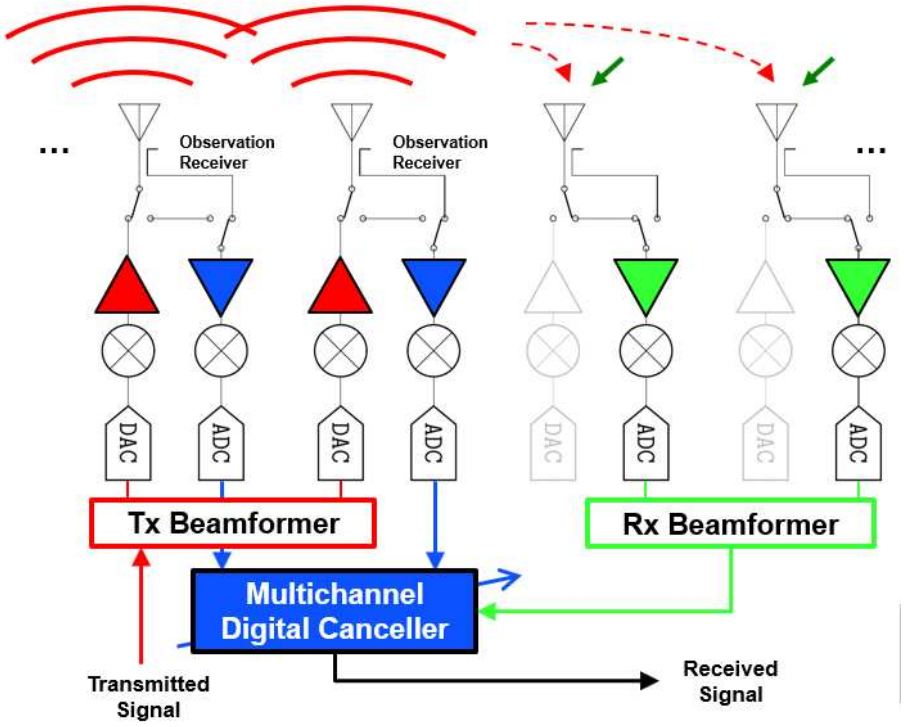


Figure 6.1: Diagram of an example feedback network within a phased array that enables sensing and digital cancellation of a transmitted signal to increase transmit and receive isolation.

spectral efficiency and network capacity for many radar and communications applications. Some varieties of STAR include time-division, frequency-division, and polarization-division. Portions of a phased array aperture can also be used for transmit and receive; in a phased array, this is known as aperture-level STAR [125]. For example, in a 4 x 4 array, the four quadrants containing 2 x 2 elements can be each be used in the transmit or receive mode, adding to the subarray digital phased array architecture of Chapter 1. Pure STAR operation utilizes all antenna elements at the same time, frequency, and polarization. In any of these varieties, increased isolation between transmit and receive paths of digital phased arrays is critical due to antenna coupling of the undesired transmitted signal into the receive path.

The MIT Lincoln Laboratory T/R Modules for Advanced Phased Arrays program is developing a front-end switch and feedback network to increase the path isolation, as shown in Fig. 6.1. This network replaces the commonly used circulator or switch component between the antenna and

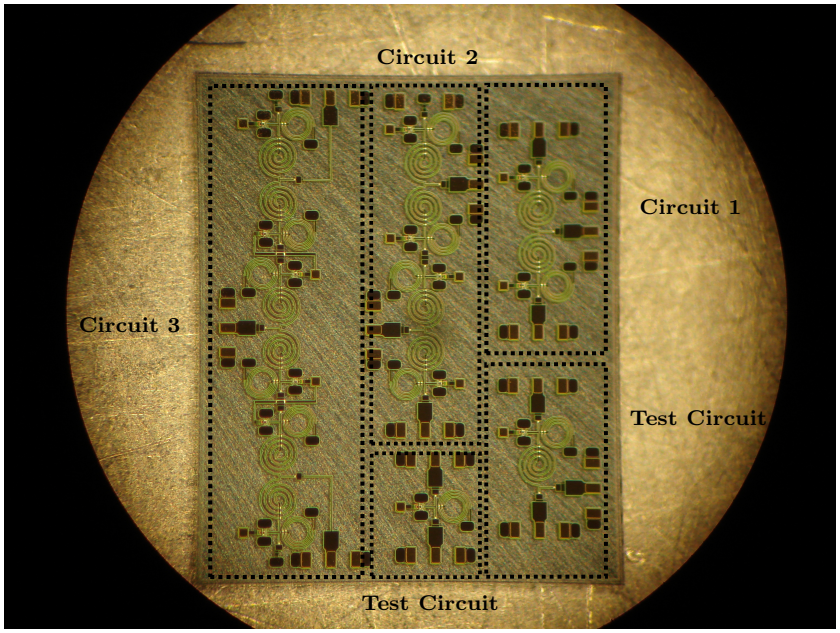


Figure 6.2: Chip photograph of the three designed switches, and test circuits, measuring 2.5 mm x 3.0 mm.

amplifiers, from Fig. 1.1, and allows for sensing of the transmitted signal. By accounting for the nonlinearities and additive phase noise introduced by the PA, and with calibrated antenna coupling information, the undesired transmitted signal in the receive path can be digitally canceled.

To begin investigating this network, the WIN 0.15 μm GaN-on-SiC process is used to investigate three types of switches with leakage that could be used as a feedback network. Beginning with a unit switch design, two and three of these are cascaded to form the two other circuits. Increasing the number of switches increases the isolation at the expense of path loss. A photograph of these switches is shown in Fig. 6.2.

Measurements and simulations of the three circuits are shown in Fig. 6.3. In general, trends agree with one another, providing a foundation for future design work. Because the single and triple-unit switches are symmetrical in both configurations, only plot is shown. For the double-unit switch, two plots are shown for each configuration. One path (either transmit or receive) will have more insertion loss than the other. Depending on the particular application and desired characteristics, one of these switches may be more appropriate to use than another.

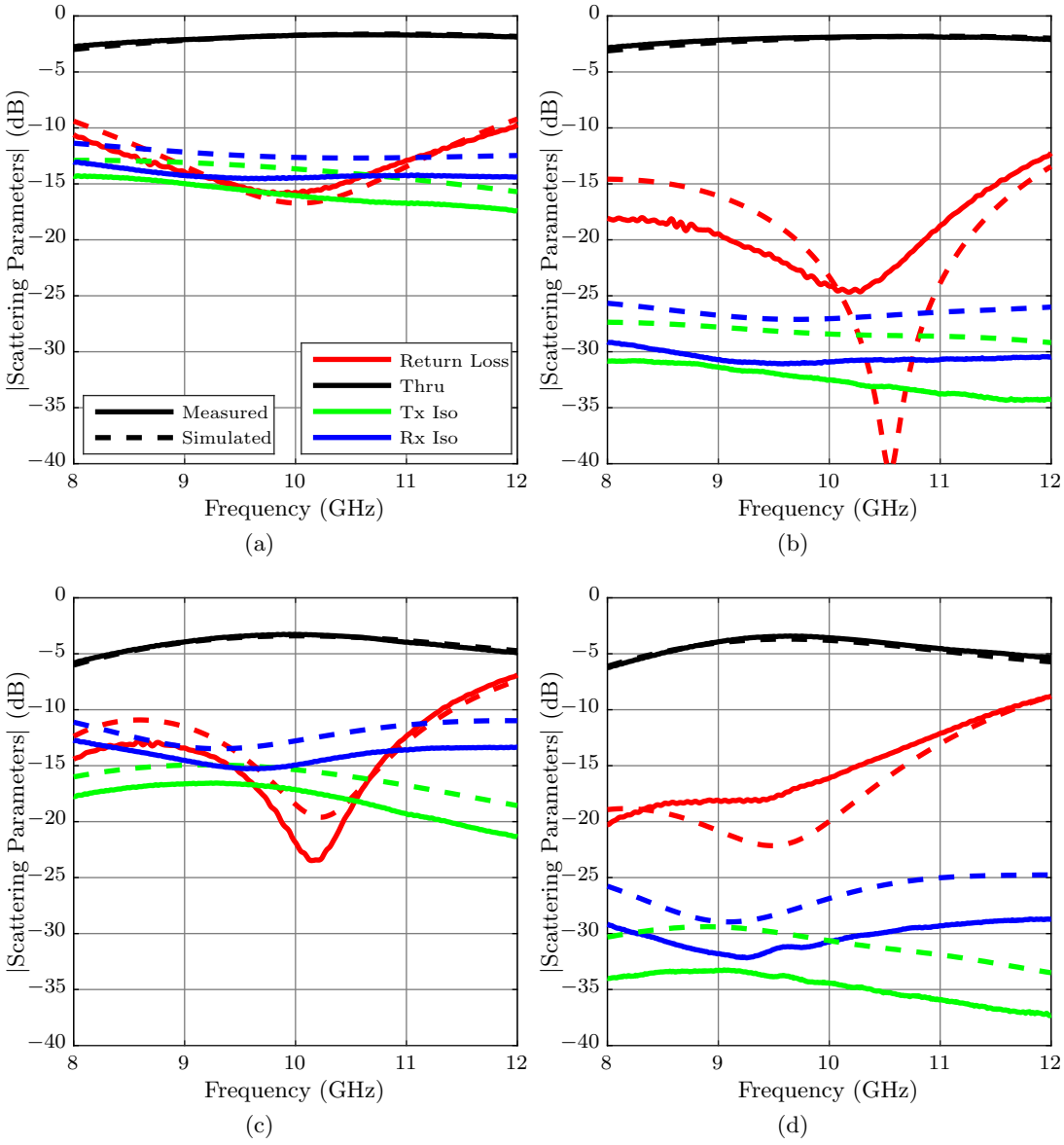


Figure 6.3: Measurements and simulations of the (a) single-unit switch, (b) double-unit switch in configuration one, (c) double-unit switch in configuration two, and (c) triple-unit switch.

Because path loss is critical for phased array sensitivity, future work involves further investigation of the switch architecture. Additionally, because component isolation values are not as critical as system-level isolation, co-designing the switch, LNA, and PA will likely minimize loss while enabling desired T/R module characteristics for STAR.

6.2.2 Impedance Matching Techniques

Section 5.1.2 implemented the ISMN design approach of Chapter 3 for non-physical Γ_1' and Γ_2' input values. Because of these inputs, a solution began with choosing a network topology known to be broadband. With additional mathematical considerations, however, an analytical approach could be investigated. For example, the Bode-Fano criterion could be integrated into the network synthesis stage, along with considering network synthesis techniques [120], to require no *a priori* knowledge of the ISMN topology.

In Section 3.1.5, a two-port network is considered. This solution could be generalized up to 4-port networks. In order to make the conclusions of that section, the characteristic equation of **A** had to be evaluated, which involved solving a second-degree polynomial equation. It is proven that 5^{th} and higher order polynomials do not have an explicit solution, and so would require numerical approximations, leaving a general N-port conclusion not possible to make. Regardless, this numerical approach may be useful in evaluating inter-stage combining networks.

6.2.3 X-Ku Diplexed Power Amplifier

To demonstrate the diplexed PA approach in a MMIC implementation, an X-Ku 8–18 GHz PA is designed using the WIN 0.15 μm GaN-on-SiC process. Several differences in this implementation occur in the filter design. Because of chip-size constraints, the band-pass hybrid approach was not chosen due to the relatively large electrical length of its transmission lines. However, due to relatively smaller lumped component tolerances, as compared to packaged parts, inductors and capacitors are feasible in the diplexer design, enabled by photolithography. Therefore, an LPF and HPF are designed as the two branches of the diplexer.

The LPF is implemented with three series inductors and shunt capacitors. High-impedance lines are used to minimize size, with little effect on filter performance. The HPF is implemented with three series capacitors and shunt shorted stubs. The stubs are designed to behave as shorted inductors, and chosen because they can be meandered to decrease size. Though initial designs began

with identical diplexer at the input and output, the final circuit in Fig. 6.4 has slightly different filters due to size considerations.

To further show that the branch PAs are interchangeable, two frequency-offset two-stage PAs are designed. The second-stage transistor is sized at $8 \times 100\,\mu$m to deliver simulated output power of greater than 1 W. For efficiency, the first stage transistor is sized at $4 \times 50\,\mu$m for a 1:4 staging ratio. Bias lines for the gate and drain of each transistor are not combined on-chip so that they can be measured separately. However, as demonstrated in Chapter 5, they can be combined. Similar integration techniques from that chapter complete the design.

The fabricated chip is mounted on a CuMo carrier using conductive silver epoxy. Eight 1 nF single-layer capacitors are connected to each bias pad, with the two gate and drain pads on the

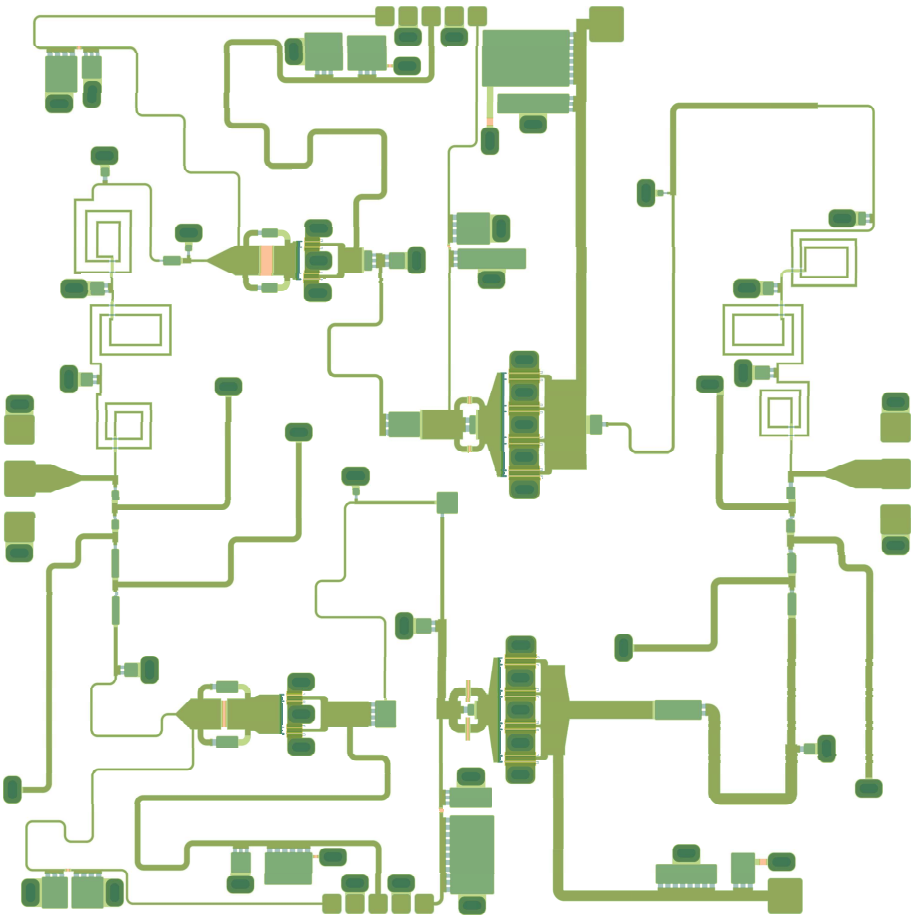


Figure 6.4: Layout of the GaN-on-SiC diplexed PA designed for 8–18 GHz. The size of the chip is 2.5 mm x 2.5 mm.

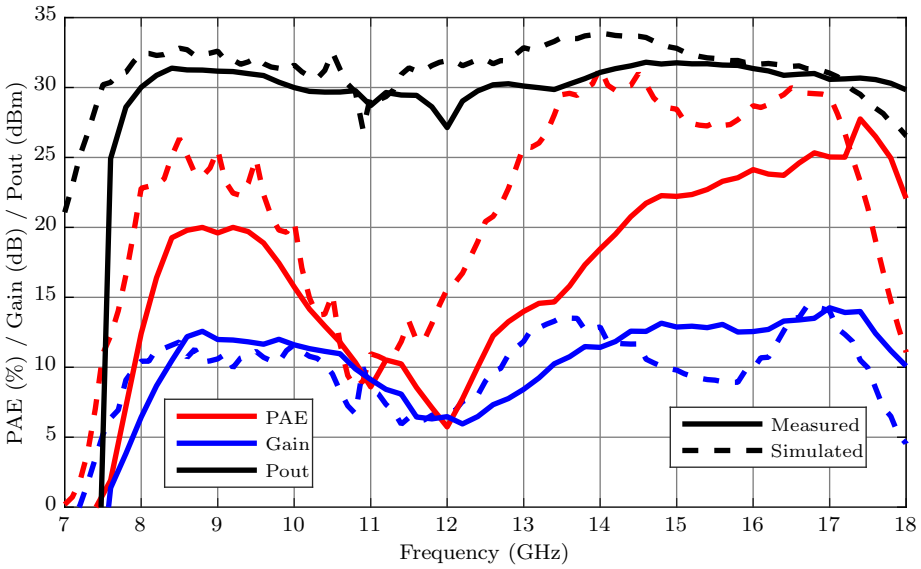


Figure 6.5: Saturated large-signal performance of the GaN-on-SiC diplexed PA designed for 8–18 GHz.

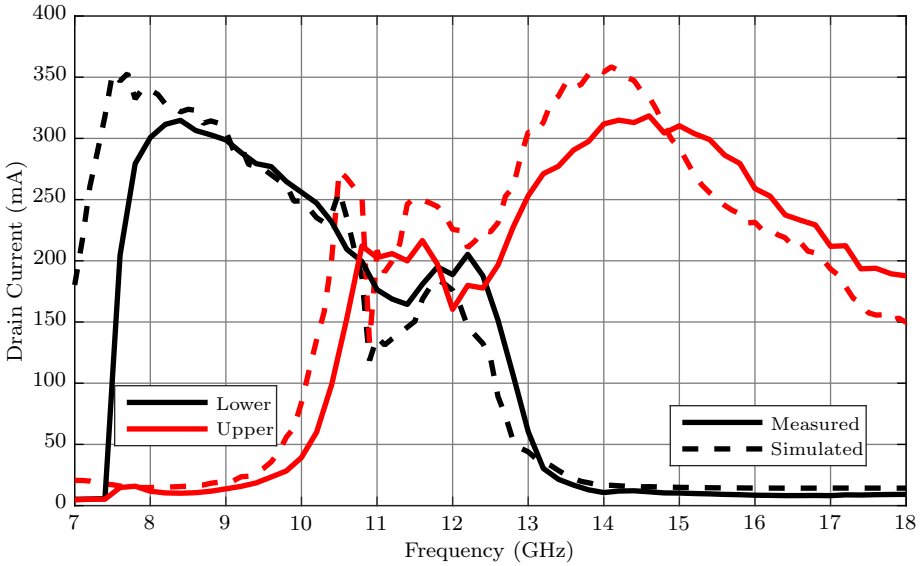


Figure 6.6: Saturated large-signal current of the two branches of the GaN-on-SiC diplexed PA designed for 8–18 GHz.

top and bottom connected together with four 100 nF single-layer capacitors, and probed. After calibration, the large-signal saturated performance, as a function of frequency, of the chip is shown in Fig 6.5. As seen, the trends of simulations and measurements tend to agree; however, decreased output power contributes to a decrease in PAE.

To investigate the decrease, corresponding saturated large-signal currents of the two branches of the PA are plotted in Fig. 6.6. These trends agree fairly well, indicating that increased loss is likely due to mismatch from un-characterized coupling in the circuit. Characterizing this, or any other diplexed PA, with a wideband signal covering the entire bandwidth of operation would be an interesting test to confirm the simultaneous operation of the diplexed branches and transition band between them. As size was a significant hindrance during this design process, investigations towards footprint miniaturization will be especially valuable for MMIC implementations. One such suggestion is given in the next section.

6.2.4 Complex Terminated Multiplexed Power Amplifier

Additional wideband modulated signal testing of the hybrid diplexed PA would be interesting to confirm the operation of the transition band, as previously described for the MMIC implementation. For example, the results of Section 5.4 could be replicated with two commercial PAs and two diplexers, as concurrent signal tests with a tone in the transition band were not performed. In this case, with signals concurrently present in the lower, transition, and upper bands, the branch PAs of the diplexed PAs are no longer operating non-concurrently and can be expected to suffer some performance degradation. However, as compared to its "standard" broadband counterpart, improved performance is still possible as each branch amplifier covers only a smaller frequency subset.

It is a natural extension of the diplexed power amplifier architecture to three branches with a triplexer, or more with a multiplexer. However, additional care must be used when designing the multiplexer, as more branches typically increases the combining loss [57]. This could lead to an interesting trade-off study of: (1) fixing the total bandwidth and increasing the number of branches to increase branch PA efficiency; and (2) fixing the branch PA bandwidth and increasing the total PA bandwidth. It is not clear if two branches is the optimal split for an octave bandwidth. In this multiplexing case, it becomes important to ensure the branch filters have high rejection in all undesired paths.

Furthermore, more complicated filters could be investigated. For example, dual BPFs are common in literature, and it may be possible to design a dual-BPF diplexer, with each branch allowing a non-overlapped dual band-pass frequency response. With this filter response, dual-band PAs, such as those of Chapter 4, can be incorporated into the multiplexed PA architecture.

In this thesis, the diplexers and branch PAs of Chapter 5 were designed for 50 Ω for simple integration and test. This, however, is not necessary, and may not even be the best approach for a multiplexed architecture. Rather than designing the combined/split multiplexer ports to 50 Ω, one may instead design them to the complex source and load-pull impedances of the device, such as in [40], reducing footprint. Due to the reactive terminations, matching bandwidth limitations must be considered, and therefore it is not clear if a diplexer-based approach would be able to cover an octave frequency bandwidth with this approach.

Filter implementation also affects harmonic terminations, which in turn affects PA efficiency and linearity. In LPF and HPF-based diplexers, only the LPF removes harmonic content, improving linearity, and introduces a high-$|\Gamma|$ harmonic impedance to the PA, which could be incorporated with the OMN for increased efficiency. As the HPF does not have these properties, and this case is limited to two branches, BPF-based multiplexers are a more general solution with similar performance benefits of the LPF. However, additional care should taken during the filter design stage for three reasons: (1) a BPF could be large in MMIC implementations, as the previous section demonstrated; (2) a BPF based on a periodic structure, such as a transmission line, could allow odd-harmonic content to pass through; and (3) high rejection is required across all stop bands of the multiplexed frequency range.

Group delay was not investigated in this work, but is important in certain applications. Filters, such as the BPFs of the diplexers, tend to have increased group delay around the pass-band edges [126]. The output impedance was tuned to maintain a flat output power response, and for fixed PA output matching networks, it may be possible to tune the input impedance of the PA to maintain an appropriate input match while also flattening the group delay. For example, using two of the final EM-simulated diplexers from Section 5.4, such that the low-pass ports are

connected directly, along with the high-pass ports, the group delay of the back-back structure is simulated. A maximum value of 1770 ps occurs near the center of the band, while a minimum value of 700 ps occurs near the edge, with the shape being roughly symmetric. Redesigning the diplexers could even the band edges, while input impedance tuning could possibly flatten this group delay response through the transition band.

6.2.5 Efficiency Enhancement of Multiplexed Power Amplifiers

One factor contributing to performance degradation of the diplexed PA is the load presented by the diplexer to each PA in the transition band. Considering (5.9), even if each PA had a well-matched output impedance, the diplexer load always equals at least S_{22}. In band, this is not an issue because the value is low, but this value necessarily increases in the transition band, resulting in degraded branch PA performance [98,127]. This could be improved with a tunable network, [98], or with signal correction, [128], but is not considered here. Stability, however, is ensured over a wide range of port terminations [129].

Even though flat output power of a multiplexed PA can be maintained, other factors contribute to an efficiency degradation in the transition band. Due to the power split of the multiplexers, in the worst case, each branch PA will have half the input power. Because efficiency degrades in back-off, this necessarily results in lower transition-band efficiency. This could be incorporated into the PA design to some extent by designing for maximum back-off efficiency. Over-driving the system by 3 dB may lead to a degraded linearity trade-off. Therefore, this inherent efficiency response will be difficult to correct in the RF domain. One alternative could be a pseudo-supply modulation approach. By lowering the shared drain voltage when signals are present in the transition band, efficiency could be increased at the expense of gain. This supply would only have to change as fast as the signals do in frequency, rather than as fast as they do in time with typical supply modulation.

The modular nature of the multiplexed PA architecture allows for many different kinds of amplifiers to be used in each branch, depending on the specific design requirements, such as ones

based on a reduced conduction angle (class-AB, class-B, class-C), harmonic terminations (class-F), switching (class-D, class-E), complex terminations (class-J), push-pull, distributed, balanced, and many others. For example, if a Doherty PA is utilized, the back-off efficiency of the overall amplifier can be improved. As Doherty PAs are limited in bandwidth due to their $\lambda/4$ output combining transmission line, it may be necessary to design three or more branches to cover an octave frequency bandwidth. Regardless, by designing several frequency-offset Doherty PAs with a multiplexer, broad bandwidth and back-off efficiency may be achievable. This approach requires doubling the number of transistors. Minimally, with a diplexer, at least four transistors are required. With size constraints, the large footprint of this approach may not be ideal. Alternatively, supply modulation may be utilized instead of a Doherty PA. By using single-ended branch PAs and low-order filters, size can be kept relatively small.

6.3 Publications

Patents: [130]

Journals: [4, 75, 76]

Conference Proceedings: [18, 20, 90, 131]

Conference Presentations: [132, 133]

Bibliography

[1] Keysight Technologies, Inc. Concepts of orthogonal frequency division multiplexing (OFDM) and 802.11 WLAN. [Online]. x, 5, 8

[2] J. Hoversten, "Efficient and linear microwave transmitters for high peak-to-average ratio signals," Ph.D. dissertation, University of Colorado Boulder, 2010, pp. 27–54. x, 12, 14, 29

[3] M. R. Duffy, G. Lasser, M. Olavsbråten, E. Berry, and Z. Popović, "Efficient multisignal 2–4-GHz power amplifier with power tracking," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5652–5663, 2018. xvii, 80, 81, 95, 102

[4] P. Zurek, T. Cappello, and Z. Popović, "Broadband diplexed power amplifier," IEEE Microwave and Wireless Components Letters, vol. 30, no. 11, pp. 1073–1076, 2020. xviii, 84, 86, 94, 108, 111, 121

[5] J. S. Herd and M. D. Conway, "The evolution to modern phased array architectures," Proceedings of the IEEE, vol. 104, no. 3, pp. 519–529, 2016. 2, 3, 20

[6] E. Kowalski, M. D. Conway, A. Morris, and C. Parry, "Multifunction phased array radar advanced technology demonstrator (MPAR ATD) nearfield testing and fielding," in 2019 IEEE Radar Conference (RadarConf), 2019, pp. 1–4. 2, 20

[7] C. Pfeffer, R. Feger, C. Wagner, and A. Stelzer, "FMCW MIMO radar system for frequency-division multiple TX-beamforming," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 12, pp. 4262–4274, 2013. 2, 3

[8] F. J. Ortega-Gonzalez, D. Tena-Ramos, M. Patiño-Gomez, J. M. Pardo-Martin, and D. Madueño-Pulido, "High-power wideband L-band suboptimum class-E power amplifier," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 10, pp. 3712–3720, 2013. 2

[9] Y. A. Atesal, B. Cetinoneri, K. M. Ho, and G. M. Rebeiz, "A two-channel 8–20-GHz SiGe BiCMOS receiver with selectable IFs for multibeam phased-array digital beamforming applications," IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 3, pp. 716–726, 2011. 2, 3

[10] S. Drews, F. Rautschke, D. Maassen, C. T. Nghe, and G. Boeck, "A 10-W S-band power amplifier for future 5G communication," in 2017 47th European Microwave Conference (EuMC), Oct 2017, pp. 152–155. 2, 80, 99

[11] L. Zhang, A. Natarajan, and H. Krishnaswamy, "Scalable spatial notch suppression in spatio-spectral-filtering MIMO receiver arrays for digital beamforming," IEEE Journal of Solid-State Circuits, vol. 51, no. 12, pp. 3152–3166, 2016. 2, 3

[12] H. M. Nemati, H. Cao, B. Almgren, E. T, and C. Fager, "Design of highly efficient load modulation transmitter for wideband cellular applications," IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 11, pp. 2820–2828, 2010. 2

[13] J. Jeong, N. Collins, and M. P. Flynn, "A 260 MHz IF sampling bit-stream processing digital beamformer with an integrated array of continuous-time band-pass $\delta\sigma$ modulators," IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1168–1176, 2016. 2, 3

[14] B. Sadhu, Y. Tousi, J. Hallin, S. Sahl, S. K. Reynolds, O. Reström, K. Sjögren, O. Haapalahti, N. Mazor, B. Bokinge, G. Weibull, H. Bengtsson, A. Carlinger, E. Westesson, J. E. Thillberg, L. Rexberg, M. Yeck, X. Gu, M. Ferriss, D. Liu, D. Friedman, and A. Valdes-Garcia, "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3373–3391, 2017. 2

[15] W. Hong, Z. H. Jiang, C. Yu, J. Zhou, P. Chen, Z. Yu, H. Zhang, B. Yang, X. Pang, M. Jiang, Y. Cheng, M. K. T. Al-Nuaimi, Y. Zhang, J. Chen, and S. He, "Multibeam antenna technologies for 5G wireless communications," IEEE Transactions on Antennas and Propagation, vol. 65, no. 12, pp. 6231–6249, 2017. 2, 3

[16] W. H. Weedon, "Phased array digital beamforming hardware development at applied radar," in 2010 IEEE International Symposium on Phased Array Systems and Technology, 2010, pp. 854–859. 3

[17] S. Warnock, C. L. Chen, J. Knecht, R. Molnar, D. R. Yost, M. Cook, C. Stull, R. Johnson, C. Galbraith, J. Daulton, W. Hu, G. Pinelli, J. Perozek, T. Palacios, B. Zhang, J. Herd, and C. Keast, "InAlN/GaN-on-Si HEMT with 4.5 W/mm in a 200-mm CMOS-compatible MMIC process for 3D integration," in 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 289–292. 4, 20, 21

[18] P. Zurek, M. Foreman, R. Johnson, C. Galbraith, J. Estrada, and Z. Popovic, "Design of ungrounded CPW GaN-on-Si MMICs," in 2018 International Applied Computational Electromagnetics Society Symposium (ACES), 2018, pp. 1–2. 4, 20, 37, 110, 121

[19] Z. Popović, "Amping up the PA for 5G: Efficient GaN power amplifiers with dynamic supplies," IEEE Microwave Magazine, vol. 18, no. 3, pp. 137–149, 2017. 4

[20] P. Zurek and Z. Popović, "Two-stage concurrent X/Ku dual-band GaAs MMIC power amplifier," in 2020 IEEE MTT-S International Microwave Symposium (IMS), 2020. 4, 78, 111, 121

[21] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90 - 100-GHz 4 x 4 SiGe BiCMOS polarimetric transmit/receive phased array with simultaneous receive-beams capabilities," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 8, pp. 3099–3114, 2013. 4

[22] H. T. Dabag, B. Hanafi, F. Golcuk, A. Agah, J. F. Buckwalter, and P. M. Asbeck, "Analysis and design of stacked-FET millimeter-wave power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 4, pp. 1543–1556, 2013. 4

[23] U. Schmid, H. Sledzik, P. Schuh, J. Schroth, M. Oppermann, P. Bröckner, F. van Raay, R. Quay, and M. Seelmann-Eggebert, "Ultra-wideband GaN MMIC chip set and high power amplifier module for multi-function defense AESA applications," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 8, pp. 3043–3051, 2013. 4, 79

[24] T. Kinghorn, I. Scott, and E. Totten, "Recent advances in airborne phased array radar systems," in 2016 IEEE International Symposium on Phased Array Systems and Technology (PAST), 2016, pp. 1–7. 4, 79

[25] Z. Shen, A. Papasakellariou, J. Montojo, D. Gerstenberger, and F. Xu, "Overview of 3GPP LTE-advanced carrier aggregation for 4G wireless communications," IEEE Communications Magazine, vol. 50, no. 2, pp. 122–130, February 2012. 4, 14, 58, 79

[26] S. A. Bassam, W. Chen, M. Helaoui, and F. M. Ghannouchi, "Transmitter architecture for CA: Carrier aggregation in LTE-advanced systems," IEEE Microwave Magazine, vol. 14, no. 5, pp. 78–86, July 2013. 4, 14, 58, 79

[27] A. M. Kinghorn, "Where next for airborne AESA technology?" in 2008 IEEE Radar Conference, 2008, pp. 1–4. 4, 79

[28] S. Lien, S. Shieh, Y. Huang, B. Su, Y. Hsu, and H. Wei, "5G new radio: Waveform, frame structure, multiple access, and initial access," IEEE Communications Magazine, vol. 55, no. 6, pp. 64–71, 2017. 5, 10, 79

[29] M. Jaber, M. A. Imran, R. Tafazolli, and A. Tukmanov, "5G backhaul challenges and emerging research directions: A survey," IEEE Access, vol. 4, pp. 1743–1766, 2016. 5, 10, 79

[30] S. B. Weinstein, "The history of orthogonal frequency-division multiplexing [history of communications]," IEEE Communications Magazine, vol. 47, no. 11, pp. 26–35, 2009. 5

[31] T. D. Chiueh and P. Y. Tsai, OFDM Baseband Receiver Design for Wireless Communications. Wiley, 2007. 5, 6, 8, 9

[32] IEEE Standard for Information technology– Local and metropolitan area networks– Specific requirements– Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: Further Higher Data Rate Extension in the 2.4 GHz Band, IEEE Std., 2003. 5

[33] J. Zyren and W. McCoy, "Overview of the 3GPP long term evolution physical layer," Freescale Semiconductor, Tech. Rep. 3GPPEVOLUTIONWP, 2007. [Online]. [Online]. Available: https://www.nxp.com/docs/en/white-paper/3GPPEVOLUTIONWP.pdf 5

[34] "Designing 5G NR: The 3GPP release 15 global standard for a unified, more capable 5G air interface," [Online], Qualcomm, Sept. 2018. 5

[35] J. Hagenauer, E. Offer, and L. Papke, "Iterative decoding of binary block and convolutional codes," IEEE Transactions on Information Theory, vol. 42, no. 2, pp. 429–445, 1996. 5, 6

[36] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error-correcting coding and decoding: Turbo-codes. 1," in Proceedings of ICC '93 - IEEE International Conference on Communications, vol. 2, 1993, pp. 1064–1070 vol.2. 6

[37] N. Benvenuto and G. Cherubini, Algorithms for Communications Systems and their Applications. Wiley, 2002. 6, 8, 10

[38] F. H. Raab, P. Asbeck, S. Cripps, P. B. Kenington, Z. B. Popović, N. Pothecary, J. F. Sevic, and N. O. Sokal, "Power amplifiers and transmitters for RF and microwave," IEEE Transactions on Microwave Theory and Techniques, vol. 50, no. 3, pp. 814–826, 2002. 10, 13

[39] S. Preis, T. Arnous, Z. Zhang, P. Saad, and G. Boeck, "Bandwidth versus efficiency performance using power combining in GaN HEMT power amplifiers," in 2013 European Microwave Conference, 2013, pp. 696–699. 12, 52, 54

[40] J. A. Estrada, J. R. Montejo-Garai, P. de Paco, D. Psychogiou, and Z. Popović, "Power amplifiers with frequency-selective matching networks," IEEE Transactions on Microwave Theory and Techniques, pp. 1–1, 2020. 13, 119

[41] I. Keysight Technologies. EVM (digital demod). [Online]. 15

[42] S. A. Bassam, M. Helaoui, and F. M. Ghannouchi, "2-D digital predistortion (2-D-DPD) architecture for concurrent dual-band transmitters," IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 10, pp. 2547–2553, 2011. 15, 65, 80, 99, 100, 101

[43] M. S. Shur, "GaN based transistors for high power applications," Solid-State Electronics, vol. 42, no. 12, pp. 2131–2138, 1998. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0038110198002081 20

[44] R. Leblanc, N. S. Ibeas, A. Gasmi, F. Auvray, J. Poulain, F. Lecourt, G. Dagher, and P. Frijlink, "6W Ka band power amplifier and 1.2dB NF X-band amplifier using a 100nm GaN/Si process," in 2016 IEEE CSICS, Oct. 2016, pp. 1–4. 20, 30

[45] L. Pattison, T. Boles, N. Tuffy, and G. Lopes, "Improving GaN on Si power amplifiers through reduction of parasitic conduction layer," in 2014 9th European Microwave Integrated Circuit Conference, 2014, pp. 92–95. 20, 30

[46] J. Kim, H. Park, D. Kim, M. Lee, K. Seo, and Y. Kwon, "RF parametric study on AlGaN/GaN HEMTs on Si-substrate for millimeter-wave PA," in 2013 APMC Proceedings, Nov. 2013, pp. 775–777. 20

[47] T. E. Kazior, J. R. LaRoche, and W. E. Hoke, "More than moore: GaN HEMTs and Si CMOS get it together," in 2013 IEEE CSICS, Oct. 2013, pp. 1–4. 20, 21

[48] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, Microstrip Lines and Slotlines. Boston, MA: Artech House, 1996, pp. 375–451. 21, 23

[49] How EM works. [Online]. Available: https://www.sonnetsoftware.com/products/sonnet-suites/how-EM-works.html 23

[50] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," IEEE Transactions on Microwave Theory and Techniques, vol. 36, no. 7, pp. 1151–1159, 1988. 29

[51] M. Roberg and Z. Popović, "Analysis of high-efficiency power amplifiers with arbitrary output harmonic terminations," IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 8, pp. 2037–2048, Aug 2011. 29, 62

[52] S. Shukla and J. Kitchen, "GaN-on-Si switched mode RF power amplifiers for non-constant envelope signals," in 2017 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), Jan. 2017, pp. 88–91. 29

[53] A. Z. Markos, K. Bathich, D. Gruner, O. Bengtsson, and G. Boeck, "A 4W GaN power amplifier for C-band application," in German Microwave Conference Digest of Papers, March. 2010, pp. 118–121. 29

[54] M. R. Hasin, J. Kitchen, and B. Ardouin, "GaN-on-Si transformer-coupled class D power amplifier," in 2015 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR), Jan. 2015, pp. 1–3. 30

[55] S. C. Cripps, RF Power Amplifiers for Wireless Communications, 2nd ed. Artech House, 2006. 31, 32

[56] R. Mavaddat, Network Scattering Parameters. World Scientific Publishing Co. Pte. Ltd., 1996, pp. 84, 99–103, 151. 32, 39, 42, 48, 49

[57] S. R. Schafer, "Carrier and envelope frequency measurements for supply-modulated microwave power amplifiers," Ph.D. dissertation, University of Colorado Boulder, 2015, pp. 146. 32, 88, 118

[58] C. Campbell, Microwave Monolithic Power Amplifier Design. John Wiley & Sons, Inc., 2013, pp. 1–17. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/047134608X.W8180 33, 34, 68, 69, 84

[59] B. S. Yarman and H. J. Carlin, "A simplified "real frequency" technique applied to broad-band multistage microwave amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 30, no. 12, pp. 2216–2222, 1982. 39, 47, 54

[60] H. Carlin and B. Yarman, "The double matching problem: analytic and real frequency solutions," IEEE Transactions on Circuits and Systems, vol. 30, no. 1, pp. 15–28, 1983. 39, 54

[61] Y. Wu, Y. Su, and P. Zhang, "The analytic theory of semiuniform lossy broadband matching networks," in 1988 IEEE International Symposium on Circuits and Systems (ISCAS), 1988, pp. 2773–2776 vol.3. 39

[62] E. Kerherve, P. Jarry, and P. M. Martin, "Design of broad-band matching network with lossy junctions using the real-frequency technique," IEEE Transactions on Microwave Theory and Techniques, vol. 46, no. 3, pp. 242–249, 1998. 39

[63] H. J. Carlin and A. B. Giordano, Network Theory: An Introduction to Reciprocal and Nonreciprocal Circuits. Prentice-Hall, Inc., 1964, pp. 269–277. 39, 40, 41

[64] C. R. Chappidi and K. Sengupta, "Globally optimal matching networks with lossy passives and efficiency bounds," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 257–269, 2018. 39

[65] V. Belevitch, "Elementary applications of the scattering formalism in network design," IRE Transactions on Circuit Theory, vol. 3, no. 2, pp. 97–104, 1956. 47

[66] G. Gonzalez, Microwave Transistor Amplifiers: Analysis and Design, 2nd ed. Prentice-Hall, Inc., 1997. 49

[67] H. W. Bode, Network Analysis and Feedback Amplifier Design. New York: Van Nostrand, 1945. 50

[68] S. Darlington, "Synthesis of reactance 4-poles which produce prescribed insertion loss characteristics: Including special applications to filter design," Journal of Mathematics and Physics, vol. 18, no. 1-4, pp. 257–353, 1939. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/sapm1939181257 50, 51, 52

[69] R. M. Fano, "Theoretical limitations on the broadband matching of arbitrary impedances," Journal of the Franklin Institute, vol. 249, no. 1, pp. 57 – 83, 1950. 50, 52, 53

[70] A. R. Kerr, "Some fundamental and practical limits on broadband matching to capacitive devices, and the implications for SIS mixer design," IEEE Transactions on Microwave Theory and Techniques, vol. 43, no. 1, pp. 2–13, 1995. 51, 52

[71] C. Berrached, D. Bouw, M. Camiade, and D. Barataud, "Wideband high efficiency high power GaN amplifiers using MIC and quasi-MMIC technologies," in 2013 European Microwave Conference, 2013, pp. 1395–1398. 52

[72] J. Xia, X. W. Zhu, and L. Zhang, "A linearized 2–3.5 GHz highly efficient harmonic-tuned power amplifier exploiting stepped-impedance filtering matching network," IEEE Microwave and Wireless Components Letters, vol. 24, no. 9, pp. 602–604, 2014. 54

[73] M. Olavsbråten, T. Mathiesen, and E. Berry, "Design of an efficient wideband (1–5GHz) 10W PA in GaN technology using harmonic tuning," in 2017 IEEE 18th Wireless and Microwave Technology Conference (WAMICON), 2017, pp. 1–5. 54, 80

[74] D. Pozar, Microwave Engineering, 4th ed. John Wiley & Sons, Inc., 2015. 54

[75] P. Zurek and Z. Popović, "Non-conjugate double-matching networks," Submitted to the IEEE Microwave and Wireless Components Letters, pp. 1–4, 2021. 57, 108, 110, 111, 121

[76] ——, "Broadband efficient flat-gain diplexed power amplifier for concurrent signals," Submitted to the IEEE Transactions on Microwave Theory and Techniques, pp. 1–11, 2021. 57, 108, 110, 111, 121

[77] G. Nikandish, E. Babakrpur, and A. Medi, "A harmonic termination technique for single- and multi-band high-efficiency class-F MMIC power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 5, pp. 1212–1220, May 2014. 58, 59, 64, 72

[78] J. Shao, D. Poe, H. Ren, B. Arigong, M. Zhou, J. Ding, R. Zhou, H. S. Kim, and H. Zhang, "Dual-band microwave power amplifier design using GaN transistors," in 2014 IEEE 57th Int. Midwest Symp. Circ. Syst. (MWSCAS), Aug 2014, pp. 559–562. 58, 60, 64

[79] E. Arabi, P. E. de Falco, J. Birchall, K. A. Morris, and M. Beach, "Design of a triple-band power amplifier using a genetic algorithm and the continuous mode method," in 2017 IEEE Topical Conf. RF/Microwave Power Ampl. Radio Wireless Appl. (PAWR), Jan 2017, pp. 48–51. 58, 64

[80] C. Sanchez-Perez, M. Ozen, C. M. Andersson, D. Kuylenstierna, N. Rorsman, and C. Fager, "Optimized design of a dual-band power amplifier with SiC varactor-based dynamic load modulation," IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 8, pp. 2579–2588, Aug 2015. 58, 64

[81] R. Kalyan, K. Rawat, and S. K. Koul, "Design of reconfigurable concurrent dual-band power amplifiers using reconfigurable concurrent dual-band matching network," in 2016 IEEE MTT-S Int. Wireless Symp. (IWS), March 2016, pp. 1–4. 58, 64

[82] S. K. Zhu, Q. F. Cheng, h. P. Fu, H. F. Wu, and J. G. Ma, "A highly efficient concurrent dual-band class-F power amplifier for applications at 1.7 and 2.14 GHz," in 2015 IEEE MTT-S Int. Microw. Symp., May 2015, pp. 1–4. 58, 64

[83] Q. F. Cheng, H. P. Fu, S. K. Zhu, and J. G. Ma, "Two-stage high-efficiency concurrent dual-band harmonic-tuned power amplifier," IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 10, pp. 3232–3243, Oct 2016. 58

[84] R. Quaglia, V. Camarchia, and M. Pirola, "Dual-band GaN MMIC power amplifier for microwave backhaul applications," IEEE Microwave and Wireless Components Letters, vol. 24, no. 6, pp. 409–411, June 2014. 59, 72

[85] A. Alizadeh, M. Frounchi, and A. Medi, "Dual-band design of integrated class-J power amplifiers in GaAs pHEMT technology," IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 8, pp. 3034–3045, Aug 2017. 59, 72

[86] G. Lv, W. Chen, X. Chen, and Z. Feng, "An energy-efficient Ka/Q dual-band power amplifier MMIC in 0.1-μm GaAs process," IEEE Microwave and Wireless Components Letters, vol. 28, no. 6, pp. 530–532, June 2018. 59, 72

[87] K. Choi, H. Park, M. Kim, J. Kim, and Y. Kwon, "A 6–18-GHz switchless reconfigurable dual-band dual-mode PA MMIC using coupled-line-based diplexer," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5685–5695, Dec 2018. 59, 72

[88] X. Chen, W. Chen, G. Su, F. M. Ghannouchi, and Z. Feng, "A concurrent dual-band 1.9-2.6-GHz Doherty power amplifier with intermodulation impedance tuning," in 2014 IEEE MTT-S Int. Microw. Symp. (IMS2014), June 2014, pp. 1–4. 64

[89] T. Cappello, A. Duh, T. W. Barton, and Z. Popović, "A dual-band dual-output power amplifier for carrier aggregation," IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 7, pp. 3134–3146, 2019. 64

[90] P. Zurek, T. Cappello, and Z. Popović, "A concurrent 2.2/3.9-GHz dual-band GaN power amplifier," in 2019 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), 2019, pp. 1–4. 78, 80, 111, 121

[91] D. Dening, "Multi-mode/ multi-band power amplifier," U.S. Patent 6 970 040 B1, 2005. 79

[92] A. Hadjichristos, P. H. See, B. Nejati, G. Klemens, J. N. L. Frederick, G. S. Sahota, M. Cassia, N. M. Pletcher, Y. Zhao, and T. A. Myers, "Multi-mode multi-band power amplifier module," U.S. Patent 8 971 830 B2, 2015. 79

[93] C. H. Lee, W. Kim, M. Ahn, J. Cha, Y. Park, and A. Hadjichristos, "Multi-mode multi-band power amplifiers," U.S. Patent 9 160 377 B2, 2015. 79

[94] A. Bettidi, A. Cetronio, M. De Dominicis, G. Giolo, C. Lanzieri, A. Manna, M. Peroni, C. Proietti, and P. Romanini, "High power GaN-HEMT microwave switches for X-band and wideband applications," in 2008 IEEE Radio Frequency Integrated Circuits Symposium, 2008, pp. 329–332. 79

[95] I. Lim and S. Lim, "Substrate-integrated-waveguide (SIW) single-pole-double-throw (SPDT) switch for X-band applications," IEEE Microwave and Wireless Components Letters, vol. 24, no. 8, pp. 536–538, 2014. 79

[96] J. B. Muldavin and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches. 2. design," IEEE Transactions on Microwave Theory and Techniques, vol. 48, no. 6, pp. 1053–1056, 2000. 79

[97] A. M. Mahmoud Mohamed, S. Boumaiza, and R. R. Mansour, "Reconfigurable doherty power amplifier for multifrequency wireless radio systems," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 4, pp. 1588–1598, 2013. 79

[98] D. Ji, J. Jeon, and J. Kim, "A novel load mismatch detection and correction technique for 3G/4G load insensitive power amplifier application," IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 5, pp. 1530–1543, 2015. 79, 120

[99] A. Grebennikov, N. Kumar, and S. B. Yarman, Broadband RF and Microwave Amplifiers. CRC Press, 11 2015. 80

[100] C. Duperrier, M. Campovecchio, L. Roussel, M. Lajugie, and R. Quere, "New design method of uniform and nonuniform distributed power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 49, no. 12, pp. 2494–2500, Dec 2001. 80

[101] K. Krishnamurthy, R. Vetury, S. Keller, U. Mishra, M. J. W. Rodwell, and S. I. Long, "Broadband GaAs MESFET and GaN HEMT resistive feedback power amplifiers," IEEE Journal of Solid-State Circuits, vol. 35, no. 9, pp. 1285–1292, Sep. 2000. 80

[102] B. Amado-Rey, Y. Campos-Roca, C. Friesicke, F. van Raay, H. Massler, A. Leuther, and O. Ambacher, "A G-band broadband balanced power amplifier module based on cascode mHEMTs," IEEE Microwave and Wireless Components Letters, vol. 28, no. 10, pp. 924–926, Oct 2018. 80

[103] R. J. Bayruns and J. VanSaders, "Wideband RF power amplifier for multi-mode multi-band applications," U.S. Patent 8 461 931 B1, 2013. 80

[104] M. R. Duffy, E. Berry, G. Lasser, and Z. Popović, "An efficient linearized octave-bandwidth power amplifier for carrier aggregation," in 2018 IEEE/MTT-S International Microwave Symposium - IMS, June 2018, pp. 473–476. 80, 99

[105] H. Taleb-Alhagh Nia and V. Nayyeri, "A 0.85–5.4 GHz 25-W GaN power amplifier," IEEE Microwave and Wireless Components Letters, vol. 28, no. 3, pp. 251–253, March 2018. 80, 99

[106] K. Chen and D. Peroulis, "Design of broadband highly efficient harmonic-tuned power amplifier using in-band continuous class-F^{-1}/F mode transferring," IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 12, pp. 4107–4116, Dec 2012. 80, 99

[107] P. Saad, C. Fager, H. Cao, H. Zirath, and K. Andersson, "Design of a highly efficient 2–4-GHz octave bandwidth GaN-HEMT power amplifier," IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 7, pp. 1677–1685, July 2010. 80, 99

[108] M. Roberg, M. Pilla, S. Schafer, T. R. Mya Kywe, R. Flynt, and N. Chu, "A compact 10W 2-20 GHz GaN MMIC power amplifier using a decade bandwidth output impedance transformer," in 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 261–264. 80

[109] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," IEEE Microwave and Wireless Components Letters, vol. 26, no. 6, pp. 443–445, 2016. 80

[110] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-input load modulated balanced amplifier with octave bandwidth," IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 12, pp. 5181–5191, 2017. 80

[111] X. Chen, W. Chen, F. M. Ghannouchi, Z. Feng, and Y. Liu, "Enhanced analysis and design method of concurrent dual-band power amplifiers with intermodulation impedance tuning," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 12, pp. 4544–4558, 2013. 80, 106

[112] P. A. Laporte, M. E. Rollins, and H. Cao, "Linearization of intermodulation bands for concurrent dual-band power amplifiers," U.S. Patent 9 385 762 B2, 2016. 80

[113] P. Roblin, C. Quindroit, N. Naraharisetti, S. Gheitanchi, and M. Fitton, "Concurrent linearization: The state of the art for modeling and linearization of multiband power amplifiers," IEEE Microwave Magazine, vol. 14, no. 7, pp. 75–91, 2013. 80

[114] R. M. Foster, "A reactance theorem," The Bell System Technical Journal, vol. 3, no. 2, pp. 259–267, 1924. 82

[115] P. Regalia and S. Mitra, "A class of magnitude complementary loudspeaker crossovers," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 35, no. 11, pp. 1509–1516, 1987. 87

[116] N. Dang-Duy, "A novel method for the design of broadband class E power amplifier with contiguous diplexer," in 2016 URSI Asia-Pacific Radio Science Conference (URSI AP-RASC), 2016, pp. 1–3. 87

[117] F. Raab, "Technique for wideband operation of power amplifiers," U.S. Patent 6 252 461, Aug 24, 1998. 87, 88, 93

[118] F. H. Raab, "Split-band modulator for Kahn-technique transmitters," in 2004 IEEE MTT-S International Microwave Symposium Digest (IEEE Cat. No.04CH37535), vol. 2, 2004, pp. 887–890 Vol.2. 87

[119] V. Yousefzadeh, E. Alarcon, and D. Maksimović, "Band separation and efficiency optimization in linear-assisted switching power amplifiers," in 2006 37th IEEE Power Electronics Specialists Conference, 2006, pp. 1–7. 87

[120] G. L. Matthaei, L. Young, and E. M. T. Jones, Microwave Filters, Impedance-Matching Networks, and Coupling Structures. New York, NY, USA: McGraw-Hill, 1964, ch. 4. 88, 115

[121] C. Nguyen, "Design and performance of novel printed-circuit spurline bandpass filters," IEEE Microwave and Guided Wave Letters, vol. 2, no. 11, pp. 437–438, 1992. 88

[122] R. Zhang and L. Zhu, "Design of a wideband bandpass filter with composite short- and open-circuited stubs," IEEE Microwave and Wireless Components Letters, vol. 24, no. 2, pp. 96–98, 2014. 88

[123] J. Xu, W. Wu, and C. Miao, "Compact microstrip dual-/tri-/quad-band bandpass filter using open stubs loaded shorted stepped-impedance resonator," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 9, pp. 3187–3199, 2013. 88

[124] J. X. Yun and R. G. Vaughan, "A view of the input reflection coefficient of the N-port network model for MIMO antennas," in 2011 IEEE International Symposium on Antennas and Propagation (APSURSI), 2011, pp. 297–300. 90

[125] J. P. Doane, K. E. Kolodziej, and B. T. Perry, "Simultaneous transmit and receive performance of an 8-channel digital phased array," in 2017 IEEE International Symposium on Antennas and Propagation USNC/URSI National Radio Science Meeting, 2017, pp. 1043–1044. 112

[126] H. Shaman and J. Hong, "A novel ultra-wideband (UWB) bandpass filter (BPF) with pairs of transmission zeroes," IEEE Microwave and Wireless Components Letters, vol. 17, no. 2, pp. 121–123, 2007. 119

[127] A. Keerti and A. H. Pham, "RF characterization of SiGe HBT power amplifiers under load mismatch," IEEE Transactions on Microwave Theory and Techniques, vol. 55, no. 2, pp. 207–214, 2007. 120

[128] H. Zargar, A. Banai, and J. C. Pedro, "A new double input-double output complex envelope amplifier behavioral model taking into account source and load mismatch effects," IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 766–774, 2015. 120

[129] A. Suárez, F. Ramírez, and S. Sancho, "Stability analysis of power amplifiers under output mismatch effects," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 10, pp. 2273–2289, 2014. 120

[130] P. Zurek and Z. Popovic, "Broadband diplxed power amplifier," U.S. Patent submitted, 2021. 121

[131] J. Estrada, P. Zurek, and Z. Popović, "Harvesting of aircraft radar altimeter sidelobes for low-power sensors," in 2018 International Applied Computational Electromagnetics Society Symposium (ACES), 2018, pp. 1–2. 121

[132] C. Cooke, P. Zurek, and Z. Popovic, "Harmonic generation with nonlinear transmission lines," Presentation, 2017 URSI National Radio Science Meeting. 121

[133] P. Zurek, M. Foreman, and Z. Popovic, "Ungrounded cpw gan-on-si pa mmic components," Presentation, 2018 URSI National Radio Science Meeting. 121

[134] G. Babur, O. A. Krasnov, A. Yarovoy, and P. Aubry, "Nearly orthogonal waveforms for MIMO FMCW radar," IEEE Transactions on Aerospace and Electronic Systems, vol. 49, no. 3, pp. 1426–1437, 2013.

[135] "Who needs RF when we can digitize at the antenna?" International Microwave Symposium Panel Session, IEEE, Los Angeles, CA, August 2020.

[136] K. Kurokawa, "Power waves and the scattering matrix," IEEE Transactions on Microwave Theory and Techniques, vol. 13, no. 2, pp. 194–202, March 1965.

[137] D. S. Ricketts, L. Xiaofeng, and H. D, "Electrical soliton oscillator," IEEE Transactions on Microwave Theory and Techniques, vol. 54, no. 1, pp. 373–382, 2006. 143

[138] D. A. Frickey, "Conversions between S, Z, Y, H, ABCD, and T parameters which are valid for complex source and load impedances," IEEE Transactions on Microwave Theory and Techniques, vol. 42, no. 2, pp. 205–211, Feb 1994.

[139] L. Marzall and Z. Popović, "An X-band quasi-circulator GaAs MMIC," in 2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), 2019, pp. 1–4.

[140] N. Yanduru, R. Monroe, and M. Brobston, "Apparatus and method for a switched capacitor architecture for multi-band Doherty power amplifiers," U.S. Patent 8 576 010 B2, 2013.

[141] J. B. Muldavin and G. M. Rebeiz, "High-isolation CPW MEMS shunt switches. 1. modeling," IEEE Transactions on Microwave Theory and Techniques, vol. 48, no. 6, pp. 1045–1052, 2000.

[142] IEEE Standard for Information technology– Telecommunications and information exchange between systems Local and metropolitan area networks– Specific requirements–Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications–Amendment 4: Enhancements for Very High Throughput for Operation in Bands below 6 GHz., IEEE Std 802.11ac-2013 (Amendment to IEEE Std 802.11-2012, as amended by IEEE Std 802.11ae-2012, IEEE Std 802.11aa-2012, and IEEE Std 802.11ad-2012), 2013.

[143] R. Quaglia, V. Camarchia, T. Jiang, M. Pirola, S. Donati Guerrieri, and B. Loran, "K-band GaAs MMIC doherty power amplifier for microwave radio with optimized driver," IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 11, pp. 2518–2525, 2014.

[144] F. Raab, "Wideband, minimum-rating filters and multicouplers for power amplifiers," U.S. Patent 6 552 634 B1, Apr 22, 2003.

[145] C. Quindroit, N. Naraharisetti, P. Roblin, S. Gheitanchi, V. Mauer, and M. Fitton, "FPGA implementation of orthogonal 2D digital predistortion system for concurrent dual-band power amplifiers based on time-division multiplexing," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 12, pp. 4591–4599, 2013.

[146] C. Nguyen, "Miniaturized multi-octave band-pass filters," in IEEE Antennas and Propagation Society International Symposium. 1995 Digest, vol. 2, 1995, pp. 1210–1213 vol.2.

[147] N. D. Lopez, X. Jiang, D. Maksimovic, and Z. Popović, "Class-E power amplifier in a polar EDGE transmitter," in 2006 IEEE MTT-S International Microwave Symposium Digest, 2006, pp. 785–788.

[148] D. J. Shepphard, J. Powell, and S. C. Cripps, "A broadband reconfigurable load modulated balanced amplifier (LMBA)," in 2017 IEEE MTT-S International Microwave Symposium (IMS), 2017, pp. 947–949.

[149] M. R. Duffy, G. Lasser, G. Nevett, M. Roberg, and Z. Popović, "A three-stage 18.5–24-GHz GaN-on-SiC 4 W 40 % efficient MMIC PA," IEEE Journal of Solid-State Circuits, vol. 54, no. 9, pp. 2402–2410, 2019.

[150] P. Chen, S. He, X. Wang, and Z. Dai, "1.7/2.6 GHz high-efficiency concurrent dual-band power amplifier with dual-band harmonic wave controlled transformer," Electronics Letters, vol. 50, no. 3, pp. 184–185, January 2014.

[151] C. Huynh, J. Bae, and C. Nguyen, "A millimeter-wave 0.18-um BiCMOS dual-band power amplifier," in 2014 IEEE Int. Wireless Symp. (IWS 2014), March 2014, pp. 1–3.

[152] M. L. Chuang, "Dual-band impedance transformer using two-section shunt stubs," IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 5, pp. 1257–1263, May 2010.

[153] L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, and C. R. Giardina, "A robust digital baseband predistorter constructed using memory polynomials," IEEE Transactions on Communications, vol. 52, no. 1, pp. 159–165, Jan 2004.

[154] M. R. Duffy, G. Lasser, J. Vance, M. Olavsbråten, T. Barton, and Z. Popović, "Bandwidth-reduced supply modulation of a high-efficiency X-band GaN MMIC PA for multiple wideband signals," in 2017 IEEE MTT-S Int. Microw. Symp. (IMS), June 2017, pp. 1850–1853.

[155] A. Duh, S. Rahimizadeh, T. Barton, and Z. Popović, "A 3.5/5.9-GHz dual-band output matching network for an efficiency-optimized multiband power amplifier," in 2018 IEEE Topical Conf. RF/Microw.Power Amp. Radio Wireless Appl. (PAWR), Jan 2018, pp. 75–78.

[156] A. Jarndal, A. Z. Markos, and G. Kompa, "Improved modeling of GaN HEMTs on Si substrate for design of RF power amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 59, no. 3, pp. 644–651, March. 2011.

[157] A. Jarndal, P. Aflaki, L. Degachi, A. Birafane, A. Kouki, R. Negra, and F. M. Ghannouchi, "On the large-signal modeling of AlGaN/GaN HEMTs for RF switching-mode power amplifiers design," in 2009 Asia Pacific Microwave Conference, Dec. 2009, pp. 2356–2359.

[158] R. Garg, Analytical and Computational Methods in Electromagnetics. Boston, MA: Artech House, 2008.

[159] J. Verspecht, "Generation and measurement of a millimeter-wave phase dispersion reference signal based on a comb generator," in 2016 IEEE MTT-S International Microwave Symposium (IMS), May 2016, pp. 1–4. 135

[160] Q. Li, W. Jiang, Y. Xu, and F. Nian, "Analysis and design of wide-band comb generator based on SRD," in 2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT), vol. 1, May 2012, pp. 1–3. 135

[161] P. Srivastava, P. P. Kumar, and C. V. N. Rao, "Design and development of multi-frequency comb generator for space borne microwave active sensors," in 2008 International Conference on Recent Advances in Microwave Theory and Applications, Nov 2008, pp. 445–447. 135

[162] E. Carman, M. Case, M. Kamegawa, R. Yu, K. Giboney, and M. Rodwell, "V-band and W-band broadband, monolithic distributed frequency multipliers," in 1992 IEEE MTT-S Microwave Symposium Digest, June 1992, pp. 819–822 vol.2. 135

[163] (2016) NLTL GaAs comb generators. [Online]. Available: https://www.macom.com/products/frequency-generation/nltl-gaas-comb-generators/ 135

[164] J. Breitbarth, "Design and characterization of low phase noise microwave circuits," Ph.D. dissertation, University of Colorado Boulder, 2006. 135, 142

[165] M. Remoissenet, Waves Called Solitons, 3rd ed. Berlin: Springer, 1999. 136

[166] P. P. Labs, "A new breed of comb generators featuring low phase noise and low input power," IEEE Microwave Journal, vol. 49, no. 5, pp. 278–280, May 2006. 142

[167] M. J. W. Rodwell, M. Kamegawa, R. Yu, M. Case, E. Carman, and K. S. Giboney, "GaAs nonlinear transmission lines for picosecond pulse generation and millimeter-wave sampling," IEEE Transactions on Microwave Theory and Techniques, vol. 39, no. 7, pp. 1194–1204, Jul 1991. 136

Appendix A

Harmonic Comb Generation

A.1 Motivation

Comb generators are used as phase-locked frequency multipliers in high-frequency measurement systems, e.g. [159], or for local oscillators in multi-carrier broadband communications systems. Step recovery diodes (SRDs) commonly used for harmonic generation, e.g. [160], can generate narrow pulses but have poor phase noise characteristics due to added shot and recombination noise. Switching-type BJT circuits have also been explored in [161], but require complicated circuit designs, as output power typically falls off rapidly at high frequencies. Compared to SRD and BJT circuits, varactor based non-linear transmission lines (NLTLs) allow a wider range of input frequencies in a single circuit. Much of the previous analysis of NLTL frequency generators focuses on single frequency multipliers using the second or third harmonic [162]. NLTLs are capable of producing higher order harmonics, allowing for higher frequency multiplication and have been shown to result in phase noise at the theoretical limit of $20\log N$, where N is the multiplication factor [164]. Commercially available NLTL comb generators are implemented monolithically in GaAs [163], while the goal of this chapter is to perform a study with low-cost hybrid circuits.

Considered are several hybrid NLTL wideband low phase noise comb generator circuits with hyperabrupt varactor diodes periodically loaded along a CPW transmission line. Two broadband input frequency ranges are considered: 50 MHz to 150 MHz and 500 MHz to 1000 MHz. A study of harmonic output power level optimization is performed to the 10^{th} harmonic as a function of input power, varactor diode characteristics, diode spacing, diode bias, and line impedance. Transmission

line and soliton propagation theory are examined to explore the limitations of harmonic generation using NLTLs. Characteristics of commercially available diodes are analyzed to optimize higher order harmonic output power levels. Nonlinear harmonic balance simulations with Spice diode models are used to simulate the behavior of several different comb generators in order to observe trends and make quantitative conclusions.

A.2 Background

The hybrid circuits considered here are comprised of a CPW line periodically loaded with hyperabrupt varactor diodes. Diodes are placed in parallel to balance the CPW structure, shown in Fig. A.1(a), with a photograph of one of the lines shown in Fig. A.2. Each line segment and parallel diode section can be modeled as the transmission line shown in Fig. A.1(b). A 75 Ω CPW line is chosen, as higher impedance lines have lower capacitance, which increases the influence of the nonlinear shunt capacitance over the linear CPW capacitance accumulated over the length of the line connecting two adjacent diodes.

The soliton wave equation of the transmission line, including dispersion and nonlinear capacitance, is given by [165]:

$$\frac{d^2V}{dt^2} - \frac{\delta^2}{L_{CPW}C_j}\frac{d^2V}{dz^2} = \frac{\delta^4}{12L_{CPW}C_j}\frac{d^4V}{dz^4} + \frac{bd^2V}{dt^2} \tag{A.1}$$

where $V(z,t)$ is the voltage along the line, b is the nonlinearity slope of the capacitance-voltage curve, δ is the dispersion constant, and v_0 is the wave velocity at the beginning of the line ($z = 0$). The solution for $V(z,t)$ is given by [165], [167].

$$V(z,t) = \frac{3(v^2 - v_0^2)}{2bv^2} \cdot \operatorname{sech}^2\left[\frac{\sqrt{3(v^2 - v_0^2)}}{v_0}\frac{(z - vt)}{\delta}\right] \tag{A.2}$$

A continuous sinusoidal RF input generates a soliton pulse train in the time domain, shown in Fig. A.3(a) for parameters that are close to the measured pulse width given in the next section. In the frequency domain this response has a Gaussian envelope, with the 10^{th} harmonic at -21 dBc.

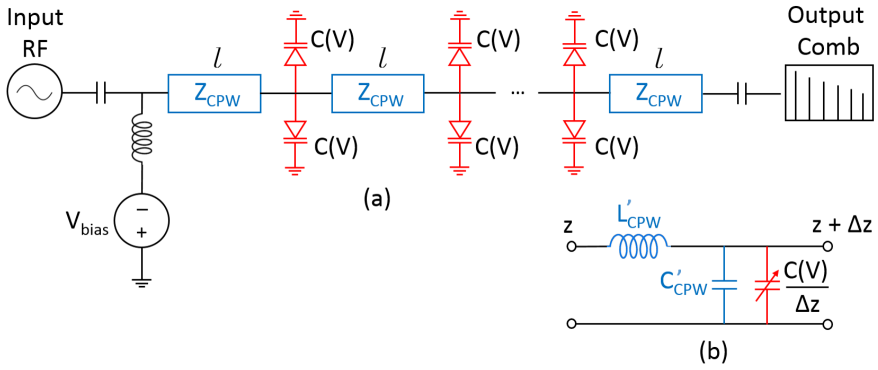


Figure A.1: (a) NLTL circuit schematic, consisting of a length of CPW line with varactor diodes connected in shunt. (b) Lossless NLTL transmission-line unit cell model with nonlinear shunt diode capacitance averaged over line length between two diodes, where L'_{CPW} and C'_{CPW} are the line distributed parameters.

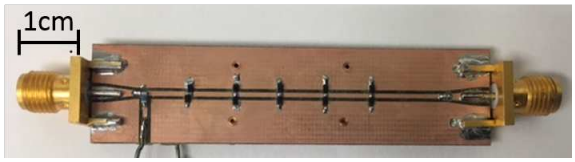


Figure A.2: 500 MHz to 1000 MHz input frequency NLTL fabricated with Skyworks SMV1247 diodes. The diode spacing is 7.7 mm, input power is 24 dBm, and reverse bias is 3.2 V.

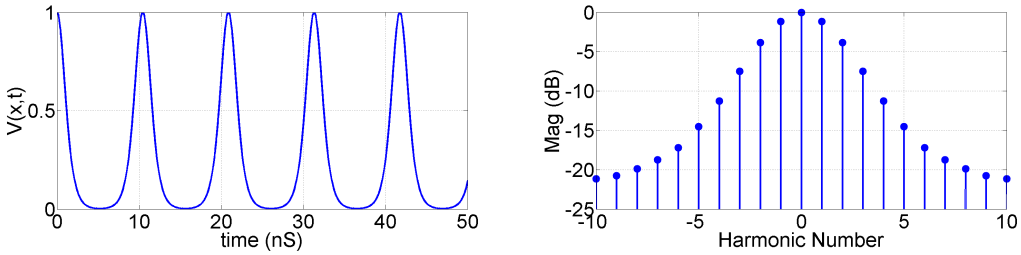


Figure A.3: (a) Soliton pulse train described by (1) with normalized voltage, pulse width is on the order of nanoseconds. (b) Gaussian shaped envelope of the harmonic output comb in frequency domain.

This pulse shape has a fast drop-off in harmonic power and needs to be modified in order to produce 2^{nd} through 10^{th} harmonics with improved uniformity of relative power distribution. In order to do that, a study is performed in terms of properties that can increase output power levels at harmonics above 5^{th} order.

A.3 Varactor Diode Characteristics

CPW impedance (Z_{CPW}), diode spacing (Δz), and characteristics of commercially available varactor diodes, specifically the $C(V)$ nonlinearity and the parasitic reactances, are investigated in simulation for influence on frequency generation. Several circuit topologies are compared for highest output power from the 5^{th} through 10^{th} harmonic. Hyperabrupt varactor diodes have the greatest capacitance versus reverse voltage variation, given by:

$$C_j(V_r) = \frac{C_{j0}}{\left(1 + \frac{V_r}{V_j}\right)^M}, \tag{A.3}$$

where C_{j0} and V_j are the diode junction capacitance and voltage, respectively, and M is the nonlinearity factor. The parasitic capacitance C_p and lead inductance L_s (Fig. A.4) are also influential. Five diodes are compared to show how these properties effect harmonic generation, listed in Table A.1, where the red and blue numbers correspond to the red and blue spectral lines in Fig. A.5.

Fig. A.5 shows a comparison of the harmonic output power for various diode circuits, compared with an ideal Gaussian. The nonlinearity factor M is the most influential parameter on harmonic generation, and diode SMV1247 produces about 10 dB more power relative to the Gaussian envelope at the 5^{th} through 10^{th} harmonic. The parasitic capacitance C_p in the SMV1801 circuits lowers the contribution of the nonlinear capacitance to the overall output voltage and therefore diodes with lower C_p are chosen. At the frequencies presented in this paper, for $C_p > 1$ pF higher order harmonic generation is degraded. The spacing of the diodes along the line determines the

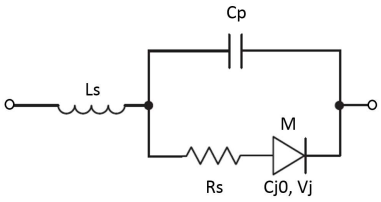


Figure A.4: Equivalent diode circuit showing the intrinsic junction capacitance and voltage, as well as basic package parasitics.

Table A.1: Skyworks Varactor Diode Characteristics

Diode (SMV-)	**1206**	**1247**	**1281**	**1801**	**2023**
C_{j0} (pF)	26.5	8.47	13	85	12.23
V_j (V)	1.1	80	14	10	4
M	**0.85**	70	6	4.4	1.4
C_p (pF)	0.25	0.54	0.62	**2.6**	0
L_s (nH)	0.7	0.7	1.2	0.8	1.5

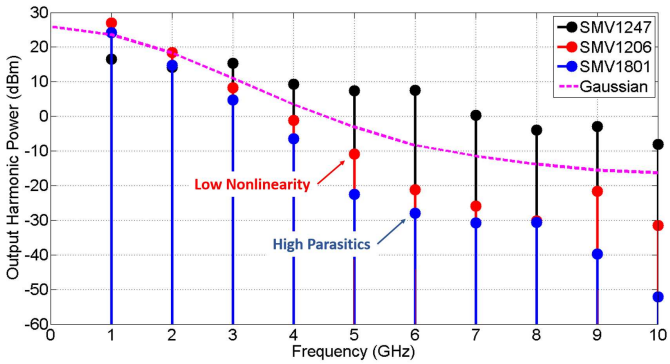


Figure A.5: Comparison of the simulated harmonic output power of select diodes. High M factor, junction capacitance (C_{j0}), and junction voltage (V_j) produce the most drastic capacitance variation. Packaging parasitics degrade harmonic level uniformity. The simulated half-voltage pulse width is approximately 3 ns for the SMV1247 NLTL with 1 GHz input frequency.

average impedance of the transmission line sections, which is important for low return loss. The diode spacing is optimized at discrete bias steps to provide the highest output power at the 5^{th} through 10^{th} harmonics.

A.4 Input Power and Reverse Bias

Fig. A.6 shows the capacitance curve of select diodes with a wide range of M factors. The bias levels that produce the highest 5^{th} through 10^{th} harmonic levels are marked along the capacitance curve at various input powers. Extremely nonlinear diodes, such as the SMV1247, produce the highest harmonic output power at lower bias levels where the capacitance ratio is greatest. For $M > 40$, the optimal bias level is chosen so the varactor does not enter forward conduction. In diodes with a lower M-factor, higher bias must be applied to generate the higher order harmonics.

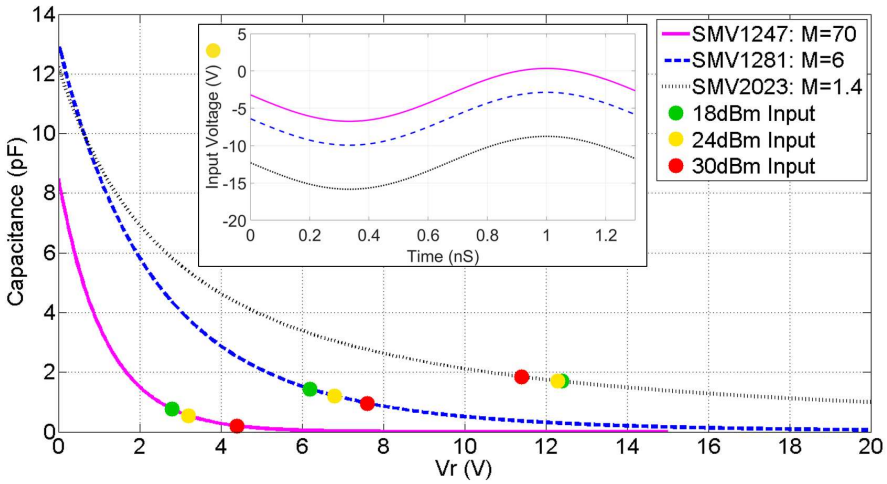


Figure A.6: Capacitance vs. reverse bias curves for select diodes. Ideal bias levels for various input powers are indicated by green, yellow, and red markers. Input sinusoid is shown for 24 dBm input with ideal bias.

When the nonlinearity is not as strong, the operating point moves away from the knee of the capacitance curve and relies on bias voltage increase to raise the harmonic power levels.

A.5 Experimental Results: Harmonic Generation

A hybrid NLTL is fabricated using the SMV1247 diode, with diode separation of 7.7 mm, input power of 24 dBm, and reverse bias of 3.2 V, shown in Fig. A.2. Harmonic output power is measured out to $10f_0$ with an f_0 of 500 MHz, 750 MHz, and 1000 MHz. The results are shown in Fig. A.8, and the harmonic levels range from about 20 dBm to -20 dBm. The diode spacing was optimized for f_0 =750 MHz and we begin to see impedance mismatches in the lower harmonics for f_0 =500 MHz. The spacing can be further tuned to reduce reflections across the band.

Several hybrid circuits are also designed and fabricated for the lower frequency range to demonstrate scalability of the design procedure, shown in Fig. A.7. In this case, the SMV1247 diode is used with a 2.8 V reverse bias and a 24 dBm input power. Output harmonic power levels for the 50-150 MHz range are shown in Fig. A.9, exhibiting similar harmonic levels as the higher frequency circuit. In all cases, the simulations predict the trends while the absolute level of harmonics is not as well predicted at the higher frequencies due to the limitations of the Spice model.

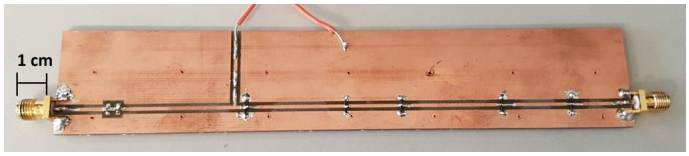


Figure A.7: 50 MHz to 150 MHz input frequency NLTL fabricated with SMV1247 diodes. The input power is 24 dBm, and reverse bias is 3.2 V.

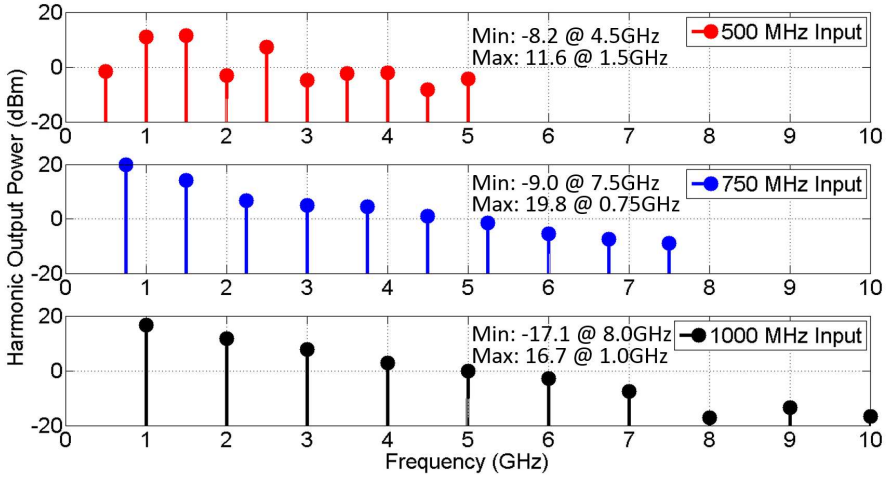


Figure A.8: Measured output harmonic levels over input frequency range of 500 MHz to 1000 MHz. The circuit is designed for f_0=750 MHz, but was shown to operate with 66% input bandwidth. At f_0, harmonics degrade by 28.8 dB over 10 harmonics.

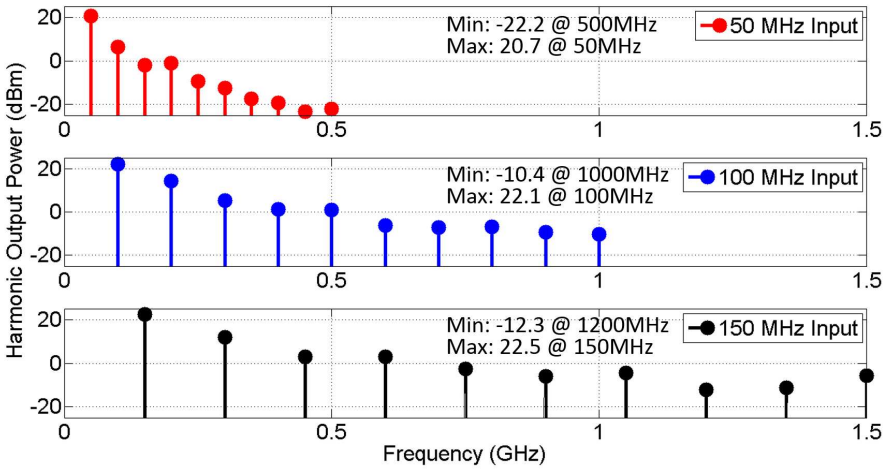


Figure A.9: Measured output harmonic levels over input frequency range of 50 MHz to 150 MHz. This circuit is shown to operate over 100% bandwidth with f_0=100 MHz.

A.6 Experimental Results: Phase Noise

Superior phase noise is one driving factor for the use of varactor-diode NLTLs. Residual phase noise measurements are performed using the frequency translated cross-correlated phase noise measurement system shown in Fig. A.10, where a very low phase noise crystal oscillator (Crystek) output is amplified with a linear Keysight instrumentation amplifier and divided into three paths, with top and bottom identical reference channels. The NLTLs on the outer reference paths serve to multiply the reference path frequency to mix with the harmonic of interest of the NLTL DUT. The cross-correlated phase noise measurement system operates similarly to a two-path discriminator system, but has two identical reference paths, allowing the phase noise contribution of the mixer and IF LNAs to be correlated out [164]. The phase noise of the reference path devices is also negligible, as only the noise common to both mixers is correlated. Absorptive filters (MiniCircuits) are used as diplexers to avoid reflections of the fundamental and the harmonics that are not in the pass-band.

This appendix shows the results of the 2^{nd} harmonic measured for an NLTL fabricated with SMV1247, SMV1281, and SMV2023 diodes with a 1000 MHz input frequency in Fig. A.11. This result will ideally scale with each harmonic as $20 \log N$. The highly nonlinear SMV1247 diode operates at a lower bias voltage, while SMV2023 operates near breakdown, suggesting that high bias voltages generate excess phase noise. Measurements achieve -154 dBc/Hz at 1 kHz offset and -163 dBc/Hz at 10 kHz offset. These results improve upon SRD circuits with similar parameters by as much as 15 dBc/Hz [166]. The spurs in the data are due to power supply and other external sources. In the NLTLs presented here, the biasing is done with a standard broadband bias-tee, but resistive bias techniques have been shown to lower the phase noise [164].

A.7 Summary and Future Work

Presented is a trade-off study of NLTL multiplier circuit parameters with a goal of increased power in higher-order harmonics. For commercially-available low-cost varactor diodes, the best

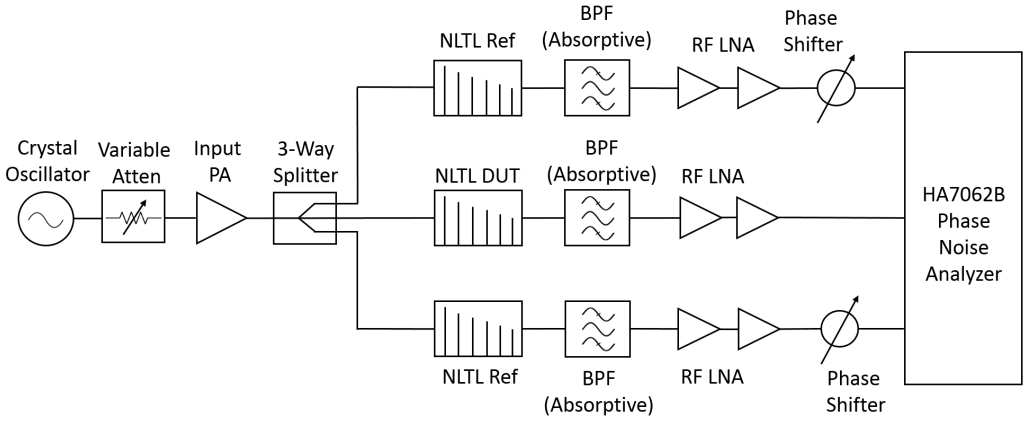


Figure A.10: Block diagram of a frequency translated cross-correlation phase noise measurement system. The phase noise from the center channel DUT is correlated, while noise generated from the source and reference paths are not.

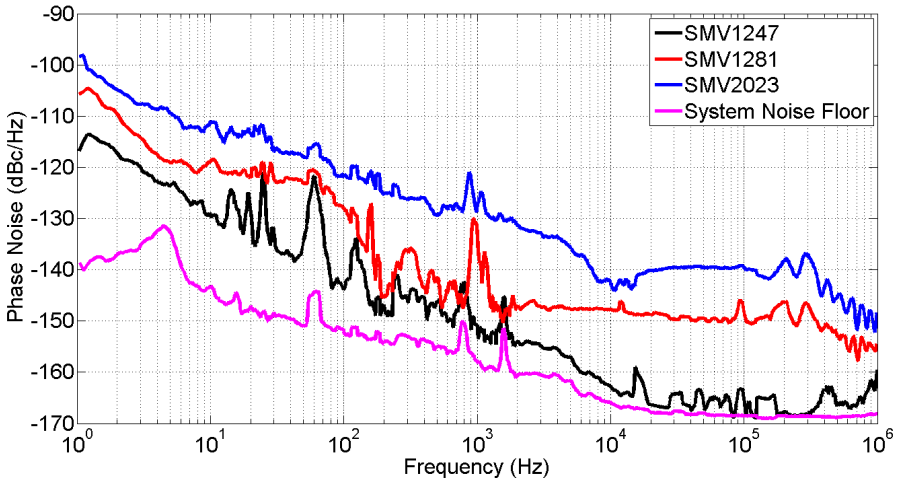


Figure A.11: Phase noise measurements of SMV1247, SMV1281, and SMV2023 diode NLTLs. Higher bias voltages produce higher phase noise. Highly nonlinear diodes are needed to not operate near breakdown for lower phase noise.

performing hybrid comb generator exceeds a Gaussian envelope by >10 dB at all harmonics above the 5^{th}. An in-house cross-correlation phase noise measurement system was used to evaluate phase noise performance at the various harmonics. The qualitative conclusions of this work have the potential to further improve characteristics of monolithically integrated NLTLs or resonator-based comb generators [137].