Broadband Diplexed Power Amplifier

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Abstract—We present a diplexed power amplifier (PA) architecture for achieving more than octave bandwidth with high efficiency. Two relatively narrowband single-stage PAs are connected with a contiguous diplexer-combiner network. The average efficiency across the larger than octave band is maintained with a flat gain response from 1.8 to 4 GHz. To maintain efficiency, the two transistors are biased in class B. One of the paths is turned on in each subband, and in the transition region, the two PAs power combine. In both element amplifiers, a 7-W Qorvo GaN packaged device is used to achieve approximately 35% fractional bandwidth, from 1.8 to 2.7 and 3 to 4 GHz, respectively. Averaged over the full band, the amplifier achieves an average measured power-added efficiency of 43.7%, the output power of 38.0 dBm, and the gain of 8.8 dB. Linearization using digital predistortion is demonstrated, with the benefit of reduced complexity due to the frequency isolation of the two PA branches.

Index Terms—Broadband amplifiers, gallium nitride (GaN), power amplifiers (PAs).

I. INTRODUCTION

BROADBAND power amplifiers (PAs) are becoming increasingly important for communications and radar [1]. Commonly used architectures include distributed, traveling-wave, feedback, and balanced configurations [2]. The first three can achieve decades of bandwidth [3], [4], while balanced PAs achieve around an octave [5]. Single-ended PAs have been designed to cover an octave or more, using methods such as stepped impedance lines [6]–[8], transferring from F^{-1} to F modes of operation [9], or resonating output transistor capacitance [10]. Here, we present an alternative 1.8–4-GHz PA architecture using a straightforward design method that is, in principle, scalable to wider bandwidths by increasing the number of PA paths. The PA block diagram and an example implemented circuit are shown in Fig. 1. Diplexer divider and combiner three-port networks connect element amplifiers PA$_1$ and PA$_2$, each operating over an approximate 35% bandwidth.

This work combines a stepped-impedance matching with a relatively simple diplexer design, enabling large overall bandwidth using two PA paths. Compared with a switched multiband PA, this approach has reduced active part count and
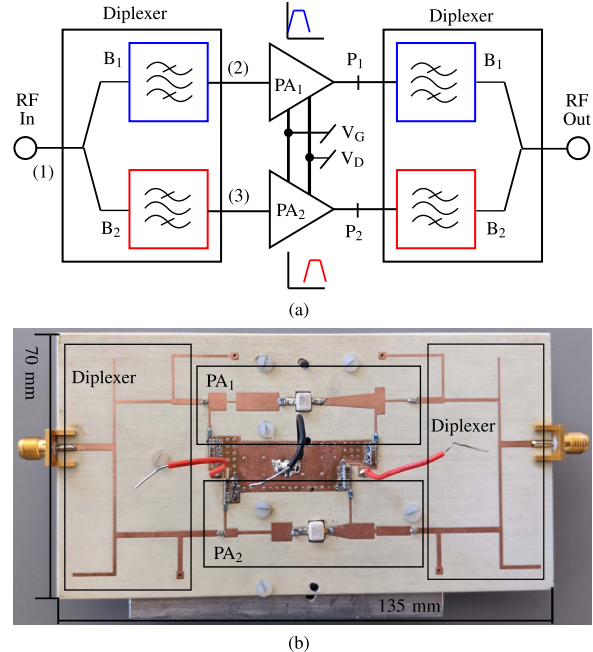
Fig. 1. (a) Broadband PA architecture, where diplexers connect efficient element PAs to cover the desired bandwidth. The transistors are biased in class B so that only one amplifier is turned on in each band. In the transition band, the diplexers act as power dividers/combiners. The diplexer ports are labeled in parentheses, and the two bands are B$_1$ and B$_2$. (b) Fabricated hybrid PA on a Rogers 4350B substrate operating from 1.8 to 4 GHz.

most significantly allows for amplification of multiple simultaneous widely spaced signals. Compared with a more standard broadband PA, the linearity is improved when amplifying concurrent signals. By combining two offset and relatively narrowband and efficient PAs with a diplexer (see Section II), performance can be maintained across both bands with a single RF input–output (see Section III). In addition, linearization becomes simpler to implement than in the case of a standard broadband PA (Section IV).

II. DIPLEXER AND ELEMENT PA DESIGN

It is essential that the diplexer has high isolation between ports (2) and (3) in Fig. 1 so that the input signal in each band only turns on one element class-B PA. Two bandpass filters (BPFs) are designed as the branches of a diplexer to introduce a transmission null in each reject band, using open stubs. To reduce combining losses, the filter is contiguous and matched in the transition region. Two frequency bands, B$_1$ and B$_2$, correspond to both the diplexer and the element PAs. In the implemented circuit, the lower band PA and $|S_{21}|$ of the diplexer cover $f_1 = 1.8$ GHz/1.6 GHz to $f'_1 = 2.8$ GHz/2.7 GHz, respectively, of B$_1$, while the
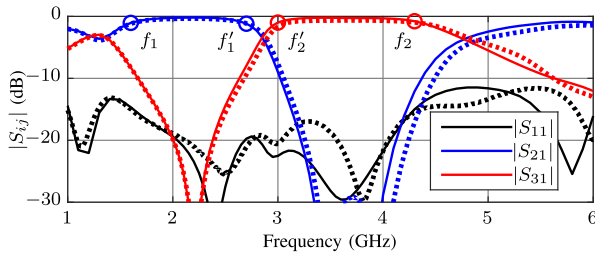
Fig. 2. Microstrip diplexer electromagnetically simulated (solid) and measured (dotted) results. The same diplexer is used to combine the two element PAs. Frequencies f_1, f_1' and f_2, f_2' used in the design process to obtain match in the transition band are labeled.

upper band PA and diplexer $|S_{31}|$ cover the range from $f_2' = 2.8$ GHz/3 GHz to $f_2 = 4$ GHz/4.3 GHz, respectively, of B_2. To minimize footprint, the diplexer microstrip networks consist of shunt open and shunt shorted stubs connected with transmission-line sections. After choosing the topology, the diplexer is designed iteratively using circuit and full-wave electromagnetic simulations.

A photograph of the fabricated diplexer within the full PA is shown in Fig. 1(b). The passive subcircuit was measured separately, and the results are plotted in Fig. 2. The diplexer maintains a measured insertion loss of 0.36–1.43 dB and better than a 15 dB reflection loss from 1.6 to 4.3 GHz. From frequencies where the insertion loss is 1 dB above the minimum loss in each band, the transition band of the diplexer is between $f_1' = 2.7$ GHz and $f_2' = 3$ GHz.

A center frequency of 3 GHz is chosen for this design with the goal of maximizing bandwidth. The T2G6000528-Q3 7 W Qorvo GaN packaged device is selected because it can operate from dc to 6 GHz with $P_{out} = 38$ dBm. While operating in one of the passbands B_1 or B_2, ideally, the other transistor will be turned off so that it does not draw power, keeping overall efficiency similar to that of a single-ended PA. Therefore, the transistors are biased near pinch-off in class B at 0.1% of I_{max}, where $V_{gate} = -3$ V, with an associated minimal (0.3% point) reduction in power-added efficiency (PAE) due to the other transistor's current draw.

Using stepped impedance lines, two 50-Ω element PAs operating in the passbands $B_1 = 1.8$–2.8 GHz and $B_2 = 2.8$–4 GHz are designed. Modelithics models are used for each of the lumped and active components. The transistor is simulated with a 0.17-nH source inductance and 0.8-Ω source resistance to account for mounting parasitics. Harmonic-balance and full-wave electromagnetic simulations are performed, with simulated and measured results in Fig. 3 for the two bands. Note that the gate bias had to be reduced to -3.4 V/0.4 mA from the nominal -3 V/3.6 mA predicted by the nonlinear model to exhibit a class-B gain. The two PAs maintain an average measured PAE over their respective bands of 55.3%/49.4% with average output power and a gain of 37.2 dBm/38.5 dBm and 10.0 dB/8.9 dB, respectively.

III. BROADBAND PA DESIGN AND PERFORMANCE

The two RF paths are split and combined with the same diplexer designed for 50-Ω ports. Previous related work in [11] uses a negative-component signal processor in the digital
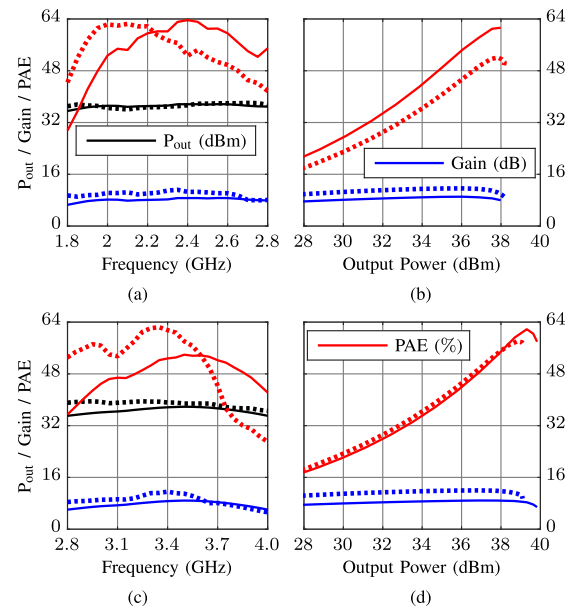

Fig. 3. Lower (a), (b) and upper-band (c), (d) PA simulated (solid) and measured (dotted) large-signal parameters, where (b) is measured at 2.5 GHz and (d) at 3.5 GHz. Both amplifiers are biased at -3.4 V/0.4 mA.

domain for splitting the two RF paths. Band splitting was also used in envelope modulators for envelope-tracking amplifiers up to 5 MHz in [12] and extended to 10 MHz [13].

Using the characterized diplexer (see Fig. 2) and the initial separate design of the element PAs, all matching networks are adjusted to improve performance in the transition band. Measurement results for the final PA are shown in Fig. 4. Note that the gate bias had to be reduced to -3.3 V/2.3 mA from -3 V/7.2 mA predicted by the nonlinear device model, to maintain class-B operation. Averaged over the band, an average measured PAE of 43.7% and corresponding average output power and gain of 38 dBm and 8.8 dB, respectively, are achieved. Because each element PA has PAE maximized within its corresponding band, there is a degradation in performance out-of-band, contributing to the drop in efficiency between B_1 and B_2. One could design the element PAs to be more efficient in the transition region with flat PAE, but maximal efficiency would drop. The relationship between the contiguous diplexers and element PAs is chosen to maintain constant gain and output power across the band.

Table I compares this work to similar broadband PAs. Although nonlinear simulations predict measurement trends, a frequency shift between the two contributes to performance degradation. Some possible reasons, resulting from previous experience with this device, include degradation of the device at higher frequencies and manufacturing tolerances. In addition, the operating point is in class B, whereas most transistor nonlinear models are validated for class A or AB, and therefore, some disagreement is expected.

For a fair comparison, a broadband PA is designed with the same Qorvo transistor and the same bias, following closely that in [6], with simple device replacement. Comparisons between the diplexed and broadband PA full-wave electromagnetic simulations show that average values of PAE, output power,

TABLE I
SUMMARY OF BROADBAND CONTINUOUS-WAVE (CW) PA PERFORMANCE

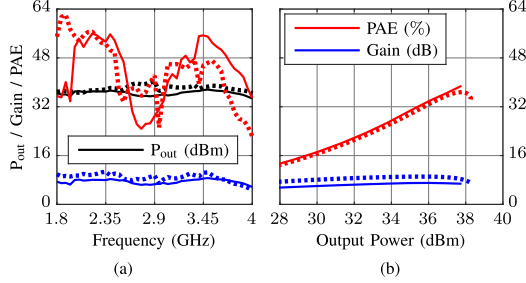| Ref.	Freq. (GHz)	PAE (%)	P_{out} (dBm)	Gain (dB)
[6]	2–4	48–62	40–42	9–10
[7]	1.9–4.2	40–61	40–40.8	11–12
[8]	0.85–5.4	45–55	43.5–45	8–9.5
[9]	1.3–3.3	55–78	40–40.4	10–13
[10]	1.9–4.3	48–62	40–41.8	9–11
This work	1.8–4	22.3–62	36.4–40.3	4.7–10.7

Fig. 4. Simulated (solid) and measured (dotted) large-signal parameters over frequency (a) and power at 3 GHz of (b) full circuit depicted in Fig. 1(b). The PA is biased at −3.3 V/2.3 mA.

and gain are 48%/49%, 39 dBm/39 dBm, and 8 dB/8 dB. This suggests that linearity can be improved without sacrificing performance as compared to a standard broadband PA.

IV. LINEARIZATION WITH DIGITAL PREDISTORTION

The nonlinearity seen in Fig. 4 will result in spectral regrowth when concurrent modulated signals are amplified. The goal of the diplexed architecture is to reduce additional distortion due to intermodulation between the two bands. Simple digital predistortion (DPD) can be implemented by using a 1-D memory polynomial model

$$z(n) = \sum_{m=0}^{M} \sum_{k=0}^{K} c_{mk} x(n-m)|x(n-m)|^k \tag{1}$$

where $x(n)$ is the original baseband signal to transmit, c_{mk} are the correction coefficients, $z(n)$ is the predistorter output, M is the memory order, and K is the nonlinearity order. When a single-ended broadband PA amplifies concurrent signals, cross-modulation distortion can be corrected using a more complicated 2-D memory polynomial model [14]

$$z_1(n) = \sum_{m=0}^{M} \sum_{i=0}^{K} \sum_{j=0}^{i} c_{1,mij} x_1(n-m)$$
$$\times |x_1(n-m)|^{i-j}|x_2(n-m)|^j$$
$$z_2(n) = \sum_{m=0}^{M} \sum_{i=0}^{K} \sum_{j=0}^{i} c_{2,mij} x_2(n-m)$$
$$\times |x_2(n-m)|^{i-j}|x_1(n-m)|^j \tag{2}$$

where the two baseband outputs, $z_1(n)$ and $z_2(n)$, of the predistorters are separately computed by two equations for

Fig. 5. (a) Measured gain dispersion and (b) output spectra at 2.5 GHz of the PA fed with two modulated 20-MHz multitone signals with peak powers of 29-dBm and 10-dB PAPR at 2.5 and 3.5 GHz. Red crosses are without DPD, blue points are with DPD, and dashed black lines depict the ideal case. Measurements are made with an NI PXIe-5646 200-MHz VST.
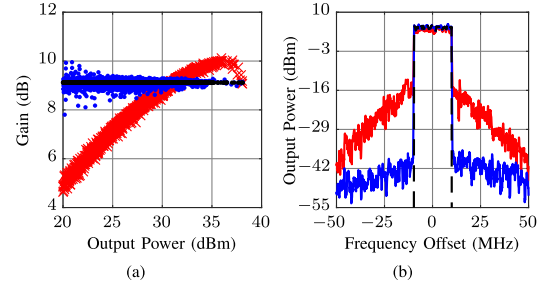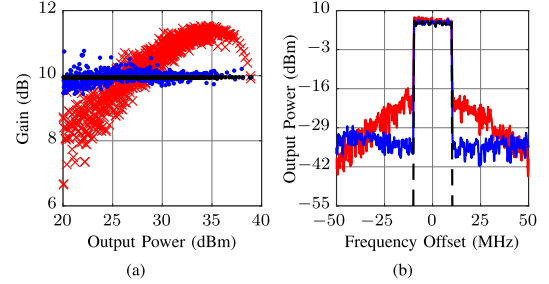

Fig. 6. (a) Measured gain dispersion and (b) output spectra at 3.5 GHz of the PA fed with two modulated 20-MHz multitone signals with peak powers of 29-dBm and 10-dB PAPR at 2.5 and 3.5 GHz. Red crosses are without DPD, blue points are with DPD, and dashed black lines depict the ideal case. Measurements are made with an NI PXIe-5645 80-MHz VST.

inputs $x_1(n)$ and $x_2(n)$. The digital complexity of the resulting 2-D memory polynomial in (2) scales as $N \times N = N^2$ [14]. The quadratic dependence can generate large memory requirements in the digital baseband, making the 2-D model less attractive. The broadband diplexed PA architecture reduces the requirements on the DPD complexity by virtue of isolation between the two PA branches. We separately model the two branches with 1-D memory polynomials, thus reducing the digital memory complexity from N^2 to $2N$.

This method is validated experimentally with two synchronized National Instrument VSTs (PXIe-5646 and PXIe-5645), with bandwidths of 200 and 80 MHz, respectively. At carrier frequencies of 2.5 and 3.5 GHz, two different 20-MHz multitone signals with peak powers of 29-dBm and 10-dB PAPR are generated, using the same test bench as in [15]. DPD is applied to linearize the full circuit, with Figs. 5(a) and 6(a) highlighting the gain dispersion and Figs. 5(b) and 6(b) the output spectra of the PA. With DPD, linearized gains are measured to be 8.6 and 10.7 dB in the two bands, while the average PAE drops from 21.3% to 19.2%. The ACLR improves from −24.7 dBc/−27.2 dBc to −41.6 dBc/−34.2 dBc, while the NRMSE improves from 18.7%/14.5% to 1.6%/2.6% at 2.5 GHz/3.5 GHz. It is noted that the linearity improvement in the upper band is limited by the 80-MHz bandwidth of the VST.

In summary, we demonstrate experimentally an efficient diplexed broadband PA with a relatively simple implementation of linearization for concurrent multiband signals. The architecture can potentially scale in bandwidth with the use of a multiplexer and more PA branches.

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