Design of Ungrounded CPW GaN-on-Si MMICs

Philip Zurek*, Myles Foreman*, Ryan Johnson†, Christopher Galbraith†, José Estrada*, and Zoya Popovic*
*Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, Colorado 80309-0425
†MIT Lincoln Laboratory, Lexington, Massachusetts 02421-6426

***Abstract*—This work presents a study of circuit component design in a new GaN-on-Si process being developed by the MIT Lincoln Laboratory. The process uses a thick silicon substrate with no through-vias with a multi-layer stack-up. Examples of components required for MMIC design include lines of various impedances, shorted and open stubs, tees, meander lines, and capacitors. Because the fabrication process requires the use of ungrounded CPW lines, underpasses are necessary to connect ground planes and a study of 50-Ohm lines with several underpass spacings is performed. The large range of dimensions and dielectric constants presents a challenge for full-wave simulations, and a comparison between Ansys HFSS and Sonnet Software is presented for a variety of passive circuit components implemented in the GaN-on-Si MMIC stack-up.**

I. Introduction

Gallium nitride (GaN) is established as a high-voltage semiconductor with broad applications, including those at microwave and millimeter-wave frequencies. At frequencies above UHF, MMIC passive and active circuit components with a GaN active layer are typically fabricated on a silicon carbide (SiC) substrate. However, SiC is expensive and not easily integrated with CMOS. To overcome this, GaN MMICs on silicon (Si) substrates are being developed that keep lag effects low [1], reduce the parasitic conduction layer [2], optimize device periphery [3], and integrate with CMOS [4].

In this work, we explore a different GaN-on-Si process under development at the MIT Lincoln Laboratory. A stack-up of the process is shown in Fig. 1, where a GaN active layer is epitaxially-grown on a high-resistivity Si substrate with three metal layers and no through-vias. AlGaN is used as a barrier layer (not shown). The fabrication process also includes high-electron mobility transistors (HEMTs) of varying gate lengths (from 120 to 200 nm), periphery, gate-source spacing, and gate-drain spacing. Metal structures are written using lithography. Several numerical challenges arise from the complex stack-up. The eight layer thickness ranges from 90 nm to 1.065 mm, while the guided wavelength at X-band is on the order of 15 mm. Appropriate port excitation and model de-embedding also need to be considered. In this paper, several CPW circuit components are designed and simulated using both Finite Element (FEM) Ansys HFSS and Method of Moments (MoM) Sonnet Software. Our goal is to establish which method agrees better with measurements.

Coplanar waveguide transmission lines can be evaluated using the conformal mapping method described in [5], which results in the characteristic impedance given by:

$$Z_{0cp} = \frac{30\pi}{\sqrt{\epsilon_{re}}} \frac{K'(k_1)}{K(k_1)}, \tag{1}$$

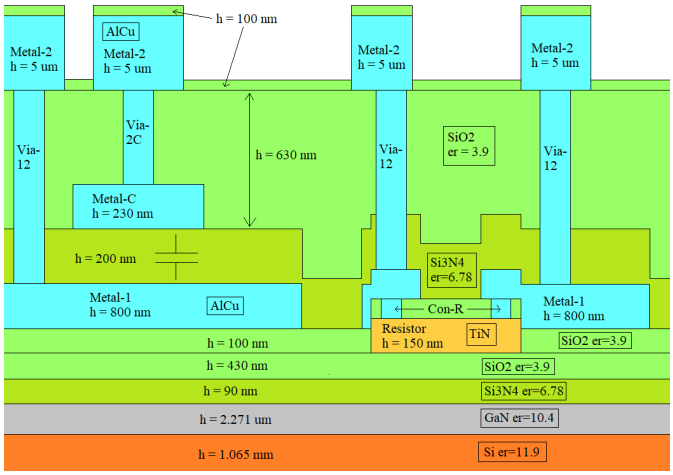

Fig. 1. GaN-on-Si process stack-up (not to scale). CPW lines are made in the Metal-2 layer (blue). Underpasses are made using the Metal-1 layer. Capacitors are made using Metal-C and Metal-1 layers. The various dielectrics and their permittivities are shown in green, GaN in purple and the Si substrate in orange. HEMT metal layers are omitted since this paper focuses on passive circuit components.

where K is the complete elliptic integral of the first kind (K' is its complement), k_1 is its argument, and ϵ_{re} is the effective dielectric constant. The constant ϵ_{re} can be determined as the weighted sum of each dielectric layer's filling factor and relative permittivity. This approach is used as a starting point in design, e.g., for a gap width of 34 μm and conductor line width of 40 μm, Z_{0cp} = 50 Ω. However, when simulated using HFSS, a gap width of 25 μm produced a 50-Ω line due to the influence of the conductor thickness, pointing to the need for detailed electromagnetic simulations.

II. Passive Component Design and Results

Because this GaN-on-Si process does not include through-vias to a ground plane, CPW transmission lines are used, whereas typical MMICs use microstrip transmission lines [1]. Along with the Metal-2 layer (see Fig. 1) used for the CPW lines, the Metal-1 layer is used to create underpasses to connect the CPW reference planes and for capacitor electrodes in conjunction with the Metal-C layer. An example ADS layout of a portion of a 50-Ω line with a λ/4 shunt shorted stub is included in Fig. 2. Because of the fringing fields associated with the inductive nature of the short, this line is modeled in ADS as having a length extension of 10 μm [5].

For a full stack-up model, Sonnet requires memory on the order of 30 GB for more complex circuit geometries, such as capacitors and meander lines, whereas HFSS requires 13 GB. In HFSS, lumped ports are used to excite the transmission

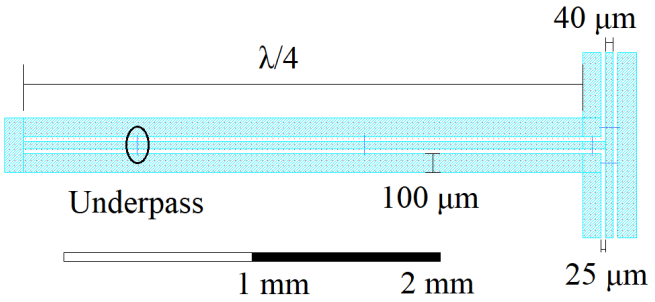

Fig. 2. ADS layout of a 50-Ω CPW line with $\lambda/4$ shunt shorted stub and $\lambda/10$ spaced underpasses, currently in fabrication. Labeled line width, gap width, and ground width are the same everywhere in this layout.

line so that the radiation boundary can be properly set up a distance $\lambda/10$ away. The shorted stub of Fig. 2, e.g., requires 8.35 hours to solve in Sonnet and 2.82 in HFSS with a full stack-up using a computer with 16 GB of RAM and an Intel i7 3.4 GHz processor.

To reduce simulation times, the stack-up is simplified by combining the two dielectric layers between Metal-2 and Metal-1 into a single homogeneous effective dielectric with a relative permittivity of 4.55 (1 % below weighted average). Similarly with the layers at Metal-1 and below, but not including Si, a second effective dielectric layer with relative permittivity 6.1 is included in the simulations (29 % below weighted average). The Si thickness was reduced to 600 μm by 44 %. These changes have little effect on performance, but decrease simulation times by about 95 % for complicated geometries.

Underpasses are added at varying intervals with necessary adjustments to produce varying impedance transmission lines, summarized in Table I. For the 50-Ω line with $\lambda/10$ spacing, plots of loss and $|S_{11}|$ for Z_L = 15 Ω are included in Fig. 3.

TABLE I. Varying Impedance Transmission Line Dimensions

ϵ_{re} HFSS	ϵ_{re} Sonnet	Underpass Spacing	Z_0	HFSS Line Width	HFSS Gap Width
4.96	5.06	none	50 Ω	40 μm	23 μm
5.61	5.38	$\sim \lambda/20$	50 Ω	40 μm	28 μm
5.20	5.18	$\sim \lambda/10$	50 Ω	40 μm	25 μm
5.11	5.01	$\sim \lambda/4$	50 Ω	40 μm	24 μm
4.83	5.05	$\sim \lambda/10$	30 Ω	74 μm	8 μm
4.83	4.95	$\sim \lambda/10$	75 Ω	16 μm	37 μm

Sonnet gives a resonant spike around 28 GHz due to the PEC boundaries imposed by the simulation method. The disagreement between the two simulations is about a 0.5 dB in $|S_{11}|$, 0.2 dB/mm in loss, with a nearly identical phase response (not plotted). It is found that each underpass adds about one effective degree of electrical line length. The ground plane width is also varied from 50 μm to 150 μm, with 100 μm chosen as the smallest distance that still gives expected performance.

The tee junction from Fig. 2 is simulated, separately from the entire circuit, in HFSS and Sonnet. Fig. 4 shows the tee and stub results. S-parameters demonstrate relatively good agreement between HFSS and Sonnet. Greater loss improves matching because more power is dissipated rather than reflected. Footprint miniaturization was studied on a four-turn

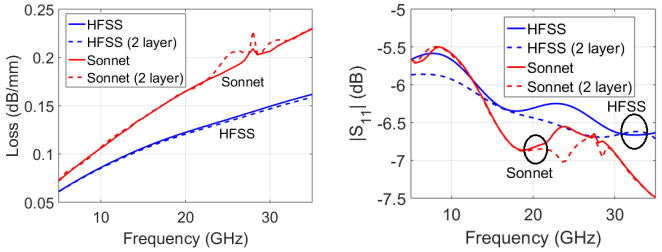

Fig. 3. (a) Loss (dB/mm) and (b) $|S_{11}|$ comparison between HFSS (gap = 25 μm) and Sonnet (gap = 21 μm) of a 50-Ω line with $\lambda/10$ underpass spacing. (a) is terminated in a 50-Ω load and (b) in a 15-Ω load.

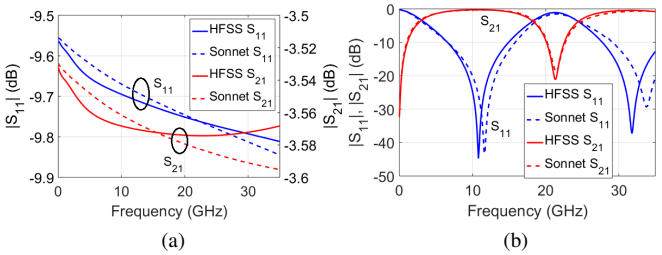

Fig. 4. HFSS and Sonnet S-parameters of: (a) tee junction and (b) quarter-wave shorted stub.

half-wavelength meander line with 100 μm ground plane width between lines requiring a 28 μm gap width to maintain 50-Ω characteristic impedance. In addition, they are about 20 % shorter due to coupling. As width between lines increases, the meander line length approaches a half-wavelength, as expected. Lumped components are also investigated. Using the stack-up of Fig. 1, 0.3 fF/μm^2 is expected for the capacitors. An HFSS simulated 60 μm x 80 μm DC blocking capacitor, e.g., has a capacitance of 1.55 pF at DC (1.44 pF calculated) and 1.46 pF at 10 GHz. Sonnet results in a DC capacitance of 1.58 pF for the same capacitor.

Acknowledgment

This work is supported under the Assistant Secretary of Defense (ASD) for Research and Engineering Contract No. FA8721-05-C-0002 and/or FA8702-15-D-0001. Any opinions, findings, conclusions or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the ASD.

References

[1] R. Leblanc, N. S. Ibeas, A. Gasmi, F. Auvray, J. Poulain, F. Lecourt, G. Dagher, and P. Frijlink, "6w ka band power amplifier and 1.2db nf x-band amplifier using a 100nm gan/si process," in 2016 IEEE CSICS, Oct. 2016, pp. 1–4.

[2] L. Pattison, T. Boles, N. Tuffy, and G. Lopes, "Improving gan on si power amplifiers through reduction of parasitic conduction layer," in 2014 9th EuMIC, Oct. 2014, pp. 92–95.

[3] J. Kim, H. Park, D. Kim, M. Lee, K. Seo, and Y. Kwon, "Rf parametric study on algan/gan hemts on si-substrate for millimeter-wave pa," in 2013 APMC Proceedings, Nov. 2013, pp. 775–777.

[4] T. E. Kazior, J. R. LaRoche, and W. E. Hoke, "More than moore: Gan hemts and si cmos get it together," in 2013 IEEE CSICS, Oct. 2013, pp. 1–4.

[5] K. C. Gupta, R. Garg, I. Bahl, and P. Bhartia, Microstrip Lines and Slotlines. Boston, MA: Artech House, 1996, pp. 375–451.