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SWITCHED-MODE MICROWAVE CIRCUITS FOR HIGH-EFFICIENCY TRANSMITTERS

by

MANOJA DAYAWANSA WEISS

B.S. Electrical Engineering, Grove City College, 1993

M.S. Electrical Engineering, Penn State University, 1995

A thesis submitted to the

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Switched-Mode Microwave Circuits for High-Efficiency Transmitters

Thesis directed by Professor Zoya Popović

In wireless communications systems, the transmit front-end consumes a large fraction of the total available power. In particular, the power amplifier preceding the antenna can consume more than 50% of the total average power. Therefore, increasing the power amplifier efficiency is essential to extend battery lifetime (e.g. on a satellite or in portable applications) and reduce power lost to heat that leads to thermal degradation of the electronics in the front end. Both these factors are important in reducing the total cost of the system. By integrating efficient power amplifiers in each unit cell of a transmit antenna array, a transmitter front-end may be optimized for efficient amplification and for combining the output of each unit cell in the low-loss medium of free space. In this thesis, traditionally low-frequency switched-mode class-E and -F high-efficiency amplifier circuits have been extended in operation to 10 and 20 GHz with record efficiencies ranging from a 74% efficient power amplifier at 10 GHz to a 42% efficient power doubler at 20.8 GHz. These circuits are designed for integration with antennas in an active array configuration.

The design of the 10 GHz class-E power amplifier is a non-conventional integrated circuit-field design well suited for active antenna arrays with small unit-cell size. A smaller unit cell size allows greater packing density in the array, which in turn allows for lower array losses, and therefore higher power combining efficiency. With the proper biasing and RF input to a class-E amplifier, the circuit presented to the output terminals of the MESFET enables high efficiency operation by offsetting the phase of the current relative that to the voltage waveform, thereby minimizing losses. This can be accomplished with an output circuit having a complex output impedance, whose imaginary part is used to adjust the phases of the current and

the voltage so that the device operates as a switch with minimal losses, while the real part of the impedance is the desired load to which the power is delivered. In this work, both standard 50 Ω loads and radiating (antenna) loads are considered. In the case of the antenna load, the best performance is achieved if the antenna and power amplifier are integrated. This is accomplished for an antenna impedance that is not purely real, but designed to be the optimal impedance for the class-E mode of operation. The implemented circuit with a non-resonant slot antenna exhibits a measured output power of 100 mW with 74% drain efficiency and 62% power-added-efficiency. In addition, the overall size is two times smaller than if a standard resonant antenna were connected to a PA designed for a standard 50 Ω load.

Having optimized unit cell efficiency and size using a novel integrated active antenna, suitable linearization methods must be applied when using these circuits in transmitter systems. In most modern wireless communications systems, the envelope-varying modulation techniques require linearity of the PA for low signal distortion. Linear amplifiers such as class-A and -B, on the other hand, have inherently low efficiencies; for example, the efficiency of class-A amplifiers is limited to 50%. Where high efficiency is needed, the solution is to linearize high-efficiency nonlinear amplifiers. In this work, an 8.4 GHz class-F PA was characterized when different linearization techniques are applied. The two-tone intermodulation distortion and overall efficiency were compared for the different techniques, leading to a technique for which the average efficiency for multicarrier signals was increased from 10% without linearization to 44% with linearization. With the linearization, the intermodulation distortion was reduced from -17 dBc to -28 dBc.

The carrier frequencies for commercial applications have been moving into the millimeter-wave region. For example, the 24 GHz unlicenced band has been extensively used in wireless sensor applications, and local to multipoint distribution systems (LMDS) have been allocated the 27-28 GHz range. As an alternative to

building low-phase-noise frequency-stable oscillators at high frequencies, often times a low-frequency, high quality, stable and low-cost oscillator is used to feed a chain of frequency multipliers which produce the desired carrier signal. To minimize heating of the temperature-sensitive oscillator, it is desirable to maximize the efficiency of the frequency multiplier chain while maintaining output power levels on the order of 0-10 dBm. The class-E topology is well suited for such an application.

In this thesis, the work in class-E PAs has been extended to a 10.4 to 20.8 GHz frequency doubler that achieved 0.83 dB conversion gain and 7.1 dBm output power with 42% drain efficiency and 31% overall efficiency. Nonlinear theoretical analysis of switched-mode frequency multipliers reveals that the drain voltage for a doubler must be 4 times smaller than for an amplifier with the same device. This limits the theoretical output power of a class-E doubler to a fourth of that obtained for an amplifier. A simplified technique for estimating the switching duty cycle is also formulated, since a doubler requires a 25% duty cycle to operate in class-E mode. This is harder to control than the 50% duty cycle required by a class-E amplifier. A sweep of bias points and input power is carried out to ascertain the best operating point for maximal efficiency with conversion gain greater than unity.

A design for a spatially combined frequency doubler array is presented as the conclusion to this study on high-efficiency transmitter front-ends. For constant envelope applications, this array may be used as the final stage in the transmitter, but for varying-envelope signals, an ampliifer stage amplitude-modulation through the bias must follow, since the frequency multipliers are extremely nonlinear and cannot be linearized by bias modulation.

DEDICATION

To Tim and Sita

I am always doing that which I cannot do, in order that I may learn how to do it.

- Pablo Picasso

If at first you don't succeed, try, try again.

Then give up. No use being a damned fool about it.

- W. C. Fields

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Many thanks to our friendly and very helpful secretary Rachael Tearle, and to Helen Frey, our longtime former secretary, without whom most of this work simply could not have been done in time. I'd also like to acknowledge the help of Pam Wheeler, who made sure my paperwork was always in order.

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The present members of the group are great to work with and have lunch on the Hill with. It was also very nice having McCoy Grill lunches with Naoyuki Shino while envying Darko Popović's appetizing home-cooked entres. Thank you to Srdjn Pajic, Stephania Romisch, and her husband Steve Jefforts who during a late, Italian-animated and red-eyed night, helped me formulate the calculation of

duty cycle presented in Ch. 7. Paul Smith is a source of good cheer in the lab, and I especially enjoying learning (fake) Kung Fu fighting to show Michael that cheery people can get angry too. Joe Hagerty's eye for detail in helping me put together cool graphics, and patient ear in listening to my tirades, were welcome. They say misery loves company; I was indeed fortunate to have Jan Peeters Weem defend the same day as I - his company through all the thesis-defense procedure was appreciated, even though sometimes it was hard to get him to be quiet and let me work (he was ahead and I was behind)!

At the end of this long list of people who have helped me to complete this work, come the least noticed but most important forces in my life: my parents, Amma and Thaathta, my sister, Anoma McCoy, and especially my husband, Tim Weiss, who have inspired me, supported me, and loved me through it all.

Thank you.

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CHAPTER 1

INTRODUCTION

1.1 Prologue

Wireless communication systems have advanced signficantly from the simple components Guglielmo Marconi used to transmit radio signals across the Atlantic ocean at the turn of the 20^{th} century. Today, mobile and satellite communications permeate all aspects of our lives. The number of mobile and cellular phones has skyrocketed in recent years while satellite communication traffic including international telephone calls and DBS-TV (direct broadcast satellite television) has also increased substantially.

Commercial cellular and PCS mobile communications [1] currently occupy the 800 MHz-2 GHz spectral region. Military and commercial satellite communications [2] including voice, data, and DBS-TV operate at higher frequencies ranging from 4-30 GHz, and are moving up higher to 60 GHz and beyond in order to facilitate higher data rates and a wider range of services. While the initial technological achievements in both mobile and satellite communications were geared to provide reliable service with wide functionality, there is a current focus on lowering the cost of service while maintaining superior quality. One of the main approaches to reducing system and operating costs is the conservation of system power resources and minimization of power wasted as heat. Of the approximately 250 W of power produced by the solar-cell arrays on a typical satellite, more than 125 W is dissipated as heat due to inefficient operation of the transmitter power amplifiers [2].

1.2 Reducing Costs by Conserving Power

The power amplifiers (PAs) in a wireless transmitter amplify the signal to high power levels before delivering it to the antenna for transmission. The transmit power should be high enough that the signal received at the destination is clear and within the error-tolerances of the receiver. For example, the power amplifier in a communications satellite has an output power level on the order of 40 W. To deliver this amount of power to the antenna, the PA consumes on average about 75% of the total available power [2]. If the PA operates at about 30% efficiency [2], then 70% of 75% of the total power is converted to heat. In other words, 52.5% of the total system power is dissipated as heat in the power amplifier.

During an eclipse, the satellite is powered by onboard batteries whose lifetime is limited by the unnecessary waste of power by conversion to heat. Battery lifetime is also of concern to the cellular phone user whose talk-time is cut short due to inefficient use of batter power. By using more efficient PAs in these transmitters, satellite solar-cell arrays may possibly be made smaller while batteries will last longer, lengthening the satellite lifetime as well. Cellular phone usage will be cheaper since batteries will last longer, while cellular base-stations can reduce costs by drawing less electricity.

The heat generated due to inefficient power usage in the power amplifiers not only wastes valuable solar-cell or battery power, but also causes thermal degradation of electronic devices and necessitates bulky heat-sinking measures to cool the transmitter. In addition to the cost-cutting benefits of increased power amplifier efficiency, reduced heat dissipation eases the heat-sinking requirements of the system. This is very important in satellite communications where thermal waste managment is a challenge due to the harsh environment of space where the temperature varies from approximately 4 K to hundreds of Kelvin when exposed to direct sunlight. Less heat-sinking also means less size and weight of the system, which directly translates

to further cost savings in the satellite launching process.

Some of the approaches being taken to improve the power-efficiency of transmitters include the use of high-efficiency power amplifiers [3], the formulation of power-efficient modulation techniques [4], and real-time power control of the power amplifiers [5]. The work presented in this thesis concentrates on the design of high-efficiency switched-mode power amplifiers which, through their nonlinear switching behaviour, are able to achieve practical efficiencies 10-30% higher than conventional PAs. As described in Ch. 6, increasing PA average efficiency from 30% to 50% lengthens battery lifetime by about a factor of 1.7 while reducing heat wasted by a factor of 2.3.

1.3 Switched-Mode Power Amplifiers and Frequency Multipliers

When using solid-state devices such as Field Effect Transistors (FETs) as switching power amplifiers, highly efficient operation can be obtained. This is because the voltage and current at the switch are nonzero at alternating time intervals, rendering the current-voltage product at any given time, to be ideally zero. This concept has been applied to power amplifiers at frequencies at UHF, VHF, and up to 5 GHz, while the work contained herein takes switched-mode PA operation to 10 GHz with 100 mW output power and an efficiency of over 30% above the manufacturer rating for conventional PA operation without switching. The power amplifiers discussed here are at X-band which is used in satellite communications. However, the work presented here is applicable for cellular communications as well.

The heat minimizing properties of switched-mode FETs are also suitable for high-efficiency frequency multipliers, which differ from power amplifiers in that the output is taken at a harmonic of the input frequency. FET frequency multipliers are part of the signal-generation circuitry in a transmitter. In this frequency-synthesis circuitry, a signal from a low-frequency, high-quality oscillator is multiplied up to

the desired frequency of operation to produce the local oscillator (LO) signal. In addition to wasting power, an inefficient multiplier chain which produces heating may contribute to changes in the oscillator which could cause the frequency to drift [6]. With this in mind, switched-mode high-efficiency FET frequency multipliers are investigated in this thesis as a method of minimizing heat-dissipation in the frequency-synthesis circuitry of a transmitter.

1.4 Organization of Thesis

As discussed in the previous sections, for purposes of maximizing the power-efficiency of a communications link, the key component to optimize is the transmitter power amplifier, since it handles high amounts of RF power. These power amplifiers are usually travelling wave tube amplifiers (TWTAs) and are based on vaccuum tube technology. A more attractive option that is gaining attention today is to use solid-state power amplifiers (SSPAs) which are small, light, and have longer lifetimes than TWTAs, though they have lower output power levels and are less efficient. Solid-state power amplifiers at X-band and higher are built around solid-state devices such as MEtal Semiconductor Field Effect Transistors (MESFETS), and High Electron Mobility Transistors (HEMTs). Since each device can handle only a limited amount of power, the combination of several single-device amplifiers is necessary to obtain the output power requirements of the satellite transmitter.

In this thesis, solid-state devices are used in nonlinear switched-mode power amplifier architectures previously demonstrated at frequencies up to 5 GHz. The switched-mode power amplifier design methodology is extended to X-band with output power ranging from 100 mW at 10 GHz to 1.7 W at 8.35 GHz. The DC-RF conversion efficiencies for these X-band PAs are 74% and 64% respectively. These architectures, such as class-E and -F PAs, are discussed in Ch. 2 in comparison with other classes of power amplifiers. The verification of X-band class-E and -F operation

from time-domain measurements is presented for the first time in Ch. 3.

Since the power levels obtained from these solid-state amplifiers are on the order of 1 W, power combining methods suitable for use in a 20-30 W transmitter system are compared in Ch. 4. These methods are: chip-level, circuit-level, and spatial power combining.

In the market-driven arena of cellular and PCS mobile communications, commercial organizations are recognizing the importance of high-efficiency power amplifiers in driving down costs without compromising performance figures of merit such as signal quality and system functionality. This has given rise to widespread interest in new fields such as the linearization of nonlinear high-efficiency PAs and promises to integrate the areas of microwave PA design, digital signal processing, communications, and power electronics to provide efficient and high-performance wireless communications around the 0.8-2 GHz cellular/PCS bands. To further this study into higher frequencies, a comparison of efficiency-enhancing linearization methods is carried out using a single 8.4 GHz switched-mode PA. This work is presented in Ch. 6 which discusses dynamic biasing methods for linear high-efficiency transmitters.

Ch. 5 presents an efficient and compact transmitter which has a class-E power amplifier at 10 GHz integrated with an antenna. This integration is done by designing the antenna to directly match the transistor output to the impedance necessary for class-E operation. This method avoids the use of separate matching circuitry at the transistor output and therefore minimizes output circuit losses and area. The transmitter is half the size of a conventional transmitter consisting of the PA, output matching circuitry, and a 50 Ω antenna.

As communication frequencies get into the millimeter-wave region to allow for larger bandwidth and higher data rates, the task of generating pure signals at these frequencies becomes more challenging. An alternative is to generate the signal

at a low-frequency and use frequency multipliers to obtain the desired LO signal. This method is more preferable than designing an oscillator at the desired frequency since it isolates the oscillator from the output of the power amplifier. This increases system stability and separates the heat-producing power amplifier stages from the temperature sensitive oscillator stage. Class-E frequency multipliers, introduced in Ch. 7, offer an energy- and cost-saving alternative to using diodes or class-A and -B frequency multipliers. A 10.4/20.8 GHz class-E frequency doubler with 31.6% overall efficiency, 7.1 dBm output power and 0.83 dB conversion gain is presented in Ch. 8.

Finally, in Ch. 9, the high points of this thesis are highlighted while future research endeavours in the area of high-efficiency microwave circuits, are suggested.

CHAPTER 2

THEORY OF SWITCHED-MODE CLASS-E AND -F POWER AMPLIFIERS

2.1 Definitions of Efficiency

The function of a power amplifier (PA) is to convert DC power to RF power by amplifying a given input RF signal. The efficiency with which this amplification takes place can be described in terms of drain efficiency, η_D, power-added efficiency, PAE, and overall efficiency, η.

Drain efficiency, or DC-RF conversion efficiency, is a measure of how well the DC power is converted to output RF power, while PAE indicates the gain of the amplifier as well, since it is the ratio of the difference in output and input power to the DC power. Overall efficiency is a good indicator of system heat output since it compares total input power with total output power. These three types of efficiency are defined as

$$\eta_D = \frac{P_{out}}{P_{dc}}, \tag{2.1}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}, \tag{2.2}$$

$$\text{and} \quad \eta = \frac{P_{out}}{P_{in} + P_{dc}}. \tag{2.3}$$

In terms of drain efficiency and gain, $G = P_{out}/P_{in}$,

$$PAE = \eta_D(1 - \frac{1}{G}) \tag{2.4}$$

$$\text{and} \quad \eta = \frac{\eta_D}{\frac{\eta_D}{G} + 1}. \tag{2.5}$$

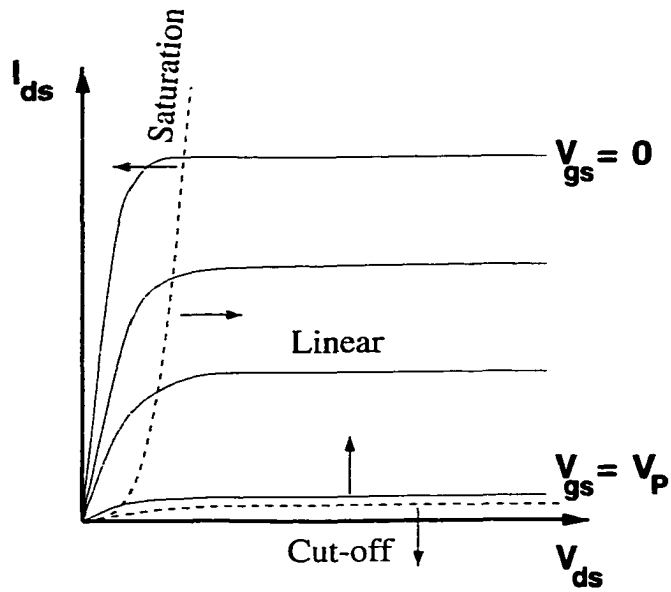


Figure 2.1. Transistor I-V curves showing the linear and nonlinear regions of operation. The two nonlinear regions are the cut-off and saturation regions. The drain current is clipped during cut-off, and the drain voltage is clipped when the device enters the saturation region.

2.2 Linearity and Power Amplifier Saturation

Amplifier linearity [7] describes the ability of the PA to correctly reproduce the amplitude and phase of the input signal at the amplifier output. At a given frequency, the output amplitude should vary linearly *with the input signal amplitude* while the phase difference between the output and input signals should remain a constant. (As a function of frequency, the phase should vary linearly. However, the bandwidths of concern for an X-band carrier are quite small - less than 1% - and therefore the frequency dependancy of phase is not considered here.) Typically, amplitude nonlinearity causes more signal distortion than phase variation. Linearity is a function of PA saturation, particularly the amount of time per period when the device is in the saturated region of operation. This region is shown in the transistor I-V curves of Fig. 2.1.

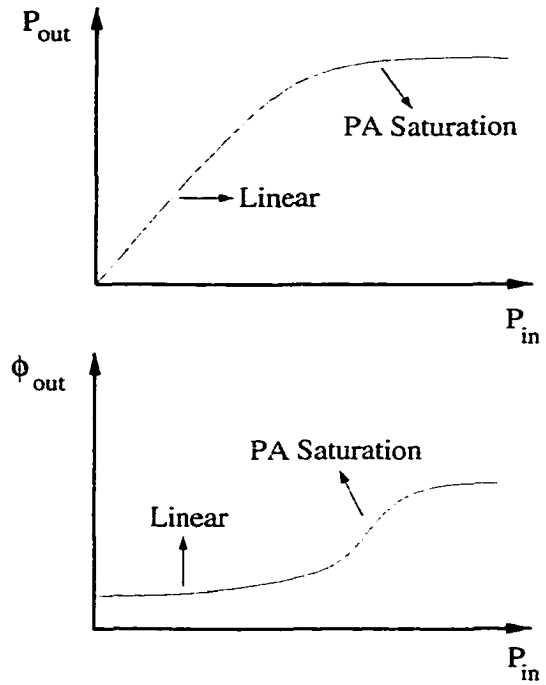


Figure 2.2. Gain compression and phase variation due to PA saturation. P_{out} is the output power, ϕ_{out} is the phase of the output signal and P_{in} is the input power.

Linearity is not a concern when amplifying signals with a constant amplitude. This is because power amplifier saturation is a function of input signal amplitude. If the amplitude remains a constant, the saturation is at a constant level and therefore the gain of the amplifier will remain the same, as will the phase of the output signal. For FM signals, the phase may vary nonlinearly with frequency, but as mentioned before, the bandwidths of typical signals at X-band are small (less than 1%) and therefore this effect is not considered in this work.

The gain-compressed nonlinear behavior that occurs at large input signal levels is caused by saturation of the power amplifier. The phase of the output signal is also a function of the degree of saturation, and therefore there is significant signal distortion as the amplifier approaches the saturation regime. This is shown qualitatively in Fig. 2.2.

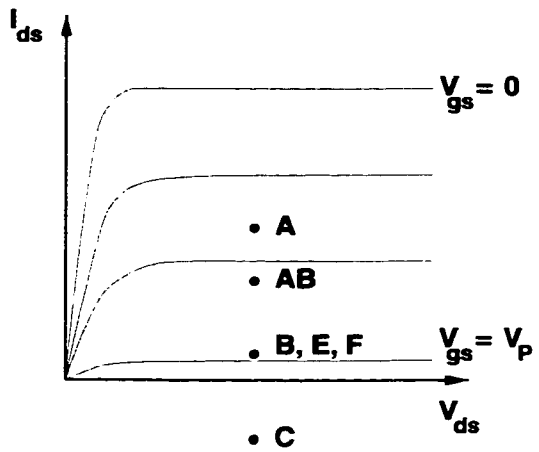


Figure 2.3. Bias points for different classes of power amplifiers. Each class is defined by the gate bias and the magnitide of the drive signal.

Linearity is usually defined in terms of spectral distortion at the output when two closely spaced frequencies are input to the power amplifier. This is discussed in more detail in Chapter 6.

2.3 Classes of Power Amplifiers

Most microwave power amplifiers (PAs) used today operate in class-A, -AB or -C. Class-D, -E and -F switched-mode power amplifiers are used in some transmitter stations and satellite applications where efficiency is a major concern. Good discussions of the various classes of power amplifiers are found in [7] and [8]. A short summary of the information given in these books is provided here for completeness. Fig. 2.3 shows the biasing of the different classes of power amplifiers while Fig. 2.4 portrays the drain current and voltage waveforms of each class.

2.3.1 Current-Source vs. Switched-Mode PAs Class-A and -B amplifiers are operated as voltage- or current-controlled current sources with a small-signal RF input for high linearity. A small input signal ensures that the PA remains in the linear region of the PA input-output characteristic of Fig. 2.2. Class-AB and

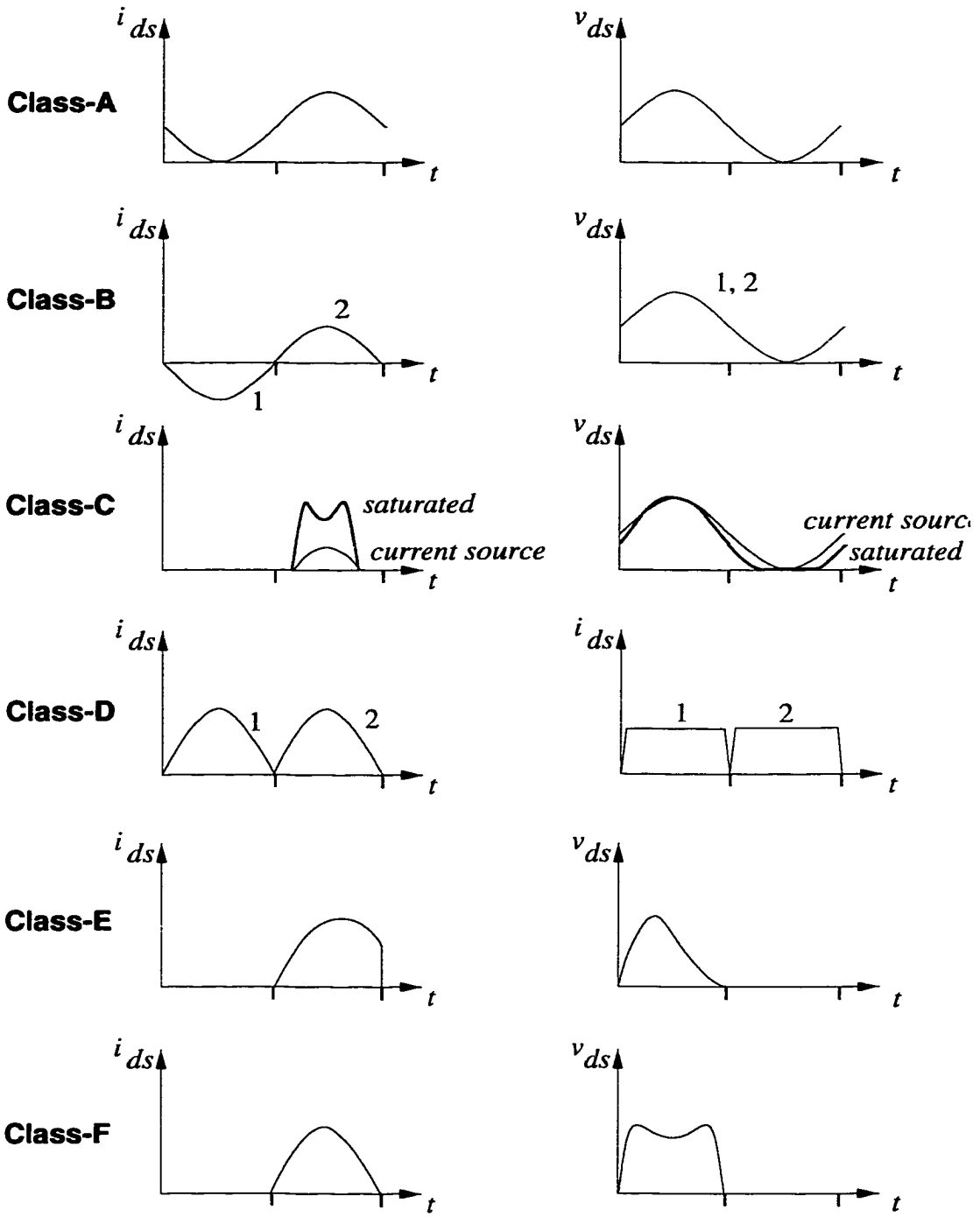


Figure 2.4. Time-domain current and voltage waveforms for several different classes of microwave power amplifiers. Classes-B and -D are usually implemented in a push-pull configuration with two-transistors; the waveforms at each transistor (1 and 2) are shown for these classes.

-C amplifiers, on the other hand are nonlinear, have higher efficiency than an A or B-class amplifier. Class-C power amplifiers have the highest efficiency among these, but have reduced output power. Saturated class-C PAs are driven slightly into saturation such that voltage clipping occurs as shown in Fig. 2.4, making linear drain amplitude modulation possible.

Switched-mode power amplifiers have high efficiency because the vi Joule losses in the transistor are minimized by operating it as a switch, i.e. there is zero drain-source voltage when the switch current flows, and zero current when the voltage is nonzero. In switched-mode class-D, E and F amplifiers, the transistor is heavily saturated by a large input signal, while the device is biased near cut-off. The voltage- and current-clipping caused by these two factors make it possible to operate the transistor as a switch, with 100% theoretical drain efficiency. In the real world, however, transistor switches have stray reactances, a saturation ON resistance, and nonzero switching time, factors which contribute to reduced efficiencies.

2.3.2 Class-A Class-A amplifiers are optimized for high gain or output power. High linearity is obtained by operating under small-signal conditions. They are biased in the middle of the active portion of the I-V curves of Fig. 2.3 and have a theoretical maximum drain efficiency of 50%. The drain-source voltage and current waveforms are shown in Fig. 2.4. When made to operate under large signal excitation, class-A amplifiers can have higher drain efficiencies at the expense of linearity. This higher drain efficiency when operating several dB into compression has a theoretical maximum value of 81%, since a substantial portion of the power is converted into harmonics which are dissipated in the load.

2.3.3 Class-B Class-B amplifiers have high gain, output power and linearity, and also operate under small-signal conditions, with slightly higher drain efficiency (78.5% theoretical maximum) than class-A power amplifiers due to the fact that they are biased near pinch-off and therefore only conduct for half the period.

They are usually used in a push-pull configuration with two transistors such that the output current is a full sinusoidal waveform and the output power is double that of a class-A power amplifier with the same device. For the same power output as a class-A amplifier, class-B power amplifiers can be designed using a single transistor with a tuned circuit at the output to filter out the harmonics produced by the current clipping. However, this makes the circuit narrowband.

2.3.4 Class-AB A good compromise between the low 50% drain efficiency and the narrowband operation of a single-ended class-B amplifier with 78.5% efficiency is a class-AB power amplifier which provides higher output power than both class-A and B, but is a nonlinear amplifier. More details of this class of PA, biased somewhere between the middle of the active region and pinch-off, are found in [8].

2.3.5 Class-C Another nonlinear option for power amplification is the class-C power amplifier. Conducting for less than half the period, as shown in Fig. 2.4, this PA sacrifices output power for efficiency as the conduction cycle gets smaller, and has an efficiency larger than class-B, approaching 100% as the conduction cycle and output power go to zero. Since they are nonlinear, class-C PAs are only used in applications with constant-amplitude signals. Class-C amplifiers, though usually used in the active and cut-off regions, are sometimes operated with large input signals such that the transistors enter saturation during a part of the conduction cycle. This results in slightly higher output power and efficiency, but the main advantage is that amplitude modulation can be accomplished through the drain or collector bias to obtain linear amplification.

2.3.6 Class-D The original switched-mode power amplifier is the class-D PA, which is very similar to the class-B PA in that it is operated in a push-pull configuration. However, the two transistors have completely offset voltage and current waveforms as seen in Fig. 2.4, since there is current only when the voltage

across the transistor is zero. This is switched-mode operation, and results in zero power losses within the transistor. It can be thought of as a modified large-signal class-B amplifier, where energy that would be otherwise dissipated in the transistor is stored in the switch capacitor and released into the output circuit. Class-D power amplifiers are used extensively for audio applications and have yet to find a niche in the microwave arena due to the switch resistance and finite switching times causing overlap between the voltage and current waveforms.

2.3.7 Class-E and -F Class-E and -F power amplifiers are operated single-ended in switched-mode with tuned circuits at the output to tune out undesired harmonics which are produced by the nonsinusoidal transistor waveforms. The theory behind these amplifiers is detailed in the following sections.

2.4 Class-E Power Amplifier Theory

Switched-mode amplifiers, such as class-D described above, have 100% theoretical efficiencies because the drain-source voltage and current are completely offset from one another, making their product, which is the dissipated power in the transistor, zero. Therefore, all power is delivered to the load. The transistor is operated as a switch by biasing it near pinch-off and driving it with a large enough RF signal, which produces a gate-voltage swing that is below the threshold voltage for a portion of the period. During this time, the transistor current is clipped at zero. However, when it starts to conduct, the voltage becomes clipped at zero due to device saturation. The output of the transistor can be idealized as a switch in parallel with the drain-source capacitance, as shown in Fig. 2.6. The switch is open (OFF) when the gate voltage swings below the threshold value, and is closed (ON) at all other times as shown in Fig. 2.5. During the OFF cycle, energy is stored in the output capacitor. If the switch is an ideal one, this does not cause any concern, but for a practical switch with a series resistance, the energy discharge causes power dissipation in this

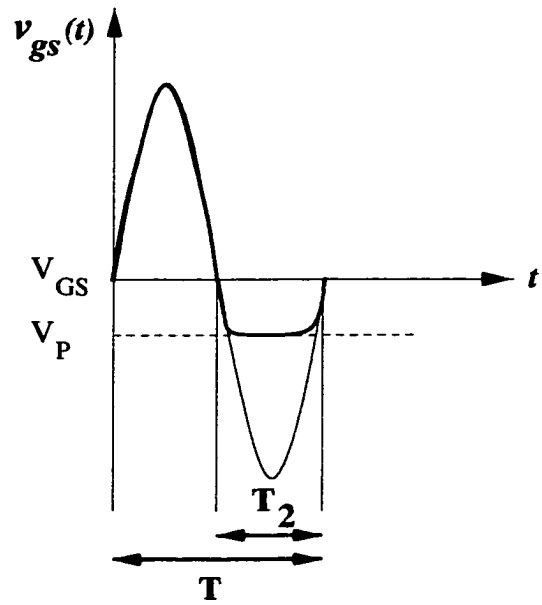


Figure 2.5. Sketch of time-domain gate-source voltage waveform in a FET caused by a large input RF power show how switching occurs. The duty cycle, D, is the ratio T_2/T. This input waveform controls the state of the transistor switch shown in Fig. 2.6.

resistance.

Class-E power amplifiers, first introduced by the father and son team of Nathan and Alan Sokal in 1975 [9], make use of harmonic tuning at the output of the amplifier circuit to recycle energy stored in the parasitic output capacitances of the transistor switch. As mentioned above, this energy is normally dissipated in the switch resistance if the switch turns ON while there is a voltage across the capacitor, limiting the efficiency. However, if the transistor switch voltage goes to zero before the switch turns on, the stored energy is zero and therefore there is no power dissipated in the transistor. An excellent analysis of the transmission line class-E PA is given in [10] and [3].

The basic circuit diagram of a class-E amplifier is shown in Fig. 2.6. L_o and C_o comprise a tuned-circuit at the output frequency that ideally filters out all harmonics. At the output frequency, the transistor output is presented with the

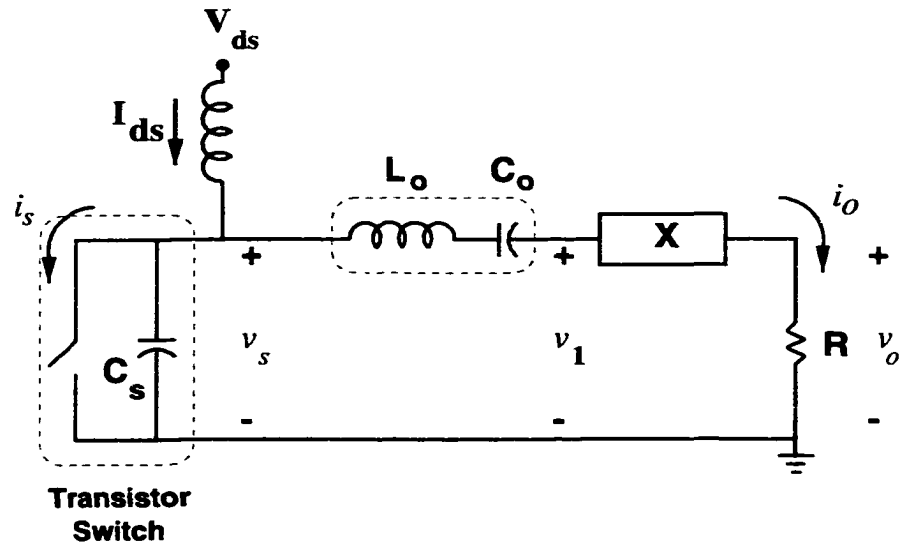


Figure 2.6. Basic circuit representation of a class-E amplifier, with the transistor used as a switch. The reactances due to L_o and C_o cancel each other at the fundamental frequency, allowing the transistor output to see a load $R + jX$ and The output circuit, including the switch capacitance, filters out all higher harmonics to provide a sinusoidal voltage and current at the load R.

impedance $R+jX$. By assuming that the output current and voltage are sinusoidal, the voltage and current waveforms at the switch, the load impedance at the fundamental frequency, and the DC voltage and current can be found. The sinusoidal output current flows through the ideal switch during the ON cycle and through the capacitor during the OFF cycle. The operation of the circuit is described well in [8] and [7] and is discussed in more detail in Chapter 7.

The differential equation which defines the capacitor voltage $v_s(t)$ during the OFF cycle is

$$C_s \frac{dv_s}{dt} = I_{ds}[1 - A\sin(N\omega t + \phi)], \tag{2.6}$$

where C_s is the switch output capacitance, I_{ds} is the drain DC current, AI_{ds} is the amplitude of the output current, and ϕ is the phase of the output current. Eq. 2.6

can be solved by integrating during the switch OFF cycle, to obtain

$$\begin{aligned} v_s(t) &= \int \frac{I_{ds}}{C_s}[1 - A\sin(N\omega t + \phi)]dt \qquad 0 < t < DT \\ &= \frac{I_{ds}}{C_s}[t + \frac{A}{N\omega}\cos(N\omega t + \phi)] + K, \end{aligned} \tag{2.7}$$

which describes the voltage waveform between time $t = 0$ to time $t = DT$ where D is the the duty cycle of the switch, and $T = 2\pi/\omega$ is the period of the output signal. The product DT is therefore the end of the switch OFF cycle. I_{ds} is the DC drain current and C_s is the switch capacitance. The unknowns in Eq. 2.7 are K (the integration constant), A, and ϕ. The optimum duty cycle, D, also must be specified, making a total of four unknowns. Therefore, in order to solve for v_s at any arbitrary time t during the OFF cycle four equations are necessary. These are listed below.

$$v_s(0) = 0 \tag{2.8}$$

$$v_s(DT) = 0 \tag{2.9}$$

$$\left.\frac{dv_s}{dt}\right|_{DT} = 0 \tag{2.10}$$

$$D = 0.5 \tag{2.11}$$

The conditions specified by Eqs. 2.8 and 2.9 provide 100% efficiency by offseting the current and voltage switch waveforms. When imposed on Eq. 2.7, they give $K = A/(N\Omega)$ and $\cos\phi = \pi/(2A)$. Condition 2.10 allows the switch current to turn on softly, without an abrupt change from zero to some finite value and together with the last condition, gives a maximum output power capability. What is done is to vary the slope and the duty cycle and calculate the corresponding output power capability in order to find the optimum combination.

Output power capability can be described by means of a *power utilization factor* for the device. It is the ratio of output power to the product of maximum drain-source voltage and current, and is given by

$$p_c = \frac{P_{o,max}}{v_{max}i_{max}}, \tag{2.12}$$

where $P_{o,max}$ is the maximum output power, and v_{max} and i_{max} are the maximum voltage and current at the switch for a given DC drain voltage and load. p_c is a measure of how much output power the amplifier can provide without putting undue stress on the device by requiring exceedingly large drain-source voltage and current swings. Maximizing it allows the highest power output the device is capable of. More information on this is available in [7]. This quantity provides a good method of comparison between different amplifier designs that have the same DC drain-source voltage and current. It provides a cost/watt figure for the power amplifier, since larger voltage and current swings at the switch may indicate the need for a more costly higher-power device. For example, a particular output load which increases $P_{o,max}$ by a factor of two may seem desirable at first glance. However, if this output power increase comes at the cost of requiring a maximum switch current swing, i_{max}, greater than the capability of the device in question, the design is impractical with the device proposed and a different device must be used. By varying both the slope of the voltage waveform at $t = DT$ and the duty cycle D, the maximal power output capability is found to occur at $D = 0.5$ and a slope of zero.

The unknowns K, A, and ϕ can be found by using the conditions listed in Eqs. 2.8-2.11 to solve the differential equation given in Eq. 2.7. The unknowns are found to be:

$$K = -\frac{I_{ds}}{C_s}\frac{A}{N\omega}\cos(\phi), \tag{2.13}$$

$$A = 1.862, \tag{2.14}$$

$$\text{and} \qquad \phi = -0.5669 \qquad \text{rad.} \tag{2.15}$$

The switch current waveform during the ON time is given by

$$i_s(t) = I_{ds}(1 - A\sin(\omega t + \phi)), \tag{2.16}$$

which shows that the maximum switch current, i_{max}=$(1 + A)I_{ds}$ and cannot exceed

the maximum drain current of the device, I_{max}. Therefore, we find the maximum DC drain current is $I_{max}/(1+A)$, or $I_{ds} = I_{max}/2.86$.

The DC component of the switch voltage is the drain bias and can be found by averaging Eq. 2.7 over a period. The drain voltage is given by

$$V_{ds} = \frac{I_{max}}{56.5 C_s f}, \tag{2.17}$$

where I_{max} is the maximum drain-source current of the device. The maximum frequency of class-E operation is therefore

$$f_{max} = \frac{I_{max}}{56.5 V_{ds} C_s}. \tag{2.18}$$

For a given device, ideal class-E operation is not possible above this frequency due to long switching times. However, suboptimal class-E operation, with less than 100% efficiency is possible up to 2 to 4 times f_{max}.

The load impedance necessary at the output of the transistor switch is given by the ratio of the fundamental component of the switch voltage to the output current. This impedance is given by

$$Z_{net} = \frac{0.0446}{C_s f} e^{j49.05^\circ} \tag{2.19}$$

As seen in the above equations, the output capacitance of the transistor is required to design a class-E amplifier with a given device. This output capacitance can be approximated by the drain-source capacitance of the transistor, which is de-embedded from the s-parameters of the device. First, the y-parameters of the transistor circuit model shown in Fig. 2.7 are calculated:

$$y_{11} = \frac{1}{Z_0} \frac{(1-s_{11})(1+s_{22}) + s_{12}s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21})} \tag{2.20}$$

$$y_{12} = \frac{1}{Z_0} \frac{-2s_{12}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21})} \tag{2.21}$$

$$y_{21} = \frac{1}{Z_0} \frac{-2s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21})} \tag{2.22}$$

$$y_{22} = \frac{1}{Z_0} \frac{(1+s_{11})(1-s_{22}) + s_{12}s_{21}}{(1+s_{11})(1+s_{22}) - s_{12}s_{21})} \tag{2.23}$$

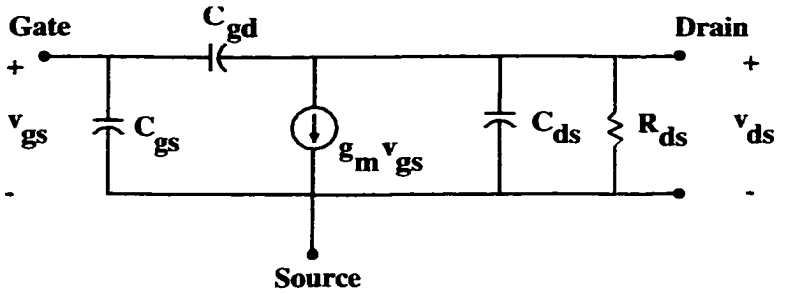


Figure 2.7. Small signal circuit model for a MESFET. The output capacitance of the transistor switch can be considered to be the drain-source capacitance, C_{ds} in parallel with the gate-drain capacitance, However, C_{gd} is much smaller than C_{ds} and therefore the switch capacitance is considered to be just C_{ds}.

Then, the circuit parameters are obtained from the y-parameters as follows:

$$g_m = \Re(y_{12}) \tag{2.24}$$

$$R_{ds} = \frac{1}{\Re(y_{22})} \tag{2.25}$$

$$C_{gd} = \frac{-\Im(y_{12})}{2\pi f} \tag{2.26}$$

$$C_{gs} = \frac{\Im(y_{11})}{2\pi f} - C_{gd} \tag{2.27}$$

$$C_{ds} = \frac{\Im(y_{22})}{2\pi f} - C_{gd} \tag{2.28}$$

The circuit is built using transmission-line input and ouput matching, with two 45° sections of line providing a second harmonic open, and then two sections of line which provide the class-E impedance.

2.5 Class-F Power Amplifier Theory

Class-F power amplifiers are probably the oldest form of high-efficiency power amplifier. The principle of operation for class-F is the addition of a third harmonic component to the transistor voltage waveform in order to flatten it. In [7], Raab shows that the drain-source voltage waveform is

$$v_s(t) = V_{ds}(1 + \frac{9}{8}\sin(\omega t) + \frac{1}{8}\sin(3\omega t)) \tag{2.29}$$

for maximum flattening and maximum fundamental output power. This flattening allows a higher fundamental component to exist while keeping the transistor voltage swing within its physical limitations. Thus, a class-F PA can provide more fundamental frequency output power than a class-A PA for no increase in the DC input power. This results in increased efficiency, up to 88.4%.

By shorting all even harmonics and driving it hard, the class-F voltage waveform can be made more square since it contains all odd harmonics. This is switched-mode class-F operation, and can be 100% efficient.

The output load impedance at the fundamental frequency is often determined by the so-called *power match* discussed in [8] and [11]. The transistor output is matched not for maximum gain, but for maximum output power. The conjugate match for maximum gain may require voltages that the transistor is not capable of, and therefore the output power saturates at a lower level than if matched for maximum output power. The power match is done by first calculating the transistor output resistance based on the I-V characteristics. If the maximum output current swing is half the maximum drain current, and the maximum output voltage swing is equal to the DC drain voltage, the load line dictates an output load of

$$R_{opt} = \frac{2V_{ds}}{I_{max}} \tag{2.30}$$

for maximum power transfer, both for the linear and the saturated transistor [11]. The transistor output is represented by the output capacitance as de-embedded from s-parameters, in parallel with R_{opt}, and in series with a lead inductance. This is shown in Fig. 2.8. For a power-match, the transistor is presented with a load resistance equal to R_{opt}, and all even harmonics are short-circuited. Therefore, only the fundamental and odd harmonics exist at the transistor switch, squaring the voltage waveform as shown in Fig. 2.4.

The input to the transistor is matched to 50 Ω for maximum power transfer.

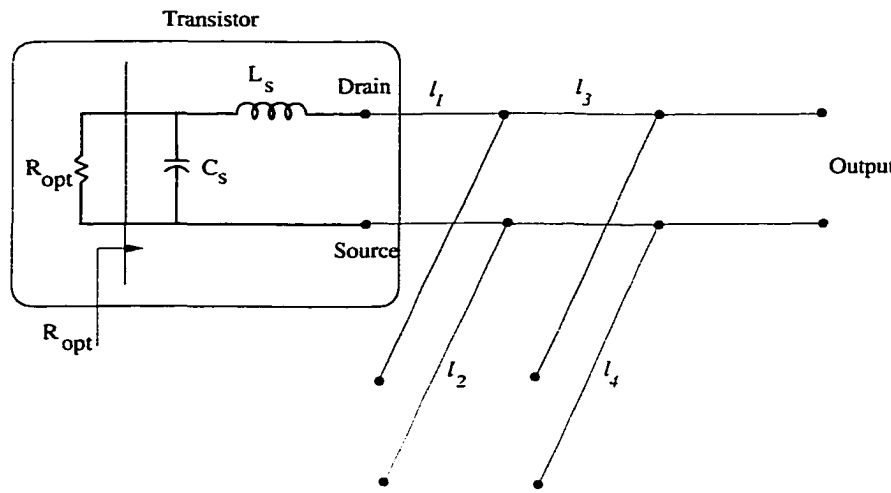


Figure 2.8. Output match for a class-F power amplifier. The drain-source capacitance and the lead inductance of the transistor are incorporated into the output matching circuitry. For maximum power transfer, the output resistance seen by the transistor is R_{opt}, the equivalent resistance of the transistor output. The transmission lines of lengths l_1 and l_2 provide a second harmonic short while l_3 and l_4 transform the load impedance at the output (usually $50\,\Omega$) to R_{opt}, as seen from the transistor.

CHAPTER 3

TIME-DOMAIN OPTICAL SAMPLING OF SWITCHED-MODE MICROWAVE AMPLIFIERS

3.1 Introduction

As discussed in detail in the previous chapter, the transistor is used as a switch in high-efficiency class-E and class-F power amplifiers, and the harmonics of the switched voltage are reflected back towards the transistor before reaching the load, such as has been demonstrated in the MHz range [9]–[12], and up to 10 GHz [13].

If large signal models of the transistor are available, the design of class-E and F amplifiers includes simulating the time-domain waveforms at the switch using *Spice* modeling or harmonic balance methods to verify their shapes and the offset between the current and voltage waveforms. In [10], such simulations are used in the design of microwave power amplifiers at 0.5-1 GHz. However, as class-E and -F amplifiers are scaled to X-band, the available large-signal models become inaccurate for switched-mode operation due to the large number of parasitic elements which must be de-embedded from measurements.

Therefore, the design is carried out in an approximate manner, using small signal *s*-parameters, as described in Chapter 2, without the luxury of verifying the class of operation from the simulated waveforms.

One verification of class-E or class-F performance is simply obtaining high efficiency while maintaining high output power. However, this leaves an ambiguity

in the specific class of operation of the circuit, and therefore does not validate the design. Knowledge of the switch waveform would significantly add to the understanding of circuit performance and the ability to improve the design.

At low frequencies (up to about 500 MHz), the switch voltage can be measured across the drain-source terminals with a large resistance in series with the oscilloscope probe [3]. At higher frequencies it is not possible to measure these waveforms due to the loading from the inductive leads of the resistor and the difficulty in making high-impedance probes at these frequencies. Recent advancements in photoconductive probing of microwave circuits [14, 15] have paved a way to non-intrusively measure such voltage waveforms up to very high frequencies. The measurements presented in this chapter are the result of a collaboration with Dr. John Whitaker at the University of Michigan, Ann Arbor. We are grateful to Dr. Whitaker for using our circuits to test his optical probing method. A brief description of the probe and experimental sampling setup is given below for completeness.

3.2 Photoconductive Probing

The photoconductive probe utilized in the time-domain measurement of the high-efficiency amplifier response is a micromachined, optical-fiber-coupled, optoelectronic sampling head [16, 17, 18]. Shown in Fig. 3.1, the probe head itself utilizes a 1.5 μm-thick substrate layer of GaAs, which was grown epitaxially at 200 C (so-called low temperature GaAs) and then annealed at 600 C. The GaAs layer prepared in this fashion has a one-picosecond carrier relaxation time (so the sampling gate was active for only a brief time), a resistivity of 10^7 Ω-cm (so the photogate would have high off-state resistance), and a breakdown voltage of nearly 10^6 V/m. The photogate consisted of a 30 x 30μm gold pattern of interdigitated fingers, which are 1.5 μm in width with 1.5 μm separations. The probe, with its 7 μm-wide tip that

Figure 3.1. Micromachined photoconductive probe with optical fiber built in the research group of Dr. John Whitaker at the University of Michigan, Ann Arbor.

extends out past the GaAs for contacting circuit metalizations, can sense the potential on an exposed interconnect or the field associated with a buried interconnect. A photocurrent proportional to the potential within the sampling window is then generated at the photogate before being converted back into a voltage signal.

The current to voltage conversion is accomplished by a JFET source follower circuit [19] with an input resistance of 1 TΩ and an input capacitance of 3 pF. This high input resistance avoids charge drainage from the device under test so that measurement with minimal invasiveness is achieved. Due to the small amount of charge necessary to load the source follower input, the actual voltage level is built up in a short time, allowing a higher modulation bandwidth and the ability to measure absolute voltage levels. In addition, the high input resistance of the source follower allows the instantaneous DC voltage at the probe node to be determined at the output of the source follower, and thus both AC and DC signals can be measured simultaneously.

In this measurement system, shown in Fig. 3.2, the probe is illuminated by a train of femtosecond-duration laser pulses, and the output voltage is recorded

on a low-frequency oscilloscope. The output voltage is a down-converted replica of the unknown microwave signal. If a frequency-domain output is required, a lock-in amplifier or a spectrum analyzer can be used in place of the oscilloscope. For an unknown microwave signal with frequency f_m, heterodyne mixing and equivalent time-sampling dictate the following relationship between the microwave frequency and the intermediate frequency:

$$f_m = nf_{rep} \pm f_{IF}, \tag{3.1}$$

where n is an integer and $f_{rep} = 80\,\text{MHz}$ is the laser pulse repetition frequency. The intermediate frequency f_{IF} is typically in the kHz range and provides a replica of the unknown microwave signal. The Ti:sapphire laser used in this system is phase-locked to the microwave source so that the in-circuit electrical signal can be determined in amplitude and phase. The probe has a 3.5 ps time response, which relates to a bandwidth over 100 GHz. Therefore, the probe should exhibit a frequency response which extends into the millimeter-wave region.

3.3 Photoconductive Probing of High Efficiency Amplifiers

The optical probing technique discussed above was used to measure the characteristic switch waveforms of two 8 GHz switched-mode amplifiers, one operating in class-E and the other in class-F mode. These amplifiers are built on RT Duroid substrates with $\epsilon_r = 2.2$ and 0.508 mm thickness. The general outline of the two circuits is given in Fig. 3.3. The input to the amplifiers is at point **A**, and **E** is the output. Harmonics generated at the drain are reflected back to the input through the feedback capacitance C_{gd} between the device gate and drain, resulting in reduced efficiency of the amplifier. The input circuit, in addition to performing a matching function, must also filter these reflected harmonics. The output circuit also filters out harmonics and provides the correct loading to the transistor at the

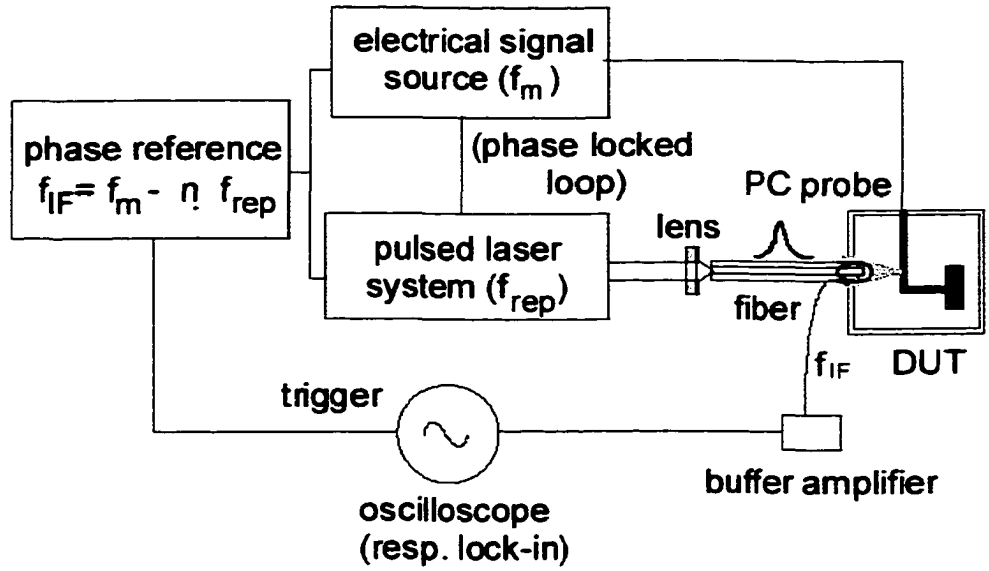


Figure 3.2: Optical sampling measurement setup.

fundamental frequency. The points at which the circuit is probed are shown as **A**, **B**, **C**, **D**, and **E** in this figure and correspond to plots given in this paper. The gate and drain gold leads are soldered to the rest of the circuit so that an exposed gold area exists for the probe to contact.

The measured waveform amplitudes cannot be used to calculate power since the local impedance is unknown. However, they are very useful in analyzing the harmonic content of the waveform. Point **A** represents the input plane of the amplifier. Ideally, the input circuit filters out any harmonics reflected to the gate from the drain, and the voltage at this point is a sine wave. Point **B**, representative of the switch voltage, is on the gold drain lead of the package as close to the transistor as the probe can be positioned, and indicates the class of operation of the amplifier. This waveform is not identical to the switch voltage due to package output parasitics, especially the small lead inductance. We estimate from measurement that the

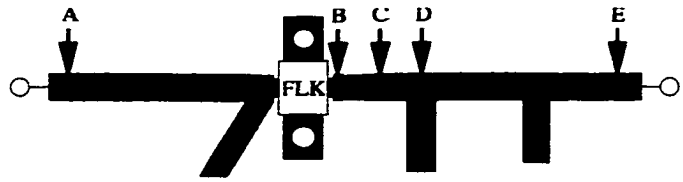


Figure 3.3. General outline of class-E and -F amplifier circuits showing locations of optical probing. FLK represents the Fujitsu MESFET in the PA. The class-E PA is based on the FLK202MH-14 and the class-F is based on the FLK052WG.

package lead inductance is about 0.25 nH. The effect of this series parasitic element is an increase of about 10-20 ps in rise and fall times of an ideal square wave at the intrinsic device output. This means that the waveform at the intrinsic device leans more towards the rising edge compared to the waveform measured at **B**. The waveforms at **C**, **D** and **E** are helpful in analyzing the filtering functions of the output circuit. The voltage at **E** should be a sine wave if proper filtering is taking place.

3.4 Class-F Nonlinear Amplifier

3.4.1 Electrical Measurements Class-F amplifier design requires an output impedance given by Eq. 2.30 at the fundamental switching frequency. In addition, the output circuit presents a short circuit at all even harmonics and an open circuit at all odd harmonics. The amplifier is built with the Fujitsu FLK052WG packaged MESFET previously used at C-band and presented in [10]. The substrate is 0.508 mm Rogers Duroid RT5880 (ϵ_r=2.2) and the optimum output resitance is 80 Ω, while the output capacitance and series inductance are 0.4 pF and 0.25 nH respectively. The fundamental is terminated in the impedance for maximum saturated power delivered to the load, as outlined in Chapter 2, while the drain capacitance and drain lead inductance of the MESFET are included in the external tuned circuit. The second harmonic is terminated in a short. The layout of the amplifier is shown in Fig. 3.4(a). The 3.81 mm line and 4.12 mm open stub provide the second harmonic short. These in combination with the 4.84 mm line and the 3.59 mm open

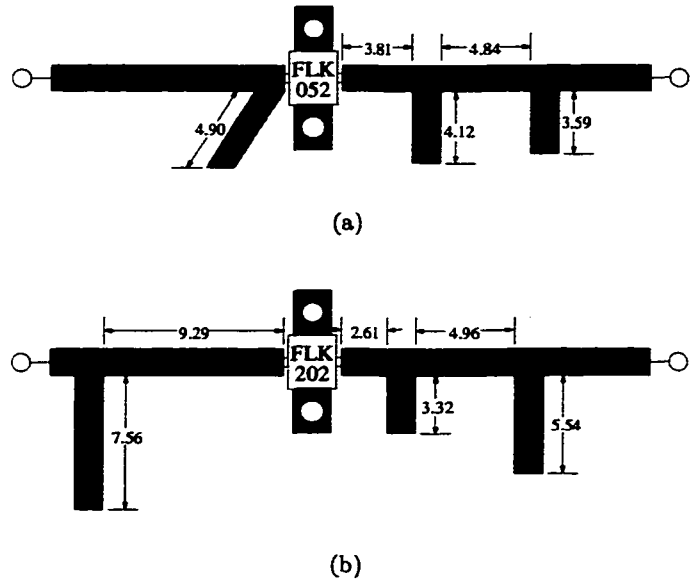


Figure 3.4. Microstrip layout of the class-F amplifier using the FLK052 (a)and the class-E amplifier using the FLK202 (b). The substrate is 0.508 mm thick RT5880 Duroid (ϵ_r=2.2) All dimensions are given in mm.

stub provide the fundamental match. Electrical measurements at 8.0 GHz show a drain efficiency of 73%, a power-added efficiency (PAE) of 61%, and 28.6 dBm output power with an input power of 22 dBm. The device is biased at -0.9 V at the gate and 1 V at the drain. Harmonic balance simulations of the waveforms were not possible because a reliable large signal model for the transistor was not available. The design, fabrication and measurement of this amplifier were carried out by Dr. Eric Bryerton, now with the National Radio Astronomy Observatory in Charlottesville, Virginia.

3.4.2 Optical Time-Domain Measurements The input waveform measured at point **A** in Fig. 3.3 is a sinusoidal waveform biased at about -1.0 V, as is shown in Fig. 3.5. Since there is very little harmonic content in the waveform at **A**, we can conclude that there is no significant harmonic power being reflected back to the input of the amplifier.

Fig. 3.6 shows the voltage waveforms at points **B**, **C**, and **D** in Fig. 3.3.

The waveform at **B** shows the square shape of the switch voltage, which is consistent with class-F operation. The two peaks in the waveform are due to the fundamental frequency and the third harmonic, as is evidenced by the spacing between peaks. The second harmonic does not appear in this waveform since it is presented with a short at the output. Higher harmonics are not present because the transistor does not have gain at these harmonic frequencies.

However, in Fig. 3.6, it is evident that there is a significant second harmonic contribution at point **C** (Fig. 3.3). This is due to the standing wave between the transistor output and the first stub, which provides the second harmonic short. The second harmonic is not strong in the waveform at point **D**. The distortion in the waveform indicates that there is some second harmonic leakage beyond the first stub.

Beyond the second output stub, at point **E**, the output waveform is sinusoidal. This is shown in Fig. 3.5 along with the input waveform for comparison. This is part of the design of a class-F circuit, in which the output circuit must filter out the harmonics in the switched waveform. These measurements provide supporting evidence of the proper waveforms inside the power amplifier and therefore substantiate the class-F design.

3.5 Class-E Nonlinear Amplifier

3.5.1 Electrical Measurements A class-E amplifier was built with the Fujitsu FLK202MH-14 packaged MESFET, which has a gate periphery four times larger than the FLK052. The output capacitance extracted from the manufacturer-provided s-parameters is 0.94 pF. Using Eq. 2.19 at 8 GHz, a class-E PA was designed and built on the same RT Duroid 5880 as the class-F PA. The microstrip layout is shown in Fig. 3.4(b). The second harmonic is terminated in an open circuit, provided by the 2.61 mm line and 3.32 mm stub. The 4.96 mm line and 5.54 mm stub in

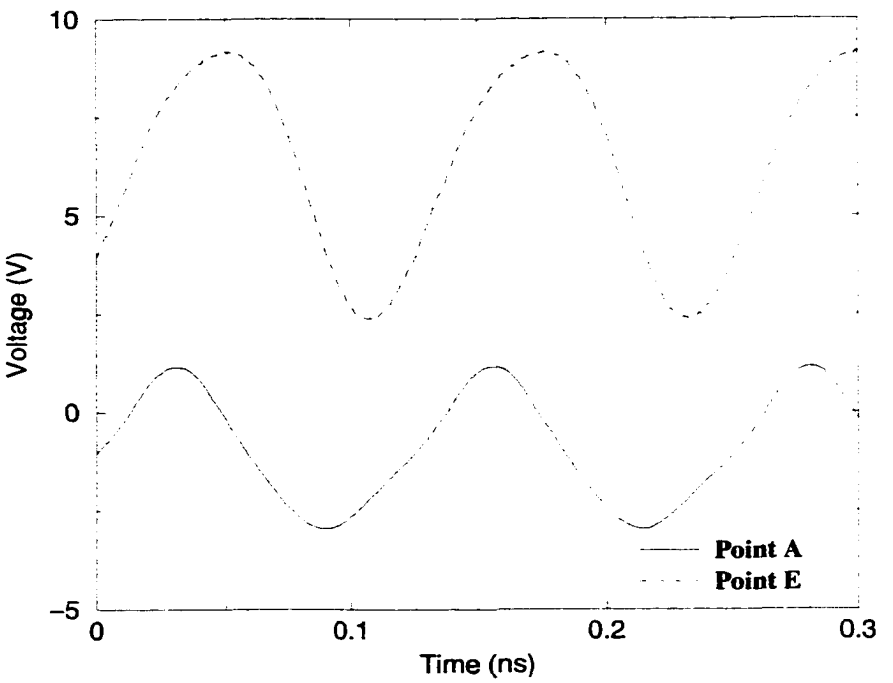


Figure 3.5. Optically sampled waveforms at points **A** and **E** in the class-F circuit, corresponding to the input and output respectively. The input and output waveforms are both approximately sinusoidal signals.

combination with the second harmonic circuitry provide the class-E impedance at the fundamental. Power measurements result in a drain efficiency of 64%, PAE of 48%, and 31.5 dBm output power at 8.35 GHz. The optical measurements were made at 8.32 GHz, since the microwave frequency must be a multiple of the laser repetition frequency of 80 MHz according to Eq. (3.1). The bias for the amplifier is V_{ds}=7 V, V_{gs}=-0.9 V.

3.5.2 Optical Time-Domain Measurements For the class-E circuit, only voltages at points **B** and **E** in Fig. 3.3 are shown, since they are the salient waveforms of class-E operation.

Fig. 3.7 shows the voltage at point **B**, which is the voltage waveform across the switch. For comparison, a harmonic balance simulation at 500 MHz for a different class-E amplifier [20] is shown in Fig. 3.8. A suitable nonlinear model was available

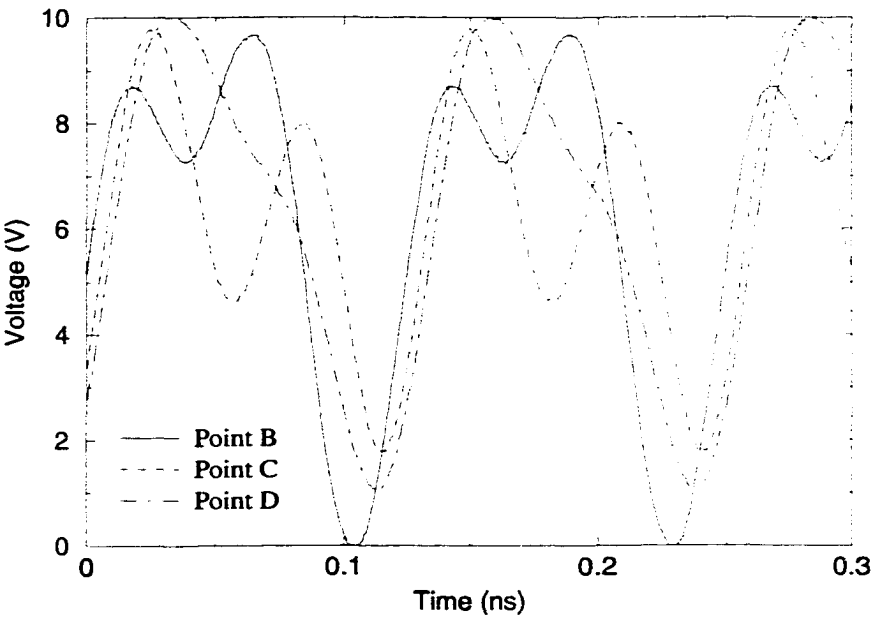


Figure 3.6. Optically sampled waveforms at points **B**, **C** and **D** in the class-F circuit. In the switch waveform at **B**, the fundamental and third harmonic approximate a square wave. At **C**, which is before the second harmonic shorting stub, there is a significant second harmonic component, and at **D**, the harmonics have mostly been filtered out. These waveform amplitudes cannot be used to calculate power since the local impedance is unknown.

for this MESFET (Siemens CLY5). The switch voltage waveform in this case is not square, but has considerable fundamental and second harmonic content, giving it the shape of a narrow, left-skewed half-sinusoid. The measurement also shows the second harmonic portion of the waveform, which produces the left-skewed voltage wave. The simulated voltage is close to zero for nearly half of the period, approaching ideal class-E operation. The measured voltage, however, is not flat in this half of the period, resulting in a higher vi product (loss). This is consistent with non-optimal class-E operation, since the circuit is operated above the critical frequency for class-E operation, in this case, about 1.5 GHz [21, 10]. The measured class-E waveform is very different from the class-F switch voltage in Fig. 3.6 which depicts a square wave consisting of the fundamental and third harmonic.

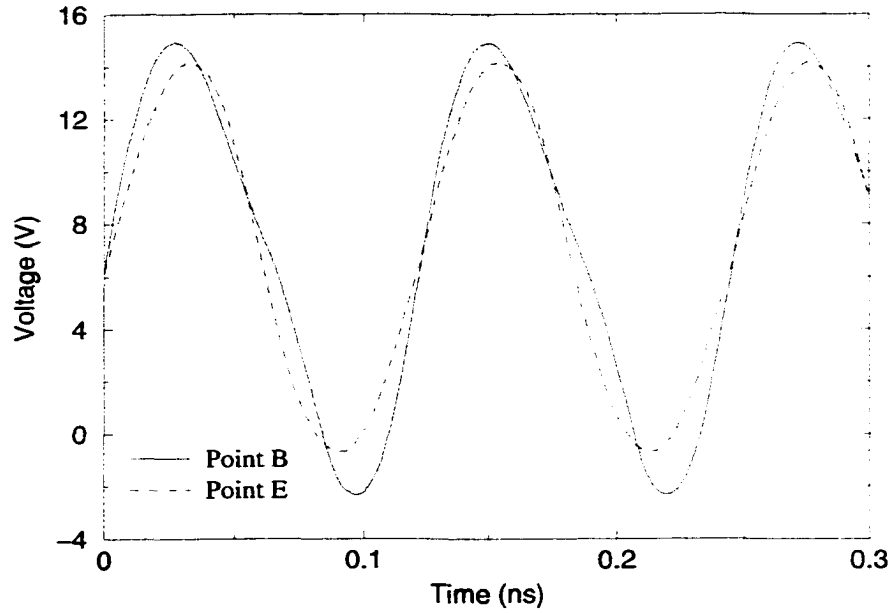


Figure 3.7. Measured waveforms at points **B** and **E** in the class-E circuit. The shape of the voltage wave at **B** is similar to that in Fig. 3.8, with a second harmonic component in the waveform. The output wave at **E** is sinusoidal.

At point **E**, the filtered output waveform appears as a sinusoidal pattern as shown in Fig. 3.7. This analysis verifies that the power amplifier is indeed operating in the expected suboptimal class-E mode.

3.6 Conclusion

Optical sampling was used to examine the harmonic content of the voltage waveform at various characteristic points in several nonlinear microwave circuits. This information is vital in verifying the class of operation of high-efficiency switched-mode power amplifiers, since the specific class depends on the shape of the switch waveform. The class-F and E power amplifiers examined in this study were found to operate in the correct mode. In the absence of good large-signal models for the Fujitsu power transistors used here, this optical sampling analysis substantiates the approximate design method based on small-signal parameters.

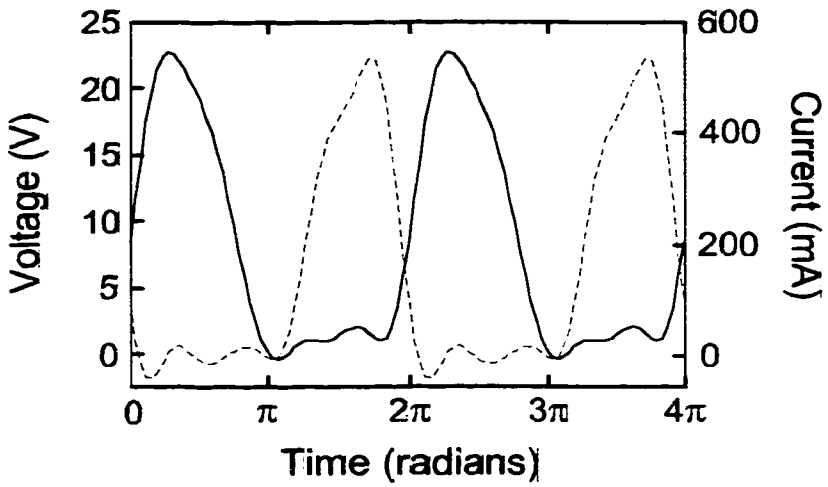


Figure 3.8. Simulated waveform at point **B** of a 500 MHz class-E circuit using a Materka-Kacprzak nonlinear model for a Siemens CLY5 MESFET. The solid line is voltage and the dashed line denotes current.

CHAPTER 4

EFFICIENCY OF CHIP-LEVEL VERSUS EXTERNAL POWER COMBINING

4.1 Introduction

With today's device technology, high-efficiency microwave power amplifiers such as the class-E and F varieties detailed in the previous chapters have typical output powers ranging from 100 mW to a few watts. For a large number of applications, e.g., satellite transmitters, tens of watts of microwave power are required. In order to obtain the desired power, it may be desirable to use larger devices capable of higher output power. However, the efficiency becomes lower as device size increases, so combining smaller amplifiers to achieve these power levels is an attractive option. The work in this chapter compares several different power-combining architectures with optimization of power consumption in mind and defines a power-combining efficiency useful for that purpose. The analysis presented in this chapter is the combined effort of this author and Dr. Eric Bryerton.

There are two basic methods of power combining: internal (or chip-level) and external. The latter includes methods such as circuit corporate and spatial power combiners. At the device level, the gate periphery can be enlarged to increase the power potential of the individual device at the expense of gain and efficiency. Alternatively, smaller and more efficient amplifiers can be combined externally (off-chip). Both internal and external power combining can be used together. For instance, ten 1 mm MESFETs can be circuit-combined instead of twenty 0.5 mm devices for the same output power.

The Fujitsu FLK052WG MESFET and the Fujitsu FLK202MH-14 are used in this work for a comparison. The FLK052 and the FLK202 have the same intrinsic structure, but the periphery of the FLK202 is four times larger [22]. They are both packaged devices.

4.2 Chip-level power combining

Considering that the FLK202 is physically four times larger than the FLK052, the output power might be expected to be four times larger as well. A more important goal in low-power electronics, however, is to minimize power dissipation. It is therefore more relevant to define the chip-level power-combining efficiency ($\mathrm{PCE_{chip}}$) as the ratio of the *overall efficiency* of the FLK202 amplifier to that of the FLK052 amplifier,

$$\mathrm{PCE_{chip}} = \frac{\eta_{\mathrm{AMP,202}}}{\eta_{\mathrm{AMP,052}}}, \tag{4.1}$$

where η_{AMP} is the overall efficiency, given by

$$\eta_{\mathrm{AMP}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{DC}} + P_{\mathrm{in}}}. \tag{4.2}$$

In order to accurately calculate $\mathrm{PCE_{chip}}$ for the FLK202 MESFET, both devices should be used in a power amplifier that yields the highest possible efficiency at a given frequency and bias point. It was found experimentally that, around 8 GHz, the FLK052 gave the best overall efficiency in a class-F amplifier and the FLK202 gave the best overall efficiency in a class-E amplifier, while maintaining an output power approximately equal to the maximum capability of each device. The design and fabrication of these circuits are described in further detail in Chapter 3.

The output power and efficiency for each amplifier were measured as a function of frequency and input power. Fig. 4.1 shows the output power and overall efficiency versus frequency for the FLK052 class-F and the FLK202 class-E amplifiers.

Device	P_{in}	P_{out}	Gain	η_{AMP}	P_{heat}
FLK202	500 mW	1.700 W	5.3 dB	57%	1.300 W
FLK052	125 mW	685 mW	7.4 dB	64%	391 mW

Table 4.1. Summary of measurements for the class-F power amplifier using the FLK052 and the class-E power amplifier using the four-times larger FLK202. P_{heat} is the power dissipated as heat.

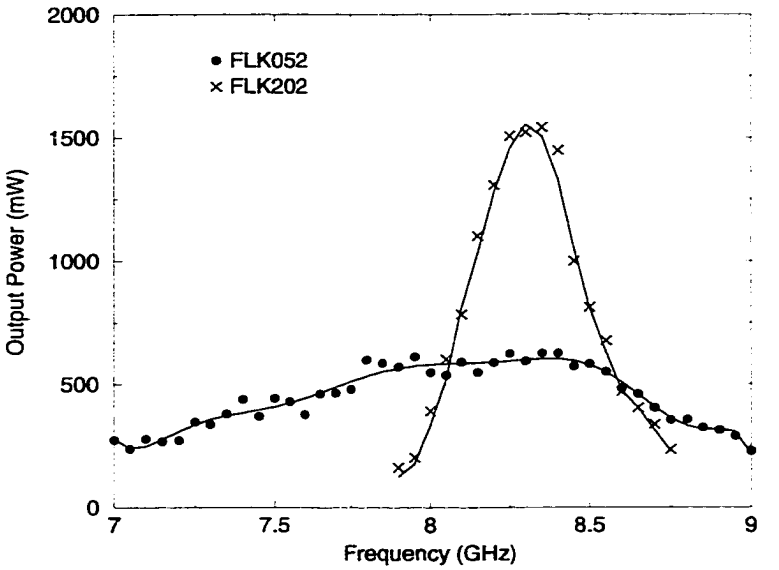
Fig. 4.2 shows the output power and overall efficiency versus input power for the FLK052 amplifier and the FLK202 amplifier. Table 4.1 shows the highest measured overall efficiency for each amplifier over a range of freqeuncies and input powers. The FLK052 class-F amplifier has a maximum η_{AMP} at 8.4 GHz of 64% with 685 mW output power. The FLK202 class-E amplifier has a maximum η_{AMP} at 8.35 GHz of 57% with 1.7 W output power. From Eq. 4.1, the chip-level PCE of the FLK202 is 89%. The time-domain waveforms at the input, output and switch are discussed in Chapter 3, and indicate proper class-E and -F operation of the amplifiers.

4.3 Circuit Level Power Combining

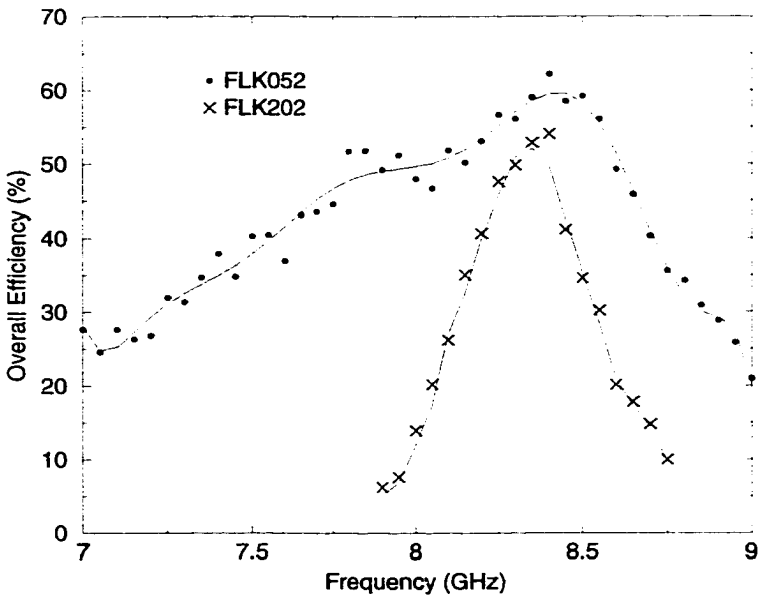
In a circuit corporate combiner, shown in Fig. 4.3, the outputs from each amplifier are successively combined using two-way adders such as Wilkinson combiners. Table 4.2 shows a comparison, for the same input power, between the circuit corporate combining of 16 FLK202 amplifiers and 64 FLK052 amplifiers for 0.2 dB loss per stage. To find the overall efficiency of the entire system (η), the overall efficiency of the amplifier (η_{AMP}) is multiplied by the power-combining efficiency of the combining network (PCE_{ckt}), given by

$$PCE_{ckt} = 10^{\frac{-n\,L}{10}}, \tag{4.3}$$

where L is the loss per stage in dB and n is the number of stages. The total number of elements, N, is 2^n. Even for a low-loss combiner (0.2 dB loss), the overall efficiencies are approximately equal, but it would be less complex and use less space to combine

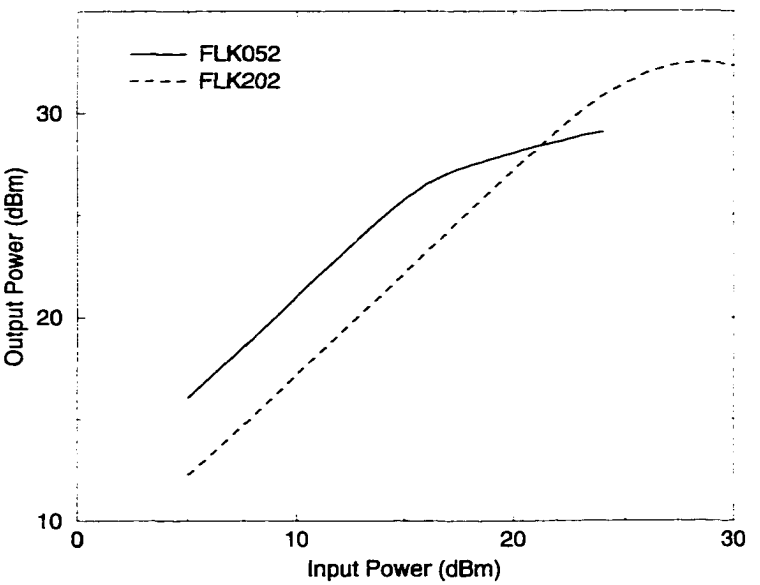


(a)

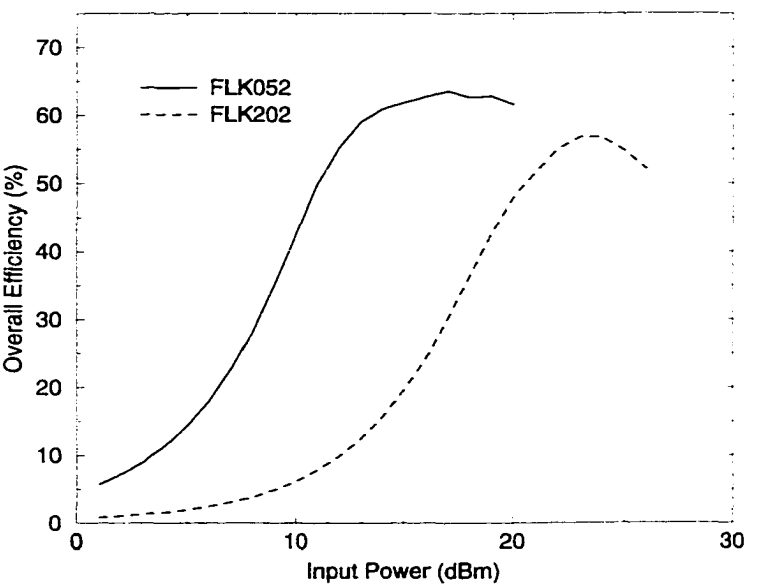


(b)

Figure 4.1. Output power (a) and overall efficiency (b) versus frequency for the FLK052 class-F amplifier (solid line) and the FLK202 class-E amplifier (dashed line). The input power is 20 dBm for the FLK052 class-F amplifier and 26 dBm for the FLK202 class-E amplifier. V_{DS}=7.0 V and V_{GS}=-0.9 V.



(a)



(b)

Figure 4.2. Output power (a) and overall efficiency (b) versus input power for the FLK052 class-F amplifier (solid line) and the FLK202 class-E amplifier (dashed line). The frequency is 8.4 GHz for the FLK052 amplifier and 8.35 GHz for the FLK202 amplifier. V_{DS}=7.0 V and V_{GS}=-0.9 V.

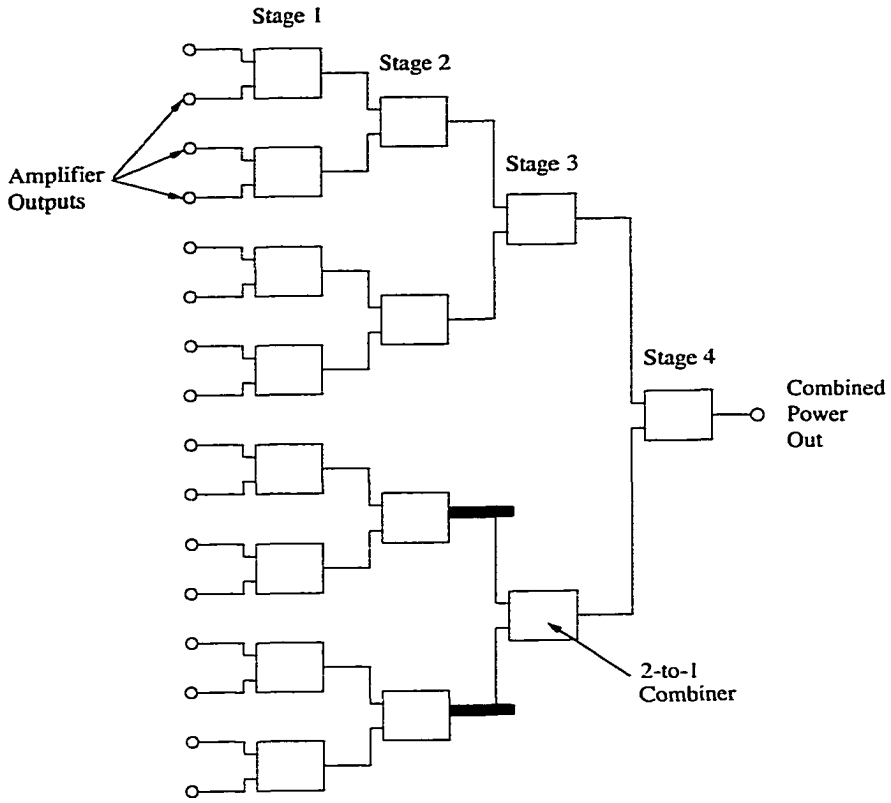


Figure 4.3. A circuit corporate power combiner. The output of an amplifier is connected to each circle.

the four larger FLK202 amplifiers.

4.4 Spatial Power Combining

Spatial, or *quasi-optical*, power combining, shown in Fig. 4.4, eliminates the need for complicated and lossy corporate networks. In this approach, the output of each amplifier is connected to an antenna. The powers from all the devices are thus coherently combined in free space in a single stage. The power-combining efficiency is therefore independent of the number of elements. This approach was first demonstrated in 1968 with a 100-element array at 410 MHz [23]. Other examples inlude a two-stage 14-element X-band lens array with 75% power-combining efficiency [24]

Device	N	η_{AMP}	Stages	PCE_{ckt}	P_{out}	η	P_{heat}
FLK202	16	57%	4	83%	22.6 W	47%	25.5 W
FLK052	64	64%	6	76%	33.3 W	49%	34.7 W

Table 4.2. This table compares the circuit-combining efficiencies of a 4-stage FLK202 system and a 6-stage FLK052 system, each with 8 W of RF input power. The two-way corporate combiners have 0.2 dB loss per stage. η_{AMP} is the overall efficiency of the amplifier, PCE_{ckt} is the power-combining efficiency of the corporate network, and η is the overall efficiency of the entire system. P_{heat} is the total power dissipated as heat in the system.

and a 4-element 5-GHz class-E array with 64% power-added efficiency and an estimated PCE of about 80% [10]. A survey of spatial power combining techniques can be found in [25].

Table 4.3 shows a comparison between spatially combining 16 FLK202 amplifiers and 64 FLK052 amplifiers. The overall efficiency of the entire system is η_{AMP} times the PCE of the spatial combiner (PCE_{spc}). A value of 75% is assumed for PCE_{spc}. This includes the efficiency of the antennas. P_{out} is equal to the output power from each amplifier multiplied by $N \cdot PCE_{spc}$. The area of the combining array assumes a unit cell size of 0.8λ x 0.8λ, and is therefore equal to $0.64 \cdot N\lambda^2$. The directivity, D, assumes an effective area equal to the physical area and is therefore equal to $\frac{4\pi}{\lambda^2}$-Area. The effective isotropic radiated power (EIRP) is the directivity multiplied by P_{out}.

Since the power-combining efficiency is independent of the number of elements, it is more efficient in a spatial combiner to use a larger number of smaller

Device	N	η_{AMP}	P_{out}	η	P_{heat}	Heat Flux	D	EIRP
FLK202	16	57%	20.4 W	43%	27.0 W	207 $\frac{mW}{cm^2}$	21.1 dB	2.63 kW
FLK052	64	64%	32.9 W	48%	35.6 W	68 $\frac{mW}{cm^2}$	27.1 dB	16.9 kW

Table 4.3. This table compares, for the same input power (8 W), the spatial power combining of 16 FLK202 amplifiers and 64 FLK052 amplifiers. The heat flux calculations assume a unit cell size of 0.8λ x 0.8λ. The directivity, D, assumes an effective area equal to the physical area. P_{heat} is the total power dissipated as heat in system. A power combining efficiency of 75% is assumed.

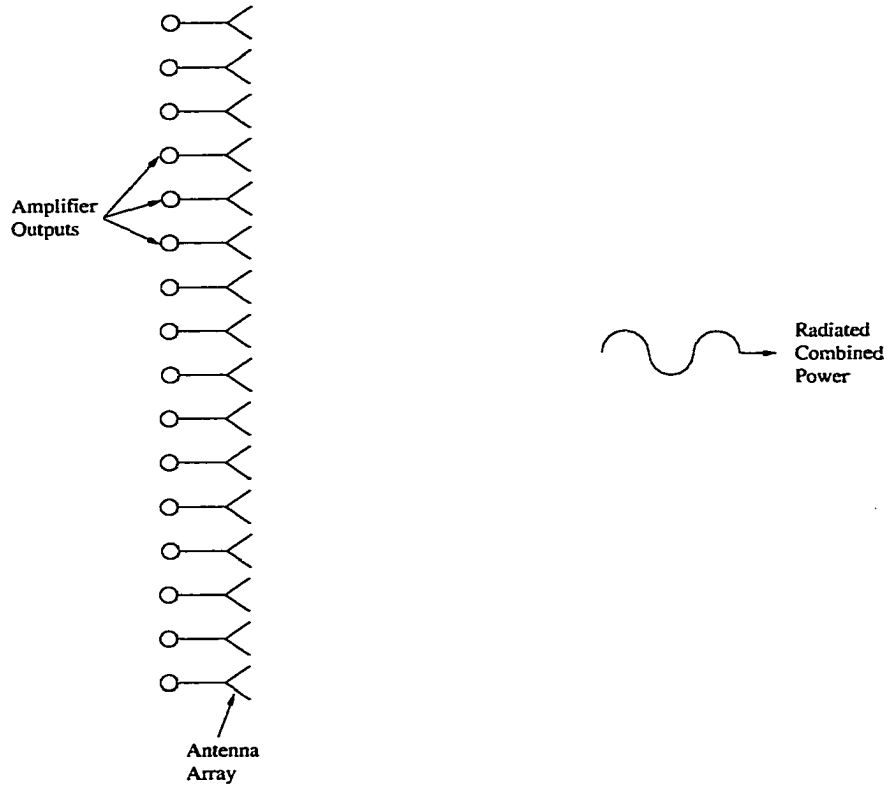


Figure 4.4. A spatial power combiner. The output of an amplifier is connected to each circle.

amplifiers, if space is not an issue. In addition, a larger array has a higher directivity, so the effective isotropic radiated power (EIRP) is also higher. Thermal management also becomes easier if a larger numbers of smaller devices are used, since the heat flux is much less.

In order to compare circuit to spatial combining, an antenna should be placed at the output of the circuit combiner. Assuming that the choice of antenna is not constrained by size or substrate considerations, unlike the spatial combiner, this antenna can be close to 100% efficient. A comparison of circuit combining to spatial combining shows that for 0.2 dB loss per stage, a circuit combiner with more than six stages (64 elements) will have a lower PCE than the 75% spatial combiner.

Since output power-combining efficiencies are being compared, the input

power distribution (feed) network has not been mentioned. A spatial power combiner can either be circuit fed, using a corporate structure similar to Fig. 4.3 as a divider, or spatially fed, where the feed is also in free space. The circuit-fed approach has the same problems with loss as a circuit combiner, but amplifiers can be placed in the input network to account for this.

The spatially fed approach has two problems: spillover loss and amplitude and phase nonuniformities. As with the circuit-fed approach, spillover loss results in the need of extra amplification at the input. Phase nonuniformities can be eliminated by using a constrained lens approach [26] or by using an external lens to generate a Gaussian beam [27]. Amplitude nonuniformities can cause problems since each amplifier element will have a different input power, resulting in different output powers, efficiencies, and amount of phase compression for each element in the array. These factors reduce the overall efficiency and power combining efficiency of the output array. A thorough comparison between circuit-fed and spatial-fed combiners can be found in [28].

4.5 Conclusions

Using MESFETs with identical intrinsic structure but different gate peripheries, high-efficiency power amplifiers were designed. Also, a new definition of power-combining efficiency is given, applicable to the problem of minimizing power dissipation. Measurements indicate, for the larger device, a chip-level PCE of 89% in terms of overall efficiency. However, this approach is limited by propagation delays as the device periphery increases. Also, the input impedance drops as the number of gate fingers increases, reducing bandwidth.

Using these power amplifiers, an overall efficiency was calculated for circuit and spatial combiners. In circuit combiners, a small number of larger devices was found to be more efficient. In spatial combiners, it is more efficient to use a large

number of smaller devices. In addition, in applications that require an antenna array at the transmitter output, distributed amplification (spatial combining) has advantages with respect to EIRP and thermal management.

CHAPTER 5

A 10 GHZ HIGH EFFICIENCY ACTIVE ANTENNA FOR SPATIAL POWER COMBINING

5.1 Introduction

In the previous chapter, the discussion on different power-combining methods was concluded by the observation that for large numbers of smaller amplifiers with more bandwidth, spatial combining has the most potential for high overall system efficiency. However, in antenna arrays for spatial combining, the spacing between elements needs to be between $\lambda/2$ and λ to have one main well-defined beam that combines all the powers efficiently. Each unit cell contains at least one antenna and one amplifier circuit with associated feed and bias lines. Usually, the antenna is designed to have a $50\,\Omega$ input impedance at the design frequency and the amplifier output is matched to a $50\,\Omega$ load. In this type of design, it is often difficult to fit the antenna and amplifier circuit in the available unit-cell space. In this chapter, a new design methodology in which the antenna is treated as an optimal amplifier load, is outlined. Because the antenna is directly matched to the amplifier output, the size of the array element can be reduced considerably.

As outlined in Chapter 2, class-E power amplifiers with high power-added-efficiency (PAE) use the transistor as a switch where the vi product is zero while the harmonics of the switched voltage are reflected back towards the switch before reaching the load [9, 7]. This is usually accomplished by the use of matching circuits and filters. The losses within the switching transistor are thus minimized. A 7%

increase in PAE was achieved without degrading the radiation properties by using an integrated antenna that provided harmonic tuning [29].

Previous work on integrated active antennas has included a circular sector patch antenna providing the load to a 2.55 GHz class-F amplifier in which the feed position and sector angle in the circular patch were optimized for the correct load and harmonic tuning. The PAE of this active antenna was 63% with 24.4 dBm output power [30]. Other work has explored broadband harmonic tuning by using a photonic bandgap structure consisting of a microstrip line with a periodically etched ground plane. The radiator was a slot antenna connected to this microstrip line. A PAE of over 50% and output power above 22 dBm was obtained from 3.7-4.0 GHz [31].

As the frequency increases, it becomes more difficult to get high PAE because the transistor internal reactances and resistances are larger and cause simultaneously high current and voltage across the switch. This increases power loss in the transistor and reduces efficiency. For example, at 0.5 GHz, a transmission line class-E amplifier was demonstrated with 80% PAE and 27.4 dBm output power [10]. However, at 5 GHz, the same circuit topology resulted in 72% PAE and 27.8 dBm output power. We have extended the class-E topology to 10 GHz, achieving 62% PAE at a reduced output power level of 20 dBm and a 74% corresponding drain efficiency. The class-E performance is achieved by using a microstrip-fed integrated antenna instead of matching and filtering circuits.

In microstrip class-E power amplifiers, the output load at the fundamental frequency is given by:

$$Z_L = \frac{0.0446}{fC_s} e^{j49.0524^\circ}, \tag{5.1}$$

where f is the fundamental frequency, and C_s is the transistor switch output capacitance [32]. At harmonics of the fundamental frequency, the output must be an open circuit. These conditions result in a switch voltage which is zero while current

is nonzero, and vice versa. The theoretical drain efficiency of the class-E circuit is 100%. Although the output must present an open circuit to all harmonics in an ideal class-E circuit, it was demonstrated in [10] that adequate phase offset between the voltage and current waveforms can be obtained by only considering the second harmonic. The gain of the transistor at the third harmonic is usually negligible and therefore the third harmonic content at the output is minimal.

Above a critical frequency dependant on the device, ideal class-E behaviour is not possible and the efficiency decreases [21]. This critical frequency is proportional to the maximum current handling capability of the device and inversely proportional to the output capacitance [10]. In most commercial X and Ku band devices, however, the output capacitance is proportional to the maximum current. Their ratio therefore stays approximately constant and the critical frequency for 100 mW devices is about 6 GHz, causing the efficiency to degrade above this value.

In microstrip class-E amplifiers presented in [32], tuned microstrip matching circuits at the output of the transistor provide the proper operating conditions. It is possible to design an antenna with input impedance given by Eq. (5.1), which removes the need to have a matching circuit and directly couples the amplifier power to the power of a wave in free space. Since a second-resonant slot antenna has a relatively wide bandwidth (compared to eg. a patch antenna), its impedance could provide an approximate class-E match to the transistor over a wide frequency range while maintaining high efficiency. A slot antenna was chosen as the amplifier load instead of a patch antenna due to its larger bandwidth (approximately 20%) at the second resonance. Even though the slot antenna presented here is not a resonant structure, it is close to the second resonance and therefore relatively broadband.

5.2 Passive Antenna Design and Measurement

An Alpha AFM04P2 power MESFET chip with an output capability of 21 dBm was used as the switch in the class-E amplifier. Since there is no available large signal model for this transistor, the switch (drain-source) capacitance was estimated using small signal s-parameters to be 0.107 pF. This does not take into account the nonlinear nature of this output capacitance, which causes it to vary with varying gate-drain and gate-source voltage. For a more precise design, a large signal model for the device is required. According to Eq. (5.1), the required load impedance for this capacitance is $41.67\,\Omega, \angle 49.0524°$, and s_{11} relative to $50\,\Omega$ is -6.67 dB, $\angle 104°$.

This reflection coefficient is provided by the slot antenna, which is microstrip-fed with a 90° tuning stub and is initially designed to be a second-resonant antenna at 10 GHz. The antenna length and width were then optimized using Ansoft's Ensemble and HP Momentum to obtain the desired class-E reflection coefficient magnitude. A 7 mm long transmission line between the antenna and the amplifier provides the correct phase of the reflection coefficient. At the second harmonic, the tuning stub is 180° long and therefore the load impedance at the second harmonic is merely the reactance of the line, which has a length of 12 mm from the open end to the transistor. Since this is approximately 360° at 20 GHz, the reactance is close to an open circuit and therefore presents a large impedance at the second harmonic. Although this is not ideal, it is sufficient for approximate class-E operation. The simulated input impedance of the antenna is shown on a Smith chart in Fig. 5.1. As seen in this figure, the antenna is not a resonant antenna. The slot antenna is 20 mm long, 2 mm wide, and is fed at the center.

A passive antenna was fabricated in order to measure the radiation patterns and the impedance as seen by the transistor. The measured reflection coefficient of the passive antenna is $s_{11} = -6.8\,\text{dB}, \angle 106°$. This value is in good agreement with the simulation shown in Fig. 5.1. The antenna gain was measured between 9 and

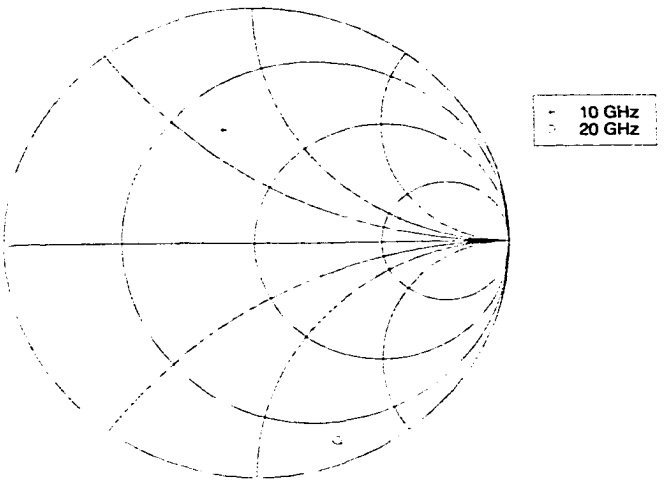


Figure 5.1: Input impedance of the passive antenna at 10 GHz (+) and 20 GHz (o).

11 GHz and ranged from about -3 dB to 4 dB. The negative gain comes from broadside nulls in the antenna pattern at certain frequencies. The nulls may be caused by the center-feed, and have been previously observed in second-resonant slots [3]. These measured values of gain agreed well with the simulations at 10 GHz and above, but the negative gain below 10 GHz was lower than expected. The crosspolarization ratio is approximately 19 dB. The gain of the antenna is approximately 2.3 dB at 10 GHz.

5.3 Active Antenna Design and Measurement

The active antenna circuit was fabricated on a RT Duroid substrate with $\epsilon_r = 2.2$. The circuit outline is shown in Fig. 5.2. The Alpha AFM04P2 MESFET has a 0.25 μm gate length and a 400 μm gate periphery, which allows a maximum current of approximately 150 mA and a maximum output power of 21 dBm up to 18 GHz. The DC drain-source series resistance, which is the switch ON resistance, R_s, is approximately 4.55 Ω. As stated above, the output capacitance, C_s, is 0.107 pF.

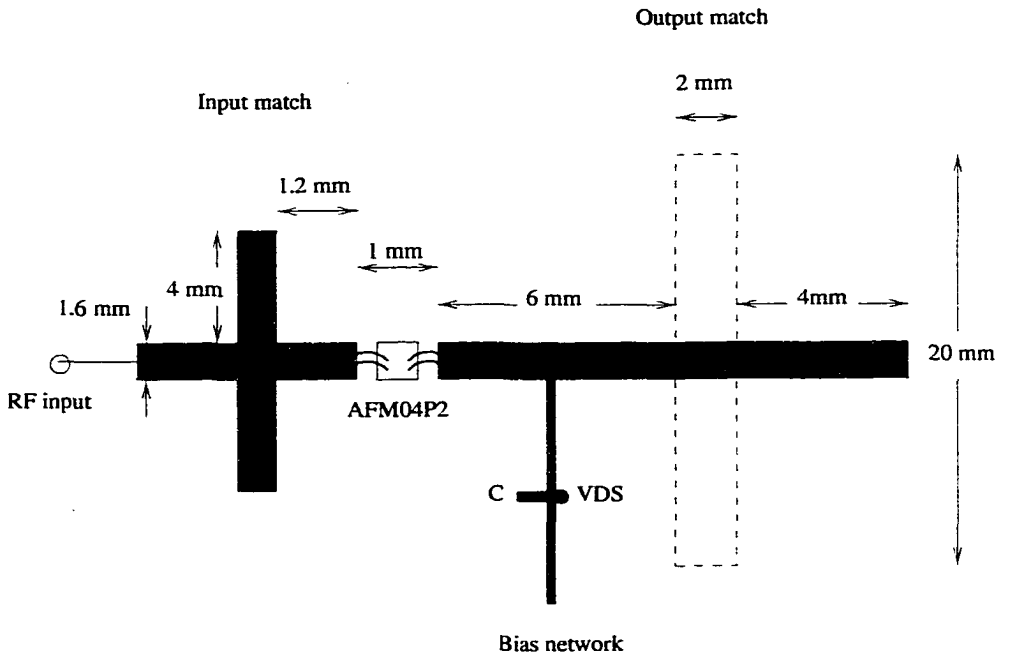


Figure 5.2. Circuit layout of the 10 GHz active antenna. The capacitor C is part of the bias network and provides an RF short.

In [10] the expected drain efficiency is given by

$$\eta_D = \frac{1 + (\frac{\pi}{2} + \omega_s C_s R_s)^2}{(1 + \frac{\pi^2}{4})(1 + \pi\omega_s C_s R_s)^2}, \tag{5.2}$$

where $\omega_s = 2\pi f$. This equation takes into account loss in the switch due to the switch voltage being nonzero when current flows through R_s. A thorough analysis can be found in [3]. According to this equation, a drain-efficiency of 85% is predicted for the AFM04P2.

The MESFET is mounted on a brass platform which is epoxied to the ground plane. The gate and drain are wire-bonded onto the microstrip lines. DC biasing is supplied 45° away from the transistor output so as to present an open to the transistor at the second harmonic. The overall size of the active antenna is about $0.4\lambda^2$ where λ is the wavelength in free space.

The performance of the final integrated antenna was measured using the Friis transmission formula, since the output of the circuit couples directly to free

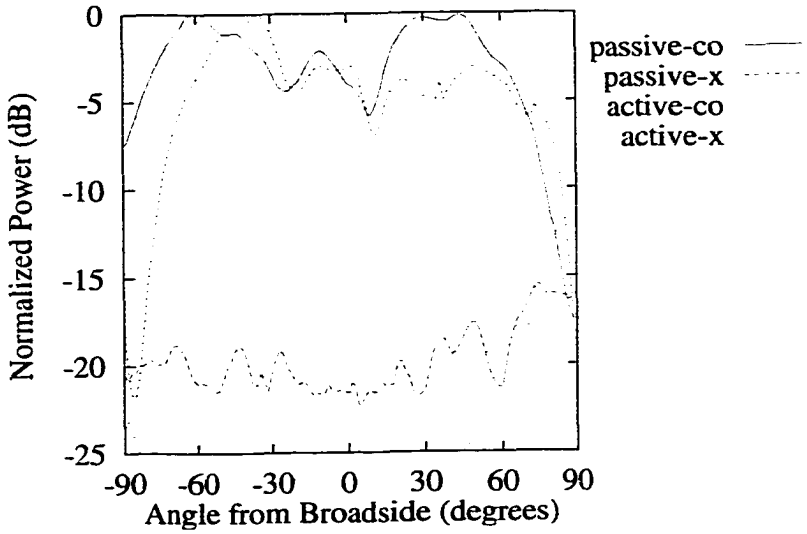


Figure 5.3. Copolar (co) and crosspolar (x) radiation patterns in the E-plane of the passive and active antennas.

space. The gain of the active antenna is the product of the amplifier gain and the passive antenna gain. However, it was necessary to determine if the directivity of the active antenna is equal to that of the passive antenna. This was accomplished by comparing the radiation patterns of the active and passive antennas as shown in Fig. 5.3 and Fig. 5.4. The active antenna pattern is similar in shape to that of the passive antenna. Therefore, the directivities of the active and passive antennas were assumed to be equal. In simulations with varying length of the feed line, leaving the stub length and the antenna dimensions constant, the magnitude of the nulls varied from 0.5 to 2 dB while the position varied by about 20_o. The measured nulls occur at approximately the same angles as in the simulation, but they are deeper. This is believed to be in part due to the feed line connector. The cross-polarizations in the two antennas are the same.

The input power is varied from -5 dBm to 18 dBm and the transmitted power is received by a standard gain horn antenna in the far field. Using the Friis formula and the measured directivity of the passive antenna, the transmitted power

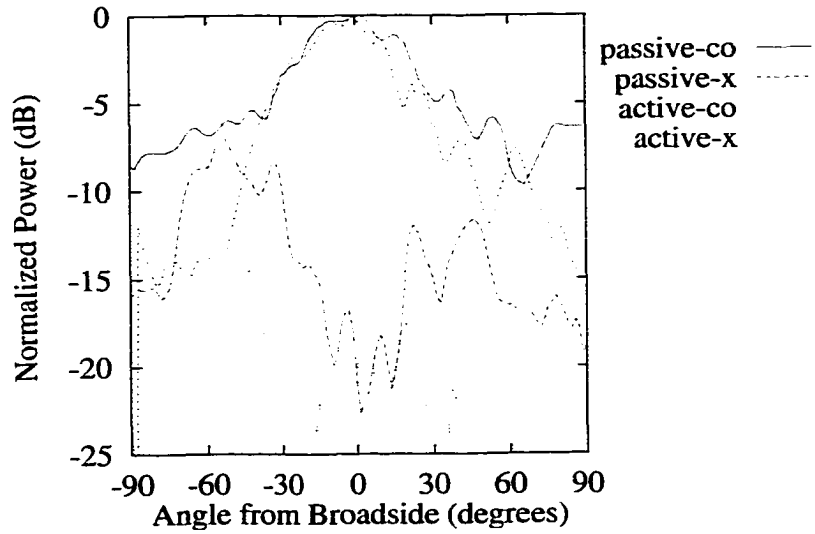


Figure 5.4. Copolar (co) and crosspolar (x) radiation patterns in the H-plane of the passive and active antenna.

was calculated as shown in Fig. 5.5. The maximum measured power is 20.5 dBm. The efficiency of the amplifier with varying input power is shown in Fig. 5.6. As seen here, the peak PAE of 62% is obtained at 12 dBm, or approximately 5 dB gain compression. The corresponding drain efficiency is 74%, with approximately 20 dBm output power. The maximum drain efficiency is 79%, obtained at 18 dBm input power. This is 6% lower than predicted by Eq. (5.2). This discrepancy may indicate that the estimates of the output capacitance and/or series resistance used in the design are slightly lower than the realistic values. This reiterates the need for large signal models in the design of high-efficiency power amplifiers.

The frequency dependance of the output power and efficiency is shown in figures 5.7 and 5.8 for 12 dBm input power. From 9.7 GHz to 10.1 GHz, the PAE is above 50% and the output power is above 19 dBm.

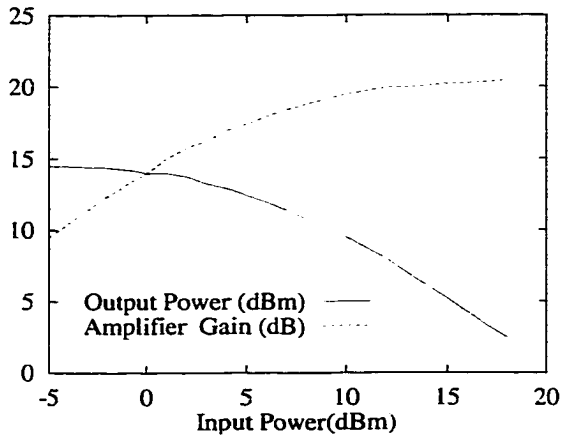


Figure 5.5. Output power and gain of the active antenna for varying input power. V_{gs}=-1.2 V, V_{ds}=4.0 V, I_{ds} varies slightly around 35 mA.

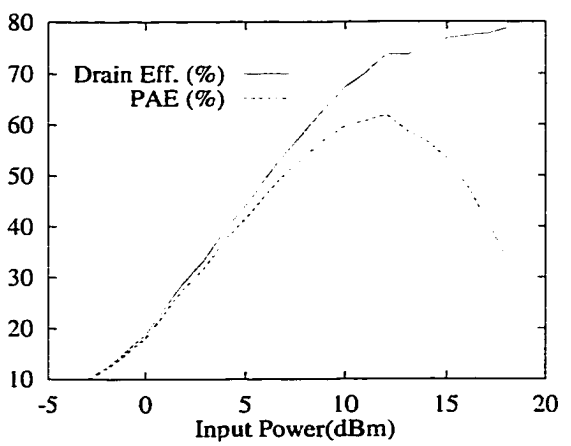


Figure 5.6. Drain efficiency and PAE of the active antenna for varying input power. V_{gs}=-1.2 V, V_{ds}=4.0 V, I_{ds} varies slightly around 35 mA.

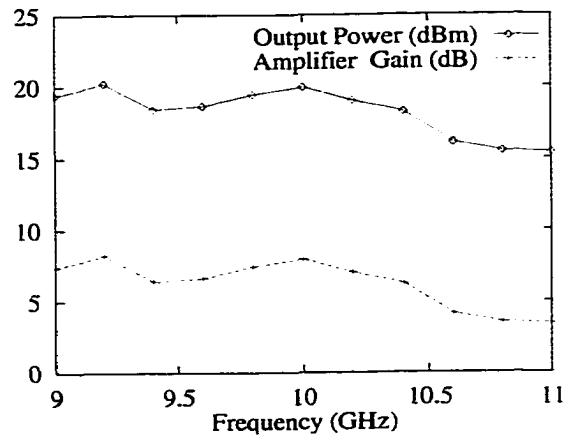


Figure 5.7. Output power and gain of the active antenna from 9 to 11 GHz for 12 dBm input power.

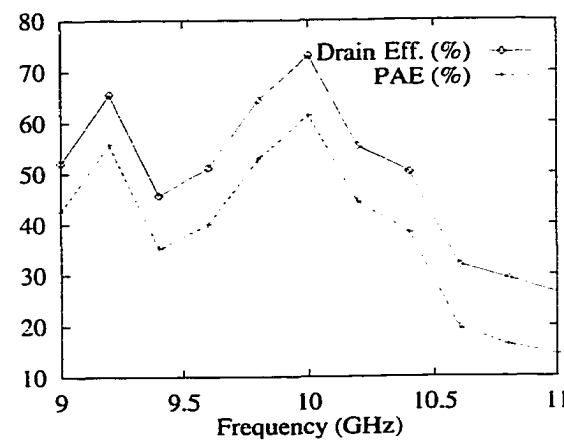


Figure 5.8. Drain efficiency and PAE of the active antenna from 9 to 11 GHz for 12 dBm input power.

5.4 Conclusions

A 10 GHz high-efficiency power amplifer was integrated with a slot antenna which provides the correct output load to the transistor without the use of a matching circuit. The antenna is also designed to provide harmonic tuning at the second harmonic. This results in a smaller circuit and lower output losses, which affect the efficiency much more than input losses. The radiation patterns of the antenna are similar for both passive and active antennas. The maximum drain efficiency is 74% with 62% PAE and an EIRP of 22.3 dBm. The PAE and power remain above 50% and 19 dBm, respectively, over a relatively broad bandwidth of 400 MHz. The size of the active antenna is approximately $0.4\lambda^2$. These results show that this active antenna is suitable for spatial power combining in a high efficiency transmitter array.

CHAPTER 6

LINEARITY OF X-BAND CLASS-F POWER AMPLIFIERS IN HIGH-EFFICIENCY TRANSMITTERS

6.1 Introduction

In the preceding chapters, the importance of reducing transmitter size, weight, and power consumption by employing high efficiency PAs was discussed. However, when amplifying signals with varying envelopes, efficiency is less of a concern than signal distortion, which renders high-efficiency class-E and F PAs useless due to their inherent nonlinear behavior.

Most communication signals with variable envelopes, such as QAM (quadrature amplitude modulation), are typically amplified by linear but inefficient PAs, such as class-A and -AB, to minimize signal distortion. In addition, the PA is often operated below its maximum power capability in order to avoid nonlinearities occuring at high output power levels. This further reduces its efficiency. One method of enhancing the PA efficiency is a technique known as envelope tracking, in which the drain bias voltage varies proportionally with the input signal envelope while maintaining the active device in the linear regime [33]-[35]. A class-A or B PA can also be maintained in extended saturation and hence high-efficiency, by providing optimum drain and gate biases [36]. Alternatively, the Kahn envelope elimination and restoration (EER) technique [37] allows the use of saturated high-efficiency power amplifier classes such as E and F in linear transmitter systems. This method, which we refer to as the classical Kahn method, has been successfully demonstrated from

HF through L band using saturated class-AB PAs [38, 39].

Modifying the Kahn method to include dynamic power control provides increased efficiency by conserving RF power consumption at low signal envelope levels. This method has been demonstrated at L band using class-AB PAs [39] and shows promise for use at higher frequencies. The novelty of this work is that it experimentally compares a single X-band PA under different efficiency-enhancing modes of operation, namely: linear with fixed bias; envelope tracking; and Kahn EER with and without dynamic power control. The goal of the measurements presented here is to determine the relationship between drain bias and RF drive level which gives increased average efficiency without sacrificing linearity of the PA.

The results presented here are obtained by manually varying the drain bias and RF drive level according to specific relationships. These control schemes may be implemented, for example, by using DC-DC converters [34]. For highest linearity, predistortion techniques derived from the signal envelope can be implemented using DSP (digital signal processing).

6.2 Background of Kahn EER and Dynamic Power Control

The basic premise of the Kahn method is that any narrow-band signal is equivalent to simultaneous amplitude and phase modulation of a carrier. As shown in the block diagram of Fig. 6.1, the envelope is detected and amplified to high power levels by an efficient amplitude modulator, such as a class S modulator [7], [39]. The class-D, -E or -F PA is operated with high efficiency by correct choice of the fixed input RF power level. The envelope is restored to the carrier through the drain bias. When saturated, the RF input/output characteristics become increasingly nonlinear due to the variation of g_m, C_{gs}, C_{gd}, R_{ds} with gate-source and drain-source voltages. In heavy saturation (switched-mode), the output voltage depends only on the voltage being switched, the drain voltage, and not on nonlinear device

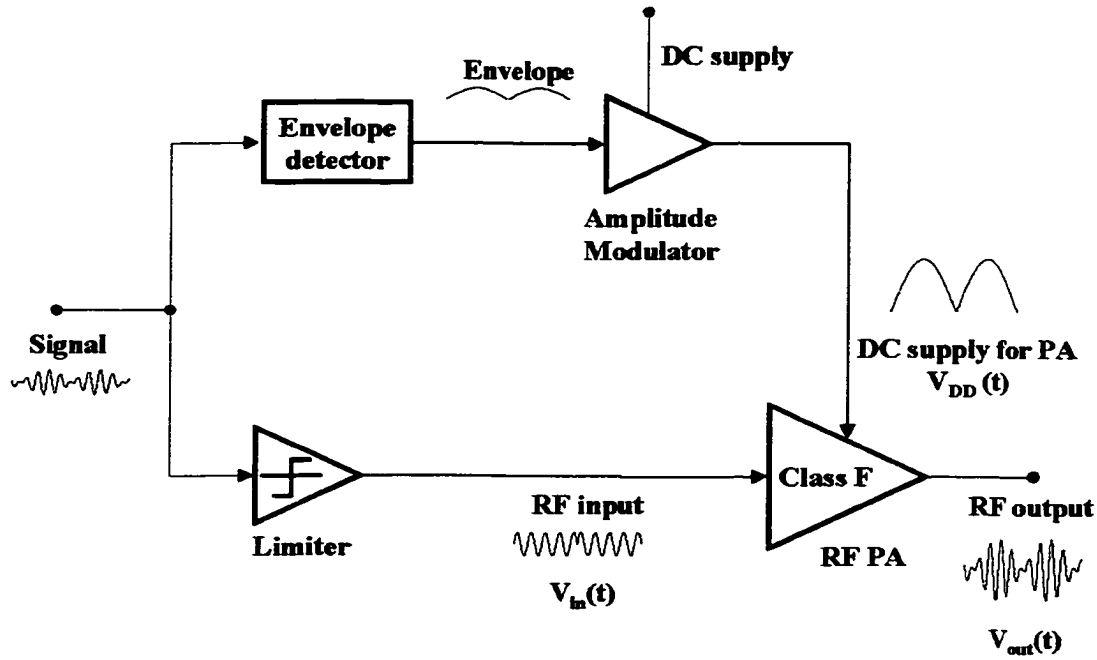


Figure 6.1. Block diagram of a classical Kahn EER transmitter system. The signal is separated into envelope and phase data, and the phase-modulated carrier drives the PA. The amplitude is restored by modulation through the drain DC supply.

parameters. Therefore, theoretically, perfect linearity can be obtained through drain amplitude modulation. In practice, the switch is nonideal and consequently some nonlinear behavior appears in drain amplitude modulation. This gives efficient linear amplification of the RF signal, since the PA gain is proportional to the drain bias.

In the classical Kahn method of Fig. 6.1, the amplitude of the phase-modulated drive signal is kept fixed at a large enough value to ensure optimal PA saturation and high efficiency at the peak envelope level. However, for lower envelope levels, a smaller drive signal is sufficient to cause the same degree of saturation and high efficiency. The same degree of saturation implies that the device is spending the same amount of time per period, in saturation. Therefore, by regulating the RF drive amplitude in proportion to the signal envelope, the efficiency of the Kahn method can be optimized over all envelope levels. Referred to as Kahn EER

with drive modulation, this method conserves RF drive power while keeping the PA saturated and provides linear, efficient amplification.

In contrast to the Kahn EER method, conventional linear PAs are not saturated, and the drain bias is kept fixed while the varying-envelope signal drives the PA. This fixed drain bias is large enough to allow maximum linear voltage swing for the highest signal envelope. Since smaller drive levels require less DC power for the same gain, this amplification method is not efficient at low drive levels. To alleviate this problem, the drain bias can be made to track the envelope of the input signal in order to regulate DC power consumption. This dynamic power control method, known as envelope tracking, allows higher efficiencies for all signal levels while keeping the PA in the linear regime.

6.3 Average Efficiency

The instantaneous efficiency of a PA is a function of the instantaneous input and output power and the class of operation. In this work, the instantaneous efficiency is defined as

$$\eta(E) = \frac{P_o(E)}{P_i(E)}, \tag{6.1}$$

where $P_o(E)$ is the output RF power and $P_i(E)$ is the total input RF and DC power as a function of the signal envelope, E. Depending on the class of operation of the PA, the instantaneous efficiency is proportional to the output power or the output voltage (envelope of signal). In practical PAs, the instantaneous efficiency usually achieves a maximum when the gain is compressed by about 3 dB.

Average efficiency is a good indicator of average power consumption in most communication systems with time-varying envelopes. It is defined as:

$$\overline{\eta} = \frac{\overline{P_o}}{\overline{P_i}}, \tag{6.2}$$

where $\overline{P_o}$ is the average output power and $\overline{P_i}$ is the average total input power. The

average input power is calculated as the expected value of $P_i(E)$, and the output power is calculated similarly. If the probability distribution function (PDF) of the envelope, $p(E)$ is known, where E is the envelope, the average input and output power can be calculated as

$$\overline{P_i} = \int_0^{E_{max}} P_i(E)p(E)dE, \tag{6.3}$$

and

$$\overline{P_i} = \int_0^{E_{max}} P_i(E)p(E)dE,$$

$$\overline{P_o} = \int_0^{E_{max}} P_o(E)p(E)dE. \tag{6.4}$$

The PDF of the envelope is a measure of the relative time corresponding to different envelope levels. The PDFs of some common signals are shown in Fig. 6.2. For frequency modulated (FM) and other constant-amplitude signals such as AMPS (Advanced Mobile Phone Service), the signal is always at peak output. Shaped-pulse data signals such as QAM have PDFs with peak-to-average power ratios of 3 to 6 dB [40]. Multi-carrier signals such as OFDM (offset frequency division multiplex) have Rayleigh PDFs [41] with typical peak-to-average ratios from 7 to 13 dB. Such signals are used in cellular communications, multi-beam satellite systems, and digital broadcasting.

The energy stored in a battery can be thought of as the product of average power drawn and the battery lifetime. Therefore, by increasing the average efficiency of a PA from 30% to 50% (a factor of 1.7), for the same average output power, the average input power drawn from the battery is reduced by 1.7 times, and the battery lifetime increased 1.7 times. At the same time, the average heat output is reduced by a factor of 2.3. Higher average efficiency [42] is obtained by having increased efficiency *over a large range of signal envelopes.*

In order to measure the average efficiency of different ampifier modes, we measure $P_i(E)$ and $P_o(E)$ for a sinusoidal input signal with amplitude E. From this measured data, the average input and output power is then calculated for a signal

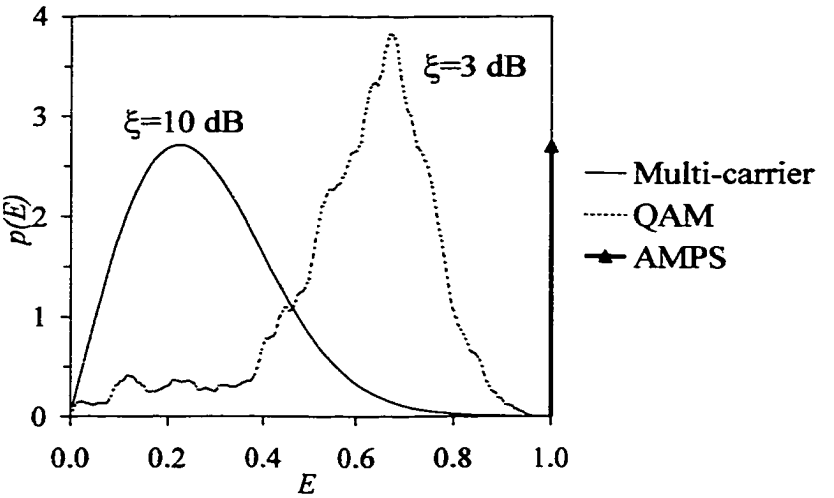


Figure 6.2. The probability distribution functions, $p(E)$, of some common signals. The Rayleigh distribution is for OFDM (multi-carrier) signals and the constant amplitude signal used in AMPS is always at peak power. E is the normalized time-varying signal envelope. ξ is the peak-to-average ratio, given in dB.

with any type of modulation with a known PDF. Note that for the Kahn modes, E is the drain voltage since the amplitude information is fed through the drain bias, and for the linear modes, E is the amplitude of the RF input signal since the drain bias is held a constant while the signal is fed into the RF input.

6.4 Linearity

6.4.1 Intermodulation Distortion In signals such as OFDM, discussed in 6.3, varying envelope levels give rise to AM and AM/PM effects which cause intermodulation distortion (IMD) in the output signal. For example, consider a nonlinear transfer function

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 + \ldots + a_n v_{in}^n, \tag{6.5}$$

where v_{in} and v_{out} are the system input and output signals in a system with an n-th order nonlinearity. a_1–a_n, are gain terms for each order. If v_{in} is a pure tone with a

constant amplitude, harmonics of each order will be generated by the system according to the transfer function in Eq. 6.5. Being out of band, these harmonics are easily filtered to obtain a pure-tone output signal. Therefore, there is no intermodulation distortion for a single-tone constant-envelope signal in a nonlinear system.

On the other hand, if the input signal contains multiple tones, the system nonlinearity creates in-band additives to the input signal spectrum, caused by *odd order* mixing of tones. For example, in the case of a two-tone input signal consisting of the sum of two single-tone constant-amplitude signals, second order mixing products, $(\omega_1 \pm \omega_2)$, fourth order products $(2\omega_1 \pm 2\omega_2)$, and all other even-order products don't distort the output signal since they are out-of band spectral components which are easily filtered out. The problems are caused by third order mixing products $(2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1)$, fifth order products, $(4\omega_1 \pm \omega_2$ and $4\omega_2 \pm \omega_1)$, and all other odd-order products. Usually, the third- and fifth-order products contribute most to the unwanted spectral growth at the signal output. The same is true for any multi-tone signal.

A signal with an arbitrary time-varying envelope can also be represented as a multi-tone signal. For example, an input signal with a time-varying single-frequency sinusoidal envelope, $A_{in}(t) = E\cos(\omega_m t)$, can be written as

$$\begin{aligned} v_{in} &= A_{in}(t)\cos(\omega_c t) \\ &= E\cos(\omega_m t)\cos(\omega_c t), \end{aligned} \tag{6.6}$$

where E is the envelope maximum, ω_m is the slowly varying modulating signal frequency, and ω_c is the carrier frequency. This can now be re-written as:

$$\begin{aligned} v_{in} &= \frac{E}{2}\cos((\omega_c - \omega_m)t + \frac{E}{2}\cos((\omega_c + \omega_m)t)) \\ &= \frac{E}{2}[\cos(\omega_1 t) + \cos(\omega_2 t)], \end{aligned} \tag{6.7}$$

which is the sum of the constant-amplitude single tones ω_1 and ω_2.

Several conventions are used in the literature to represent the degree of nonlinearity in a system. The figure of merit used in this thesis is the IMD (InterModulation Distortion) ratio, which is the the power in the highest-magnitude odd-order intermodulation product relative to the power in one of the tones in a two-tone signal as given by Eq. 6.7.

$$\text{IMD} = \frac{\text{Power in highest odd}-\text{order mixing product}}{\text{Power in one of the two input tones}} \tag{6.8}$$

This IMD is usually measured at the output of the power amplifier when it is under a two-tone excitation. The IMD varies as the power in the two-tone signal is varied, and is therefore usually quoted for peak output power conditions (the envelope of the output signal is maximum) when the distortion is typically worst.

6.4.2 Two-tone IMD Calculation based on Behavioral Modeling

Since two high-power sources at X-band were not available to measure the IMD at peak output power, it was calculated based on measurements of gain compression and phase distortion for a single tone excitation of the PA as a function of input signal power, or analogously, input signal envelope, E. This input RF signal can be written as $V_{in}(E) = E\cos(\omega t)$. The output signal as a function of this input signal amplitude (envelope) is then given by

$$V_{out}(E) = A_{out}(E)\cos(\omega t + \phi(E)), \tag{6.9}$$

where $A_{out}(E)$ is the amplitude modulation (AM) characteristic, and $\phi(E)$ is the amplitude to phase modulation (AM/PM), both of which are measured for each PA mode. Using this data, a behavioral model of each PA mode can be formulated that is then analyzed under a two-tone excitation. For the linearity calculation, a two-tone signal such as

$$V_{in,two-tone} = \frac{E}{2}\cos(\omega_1 t) + \frac{E}{2}\cos(\omega_2 t) \tag{6.10}$$

is input to the behavioral model. This two-tone signal can also be represented as

$$V_{in,two-tone} = E\cos(\frac{\omega_1 - \omega_1}{2}t)\cos(\frac{\omega_1 + \omega_1}{2}t), \tag{6.11}$$

which is a signal of frequency $\frac{\omega_1+\omega_2}{2}$ modulated by a slowly varying envelope of amplitude E and frequency $\cos(\frac{\omega_1-\omega_1}{2}t)$. This expression can be written as

$$V_{in}(E) = A_{in}(t)\cos(\omega t). \tag{6.12}$$

Thus, $V_{out}(t)$ can be calculated using Eqs. (6.9) and (6.12). Using a discrete Fourier Transform, the spectrum of the output signal, V_{out} , can then be analyzed. The power ratio between the carrier and the highest of the 3^{rd} and 5^{th} intermodulation distortion products is defined as the IMD. The IMD at peak output power is calculated for the Kahn modes. For the linear modes, the IMD is calculated at peak output power and at backed-off power. An acceptable value for IMD for communication applications is 30 dBc (dB below the carrier).

6.5 Definition of PA Modes

This work characterizes a single power amplifier for operation in five different biasing modes in order to determine the best method of dynamic bias control for high efficiency and linearity. Two linear modes of operation, one with fixed and the other with dynamic drain bias (envelope tracking), are compared with three modes of saturated PA operation, one being the classical Kahn method described in section 6.2, and the other two being modified Kahn methods with drive modulation. The five PA modes represent specific relationships between the drain voltage and RF signal amplitude, and are shown graphically in Fig. 6.3(a) as listed below:

(1) Linear: the signal is fed directly into the RF input, and the drain voltage is fixed. This mode is called linear mode because the amplifier is unsaturated;

(2) ET (Envelope Tracking): Linear operation with dynamic drain voltage proportional to signal envelope;

(3) Kahn: Classical Kahn operation as in Fig. 6.1 with fixed RF drive;

(4) Kahn FDM (Full Drive Modulation): modified Kahn mode, with dynamic RF input amplitude proportional to signal envelope; and

(5) Kahn PDM (Partial Drive Modulation): another modified Kahn mode. Similar to the Kahn FDM mode, but having a minimum value for the drive, in order to increase efficiency at low envelope levels.

The fixed-bias linear mode and the Kahn mode are not dynamic in that either the drain is kept fixed or the drive is kept fixed, as can be seen in Fig. 6.3(a). The envelope tracking, Kahn FDM, and Kahn PDM modes are dynamic since both the drain and the drive amplitudes change simultaneously. Fig. 6.3(b) shows the instantaneous efficiency of the PA used in this study as a function of drain bias and drive amplitude. It is apparent from this graph that dynamic control of both values is necessary for maintaining high instantaneous efficiency.

Analogously, variation of the gate bias (quiescent current) in a RF PA also results in significant savings of DC-input power. However, minimum drive and gate bias levels are often required to ensure proper operation of the RF final amplifier and modulator [43]. The minimum drive/gate-bias level ensures saturation of the PA in spite of gain reduction and/or reduces amplitude-to-phase conversion by decreasing the degree of saturation so that nonlinear capacitance variations are reduced. All five PA modes listed above were measured with various gate biasing schemes. However, there was almost no change in average efficiency between these PA schemes, and the linearity proved to be low. Therefore, for all measurements described in the following text, the gate bias is kept fixed.

6.6 Measurements

The power amplifier used for this study is an 8.4 GHz class-F PA [44] designed with a Fujitsu FLK052WG MESFET, and described in Chapters 3 and 4.

This PA provides a maximum instantaneous efficiency of 55% with 610 mW of output power and 5.3 dB saturated gain with $V_{GS} = -0.9\,V$ and $V_{DS} = 7\,V$. The electrical characteristics of this power amplifer are discussed in Chapter 4.

Each PA mode is implemented by manually changing the drain voltage and drive signal amplitude according to the relationships shown in Fig. 6.3(a). By monitoring the RF and DC power levels, and the phase of the output signal, $P_i(E)$, $P_o(E)$, $V_{out}(E)$, $\phi(E)$ are measured for each PA mode. E is the RF signal amplitude for the linear modes and the drain voltage for the Kahn modes. The power and phase are measured using an HP70820A Transition Analyzer. An HP83020A preamplifier is used to amplify the power levels from an HP83650A synthesized sweeper so as to saturate the class-F PA. From this data, the average efficiency and linearity are calculated for each mode as described in section 6.3.

6.7 Comparison of Modes

The effect of dynamic biasing on average efficiency can be shown by comparing the measured instantaneous efficiency as a function of output signal amplitude, as illustrated in Fig. 6.4. The linear amplifier with fixed bias has very low efficiency at low power levels. The Kahn method, where the RF drive level is fixed, has higher efficiency on average than the linear case due to PA saturation. However, the dynamic biasing schemes (envelope tracking, Kahn FDM, and Kahn PDM) have much higher efficiency over the entire range of output levels. Kahn PDM has the best efficiency performance of all the modes. Based on measurements of $P_i(E)$ and $P_o(E)$ and the PDFs given in Fig. 6.2, the predicted average efficiency for multi-carrier and QAM signals is calculated as shown in Table 6.1.

Each of the techniques, however, exhibits different AM/PM characteristics, $\phi(E)$, as shown in the measured data in Fig. 6.5. The classical and PDM Kahn methods have a large increase in AM/PM, due to deep saturation of the PA at low

envelope levels.

The measured amplitude modulation linearity, given by the input-output transfer characteristic $V_{out}(E)$, is shown in Fig. 6.6. The peak output level for all modes is about 8 V. The linear modes saturate at high envelope levels and therefore must be operated in back-off for high linearity. The Kahn modes, on the other hand, have input-output characteristics which are approximately straight lines over the entire envelope range. However, the classical Kahn and Kahn PDM modes suffer from *feedthrough*, which occurs in an amplifier when a zero input signal envelope on the drain results in a non-zero output due to the feedback capacitance of the device. This degrades the linearity and also reduces dynamic range of the output. The Kahn FDM technique gives no feedthrough and gives the highest amplitude modulation linearity.

6.7.1 Multicarrier Results The predicted linearity and average efficiency of the various techniques are summarized in Table 6.1. The presented data includes the average efficiency for multi-carrier signals with a 10 dB peak to average ratio, and for QAM signals with a 3 dB peak to average ratio. Peak power for all modes is about 0.6 W, corresponding to a maximum output envelope of about 8 V. The probability distribution functions of both these signals are shown in Fig. 6.2. The overall amplifier linearity is obtained from a combination of the measured AM and AM/PM effects, as described in section 6.3. One would expect the linear mode in back-off to have the highest linearity, measured to be 27 dBc, albeit with low efficiency (less than 10%). Instead, the FDM Kahn technique, yields a slightly better linearity, 28 dBc, with a significantly improved average efficiency of 44% (at least a factor of 4.4 improvement).

6.7.2 QAM Results For QAM signals, the classical Kahn method gives better efficiency than the linear fixed-bias mode, but the dynamic biasing

Power amplifier modes 8.4 GHz	Predicted IMD ratio (dBc)	Predicted average efficiency		Peak Power (W)
		Multi-carrier -10 dBPEP	QAM -3 dBPEP	
Kahn	23.8	26.4%	43.8%	0.66
Kahn-FDM	27.7	43.7%	53.4%	0.66
Kahn-PDM	26	46.7%	54.4%	0.62
Linear (fixed drain)				
Full power	17	9.5%	28.7%	0.61
0.67 of full power	27			0.41
Envelope tracking				
Full power	23.1	36.1%	49.5%	0.72
0.7 of full power	24.6			0.50

Table 6.1. Comparison of average efficiency and linearity results. The predicted values are obtained by analyzing PA models formed by measuring the characteristics of each mode under a single-tone excitation.

schemes (envelope tracking, FDM and PDM Kahn) have much higher average efficiencies and are all comparable. This is because the PDF for the QAM signal is only 3 dB below the peak envelope level, where all the dynamic biasing schemes have similar performances.

6.7.3 Summary of Results In reviewing the efficiency and linearity data of Table 6.1, it is important to note the following:

(1) Kahn EER can be used to linearize highly nonlinear amplifiers such as saturated class-F and E;

(2) The average efficiency and linearity of Kahn EER can be increased by drive modulation;

(3) The average efficiency and linearity of a fixed bias class-F amplifier can be increased by dynamic drain biasing (envelope tracking);

(4) Dynamic modes have higher average efficiency and linearity;

(5) For approximately the same output power, the saturated dynamic modes (Kahn FDM, PDM) give higher efficiency and linearity than the dynamic linear method (ET); and

(6) Kahn EER with full drive modulation gives the highest linearity at the peak output level, while increasing the average efficiency of the PA by a factor of 4.4 over the case of the unlinearized, fixed-bias PA.

6.8 Discussion

In summary, this chapter discusses the average efficiency and linearity of an 8.4 GHz class-F nonlinear X-band PA intended for use in transmitters with time-varying signal envelopes. The class-F amplifier has a high instantaneous efficiency for high signal amplitudes, but low efficiency for smaller signals, yielding a poor efficiency when averaged over time. We show experimentally that several different dynamic power control techniques can be used to improve the average amplifier efficiency, and that the best simultaneous efficiency and linearity is obtained by a modified Kahn EER technique. For example, the average efficiency for a Rayleigh distribution of signal amplitudes (multi-carrier OFDM) was improved to 44% for this amplifier at a peak output power of 0.6 W, with intermodulation distortion products suppressed to 28 dBc. The same amplifier operated in linear fixed-bias mode has only 10% average efficiency, with 17 dBc distortion at the same output power.

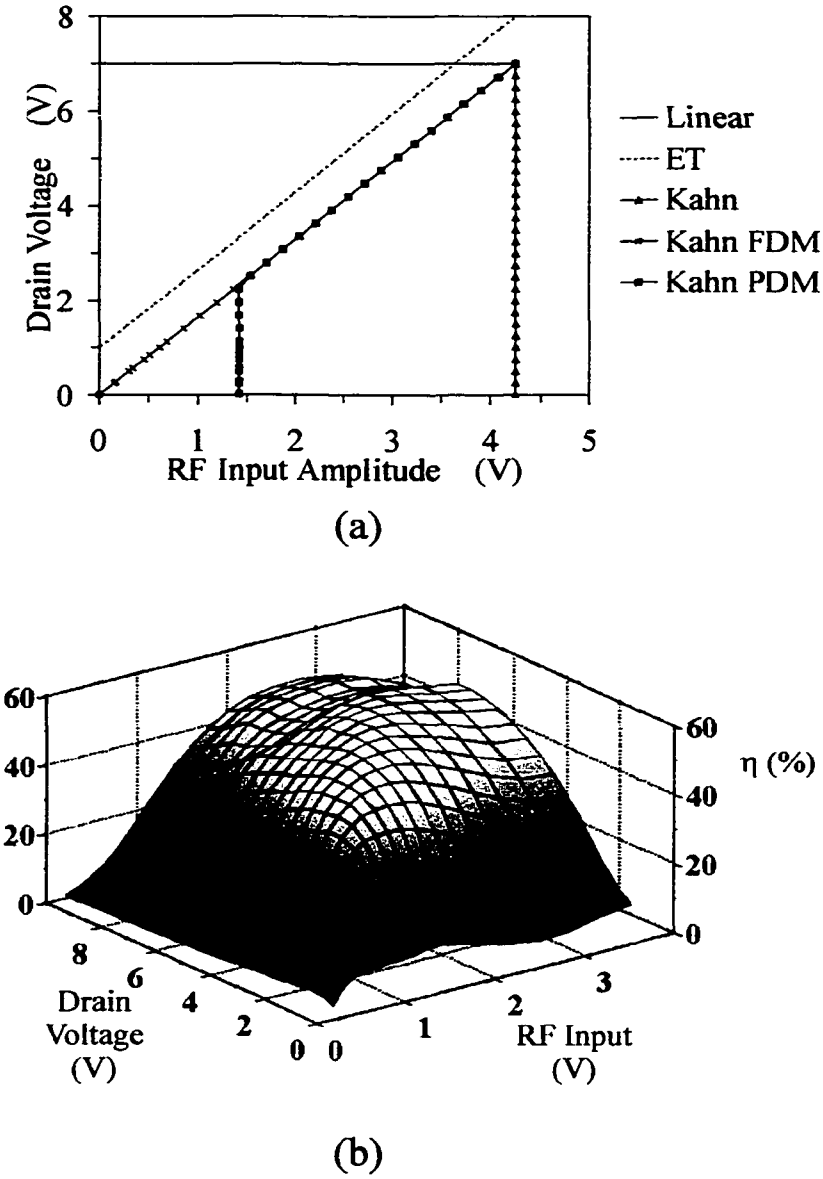


Figure 6.3. (a) The five modes of PA operation compared in this paper. Each mode represents a specific relationship between the drain bias and the instantaneous envelope of the RF input. Two linear modes are compared with three Kahn modes where the PA is saturated. (b) Instantaneous efficiency as a function of drain bias and RF input amplitude. By varying both voltages in a dynamic manner, the efficiency can be optimized for all input envelope levels.

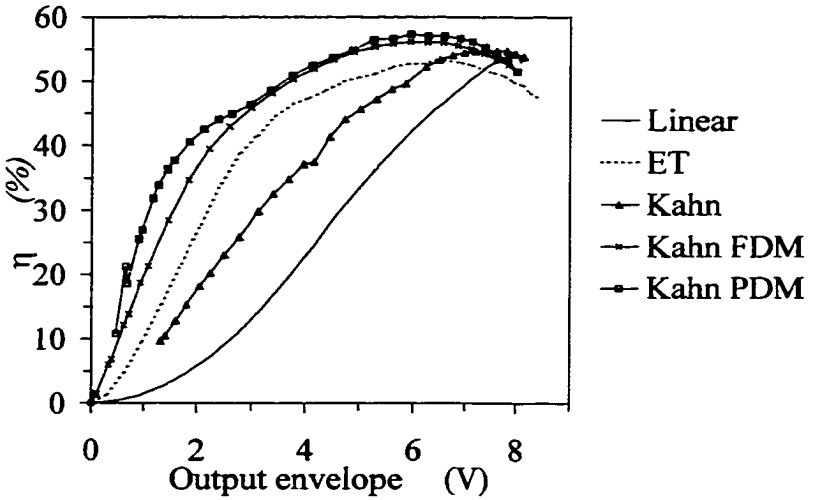


Figure 6.4. Measured instantaneous efficiency of the PA modes. The efficiency is decreased for low signal levels.

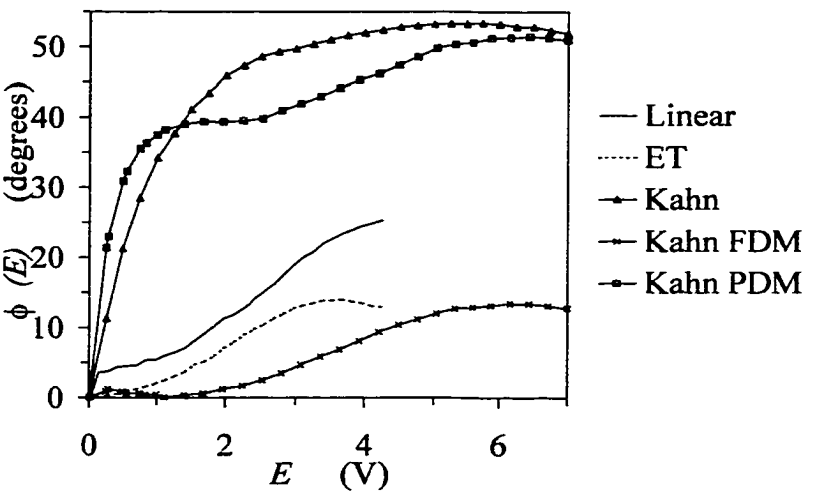


Figure 6.5. Measured AM/PM of the PA modes. For the Kahn modes, the envelope is the drain voltage (0-7 V), and for the linear modes, it is the amplitude of the RF input (0-4.24 V).

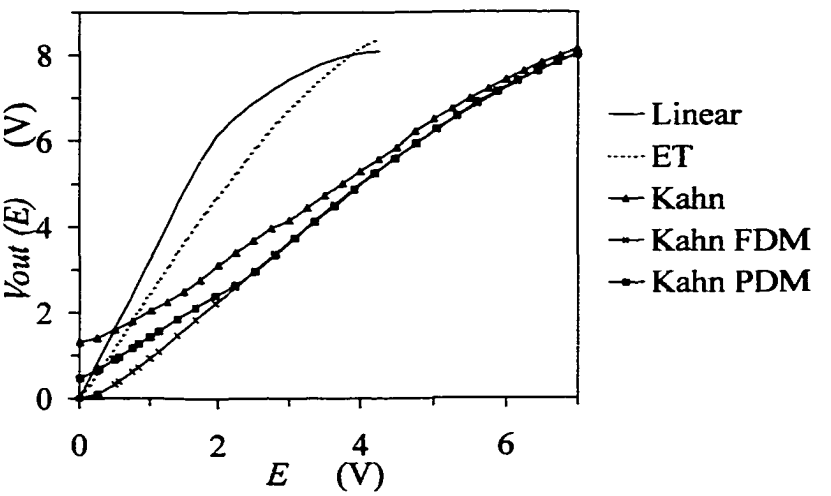


Figure 6.6. Amplitude modulation linearity of the PA modes. V_{out} is the amplitude of the output signal, which has a peak value of about 8 V. For the Kahn modes, the envelope is the drain voltage (0-7 V), and for the linear modes, it is the amplitude of the RF input (0-4.24 V).

CHAPTER 7

HIGH-EFFICIENCY CLASS-E FREQUENCY MULTIPLIERS

7.1 Introduction

The previous chapters in this thesis have discussed the performance of switched-mode high-efficiency power amplifiers at microwave frequencies up to 10 GHz, while nothing has been said about the generation of the signal itself. In most modern microwave and millimeter-wave communication systems, the signal from a low-frequency, high-quality oscillator is multiplied up to the desired frequency by a chain of frequency multipliers, a general background of which can be found in [6]. One of the main objectives in the use of frequency multipliers at microwave and millimeter-wave frequencies is to separate the signal generating circuitry from the amplification circuitry. This physical and electrical isolation reduces heating of the oscillator due to heat generated by the power amplifiers, while at the same time avoiding potentially unstable feedback of the power amplifier output into the oscillator. As a commercial example, automotive radar systems at 60 and 76 GHz have been reported to use frequency doublers [45], [46]. The output of this frequency multiplier chain is the local oscillator (LO) signal which produces the RF carrier when mixed with the modulated intermediate frequency (IF) signal.

Although transistor frequency multipliers do not consume the vast amounts of power that power amplifiers do, they are the primary cause of power dissipation in LO circuitry, and recent efforts have focused on the design of power-efficient frequency multipiers. For example, low-cost, low-power frequency multipliers with

outputs at 762 MHz and 3.050 MHz have been fabricated for mobile wireless applications [47]. Apart from wasting available power resources, the heat that is produced by the frequency multipliers can cause thermally induced instabilities in the oscillator frequency [6].

High-efficiency class-E frequency multipliers could present a viable method of minimizing heat dissipation near the oscillator as well as lowering power consumption in the LO circuitry. This chapter presents a 10.4/20.8 GHz MESFET frequency doubler designed to be highly efficient by operating in class-E mode, in addition to providing conversion gain.

7.2 Conversion Gain, Efficiency, and Harmonic Rejection

There are several parameters of interest when comparing different frequency multipliers. Most important among these are conversion gain, DC-RF or drain efficiency and overall efficiency, which are defined as,

$$G = \frac{P_{out}(Nf)}{P_{in}(f)}, \tag{7.1}$$

$$\eta_D = \frac{P_{out}(Nf)}{P_{dc}}, \tag{7.2}$$

$$\text{and} \qquad \eta = \frac{P_{out}(Nf)}{P_{in}(f) + P_{dc}}, \tag{7.3}$$

where $P_{out}(Nf)$ is the output power at the desired harmonic and $P_{in}(f)$ is the input fundamental power. P_{dc} is the input DC power. Typically the efficiency quoted in the literature on multipliers is the conversion efficiency, which is the gain expressed as a percentage. A conversion efficiency of less than 100% implies a conversion loss. In this work, the term *conversion efficiency* will be avoided in favor of the term conversion gain. The only efficiencies of importance here are the drain and overall efficiencies, since they determine the DC and RF power consumption of the multiplier.

Another important quantity to consider in frequency multiplier design is the

harmonic rejection. The fundamental power at the output must be much lower than the power at the desired harmonic. This is usually accomplished by using an open or shorted output stub to suppress fundamental frequency output power. Harmonic rejection is presented as a ratio of fundamental power to desired harmonic power, in dBc, or dB below the carrier, and an acceptable value is about 20 dBc. At the input, a shorted or open stub at the output frequency is used to suppress parasitic feedback of output power to the input. The input and output harmonic terminations of the frequency multiplier can have a profound effect on the conversion gain, as discussed in detail by several authors in [48], [49] and [50].

7.3 Types of Frequency Multipliers

Any nonlinear device can be used as a frequency multiplier; Schottky diodes which act as nonlinear resistances and varacter diodes which are nonlinear capacitances are good candidates for this purpose. Transistor frequency multipliers rely on nonlinear resistances and capacitances within the device as well as nonlinear current-voltage relationships.

7.3.1 Diode Frequency Mutipliers A thorough treatise on this subject can be found in [51], which presents most of the theory behind diode frequency mulitiplier operation. Schottky diodes offer broadband operation due their resistive nature while varacter diodes and Gunn diodes have lower phase-noise. Essentially, the capacitive or resistive nonlinearity in a diode is exploited to generate higher harmonic components of a fundamental input frequency. The harmonic of interest is then extracted by suitable output circuit matching.

As an example, in COMSAT communication satellites, the signal generated by a high-Q, stable 9.5 GHz oscillator is doubled by a diode chain for use as a beacon [52]. Operating with a conversion gain of -2.2 dB, this diode multiplier has an output power of 14.8 dBm at 19 GHz. In [53] a 40/80 GHz balanced doubler using

six varacter diodes gives 96 mW of output power with an input of 200 mW, which corresponds to a conversion gain of -3.2 dB. At 25 and 40 GHz, 100 mW output power levels are obtained for diode doublers with a conversion gain of about -4.5 dB [54]. As can be seen from these examples, diode mutipliers are lossy since diodes cannot provide signal gain. The maximum gain is then unity, although in practice losses within the diodes limit the gain to below unity. Therefore, high-gain amplifiers, which are typically inefficient, must be used to obtain sufficient output power. On the other hand, transistors such as bipolar junction transistors (BJTs), metal semiconductor field effect transistors (MESFETs) and high electron mobility transistors (HEMTs) can amplifiy the generated harmonic signal, and therefore can give greater gain and output power.

7.3.2 FET Frequency Multipliers To overcome the lossy nature of diode multipliers and achieve frequency multiplication with small conversion losses or conversion gain, transistor frequency multipliers have been investigated, as discussed at length by Camargo in [55]. For integration into MMICs, FET-based multipliers are most attractive since FETs are the building blocks of MMICs. Therefore, this discussion is limited to recent results obtained using FETs such as MESFETs, HEMTs and pHEMTs. In particular, the focus is on frequency doubling.

Harmonic generation occurs in FETs due to several nonlinear mechanisms, including nonlinearity of the input gate-source capacitor, the nonlinear transconductance, the nonlinear output conductance, and the clipping of the drain-source current. A comparison of these nonlinearities for frequency doubling is carried out by Gopinath et.al. in [56], which shows that current-clipping gives considerably higher second harmonic levels than the other mechanisms. Current-clipping is achieved by biasing the FET near pinch-off or near $V_{gs} = 0V$, which is near forward conduction of the transistor.

Since current-clipping is the main mechanism for generating second harmonic content, the switched current of class-E amplifiers seems suitable for frequency doubler design with both high gain, harmonic output power and high drain efficiency.

At X-band output frequencies, the doubler conversions gains reported are in the -3 to 8 dB range [56], [57], [58], [59], [60], [61]. The highest drain efficiency found in the literature at X-band is 66.7%, with 1 dB gain and 13 dBm output power at 8 and 12.5 GHz [61]. All other reported drain efficiencies in the references given above, are about 10%, while output power are on the order of 10-20 dBm.

At K-band (18-26 GHz), doubler conversion gains of 4 dB and -1.8 dB are reported 18 and 20 GHz output frequencies [58] while at a 24 GHz output frequency, -1.9 dB conversion gain was obtained with a drain efficiency of about 5% [62]. The typical output power is about 0 dBm.

7.3.3 Class-E Frequency Multipliers Class-E power amplifiers have a theoretical DC-RF power conversion efficiency of 100% by operating the transistor as a switch [9] and have been demonstrated at microwave frequencies upto 10 GHz [63]. Class-E multipliers with drain efficiency greater than 95% have been discussed and tested at an output frequency of 3.37 MHz [64]. In [65], class-E multipliers have been demonstrated at 1 GHz and 5 GHz output frequencies with power-added efficiencies of 35% and 29% respectively. The corresponding conversion gains for the last two cases are 8.5 dB and 5.2 dB [13].

The use of class-E topology at higher frequencies is limited only by device output capacitance, maximum current capability, and drain voltage [10]. For today's typical devices this frequency limitation is at about 1-6 GHz. The results obtained for class-E power amplifiers in [65] and [63] are at frequencies about a factor of 1.5-3 above the maximum frequency for ideal class-E operation. This causes class-E performance to be suboptimal, with a resulting decrease in achievable efficiency. However, even in suboptimal mode, the efficiency of class-E circuits is higher than

other classes. A drain efficiency of 74% and a PAE of 62% were measured at 10 GHz on an active antenna [63] using a commercial device produced by Alpha Industries. The same device is used here in a 10.4/20.8 GHz frequency doubler.

The main objective of this work is to demonstrate the viability of suboptimal class-E frequency doublers as an alternative method of RF power generation at K-band with high DC-RF efficiency, reasonably high output power and conversion gain. As a secondary objective, the drain- and gate-biasing requirements and output power are compared for class-E amplifiers and class-E frequency doublers, in order to further investigate class-E operation at microwave frequencies.

7.4 Previous Work on Class-E Multipliers

The design of class-E frequency multipliers has been analyzed by Zulinski and Steadman in [64], assuming an ideal switch and an output circuit with infinite Q. In the basic circuit diagram of Fig. 7.1, the transistor is switched between ON and OFF states by a rectangular wave of duty cycle D and period T. The corresponding radial frequency is ω. The only difference between this analysis and the class-E amplifier theory presented in Chapter 2 is that the output is constrained by the tuned circuit to be at a harmonic $N\omega$; for $N = 1$, the analysis simplifies to the case of the class-E amplifier. However, this small difference causes the operating conditions (duty cycle, output impedance and drain voltage) for a class-E multiplier to be quite different from that of an amplifier. The work in [64] is summarized here for clarity. The goal is to obtain design conditions for a class-E multiplier of order N when the load R and switching frequency f are known.

The duty cycle, D, is the fraction of the period $T = 2\pi/\omega$ for which the switch is OFF, and the switch voltage, v_s, is nonzero. The DC current is I_{ds} and the output current is

$$i_o = A\sin(N\omega t + \phi) \tag{7.4}$$

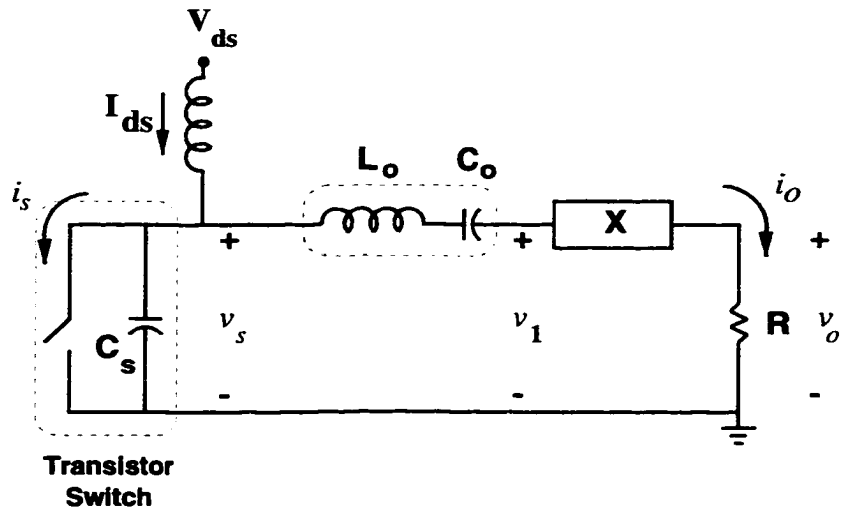


Figure 7.1. The switch and output circuit for the general class-E multiplier circuit. The transistor switch is represented as an ideal switch in parallel with a capacitance. L_o and C_o comprise an ideal tuned circuit, providing the transistor output with a load impedance $Z_{net} = R + jX$ at the output frequency, while presenting an open circuit to all higher harmonics.

The current through the capacitor during the OFF cycle is $C_s \frac{dv_s}{dt}$. By considering Kirchoff's current law at the drain node, the following differential equation is obtained for the OFF cycle.

$$C_s \frac{dv_s}{dt} = I_{ds}[1 - A\sin(N\omega t + \phi)] \tag{7.5}$$

Eq. 7.5 can be solved by integrating to obtain an expression for the time-domain switch voltage as follows.

$$\begin{aligned} v_s(t) &= \int \frac{I_{ds}}{C_s}[1 - A\sin(N\omega t + \phi)]dt \\ &= \frac{I_{ds}}{C_s}[t + \frac{A}{N\omega}\cos(N\omega t + \phi)] + K, \quad 0 < t < DT. \end{aligned} \tag{7.6}$$

The unknowns in Eq. 7.6 are C_s, K, A, ϕ and D. Therefore, in order to solve for v_s at any arbitrary time t during the OFF cycle, five equations are necessary, and are obtained by considering the requirements for 100% DC-RF efficiency and maximal output power capability.

100% DC-RF conversion efficiency is obtained when the switch voltage is zero during the ON state. This means that during the OFF state, the switch voltage must begin and end at zero, implying that $v_s(t) = 0$ for $t = 0, DT$. This supplies two equations for the solution of Eq. 7.6. A third equation is provided by the condition that the input DC power must equal the output power dissipated in the load resistance, or $V_{ds}Ids = (AI_{ds})^2/2R$. V_{ds} is the time-average of the switch voltage waveform of Eq. 7.6.

Two more equations can be obtained by maximizing the output power capability defined in Eq. 2.12. The maximal output power capability for a general class-E multiplier is found by setting R and the ratio V_{ds}/I_{ds}, and calculating the output power capability for various values of ξ and D; ξ is the slope, dv_s/dt, with which the voltage waveform goes to zero at the end of the OFF cycle, at $t = DT$. The optimum values are found to be $\xi = 0$, and $D = 0.5/N$. ξ determines the magnitude of the current at switch turn-on due to capacitor discharge through the switch. It affects both the output power and the voltage and current swings (apart from the current impulse) at the switch. The duty cycle affects the generation of the desired harmonic.

In summary, three equations enforce the condition of 100% DC-RF efficiency, and two equations pertain to maximizing the output power capability. With these five conditions, it is possible to solve for the unknowns to obtain the following main results for class-E multiplier design:

$$C_s = \frac{0.1836}{N^2 R\omega}, \tag{7.7}$$

$$\text{and} \quad X = 1.1525R. \tag{7.8}$$

Additionally, expressions for $v_s(t)$, $i_s(t)$ and P_{out}, among others, are also presented in the Zulinski paper. For the purposes of this thesis, it is more appropriate to assume the switch capacitance is known and solve for the load impedance, $Z_{net} = R + jX$,

necessary at the desired harmonic. This is the direction taken by the analysis that follows, in which the goal is to study the relationship between the drain voltage, gate biasing conditions and the switching frequency for class-E amplifiers and doublers.

7.5 Simplified Class-E Multiplier Analysis

In addition to a re-interpretation of previous work as needed for practical microwave high-efficiency multipliers, this thesis contributes a new theoretical derivation for the critical frequency between ideal and suboptimal class-E operation, and the estimation of the duty cycle. The maximum switching frequency for class-E operation is an important consideration in the design of a class-E multiplier circuit, since it is determined by the device being used, the bias point and the multiplier order. If these factors dictate a maximum frequency less than the switching frequency desired, then a new device and/or bias point must be chosen. The duty cycle is a very important criterion for class-E multiplier operation. It determines the load impedance presented to the transistor output, and therefore class-E operation. Only by biasing and driving the multiplier such that the correct duty cycle is obtained, can class-E waveforms be expected.

This analysis begins with the same differential equation (Eq. 7.5) as Zulinski, but the transistor capacitance is known instead of the load, and time is referenced to the begining of the OFF cycle instead of the center. The analysis in this section is more tractable than that in Zulinski's paper and therefore more instructive to the beginner.

In analogy to the class-E power amplifier theory in section 2.4, the differential equation in Eq. 7.5 is solved with the following four boundary conditions:

$$v_s(0) = 0, \tag{7.9}$$

$$v_s(DT) = 0, \tag{7.10}$$

$$\left.\frac{dv_s}{dt}\right|_{t=DT} = 0, \tag{7.11}$$

$$\text{and} \quad D = 0.5/N. \tag{7.12}$$

The first three conditions are idential to the class-E power amplifier case, wheras the duty cycle is now a function of N. The following results are obtained:

$$K = -\frac{I_{ds}}{C_s}\frac{A}{N\omega}\cos(\phi), \tag{7.13}$$

$$A = 1.862, \tag{7.14}$$

$$\text{and} \quad \phi = -0.5669\,\text{rad}. \tag{7.15}$$

It should be pointed out here that these results are slightly different from Zulinski and Steadman's in that ϕ, given in radians, is independant of N. This is due to the fact that in this analysis time is referenced to the beginning of the duty cycle. When time is referenced to the center of the OFF cycle, the duty cycle and the duty cycle start time are functions of the desired harmonic. This results in the phase of the output current and voltage also being functions of the output harmonic.

The switch voltage and current waveforms are shown graphically in Fig. 7.2. The voltage waveform during the OFF cycle is presented in Eq. 7.6 and the current waveform during the ON cycle is

$$i_s(t) = I_{ds}[1 - A\sin(N\omega t - \phi)] \tag{7.16}$$

where maximum possible current swing is assumed such that $I_{ds} = I_{max}/(1 + A)$.

As seen in Fig. 7.2, the voltage swing at the switch decreases for the doubler ($N = 2$) compared to the amplifier ($N = 1$) while the current swing remains the

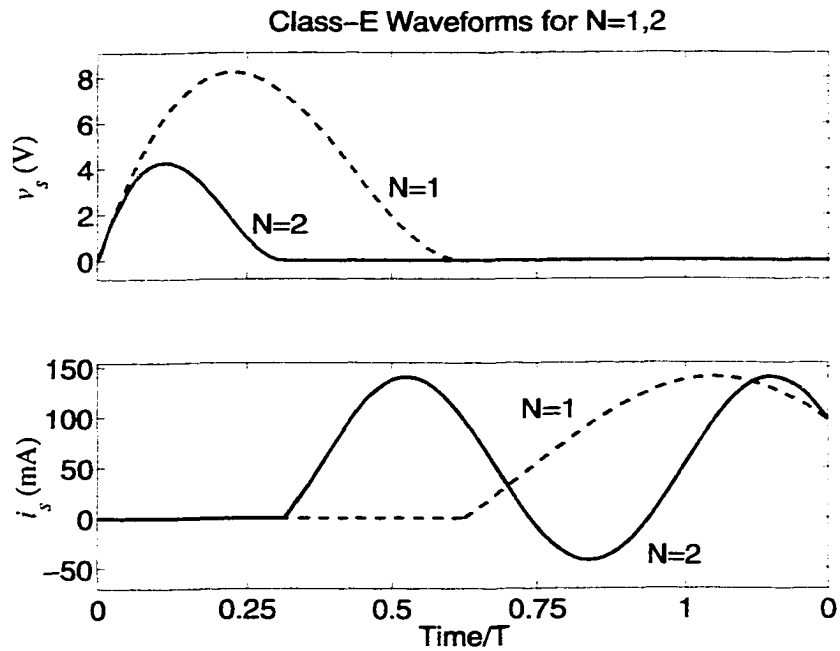


Figure 7.2. Simulated switch voltage and current waveforms for a class-E amplifier and a doubler designed with an Alpha AFM04P2 MESFET. The switch capacitance is 0.107 pF, the switching frequency is 10 GHz, and the maximum drain current is 140 mA.

same. The output voltage swing is also reduced as N increases, even though the output current is the same. This produces a reduction in the output power. The reduction in switch voltage swing with N is the result of the device having to charge and discharge in a shorter duty cycle. The slope at which the switch capacitor charges is a constant regardless of N, and depends only on the ratio I_{max}/C_s. For higher output power it is desirable to maximize this ratio.

Also of note is that the switch current for $N > 1$ is bidirectional (both positive and negative) whereas it is unidirectional for the case of the class-E amplifier. This makes FETs rather than BJTs more suited to the design of class-E multipliers since FETs can support bidirectional current flow when the drain and source voltages are reversed.

7.6 Extended Analysis of Class-E Multipliers

Using the previously reported class-E multiplier analysis presented in the previous sections, the drain biasing, frequency limitations, output power considerations, and duty-cycle determination is analyzed in more detail in the following sections.

7.6.1 Drain Biasing of Class-E Multipliers By performing a Fourier series analysis on the time domain switch waveform, the DC drain voltage is found.

$$\begin{aligned} V_{ds} &= \frac{1}{T_s}\int_0^{DT} v_s(t)dt \\ &= \frac{I_{ds}}{2\pi^2 C_s f N^2} \end{aligned} \tag{7.17}$$

The procedure is similar to those discussed in [3]. T and f are the switching period and frequency respectively. Since the maximum possible switch current is $i_{max} = I_{max} = (1+A)I_{ds}$, the drain voltage for class-E operation can be written thus:

$$V_{ds} = \frac{I_{max}}{56.5 C_s f N^2} \tag{7.18}$$

This means that for the same switching frequency, the drain voltage must decrease as N^2 for an output at a harmonic Nf. This is primarily because the duty cycle decreases with N, while the capacitor-charging slope at $t = 0$ remains the same. This implies a lower peak switch voltage and correspondingly small DC component.

If a drain voltage lower than the knee voltage of the device is required, then a class-E multiplier of that order is not possible. Suboptimal operation might be possible with a slightly higher drain voltage, but degradation in efficiency and output power will result.

7.6.2 Maximum Class-E Frequency of Operation Eq. 7.18 can be rearranged to solve for the maximum frequency of class-E operation at a given drain voltage for a given device:

$$f_{max} = \frac{I_{max}}{56.5 V_{ds} C_s N^2} \tag{7.19}$$

This frequency limit occurs because of a finite capacitor-charging slope, as discussed in the previous sections. By using a device with a larger ratio of maximum current to switch capacitance, this slope can be increased, with a resulting increase in the maximum switching frequency. Also, reducing drain voltage will allow the charging and discharging of the capacitor to occur within the duty cycle since the peak of the waveform will be lowered.

In addition, when building higher-order multipliers with suboptimum class-E operation ($f > f_{max}$), the drain voltage must be decreased to maintain the same f_{max}. This may be considered as maintaining the same level of suboptimal behavior.

7.6.3 Load Impedance of a Class-E Frequency Multiplier The previous sections discussed DC drain voltage and frequency requirements for class-E operation using a given device. The next important design consideration is the load impedance presented to the transistor output. The output circuit is considered to have infinite Q at the frequency of the desired output harmonic, which causes a sinusoidal current to flow in the load at this frequency. Therefore, all other harmonics are presented with an open circuit while the desired harmonic has a load impedance given by the ratio of output voltage, v_1, to output current i_o.

In the following analysis, $\omega = 2\pi f$ is used such that the final expressions are obtained as functions of frequency, f. The complex Fourier series of the switch voltage waveform is given by,

$$v_s(t) = K_0 + \sum_{n=-\infty}^{\infty} K_n e^{j2\pi nft} \tag{7.20}$$

where K_0 is the time average or V_{ds}, and the complex coefficients K_n are calculated as usual using the following equation.

$$K_n = \int_0^{DT} v_s(t) e^{-j2\pi nft} dt. \tag{7.21}$$

The harmonic component corresponding to N is given by

$$V_s(Nf) = (K_N + K_{-N})\cos(2\pi Nft) + j(K_N - K_{-N})\sin(2\pi Nft), \tag{7.22}$$

and is found to be

$$V_s(Nf) = \frac{3.278\, I_{ds}\, e^{-1.2816}}{4\pi^2 C_s f N^2}\, e^{j2\pi N f t}. \tag{7.23}$$

This voltage appears across the load impedance that bears a current

$$I_s(Nf) = 1.862\, I_{ds}\, e^{-j0.5669}\, e^{-j\pi/2}\, e^{j2\pi N f t}. \tag{7.24}$$

The load impedance, $Z_{net} = R + jX$, is then calculated from the ratio of the voltage and current phasors.

$$Z_{net}(Nf) = \frac{0.0446}{C_s f N^2}\, e^{j49.05^\circ} \tag{7.25}$$

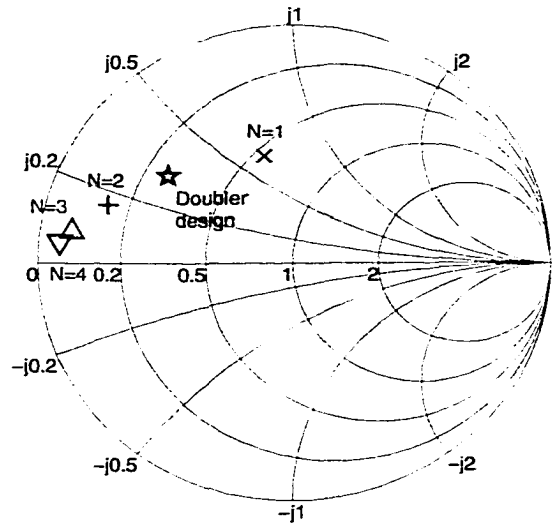
All other harmonics are presented with an open circuit. For the case of the class-E amplifier, this equation is the same as that presented in [3] and [10]. For frequency multipliers, the load impedance scales as $1/N^2$.

As an example, consider a practical MESFET device manufactored by Alpha Industries, AFM04P2. Based on the device specifications provided by the manufacturer, the optimum loads were calculated and are shown in Fig. 7.3. As can be seen, the load impedance changes with N and approaches a short circuit as the multiplier order is increased, causing output mismatch problems in a $50\,\Omega$ environment to become more pronounced, limiting the gain of the frequency multiplier.

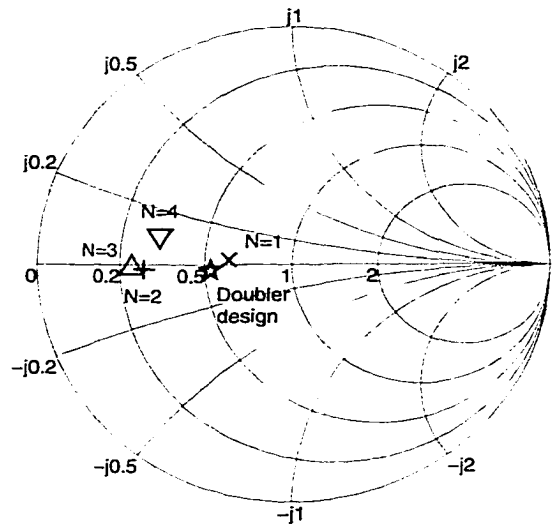
7.6.4 Output Power of a Class-E Frequency Multiplier The output power is the power delivered to the real part of the load impedance, R, and can be calculated from $i_o^2 R$. It is given by

$$P_o = \frac{0.0062\, I_{max}^2}{C_s f N^2}. \tag{7.26}$$

This shows that the output power for an ideal doubler is 6 dB lower than that for an ideal class-E amplifier, assuming that switch capacitance and parasitic resistance remain the same at the doubled frequency. The drain-source capacitance de-embedded from s-parameters is 0.107 pF at 10 GHz, and 0.103 pF at 20 GHz. This is a change



(a)



(b)

Figure 7.3. (a) Class-E load impedance as a function of multiplier order N for the Alpha AFM04P2 transistor. The switch capacitance is about 0.107 pF and the switching frequency is 10 GHz. For higher-order multipliers, the load impedance approaches zero and becomes difficult to match at the output. (b) Comparison of class-E load impedance with the conjugate match (class-A) required for high gain. Points closer to the center of the Smith chart indicate that the class-E load impedance and the class-A load impedance are similar, whereas points further away from the center indicate that the class-E impedance deviates from that required for high-gain operation.

of less than 4%. The parasitic resistance may change slightly with frequency due to the skin-effect, but this is not a significant effect. There is also the issue of the device gain being lower at the doubled frequency, which might lead to lower output power for the doubler than predicted by Eq. 7.26.

7.6.5 Gate Bias and Duty Cycle for Maximum Harmonic Generation For class-E doubler operation, the duty cycle is critical since the load impedance is calculated for a duty cycle of 0.25. For other duty cycles, the amplifier will not have class-E waveforms at the switch. The duty cycle of the transistor switch is determined by the gate bias, which determines the ON/OFF threshold, the RF input power, which does the switching, and the input reflection coefficient. A vague guess for the gate bias is the value which gives a current of approximately $I_{ds} = I_{max}/2.86$ based on DC I-V curves. This predicted gate bias is different when RF power is input to the transistor. The RF input power necessary to switch at a particular duty cycle is not known without the aid of large-signal simulations.

An approximate method is formulated here for determining the duty cycle of a switched-mode circuit for a given RF input, gate bias, pinch-off voltage, gate capacitance and approximate gate-source series resistance. This method assumes perfect RF isolation between the input and output of the transistor such that a sinusoidal voltage swing can be assumed across the gate source input capacitor. This is a reoasonable first-order approximation if proper harmonic terminations exist at the input to the transistor such that harmonic content is minimized.

Fig. 7.4 shows that the average power drawn from the source is dissipated in the input resistance Rs. Therefore, the current charging the input capacitor C_{gs} is

$$i_{in} = \sqrt{\frac{P_{in}(1 - s_{11}^2)}{R_s}} \tag{7.27}$$

where s_{11} is the input return loss of the multiplier. Therefore, the amplitude of the

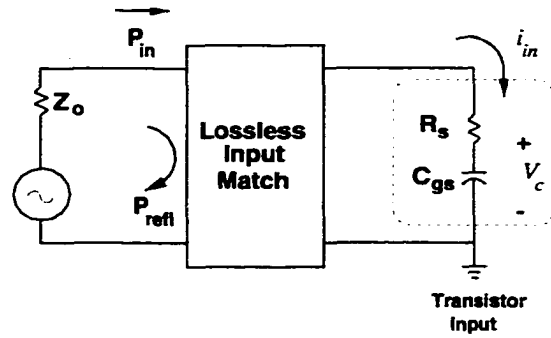


Figure 7.4. The switch and output circuit for the general class-E multiplier circuit. The transistor switch is represented as an ideal switch in parallel with a capacitance. L_o and C_o comprise an ideal tuned circuit, providing the transistor output with a load impedance $Z_{net} = R + jX$ at the output frequency, while presenting an open circuit to all higher harmonics.

sinusoidal voltage across the gate capacitor is

$$V_c = \frac{1}{\omega C_{gs}} \sqrt{\frac{P_{in}(1 - s_{11}^2)}{R_s}}. \tag{7.28}$$

The duty cycle of the switch voltage can be estimated as:

$$D = \frac{T_2}{T} = 0.5 - \frac{1}{\pi} \arcsin \frac{(V_{gs} - V_P)}{V_c} \tag{7.29}$$

where T_2 is defined in Chapter 2 in Fig. 2.5, and it is assumed that $V_{gs} > V_P$, which applies for duty cycles less than 0.5.

As a practical example, the manufacturer provides s-parameters for the Alpha AFM04P2 MESFET and the gate capacitance, $C_{gs} = 0.42\,\text{pF}$, is extracted using the method described earlier in Chapter 2. The gate resistance is typically about $2\,\Omega$ for microwave power transistors. From a nonlinear TOM3 model provided by Alpha Industries, the gate resistance for the AFM04P2 is found to be R_s=1.8 Ω. If a nonlinear model is not available, as is often the case, the total gate-source resistance is approximately $2\,\Omega$ for most microwave FETs [66]. (*Note:* The aforementioned TOM3 model could not be used successfully in the simulation of the circuits discussed here due to its inability to represent switched-mode operation.) The pinch-off voltage

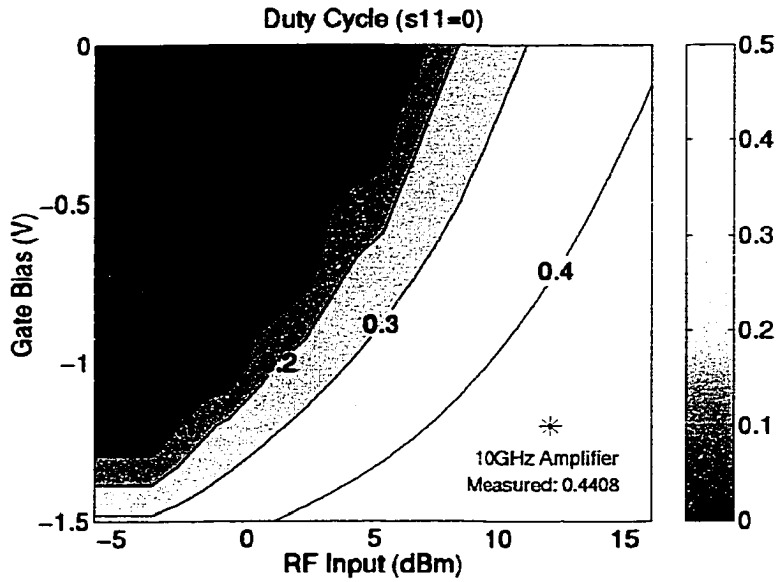


Figure 7.5. The calculated duty cycle as given by Eq. 7.29, assuming a perfect input match.

is V_P=-1.8 V. Therefore it is possible to find the duty cycle for different combinations of P_{in} and V_{gs}. The typical values range from 0.1 to 0.5, as shown in Fig. 7.5. For the 10 GHz class-E power amplifier of Ch. 5, the duty cycle calculated from measured gate bias and RF input power values is 0.4408 and is also shown in this figure. This agrees reasonably well with the expected duty cycle of 0.5 for class-E power amplifier operation.

7.7 Conclusion

In this chapter, class-E multiplier theory was presented, with the addition of two new contributions, one being the derivation of the maximum switching frequency for class-E operation, and the other being the first-order determination of the switching duty cycle.

The maximum switching frequency depends on the device current capability and output capacitance as well as on the drain bias voltage and the order of

multiplication. In this work, it is shown that when designing a frequency doubler, the maximum switching frequency is lower by a factor of N^2 compared to a class-E amplifier using the same device at the same drain voltage. This means that a device used for a 10 GHz suboptimal class-E amplifier factor of 2 above the maximum frequency for class-E amplifier operation cannot be used as a 10/20 GHz doubler that operates at the same degree of suboptimal behavior, *unless* the bias voltage is reduced by a factor of N^2.

The duty cycle of a switched-mode class-E amplifier is 50%, which in practice is accomplished by biasing the amplifier near pinch-off and driving it with a large RF input signal. For a class-E frequency doubler, however, the duty cycle is 25%, and the bias/drive points that give this duty cycle are not as obvious as for the case of the amplifier. Therefore, a simple model of the transistor input was used to estimate to first order, the duty cycle of an amplifier, based on knowledge of the gate bias, RF drive power, input gate capacitance and gate-source resistance. For most microwave MESFETs, the gate-source resistance is on the order of 2 Ω.

In the next chapter, the theory presented in this chapter is applied to the design of a 10/20 GHz class-E frequency doubler. By comparing this frequency doubler with the class-E amplifier of Chapter 5, the simplified class-E theory and the new contributions on the class-E critical frequency and the duty cycle calculations are verified.

CHAPTER 8

A CLASS-E X/K-BAND FREQUENCY DOUBLER WITH CONVERSION GAIN

8.1 Design

The class-E frequency multiplier theory presented in the earlier chapter is evaluated in this chapter by designing a 10/20 GHz class-E frequency doubler to compare with the 10 GHz class-E amplifier described in Chapter 5. 20 GHz is currently used for satellite communications, which is an area where high-efficiency circuits can be useful for making good use of limited resources and reducing system heat-sinking requirements.

An AFM04P2 medium power MESFET with 21 dBm output power capability is used as the switch for a 10/20 GHz frequency doubler. The small signal circuit model shown in Fig. 8.2 is extracted from modified s-parameters after de-embedding a bond-wire inductance of 0.1 nH. These intrinsic s-parameters are then used to obtain y-parameters from which the component values are obtained as described in Chapter 2. The 0.1 nH value was obtained by calculating the parallel inductance of two bond wires, where the inductance of each wire was found from a two-wire line model (equivalent to a single bond wire reflected in a ground plane). This is shown in Fig. 8.1. The equation for calculating the bond wire inductance is

$$L_{bond} = 2 \ln \left(\frac{4h}{d} \right) \quad \text{nH cm}^{-1} \tag{8.1}$$

where h, d, and l are shown in Fig. 8.1.

The required load impedance for a class-E doubler with a switching frequency of 10 GHz is obtained from Eq. 7.27 and the component values in Fig. 8.2.

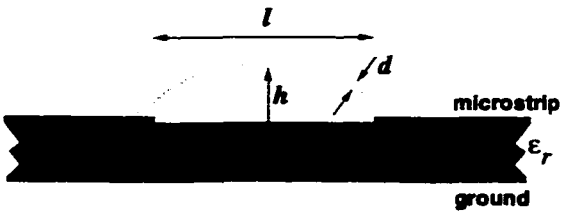


Figure 8.1. Schematic diagram of a bond-wire on microstrip lines. The bond-wire inductance is calculated using Eq. 8.1 by reflecting the bond-wire in the ground plane.

$Z_{net} = 7.09 + j8.17\Omega$ is the desired load impedance at 20 GHz. This value is then optimized on HP ADS such that the small-signal gain of the doubler and the fundamental rejection are maximized, while the output mismatch of the class-E amplifier is minimized for high conversion gain. This necessitates a compromise between the ideal class-E match and an ideal output match to $50\,\Omega$. The final value of the load impedance at 20 GHz is $Z_{load} = 13.65 + j15.74\Omega$, and the output mismatch is $s_{22} = -6\,\text{dB}$. This load impedance was chosen since it maintains the load angle required for class-E operation. The magnitude of the impedance is higher than the ideal doubler class-E impedance.

The microstrip circuit was fabricated on Rogers TMM10 with a dielectric constant of 9.2 and a thickness of 0.381 mm. An LPKF milling machine was used to mill the circuit shown schematically in Fig. 8.3. A hole milled in the dielectric

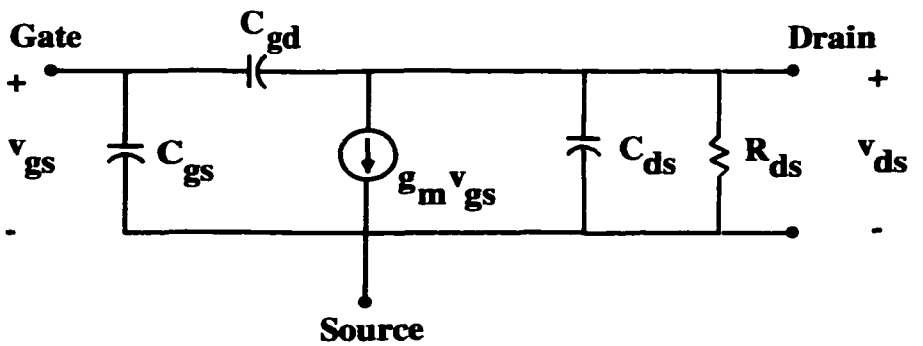


Figure 8.2. MESFET small signal circuit model used to extract the output capacitance of the transistor switch.

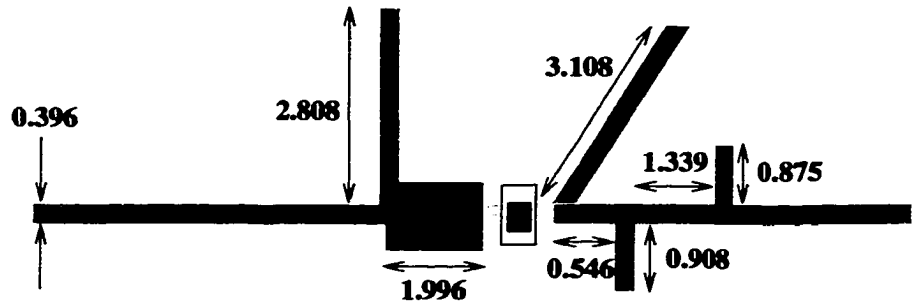


Figure 8.3. Outline of the fabricated 10.4/20.8 GHz multiplier circuit. The dimensions are in millimeters, and the substrate is 0.381 mm in height, with ϵ_r=9.2.

allows room for a platform upon which the transistor is epoxied. A separate ground plane is epoxied onto the dielectric ground plane for the transistor platform to be mounted. Due to the difficulty in finding or constructing a sufficiently small metal platform, one is constructed using shorted chip resistors which are comparable to the size of the transistor.

The microstrip lines are wire-bonded to CPW/microstrip transitions (obtained from JMicroTechnology, Inc.). These transitions made it possible to perform the measurements on a Cascade 9000 Probe Station since soldering connectors to the circuit would put too much torque on the circuit edges, causing the brittle substrate to break.

8.2 Small-Signal Measurements

The measured and simulated s-parameters for this circuit are shown in Fig. 8.4. The simulations were originally carried out for an input match at 10 GHz and class-E operation at the output at 20 GHz. However, since the measured input match is at 10.4 GHz, the simulations were modified to include a 0.075 mm overetch of the lines during the milling of the circuit. This overetch results in the simulated results of Fig. 8.4, which match the measurment reasonably well.

These s-parameter measurements are relative to microstrip calibration standards built using the CPW/microstrip transitions. Simulations were carried out on HP ADS, assuming ideal transmission lines without T-junction or open stub models since prior experience has shown that this gives better agreement with measured data. For fabrication, the open stubs are corrected according to [67] by adding 0.362 mm, to account for the shortening effect due to the T-junctions and the lengthening effect due to the open end.

The simulated class-E/A performance at 20.8 GHz is shown in Fig. 8.5 to verify that the frequency shift will not degrade the doubler performance significantly.

8.3 Large-Signal Measurements

8.3.1 Measurement Setup An HP70820A Microwave Transition Analyzer was used to measure the power and efficiency performance of the frequency doubler as a function of input power, drain voltage and gate voltage. The quantities measured are listed below.

(1) Output power at 10.4, 20.8, and 31.2 GHz

(2) Reflected power at 10.4, 20.8 GHz

(3) DC drain voltage and current, gate voltage

The output power at the various harmonics is used to quantify harmonic rejection and output power at the doubled frequency, while the reflected power indicates the input match at the fundamental as well as the amount of second harmonic power wasted by reflection towards the input. Efficiency is calculated from the output power and DC power. Output power at 41.6 GHz was not measured since the gain at this frequency is very low.

8.3.2 DC Bias and RF Input Power These data are taken at several drain and gate biases in order to verify the trends predicted by the class-E theory presented in Sec. 7.6.1. From Eq. 7.20, the predicted drain bias is 0.6 V,

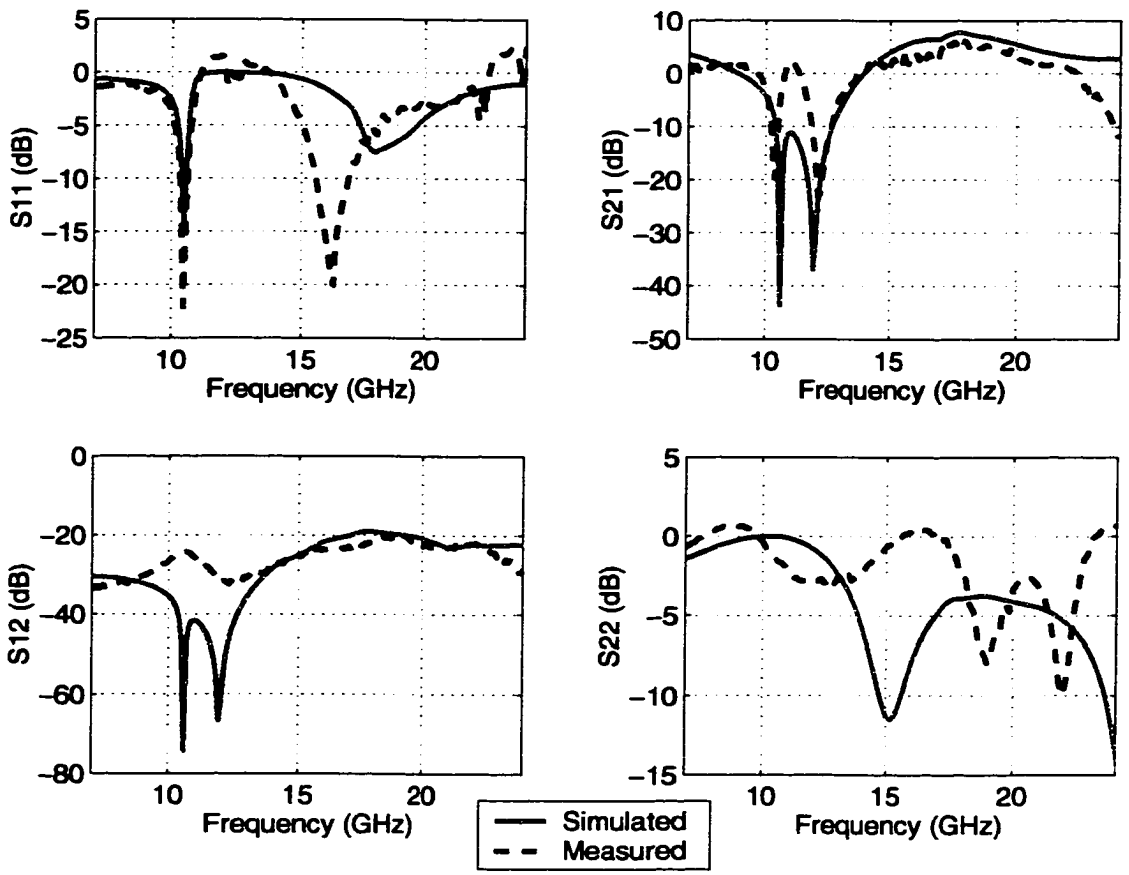


Figure 8.4. Measured vs. simulated s-parameters for the X/K-band frequency doubler. The simulations were carried out on HP ADS. A line overetch of 0.075 mm is used in the simulations to account for the 4% upward shift in input match frequency from the design of 10 GHz to the measured 10.4 GHz.

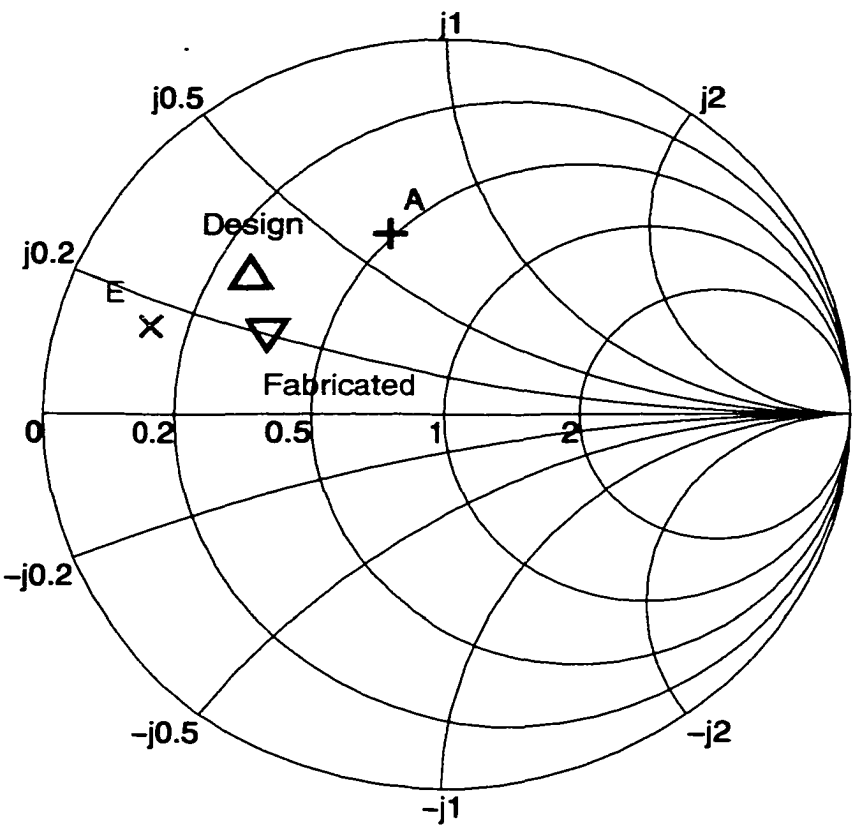


Figure 8.5. Load impedance of the fabricated circuit at 20.8 GHz compared to the ideal class-E and class-A doubler load impedances. As seen in this figure, the fabricated multiplier is close to the design point and operates somewhere between these two classes.

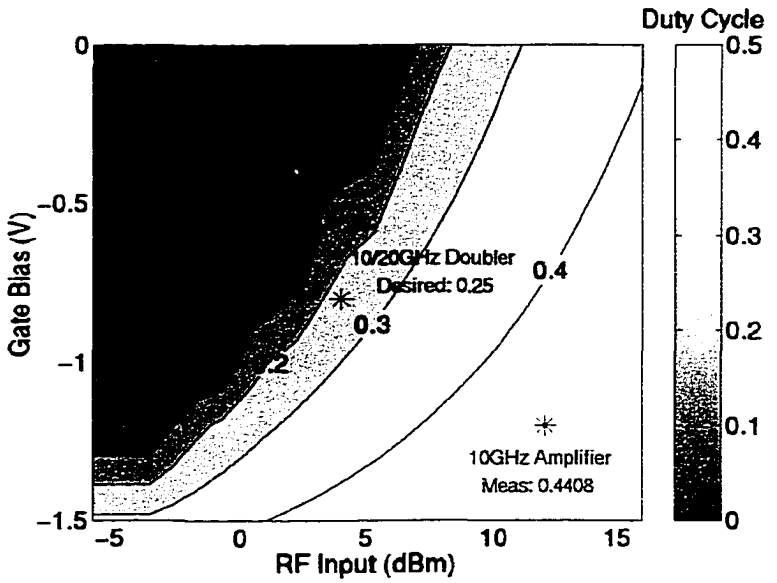
while the drain current is about 40 mA. From DC current-voltage measurements this combination of DC drain voltage and current corresponds to an initial guess for gate voltage of about -0.8 V. This vague estimate of the required gate bias will change once RF input power is applied. Since the knee voltage is about 1 V, drain voltages below this were not used in the measurements. The drain voltages used were V_{ds}=0,1,2,..5 V, and the gate voltages were V_{gs}=0,-0.2,-0.7,-1,-1.2, and -1.5 V. The pinch-off voltage of the device is about -1.8 V. At each bias point, the RF input power was varied from -6 to 17 dBm.

The various combinations of gate bias and RF input power are used to test the doubler at different duty cycles whereas the different drain bias points are used to verify Eq. 7.31 to compare the drain bias point of a class-E doubler to that of a class-E amplifier at the same switching frequency.

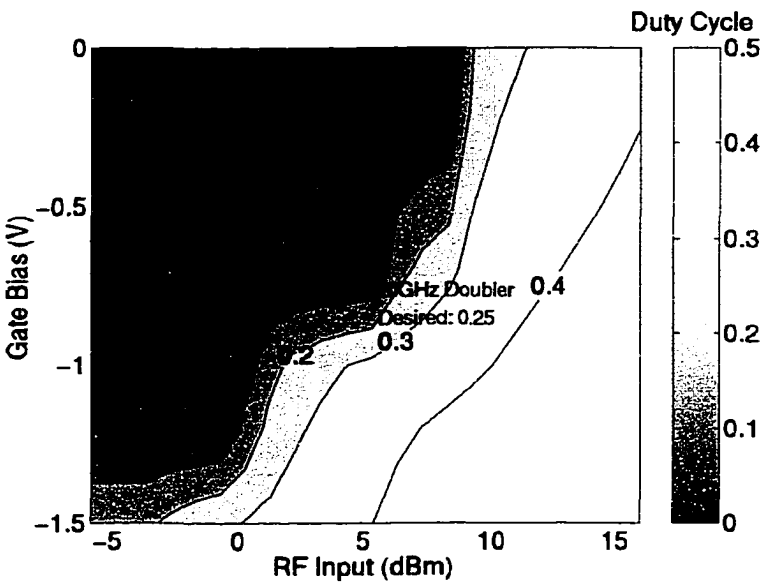
8.4 Measured Performance at Different Duty Cycles

The duty cycle is calculated from Eq. 7.31 for different combinations of gate bias and RF input power and is shown in Fig. 8.6. The input match or return loss, s_{11}, is measured at each bias/drive point and used in the calculation. The drain voltage is 1 V. For higher drain voltages, this plot changes since the reflection coefficient is different. Fig. 8.6 shows the effect of input match on duty cycle. The bias/drive point for 25% switching duty cycle, predicted assuming a perfect input match, is not consistent with that duty cycle once the actual input match is taken into account.

The performance of the doubler is plotted in contour format in Figs. 8.7 and 8.8 for the different gate bias and RF input power combinations which specify duty cycle. The shaded areas in these contour graphs are duty cycle, while the black contour lines correspond to power, conversion gain, or efficiency. The drive/bias combination predicted assuming a perfect input match and the DC operating point,



(a)



(b)

Figure 8.6. The calculated duty cycle as given by Eq. 7.31 for (a) a perfect input match, and (b) the measured input match. The blue star is the expected approximate operating point based on DC properties and a perfect input match assumption.

is shown as a blue star for comparison.

The output power in Fig. 8.7(a) increases with input power, with a maximum of about 7 dBm for an input power of about 10 dBm. For higher input powers, the output power decreases as the second harmonic generation is reduced. The conversion gain is shown in the contours of Fig. 8.7(b). As can be seen from this plot, a maximum conversion gain of over 5 dB can be obtained for low input powers and -1 V gate voltage.

The drain efficiency is shown in the contours of Fig. 8.8(a) As can be seen from this plot, the drain efficiency is as high as 50% for certain duty cycles. Fig. 8.8(b) shows the overall efficiency contours with a maximum of over 30%.

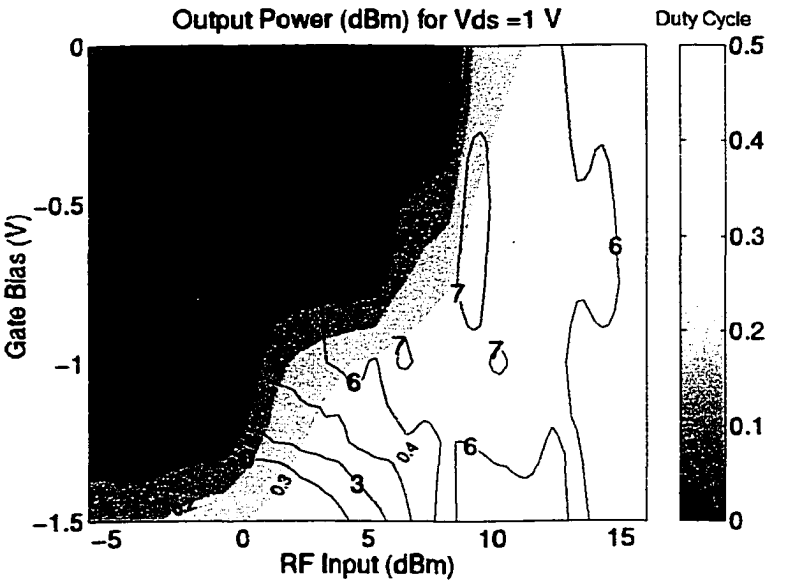
From Figs. 8.7 and 8.8 it is clear that a gate bias of -1 V gives higher output power, efficiency and conversion gain, albeit at different RF input power levels. By plotting similar data at higher drain voltages, it is seen that increasing the drain bias has no effect in producing higher performance. Fig. 8.9 shows that there is a remarkable decrease in performance for higher drain voltages. This is consistent with Eq. 7.20 which predicts a drain voltage of about 0.6 V for the class-E doubler.

As seen in Fig. 8.9, a drain voltage of 1 V provides the highest efficiency and power. Fig. 8.9(a) depicts the variation of drain efficiency with drain voltage and RF input power. There is clearly a higher efficiency for a drain voltage of 1 V. Fig. 8.9(b) shows the output power at 20.8 GHz with a maximum output power of 7.1 dBm; increasing drain voltage does not produce increased output power.

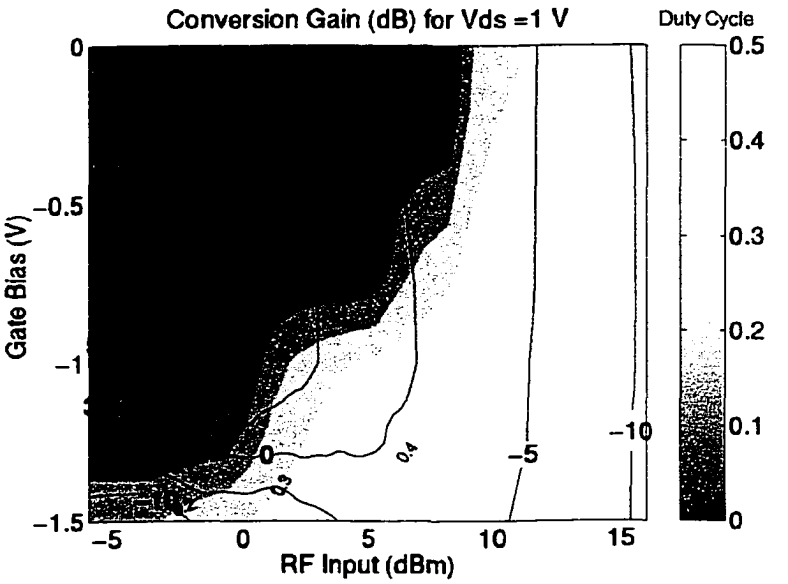
8.5 Optimum Measured Performance

The doubler performance can be optimized for drain efficiency, overall efficiency, output power, or conversion gain. The following is a list of optimum points based on Figs. 8.7 and 8.8.

Since the optimum points occur mostly at V_{ds}=1 V, and V_{gs}=-1 V, the power

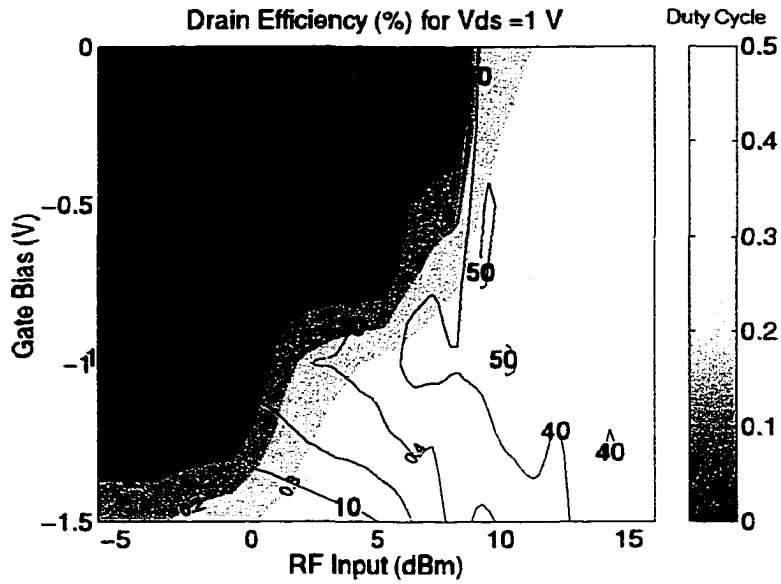


(a)

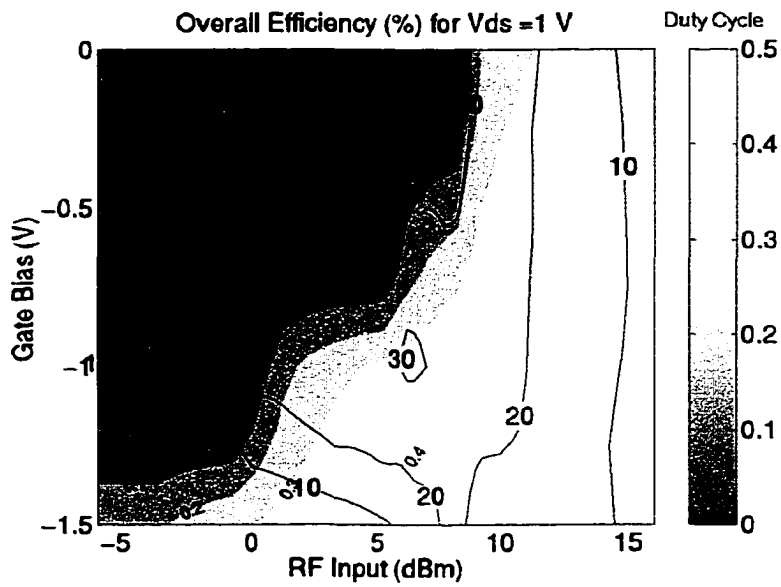


(b)

Figure 8.7. Measured output power (a) and conversion gain (b) contours of the 20.8 GHz doubler vs. duty cycle, shown by the shaded areas. The blue star is the expected approximate operating point based on DC properties and a perfect input match assumption.

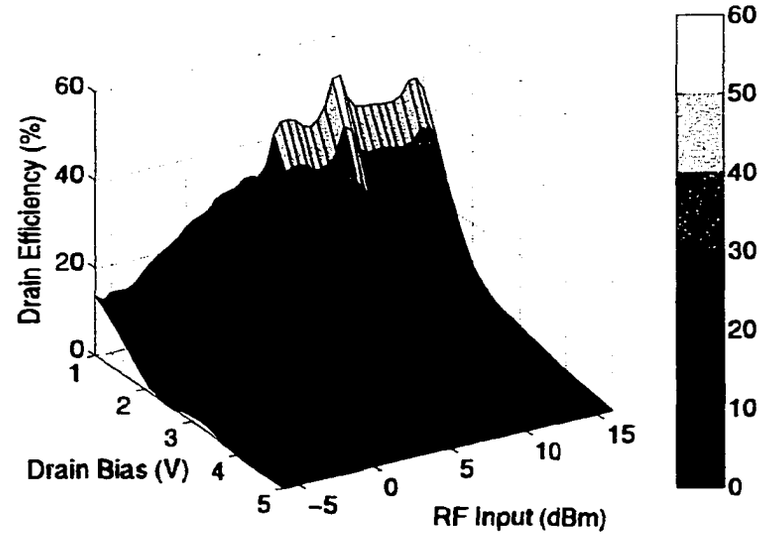


(a)

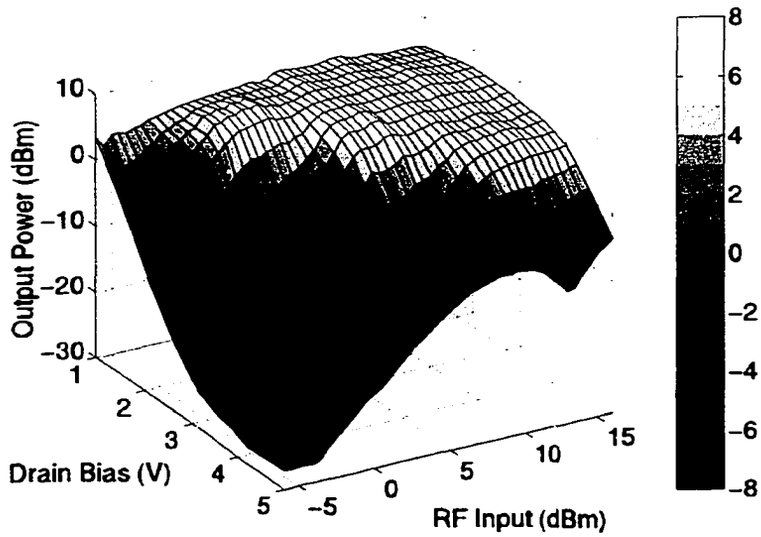


(b)

Figure 8.8. Measured drain (a) and overall (b) efficiency contours of 20.8 GHz doubler. The blue star is the expected approximate operating point based on DC properties and a perfect input match assumption.



(a)



(b)

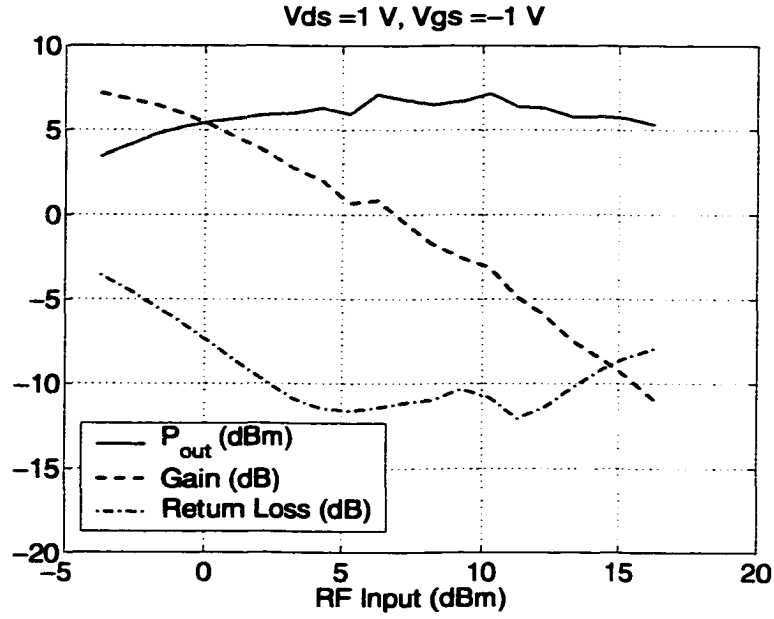
Figure 8.9. Measured drain efficiency (a) and output power (b) of the 20.8 GHz doubler vs. drain bias and RF input power for V_{gs}=1 V. The efficiency is highest for V_{ds}=1 V, and there is no significant increase in output power as the drain voltage is increased.

Table 8.1. Optimum Operating Points and Performance of the 10.4/20.8 GHz Doubler. η_D is the drain efficiency and η is the overall efficiency. For the duty cycle calculations, V_P=-1.8 V and R_S=1.8 Ω, and C_{gs} = 0.42 pF.

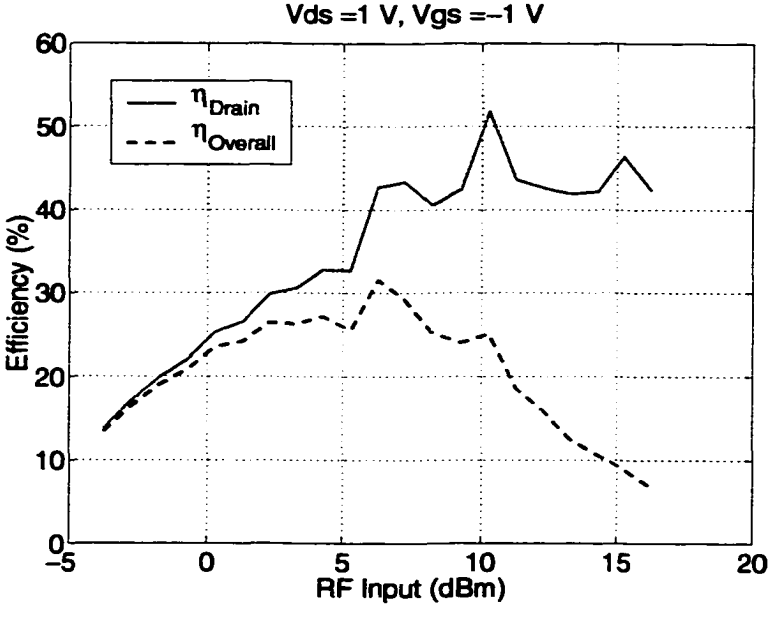
Property	Optimized Property			
	P_{out} and η_D	G	η	G and η
V_{ds} (V)	1	1	1	1
V_{gs} (V)	-0.7	-1	-1	-1
P_{in} (dBm)	9.265	-3.735	6.265	0.265
s_{11} (dB)	-7.4	-3.56	-11.46	-7.68
Duty Cycle	0.3380	-	0.3443	0.04
P_{out}(dBm)	7.495	3.445	7.095	5.495
Gain (dB)	-1.77	7.18	0.83	5.23
η_D (%)	51	13.8	42.7	25.3
η (%)	28.9	13.5	31.6	23.5

sweeps for this bias point are presented in Fig. 8.10. The Data presented in this figure include output power, return loss, conversion gain, drain efficiency, and overall efficiency. As can be seen in Table. 8.1, the optimum conversion gain occurs for a regime in which the device is not in switched-mode, evidenced by a complex duty cycle. Therefore, device nonlinearities other than switching are the sources of harmonic generation for maximum conversion gain. A gain of 5.23 dB can be obtained with efficiencies of about 25% and about 5.5 dBm output power. The duty cycle for this case is 0.04, indicating that mechanisms other than switching are causing the harmonic generation for this data point. However, for both optimum efficiency (η_D and η) points, the duty cycle is 0.34, meaning that switching is taking place. Since this value is different from the desired value of 0.25, it may imply a class of operation between class-E and saturation class-A which has a duty cycle of 0.5. On the other hand, it may imply that the duty cycle calculation must be modified to include effects such as reflection of harmonics to the input.

The harmonic rejection of the class-E doubler at V_{gs}=-1 V, V_{ds}=1 V is shown in Fig. 8.11 as the input RF power varies.



(a)



(b)

Figure 8.10. Measured output power and conversion gain, (a) and drain and overall efficiency (b) of the 20.8 GHz doubler as a function of input RF power. The bias point is V_{ds}=1 V, and V_{gs}=–1 V.

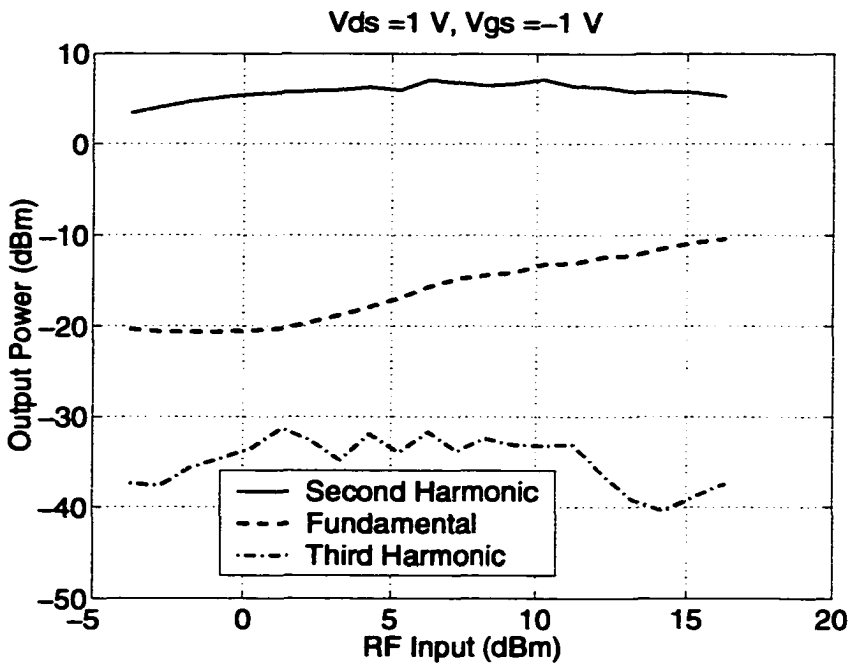


Figure 8.11. Measured harmonic rejection of the 20.8 GHz doubler vs. RF input power for V_{ds}=1 V and V_{gs}=-1 V.

8.6 Reflection of Harmonic Power Towards The Input

When calculating the switching duty cycle as presented in Chapter 7, a sinusoidal voltage swing across the input capacitor was assumed for simplicity of analysis. However, in reality, harmonics generated at the output of the transistor are reflected back to the input through the feedback capacitor C_{gd}. The reflected second harmonic component was measured at the input as shown in the experimental setup of Fig. 3.2 in order to quantify the effect of this feedback capacitor. No harmonic tuning was used at the input of the multiplier so that this effect could be measured. In practical multipliers, a shorted or open stub would be used at the input to supress this feedback.

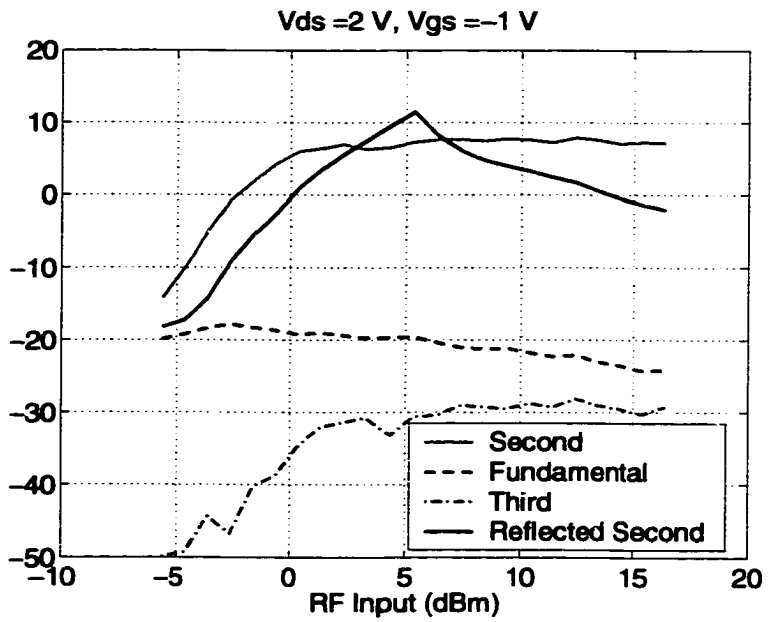
The measurements were carried out at V_{ds}=2 V due to equipment failure. (*Note:* Uncalibrated measurements made later at V_{ds}=1 V show the same type of behavior, but are not presented here.) However, the conclusions drawn from these

measurements also apply at the optimum drain bias of V_{ds}=1 V also. The reflected power is shown in Fig. 8.12 together with the output power. Also shown are the efficiencies corresponding to the different power levels.

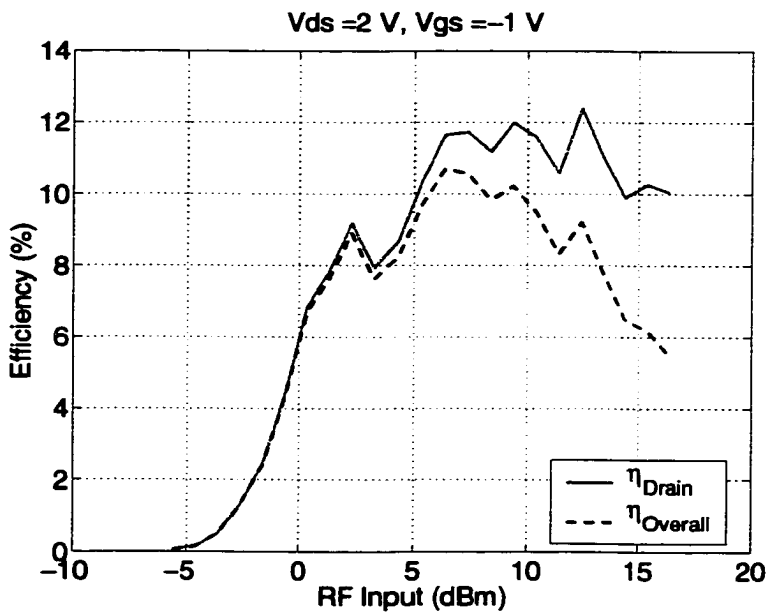
This reflected power data shows that there is a considerable second harmonic content at the input at the point of maximum overall efficiency, which occurs at an input power of 6.4 dBm. The second harmonic power at the input is 8.2 dBm. Therefore, the voltage across the input capacitor cannot be assumed to be sinusoidal and the duty cycle calculation must be updated to account for a second harmonic component. Unlike the simple fundamental-frequency analysis presented in section 7.6.5, this second harmonic analysis needs to include a time-domain analysis since the duty cycle depends on the time-domain voltage swing at the transistor input. By utilizing adequate input harmonic filtering, better agreement between the calculation and measurement can be expected.

8.7 Comparison with 10 GHz Class-E Amplifier

The 10 GHz class-E amplifier to which the doubler is compared, is the active integrated antenna described in Chapter 5. For this amplifier, theory dictates a class-E amplifier drain bias of V_{ds}=2.4 V, I_{ds}=42-52 mA for a device with no switch resistance or other parasitic losses. The pinch-off voltage of the Alpha AFM04P2 MESFET used for this amplifier is -1.8 V. The fabricated amplifier is is biased at V_{ds}=4 V, I_{ds}=35 mA, V_{gs}=-1.2 V and requires 12 dBm input power for an optimal PAE of 62%. The input reflection coefficient is approximately -15 dBm. According to the method devoloped in Ch. 7, a duty cycle of 0.4408 is calculated from these measured values, which agrees moderately well with the desired value of 0.5, but demonstrates the need for a more accurate calculation the duty cycle, including more accurate values of gate-source capacitance and input resistance. The DC resistance across the drain-source terminal is measured to be about 4.5Ω. This is partially



(a)



(b)

Figure 8.12. Measured output and reflected power (a) and drain and overall efficiency (b) of the 20.8 GHz doubler as a function of input RF power. The bias point is V_{ds}=2 V, and V_{gs}=-1 V.

responsible for the need for a larger drain voltage than the theoretical prediction.

Based on the class-E theory in the previous chapter, the expected bias point of the frequency doubler is about V_{ds}=0.6 V and I_{ds}=42-52 mA, indicating a rough estimate for gate bias, V_{gs} ≈-0.8 V, based on measured transistor DC I-V curves. The measured bias-point data at the point of optimal overall efficiency are V_{ds}=1 V, I_{ds}=10 mA, V_{gs}=-1 V while the RF input power is 6.265 dBm. The drain and gate voltages are quite close to the expected values, but the drain current is suprisingly low. This is found to be partly due to the measured DC characteristics of the device which has low current values for V_{gs} <-0.7 V, and partly because the drain voltage is near the knee region. The duty cycle at the optimal efficiency point is 0.3443, which agrees moderately well with the required value of 0.25, but indicates that refinement of the duty cycle calculation is warranted. It is also probable that the doubler performs in a hybrid class-E/A mode.

The output power of the doubler, when operating with optimal overall efficiency, is 7.1 dBm, which is approximately 12.9 dB lower than the 20 dBm output power of the 10 GHz class-E amplifier. Theoretically, an ideal class-E doubler produces 6 dB less power than an ideal class-E amplifier with the same device and same switching frequency. In these experimental results however, the doubler output is lower by an additional 6.1 dB. This is partly due to a significant amount (approximately 3 dB) of harmonic power being reflected back to the input via internal feedback. Additional losses could be due to lower gain at 20.8 GHz and the fact that the output matching is not an ideal class-E but a hybrid class-E/A design.

8.8 Discussion

We have shown that class-E multiplier design can be extended to K-band with commercial transistors to obtain high DC-RF (42.7%) and overall (31.6%) efficiency with 0.83 dB conversion gain. 5.23 dB conversion gain and 5.5 dBm output

power can be obtained at a decreased 23.5% overall efficiency.

Therefore, class-E doublers are a more power efficient alternative to diode doublers which exhibit conversion loss. Class-E doublers also provide higher efficiency than other transistor doublers.

Specifically the following conclusions can be drawn from this work:

(1) In order to operate at the same level of suboptimum class-E behavior, doublers must be biased at lower drain voltages than class-E amplifiers using the same device.

(2) As the order of the multiplier increases (e.g. tripler) the output match deteriorates, limiting the conversion gain.

(3) The gate bias of the doubler must be set carefuly in order to operate with approximately 0.25 duty cycle. This is the only duty cycle at which the class-E waveforms can be obtained with the impedance given in Eq. 7.27. Therefore, it is useful to have a method of estimating duty cycle at a particular combination of gate bias and RF input power.

(4) The duty cycle can be approximately estimated by analyzing the input circuit at a particular RF input power and gate bias, and assuming a sinusoidal voltage swing across the input capacitor.

(5) No second harmonic tuning was applied at the input. A significant amount of reflected second harmonic power was measured, causing the gate voltage swing to deviate from a sinusoidal shape. This demonstrates the need for input harmonic tuning. If input harmonic tuning is used to limit harmonic reflections, then the approximate method of calculating duty cycle can be used to estimate the gate bias and RF input power.

(6) Measurements indicate that approximately half the generated harmonic power is reflected towards the input. The conversion gain and efficiency of the multiplier could be improved significantly if proper harmonic filtering is used.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

9.1 Summary and Conclusions

The main thrust of the work presented in this thesis has been to push low-frequency switched-mode power amplifier design towards the millimeter-wave region of the spectrum. Past work on class-E and F transmission-line microwave power amplifiers has shown that high power efficiencies can be obtained at frequencies upto 5 GHz. By designing and building class-E and F amplifiers at 8 GHz, and 10 GHz, this work demonstrates that this power amplifier architecture is applicable for high-efficiency applications at X-band, at frequencies up to four times the maximum frequency for class-E operation.

Time-domain waveforms measured at 8 GHz using a novel optical sampling technique were used to verify class-E and F operation of microwave power amplifiers. These measurements, presented in Chapter 3, substatiate the approximate design procedures used due to lack of suitable large signal models. These time-domain measurements demonstrate the suboptimal behavior of the circuits since the class-E and F waveforms have nonideal switching duty cycles. The technique of measuring waveforms in nonlinear microwave circuits proves to be very useful in the better understanding of switch mode operation at microwave frequencies.

In order to increase the total output power of class-E and F high-efficiency power amplifiers, Chapter 4 considers methods of combining the power of several

units. Spatial combining provides a more efficient method of combining large numbers of units, while circuit combining is a lower-loss method for small numbers. Spatial combining requires the outputs of all amplifier elements to be radiated into free space, where they coherently combine to give high output power.

The 10 GHz novel active integrated antenna presented in Chapter 5 is well-suited to spatial power-combining of high-efficiency power amplifies. The novel antenna performed class-E amplification as well as radiating with about 2 dB directivity. The size of an array unit cell using this active antenna is about half the size of a conventional amplifier integrated with a 50 Ω antenna. The concept of designing antennas designed to have the class-E load impedance is especially useful for cases when the class-E impedance causes output mismatches that limit the power available from the output of the power amplifier. This active antenna has a power output of 100 mW, a compressed gain of 8 dB, a drain efficiency of 74%, and a power-added efficiency of 62%.

High-efficiency power amplifiers are limited in their usefulness if the signal distortion due to their inherent nonlinearities are is not remedied. The work presented in this Chapter 6 is an experimental study of different methods of linearizing an 8.4 GHz class-F switched-mode amplifier by controling the relationship between the drain bias and the RF input signal amplitude. Five different methods which have been previously demonstrated in the literature at various frequencies and with different devices, are compared with each other using a single power amplifier. This allows the direct comparison of the effectiveness of each method with regards to both efficiency and signal distortion. It was shown that simultaneously varying the drain bias and the input signal amplitude results in higher efficiency and linearity than if one or the other is kept constant. Also, the proportional variation of the two voltages while the device is kept in constant saturation is seen to perform with higher efficiency and linearity than when the device is never allowed to saturate. In conclusion,

proportionally varying the drain bias and the input signal amplitude of the class-F power amplifier resulted in 44% average efficiency for multicarrier signals, while the spectral distortion was 28 dB below the desired frequency components. For the unlinearized amplifier, the average efficiency was 10% and the distortion was 17 dB below the desired frequency.

In the quest to build high-efficiency circuits at K-band and higher, a class-E frequency doubler was built, as described in Chapters 7 and 8, with the same device as that used for the 10 GHz active antenna. A 20.8 GHz power output of over 5 mW, a drain efficiency of 42%, and a conversion gain of 0.83 dB was obtained The input signal is 10.4 GHz, and therefore the circuit operates at a reduced drain voltage, at the same degree of suboptimal behavior as the 10 GHz active antenna. An approximate method of determining the duty cycle of the switch based on gate bias, RF input power, and input reflection coefficient, was formulated. In the absence of large signal models for the device, this method is very useful in estimating the necessary gate bias for class-E multiplier operation. This method predicted a duty cycle of 0.3443 at the optimal bias point where the overall efficiency of the doubler was maximized; the theoretical duty cycle for class-E performance is 0.25. When the same method was applied to calculate the duty cycle of the 10 GHz class-E active antenna, a value of 0.4408 was obtained, which supports the applicability of the approximate first-order method. Measurements of reflected second harmonic power at the doubler input show that there may be a significant second harmonic component in the gate voltage swing. Therefore, the duty cycle calculation must be modified to include harmonic content.

9.2 Suggestions for Future Work

9.2.1 Push the Limits of Suboptimal Class-E Behavior Since this work has shown reasonably high efficiency at frequencies upto 4-times the critical

frequency for class-E operation, it is necessary to pursue the task of taking class-E operation into the millimeterwave region. For example, the Alpha AFM04P2 MESFET used for the 10 GHz active antenna and the 10.4/20.8 GHz frequency doubler has a class-E critical frequency of about 6 GHz when used at a drain voltage of 4 V in an amplifier configuration. This would imply that it is possible to obtain good amplifier performance from this device upto 4-times this critical frequency, at 24 GHz.

9.2.2 Study of Switched-Mode Amplifier Input Circuit and Duty Cycle The waveforms from this circuit should be measured using the time-domain optical techniques since both circuits measured in this thesis were packaged devices. The Alpha AFM04P2 MESFET is a chip, and therefore it may be possible to perform the optical probing on the gate and drain pads themselves, which would help immensely to study not only the switch waveforms at the drain, but also the switching waveform at the gate.

The study of switching duty cycle should be extended to include harmonic content at the gate. This may be carried out by including a harmonic generator across the gate resistance and capacitance which contributes various harmonic voltages to the gate voltage swing. A time-domain analysis is necessary to determine the duty cycle.

9.2.3 Power Combining A class-E frequency doubler antenna-array could be built to show the spatial power combing properties of switched-mode circuits at K-band. At lower frequencies, the large size of the arrays cause problems due to nonuniform amplitude distribution across the array. This causes the array elements to be saturated at different levels, with different efficiences, output powers, and output phases. All these factors limit the output power and power combining efficiency of the array. At K-band, the array size will be smaller and therefore the feed nonuniformities across the array will be less.

A first-order design for the frequency doubler unit-cell is shown in Fig. 9.1. The receive-side unit cell has a 10 GHz patch antenna which, in addition to being a receive element, also performs the function of a 4-way power divider if the antenna feeds are positioned properly on the nonradiating edges. Four vias guide the power through the substrate to the transmit side of the array where four doubler unit cells generate the doubled frequency and transmit using patch antennas designed to directly provide the class-E load impedance to the devices at the second harmonic. This will avoid problems with output mismatch in the doubler circuits.

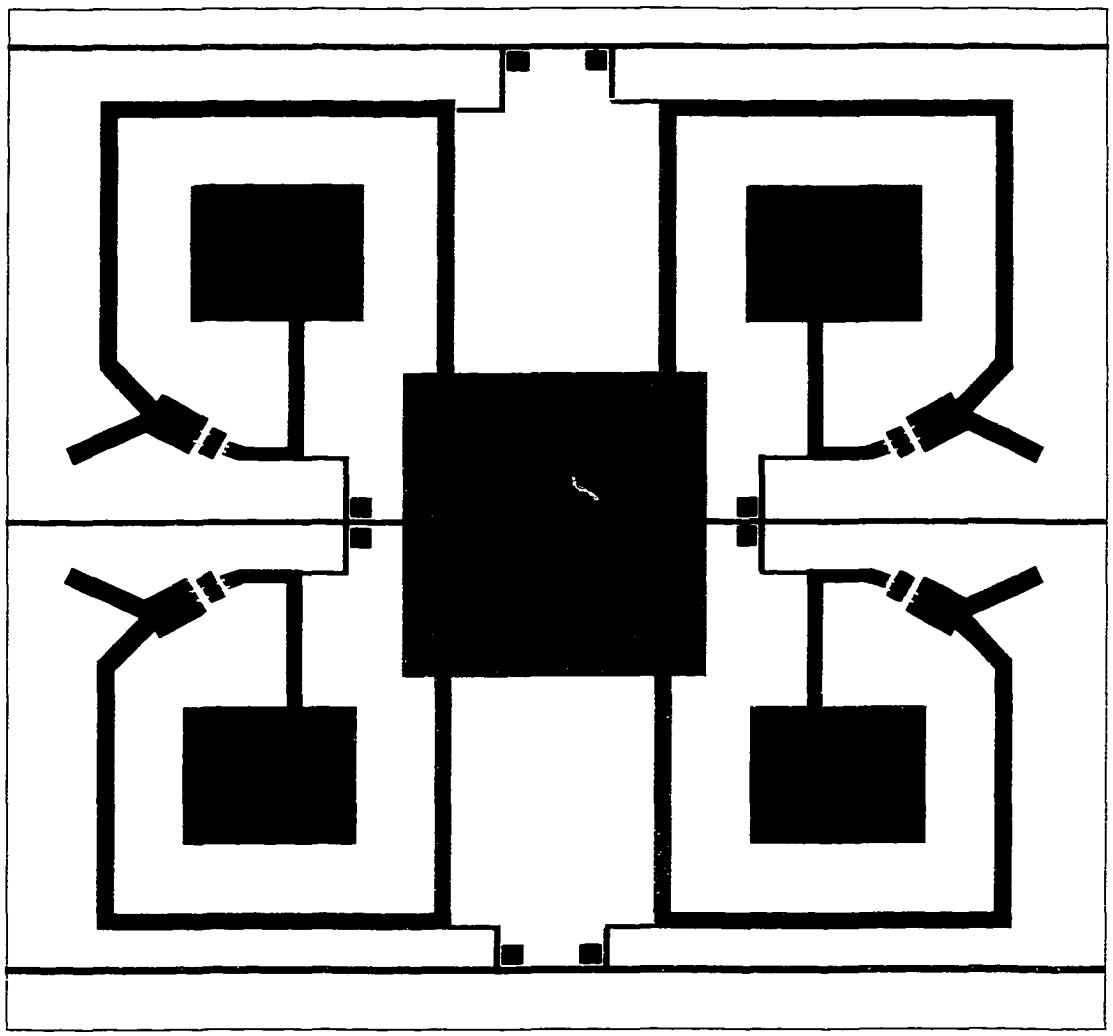


Figure 9.1: Proposed design concept for a class-E frequency doubler array.

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