X-band Class-E Power Amplifiers with Dynamic Bias Control

by

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Thesis directed by Prof. Zoya Popović

Multifunctional RF front ends need to transmit signals with varying peak-to-average ratios requiring high linearity which often implies low efficiency. This thesis studies high-efficiency class-E microwave power amplifiers as a potential candidate for linear amplification. Most part of this work is based on a class-E PA designed at 10 GHz with output power of 20.3 dBm(0.7 dB less than the specified maximum output power) and drain efficiency of 67 %.

Generally, a class-E PA is designed to operate in the saturated (nonlinear) regime and does not maintain high efficiency at lower input power levels. To enable class-E amplification of signals with varying envelopes, the idea of dynamic control of the bias supply is brought up. A coupler and detector at the output of the PA provide a feedback signal to the drain bias controller based on an efficient DC-DC converter. The feedback signal is compared with a reference voltage and the drain bias is varied to obtain the desired output power. When compared with a PA with constant drain bias, the average efficiency of the PA with dynamic biasing is improved by a factor of 1.4 over an output power between 15 and 20 dBm.

The linear relationship between the drain bias and output signal amplitude of a class-E PA enables linearization using the Envelope Elimination and Restoration (EER) technique. In this thesis, linearity characterization of X-band class-E power amplifiers using different technologies operating in EER mode is discussed. The PA is characterized in terms of its AM-AM, AM-PM conversion and two-tone intermodulation products in the context of EER mode of operation. Measurements of intermodulation distortion are compared with harmonic balance simulations using a TOM model provided by the device

manufacturer. It is shown experimentally and through simulations that the amplifier in EER mode has improved linearity while maintaining high-efficiency operation. To achieve better linearity, a lookup-table based baseband open-loop digital predistortion is proposed and carried out at two-tone frequency spacing of 20 KHz, 200 KHz, 625 KHz and 1 MHz.

The last part of the thesis is investigation of class-E amplifier driven phased array for efficiency and increased functionality. Side lobe control and scanning of the array is accomplished by dynamically biasing the class-E PAs. The study is based on a 11-element 1-dimensional rectangular patch antenna array. AM-AM, AM-PM effect on side-lobe control and effect of scan reflection coefficients on PA behavior is studied.

Future work relating to the linearity of class-E PAs includes: 1) incorporation of adaptive feedback loop in the baseband predistortion to further linearize the PA; 2) correction for memory effects in the predistortion; 3) limitation of the feedthrough voltage by controlling the driver stage. Future work concerning active antenna arrays are realization of the active antenna array and testing of its steering, side lobe control and optimization.

Dedication

To my Alusiin Gobi.

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Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Introduction

1.1 Introduction

Modern wireless communication systems demand increasingly more power conservation and channel capacity. As a consequence, higher efficiency and linearity are expected from power amplifiers (PA). In this work, class-E power amplifiers are studied for potential applications in multifunctional RF front ends [3]. The class-E mode of operation, first proposed by Ewing [4] in 1964 and later by Artym [5] and Sokal [6], has ignited research interest due to its high efficiency and simple circuitry. Raab [7] analytically solved the class-E circuit and derived the load impedance required for optimal operation. Later Kazimierczuk et.al. [8] analyzed the class-E circuit with different load Q factors and duty cycle of the device switching. Publications have shown that class-E PAs can achieve 96.5 % drain efficiency at VHF (145 MHz), 79 % at UHF and up to 74 % at X-band [9]. Negra et al. designed a Ka-band MMIC class-E PA in GaAs pHEMT technology and achieve 56.2 % drain efficiency[10, 11].

In a PA, the largest contribution to loss is the power dissipated in the transistor. In class-E mode of operation, the active device acts as a switch driven into saturation. The waveforms of voltage and current through the device won't overlap in time domain and hence there is no power dissipation. Furthermore, in class-E mode, the load network is designed so that the voltage across the device reaches zero with zero slope when the device is turned on. Sometimes referred to as "soft switching", this makes the PA

more tolerant to circuit variations and device transition time. The specific output load impedance value is derived by Raab [7] and it is inversely proportional to the operating frequency and output parallel capacitance. Another advantage of the class-E PA is that the output capacitance of the device becomes part of the parallel capacitor required for class-E operation and does not contribute to additional parasitic loss. It is mentioned by Sokal [9] that the power losses in a class-E PA are about 2.3 times lower than the loss in conventional class-B PA with same output power, frequency and transistor.

Mader et al. [12, 13] extended class-E concept to microstrip circuits at microwave frequencies. Class-E PAs were designed at 500 MHz with drain efficiency of 85 % and PAE of 80 % [12] and up to 5 GHz with drain efficiency of 81 % and PAE of 72 % [14]. The class-E operation is confirmed with time-domain drain voltage waveform measurements. Pajić [15] summarized the class-E design approach with the aid of *agilent ADS* simulation and load-pull measurements. This work was also extended to 10-GHz two-stage class-E amplifiers with power added efficiency of 52 % [11].

In this work, properties of class-E circuit are further studied focusing on dynamically biasing the PA for improved efficiency, power output and linearity. The experimental part of the research is at 10 GHz using a class-E PA designed with GaAs MESFET AFM04P2 from *Alpha industries*. The nominal output power is 20.3 dBm (0.7 dB less than the specified maximum output power) and drain efficiency is 67 %. The class-E PAs designed in this work follow the design method outlined in [15].

In characterizing a RF/microwave PA, common measures of efficiency are drain/collector efficiency (η_D or η_C), power added efficiency (PAE) and total efficiency (η). They are defined as follows:

$$\eta_D(\text{or } \eta_C) = \frac{P_{out}}{P_{DC}} \tag{1.1a}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.1b}$$

$$\eta = \frac{P_{out}}{P_{DC} + P_{in}} \tag{1.1c}$$

where, P_{in}, P_{out} are the input and output RF/microwave power; P_{DC} is the DC power consumed by the PA. Drain/collector efficiency is a measure of DC power to RF/microwave power conversion. PAE is the most commonly used efficiency measure and takes into account of the input power. Total efficiency η is the ratio of total output power and total input power, including both RF/microwave and DC power, and shows the power dissipation in the circuit most clearly.

1.2 Thesis organization

This thesis is composed of seven chapters and a brief overview of each chapter is given below.

- In Chapter 2, the analysis of the class-E circuit is presented for the purpose of finding the tolerance of the PA to the impedance variation at the fundamental and second harmonic frequencies using frequency-domain approach [2]. The analysis of load impedance at fundamental frequency it is assumed that the load network presents an open at all harmonic frequencies. Raab [16] examined the impact of load impedance variation on class-E PA performance analytically under similar assumption for some discrete impedance values. In this work, load impedance are sampled uniformly across the Smith chart and contour plots of parameters characterizing the PA are found. It is shown that the class-E circuit is tolerant of impedance variation. For analysis of impedance sweeping at the second harmonic frequency, the load network is assumed to provide an open circuit at frequencies above the second harmonic. The impedance at the second harmonic is again sampled uniformly across the Smith chart. At each sampled impedance value at the second harmonic frequency, the impedance value at the fundamental frequency is determined to satisfy the "soft switching" boundary conditions. Once the impedance values at first and second harmonic frequencies are known, the circuit can be analyzed for efficiency, power etc. The characterizing parameters of the circuit are shown as contour plots on the Smith chart. The only loss in the circuit

is the power contained in the second harmonic and when its power level is over 40 dB below the signal at fundamental frequency, the efficiency degradation is less than 10 %.

- In Chapter 3, slow dynamic biasing is used for efficiency improvement at lower power levels for 10-GHz class-E PA built using a GaAs MESFET AFM04P2. A similar approach has been applied for efficiency improvement at lower frequencies[17, 18]. The linear relationship between the output signal amplitude and drain bias of a class-E PA enables output power control through drain bias. Our measurement shows that the drain efficiency improved from 41.5% to 60% assuming uniform probability distribution function of the output power in the given range. Although the complexity of the PA circuit increases when the DC/DC converter is added in a feedback loop, it is shown that the overall average efficiency is improved significantly, justfying the addition of dynamic biasing.

- In Chapter 4, the linearity of a class-E PA is characterized in Envelope Elimination and Restoration (EER) mode of operation and a full implementation of a digitally controlled X-band transmitter is demonstrated in collaboration with Yousefzadeh and professor Maksimovic [19]. In a power amplifier design, efficiency and linearity always need to be compromised. Wireless communication is facing scarce bandwidth and to increase channel capacity, the modulation will need to include both amplitude modulation (AM) and phase modulation (PM), which requires a linear PA. The linear relationship between the output signal voltage and drain bias enables a class-E PA to operate in EER mode [20], in which a relatively narrow-band signal is separated into a low-frequency AM signal and a constant-envelope PM signal. The low-frequency AM part of the signal can be amplified by linear amplifier efficiently while the PM signal drives the PA into saturation all the time and hence the PA maintains high efficiency. Linearization of class-E using EER technique has been reported at lower frequencies, e.g. an EER transmitter at HF/VHF is demonstrated in [21] with IMD3 of better than -40 dBc is achieved. Limited work has been done in EER at microwave frequencies. For example,

in [22] the efficiency and linearity behavior of a 8.4-GHz class-F PA is studied for both general linear mode (with constant biasing) and EER mode, for different manually controlled drain bias schemes. An IMD3 level of -27 dBc with a time-average efficiency for a multi-carrier signal with 10-dB peak-to-average ratio of 44% is obtained for a modified EER mode compared to a 10% efficient backed-off class-A PA with the same IMD3 ratio, using the same device. In this thesis, statically measured AM-AM, AM-PM and two-tone test results are analyzed. Efficient wide-band envelope tracking, which is required in the EER scheme, is achieved through a combination of a switched-mode power converter and a linear class-AB amplifier. In the two-tone test, the frequency spacing is 1 MHz and upper side IMD3 level of -25.4 dBc and lower side IMD3 level of -20.7 dBc is achieved. Borges de Carvalho and Pedro [23] explained the cause of asymmetry in the spectrum and attributed it to biasing matching network. It is concluded the EER can be effectively used to linearize the class-E PAs at X-band frequencies.

- In Chapter 5, lookup table (LUT) based baseband digital predistortion is used to improve linearity of the class-E PA. Predistortion offers optimum efficiency and size compared with other two linearization techniques, namely feedforward and feedback [1]. Moreover, with the advances in DSP technology today, baseband digital predistortion becomes more viable for linearization. The IMD3 level of below -30 dBc is usually the requirement for a transmitter [24]. In our predistortion measurement, an IMD3 level of -33 dBc is obtained for a two-tone frequency spacing of 20 kHz. But as the modulation frequency increases, the IMD level deteriorates and also becomes asymmetric due to device memory effects. Open-loop predistortion technique is used here and better linearity is expected with the use of adaptive feedback loop. Device performance changes due to aging, temperature and power supply fluctuation can be corrected through adaptively updating the LUT. However, memory effects remain a problem since memory effects are usually associated with active device low-frequency dispersion, electrothermal interactions and bias circuitry [25]. In addition to the digital

predistortion, this chapter examines optimal load for linearity using a load-pull experimental technique under EER two-tone input. Load-pull has been an important tool for PA design [26] especially for saturated PA. In this thesis *FOCUS* load-pull system is used to measure two-tone intermodulation distortion (IMD) of the class-E PA in both general and EER mode of operation. As expected, load impedance for optimal IMD level are different for this two kind of operation. For the design of class-E with application in EER, the choice of load impedance should accommodate for IMD level.

- In Chapter 6 the possible benefits of using class-E amplifiers as the driving amplifier for an active phased array are studied. Specifically, use of dynamically biased class-E PAs at each antenna element for side-band level control and compensation for mismatch due to scanning are examined. The effect of AM-AM, AM-PM properties of the PA and PA performance with different load impedances are simulated or measured.

In the last chapter, main contributions are reviewed and some directions for future is suggested.

Chapter 2

Theoretical Analysis of Impact of Impedance Variation on Class-E Behavior

The circuit diagram for ideal class-E mode of operation is shown in Fig 2. The active device is modeled as an ideal switch. The parallel capacitor C_s can include output capacitance of the device and external capacitance between drain/collector and source/emitter. The low-pass filter from the series inductor and capacitor is a short at the fundamental frequency and an open at all harmonic frequencies. The load Z_L is a specific complex impedance required by class-E operation. The RFC (radio frequency choke) is an open at fundamental and higher harmonic frequencies. The ideal class-E circuit was analyzed by Raab for a 50 % switching duty cycle, and calculation leading to an optimal value of Z_L is given in [7]. Kazimierczuk et al. [8] solved the circuit for arbitrary duty cycle and Q factor of the harmonic filter. The analysis of the class-E circuit is based on the two boundary conditions in the time domain waveform, that is the time-domain waveform of the voltage across the switch, $v_s(t)$ in Fig 2, goes to zero with zero derivative as the switch closes. The waveforms of the current and voltage of the switch normalized to their DC values are shown in Fig 2 for one period. The boundary conditions, which are also referred to as "soft switching", enforce no power dissipation in the switch and the circuit becomes less sensitive to circuit variations. Ideally, drain/collector efficiency of class-E amplifier is 100 %, assuming the transistor is an ideal lossless switch.

The class-E PAs built in this work follows the design method described by Mader [12]. The parallel capacitance C_s in Fig. 2 is the output capacitor of the active device. At the load side, only the second harmonic is open-circuited, which was shown to be adequate [13]. So, in our design process the major concern is the degradation of class-E operation as the impedances at the fundamental and second harmonic frequency deviate from the optimal values. In order to quantify the deterioration of class-E behavior as a function of impedance variation, the class-E circuit is analyzed here in the frequency domain based on the technique developed by Kee [2]. The device used in most part of this work is a MESFET AFM04P2 from *Alpha industries*. The parallel capacitor at its output port is estimated from its S parameters to be 0.107 pF([27]). The PA design using this particular device was first developed by S. Pajić and the measured second harmonic level at the output is over 40 dB below the power at fundamental frequency.

2.1 Circuit governing equations for frequency domain analysis

For the frequency domain analysis of the class-E mode, the circuit shown in Fig 2.3 [2] is used. The load network is composed of bandpass filters at each of the harmonic frequencies and present an impedance Z_k $(0 \leq k \leq N)$ at frequency $k \times f_o$, where f_o is the fundamental frequency. For harmonic frequencies above $N \times f_o$ the load network is assumed to be open. Our goal is to find the dependence of the circuit on Z_0 and Z_2.

Referring to Fig. 2.3, the sum of current flowing out of the switch and capacitor can be expressed as

$$i_x(\theta) = a_0 + \sum_{k=1}^{N} [a_k \cdot \cos(k\theta) + b_k \cdot \sin(k\theta)] \tag{2.1}$$

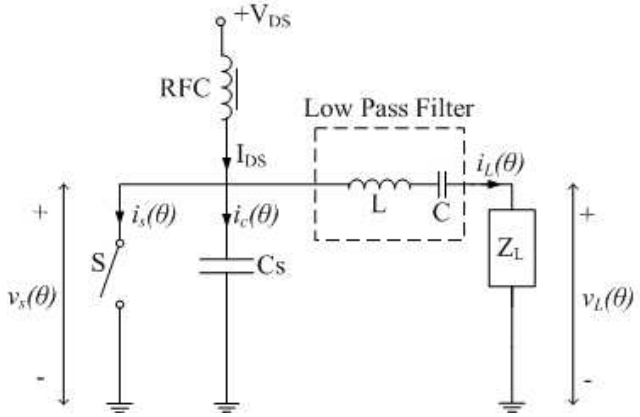


Figure 2.1: The circuit diagram of an ideal class-E amplifier. The active device is modeled as a switch and its output capacitance is a part of the parallel capacitor C_s; The low-pass filter comprised of L and C is a short at the fundamental frequency and an open at all harmonic frequencies; The complex load Z_L is the optimal impedance for class-E operation. RFC (RF choke) is a short at DC and an open at fundamental and higher frequencies.

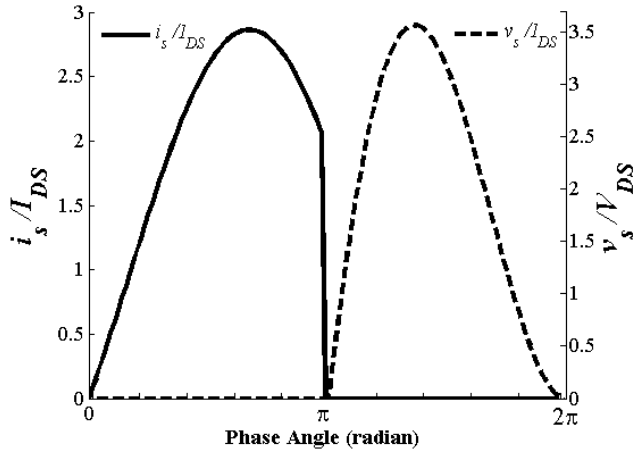


Figure 2.2: The current and voltage waveforms across the transistor (switch) of an ideal class-E amplifier. The values are normalized to their DC values (V_{DS}, I_{DS}).

where angular frequency $\theta = 2\pi f_o t$. Fourier transform coefficients of i_x are

$$I_x(k) = \begin{cases} a_0, & k = 0 \\ a_k - j(b_k/2), & 1 \le k \le N \\ a_k + j(b_k/2), & -k \le k \le -1 \\ 0, & |k| > N \end{cases} \tag{2.2}$$

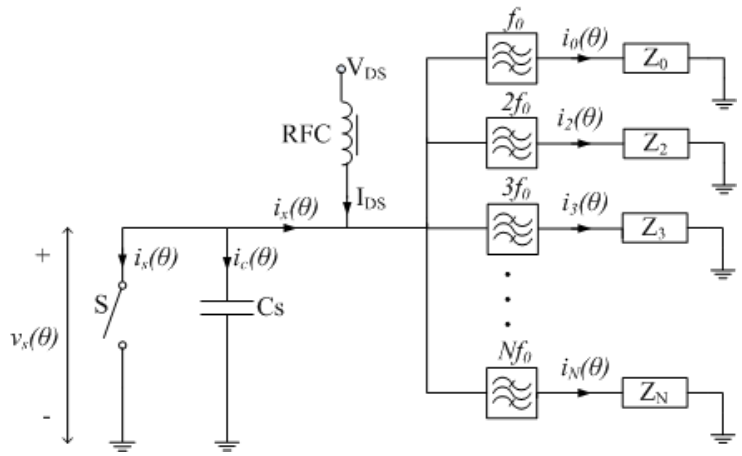


Figure 2.3: The circuit diagram of a class-E amplifier for the frequency domain analysis. The load is decomposed into parallel branches corresponding to fundamental and harmonic frequency terminations. The band-pass filter at k-th branch is a short at kf_o and an open at other frequencies. Z_k is the complex impedance presented to the active device at frequency kf_o [2].

When the switch is closed, no current flows through the capacitor and $i_s = -i_x$; when the switch is open, $i_s = 0$. At the moment the switch closes, if there is charge, Q, stored in the capacitor it will discharge through the switch instantly. This instant discharge causes an impulse $Q\delta(\theta)$ in the current i_s. So, i_s is written as

$$i_s(\theta) = -s(\theta) \cdot i_x(\theta) + Q \cdot \delta(\theta) \tag{2.3}$$

where,

$$s(\theta) = \begin{cases} 1 & 0 \leq \theta < 2\pi D \\ 0 & 2\pi D \leq \theta < 2\pi \end{cases}$$

and D is the duty cycle of the switch, which can be between 0 and 1. As shown in Fig. 2 it is assumed that the switch is closed during $[0, D \cdot 2\pi]$ and open for the rest of the period.

Similarly, the current flowing into the capacitor can be written as

$$i_c(\theta) = -\bar{s}(\theta) \cdot i_x(\theta) - Q \cdot \delta(\theta) \tag{2.4}$$

where,

$$\bar{s}(\theta) = \begin{cases} 0 & 0 \le \theta < 2\pi D \\ 1 & 2\pi D \le \theta < 2\pi \end{cases}$$

The Fourier transforms of the two expressions above at kth harmonic ($0 \le k \le N$) are

$$\begin{aligned} I_s(k) &= \frac{1}{2\pi} Q - S(k) \otimes I_x(k) \\ &= \frac{1}{2\pi} Q - \sum_{l=-N}^{N} S(k-l) I_x(l) \end{aligned} \tag{2.5}$$

$$\begin{aligned} I_c(k) &= -\frac{1}{2\pi} Q - \bar{S}(k) \otimes I_x(k) \\ &= -\frac{1}{2\pi} Q - \sum_{l=-N}^{N} \bar{S}(k-l) I_x(l) \end{aligned} \tag{2.6}$$

where, $\otimes$ denotes convolution; $S(k)$ and $\bar{S}(k)$ are the Fourier transformation of $s(\theta)$ and $\bar{s}(\theta)$, and $\bar{D} = 1 - D$, resulting in

$$S(k) = \begin{cases} D, & k = 0 \\ \dfrac{\sin(2\pi D k)}{2\pi k} - j\dfrac{\sin^2(\pi D k)}{\pi k}, & k \ne 0 \end{cases} \tag{2.7}$$

$$\bar{S}(k) = \begin{cases} 1 - D, & k = 0 \\ \dfrac{\sin(2\pi \bar{D} k)}{2\pi k} + j\dfrac{\sin^2(\pi \bar{D} k)}{\pi k}, & k \ne 0 \end{cases} \tag{2.8}$$

Voltage builds up across the switch when the capacitor is being charged, so

$$\begin{aligned} v_s(\theta) &= \frac{1}{C_s} \int_0^{\theta'} i_c(\theta')\, d\theta' \\ &= \begin{cases} 0, & 0 < \theta < 2\pi D \\ \dfrac{1}{\omega_o C_s} \int_{2\pi D}^{\theta} i_c(\theta')\, d\theta', & 2\pi D < \theta < 2\pi \end{cases} \end{aligned} \tag{2.9}$$

Its Fourier transform is

$$V_s(k) = -j \frac{1}{\omega_o C_s} \frac{I_c(k)}{k} \qquad k \ne 0 \tag{2.10}$$

At each frequency

$$Z_k \cdot I_x(k) = V_s(k), \qquad 0 < k \le N \tag{2.11}$$

Substituting Eq. (2.10) into above expression, the following is obtained:

$$jk\omega_o C_s Z_k I_x(k) - I_c(k) = 0, \qquad 0 \le k \le N \tag{2.12}$$

The above equation is also valid for $k = 0$ case since the DC component of the current through the capacitor is zero. Substituting Eq. (2.6) into Eq. (2.12) gives

$$jk\omega_o C_s Z_k I_x(k) + \frac{1}{2\pi} Q + \bar{S}(k) \otimes I_x(k) = 0, \quad 0 \le k \le N \tag{2.13}$$

Now we can normalize the impedance values, Z_k, to the impedance value of the parallel capacitor, $\frac{1}{\omega_o C_s}$:

$$R_{ok} = \mathrm{Re}(Z_k)\omega_o C_s \tag{2.14a}$$

$$X_{ok} = \mathrm{Im}(Z_k)\omega_o C_s \tag{2.14b}$$

Substitute equations (2.2),(2.8) and (2.14) into Eq. (2.13). The results for $D = 0.5$ (i.e. 50 % duty cycle) are shown below. When $k = 0$,

$$\frac{1}{2} a_0 - \sum_{l=1}^{N} \left(\frac{1 - (-1)^l}{2\pi l} \right) b_l + \frac{1}{2\pi} Q = 0 \tag{2.15}$$

When $k \neq 0$ the real part of the equation is

$$(\frac{1}{4} - \frac{kX_{ok}}{2}) a_k + \frac{kR_{ok}}{2} b_k + \frac{1}{2\pi} Q + \sum_{\substack{l=1 \\ l \neq k}}^{N} \frac{l\big(1 - (-1)^{k+l}\big)}{2\pi(k^2 - l^2)} b_l = 0 \tag{2.16}$$

the imaginary part gives

$$\frac{1 - (-1)^k}{2\pi k} a_0 + \frac{kR_{ok}}{2} a_k - \left(\frac{1}{4} - \frac{kX_{ok}}{2} \right) b_k + \sum_{\substack{l=1 \\ l \neq k}}^{N} \frac{k\big(1 - (-1)^{k+l}\big)}{2\pi(k^2 - l^2)} a_l = 0 \tag{2.17}$$

The linear system of equations from (2.15) to (2.17) are the governing equation set for the circuit shown in Fig 2.3 with duty cycle of 50 %. There are (2N+1) equations and (2N+2) unknowns $(a_0, a_1, \ldots, b_1, b_2, \ldots, Q)$. The equations above can be written

in the following matrix form:

$$[A]_{(2N+1)\times(2N+2)} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ b_1 \\ b_2 \\ \vdots \\ Q \end{bmatrix}_{2N+2} = 0 \tag{2.18}$$

Now the class-E requirements will be imposed to the circuit governing equations (2.18). The boundary conditions are:

$$V_s|_{\theta=0} = 0 \tag{2.19a}$$

$$\left.\frac{dV_s}{d\theta}\right|_{\theta=0} = 0 \tag{2.19b}$$

The voltage across the capacitor at the instant of transition is zero which means that the charge on the capacitor at that moment is zero, $Q = 0$. Together with linear system in Eq. (2.18), there are now $2N + 2$ unknows and equations.

$$\begin{bmatrix} [A]_{2N+1} \\ Q \end{bmatrix}_{2N+2} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ b_1 \\ b_2 \\ \vdots \\ Q \end{bmatrix}_{2N+2} = 0 \tag{2.20}$$

For this homogeneous system to have nontrivial solution, the determinant must be zero:

$$\begin{vmatrix} [A]_{(2N+1)\times(2N+2)} \\ [0\ 0\cdots\ 1]_{1\times(2N+2)} \end{vmatrix} = 0 \tag{2.21}$$

Based on equations (2.9),(2.4) and (2.1) the second boundary condition, Eq. (2.19b) becomes

$$\begin{aligned}\left.\frac{dV_s}{d\theta}\right|_{\theta=0} &= \frac{1}{\omega_o C_s} i_c|_{\theta=0} \\ &= -\frac{1}{\omega_o C_s} \sum_{k\in\{0,N\}} a_k \\ &= 0\end{aligned} \tag{2.22}$$

therefore,

$$\sum_{k\in\{0,N\}} a_k = 0 \tag{2.23}$$

With Eq. (2.18), there is another homogeneous system of size $2N+2$.

$$\begin{bmatrix} [A]_{(2N+1)\times(2N+2)} \\ \begin{bmatrix}1\ 1\cdots\end{bmatrix}_{1\times(N+1)}\ \begin{bmatrix}0\ 0\cdots\end{bmatrix}_{1\times(N+1)} \end{bmatrix}_{\substack{(2N+2)\times \\ (2N+2)}} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ b_1 \\ b_2 \\ \vdots \\ Q \end{bmatrix}_{\substack{(2N+2) \\ \times 1}} = 0 \tag{2.24}$$

Again the determinant must go to zero to have nontrivial solutions.

$$\begin{vmatrix} [A]_{(2N+1)\times(2N+2)} \\ \begin{bmatrix}1\ 1\cdots\end{bmatrix}_{1\times(N+1)}\ \begin{bmatrix}0\ 0\cdots\end{bmatrix}_{1\times(N+1)} \end{vmatrix} = 0 \tag{2.25}$$

The impedance values need to satisfy Eq. (2.25) and Eq. (2.21) to meet the "soft switching" boundary conditions for class-E operation.

The voltage and current waveforms can be found when all impedances and DC bias values are known. a_0, the DC portion of the current i_x is supplied by the DC source and is equal to I_{DS}. When combined with linear system of equations (2.18), the

following results:

$$\begin{bmatrix} [A]_{(2N+1)\times(2N+2)} \\ \begin{bmatrix}-1\ 0\cdots\end{bmatrix}_{1\times(N+1)}\ \begin{bmatrix}0\ 0\cdots\end{bmatrix}_{1\times(N+1)} \end{bmatrix}_{\substack{(2N+2)\times \\ (2N+2)}} \begin{bmatrix} a_0 \\ a_1 \\ \vdots \\ b_1 \\ b_2 \\ \vdots \\ Q \end{bmatrix}_{\substack{(2N+2) \\ \times 1}} = \begin{bmatrix} I_{DS} \\ 0 \\ \vdots \end{bmatrix}_{\substack{(2N+2) \\ \times 1}} \tag{2.26}$$

This is an inhomogeneous system of equations describing the circuit in Fig. 2.3. With impedance values, $Z_k (0 \leq k \leq N)$ known, waveform coefficients can be calculated and time domain waveform for voltage and current across the switch will be obtained. This formulation is reported in reference [2], where it is used to develop class-E/F PA by optimizing load impedance at harmonic frequencies. Our goal is to extend this theory in order to be able to perform theoretical load-pull analysis for the impedance at the fundamental frequency and second harmonic and find the tolerances of the class-E circuit operation to the impedance values. Load-pull is the most accepted experimental technique for high efficiency and high power microwave PA design, and in Chapter 5 load-pull measurement results will also be shown.

2.2 Effect of impedance variations at fundamental frequency

The influence of impedance variation at the fundamental frequency is analyzed assuming the load network provides an open-circuit at second and higher harmonic frequencies based on the derivation in last section. The impedance at the fundamental frequency will be swept and contour plots for drain efficiency, power capability and output power will be plotted on the Smith chart.

Since all higher order harmonic frequencies are open-circuited by the load network,

$N = 1$ in the equations derived in previous section. The normalized impedance at the fundamental frequency is $Z_{o1} = R_{o1} + jX_{o1}$ and i_x becomes

$$i_x(\theta) = a_0 + a_1 \cos(\theta) + b_1 \sin(\theta) \tag{2.27}$$

The matrix A in Eq. 2.18 becomes

$$A = \begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{\pi} & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & \frac{R_{o1}}{2} & 0 \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 \end{bmatrix} \tag{2.28}$$

The class-E impedance will be calculated from Eq. (2.21) and Eq. (2.25), which in this case reduce to:

$$\begin{vmatrix} \frac{1}{2} & 0 & -\frac{1}{\pi} & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & \frac{R_{o1}}{2} & 0 \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 \\ 0 & 0 & 0 & 0 \end{vmatrix} = 0 \tag{2.29a}$$

$$\begin{vmatrix} \frac{1}{2} & 0 & -\frac{1}{\pi} & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & \frac{R_{o1}}{2} & 0 \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 \\ 1 & 1 & 0 & 0 \end{vmatrix} = 0 \tag{2.29b}$$

Solving the equation set results in the normalized impedance for the optimal class-E operation:

$$R_{o1} = \frac{8}{4\pi + \pi^3} = 0.1836 \tag{2.30a}$$

$$X_{o1} = \frac{-4 + \pi^2}{8 + 2\pi^2} = 0.2116 \tag{2.30b}$$

Note that there is a second solution which is trivial and gives $R_{o1} = 0$.

Current waveform coefficients are calculated from Eq. (2.26):

$$\begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{\pi} & \frac{1}{2\pi} \\ 0 & \frac{1}{4}-\frac{X_{o1}}{2} & \frac{R_{o1}}{2} & 0 \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & \frac{X_{o1}}{2}-\frac{1}{4} & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ Q \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ I_{DS} \end{bmatrix} \tag{2.31}$$

Substituting the values of the fundamental impedance, the waveform coefficients are found to be:

$$\begin{bmatrix} a_0 \\ a_1 \\ b_1 \\ Q \end{bmatrix} = \begin{bmatrix} -I_{DC} \\ I_{DC} \\ -\frac{\pi}{2}I_{DC} \\ 0 \end{bmatrix} \tag{2.32}$$

The voltage across the switch,v_s, during period $\theta \in [\pi\ 2\pi]$ is

$$\begin{aligned} v_s(\theta) &= \frac{1}{\omega_o C_s}\int_{\pi}^{\theta} i_c(\theta')d(\theta') \\ &= -\frac{1}{\omega_o C_s}(a_0(\theta-\pi)+a_1\sin(\theta)+b_1\cos(\theta)+b_1) \\ &= \frac{1}{\omega_o C_s}I_{DC}\big((\theta-\pi)-\sin(\theta)-\frac{\pi}{2}\cos(\theta)-\frac{1}{2}\pi\big) \end{aligned} \tag{2.33}$$

The average (DC) and maximum values of the i_x and v_s are

$$\begin{aligned} i_{x,DC} &= I_{DS} \\ i_{x,max} &= i_s|_{\theta=2.14} = 2.86 I_{DS} \\ v_{s,DC} &= \frac{1}{\pi\omega_o C_s}I_{DC} \\ &= V_{DS} \\ v_{s,max} &= v_s|_{\theta=4.28} = 3.55 V_{DS} \end{aligned} \tag{2.34}$$

The waveforms of i_x and v_s normalized to their average values are shown previously in Fig 2. The RF output voltage across the real part of the impedance R_1 is

$$V'_{out} = R_1\sqrt{a_1^2+b_1^2} = \frac{4}{\sqrt{4+\pi^2}}V_{DC} = 1.074 V_{DC} \tag{2.35}$$

When a matching network is used to transform the $50-\Omega$ load to the desired impedance of $R_1 + jX_1$, the output voltage across the load is

$$V_{out} = \sqrt{\frac{50}{R1}} V_{out} = \sqrt{\frac{50}{R_1}} \frac{4}{\sqrt{4+\pi^2}} V_{DC} \tag{2.36}$$

Hence, there exist a linear relationship between the drain bias and output voltage. This property is the basis for the application of class-E PA to EER schematic, as will be discussed later.

The Output power and power capability (as defined in [24]) are

$$P_{out} = \frac{1}{2}|i_x - i_{x,DC}|^2 R_1 = \frac{1}{\pi\omega_o C_s} I_{DC}^2 = \pi\omega_o C_s v_{s,DC} \tag{2.37a}$$

$$P_{cp} = \frac{P_{out}}{v_{s,max} i_{s,max}} = 0.098 \tag{2.37b}$$

In this work, as mentioned earlier, the device used in the measurements is a GaAs MESFET AFM04P2 from *Alpha Industries*. In saturation, the MESFET is approximated by a switch in parallel with a capacitor. The parallel capacitance for this device found from S parameter deembedding is $Cs = 0.107\,\text{pF}$. The operating frequency is $f_o = 10\,\text{GHz}$. The DC bias voltage, V_{DS} is generally given. However Eq. (2.26) solves the circuit assuming DC bias current, I_{DS}, is known. Eq. (2.9) shows that DC voltage and current coefficients (I_{DS}, $a_0, \cdots, a_N$) scale linearly, which enables the analysis of the circuit for constant DC voltage bias.

The reactance of the output capacitor is $\frac{1}{\omega_o C_s} = 148.7\Omega$. The impedance is swept and for each value Eq. (2.31) is solved. Based on the waveform of the voltage and current of the switch drain efficiency, normalized output power and power capability are calculated and their contour plots are shown in Fig. 2.4. In Fig. 2.4(a) the optimal impedance for ideal class-E operation is indicated by the cross sign, which corresponds to 100 % drain efficiency and its value is $Z_{opt} = 27.3013 + j31.4649$. When Z_{opt} is normalized with respect to $\frac{1}{\omega_o C_s}$ with $Cs = 0.107\,\text{pF}$, Eq. (2.30) is obtained. The drain efficiency shows considerable tolerance on the impedance change. When the load

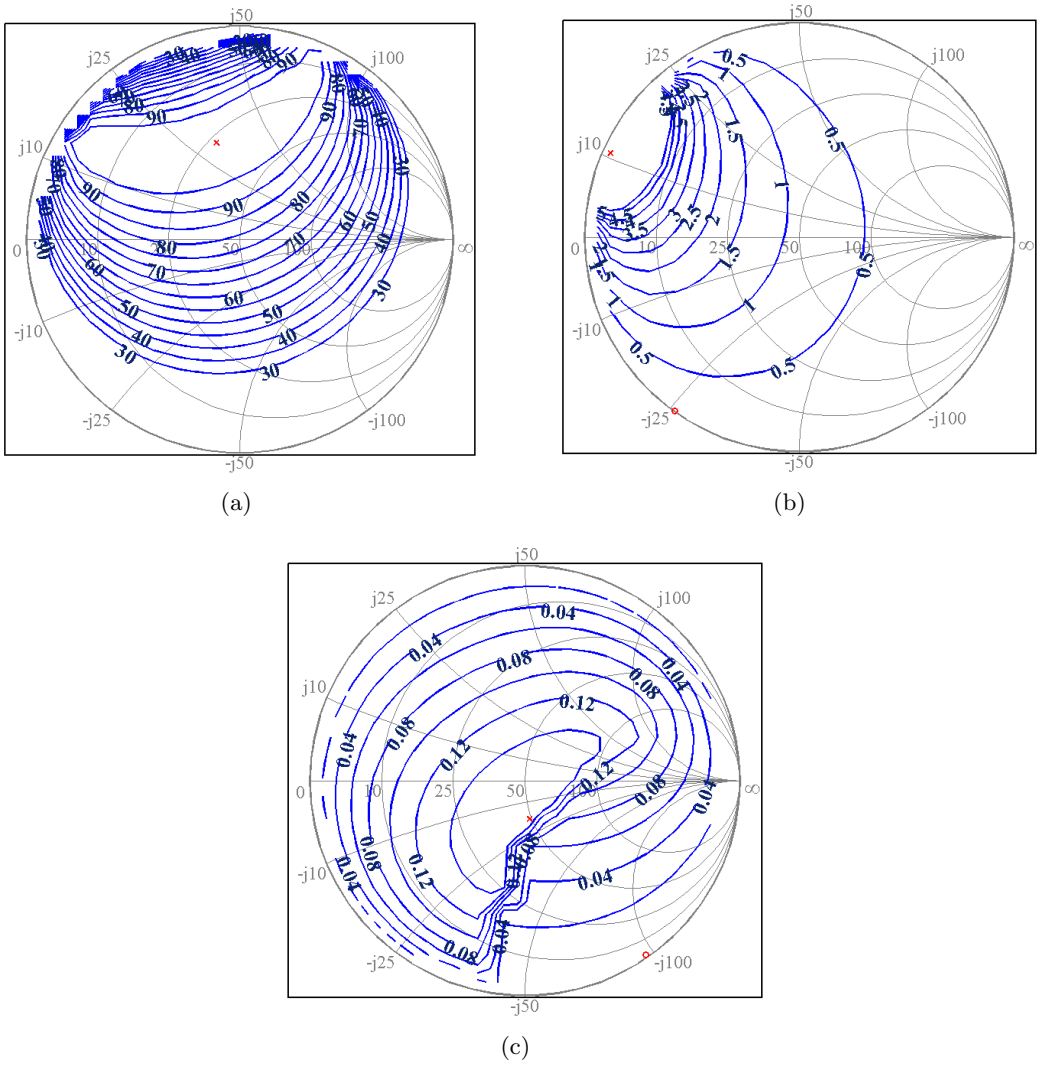


Figure 2.4: Class-E circuit behavior characterization as load impedance takes on discrete values uniformly sampled in the Γ place. (a)Drain efficiency (%) of the circuit. The cross sign is the optimal impedance for ideal class-E operation, $\Gamma_{opt} = -0.1098 + j0.4517$. (b)The normalized output power (W) of the circuit. The normalization value is the output power of the circuit when the load is the optimal value Z_{opt}. (c)The power capability of the circuit.

changes within a circle of radius 0.2, that is $|\Gamma_{opt} - \Gamma_{load}| \leq 0.2$, the drain efficiency is over 90 %. Fig 2.4 shows that ideal class-E impedance does not provide maximum output power and power capability. The stress on the device is worst in class-E compared with class-A/B/C and class-F [24]. As will be discussed in the next chapter, in our design practice, the power amplifier is optimized for both output power and efficiency.

2.3 Effect of impedance variation at second harmonic frequency

In the design of the class-E PA, the second harmonic is explicitly terminated by an open-circuit. Next we will examine the effect of the impedance at the second harmonic frequency $R_2 + jX_2$ while assuming higher harmonics are open-circuited and "soft switching conditions" are satisfied. The impedance at the second harmonic is swept. At each impedance value swept, $R_2 + jX_2$, based on Eq. (2.21) and Eq. (2.25), impedance value at fundamental frequency, $R_1 + jX_1$, satisfying the two boundary conditions is calculated. The resulting load network presents $R_1 + jX_1$ at fundamental frequency, $R_2 + jX_2$ at the second harmonic frequency and the circuit satisfies the "soft switching" operating conditions. Therefore, the only loss in the power will be power contained in the second harmonic.

When $N = 2$, based on Eq. (2.15) to Eq. (2.17) the matrix A becomes

$$A = \begin{bmatrix} \frac{1}{2} & 0 & 0 & -\frac{1}{\pi} & 0 & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & 0 & \frac{R_{o1}}{2} & -\frac{2}{3\pi} & \frac{1}{2\pi} \\ 0 & 0 & \frac{1}{4} - X_2 & \frac{1}{3\pi} & R_2 & \frac{1}{2\pi} \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & -\frac{1}{3\pi} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 & 0 \\ 0 & \frac{2}{3\pi} & R_2 & 0 & X_2 - \frac{1}{4} & 0 \end{bmatrix} \tag{2.38}$$

The impedance at the fundamental frequency is chosen to satisfy the boundary condi-

tions. At $N = 2$, Eq. (2.21) and Eq. (2.25) become

$$\begin{vmatrix} \frac{1}{2} & 0 & 0 & -\frac{1}{\pi} & 0 & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & 0 & \frac{R_{o1}}{2} & -\frac{2}{3\pi} & \frac{1}{2\pi} \\ 0 & 0 & \frac{1}{4} - X_2 & \frac{1}{3\pi} & R_2 & \frac{1}{2\pi} \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & -\frac{1}{3\pi} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 & 0 \\ 0 & \frac{2}{3\pi} & R_2 & 0 & X_2 - \frac{1}{4} & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{vmatrix} = 0 \tag{2.39a}$$

$$\begin{vmatrix} \frac{1}{2} & 0 & 0 & -\frac{1}{\pi} & 0 & \frac{1}{2\pi} \\ 0 & \frac{1}{4} - \frac{X_{o1}}{2} & 0 & \frac{R_{o1}}{2} & -\frac{2}{3\pi} & \frac{1}{2\pi} \\ 0 & 0 & \frac{1}{4} - X_2 & \frac{1}{3\pi} & R_2 & \frac{1}{2\pi} \\ \frac{1}{\pi} & \frac{R_{o1}}{2} & -\frac{1}{3\pi} & \frac{X_{o1}}{2} - \frac{1}{4} & 0 & 0 \\ 0 & \frac{2}{3\pi} & R_2 & 0 & X_2 - \frac{1}{4} & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 \end{vmatrix} = 0 \tag{2.39b}$$

The results for above calculations are shown in Fig. 2.5. For certain values of impedance at the second harmonic frequency, equation set (2.39) cannot be solved, that is "soft switching" boundary conditions cannot be satisfied by proper choice of impedance at fundamental frequency. These impedance values are shown as the shaded area in each Smith chart. Fig. 2.5(a) shows that when the second harmonic level is less than 40 dBc the drain efficiency degrades less than 10 %. Fig. 2.5 shows that the impedance at the second harmonic can be optimized for output power or device stress (described by power capability) without sacrificing drain efficiency. Especially, when the impedance at the second harmonic is more capacitive while staying close to the $|\Gamma| = 1$ circle, more output power can be obtained. As mentioned earlier in this chapter, in the PA built, power level at the second harmonic is about 40 dB below the power at fundamental frequency. So, the termination of the second harmonic in the PA is adequate concerning drain efficiency degradation.

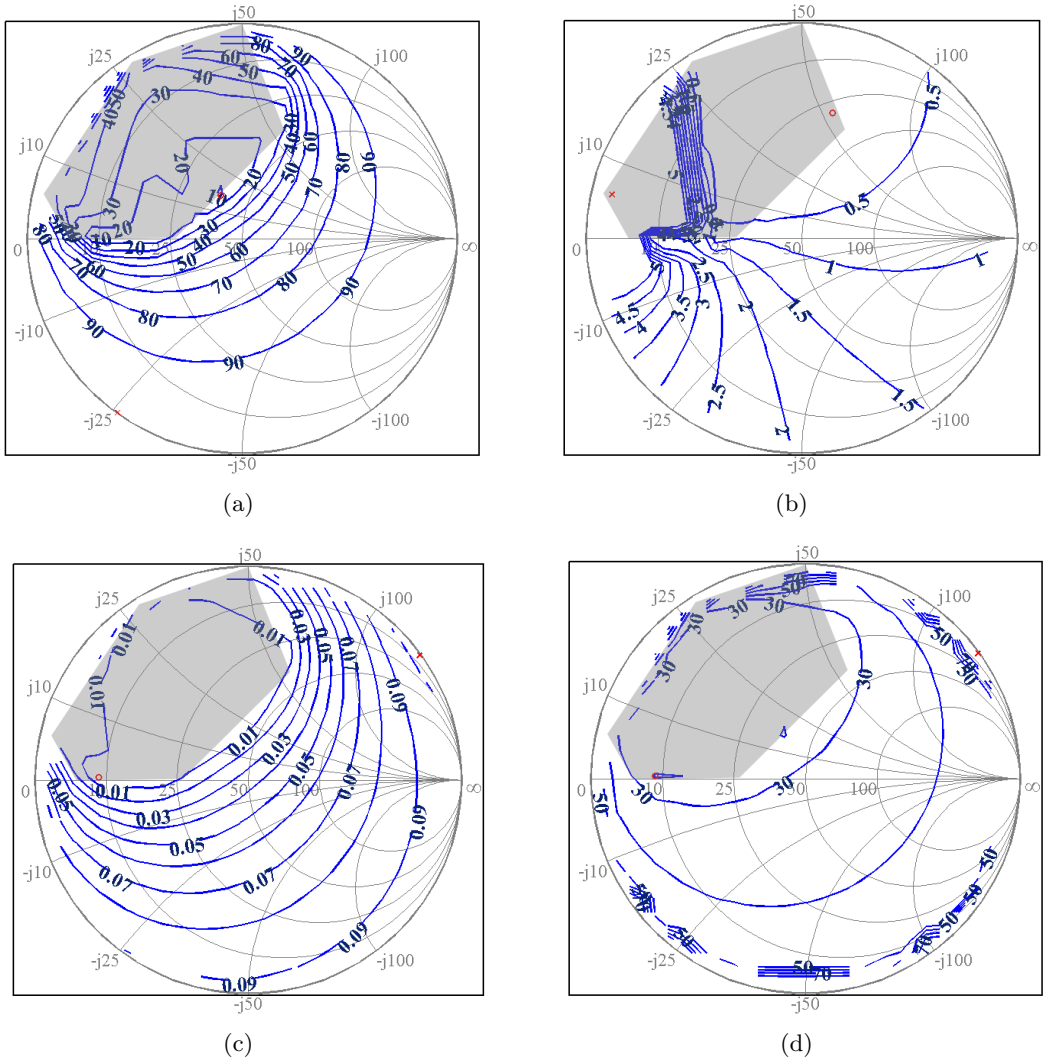


Figure 2.5: Class-E circuit behavior characterization as load impedance at second harmonic frequency varies: (a)Drain efficiency (%). (b)Output power (W) normalized to the ideal class-E case, that is impedance at second harmonic is an open-circuit. (c)Power capability. (d)The second harmonic power level relative to the power at fundamental frequency (dB).

2.4 Discussion

In this chapter the sensitivity of class-E PA to the load variation at fundamental frequency and second harmonic is discussed through analytical approach. It is verified that ideally, class-E circuit is quite tolerant of impedance change. The load-pull measurement of the class-E circuit of the MESFET AFM04P2 device has been performed

by Pajić [27]. In this work, similar measurements are carried out and results are shown in Chapter 5. The measurement of load-pull of impedance at second harmonic is left as future work and believe this will help clarify and improve design strategy for class-E PA at microwave frequencies.

Chapter 3

Dynamic Biasing of Class-E PA for Output Power Control

High-efficiency power amplifiers are designed to operate in the saturated regime. As a consequence, when a range of output power levels is required, such as in the case of mobile phone communications, the efficiency suffers at the lower power levels. The idea of dynamic control of the bias supply is brought up to increase the efficiency for low output power levels by optimally varying the bias supply. Hanington et al. [17] designed a dynamic control circuit using a boost DC-DC converter, and demonstrated an increase in average efficiency by a factor 1.64 (from 3.89% to 6.38%) for a 1-MHz bandwidth CDMA signal input to a 950-MHz HBT class-A power amplifier. The same authors applied a DSP controlled DC/DC converter and a predistortion technique to a 950-MHz CDMA signal amplifier and showed improvement in efficiency (by a factor of 1.4) as well as linearity (8dB improvement in ACPR) [28]. Staudinger et al. [18] and Raab et al. [29] used a class S modulator to supply the dynamic changing drain bias at low microwave frequencies (835MHz and L-band). In [18], the average efficiency for CDMA signals was increased by a factor of 5 over the constant bias case.

This chapter describes the implementation of the high-efficiency 10-GHz class-E amplifier with dynamic drain bias control that maintains high efficiency over a range of output power levels. The 10-GHz design frequency is 10 times higher than the carrier frequencies in referenced material, making the high-efficiency switch-mode design more difficult. First, design and characterization of the class-E PA using MESFET device is

shown. Next, the efficiency improvement over certain output power range is presented. Finally is the results for the same approach appied to class-E PA designed using DHBT and PHEMT devices.

3.1 Class-E PA characterization

In the previous chapter it is mentioned that most part of the work in this thesis uses GaAs MESFET AFM04P2 from *Alpha industries* for the PA design. The first class-E PA using this device is designed by Srdjan Pajić and the PAs built for this work is based on his design. For the design details please refer to [27]. Numerous PAs have been built in this work and due to different devices and individual tweaking, there are somewhat difference between them as will be noticed in later chapters. The substrate used in the PA implementation is Rogers^{TM} TMM6 with $\epsilon_r = 6$ and a thickness of 0.635 mm. The chip device is mounted on a ground pedestal to minimize bond-wire inductances. In saturation, this particular MESFET's output port is approximated as parallel connection of a switch and a capacitor of 0.107 pF[27]. The PA built is shown in Fig. 3.1. The output port consists of two stubs, one for second harmonic open-circuit termination and the other is for providing the optimal load impedance, which is found to be $Z_{opt} = 27.3 + j32.5\,\Omega$ at fundamental frequency in Chap 2. After the matching section there is a 20-dB coupler and a detector for sensing the output power, which are for output power control as will be discussed. The input matching network maximizes the compressed amplifier gain.

3.1.1 Class-A PA characterization

The power amplifier operates in class-E switched mode with 67% drain efficiency at an output power of 20.3dBm, 0.7dB less than the specified maximum power for the device. Fig. 3.2 shows the measured power, efficiency and gain of the PA in terms of input and output power. The results in Fig. 3.2(a) are measured for a fixed input

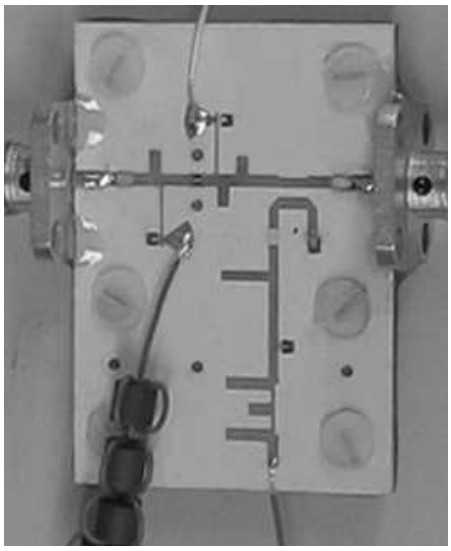


Figure 3.1: Class-E PA built using MESFET AFM04P2 (*Alpha industries*), includes input and output matching circuits, biasing circuits and output power detector (coupler, Schottky diode and low-pass filter).

power of 12 dBm, gate bias of -1.4 V and varying drain bias. The output power and efficiency in Fig. 3.2(b) are measured with a gate bias of -1.4 V, a drain bias of 4.0 V and varying input power. The PA drain bias properties are characterized in Fig. 3.2(c), which shows that at drain, the PA behaves as a resistor of constant value as the output power changes.

3.1.2 Drain voltage waveform probing

To verify that the PA is operating in class-E mode, another PA is built to probe the drain voltage waveform of the PA. The diagram of the PA and test setup are shown in Fig. 3.3. For simplicity, no bias line or the output coupler section is built on the PA. A resistor of 1 KΩ is connected between the drain and tapered 50-Ω line, which then connected to the oscilloscope. The resistor is placed as close to the drain of the device as possible. The resistor size is 0.3 mm by 0.6 mm. It is hoped that the resistor don't disturb the class-E operation. In the setup, through a divide-by-8 frequency

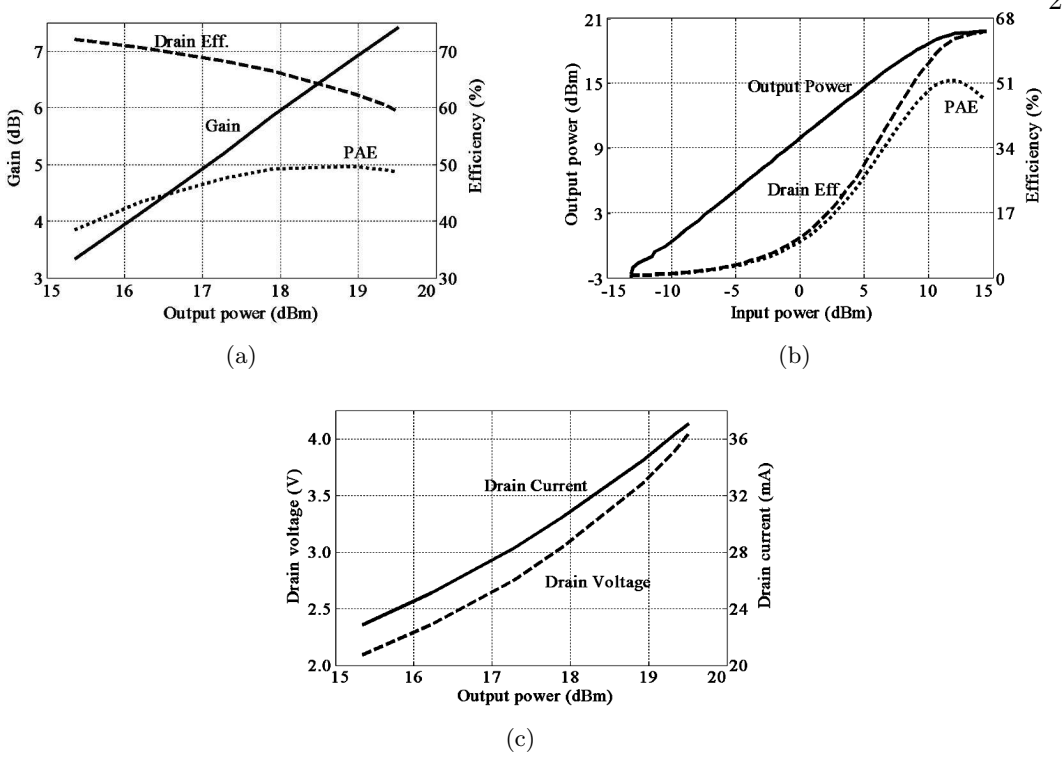
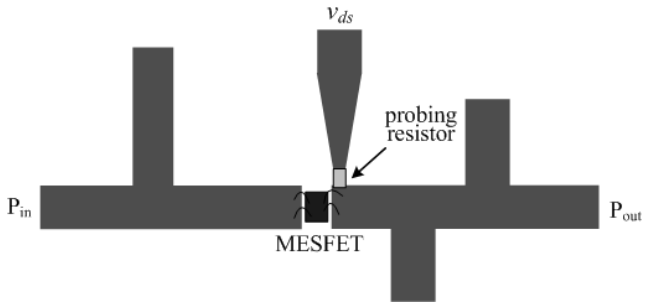
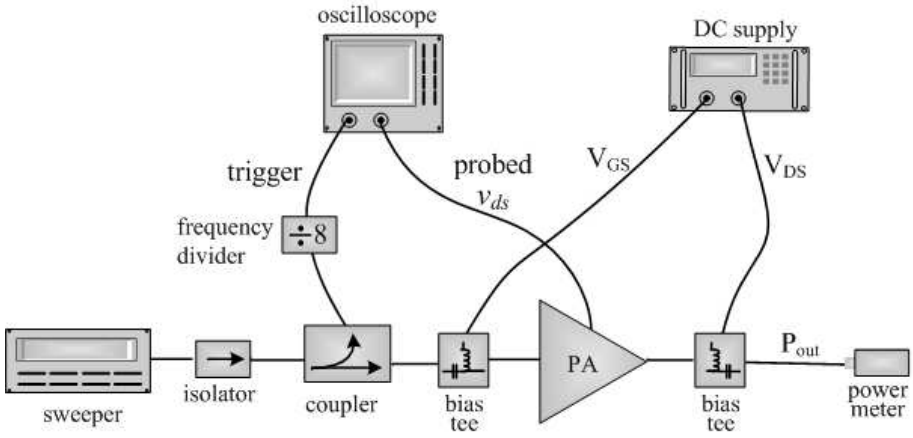


Figure 3.2: Measured characteristics of the class-E PA: (a) gain and efficiency as a function of output power; (b) output power and efficiency as a function of input power; (c) measured drain voltage and current of the PA vs. output power for constant input power.

divider the signal from the sweeper becomes 1.25 GHz and fed to the trigger port of the oscilloscope (which has a maximum frequency limit of 2 GHz). HP 54750 digitizing oscilloscope, which has a bandwidth of 50 GHz, is used to record the time-domain signal. The input impedance of the signal port is 50 Ω. The signal shown on the scope will be approximately 1/21 of the drain voltage. The matching network of the PA is tweaked to find the optimum efficiency and output power. The waveform of the drain voltage is shown in Fig. 3.4. In the waveform captured, the rising edge is sharper than its falling edge and the duty cycle is approximately 50%. The reason voltage doesn't drop down to zero may due to the seris ON-resistance of the device. A comparison between the ideal class-E waveform is made in Table 3.1. The maximum voltage is smaller and the output voltage is less then the theoretical results. This may due to the parasitics in the



(a)



(b)

Figure 3.3: Drain voltage probing of the class-E PA: (a) the circuit layout of the PA; (b) measurement setup.

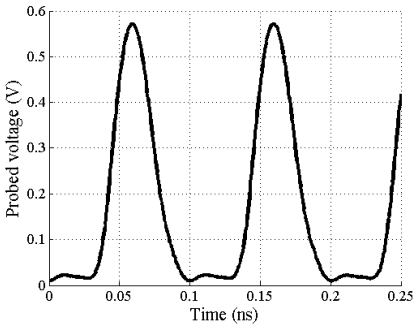


Figure 3.4: Wavefrom at the drain of the device

circuit for measurement(parasitics in the resistor, etc.). so, the device is operating in close to class-E mode. A comparison of the PA behavior with and without the probing

resistor is compared in Table 3.2.

	V_{max}	V_{DC}	V_{out}
meas.	12.01	4.05	2.88
ideal	14.42	4.05	5.87

Table 3.1: Comparison of measurement and ideal drain voltage

	P_{out} (dBm)	V_{DS} (V)	I_{DS} (mA)	$\eta_D(\%)$
with r_p	19.18	4.05	39.1	52.3
no r_p	19.56	4.05	34.1	65.4

Table 3.2: Comparison of PA behavior with and without the probing resistor. r_p is the probing resistor.

3.2 Measurement setup and results for output power control

Measurement setup for the class-E PA applied in output power control is shown in Fig. 3.5. Output power of the PA is sensed through a 20-dB coupled line coupler and

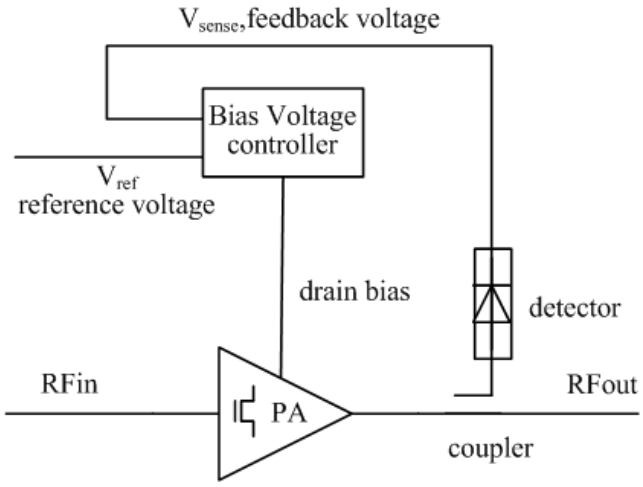


Figure 3.5: The measurement diagram for output power control

a single diode detector following the output PA matching circuit. The insertion loss of the coupler is less than 0.5dB, with connectors contributing about 0.2dB in addition. An *Agilent* HSCH-5332 Schottky diode is used for the detector. Input matching is

provided by a single stub, and at the output the 10-GHz signal is filtered to obtain the signal V_{sense}. In the feedback loop, this signal is compared with a reference V_{ref}, which serves as the power command signal. The loop is closed through the DC-DC converter (designed by Vahid Yousefzadeh [30]) that adjusts the drain bias to the PA such that the measured output power signal matches the command power signal. The values for V_{ref} are based on the characterization of coupler and detector at the output of the PA.

The efficiency of the high-efficiency Buck DC-DC converter is about 96% efficient and is shown in Fig. 3.6. The efficiency of the PA with the closed-loop power control

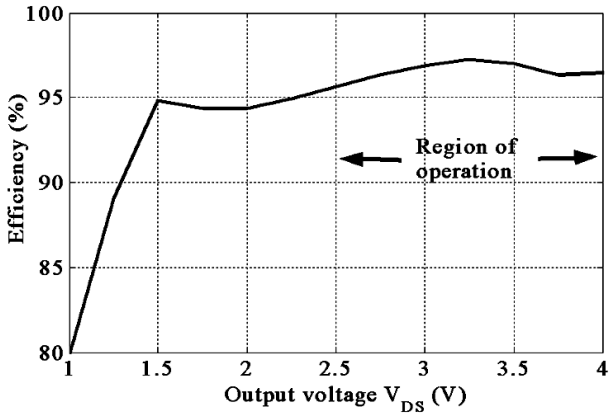


Figure 3.6: Measured efficiency of the DC-DC converter as a function of the output voltage V_{DS} for the PA as the load.

and with constant input power of 12dBm is measured and is shown in Fig. 3.7 over the output power range of 15dBm to 20dBm. The gate bias voltage is kept at -1V. Several curves are compared in Fig. 3.7. The curve with the lowest overall efficiency is measured for constant drain bias while the output power is varied. The highest efficiency curve, with an average drain efficiency of 62.3% is measured for the PA alone where the drain bias is varied manually. The solid line with an average efficiency of 60.4% is obtained with the entire closed-loop circuit from Fig. 3.5 and the loss due to the connectors and coupler calibrated out. The dotted curve shows the slightly lower measured total efficiency that includes the connector loss, which can easily be eliminated by fabricating

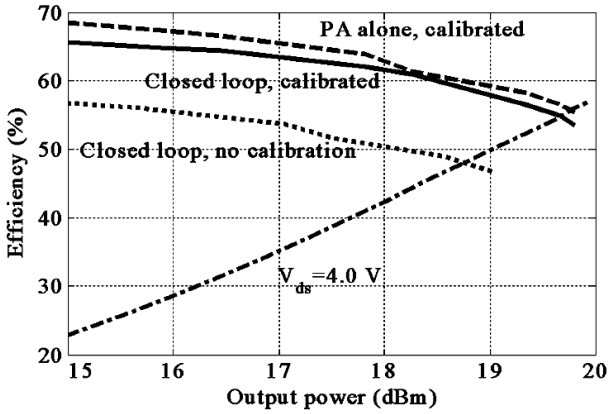


Figure 3.7: Measured efficiency for the PA with constant drain bias (dash-dot line), the PA with manual drain bias control (dashed line), the entire closed loop system when the connector loss and coupler loss is calibrated out (solid line), and the uncalibrated closed loop system (dotted line).

the PA and coupler/detector circuit on the same substrate. The average efficiency is calculated from measured data as an unweighted average, and a summary is as follows:

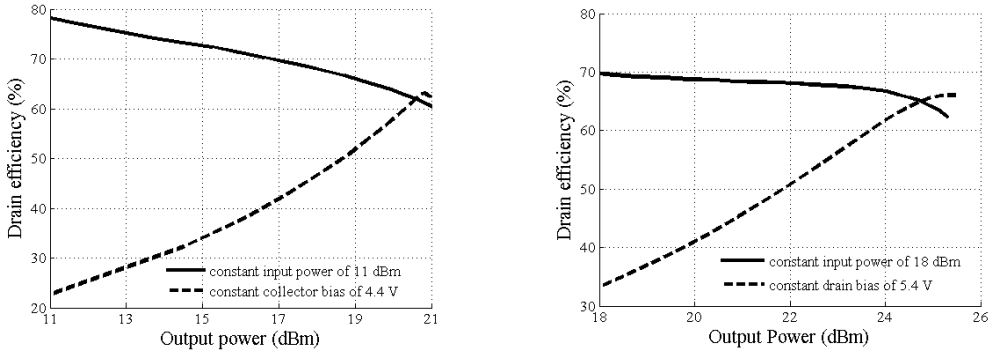
$$\begin{aligned} \eta_{PA} &= 62.3 \\ \eta_{loop} &= 60.4 \\ \eta_{loop,connectors} &= 50.7 \\ \eta_{constantVds} &= 41.5 \end{aligned}$$

where η_{PA} is the drain efficiency of the class-E power amplifier at optimal bias and constant input power, η_{loop} is the efficiency of the entire closed loop for the same conditions, $\eta_{loop,connectors}$ is the measured efficiency that includes the coupler and connector losses, and $\eta_{constantVds}$ is the efficiency of the PA for constant drain bias and varying input power. The conclusion presented in Fig. 3.7 is that the average efficiency is increased by a factor of 1.46 when efficient dynamic biasing is used in the feedback loop of an efficient PA, assuming a uniform power probability distribution. The effect would be more dramatic for a low-efficiency PA and for signals which have more occurrences of lower power levels. For any other probability density function of power distribution, the

corresponding improvement can be calculated from the curves in Fig. 3.7.

3.3 Dynamic biasing applied to PA with DHBT and PHEMT devices

Using same procedure, class-E PAs are designed using InP DHBT from *Northrop-Grumman Space Technology* (NGST) and GaAs PHEMT from *Raytheon*[27]. These two PAs are designed by Srdjan Pajić and their details can be found in [27]. The efficiency improvement through dynamic biasing for the PAs are calculated from related measurements(not considering loss in the surrounding circuitry). Fig. 3.8 shows the results



(a) (b)

Figure 3.8: The calculated efficiency of the PA made with DHBT and PHEMT under power control through dynamic bias: (a)DHBT; (b)PHEMT.

for the two amplifier under dynamic biasing for output power control. The average efficiency under uniform distribution assumption for DHBT is 41.3% with constant collector bias voltage and 70.0% with dyanamic biasing; for PHEMT is the values are 49.3% and 67.8%.

3.4 Conclusion

This chapter presents a 10-GHz MESFET, DHBT and PHEMT class-E power amplifier with a dynamic drain bias control that allows efficient operation over a range of

output power levels. Drain efficiency of the MESFET PA, when averaged over the output power range, is increased from 41.5% to 60%, including the losses in the adaptive DC-DC converter. The MESFET PA includes a coupler/detector self-assessment circuit at the output port, and is pre-characterized to provide a reference voltage function for bias optimization. It is relevant to compare the heat dissipation for the PA with and without dynamic bias control. For a uniform probability distribution function of the output power in the given range, the constant-drain bias PA dissipates on average 88mW, while the dynamically-biased PA dissipates 45 mW, or around a factor of 2 less. This work demonstrates one possible optimization process using dynamic biasing, namely maintaining high efficiency over a range of output powers. Clearly, for applications that require very high linearity (e.g., CDMA), this highly compressed PA mode is not suitable. The method however is quite general, and other power amplifier improvements are gate bias control for temperature stabilization, bias control for increasing average efficiency for input signals with varying envelopes, and bias control for linearity.

Chapter 4

Linearity of Class-E Power Amplifiers in EER Operation

High-efficiency class-E power amplifiers can accomplish ultra-high efficiencies by driving the transistor as a switch [12, 31]. Since the transistor is driven into deep saturation, these amplifiers exhibit high nonlinearities and are not useful for some types of signal modulations [22]. For multifunctional systems where power is the prime resource, a high-efficiency transmitter with linearity that adapts to the input signal type has the potential of significant power savings over time. This chapter presents systematic nonlinearity characterization of X-band class-E PAs, with the goal of using adaptive fast and slow bias control for improving linearity, as will be discussed next chapter.

4.1 EER and lineartity of class-E PA in EER mode

Dynamic biasing can be used for efficiency improvement as shown in the previous chapter, but also for linearization of highly saturated efficient PA, such as in the Envelope Elimination and Restoration (EER) technique. EER technique was first brought up by Kahn [20] in 1952. In EER technique, the input signal is characterized as simultaneous amplitude and phase modulated signal and the signal is separated into phase modulated signal and low frequency amplitude modulated signal. The drive contains only phase information with a constant amplitude, while the amplitude information is provided through the bias, thus restoring the envelope information at the output. A block diagram of the EER concept is shown in Fig. 4.1.

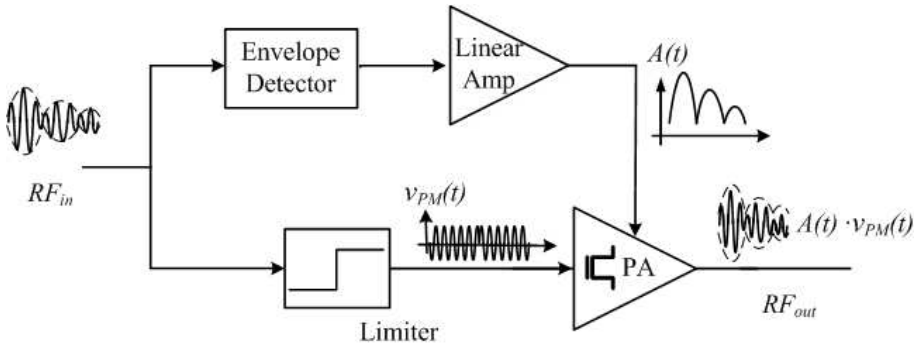


Figure 4.1: Schematic of EER operation concept. The input signal is separated into two branches. Amplitude of the input signal is extracted and amplified by low-frequency linear amplifier and used for biasing the PA. The phase-modulated constant-amplitude signal directly go through the PA. At the output the two signal recombine and original signal is amplified.

A number of authors have demonstrated EER transmitters at lower frequencies, e.g., an EER transmitter for HF/VHF is demonstrated in [21] where a class-D PA at 3.5 MHz with a class-S modulator is used. The system efficiency is about 60% and a two-tone IMD3 (3rd order intermodulation distortion) of better than −40 dBc is achieved with the envelope detector as a major source of nonlinearity. In [32], the effect of envelope modulator bandwidth and time delay between the envelope and phase signal on the linearity is studied theoretically. An attempt to limit the feedthrough, another cause of nonlinearity, by modulating the input signal drive improves both efficiency and linearity, is shown in [33], while [34] theoretically analyzes the effect of load network and RF choke on the linearity.

Limited work has been done in EER at microwave frequencies. For example, in [22] the efficiency and linearity behavior of a 8.4-GHz class-F PA is studied for both general linear mode (with constant biasing) and EER mode, for different manually controlled drain bias schemes. An IMD3 ratio of −27 dBc with a time-average efficiency for a multi-carrier signal with 10-dB peak-to-average ratio of 44% is obtained for a modified EER mode. This is a factor of 4.4 improvement over a 10% efficient backed-off class-A PA with the same IMD3 ratio, using the same device.

The class-E switched mode amplifier naturally lends itself to EER, as shown in Eq. (2.36) the output voltage is linearly proportional to the drain bias. This in turn means that control of the drain bias according to the envelope of the input signal accomplishes envelope amplification.

For operation in EER mode, the linearity of the class-E PA is characterized by considering the drain bias as the input signal amplitude. In this context, the AM-AM conversion is measured as the increase in output voltage when the drain bias is increased linearly and measured AM-AM and AM-PM characteristics are shown in Fig. 4.2 for high (14.2 dBm) and low (1.1 dBm) input power level. When the drain bias is 5 V, the small-signal gain of the PA in general linear mode is about 9 dB at an input power of 1.1 dBm, and saturates at 6.5 dB for the high input power of 14.2 dBm. For high input power, the PA output voltage varies linearly with drain bias (solid line) and when the input power is reduced, the PA AM-AM characteristics are no longer linear, since class-E PAs are designed to operate with high input power. This is consistent with the approach shown in Fig. 4.1 where the level of the input signal to the PA is kept at a constant high level. Another feature in Fig. 4.2 is existence of an output voltage with zero drain bias, referred to as feedthrough, which introduces distortion in signals that have envelope zero crossings. For AM-PM conversion, the relative phase between input and output signals of the PA is measured for a linearly increasing drain bias. The class-E PA shows considerable AM-PM conversion for low levels of drain bias, introducing again distortion for signals with envelope zero-crossings.

4.2 Two-tone measurement of class-E PA in EER mode

Another important measure of linearity, the intermodulation distortion, is usually measured using a two-tone test [35]. Two signals with same amplitude and certain frequency offset (f_1, f_2) are sent through the PA and at the output harmonic regrowth is examined as an indication of nonlinearity. The third and fifth order intermodulation

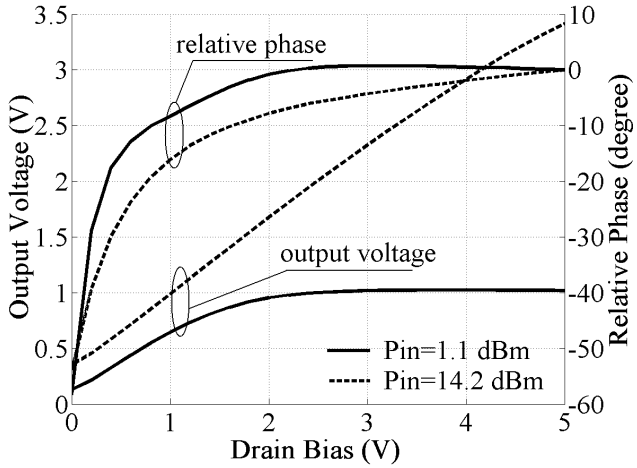


Figure 4.2: Measured AM-AM and AM-PM characteristics of the class-E PA with the amplitude modulation through the drain bias. The solid line is the result for a low (1.1 dBm) input signal, while the dashed line corresponds to a high input power level of 14.2 dBm when the output power is the maximum 20.6 dBm.

products, which are at frequencies $2f_1 - f_2$, $2f_2 - f_1$ and $3f_1 - 2f_2$, $3f_2 - 2f_2$, are of most interest and they are referred as upper and lower side IM3 and IM5, and their offset from the fundamental two tones are noted by upper and lower side IMD3 and IMD5. Here presents two types of two-tone measurements for frequency spacing of 1 MHz: standard measurement for PA at a constant drain bias of 4.2 V with two-tone test signals at 9.9995 and 10.0005 GHz, and a two-tone test for the PA in EER mode.

4.2.1 Two-tone measurement

The way two-tone test is carried out in EER operation needs some explanation. In a two-tone test ($f_2 > f_1$), the input signal is

$$\begin{aligned} v(t) &= A\cos(2\pi f_1 t) + A\cos(2\pi f_2 t) \\ &= 2A\cos(2\pi\frac{f_1+f_2}{2}t)\cos(2\pi\frac{f_2-f_1}{2}t) \end{aligned} \tag{4.1}$$

The signal can be written in following form as both AM and PM modulated signal,

$$\begin{aligned} v(t) &= 2A\left|\cos(2\pi\frac{f_2-f_1}{2}t)\right|\cos\left[2\pi\frac{f_1+f_2}{2}t+\phi(t)\right] \\ &= 2A\left|\cos(2\pi\frac{f_m}{2}t)\right|\cos\left[2\pi f_c t+\phi(t)\right] \\ &= A(t)v_{PM}(t) \end{aligned} \tag{4.2}$$

where f_c is the center frequency, f_m is the spacing between the two tones and are 10 GHz and 1 MHz respectively. In the context of modulation, f_c is the carrier frequency and f_m is the modulation frequency. $A(t)$ is the amplitude modulation signal which is a rectified sinusoidal with frequency of f_m and $\phi(t)$ alternates from 0 to π at half the frequency. Referring to the EER schematic in Fig 4.1, $A(t)$ modulates the drain bias of the PA and the phase modulated signal $v_{PM}(t)$ is the input to the PA.

4.2.2 EER two-tone measurement setup

Fig. 4.3 demonstrates a full implementation of an X-band EER transmitter. Efficient wide-band envelope tracking is designed by Vahid Yousefzadeh [36, 19], which

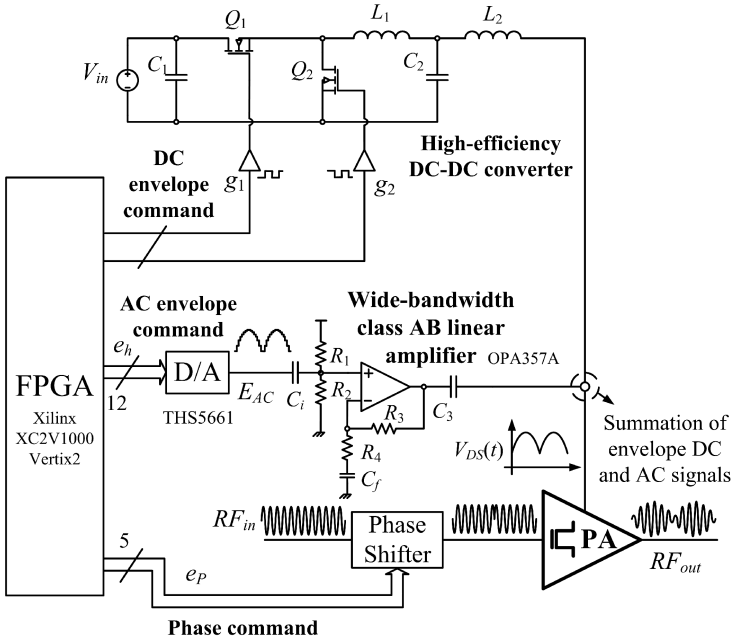


Figure 4.3: Block diagram of the EER system with FPGA bias control. The RF PA is a class-E 10-GHz MESFET amplifier. The envelope signal is split into a DC component which controls the DC-DC synchronous Buck converter and an AC component which provides envelope AC variations. The phase of the signal provides control of the phase of the carrier input to the PA through a X-band digitally-controlled phase shifter.

is required in the EER scheme, is achieved through a combination of a switched-mode power converter and a linear class-AB amplifier (OPA357A). Similar combined switching/linear amplifiers have been reported for audio applications [37] and for EER transmitters [38, 39]. The digital PA system controller is constructed using a Xilinx Virtex-II V2MB1000 FPGA. The system controller allows the flexibility of generating arbitrary look-up table based periodic envelope and phase waveforms for testing the PA. In this test setup we have not considered generation of arbitrary complex modulation signals. The DC portion of the envelope signal is provided through an efficient synchronous Buck DC-DC switching converter. Referring to the measurement setup in Fig 4.3, $A(t)$ and $\phi(t)$ are controlled by the envelope command signal e_h and the phase command signal e_P. $A(t)$ becomes the drain bias voltage, $V_{DS}(t)$, which is shown in Fig. 4.4 along with the phase control signal of the input RF signal for two-tone case. When the relative

time delay between those two signals changes between $\Delta t = 0$ and $\Delta t = 1/(2f_m)$, the alignment of the waveforms in time domain changes from synchronous to asynchronous. We refer to these conditions as "in phase" and "out of phase", respectively. In the experiments presented here, $f_c = 10\,\text{GHz}$ and $f_m = 1\,\text{MHz}$. The power switches Q_1 and Q_2 in the DC-DC converter are controlled by the complementary gate-drive signals g_1 and g_2 generated by the FPGA controller [30]. The duty cycle of Q_1 adjusts the DC value of the envelope signal. The AC portion E_{AC} of the envelope signal is generated by the FPGA through the THS5661 12-bit 100 MSPS D/A converter. The AC portion is then buffered and amplified by a wide-band class-AB amplifier, constructed around the OPA357 op-amp. The DC and AC signals are coupled through the inductor L_2 and capacitor C_3 to obtain the supply voltage $V_{DS}(t)$ for the class-E PA. The phase of the RF input signal for the PA is controlled by a TriQuint TGP6336-EEU 5-bit X-band digitally-controlled phase shifter. The phase shifter has around 9 dB loss, requiring a pre-amplifier at the input (not shown for clarity).

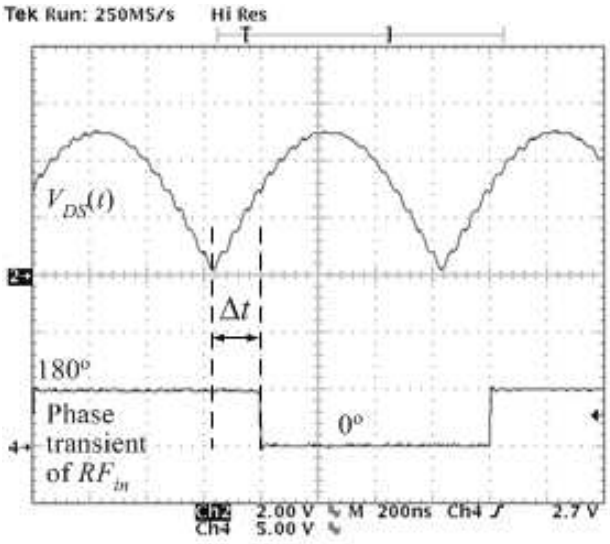


Figure 4.4: Generated drain bias and phase of the input RF signal for two-tone test of the PA in EER mode. Δt is the time delay between the two signal.

4.2.3 Two-tone characterization of PA in general linear mode

We present two types of two-tone measurements for frequency spacing of 1 MHz: the standard measurement for a PA at a constant drain bias of 4.2 V with two-tone test signals at 9.9995 and 10.0005 GHz, and a two-tone test for the PA in EER mode. The measurements are compared to nonlinear harmonic-balance Agilent ADS simulations with a TOM (TriQuint's Own Model) nonlinear model [40] for the MESFET (provided by the manufacturer). Fig. 4.5 shows the level of intermodulation product vs. input power at a drain bias of 4.2 V. As expected, the class-E PA has poor linearity: at an input power of 14 dBm, the IMD3 is around −10 dBc, while the IMD5 (fifth order intermodulation product) is about −25 dBc. The figure also shows an asymmetry in the upper and lower intermodulation sideband, commonly observed in RF PAs and attributed to memory effects [35], which will be discussed more in Chapter 5.

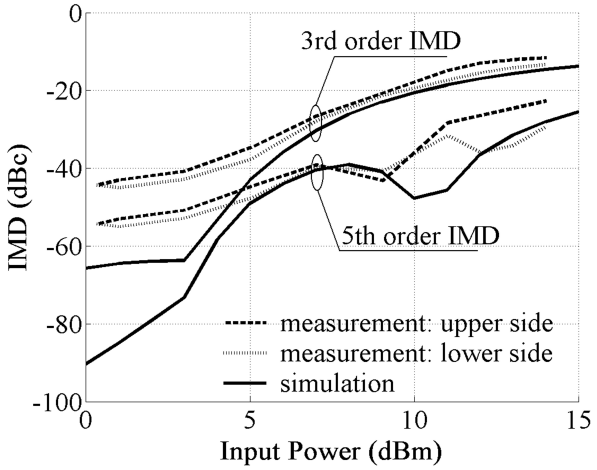


Figure 4.5: Measured and simulated two-tone test of the class-E PA. IMD3 and IMD5 as a function of input power. The "upper and lower side" labels refer to the sidebands produced by the two-tone test.

4.2.4 Two-tone characterization of class-E PA in EER mode

Fig. 4.7 shows the measured bias dependence of the fundamental frequency output voltage, as well as the voltage of the third and fifth intermodulation products for a phase-

modulated signal, which is given previously as $v_{PM}(t) = \cos[2\pi f_c t + \phi(t)]$. All three voltages are approximately linearly dependent on the drain bias. This indicates that the EER mode of operation can linearize the PA to some extent.

Fig. 4.6 shows normalized output spectrum of EER two-tone test. The input signal power is 13 dBm. The upper and lower side IMD3 are -25.4 dBc, -20.7 dBc; upper and lower side IMD5 are -27.0 dBc and -25.4 dBc. The spurious signals in the spectrum, which are also present in the spectrum of phase modulated signal $v_{PM}(t)$, may be due to the transition of the phase between zero and π.

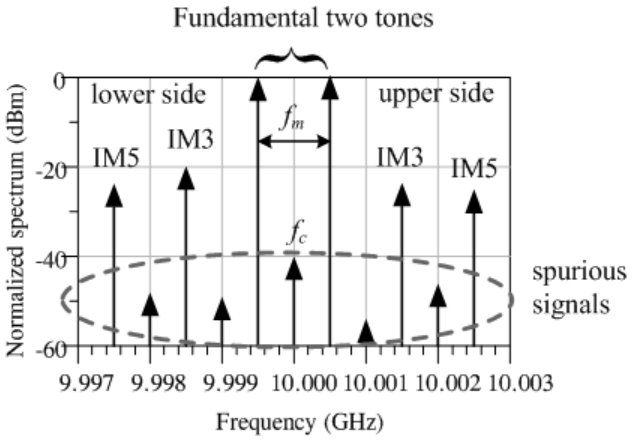


Figure 4.6: The normalized spectrum of the output signal from EER two-tone test. The values are normalized to the power of the fundamental two tones.

Fig. 4.8 shows the measured power of the fundamental and the 3rd and 5th intermodulation products as a function of input power to the PA, for $\Delta t = 0$ (in phase) and $\Delta t = 1/[2(f_2 - f_1)]$ (out of phase), respectively. The two sets of curves (solid and dashed lines) correspond to the upper and lower sidebands. As expected, the in-phase case shows a slower increase in intermodulation product power as the input power increases. The IMD3 and IMD5 for $\Delta t = 0$ (in phase) and $\Delta t = 1/(2f_m)$ (out of phase) are presented in Fig. 4.9 (a) and (b), respectively, and summarized as follows:

- For the in-phase case the measured IMD3 and IMD5 are -20 dBc and -25 dBc, respectively, where ideally no intermodulation products should be present.

- For the out-of-phase case the measured IMD3 and IMD5 are -3 dBc and -11 dBc, respectively. The calculated theoretical results (ideal class-E) for are IMD3 of 0 dBc and IMD5 of -9.5 dBc. The reason for the difference is attributed to nonlinearity caused by AM-PM, feedthrough and memory effects.

- Harmonic balance simulations of the IMD levels agree well with the measurements.

- For the in-phase case, with input power increase the IMD level decreases due to the dynamic biasing. This can also be understood by observing the results in Fig. 4.2.

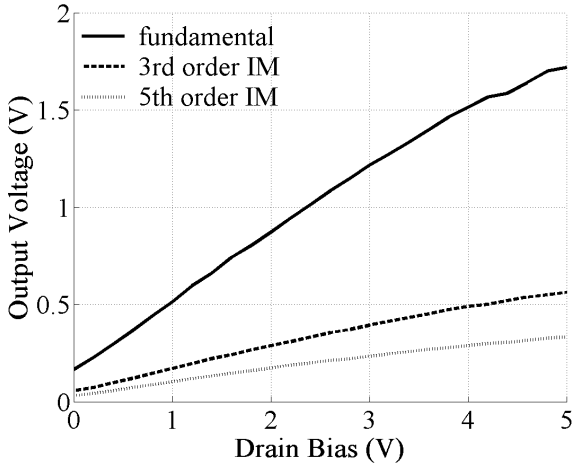


Figure 4.7: Measured intermodulation product level as a function of drain bias, for a phase-modulated input signal. The output voltage is calculated from the measured power across a 50-Ω load.

4.3 Frequency Response of PA in EER Mode

The results discussed so far are for single-frequency or narrowband operation. It is of interest to examine the behavior of the class-E EER mode over a range of frequencies around the class-E design frequency. The AM-AM of the class-E PA in EER mode, that is output voltage vs. the drain bias, is measured from 8 to 12 GHz.

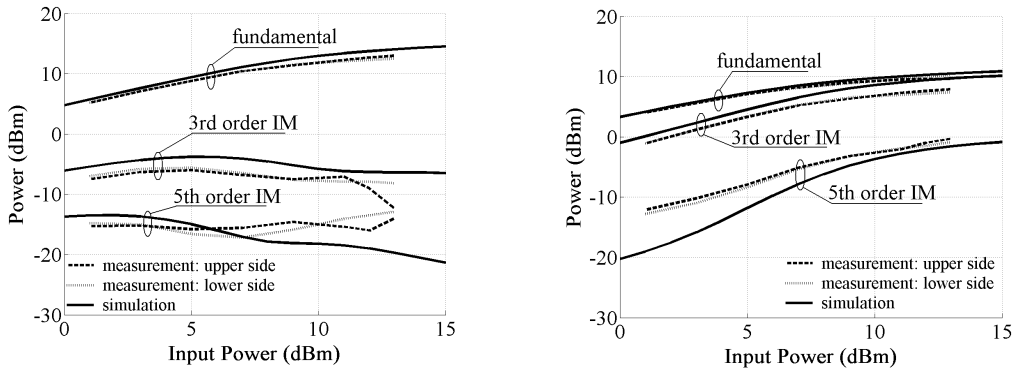


Figure 4.8: Measured power of the fundamental and the 3rd and 5th intermodulation products as a function of input power to the PA: (a)$\Delta t = 0$ (in phase) (b) $\Delta t = 1/\left[2(f_2 - f_1)\right]$ (out of phase). The three sets of curves correspond to the upper and lower sidebands and simulation results.

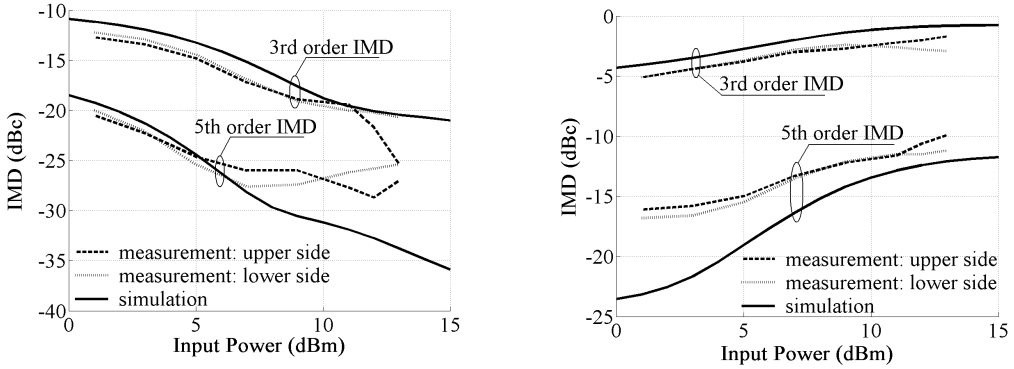


Figure 4.9: Measured power of the fundamental and the 3rd and 5th intermodulation products as a function of input power to the PA: (a)$\Delta t = 0$ (in phase) (b) $\Delta t = 1/\left[2(f_2 - f_1)\right]$ (out of phase). The three sets of curves correspond to the upper and lower sidebands and simulation results.

Fig. 4.10 shows the output voltage vs. drain bias for five different frequencies. When the frequency deviates from 10 GHz, the PA class of operation changes, resulting in degraded linearity. Typical class-E mode bandwidth is on the order of 10% (e.g., [31]) and is limited by the output matching network that provides harmonic termination and the optimal fundamental load for high efficiency operation. Fig. 4.11(a) and 4.11(b) show the frequency dependance of the quantity $P_{out}/(V_{ds}^2/2Z_o)$, which represents the ratio of the RF output power to the bias voltage across a 50-Ω load and drain efficiency.

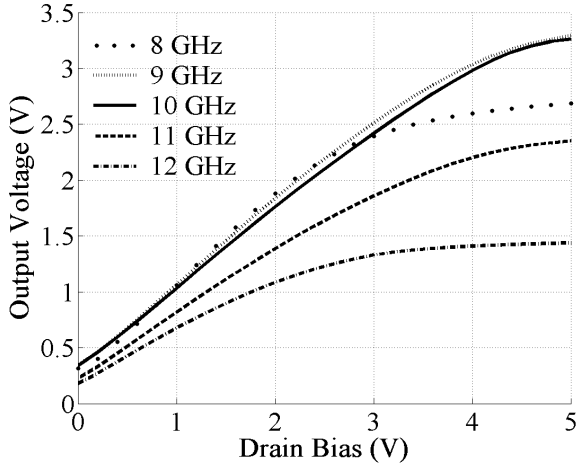


Figure 4.10: Measured output voltage (50-Ω load) as a function of drain bias (AM-AM) for different frequencies around the 10 GHz design frequency.

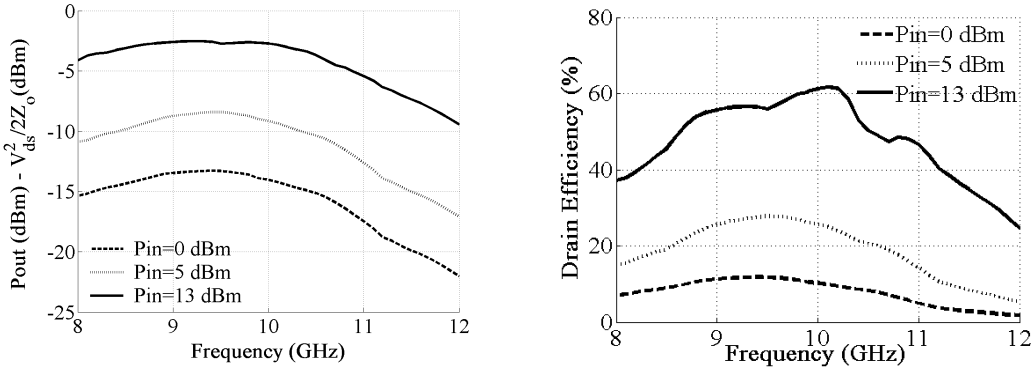


Figure 4.11: Frequency dependence of (a) the quantity $P_{out}/(V_{ds}^2/2Z_o)$, which represent the ratio of the RF output power to the bias voltage across 50-Ω load. (b) drain effiency

In this way, a 1-dB bandwidth for EER mode can be defined and is measured to be around 24% (8.1 to 10.5 GHz) and the 10% drain efficiency bandwidth is 15% (8.9 to 10.4 GHz).

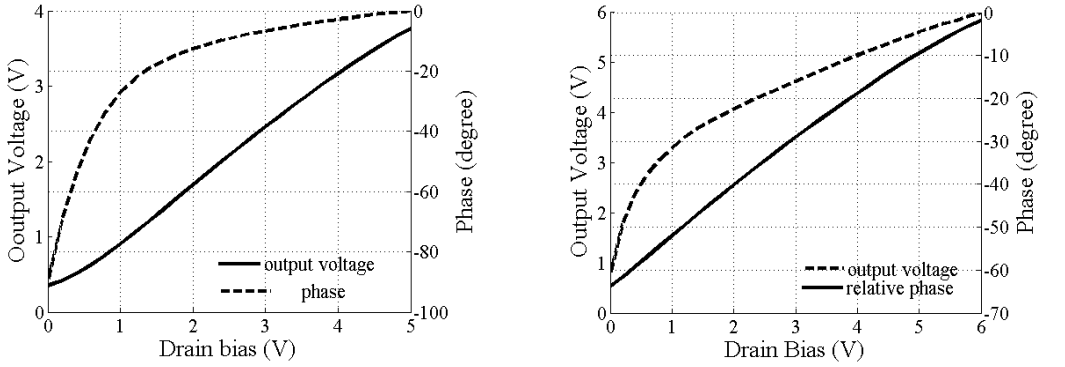
4.4 Comparison between DHBT and PHEMT

Dr. Srdjan Pajic [27] designed a class-E power amplifier using an InAlAs/InGaAs DHBT transistor from *Northrop Grumman Space Technologies*, and a AlGaAs/InGaAs/GaAs HEMT provided by *Raytheon*. They have similar dimensions and bias conditions. Design details and characterization of each PA are also shown in [27]. Here characterizations of these two PAs while operating in EER are shown to complete the comparison. The optimal operation conditions for the DHBT are collector bias of 4.35 V, base bias of 0.35 V and input power of 11 dBm. For the PHEMT a drain bias of 5.4 V, gate bias of -0.75 V and input power of 18 dBm are set. Fig. 4.12 shows the AM-AM and AM-PM behavior for the two devices. It is noticed that the ratio between output voltage and drain bias is higher for the PHEMT. This is partially due to a larger value of the output capacitor. The equivalent output capacitances of the DHBT and PHEMT are 0.19 pF and 0.25 pF respectively. According to Eq. 2.36 the gain is in inverse relationship with the real part of the optimal impedance R_1, and R_1 is in inverse relationship with output capacitance as in Eq. (2.30) and Eq. (2.14). The relationships are listed below for reference:

$$V_{out} = \sqrt{\frac{50}{R_1}} \frac{4}{\sqrt{4+\pi^2}} V_{DC}$$

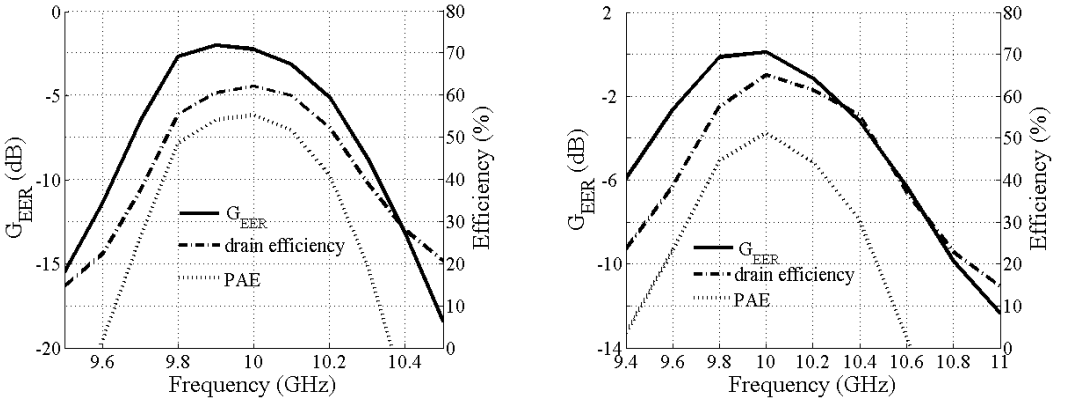
$$R_1 = \frac{R_{o1}}{\omega_o C_s} = 0.1836 \cdot \frac{1}{\omega_o \cdot C_s}$$

The bandwidth properties of the two PAs are shown in Fig. 4.13. In Fig. 4.13, G_{EER} is the conversion ratio between the drain bias voltage and output signal amplitude. In terms of power, G_{EER} can be expressed as $G_{EER} = P_{out}/(V_{ds}^2/2Z_o)$ with $Z_o = 50\,\Omega$. Maximum phase shift due to AM-PM conversion, feedthrough voltage, G_{EER} and its



(a) (b)

Figure 4.12: AM-AM and AM-PM for class-E PA designed using HBT and PHEMT device. (a) HBT. (b) PHEMT



(a) (b)

Figure 4.13: Bandwidth property of drain efficiency, PAE and G_{EER} of the class-E PA designed using HBT and PHEM devices. (a) HBT. (b) PHEMT.

respective 1-dB bandwidth, drain efficiency and its respective 10$\dot{\%}$ bandwidth of the class-E PA using three different devices are summerized in Table 4.1. The MESFET based class-E PA manifests maximum bandwidth and small feedthrough voltage; the DHBT PA has the maximum AM-PM conversion and the PHEMT PA has the maximum efficiency, G_{EER} and feedthrough voltage.

	PhaseShift (degree)	Feedthrough	G_{EER}(dB) /BW(GHz)	η_D(%) /BW(GHz)
MESFET	54.2	0.35	−2.7/2.4	61.2/1.5
DHBT	90.0	0.35	−2.2/0.3	62.1/0.4
PHEMT	61.2	0.51	0.1/0.5	65.0/0.5

Table 4.1: Maximum phase shift in AM-PM conversion, feedthrough voltage, G_{EER} and its respective 1-dB bandwidth, drain efficiency and its respective 10 % bandwidth of the class-E PA using MESFET, DHBT and PHEMT devices.

4.5 Intermodulation products vs. input power

It is well known that the power of the third order intermodulation product, IM3, for a linear PA has an approximate slope of 3:1 and the fifth order intermodulation product,IM5, has a slope of 5:1(on dB scale) when plotted vs. input power. Since the AM-AM property of the class-E PA shown in Fig. 4.2 follows similar trend to that of linear PAs, except for the considerable amount of feedthrough and much lower gain, it will be interesting to find out how intermodulation products (IM3, IM5) for class-E (in EER mode) vary as input power increases, assuming the same AM-AM conversion characteristic as in a linear PA. By expanding the output voltage in terms of input voltage up to the third order power series gives

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \tag{4.3}$$

For a single tone input, $A\sin(\omega_o t)$, the output signal amplitude $v_{out,s}$ is given as

$$v_{out,s} = a_1 A \sin(\omega_o t) \tag{4.4}$$

which is true for EER operation also. For a linear PA with a two-tone input ω_1, ω_2, the third-order intermodulation product $v_{out,IM3}$ is [41]

$$v_{out,IM3} = \frac{3}{4} a_3 A^3 \cos((2\omega_1 - \omega_2)t) \tag{4.5}$$

Since $v_{out,IM3}$ is proportional to the cube of the input signal amplitude, IM3 vs. input power (in db) has a slope of 3:1, while the fundamental signal has a slope of 1:1. When

expanded the output voltage to 5th order, the IM5 will appear in the output with amplitude [41]

$$v_{out,IM3} = \frac{5}{8} a_5 A^5 \cos((3\omega_1 - 2\omega_2)t) \tag{4.6}$$

So, the power of IM5 has a slope of 5:1 when plotted as a function of input power on a logarithmic scale.

In EER mode of operation, the input signal is separated into phase-modulated and amplitude-modulated signals. For a two-tone test, the input signal amplitude is a full-wave rectified sinusoid and its expression is $v_{in} = 2A\left|\cos(2\pi\frac{f_m}{2}t)\right|$. Substitute into Eq. (4.3), v_{out} is amplitude-modulating signal for the (0, π) phase-modulated signal at the output. The output signal is written as

$$v_{out,EER} = (a_1 2A|\cos(\omega_m t)| + a_2(2A|\cos(\omega_m t)|)^2 + a_3(2A|\cos(\omega_m t)|)^3)\cos(\omega_c t + \phi(t)) \tag{4.7}$$

where,

$$\phi(t) = \begin{cases} 1 & 2k\pi \le \frac{\omega_m}{2}t < (2k+1)\pi \\ 0 & (2k+1)\pi \le \frac{\omega_m}{2}t < 2(k+1)\pi \end{cases}$$

and $k = 0, 1, ...$

The Fourier series are calculated in Mathematica and the amplitude of the third-order and fifth-order intermodulation products are (the last term in each is neglected)

$$V_{out,EER,IM3} = \frac{16}{15\pi} a_2 A^2 + a_3 A^3 \tag{4.8a}$$

$$V_{out,EER,IM5} = \frac{16}{105\pi} a_2 A^2 \tag{4.8b}$$

In the power series, terms with a_2 dominates and IM3 and IM5 vs. input power both has a slope of 2:1, which is slower compared with linear PA case. In above calculations the effect of AM/PM is neglected, which is more serious in EER mode as the device is saturated.

The effects of AM-PM and feedthrough is not negligible in the class-E PA used. The class-E PA's AM-AM and AM-PM properties (PA used in Chapter 5, Fig. 5.4)

are polynomial approximated. The approximation is then used to calculated the IM products vs. input power. The polynomial approximations of the AM-AM and AM-PM of the PA are:

$$A_{AM}(v_{ds}) = 0.3316 + 0.6425v_{ds} + 0.0262v_{ds}^2 - 0.0063v_{ds}^3 \tag{4.9a}$$

$$\phi_{PM}(v_{ds}) = -53.14 + 73.17v_{ds} - 50.58v_{ds}^2 + 18.00v_{ds}^3 - 3.10v_{ds}^4 + 0.21v_{ds}^5 \tag{4.9b}$$

The approximation almost exactly overlap with the AM-AM and AM-PM curve when $v_{ds} < 5\,\mathrm{V}$. For rectified sinusoidal waveform whose maximum value less than 5 V, the calculated IMD3 and IMD5 are plotted in Fig. 4.14. Due to the effects of the feedthrough

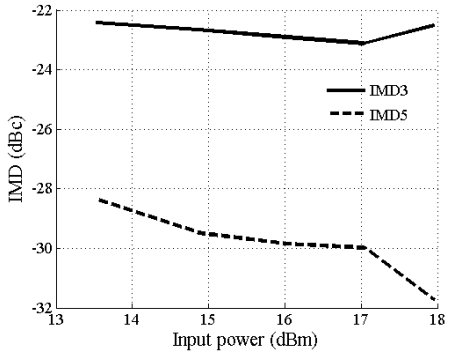


Figure 4.14: Intermodulation products, IMD3 and IMD5, vs. input power calculated from AM-AM and AM-PM polynomial approximation

and AM-PM, the 2:1 curve is not obtained. The IMDs actually fluctuates with the input power. This may due to the fact that as input power increase, that is as the rectified sinusoidal signal increase, the effect of feedthrough will decrease, but the effect of phase distortion, gain flattening will increase.

4.6 Conclusion

In summary, this chapter presents linearity characterization of highly-saturated high-efficiency class-E X-band PAs operating in EER technique. It is shown both experimentally and in simulations that the EER mode with dynamic biasing of the PA can

improve linearity significantly. Harmonic balance simulations are shown to be useful for design that includes linearity considerations. The results in this chapter demonstrate the possibility of more generally adaptive PAs. Any input signal can be presented in baseband in polar instead of I/Q form, allowing nonlinear PAs to be used when linearity is a requirement. In addition, the FPGA in Fig. 4.3 can be used for basedband predistortion, which is the topic of next chapter.

Chapter 5

Baseband Predistortion of Class-E PA in EER Mode

Two-tone testing of class-E PA in EER mode from previous chapter showed that the requirement of an IMD level of -30 dBc was not met. Linearity can be improved without sacrificing too much efficiency by employing a linearization technique. The three main types of linearization techniques are feedforward, feedback and predistortion. In Table 5.1 these three linearization techniques are compared [1]. In the feedforward technique, a delayed sample of the input signal is compared with correctly attenuated sample of the output signal. The signal difference is amplified appropriately and subtracted from the output signal. The feedforward technique has good linearity, bandwidth and stability, but poor efficiency and complex circuitry [41]. In the feedback technique, the envelopes of the input and output signals are compared and the gain of the amplifier is adjusted to minimize the difference [41]. Table 5.1 shows that predistortion is the optimal choice considering efficiency and size. It offers medium performance for nonlinearity cancellation and bandwidth. With increasing capabilities of DSP technology, baseband digital predistortion becomes increasingly common. In this chapter, lookup table (LUT) based digital baseband predistortion is used for the linearization of a X-band class-E PA in EER operation.

technique	cancellation performance	band-width	PAE	size
feedback	good	narrow	medium	medium
feedforward	good	wide	low	large
predistortion	medium	medium	high	small

Table 5.1: Relative comparsion of the linearization performance of feedback, feedforward and predistortion techniques [1].

5.1 Digital baseband predistortion of class-E PA in EER mode

The basic idea of predistortion can be explained as follows: the input signal is distorted in a complimentary manner to the PA distortion characteristics before being amplified by the PA. The distortion introduced by the PA cancels with the distortion from predistorter and the original signal is linearly amplified. The circuit providing the complementary distortion is called a predistorter. Fig. 5.1(a) shows the concept of predistortion, with the predistorter in front of the PA. The relationship between the transfer functions of the predistorter and PA is

$$V_{out} = F\big(G(V_{in})\big) = A \cdot V_{in}$$

where A is the desired gain of the PA. Fig. 5.1(b) shows the relationship between transfer functions of the PA, predistorter and total system more intuitively. When the signal is predistored before being modulated or upconverted, the predistortion technique is called baseband predistortion. Baseband predistortion is mostly carried out with digital circuits since it is at a lower frequency. The cancellation effect of the nonlinearity can be improved further by tracking the PA changes and updating the predistorter based on output signal sensed by the feedback loop. Successful linearity improvements through baseband digital predistortion for various wireless modulation schemes have been shown by a number of references. Faulkner et al. [42] used lookup table (LUT) based adaptive predistorter to correct for the amplitude and phase of a class-C PA operating at 900 MHz and obtain 30 dB reduction in IMD3. Kim et al. [43] used LUT

based baseband predistortion with adaptive feedback loop improved out-of-band spectra by 15 dB for a LDMOS PA opearating at 880 MHz with CDMA2000 modulated signal as the input. Several aspects of predistortion, such as LUT indexing [44], memory effects correction [45] and other circuit element optimizations [46] attracted considerable research interest.

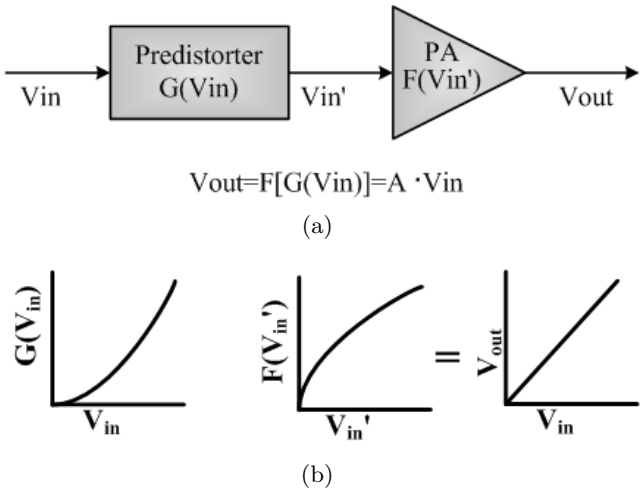


Figure 5.1: (a) The concept of predistortion. The predistorter distorts the input signal in a way complementary to the distortion of the PA. (b) An illustration of the transfer function of predistorter, PA and final linearized system.

Published works showed application of digital baseband predistortion for linearization of class-E PAs in EER mode. The AM-PM conversion of a class-E PA is serious since the device is saturated. Sowlati et al. [47] used a phase-correcting feedback loop to predistort the phase of the input signal and eliminate the AM-PM distortion. The phase of the output and input signal with certain delay is compared and the phase error signal is used for control of phase shifter to predistort the phase of the input signal. The AM-PM is corrected from about 30 degrees to 4 degrees at 835 MHz and met the requirement of the North American Digital Celluar standard. Reynaert et al. [48] presented a fully integrated CMOS class-E PA at 1.75 GHz with polar predistortion and met the Class E3 EDGE requirements concerning output power, EVM and spectral mask. With linearization, the PA's efficiency is over 40 % for the output power range.

The efficiency of the whole system is 30 %. Wang et al. [49] designed a silicon bipolar class-E PA for application in WLAN 802.11g. Operating in EER and with baseband predistortion as well as adaptive time alignment the PAE of the whole system achieved PAE of 28 %, which doubled that of the class AB amplifier.

The block diagram of baseband LUT based polar predistortion for EER used in this chapter is shown in Fig. 5.2. The LUT is uniformly indexed by the input signal amplitude. LUT is constructed based on the AM-AM and AM-PM of the PA and is the predistorter. The feedback loop for adaptively updating the LUT is shown but not used in this work.

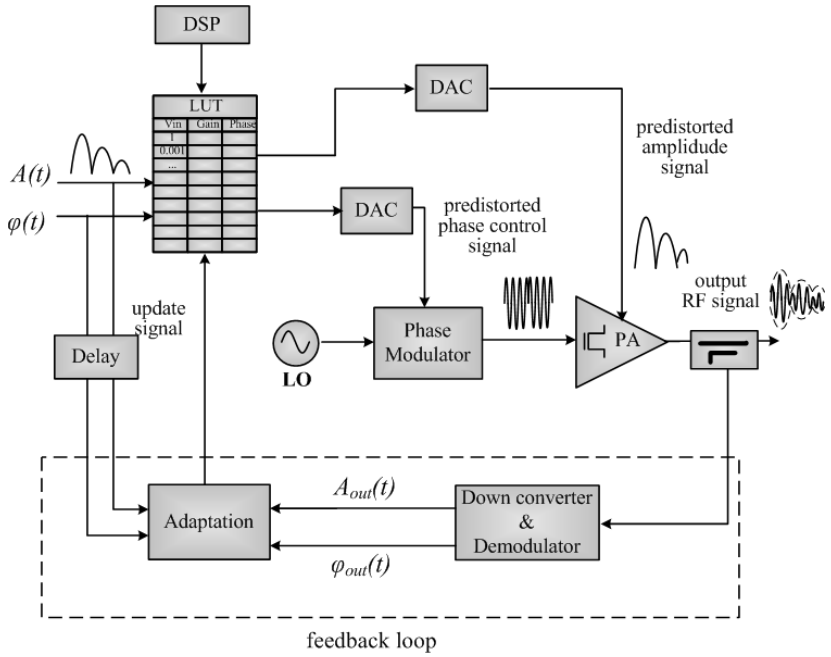


Figure 5.2: Schematic of polar baseband predistortion in EER technique.

5.2 Experimental results

The schematic of the setup is the same as shown in Fig. 4.1 in the previous chapter. In the measurement LUT is programmed on a FPGA chip. The phase shifter is an analog phase shifter HMC538LP4 from *Hittite Microwave Corporation* with modu-

lation bandwidth of 50 MHz. The phase shifter is characterized in Fig. 5.3 showing the dependence of relative phase shift on the control voltage, which is approximately linear. Phase shift of 180 degrees can be obtained with voltage difference of 1 V and insertion loss variation within 1 dB. The predistortions are tested at frequency spacing of 20 kHz, 200 kHz, 625 kHz and 1 MHz. The size of the LUT or number of samples per period is determined by the sampling frequency, which is limited by the D/A converter, and two-tone spacing.

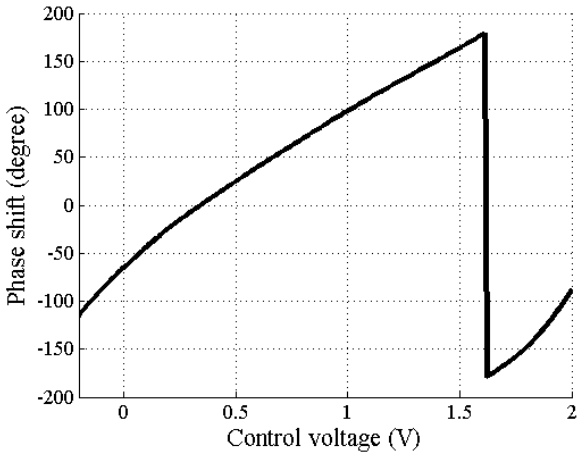


Figure 5.3: The characterization of the phase shift vs. control voltage of phase shifter HMC538LP4 from *Hittite Microwave Corporation* at 10 GHz.

The LUT is formulated based on the statically measured AM-AM and AM-PM properties of the PA. Since a slightly different PA from that in Chapter 4 (same device) is used, the conversion characteristics are shown in Fig. 5.4. A rectified sinusoid signal with a maximum value of 4.5 V is chosen for the drain bias of the EER two-tone signal considering the optimal and maximum bias condition of the PA. Based on the AM-AM and AM-PM properties of the PA and setting the desired ratio between the output voltage and drain bias to be 0.7, the required original (non-predistored) and predistorted drain bias and phase shifter control voltages are shown in Fig. 5.5. In the calculation of the phase shifter control voltage, the phase shifter conversion characteristic shown in

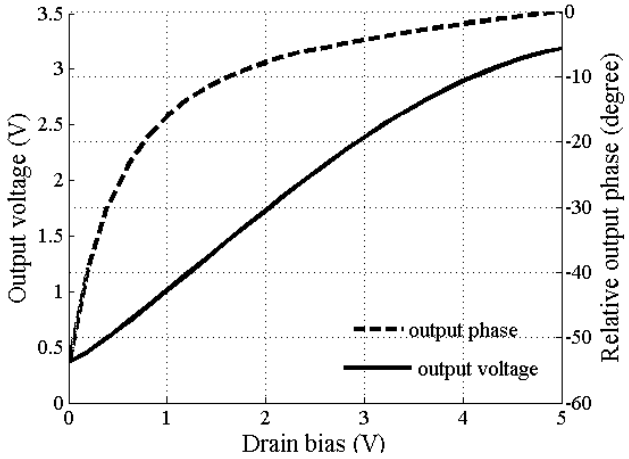
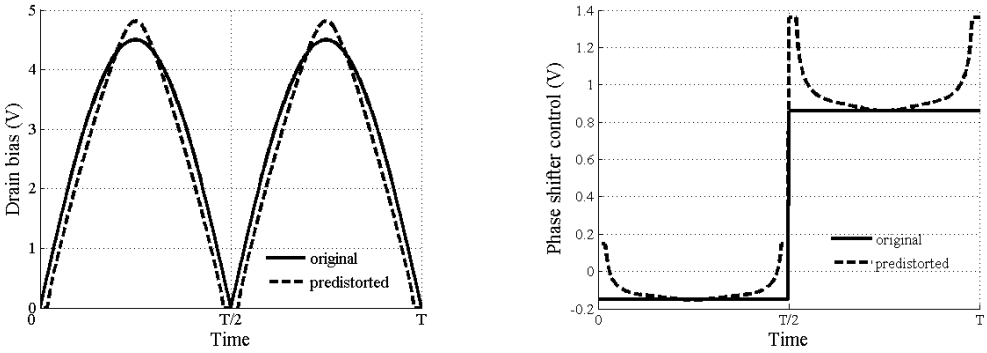


Figure 5.4: The AM-AM and AM-PM conversion characteristic of the PA

Fig. 5.3 is taken into account. Feedthrough, existance of output power when drain is



(a) (b)

Figure 5.5: Original and desired predistorted drain bias and phase control voltage. One period is $T = 2/f_m$, where f_m is the frequency spacing of the two tones. The predistortion is designed for voltage gain (ratio of output voltage and drain bias) of 0.7.

biased at zero V, cannot be corrected by predistortion alone. When the output voltage needs to be corrected to a value less than the feedthrough voltage (0.36 V based on Fig. 5.4) , the drain bias is set to 0 V. So, the waveform of the predistorted drain bias is flat and equals to zero for small portions of the period.

5.2.1 Predistortion at two-tone frequency spacing of 20 kHz

For a two-tone frequency spacing of 20 kHz, each period of the rectified sinusoid has 623 samples. The measured drain voltage and phase shifter control voltage are shown in Fig. 5.6 for both the original and predistorted case. The spectra with and

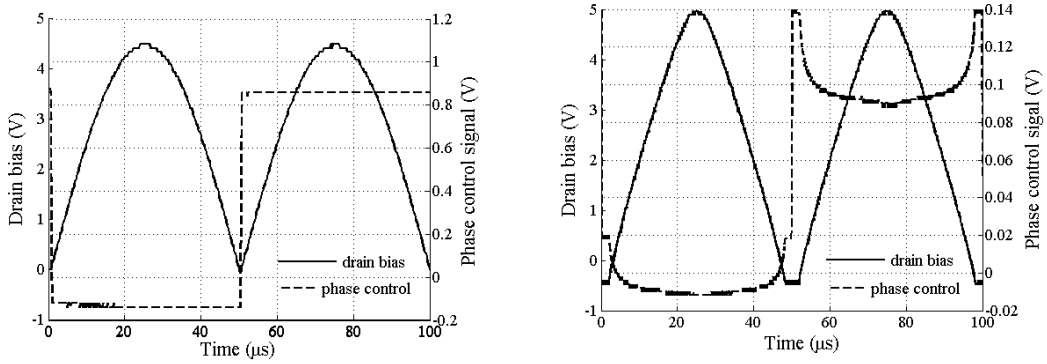


Figure 5.6: Original and desired predistorted drain bias and phase control voltages for EER two-tone spacing of 20 kHz. (a) Original drain bias and phase shifter control signal. The maximum value of drain bias is 4.5V. (b) Predistorted drain bias and phase shifter control signal.

without predistortion are shown in Fig. 5.7. The IMD3 is improved by over 10 dB from

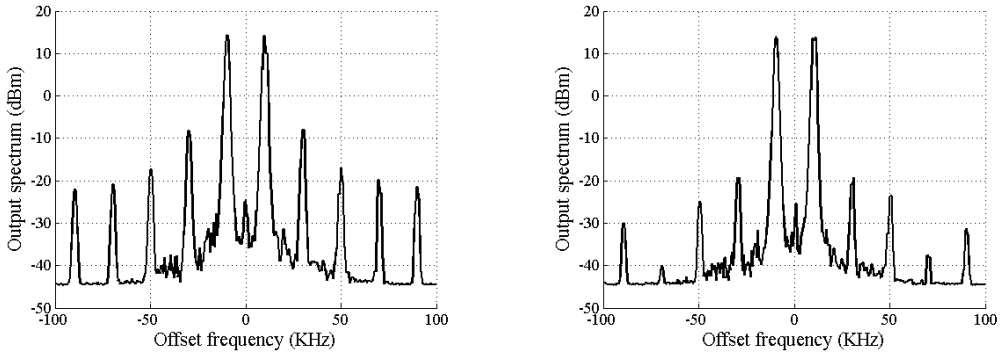
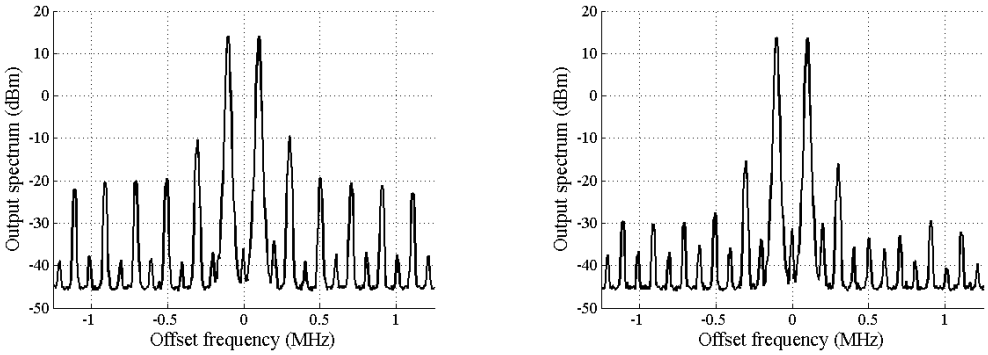


Figure 5.7: Spectrum of (a) original and (b) predistorted EER two-tone test. The two-tone spacing is 20 kHz.

-22.5 dBc to -33.2 dBc and met the requirement of IMD3 level of -30 dBc. The IMD5 is improved from -31.6 dBc to -38.8 dBc.

5.2.2 Predistortion at two-tone frequency spacing of 200 kHz

At two-tone spacing of 200 kHz, 124 samples are used in each period of the rectified sinusoid. The original and predistorted spectra are shown in Fig. 5.8.



(a) (b)

Figure 5.8: Spectrum of (a) original and (b) predistorted EER two-tone test. The two-tone spacing is 200 KHz.

Asymmetry exists in both the original spectrum and the predistorted spectrum. Predistortion improved the linearity but the IMDs levels are over -30 dBc. The IMD values and improvements are listed in Table 5.2.

5.2.3 Predistortion at two-tone frequency spacing of 625 kHz

At two-tone spacing of 625 kHz, the original and predistorted spectra are shown in Fig. 5.9. There are 40 samples in in each period of the rectified sinusoid.

Asymmetry becomes more serious in the spectrum and IMD improvements also decrease. The IMD values and improvements are listed in Table 5.3.

5.2.4 Predistortion at two-tone frequency spacing of 1 MHz

At two-tone spacing of 1 MHz, the original and predistorted spectra are shown in Fig. 5.10. There are 25 samples in each period of rectified sinusoid.

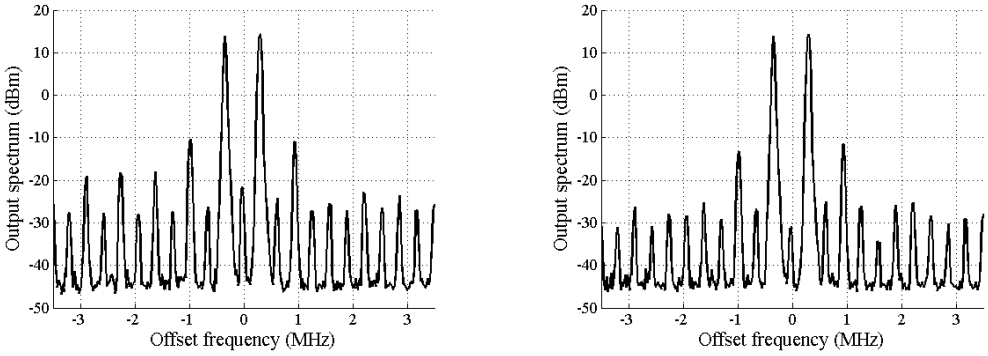
Asymmetry becomes more serious in the spectrum. Predistortion improved the

	$IMD3_L$	$IMD3_U$	$IMD5_L$	$IMD5_U$
org. (dBc)	−24.30	−23.61	−33.41	−33.64
pred. (dBc)	−28.85	−29.77	−41.25	−47.32
impr. (dB)	4.55	6.16	7.84	13.68

Table 5.2: IMD values in EER two-tone test with frequency spacing of 200 kHz. In the table, 'org.' represents two-tone test with no predistortion; 'pred.' represents predistortion and 'impr.' is the improvement due to predistortion.

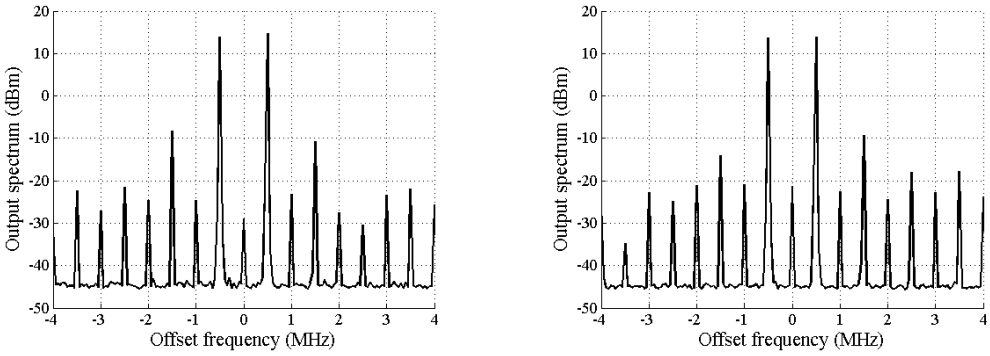
	$IMD3_L$	$IMD3_U$	$IMD5_L$	$IMD5_U$
org. (dBc)	−24.23	−25.35	−31.86	−40.31
pred. (dBc)	−27.12	−25.82	−39.12	−48.6
impr. (dB)	2.89	0.47	7.26	8.29

Table 5.3: IMD values in EER two-tone test with frequency spacing of 625 kHz. In the table, 'org.' represents two-tone test with no predistortion; 'pred.' represents predistortion and 'impr.' is the improvement due to predistortion.



(a) (b)

Figure 5.9: Spectrum of (a) original and (b) predistorted EER two-tone test. The two-tone spacing is 625 KHz.



(a) (b)

Figure 5.10: Spectrum of (a) original and (b) predistorted EER two-tone test. The two-tone spacing is 1 MHz.

lower-side IMD but the IMD in the upper side is now worse. The IMD values and improvements are listed in Table 5.4.

5.2.5 Discussion

Table 5.5 lists the IMD values for the above measured predistorted EER two-tone test. The -30 dBc is only achieved at frequency spacing of 20 KHz. As frequency spacing increases, asymmetry becomes more obvious and improvement deteriorates.

In Chapter 4, section 4.5 the intermodulation distortion vs. input power is cal-

	$IMD3_L$	$IMD3_U$	$IMD5_L$	$IMD5_U$
org. (dBc)	−22.24	−25.50	−35.49	−45.15
pred. (dBc)	−27.61	−23.17	−38.51	−31.98
impr. (dB)	5.37	−2.33	3.02	−13.17

Table 5.4: IMD values in EER two-tone test with frequency spacing of 1 MHz. In the table, 'org.' represents two-tone test with no predistortion; 'pred.' represents predistortion and 'impr.' is the improvement due to predistortion.

	$IMD3_L$	$IMD3_U$	$IMD5_L$	$IMD5_U$
20 KHz (dBc)	−33.17	−32.91	−38.81	−37.2
200 KHz (dBc)	−28.85	−29.77	−41.25	−47.32
625 KHz (dBc)	−27.12	−25.82	−39.12	−48.6
1 MHz (dBc)	−27.61	−23.17	−38.51	−31.98

Table 5.5: Lower and upper side IMD3 and IMD5 values in EER two-tone test after predistortion at four different two-tone spacing.

culated based on the AM-AM and AM-PM property measured statically. To compare with the measurement in EER mode, IMD3 and IMD5 are measured for varying input power. In the EER scheme, as discussed before, the drain bias is the amplitude of the input signal. Following this argument, the power of a single tone at the input of the two-tone measurement is related to the maximum value of the rectified sinusoidal drain bias as:

$$P_{in} = 10\log\Big(\frac{(\frac{v_{ds,max}}{2})^2}{2R}1000\Big)$$

where, $v_{ds,max}$ is the maximum value of the drain bias voltage.

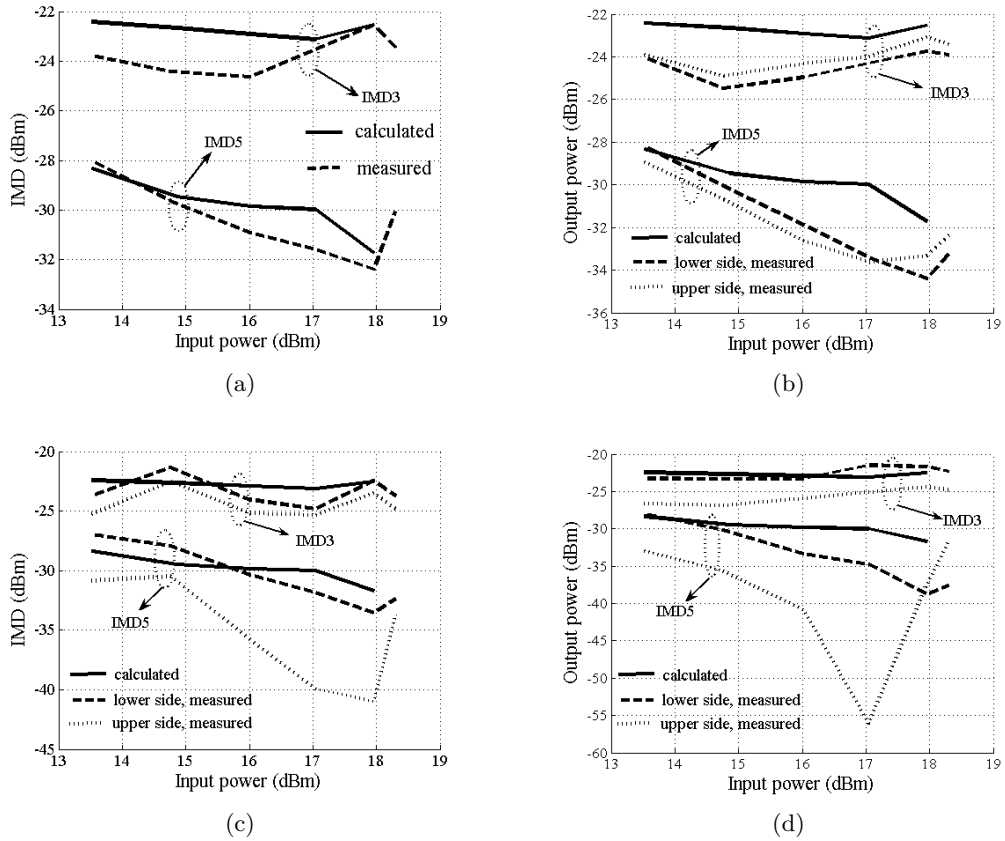


Figure 5.11: Intermodulation products, IMD3 and IMD5, vs. input power. Calculated values from Fig. 4.14 is shown with measured values at four different frequencies. (a) 20 kHz. (b) 200 kHz. (c) 625 KHz. (d) 1 MHz.

Fig. 5.11 shows IMD3 and IMD5 vs. input power in the context of EER for frequency spacings of 20 kHz, 200 kHz, 625 kHz. The calculated values based on AM-

AM and AM-PM from Fig. 4.14 are also shown for comparison. At a frequency spacing of 20 KHz, the measured and calculated value matches within 2 dB. As the frequency spacing increases, the difference between the measured and calculated results increases. Since the calculated values are based on statically measured AM-AM and AM-PM data, for two-tone spacing of 20 kHz, the predistortion based on the same AM-AM and AM-PM is expected to work the best, which is shown through measurements.

As frequency spacing increases, the number of samples in each period of the rectified sinusoid decreases. Simulation based on the TOM model of the MESFET shows that with 30 samples in each period, IM3 can be corrected to be below than -30 dBc. In addition, memory effect is apparent in the non-predistored spectrum of the two-tone test. Therefore, it is concluded that the major contribution to the nonideal nonlinearity correction is due to the memory effects. To improve the predistortion for wider tone spacing, memory effects need to be taken into account.

Memory effects in a PA can show up in the form of asymmetry in intermodulation distortion sidebands and dependence of intermodulation distortion on tone spacing [50]. Memory effects cause the AM-AM and AM-PM behavior of the PA to depend on modulation frequency and limits the amount of correction that predistortion can accomplish. The cause of asymmetry has been studied by many and summerized by Borges de Carvalho and Pedro [51]. These mechanisms include biasing network (Bosch and Gatti [52]), envelope termination (Sevic [53]), out-of-band termination (Aparin and Persico [54]) and can be included into the biasing matching network [23]. A mathematical treatment results in a necessary condition for the asymmetry of the IMD side bands to be reactive baseband load impedance with the real part of the IMD components do not override the imaginary parts of baseband and second harmonic contribution. Specifically for class-E operation, Kazimierczuk [34] shows the intermodulation asymmetry may due to the bias line inductance. Vuolevi et al. [50] proposed envelope filtering and envelope injection techniques for compensating memory effects. Draxler et al. [45] was able to correct the

memory effect by an iterative technique of successive approximation in predistortion. It is shown that RMS error of a PA for WCDMA in EER operation is corrected from 3.5 % to 2.7 %. Correction of memory effects will be part of the future research.

5.3 Load-Pull characterization of class-E PA

The design of a power amplifier is always a compromise between efficiency, output power and linearity. To achieve high efficiency while meeting the required linearity, Sechi [26] points out the sensitivity of the linearity on the impedance, and shows the importance of choice of load impedance based on compromise between efficiency and linearity. Load-pull has been widely used for this purpose. Load-pull has also been used to optimize envelope termination [53].

Here we will compare the load impedance dependence of the class-E PA in both general two-tone and EER two-tone excitation. The load-pull system used in this work is *FOCUS Microwaves*'s Computer Controlled Microwave Tuner measurement system. The measurement system diagram is shown in Fig. 5.12. For the TRL calibration, the fixture at the load side includes a shunt stub providing an open circuit at the second harmonic frequency. For details, please refer to [27]. The load impedance swept is limited to $|\Gamma| \leq 0.8$ due to stability consideration and the region is shown to be enough for our purpose. For the two-tone load-pull, the majority of the measurement is at a frequency spacing of 20 kHz since based on previous measurement, the influence of memory effects is shown to be small at this frequency. Load-pull measurements are performed for both general two-tone and EER two-tone tests and the results are compared.

5.3.1 Single tone load-pull

First load pull is performed at 10 GHz for a single tone (CW) input. The source impedance is determined by source-pull measurement of the device. The optimal op-

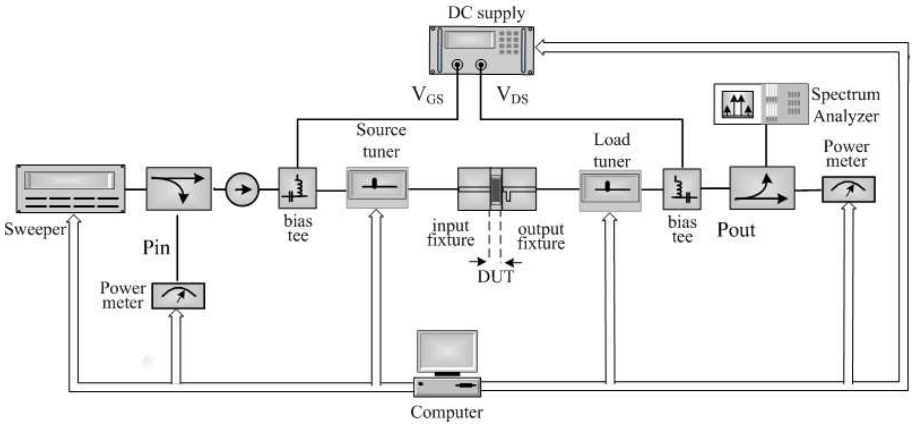
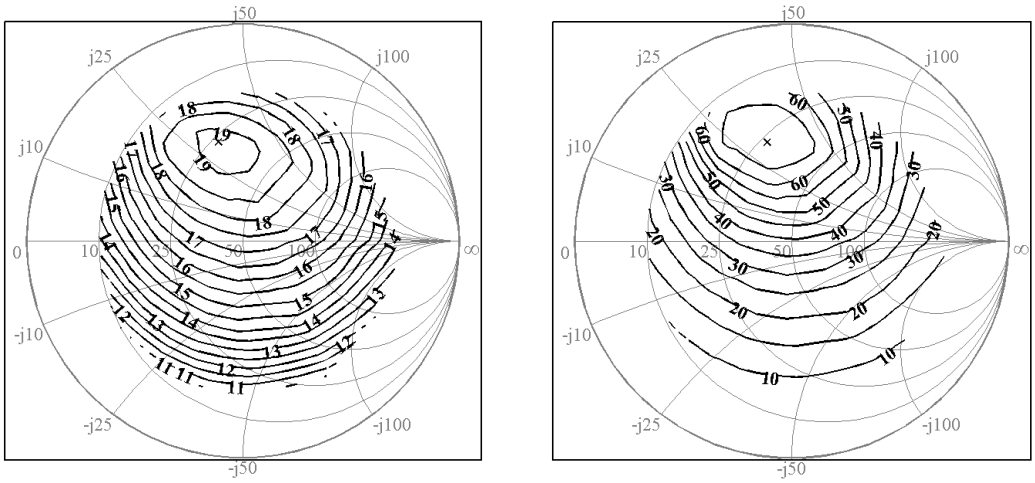


Figure 5.12: System setup for computer controlled load-pull measurement from *FOCUS Microwaves*. For each load impedance value swept, the computer takes all measured data and computes related parameters. The output fixture includes a shunt stub providing an open at second harmonic frequency.



(a) (b)

Figure 5.13: Single tone load-pull results. (a) Load-pull contour for output power. Maximum value is 19.24 dBm at load impedance of $29.88 + j29.51\,\Omega$. (b) Load-pull contour for drain efficiency. Maximum value is 72.4 % at load impedance of $26.29 + j33.26\,\Omega$.

erating point is obtained as $Z_s = 8.15 + j27.30\,\Omega$ and $Z_L = 27.66 + j29.54\,\Omega$. With $P_{in} = 11.98\,\text{dBm}$, $V_{DS} = 4.5\,\text{V}$, $V_{GS} = -1.8\,\text{V}$ and $I_{DS} = 25.4\,\text{mA}$, the device gives, $P_{out} = 19.33\,\text{dBm}$, $\eta_D = 72.27\,\%$ and $G = 7.35\,\text{dB}$. Z_L and Z_s are the load and source impedances seen by the device. The load-pull contours for output power and drain efficiency are shown in Fig. 5.13. In all the contour plots shown in this chapter, a cross and a circle marker are used to indicate the impedance values corresponding to the maximum and minimum value of the parameter plotted.

Theoretical calculated load-pull results for ideal class-E circuit with $Cs = 0.107\,\text{pF}$ at 10 GHz is shown in Fig. 2.4 in Chapter 2. For ideal class-E mode, 100 % drain efficiency is obtained at the impedance value of $Z_{ideal} = 27.3 + j31.5\,\Omega$. Single-tone load-pull measurement shows that load impedance $Z_opt = 26.29 + j33.26\,\Omega$ gives maximum drain efficiency of 72.4 %. The two impedance values are very close. Comparison of the theoretically calculated contour plots of drain efficiency and output power with the measured ones in Fig. 5.13 shows: 1)the shape of the contours for drain efficiency is somewhat different, but both are closed loops and maximum drain efficiency points are almost the same; 2) For the contour of output power, the measured one and calculated one are different. This is mostly due to the active device maximum ratings. For the drain efficiency, the 10% off from the maximum drain efficiency almost fell on the circle of $|\Gamma_{opt} - \Gamma_{load}| \leq 0.2$, which is comparable with the ideal case.

5.3.2 General two-Tone load-pull

The two-tone load-pull is performed at input power of 12 dBm and 10 dBm (power of each tone is 9 and 7 dBm) with frequency spacing of 20 kHz. Frequencies of the two tones are 10 GHz±10 kHz. The load-pull contours of output power and drain efficiency for an input power of 12 dBm are shown in Fig. 5.14. Fig. 5.15 shows load-pull contours of lower side IMD3 and IMD5 products. The load-pull measurement results for input power of 10 dBm are shown in Fig. 5.16 for output power and drain efficiency, and

in Fig. 5.17 for lower side IMD3 and IMD5 contours. The contour plots for output power and drain efficiency for both cases follow a similar pattern as the single tone input case. The contour for IMDs for two input power level also has similar trend. The intermodulation products are nearly symmetrical, so only the lower side IMDs are compared.

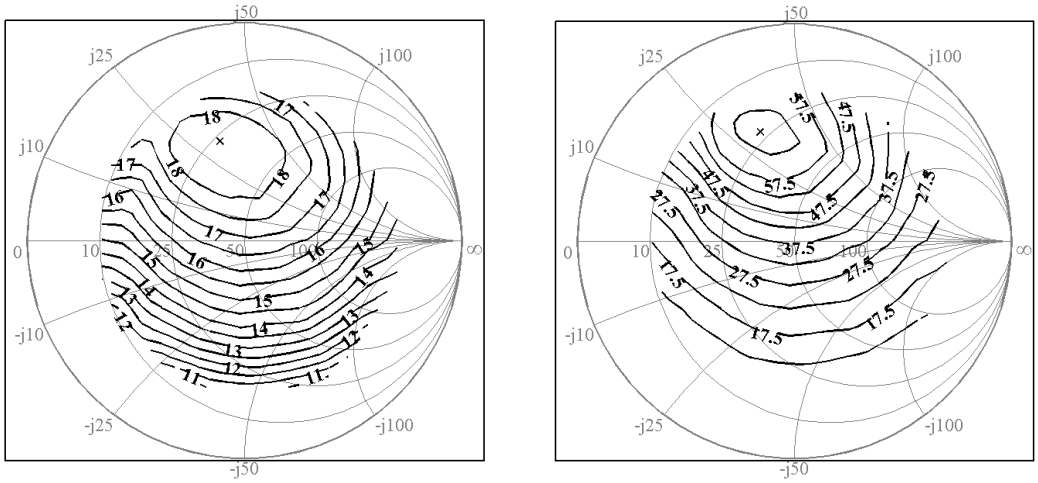
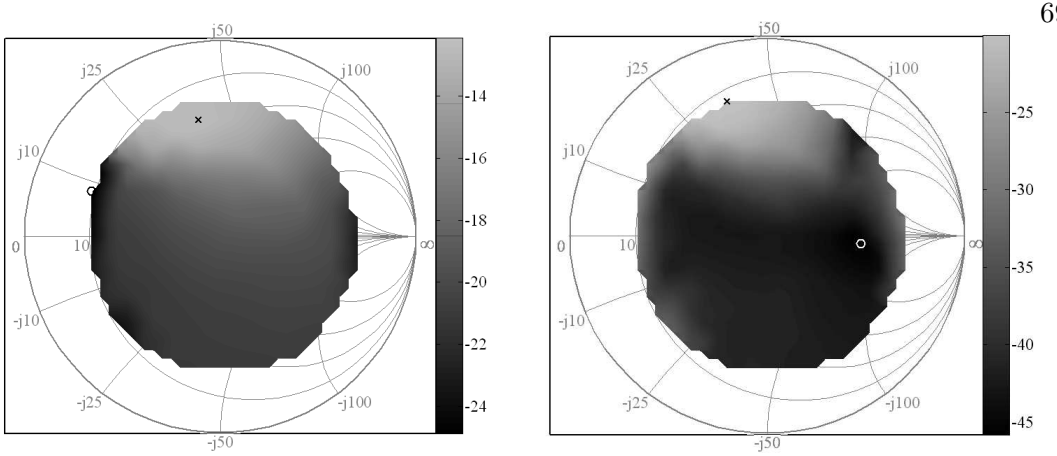


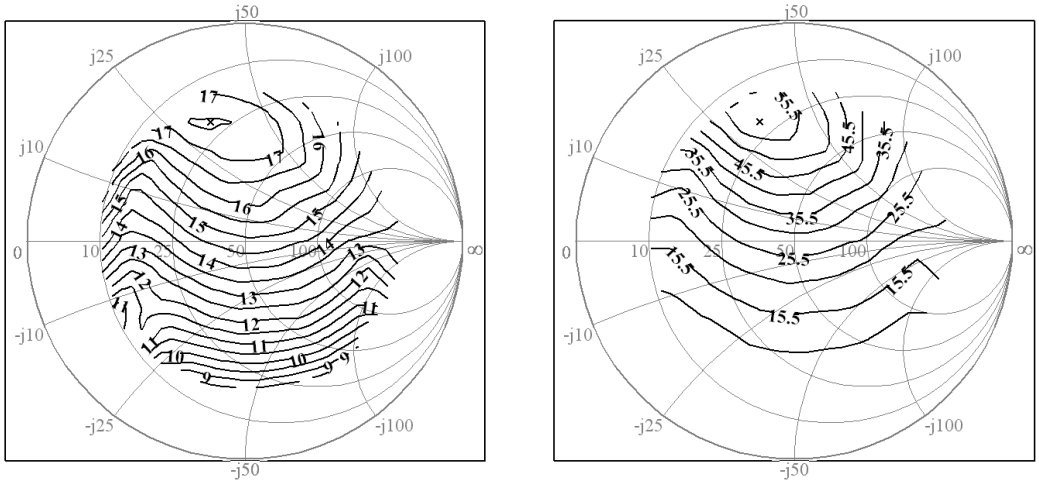
Figure 5.14: General two-tone load-pull results for input power 12 dBm. (a) Load-pull contour for output power. Maximum value is 18.5 dBm at load impedance of $26.93 + j31.53\,\Omega$. (b) Load-pull contour for drain efficiency. Maximum value is 64.5 % at load impedance of $22.72 + j31.47\,\Omega$.

The single-tone load-pull of output power and drain efficiency overlapped with general two-tone lower side IMD3 is shown in Fig. 5.18 and Fig. 5.19. Looking at the IMD3 contour, at some region the constant IMD3 level curves are more dense. For an input power of 12 dBm, an output power drop of 1 dB or drain efficiency drop of 10 % will cause IMD3 to decrease 4 dB (Fig. 5.18). Both output power and drain efficiency contours are closed loops and the IMD contours much less curved. So it is possible to have similar output power and drain efficiency, while IMD3 levels differ significantly. For input power of 10 dBm, the IMD contours are more dense (FIg. 5.19). For an output power drop of 1 dB or drain efficiency drop of 10 %, IMD3 could decrease 8 dB.



(a) (b)

Figure 5.15: General two-tone load-pull results for input power of 12 dBm. (a) Load-pull contour for lower-side IMD3 (dBc). Minimum value is −25.2 dBc at load impedance of $9.25 + j8.26\,\Omega$. (b) Load-pull contour for lower-side IMD5 (dBc). Minimum value is −45.7 dBc at load impedance of $139.32 - j14.4\,\Omega$.

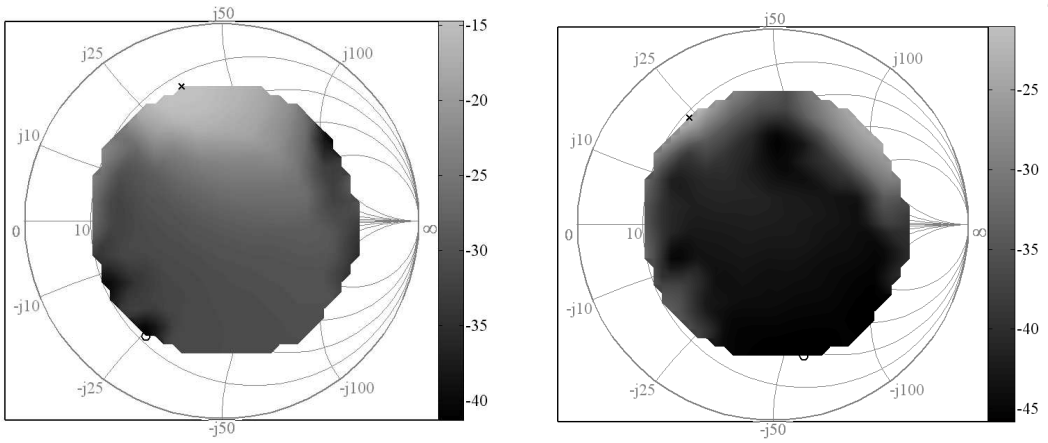


(a) (b)

Figure 5.16: General two-tone load-pull results for input power of 10 dBm. (a) Load-pull contour for output power. Maximum value is 17.57 dBm at load impedance of $20.62 + j33.32\,\Omega$. (b) Load-pull contour for drain efficiency. Maximum value is 58.8 % at load impedance of $20.62 + j33.32\,\Omega$.

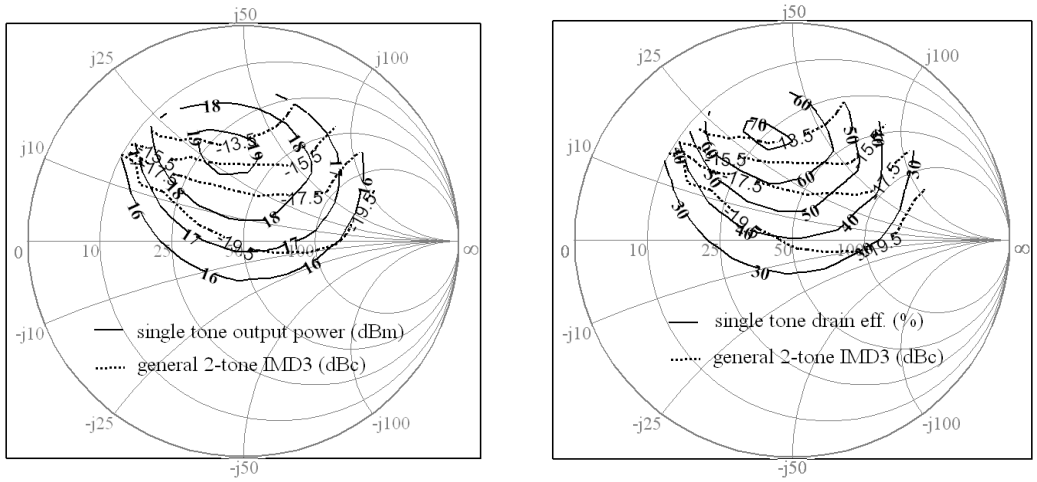
5.3.3 EER two-tone load-pull

To measure the load-pull of IMD power level, the drain voltage of the class-E PA is biased with rectified sinusoidal signal with frequency of 20 kHz and input signal to



(a) (b)

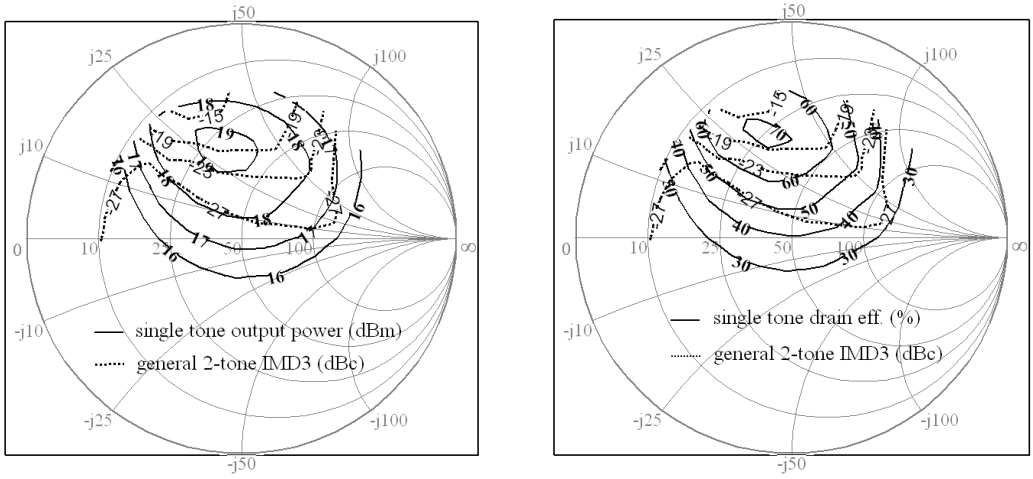
Figure 5.17: General two-tone load-pull results for input power of 10 dBm. (a) Load-pull contour for low side IMD3 (dBc). Minimum value is −41.5 dBc at load impedance of $11.43 - j25.78,\Omega$. (b) Load-pull contour for low side IMD5 (dBc). Minimum value is −46.0 dBc at load impedance of $22.63 - j57.91\,\Omega$.



(a) (b)

Figure 5.18: Single-tone load-pull contour overlapped with general two-tone load-pull contour at input power of 12 dBm. (a) Single-tone load-pull contour of output power and general two-tone load-pull contour of IMD3. (b) Single-tone load-pull contour of drain efficiency and general two-tone contour of IMD3.

the device is 10 GHz signal with 10 kHz zero-and-π phase modulation. The power of the input constant amplitude, phase-modulated signal is 12 dBm. The maximum value of the rectified sinusoid is 4.5 V and 5.0 V. The load-pull is performed and EER two-tone



(a) (b)

Figure 5.19: Single-tone load-pull contour overlapped with general two-tone load-pull contour at input power of 10 dBm. (a) Single-tone load-pull contour of output power and general two-tone load-pull contour of IMD3. (b) Single-tone load-pull contour of drain efficiency and general two-tone contour of IMD3.

load-pull results are obtained.

Fig. 5.20 and Fig. 5.21 show the load-pull contours for low-side IMD3, IMD5 and output powers for two different level of drain biasing rectified sinusoid. The IMD contour plots are completely different in this case from IMD contours from general two-tone load-pull. The contour plots for output power for both cases follow similar pattern as single tone case. The contours for IMDs for two drain bias levels have similar trend. It is difficult to say which of the two bias voltage level have better linearity. As shown in the previous section, in EER 2-tone measurement, the IMD values fluctuate with input power associate with drain bias.

The single-tone load-pull of output power and drain efficiency together with EER two-tone IMD is shown in Fig. 5.22 and Fig. 5.23 for maximum drain bias voltage of 4.5 V and 5.0 V. The linearity seems better for a general two-tone input. However, when the device is saturated more, the IMDs for EER is expected to improve while for general case will deteriorate. For design of class-E PA with application in EER technique, the load should be chosen to minimize IMD under EER case. Examining Fig. 5.23, an

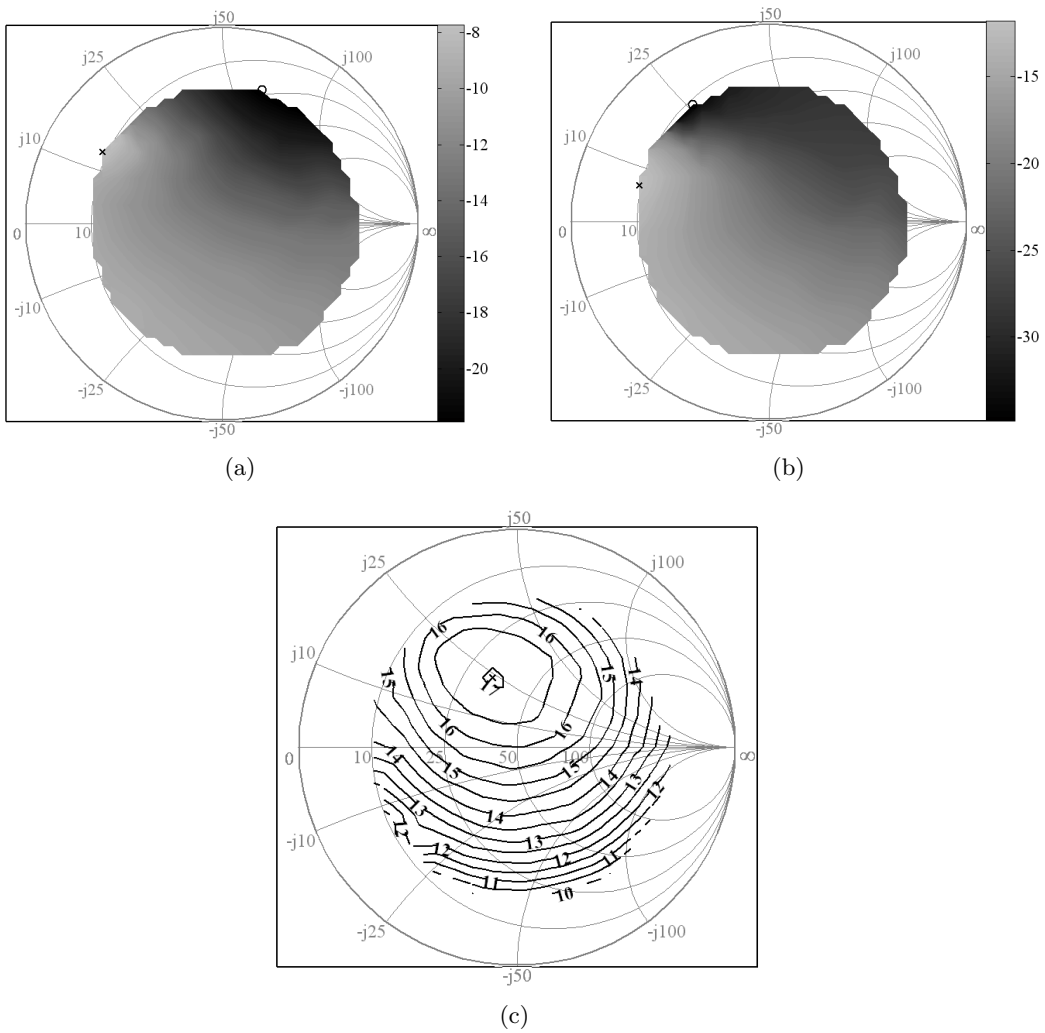


Figure 5.20: EER two-tone load-pull contour of intermodulation products. The peak value of the rectified sinusoid is 4.5 V. (a) Load-pull contour for low side IMD3. Minimum value is $-22.1\,\mathrm{dBc}$ at load impedance of $34.48 + 81.16\,\Omega$. (b) Load-pull contour for low side IMD5. Minimum value is $-35.1\,\mathrm{dBc}$ at load impedance of $12.91 + j35.63\,\Omega$. (c) Load-pull contour for output power. Maximum value is $17.45\,\mathrm{dBc}$ at load impedance of $26.93 + j31.53\,\Omega$.

output power drop of 1 dB or drain efficiency drop of 10 %, will cause IMD3 to decrease by 4 dB. In the general two-tone case, it is possible to have similar output power and drain efficiency while IMD3 differs significantly.

The impedance values for maximum output power, drain efficiency and intermodulation products during the above mentioned load-pull processes are listed in Table 5.6.

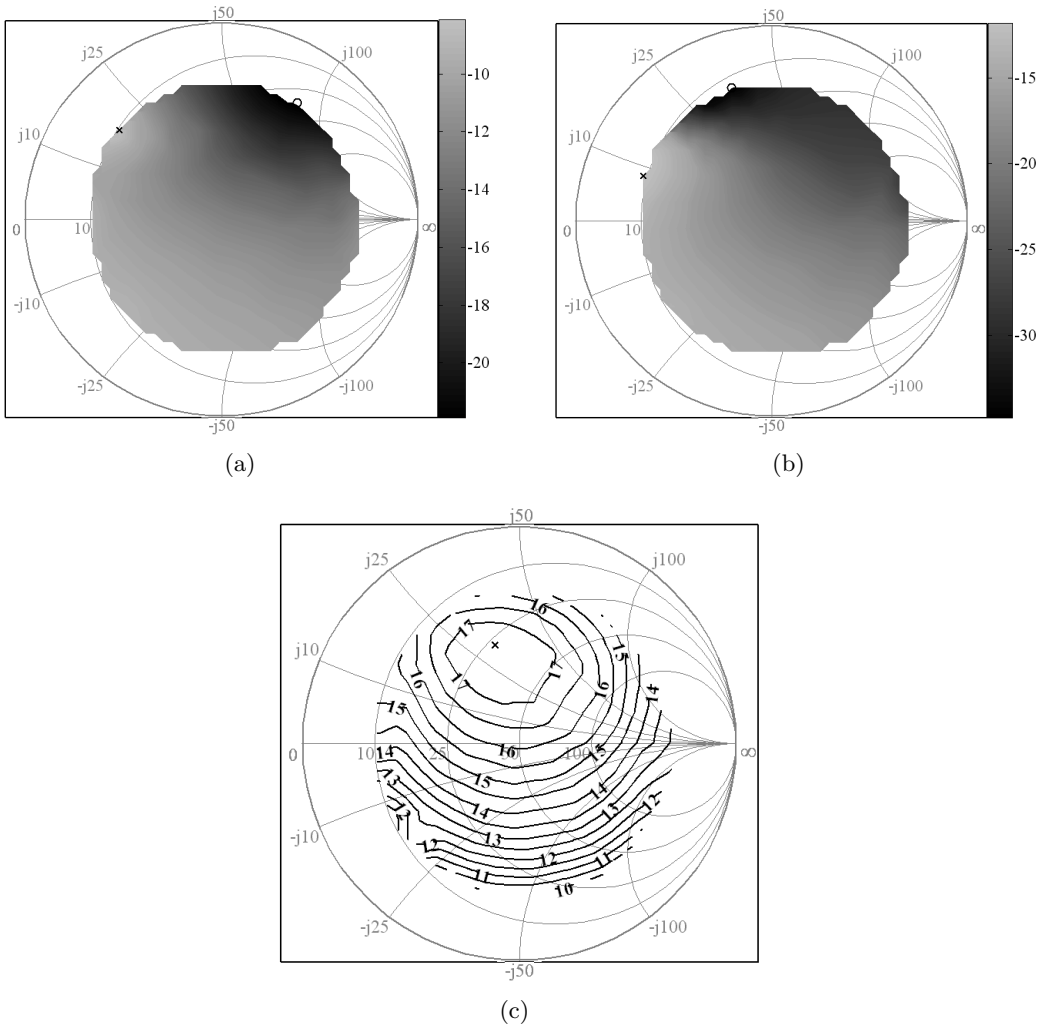
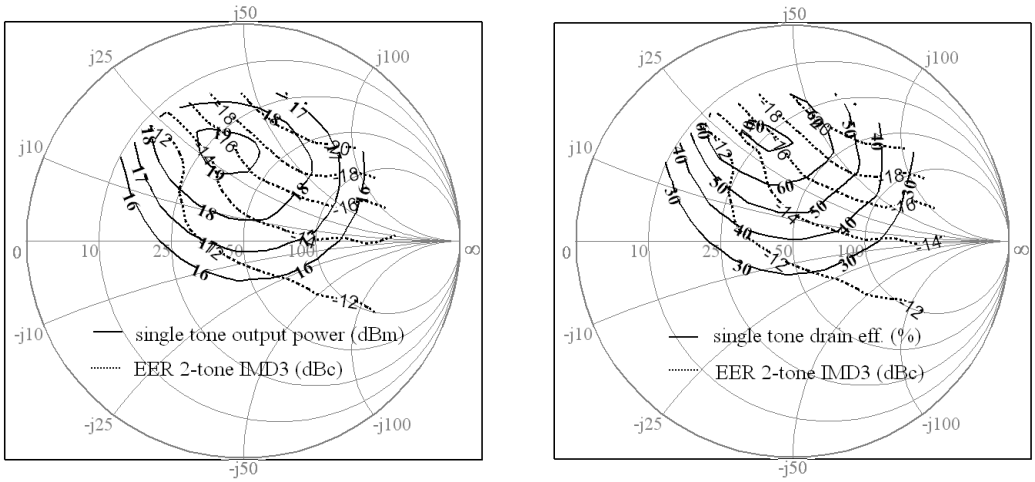


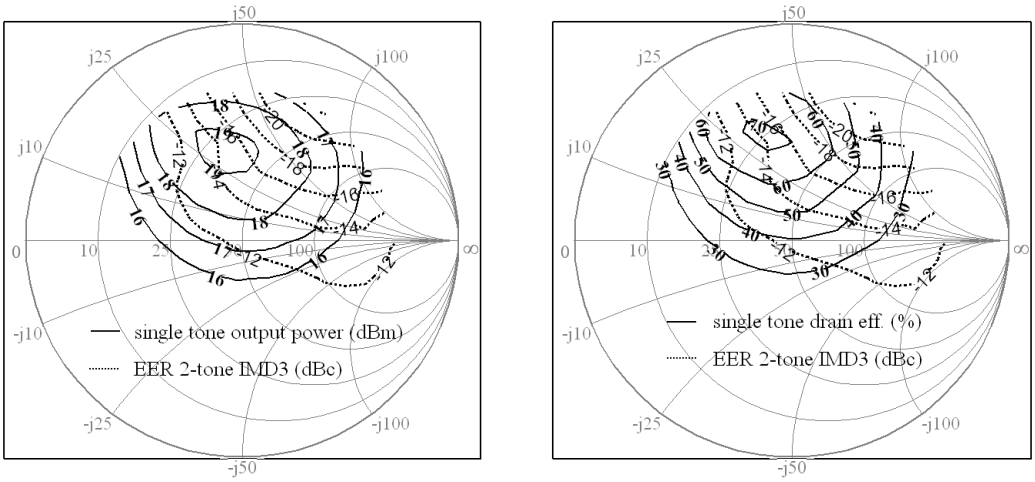
Figure 5.21: EER two-tone load-pull contour of intermodulation products. The peak value of the rectified sinusoid is 5.0 V. (a) Load-pull contour for low side IMD3. Minimum value is $-22.1\,\text{dBc}$ at load impedance of $34.48 + 81.16\,\Omega$. (b) Load-pull contour for low side IMD5. Minimum value is $-35.1\,\text{dBc}$ at load impedance of $12.91 + j35.63\,\Omega$. (c) Load-pull contour for output power. Maximum value is $17.45\,\text{dBc}$ at load impedance of $26.93 + j31.53\,\Omega$.

The impedance which gives maximum output power in all cases stay close. In the general two-tone test, the impedances which results in minimum IMD3 and IMD5 may seem very different for input power levels of 10 dBm and 12 dBm. But based on the their contour plots, it seems if more impedance points are taken, the impedances which provide minimum IMD3 and IMD5 for the two cases are close to each other. For two different drain biases, the impedances which give minimum IMDs for EER two-tone



(a) (b)

Figure 5.22: Single-tone load-pull contour overlapped with EER two-tone load-pull contour. The peak value of the rectified sinusoid is 4.5 V. (a) Single-tone load-pull contour of output power and EER two-tone load-pull contour of IMD3. (b) Single-tone load-pull contour of drain efficiency and EER two-tone contour of IMD3.



(a) (b)

Figure 5.23: Single-tone load-pull contour overlapped with general two-tone load-pull contour.The peak value of the rectified sinusoid is 5.0 V. (a) Single-tone load-pull contour of output power and EER two-tone load-pull contour of IMD3. (b) Single-tone load-pull contour of drain efficiency and EER two-tone contour of IMD3.

are not significantly different. The optimal impedances for IMD are different for the general two-tone test and EER two-tone test. Also, IMD3 and IMD5 contours converge at different impedances.

	1T	general 2T 10 dBm	general 2T 12 dBm	EER 2T 5.0 V	EER 2T 4.5 V
$P_{out,max}$ (dBm)	19.24	17.57	18.50	17.45	17.03
Z_L	$29.88 + j29.51$	$20.62 + j33.32$	$26.93 + j31.53$	$26.93 + j31.53$	$32.96 + j23.92$
$DEff(\%)$	72.4	58.8	64.5		
Z_L	$26.29 + j33.26$	$20.62 + j33.32$	$22.72 + j31.47$		
$IMD3_{min}$ (dBc)		-41.5	-25.2	-22.1	-22.1
Z_L		$11.43 - j25.78$	$9.52 + j8.26$	$34.48 + j81.16$	$22.48 + j62.02$
$IMD5_{min}$ (dBc)		-46.0	-45.7	-35.1	-35.1
Z_L		$22.63 - j57.91$	$139.32 - j14.4$	$12.91 + j35.63$	$11.09 + j26.10$

Table 5.6: The maximum output power, drain efficiency and intermodulation products during the 1-tone and 2-tone load-pull. 1T and 2T stands for 1-tone and 2-tone load-pull; for general 2-tone load-pull, input power level of 10 and 12 dBm is listed; for the EER 2-tone test maximum drain bias of 5.0 and 4.5 V is listed.

5.3.4 Discussion

Load-pull measurements show that for the same output power and efficiency at single tone, the IMD values can be different. For example, at $Z_L = 31.1 + j26.7\,\Omega$, EER IMD3=-13.9 dBc, single tone drain efficinecy is 66.9 % and output power is 19.1 dBm. At $Z_L = 39.8 + j39.6\,\Omega$, EER IMD3=-16.6 dBc, drain efficinecy is 66.2 % and output power is 19.0 dBm. The performance difference between these two impedance values cannot be noticed in single-tone meaurement. However, in the EER two-tone test, there is about 3 dB difference in IMD3. So, IMD load-pull is necesary for obtaining output imedance while best linearizes a class-E PA in EER mode. Two-tone measurements for general two-tone and EER two-tone are also performed at frequency spacings of 640 KHz and 1 MHz. The frequency spacing does not affect much of the impedance values that give maximum output power, maximum drain efficiency and lowest IMDs.

Chapter 6

Active Antenna Array

It was shown in Chapter 4 that class-E amplifiers can be dynamically biased in order to obtain output power control, linearity improvement, etc. Here we will discuss the possibility of using class-E amplifiers in an active array. First, slow dynamic biasing for side-lobe level control by amplitude tapering is examined. Next, the effect of active scan reflection coefficients (SRC) of the array elements on the class-E PAs is studied. The possibility of correcting for the effects of SRC using dynamic biasing are investigated and certain limitations are shown. This is performed on an 11-element half-wavelength uniformly spaced square patch array around 10 GHz, using measured PA data and simulated antenna characteristics. The active array with the PAs, phase shifters and distributed bias control is shown schematically in Fig 6.1.

Due to mutual coupling, the reflection coefficient of each element in the array is different than that of the isolated antennas. As the antenna array beam is steered, the coupling between the elements, and thus the reflection coefficients at the element feed ports, change. The matrix of reflection coefficients, $[S_{ij}]$, at the antenna ports for different scan angles are the S-parameters of the antenna array viewed as a multiport network. The scan reflection coefficients, Γ_i, of element i when the array is steered to a certain angle θ can be calculated as [55]

$$\Gamma_i = \sum_j S_{i,j} \frac{A_j}{A_i} \tag{6.1}$$

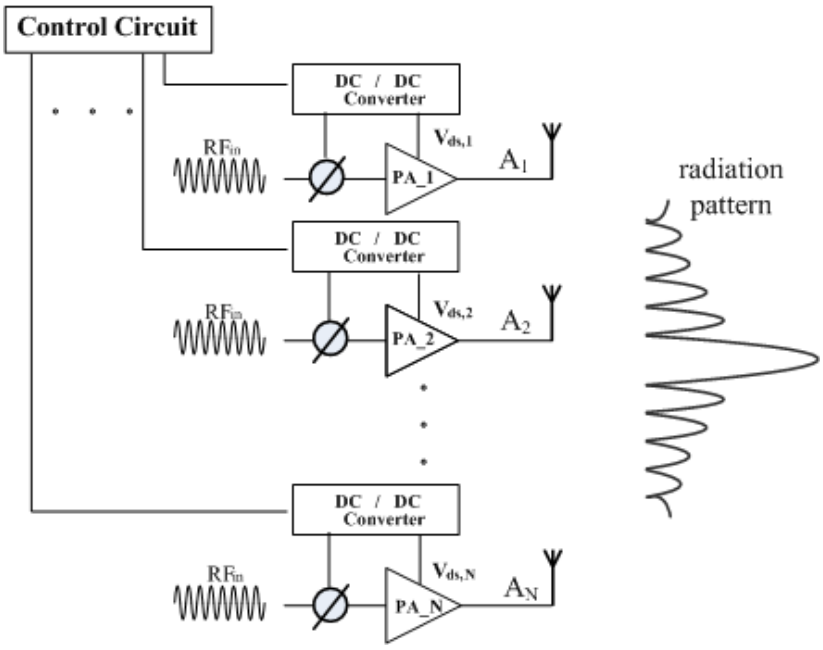


Figure 6.1: Schematic diagram of active transmit antenna array. Each element is driven by a high-efficient class-E PA. Beam steering is accomplished through phase shifters.

where j also denotes an element in the array. The antenna array elements are driven with complex excitations A_i to simulate phase shifters and amplitude control. For the case of an infinite array, all elements look the same and in the absence of edge effects, all Γ_is are the same for a given scan angle.

6.1 Scan reflection coefficients of antenna array

The find the SRC, the scattering parameters of the antenna array need to be determined. *Ansoft Designer* is used to simulate the patch antenna arrays. First a single patch is designed for a center frequency of 10 GHz with a return loss of 23 dB and a gain of about 4.8 dB on a 20 mil thick substrate with $\epsilon_r = 6$. Fig. 6.2 shows the input reflection coefficient and co-polarized pattern of the single element. The characteristics

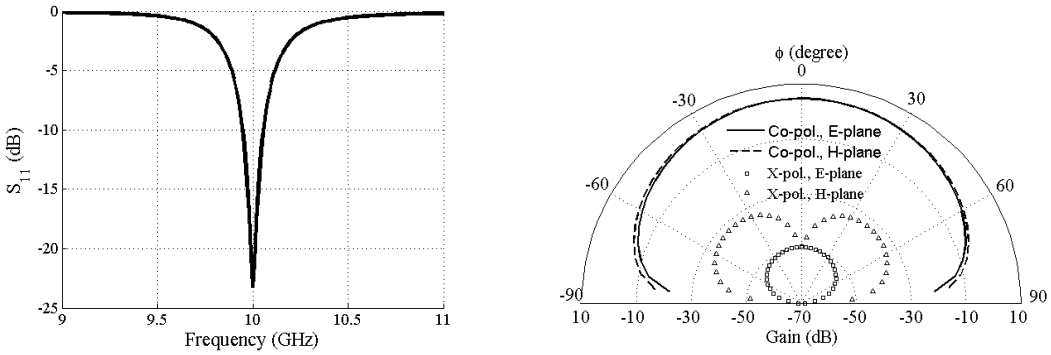


Figure 6.2: Simulated characterization of single patch antenna. (a) Input reflection coefficient of single patch antenna. (b) Directivity pattern.

of the element are included in the array simulation. The resulting array gain is 19 dB and the S-parameters are obtained. Based on Eq. 6.1 the SRCs are calculated for the 11 array elements for 3 scan angles and are shown in Fig. 6.3(a). Fig. 6.3(b) shows the SRC of the center element of the array as a function of scan angle, and the reflection coefficient is seen to vary over a large range, with a best match at $\pm 42°$. This is the case for a 50-Ω input feed line, but a matching network can be inserted to optimize the match for any angle at the expense of the match at the other angles. In the presented case, the output of a class-E PA matched to a 50-Ω load is connected directly to the antenna, and for the purpose of the study the matching was not varied. However, it will be shown that an impedance tuner at the output would be beneficial if one could be made with low insertion loss.

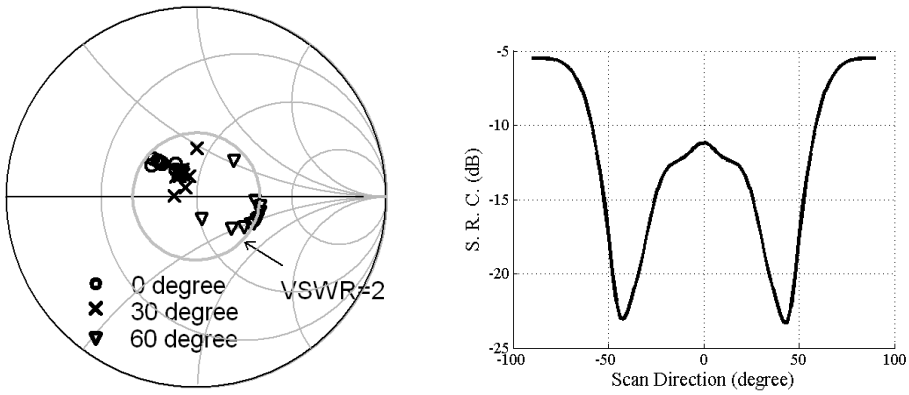


Figure 6.3: (a) Scan reflection coefficient of each element of an 11-element array for three scan angles (0, 30 and 60 degrees). (b) Amplitude of the SRC of the center element vs. scan angle.

At the fundamental frequency of 10 GHz, the load impedance is within a VSWR=2 circle for scan angles up to $\pm 60^{\circ}$. In general, when the impedance presented to the output of a highly saturated PA deviates from $50\,\Omega$, instabilities, efficiency reduction and increased voltage or current stress on the device can result. The effects of the scanning impedance on the ideal class-E PA is investigated using the method described in Chapter 2. In contrast to the case in Chapter 2, the impedance varied here is the impedance of the load behind the matching network, which is ideally $50\,\Omega$, not the impedance presented to the transistor drain port. Fig. 6.4 shows the effects on drain efficiency, power capability and output power when the load deviates from 50 Ω and is allowed to be any possible passive impedances. Table 6.1 summarizes the degradation of the amplifier as the VSWR increases. The normalization value is with respect to the value at $50\,\Omega$.

This effect is quantified experimentally using a coaxial impedance tuner from *Focus Microwaves* which can cover a nominal VSWR of 20:1. The setup is shown in Fig 6.5. The desired impedance is provided by the load side tuner of the *Focus* tuner system. The impedance is tuned to the SRC calculated for 30 and 60 degrees of scan angle. Gate and drain bias voltage is swept and output power, bias voltage and currents are measured and related parameters are calculated.

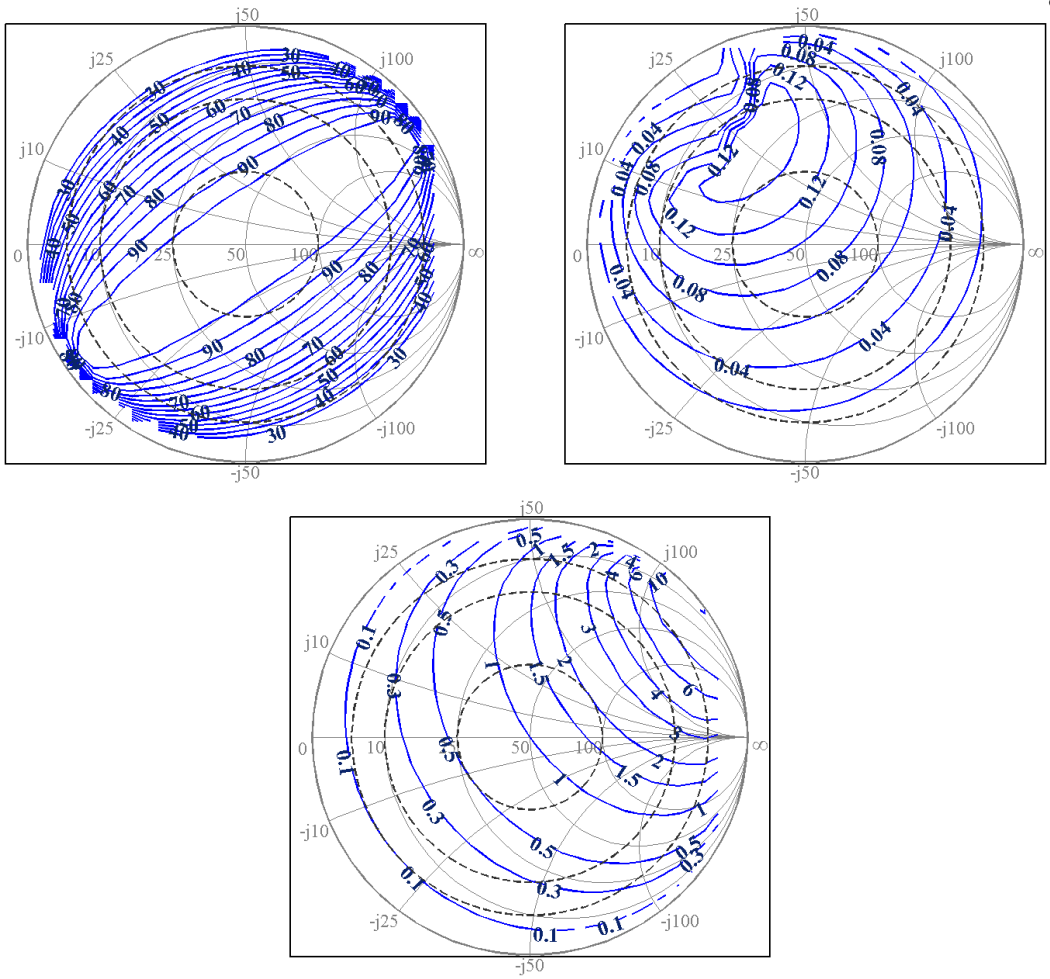


Figure 6.4: Load variation for ideal class-E PA. (a) Drain efficiency (%). (b) Power capability. (c) Normalized output power (W) at fundamental frequency. The normalization value is the output power of the PA when the load is 50 Ω.

The results are shown in Fig 6.6, Fig 6.7 and Fig 6.8. The gate bias is fixed at -1.4 V. Fig. 6.6 shows the effect of SRC change for several scan angles on a class-E PA. Because we have shown that the best match is at 42 degrees, it is seen that the drain efficiency is highest at 30 degrees scan angle and degrades at 0 and 60 degrees by as much as 15%, depending on the drain bias voltage. The drain bias voltage is chosen as the horizontal axis because our goal is to show that dynamic biasing of the drain can help improve active array performance, e.g. reduce side-lobe levels. This is apparent in Fig 6.6(b), where the load current, which is the current through the

VSWR	$\eta_D(\%)$	P_{cp}	$P_{out,norm}(W)$
1	100	0.098	1
2	87∼100	0.06∼0.14	0.5∼2
5	55∼100	0.025∼0.15	0.2∼5
10	34∼100	0.015∼0.15	0.1∼11

Table 6.1: Drain efficiency, power capability and normalized output power at VSWR circle of 2, 5 and 10.

antenna, will determine the array pattern. Figs. 6.7 and 6.8 show the performance of all 11 PAs in the active array for a 30-degree and a 60-degree scan angle, respectively. Table 6.2 summarizes the results when the drain bias deviates from the optimal value by 10%. Table 6.3 summarizes the maximum and minimum value of drain efficiency, current into the antenna and output power among 9 elements. The elements at the two ends are not included since their difference between other elements are relatively large. Based on simulation, the phase shift introduced by the PA under different loading is within 5 degrees for 30 degree of scanning and 8 degrees for 60 degree of scanning (not considering the two elements at two ends). This need to be varified by measurements and corrected by control of the phase shifters.

From Fig 6.6(a), at optimal drain bias of $4.2\,V$, the drain efficiency changes over 10% when the array is directed towards 60 degree, which can't be corrected without sacrificing too much of the output power. The solution to it may be a tuner between the antenna and PA. This can also be explained from the fact that the ouput capacitance of the device is not dependent on the drain bias, a result shown previously. Comparing

	0°			30°			60°			50 Ω
V_{DS}(V)	3.8	4.2	4.6	3.8	4.2	4.6	3.8	4.2	4.6	4.2
DEff(%)	56.05	55.12	53.99	60.09	58.79	57.41	52.45	48.67	44.78	60.5
I_{out}(mA)	60.33	65.08	69.59	55.63	59.66	63.39	42.35	43.35	43.67	57.54
P_{out}(dBm)	17.09	17.75	18.59	18.24	18.85	19.60	19.27	19.47	19.54	19.47

Table 6.2: The drain efficiency, input current to the antenna and output power from the center PA for drain bias voltage of 3.6, 4.2 and 4.6 V.

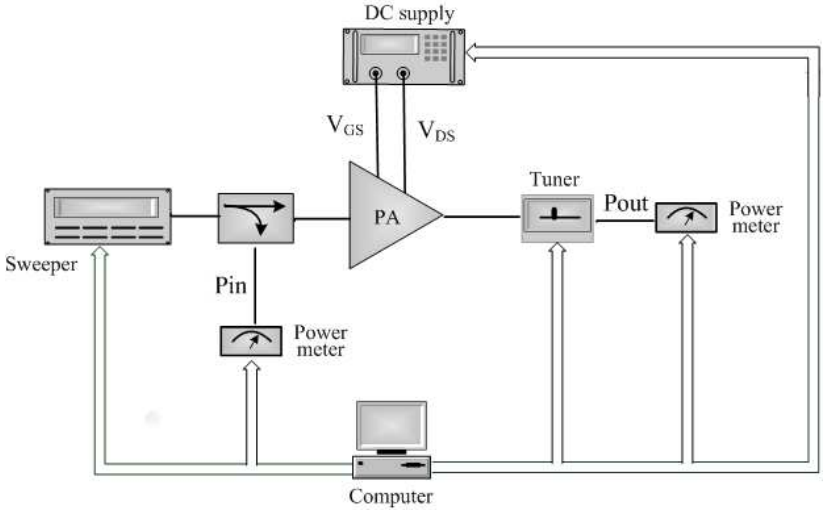


Figure 6.5: The diagram for measurement of PA with different load termination. Load-side tuner is used to provide different load impedances.

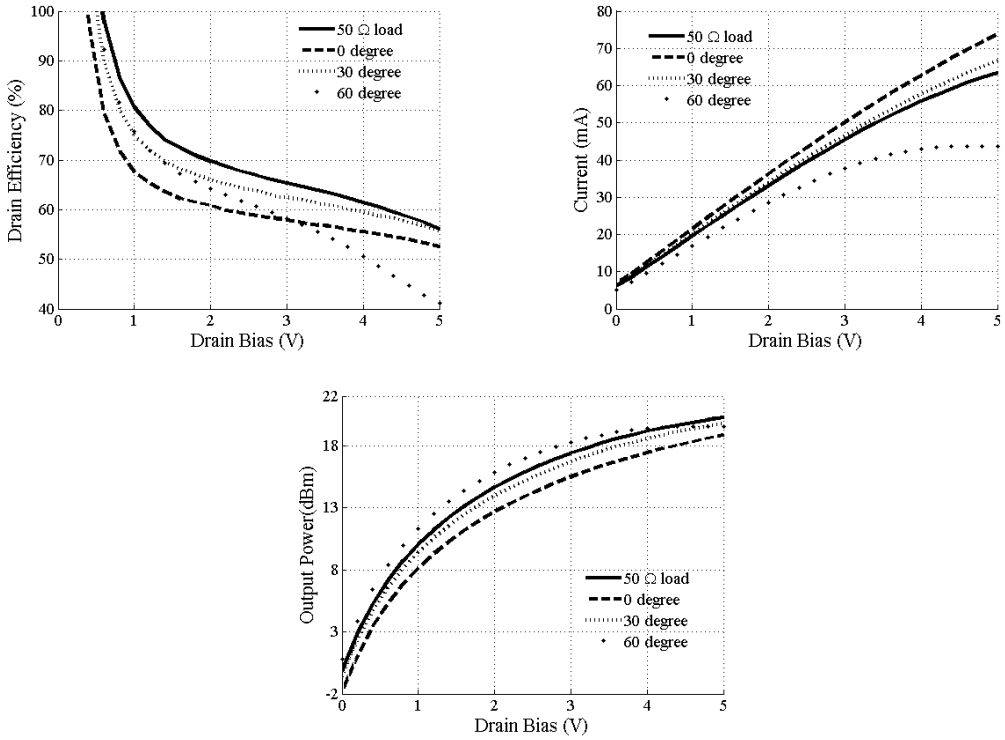


Figure 6.6: Performance of the PA terminated with load impedances corresponding to SRC of center element of the 11-element active array at three scan directions. (a) Drain efficiency. (b) Load current. (c) Output power.

the behavior of the 11 elements at 30 and 60 degree of scanning, at 60 degree of scan

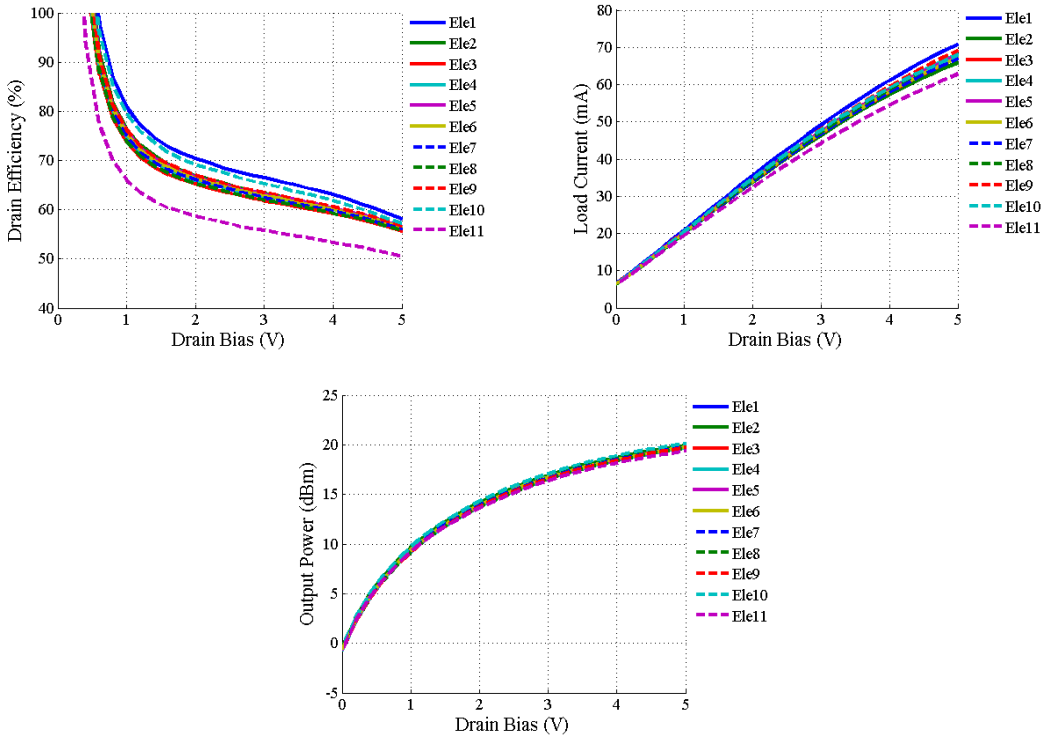


Figure 6.7: Performance of the PA terminated with SRC of 11 elements at 30 degree scan angle. (a) Drain efficiency. (b) Load current. (c) Output power.

angle, the element behavior differs by larger amount.

The SRC previously calculated is the impedance when all ports are excited by standard 50 Ω source. In our case, the antenna elements are connected with class-E PA. The impedance each PA sees in this situation is simulated using *ADS*. The class-E PA is modeled using an ideal switch with on resistance of 1Ω and off resistance of 1 MΩ. The matching network uses two stubs with ideal transmission lines. The SRC measured in this case is very close to the one calculated previously using an ideal 50Ω source under different scan angles. The current flowing into each port is compared with the ideal excitation current, showing magnitude and phase changes in the currents. The array factor calculated using these current coefficients and those from a 50-Ω source almost the same, and also agrees well with *Designer* simulations with 50Ω sources for up to 60 degrees of scanning.

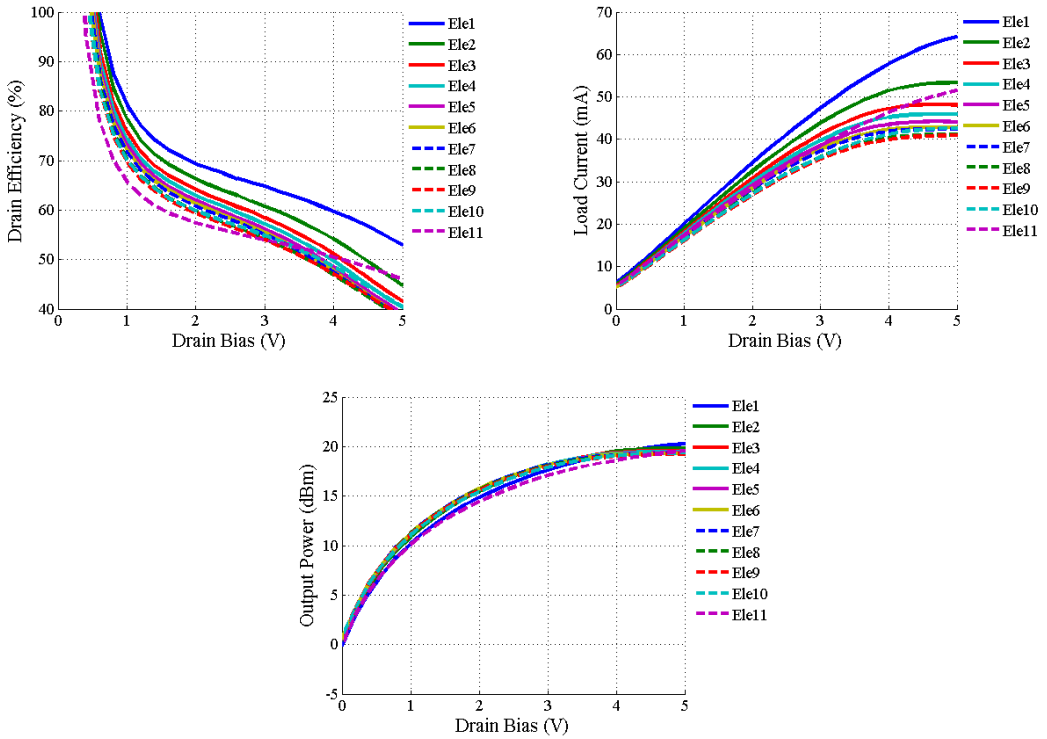


Figure 6.8: Performance of the PA terminated with SRC of 11 elements at 60 degree scan angle. (a) Drain efficiency. (b) Load current. (c) Output power.

	30°		60°	
DEff(%)	58.74	60.97	45.11	52.39
I_{out}(mA)	59.12	61.57	40.38	52.23
$P_o$ut(dBm)	18.66	19.20	19.12	19.64

Table 6.3: The maximum and minimum value of drain efficiency, antenna input current and output power among 9 elements (the 1st and 11th element are not counted) at drain bias of 4.2 V.

6.2 Side lobe level control of the radiation pattern

In this section the use of the class-E PA in side-lobe controlled array, specifically Tschebyschev array is discussed. The previous measurement results for the PA are used here.

6.2.1 Comparison of side lobe control between class-E and class-A

The radiation pattern of a single patch is calculated from *Designer* and used for the calculation of side lobe level (SSL) of the array. For 11-element Tschebyschev array, the amplitude ratio between elements are (0.367 0.457 0.656 0.833 0.956 1 0.956 0.833 0.656 0.457 0.367). Based on the relationship between the drain bias and output voltage, the drain bias is used for obtaining the correct ratio of signal level at the antenna element. Drain efficiency, total output power of the PA and side lobe level is the main parameter we want to examine.

The class-E PA is modeled in Matlab based on the interpolation of early measurement data of class-E PA (Chapter 3). Its behavior is shown again in Fig 6.9 for reference. The drain bias of the center PA is swept from 0 to 5 V and the bias of other

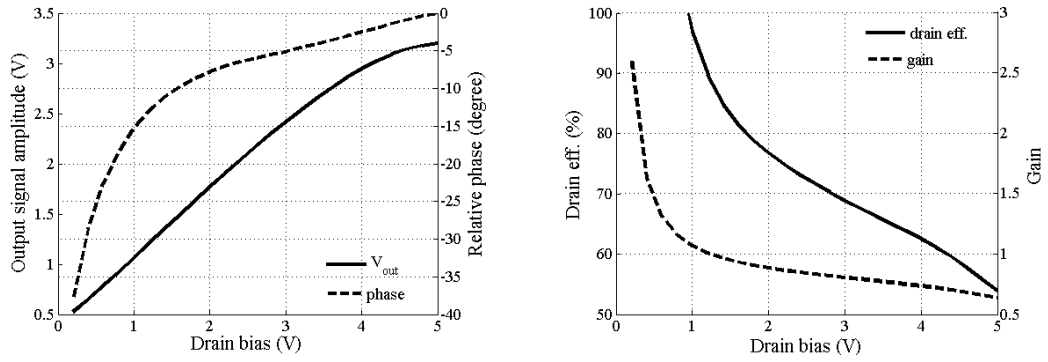


Figure 6.9: Class-E PA characterization (a) AM/AM and AM/PM; (b) drain efficiency and gain (ratio of output voltage and drain bias).

element varies according to the ratio. The results are shown in Fig 6.10. The drain efficiency and output power follows same trend as single class-E PA. The fluctuation

in the side lobe level is mainly caused by the AM/PM effect of PA. The directivity and maximum direction of radiation is not influenced. Here, as observed, the effect of mutual impedance is not considered.

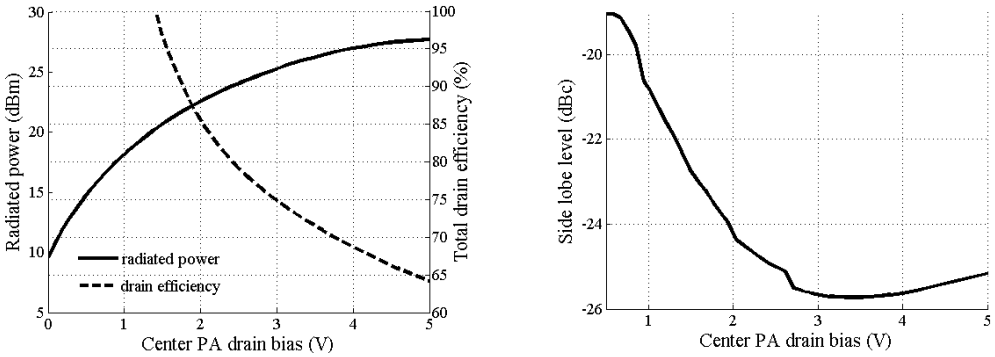


Figure 6.10: Characterization of 11-element active array antenna with class-E PAs as the driver amplifiers. (a) Radiated power and drain efficiency. (b) Side lobe level.

For comparison, active array with class-A PA using same device is characterized. The performance of class-A PA is shown in Fig 6.11. The input power to the center

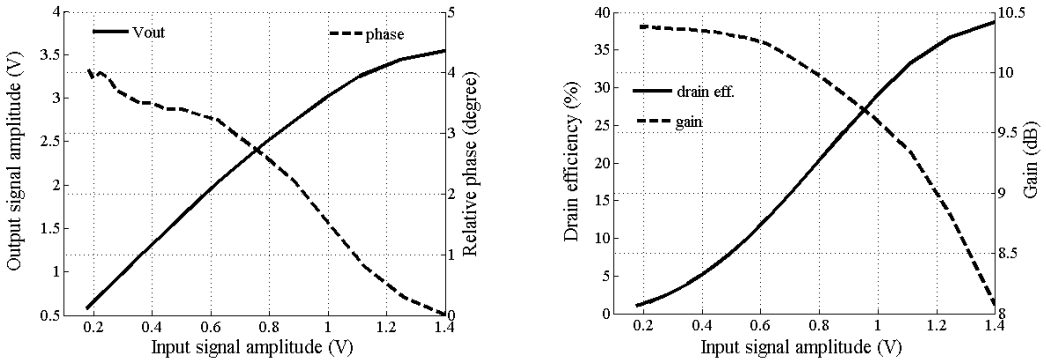


Figure 6.11: Class-A PA characterization (a) AM/AM and AM/PM; (b) drain efficiency and gain.

element is swept from -20 dBm to 11 dBm and the input power to the other elements are set so that to generate the desired signal amplitude ratio at each element. The results are shown in Fig 6.12. The drain efficiency and output power follows similiar trend as the signal class-A PA. Since the AM/PM conversion is small, the SSL level

almost doesn't change compared with the class-E case.

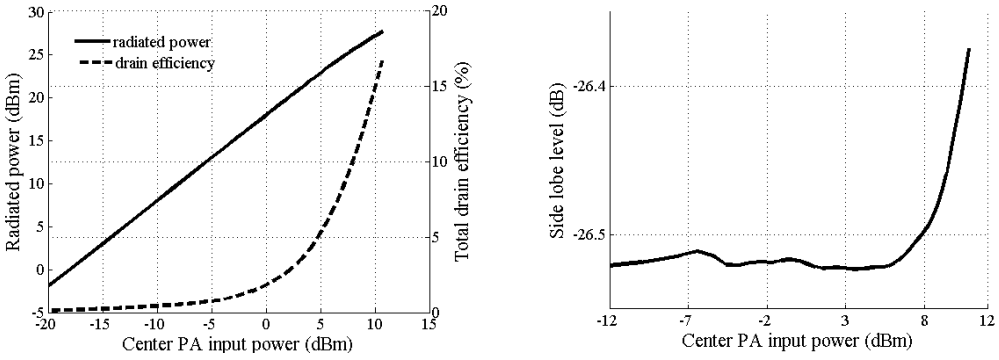


Figure 6.12: Characterization of 11-element active array antenna with class-A PAs as the driver amplifiers. (a) Radiated power and drain efficiency. (b) Side lobe level.

For class-E, the AM/PM conversion causes up to 6 dB. The SSL deterioration is worse at lower power levels, since AM-PM is more serious when drain bias level is lower.

The SRC of the 11-element patch antenna array is calculated for tapered excitation case based on Eq. 6.1. It shows that the results are almost same as uniform excitation case. So amplitude tapering doesn't affect the mutual impedance much.

6.3 Conclusion

In this chapter, analysis of an active transmit scanning array with class-E PAs in each antenna element is presented. We postulate that by distributing the bias control circuit, some performance improvement can be obtained. In applications where circulators or isolators are not desirable, such as portable arrays, when the beam of the array is scanned, the impedance presented to each PA in the array will be different and will vary with scan angle. Through simulations using experimentally-obtained amplifier data, it is found that the dynamic biasing at each element can help maintain efficiency only to a certain degree. For larger scan angles, efficiency and power loss cannot be compensated through bias control, and we conclude that some type of tuner network becomes necessary. In the simpler case of taper (sidelobe) control, it is shown that distributed

biasing can be effectively applied without sacrificing efficiency. The initial work done in this thesis shows that it may be possible to produce ("stamp out") large numbers of identical elements (PAs integrated with antennas), but then make each element in the array slightly different through digital bias control. The digital control thus enables innexpensive manufacturing, while allowing optimized element performance for the case of sidelobe level control.

Chapter 7

Conclusion And Future work

7.1 Thesis Summary

This thesis explores the possibility of using class-E PAs for amplifying signals with both amplitude modulation and phase modulation at carrier frequency of 10 GHz. The class-E PA is nonlinear since the active device operates as a switch by being driven into saturation. Dynamic biasing, specifically the dynamic biasing of the drain voltage (FET), is investigated as a possible method for linearization of the class-E PA, based on the amplifier's linear relationship between the drain bias and output signal amplitude. Most of this work is based on a class-E PA designed at 10 GHz using a GaAs MESFET AFM04P2 from *Alpha industries*, with a maximum output power of 20.3 dBm(0.7 dB less than the specified maximum output power) and drain efficiency of 67 %. It is also briefly shown that HBT and PHEMT devices behave similarly.

An ideal class-E circuit is analyzed theoretically for different impedance at the fundamental and second harmonic frequencies. For impedance sweeping at fundamental frequency, all higher harmonics are open-circuited. For impedance sweeping at second harmonic frequency, all higher harmonics are open circuited and the impedance at fundamental frequency is determined to satisfy the "soft switching" condition. The result shows that the class-E mode is tolerant to impedance change. Thus the PA design is validated.

Slow dynamic biasing is shown to increase the efficiency for lower output power

level while maintaining same input power level. Thus, the power of the PA can be controlled directly through efficient bias control. The efficiency of the PA with dynamic biasing is improved by a factor of 1.4 over an output power between 15 and 20dBm. In fast dynamic biasing, the EER technique becomes a logical choice for linearizing the class-E PA. Due to the linear relationship between the drain bias voltage and output signal amplitude, the class-E PA lends itself naturally to the EER technique. When operated in EER, the 10-GHz class-E PA generates upper side IMD3 of -25.4 dBc and lower side IMD3 of -20.7 dBc at two-tone frequency spacing of 1 MHz. To meet the linearity requirement of IMD3$\leq$-30 dBc, open-loop lookup table based digital baseband predistortion is performed. Efficient wide-band envelope tracking for biasing the PA is achieved through a combination of a switched-mode power converter and a linear class-AB amplifier. The digital PA system controller is constructed using a Xilinx Virtex-II V2MB1000 FPGA. The system controller allows the flexibility of generating arbitrary signals for the drain bias and phase shifter control with or without predistortion from a lookup-table. With predistortion, IMD3 requirement of -30 dBc is met at a two-tone spacing of 20 kHz, but not for higher values of two-tone frequency spacing. The linearity can be further improved as suggested in the next section.

Finally, the application of the class-E PA as the driver for active phased array antennas is discussed with emphasis on dynamic biasing of each driver PA for side lobe control and array steering. A 11-element 1-D patch antenna array is taken as an example. Issues related to these application include, AM-AM and AM-PM effect of the PA and impedance variation of load impedance on PA behavior.

Specific contributions of this work are:

- Theoretical load-pull of class-E PA is performed for impedance at fundamental frequency while assuming higher harmonic frequencies are open-circuited. The tolerance of the class-E operation on load impedance variation is observed.

Impedance at second harmonic frequency is swept. It is found that with second harmonic level over 40 dB less than signal at fundamental frequency, efficiency can be kept over 90 %;

- Open-loop digital baseband predistortion of the class-E PA at X-band in EER mode of operation is performed. At frequency spacing of 20 KHz, the IMD3 of -33 dBc is obtained.

- Load-pull measurement of IMD for class-E PA operating in EER mode is performed. The results are compared with two-tone load-pull results in general two-tone. The impedance values which optimize the IMD in EER two-tone is different from those in general two-tone.

7.2 Proposed future work

Based on present results of this work following future research work is suggested.

As shown in Chapter 5, the predistortion in EER mode meets the -30 dBc requirement at this point only for relatively narrow bandwidth signals (two-tone spacing of 20 kHz). When the center frequency is at 10 GHz, the modulation frequency can be tens of MHz. Linearity needs to be improved for wider bandwidth signals, i.e. wider two-tone frequency spacing in the linearity measurement. Possible ways to improve linearity include:

- Some improvements can be obtained with adaptive feedback loop in predistortion, which mainly corrects for device performance changes due to aging, temperature and power supply fluctuation. The feedback loop can also correct inaccuracy in the predistortion value caused by device characterization process or performance fluctuation between devices. Ref. [42, 43] are recommended as a start.

- Limiting feedthrough voltage by modulating a driver stage will bring both linearity improvement and efficiency increase [33];

- Memory effects are a major issue for the PA used in this work and correction by trying some of the memory correcting predistortion methods described in [50, 45] is highly suggested.

Load-pull characterization of the device shows further improvement in linearity can be obtained by:

- Redesigning the PA based on two-one load-pull in EER mode. In this work, the PA is designed without knowledge of IMD load-pull results.

- As suggested by reference [53], envelope load-pull can be performed to find the optimal impedance for envelope signal termination.

Finally, it is suggested to test an active phased array driven with class-E PAs with dynamic biasing circuitry to verify the study results from Chapter. 6.

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