DELTA-SIGMA MODULATED RF TRANSMITTERS

by

QIANLI MU

B.E., Beijing University of Aeronautics and Astronautics, 2003

M.S., University of Colorado at Boulder, 2005

A thesis submitted to the
Faculty of the Graduate School of the
University of Colorado in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy
Department of Electrical and Computer Engineering
2008

This thesis entitled:

Delta-Sigma Modulated RF Transmitters

written by Qianli Mu

for the Doctor of Philosophy degree

has been approved for the

Department of Electrical and Computer Engineering

by

_____

Prof. Zoya Popović

_____

Prof. Dragan Maksimović

Date _____

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Mu, Qianli (Ph.D., Electrical Engineering)

Delta-Sigma Modulated RF Transmitters

Thesis directed by Professor Zoya Popović

This thesis presents the analysis, design, and measurements of the front end of a bandpass delta-sigma modulated RF transmitter. Currently, there is considerable interest in "direct" digital RF transmitters for simultaneous multi-task transmitting, where extraordinarily linear signal conversion is required. The delta-sigma modulated conversion provides a promising approach. Conceptually, a delta-sigma modulated RF transmitter has three stages: a bandpass delta-sigma modulator, a one-bit power digital-to-analog converter (DAC), and bandpass filtering circuits.

The one-bit power DAC has primary importance in the transmitter implementation, because it directly determines the system linearity performance. In this thesis, a circuit approach is described for analyzing the generation mechanisms of the nonlinear inter-symbol interference (ISI) in the one-bit power DAC. Single-ended and differential converter topologies are theoretically analyzed and experimentally characterized with a three-tone delta-sigma test signal. Additionally, the linearity performance of single-ended and differential configuration DACs with different bandpass filters is discussed, where the fundamental idea is that the load-circuit effect on the linearity performance of the DAC is determined by its input impedance.

Dedication

To mom, dad, and Jia, who I cherish and love the most.

Acknowledgments

The last six years of the graduate study toward my Ph.D. thesis was a very special and wonderful journey in my life. I am grateful to all the people that I have worked and lived with. Without you, it would not be as colorful as what I memorize today.

Most of all, I would like to thank my advisor Prof. Zoya Popović for her invaluable guidance, support and encouragement. I really appreciate the research environment that she provides to the Active Antenna Research Group. I would also like to thank Dr. Jeffrey Coleman from Naval Research Laboratory for his suggestions, technical inputs and constructive comments on this thesis work. My sincere thanks also go to the committee members: Prof. Edward Kuester, Prof. Dejan Filipović, Prof. Dragan Maksimović, and Prof. James Curry.

Without the help and support from my colleagues and friends, the completion of this thesis would not be possible. I thank Dr. Scholnik, Luke Sankey, Mark Norris, and Miloš Janković for their collaboration and cooperation on the delta-sigma project. I thank Dr. Srdjan Pajić, Dr. Jason

Breitbarth, Dr. Hung Loui, and Dr. Sébastien Rondineau for the valuable ideas and help that they offered me generously. I thank Dr. Nestor López and John Hoversten for the discussions on power amplifiers. I would also like to extend my thanks to the past and present members of the Active Antenna Group: Dr. Marcelo Perotoni, Dr. Paul Smith, Dr. Narisi Wang, Dr. Patrick Bell, Christi Walsh, Dr. Alan Brannon, Dr. Kenneth Vanhille, Dr. Charles Dietlein, Mabel Ramírez, Mike Elsbury, Negar Ehsan, Nicola Kinzie, Evan Cullens, Jonathon Chisum, Erez Falkenstein, Jason Shin, and John O'Brien; and members in the downstairs EM office: Dr. Milan Lukić, Dr. Michael Buck, Dr. Yongjae Lee, Kim Kichul, Yuya Saito, Yaowen Hsu, Miao Tian, and Hongyu Zhou. I thank you all for the collaboration and friendship. I would also like to acknowledge our administrative staff: Jarka Hladišová, Adam Sadoff, and Rachael Tearle.

I would like to thank my Chinese friends: Jun Liu, Dr. Lianjun Jiang, Xin Geng, Chunyan Gu, Min Liu, Dr. Qi Wu, Dr. Wenjin Mao, Rundong Zhu, and the others. Without you, I could not image how I would get through the time when I first came to the United States.

Finally, I want to thank my parents and my wife, Jia, for their continuous love and understanding. I am truly grateful for being in such a family.

Contents

Tables

Figures

Chapter 1

Introduction

This thesis presents the design and characterization of the system components for a radio frequency (RF) bandpass $\Delta\Sigma$ modulated transmitter, which is viewed as a way to realize multi-function transmitters for software radio or radar. In the rest of the chapter, first a brief overview of the background, motivation and contribution of the work will be given, followed by a chapter-by-chapter summary of the thesis.

1.1 Overview

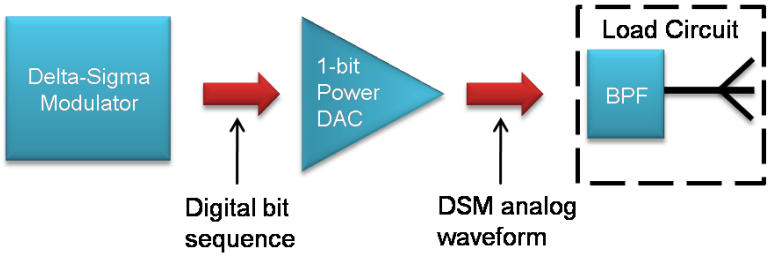
1.1.1 Background and Motivation

The concept of software radio was first presented at the May 1992 IEEE National Telesystems Conference by Mitola [1]. "A software radio is a set of Digital Signal Processing (DSP) primitives, a meta-level system for com-

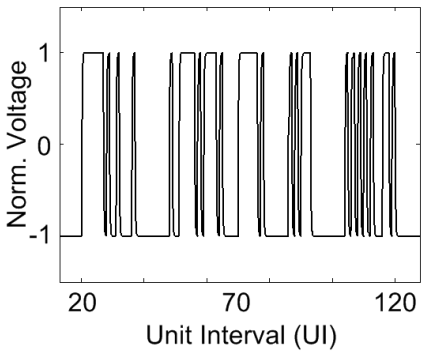
bining the primitives into communications systems functions (transmitters, channel model, receiver...) and a set of target processors". It is an ideal multi-mode system which can incorporate additional functionality by simply modifying the software [2], with the goal of reducing the content of radio frequency (RF) and other analog components in traditional radios.

The final stage of a classical transmitter architecture is based on linear power amplifiers, in a variety of different architectures including Envelope Elimination and Restoration (EER), polar loop, LInear amplification with Nonlinear Components (LINC), Combined Analogue Locked Loop Universal Modulator (CALLUM), LInear amplification employing Sampling Techniques (LIST) and transmitters based on bandpass $\Delta\Sigma$ modulators [3]. Most current RF front ends require the analog carrier mixing process, except for $\Delta\Sigma$ modulated transmitters, where the signal is directly digital-to-analog (D/A) converted at the radio frequency, and the digital circuits are at the very front end of the transmitter. The properties mentioned above of the $\Delta\Sigma$ modulated transmitters make them good candidates for software radio implementation, where transmitter flexibility is a key factor.

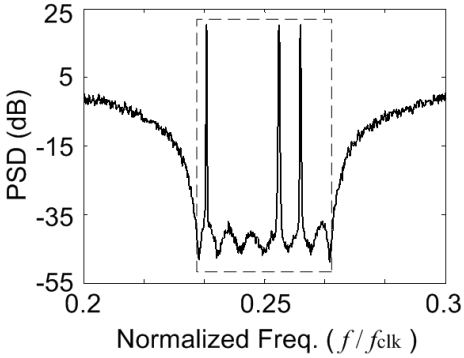
Bandpass $\Delta\Sigma$ modulation offers high signal linearity, or signal-to-noise ratio (SNR), in the signal band with a low-level, e.g. one-bit, quantizer [4]. The quantization noise created by the low-level quantizer is spectrally shaped and pushed out of the signal band. After bandpass filtering, high SNR is provided as in a conventional multi-bit Nyquist converter, by trading the circuit precision with speed. This technique has been widely used at audio frequen-



(a)



(b)



(c)

Figure 1.1: Direct digital RF transmitter using bandpass $\Delta\Sigma$ modulated conversion. (a) Block diagram. (b) Normalized one-bit-converter output $v(t)/V_{ref}$. (c) Normalized output power spectrum density (PSD) $(f_{clk}/V_{ref}^2)S(f/f_{clk})$.

cies. As digital circuits became faster, bandpass $\Delta\Sigma$ modulation has drawn more attention to microwave and radio frequency (RF) transmitter designs [3, 5, 6, 7, 8, 9, 10]. Using bandpass $\Delta\Sigma$ modulation was first proposed as a method to improve linearity and efficiency of a conventional radio transmitter [5]. Then, a digital radio transmitter based on the modulation was suggested to increase the system flexibility [7, 11]. A generalized high-level system block diagram of a bandpass $\Delta\Sigma$ modulated RF transmitter is shown

in Fig. 1.1, and an example $\Delta\Sigma$ modulated signal is shown in both time and frequency domains, where V_{ref} represents the DC reference voltage for the two-level DAC, and f_{clk} is the clock frequency. In this transmitter, the conventional power amplifier (PA) can be combined with the D/A converter, which can now be referred to as a power DAC, and based on the $\Delta\Sigma$ modulated pulse waveform it is thought that high power, efficiency and linearity can be achieved simultaneously using nonlinear active devices.

All mentioned advantages of $\Delta\Sigma$ modulated transmitters are based on the assumption that the circuit components are ideal. Even though electronics has been increasingly faster, it is still not fast enough to allow modeling the circuit parts as ideal components. Because of these hardware nonidealities, the analog output of the high-frequency one-bit $\Delta\Sigma$ DAC suffers from impairments, such as clock jitter (random timing error) [12] and nonlinear intersymbol interference (ISI) [13, 14], which add an inherent analog noise floor to the DAC output. The noise increases in proportion to the clock frequency.

Circuit-caused nonlinear ISI problems in DACs are more difficult to detect than jitter problems. Although the effects of circuits nonidealities on the DAC performance are analyzed in [15, 16], they are not recognized as nonlinear ISI effects. A general nonlinear ISI model for one-bit DAC is presented in [13, 14]. If a model for the circuit components and the nonlinear effects can be formulated, it can be used to evaluate the signal linearity for different DAC configurations and also guide the surrounding circuit design.

In order to alleviate the circuit speed requirements, Scholnik and Coleman adopted the multi-dimensional $\Delta\Sigma$ modulation technique from acoustic frequencies [17] and developed space-time vector $\Delta\Sigma$ modulation for RF antenna arrays [18, 19]. The main idea of the algorithm is to introduce spatial oversampling with an array of antennas in order to reduce the temporal oversampling rate.

1.1.2 Contributions

In this thesis, we focus on the design and characterization of the power DAC for an RF $\Delta\Sigma$ modulated transmitter. DAC output filter designs are discussed, as well as the antenna design for the transmitter and the antenna array input impedance characterization for the spatial-temporal $\Delta\Sigma$ modulation.

The major contributions of this work are that,

- Using the general nonlinear ISI model, a procedure to analyze the effects of circuit components on the $\Delta\Sigma$ one-bit DAC analog output signal is developed;
- Several configurations of one-bit power DACs are designed, characterized and compared;
- Different types of bandpass filtering load circuits for one-bit DACs are characterized in terms of the DAC linearity performance;

- A method to characterize antenna array input impedance matrix, especially for closely spaced array, is proposed.

1.2 Thesis Organization

The outline of the thesis is as follows:

- Chapter 2 gives detailed background information about $\Delta\Sigma$ modulation in different domains (time, space, and time-space), transmitter architectures based on $\Delta\Sigma$ modulation, work on $\Delta\Sigma$ DAC related to RF transmitters, and general nonideal hardware effects in $\Delta\Sigma$ transmitters.

- Chapter 3 presents an initial $\Delta\Sigma$ modulated single-channel wireless transmission measurement. It is a proof of concept, showing that a $\Delta\Sigma$ modulated RF signal can be directly transmitted and that the antenna operates as a suboptimal bandpass filter. Additionally, the experiment demonstrates the effects of hardware nonidealities on the analog signal spectrum. The relationship between the asymmetric transition waveform and the nonlinear intersymbol interference is discussed.

- Chapter 4 describes a procedure to analyze single-ended and differential power DACs based on the general nonlinear ISI model. First, the circuit model of the DACs is separated into two parts, where one only contains components with no memory but might be nonlinear,

and the other one contains only linear time-invariant components but associated with memory. Second, by using change of variables in the voltage and current at the separation plane, a circuit analysis is carried out in analogy with the multi-reflection analysis in transmission lines, and recursion relationships for the current at the separation plane are formulated based on the current expressions on two sides of the circuit. Based on the analytical current solution at the separation plane, nonlinear effects due to circuit components are discussed in terms of the source and load in the equivalent circuit. Finally, performances of single-ended and differential configuration power DACs are compared, with the conclusion that the differential configuration improves output analog signal linearity.

- Chapter 5 presents measurement results for single-ended and differential power DACs with both resistive and inductive bias circuits. The results confirm that the differential DACs have better linearity performance than the single-ended ones in terms of sensitivity to gate bias change. Nonlinear effects due to component mismatch are also shown in the measurements, and reduced through external control.

- Chapter 6 provides a discussion of different types (reflective and absorptive) of bandpass filter designs for both single-ended and differential DACs. Through time-domain circuit simulations, the filters are characterized for output signal linearity in terms of Q-factor and in-

band matching impedance. It is shown that for single-ended DACs, an absorptive bandpass filter is better for signal linearity, while for differential DACs, reflective bandpass filters can be used for better power efficiency. The simulation results also suggest that the first section in the reflective bandpass filter circuit should be a parallel and not a series section. The same conclusion can be drawn based on the theoretical analysis in Ch. 4. Measurement results for a differential DAC with a reflective bandpass filter are given.

- Chapter 7 summarizes the presented work and discusses the related future work, such as differential DAC fabrication in GaAs Monolithic Microwave Integrated Circuits (MMIC) TriQuint foundry technology, antenna array design and characterization for the $\Delta\Sigma$ modulated transmitters, and $\Delta\Sigma$ modulated bit sequence predistortion based on the nonlinear ISI effects from hardware nonidealities.

Chapter 2

Background

In this chapter, $\Delta\Sigma$ modulation concepts are introduced in time, space, and time-space domains, different architectures of $\Delta\Sigma$ modulated RF transmitters are described, work that has been done on $\Delta\Sigma$ DAC related to RF transmitters is reviewed, and general nonideal hardware effects in $\Delta\Sigma$ transmitters are explained.

2.1 Delta-Sigma Modulation in Different Domains

2.1.1 Temporal Delta-Sigma Modulation

Computational and signal processing tasks are now performed predominantly by digital means. However, the physical world remains stubbornly analog.

Therefore, data converters between analog and digital signals are indispensable in modern signal processing systems. Usually, data converters (both analog-to-digital and digital-to-analog) can be classified as Nyquist-rate and oversampled converters [20, 21].

For Nyquist-rate converters, there exists a one-to-one correspondence between the input and output samples. Each input sample is separately processed, regardless of the earlier input samples; the converter has no memory. The quantization noise in Nyquist-rate converters is directly related to the amplitude-sampling level. Because of practical implementation accuracy and conversion time limitations, Nyquist-rate converters cannot satisfy applications (such as digital audio) that require high resolution and linearity.

Oversampled converters, also known as (temporal) $\Delta\Sigma$ converters, are able to achieve over 20 effective number of bits resolution by fast sampling the data and spectrally shaping the quantization noise of a low-resolution (2-level) quantizer. The oversampling rate is typically 8 to 512 times faster than the Nyquist case. $\Delta\Sigma$ converters generate each output utilizing preceding input values. In order to evaluate the converter's accuracy, time-domain waveform needs to be recorded over a long enough time range, and the corresponding frequency-domain spectrum is examined. Generally, $\Delta\Sigma$ converters achieve high linearity by trading the hardware dynamic range with speed.

Although a full transmit/receive (T/R) $\Delta\Sigma$ modulated system requires both ADCs and DACs, as shown in Fig. 2.1, the work in this thesis focuses on the transmitter, and therefore DACs are of primary interest. The most

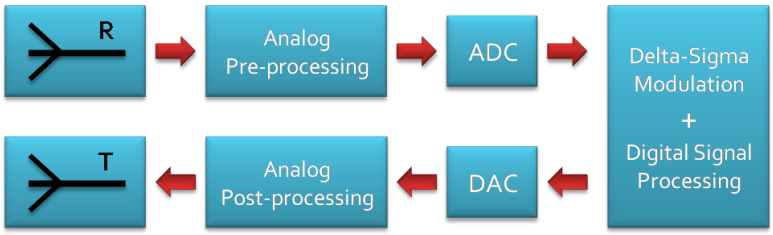


Figure 2.1: A general block diagram of a transceiver system.

common architecture for the $\Delta\Sigma$ modulator in the DAC is shown in Fig. 2.2(a) [22]. It consists of a feedback loop around a low-resolution quantizer, with a one-step delay and an LTI filter in the feedback path. The input and output $s(n)$ and $q(n)$ are both discrete time signals, where the example waveforms and spectra are shown in Fig. 2.2(b) and (c) respectively, and $e(n)$ represents the quantization error of the quantizer. It is an error feedback architecture, where the quantization error is fed back through the loop filter. Conceptually, the $\Delta\Sigma$ modulator attempts to predict the in-band portion of the quantization error, and subtracts it out before the quantizer. Thus the loop filter can also be thought as an one-step-ahead signal-band predictor.

2.1.2 Spatial Delta-Sigma Modulation

Halftoning is the process of reducing a continuous-valued image to a discrete-valued image, generally for reproduction on equipment with high spatial resolution but limited color range, such as laser and ink jet printers. In 1975, Floyd and Steinberg introduced error diffusion for halftoning grey-level images [23]. Since then, researchers have been trying to understand the mecha-

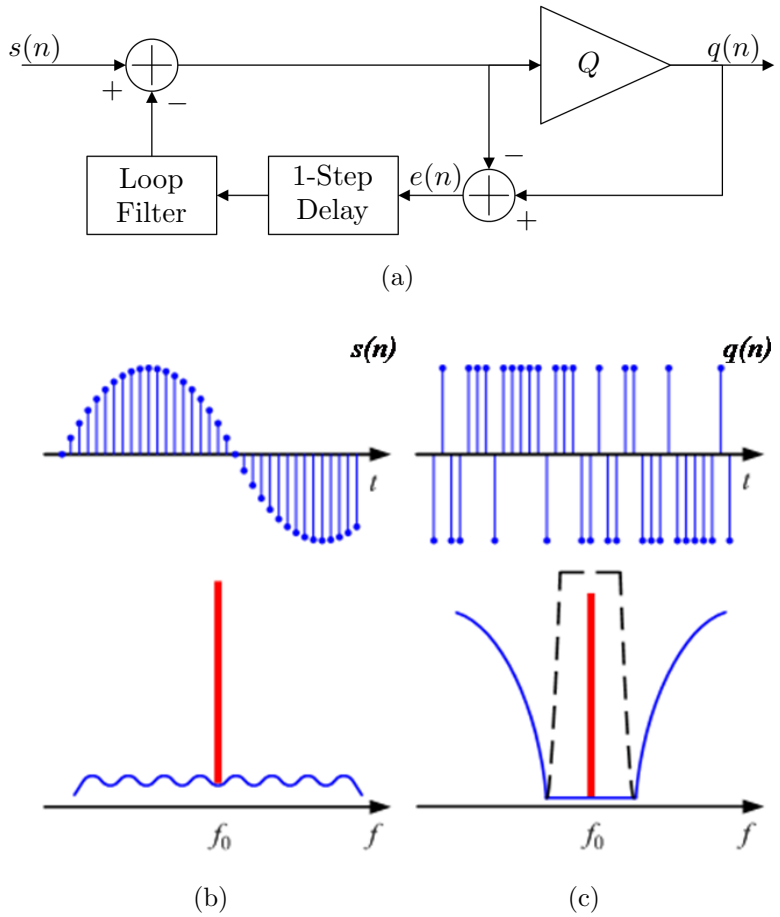
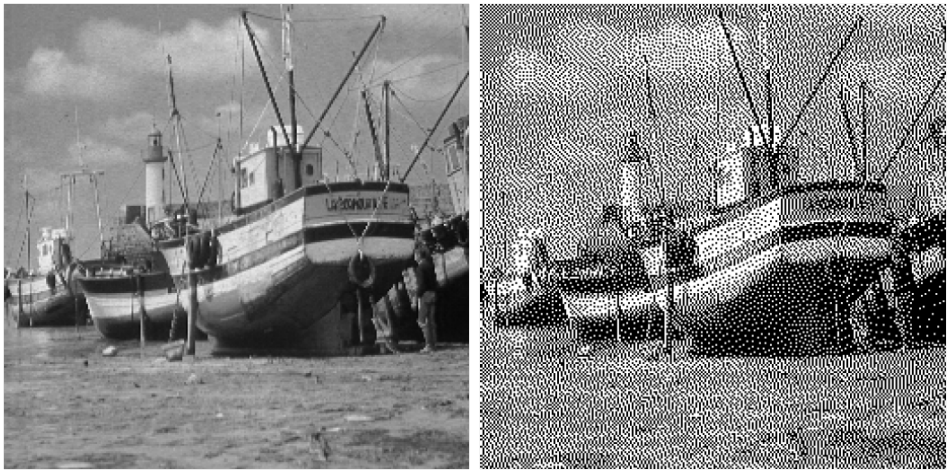


Figure 2.2: (a) Block diagram of an error feedback $\Delta\Sigma$ modulator. 'Q' represents the low-resolution quantizer. (b) Example waveform and spectrum of $s(n)$. (c) Example waveform and spectrum of $q(n)$. (In the spectrum plots, the red lines represent the signal, the blue lines represent the quantization noise, and the dashed line in (c) represents passband of $\Delta\Sigma$ modulation.)

nism of how the error filter affects the halftoned results. During the 1990s, the connection between error diffusion and $\Delta\Sigma$ modulation has been published. The equivalent circuit for error diffusion is identical to the noise shaping feedback modulator used in conventional D/A conversion [24]. Therefore, it

is also recognized as a two-dimensional (spatial) $\Delta\Sigma$ modulation.



(a) (b)

Figure 2.3: Example of Floyd-Steinberg error diffusion halftoning. ((a) original and (b) halftoned) [23]

Similar to temporal $\Delta\Sigma$ modulation in D/A conversion, which trades sample amplitude resolution with sample rate, spatial $\Delta\Sigma$ modulation in digital halftoning compromises a picture's grey-scale resolution with pixel spatial resolution. In temporal $\Delta\Sigma$ modulation, analog filters are used after the modulator to extract the wanted signals. In spatial $\Delta\Sigma$ modulation, the human eye is the equivalent low-pass filter, where the cutoff frequency is tuned as the viewing distance changes. As the example of Floyd-Steinberg error diffusion shown in Fig. 2.3, the two pictures carry the same amount of information if the viewer with normal vision stands far enough away.

2.1.3 Spatial-Temporal Delta-Sigma Modulation

After introducing temporal and spatial $\Delta\Sigma$ modulation, it is natural to consider a joint modulation scheme including both techniques. In 1998, a new beam-forming technique for an ultrasonic transmitting array using multi-dimensional $\Delta\Sigma$ modulation was introduced [17]. In 2004, Coleman and Scholnik derived theoretically the vector format temporal and spatial $\Delta\Sigma$ modulation algorithm for RF and microwave transmitters [18, 19].

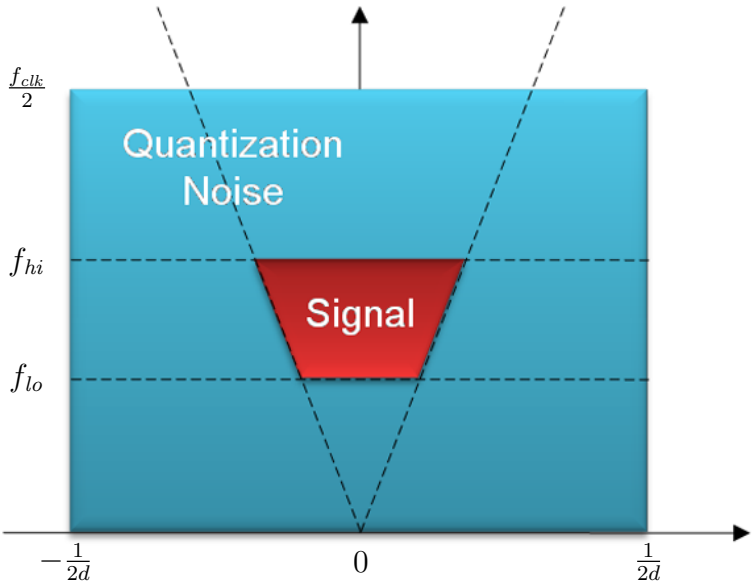


Figure 2.4: Signal and noise geometry for a spatial-temporal $\Delta\Sigma$ modulated transmitter, where $f_{hi,lo} = f_{clk} \pm f_{BW}/2$

The spatial-temporal $\Delta\Sigma$ modulator block diagram is the same as the one in Fig. 2.2, except that now all the signals are $M \times 1$ vectors, the quantizer is a vector quantizer, and the loop filter is an $M \times M$ matrix, where M repre-

sents the number of antenna elements in the transmitter. The details of the derivation can be found in [22]. Briefly, the quantization noise is shaped in a multi-dimensional (space-time) frequency domain as illustrated in Fig. 2.4, where the x-axis represents the temporal frequency, and the y-axis represents the spatial frequency. The signal clock period T is the temporal sampling spacing, and the antenna element distance d is the spatial sampling spacing. The rectangular region defined by limits $[0, 1/2T]$ and $[-1/2d, 1/2d]$ corresponds to the fundamental Nyquist band in spatial-temporal frequency domain. The trapezoidal region corresponds to the transmitted signal bandwidth, and the region outside of the trapezoid represents the quantization noise. The signal SNR is determined by the multi-dimensional over-sampling ratio (OSR), which is the product of the OSR in time and space domains, defined as

$$OSR_{time} = \frac{f_{clk}}{2f_{BW}}, \tag{2.1}$$

$$OSR_{space} = \frac{\lambda_0}{2d}, \tag{2.2}$$

where f_{clk} is the clock speed and equal to $1/T$, f_{BW} is the one-sided signal bandwidth, and λ_0 is the wavelength at the center frequency of the signal band.

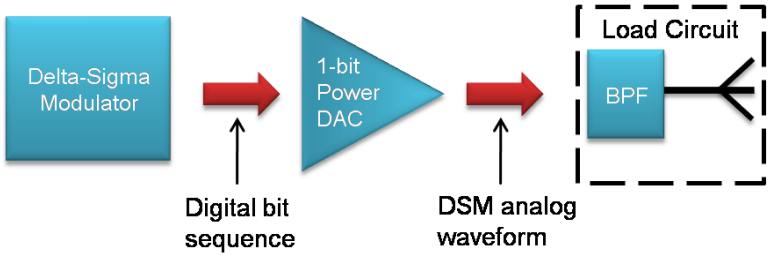


Figure 2.5: Block diagram of a single-channel temporal $\Delta\Sigma$ modulated RF transmitter.

2.2 Bandpass Delta-Sigma Modulated RF Transmitters

A generalized high-level system block diagram of a single-channel bandpass $\Delta\Sigma$ modulated RF transmitter is shown in Fig. 1.1(a), and for convenience repeated here in Fig. 2.5. The system can be divided into three stages: $\Delta\Sigma$ modulation, power DAC, and bandpass filter. The $\Delta\Sigma$ modulation, also known as noise-shaped coding, reduces a high-resolution digital signal to a low resolution digital signal, and the large amount of quantization noise that results from the coarse quantization is spectrally shaped to minimize interference with the signal. The second stage is a one-bit power DAC, which translates the digital signal into an analog pulse waveform with some power gain. The last stage is the load circuit, or analog filtering, which ideally removes all the out-of-band quantization noise and linearly passes the in-band signal. The analog filtering is dependent on how the DAC is implemented. To briefly explain this, let us consider the operating region of

the active device used to implement the DAC. If it is driven in the linear region, the efficiency of the modulator will be low, because of the power dissipation within the active device, and the filter design is straightforward. If the device is driven in the nonlinear region to increase its power conversion efficiency, then the filter design is not independent of the DAC design, as will be shown in Chs. 4 and 6.

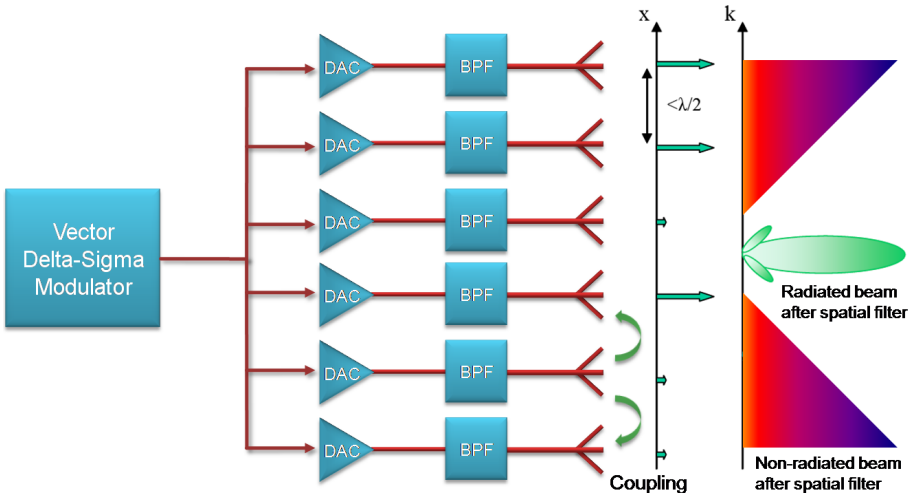


Figure 2.6: Block diagram of an multi-channel spatial-temporal $\Delta\Sigma$ modulated RF transmitter.

The block diagram of a multi-channel bandpass $\Delta\Sigma$ modulated RF transmitter with spatial-temporal $\Delta\Sigma$ modulation is shown in Fig. 2.6. The hardware implementation for the multi-channel spatial-temporal $\Delta\Sigma$ modulated transmitter is strongly dependent on the single-channel case, and the coupling effect between the closely-spaced antenna element needs to be taken into account for the single-channel design, because it changes the input impedance of the load circuit. Most of the effort of this work is spent on studying and

analyzing the circuit components for a single-channel $\Delta\Sigma$ modulated RF transmitter.

2.3 Delta-Sigma DAC Literature Review

DAC design is crucial for the $\Delta\Sigma$ transmitter implementation. Among the related literature, an RF DAC with 60 dB in-band SNR measured at 942 MHz with 17.5 MHz bandwidth is demonstrated in [25]. This converter cannot be directly utilized for $\Delta\Sigma$ RF transmitters due to low output power and efficiency. Using switching-mode active devices with $\Delta\Sigma$ signals to achieve both high linearity and efficiency for power amplifiers (PA) is presented in [26, 27], where both simulated and measured results suggest that it is a very promising approach. Different class-D PA topologies for one-bit bandpass $\Delta\Sigma$ D/A converters are compared in [28] in terms of the power efficiency. Analytical design equations for an efficient RF complementary voltage-switched class-D amplifier with $\Delta\Sigma$ driven signals are derived in [29]. An H-bridge class-D PA with over 30% drain efficiency when driven by a $\Delta\Sigma$ modulator is presented in [30], where detailed analysis of the PA efficiency is given. GaAs-HBTs and GaN-HEMTs are used to implement switching-mode amplifiers and efficencies are compared under $\Delta\Sigma$ drive in [31]. Other high-efficiency 50% duty cycle switched-mode linearied RFPAs have been demostrated up to X-band in, e.g. [32, 33].

Among the above listed work, little attention is paid to the signal linearity

in terms of nonlinear ISI. Nonlinear ISI in the one-bit $\Delta\Sigma$ modulated DAC is studied by Gupta and Collins in [34, 35]. In the work, a set of distinct sequences are creatively generated to measure different orders of nonlinear ISI in the DAC hardware, and methods to reduce such nonlinear effects are proposed in terms of signal generation, but, from the circuit point of view, causes of the nonlinear ISI was not the focus.

2.4 Hardware Nonidealities in Delta-Sigma Transmitters

As mentioned in Ch. 1, nonlinear effects in $\Delta\Sigma$ DACs are caused by hardware nonidealities and shown as nonlinear ISI and random jitter. Here, we list the possible nonideal hardware effects in $\Delta\Sigma$ transmitters as following:

- system clock with jitter,
- additive phase noise of the system components,
- finite operating bandwidth of the components,
- parasitics of the components, especially parasitic reactances,
- loss in the components and environment temperature change.

The first two items are probably related to random jitter effect, and the third and fourth items could be the causes of nonlinear ISI effect. In the

later chapters of this thesis, more detailed examination of the relationship between these hardware nonidealities and nonlinear effects in DACs will be given.

Chapter 3

Direct Digital Link Transmitter

3.1 Introduction

This chapter presents simulations and measurements for a single channel of a directly-transmitted RF frequency $\Delta\Sigma$ modulated signal. A high performance commercial Field Programmable Gate Array (FPGA) is used to generate 2 Gb/s $\Delta\Sigma$ bit sequences. The signal bandwidth is 25 MHz. Retiming circuitry is implemented to reduce jitter, and a variety of hardware effects on the SNR are studied. Since many potential applications, such as radar and arbitrary waveform generation, require pulsed or repeated waveforms, the effect of finite length $\Delta\Sigma$ sequences on output signal spectra is examined.

3.2 Ideal Delta-Sigma Modulated Single-Channel Transmitter

The single channel system, which is the focus of this chapter, is shown in Fig. 3.1. The quantization noise due to one bit quantization is shaped in the time frequency domain to be out of the signal band that is radiated by the antenna. The *noise-shaping function* $h(n)$ and its discrete-time Fourier transform $H(f)$ are defined as

$$h(n) = \delta(n) - g(n-1), \tag{3.1}$$

$$H(f) = 1 - G(f)e^{-j2\pi f}, \tag{3.2}$$

The output signal of the $\Delta\Sigma$ modulator $q(n)$, which is a binary bit sequence with levels {-1, 1}, and its *power spectral density* (PSD) $R_q(f)$ are

$$q(n) = s(n) + (h * e)(n), \tag{3.3}$$

$$R_q(f) = R_s(f) + \sigma^2|H(f)|^2, \tag{3.4}$$

where the quantization noise is assumed to be white noise with power spectral density σ^2, and $R_s(f)$ is the PSD of $s(n)$. Ideally, the output signal of the digital/analog converter $y_t(t)$ has the power spectrum

$$R_y(f) = \frac{1}{T}R_s(f) + \frac{\sigma^2}{T}|H(f)|^2. \tag{3.5}$$

The theoretical spectrum $R_y(f)$ of a bandpass $\Delta\Sigma$ modulated test signal is shown in Fig. 3.2. For the direct transmission test, the band of interest is centered at 500 MHz, which is one quarter of the digital clock rate 2 Gb/s.

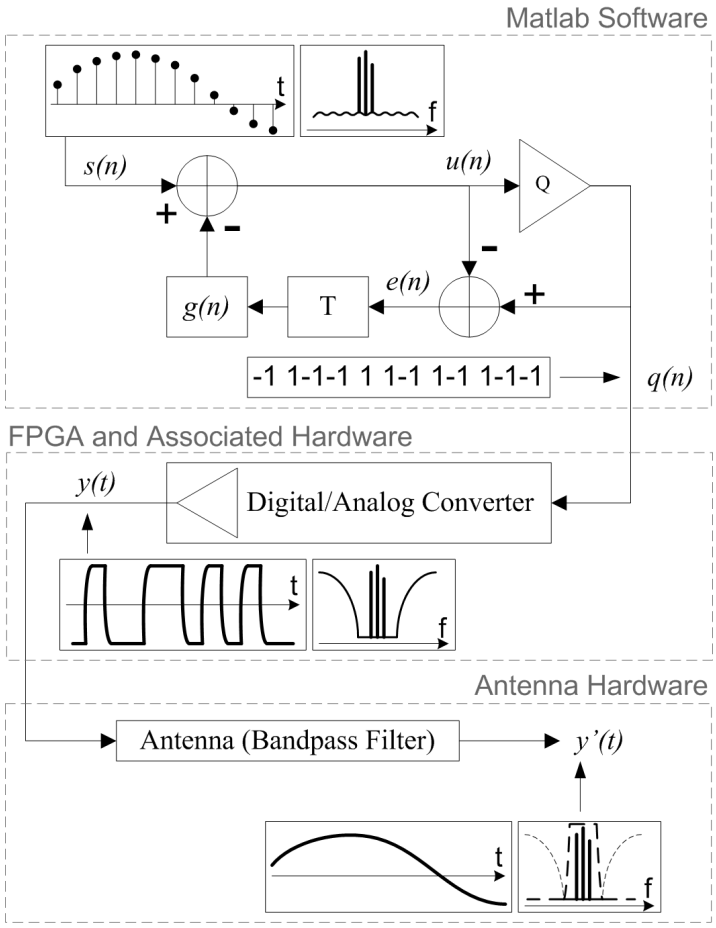


Figure 3.1: Single-channel system block diagram. Digitized three-tone signal $s(n)$ is $\Delta\Sigma$ encoded in software resulting in a one-bit digital signal $q(n)$. The digital signal is converted to an analog signal $y(t)$ through a binary digital/analog converter. A sketch of the time domain signal and noise shaped spectrum are shown in the inset. The antenna that follows is a bandpass filter which filters the noise and radiates the signal $y'(t)$.

The windowed $\Delta\Sigma$ signal spectral density can be expressed as $S_{qw}(f) = E[\hat{R}_q(f)]$, where $E[\ ]$ denotes expectation (average) and

$$\hat{R}_q(f) = \frac{\left| \sum_{n=0}^{N-1} w(n)q(n)e^{-j2\pi fn} \right|^2}{\|w\|_2^2}, \tag{3.6}$$

where $w(n)$ represents the window function, and $\|w\|_2^2$ is the energy of the window. Substituting (3.3), $S_{qw}(f)$ can be rewritten as

$$S_{qw}(f) = \frac{1}{\|w\|_2^2}|W(f) * R_s(f)|^2 + \frac{\sigma^2}{\|w\|_2^2}|W(f)|^2 * |H(f)|^2. \tag{3.7}$$

Detailed derivation of (3.7) can be found in [22]. Its first term illustrates the window effect to the signal spectrum (signal leakage), and the second term shows the effect to the noise spectrum (noise leakage).

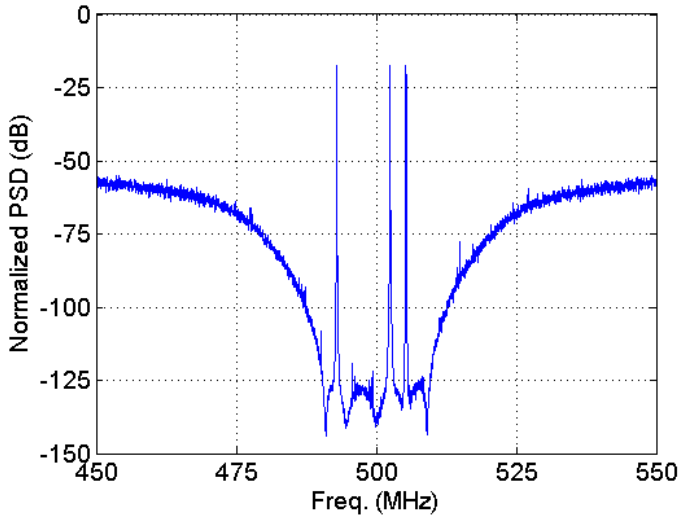


Figure 3.2: Ideal spectrum for the bandpass $\Delta\Sigma$ modulated three-tone test signal centered at 500 MHz with 20 MHz bandwidth, where the tones are at 493 502.5 and 505.3 MHz respectively.

3.3 Implementation and Measurement Results

A block diagram of the hardware implementation is shown in Fig. 3.3. The development board has a Virtex-II Pro XC2VP30 hybrid chip which contains both FPGA fabric as well as dual Power PC processors. The chip has RocketIO^{TM}differential serial transceivers capable of a 3.125 Gb/s transmit rate, as well as DDR memory to support large throughput requirements. An external differential clock input allows us to connect an extremely stable clock source, and thereby allows for an arbitrary transmit rate (up to the maximum capability of the hardware). For these experiments, the external clock was set to 2 GHz to create the 2 Gb/s bit transmit rate. The external clock is configured as the input to the RocketIO^{TM}transceiver, but since the transceiver includes a 20-bit parallel to serial converter (implemented with an on-chip 20$\times$ clock multiplier), we set our clock source to the desired switching rate and divide it by 20 with frequency dividers before connecting it to the input of the FPGA board.

Software running on one of the Power PC cores communicates on a simple RS-232 serial interface to a desktop PC for control and data download. After the user downloads a bit sequence to memory, a looping process is enabled that continually reads data from memory and sends it to the transceiver without interruption. In this way, a pure $\Delta\Sigma$ bit sequence is transmitted continuously. For our measurements, sequence length is limited to 983040

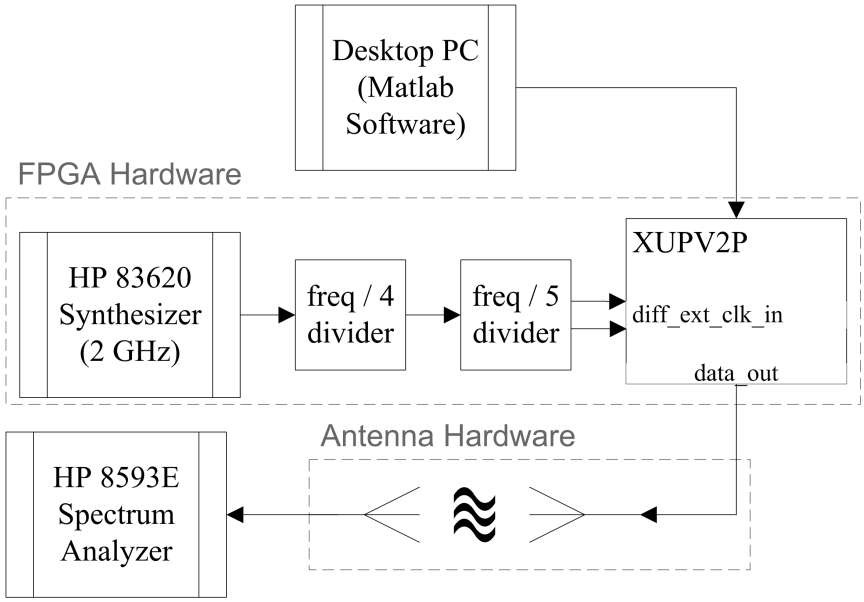


Figure 3.3: $\Delta\Sigma$ single channel hardware block diagram. The PC generates the $\Delta\Sigma$ bit sequence. The FPGA hardware generates the $\Delta\Sigma$ waveform. Antenna hardware is the bandpass filter for the signal.

(60/64 of 1 MB) bits because of the limitation on the data storage size of the FPGA board.

The output of the FPGA is connected to the transmit half of a wireless link, from which the received signal is captured and displayed by a spectrum analyzer. Fig. 3.5 shows the spectra of the signals both before and after the wireless link. The transmit and receive antennas are quarter-wave monopoles above one-wavelength square ground planes. These test antennas have sufficient bandwidth for the sample signal. The wireless link is a bandpass filter, therefore the shaped quantization noise power is filtered before it is radiated. A small amount of the characteristic $\Delta\Sigma$ shape is still discernible in the

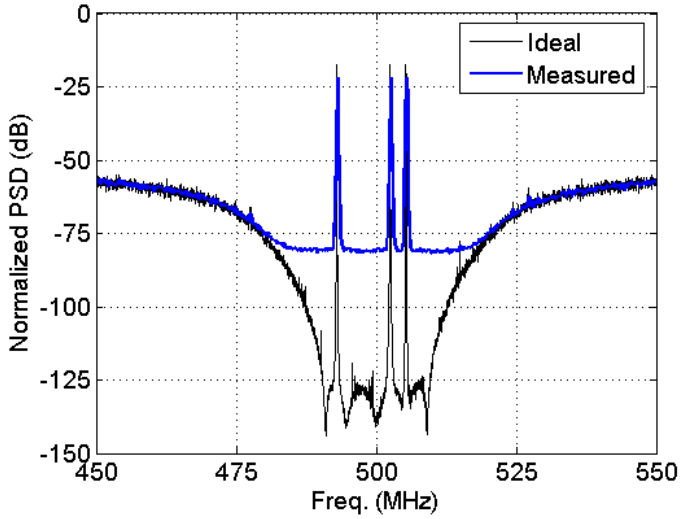


Figure 3.4: The ideal bandpass $\Delta\Sigma$ modulated test signal spectrum overlaid with the measured spectrum. The adopted hardware cannot produce the ideal spectrum, but the goal here is to determine what causes the $> 50\,\mathrm{dB}$ rise in in-band noise, and how it can be reduced.

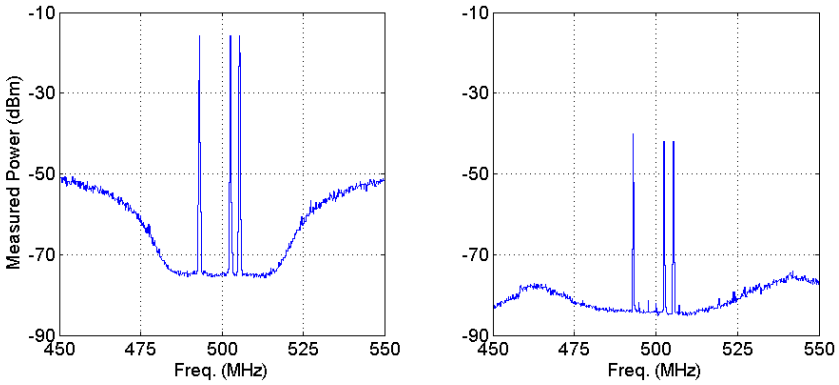


Figure 3.5: Measured bandpass $\Delta\Sigma$ modulated test signal spectra before (left) and after (right) the antennas.

received spectrum because the antenna does not perform as an ideal filter. Based on the Friis transmission equation, we expect the received power to be

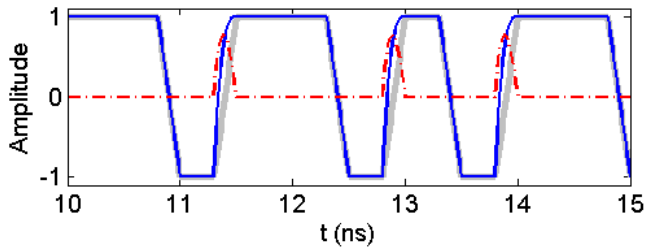
at least 22 dB lower than the transmitted power, assuming perfect impedance matching, polarization matching, and coplanar monopoles. It can be seen in Fig. 3.5 that the received power level is about 25 dB below the transmitted power, as expected.

3.4 Analysis of Hardware Effects

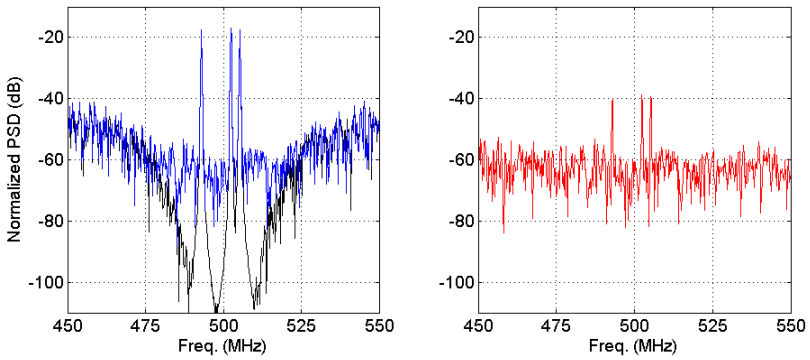
The $\Delta\Sigma$ spectrum is very sensitive to the variance of the waveform generated at the output of the linear pulse modulator. Different nonidealities introduced by the hardware can corrupt the ideal spectrum depending on their relative amplitude level to the expected in-band SNR. Asymmetry of the waveform and random jitter issues are what we mainly focus on in the analysis of influence from hardware because they are the most common problems that degrade the $\Delta\Sigma$ spectrum [12]. All the simulations are done based on the switching characteristics of the RocketIO^{TM}transmitter block on the XUPV2P development board [36].

3.4.1 Waveform Asymmetry

Waveform asymmetry of $\Delta\Sigma$ sequences can be interpreted as different rise and fall edge shapes or times. Their effects are simulated in Matlab by using a 10,000 bit three-tone $\Delta\Sigma$ sequence. Figure 3.6 shows that the noise shaping spectrum degradation caused by waveform asymmetry is determined by the amplitude of the signal that is the difference of the ideal waveform and



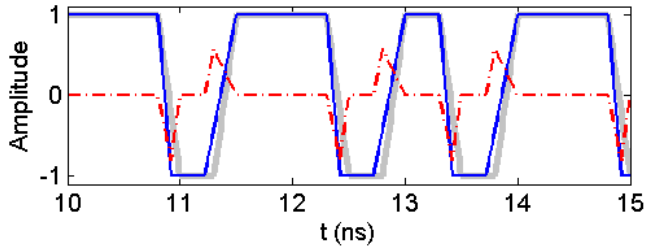
(a)



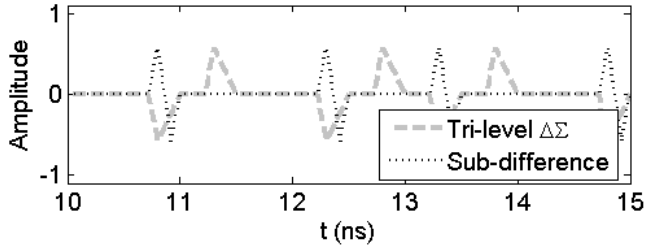
(b)

Figure 3.6: Simulated waveforms (a) and spectra (b) of $\Delta\Sigma$ sequence with asymmetric transition shapes. (The black lines are the symmetric case, the blue lines are the asymmetric case, and the red lines represent the difference signal between the symmetric and asymmetric cases. Parameters are chosen based on [36].)

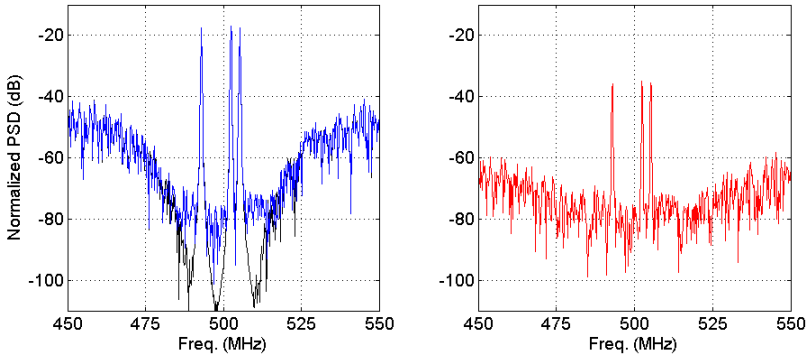
the generated waveform, correlated with the ideal waveform. The difference signal for the asymmetric time case can be decomposed into a symmetrical tri-level $\Delta\Sigma$ signal and the remainder, which we call the sub-difference signal as in Fig. 3.7(b). It is this sub-difference signal that causes the ideal noise notch to be obscured, as shown on the right side of Fig. 3.7(c).



(a)

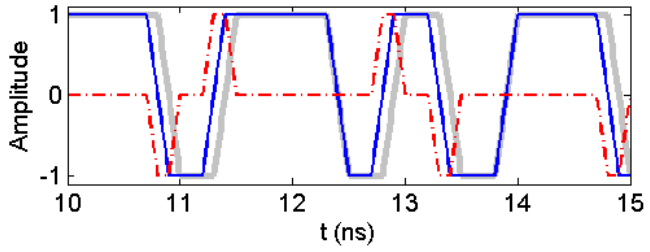


(b)

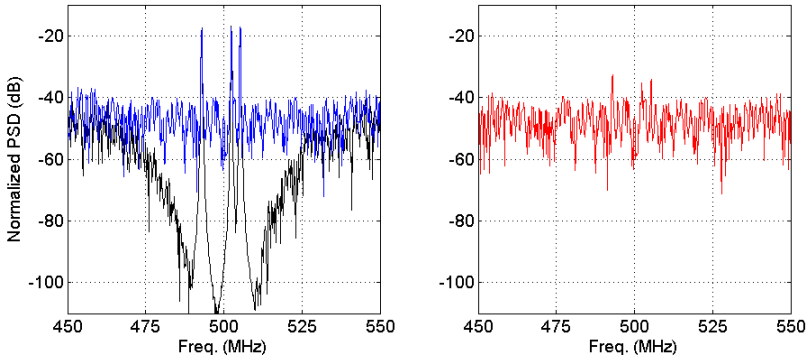


(c)

Figure 3.7: Simulated waveforms (a) and spectra (c) of $\Delta\Sigma$ sequence with asymmetric transition times. (b) Sub-difference components. (Legends are the same as in Fig. 3.6, and parameters are chosen based on [36])



(a)



(b)

Figure 3.8: Simulated random jitter waveform (a) and spectra (b) of $\Delta\Sigma$ sequence with random jitter effect. (Legends are the same as in Fig. 3.6, and parameters are chosen based on [36])

3.4.2 Random Jitter

Random jitter is the jitter introduced by the accumulation of random processes inside the system. In our simulation, we analyze the effect of random jitter by assuming that it is sufficiently small so as to not cause a bit error in the sequence. From the results shown in Fig. 3.8, it can be seen that the random jitter effect is similar to the effect of waveform asymmetry in that it also decreases the SNR inside the notch and is determined by the differ-

ence signal. However, the random jitter shows a much stronger distortion of the spectrum here simply because the difference pulse sequence has a much larger amplitude.

3.4.3 Hardware Improvements

From the above results, it can be seen that the influence of the hardware can be quantified based on the difference signal amplitude and its correlation to the $\Delta\Sigma$ sequence. Random jitter shows a stronger effect on the spectrum degradation, compared to other nonidealities. In order to reduce its effect, a cleaner clock source has to be used in signal generation, and re-timing circuitry can be added to the output of the linear pulse modulator to further reduce the jitter. To reduce the effect of waveform asymmetry, either a balanced differential configuration system or a different pulse waveform, like return-to-zero (RZ) pulses, can be used [37]. However, disadvantages of these approaches are a higher requirement on the circuit symmetry and the clock frequency, respectively.

Jitter can be related to the phase noise of the clock (oscillator) [38]. The FPGA clock was measured to have a poor phase noise of -65 dBc/Hz at 10 kHz offset, which corresponds to the roughly 50 dB increase in noise floor (Fig. 3.8). The top plot in Fig. 3.9 shows the measured eye diagram for this case. When an HP 83620 synthesizer is connected to the external clock input of the FPGA, the eye diagram improves (center plot in Fig. 3.9). This would correspond to over 20 dB improvement in noise floor. To further reduce the

effect of jitter, a re-timing circuit is added at the output of the FPGA. The circuit consists of a high-speed D flip-flop (ONSemi MC100EP52) and the resulting eye diagram is shown in Fig. 3.9 for comparison. The D flip-flop is designed to operate into a broadband 50-Ω load, and thus needs to be matched to operate with the antenna.

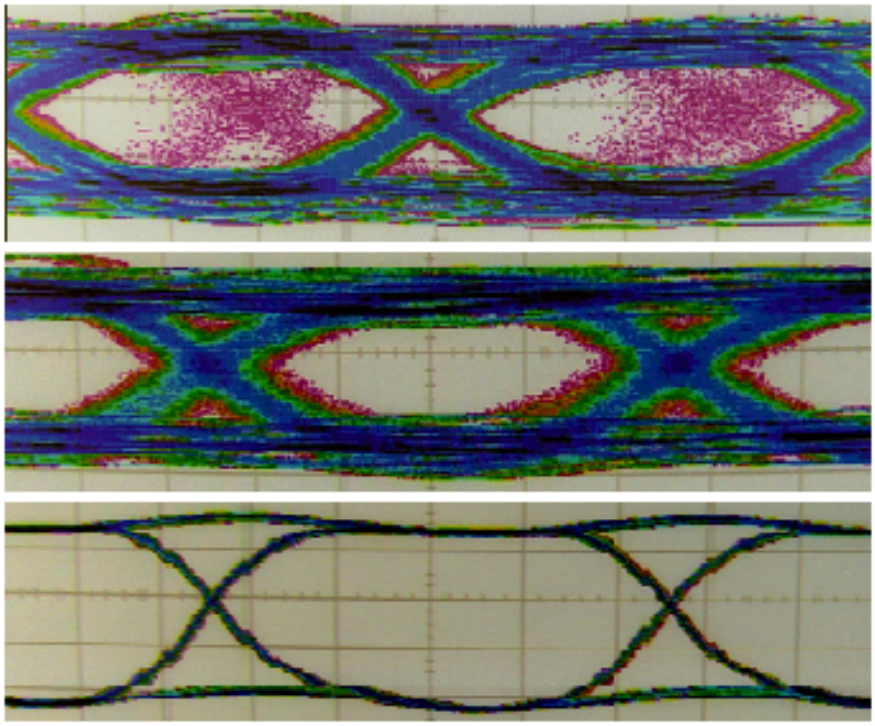


Figure 3.9: Measured eye diagrams for on-board clock (top), external clock (center), and external clock with retiming circuit (bottom). Scale is 200 mV/div, 100 ps/div.

3.5 Conclusions and Discussions

3.5.1 Conclusions

In summary, we have demonstrated a 2 Gb/s $\Delta\Sigma$ modulated directly digitally driven wireless link. It is a proof of concept, showing that $\Delta\Sigma$ modulated RF signal can be directly transmitted and that the antenna works as a band-pass filter. Hardware nonidealities in the system, like asymmetric transition edges of the waveform and clock jitter, are diagnosed, and the corresponding nonlinear effects on the analog signal spectrum are studied. The clock jitter can be improved by a better signal clock and, additionally, using an external re-timing circuit.

3.5.2 Discussions

The nonlinear effects caused by different rise and fall edges of the waveform is actually a type of nonlinear intersymbol interference (ISI). A simple discussion of the relationship between the asymmetric transition waveforms and nonlinear ISI is given here as an introduction to the more detailed derivation in the next chapter.

In DACs, a linear time-invariant D/A conversion is defined as

$$s(t) = \sum_n d(n)u(t - nT), \tag{3.8}$$

where $s(t)$ is the analog output signal, $d(n)$ is the binary digital bit sequence with values $\{-1, 1\}$, T is the digital clock period, and $u(t)$ represents the

analog unit pulse waveform.

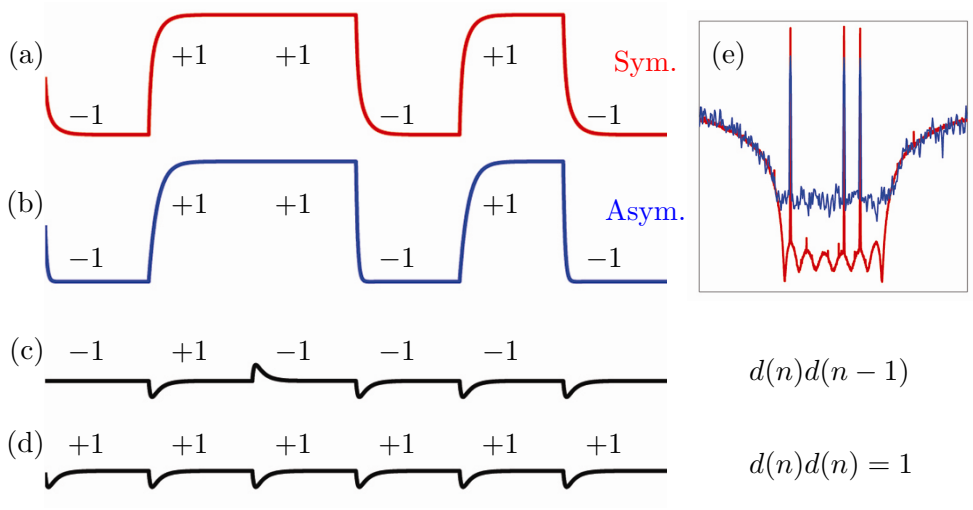


Figure 3.10: Nonlinear ISI from the output waveform of an one-bit converter with one-clock memory. (a) Symmetric rise, fall transition waveform. (b) Asymmetric rise, fall transition waveform. (c) Second-order nonlinear ISI component. (d) Data-independent component. (e) Normalized PSD for symmetric and asymmetric cases for a three-tone test signal (the axes limits and labels are the same as in Fig. 1.1(c)).

Suppose the one-bit converter output looks like that in Fig. 3.10(a), with mirror image rise and fall waveforms that settle in less than the RF clock period T. In this case, the unit pulse width is less than $2T$. The spectrum looks like the lower curve in Fig. 3.10(e). An output corresponding to nonideal conversion is shown in Fig. 3.10(b), with fall time shorter than the rise time. This (b) waveform can be modeled as the sum of the (a), (c),

and (d) waveforms:

$$
\begin{aligned}
s(t) = &\sum_n d(n)u_1(t-nT) && \Big\}\text{(a) linear term} \\
&+\sum_n d(n)d(n-1)u_2(t-nT) && \Big\}\begin{matrix}\text{(c) } 2^{nd}\text{-order} \\ \text{nonlinear term}\end{matrix} \\
&+\sum_n u_0(t-nT) && \Big\}\begin{matrix}\text{(d) data-indep.} \\ \text{(nonlinear) term.}\end{matrix}
\end{aligned} \tag{3.9}
$$

Nonlinear ISI term (c) in (3.9) raises the signal-band noise floor from the lower to the upper curve in Fig. 3.10(e). In practice, very small asymmetries, as shown in the previous section, can raise the floor of a deep signal-band noise notch by 20 dB or more [13].

Fig. 3.11 generalizes this waveform nonlinear ISI to longer nonlinear memories [13, 14]. This model enables simple estimates of nonlinear spectral effects of $\Delta\Sigma$ modulated D/A conversion. Some standard linearity measures, such IP3 and IP5, assume a power-type nonlinearity and thus are not meaningful in the context of a one-bit RF DAC. Others, such as ACPR and EVM, can be used to characterize linearity for specific applications but are less useful in understanding and predicting the fundamental underlying nonlinear effects. In this thesis, an attempt has been made to develop a more intuitive model specifically for $\Delta\Sigma$ modulated signal nonlinearities.

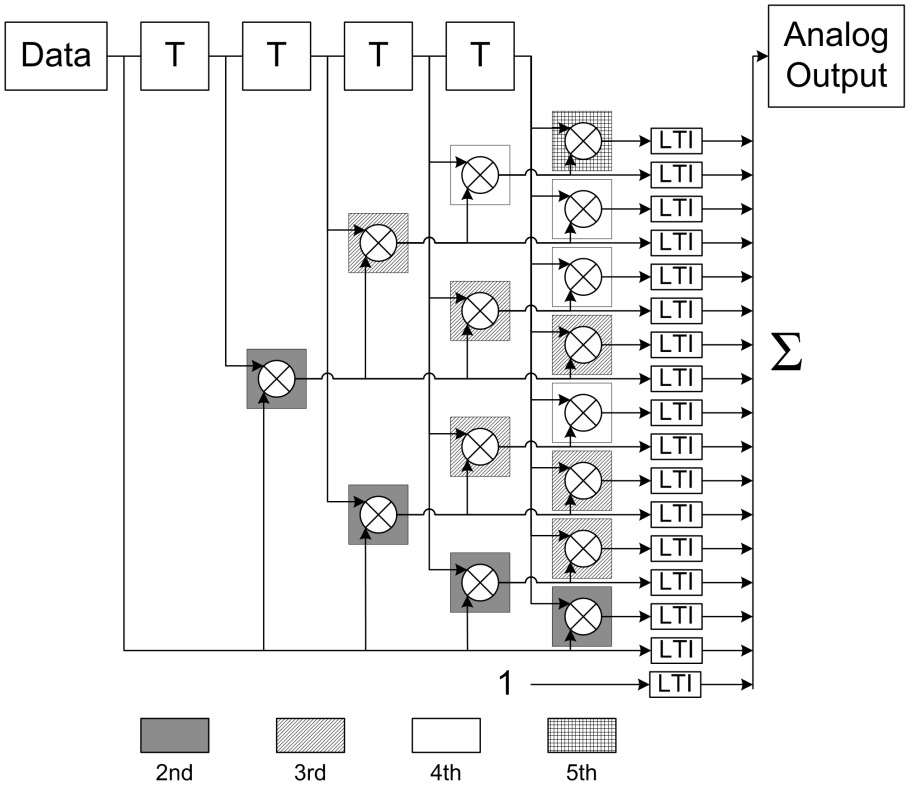


Figure 3.11: Generalized nonlinear-ISI model for time-invariant D/A conversion with $L = 4$ clock memory. Each LTI output uses its own unit pulse responses to map its discrete-time input data to the continuous-time output. The total analog output is the sum of all the LTI responses. The model is parameterized by the memory length L and the unit pulse responses. The number of expansion terms of the model is equal to $2^L + 1$.

Chapter 4

Nonlinear ISI Analysis for One-Bit DAC Circuits

4.1 Introduction

The published work on power amplification with nonlinear active devices and $\Delta\Sigma$ modulation at RF, overviewed in Ch. 2 background discussion, has focused on the power efficiency of the active circuit, where very little attention was drawn to the signal linearity. However, the advantage of providing high signal linearity is the fundamental reason for using bandpass $\Delta\Sigma$ modulation in RF transmitters. In order to draw attention to the signal linearity, we refer to the active circuit as an RF power DAC instead of a PA.

To illustrate the fundamental generation of nonlinear ISI in a DAC, consider a simple equivalent circuit in Fig. 4.1(a), where a DC bias current I_b

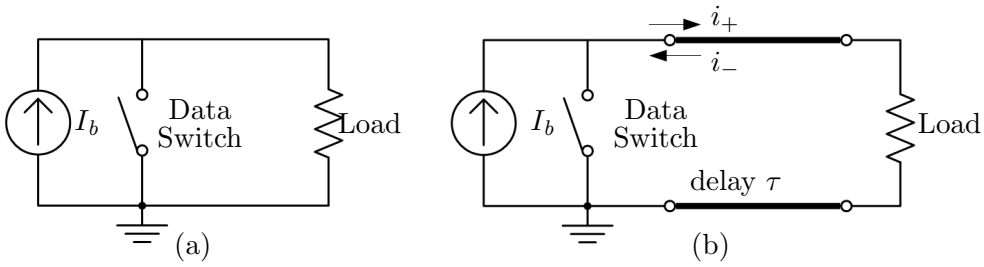


Figure 4.1: Simple one-bit DAC ideal circuit models: (a) linear (b) nonlinear.

is data-switched through the load. Now a simple memory in the form of a transmission-line delay is added between the DAC and the load, as in Fig. 4.1(b). If the load is matched to the transmission line, circuit in Fig. 4.1(b) reduces to (a), where no nonlinear ISI will be generated. However, if there is mismatch, the modulated forward current $i_+(t)$ is reflected from the load to create a modulated reverse current $i_-(t)$, which is now again modulated by the data-controlled switch. After N round trips an N^{th}-order nonlinear ISI component proportional to $\rho(t-\tau)\rho(t-3\tau)\cdots\rho(t-(2N-1)\tau)$ enters the load. Here, in such a simple model, the transmission-line delay created the nonlinear ISI. In practice, parasitic reactances inside the DAC have similar nonlinear effect, which will be shown in the later sections.

In this chapter, the concepts and circuits for ultra-linear one-bit conversion at UHF clock rates, using approaches scalable to microwave clock rates, are presented. Based on the general DAC nonlinear model presented in Ch. 3, nonlinear intersymbol interference (ISI) generated in RF one-bit DACs is studied. An intuitive circuit analysis approach is introduced for analyzing

the nonlinear ISI effects in single-ended and differential DACs.

4.2 Single-Ended One-Bit Power DAC

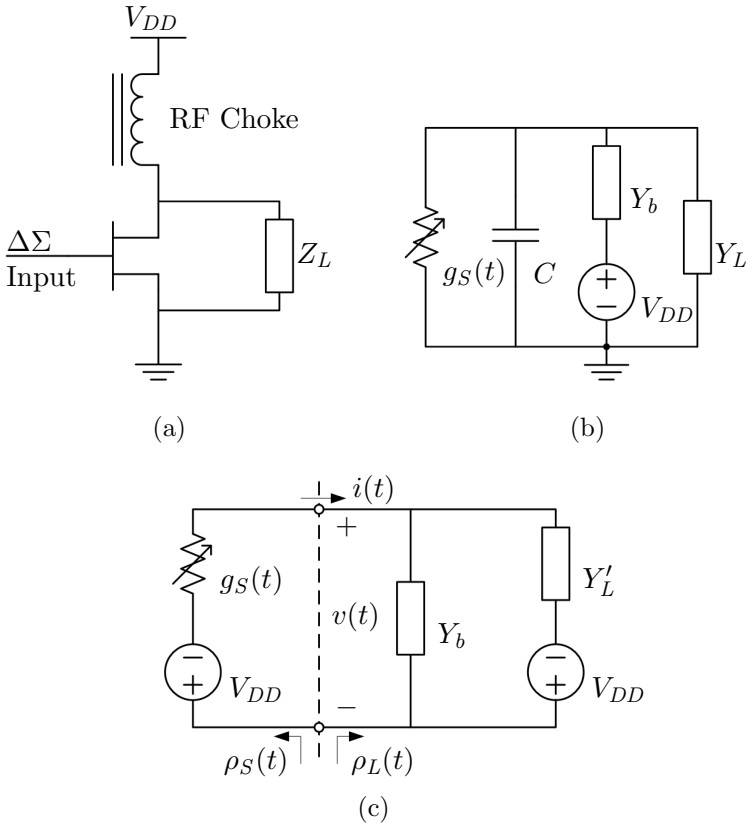


Figure 4.2: Single-ended one-bit DAC circuit diagram (a), simplified circuit model (b), and equivalent circuit model (c). ($Y_L = 1/Z_L$)

In this section, first an approximate circuit model for a single-ended power DAC is formulated. The output signal expression is solved in the time domain, and a description of different nonlinear effects follows.

The circuit diagram of a single-ended converter is shown in Fig. 4.2(a). Ideally, a transistor can be modeled as a perfect switch when it is driven by large binary digital signals. However, at RF frequencies, this model is inaccurate. A simplified circuit model for the converter is shown in Fig. 4.2(b). The transistor is modeled as a time varying conductance $g_S(t)$ in parallel with an output capacitance C. The input of the circuit is modeled by $g_S(t)$ which changes between the steady state conductances g_{on} and g_{off}, with transitions $g_{rise}(t)$ and $g_{fall}(t)$. The output capacitance C is assumed to be linear and equal to C_{ds} in parallel with the series capacitance of C_{gs} and C_{gd}. The RF choke of the bias circuit is represented by Y_b. The DC block and the load of the converter are combined together and labeled as Z_L and Y_L in Fig. 4.2(a) and (b), respectively.

4.2.1 Current Solution at The Reference Plane

To better understand the converter-generated nonlinear ISI, by changing the reference ground, an equivalent circuit model is formulated as in Fig. 4.2(c), and

$$Y_L'(s) = Y_L(s) + sC. \tag{4.1}$$

In the equivalent circuit model, a reference plane is inserted as indicated by the dashed line. The source circuit consists of V_{DD} and $g_S(t)$ which is time varying but memoryless. The load circuit is LTI but reactive, resulting in memory.

Key to the detailed analysis below is the use of the alternative circuit variables $i^+(t)$ and $i^-(t)$ defined by the change-of-variable relationship

$$\begin{pmatrix} i(t) \\ v(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix} \begin{pmatrix} i^+(t) \\ i^-(t) \end{pmatrix}, \tag{4.2}$$

where R_{ref} is an arbitrary reference impedance, but a proper choice of R_{ref} can simplify the nonlinear ISI analysis, which will be shown later. By writing KCL to characterize the source and load sides in the time and Laplace domains respectively, we obtain

$$i(t) = -g_S(t)(v(t) + V_{DD}), \tag{4.3}$$

$$I(s) = Y_t(s)V(s) + Y'_L(s)V_{DD}(s), \tag{4.4}$$

where

$$Y_t(s) = Y_b(s) + Y'_L(s). \tag{4.5}$$

Since we are interested in the steady state response of the circuit, if V_{DD} is an ideal DC voltage source, and because the load circuit is AC coupled to the transistor, then (4.4) can be simplified as

$$I(s) = Y_t(s)V(s). \tag{4.6}$$

After change of variables, $i^+(t)$ and $i^-(t)$ are solved respectively as

$$i^+(t) = \rho_S(t)i^-(t) - m(t)V_{DD}/(2R_{ref}), \tag{4.7}$$

$$I^-(s) = \mathcal{R}_L(s)I^+(s), \tag{4.8}$$

$$i^-(t) = \rho_L(t) * i^+(t), \tag{4.9}$$

where

$$\rho_S(t) = (1 + R_{ref} g_S(t))^{-1}(1 - R_{ref} g_S(t)), \tag{4.10}$$

$$m(t) = (1 + R_{ref} g_S(t))^{-1} 2R_{ref} g_S(t), \tag{4.11}$$

$$\mathcal{R}_L(s) = (1 + R_{ref} Y_t(s))^{-1}(1 - R_{ref} Y_t(s)), \tag{4.12}$$

and $*$ denotes continuous-time convolution, while $\rho_L(t) \leftrightarrow \mathcal{R}_L(s)$ is a Laplace transform pair.

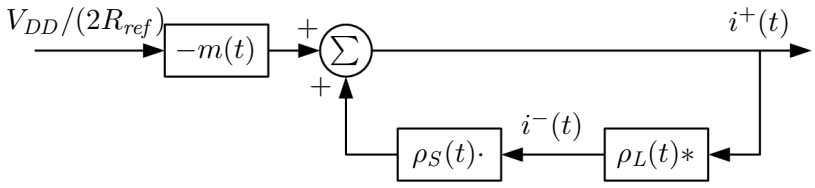


Figure 4.3: Transfer function block diagram of the positive current. ('$\cdot$' denotes a time domain product, and '$*$' denotes a continuous-time convolution.)

Based on (4.7) and (4.9), a transfer function block diagram is shown in Fig. 4.3. By straightforward substitution, $i^+(t)$ and $i^-(t)$ can be expressed as

$$i^+(t) = \sum_{k=0}^{\infty} i_k^+(t), \tag{4.13}$$

$$i^-(t) = \sum_{k=1}^{\infty} i_k^-(t), \tag{4.14}$$

with terms given by the recursion, modeled on (4.7) and (4.9),

$$i_0^+(t) = -m(t)V_{DD}/(2R_{ref}), \tag{4.15}$$

$$i_k^-(t) = \rho_L(t) * i_{k-1}^+(t), \tag{4.16}$$

$$i_k^+(t) = \rho_S(t) i_k^-(t), \tag{4.17}$$

and $(k > 0)$. Therefore, the total current at the reference plane is

$$i(t) = \sum_{k=0}^{\infty} i_k^+(t) - \sum_{k=1}^{\infty} i_k^-(t). \tag{4.18}$$

In the above derivation, no transmission line is assumed. However, the expressions (4.10) and (4.12) are analogous to the reflection coefficients from transmission-line theory.

4.2.2 Nonlinearities

Because the load circuit is LTI, the nonlinear ISI terms will first show up in the positive current $i^+(t)$. Using (4.13) and the nonlinear ISI model described in Ch. 3.5.2, we next show how different parts of the converter affect the output signal quality in terms of the nonlinear ISI, and how the choice of R_{ref} affects the analysis.

Nonlinear ISI from the source

In order to analyze the nonlinear effects from the source side alone, we assume that there is no reflection from the load. Therefore, the total positive current

becomes,

$$i^+(t) = i_0^+(t) = -m(t)V_{DD}/(2R_{ref}). \tag{4.19}$$

If the transistor is fast enough, where the transition processes $g_{rise}(t)$ and $g_{fall}(t)$ are shorter than a clock period ($t < T$), then only a one-clock period of memory will exist in $g_S(t)$. This translates to a switching device with relatively small parasitic capacitances. Then, based on the nonlinear ISI model shown in Fig. 3.11, $m(t)$ takes the form of (3.9). By defining $\alpha(t) = \ln(R_{ref}g_S(t))/2$, $m(t)$ can be rewritten as

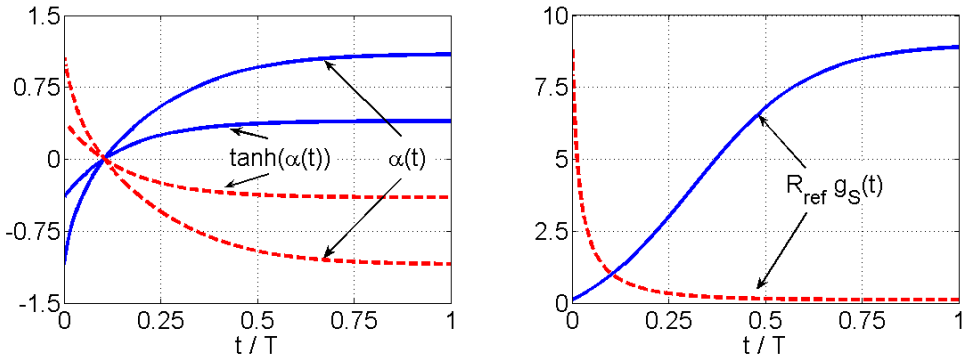
$$m(t) = 1 + \tanh \alpha(t). \tag{4.20}$$

It can be seen that $m(t)$ represents a linear D/A conversion only if its rising and falling waveforms are symmetric. Based on the property of the *tanh* function, the symmetry requirement demands that $\alpha_{rise}(t) = -\alpha_{fall}(t)$, and is equivalent to

$$R_{ref}^2 g_{rise}(t) g_{fall}(t) = 1. \tag{4.21}$$

Now, it can be easily seen that the symmetry of $m(t)$ does not imply the symmetry of $R_{ref}g_S(t)$, as illustrated by the example waveforms in Fig. 4.4.

In practice, the switching processes of $R_{ref}g_S(t)$ are determined by the device physical parameters and the bias conditions. It is difficult to provide the exact transition edges that are needed for a linear D/A conversion of $m(t)$. However, it is possible to reduce the nonlinearities by choosing a faster device or tuning the bias conditions.



(a) (b)

Figure 4.4: (a) Rising and falling edge waveforms of $\tanh \alpha(t)$ and $\alpha(t)$, where $\alpha(t) = \ln(R_{ref} g_S(t))/2$. (b) Corresponding rising and falling edge waveforms of $R_{ref} g_S(t)$.

Nonlinear ISI from the load

In order to analyze the nonlinear effects from the load side alone, we assume that there is no nonlinear ISI from the source. Based on the previous results, this means that the waveform of $\tanh \alpha(t)$ is symmetric, and $m(t)$ has the form

$$m(t) = 1 + \tanh \alpha(t) = 1 - \sum_n d(n) u(t - nT). \tag{4.22}$$

Based on (4.10),

$$\rho_S(t) = 1 - m(t). \tag{4.23}$$

Under the above assumption, $\rho_S(t)$ becomes

$$\rho_S(t) = \sum_n d(n) u(t - nT). \tag{4.24}$$

Substitute above into (4.15) and (4.17). For $k = 0$,

$$i_0^+(t) = \frac{V_{DD}}{2R_{ref}} \left(-1 + \sum_n d(n)u(t - nT) \right) \tag{4.25}$$

For $k = 1$,

$$i_1^-(t) = \frac{V_{DD}}{2R_{ref}} \left(B_1 + \sum_n d(n)b_1^1(t - nT) \right), \tag{4.26}$$

where

$$B_1 = \rho_L(t) * (-1) = -\mathcal{R}_L(0), \tag{4.27}$$

$$b_1^1(t) = \rho_L(t) * u(t), \tag{4.28}$$

and then from (4.17)

$$\begin{aligned} i_1^+(t) = \frac{V_{DD}}{2R_{ref}} \Bigg(& \sum_n d(n) f_1^1(t - nT) \\ & + \sum_{m \geq 0} \sum_n d(n)d(n - m) f_1^{2,m}(t - nT) \Bigg), \end{aligned} \tag{4.29}$$

where the causality of $u(t)$ and $\rho_L(t)$ zeros the $m < 0$ terms and

$$f_1^1(t) = u(t)B_1, \tag{4.30}$$

$$f_1^{2,m}(t) = u(t)b_1^1(t + mT). \tag{4.31}$$

Fig. 4.5 graphically illustrates how the unit pulse waveform of each $f_1^{2,m}(t)$ is constructed. Be aware that the term associated with $m = 0$ does not represent a nonlinear ISI effect. For mathematical simplicity, here it is grouped together with terms $m \geq 0$.

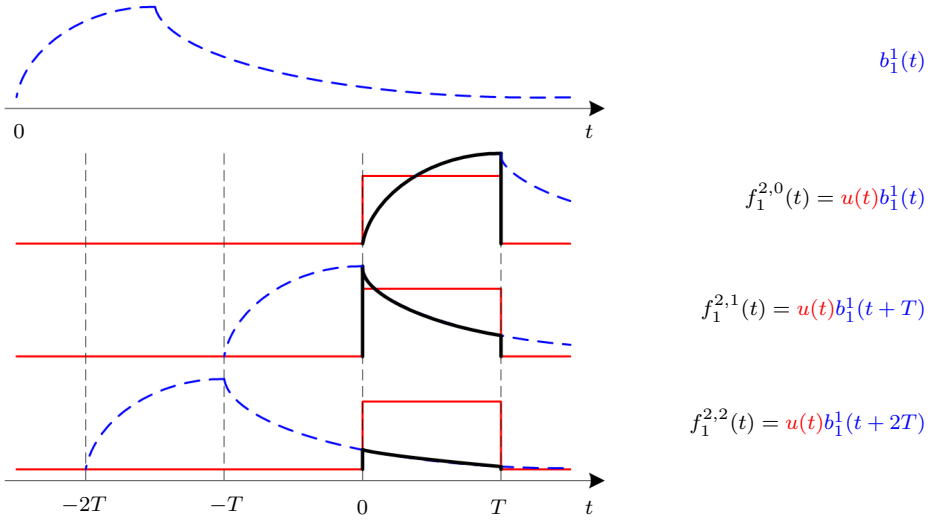


Figure 4.5: Unit pulse waveforms of $f_1^{2,m}(t)$. ($b(t)$ dash line, $u(t)$ thin-solid line, $f(t)$ thick-solid line.)

Similarly, higher order $i_k^+(t)$ can be expanded as

$$i_k^+(t) = \frac{V_{DD}}{2R_{ref}}\Bigg(\sum_n d(n) f_k^1(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m) f_k^{2,m}(t-nT) + \sum_{l\geq m}\sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-l) f_k^{3,m,l}(t-nT) + \cdots \Bigg). \quad (4.32)$$

Therefore, the total positive current has the form

$$i^+(t) = \frac{V_{DD}}{2R_{ref}}\Bigg(\sum_n d(n) p_1(t-nT) + \sum_{m>0}\sum_n d(n)d(n-m) p_2^m(t-nT) + \sum_{l>m}\sum_{m>0}\sum_n d(n)d(n-m)d(n-l) p_3^{m,l}(t-nT) + \cdots \Bigg). \quad (4.33)$$

where $p(t)$ with different superscripts and subscripts represents different LTI unit pulse responses. The subscripts denote the response order, where the 0^{th} order is the data-independent response, but not included in (4.33), the 1^{st}

order is the linear response, and the 2^{nd} and higher orders are the nonlinear ISI responses. The superscripts indicate the time delay between the current bit and the interfered bits, measured in clock periods. The LTI unit pulse responses $p(t)$ are determined by $\rho_L(t)$ and $g_S(t)$.

Since $\rho_L(t) \neq 0$, as shown in the previous derivation, $p(t)$ for 2^{nd} and high order terms in (4.33) will not be zero. Therefore, nonlinear ISI exists. In Fig. 4.2(b), the load circuit in the derivation models the actual load circuit combined with the output capacitance of the transistor and the bias circuit. Even for the ideal case of a purely resistive load and an ideal bias circuit, the capacitance would cause memory and stretch the pulse shape in the time domain, which generates intersymbol interference. Therefore, nonlinear effects are unavoidable in a single-switch converter.

As an example, Fig. 4.6 shows the $p(t)$ waveforms for different nonlinear ISI terms for a DAC circuit. In this simple model, the transistor is assumed to be an instantaneous switch with $R_{on} = 1\,\Omega$ and $R_{off} = 2.5\,\mathrm{k}\Omega$, biased by an ideal current source, and connected to a parallel RC load circuit with $C = 1\,\mathrm{pF}$ and $R_L = 50\,\Omega$. Based on these parameters, the time-oversampled waveforms are numerically calculated in Matlab based on the series format current expression.

4.2.3 Choosing R_{ref}

As mentioned previously, R_{ref} is an intermediate parameter for decomposing the signal of interest into a series format, and, mathematically, it can be

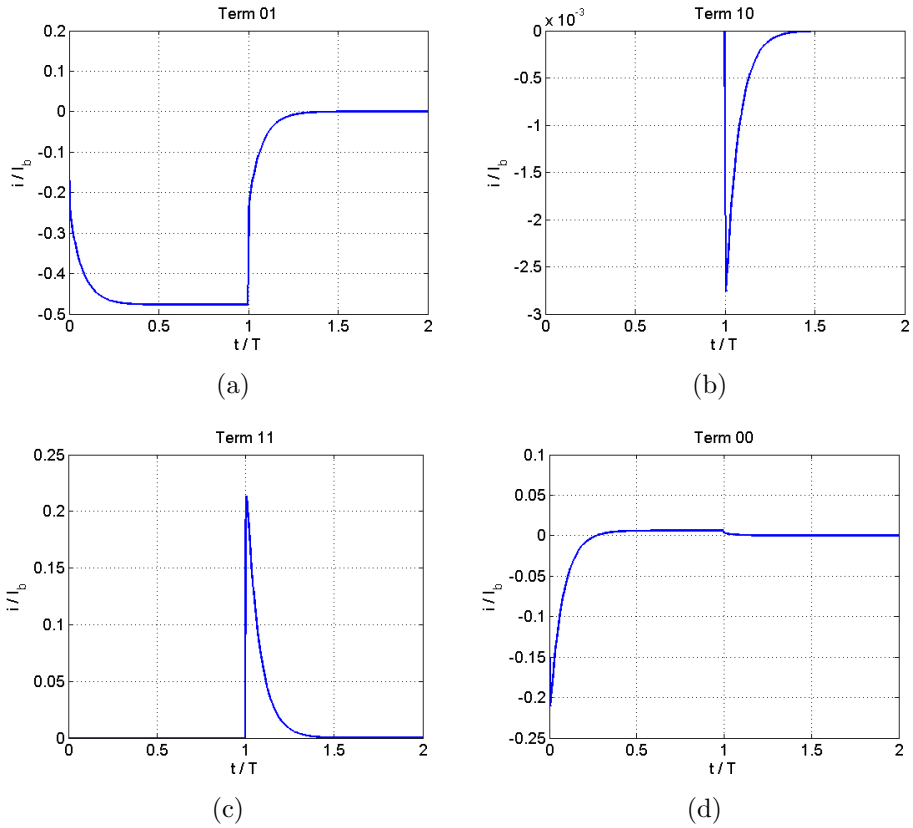


Figure 4.6: Example waveforms of $p(t)$ for different nonlinear ISI terms. (a) Waveform of linear term $p_1(t)$, (b) waveform of linear term $p_1(t)$ with one-clock delay, (c) waveform of 2^{nd}-order nonlinear term $p_2(t)$, and (d) waveform of 0^{th}-order term $p_0(t)$.

arbitrary. However, its value does affect how complicated the series expansion process is. For example, if $Y_t(s) = R_L^{-1}$, by choosing $R_{ref} = R_L$, there is no reflection from the load circuit ($\rho_L = 0$). The total current at the reference plane reduces to (4.19).

If R_{ref} is chosen to be different from R_L, based on (4.10) and (4.12), both $\rho_S(t)$ and $\rho_L(t)$ are non-zero. In order to solve $i(t)$, full series expansions of

$i^+(t)$ and $i^-(t)$ are needed. However, the physical circuit is not changed for these two cases. Therefore, the current expression at the reference plane has to have the form as in (4.19), but a proper choice of R_{ref} makes the series expansion analysis tractable.

If the series expansion is calculated numerically, the effect of the R_{ref} choice is reflected by the numerical accuracy of the result. For instance, using the same DAC circuit model and parameters as in the example of $p(t)$ waveforms calculation, in order to keep SNRs of the calculated output signal to be the same with different R_{ref} values, Fig. 4.7 shows how the values of other parameters in the numerical analysis are changed, where N_{pts} represents the number of point for oversampling the pulse waveform, and k represents the number of nonlinear ISI order for truncating the series expansion.

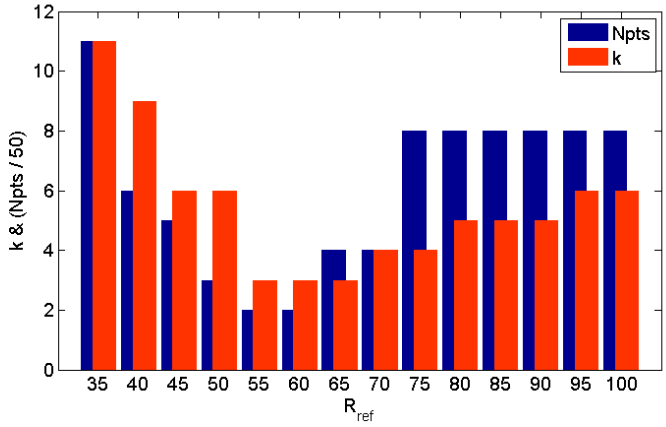


Figure 4.7: Example of R_{ref} effect on series expansion numerical analysis. (N_{pts} represents the number of point for oversampling the pulse waveform, and k represents the number of nonlinear ISI order for truncating the series expansion.)

4.3 Differential One-Bit Power DAC

Generally, due to configuration symmetry, differential circuits provide better linearity performance. Following the same analysis procedure as in the previous section, nonlinear ISI effects inside a differential one-bit converter are rigorously studied and presented next. First, we define even and odd mode variables as

$$var_{\Sigma} = var_1 + var_2 \tag{4.34}$$

$$var_{\Delta} = var_1 - var_2 \tag{4.35}$$

The circuit diagram of a differential one-bit power DAC is shown in Fig. 4.8(a). By modeling the transistors and the bias circuits in the same way as the single-ended case, a simplified circuit model shown in Fig. 4.8(b) is obtained. The components inside the dashed-line box can be treated as a two-port network, and its Y-parameters follow the relationship

$$[Y'_L(s)] = \begin{bmatrix} sC_1 + Y_L(s) & -Y_L(s) \\ -Y_L(s) & sC_2 + Y_L(s) \end{bmatrix}. \tag{4.36}$$

Again, by changing the reference ground, an equivalent circuit model is formulated and shown in Fig. 4.8(c).

4.3.1 Current Solution at The Reference Plane

Similar to the singled-ended case, at the reference plane in Fig. 4.8(c), as indicated by the dashed line, writing KCL to characterize the source and

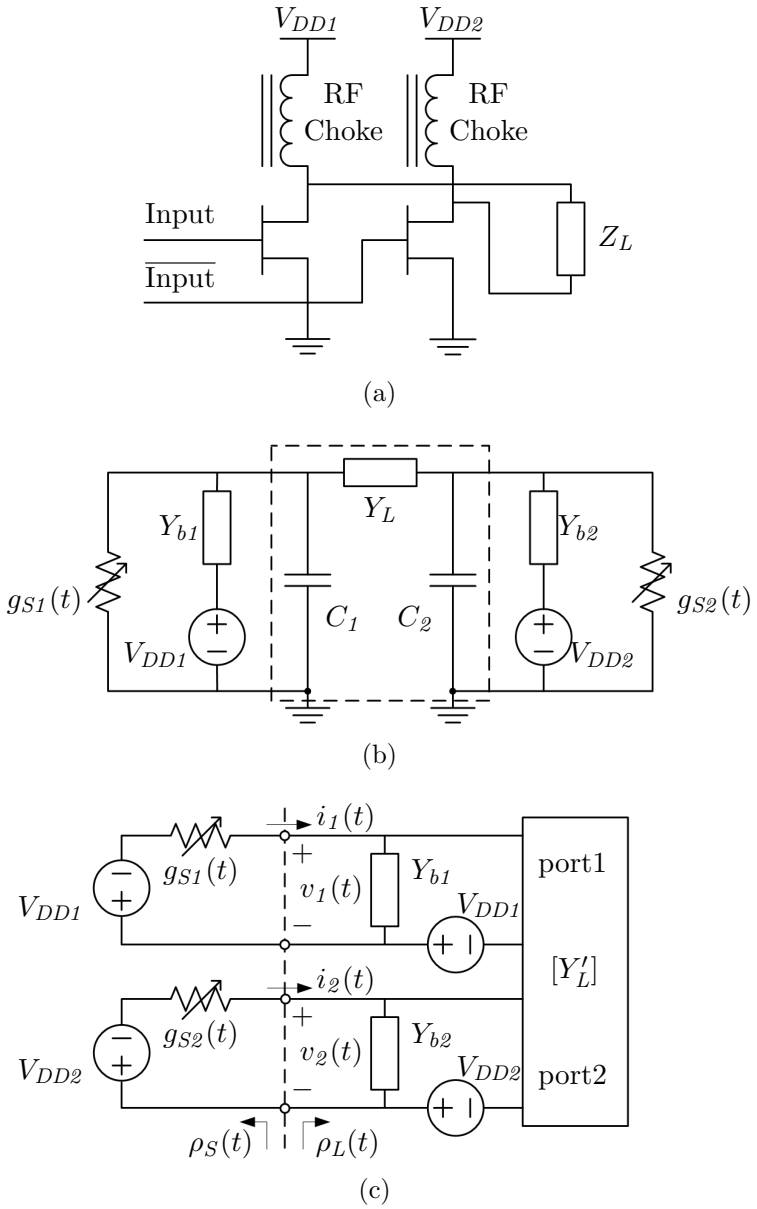


Figure 4.8: Differential one-bit converter (a) circuit diagram; (b) simplified circuit model; (c) equivalent circuit model. The components in the dashed box in (b) are shown as the 2-port network in (c).

load in the time and Laplace domains respectively, there are

$$\begin{pmatrix} i_1(t) \\ i_2(t) \end{pmatrix} = - \begin{bmatrix} g_{S1}(t) & 0 \\ 0 & g_{S2}(t) \end{bmatrix} \begin{pmatrix} v_1(t) + V_{DD1} \\ v_2(t) + V_{DD2} \end{pmatrix}, \tag{4.37}$$

$$\begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} = [Y_t(s)] \begin{pmatrix} V_1(s) \\ V_2(s) \end{pmatrix} + [Y'_L(s)] \begin{pmatrix} V_{DD}(s) \\ V_{DD}(s) \end{pmatrix}, \tag{4.38}$$

where

$$[Y_t(s)] = [Y'_L(s)] + \begin{bmatrix} Y_{b1}(s) & 0 \\ 0 & Y_{b2}(s) \end{bmatrix}. \tag{4.39}$$

For the steady state response of the circuit, if V_{DD} is an ideal DC voltage source, and because the load circuit is AC coupled to the transistor, (4.38) can be simplified as

$$\begin{pmatrix} I_1(s) \\ I_2(s) \end{pmatrix} = [Y_t(s)] \begin{pmatrix} V_1(s) \\ V_2(s) \end{pmatrix}. \tag{4.40}$$

Define even and odd mode variables, as in (4.34) and (4.35), and the change-of-variable relationship

$$\begin{pmatrix} i_\Sigma(t) \\ v_\Sigma(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix} \begin{pmatrix} i_\Sigma^+(t) \\ i_\Sigma^-(t) \end{pmatrix}, \tag{4.41}$$

$$\begin{pmatrix} i_\Delta(t) \\ v_\Delta(t) \end{pmatrix} = \begin{bmatrix} 1 & -1 \\ R_{ref} & R_{ref} \end{bmatrix} \begin{pmatrix} i_\Delta^+(t) \\ i_\Delta^-(t) \end{pmatrix}, \tag{4.42}$$

Solving for $[i^+(t)]$ and $[I^-(s)]$ respectively,

$$\begin{pmatrix} i_\Sigma^+(t) \\ i_\Delta^+(t) \end{pmatrix} = [\rho_S(t)] \begin{pmatrix} i_\Sigma^-(t) \\ i_\Delta^-(t) \end{pmatrix} - [m(t)] \frac{1}{2R_{ref}} \begin{pmatrix} V_{DD\Sigma} \\ V_{DD\Delta} \end{pmatrix}, \tag{4.43}$$

$$\begin{pmatrix} I_\Sigma^-(t) \\ I_\Delta^-(t) \end{pmatrix} = [\mathcal{R}_L(s)] \begin{pmatrix} I_\Sigma^+(t) \\ I_\Delta^+(t) \end{pmatrix}, \tag{4.44}$$

where

$$[\rho_S(t)] = (\mathrm{I} + R_{ref}[g_S(t)])^{-1} (\mathrm{I} - R_{ref}[g_S(t)]), \tag{4.45}$$

$$[m(t)] = (\mathrm{I} + R_{ref}[g_S(t)])^{-1} 2R_{ref}[g_S(t)], \tag{4.46}$$

$$[\mathcal{R}_L(s)] = (\mathrm{I} + R_{ref}[Y_t^{\Sigma\Delta}(s)])^{-1} (\mathrm{I} - R_{ref}[Y_t^{\Sigma\Delta}(s)]), \tag{4.47}$$

and

$$[g_S(t)] = \frac{1}{2} \begin{bmatrix} g_{S\Sigma}(t) & g_{S\Delta}(t) \\ g_{S\Delta}(t) & g_{S\Sigma}(t) \end{bmatrix}, \tag{4.48}$$

$$[Y_t^{\Sigma\Delta}(s)] = \frac{1}{2} \begin{bmatrix} \sum_{i,j} Y_{tij} & \sum_i (Y_{ti1} - Y_{ti2}) \\ \sum_j (Y_{t1j} - Y_{t2j}) & \sum_{i=j} Y_{tij} - \sum_{i \neq j} Y_{tij} \end{bmatrix}, \tag{4.49}$$

$$= \frac{1}{2} \begin{bmatrix} Y_{b\Sigma}(s) + sC_\Sigma & Y_{b\Delta}(s) + sC_\Delta \\ Y_{b\Delta}(s) + sC_\Delta & Y_{b\Sigma} + sC_\Sigma + 4Y_L(s) \end{bmatrix}. \tag{4.50}$$

Similar to the singled-ended case, the transfer function block diagram in Fig. 4.3 can be used for the differential converter. Instead of scalars, V_{DD}, $i^+(t)$, and $i^-(t)$ become 2×1 vectors; $m(t)$, $\rho_S(t)$ and $\rho_L(t)$ become 2×2

matrices. The positive and negative current components of the even and odd modes at the reference plane can be expressed as

$$\begin{pmatrix} i_{\Sigma}^{+}(t) \\ i_{\Delta}^{+}(t) \end{pmatrix} = \sum_{k=0}^{\infty} \begin{pmatrix} i_{\Sigma k}^{+}(t) \\ i_{\Delta k}^{+}(t) \end{pmatrix}, \tag{4.51}$$

$$\begin{pmatrix} i_{\Sigma}^{-}(t) \\ i_{\Delta}^{-}(t) \end{pmatrix} = \sum_{k=1}^{\infty} \begin{pmatrix} i_{\Sigma k}^{-}(t) \\ i_{\Delta k}^{-}(t) \end{pmatrix}, \tag{4.52}$$

with the recursion relationship

$$\begin{pmatrix} i_{\Sigma 0}^{+}(t) \\ i_{\Delta 0}^{+}(t) \end{pmatrix} = -[m(t)]\frac{1}{2R_{ref}} \begin{pmatrix} V_{DD\Sigma} \\ V_{DD\Delta} \end{pmatrix}, \tag{4.53}$$

$$\begin{pmatrix} i_{\Sigma k}^{-}(t) \\ i_{\Delta k}^{-}(t) \end{pmatrix} = [\rho_L(t)] * \begin{pmatrix} i_{\Sigma(k-1)}^{+}(t) \\ i_{\Delta(k-1)}^{+}(t) \end{pmatrix}, \tag{4.54}$$

$$\begin{pmatrix} i_{\Sigma k}^{+}(t) \\ i_{\Delta k}^{+}(t) \end{pmatrix} = [\rho_S(t)] \begin{pmatrix} i_{\Sigma k}^{-}(t) \\ i_{\Delta k}^{-}(t) \end{pmatrix}. \tag{4.55}$$

The total current at the reference plane is

$$\begin{pmatrix} i_{\Sigma}(t) \\ i_{\Delta}(t) \end{pmatrix} = \sum_{k=0}^{\infty} \begin{pmatrix} i_{\Sigma k}^{+}(t) \\ i_{\Delta k}^{+}(t) \end{pmatrix} - \sum_{k=1}^{\infty} \begin{pmatrix} i_{\Sigma k}^{-}(t) \\ i_{\Delta k}^{-}(t) \end{pmatrix}. \tag{4.56}$$

4.3.2 Nonlinearities

In order to make the notations in later derivations easier to follow, we define $\overline{s}(t)$ as the analog output signal when the digital input sequence is $-d(n)$.

Again, we show how different parts of the differential converter affect the output signal quality based on the positive current solution and the nonlinear

ISI model. We focus on the odd mode positive current, since it is the desired signal in this type of circuit. The analysis of the nonlinear ISI from the source and the load is done under the condition that the components in the two branches of the differential driver are identical, which means $V_{DD1} = V_{DD2} = V_{DD}$, $g_{S1}(t) = \overline{g_{S2}}(t)$, $Y_{b1}(s) = Y_{b2}(s) = Y_b(s)$, and $C_1 = C_2 = C$. Nonlinear effects caused by component mismatch are addressed later.

Nonlinear ISI from the source

If $[\rho_L] = 0$, the total positive current is

$$\begin{pmatrix} i_\Sigma^+(t) \\ i_\Delta^+(t) \end{pmatrix} = \begin{pmatrix} i_{\Sigma 0}^+(t) \\ i_{\Delta 0}^+(t) \end{pmatrix} = -[m(t)]\frac{1}{2R_{ref}} \begin{pmatrix} V_{DD\Sigma} \\ V_{DD\Delta} \end{pmatrix}. \tag{4.57}$$

The general expression for $[m(t)]$ is

$$[m(t)] = \begin{bmatrix} m^{cc}(t) & m^{dc}(t) \\ m^{dc}(t) & m^{cc}(t) \end{bmatrix} \tag{4.58}$$

where, after considerable algebra,

$$m^{cc}(t) = \frac{1}{2}\left(\frac{2R_{ref}g_{S1}(t)}{1 + R_{ref}g_{S1}(t)} + \frac{2R_{ref}g_{S2}(t)}{1 + R_{ref}g_{S2}(t)}\right), \tag{4.59}$$

$$m^{dc}(t) = -\frac{1}{2}\left(\frac{2}{1 + R_{ref}g_{S1}(t)} - \frac{2}{1 + R_{ref}g_{S2}(t)}\right). \tag{4.60}$$

When the transistors and bias circuits in the differential converter are identical, each element of the positive current vector in (4.57) can be expanded

as:

$$i_{\Sigma}^{+}(t) = -\left(\frac{R_{ref}\, g_{S1}(t)}{1 + R_{ref}\, g_{S1}(t)} + \frac{R_{ref}\, \overline{g_{S1}}(t)}{1 + R_{ref}\, \overline{g_{S1}}(t)}\right)\frac{V_{DD}}{R_{ref}}, \tag{4.61}$$

$$i_{\Delta}^{+}(t) = \left(\frac{1}{1 + R_{ref}\, g_{S1}(t)} - \frac{1}{1 + R_{ref}\, \overline{g_{S1}}(t)}\right)\frac{V_{DD}}{R_{ref}}. \tag{4.62}$$

It can be seen that, as expected for a purely differential circuit,

$$\overline{i_{\Sigma}^{+}}(t) = \quad i_{\Sigma}^{+}(t), \tag{4.63}$$

$$\overline{i_{\Delta}^{+}}(t) = -i_{\Delta}^{+}(t). \tag{4.64}$$

If the assumption for the single-ended converter is also true here, where the transistors switch fast enough and the transition processes of $g_S(t)$ are within one clock period, both even and odd mode currents would have a form of expression as in (3.9). Based on (4.63) and (4.64), $i_{\Sigma}^{+}(t)$ and $i_{\Delta}^{+}(t)$ are simplified as

$$i_{\Sigma}^{+}(t) = \frac{V_{DD}}{R_{ref}}\left(\sum_{n} u_0(t - nT) + \sum_{n} d(n)d(n-1)u_2(t - nT)\right), \tag{4.65}$$

$$i_{\Delta}^{+}(t) = \frac{V_{DD}}{R_{ref}}\sum_{n} d(n)u_1(t - nT). \tag{4.66}$$

It can be seen that when the circuit components in the differential driver are identical and the transistors are relatively fast, the positive odd mode current does not have any nonlinear ISI. This is achieved with no restriction on $g_S(t)$. In fact, this was the original motivation for considering a differential circuit configuration.

Nonlinear ISI from the load

If we define

$$\alpha_1(t) = \frac{\ln(R_{ref} g_{S1}(t))}{2}, \tag{4.67}$$

$$\alpha_2(t) = \frac{\ln(R_{ref} g_{S2}(t))}{2}, \tag{4.68}$$

equations (4.59) and (4.60) are rewritten as

$$m^{cc}(t) = 1 + \frac{1}{2}\left(\tanh\alpha_1(t) + \tanh\alpha_2(t)\right), \tag{4.69}$$

$$m^{dc}(t) = \frac{1}{2}\left(\tanh\alpha_1(t) - \tanh\alpha_2(t)\right), \tag{4.70}$$

Based on (4.46) and (4.45),

$$[\rho_S(t)] = \mathrm{I} - [m(t)] = \begin{bmatrix} \rho_S^{cc}(t) & \rho_S^{dc}(t) \\ \rho_S^{dc}(t) & \rho_S^{cc}(t) \end{bmatrix}, \tag{4.71}$$

where

$$\rho_S^{cc}(t) = -\frac{1}{2}\left(\tanh\alpha_1(t) + \tanh\alpha_2(t)\right), \tag{4.72}$$

$$\rho_S^{dc}(t) = -\frac{1}{2}\left(\tanh\alpha_1(t) - \tanh\alpha_2(t)\right). \tag{4.73}$$

If the transistors switch fast enough, we can define

$$\begin{aligned}\tanh\alpha_1(t) = & -\sum_n u_0(t-nT) - \sum_n d(n)u_1(t-nT) \\ & -\sum_n d(n)d(n-1)u_2(t-nT),\end{aligned} \tag{4.74}$$

and if the transistors and bias circuits in the differential converter are identical, we have

$$\begin{aligned}\tanh\alpha_2(t) &= \tanh\overline{\alpha_1}(t)\\ &= -\sum_n u_0(t-nT)+\sum_n d(n)u_1(t-nT)\\ &\quad -\sum_n d(n)d(n-1)u_2(t-nT).\end{aligned} \tag{4.75}$$

Therefore,

$$m^{cc}(t) = 1-\sum_n u_0(t-nT)-\sum_n d(n)d(n-1)u_2(t-nT) \tag{4.76}$$

$$m^{dc}(t) = -\sum_n d(n)u_1(t-nT), \tag{4.77}$$

$$\rho_S^{cc}(t) = \sum_n u_0(t-nT)+\sum_n d(n)d(n-1)u_2(t-nT), \tag{4.78}$$

$$\rho_S^{dc}(t) = \sum_n d(n)u_1(t-nT), \tag{4.79}$$

and the load reflection $[\rho_L(t)]$ is

$$[\rho_L(t)] = \begin{bmatrix} \rho_L^{cc}(t) & 0 \\ 0 & \rho_L^{dd}(t) \end{bmatrix}, \tag{4.80}$$

Based on the above conditions, the transfer function diagram in Fig. 4.3 can be expanded as in Fig. 4.9.

Substitute the above expressions for $[m(t)]$, $[\rho_S(t)]$, and $[\rho_L(t)]$ into (4.53)

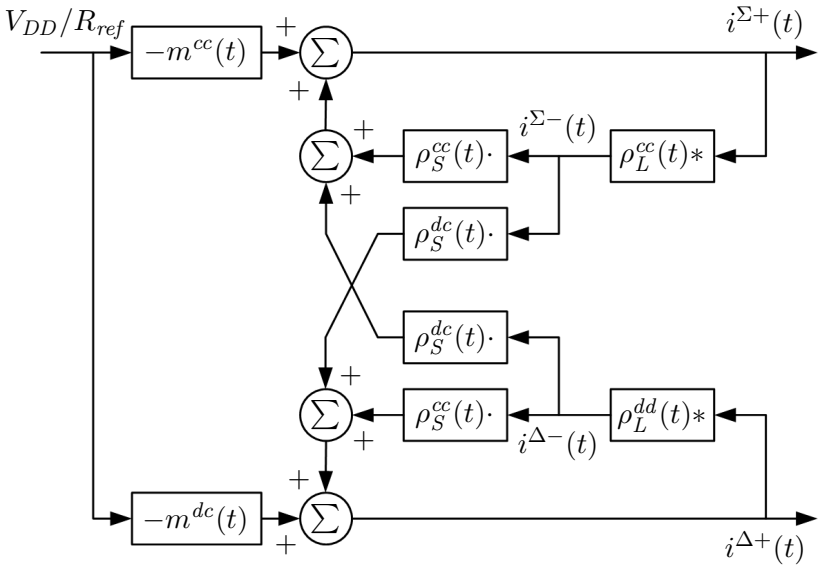


Figure 4.9: Expanded transfer function block diagram of the differential one-bit converter when the transistors and bias circuits are identical.

(4.54) and (4.55). For $k = 0$,

$$i^{+}_{\Sigma 0}(t) = \frac{V_{DD}}{R_{ref}}\left(-1 + \sum_n u_0(t - nT) + \sum_n d(n)d(n-1)u_2(t - nT)\right), \tag{4.81}$$

$$i^{+}_{\Delta 0}(t) = \frac{V_{DD}}{R_{ref}} \sum_n d(n)u_1(t - nT). \tag{4.82}$$

For $k = 1$,

$$i^{-}_{\Sigma 1}(t) = \frac{V_{DD}}{R_{ref}}\left(B_1 + \sum_n b_1^0(t - nT) + \sum_n d(n)d(n-1)b_1^{2,1}(t - nT)\right), \tag{4.83}$$

$$i^{-}_{\Delta 1}(t) = \frac{V_{DD}}{R_{ref}} \sum_n d(n)b_1^1(t - nT), \tag{4.84}$$

and

$$i^+_{\Sigma 1}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_n f_1^0(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)f_1^{2,m}(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-1)d(n-m)d(n-m-1)f_1^{4,1,m,m+1}(t-nT)\Bigg), \tag{4.85}$$

$$i^+_{\Delta 1}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_n d(n)f_1^1(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-m-1)f_1^{3,m,m+1}(t-nT).\Bigg) \tag{4.86}$$

Similarly, higher order $i^+_k(t)$ can be expanded as

$$i^+_{\Sigma k}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_n f_k^0(t-nT) + \sum_{m\geq 0}\sum_n d(n)d(n-m)f_k^{2,m}(t-nT) + \sum_{j\geq l}\sum_{l\geq m}\sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-l)d(n-j)f_k^{4,m,l,j}(t-nT) + \cdots\Bigg), \tag{4.87}$$

$$i^+_{\Delta k}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_n d(n)f_k^1(t-nT) + \sum_{\ell\geq m}\sum_{m\geq 0}\sum_n d(n)d(n-m)d(n-\ell)f_k^{3,m,\ell}(t-nT) + \cdots\Bigg). \tag{4.88}$$

By summing all $i^+_{\Sigma k}(t)$ and $i^+_{\Delta k}(t)$, expressions for $i^+_{\Sigma}(t)$ and $i^+_{\Delta}(t)$ now have

the forms:

$$i_{\Sigma}^{+}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_{n} p_0(t-nT) + \sum_{m>0}\sum_{n} d(n)d(n-m)p_2^{m}(t-nT) + \sum_{j>\ell}\sum_{\ell>m}\sum_{m>0}\sum_{n} d(n)d(n-m)d(n-\ell)d(n-j)p_4^{m,\ell,j}(t-nT) + \cdots \Bigg), \tag{4.89}$$

$$i_{\Delta}^{+}(t) = \frac{V_{DD}}{R_{ref}}\Bigg(\sum_{n} d(n)p_1(t-nT) + \sum_{\ell>m}\sum_{m>0}\sum_{n} d(n)d(n-m)d(n-\ell)p_3^{m,\ell}(t-nT) + \cdots \Bigg). \tag{4.90}$$

It can be seen that there are only even-order nonlinear terms in the common and odd-order terms in the differential mode positive current. Since the load is differential, even-order nonlinear ISI terms will be rejected. Therefore, nonlinear effects from the load reflection are reduced in the differential converter compared to the single-ended case.

Nonlinear ISI from component mismatch

When the components inside the differential pair are identical, the differential driver has substantial advantages over the single-ended driver in terms of output signal linearity. However, if it fails to satisfy such a condition, nonlinearities will be generated. For instance, when the two transistors are mismatched, the 2^{nd} order nonlinearity will be generated in the odd mode current from the source circuit because $g_{S1}(t) \neq \overline{g_{S2}}(t)$, and even-order nonlinearities will be generated from the load circuit because $C_1 \neq C_2$.

Nonlinear effects due to component mismatch can be quantified with a derivation similar to the above, but the derivation is cumbersome. The conclusion, however, is that in differential driver design it is important to consider the effects of component mismatch on linearity, but it will be easier to quantify these with specific transistor models through circuit simulations.

4.4 Summary

In this chapter, based on the introduced circuit analysis approach, the nonlinear ISI effects inside single-ended and differential one-bit DACs have been analyzed. Based on the equivalent circuit models of DACs in Fig. 4.2(c) and 4.8(c), the generation of nonlinear ISI has been mainly categorized as *Source Effects* and *Load Effects*. An additional class, *Components Mismatch Effects*, is added to the differential DAC. The load in the equivalent circuit models includes DAC bias circuit, transistor parasitics, and the actual load circuit. The derivation shows that the nonlinear ISI effects generated by these components are based on the same kind of mechanism.

Through the theoretical analysis, the differential configuration shows substantial advantage over the single-ended case in terms of signal linearity, which is expected. However, the advantage is only provided when the circuit components in the differential converter are identical. Otherwise, additional nonlinear ISI effects are introduced.

Chapter 5

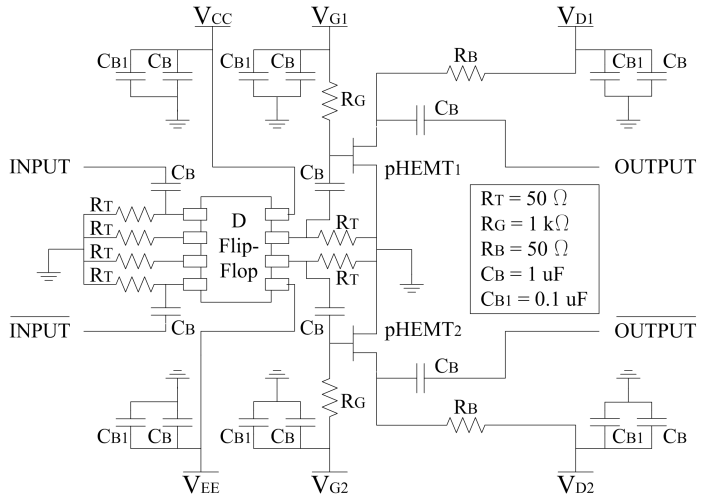
One-Bit Power DAC Design and Characterization

The analysis presented in the previous chapter shows that differential DACs have improved linearity over single-ended DACs for $\Delta\Sigma$ modulated signals. To experimentally evaluate the linearity improvement, for a differential one-bit power DAC over a single-ended converter, several circuits were fabricated and characterized. The design process and the linearity and efficiency performance measurements of the DACs are presented in this chapter.

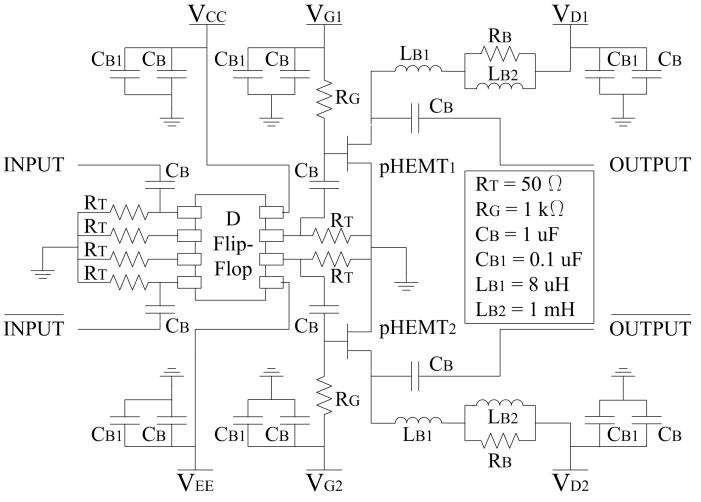
5.1 One-bit Power D/A Converters Design

Discrete power pHEMTs from TriQuint Semiconductor (TGF2022-06) are used for the converter designs. The circuit diagrams of the differential DACs

are shown in Figs. 5.1. The circuits are fabricated on a Rogers TMM substrate with $\epsilon_r = 3.27$ and 0.381 mm thickness, as in Figs. 5.2.



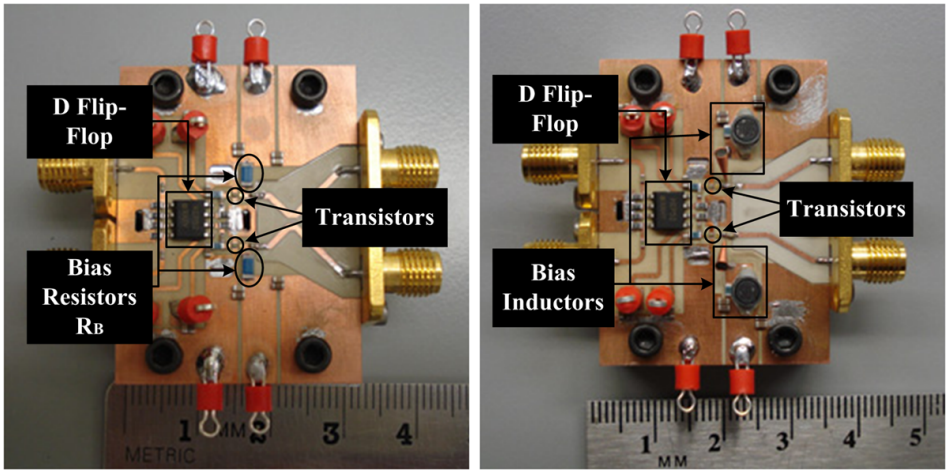
(a)



(b)

Figure 5.1: Circuit diagrams of a resistively-biased (a) and an inductively-biased (b) differential DACs.

The $\Delta\Sigma$ signal is a pseudo-random pulse train and, theoretically, has infinite bandwidth. The input circuit design goal is minimal waveform distortion at the transistor gate, since this will directly affect $g_S(t)$. A broadband bias circuit is critical and can be either resistive or inductive. The lossy resistive bias circuit, Fig. 5.1(a), provides a constant response over a broad bandwidth, while the inductive bias circuit, Fig. 5.1(b), has inherent bandwidth limitations. To understand the trade-off between signal quality and efficiency, both types of bias circuits are designed and characterized.



(a) (b)

Figure 5.2: Photographs of a resistively-biased (a) and an inductively-biased (b) differential DACs.

For a resistively biased DAC, the output signal peak-to-peak voltage V_{pp} and the pulse modulation drain efficiency η_{PMD} can be expressed in terms of the bias resistor R_B. By modeling the transistor as an ideal switch and the

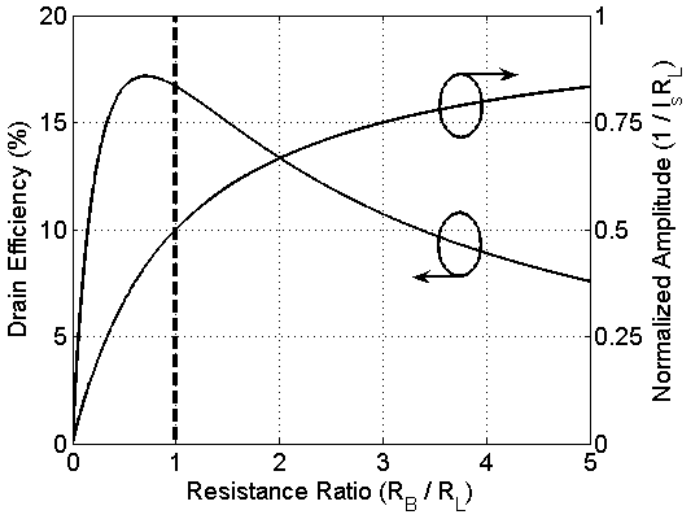


Figure 5.3: Single-ended resistively-biased DAC efficiency and voltage swing as a function of the ratio of bias and load resistors (R_B/R_L) is used to choose the values for R_B, R_L. The dashed lines shows the value chosen for the design in this work.

load as a resistor R_L, the following relationships are obtained,

$$V_{pp} = I_s R_L \frac{R_B}{R_B + R_L} \tag{5.1}$$

$$\eta_{PMD} = \frac{R_B R_L}{(R_B + R_L)^2 + R_B^2 + R_B R_L}, \tag{5.2}$$

where I_s is the saturation current of the transistor. The output peak-to-peak voltage, normalized to $I_s R_L$, and the pulse modulation drain efficiency are plotted versus R_B/R_L, in Fig. 5.3. The resistor value is chosen as $R_B = R_L = 50\,\Omega$ for higher efficiency with some sacrifice in the voltage range.

A broadband inductive bias circuit is designed with an $8\,\mu$H broadband conical inductor resonant around 40 GHz, in series with a 1 mH inductor and a parallel $1\,\text{k}\Omega$ resistor that damps the parasitic resonances. The isolation

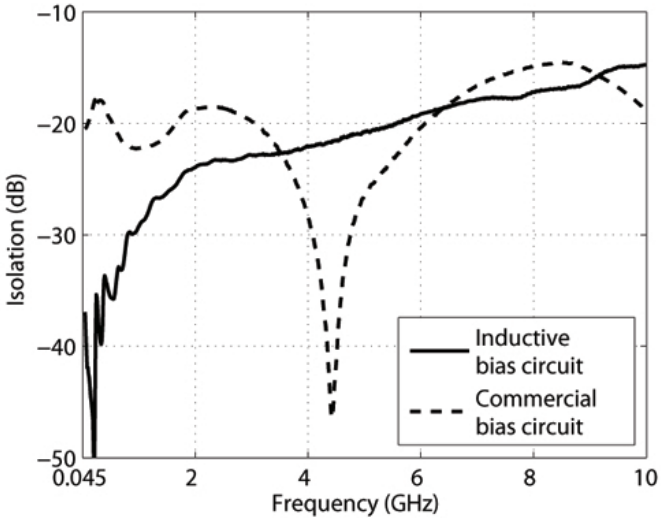


Figure 5.4: Measured isolation of inductively-biased circuit, compared to a broadband commercial bias circuit [39], exhibits the desired flat frequency response.

performance of the inductive bias tee is compared to a commercial component [39], resulting in the plots in Fig. 5.4, which show a flat frequency response of the RF-DC isolation.

The digital input signal to the designed DAC is provided by an FPGA as discussed in the next section. A differential data and clock D flip-flop chip from On Semiconductor (MC100EP52) with standard emitter-couple logic is used as a buffer stage, which outputs 800 mV peak-to-peak into a 50 Ω termination.

5.2 Measurement Parameters

Since the one-bit converter characterization is different from that of conventional amplifiers, we next briefly explain the measurement parameters and procedures.

Signal-to-noise-and-distortion (SINAD) is the ratio of the signal to the noise-and-distortion component inside the signal band, also known as SNDR, and is a common DAC metric. We use it to characterize linearity expressed in dB and calculated from a spectrum analyzer measurement.

Output signal RMS voltage (V_{RMS}) is the RMS voltage of the converter output pulse waveform, in volts. It is used to characterize the output signal amplitude level and measured by an oscilloscope.

Pulse modulation drain efficiency (η_{PMD}) is the ratio of the driver output BPDSM pulse waveform power to the drain bias DC power. The pulse waveform power is calculated based on v_{oRMS} and the load resistance. This parameter is different from the conventional amplifier drain efficiency, because the $\Delta\Sigma$ pulse waveform contains both signal and noise power. In order to measure the conventional drain efficiency of the driver, signal filtering is needed. Pulse modulation drain efficiency is used here to characterize the loss factors inside the bias circuit and the transistor.

5.3 Driver Measurement Results

5.3.1 Measurement Setup

The measurement setup block diagram is shown in Fig. 5.5. A Xilinx Virtex-II Pro XC2VP30 FPGA development board is used for streaming the pre-computed $\Delta\Sigma$ bit sequences to the converter. The data sequences were generated offline using an error-feedback loop with quantizer dithering [40] and a custom FIR loop filter [22]. The board has RocketIO^{TM} differential serial transceivers capable of a 3.125 Gb/s transmit rate, as well as DDR memory to support large throughput requirements. Because of the speed limit of the front bus connecting DDR and DMA, the data clock rate is set at 1.5 GHz. An external clock signal provided by an HP83620 synthesizer followed by a frequency divider reduces the jitter of the FPGA board [41]. An HP8565E spectrum analyzer is used to record the output signal spectrum for calculating SINAD, and an HP7082A digital sampling oscilloscope is used to measure the signal V_{RMS}.

A bandpass filter is inserted between the output of the converter and the spectrum analyzer to reduce the out-of-band noise. The filter is chosen to be absorptive to eliminate reflections from the load, which cause additional nonlinear ISI. A lossy filter is not the right choice for an integrated DAC, and it is used here only for characterization purposes. A terminated bridge balun circuit is used for the differential converter measurements, as shown in Fig. 5.6. Single-ended converters were measured by using half of the differential

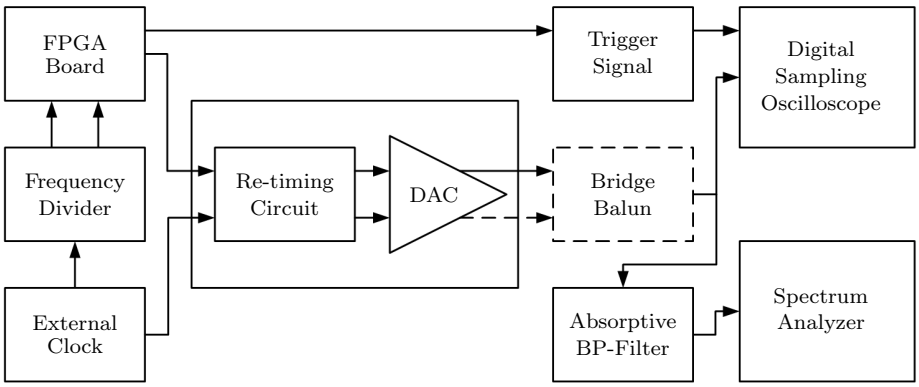


Figure 5.5: Measurement setup block diagram. The $\Delta\Sigma$ modulated one-bit digital signal is fed into the power DAC from an externally clocked FPGA board. A D flip-flop is inserted at the input of the DAC to reduce the random jitter effect. Measurement results in time and frequency domains are recorded by an oscilloscope and a spectrum analyzer, respectively. A bridge balun circuit is used for the differential measurement setup.

converter and biasing the other half at cutoff. All the measurement results are taken with a three-tone 60 MHz bandwidth $\Delta\Sigma$ test signal centered at 375 MHz with a 1.5 Gb/s clock rate, as shown in Fig. 1.1(c).

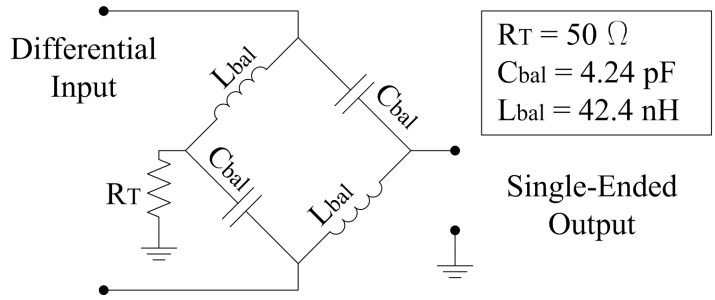
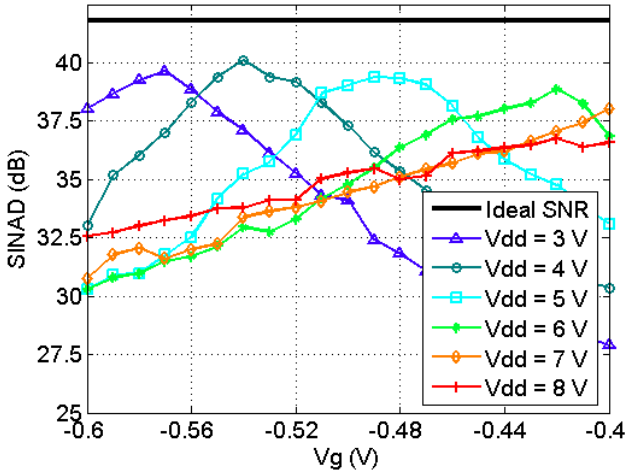
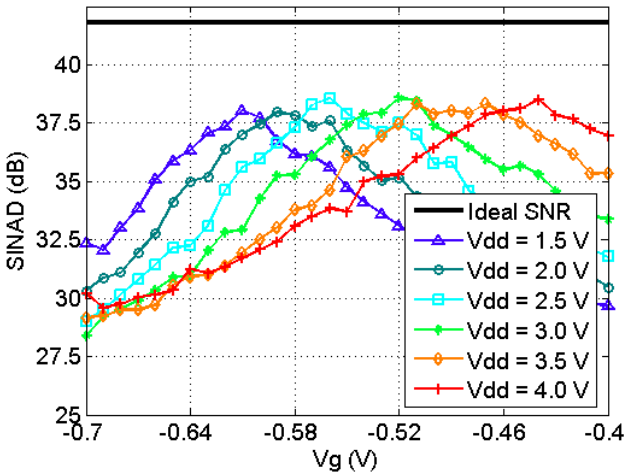


Figure 5.6: Circuit diagram of the terminated bridge balun.

5.3.2 Converter Linearity Measurement Results



(a)



(b)

Figure 5.7: Measured SINAD for resistively biased (a) and inductively biased (b) single-ended DACs at different gate and drain bias voltages. The flat solid line shows the SINAD for an ideal circuit.

The measured SINAD of the resistively biased single-ended converter at

different gate and drain bias voltages is shown in Fig. 5.7(a). The ideal SINAD of the testing $\Delta\Sigma$ signal is 41.8 dB. At different drain bias levels, the measured SINAD is very sensitive to the gate bias voltage. This is because the reference voltage at the transistor gate directly affects the waveform of the switching conductance $g_S(t)$, which causes nonlinear ISI effects and increases the noise floor in the signal band. For instance, Fig. 5.8 shows the relative signal power spectrum density (PSD) for the best and the worst measured SINAD when $V_{DD} = 4\,\mathrm{V}$. It can be seen that the SINAD drop is directly related to the in-band noise level increase, which is caused by nonlinear effects.

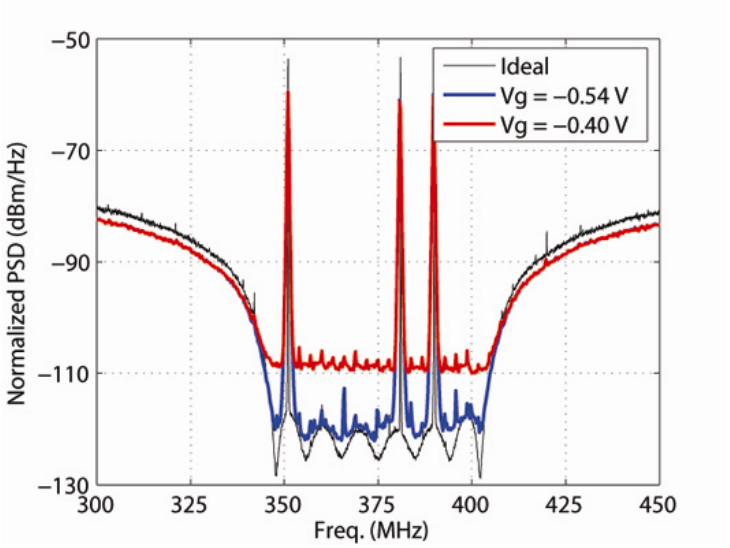
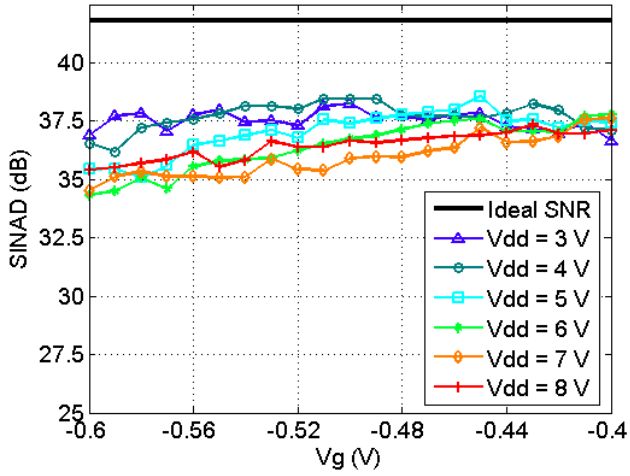
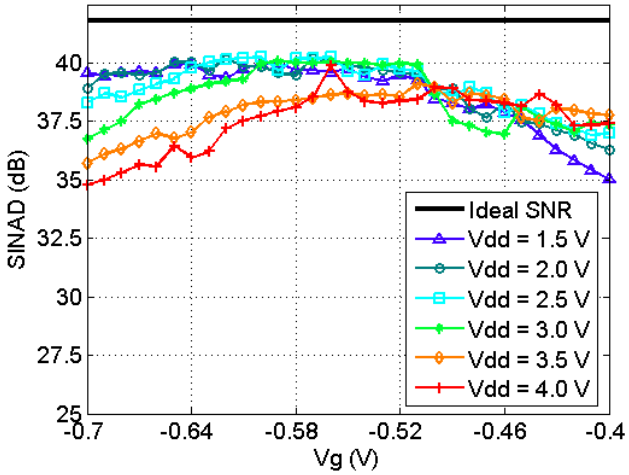


Figure 5.8: Measured output signal PSD of the resistively biased single-ended converter at $V_g = -0.54\,\mathrm{V}$ (the best measured SINAD) and $V_g = -0.40\,\mathrm{V}$ (the worst measured SINAD) when $V_{DD} = 4\,\mathrm{V}$. (Signal PSD is normalized to a 1 V peak value waveform.)



(a)



(b)

Figure 5.9: Measured SINAD for resistively biased (a) and inductively biased (b) differential DACs at different gate and drain bias voltages. The flat solid line shows the SINAD for an ideal circuit.

Measured SINAD results of the inductively biased single-ended converter are shown in Fig. 5.7(b). Although similar dependence on bias is seen, the

best achievable SINAD is slightly worse than for the resistively biased case. This is most likely due to the frequency dependence of the inductive bias circuit, which causes extra load reflection to the switching transistor.

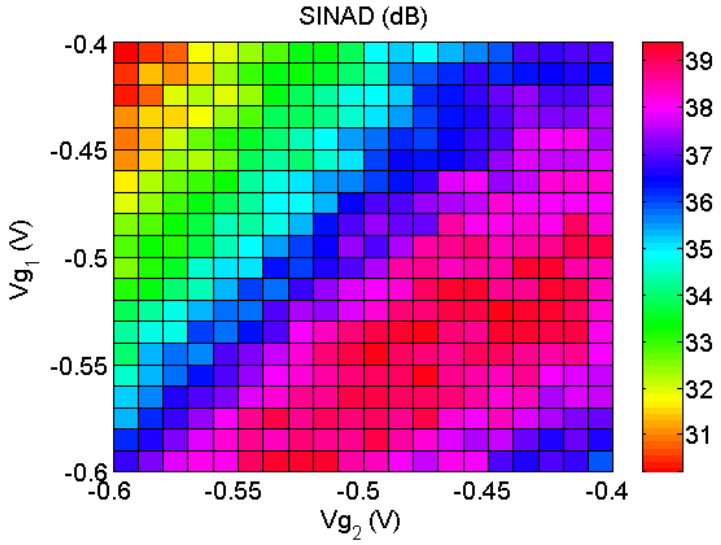


Figure 5.10: Measured SINAD of the resistively biased differential converter at $V_{dd} = 3$V and different gate bias voltages.

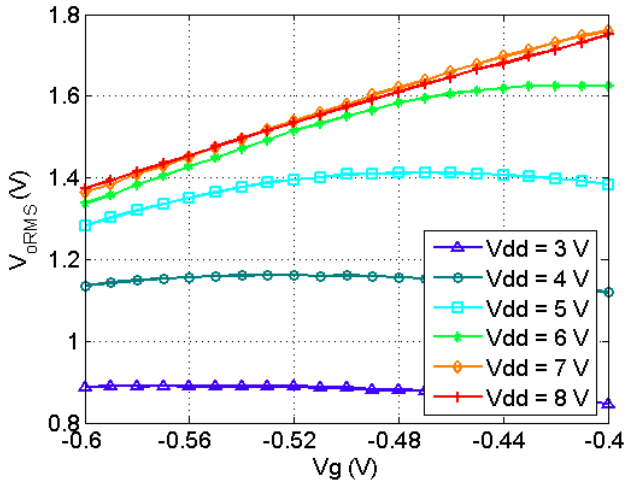
The differential converter SINAD results compared to the single-ended ones are much less sensitive to the transistor gate bias voltage, as shown in Fig. 5.9(a). This agrees with the conclusion from the theoretical derivation in Ch. 4, i.e. the differential driver output signal linearity is less dependent on $g_S(t)$. However, we also notice that the best SINAD at different drain bias for the resistively biased differential converter is worse than the one for the single-ended case. This is due to the mismatch between components in each differential pair. As an external control method, by tuning the gate bias of each transistor respectively, better SINAD results can be obtained,

as shown in Fig. 5.10. This proves that having identical transistors and other circuit components is very critical in the differential converter implementation. Compared to the single-ended case, the SINAD of the inductively biased differential converter in Fig. 5.9(b) shows not only less sensitivity to the transistor gate bias voltage but also better linearity, since the even-order nonlinear ISI effects caused by the time-varying conductance of the transistor and the drain bias inductor are reduced in the differential configuration.

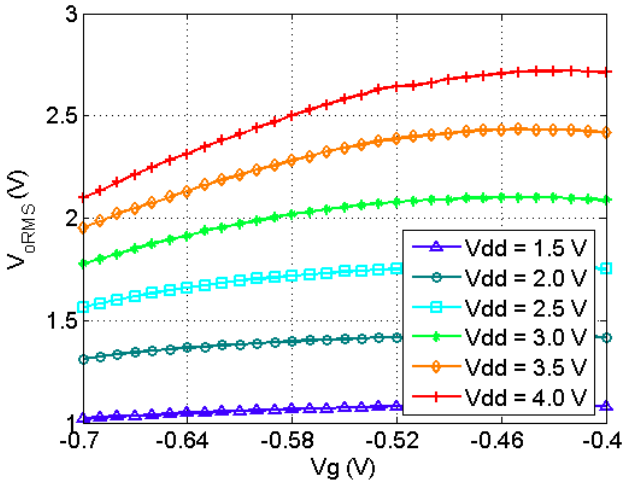
5.3.3 Converter Efficiency Measurement Results

The measured single-ended converter output signal RMS voltages at different bias conditions are shown in Fig. 5.11. The relative pulse modulation drain efficiency is calculated and plotted in Fig. 5.12. As expected, the inductively biased converter has much higher efficiency. The major loss factor in the resistively biased converter is the current through the bias resistor, and its ideal pulse modulation drain efficiency is only 16.67%, as in Fig. 5.3. By comparing Fig. 5.7 and 5.12, it can be seen that the gate bias voltage values for the best-achievable SINAD and efficiency are closer for the inductively biased DAC than the resistively biased case. This shows another advantage of using inductive bias circuit, besides better power-conversion efficiency.

For both cases, the measured efficiencies are lower than the theoretical prediction, in part due to the switching loss of the transistor. In addition, the input signal is too low for large drain biases, as can be seen from the saturation of V_{RMS} results in Fig. 5.11(a). Because the balun circuit that is



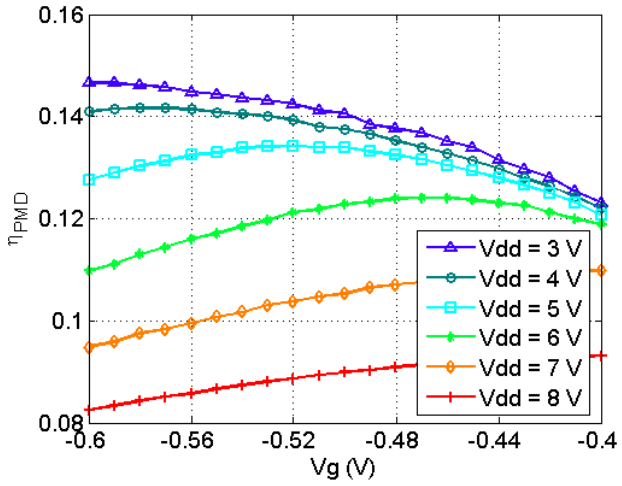
(a)



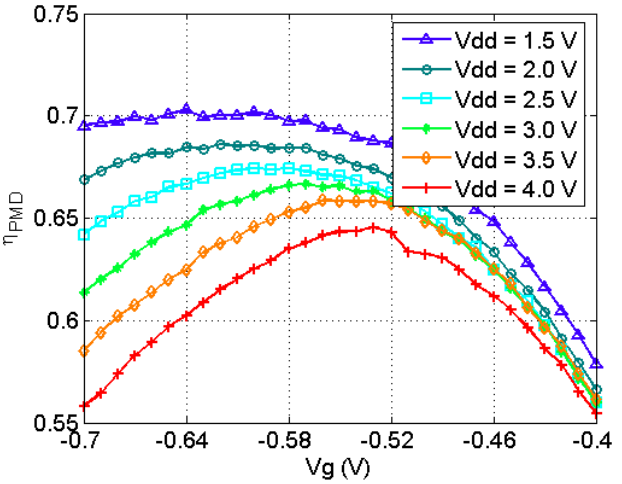
(b)

Figure 5.11: Measured V_{oRMS} of the single-ended converter at different gate and drain bias voltages: (a) resistively biased, (b) inductively biased.

used in the differential measurement setup has limited operation bandwidth, the output signal waveform of differential DACs could not be accurately



(a)



(b)

Figure 5.12: Measured η_{PMD} of the single-ended converter at different gate and drain bias voltages: (a) resistively biased, (b) inductively biased.

captured by the oscilloscope. Therefore, efficiency measurements were not performed for differential converters. However, the results for the single-

ended configuration provide an upper bound for the differential case. Ideally, the pulse modulation efficiencies for both cases should be the same.

5.4 Summary

In this chapter, single-ended and differential one-bit DACs are designed, built and tested with both resistively and inductively biased circuits. Measurement results have confirmed that, compared to the differential configuration, the single-ended case is more sensitive to the bias voltage change, which is modeled as the change of $g_S(t)$ in the theoretical analysis in Ch. 4. The inductive bias circuit, as expected, has much lower loss than the resistive bias. However, the frequency dependence of the inductor may distort the signal linearity, as shown by the results of the single-ended inductively-biased DAC. The differential configuration helps to reduce this effect. Nonlinear effects caused by components difference in the differential pairs are also seen from the results. Tuning bias voltages separately works as an external control method to reduce the nonlinear ISI.

The measurement results presented in this chapter are obtained by connecting the DACs' output to the instrument through an absorptive bandpass filter. Additionally, a terminated bridge balun circuit is used in the differential DAC measurement to converter the differential into single-ended mode. The absorptive filter reduces the extra reflection from the load circuit, and allow us to better characterize the linearity performance of the DAC alone.

More detailed analysis and discussion on effects of the bandpass filtering load circuits on DAC's linearity performance will be given in the next chapter.

Chapter 6

Bandpass Filter Design for One-Bit Power DAC

6.1 Introduction

Bandpass filtering is an indispensable last step in the bandpass $\Delta\Sigma$ D/A conversion [4]. For conventional current-steering $\Delta\Sigma$ DACs [42], the bandpass filtering load circuit is designed as an isolated component, where the linearity performance is thought to be independent from the filter. This assumption is valid, however, only when the transistors in current-steering $\Delta\Sigma$ DACs are driven in the linear operating region. In such a case, combined with the bias circuit, the transistor is modeled as a $\Delta\Sigma$ modulated source with a constant source impedance. If the system impedance is matched with the source impedance, the reflections from the load circuit will be absorbed.

Therefore, the *multiple-reflection* phenomenon described in Ch. 4 does not exist here, and there will be no nonlinear ISI effect from the load circuit.

However, for one-bit $\Delta\Sigma$ power DAC design, the transistors are driven as time-varying resistances, and conventional impedance matching cannot be applied. Under this condition, the bandpass filtering load circuit can no longer be taken as an independent part in the DAC design. In this chapter, first, the linearity performance of single-ended and differential one-bit power DACs with different bandpass filters (BPFs) is discussed. In addition, design and characterization of a differential reflective BPF is given; followed by preliminary measurement results of a differential inductively-biased one-bit DAC cascaded with the designed BPF.

6.2 Absorptive Bandpass Filter Design

Based on the out-of-band response, BPFs can be categorized as reflective [43, 44] and absorptive [45, 46], as shown in Fig. 6.1. Theoretically, the reflective BPFs are lossless, with $|S_{21}| = |S_{12}| = 1$ and $|S_{11}| = |S_{22}| = 0$ in the passband. From power conservation, reflective BPFs exhibit a high reflection in the stopband, which is usually undesirable in digital-circuit applications, because it can create signal interference. For example, Fig. 6.2 shows the simulated $\Delta\Sigma$ signal spectra with different types of filters. It can be seen that the in-band noise floor does not change in the absorptive filtered signal spectrum, while it increases in the reflective filtered one, which is caused

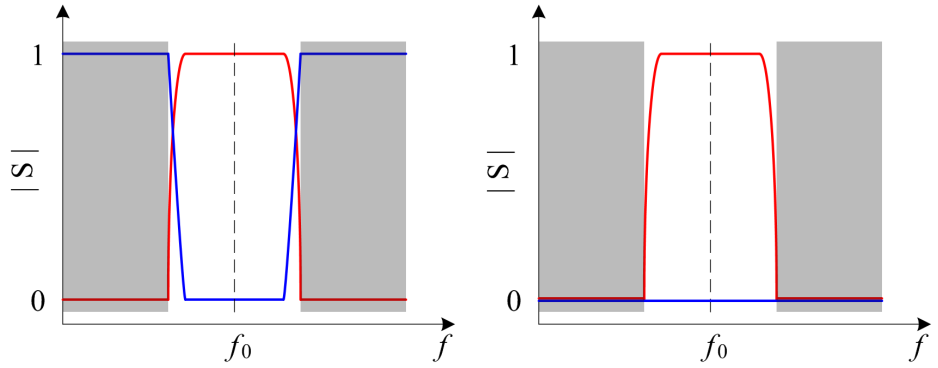


Figure 6.1: Example S-parameters of reflective (a) and absorptive (b) BPFs. (The red curve represents the transmission coefficient, the blue curve represents the reflection coefficient, and the shaded area represents the stopband of the filter.)

by the reflection-generated nonlinear ISI. By introducing lossy elements into the network, absorptive BPFs exhibit little or no reflection in both passband and stopband, at the expense of efficiency. In the rest of this section, two different absorptive (low- and no-reflection) BPFs will be explained based on their circuit models.

6.2.1 Low-Reflection Bandpass Filter

Based on the lossy transmission-line model, a class of low-reflection quasi-Gaussian low-pass filters and their lumped-element approximations are presented in [45], and the corresponding BPFs are presented in [46]. A lumped-element ladder-network approximation of a lossy transmission line is shown in Fig. 6.3(a). By a simple rearrangment of the elements, a low-pass filter

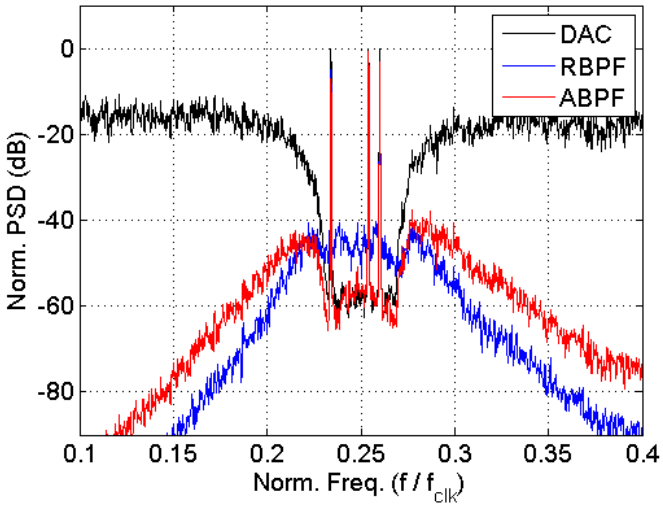


Figure 6.2: Example $\Delta\Sigma$ signal spectra with different types of BPFs. (The passband bandwidth for both 4^{th}-order reflective and absorptive filters is 50 MHz.)

can be obtained as in Fig. 6.3(b), which is also referred to as a complete Gaussian transmission line because of the similar transfer characteristic to a Gaussian filter. An incomplete model is shown in Fig. 6.4(a), where resistors exist only in shunt branches so that the total number of resistors is halved when compared with Fig. 6.3(b). (By duality, resistors can be located only in series branches). For implementation purpose, the lumped-element approximation can be truncated with a finite number of cells, where a cell is defined as the combination of a series branch with a shunt branch. The number is determined by the performance requirement. Usually, in order to have a symmetric topology, the first branch is broken into two halves, and each half is connected to the input or the output respectively, as in Fig. 6.4(b).

Again, a dual alternative, beginning and ending with a series branch, is possible. Using the standard low-pass-to-bandpass filter transformation, based on the model in Fig. 6.4(b), a low-reflection BPF lumped-element model is obtained, as in Fig. 6.5(a).

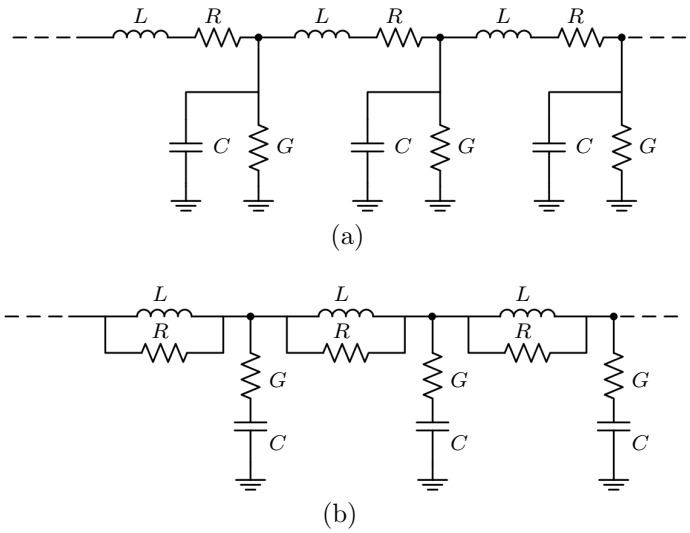


Figure 6.3: Lumped-element approximations of a lossy (a) and a complete Gaussian (b) transmission lines.

6.2.2 No-Reflection Bandpass Filter

As in Fig. 6.5(b), by combining the two half-branches at the input and the output of the model in Fig. 6.5(a), we get a direct low-pass-to-bandpass filter transformation of the lumped-element approximation of the incomplete Gaussian transmission line. Although the BPF is now unreciprocal, by connecting a broadband matched real load at the output, broadband zero reflection is achieved at the input. We refer this type of filter as a *No-Reflection*

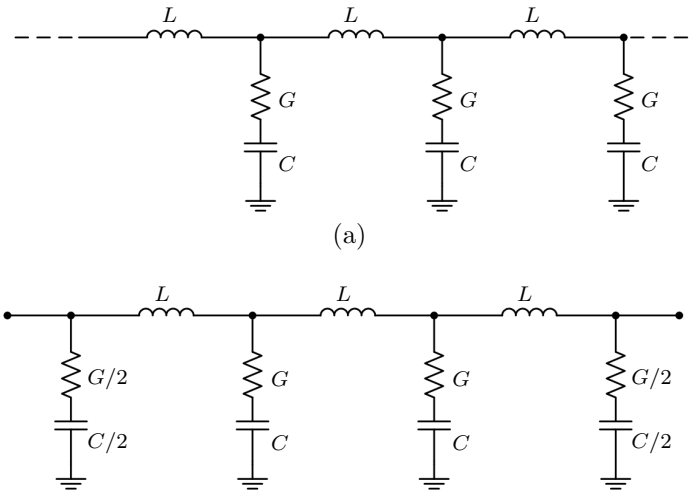


Figure 6.4: Lumped-element approximations for an incomplete Gaussian transmission line (a) and a low-reflection low-pass filter (b).

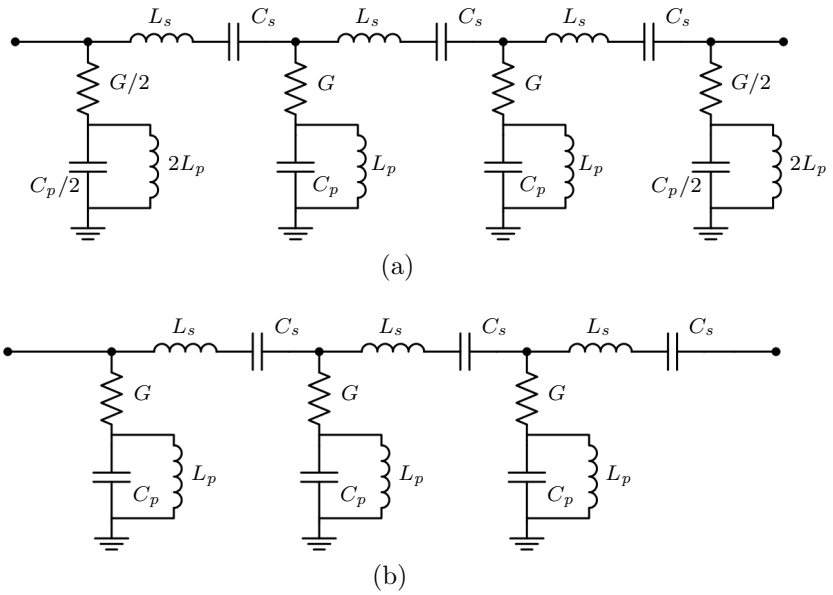


Figure 6.5: Lumped-element approximations of a low-reflection (a) and a no-reflection (b) BPF.

BPF. It can be particularly useful for digital signal measurement and worked as a filtering stage at the input of instruments, where the instrument input impedance is usually a broadband 50 Ω. Additionally, because of similar to the Gaussian transfer characteristic, both low- and no-reflection filters provides good group delay performance.

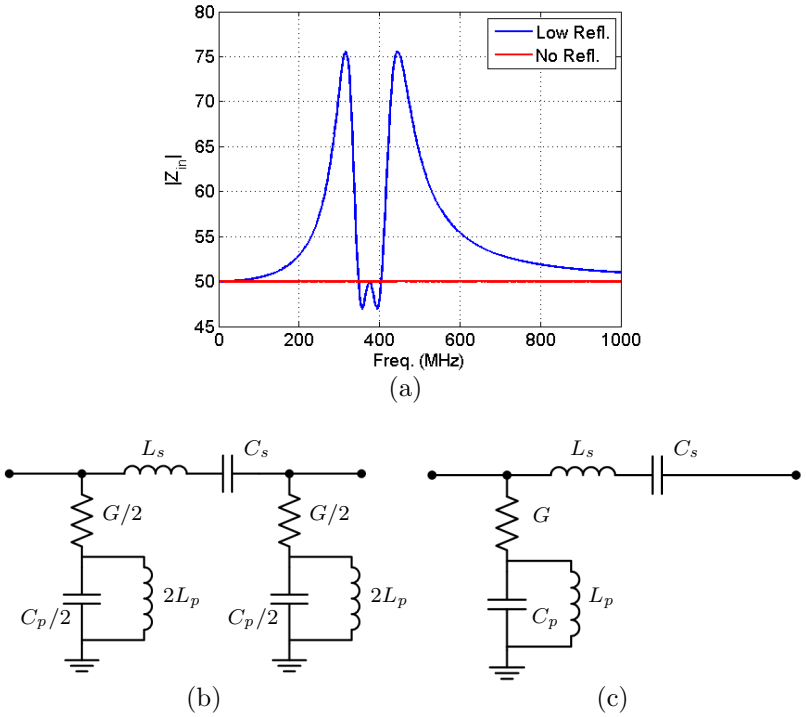


Figure 6.6: (a) The input impedances of the single-cell low-reflection and no-reflection BPFs. Lumped-element approximations for a single cell low-reflection (b) and no-reflection (c) BPF.

Figure 6.6(a) shows the input impedances of single-cell low- and no-reflection BPFs, in Fig. 6.6(b) and (c), with the same value components, where $L_s = 113.7\,\text{nH}$, $C_s = 1.6\,\text{pF}$, $L_p = 4.0\,\text{nH}$, and $C_p = 45.5\,\text{pF}$. It can be

seen that the input impedance varies in a small range for the low-reflection BPF. This variance may cause nonlinear ISI, which will be explained in the next section. It can be proven mathematically that, for the circuit as in Fig. 6.6(b), broadband constant input impedance is achievable when the following conditions are satisfied:

$$L_s C_s = L_p C_p = \frac{1}{\omega_c^2}, \tag{6.1}$$

$$\frac{L_s}{C_p} = \frac{L_p}{C_s} = Z_0^2, \tag{6.2}$$

where ω_c is the resonant center frequency, and Z_0 is the system characteristic impedance.

6.3 Reflective Bandpass Filter Design

For conventional $\Delta\Sigma$ D/A conversion, narrow bandpass filtering is inevitable; the higher the signal-to-noise ratio, the higher the over-sampling rate, which translates to narrower passband. Although reflection is unavoidable for the reflective BPF, it is still possible to consider it as the load circuit in $\Delta\Sigma$ DAC, as long as the introduced nonlinear ISI is kept lower than the required noise level. In this section, by distinguishing different filters based on parameters such as quality factor (Q) and in-band load resistance (R_L), the effects of reflective BPFs on DACs' linearity performance are investigated.

6.3.1 Filter Topology Effects

In order to better understand the nonlinear ISI effects created by different reflective BPFs, time-domain circuit simulations are done in Matlab Simulink with the three-tone $\Delta\Sigma$ test signal as in Fig. 1.1(c). In the simulations, the DAC is modeled as an instantaneous switch, with $R_{on} = 1\,\Omega$ and $R_{off} = 2.5\,\mathrm{k}\Omega$, connected to an ideal bias circuit (an ideal voltage source in series with an ideal RF choke). This allows us to study the nonlinear effects generated from the load circuit alone. The reflective BPFs are simplified as parallel and series RLC circuits. The capacitor and the inductor values for the parallel and series LC circuits are defined in terms of the center frequency ω_0, the quality factor Q, and the load resistance R_L as:

$$C_p = \frac{Q}{\omega_0 R_L}, \tag{6.3}$$

$$L_p = \frac{R_L}{\omega_0 Q}, \tag{6.4}$$

$$C_s = \frac{1}{Q\omega_0 R_L}, \tag{6.5}$$

$$L_s = \frac{Q R_L}{\omega_0}. \tag{6.6}$$

The center frequency of the BPF is determined by the $\Delta\Sigma$ signal. For the test signal as in Fig. 1.1, since $f_0 = 1/4 \cdot f_{clk}$, the filter center frequency becomes $\omega_0 = \frac{\pi}{2} f_{clk}$.

Figure 6.7(a) shows the simulation circuit models of a single-ended DAC with parallel and series RLC load circuits. A current meter is inserted between the switch and the filter. As described in Ch. 4, from this point to

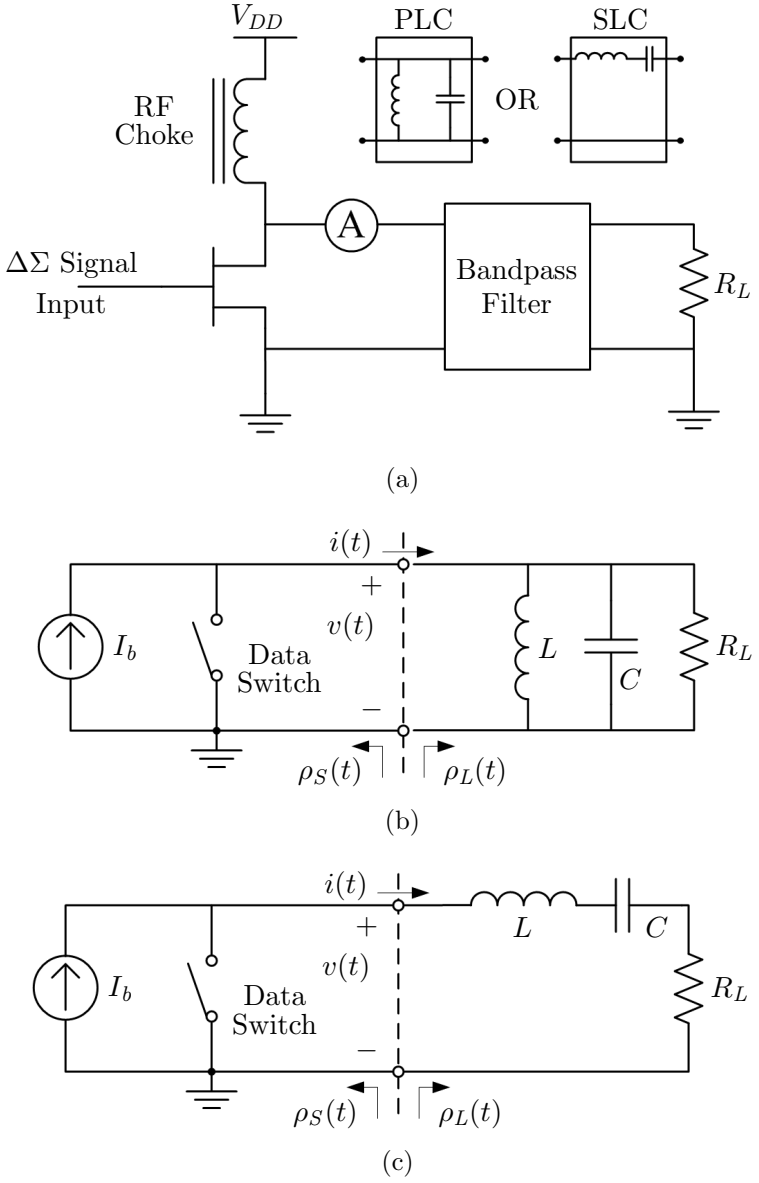


Figure 6.7: Single-ended DAC circuit diagram (a) and models with parallel (b) and series (c) RLC load circuits.

the right in the circuit model, all the components are linear time-invariant. Therefore, the nonlinear ISI is first generated at this point, and its level

can be determined by calculating the in-band signal-to-noise-and-distortion (SINAD) of the recorded current waveform. Table 6.1 shows the calculated SINAD in dB for both parallel and series RLC load circuits when sweeping the values of Q and R_L in our interested range.

Table 6.1: Simulated SINAD (dB) of a single-ended DAC with parallel and series RLC load circuits with the three-tone test signal.

Parallel	$Q = 1$	5	10	50	100
$R_L = 1$	15.84	17.99	20.19	26.50	29.88
5	8.28	8.66	10.52	16.13	19.37
10	6.38	5.83	7.34	12.62	15.47
50	4.15	1.25	1.93	6.20	8.47
100	3.69	-0.13	0.22	4.00	6.04
Series	$Q = 1$	5	10	50	100
$R_L = 1$	7.23	2.09	0.71	-0.60	-0.52
5	5.35	1.07	0.21	0.36	1.24
10	5.11	1.08	0.44	1.38	2.70
50	5.24	2.21	2.37	5.57	7.96
100	5.68	3.44	4.00	8.26	10.73

Generally speaking, in the sweeping value range, the parallel RLC load circuit shows better linearity performance than the series case. To better understand this phenomenon, based on the theoretical analysis in Ch. 4, let us analyze the current waveform of $i(t)$ at the reference plane, as shown by the dashed lines in Fig. 6.7(b) and (c). Based on (4.12),

$$\begin{aligned}\mathcal{R}_L(s) &= (1 + Y(s)R_{ref})^{-1}(1 - Y(s)R_{ref}) \\ &= -1 + \frac{2}{1 + Y(s)R_{ref}} \\ &= 1 - \frac{2}{1 + Z(s)G_{ref}}.\end{aligned} \tag{6.7}$$

By substituting (6.3), (6.4), (6.5) and (6.6), we have

$$\mathcal{R}_L^p(s) = -1 + \frac{2\omega_0 R_L}{QR_{ref}} \cdot \frac{s}{s^2 + \frac{\omega_0(R_{ref}+R_L)}{QR_{ref}}s + \omega_0^2}, \tag{6.8}$$

$$\mathcal{R}_L^s(s) = 1 - \frac{2\omega_0 R_{ref}}{QR_L} \cdot \frac{s}{s^2 + \frac{\omega_0(R_{ref}+R_L)}{QR_L}s + \omega_0^2}, \tag{6.9}$$

where $\mathcal{R}_L^p(s)$ and $\mathcal{R}_L^s(s)$ represent the "reflection" coefficients of parallel and series RLC load circuits, respectively. The Laplace and time-domain transform pairs are $\mathcal{R}_L^{p,s}(s) \leftrightarrow \rho_L^{p,s}(t)$, and

$$\rho_L^p(t) = -\delta(t) + r_p(t), \tag{6.10}$$

$$\rho_L^s(t) = \delta(t) - r_s(t), \tag{6.11}$$

where

$$r_p(t) = \mathcal{L}^{-1}\left(\frac{2\omega_0 R_L}{QR_{ref}} \frac{s}{s^2 + \frac{\omega_0(R_{ref}+R_L)}{QR_{ref}}s + \omega_0^2}\right), \tag{6.12}$$

$$r_s(t) = \mathcal{L}^{-1}\left(\frac{2\omega_0 R_{ref}}{QR_L} \frac{s}{s^2 + \frac{\omega_0(R_{ref}+R_L)}{QR_L}s + \omega_0^2}\right). \tag{6.13}$$

The derivation in Ch. 4 shows that the nonlinear ISI generated from the load circuit is directly related to the time-domain waveform of $\rho_L(t)$. Since the first term of $\rho_L^{p,s}(t)$ is a delta function, the second terms $r_{p,s}(t)$ dominates in the generation of nonlinear ISI effects. By letting $R_{ref} = 50\,\Omega$, chosen based on the switch *on* and *off* resistances defined in the simulation, the time-domain waveforms of $r_{p,s}(t)$ for different Q and R_L can be solved based on (6.12) and (6.13).

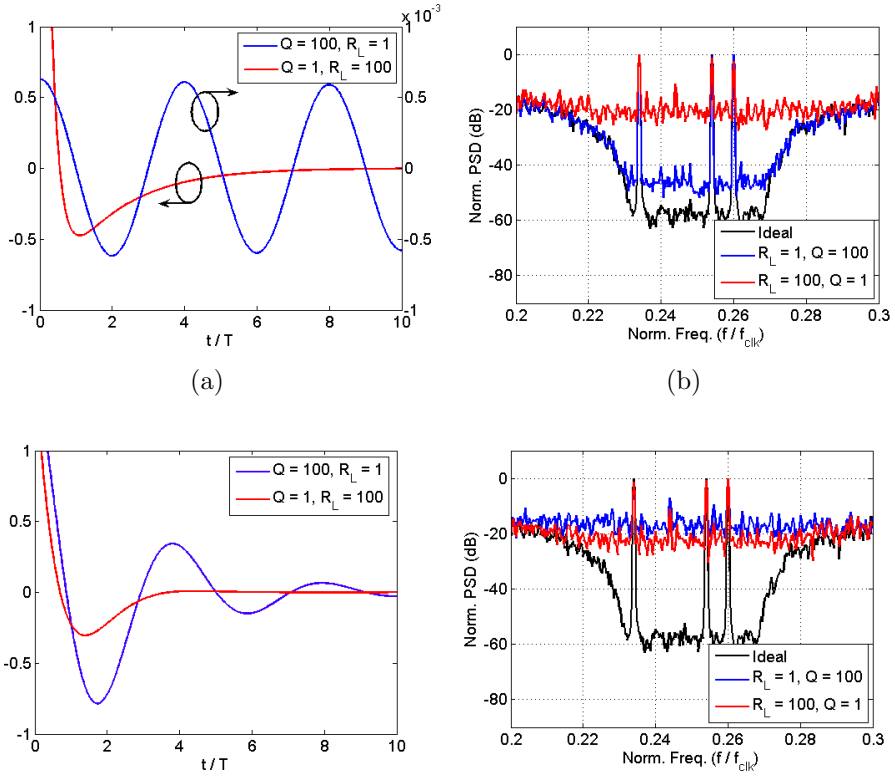


Figure 6.8: Waveform (a) and spectrum (b) of $r_p(t)$ for $Q = 100, R_L = 1$ and $Q = 1, R_L = 100$. Waveform (c) and spectrum (d) of $r_s(t)$ for $Q = 100, R_L = 1$ and $Q = 1, R_L = 100$.

From the form of expression for (6.12) and (6.13) in the Laplace domain, it can be seen that there are three different types of time-domain waveforms of $r_{p,s}(t)$: under damping, critical damping, and over damping. Through comparing the simulated SINAD in Table 6.1 and the corresponding time-domain waveforms of $r_{p,s}(t)$, we can discover that SINAD is improved when $r_{p,s}(t)$ is either under-damped or over-damped. For example, Fig. 6.8 shows

the waveforms and spectra of $r_{p,s}(t)$ for $Q = 100, R_L = 1$ and $Q = 1, R_L = 100$. Although the noise floor of the spectrum in most of the cases is quite high, we can notice that when $r_{p,s}(t)$ is more under-damped, the envelope waveform has a smaller amplitude, which corresponds to smaller amplitude of the nonlinear ISI terms; when $r_{p,s}(t)$ is more over-damped, the envelope waveform decays faster, which corresponds to fewer nonlinear ISI terms. In order to achieve good SINAD for single-ended configuration, it requires the time-domain waveform of the load circuit to be either significantly under- or over-damped.

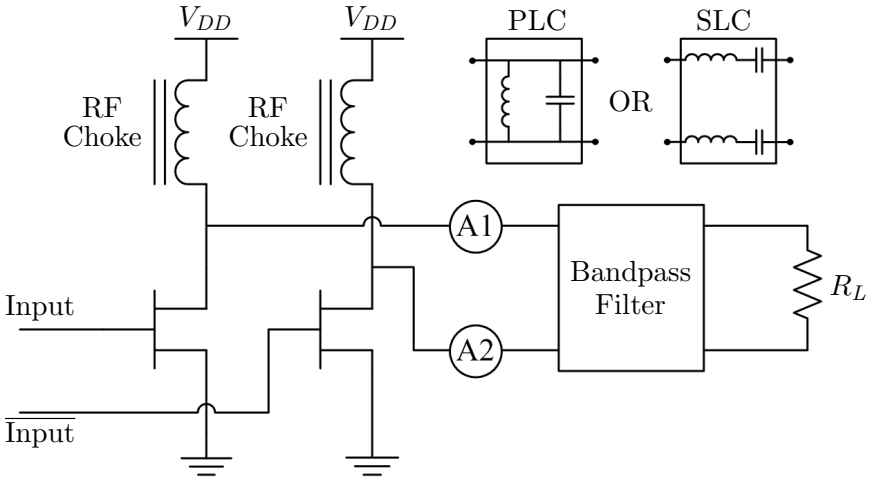


Figure 6.9: Circuit diagram of the differential DAC with differential parallel and series RLC load circuits.)

Similar time-domain circuit simulations are done for the differential DAC with both differential parallel and series RLC circuits, as the diagram shown in Fig. 6.9. The SINAD is calculated based on the difference between the

currents recorded by the current meters, $A1$ and $A2$. The simulated SINAD is shown in Table 6.2, where a similar trend of SINAD versus Q and R_L can be found. The differential configuration offers an overall improvement in SINAD compared to the single-ended case, since the even-order nonlinear ISI terms are reduced.

Table 6.2: Simulated SINAD (dB) of a differential converter with parallel and series RLC load circuits with the three-tone test signal.

Parallel	$Q = 1$	5	10	50	100
$R_L = 1$	41.80	41.86	41.86	41.87	41.87
5	41.19	41.66	41.73	41.79	41.82
10	39.72	41.18	41.38	41.70	41.79
50	30.63	35.04	36.70	40.26	41.25
100	25.66	30.17	32.33	37.96	40.09
Series	$Q = 1$	5	10	50	100
$R_L = 1$	35.57	27.11	21.33	19.72	8.90
5	28.35	21.21	19.33	7.32	7.70
10	24.30	18.87	10.01	7.88	9.41
50	17.77	9.44	8.99	10.63	11.80
100	14.08	10.04	10.63	12.08	12.02

From the simulated results for both single-ended and differential DACs, it can be seen that although both parallel and series RLC circuits demonstrate the same trend of linearity performance change as varying R_L and Q, the parallel configuration has better results for the practical range of R_L and Q ($\in [1, 100]$) of interest.

6.3.2 Filter Order-Number Effects

Based on the previous conclusion, for the test signal with a 60 MHz bandwidth and centered at 375 MHz, reflective BPFs with a parallel LC as the first circuit branch provides better linearity performance for the one-bit DAC. Next, effects of the filters' order number on single-ended and differential DACs' signal linearity is investigated. The differential filter is obtained by imaging the single-ended filter circuit over the ground plane and removing the actual ground connection. With a differential load, the symmetric configuration provides common mode rejection.

Table 6.3: Simulated SINAD (dB) of a single-ended and a differential DAC with different orders' maximally flat BPFs with the three-tone test signal.

Single-Ended	2^{nd} order	3^{rd} order	4^{th} order
$R_L = 1$	17.71	18.28	18.51
5	9.12	9.38	9.55
10	6.06	6.14	6.33
50	0.38	0.11	0.42
100	-1.74	-2.06	-1.70
Differential	2^{nd} order	3^{rd} order	4^{th} order
$R_L = 1$	41.80	41.83	41.81
5	40.80	40.99	40.94
10	38.68	39.06	39.05
50	28.61	28.86	29.20
100	23.91	23.89	24.40

Table 6.3 shows the simulated SINAD for both single-ended and differential DACs using different orders of a 60 MHz maximally flat BPF as the load circuit. It can be seen that SINAD changes very slightly as the fil-

ter order is increased, since the filter order does not have a large effect on input impedance. This observation is very useful. In different $\Delta\Sigma$ one-bit DAC designs, after determining the right values for Q and R_L to provide the needed DAC linearity performance, the optional BPF can be designed by determining just the order. However, in a realistic filter, the insertion loss increases with increasing the filter order. Therefore, the filter design is a tradeoff between order and loss.

6.4 Differential Reflective Bandpass Filter Design and Characterization

Besides considering the linearity performance, in the one-bit power DAC design, power conversion efficiency is also a big concern, and the remainder of the chapter attempts the design and characterization of a differential reflective BPF as the load circuit for a differential inductively-biased one-bit DAC. The characterization of a four-port network as a differential two-port network is also given.

6.4.1 Differential Reflective Bandpass Filter Design

Because the $\Delta\Sigma$ test signal is centered at 375 MHz, lumped components are chosen for the BPF implementation. To reduce the design uncertainty caused by the lumped inductor and capacitor value tolerance, a capacitively-coupled

resonator BPF is chosen. The ideal single cell circuit model for the single-ended and differential topologies are shown in Fig. 6.10. With such a circuit configuration, the number of different value components are kept to be the minimum for a BPF, which is only three. Higher-order filters can be realized by cascading more single cells together, where the single cell is designed based on the cell number and the signal bandwidth.

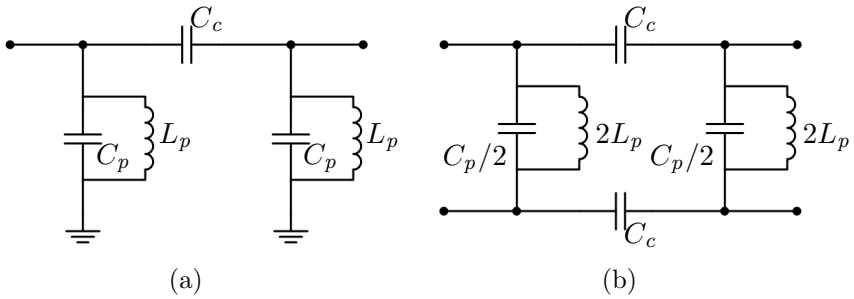


Figure 6.10: Ideal circuit model of a single-ended (a) and differential (b) single-cell capacitively coupled resonator BPF.

Based on the conclusions from Sec. 6.3.1, better signal linearity can be obtained when a small-valued inductor is used in the shunt branch of the BPF. Surface mount air-core inductors from Coilcraft are chosen to reduce the insertion loss of the filter. The 0906 package inductor with $1.65 \pm 10\%$ nH inductance is used in the design. By tuning the component values in the circuit simulation based on the determined inductance, the $22 \pm 5\%$ pF and $68 \pm 5\%$ pF 0603 package capacitors are chosen for the coupled capacitor and the shunt capacitor, respectively.

In order to be able to perform time-domain simulation in Matlab Simulink,

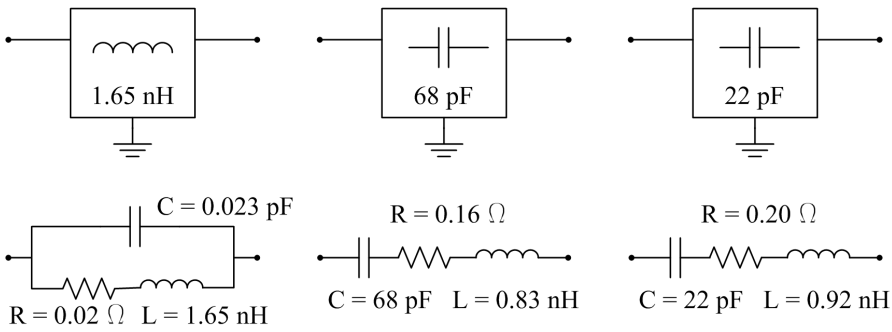


Figure 6.11: Circuit models for the lumped inductor and capacitors.

the circuit models of the lumped components are extracted from the S-parameters provided by the manufacturer, as shown in Fig. 6.11. Based on the S-parameters of the components and the extracted circuit models, the simulation results of the single cell BPF are shown in Fig. 6.12. Figure 6.13 shows the implemented single cell differential capacitively coupled resonator BPF.

6.4.2 Differential Two-Port Network Characterization

The designed differential BPF is a four-port network. By using Agilent PNA E8364B, with an SOLT calibration, a direct four-port measurement of the circuit shown in Fig. 6.13 is done.

In order to eliminate the effect of the transition circuits on the measured results of the differential BPF, a two-port TRL calibration is done to extract the two-port S-parameters of the transition circuit, and its relative de-embedded two-port S-parameters are calculated. Based on this de-embedded

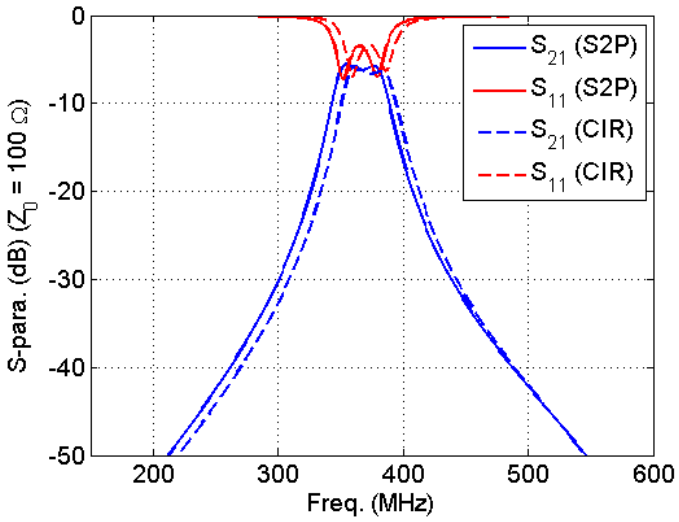


Figure 6.12: Simulation results of the single cell differential BPF with components' S-parameters and circuit models.

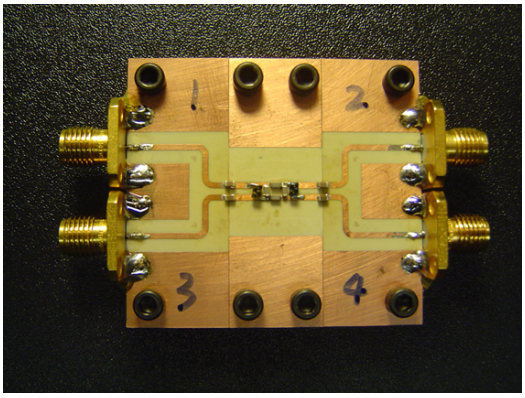


Figure 6.13: Photograph of the single cell differential capacitively-coupled resonator BPF.

two-port S-parameters of the transition circuit and the measured four-port S-parameter, the response of the differential BPF can be computed. The computation can be easily done in a circuit simulator using the model from

Fig. 6.14.

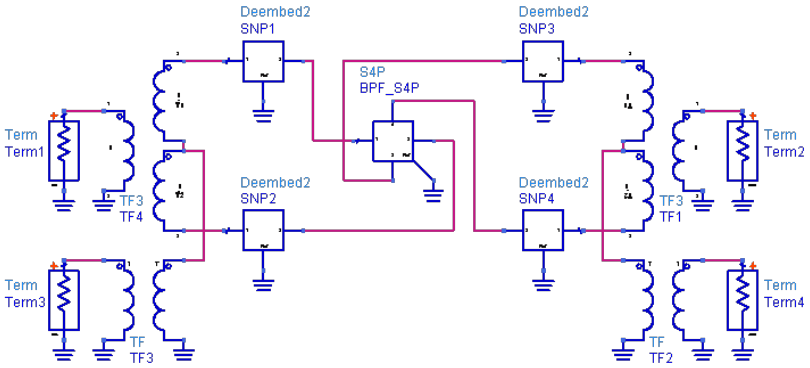


Figure 6.14: ADS circuit model for four-port mixed-mode S-parameters extraction.

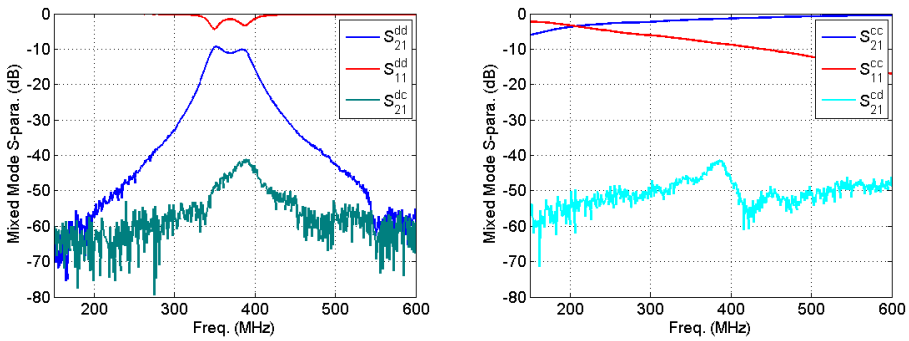
The model in Fig. 6.14 can also be used to calculate the network responses in terms of mixed-mode S-parameters [47] which is a better way to describe the responses of differential circuits. For example, a conventional four-port S-parameter matrix can be transformed into a 4×4 mixed-mode S matrix which consists of four 2×2 sub-matrices, as:

$$\begin{bmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{bmatrix} \Rightarrow \begin{bmatrix} S_{11}^{dd} & S_{12}^{dd} & S_{11}^{dc} & S_{12}^{dc} \\ S_{21}^{dd} & S_{22}^{dd} & S_{21}^{dc} & S_{22}^{dc} \\ S_{11}^{cd} & S_{12}^{cd} & S_{11}^{cc} & S_{12}^{cc} \\ S_{21}^{cd} & S_{22}^{cd} & S_{21}^{cc} & S_{22}^{cc} \end{bmatrix},$$

where the upper left 2×2 matrix represents the differential-mode to differential-mode response, the upper right 2×2 matrix represents the common-mode to differential-mode response, the lower left 2×2 matrix represents the

differential-mode to common-mode response, and the lower right 2×2 matrix represents the common-mode to common-mode response.

6.4.3 Measurement Results

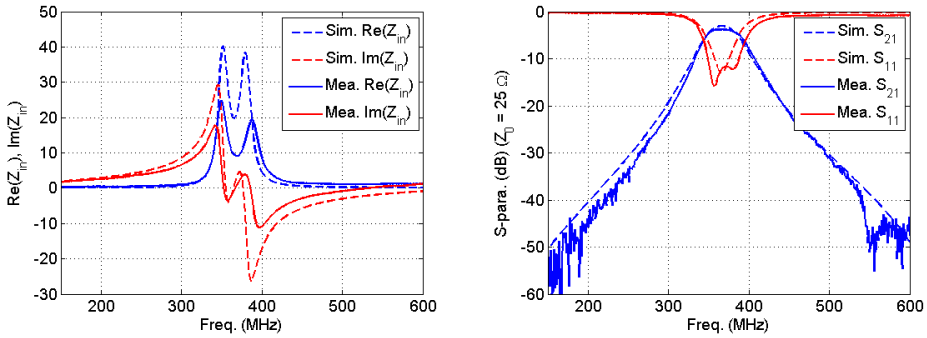


(a) (b)

Figure 6.15: Measured mixed-mode S-parameters of the differential BPF: (a) differential mode, (b) common mode.

The measured de-embedded mixed-mode S-parameters of the differential BPF are shown in Fig. 6.15. Good rejection between the differential and common mode can be seen from the results. Poor differential-mode reflection coefficient is due to the differential BPF not being designed for $100\,\Omega$ (the differential mode impedance for a standard single-ended $50\,\Omega$ system is $100\,\Omega$). This can be seen from the extracted input impedance results for both simulated and measured results, as shown in Fig. 6.16(a). If the differential port impedance is changed to $25\,\Omega$, the differential-mode S-parameters for both simulation and measurement can be re-calculated and shown in Fig.

6.16(b).



(a) (b)

Figure 6.16: Comparison between the simulated and measured results of the differential BPF: (a) input impedance, (b) differential-mode S-parameters in a 25 Ω differential system.

6.5 Differential One-Bit DAC with Reflective Bandpass Filter

A differential one-bit DAC connected to the reflective BPF is designed and built, as shown in Fig. 6.17. Similar to the differential configuration measurement procedure described in Ch. 5, a 50 Ω terminated lumped-element bridge balun is used as a mode conversion circuit between the differential output of the filter and the single-ended input of the measurement instrument.

Although the differential reflective BPF is designed for 25 Ω, being terminated by a 100 Ω differential load, the DAC output signal linearity perfor-

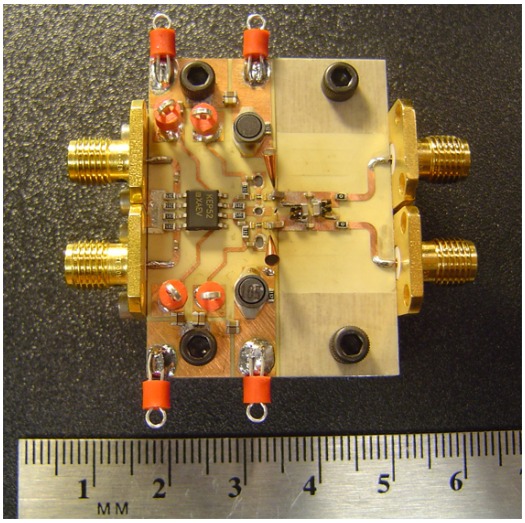
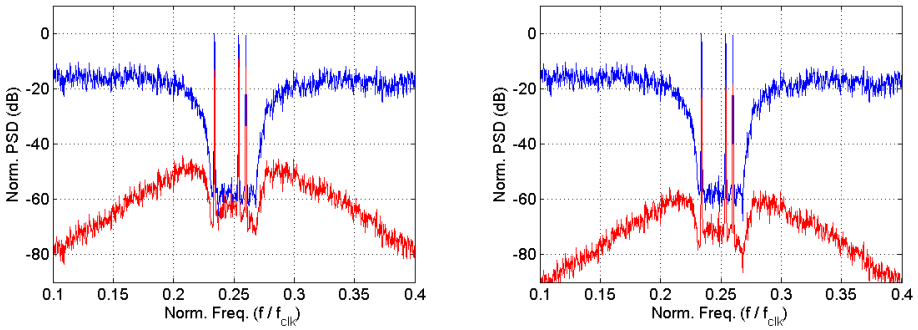


Figure 6.17: Photograph the differential one-bit DAC with the reflective BPF.

mance is not strongly affected. In order to prove this, time-domain simulations are done in Matlab Simulink with modeling the lumped components as the equivalent circuits shown in Fig. 6.11. Current waveforms at the intersection between the DAC and the BPF and across the load are recorded, and the relative frequency-domain spectra are calculated, as shown in Fig. 6.18. It can be seen that the signal spectra at the output of the DAC for both cases (25 Ω and 100 Ω terminations) are similar. The difference between the signal spectra across the load is due to different load reflections.

In-band SINAD at different gate and drain bias voltages of the DAC is measured and plotted together with the simulated result in Fig. 6.19. The nonlinear ISI effects from the transistors and the mismatch between components are not modeled in the simulation. Therefore, the simulated



(a) (b)

Figure 6.18: Simulated signal spectra at the outputs of the DAC and the BPF when the termination resistance is 25 Ω (a) and 100 Ω (b).

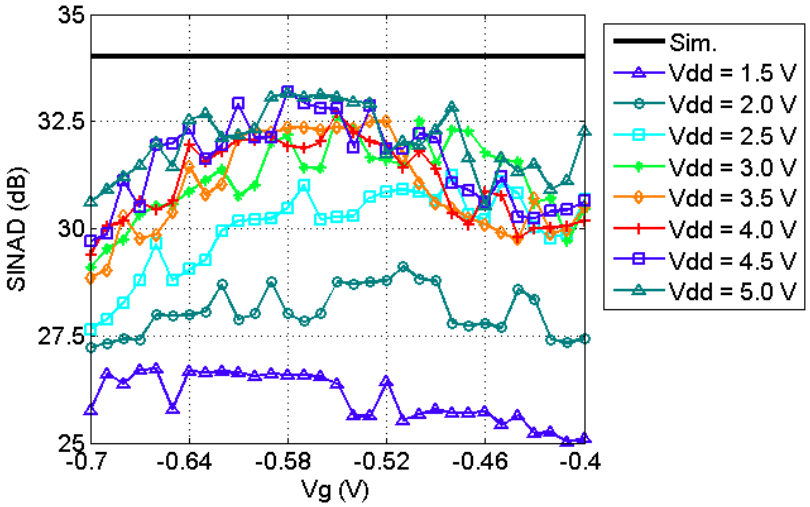


Figure 6.19: Measured and simulated SINAD of the differential one-bit DAC with the reflective BPF.

SINAD is expected to be better than the measured case.

At the same bias conditions ($V_g = -0.55\,\mathrm{V}$ and $V_d = 3\,\mathrm{V}$), the output signal spectra of the DAC with and without the bandpass load circuit,

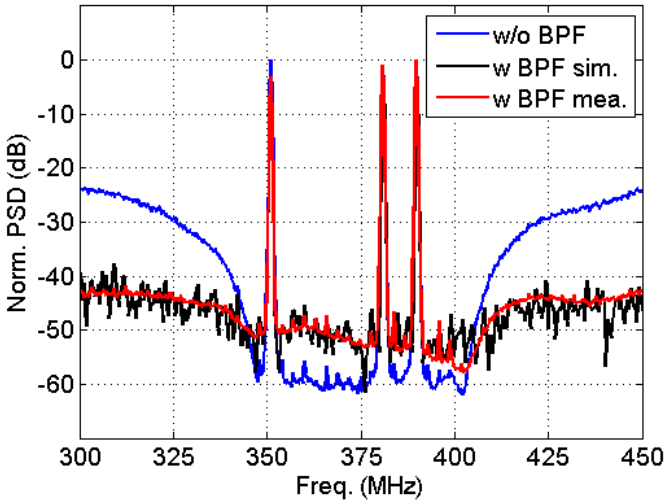


Figure 6.20: Measured output signal spectrum without the BPF, and the simulated and measured signal spectra with the BPF.

respectively, are plotted in Fig. 6.20. It can be seen that most of the out-of-band quantization noise is filtered out by the BPF. However, the filtering effect is not as strong as expected, and the in-band noise floor is increased, which is mainly due to the common-mode feed-through and the reflection from the BPF. The common-mode feed-through is caused by the narrow-band common-mode rejection of the bridge balun. As a comparison, Fig. 6.21 shows the simulated load signal spectra of the DAC with a differential BPF when a differential load is connected, and a single-ended load is connected through the terminated bridge balun circuit. Additionally, because of the common-mode feed-through, the differential-mode power-conversion efficiency of the DAC cannot be measured.

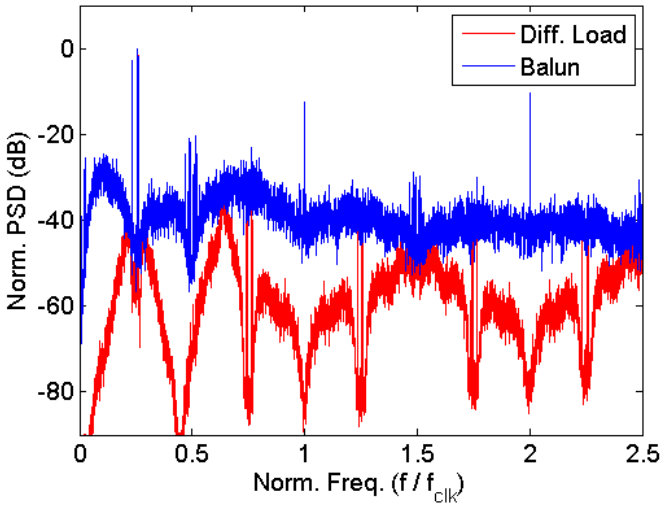


Figure 6.21: Simulated load signal spectra with differential termination and single-ended termination after a narrow-band bridge balun.

6.6 Summary

In this chapter, the effects of different types of BPFs on the linearity performance of the one-bit DAC were discussed. Based on the lossy transmission line lumped-element approximation, symmetric and asymmetric topologies of absorptive BPFs are introduced. The symmetric configuration provides low input reflection and the asymmetric case provides zero input reflection when a broadband matched load is connected at the output. For reflective BPFs with parameters Q and $R_L \in [1, 100]$, using a shunt circuit branch as the first section in the BPF offers better signal linearity, compared to using a series branch. Changing the order number of the same type of BPF affects the output signal linearity only slightly, since the filter order does not have

a large effect on input impedance, but affects the noise band rejection.

A differential reflective BPF with capacitively-coupled resonator configuration is designed and built. With the introduced differential (four-port) device characterization procedure, the filter is measured and compared with the simulation results, where good agreement is achieved. An inductively-biased differential DAC is tested with the differential reflective BPF. An obvious filtering effect on the out-of-band quantization noise is seen. Although the in-band noise level is higher compared to the case without filtering, the measured SINAD agrees with the simulated result, and the spectrum degradation is caused by the reflection from the BPF and the common-mode feed-through. A broadband balun circuit needs to be designed in the future to have better suppression of the common mode signal.

In a practical $\Delta\Sigma$ modulated transmitter, the bandpass filtering can be done by multi-stage filtering and combining different types of filters. The conclusions presented in this chapter can still be applied, where the fundamental idea is that the load-circuit effect on the linearity performance of the DAC is determined by its input impedance.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

$\Delta\Sigma$ modulation has been considered as a method to realize multi-functional transmitters. Theoretically, this approach can produce transmitted signals with high linearity, power and efficiency. In terms of hardware implementation, a $\Delta\Sigma$ modulated RF transmitter can be divided into three stages as: $\Delta\Sigma$ modulator, low-level (one-bit) power DAC, and load circuit. As the interface between the digital and analog signals, the power DAC is a very important part of the system. In order to understand the nonideal hardware effects on the DAC linearity performance, nonlinear ISI in $\Delta\Sigma$ modulated one-bit power DACs has been analyzed in this thesis.

Based on the general nonlinear ISI model of a DAC, an equivalent circuit models in which the transistor switch is modeled as a time-varying conduc-

tance is developed. Following the Hammerstein model, the equivalent circuit is separated into the memoryless time-varying source circuit and the linear time-invariant load circuit. The theoretical solution of the current at the reference plane between the source and load circuits is derived. Based on this, the nonlinear ISI effects generated from the defined source and load are examined. Specifically, the derivation shows that the single-ended power DAC configuration suffers from the nonlinear effects caused by the nonideal switching process and the finite bandwidth response of the components in the load. The differential DAC has improved linearity since the even-order nonlinearities are eliminated, but this is only guaranteed when the circuit elements in the two differential pairs are identical.

Single-ended and differential one-bit power DACs with resistive and inductive bias circuits are designed and characterized. The measurements are done based on a three-tone $\Delta\Sigma$ test signal centered at 375 MHz with 60 MHz possible signal bandwidth. The measured results demonstrate that the single-ended DAC is more sensitive to the bias voltage change than the differential case, and, because of the frequency dependence, the inductive bias circuit introduces stronger nonlinearities compared to the resistive one, but is more efficient. Additionally, nonlinear effects from component mismatch are noticed in the measurements for the differential DAC. It is shown that separate tuning of the bias voltages can be used as an external control method to reduce this effect. All experimental results agree qualitatively with theoretical conclusions.

Based on the nonlinear ISI analysis of the single-ended and differential DACs, effects of output reflective and resistive bandpass filters on the linearity performance of DACs are characterized. Both analytical and simulated results suggest that the single-ended DAC performs better with an absorptive filter, because the nonlinear effects generated by the load reflections at the output are reduced. A differential DAC with a reflective bandpass filter shows improved linearity performance over a single-ended case. It is shown that, for different $\Delta\Sigma$ signals, in order to keep the nonlinear effects lower than the in-band noise level, parameters for the differential reflective bandpass filter need to be carefully chosen. In addition, a no-reflection absorptive bandpass filter configuration is proposed, and the approach to measure and characterize a four-port differential circuit is described.

7.2 Future Work

Although this thesis provides a thorough analysis of the nonideal hardware nonlinear effects on the $\Delta\Sigma$ modulated RF transmitter, there are other aspects of the system implementation that remain to be addressed. In this section, some initial work in the remaining topics is described.

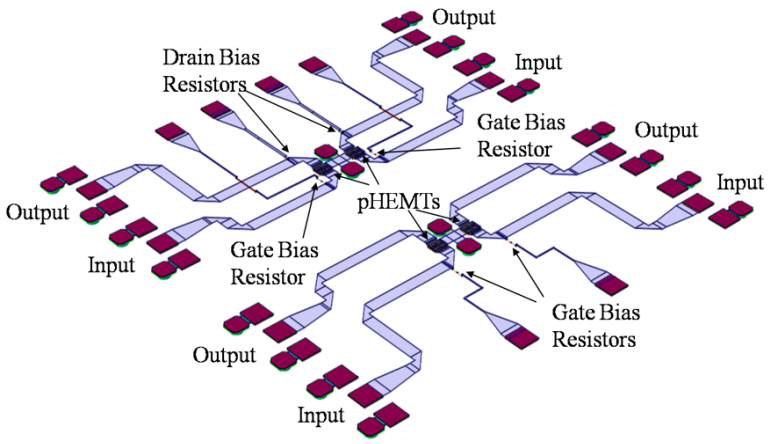
7.2.1 DAC Implementation in MMIC

As presented in Ch. 4, the differential one-bit DAC has improved linearity under the condition that the components in the differential pairs are identical.

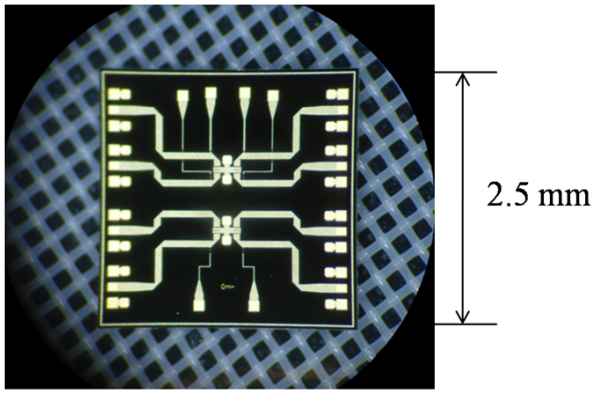
Mismatch between the components will generate additional nonlinear ISI effects. Therefore, it is important to design the DAC circuit to minimize the effects of differences.

The gallium arsenide (GaAs) Monolithic Microwave Integrate Circuits (MMIC) TriQuint foundry technology provides a method to reduce the components mismatch in the differential DAC implementation. Being able to fabricate the differential pairs, especially the transistors, on the same wafer through the same manufacturing process, keeps the uncertainty in device mismatch at a minimum. In addition, the load circuit can be designed on the same MMIC chip as the DAC, where the electrical length of the connection transmission line is shortened and the input impedance of the load circuit can be better controlled.

In the TriQuint TQPED pHEMT 150 mm, 0.5 μm process, both depletion and enhancement mode pHEMTs can be manufactured. In our design, enhancement mode pHEMTs are chosen based on the consideration of device switching speed. The three-dimensional layout plot and photograph of the designed MMIC chip is shown in Fig. 7.1. The 2.5 mm by 2.5 mm chip includes two different differential DAC designs. One is a resistively-biased differential DAC, which has four DC bias pads, and a 50 Ω resistor is used in each drain bias circuit. The other one is designed for a differential inductively-biased DAC, where the inductive bias circuit will be added externally. The MMIC chip has gone through the TriQuint layout verification, has been fabricated, and remains to be packaged for testing.



(a)

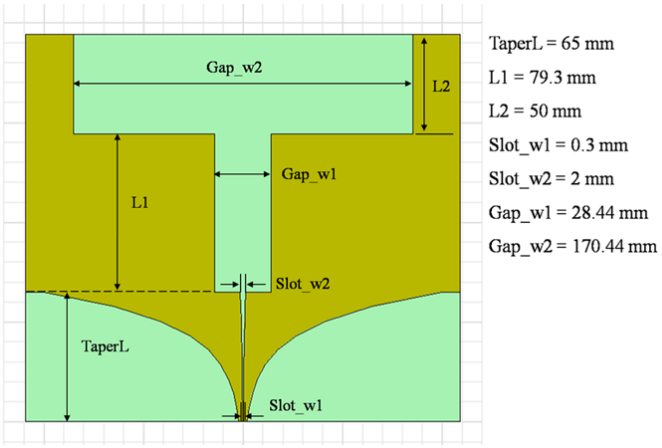


(b)

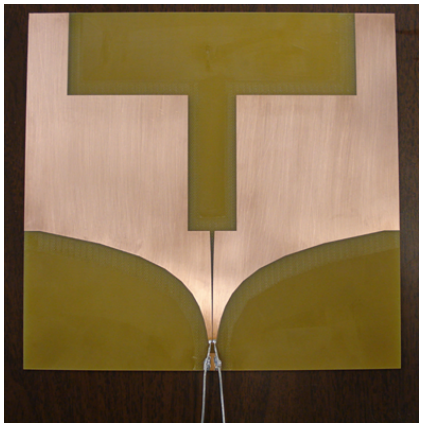
Figure 7.1: The three-dimensional layout plot (a) and photograph (b) of the designed MMIC chip.

7.2.2 Antenna Design and Array Characterization

The antenna in $\Delta\Sigma$ transmitters should be included as part of the load circuit. For a differential one-bit power DAC, a differentially-fed antenna is preferred, since a single-ended antenna would require an additional broadband balun. Conventional antennas that have two conductors and a symmetric geome-



(a)



(b)

Figure 7.2: The schematic (a) and photograph (b) of the designed antenna.

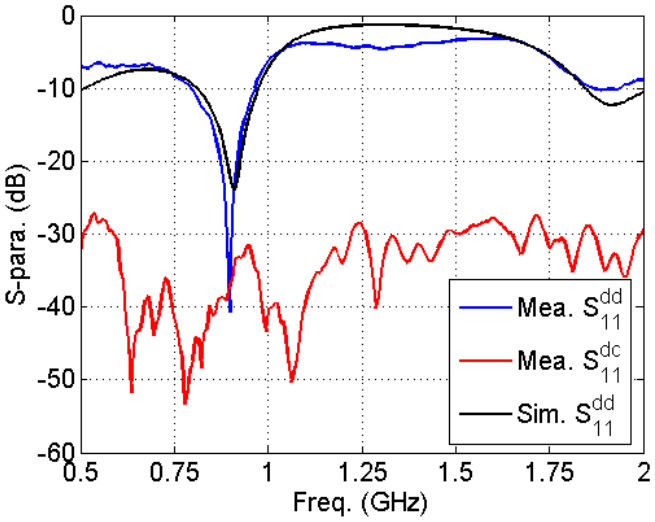
try can be modified to feed differentially. For spatially oversampled linear antenna arrays (period $< \lambda/2$), a printed antenna element is chosen for a preliminary study. A single antenna is designed at 915 MHz and fabricated, as shown in Fig. 7.2. The design frequency is chosen to be in the amateur radio frequency band, allowing measurements outside of a chamber. The an-

tenna is designed based a Vivaldi antenna, where a gradual taper transition is replaced by a quasi-quarter wavelength slot line at the design frequency.

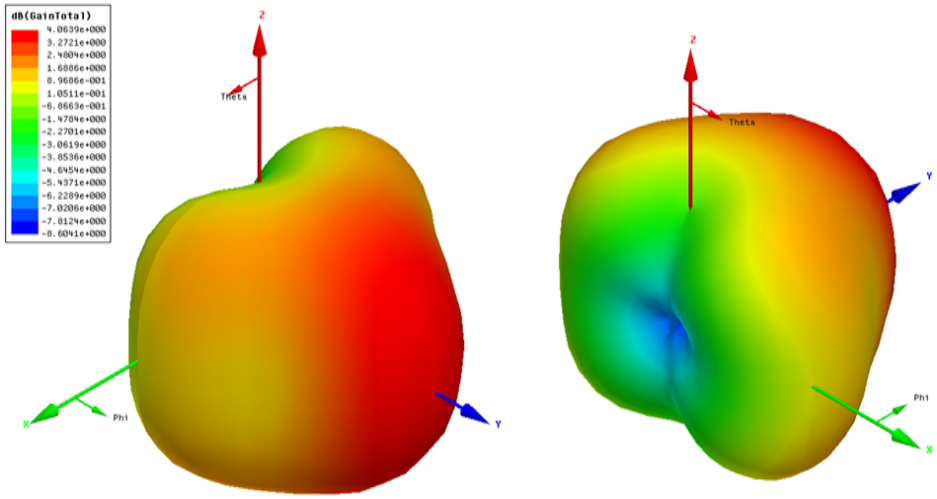
The measured and simulated differential-mode reflection coefficient of the antenna are shown in Fig. 7.3(a), where the measured common-to-differential mode rejection is also plotted. The simulated radiation pattern of the antenna at 915 MHz is shown in Fig. 7.3(b), where the antenna peak gain is 4.07 dB at the end-fire direction. In the future, the antenna should be tested with a 26 MHz bandwidth $\Delta\Sigma$ modulated signal, centered at 915 MHz.

Antenna Array Input Impedance Characterization

In the spatial-temporal $\Delta\Sigma$ modulated RF transmitters, spatially-oversampled antenna arrays need to be used. The spatial-temporal $\Delta\Sigma$ modulator requires the array to have an uniform input impedance matrix, as in an infinite array. In order to satisfy the requirement, passive elements need to be added at the edges of the array. For example, the two-dimensional input impedance



(a)



(b)

Figure 7.3: (a) Simulated and measured differential-mode reflection coefficient of the antenna, and measured common-to-differential mode rejection. (b) Simulated antenna radiation pattern (front and back views) at 915 MHz.

matrix for a finite element array with passive elements looks like

$$[Z_{in}] = \begin{bmatrix} Z^p_{11} & & & \cdots & & & \\ & \ddots & & & & & \\ & & Z^p_{ii} & & & & \\ & & & \begin{bmatrix} Z^a_{jj} & \cdots & Z^a_{jk} \\ \vdots & \ddots & \\ Z^a_{kj} & \cdots & Z^a_{kk} \end{bmatrix} & & & \\ \vdots & & & & & & \\ & & & & Z^p_{ll} & & \\ & & & & & \ddots & \\ & & & & & & Z^p_{nn} \end{bmatrix},$$

where superscripts p represents passive elements and a represents active elements. Ideally, when the active elements have uniform input impedances, the elements in the diagonal direction of the sub-matrix in $[Z_{in}]$ should be all the same.

Based on the single differentially-fed antenna element design for the DAC, here, we propose a method to measure the differential-mode input impedance matrix of the antenna array, and the correct number of "guarding" passive elements for spatially-oversampled arrays can be decided based on it. For a differentially-fed N-element linear array, it can be treated as a $2N$-port network or, ideally, an N-port differential network. With the four-port measurement capability of the Agilent PNA E8364B, multiple differential two-port measurement are done with the remaining antenna elements terminated, where the total measurement number is $N(N-1)/2$. Based on these four-

port measurement results, a $2N$-port scattering matrix can be constructed, and the corresponding N-port differential-mode scattering matrix can be extracted and transformed to the differential-mode input impedance matrix.

7.2.3 Delta-Sigma Modulated Bit Sequence Predistortion

The classical $\Delta\Sigma$ modulation at RF frequencies has been referred to as a naive solution by Gupta [35], because the signal linearity is so vulnerable to hardware nonidealities. He developed a new solution, the M-algorithm, to reduce the signal sensitivity to nonideal hardware effects. Similarly, Scholnik demonstrates that it is possible to encode the $\Delta\Sigma$ bit sequence that certain nonlinear ISI order terms are suppressed in the signal spectrum. We refer to this method as $\Delta\Sigma$ modulated bit sequence predistortion.

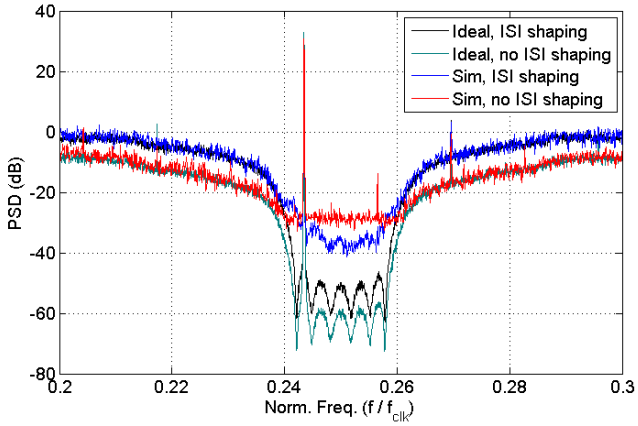


Figure 7.4: Simulated signal spectra with $\Delta\Sigma$ modulated bit sequence predistortion.

As an example, Fig. 7.4 shows the signal spectra for $\Delta\Sigma$ modulation with and without predistortion. It can be seen that the ideal signal has better SNR if predistortion is not included in the modulation. However, if the signals passing through the same DAC, where nonlinear ISI effects exist, the predistorted bit sequence shows better performance, since the 2^{nd} and 3^{rd} orders of nonlinear ISI has been reduced in the example data.

There is a trade-off between the level of predistortion and noise shaping in the $\Delta\Sigma$ modulated bit sequence. Predistortion on massive nonlinear order terms is not practical, since the advantage of $\Delta\Sigma$ modulation is lost in that case. Based on the work presented in this thesis, a more efficient predistortion can be applied if a better understanding of nonlinear ISI in hardware systems is gained.

7.2.4 Conclusions and Future Directions

Ideally, $\Delta\Sigma$ modulated RF transmitters provide an approach to realize high power, efficiency and multi-functional transmission. However, hardware non-idealities impair the system performance. The work presented in this thesis helps in the understanding of nonlinear ISI effects caused by nonideal hardware components, and guides the system components design in terms of linearity performance. Besides the ongoing work mentioned above, future work should also focus on increasing DAC output power with different active devices or multi-stage design, and testing the system with different center frequency and bandwidth $\Delta\Sigma$ modulated signals.

Bibliography

[1] J. Mitola, "Software radios: Survey, critical evaluation and future direction," in *IEEE National Telesystems Conference*, 1992. 1

[2] J. Mitola and Z. Zvonar, *Software Radio Technologies*, The Institiure of Electrical and Electronics Engineers, Inc., 2001. 2

[3] J. Vankka, *Digital Synthesizers and Transmitters for Software Radio*, Springer, 2005. 2, 3

[4] R. Schreier and M. Snelgrove, "Bandpass delta-sigma modulation," in *Electron. Lett.*, Nov. 1989, vol. 25. 2, 82

[5] P. M. Asbeck, T. Itoh, Y. Qian, M. F. Chang, L. Milstein, G. Hanington, P. F. Chen, V. Schultz, D. W. Lee, and J. Arun, "Device and circuit approaches for improved linearity and efficiency in microwave transmitters," in *Microwave Symposium Digest, 1998 IEEE MTT-S International*, Jun. 1998, vol. 1, pp. 327–330. 3

[6] P. Asbeck, L. Larson, Z. Popović, and T. Itoh, *RF Technologies for Low-Power Wireless Communications*, chapter Power Amplifier Approaches for High-Efficiency and Linearity, pp. 189–228, Wiley and Sons, 2001. 3

[7] A. Splett, J. Dressler, A. Fuchs., R. Hofmann, B. Jelonnek, H. Kling, E. Koenig, and A. Schultheiss, "Solutions for highly integrated future generation software radio basestation transceivers," in *Custom Integrated Circuits, 2001, IEEE Conference on.*, May 2001, pp. 511–518. 3

[8] I. Galton, "Delta-sigma data conversion wireless transceivers," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, no. 1, pp. 302–315, Jan. 2002. 3

[9] J. Rode, J. Hinrichs, and P. M. Asbeck, "Transmitter architecture using digital generation of RF signals," in *Radio and Wirelss Conf.*, Aug. 2003. 3

[10] J. Ketola, J. Sommarek, J. Vankka, and K. Halonen, "Transmitter utilizing bandpass delta-sigma modulator and switching mode power amplifier," in *Proc. of the 2004 International Symposium on Circuits and Systems*, May 2004, vol. 1, pp. I–663–6. 3

[11] P. M. Asbeck, L. E. Larson, and I. G. Galton, "Synergistic design of DSP and power amplifiers for wireless communications," *IEEE Trans. Microwave Theory and Techniques*, vol. 49, no. 11, pp. 2163–2169, Nov. 2001. 3

[12] H. Tao, L. Toth, and J. M. Khoury, "Analysis of timing jitter in band-

pass sigma-delta modulators," *IEEE Trans. Circuits and Systems II*, vol. 46, no. 8, pp. 991–1001, Aug. 1999. 4, 28

[13] J. O. Coleman, "The spectral products created by nonlinear intersymbol interference in NRZ data," in *IEEE Asilomar Conf. on Signals, Systems, and Computers*, Nov. 2005. 4, 36

[14] J. O. Coleman, "Modeling finite-memory nonlinearity in unit DAC elements, binary storage channels, and BPSK data channels," in *Proc. 17th (ECS/IEEE) European Conf. on Circuit Theory and Design*, Aug. 2005. 4, 36

[15] T. Shui, R. Schreier, and F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," *IEEE Jour. Solid-State Circuits*, vol. 34, no. 3, pp. 331–338, Mar. 1998. 4

[16] J. J. Wikner and N. Tan, "Modeling of CMOS digital-to-analog converters for telecommunication," *IEEE Trans. Circuits Systems II*, vol. 46, pp. 489–499, May 1999. 4

[17] Y. Tamura, N. Kawakami, O. Akasaka, M. Okada, and K. Koyama, "Beam-forming using multi-dimensional sigma-delta modulation," in *Proc. IEEE Ultrasonics Symp.*, 1998, pp. 1077–1080. 5, 14

[18] D. P. Scholnik and J. O. Coleman, "Joint spatial and temporal delta-sigma modulation for wideband antenna arrays and video halftoning," in *Proc. IEEE International Conf. Acoustic, Speech, and Signal Processing*, Salt Lake City, UT, May 2001. 5, 14

[19] D. P. Scholnik and J. O. Coleman, "Space-time vector delta-sigma modulation," in *Proc. 2002 International Symp. on Circuits and Systems*, Scottsdale, AZ, May 2002. 5, 14

[20] F. Maloberti, *Data Converters*, Springer, 2007. 10

[21] R. Schreier and G. C. Temes, *Understanding Delta-Sgma Data Converters*, The Institiure of Electrical and Electronics Engineers, Inc and John Wiley & Sons, Inc, 2005. 10

[22] D. P. Scholnik, *Shared Wideband Transmit Antenna Arrays: Optimal Pattern Synthesis and Spatio-Temporal Delta-Sigma Modulation*, Ph.D. thesis, University of Maryland, 2006. 11, 15, 24, 71

[23] R. Floyd and L. Steinberg, "An adaptive algorithm for spatial grayscale," in *Proc. Soc. Image Display*, 1976, vol. 17, pp. 75–77. 11, 13

[24] T. D. Kite, B. L. Evans, A. C. Bovik, and T. L. Sculley, "Digital halftoning as 2-D delta-sigma modulation," in *Proc. IEEE Int. Conf. Image Processing*, 1997, pp. 799–802. 12

[25] S. Luschas, R. Schreier, and Hae-Seung Lee, "Radio frequency digial-to-analog converter," *IEEE Jour. Solid-State Circuits*, vol. 39, no. 9, pp. 1462–1467, Sep. 2004. 18

[26] A. Jayaraman, P. F. Chen, G. Hanington, L. Larson, and P. M. Asbeck, "Linear high-efficiency microwave power amplifiers using band-

pass delta-sigma modulators," in *IEEE Microwave Guided Wave Letters*, Mar. 1998, vol. 8, pp. 121–123. 18

[27] M. Iwamoto, A. Jayaraman, G. Hanington, P. F. Chen, A. Bellora, W. Thorton, L. E. Larson, and P. M. Asbeck, "Bandpass delta-sigma class-S amplifier," in *Electron. Lett.*, Jun. 2000, vol. 36, pp. 1010–1012. 18

[28] J. Sommarek, A. Virtanen, J. Vankka, and K. Halonen, "Comparison of different class-D power amplifier topologies for 1-bit bandpass delta-sigma D/A converters," in *Proc. of Norchip Conf.*, Nov. 2004. 18

[29] T. Johnson and S. Stapleton, "RF class-D amplification with bandpass sigma-delta modulator drive signals," *IEEE Trans. Circuits and Systems I*, vol. 53, no. 12, pp. 2507–2520, Dec. 2006. 18

[30] T. Hung, J. Rode, L. E. Larson, and P. M. Asbeck, "Design of H-bridge class-D power amplifiers for digital pulse modulation transmitters," *IEEE Trans. Microwave Theory and Techniques*, vol. 55, no. 12, pp. 2845–2855, Dec. 2007. 18

[31] C. Meliani, J. Flucke, A. Wentzel, J. Würfl, W. Heinrich, and G. Tränkle, "Switch-mode amplifier ICs with over 90% efficiency for class-S PAs using GaAs-HBTs and GaN-HEMTs," in *Microwave Symposium, 2008. IEEE/MTT-S International*, Jun. 2008. 18

[32] M. Weiss, Z. Popović, and F. H. Raab, "Linearity of x-band class-f power amplifiers in high-efficiency transmitters," *IEEE Trans. Microwave Theory and Techniques*, vol. 49, no. 6, pp. 1174–1179, Jun. 2001. 18

[33] N. Wang, X. Peng, V. Yousefzadeh, D. Maksimović, S. Pajić, and Z. popović, "Linearity of x-band class-e power amplifiers in eer operation," *IEEE Trans. Microwave Theory and Techniques*, vol. 53, no. 3, pp. 1096–1102, Mar. 2005. 18

[34] A. K. Gupta, J. Venkataraman, and O. M. Collins, "Measurement and reduction of ISI in high-dynamic-range 1-bit signal generation," *IEEE Trans. Circuits and Systems I*, vol. 55, pp. 3593–3606, Dec. 2008. 19

[35] A. K. Gupta, *High-Bandwidth, High-Dynamic Range Signal Generation Using 1-Bit Digial-to-Analog Conversion*, Ph.D. thesis, Notre Dame, 2005. 19, 119

[36] Xilinx, *Virtex-II Pro and Virtex-II Pro X Platfom FPGAs: DC and Switching Characteristics*, ds083-3 (v4.2) edition, March 2005. 28, 29, 30, 31

[37] J. F. Jensen, G. Raphavan, A. E. Cosand, and R. H. Walden, "A 3.2 ghz second-order delta-sigma modulator implemented in InP HBT technology," *IEEE Jour. Solid-State Circuits*, vol. 30, no. 10, pp. 1119–1127, Oct. 1995. 32

[38] J. V. Adler, "Clock-source jitter: A clear understanding aids oscillator selection," in *Design Feature, Vectron Internatinal, EDN*, Feb. 1999. 32

[39] Picosecond Pulse Labs, *Model 5550B Bias Tee*. 69

[40] S. R. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data*

Converters: Theory, Design, and Simulation, The Institiure of Electrical and Electronics Engineers, Inc., 1997. 71

[41] Q. Mu, L. Sankey, and Z. Popović, "2 gb/s delta-sigma directly driven wireless link," in *Microwave Symposium, 2007. IEEE/MTT-S International*, Jun. 2007. 71

[42] T. Shui, *Lowpass and Bandpass Current-Mode ΣΔ DAC's Employing Mismatch-Shaping*, Ph.D. thesis, Oregon State University, Corvallis, 1998. 82

[43] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, Artch House, 1980. 83

[44] D. M. Pozar, *Microwave Engineering*, John Wiley & Sons, Inc., 1998. 83

[45] A. R. Djordjević, A. G. Zajić, A. S. Stković, M. M. Nikolić, Z. A. Maričević, and M. F. C. Schemmann, "On a class of low-reflection transmission-line quasi-gaussian low-pass filters and their lumped-element approximations," *IEEE Trans. Microwave Theory and Techniques*, vol. 51, no. 7, pp. 1871–1877, Jul. 2003. 83, 84

[46] A. R. Djordjević and A. G. Zajić, "Low-reflection bandpass filters with a flat group delay," *IEEE Trans. Microwave Theory and Techniques*, vol. 53, no. 4, pp. 1164–1167, Apr. 2005. 83, 84

[47] W. R. Eisenstadt, B. Stengel, and B. M. Thompson, *Microwave Differ-*

ential Circuit Design Using Mixed-Mode S-Parameters, Artech House, 2006. 102