# Multi-Frequency Measurements for Supply Modulated Transmitters

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Abstract—Transmitters for high peak-to-average power ratio communication are increasingly using supply modulation to improve efficiency. In addition to a dc component, the dynamic supply may contain ac components up to 500 MHz. The low-frequency (LF) dynamic impedance of the supply terminal of a power amplifier (PA) is often unknown and available nonlinear transistor models are unable to predict dynamic LF effects required for design of wideband efficient supply modulators (SMs). This paper describes a technique to calibrate and measure multi-port multi-frequency parameters of a transistor and PA under supply modulation conditions. The measurement setup is used to characterize the complex drain impedance of GaN transistors and PAs in large-signal operation at X-band with 1-500-MHz LF excitation on the drain terminal, over a range of input power levels. In addition, the LF drain impedance of a 10-GHz monolithic microwave integrated circuit PA with 4-W output power and 60% peak power-added efficiency is measured when the PA is connected to a simple switched resonant SM. The main motivation for this work is to obtain knowledge of the dynamic supply-port impedance that can enable improved PA and SM co-design.

*Index Terms*—Drain impedance, envelope tracking (ET), highefficiency transmitters, microwave power amplifiers (PAs), transition characterization.

## I. INTRODUCTION

W IRELESS systems have increasingly complex modulation schemes and increasing signal bandwidths in order to improve capacity [1]. Such signals have high peak-to-average power ratios (PAPRs) and it is a challenge to design an efficient transmitter that meets linearity requirements, especially for signal bandwidths exceeding a few tens of megahertz. A common transmitter power amplifier (PA) that addresses this problem is the Doherty amplifier [2], which suffers from bandwidth limitations, although there have been recent demonstrations with increased bandwidth operation [3]. Other solutions for amplifying high PAPR signals include outphasing [4] and various forms of supply modulation [5]. Additionally, supply modulation has also been shown to be beneficial to Doherty [6] and outphasing PAs [7].

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Digital Object Identifier 10.1109/TMTT.2015.2458962



Fig. 1. Simplified block diagram of a supply-modulated transmitter. The baseband signal is expressed in envelope and phase form, where most of the envelope signal is input to the drain of the PA through an efficient SM. The phase and a portion of the envelope are unconverted to the carrier that drives the PA input. In this configuration, the device is under multi-frequency excitation and can be viewed as a three-port (ports 1 and 2 are RF, while port 3 is LF). The PAE ( $P_{out}$ ) variation is shown for *static*  $V_{da}$ , however, this variation of PAE is not necessarily true for a variation in supply voltage ( $V_{if}(t)$ ).

Efficiency improvement by supply modulation comes from decreasing wasted dc power when the output power of the RF power amplifier (RFPA) is reduced. Various forms of supply modulation include envelope elimination and restoration (EER) [5], envelope tracking (ET) [8], and polar [9]. Fig. 1 shows a general block diagram of a supply-modulated transmitter with an illustration of power-added efficiency (PAE) versus output power  $(P_{out})$ , PAE $(P_{out})$ , and its dependence on supply voltage  $(V_{dd})$ . The supply modulator (SM) needs to provide sufficient power while following the signal envelope, which for high bandwidth signals implies high supply slew rates [10]. In addition, common stability capacitors in the supply dc circuit have to be eliminated because the supply has high-bandwidth signal content [11], [12]. A problem rarely addressed in the literature is the dynamic envelope-frequency impedance that the PA presents to the SM.[13]1 Additionally, most commercial nonlinear RF transistor models are not designed to predict low-frequency (LF) dynamic behavior at the drain supply port, where the drain supply port is considered the third port. Multi-frequency three-port measurements are therefore very useful for supply-modulated RFPA transmitter co-design.

Related previous work can be found in papers on LF measurements for device characterization [14]–[21], baseband impedance investigation for linearity [22]–[26], and bias line instabilities [12], [27]. Very few systems have been designed to characterize transistors under drive while simultaneously measuring or monitoring baseband (< 500 MHz) performance or properties. However, [28] creates a basic mixer-like transfer function to model inter-modulation products mixed from a

Manuscript received February 05, 2015; revised June 25, 2015; accepted July 11, 2015. Date of publication August 05, 2015; date of current version September 01, 2015. This work was funded by the Office of Naval Research (ONR) under the Defense Advanced Research Projects Agency (DARPA) Microscale Power Conversion (MPC) Program N00014-11-1-0931.

<sup>&</sup>lt;sup>1</sup>This paper is an expanded version from the IEEE MTT-S International Microwave Symposium, Phoenix, AZ, USA, May 17–22, 2015

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Fig. 2. Simplified diagram of measurement setup for a transistor. The RF path uses power sensors to measure the performance of a DUT under normal operating conditions. The tuners present RF loads to the DUT and are approximately short 50- $\Omega$  transmission lines at low frequencies (< 1 GHz). The LF path generates an LF signal and includes biasing for the drain of the DUT. A coupler with an oscilloscope measures the forward and reverse wave parameters of the LF path. The RF and LF paths are split with a special bias tee that differentiates the RF and LF signals (diplexer). A similar bias tee is used on the gate to terminate the LF impedances in 50  $\Omega$  and provide bias. The DUT shown in the figure is a transistor, but can also be a PA.

baseband injection at the drain. Also, efforts have been made to measure and model the nonlinear current source of a transistor by simultaneously exciting LF (< 10 MHz) and RF on the gate of the device and measuring response at LF and RF [29], [30].

For literature in device characterization, device behavior at frequencies less than 1 MHz is important for accurate transistor modeling that takes into account thermal and trapping effects. In [14], it is shown that LF 5 Hz to 1 GHz *S*-parameters of GaN transistors can be used to separate trapping from thermal effects. In [15] and [16], active bias tees with very high LF impedances were implemented from about 5 Hz to 1 MHz to measure LF dispersion. Another application of LF in device characterization is the use of the baseband signal to control the RF impedance of a load–pull setup [18]. Here the baseband in-phase/quadrature (I/Q) are used as the feedback in a closed-loop active load–pull setup. More advance setups involve active envelope frequency load–pull to present a constant impedance across the baseband frequencies [19], [31].

To investigate baseband effects on linearity, a time-domain measurement on a 835-MHz class-B PA under two-tone excitation showed that there is an optimal IF impedance for linearity [22]. Gate voltage dependence and tone separation was investigated in [23], while [24] implements a control circuit to change the baseband impedance. A six-port reflectometer was developed in [25] so that the baseband impedance can be varied with variable gate and drain biases. While [22]–[25] showed useful data for linearity investigations, the results are usually limited to a single-tone RF excitation and no injected power into the drain/collector (the third port) of the transistor. In contrast, our work presents measurements of the broadband drain supply impedance while the PA is under normal large-signal operating conditions, possibly with modulation, and with LF power injected into port 3 to model supply modulation.

A few papers monitor and control the LF stability of a transistor by varying capacitance and/or resistance values on the bias line [12], [27]. The methods presented in these papers accurately measure and account for bias line instabilities, but are specific to the measured PA module and do not give any information on the LF parameters of the transistor themselves.

In this paper, both a single transistor and an amplifier are tested in a three-port configuration under excitation on all ports. The RF impedance and LF impedance are measured in a nominal operating condition under multi-frequency excitation, which is an important difference from previous reported work. The measurement system from Fig. 2 is a system to simultaneously measure the LF drain impedance and dynamics of a transistor while in large-signal RF operation with modulated signals. The carrier frequency in this case is 10 GHz while the LF excitation covers 1–500 MHz. The work in this paper is an extension of [13].

Section II details the measurement setup and calibration. Sections III – V present measured data on an X-band GaN transistor, monolithic microwave integrated circuit (MMIC) PA, and PA with a resonant SM, respectively.

#### II. LF MEASUREMENT SETUP

The test system shown in Fig. 3 was developed to measure LF impedances over a wide bandwidth ( $\sim 1-500$  MHz) while simultaneously measuring the large-signal RF performance of a device-under-test (DUT). The RF path uses a spectrum analyzer to distinguish multiple tones at RF frequencies. Fundamental frequency tuners are used to adjust the RF loading of the transistor. In the LF path, an oscilloscope is used to acquire the time-domain waveform. The oscilloscope is the National Instruments NI PXIe-5162, which has 10 bits of vertical resolution with 2.5-GS/s simultaneous sampling on two channels. The sample rate is controllable with an external clock input and internal rate multipliers and dividers. The two coupled voltage waveforms  $(V_1, V_2)$  are digitized and the Fourier transform taken to find the voltage wave, which can then be converted to pseudo-wave parameters  $(R_1, R_2)$  [32]. The LF signal is ac coupled onto the dc drain voltage. This allows an RF signal generator to provide a LF signal up to the bandwidth of the bias tee. The entire dc + LF block can be replaced with an SM that



Fig. 3. Photograph of setup with labeled: 1) RF source, 2) gate tuner, 3) probe station with DUT, 4) drain tuner, 5) bias tee, 6) LF coupler, 7) oscilloscope, and 8) LF source.

simultaneously supplies the dc and LF signals without re-calibration.

The RF carrier frequency used in this paper is 10 GHz, which is far from the LF of < 500 MHz. This allows simpler filter design of the bias tee to differentiate the RF and LF signals.

#### A. Bias Tee

The bias tee is of particular interest for wide-bandwidth signals as it must be designed to pass the LF content to the transistor while blocking the same content from leaking out to the RF load. The function of the bias tee is similar to a diplexer, but somewhat simpler. For the measurements presented in this paper, the circuit is a parallel combination of a small dc blocking capacitor (in the RF path) and a seventh-order low-pass filter (in the LF path). The bandwidth of the low-pass filter is 1 GHz, which is adequate to pass large bandwidth envelope signals. A small blocking capacitor is necessary to restrict the LF signal from passing to the RF load. As the low-pass filter requires large inductance and capacitance values, parasitics of the elements causing resonances in the RF band are non-negligible and the primary limitation for a wide bandwidth bias tee. Additional elements (an inductor and capacitor) were used in the RF path to help flatten the frequency response in the RF band. A photograph of the bias tee used is shown in Fig. 4 along with its measured S-parameters. There is 1 dB of insertion loss through the RF path and < 0.3-dB loss through the LF path. The match is better than 40 dB at LF and 10 dB at 10.7 GHz.

# B. Calibration

The goal of the setup is to acquire the absolute voltages and currents at the DUT at low frequencies (< 500 MHz). In brief, the thru-reflect-line (TRL) calibration method is performed at RF frequencies with *S*-parameter measurements of the high-frequency couplers to determine the power meter offsets. At LF frequencies, a short-open-load (SOL) with an absolute power calibration is performed coaxially at the LF coupler (as shown by *a* and *b* in Fig. 2) before connecting to the load tuner probe station. De-embedding to the DUT requires an additional SOL calibration using an impedance substrate standard (from Cascade Mircotech). The sampling frequency and number of points used in the fast Fourier transform (FFT) is kept constant throughout the calibration and measurement giving a discrete frequency grid. The LF calibration is described in more depth in the remainder of this section.



Fig. 4. (a) Photograph and circuit diagram of wideband bias tee, which operates as a diplexer. (b) Measured performance of the bias tee.

The T-parameter matrix from the coupler to the DUT is

$$\begin{pmatrix} a \\ b \end{pmatrix} = K \begin{bmatrix} 1 & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{pmatrix} R_1 \\ R_2 \end{pmatrix}.$$
 (1)

The raw digitized parameters  $R_i$  are measured from the oscilloscope and converted into the frequency domain with an FFT. Using the SOL, three of the four *T*-parameters can be found. To facilitate this computation,  $T_{11}$  is assumed to be 1 and a scaling factor, *K*, is used for the absolute power calibration. The reflection coefficient can be written as

$$\Gamma_{\rm std} = \frac{b}{a} = \frac{T_{21}R_1 + T_{22}R_2}{R_1 + T_{12}R_2} \tag{2}$$

where  $\Gamma_{std}$  is the known reflection coefficient of a calibration standard. Using three different standards gives three equations

$$\begin{bmatrix} \Gamma_s R_{2,s} & -R_{1,s} & -R_{2,s} \\ \Gamma_o R_{2,o} & -R_{1,o} & -R_{2,o} \\ \Gamma_l R_{2,l} & -R_{1,l} & -R_{2,l} \end{bmatrix} \begin{bmatrix} T_{12} \\ T_{21} \\ T_{22} \end{bmatrix} = \begin{bmatrix} -\Gamma_s R_{1,s} \\ -\Gamma_o R_{1,o} \\ -\Gamma_l R_{1,l} \end{bmatrix}$$
(3)

where  $R_{i,\text{std}}$  is the measured value with the calibration standards SOL (as denoted in the subscript) connected to the reference plane. Equation (3) is solved for the three *T*-parameters.

Next, a calibrated power meter is connected to the same coaxial plane as the SOL for the power calibration. The calibrated power meter measures the absolute power at the reference plane regardless of the reflection coefficient mismatch: the power measured is the incident power  $P_i = |a|^2$ . In the setup, the measured power directly gives |a|. The reflection coefficient of the power meter can be found using the T-parameters solved for in (3), which allows the computation of the scaling parameter, K. Computation of the calibrated



Fig. 5. Nonlinear device model is not valid under dynamic operation at low frequencies, as expected. Comparison between simulated and measured LF impedance at 10 MHz for the  $10 \times 90 \ \mu m$  device at  $V_d = 20$  V and  $I_{dq} = 100 \text{ mA/mm.}$ 

pseudo-waves at the DUT from the raw measured values is easily performed by using (1). Note that the phase of K is still unknown (ultimately three complex standards were used plus one scalar standard, giving a total of seven parameters versus eight unknowns).

To find the relative phase of K between frequencies, a multisine signal is generated and measured (similar to the method presented in [33]). The Schroeder method is used to synthesize a low peak-to-average ratio multisine waveform with a 10-kHz tone spacing and an arbitrary waveform generator (ARB) generates the signal [34]. First, the relative phase of the tones are measured directly by connecting a calibrated oscilloscope to the output of the ARB. The ARB is attached to the LF coupler on the port closest to the bias tee and the multisine waveform is digitized by the oscilloscope. Since the relative phases between the frequency components are known, the phase of K can be computed by

$$\angle(K) = \angle\left(\frac{b}{T_{21}R_1 + T_{22}R_2}\right) \tag{4}$$

where b is known within a linear phase shift,  $R_i$  are measured, and  $T_{ij}$  are known from the SOL calibration.

The above calibration method allows determination of the voltage, current, and impedance at the LF port of the DUT while the other two ports are measured with standard RF instruments.

## **III. TRANSISTOR MEASUREMENT**

Before investigating the behavior of a PA, it is instructive to investigate the transistor alone. Test devices of  $10 \times 90 \ \mu m$ were fabricated in the TriQuint 0.15- $\mu m$  GaN process on a 4-mil system-on-chip (SiC). These devices are used in the MMIC PAs in the following sections.

Most nonlinear device models are not extracted at low frequencies. Fig. 5 shows a comparison between measurement and simulation of the complex impedance of the drain port over swept baseband input power (or LF input power,  $P_{\rm lf}$ ) at 10 MHz. The model is Angelov based and was extracted with 10-GHz load–pull (original application frequency) at multiple drain voltages with a bias point of 100 mA/mm. The device was measured at 100 mA/mm with a 20-V drain with 14-dBm input RF



Fig. 6. I-V curves for  $10 \times 90 \ \mu m$  device. At each point, the LF impedance is measured. The device is kept under 3.0-W power dissipation to avoid damage to the device.

power. The simulation was performed under the same parameters as the measurement. The simulation result has roughly the same impedance at low input powers, but as the LF input power increases, the trend is opposite of measurement: the LF real part of the impedance decreases by only about 50  $\Omega$  starting at 15-dBm input while the measurement starts an increasing at 2-dBm input with a total increase of 110  $\Omega$ . Another example is shown in [13, Fig. 6], simulation for one of the MMICs shows nonphysical behavior near compression, although RF simulations with the same model accurately predict carrier-frequency behavior. These examples highlight the need to characterized the device for supply modulation purposes under high multi-frequency drive.

## A. Static Drain Impedance

The I-V curves of the  $10 \times 90 \ \mu m$  device were measured and are shown in Fig. 6. At each bias point, the small-signal drain impedance was measured. The device is kept under 3.0-W power dissipation to avoid breakdown or device failure as our measurement bench is not capable of pulsed measurements. The measured LF impedance at 1 MHz is shown in Fig. 7(a). Other frequencies (up to 100 MHz) have nearly identical results because of the very small reactance under static measurements. The measured impedance is not the same as the small signal bias point resistance  $(\frac{\partial V_d}{\partial I_d})$  because of dispersive effects [16], [35], [36]. Since the measurement frequency is above the typical transition frequency for dispersion (e.g., 100 kHz in [16]), the measured impedance is closer to the S-parameters at the particular bias point instead of the dc resistance. The trends shown in Fig. 7(a) can be thought of as a bias dependent switch; at low  $V_q$ , the device is off and presents a high impedance, while when the channel is open (high  $V_q$ ), there is only the resistance of the channel itself. The saturation of the device can be seen as the increase of resistance for higher  $V_d$  (the  $V_q = -3$  V is not saturated, Fig. 6, and so the impedance still decreases for larger  $V_d$ ). Plotting the impedance versus gate voltage in Fig. 7(b), the turn-on voltage can be clearly seen at various  $V_d$  as a large decrease in drain resistance.

The frequency variation of the static bias point can easily be fit by a parallel RC circuit. However, the higher current bias points have a distinct series inductive part that indicates other effects besides a bias-dependent resistance and capacitance. This



Fig. 7. (a) Measured real part of the drain impedance at 1 MHz with no RF input. While the partial derivative of the I-V curves gives a rough approximation in trends of the drain impedance, there is a significant magnitude difference above approximately  $V_d = 5$  V. (b) Real part of the measured drain impedance plotted versus gate bias clearly shows the turn-on voltage for the device at various drain voltages.



Fig. 8. Complex impedance from 10 to 500 MHz of a few bias points of the  $10 \times 90 \ \mu m$  transistor plotted on a 50- $\Omega$  admittance grid. The lower gate bias voltage curves can easily be fit by a parallel *RC* circuit. The higher gate biases (-1 and -2 V) have an inductive part in addition to the *RC* indicating other effects under high current.

can be seen in Fig. 8 where the higher current bias points (-1 and -2 V) have a slant toward the left instead of following the constant admittance circles.

# B. Dynamic Impedance

Source–pull and load–pull were performed on the  $10 \times 90 \ \mu$ m device to find the optimum fundamental frequency RF terminations for maximum PAE at 10 GHz and  $V_d = 20$  V. The peak PAE RF load is 25.0 + j34.2. Measured output power



Fig. 9. (a) Measured RF load–pull performance on  $10 \times 90 \ \mu m$  transistor at 10 mA/mm,  $V_d = 20$  V, and RF  $P_{\rm in} = 22$  dBm. (b)  ${\rm Re}[Z_d]$  at 10 MHz plotted versus RF impedance at various input powers.

and efficiency contours are shown in Fig. 9(a). Over various RF input powers and at each load–pull point, the LF impedance is measured [see Fig. 9(b)]. The value of the real impedance varies not only with the RF load, but with the RF input power as well. For example, at the peak power RF impedance in Fig. 9(a), at low power the drain impedance is high around  $300 \Omega$  and decreases to  $150 \Omega$  at maximum power with 22-dBm input power.

Under supply modulation, the envelope can be considered in the frequency domain as a signal with power over a bandwidth. It is reasonable to expect that the impedance seen by the SM will be dependent on the power that it supplies,  $P_{\rm lf}$ . Figs. 10 and 11 show the variation in real and imaginary parts of the drain impedance versus RF and LF baseband input power for an optimum PAE RF load. When the transistor is biased in class B [see Fig. 11(a)], the impedance generally increases with baseband input power,  $P_{\rm lf}$ , and decreases with RF input power,  $P_{\rm rf}$ . At RF saturation for both 10 and 100 mA/mm, Re[ $Z_d$ ] is at a minimum and roughly uniform across  $P_{\rm in,lf}$  at 150  $\Omega$ . However, at 100 mA/mm [see Fig. 10(a)], there is a second impedance minimum for low RF and LF input power. Note that Im[ $Z_d$ ] also varies significantly over input powers and bias point [see Figs. 10(b) and 11(b)].

### IV. GaN CLASS-B PA MEASUREMENT

The MMIC chosen for measurements is a single-stage class-B PA on 0.15- $\mu$ m GaN. The PA combines two 10 × 100  $\mu$ m (number of fingers × length of finger) devices at the output for 2 mm of output stage gate periphery and 4 W of output power at saturation, and is shown in Fig. 12(a). The MMIC was mounted as in [37] with the off-chip drain



Fig. 10. Measured: (a) real and (b) imaginary drain impedance at 10 MHz and  $V_d = 20$  V versus input RF and LF power at  $I_{dq} = 100$  mA/mm.

capacitances removed. The measurement setup for a PA is simpler than the transistor setup as a bias network is already integrated on the MMIC. In this case, the bias tee was not specially designed to diplex the LF and RF frequencies. In addition to finding the impedance that the PA will present to the modulator, the purpose of the measurements here is to quantify how wide of an LF modulation bandwidth injected through the drain bias line is achievable with a pre-built PA.

The LF equivalent circuit in Fig. 12(b) shows integrated capacitors and resistors on the MMIC and the interconnection to the measurement setup. The PA was designed to work near pinch-off in class-B operation with 5 mA of quiescent current. The drain impedance of the PA was measured under RF operating conditions at 10.1 GHz. The PAE is shown in Fig. 13 and is highest at the nominal drain voltage bias of 20 V and high compression. Simultaneously, impedance was measured across the baseband frequency de-embedded to the off-chip end of the bondwire connected to the MMIC dc bias pad. Fig. 14(a) shows the impedance at 1 MHz. At this frequency, the real part of the impedance decreases and the reactance (not shown) increases with RF input power.

Fig. 15(a) and (b) shows the impedance across frequency when the amplifier is compressed (approximately 34.5-dBm output power with  $V_d = 20$  V). The high bias line capacitance of 87.8 pF causes the impedance to be very low and roughly



Fig. 11. Measured: (a) real and (b) imaginary drain impedance at 10 MHz and  $V_d = 20$  V versus input RF and LF power at  $I_{dq} = 10$  mA/mm.



Fig. 12. Layout of MMIC PAs used for drain impedance measurements. (a) X-band GaN 4-W PA. Two  $10 \times 100 \ \mu m$  devices are combined as a single-stage amplifier  $(2.3 \times 2 \ mm)$ . (b) LF equivalent lumped-element schematic. The shunt *RC* of 29.4 pF and 14  $\Omega$  is for LF stability of the MMIC. The effective shunt capacitance on the MMIC is 87.8 pF.

constant above 80 MHz. At a particular drain voltage, the impedance variation looks like a parallel RC for low frequencies. At higher baseband frequencies, the impedance looking into the bias line becomes inductive, as seen in Fig. 15(b), caused by the wirebond to the die. The equivalent parallel RC of the PA (for frequencies under 100 MHz) is shown in Fig. 16. Over input power and drain voltage, the equivalent capacitance is very close to 88 pF; the bias line capacitance is the dominating factor for the reactive impedance. The resistive part of the impedance, however, depends on the drain voltage



Fig. 13. Measured PAE of the amplifier shown in Fig. 12(a) versus output power and drain voltage.



Fig. 14. (a) Real and (b) imaginary part of the PA bias line impedance at 1 MHz. At low input power, the PA is pinched off and presents a large impedance to the drain modulator. As the RF drive power increases, the real impedance decreases below 100  $\Omega$ .

and input power, generally increasing with  $V_d$  and decreasing with  $P_{in,rf}$ .

Some of the conclusions that can be drawn from the measured data are as follows.

- From Fig. 14(a), it is seen that the real part of the drain impedance for a supply modulated PA varies substantially over drain voltage and output power. The imaginary part also varies significantly at the nominal drain voltage of 20 V. Therefore, the design of the signal-split from Fig. 1 will have a large impact on not only the PAE, but on the SM efficiency, which varies with loading.
- From Fig. 15, most of the frequency variation of the drain impedance is below 100 MHz. This is due to the on-chip



Fig. 15. (a) Real and (b) imaginary impedance of the PA bias line across frequency and drain voltage at 26-dBm input RF power. Due to the large bias line capacitance on chip, the impedance above 80 MHz is nearly zero. The area at 250 MHz at 10 V had a measured negative real impedance indicating possible bias line instabilities.



Fig. 16. Extracted resistance and capacitance of the PA over drain voltage and input power. The bias network capacitance overwhelms the small reactance of the transistors giving nearly constant equivalent capacitance over input power and drain voltage. The real part of the impedance, however, increases with  $V_d$  and decreases with  $P_{in,rf}$  agreeing with the transistor measurements [see Figs. 7(a) and 9].



Fig. 17. Block diagram of transmitter with MMIC PA and resonant modulator. There are two bias line capacitors on the MMIC fixture totaling 0.011  $\mu$ F.



Fig. 18. Time-domain drain voltage and current measured at RFPA bias pad. The RFPA is biased at: (a)  $V_g = -3.0$  V and (b)  $V_g = -4.5$  V while the modulator supply voltage is  $V_d = 8$  V for both plots.

capacitance. The SM bandwidth, efficiency, and possibly stability would be compromised in this case.

• Even when there are no off-chip drain bias capacitors such as was done for these measurements, there is a large frequency variation in the impedance. With a more conventional PA design, the bandwidth would be even more limited and stability a possible issue.

These measurements are representative of only one PA design and will be different for other designs. However, class-B was focused on here because it has the same bias point as other high-efficiency modes of operation (class-E, class-F, class-F<sup>-1</sup>). Class-A PAs will have less impedance variation as shown in the transistor measurements [see Fig. 10(a)], however, under supply modulation are limited to an efficiency of 50%. High-efficiency mode PAs designed for supply modulation must take the bias network and transistor drain impedance variation into account.

# V. TRANSMITTER MEASUREMENT

The measurement setup described here can also monitor performance of and interaction between a PA and SM. The PA from Section IV is next connected to an SM and the system measured with the LF coupler placed between the RFPA and modulator. The modulator in this case is not a standard dc-dc converter assisted with a linear amplifier commonly used for communication signals, e.g., [6], but rather a resonant modulator for AM radar pulses. Radar supply modulation has been explored by other authors and the primary benefit includes reduced radiated spectral emissions. The resonant modulator is a simple design based on a damped LC resonant circuit and has been shown to reach efficiencies > 90% [38], [39]. A simplified diagram of the resonant modulator designed for a resistive load of 220  $\Omega$  is shown in Fig. 17. The inductance and capacitance are switched (using switches SW1, SW2, and SW3) into the circuit to charge and discharge, giving an approximate Gaussian output waveform shape. Since the waveform of interest is no longer a continuous wave as the previous sections of the paper have been, it is more useful to use time-domain voltages and currents. For the measurements, the RF input power is kept constant to keep the load variation of the transistor separate from the modulator PA dynamic interaction.

The transmitter example in this paper uses a resonant modulator because it has a smooth and slow envelope that is well



Fig. 19. RF average output power and drain efficiency over a pulse. By lowering the RFPA gate voltage, the efficiency can be increased with approximately the same output power.



Fig. 20. Simulated efficiency of the resonant modulator and example buck converter versus a static resistive load.

known and has a large voltage variation, going from 0 V to the nominal voltage of the amplifier. In addition, the PA/SM combination is complete and is used as it would be in a system.

The de-embedded voltage and current at the MMIC bias pad (off-chip capacitances were de-embedded) are shown in Fig. 18 for two different gate bias voltages. In the first case [see Fig. 18(a)], the modulator switching times were adjusted for an optimum Gaussian shape for an input power of 24 dBm (red line in online version). As the input power decreases from 24 dBm down to 16 dBm, the load that the modulator sees increases, giving a higher peak voltage and increasing the optimum discharging time for the capacitor causing a negative voltage at the end of the Gaussian pulse. The current follows the same Gaussian shape as the voltage, but there is current



Fig. 21. (a) Waveform and (b) Bode plot simulation of Buck converter with fourth-order output filter designed for a 30- $\Omega$  purely real load. The converter tracks the envelope of a 20-MHz LTE waveform. The envelope is accurately tracked for the designed load of 30  $\Omega$ . However, with the measured load of the PA in Section IV (at  $V_d = 15$  V and 23.8-dBm RF input power), the higher resistance and capacitance cause distortion and significant drain voltage overshoot.

ringing at the peak of the pulse caused by SW1 turning off in the modulator.

In the second case [see Fig. 18(b)], the modulator switching times were adjusted for an optimum Gaussian shape in the voltage for an input power of 0 dBm (black line) at a bias of  $V_q = -4.5$  V. The voltage has Gaussian shape, however, the modulator is supplying very little power to the PA, as the current is very low. As the RF input power increases, the modulator sees a decreasing load, decreasing the peak voltage of the modulator. Additionally, the optimum charging time for the capacitor is decreased, giving the upswing in the voltage at the end of the Gaussian pulse for high RF input powers. However, it is evident the modulator is not designed for such a high load, as there is no current into the PA even at the optimum input power of 0 dBm: there would be no efficiency improvement of the transmitter using an SM because of the very low power that the resonant modulator supplies. This means that the resonant modulator would need to be redesigned if an input power of 0 dBm is desired with a very pinched off PA.

The average RF output power and drain efficiency of the RFPA is shown in Fig. 19. There is a clear tradeoff between RFPA efficiency and modulator distortion (which translates to distortion of the RF output pulse). With a more adequate load for the resonant modulator ( $V_g = -3.0$  V)m the RFPA only reaches 31% drain efficiency. The efficiency can be increased to 38% by pinching the device off, however, large distortions are apparent in the current waveforms from the modulator. Moreover, the resonant modulator works best for a particular load, in this case about 50  $\Omega$ , as shown in Fig. 20. Under pinch-off, the resonant modulator is far from the optimum load impedance, as the transistor has a very high impedance.

The LF measurement setup is used as a diagnostic tool for investigating and optimizing the performance of the resonant modulator when connected to the RFPA. By observing the voltage and the current at the RFPA bias line, distortion and SM/RFPA interactions can easily be seen. The two plots illustrate a tradeoff between RFPA efficiency and linearity performance of the modulator. In this case, to keep a Gaussian shape for different loads, the modulator switching times can be adjusted for the load variation of the RFPA by a simple lookup table. The more optimum solution for output power control is by adjusting the resonant modulator supply voltage directly decreasing the amplitude of the Gaussian pulse. As shown in previous sections, the impedance variation over drain voltage is smaller than the impedance variation over RF input power.

## VI. DISCUSSION

The measurements presented in this paper highlight the need to understand the RF transistor impedances at baseband over all operating conditions for optimal design of the SM. The baseband impedance can vary dramatically over input powers and bias conditions.

For the resonant pulse transmitter example in Section V, it is clear the modulator cannot handle the load variation of the PA caused by RF input power changes with a variable amplitude Gaussian pulse. Instead, the drain supply voltage on the modulator must be changed to minimize the load variation and give variable output powers. This complicates the system implementation of such a modulator requiring another variable voltage supply, albeit one that can be considerably slower than the resonant pulse modulator. In short, for this example, the modulator should be designed to supply power under a higher resistive load or the PA design should be changed to provide a more uniform impedance over RF/LF input powers. Communication transmitters commonly use a switching dc-dc converter assisted with a linear amplifier [6]. The dc-dc converter creates a large amount of noise at baseband and needs a low-pass LC filter to block switching noise from the modulator [40] and some authors have expanded the modulator output reactances to higher order filters [41]. However, even with a filter, the modulator load is determined by the transistor dynamic impedance. As an example, a Buck converter was simulated in Simulink by MathWorks with a fourth-order output filter optimized for a 30- $\Omega$  load [42]. The output voltage waveform for a 20-MHz LTE envelope is shown in Fig. 21(a). There is good tracking with the static 30- $\Omega$  load. However, with a baseband load extracted from Section IV (R= 151  $\Omega$  and C = 86 pF from Fig. 15) at a static  $V_d$  and RF input power, the waveform becomes greatly distorted with large voltage swings, which may cause damage to the amplifier. The large resistance change causes the bulk of the distortion. Fig. 21(b) shows the frequency transfer function for the converter with various loads. The amplitude shows the need for

linearization. This simulation does not include the variation in baseband impedance due to drain voltage, which would create even more distortion. With the potential variation in baseband impedance, the buck converter would no longer be at an optimal load (Fig. 20), decreasing the efficiency of the transmitter system. This further highlights the need to consider the variation in baseband impedance of a transistor or PA for different RF input powers and bias points.

These measurements would be very useful for creating a model and potential implementations for supply modulation [17], [28]. The LF ability of the measurement setup can be applied directly to modeling LF phenomena including trapping effects in the small-signal regime [14], and the nonlinear regime [17], [20], [21], [43]. The goal of this paper is to quantify the dynamic supply-terminal impedance towards the understanding of the interaction of a PA with a wideband (> 10 MHz) SM. If one considers the impedance contours in Fig. 11, the impedance seen by an SM is roughly constant when the transistor is under RF compression. If a transmitter is operated in this region, the output power dynamic range must come entirely from the variation of voltage on the drain (also known as EER) and allows high-efficiency PA operating modes (class-E, class-F, class- $F^{-1}$ ). If a transmitter trajectory includes a combination of RF and LF input power (partial drive modulation), the impedance variation can be minimized by operating the RF transistor in class-A. For the device in this paper, a 50- $\Omega$ variation is observed for a 100-mA/mm bias point compared to > 200  $\Omega$  for partial drive modulation. However, partial drive modulation limits the maximum efficiency of the PA to 50% and system to < 50% depending on the efficiency of the SM.

In summary, a measurement system is developed to characterize static and dynamic supply port impedances from 1 to 500 MHz, while the transistor/PA is under large-signal operation in X-band. The LF port is calibrated to measure the absolute voltage and current. The setup is versatile in that it can measure bare die transistors for modeling and design, PAs for co-design with an SM, and transmitters to inspect interactions between the PA and SM.

#### ACKNOWLEDGMENT

The authors are very grateful for the donation of equipment from National Instruments (Dr. T. Inoue and Dr. Truchard).

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