### Closed-Loop Adaptive Impedance Tuners for Improving RF Transmitter Efficiency

by

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### This thesis entitled: Closed-Loop Adaptive Impedance Tuners for Improving RF Transmitter Efficiency written by Luke S Sankey has been approved for the College of Electrical, Computer, and Energy Engineering

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The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

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Closed-Loop Adaptive Impedance Tuners for Improving RF Transmitter Efficiency

Thesis directed by Prof. Zoya Popović

This thesis addresses the topic of controlling reflections at the output of radio frequency power amplifiers (RFPA) in cases when the amplifier load changes, such as in handset applications in which the proximity of the human operator affects antenna impedance. Specific to handset applications, the impedance mismatch between the PA and antenna is quantified for two commercial handset antennas in various positions relative to the human body and these measurements guide the design of the tuning networks. Figures of merit are established for impedance tuners, and an overview of tuner design goals and methodologies is presented. The specific parameters most relevant for tuner design and characterization include tuning range, tuner loss (a parameter specifically developed in this work), and control.

Several analog impedance tuners are designed, implemented with different tuning devices including a hybrid tuner based on varactor diodes, and a monolithic microwave integrated circuit (MMIC) tuner. In addition, experimental validation at  $1.95\,\mathrm{GHz}$  is presented for the varactor tuner with an analysis of the figures of merit. The local optimizer tuning algorithm is used to demonstrate a closed-loop tuning system with integrated digital control. Digital impedance tuners are designed, including a pHEMT switched-capacitor MMIC tuner, as well as a tuner based on commercial MEMS switches. Experimental results for the MMIC tuner at  $2.45\,\mathrm{GHz}$  are presented in detail. In addition, a digital implementation of a PA tuner combined with closed-loop control is discussed. The performance of the tuning algorithm for various impedance mismatches is evaluated. Finally, overall RF transmitter front end system efficiency is discussed and compared to a conventional approach with no tuning. In addition to tuning impedance, the feedback signal is used as an input to an adaptive power supply. It is shown that up to  $13.2\,\%$  of total efficiency can be gained by simultaneous impedance and bias tuning for a VSWR of 4 and the specific hardware implementation discussed in this thesis.

# Dedication

Cui dono lepidum inanis libri?

To my wife Rebecca, who faithfully put up with my long hours at school, generously paid the bills, and selflessly delayed her own ambitions for five years. Without her, I never would have come to grad school.

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## Chapter 1

### Introduction

This thesis addresses the topic of controlling reflections between radio frequency power amplifiers (RFPA) and antennas in portable microwave front ends. Impedance mismatches at the antenna terminals due to changes in environment or operation result in power reflected towards the output of the final stage of the PA. Reflected power is typically dissipated and thus reduces the transmitter efficiency, and in extreme cases can damage the PA. The goal of the work presented in this thesis is to simultaneously protect the PA while improving overall efficiency through the utilization of a closed-loop impedance control network, possibly in conjunction with a dynamic power supply.

#### 1.1 Motivation for development of impedance tuning networks

A general block diagram of an RF front end transmitter is shown in Fig. 1.1. Most of this thesis will focus on the handset application in which the antenna is not directional and is variably loaded in its near field. Reactive and/or resistive loading in the near field changes the antenna impedance from the nominal matched design value.

Figure 1.1 shows a typical RF front end of a handheld transmitter where a baseband signal is modulated and then mixed with a local oscillator (LO) and amplified before being radiated. The high power RFPA output is protected from reflections by a circulator. An impedance mismatch at the antenna will cause some power to be reflected which could damage the output stage of the PA. The circulator redirects this reflected power into a load, where the power is

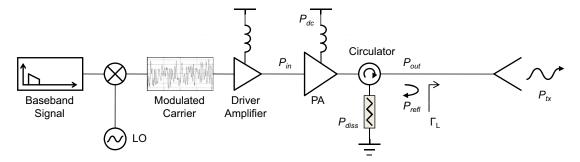


Figure 1.1: Block diagram of an RF front end, where the PA is protected from reflected power (due to impedance mismatch at the antenna) by a circulator. Additionally, a band-pass filter, diplexer, and/or a transmit/receive switch are usually included, but for the purposes of this work, they can be considered part of the load impedance.

dissipated as heat. The input signal power to the RFPA is  $P_{in}$ , the input supply power to the RFPA is  $P_{dc}$ , and the output power of the RFPA is  $P_{out}$ .  $P_{refl}$  is the power that is reflected from the antenna due to impedance mismatch  $\Gamma_L$ . In this diagram,  $P_{refl}$  is equal to the dissipated power,  $P_{diss}$ . The power transmitted by the antenna is  $P_{tx}$ , which should be maintained at a specified level for a given SNR, BER, range, and other application-specific considerations. Drain efficiency (Eq. 1.1) is defined as the percentage of DC power converted to output RF power:

$$\eta_d = \frac{P_{out}}{P_{dc}} \tag{1.1}$$

Total, or overall efficiency (Eq. 1.2) is defined as the percentage of total input power (RF+DC) converted into RF power:

$$\eta_{tot} = \frac{P_{out}}{P_{in} + P_{dc}} \tag{1.2}$$

Power added efficiency (PAE) (Eq. 1.3) is defined as the percentage of the added DC power converted into RF power.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \left(1 - \frac{1}{G}\right) \frac{P_{out}}{P_{dc}} \tag{1.3}$$

Note that for very high gain  $(P_{in} \ll P_{out})$ , high efficiency  $(P_{dc} \approx P_{out})$  amplifiers, PAE and  $\eta_{tot}$  will converge. If  $P_{dc}$  is much higher than  $P_{out}$ , then power is wasted in the PA and efficiency

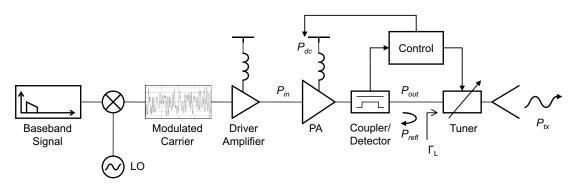


Figure 1.2: Block diagram of an RF front end, where the PA is protected from reflected power when the tuner minimizes the mismatch. The bi-directional coupler samples a portion of the forward and reflected waves which are converted to a DC voltage with detectors. The control block applies an algorithm and adjusts the tuner control and PA supply based on reflected power.

suffers. Therefore, the most efficient systems will maintain  $P_{dc}$  at a minimum level to maintain performance, continually adjusting the DC supply power to maintain the high operating efficiency of the PA.

Figure 1.2 shows the same RF front end but with the circulator replaced by an impedance matching circuit, self-assessment circuit, and controller. The incident and reflected wave voltages are measured by the detector circuit, detailed in Ch. 3. For a well-characterized system composed of a coupler, detector, and impedance tuner, the controller can calculate the voltage standing wave ratio (VSWR) magnitude, and possibly phase, and use those quantities together with the current tuner state to command the tuner to a new state that results in minimum (or acceptable)  $P_{refl}$  from the tuner/antenna interface. When the VSWR becomes larger, there are two problems: 1) a large amount of power is reflected and wasted resulting in a decrease in  $P_{tx}$ , and 2) the supply voltage may no longer be large enough to produce a linear output signal. The solution to both is to increase power to the amplifier, which reduces system efficiency. Figure 1.3 shows how overall efficiency is affected with a few decibels of loss in the output network.

Therefore, by reducing  $P_{refl}$ ,  $P_{tx}$  can be kept as high as possible, reducing the requirements on the PA, a potentially significant source of inefficiency in a transmit chain. In order for overall efficiency to be improved, there are two things to consider: the power consumed by

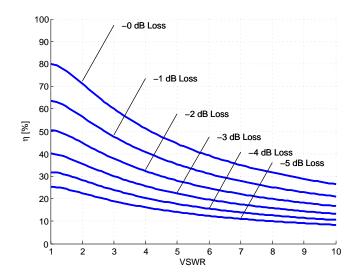


Figure 1.3: Overall efficiency suffers when there is high loss in the output network, and when VSWR is large. For this plot, the following values were used:  $P_{in} = 50 \,\mathrm{mW}, \, P_{dc} = 0.45 \,\mathrm{W},$  and  $P_{out} = 0.4 \,\mathrm{W}$  for a total efficiency of 80% before output losses are added. These values are similar to those found in [1], a 5 GHz class-E amplifier with  $P_{out} = 0.61 \,\mathrm{W}$  and PAE = 72%.

the additional tuner circuitry, and the power saved because of its use. The power consumed by the additional tuner circuitry is due to the control circuits and the tuner loss. The power saved because of the additional circuitry is due to the greater operating efficiency of the amplifier (dynamic supply voltage  $P_{dc}$ ), and the reduction in power lost due to the antenna mismatch ( $P_{refl}$ ). Power saved must be more than power consumed; therefore it is important to minimize the power loss and consumption of the tuning network and to keep the design as simple as possible.

#### 1.2 Background and state of the art review for RF tuners

Impedance tuning circuits have been demonstrated for a variety of applications, such as frequency tunable filters [2] or single frequency variable mode amplifiers [3]. In [4], an automatic tuning network for impedance matching antennas in Terrestrial Trunked Radio (TETRA) mobile stations in the UHF band (380-400 MHz) is presented, using PIN (p-type, intrinsic, n-type semiconductor) diode-switched capacitors. A low-distortion varactor-based impedance tuner is shown in [5] for use in mobile handsets.

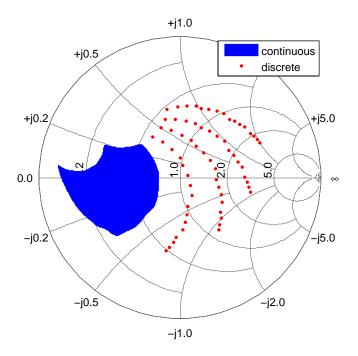


Figure 1.4: Example impedance coverage for continuous and discrete tuners. The continuous tuner can have an output impedance anywhere in the blue region, and the discrete tuner can only have output impedances where the red dots lie. Therefore, the continuous tuner can be more precisely controlled.

Tuners can be continuous or discrete, discussed in more detail in Ch. 4 and Ch. 5, respectively. An example of discrete and continuous tuner coverage is shown on the Smith chart in Fig. 1.4. The blue region indicates the output impedances that can be produced by a continuous tuner, whose analog control voltage can be swept between some  $V_{max}$  and  $V_{min}$ . The red points indicate the output impedances that can be realized by a discrete tuner, whose digital control is capable of setting the tuner impedance to a finite number of complex values.

One possible way to vary reactance is to include a varactor diode in the tuner circuit. Any diode, when reverse-biased, behaves like a voltage-controlled capacitance due to the dependence of the width of the depletion region on applied electric field (voltage). For microwave frequencies, the diodes are usually made from Si or GaAs. With reverse-bias voltage  $V_R$ , the nonlinear capacitance  $C_j$  of a semiconductor diode can be written as:

$$C_j = C_{j0} \left( 1 + \frac{V_R}{V_J} \right)^{-m}$$

Skyworks Part	$C_{j0}$	$V_0$	Type
SMS3923	0.9 pF	0.64 V	Schottky
SMV1405	2.92 pF	0.68 V	Varactor
SMV1430	$12.0\mathrm{pF}$	0.80 V	Varactor
SMV1494	58 pF	0.63 V	Varactor
SMV1129	$27.5\mathrm{pF}$	2.8 V	Varactor

Table 1.1: Example diode parameters for Schottky and varactor diodes from Skyworks.  $C_{j0}$  is the capacitance at zero bias, and  $V_0$  is the built-in voltage of the pn junction. Not every manufacturer gives these parameters.

where  $C_{j0}$  is the value of  $C_j$  obtained for zero applied bias,  $V_J$  is the built-in voltage of the junction, and m is the grading coefficient, a value that depends on the doping profile of the junction, typically  $^{1}/_{2}$  (abrupt) to  $^{1}/_{3}$  (linearly graded). Typical values for  $C_{j0}$  and  $V_{0}$  are shown in Table 1.1. In Fig. 1.5, a diode's total capacitance  $C_T$  decreases with reverse bias  $V_R$ , while Micro-electro-mechanical systems (MEMS) variable capacitors can be designed to have other functional dependence on V, depending on the mechanical design. MEMS variators vary capacitance by a physical deflection of a metal plate or beam. Variator diodes are designed to have a large tuning range, where tuning range is defined as the ratio of maximum capacitance to minimum capacitance. The variator junction is designed such that the width of the depletion region is heavily dependent on bias voltage. Common Schottky diodes can be used as variators with some tuning range, but the capacitance of the metal-semiconductor junction does not depend on V as much as the specially designed variators. PIN diodes have the smallest tuning range of the three. MEMS variable capacitors can have very large tuning ranges but also require large DC control voltages to prevent self-actuation and maintain linearity.

The capacitance tuning range for a varactor is usually 3:1 or less, and they can add non-linearities at higher power levels. In [6], packaged GaAs varactors are used in hybrid  $\pi$ -network design to implement a tuner for use around 2 GHz. With insertion loss (IL) of 0.6-0.9 dB, it matched real impedances in the 4-392  $\Omega$  range to 50  $\Omega$ . An electrically short tuner for 900 MHz was designed and measured with varactor diodes to tune both in frequency (570 MHz - 1.23 GHz) and impedance (16.5  $\Omega$  - 280  $\Omega$ ) [7]. For the frequency tuning, it was stated that IL was always

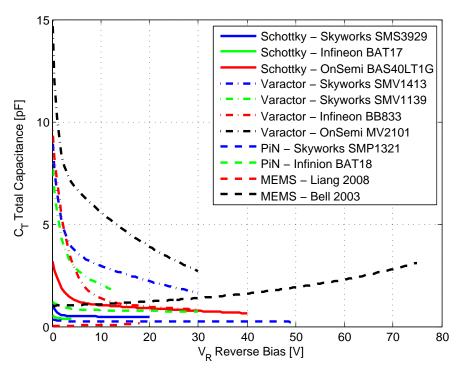


Figure 1.5: C(V) curves for a selection of RF devices. The diode's total capacitance  $C_T$  decreases with reverse bias  $V_R$ , but MEMS variable capacitors can be designed to have other curves. PIN diodes have a small tuning range, and varactors have the largest tuning range. Schottky diodes can be used as variable capacitors, but their tuning range is not as great. MEMS variable capacitors can have very large tuning ranges and control voltages.

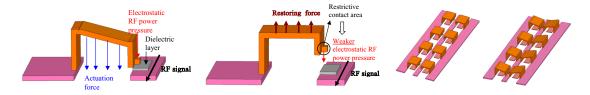


Figure 1.6: 2-state MEMS varactors from [10] showing high capacitance state on the left, low capacitance state in the center, and a varactor-loaded transmission line (impedance phase tuner) on the right.

less than 1 dB. In [8], many varactors are used in a topology designed around 2 GHz to reduce the nonlinearities that come with higher powers and lower bias voltages. Varactors tested at 2 GHz with specifically designed doping profiles that cancel out third-order intermodulation (for two-tone input) are shown in [9] and achieve good linearity.

MEMS varactors vary capacitance by a physical deflection of a metal plate or beam (Fig. 1.6). They have low loss, high power handling, but as a mechanical system, they still tend

to suffer from reliability issues. They require large control voltages to prevent self-actuation and maintain linearity, and hot-switching and stiction are challenging for some of the mechanical designs. In [11, 12], analog and 2-state varactors are used at 25-30 GHz with tunable resonant cells to tune both impedance and frequency simultaneously. A high-Q MEMS varactor with an 8.4:1 tuning range at 500 MHz was presented in [13] that was designed for use between 200-400 MHz, but suitable up to 2 GHz. In [14], a MEMS varactor with tuning range of 3:1 and power handling of 3.5 W at 30 GHz is used to make an impedance tuner with large Smith chart coverage. A loaded-line, single-stub MEMS varactor impedance tuner is developed in [15] for matching low impedances at 20 - 50 GHz, which would be useful with PAs.

Two-state MEMS varactors were shown in [16] with a 7:1 on-off ratio that are capable of handling 1 billion cycles at 1 W, 10 GHz, and up to 10 W max power. In [17], a distributed MEMS transmission-line double-slug tunable matching network was developed using 2-state varactors with an on-off ratio of up to 5:1 for use between 20-50 GHz. A hot-switching MEMS impedance phase tuner operating at high power (18 W) is presented in [10] using 2-state MEMS varactors. Frequency of operation was omitted.

Barium Strontium Titanate (BST) is a ferroelectric ceramic material whose dielectric constant changes with electric field. Thus, by changing the DC voltage across a metal-insulator-metal (MIM) parallel plate capacitor separated by BST, the capacitance changes, and tuning is realized. However, there is also an inherent non-linearity because the dielectric constant changes with input power. A 2.7:1 capacitance ratio BST varactor is used in [18] to implement an impedance tuner for matching  $13-29\,\Omega$  loads around 900 MHz to  $50\,\Omega$ . A 2.2:1 capacitance ratio BST varactor is given in [19] in a cascaded topology for reduced distortion, and then used to build an impedance tuner, a resonator, and a switchable filter for uses around 2 GHz. The tuner has very high loss of around 5 dB, and the filter has isolation of 14.5 dB and IL of 1.8 dB. In [20], a BST capacitor with capacitance range of 2:1 is used to tune the output impedance of a PA and decrease the nonlinearities due to mismatch.

Discrete tuners are more complicated than continuous tuners because a simple analog

Technology	RF loss	RF power	linearity	DC power	speed
Varactor	M	M	M	L	Н
PIN	M	H	L	M	Н
Transistor	M	M	M	M	Н
MEMS	L	M	H	L	M
BST	Н	M	L	L	Н
Mechanical	L	Н	Н	H	L

Table 1.2: Relative benefits of microwave tuner technology. H=High, M=Medium, L=Low

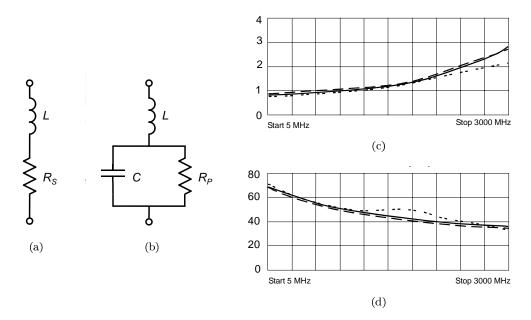


Figure 1.7: There is no ideal switch at microwave frequencies. Basic equivalent circuit models for an RF switch include parasitic reactances and loss [4, 21]. (a) "on" state, (b) "off" state. Published insertion loss in dB for an SPST RF switch, model TWP2231 from Spectrum Microwave [22] (c) "on" state, (d) "off" state. At 3 GHz, loss is 2.5 dB for the "on" state and 30 dB for the "off" state.

control voltage will not control the tuner state without additional hardware, such as an analog to digital converter (ADC); however, they integrate well into digital systems. A digital tuner works by turning on and off some amount of reactance with a switch, and usually the amount of reactance increases by a factor of 2 for each switch in order to realize a uniform distribution of possible reactances. PIN diodes, transistors, and mechanical switches all have been employed in tuner designs. At microwave frequencies, switches cannot be considered to be even approximately ideal, and a general equivalent circuit model of an RF switch is shown in Fig. 1.7. Because of

the parasitics shown, the more switches utilized in a discrete tuner, the more loss it can have.

This illustrates the trade-off in all impedance tuner designs: a tuner with a large tuning range implies more switches, resulting in higher loss.

At RF frequencies, an unbiased PIN diode is a small capacitance, and this is the "off" state. When under a small forward dc bias current ( $\sim 10 \,\mathrm{mA}$ ), the PIN diode behaves like a small ( $\sim 1\,\Omega$ ) resistor [23] at RF frequencies, and this is the "on" state. PIN diodes are used in [4] to enable or disable shunt capacitors, and in [24] to enable or disable strips of ground plane, which results in a change in characteristic impedance of the transmission line. Quite recently, PIN diodes in [25] are used to turn on and off capacitors for the purpose of increasing PAE in 1 GHz class E amplifiers for various  $P_{out}$  levels.

RF transistors are designed to be very fast, and therefore have small gate capacitance which results in small RF leakage so they work well as "off" switches. A 16-state tuner using GaAs HEMT transistors to enable and disable capacitors is shown in [26], but the tuning range is small and the loss is high. A GaAs HEMT was also used in [27, 28] to embed a source tuner in a probe tip for load-pull measurements. Unlike other designs where transistors are used to ground capacitors, the transistors here are used to short inductors, resulting in 50 different tuner states and 3 dB of IL.

A lot of work recently has gone into the optimization of MEMS switches for RF circuits because of their ability to handle power with low loss and high linearity. The first planar reconfigurable double stub tuner with MEMS switches is presented in [32] with 256 states that can match 5-108  $\Omega$  real and -60-48  $\Omega$  imaginary load impedances to 50  $\Omega$  at 20 GHz. Already mentioned for using MEMS varactors, [11] also employed 6 MEMS switches per stub to change the length of tuning stubs in a double-stub tuner. Double-stub tuners in [29] are implemented with MEMS-switched capacitor banks for 10-20 GHz usage, the largest of which had 256 states. [30, 31] show 6-50 GHz tuners that are based on a loaded transmission line topology, with up to 2048 states (11 switched MEMS capacitors). However, loss is defined to be  $1 - |S_{11}|^2 - |S_{21}|^2$ , which is actually Loss Factor as defined in [33] and only correct if port 1 is matched to the

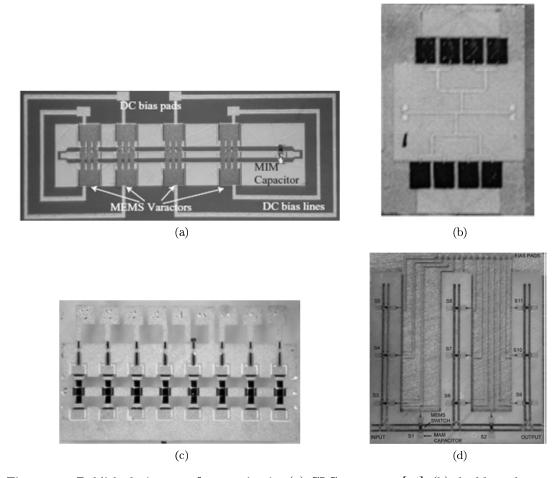


Figure 1.8: Published pictures of tuner circuits (a) CLC+  $\pi$  tuner [14], (b) double-stub tuner [29], (c) loaded transmission line [30], and (d) triple-stub tuner [31].

source [34]. More recently, a 12 stub impedance tuner centered around 1.6 GHz was built with 4096 states to match loads up to a VSWR of 3:1 [35]. A more detailed comparison of tuning circuits demonstrated to date will be given in Ch. 3.

#### 1.3 Tuners for RFPAs

A natural location for an impedance tuner is at the output of an RFPA, since their design goals are complementary. Besides always striving for high efficiency, the design purpose of an RFPA is to achieve maximum output power, while the purpose of an impedance tuner is to minimize reflected power (thus maximizing output power). An automatic closed-loop impedance

tuning system must therefore sample the incident and reflected waves to calculate and minimize VSWR. This, in turn, benefits the RFPA because when VSWR is minimized, the PA efficiency increases. Efficiency will be discussed in more detail in Ch. 6.

Combining impedance tuners with RFPAs is not a new idea. In [36], a 64-state digital tuner is designed specifically for use with X-band class E PAs, with an average loss of 1 dB. A tunable PCS band PA is presented in [20] which uses BST varactors to maintain linearity of the output signal. It showed adjacent channel power ratio (ACPR1) improvement of 4 dB, as compared to a fixed-impedance PA. A 10 GHz RFPA that can operate in either class A or sub-optimal class E by switching tuning stubs between 2 states was able to achieve  $PAE_{1 dB} = 24.1\%$  in class A mode, and  $PAE_{max} = 49\%$  in class E mode, depending on the needs of the system [3]. These are only some of the ways RFPAs can benefit from tunable networks.

The most important factor to consider when designing a tuner for use with an RFPA is overall efficiency improvement, which includes the loss added by the tuner, the signal output power that it saves, and the power it consumes while operating. Fewer components generally means less loss, less complexity, less power consumption, and less component and real-estate costs. Of course, since the RFPA is meant to output high power (< 5 W for handheld radios), the tuner must also be able to pass high power signals without distortion or catastrophic failure.

Stated operating requirements for PAs are often that it must operate properly when presented with a load VSWR of 3:1, and must not be permanently damaged if presented with a VSWR of 10:1. At a VSWR of 3, a quarter of the power is reflected. It is clear in [37] that not only is it inefficient, but the linearity of the system degrades rapidly. For a system that tries to optimize the last few points of efficiency in the transmit path, mismatch is a non-negligible source of inefficiency, and needs to be addressed. Table 1.3 summarizes VSWR and how quickly efficiency can decrease because of mismatch.

VSWR	$\frac{P_{refl}}{P_{out}}$	η
1	0	30%
2	1/9	27%
3	1/4	22%
10	2/3	10%

Table 1.3: VSWR and reflected power, and its effect on a system with 30% nominal matched efficiency.

#### 1.4 Thesis Overview

- Chapter 2 motivates the need for tuners at the output of RF amplifiers in cases when the amplifier load changes, such as in handset applications. An overview of the effects of mismatch on a power amplifier is presented along with basic impedance matching techniques for optimal power transfer. Specific to handset applications, the mismatch is quantified for two commercial handset antennas in various positions relative to the human body. These measurements guide the design of the tuning networks described in subsequent chapters.
- Chapter 3 establishes figures of merit for impedance tuners and overviews tuner design
  goals and the design methodology. The specific parameters most relevant for tuner
  design and characterization include impedance tuning range, tuner loss (a parameter
  specifically developed in this work), and control.
- Chapter 4 discusses the designs of several analog impedance tuners, implemented with different tuning devices: a hybrid tuner based on varactor diodes, and a monolithic microwave integrated circuit (MMIC) tuner. In addition, measurements are presented for the varactor tuner following the figures of merit described in the previous chapter. The local optimizer tuning algorithm is used to demonstrate the closed-loop tuning system. Some results of this chapter have been published in [38].
- Chapter 5 presents designs of digital impedance tuners in GaAs MMICs and using discrete commercial MEMS switches. Experimental results for the MMIC tuner are

presented in detail. In addition, a digital implementation of a PA tuner combined with closed-loop control is discussed. The performance of the tuning algorithm for various impedance mismatches is evaluated. This work is reported in [39].

- Chapter 6 discusses overall system efficiency with a comparison to untuned PAs. In addition to tuning impedance, the feedback signal is used as an input to an adaptive power supply developed by Dr. Rajarshi Paul and Prof. Dragan Maksimović. It is shown that up to 13.2% of PAE can be gained by simultaneous impedance and bias tuning for a VSWR of 4. These results, using the analog varactor-based tuner, are reported in [40].
- Chapter 7 discusses directions for future work and summarizes the contributions of this thesis.
- Appendix A shows additional related work done with Mr. Steve Dunbar at Texas Instruments. Load-pull measurements were performed for a commercial PA/LNA transmitter and a significant mismatch to 50 Ω was found, resulting in the recommendation for a new matching circuit. Additionally, a new printed circuit board Yagi-Uda antenna was designed and integrated with the CC2591 RF front end for significantly improving the range. This work is reported in [41].

## Chapter 2

## Mismatch in RF Amplifiers

#### 2.1 RF Power Amplifiers

An RFPA output matching circuit is typically designed for optimal power and linearity or efficiency, and assumes a constant-impedance load. If the load is mismatched, it is likely that the PA performance will degrade. A SiGe HBT RFPA in [37] is used to show an example in which operating with a VSWR of 10 at the output can reduce PAE from 31% to just 4% at a given bias point. It is therefore important to consider impedance matching networks which maintain performance over various load impedance conditions.

Rhea [42, 43] and many books show which network topologies can match specific ranges of complex impedances, and gives convenient equations from basic principles to convert lumped ideal L-C networks into distributed transmission line sections. These simple L-C matching networks (shown in Table 2.1) can match any load impedance whose reflection coefficient magnitude  $|S_{11}|$  is less than 1.

Impedance is a function of frequency and physical properties, which change with temperature, time, pressure, moisture, etc. In particular, antenna impedances change with near-field loading, which is common in handsets and portable radios (discussed in more detail later in this chapter). Therefore, an RFPA that may be designed to work well under static conditions can become unmatched, resulting in lower power, gain, and efficiency.

The three commonly used gain quantities are transducer gain, power gain, and available gain [44]. These are all power gains  $(\frac{P_{out}}{P_{in}})$ , but  $P_{in}$  can be either power available from the source

Type 1	Type 2	Type 3	Type 4
	D•	<u>-</u>	
Series L	Series C	Shunt C	Shunt L
Shunt C	Shunt L	Series L	Series C
Type 5	Type 6	Type 7	Type 8
<u> </u>	÷	□ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	
Series C	Series L	Shunt C	Shunt L
Shunt C	Shunt L	Series C	Series L
Type 9	Type 10	Type 11	Type 12
<u>-</u>		D=-()=-()	D=/() = <
Shorted Stub	Open Stub	Quarter Wave Line	Arbitrary Length Line

Table 2.1: Types of matching L-networks [42] and their topologies. The area enclosed on the smith chart contains load impedances that can be conjugately matched by the given matching network. Port 1 is on the left, of characteristic impedance, and the load is at port 2, on the right of the matching network.

 $P_{AS}$ , or power delivered to the amplifier  $P_{DS}$ , and they will be equal if the source impedance is a conjugate match to the amplifier input impedance. Likewise,  $P_{out}$  can be either power available from the amplifier  $P_{AL}$ , or power delivered into the load  $P_{DL}$ , which again will be equal if the

amplifier output impedance is a conjugate match to the load impedance.

The most commonly quoted gain for amplifiers is transducer gain  $(G_T)$ , which is a function of both the source and load impedances:  $G_T = \frac{P_{DL}}{P_{AS}}$ . When the amplifier is not well matched,  $G_T$  decreases. Power gain  $(G_P)$  tells how well the amplifier can deliver the power it receives into its load, because it assumes the input will be well-matched:  $G_P = \frac{P_{DL}}{P_{DS}}$ . Available gain  $(G_A)$ , assumes the output is well-matched and is defined as:  $G_A = \frac{P_{AL}}{P_{AS}}$ . Impedance matching networks maximize  $P_{DL}$ , and therefore  $G_A$  is not a useful quantity in this work. Since  $G_T$  and  $G_P$  both depend on load impedance, it is important to understand how they are defined and therefore how they can be maximized with a matching network. For this work,  $G_T$  will be used for gain and loss calculations unless otherwise noted.

For unpackaged RFPAs, it is important to note that due to maximum voltage and current ratings of a transistor  $(V_{max}, I_{max})$ , simple conjugate matching at the output does not necessarily result in the maximum  $P_{AL}$ . Rather, by looking at the IV curves of a transistor, a more optimum load impedance can be found, where  $R_{opt} = \frac{V_{max}}{I_{max}}$ , resulting in less gain, but higher power output  $P_{AL}$ . Cripps [45] states that as a rule of thumb, the output power can be increased by about 2 dB when matching for power instead of using conjugate (gain) matching.

#### 2.2 Load-dependent RFPA performance

As shown above, the RFPA performance depends greatly on the phase and magnitude of the reflected power at the output. For maximum power transfer from the source to the load, a conjugate match is best, as shown in most circuits textbooks [46]. This results in zero overall reflection coefficient as seen by the source, but there may be a standing wave further down the line since the reflection coefficient at the load may not be zero. Consider a simple voltage source with a source impedance  $Z_S$  connected directly to a load impedance  $Z_L$  as in Fig. 2.1 where  $Z_S$ ,  $V_S$  can be the Thévenin equivalent of a source feeding a transmission line. Power into the load  $P_L$  is then defined as:

$$P_L = \frac{|I|^2 R_L}{2}$$

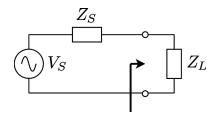


Figure 2.1: A voltage source with impedance  $Z_S$  connected to a load impedance  $Z_L$ .

Solving for I in terms of impedances and substituting gives:

$$P_{L} = \frac{1}{2} \left( \frac{|V_{S}|}{|Z_{S} + Z_{L}|} \right)^{2} R_{L} = \frac{1}{2} \frac{|V_{S}|^{2} R_{L}}{(R_{S} + R_{L})^{2} + (X_{S} + X_{L})^{2}}$$
(2.1)

 $P_L$  is maximized when the denominator is minimized. Therefore,  $X_S = -X_L$ , resulting in:

$$P_L = \frac{1}{2} \frac{|V_S|^2 R_L}{(R_S + R_L)^2}$$

which is maximized for  $R_S = R_L$ . Therefore, maximum power from the source is delivered to the load when  $Z_L = Z_S^*$ , a well-known circuit theory result. However, it is important to note that since  $R_S = R_L$ , half of the system power is dissipated in the source, and half is delivered to the load, which gives a maximum 50% efficiency. It is possible to improve the efficiency, if less delivered power is acceptable, by setting the load resistance larger than the source resistance.

A conjugate impedance match results in the maximum power transfer into a load, assuming a constant voltage source. However, this does not mean that the transistor in an RFPA is operating at its maximum current capability, and therefore it may not result in the maximum possible output power from the transistor. To take advantage of both the highest voltage  $(V_{max})$  and highest current  $(I_{max})$  capabilities of the transistor, a load line can be drawn across the transistor's IV curves whose slope represents the optimal (for highest power output) output resistance  $R_{opt}$  (see Fig. 2.2). When the transistor is asked to operate beyond its maximum voltage and/or current rating, it operates non-linearly.

While  $R_{opt}$  is a good approximation of the optimal load impedance, it is not exact. Since models for transistors are only approximations (and tend to get worse with increasing frequency), any analytical method of finding the optimal load impedance is also only an approximation. In

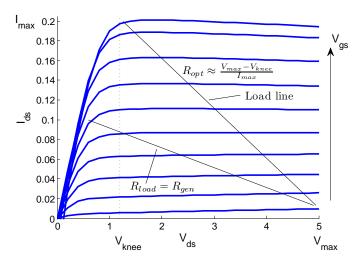


Figure 2.2: The load line produced when using a conjugate match  $(R_{load})$  does not take full advantage of the maximum voltage and current capabilities of the device. Drawing a load line  $(R_{opt})$  on the IV curves of a device is a way of approximating the optimal load impedance for maximum output power from a particular device. The data shown here is from simulations of an unpackaged TriQuint GaAs pHEMT with a 50  $\mu$ m gate width.

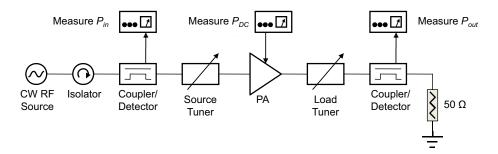


Figure 2.3: Block diagram of a passive load-pull measurement. The device under test is placed between two calibrated impedance tuners, and  $P_{in}$ ,  $P_{out}$ , and  $P_{DC}$  are all measured when searching for the optimal source and load impedance combination.

the absence of a nonlinear model, the only way to accurately find the optimal load impedance for a transistor (amplifier) is experimentally, through what is known as a load-pull measurement (Fig. 2.3). The load-pull measurement involves presenting a variety of source and load impedances to the input and output of the transistor, respectively, while measuring quantities of interest, such as gain, power level, and efficiencies, until the best impedance is found. Since no transistor device is truly unilateral, the source impedance will affect the performance of the amplifier - different source impedances will require different load impedances to find optimal

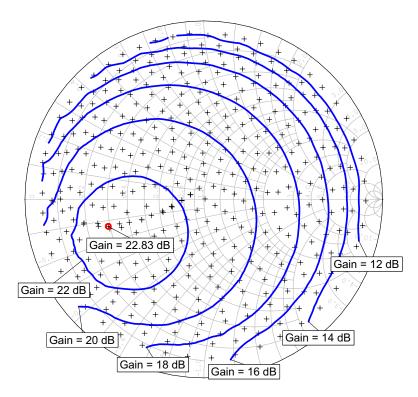


Figure 2.4: Example results from a passive load-pull measurement. Load impedances that result in constant gain are in blue, each measured impedance point is represented by a black +, and the impedance that results in the highest gain from the amplifier is shown with a red  $\circ$ . More information on this Texas Instruments CC2591 RF front end can be found in the appendix.

performance.

Commercial suppliers of microwave impedance tuners for passive load-pull include Focus Microwaves<sup>1</sup> and the Maury Microwave Corporation.<sup>2</sup> Generally, one of these tuners designed for load-pull measurements is a computer-controlled precision-machined mechanical slug tuner. Larger and more expensive models have multiple slugs, so that multiple frequencies or harmonics can be simultaneously tuned. The general process is to first measure the S-parameters of the tuner in those states that cover a desired region of the Smith chart with a desired density of points (referred to as a constellation). Then the tuner is connected to the amplifier, and those impedances are presented to the amplifier. With data from all measured points, the optimal impedance can be calculated, and contour lines plotted for various quantities. Figure 2.4 shows

<sup>&</sup>lt;sup>1</sup> http://www.focus-microwaves.com

<sup>&</sup>lt;sup>2</sup> http://www.maurymw.com

a constellation of measured points for an amplifier discussed in the appendix, and some constant gain contour lines, where impedances that fall on the line all produce the same amplifier gain. The optimal load impedance for gain is typically not the same as the optimal load impedance for power, but contours of constant gain and constant power will overlap, and a suitable compromise  $Z_{opt}$  that gives both sufficient gain and power can usually be found. The chosen load impedance  $Z_{opt}$  is not equal to  $R_{opt}$ , but  $R_{opt}$  is a good starting point when choosing what region of the Smith chart to cover with a load-pull measurement.

The matching network used to transform a 50  $\Omega$  typical load impedance into  $Z_{opt}$  at the output of the transistor must have low loss. Also, if the load is not 50  $\Omega$  and yet the matching network is designed for 50  $\Omega$ , then the matching network will not prevent all power from being reflected, and this will also decrease gain and efficiency. An example of a circuit element whose impedance is designed to be 50  $\Omega$  but is often changing is an antenna with some near-field loading. The reflection loss in the output network can be directly accounted for in efficiency calculations where it decreases  $P_{tx}$ , and in gain calculations as it decreases  $P_{DL}$ . Rewriting  $G_T$  and  $\eta_{tot}$  as a function of IL and  $P_{refl}$  gives:

$$G_T = \frac{P_{DL}\left(P_{IL}, P_{refl}\right)}{P_{AS}} \tag{2.2}$$

$$\eta_{tot} = \frac{P_{tx} \left( P_{IL}, P_{refl} \right)}{P_{in} + P_{dc}} \tag{2.3}$$

The goal of this work is to investigate these quantities after implementing an automatic impedance tuning network, and the results are discussed in Ch. 6.

A study of the effects of load impedance on the performance of power amplifiers in [37] demonstrates by example the independent effects on linearity, efficiency, gain, and output power of both magnitude and phase of load mismatch. For VSWR = 1, there is no reflected power at the output of the PA. As VSWR grows (to a maximum reported of VSWR = 10), the phase of the reflection begins to makes a big difference on whether or not the performance degrades significantly. A large reflection with the proper phase must not, strictly speaking, have a negative effect on the PA performance; however, it is clear that not all power is being delivered

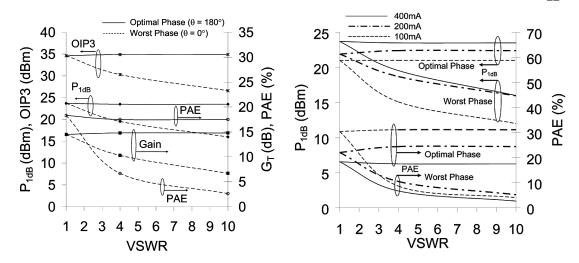


Figure 2.5: The phase of the reflection can have a large impact on the performance of the RFPA. This figure from [37] shows how magnitude and phase can have a measured effect on compression, linearity, gain, and efficiency. The PA was a SiGe HBT at  $1.88\,\text{GHz}$ ,  $V_{CC}=3.3\,\text{V}$ .

to the load while in this state. The specifics of the PA and its interconnects to the load will determine what the best phase of the load should be. It is further shown in [37] that 180 degrees away from the best case phase is the worst case phase in terms of efficiency degradation, and for a particular collector current  $I_{CE} = 200 \,\text{mA}$ , PAE was reduced from 25% down to 5% (see Fig. 2.5).

An amplifier was designed and simulated using a packaged pHEMT transistor from RFMD [47] for class A operation at 2 GHz, matched to 50  $\Omega$ . Harmonic balance simulations using the TOM3 model in Microwave Office from AWR<sup>3</sup> with  $P_{in}=19$  dBm predicted  $P_{out}=30$  dBm, with 50% drain efficiency, and power in the 2nd harmonic 36 dB down from the fundamental. When load impedance is allowed to vary, these quantities change as seen in Figs. 2.6-2.8. Highest efficiency is found with a 50  $\Omega$  load, and linearity, quantified by power in the second harmonic, degrades the most in the first quadrant of the Smith chart, which indicates the amplifier is no longer operating in the class A mode with this mismatched load.

<sup>&</sup>lt;sup>3</sup> http://www.awrcorp.com

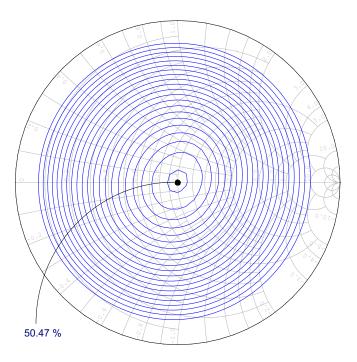


Figure 2.6: Drain efficiency of a simulated class A amplifier as a function of load impedance. Contour lines have  $2\,\%$  spacing.

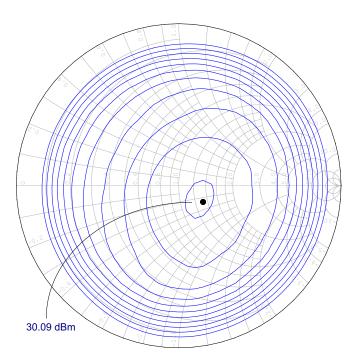


Figure 2.7: Total output power of a simulated class A amplifier as a function of load impedance. Contour lines have  $1\,\mathrm{dB}$  spacing.

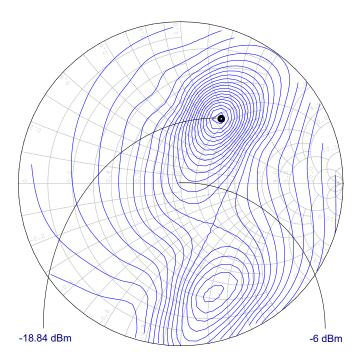


Figure 2.8: Power in the 2nd harmonic of a simulated class A amplifier as a function of load impedance. Contour lines have 1dB spacing.

#### 2.2.1 Operational Modes

Amplifiers can be made to operate in different modes by changing the load and source impedances they see. Amplifier classes are well-described in [45], among others, and will not be dealt with in great detail here. Since impedance is defined by using sine waves at specified frequencies, the linear class A amplifier is the most straight-forward when it comes to impedance matching. The reduced conduction angle of the class AB amplifier results in a slightly smaller loadline value  $R_L$  than for class A. Class C amplifiers are less linear than either class A or B, and have a slightly higher  $R_L$  than class A amplifiers. When impedance matching an amplifier, it is important to match not only the impedance at the fundamental frequency, taking into account the operational mode of the amplifier, but it is also important to present the proper load impedance at the strong harmonics. While harmonic matching is outside the scope of this thesis, it is necessary to mention that impedance matching the harmonic frequencies can be very important to achieving high-efficiency amplifier design [48].

	Class-A			Class-E	
Param.	Standard	Reconfig.	Param.	Standard	Reconfig.
$P_{out,1\mathrm{dB}}$	$20.3\mathrm{dBm}$	$19.7\mathrm{dBm}$	$P_{out, \max}$	$20.7\mathrm{dBm}$	$20.6\mathrm{dBm}$
Gain	$10\mathrm{dB}$	$10\mathrm{dB}$	Gain	$7.9\mathrm{dB}$	$7.8\mathrm{dB}$
$\eta_{D,1\mathrm{dB}}$	27.5%	26.6%	$\eta_{D,\mathrm{max}}$	61.9%	58.3%
$PAE_{1\mathrm{dB}}$	25.3%	24.1%	$PAE_{\max}$	53.2%	49%

Table 2.2: Dual-mode 10 GHz amplifier performance from [3].

As an example of the importance of impedance matching and how it differs depending on operational mode, [3] demonstrates a 10 GHz amplifier that can operate in either class A or suboptimal class E (close to AB) modes, by electronically varying the output impedance between two states and using non-commercial MEMS switches. The design results in 25% efficiency in class A mode, and 50% efficiency in sub-optimal class E mode, as shown in Table 2.2.

#### 2.3 Body proximity effects on handset PAs

Research on the interaction between humans and RF-radiating transmitters (especially in the case cell phones) has been largely focused on specific absorption rate (SAR) and health effects that may be caused by signal exposure [49–52]. As an example, effects beyond simple tissue heating were shown to be possible in a study where participants were calmer during high exposure to GSM signals, and more restless during low exposure [53]. More importantly, [54] indicates that between 53 % and 68 % of the power delivered to the antenna can be absorbed by the head. [55] concludes that better antenna design should be employed to direct RF emissions away from the head.

Besides being concerned about how RF power affects the human body, handheld transceiver designers must also deal with the fact that the human body affects the RF handset within its near field. In the presence of the human body (within wavelengths), antenna input impedance drifts from its design value [56], the radiation pattern changes, and radiation efficiency decreases [57]. Capacitive loading will typically lower resonant frequency [52, 57–59] (see Fig. 2.9) and

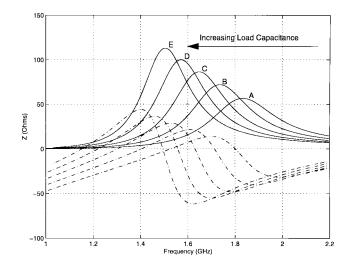


Figure 2.9: Near-field capacitive loading of a cell-phone antenna shifts the resonant frequency down (as shown in this figure from [59]), and degrades the impedance match and radiation efficiency. The solid and dashed lines represent simulated resistance and reactance, respectively, as a function of frequency. Antenna is a planar inverted-F (PIFA) designed for 1.8 GHz (curve A).

this is also the case for all three bands of a tri-band PIFA antenna in [60]. Typical handset locations with respect to the body were identified and studied in [61] where it is shown that the antenna impedance differs significantly from  $50 \Omega$ , the imaginary part varies more than the real part, and this must be considered when predicting overall transmitter/antenna performance.

The proximity of the body to a transmitting antenna is undesirable for two reasons: 1) the change in resonant frequency causes the antenna to be mismatched, thus power is reflected towards the PA, and 2) power that is transmitted from the antenna is absorbed by the body, thus degrading the radiation pattern, preventing some signal from reaching its destination. As a result of (1) an isolator (or circulator) is often inserted in the transmit path, which has the positive result of protecting the output stage of the PA, but it also has the negative result of introducing loss since all reflected power is dissipated in a resistive termination. This can reduce the overall system efficiency by requiring the PA to transmit even more power in order to maintain power density levels at the receiver. More work in antenna design that directs power away from the body (which is outside the scope of this work) could help with (2), but the rest of this section is concentrated on reducing the wasted power and improving the radiation



Figure 2.10: Sample cell phones operating around  $800\,\mathrm{MHz}$  and  $1.9\,\mathrm{GHz}$  cell uplink frequencies, with coaxial cable and SMA connector attached for antenna measurements. LG VX3200 phone is on the left; Nokia 6010 phone is on the right.

efficiency through impedance matching. The desired results include longer battery life and reduced physical temperature of the handset.

#### 2.3.1 Measuring the effect of near-field loading on cell phone antennas

Characteristics of some typical cell phone antennas were measured and confirmed the results in published literature, while gaining data to guide design and implementation of an adaptive matching network. Two sample phones were used for testing: a Nokia 6010 that operates in the GSM 850 and 1900 bands, and an LG VX3200 that operates in the CDMA 800 and 1900 bands, as well as AMPS 800. The trace was cut at the output of the PA and soldered to a small coaxial cable before the phone was reassembled (Fig. 2.10). Then each phone was measured on an Hewlett Packard 8510C VNA with SOL calibration, and a frequency sweep was recorded with the phone in two locations: in free space, and hand-held next to a human head. As seen in Fig. 2.11, for both phones, the additional capacitive loading shifted the resonant frequency down. A time lapse of antenna impedance was recorded with the Nokia 6010 phone in various locations, including in free space, next to head with hand, in rear jeans pocket while

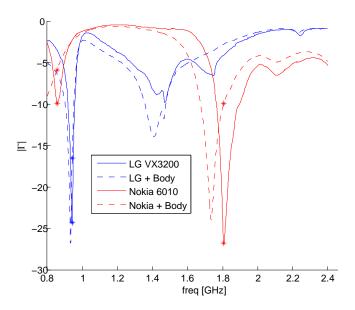


Figure 2.11: When the two cell phones from Fig. 2.10 were placed next to the body, their antenna resonances shifted down in frequency as expected.

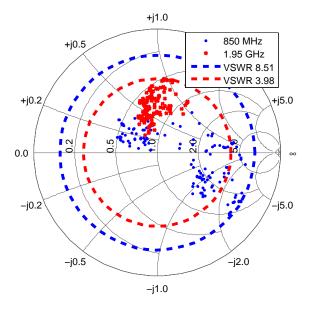


Figure 2.12: Measured antenna impedance of the Nokia 6010 cell phone over time at  $1.95\,\mathrm{GHz}$ . Maximum observed VSWR was 3.98.

sitting and standing, on a metal table, and several other locations in between. Figure 2.12 shows that the maximum measured antenna VSWR at 0.85 GHz is 8.51, and the maximum VSWR at 1.95 GHz is 3.98. The measured phase of the antenna impedance shown in the figure is not certain, as the calibration reference plane for the measurement is at the SMA connector.

Therefore, this gives an indication of what VSWR range an impedance tuner would need to match, and it was decided that a reasonable goal would be VSWR=4 and better.

# Chapter 3

### Impedance Tuner Metrics

The design of an impedance tuner depends on the application of the tuner and specifications for loss, linearity, power handling, impedance coverage and speed of adaptation. An ideal tuner would add no loss and have a tuning range approaching 100%. However, there is always a trade-off between loss and tuning range, and also between power handling and linearity. A universal figure of merit would be useful for comparing impedance tuner implementations, but different applications dictate different sets of tuner requirements. For instance, a lossy tuner with a wide tuning range might be well-suited for an application where minimization of reflected power is of the highest priority (such as in RF ablation, where the load impedance changes drastically), while a tuner with a relatively small tuning range and very low loss might be best suited for a PA where the load impedance is not expected to change much. This chapter explains the parameters that are relevant to impedance tuner design: tuning range, loss, and tuner control.

#### 3.1 Tuning Range

The tuning range of an impedance tuner can be quantified by the area enclosed by the tunable impedances on the Smith chart. An impedance tuner with 100% coverage would have a tuning area of  $\pi$  (the area of the Smith chart). But because it is impossible to match loads with unity reflection coefficients, a coverage area of  $\pi$  is impossible. Figure 3.1 shows a uniform 0.1 gamma grid whose points represent load impedances (at a single frequency) that can be matched by an hypothetical impedance tuner that covers 90% of the Smith chart.

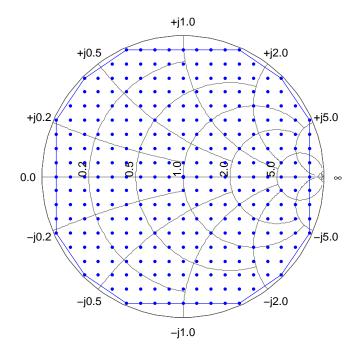


Figure 3.1: Illustration of tuner coverage. If each of the blue points on the Smith chart represent load impedances that can be matched, this tuner would have a coverage area of 90% of the Smith chart.

In addition to general coverage specifications, the density of the points is an important metric, and it is related to the allowable VSWR. Consider a few sparsely distributed load impedances on the Smith chart that can be well matched with a given tuner. Load impedances far away from them will not benefit from any of the tuner states, and so simple coverage area is not enough. To be meaningful, coverage area needs to include an additional metric stating the worst-case quality of match that can be achieved inside the area. A tuner that can present an impedance resulting in VSWR = 4 or better for load impedances covering 50% of the Smith chart might not be as good as a tuner that can present an impedance resulting in VSWR = 1.3 for load impedances that cover just 20% of the Smith chart.

Thus far, bandwidth has not been mentioned. The quarter-wave transformer, which can be thought of as a tuner with zero tuning range, presents an ideal match for only one frequency (and its odd harmonics). Acceptable matching conditions can be seen over a narrow bandwidth, but for a wideband signal, the band edges see a poorly matched load impedance.

VSWR	2	3	4	5	10	15	20	1000
Smith Chart Coverage	11%	25%	36%	44 %	67%	77%	82%	99.6%
Maximum Loss [dB]	4.75	3	2.22	1.75	0.87	0.58	0.44	0.01

Table 3.1: Smith chart coverage as a function of VSWR. A tuner that can match all loads within the VSWR=5 circle has 44% Smith chart coverage. Also shown is the equivalent attenuation that can transform an open or short circuit to the VSWR shown. A tuner with 3dB of loss can transform any impedance to VSWR=3 or less, and can present a conjugate match to impedances having VSWR no greater than 3.

The bandwidth of the quarter-wave match decreases as load impedance mismatch increases. For this work, the signals are assumed to be narrowband unless otherwise stated. Wideband matching and simultaneous matching of multiple frequencies is an even greater complexity that is not addressed in this work because impedance changes with frequency.

#### 3.2 Tuner Loss

In order to match a highly reflective load impedance (a few of them can be seen near the edge of the Smith chart in Fig. 3.1), presenting it with its complex conjugate would maximize power transfer. To create such impedances, a low-loss matching network is necessary. This is most easily explained by stating that reflecting all power would require zero loss. In practice, an impedance tuner that can produce impedances up to VSWR = 40 is considered to be low loss, but loss will go up and Smith chart coverage down as frequency increases. Consider a matched resistive attenuator, terminated with a short or open. If it is a 10 dB attenuator, then it can reflect no more than -20 dB of input power back to the source; that is, it always looks like an impedance very near the center of the Smith chart. If it is a 0.2 dB attenuator, then it can reflect as much as -0.4 dB of input power, corresponding to impedances very near the edge of the Smith chart (VSWR = 40). Table 3.1 lists load VSWR, corresponding tuner coverage area, and maximum loss as discussed here.

In some papers and books [30, 31, 62] loss is defined as:  $1 - |S_{11}|^2 - |S_{21}|^2$  following the simple argument that if the input power was not reflected back into port 1, and the power was

not delivered to port 2, then the rest of the power was "lost" by inserting the device. This is sometimes called Loss Factor [33]. However, it is shown in [34] that this definition is only valid when port 1 is matched to the source. A more appropriate measure of loss is insertion loss, defined for a general unmatched 2-port network as:

$$IL = \frac{P_{DL}}{P_{DS}} = \frac{|S_{21}|^2}{1 - |S_{11}|^2} \tag{3.1}$$

Therefore, mismatch at port 1 is factored out, but mismatch at port 2 negatively affects *IL*. As a matter of definition, port 1 of the impedance tuner is connected to the RFPA, and port 2 is connected to the dynamic load. Since it is the load impedance that is changing, the mismatch at port 2 should be factored out when calculating the insertion loss of a tuner, rather than the mismatch at port 1. In fact, since the RFPA desires to see a matched load, the tuner should be penalized with an increase in loss for not providing the proper impedance to the RFPA. This results in a modified definition of insertion loss for the special case of tuners, referred to in this work as tuner loss:

$$TL = \frac{\left|S_{21}\right|^2}{1 - \left|S_{22}\right|^2} \tag{3.2}$$

which for a reciprocal device ( $S_{21} = S_{12}$ ) would be the same as IL but with ports 1 and 2 reversed. However, an impedance tuner can, and usually will, present a different impedance at each port, and therefore is not reciprocal. Three test cases in Fig. 3.2 can help explain how loss factor, insertion loss and tuner loss differ for some canonical networks:

(A) Consider the example of an ideal transmission line between two 50  $\Omega$  ports with characteristic impedance of 20.7  $\Omega$  that is a quarter-wavelength long. In this case, only half of the power available from port 1 arrives at port 2 - the other half is reflected back into port 1. However, since the transmission line is ideal and therefore lossless, it has zero insertion loss - all power not reflected back to port 1 is delivered to the load  $(P_{DS} = P_{DL})$ . No matter what the port impedances are, all calculations agree that a lossless transmission line has no insertion loss (1 - LF = TL = IL = 1 = 0 dB).

(b) 
$$R = 100 \Omega$$

$$50 \Omega \bigcirc \bigcirc$$

(c) 
$$50 \Omega$$
  $Q = 50 \Omega$   $Q = 75 \Omega$   $Q = 75 \Omega$   $Q = 75 \Omega$ 

Figure 3.2: Canonical 2-port networks used to discuss the differences between loss factor, insertion loss, and tuner loss.

- (B) Consider now the example of a  $100 \,\Omega$  resistor in series between two  $50 \,\Omega$  ports. Basic transmission line equations tell us that twice as much power is dissipated in the resistor as is delivered to port 2, and  $^{1}/_{4}$  of the power is reflected from the network and dissipated in port 1. Therefore, of the power that gets into the network,  $^{2}/_{3}$  of the power is dissipated in the resistor, and  $^{1}/_{3}$  is delivered to port 2. The Loss Factor equation suggests that  $^{1}/_{2}$  of the power is delivered to port 2, while IL from Eq. 3.1 gives  $^{1}/_{3}$  as expected, as does TL from Eq. 3.2.
- (C) As a final example, port 1 impedance is  $50 \Omega$ , and port 2 impedance is  $75 \Omega$ . Alone,  $|S_{21}|^2$  is 0.96 due to the impedance mismatch, but since there is nothing between the ports, there is 0dB of loss. When the  $25 \Omega$  shunt resistor to ground between them is added (as seen in Fig. 3.2c), 1 LF is about  $^2/5$ , IL is  $^1/4$ , and TL is  $^1/3$ . In a tuner, the intent is for the tuner to be matched to its load. The impedance looking back into port 2 is the parallel combination of  $50 \Omega$  and  $25 \Omega$ , which is  $16^2/3 \Omega$ , so it only makes sense for this resistor "tuner" to be best suited for a  $16^2/3 \Omega$  load. In fact, a  $16^2/3 \Omega$  port 2 impedance results in the maximum power transfer into port 2, and  $|S_{21}|^2$  converges to the TL value of  $^1/3$ . Therefore, we have shown by example that TL makes the most sense for a tuner if we assume it will have a matched load at its output in the tuned

condition.

A secondary benefit of the TL definition is that it can be measured easily on a standard VNA. By assuming that port 2 will be matched in the application, the measurement of TL becomes independent of the impedance on port 2 of the VNA, and S-parameters can be measured for each tuner state and used to calculate TL directly, without having to present the ideal impedance for each tuner state to the device under test. This has been shown for a tuner meant for a  $50\,\Omega$  system, but a VNA calibrated for a different characteristic impedance (e.g.  $75\,\Omega$ ) will produce the same measurement for those (e.g.  $75\,\Omega$ ) systems.

#### 3.3 Tuner Control

A continuous tuner is one that consists of a circuit element where reactance (usually capacitance) is a function of a DC voltage. Examples of variable-reactance devices include diodes, transistors, varactors, BST capacitors, and some types of MEMS variable capacitors. The variable capacitance is used to change the characteristic impedance of a transmission line, the effective length of a tuning stub, or the effective value of a lumped component by placing it in series or in parallel with a capacitance or inductance. The analog nature of the device means that very fine control of the capacitance is possible. However, in contemporary systems, the bias voltage is usually produced by some form of DAC, which means that only a discrete number of states exist in practice, even if there are many bits of resolution.

Discrete tuners are built from switches. The switches can be transistors, PIN diodes, or MEMS devices, and they can be connected in series or in parallel. Digitally switched MEMS capacitors are beginning to come to market, notably from WiSpry<sup>1</sup> and Peregrine Semiconductor.<sup>2</sup> Digitally switched capacitors are made up from capacitor banks, for example: four capacitors would be weighted with binary coefficients 1, 2, 4, and 8, resulting in 16 states of capacitance, linearly spaced. An example showing capacitance as a function of tuner state for

<sup>&</sup>lt;sup>1</sup> http://www.wispry.com/

<sup>&</sup>lt;sup>2</sup> http://www.peregrine-semi.com/

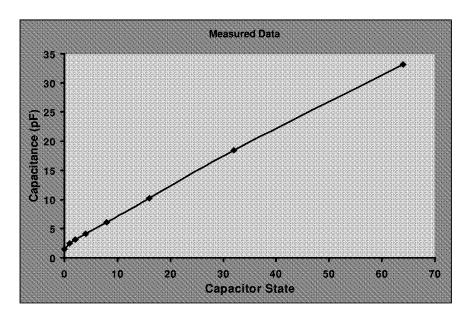


Figure 3.3: Capacitance near 300 MHz as a function of tuner state for a MEMS capacitor from [63].

a digitally variable MEMS capacitor is shown in Fig. 3.3 at a frequency near 300 MHz. It has 64 states, and a maximum 32 pF of capacitance. It works up to 5 GHz, although the maximum capacitance decreases with frequency (12 pF at 1 GHz, and 6 pF at 4 GHz).

Another type of discrete tuner is made from single-pole N-throw switches [64], with each of the N paths between the switches having a different transmission characteristic. As an example, a pair of SP4T switches would have four different paths between them, and could be used to design a phase shifter, with 0°, 45°, 90°, and 135° of relative phase between the paths. Switches are somewhat lossy when implemented with transistors, but the loss can be significantly reduced by using MEMS switches.

The control of an impedance tuner is as important as the tuner design itself, for a nonoptimal tuner state results in performance inferior to that of the circuit without a tuner. For
a static environment in which the load impedance is fixed, a tuner can be set once and left in
that optimal state. For a dynamic environment, a closed-loop tuning system is necessary to
monitor load impedance and set the tuner state accordingly. There are two requirements: the
automatic tuning system must be able to quickly detect a change in load impedance, and also

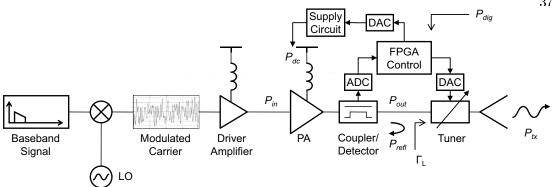


Figure 3.4: Block diagram of an RF front end, where the PA is protected by the tuner minimizing the reflected power seen by the PA. The output of the coupler/detector is converted by an ADC before being read by the FPGA. The FPGA then uses a search algorithm to set the tuner to a state that minimizes the VSWR seen by the PA. The tuner shown here is a continuous type, which means the FPGA needs a DAC to control it.

quickly reduce VSWR to an acceptable level by changing the state of the impedance tuner. How quickly depends on the application, but a GSM timeslot is 576.92  $\mu$ s long leading to the conclusion that the tuning system should be able to detect and correct for a changed load impedance within a few hundred microseconds. RFPAs may also have specifications indicating how long they can withstand various amounts of reflected power before being damaged.

To detect load impedance, a bi-directional coupler is inserted between the RFPA and the antenna (see Fig. 3.4) where it is used to sample the incident and reflected waves which are then measured with detectors. To maintain high efficiency, it is important that the coupler does not add much loss. The difference in magnitude and phase of the two waves indicates the reflection coefficient and load impedance at the output of the tuner, if the tuner and coupler are well-characterized. The control block in the figure is an FGPA that uses an ADC to sample the analog output voltages of the reflection coefficient detector, and either the magnitude, or both the magnitude and phase can be used to implement a tuner control algorithm. The tuner can be placed on either side of the bi-directional coupler, but since this work is more concerned with protecting the PA, it makes more sense to place the tuner after the coupler, so that the coupler more directly monitors the conditions at the output of the amplifier. This approach is valid for detection and minimization of VSWR, but some applications might instead desire to

maximize output power, in which case the gain/phase detector would need to be replaced by absolute power detectors. This work aims to minimize VSWR.

The ratio of incident and reflected wave power indicates the magnitude of the reflection coefficient, or VSWR. Since reflection coefficient and VSWR are defined in terms of voltage, the power ratio read by the control block is actually the square of the reflection coefficient. In any case, the goal of the control block is to minimize the reflection coefficient, through a search algorithm. Search algorithms need to continuously monitor VSWR so that when VSWR degrades beyond a set threshold (application specific), the algorithm can change the tuner state until VSWR improves to an acceptable level, or it may continue changing the tuner state until it finds an optimal state. These two different search algorithm end criteria have different implications. Using the former criterion, a single search process would be quicker, but over time more searches would occur. Using the latter criterion, each search process might take longer to complete, but the tuner state might be acceptable for a longer period of time, resulting in less total searches. Since changing tuner states has an unexpected effect on the transmitted signal, it is usually best to shorten the time taken for each search, and therefore end the search process as soon as an acceptable performance level is reached.

Additionally, it is important to note that transistors often have regions of instability in terms of the impedances presented to their input and output. In such cases, an analysis must be done to ensure that the input impedance of the tuner does not move into these forbidden areas, considering the range of load impedances the tuner will be presented with. When instability is possible, additional safeguards in the algorithm need to be set in place to prevent the tuner from causing the PA to oscillate.

The simplest tuning algorithm would be a brute-force method: search through all tuner states, and when finished, select the best tuner state – the tuner state that results in the lowest VSWR. This simple method has problems: searching through all tuner states takes a long time, but it is compounded by the notion that the load impedance might have changed during the search resulting in the best tuner state being incorrect. A slowly-changing load impedance may

exist in a particular application, but this is not the optimal search algorithm.

The search algorithm given in [65] presents a fuzzy logic approach to automatic tuning control by computing the error signal between desired and real capacitance values. However, it is not shown exactly how this error would be measured electrically. The steepest gradient algorithm is employed by [66] for 150 MHz helical antennas near human phantoms with some success, but in general, the steepest gradient method slows down near the optimum. An improvement is made by [67] to reduce the searching time using an hybrid steepest gradient method. An hybrid genetic tuning algorithm is presented in [68] but for purely theoretical cases, and computation times are hundreds of seconds. Automatic tuning in [69, 70] also takes hundreds of seconds. The quickest tuning algorithm shown in literature is in [71], where usually 10 tuning steps are needed for convergence. The tuning algorithms used in this work will be presented in later chapters, first the local optimizer, which needs a single global optimum to work well, and then a new search algorithm developed in this work. The local optimizer is shown to tune in up to 25 steps, and the new algorithm is much faster.

In summary, this chapter explains tuning range, tuner loss, and the basic needs for closed-loop tuner control, and lays a foundation for the comparison and characterization of tuners in later chapters.

### Chapter 4

# Continuous Tuner Design

The goal of the continuous tuner designs in this chapter is to come up with a simple, low-cost tuner to transform impedances of cell-phone antennas to  $50 \Omega$ . Sample cell-phone antenna impedances were measured and results presented in Ch. 2 and [72]; those impedances are used to guide the implementation of this tuner. Lastly, an investigation into the feasibility of tuning using varactors in the TriQuint TQPED GaAs process is shown.

### 4.1 Hybrid Tuner Design

It can be inferred from Table 2.1 that by combining types 1 and 3 a CLC  $\pi$ -network can be used to match loads on the entire Smith chart using a variable inductor and two variable capacitors. In lieu of a variable inductor, which is difficult to obtain at microwave frequencies with low loss, a quarter-wave section of transmission line can be used as a j-inverter to transform a variable capacitance into what behaves like a variable inductance (Fig. 4.1). A simple initial tuner design started out as a CLC tuner designed to transform  $100 \Omega$  into  $50 \Omega$  using three diodes, and was extended by adding an additional quarter-wave section and diode. The tuner

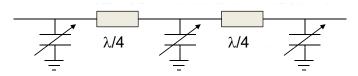


Figure 4.1: A CLC  $\pi$ -network can be realized with three variable capacitors separated by quarterwave sections of transmission line. The transmission line segments move the capacitor up into the inductive top half of the Smith chart.

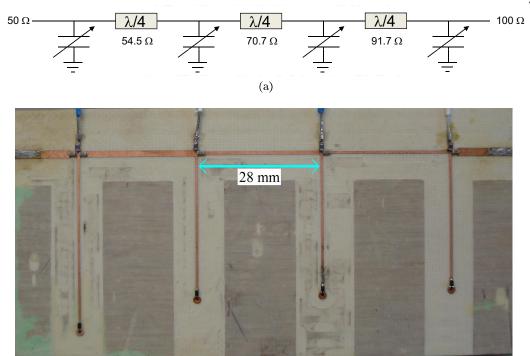


Figure 4.2: (a) Schematic and (b) photograph of variable binomial multisection transformer between  $50\,\Omega$  and  $100\,\Omega$ . The binomial multisection was chosen because it has maximum flatness in band, which loosely translates into a larger tuning range. The tuner is too large to be practical.

(b)

was essentially a binomial multisection transformer (shown in Fig. 4.2), but the size was too large to be practical – the length approaching a full guided wavelength. A different tuner design and topology was required that would be much smaller and would match to antennas that are nominally  $50\,\Omega$ .

A simple tuner topology with reasonable tuning range is the double-stub tuner (see Fig. 4.3b). Using a double-stub tuner, where all the transmission lines are of characteristic impedance  $Z_0$ , there is a range of impedances that cannot be matched. As seen in Fig. 4.3a, this range falls within a circular region tangent the edge of the Smith chart, whose radius depends on the distance d between the stubs. The shorter the distance, the larger the tuning range, but the more sensitive the tuner becomes to imperfections both in fabrication and operation. Typically, d is set to  $\lambda_g/8$  but for this design it was shortened to  $\lambda_g/10$  to increase the tuning range without sacrificing much in sensitivity.

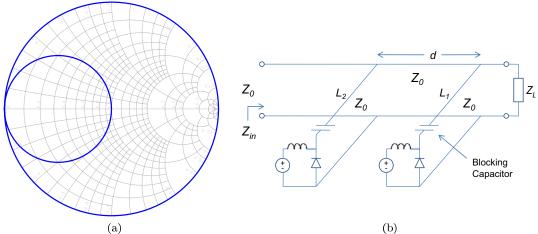


Figure 4.3: Double-stub tuner. (a) Smith chart coverage if the distance d between the stubs is set to  $\lambda_g/4$  and the stub lengths are swept from 0-180 degrees. The area inside the inner circle cannot be matched; therefore, the maximum coverage area for a double-stub tuner with  $d = \lambda_g/4$  is  $3\pi/4$ . (b) Circuit diagram of double-stub tuner with a varactor diode at the end of the two shunt stubs.

In mobile handsets, antenna impedances are designed to be 50  $\Omega$  under nominal conditions, but they vary with near-field loading. Based on previous cell phone antenna measurements [72] this antenna VSWR is expected to be no higher than 4:1 at 1.95 GHz (see Fig. 2.12). This tuner should match loads centered around 50  $\Omega$  with a resulting VSWR of 1.5:1 or better. With d chosen, from standard transmission line equations nominal stub capacitances can be calculated, which are equal for  $Z_L = Z_0$ . Abbreviating with  $t = \tan(\beta d)$ , stub susceptances  $B_1$  and  $B_2$  are as follows, where stub 1 is closest to the load:

$$B_1 = -B_L + \frac{Y_0 \pm \sqrt{G_L Y_0 (1 + t^2) - G_L^2 t^2}}{t} \quad B_2 = \frac{G_L Y_0 \pm Y_0 \sqrt{G_L Y_0 (1 + t^2) - G_L^2 t^2}}{G_L t}$$

Since the tuner is matching to  $50 \Omega$ ,  $G_L = Y_0$  and  $B_1$  and  $B_2$  become:

$$\begin{split} B_1 &= \frac{Y_0 \pm \sqrt{Y_0^2 + Y_0^2 t^2 - Y_0^2 t^2}}{t} \quad B_2 &= \frac{Y_0^2 \pm Y_0 \sqrt{Y_0^2 + Y_0^2 t^2 - Y_0^2 t^2}}{Y_0 t} \\ B_1 &= \frac{Y_0 \pm Y_0}{t} &= \frac{2}{Z_0 t} \qquad \qquad B_2 &= \frac{Y_0^2 \pm Y_0^2}{Y_0 t} = \frac{2}{Z_0 t} \end{split}$$

And since  $Z = \frac{1}{j\omega C}$ ,  $C = \frac{B}{2\pi f}$ ,

$$C = \frac{1}{Z_0 \pi f \cdot \tan(\beta d)} \tag{4.1}$$

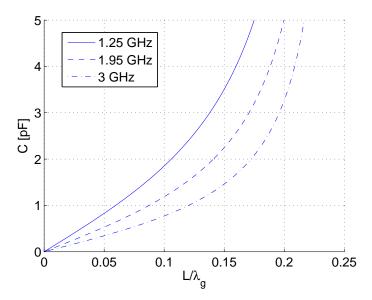


Figure 4.4: Equivalent capacitance of a  $50\,\Omega$  open microstrip stub vs. its electrical length. For stubs shorter than a quarter-wavelength, the stubs are capacitive.

The important result is that the nominal stub susceptances are the same for this special case. When  $f = 1.95\,\text{GHz}$  and  $d = \lambda_g/10$ , the required shunt capacitance for each stub is roughly 4.5 pF. There are multiple solutions for the stub lengths, and the shortest one is chosen for larger bandwidth and smaller physical size. The relationship between open-circuited stub length L and capacitance C (without any substrate-dependent open-circuit correction) is given by:

$$\frac{L}{\lambda_g} = \frac{1}{2\pi} \arctan(2\pi f \cdot C \cdot Z_0) \tag{4.2}$$

as depicted in Fig. 4.4. Given this relationship between capacitance and length, it is apparent that a stub can be completely replaced with a capacitor to save space if a small amount of additional loss (due to the parasitics of the capacitor) is acceptable. With a varactor-loaded stub, increasing the reverse bias voltage leads to a decrease in the capacitance which effectively shortens the stub length and changes the effective impedance of the tuner transmission line segment.

With a solid understanding of the double-stub tuner, a suitable varactor diode was selected. Several packaged varactors were measured in a microstrip one port circuit using an HP

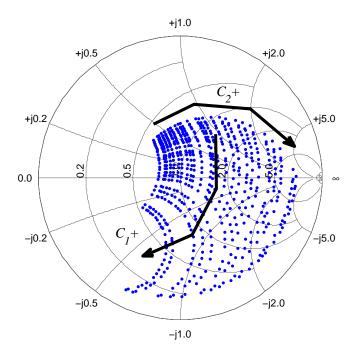


Figure 4.5: Simulated  $S_{22}$  for the continuous tuner with block diagram shown in Fig. 4.3b. Each stub was swept between 0 and 6V in  $0.25\mathrm{V}$  steps. The trend arrows indicate which output impedances correspond to the higher stub capacitance values.

8510C VNA with a TRL calibration and multiple reverse bias voltages. The inductance of the ground via at the anode is included in the measured diode model because it is the configuration in which the diode was to be used. The Skyworks<sup>1</sup> 1405 abrupt-junction tuning varactor was chosen because of its high Q, large tuning ratio, and appropriately low capacitance for this frequency.

Starting with the measurement-based varactor model, the double-stub tuner circuit was simulated in AWR Microwave Office, showing the tuning range in Fig. 4.5. The stub capacitance values can be adjusted in design to shift the coverage area on the Smith chart. Decreasing the effective length of stub 1 would shift the constellation higher, and increasing the effective length would shift the constellation lower and give it a longer "tail" towards the  $0 \Omega$  point. For this simulation, each tuner stub was swept across 25 bias points, from 0 to 6 V, which results in the 625 simulated points representing  $S_{22}$ . Since this is a continuous tuner, very fine control of the tuner state is possible with very fine control of the bias voltages. Therefore, everything within

<sup>&</sup>lt;sup>1</sup> http://www.skyworksinc.com

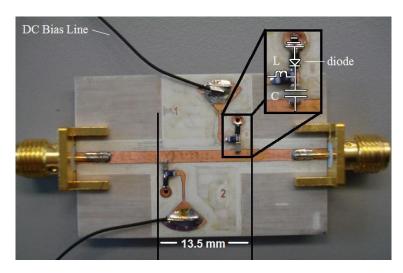


Figure 4.6: Photo of the tuner circuit  $(13.5\,\mathrm{mm}\times23.5\,\mathrm{mm})$  fabricated on  $32\,\mathrm{mil}$  Rogers RO4003 substrate.

the perimeter of the constellation could be tuned with infinite bias voltage resolution. However, the practical tuning range is larger than the Smith chart area covered by  $S_{22}$  because the points represent only those loads which can be perfectly matched for maximum power transfer. For example, if a VSWR of 3:1 is acceptable for the system, the tuning range becomes bigger than the area indicated by  $S_{22}$ .

#### 4.2 Hybrid Tuner Results

The Skyworks 1405 abrupt junction varactors were placed on  $32 \,\mathrm{mil}\ \mathrm{Rogers^2}\ \mathrm{RO4003}$  substrate, with  $\epsilon_r = 3.38$ , as depicted in Fig. 4.6. The bias for each stub consists of a surface mount, 0603-sized RF choke inductor in the DC path, and a surface mount, 0603-sized DC blocking capacitor in the RF path of the stub. The DC block performs a second important function - its capacitance also makes up the proper electrical length of the stub by combining with the varactor in series. Therefore, the final electrical length of the stub is constrained not only by the limited selection of suitable varactors, but also by the available values of capacitors and the component tolerances of each.

The final physical size of the tuner is limited by the distance between the stubs, and in

 $<sup>^2</sup>$  http://www.rogerscorp.com

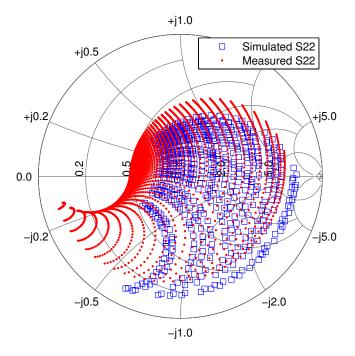


Figure 4.7: Simulated and measured tuner output impedance at  $1.95\,\mathrm{GHz}$  as the reverse bias voltages are individually varied from 0 to  $6\,\mathrm{V}$ .

total the length of the tuner is only 13.5 mm. This tuner implementation is 23.5 mm in width but could easily be halved by integrating the bias lines into the final production design and placing both stubs on the same side. The symmetric layout of the bias lines in this implementation was chosen specifically for simplifying assembly and measurement. Generally, a microstrip double-stub tuner is not the best choice for minimizing the size of the tuner, but it is relatively low loss and requires few components.

A TRL calibration was used to remove the effects of the SMA-microstrip launches, and set the reference plane to the edge of the tuner as simulated. The reference planes are shown in Fig. 4.6. The measured S-parameters with bias voltages swept in  $0.1\,\mathrm{V}$  increments are shown with the simulated points swept in  $0.25\,\mathrm{V}$  increments in Fig. 4.7. Bias voltages were swept from  $0\,\mathrm{V}$  to  $6\,\mathrm{V}$  in expectation of being integrated into a  $5\,\mathrm{V}$  system, but the varactors are designed to handle up to  $30\,\mathrm{V}$  of bias which would further decrease the stub capacitances. Good agreement is shown between simulation and measurement. It can be seen that the capacitance of stub 1 ended up being higher than anticipated in simulation, as indicated by the "tail" on the bottom of

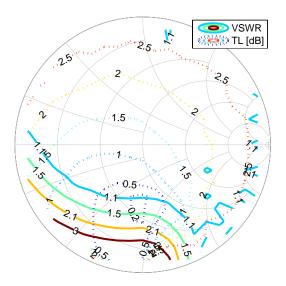


Figure 4.8: Measured tuner VSWR and TL at 1.95 GHz. While nearly the entire Smith chart can be reduced to VSWR of 3 or better, the tuner loss can be as high as 3 dB. Therefore, this tuner is best suited to match low impedances that are capacitive.

the constellation. This is largely because the simulation used two different blocking capacitors, while the actual fabricated tuner used identical components on each stub.

Figure 4.8 shows TL and best possible VSWR performance of this tuner, when loads of up to VSWR = 36 are presented at port 2. One can see that TL increases in this tuner for inductive and lower impedances. VSWR < 1.1 for a wide range of loads, and tuning area is 86% with VSWR of 3 or better, calculated from the measured S-parameters and simulated load impedances:

$$VSWR = \frac{1 + \left| \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right|}{1 - \left| \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right|}$$
(4.3)

where  $\Gamma_L = (Z_L - Z_0)/(Z_L + Z_0)$ . For a 50  $\Omega$  PA connected through an isolator to a load impedance of  $10 - j20 \Omega$ , 50% of the output power would be reflected and dissipated in the isolator. However, replacing the isolator with the tuner results in only about 12% of the transmit power lost (shown in Fig. 4.8 as  $VSWR \simeq 2$  and  $TL \simeq 0.6 \,\mathrm{dB}$ ).

The adaptive impedance tuning controller described below was designed with the goal of minimizing VSWR, even though other goals could also be set; for instance, maximizing output

power. The feedback path in this implementation is through a gain detector connected to a bi-directional coupler, which senses the relative magnitude of the incident and reflected wave powers at the output of the PA. If maximum output power were the goal, a way of measuring absolute power to the antenna would be needed.

What is a tuner state? With an arbitrary number of control inputs to a tuner, and an arbitrarily fine resolution of analog control voltages, the number of tuner states by this definition is impractically large, making the implementation of tuning algorithms entirely complex. In order to simplify the problem, consider a set of load impedances on the Smith chart, a twodimensional space (real and imaginary, or magnitude and phase). This set could cover the entire Smith chart, or just a subset where the actual load impedances are expected or known to be (if the antenna is already designed and measured, for instance). For each load impedance in the constellation (examples can be seen in Fig. 4.9), assume it is already known how to best set the tuner for best performance with that load impedance. With extensive characterization and measurement of the impedance tuner, the simple tuning algorithm need only to know the list of characterized load impedances, and then it can use a look-up table to set the tuner to the best impedance state. Thus, each available tuner state is defined by the load impedance it performs best with; therefore, if the system performance has been maximized by the tuning algorithm, knowing the tuner state implies knowledge of the load impedance, and visa-versa. From this perspective, the search space will always be in two dimensions, no matter how complex the physical tuner control is.

As mentioned in Ch. 3, a simple tuning algorithm could test all possible tuner states and then choose the state that results in the best detected performance. Simple brute force searching is too slow to be effective, and the search can be sped up considerably by looking for trends. Instead of searching all of the tuner states for the best performance, an improved algorithm can simply search adjacent tuner states looking for better performance, if the tuner states are all well characterized. The algorithm can then move through adjacent tuner states in the direction of better performance. When better performance is no longer found in adjacent tuner states,



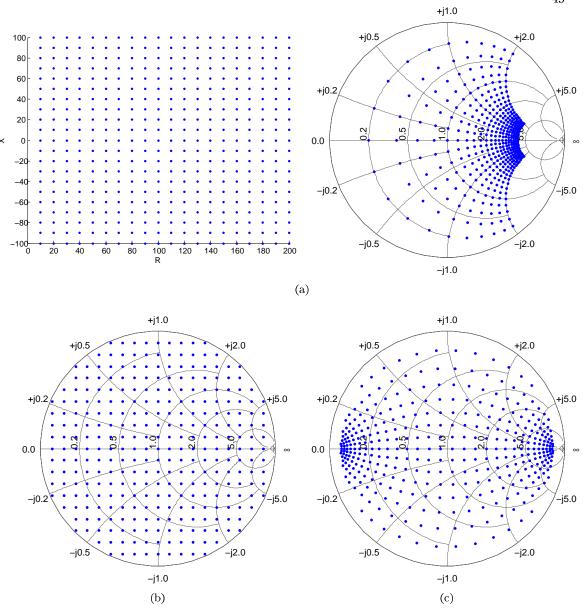


Figure 4.9: Possible impedance constellations used in characterizing impedance tuners. Using a look-up table, a tuner with any number of inputs can be reduced to a two-dimensional impedance space. Shown are: (a) grid spacing of  $10\,\Omega$ , (b) grid spacing of  $0.1\,\Gamma$  (relative to  $50\,\Omega$ ), and (c) relative spacing of  $0.1\,\Gamma$  (between each point).

the best state has been found. This algorithm is as follows:

- (1) Initialization: assume the load impedance is  $50\,\Omega$  and set the tuner to the state that is known to work best for  $50\,\Omega$  (called the  $50\,\Omega$  state).
- (2) Continuously measure VSWR until it is at an unacceptable level.

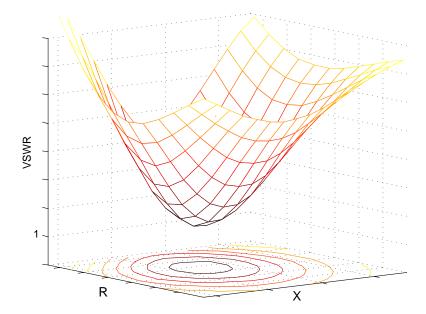


Figure 4.10: The search space must have a global minimum in order for the tuning algorithm to find it. For a given load impedance, there should be just one solution for best system performance.

- (3) Measure VSWR in nearby tuner states (e.g.  $48 \Omega$ ,  $52 \Omega$ ,  $50 + j5 \Omega$ , and  $50 j5 \Omega$  might be the nearby tuner states for a chosen impedance constellation).
- (4) Choose the nearby tuner state with the best VSWR, and assume it to be the load impedance.
- (5) Go back to step 2.

This is the local optimizer method, and it requires the search area to be smooth, with a single global minimum. Figure 4.10 illustrates VSWR as a function of load impedance with a global minimum and no local minima to help illustrate how this searching algorithm could find the best tuner state and therefore calculate the load impedance. Antenna tracking systems that use the conical scanning approach [73] are based on the same principle, and are successful because of the smooth antenna radiation patterns of the main beam. Side-lobes present challenges in these applications, as they are a local gain maximum. Similarly, local VSWR minima in the impedance space would necessitate a more complex search algorithm. The local optimizer method is used here and shown to have acceptable results later in this section.

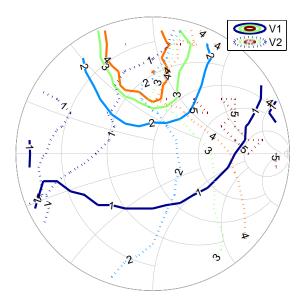


Figure 4.11: Measured varactor bias voltages V1 and V2 for the best match to a given load impedance at  $1.95\,\mathrm{GHz}$ 

The impedance constellation chosen for tuner characterization is seen in Fig. 4.9b. The characterization of the tuner system was performed and the varactor bias voltages were determined by connecting the tuner and supporting circuitry to these known loads and searching for the tuner state that resulted in the least reflected power. Because of limitations in equipment, the load impedances where VSWR was greater than 36 were limited to 36, affecting only a handful of the outermost points (worst case intended VSWR was 81). The resulting look-up table of voltages, indexed by load impedance and represented in Fig. 4.11, is loaded into the FPGA. This process could also be performed in simulation, if the full S-parameters are measured for the tuner across all control voltages; but, the tuner loss is a function of standing wave and the currents on each stub, which are not properly accounted for in S-parameters that are taken with a  $50\,\Omega$  load impedance at port 2.

Referring to Fig. 3.4, the PA used in this experiment is an Avago WS2512 with up to  $27 \,\mathrm{dB}$  of gain and  $P_{OutMax} = 28 \,\mathrm{dBm}$  between 1.92 and 1.98 GHz. The AVX CP0402P1950BN surface mount 15 dB bi-directional coupler has  $27 \,\mathrm{dB}$  of directivity, a  $20 \,\mathrm{dB}$  input match, and  $0.35 \,\mathrm{dB}$  of insertion loss. The Texas Instruments THS1030 ADC has 10-bits of resolution and runs as fast as

30 MSPS. The FPGA is a Xilinx Virtex-4 XC4VLX25, which samples the incident and reflected power from the Analog Devices AD8302 gain detector through the ADCs, and outputs a square wave with adjustable duty cycle into a filter to produce the analog tuner control voltages. The variable load used for testing is a mechanical single-slug tuner from Focus Microwaves (model 1816). The digitized gain detector output is used by two functional blocks: the tuner algorithm, and the PA bias control.

It is important that the bi-directional coupler chosen has high directivity, since directivity is the limiting factor in measuring very small reflection coefficients. The power at the isolated port of a bi-directional coupler is the vector sum of the incident power times isolation, and the reflected power times coupling. Therefore, when the magnitude of load reflection coefficient is on the order of the magnitude of the directivity, the magnitude of the reflection coefficient as calculated by comparing the quantities at the two ports of the coupler could be off by 100% (depending on the phase). For the 27dB of directivity in the coupler used, load reflection coefficients worse than -17dB in magnitude are easily determined, as the reflected power arriving at the coupler's isolated port is at least a factor of 10 greater than the amount of incident power arriving at that same port.

Initially, the tuner state is set assuming a  $50 \Omega$  load. Then the tuner voltages are set for the 8 adjacent tuner states and the FPGA checks to see if VSWR has decreased for any of them. If improvement is found, the system then assumes the new load impedance tuner state and continues searching adjacent tuner states until the state of minimum reflection is found. The algorithm quietly monitors VSWR until a predetermined level of degradation is detected in the match, at which point the control system resumes the search. A measurement of tuning system convergence is shown in Fig. 4.12 in which the load changes from  $50 \Omega$  to  $150 - j50 \Omega$  at step 0 and the closed-loop tuning system completes the search at step 37. The time between each step was 100 ms, limited by the repeat rate of the FPGA logic, which was not optimized. This version of the search algorithm was looking for the best possible state; thus, after it found an acceptable tuner state, it searched 8 adjacent states to confirm the result, and this explains

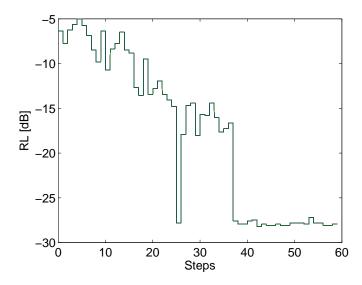


Figure 4.12: Measured adaptive tuner return loss convergence when the load changes from 50  $\Omega$  to  $150-j50\,\Omega$ . Each step is  $100\,\mathrm{ms}$ .

why there is a deep notch at step 25 before the search completes. As mentioned, the algorithm could be designed to stop searching upon finding a tuner state that meets given requirements.

### 4.3 MMIC Analog Design

TriQuint Semiconductor has offered foundry services to the university in which some analog tuner circuits have been designed. In initial designs of tunable circuits in their TQPED GaAs process, there were no varactors in the design kit, so a switched delay line was designed and measured, which is a topic of Ch. 5. The transistor in the design kit was also investigated for use as a varactor, but the simulations were not promising for use in impedance tuning circuits. Later, TriQuint added a varactor model into the design kit, and the varactor was used for a couple of exploratory designs: a tunable lumped LC transmission line (Fig. 4.13), and an amplifier with a tunable input and output match (Fig. 4.15). Varactors were placed along side common-gate transistors in the process for comparison, and it was determined that their functionality as varactors is better than the transistors, but not by much. More time needs to be spent in design and measurement of MMICs with varactors in this process for evaluation, as they are new to the process.

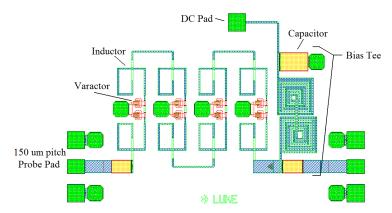


Figure 4.13: Tunable lumped LC transmission line made in TriQuint's GaAs MMIC process. There are 4 copies of a tunable cell, and each cell is an LCL T-network where the C is made up from a pair of varactors. DC bias is on the right.

The lumped LC line in Fig. 4.13 consists of four instances of a tunable transmission line cell. Each cell is an LCL T-network where the C consists of a pair of varactors. On the right is a bias tee, and there are DC blocking capacitors and 150 um probe pad launches on both ends. The varactors are controlled with a DC bias from 0-3.3 V. The idea is to change the characteristic impedance of the line, but without variable inductors, there is no way to keep  $Z_0$  constant. The line was designed in simulation such that  $S_{22}$  (in blue, Fig. 4.14) would fall approximately on the real axis of the Smith chart.

In addition to the lumped line, a tunable amplifier is shown in Fig. 4.15 for operation up to 5 GHz. Bias tees are connected to both the gate and drain of the transistor, followed by input and output matching circuits consisting of spiral inductors and varactors. The varactors in the matching circuits allow for a small amount of adjustment to the amplifier for both the case of a non-ideal load impedance, and to allow for inaccuracies in the simulation. The bias for the matching circuits is separate from the bias for the transistor operation. Simulated results of the output impedance area is shown in Fig. 4.16. Input match (not pictured) is better than -23 dB at 5 GHz for all states, but gain varies between 2.44 and 10 dB (see Fig. 4.17).

This chapter discusses the designs of several analog impedance tuners, implemented with different tuning devices: a hybrid tuner based on varactor diodes, and a monolithic microwave

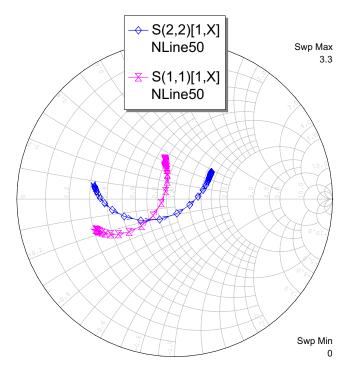


Figure 4.14: Simulated tuning range of the lumped LC transmission line. The line was designed such that with port 1 terminated in  $50 \Omega$ , the  $S_{22}$  curve would fall approximately on the real axis.

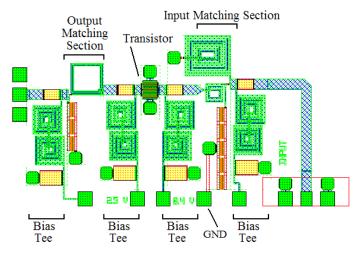


Figure 4.15: A  $5\,\mathrm{GHz}$  amplifier with  $10\,\mathrm{dB}$  of gain was made in the TriQuint GaAs process. The input and output matching circuits consist of varactors instead of capacitors, which allows for some adjustment.

integrated circuit (MMIC) tuner. In addition, measurements are presented for the varactor tuner following the figures of merit described in the previous chapter. The local optimizer

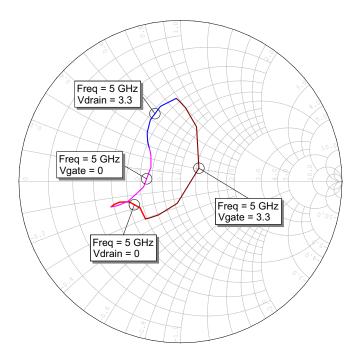


Figure 4.16: The output impedance of the amplifier at 5 GHz can fall anywhere within the perimeter shown by adjusting the bias of either the drain or gate match between 0-3.3 V.

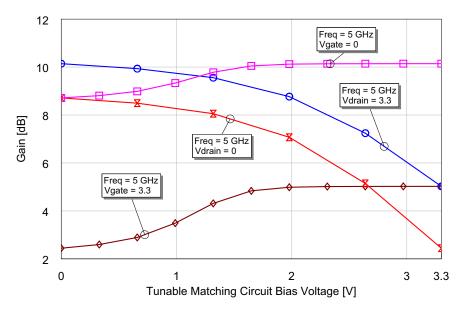


Figure 4.17: Gain at  $5\,\mathrm{GHz}$  with tunable input and output matching circuits ranges from  $2.44-10\,\mathrm{dB}$ .

tuning algorithm is used to demonstrate the closed-loop tuning system. Some results of this chapter have been published in [38].

## Chapter 5

# Discrete Tuner Design

This chapter presents results on tuners with discrete control, including a MMIC pHEMT-switched delay line, a MEMS-switched capacitor tuner, and a MMIC pHEMT-switched capacitor tuner. The tuners are integrated in a closed-loop system which includes a commercial amplifier and self-assessment circuit in the RF path.

#### 5.1 Switching Element

As discussed in Ch. 3, discrete tuners are implemented using one or many switching elements that change the reactance or phase of a circuit. The switches can be transistors, PIN diodes, or MEMS devices, and they can be in various series or parallel configurations; some examples of which are shown in Fig. 5.1. Switches in [27, 28] are used to short across inductors

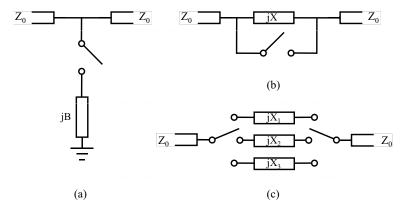


Figure 5.1: Example discrete tuner circuits (a) switch toggles shunt susceptance, (b) switch toggles series reactance, (c) switches used to select different reactance or phase.

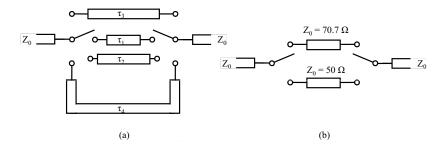


Figure 5.2: Switched lines for (a) changing phase, and (b) changing characteristic impedance.

as in Fig. 5.1b, effectively removing them from the circuit, but usually switches are used to add or remove capacitance or phase as in Fig. 5.1a, c. The PIN diode is chosen for handling high power and switching at high speed; as MEMS switches come to market they will be chosen for low insertion loss and high linearity. Transistors as switches are in widespread usage because they are readily available, and perform well enough for many applications in terms of speed, power handling, and linearity.

### 5.2 MMIC Switched Delay Line

A switchable delay line can perform impedance tuning by changing the phase between its source and load impedances (Fig. 5.2a). Depending on the characteristic impedance of the transmission line, and the length of line used, a nominally  $50 \Omega$  line could have a matching network switched to handle loads other than  $50 \Omega$ . For example, switching in a quarter-wave section of  $70.7 \Omega$  line would allow for a  $100 \Omega$  load attached to a  $50 \Omega$  system (Fig. 5.2b).

The goal for the switched delay line design in this work is to be able to shift in and out an extra 90° of phase in a  $50\,\Omega$  system at the chosen center frequency of 1.95 GHz. The physical size limitations of the reticle in the TriQuint process (5 mm by 10 mm) does not allow a straight section of line; therefore, the line could be meandered, or lumped elements could be used to create the phase delay. Both solutions were included in the switched delay line circuit design for comparison, along with a straight through section of line for comparison. The three paths resulted in the design of a reflective SP3T switch made from three pHEMTs.

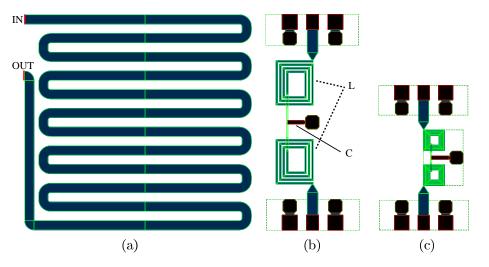


Figure 5.3: Layout of quarter-wave sections of transmission line at 1.95 GHz in the TriQuint TQPED GaAs MMIC process, (a) meandering transmission line, (b) lumped elements (large) with probe pads, (c) lumped elements (compact) with probe pads. The width of the 50  $\Omega$  line is 73  $\mu$ m, the square spiral inductors are about 3.6 nH each, and the capacitors are 1.5 pF.

The quarter wave sections shown in Fig. 5.3 were each designed to have an additional 90° of phase shift relative to the short through-path so that switching the section in or out would result in a 90° phase change. The two lumped-element versions of the phase delay circuit were also placed separately in the MMIC to allow for individual testing, and their results are shown in Figs. 5.4 and 5.5. The two versions were designed to investigate the trade-off between size and loss. The larger of the two layouts resulted in measured  $S_{21}$  of about 0.1 dB better than the smaller version, as expected. For the large version, the phase ended up 9° shorter than intended (after subtracting an extra 3° of TRL standard that can be seen in the simulation results), and for the compact version, the phase was 4° shorter than intended. In both cases, the circuit was well matched to  $50 \Omega$ . Careful observation of the measurements reveals that the matching and phase would have been closer to designed values for slightly higher frequencies, leading to the conclusion that the simulation predicts the frequency response 15% lower than in reality.

The switched delay line design consists of six transistors: three on each end to control the three different paths. There are three DC pads that control the transistors, which are pulled down to ground through a large resistance to maintain the off state of each path. When a single

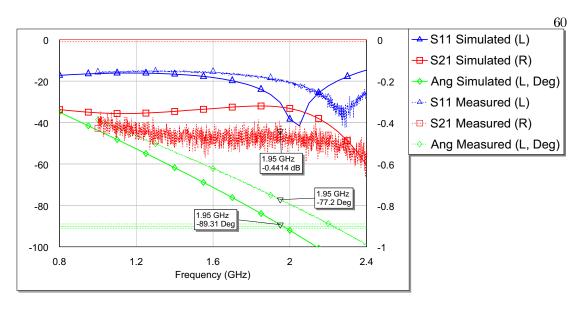


Figure 5.4: Simulated and measured data for large (Fig. 5.3b) lumped element 90° circuit.  $S_{11}$  and phase are on the left axis,  $S_{21}$  is on the right.

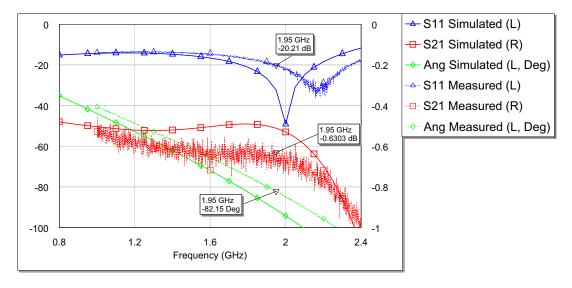


Figure 5.5: Simulated and measured data for compact (Fig. 5.3c) lumped element 90° circuit.  $S_{11}$  and phase are on the left axis,  $S_{21}$  is on the right.

DC probe at 5V is applied to one of the pads, a transistor at each end of the circuit turns on and enables RF to flow through one of the three paths, each with different electrical length. The layout of this MMIC can be seen in Fig. 5.6.

Figure 5.7 shows the comparison of simulated and measured results for the "off" state. Nearly all of the power is reflected, and the transmission coefficient is -18dB. When the center

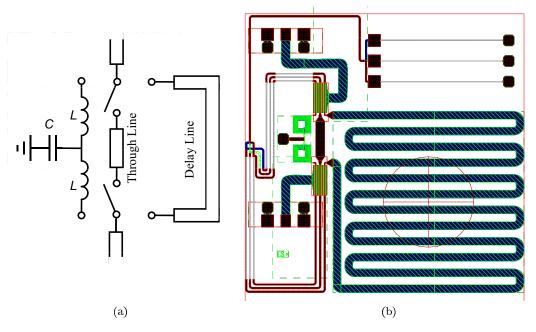


Figure 5.6: (a) Schematic and (b) layout of MMIC switched delay line. The size of the layout is 2.3 mm square. Each SP3T switch is comprised of 3 transistors, and from left to right, the paths are: compact lumped 90, through line, and meandered line.

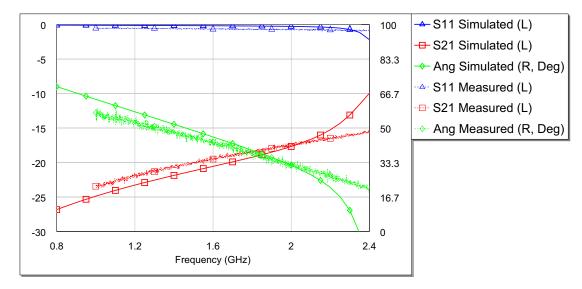


Figure 5.7: Simulated and measured S-parameters for the "off" state of the switched phase delay circuit. Transmission at 1.95 GHz is -18 dB.  $S_{11}$  and  $S_{21}$  are on the left axis, phase is on the right.

path is enabled (see Fig. 5.8), transmission increases to -5 dB, much worse than the -1 dB that was simulated. The input is also not well-matched, 2.5 dB worse than predicted. The measured

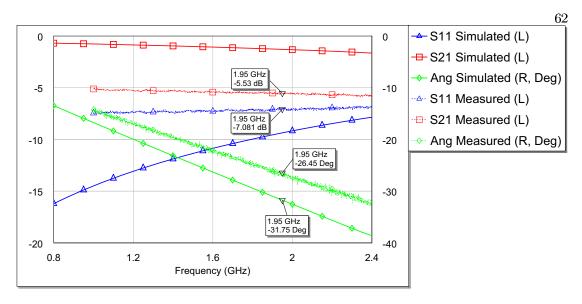


Figure 5.8: Simulated and measured S-parameters for the "through" state of the switched phase delay circuit. Transmission is worse than expected at only -5.5 dB.  $S_{11}$  and  $S_{21}$  are on the left axis, phase is on the right.

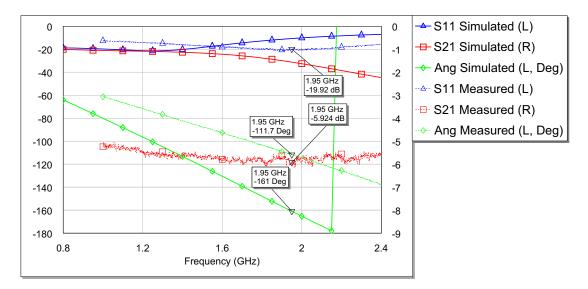


Figure 5.9: Simulated and measured S-parameters for the "meandering line" state of the switched phase delay circuit. Add 26° of phase to the measured data to get the true phase shift of this RF path: 86°.  $S_{11}$  and phase are on the left axis,  $S_{21}$  is on the right.

phase of the "through" state was -26°, which becomes the reference for calculating the length of the quarter-wave lines.

The performance of the "meandering line" path is shown in Fig. 5.9. A 2-D method of moments EM simulation was done from within AWR to account for the the mutual coupling

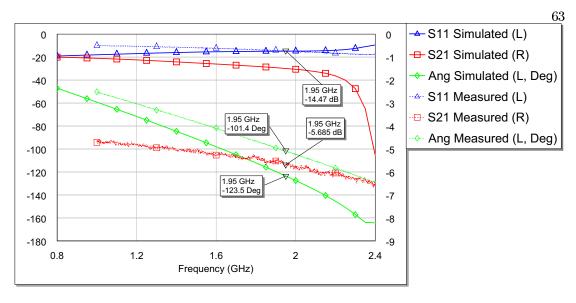


Figure 5.10: The "lumped 90" state of the switched phase delay circuit. Add 26° of phase to the measured data to get the true phase shift of this RF path: 76°.  $S_{11}$  and phase are on the left axis,  $S_{21}$  is on the right.

between the meandering line sections, which indicated the linear simulator was significantly overestimating phase for this layout. Thus the figure shows simulated phase to be high at -161°. However, the phase at 1.95 GHz was measured to be -112°, which is a true phase difference of -86°, only 4° short of the stated goal, as compared to the "through" line. An important point to note is the magnitude -6 dB of transmission coefficient, which is significant compared to the expected -1.5 dB. Just like the through line, there is an extra 4 dB of measured loss that was not expected. Similar performance was obtained from the more compact lumped quarter-wave line branch of the circuit (Fig. 5.10). The match is not as good as the meandering line at only -14.5 dB (instead of -20 dB), but the transmission is about the same as before, -6 dB, again 4 dB worse than expected. After subtracting -26° of the "through" path, the true measured phase delay in the "lumped 90" path is -76°.

The TOM3 model used in simulations of the transistors underestimates series resistance, which is revealed in these results. The extra mismatch at the switches was also not foreseen. Recall from the measured results that the input match for each of the quarter-wave paths is much better than it is for the "through" path, and this is because the reflected waves from each

of the identical SP3T switches cancel out at the input port due to the 90° of phase between them. If  $S_{11}$  was plotted across frequency, it would have a large standing wave, with nulls at every frequency where the delay is an odd multiple of  $^{\lambda}/_{4}$ . With lower switch mismatch, the standing wave would become smaller. This work concludes that using these transistors in the transmission path leads to significant losses. At nearly -3 dB per switch, the transmission coefficient is too low for practical use, and needs to be improved. A commercial SP3T GaAs pHEMT transistor switch from Skyworks indicates loss can be better than -1.2 dB for a pair of switches.

#### 5.3 MEMS Tuner Design

MEMS switches claim very low loss performance, and are suitable to be placed in the transmission path, as well as outside the direct path. An example is seen in [74] where loss for a MEMS DPDT switch at 12 GHz is 0.2 dB. Currently, the commercial availability of MEMS switches is very limited. A switched-capacitor double-stub tuner was designed using a Radant RMSW100 MEMS switch, a reflective SPST switch with advertised typical insertion loss of 0.16 dB at 2.4 GHz. The layout can be seen in Fig. 5.11, where the black outlines are microstrip, the blue squares are for the MEMS switches, and the red outlines are the plate capacitors implemented in microstrip. The design goal was for a very small tuner with low loss and large coverage. The MEMS switch performance was included in simulation using data files (generated from measurement) provided by Radant.

Each stub in this double-stub tuner was individually optimized for a range of capacitance values that maximized the Smith chart coverage and distribution. With such low-loss switches, a large coverage area is possible, along with a large tuning range for each stub. The simulated tuning range for each stub is 10:1 and the increase in capacitance for each increase in tuning state is very uniform, as is visible from Fig. 5.12. The uniform increase in capacitance with tuning state results in a relatively uniform distribution of impedance states on the Smith chart

<sup>&</sup>lt;sup>1</sup> http://www.radantmems.com

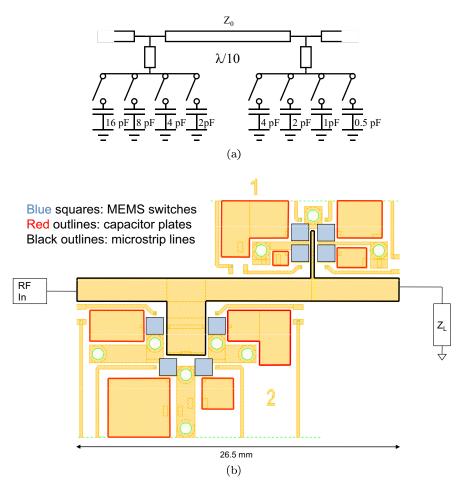


Figure 5.11: (a) Schematic and (b) compact layout of a double-stub tuner using MEMS-switched plate capacitors implemented in microstrip.

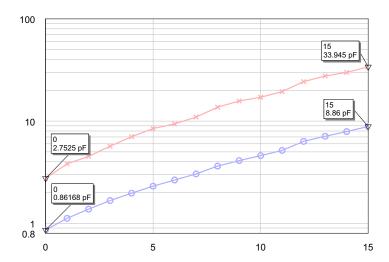


Figure 5.12: Simulated stub capacitance [pF] as a function of tuner state. Each stub has a theoretical tuning range of greater than 10:1

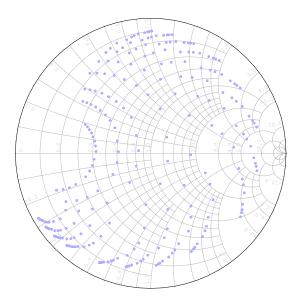


Figure 5.13: Simulated  $S_{22}$  of MEMS tuner design in all 256 states covers a large majority of the Smith chart.

(Fig. 5.13).  $S_{22}$  of all 256 possible states are shown, but the simulated results here do not take into account the EM coupling due to the close proximity of the plates, bias lines, and microstrip structures.

Before fabrication, there were two things left to explore - the actual performance of the MEMS switch, and the coupling in the circuit due to the dense layout. A test fixture (Fig. 5.14) and TRL kit were fabricated for the Radant MEMS switch, as well as a 100 V step-up power supply with a 3.3 V control. The control voltage was chosen to be compatible with the output voltage capability of the FPGA, which was intended to control the switches. Unfortunately, the MEMS switch did not function as advertised. 5 out of 5 identical switches were tested and all had a gate-to-drain resistance of only a few hundred  $k\Omega$  which resulted in a bias current orders of magnitude higher than specified, and a bias voltage lower than 100 V. Even with larger voltages, the switches would remain in the open state. As an emerging technology, no other MEMS devices were acquired nor available from vendors, but the design shows great promise, as MEMS technology and quality is expected to improve as the technology and manufacturing processes mature. At the time of this writing, other groups are having very similar problems



Figure 5.14: (a) Radant MEMS switch mounted and wire-bonded to a microstrip test fixture, and (b) test fixture attached to 100 V step-up power supply.

with a reflective SP4T Radant MEMS switch product. However, integrated tuners fabricated in adademic labs have shown that MEMS switches can be used successfully in tuner design [29].

#### 5.4 MMIC Switched Capacitor Tuner Design

The transistor as a switch has more loss than the MEMS switch, but is still a viable option to design and build a switched-capacitor double-stub tuner, especially since the MEMS switches are not an option at this time. The TriQuint TQPED GaAs process was used to design and implement this tuner, an ideal platform to further reduce the tuner circuit size, and demonstrate the possibility in which the tuner could be integrated into the same process as the RFPA. Like the previously discussed design, this switched-capacitor double-stub tuner consists of four switches on each stub, for a total of 256 tuner states. Each of the capacitor values on each tuner stub were carefully chosen so that the capacitor change was linear and centered around nominal values that resulted in a large tuning range on the Smith chart. The stub capacitances are shown in Fig. 5.15.

Three variations of the tuner design and a TRL kit were laid out on the  $5\times10$  mm reticle, where the capacitance of stub 2  $(C_2)$  was varied  $\pm5\%$ . Two of the three variations of the layout are shown in Fig. 5.16a, where the nominal layout has been overlaid with a picture of

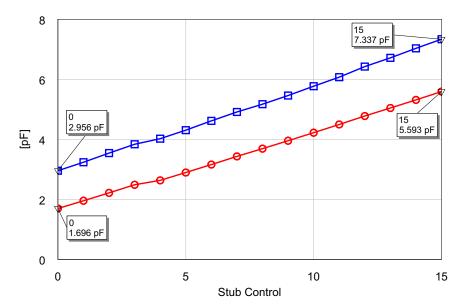


Figure 5.15: 16 states of stub capacitance for each stub in the MMIC double-stub tuner. Stub 1 capacitance is shown in red circles, and stub 2 capacitance in blue squares. The individual capacitor values are carefully chosen so that the capacitance is uniformly distributed.

the fabricated tuner. Simulation of the three variations generated the constellations shown in Fig. 5.17, with nominal design in the center.

In the design phase, the spacing between the adjacent lines was chosen from TriQuint TQPED design guidelines, but a detailed calculation of the effects of the line spacing was not performed, resulting in possible deviations between simulation and measurement. This was mitigated with three fabricated design variations in which  $C_2$  was changed. After the designs were submitted for fabrication, the linear simulations were augmented by adding coupled-line effects to areas where transmission lines were in close proximity to see how much the constellation would shift. The results are shown in Fig. 5.18. The constellation did move slightly to the left, but not significantly enough to warrant a second MMIC run. The variation in the stub 2 capacitance  $(C_2)$  resulted in a more significant constellation shift than did taking into account the mutual coupling between lines.

The loss of the switched-capacitor MMIC tuner should be relatively small, since the transistors are not located where the highest currents are (in the transmission path) but rather at the ends of the stubs. Figure 5.19 shows simulated insertion loss and  $S_{21}$  for the 50  $\Omega$  state

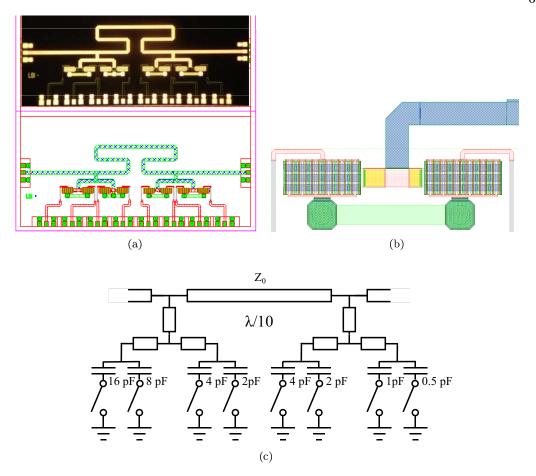


Figure 5.16: MMIC discrete double-stub tuner, reticle size  $5\times2.5\,\mathrm{mm}$ . (a) Layout and photograph of two design variations, (b) close-up of switched capacitors (yellow) and transistors, and (c) tuner schematic.

to be about 1dB, with a match of about -14dB.

#### 5.4.1 Measured results

A test fixture was fabricated to control and characterize the MMIC double-stub tuner. The mounted MMIC can be seen wire-bonded to the copper control lines in Fig. 5.20. The S-parameters of the tuner were measured across frequency for all 256 tuner states, by using a TRL calibration and 150  $\mu$ m probes. The  $S_{22}$  constellation of the nominal design is shown across frequency in Fig. 5.21 where the best coverage is seen for 2.45 GHz. The coverage at 2.45 GHz is similar to that in Fig. 5.18 at 1.95 GHz (yet rotated due to a difference in reference plane),

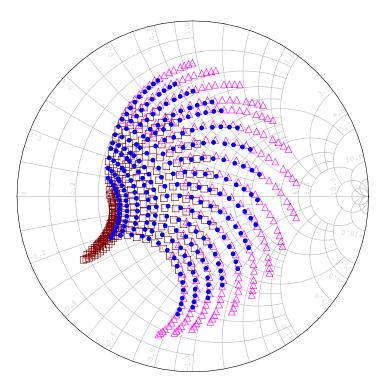


Figure 5.17:  $S_{22}$  constellations of three variations of the MMIC double-stub tuner design. The nominal design is in the center in blue dots. The constellation due to larger stub 2 capacitance is shown with magenta triangles; smaller stub 2 capacitance with brown boxes.

and as in the case of the switched delay line MMIC, the best frequency of operation is higher than simulated. The nominal design at  $2.45\,\text{GHz}$  produced the broadest  $S_{22}$  constellation out of the three design variations.

Loss is higher when  $C_1$  or  $C_2$  become larger. It is quite visible in Fig. 5.22 that as  $C_2$  increases, the loss increases quickly. Recall from Fig. 5.15 that stub 2 is the larger capacitance, and as more current flows into that stub, more losses result. For the 50  $\Omega$  case, it can be seen that loss was measured to be -1.5 dB and simulated to be -1 dB (see Fig. 5.19). As with the switched delay line MMIC, loss in this MMIC is higher than expected, but keeping the transistors out of the main current path helped to reduce the additional losses significantly.

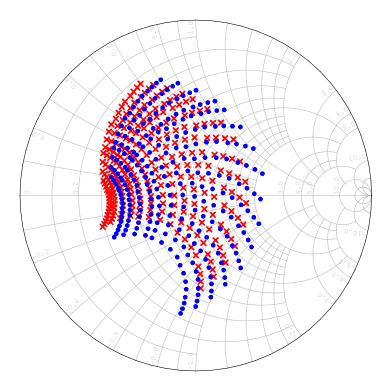


Figure 5.18: The change in the simulated  $S_{22}$  constellation due to mutual coupling is minor compared to the shift caused by varying  $C_2$ . The constellation marked by points of red  $\times$  is slightly shifted as a result of taking into account the mutual coupling between adjacent lines.

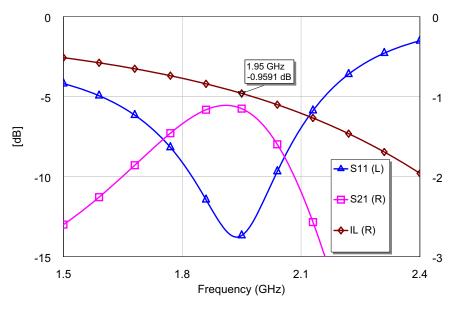


Figure 5.19: With a  $50\,\Omega$  load, simulation predicts the MMIC tuner to have about  $1\,\mathrm{dB}$  of insertion loss.  $S_{11}$  and is on the left axis,  $S_{21}$  and IL are on the right.

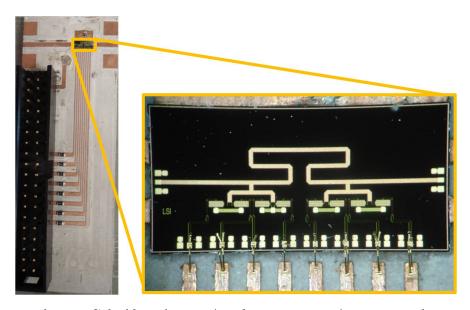


Figure 5.20: The MMIC double-stub tuner (reticle size  $5 \times 2.5 \,\mathrm{mm}$ ) was mounted on a substrate and wire-bonded to control lines. An FPGA was connected to control the tuner state. Stub 1 is on the right, stub 2 is on the left.

#### 5.4.2 Closed-Loop Tuning

The closed-loop tuning system discussed in Ch. 4 was large because it consisted of physically separate functional blocks (DAC, tuner, gain detector), and was limited in function because it could only monitor the magnitude of the reflection coefficient. The closed-loop tuning discussed here was designed specifically to integrate the functional blocks onto a single board and reduce the size of the system, while adding the ability to monitor the phase of the reflection coefficient, supporting a more advanced tuning algorithm. Therefore, a new circuit board was laid out to accommodate the FPGA connector, the MMIC tuner, the surface-mount bi-directional coupler, the gain/phase detector, and a pair of ADCs. All components can be seen mounted in Fig. 5.23.

As in the case of the tuner alone in the previous chapter, the new full system board must also be well characterized to understand the effects of the wire-bond transitions, the surface mount coupler, and any unforeseen layout or component features. With a TRL calibration, the system board was measured in all 256 states to compare it to the 256 states of the MMIC tuner alone. The difference can be seen in Fig. 5.24, and is not large enough to be of concern, although

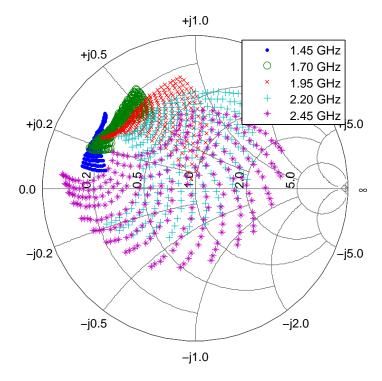


Figure 5.21: The measured Smith chart coverage for the MMIC double-stub tuner varies with frequency. The largest coverage area is for 2.45 GHz, and the points are uniformly distributed.

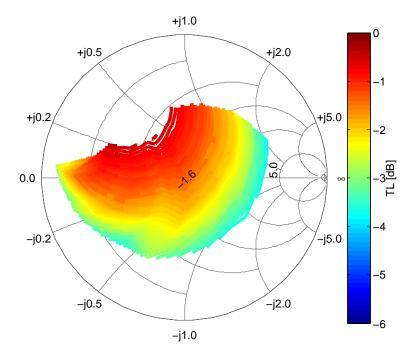
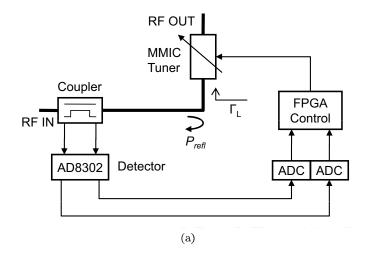


Figure 5.22: Measured tuner loss of the MMIC, using wafer probes, as a function of tuner state at 2.45 GHz. For the 50  $\Omega$  case, TL was measured to be -1.6 dB, but simulated to be -1 dB (see Fig. 5.19).



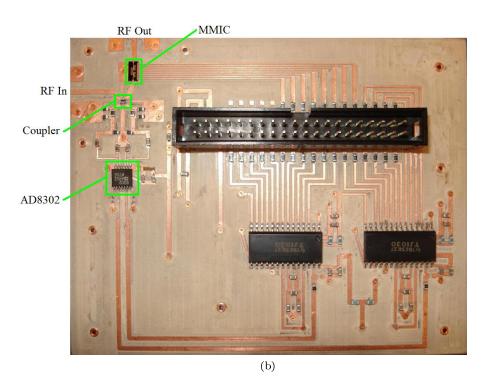


Figure 5.23: Integrated closed-loop tuning system circuit (a) block diagram, and (b) fabricated board. The FPGA connects through the 40-pin header.

it should be noted that the slight reduction in constellation size indicates higher losses. This is quantified by comparing Fig. 5.22 to Fig. 5.25, where it is seen that the loss for the MMIC system board is significant. For the  $50\,\Omega$  tuner state, loss increased from 1.6 dB to 3.9 dB, an increase of 2.3 dB, due to the addition of the surface-mounted bi-directional coupler and wire bonds. Since frequency of operation was 2.45 GHz instead of 1.95 GHz as originally planned,

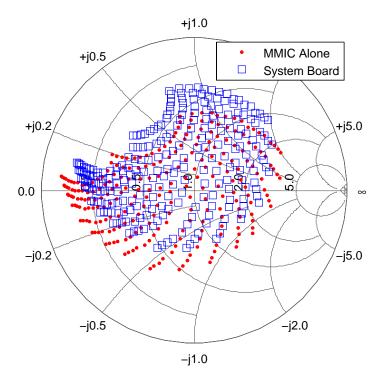


Figure 5.24:  $S_{22}$  of bare MMIC (measured with probes) compared with  $S_{22}$  of the system board. The system board has wire bonds and a bi-directional coupler in the RF path, which account for the change in the constellation.

the coupler (a narrowband component) was operating off-frequency, and is the source of the additional loss shown.

The Focus Microwaves mechanical single-slug tuner was calibrated to reproduce each of the 305 load impedances shown in the constellation of Fig. 4.9b, each of those load impedances was presented to the system board, and all 256 tuner states were measured for each. Therefore,  $256\times305$  combinations of tuner state and load impedance were used to measure full 2-port S-parameters (at 2.45 GHz) along with angle and magnitude data as detected by the system board. This complex automated measurement took about four days using an HP 8510C VNA, with an host computer capturing S-parameter data over GPIB and system board data over RS-232. The S-parameters of the system board were measured at the beginning and at the end of the four day measurement to check if the calibration drifted over time. Figure 5.26 shows the output impedance constellation of the system board both before and after, and the calibration drift

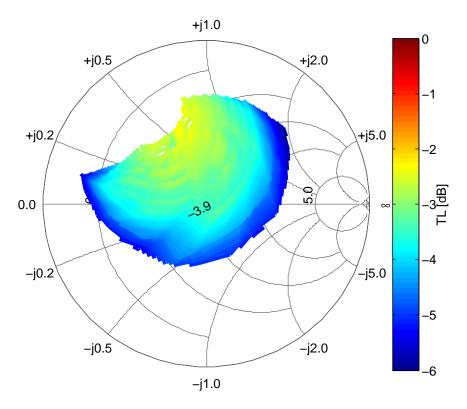


Figure 5.25: Measured tuner loss of the system board as a function of tuner state at 2.45 GHz. For the  $50\,\Omega$  case, TL was measured to be -3.9 dB, which includes the additional loss due to the bi-directional coupler.

is not a concern. Using the measured data, an impedance look-up table for each MMIC tuner state was constructed, indexed by angle and magnitude data, so that the tuning algorithm can quickly determine approximately what load impedance exists at port 2 of the system board. A secondary look-up table, indexed by load impedance, contains a value between 0 and 255, and allows the tuning algorithm to jump immediately to the tuner state that has been predetermined (from the S-parameter measurements) to be the best state for that load impedance. A final look-up table, indexed by load impedance and tuner state, contains the reflection coefficient seen at port 1 of the tuner system board, as measured by the VNA.

Since each tuner state has a unique transmission coefficient (both phase and magnitude), tuner state changes can have a negative effect on signal waveforms: the tuner state change will affect the phase and magnitude of the transmitted signal, as well as the amount of power reflected

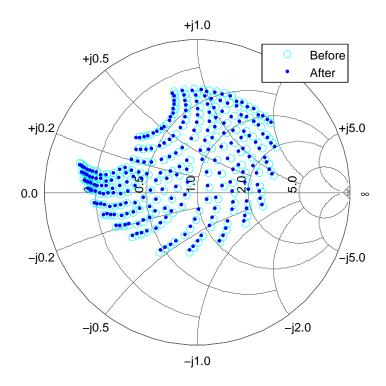


Figure 5.26: The measured  $S_{22}$  of the tuner system board before and after the 4 day measurement. The calibration drift is not enough to cause concern.

to the RFPA. If these changes occur during transmission of a modulated signal, the transmission could contain errors. Therefore, to maximize data rate means to avoid tuning unless necessary, and when tuning, to finish as quickly as possible. Therefore, this tuning algorithm was developed with two goals in mind: 1) tune as quickly as possible, and 2) tune only when necessary. In other words, minimize the number of tuner state changes.

The tuning algorithm has 5 main parts:

- (1) Measure magnitude and angle of reflection coefficient;
- (2) Determine load impedance from measured values;
- (3) Determine how well matched the system is;
- (4) Determine best tuner state for the load impedance;
- (5) Change to the new tuner state.

A decision is made after step 3 completes: if the system is well matched, as determined by a threshold, then no tuner state change is necessary, the tuning algorithm returns to step 1 and no tuner state change occurs. Another check exists after step 4: if the best tuner state is the same as the current tuner state, then there is no improvement to be made, and the tuning algorithm also returns to step 1 without changing the state of the tuner. A final check is in place after step 5: in the rare but possible case that a load impedance could cause the tuner to jump between two or more states, if step 5 is reached four consecutive times or more (consecutive is when the algorithm does not restart after step 3 or step 4), then the tuning algorithm will not change the tuner state. After step 5 completes, the algorithm continues at step 1. Through experimentation, it was determined that a change in load impedance will often result in 0 or 1 tuner state changes. Less frequently, a change in load impedance will result in 2 tuner state changes in quick succession. In rare cases, 3 tuner state changes will occur consecutively before the best tuner state is found. In all observed cases, when 4 or more tuner state changes occur, it is because the match does not meet the required threshold of step 3, and the tuner toggles between two states. This can occur when the load impedance falls in a region of the Smith chart that is incapable of being matched by the tuner.

A framework was created within Matlab in which the tuning algorithm could be tested. Figure 5.27a displays the initial condition, where the load impedance is set to  $50 \Omega$ . The figure is generated by starting at a given tuner state, and plotting a measured quantity as a function of load impedance. The three Smith chart plots are all related to reflection coefficient, which the tuning algorithm tries to minimize. For the Smith chart on the left, the measurement is reflection angle (as detected by the system board), scaled in degrees. For the Smith chart in the center, the measurement is reflection magnitude (as detected by the system board), scaled in dB. Referring to Fig. 5.27a, the tuner is in state 217, and in that state, a  $50 \Omega$  load impedance results in the raw angle measurement of 727 (58°) and the raw magnitude measurement of 267 (-16 dB). The measured angles and magnitudes when in tuner state 217 that result when other load impedances are presented can be determined from the color on the Smith chart. The Smith

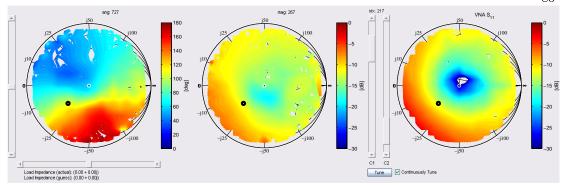
chart on the right shows the magnitude of  $S_{11}$  as measured by the VNA as a function of load impedance, when the tuner was in state 217. This represents the amount of reflected power the RFPA would see looking into the tuner under given conditions.

There are some interesting observations to make about the measured magnitude and angle of reflection coefficient. The first is the orthogonality of the constant magnitude and constant angle curves, which allows the algorithm to determine load impedance by looking in a type of grid (see Fig. 5.28). However, it is often possible that a particular set of measured magnitudes and angles has two solutions. To avoid choosing the wrong solution, an assumption is made that load impedance moves in a continuous fashion, and the closest of the two solutions will be the correct one. A more clever approach is to notice that there are two solutions in an area of interest, and change the tuner state such that the angle/magnitude grid becomes unambiguous in the area of interest. The additional measurement uniquely identifies the load impedance, but implies that a change in load impedance result in at least 2 tuner state changes.

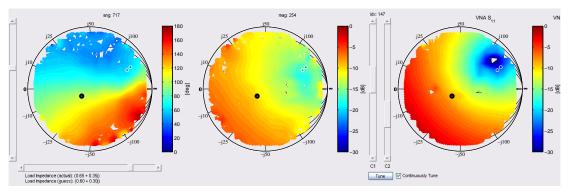
Another observation is that the conjugate of the output impedance of the system board does not line up on the load impedance that results in the smallest reflection coefficient. The black circle in Fig. 5.27a indicates the complex conjugate of  $S_{22}$  of the system board in tuner state 217, while the darkest blue in the center of the right Smith chart represents the load impedances which result in the least amount of reflected power at port 1. The explanation for this is that the tuner has more loss in state 217 than in state 135, where the output impedance of the system board is closest to 50  $\Omega$ . Higher loss means less reflected power at port 1.

Finally, note that the measured phase is always about 90° when the load impedance is the conjugate of the system board output impedance (the black circle always falls on a green constant angle contour). This is a desirable trait for this system because the AD8302 gain/phase detector cannot distinguish between positive and negative phases. The sign of the phase shown in the figures is unknown. The tuning algorithm is not sensitive to the sign of the phase because the phase change across the Smith chart is consecutive, and the phase values never reverse direction, which results in a grid that can be used to predict load impedance.

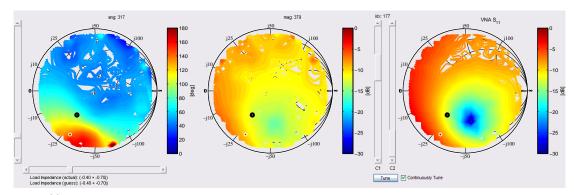




(a) System tuned to match a  $50\,\Omega$  load.



(b) System tuned for a  $93+j143\,\Omega$  load. The calculated load impedance (small red dot) is only an approximation of actual load impedance (small black dot).



(c) System tuned for a 7-j28.5  $\Omega$  load. The tuner is not able to reach the outer edge of quadrant 3.

Figure 5.27: The system board measures reflection angle (left) magnitude (center), calculates load impedance, and chooses the tuner state that resulted in the best match at port 1 as measured by the VNA (right). The actual load impedance is represented by a small black dot, the system guess at approximate load impedance is represented by a small red dot, and the tuner state is represented by a thick black circle at the location of the complex conjugate of  $S_{22}$  (refer to Fig. 5.26 for all tuner states).

The closed-loop tuning system has two fundamental metrics, Smith chart coverage, and loss. Figure 5.29 shows the unmatchable region near the edge of quadrant 3, and  $3\,\mathrm{dB}$  or more

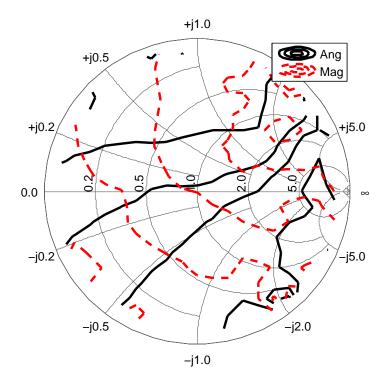


Figure 5.28: Constant angle and magnitude measurement contours for a given tuner state as a function of load impedance creates a grid that can be used to determine load impedance. In some cases, a constant angle contour will cross a constant magnitude contour twice, giving two possible solutions of load impedance.

of loss with this tuner system. If it is acceptable for VSWR to be 3 and better, and TL no greater than 3 dB, the Smith chart coverage area shown in Fig. 5.30 is 30%. A redesign of the board would spend more time ensuring that losses were minimized, especially with respect to the coupler.

This chapter presents designs of digital impedance tuners in GaAs MMICs and using discrete commercial MEMS switches. Experimental results for the MMIC tuner are presented in detail. In addition, a digital implementation of a PA tuner combined with closed-loop control is discussed. The performance of the tuning algorithm for various impedance mismatches is evaluated. Much of this work is reported in [39].

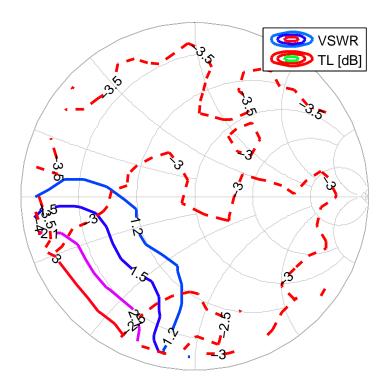


Figure 5.29: Tuner coverage and loss at 2.45 GHz for the system board. The edge of the Smith chart in quadrant 3 cannot be well matched. The loss is often around  $3\,\mathrm{dB}$ .

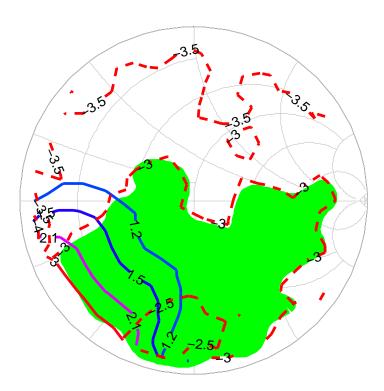


Figure 5.30: Smith chart coverage is 30% at 2.45 GHz for the system board, assuming it is acceptable to have VSWR of 3 or better, and TL of 3 dB or less.

## Chapter 6

## Transmitter Efficiency

The goal of the work presented in this thesis is to improve overall efficiency which is usually dominated by the last stage RFPA. The total efficiency of the last stage of the RF chain transmitter system in Fig. 6.1 can be defined as:

$$\eta_{tot} = \frac{P_{tx}}{P_{in} + P_{dc}}$$

where  $P_{tx}$  is power radiated by the antenna ( $P_{tx} = P_{DL}$  with antenna radiation efficiency of 100%). Loss mechanisms include conductive losses due to the finite conductivity of the metal in printed circuits and the skin effect at higher frequencies. Losses in the dielectric are not a significant source of loss at low microwave frequencies if a dedicated microwave substrate, such

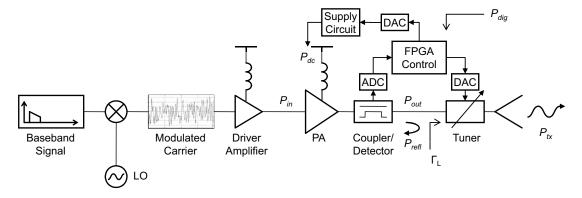


Figure 6.1: Block diagram of an RF front end, where the PA is protected by the tuner minimizing the reflected power seen by the PA. The output of the coupler/detector is converted by an ADC before being read by the FPGA. The FPGA then uses a search algorithm to set the tuner to a state that minimizes the VSWR seen by the PA. The tuner shown here is a continuous type, which means the FPGA needs a DAC to control it.

as Rogers 3203, is used. Active devices contribute to loss, as demonstrated in previous chapters, and the surface mount blocking capacitors and other bias line components contribute to loss. Some loss is due to unintended radiation, and some loss is due to mismatch where power is reflected back towards the source.

In mismatched conditions, output power from the RFPA is not delivered to the load and this work seeks to increase efficiency by minimizing mismatch. Minimizing mismatch has the added benefit that the output voltage swing of the RFPA can be reduced which allows it to operate more efficiently by reducing the bias voltage necessary to maintain performance.

#### 6.1 Efficiency Improvements with Impedance Matching

First, it must be stated that if there is no mismatch between the RFPA and the antenna, any circuit inserted between them can only add loss and therefore decrease  $P_{tx}$ . Thus, when discussing improvements in efficiency due to impedance matching, it must be granted that efficiency improvements only exist for those cases when mismatch exists, either due to a dynamically changing load impedance (e.g. an antenna with a changing near field), or a load impedance that is not known (e.g. a load that will be connected by an end user).

Consider first the amount of power delivered to an arbitrary load  $P_{DL}$  with no matching network. For example,  $P_{DL}$  into a  $100\,\Omega$  load is  $0.5\,\mathrm{dB}$  down from available source power  $(P_{AS})$  because of reflection (for a  $50\,\Omega$  system). This is called mismatch loss (ML). The power not delivered to the load because of mismatch is shown in Fig. 6.2a as a function of load impedance. It is zero in the center of the Smith chart - the matched condition. In order for a tuner to improve efficiency, for a given impedance on the Smith chart the impedance tuner must have less loss than the mismatch loss that would have existed without the tuner, plus the IL of the isolator that is being replaced  $(0.5\,\mathrm{dB})$ . Tuner loss from the three tuners presented in this work are presented in Fig. 6.2: the continuous tuner from Ch. 4, and the MEMS and MMIC tuners from Ch. 5. The region in which the tuner is a better solution than the isolator has been filled with gray, and as it is desirable to reduce the loss of the tuner, it is desirable to shrink the gray

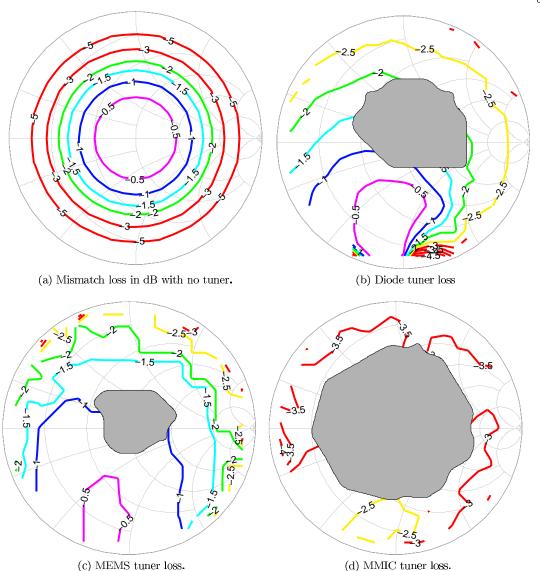


Figure 6.2: Loss of various impedance matching networks. (a) no matching network, (b) diode tuner from Ch. 4, (c) MEMS tuner from Ch. 5, and (d) MMIC tuner from Ch. 5. The gray area indicates where TL is greater than what the combination of ML and IL would be.

area. Figures 6.2b-d show the gray areas of the Smith chart where the tuner loss is worse than isolator IL plus ML. If the tuner losses could be cut in half (that is if 3dB of loss could be cut down to 1.5dB), then the less-efficient region shrinks, as shown in Fig. 6.3. In this way it can be quantified how much Smith chart coverage can be gained if tuner loss is improved.

Efficiency gains near the outside of the Smith chart can offset the efficiency losses near the center for cases when the load impedance fluctuates equally in both regions, as might be possible

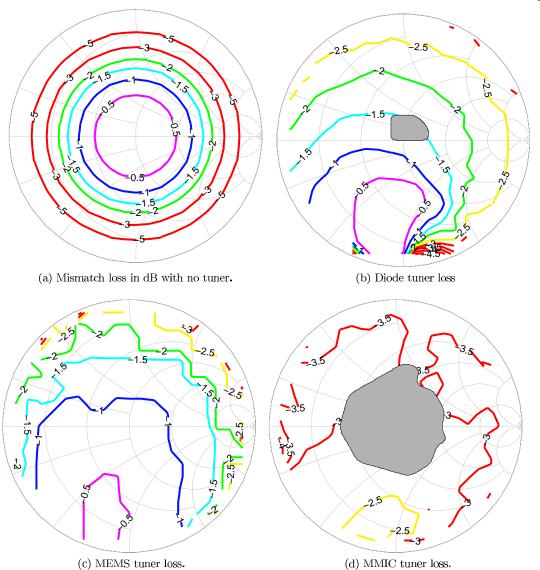


Figure 6.3: If the loss of various impedance matching networks could be cut in half (in dB) the inefficient area decreases. (a) no matching network, (b) diode tuner from Ch. 4, (c) MEMS tuner from Ch. 5, and (d) MMIC tuner from Ch. 5. The gray area indicates where TL is greater than what the combination of ML and IL would be.

with a handheld radio. Unfortunately, this is very hard to predict, as end-user environments and applications vary significantly. A probability density function of load impedance, if it existed, could be used to determine how much loss in which regions of the Smith chart were acceptable to achieve an overall efficiency improvement. The tuners shown here were designed for large tuning ranges, and so the losses can realistically be decreased by shrinking the tuning range. A

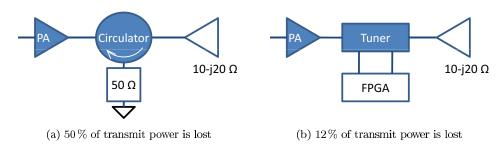


Figure 6.4: For the case where  $Z_L = 10 - j20 \Omega$ , using the adaptive tuner instead of the circulator saves power and improves overall efficiency.

good tuner loss would be in the range between -0.5 dB and -1 dB.

All three double-stub tuner designs in this work have lowest loss when matching load impedances near the bottom of the Smith chart. This area could be relocated for specific applications by adding a section of transmission line between the tuner and the load. For the case where  $Z_L = 10 - j20 \,\Omega$ , 50% of the incident power would be reflected and dissipated in the isolator or the RFPA. If instead the analog diode tuner from this work was placed between the RFPA and the load, VSWR could be tuned down to 2:1, with 0.6dB of TL, resulting in just 12% of the transmit power lost. This is depicted in Fig. 6.4.

#### 6.2 Efficiency Improvements with Adaptive RFPA Supply

The adaptive RFPA power supply allows the supply voltage headroom to be dynamically adjusted to barely accommodate the saturation limit of the RFPA for various RF transmit power levels. For example, under high load (such as a data transmission), a WCDMA RFPA typically draws 300-600 mA at 3.4 V, but under low load (such as voice transmission), it draws from the supply as little as 30 mA at 0.8 V [75]. At peak transmit power, the RFPA draws maximum current and voltage from the supply, but when operating at anything less than peak power, the adaptive power supply can significantly improve the system efficiency by reducing the overhead. Since peak transmit power only occurs when the mobile phone is very far away from the base station and transmitting data, the potential for efficiency improvement is large.

A large VSWR at the output of an RFPA can distort the transmitted signal [37] which can be mitigated by setting the supply voltage to a level that is high enough to overcome the distortion. Unfortunately, this also negatively affects efficiency by increasing the overhead. However, the inclusion of an adaptive matching network allows the VSWR to be minimized, negating the need for the excessive RFPA supply overhead, while also providing VSWR as an input to the adaptive power supply, allowing it to decrease overhead as the tuner decreases VSWR. The adaptive impedance tuner of Ch. 4 was used in conjunction with an adaptive power supply controlling an Avago WS2512 RFPA. The adaptive power supply is a non-inverting buck-boost converter that was developed by Dr. Rajarshi Paul of the University of Colorado at Boulder [76]. It is designed to be powered from a Li-ion battery with voltages ranging between 2.7V and 5.5V, and generates voltages between 0.8V and 3.6V. Special attention was given to reduce output voltage ripple and efficiency in the buck-boost mode transition region; the PID compensator uses a different set of coefficients for buck and boost modes to maintain a high gain margin. Details of the adaptive RFPA supply design and function can be seen in [40].

The adaptive power supply runs with efficiencies as high as 85%; higher than 80% in most conditions. Combining the measured data from the adaptive power supply with the measured data from the PA and impedance tuners allows transmit power  $P_{tx}$  and total efficiency  $\eta_{tot}$  to be estimated, assuming antenna radiation efficiency to be 100% in all cases. Figure 6.5 shows PAE with a mismatch of VSWR = 4 as a function of  $P_{tx}$ , for three cases: a fixed bias voltage, the adaptive bias voltage, and the adaptive bias voltage with adaptive tuning. At high transmit powers, the adaptive supply voltage is the same as the fixed supply voltage, so no improvement is seen. For lower transmit powers – the most frequent operation of the RFPA – the adaptive bias nearly doubles the efficiency over the fixed bias. When the adaptive tuning is also added, the improvement doubles for lower transmit powers. However, for higher transmit powers, the efficiency improvement is dramatic, and because the amount of mismatch is reduced, higher transmit powers are possible and efficiency improves quickly. The combination of adaptive PA bias and adaptive tuning results in the highest efficiency, as well as the highest transmit power.

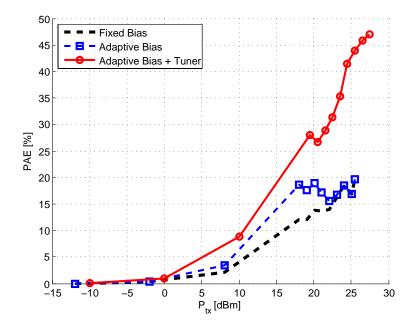


Figure 6.5: Efficiency as a function of  $P_{tx}$  for three cases: fixed PA bias, adaptive PA bias, and adaptive bias with adaptive tuning for a VSWR = 4. The combination of adaptive PA bias and adaptive tuning results in the highest efficiency, as well as the highest transmit power.

	$P_{in}$	VSWR		
		2.3	4	5.5
Diode	$0\mathrm{dBm}$	5.6%	8.3%	7.2%
	$3\mathrm{dBm}$	3.6%	7.1%	8%
MEMS	$0\mathrm{dBm}$	8.9 %	13.2%	7.6%
	$3\mathrm{dBm}$	6.9 %	12%	8.6%

Table 6.1: Improvements in  $\eta_{tot}$  by using a combination of adaptive tuning and adaptive bias, as opposed to using a fixed bias and no tuning. The best improvement is 13.2% for VSWR=4 with the MEMS tuner at  $0\,\mathrm{dBm}$  input power.

This is the best case as presented in [40, 76]; actual tuner loss was not accounted for in the estimation.

For two tuners, the analog diode tuner and the MEMS tuner, Figs. 6.6-6.9 show efficiency and transmit power as a function of VSWR (phase of reflection is 0) under the following conditions: battery voltage of  $2.7\,\mathrm{V}$ , input power  $0\,\mathrm{dBm}$  and  $3\,\mathrm{dBm}$ , amplifier gain of  $20\,\mathrm{dB}$ , and actual tuner loss. The results are summarized in Table 6.1. Loads with phase 0 were chosen in accordance with [77], where the worst case drain voltage swing was found to be at phase 0. Other reflection coefficient angles and magnitudes were also confidence tested to confirm the

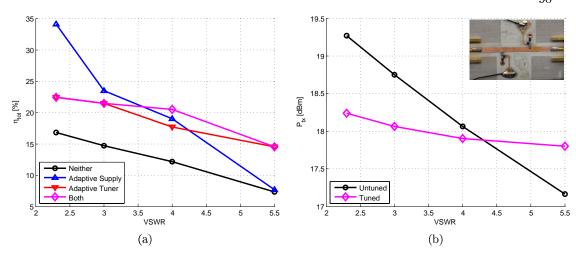


Figure 6.6: Calculated (a) total efficiency  $\eta_{tot}$  and (b) transmit power  $P_{tx}$  as a function of load VSWR (phase 0) for 0 dBm input power to the amplifier, and the diode tuner at the output.

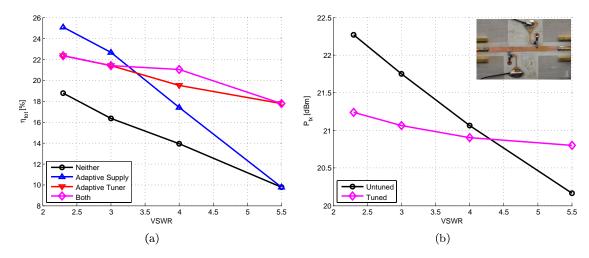


Figure 6.7: Calculated (a) total efficiency  $\eta_{tot}$  and (b) transmit power  $P_{tx}$  as a function of load VSWR (phase 0) for 3dBm input power to the amplifier, and the diode tuner at the output.

closed-loop tuning system functions in the range allowed by the tuner, but those results are not shown here. Because of the adaptive supply and tuner, the best case total efficiency improves from 27% to 37% when the RFPA is producing maximum output (8dBm RF input power, efficiency calculated assuming loss from the MEMS tuner). Because of the loss of the tuner, as discussed in the previous section, it can be seen in the figures that the best improvements in  $\eta_{tot}$  are for highly mismatched loads.

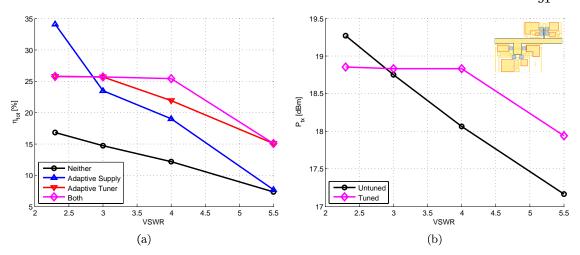


Figure 6.8: Calculated (a) total efficiency  $\eta_{tot}$  and (b) transmit power  $P_{tx}$  as a function of load VSWR (phase 0) for 0 dBm input power to the amplifier, and the MEMS tuner at the output.

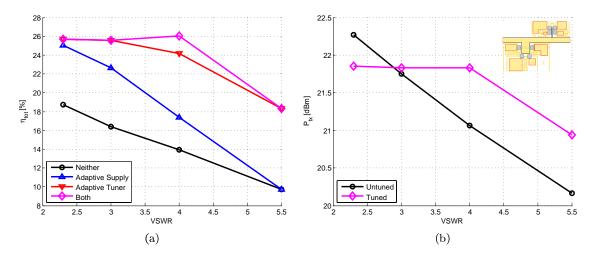


Figure 6.9: Calculated (a) total efficiency  $\eta_{tot}$  and (b) transmit power  $P_{tx}$  as a function of load VSWR (phase 0) for 3dBm input power to the amplifier, and the MEMS tuner at the output.

In summary, this chapter discusses overall system efficiency with a comparison to untuned PAs. In addition to tuning impedance, the feedback signal is used as an input to an adaptive power supply. It is shown that up to 13.2% of PAE can be gained by simultaneous impedance and bias tuning for a VSWR of 4. These results, using the analog varactor-based tuner, are reported in [40].

## Chapter 7

### Conclusions and Future Work

#### 7.1 Conclusions

The results presented in this work are useful to guide future implementations of adaptive RF front end components, and it has been shown already that the loss of the matching network plays a large role in determining if the system efficiency can be improved. If there is no mismatch between the RFPA and the antenna, anything inserted between them can only decrease  $\eta_{tot}$ . Thus, improvements in efficiency only exist when mismatch loss exists. For VSWR=2, the loss due to mismatch is 0.5 dB. Therefore, an impedance tuner that seeks to improve efficiency for loads causing a VSWR > 2 must have loss less than 0.5 dB. Figure 7.1 shows what the maximum loss of an impedance matching network should be for a target range of mismatched impedances up to mismatch loss of -10 dB, or VSWR = 38. The impedance tuner should also present an impedance that results in return loss equal to or better than the return loss shown for a given VSWR. A mismatch implies power reflection which can damage the device, e.g. the output stage of a high-power transmitter. This is avoided in standard front ends by adding an isolator or circulator, which dissipates the reflected power, thus reducing system efficiency. Therefore, the second benefit of adaptive impedance matching is eliminating the often bulky and lossy circulator/isolator while protecting the active device. Finally, when reflected power is minimized, the power amplifier output level does not need to be increased to maintain power density levels at the receiver. This leads to the third benefit of adding an adaptive tuner to the front end, namely adaptive tuning requires measurement of the mismatch and this information

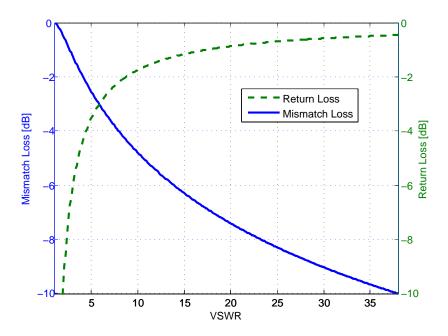


Figure 7.1: Mismatch loss and return loss in decibels as a function of VSWR. The loss of an impedance matching network should be less than the mismatch loss for the target range of impedances to be matched.

can be used to adjust the supply of the PA which improves overall efficiency. For example, a maximum improvement in  $\eta_{tot}$  of 13.2% is shown when the adaptive impedance tuning is combined with an adaptive PA power supply.

Without knowing how much time an antenna will endure near-field loading, and therefore how often the RFPA encounter high-VSWR conditions, it is difficult to say precisely whether total efficiency is improved over the long term. Since improvemens in  $\eta_{tot}$  are best for highly mismatched loads, wildly varying or routinely mismatched load impedances will benefit the most from adaptive tuning.

Furthermore, the impedance of an antenna on a handheld radio can vary greatly. In this work, confirming what is found in published literature, it is shown that VSWR=4 is a level of mismatch that exists when the antenna is close to the human body, and therefore efficiency improvements for that level of mismatch are worth investigating.

Specific contributions of this thesis are summarized as follows:

• A new measure of tuner performance is introduced, tuner loss (TL), which is shown

by example to be a more logical choice than insertion loss (IL). This new figure of merit improves on quantities such as loss factor (LF), which has been used in tuner literature to date and does not accurately describe tuner loss. This contribution has been reported in [38] and it is the hope that future publications in this field will adopt this straight-forward and valuable metric. Like LF, TL has the benefit of being easy to measure since there is no need to present a range of load impedances.

- A diagnostic circuit was integrated with both an adaptive impedance matching network and an adaptive power amplifier bias supply circuit to achieve efficiency increases not possible with either of the adaptive systems alone. An FPGA was used to implement the closed-loop algorithm, with an ADC to read the output of the diagnostic circuit. This approach, along with demonstrated results, is reported in [38–40].
- A new tuning algorithm was shown to be able to adapt to a new load impedance in no more than 3 steps, and often in only 1 tuner state change. Compared to other search algorithms that can take hundreds of seconds, and the previously quickest one that can tune in 10 steps [71], this algorithm is the quickest tuning algorithm known at the time of this work. The speed of the algorithm requires additional knowledge *a priori*, but the trade-off for speed enables the algorithm to be employed by systems that require minimal down-time, such as is the case in GSM systems with short timeslots. These results are reported in [39].
- A variety of impedance tuners were designed and fabricated, providing experimental validation of the tuning algorithms and metrics.
- As related work, load-pull measurements were performed on a commercial amplifier in
  the 2.45 GHz ISM band, leading to the recommendation of a new matching network,
  and a planar Yagi-Uda antenna was integrated onto the same PCB to demonstrate lowpower long-range wireless communication, which are reported in [41] and shown in the
  appendix.

#### 7.2 Some Directions for Future Work

It is paramount for adaptive matching networks to have low loss if they are intended to improve system efficiency. The loss of the system board could be improved by: 1) integrating a bi-directional coupler directly into the MMIC chip, eliminating the need for microstrip transitions, or 2) improving the transition from the substrate to the surface-mount coupler, and to the MMIC using wire-bonds, as indicated previously in this work by the difference of the MMIC tuner output impedance and loss before and after being mounted on the system board. Additionally, other tuner topologies will have different loss characteristics, and should be investigated along with the loss mechansim of the double-stub tuners used.

Only informal linearity measurements were taken on the diode tuner, concluding that the bias voltage must be much higher than signal voltages for the case of the diode tuner to prevent significant distortion. The effects on linearity of the MMIC tuner needs to be investigated, to formally validate the prediction that switched-capacitor tuner topologies are less susceptible to nonlinearities.

The novel tuning method presented in this work is based on a one-time calibration that is not necessarily valid for temperature variations. Further enhancements could be made to improve the validity of the look-up tables over time, if the effects of heat on each component were quantitatively known.

This work investigated tuning impedance for a single frequency for various load impedances, but an investigation of tuning impedance for a single load impedance across various frequencies would provide useful input for the design of multi-band or wide spread-spectrum technologies. Automatic tuning across frequency is done in [71, 78], and this algorithm would require the system board characterization to be performed across frequency, and additional look-up tables stored. The tuning system would then need to be able to detect frequency, or be given current frequency by a higher-level system, and use that information to choose the correct set of look-up tables.

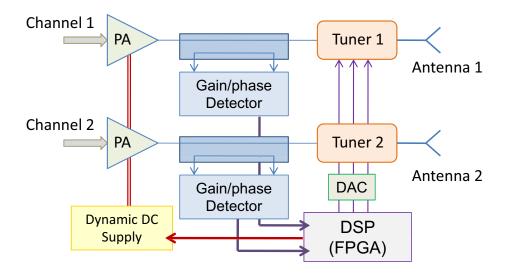


Figure 7.2: MIMO systems present a new impedance matching problem, as it is unknown if the mutual coupling between channels helps or hurts adaptive impedance matching.

Another interesting extention of this work is in multiple-input multiple-output (MIMO) systems [79] which are now emerging for increasing capacity in handsets. A possible approach is illustrated in Fig. 7.2 for the case of a  $2\times2$  MIMO system. This presents a new problem for impedance matching because near-field interactions affect multiple mutually coupled antennas. It is unknown if the additional antenna coupling helps or hinders the ability to automatically tune impedance.

A number of microwave applications in medicine can also benefit from adaptive tuning which can compensate in the variation of tissue complex impedances in the microwave regime. One such example is in using high-power microwaves for tumor ablation [80]. Another example is for using on the order of 50 W of microwave power in the 2.45 GHz ISM band for sealing blood vessels during surgery [81]. There has been increased interest in non-invasive temperature measurements inside the human body using multiple-channel microwave radiometry [82–84]. Applications include monitoring infant brain temperature for preventing a specific disease as well as monitoring core temperature of people under heavy stress or activity level [85]. Due to the large range of body tissue distribution among different humans, the probe antenna might require

 $<sup>^1</sup>$  http://www.valleylab.com/mwablation/intro.html

impedance tuning in order to increase the SNR of the Dicke receivers. In this application, low insertion loss of the tuner is critical since any loss will degrade the receiver system temperature (noise figure), pointing to the use of MEMS-based low loss tuners.

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## Appendix A

# Long-Range Low-Power Wireless Link in the 2.4 GHz IMS Band

In this paper we demonstrate a 30 km point to point link at 2.45 GHz using the TI CC2500 RF Transceiver, TI CC2591 RF Front End, and a planar Yagi-Uda antenna on an FR4 substrate. The RF Front end is first characterized in a load-pull system to find the optimal load impedance, which is then matched to the antenna. A simple test sequence is transmitted between two battery-powered stations with clear line-of-sight that are over 30 km apart.

#### A.1 Introduction

Cordless phones, Internet access points, and home security systems are a few applications found in many homes today that use frequencies in the 2.4 GHz unlicensed Industrial, Scientific and Medical (ISM) band.

In the USA, the FCC sets the limits of unlicensed use [86–88]. Systems must employ frequency hopping or digital modulation, the maximum peak conducted output power shall not exceed 30 dBm, and antennas can have up to 6 dBi gain. Generally, for each decibel of output power not used, antenna gain can be increased by a decibel. In the case of a point-to-point link, antenna gain can increase 3 dB for each decibel of output power not used. Since this paper focuses on a point-to-point link, the latter requirement applies.

It is always a goal to increase battery life and efficiency in handheld radios. In this

paper, we combine a low-cost low-power 2.4 GHz RF transceiver [89] with a 2.4 GHz RF front end PA/LNA [90] and a PCB increased-gain antenna in order to demonstrate a low-power long-range 2.4 GHz wireless link (Fig. A.1).

#### A.1.1 Link Budget

The output power of the CC2591 is 21 dBm, and the antenna gain 7 dBi, which gives 28 dBm EIRP, well below FCC limits for point-to-point links. The receiver sensitivity of the CC2500 is -104 dBm (for 1% PER at 2.4 kbps), and the CC2591 adds an additional 6 dB of sensitivity. Along with the 7 dBi antenna, the receiver has effective sensitivity of -117 dBm. The total link budget is therefore 145 dB. According to the Friis formula, with matched antenna polarization, this translates to almost 155 km of range, with just below 1 dB of link margin.

#### A.2 RF Front End Characterization

The TI CC2591 RF front end datasheet [90] suggests an output matching network for  $50\,\Omega$ . A load pull measurement was used to find the best load impedance for the maximum power transfer out of the device. Well-characterized mechanical tuners from Focus Microwaves were used at the input and output of the CC2590 and performance was measured for a large set of load impedances. Optimal load impedance for maximum gain was found to be 14.6 - 6.4j  $\Omega$ , as shown in Fig. A.2. AWR's Microwave Office was used to design a matching network implemented with surface mount (0603 package size) capacitors and inductors from AVX. With the short CPW interconnects, we expect a series 1.2 nH inductor followed by a shunt 1.7 pF capacitor to provide the best match to  $50\,\Omega$  at 2.44 GHz.

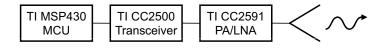


Figure A.1: Block Diagram

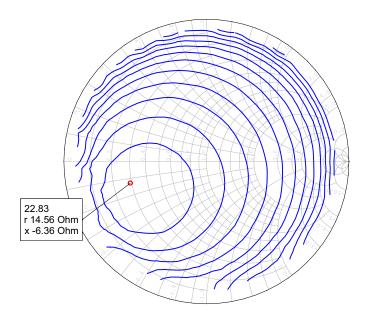


Figure A.2: Load Pull of CC2591 output stage. The blue circles show gain in 1 dB increments, with the first contour at 22 dB. Maximum gain is seen to be 22.83 dB for a 14.6 - 6.4j  $\Omega$  load.

#### A.3 Circuit Design

The design of this transceiver is heavily based upon the target board found in ez430-RF2500 evaluation kit available from Texas Instruments [91]. The MSP430F2274 and CC2500 devices are implemented verbatim from the ez430 kit, with the addition of the CC2591 PA/LNA and the antenna discussed below. This approach creates maximum potential reuse of the firmware and projects available for the ez430-RF2500 kit. Only slight modifications for operating the CC2591 were needed, and some of the many unused GPIO pins were used for this purpose. Because maximum design reuse was a goal, no additional effort was made to optimize the power consumption of this board. An adjustable linear regulator (TI TPS73701) creates a 3.6 V bus capable of powering the entire system, which was chosen because it provides the highest RF output power from the CC2591 while still being compatible with the MSP430 series of MCUs.

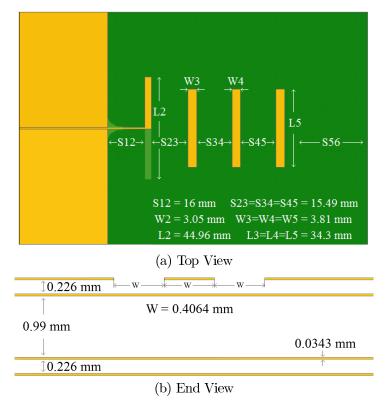


Figure A.3: (a) Top view of printed Yagi-Uda array fabricated on a four-layer 62-mil thick FR4 substrate (4" by 6" shown) with layers shown in (b). The ground plane on all 4 layers acts as the reflector. The upper arm of the feed element and all of the directors are on the first layer. The lower arm is on the second layer.

#### A.4 Antenna Design

The antenna is designed to be fabricated on the same PCB substrate as the circuit, with a total area limited to  $10 \,\mathrm{cm}$  by  $19 \,\mathrm{cm}$  (4" by 7.5") and a desired gain of 8 dBi. With input from [92, 93], a printed Yagi-Uda array was designed using full wave (HFSS) simulations and is shown in Fig. A.3. The feed dipole element is fed with a printed two-wire transmission line, and the ground plane, printed on all four layers of the pcb, acts as the reflector. The arms of the feed dipole element are printed on separate layers; referring to the figure, the bottom arm stays on the second (internal) layer, while the top arm and all of the directors reside on the top layer. Simulations were performed to optimize the feed dimensions, the director size (L3 = L4 = L5) and spacing (S23 = S34 = S45), and distance (S56) from the last director to the radiating edge

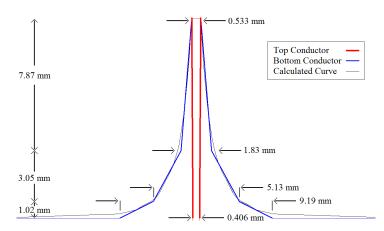


Figure A.4: Detail of balun transition from  $50\,\Omega$  microstrip line (bottom) to  $50\,\Omega$  printed two-wire dipole feed (top). The top layer (red) is a widening linear taper, and the ground plane (blue) is a 3-section linear taper that was found to satisfactorily approximate the calculated curved taper (black).

Microstrip	Printed Two-Wire	Balun
-0.114 dB	-0.13 dB	<b>-</b> 0.17 dB

Table A.1: Transmission Loss on FR4 at 2.45 GHz.

of the pcb.

Details of the balun transition are shown in Fig. A.4. The top conductor is a widening linear taper, and the dashed line in the figure shows the calculated curve for the bottom conductor that maintains a constant impedance from  $50 \Omega$  grounded CPW line (the dimensions are such that the line behaves mostly as microstrip) to  $50 \Omega$  printed two-wire transmission line. The solid line, which is a three-section narrowing linear taper with dimensions shown, adequately approximates the calculated curve. More taper sections added to geometric complexity, and fewer sections decreased balun performance. Simulated values for the transmission coefficient ( $|S_{21}|$ ) of the grounded CPW (microstrip) line, printed two-wire feedline, and the designed balun transition are summarized in Table A.1, assuming that the relative permittivity of FR4 is 4.2 and the loss tangent is 0.02 at the frequency of interest.

Simulations were done to determine the sensitivity of the antenna to director size (L3 = L4 = L5) and spacing (S23 = S34 = S45), and distance (S56) of the last director from the edge of the pcb, referring to Fig. A.3. The sensitivity of director length is shown in Fig. A.5 and the

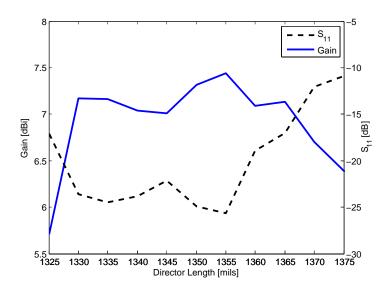


Figure A.5: Simulated realized gain and input match at 2.45 GHz as a function of director length.

resulting final dimensions of the antenna can be seen in Fig. A.3.

It was found that adding additional directors had diminishing returns because of the loss of the FR4 substrate at 2.4 GHz. For example, the printed two-wire section of the antenna feed has > 10 dB/m loss. A compromise on the number of directors was decided on that was within size constraints and achieved simulated gain performance of > 7 dBi. Using calibrated horns (model H-1498 from American Electronic Laboratories, Inc.), the antenna (fabricated at Advanced Circuits in Aurora, CO) was measured in an anechoic chamber at the University of Colorado to check maximum gain in the direction of propagation, +/- 30 degrees from boresight. Figure A.6 shows that performance matches well in this region. Limitations of the particular anechoic chamber used prevents measurements at angles > 30 degrees. Input match is shown in Fig. A.7.

#### A.5 Demonstration

Neglecting obstacles and surface features, basic line-of-sight equations tell us that two antennas each 15 m above ground have maximum 30 km range, and two antennas each 160 m above ground have a maximum 100 km range. In our testing, one antenna was near ground level,

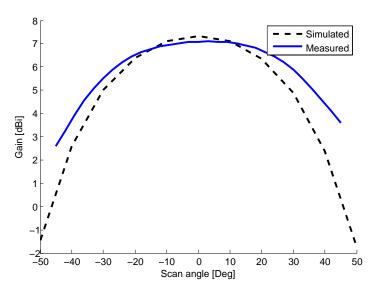


Figure A.6: HFSS simulated realized gain at 2.44 GHz is 7.3 dBi. Measured gain is 7.1 dBi.

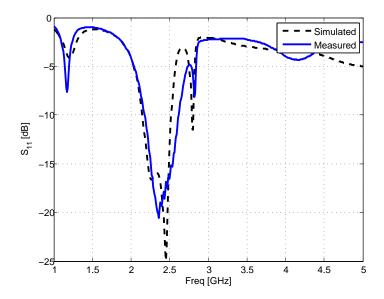


Figure A.7: Simulation and Measurement of  $S_{11}$  of the antenna are in good agreement. Measured 10 dB bandwidth is 18.5%.

while the other antenna was higher than  $500\,\mathrm{m}$  on the side of a mountain; such conditions also provide for an ideal maximum of  $100\,\mathrm{km}$  of visibility.

Since power falls off as  $r^{-2}$ , the low-power long-range figure of merit can be defined as  $FOM = 1000 \cdot d \frac{\sqrt{S}}{\sqrt{P}}$ , where d is distance in meters, S is receiver sensitivity, and P is total power necessary to run the transmitter. With 50 km of demonstrated operational range, -117 dBm of

effective receiver sensitivity, and  $0.601\,\mathrm{W}$  of required transmitter system power, this work has achieved FOM=91. It is hoped that future works in this area will use the same metric for comparison of long-range wireless links.