GaN Microwave DC–DC Converters

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***Abstract*—This paper presents the design and characterization of dc–dc converters operating at microwave frequencies. The converters are based on GaN transistor class-E power amplifiers (PAs) and rectifiers. Three topologies are presented, which are: 1) a PA and synchronous rectifier, requiring two RF inputs; 2) a PA and self-synchronous rectifier with a single RF input; and 3) a power oscillator with a self-synchronous rectifier with no required RF inputs. The synchronous 1.2-GHz class-E^2 converter reaches a maximum efficiency of 72% at 4.6 W. By replacing the RF input at the rectifier gate with a specific termination, a self-synchronous circuit demonstrates 75% efficiency at 4.6 W, with a maximum output power of 13 W at 58% efficiency. In the third topology, the PA is replaced by a power oscillator by providing correct feedback for class-E operation, resulting in a circuit requiring no RF inputs. This oscillating self-synchronous dc–dc converter is demonstrated at 900 MHz with an efficiency of 79% at 28 V and 12.8-W output power. Self-synchronous class-E transistor rectifier operation is analyzed theoretically in the time domain and validated with harmonic-balance simulations using an improved nonlinear model for a GaN HEMT. The simplified theoretical analysis provides a useful starting point for high-efficiency self-synchronous power rectifier design, which can, in turn, be extended to high-efficiency oscillating power inverter design.**

***Index Terms*—GaN, high-efficiency power amplifiers (PAs), high-frequency dc–dc converters, microwave rectifiers, RF circuits, switching PAs, ultrahigh-speed electronic circuits, VHF and UHF technology.**

I. Introduction

THE SWITCHING speed of dc–dc converters has been increasing over the past five years, e.g., [1]–[3], with a goal of reduced size, faster transient response, and increased power density, which result from reduced values and sizes of passive components (inductors and capacitors). With increasing voltages and power densities enabled by wide-bandgap semiconductors such as GaN, monolithic integration towards a chip-scale power supply becomes a possibility [4].

TABLE I
High-Frequency DC–DC Converters Comparison

Ref.	Year	f (GHz)	Technology	P_{out} (W)	η (%)
[5]	2008	0.030	MOSFET	220	87
[3]	2014	0.100	GaN	7	91
[6]	2009	0.110	LDMOS	25	86
[7]	2005	0.233	CMOS	0.55	82
[8]	2012	0.780	GaN	11.5	72
This work	2015	0.9	GaN	12.8	79
[9]	2013	1	GaN	8.5	77
This work	2015	1.2	GaN	5.0	75
[10]	1999	4.5	GaAs	0.053	64

Higher switching frequencies are accompanied by reduced efficiency and attainable power levels since the losses in both passive and active components increase with frequency. In addition, parasitic reactances in the active devices and packages limit switching frequencies, as described in [1]. Table I presents an overview of high-frequency dc–dc converters and their respective efficiencies reported in the literature. In [5], a 30-MHz 200-W Φ_2 dc–dc converter operating at up to 200 V is demonstrated. A 23-W 87% efficient boost converter switching at 110 MHz is implemented using LDMOS technology in [6]. In [7], an integrated low-power four-phase buck converter is implemented in a 90-nm CMOS process with switching frequencies of 100–317 MHz. An off-chip air-core inductor is used in this case, resulting in efficiencies from 80% to 87%. In [3], a 100-MHz switching frequency buck converter is integrated together with its drive circuitry on a single 2.3 mm $\times$ 2.3 mm chip in the TriQuint (Qorvo) 150-nm GaN on a SiC D-mode pHEMT process. This converter exhibits an efficiency of over 90% at 7 W.

Two greater than 70% efficient class-E^2 converters operating at 780 MHz and 1 GHz were demonstrated in [8] and [9]. Packaged and die 400-nm GaN HEMT devices from CREE were combined with high-Q coils and capacitors in hybrid circuit implementations. Wide-bandgap semiconductor devices, and in particular GaN HEMTs, enable high operating voltages at high frequencies, in contrast to circuits based on Si CMOS. Although very high power densities at the circuit level can be achieved with CMOS at lower frequencies (e.g., [6] and [7]), higher frequencies converters offer the potential for completely distributed implementations and fully monolithically integrated power supplies. Over two decades ago, as high as 64% efficiency was obtained with GaAs devices in a circuit based on transmission lines only, operating at 4.5 GHz at sub-watt power [10], with both a power amplifier and a power oscillator as

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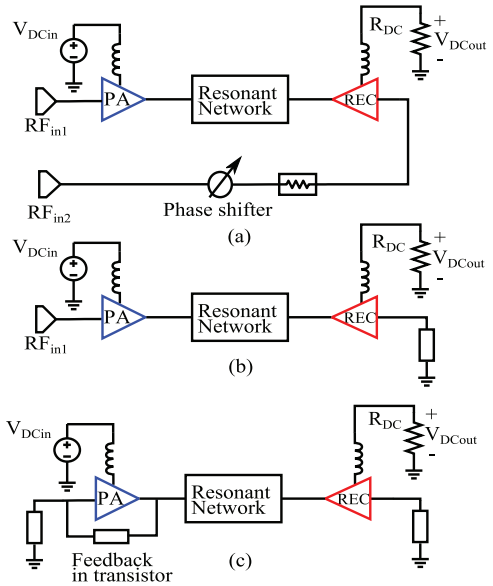


Fig. 1. Block diagram of high-frequency class-E² dc–dc converter. (a) Synchronous topology, (b) self-synchronous topology with a single RF input at the inverter input, and (c) oscillating self-synchronous topology with no RF inputs.

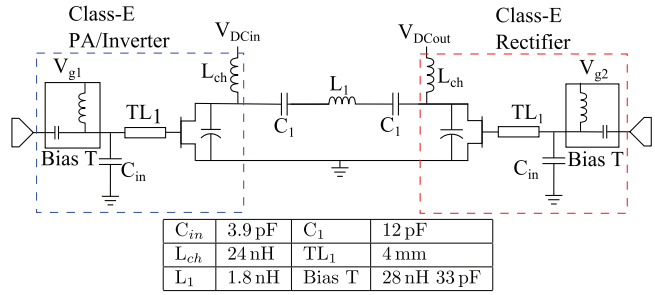


Fig. 2. Circuit schematic for class-E² converter consisting of a class-E PA and rectifier coupled through a resonant network.

the inverter stage, and a dual-diode rectifier stage. Recently, a 1.2-GHz GaN converter demonstrated 75% efficiency at 5 W [11].

In this paper, we extend the concepts from [11] to two types of self-synchronous dc–dc converters implemented with GaN microwave transistors in hybrid circuits using a combination of distributed and lumped elements. The designs are based on a resonant class-E^2 converter, first introduced in [12]. Fig. 1 illustrates the different converter topologies developed in this work, which are: (a) a synchronous topology; (b) a self-synchronous topology with a single RF input at the inverter input; and (c) a oscillating self-synchronous topology with no RF inputs.

This paper is organized as follows. Section II presents the design and measured results for the well-known synchronous operation [9], [11], [12], implemented with GaN devices at 1.2 GHz. Section III develops a simplified theoretical analysis, as well as nonlinear harmonic-balance simulations of self-synchronous rectifiers using microwave GaN transistors. The measured results at 1.2 GHz are shown to be comparable to the synchronous version, but eliminate an entire RF part of the circuit. Section IV presents a slightly lower frequency converter (900 MHz) with no RF inputs. In this circuit, the inverter is an RF oscillator, and the rectifier is self-synchronous. The efficiency of this converter reaches nearly 80% with over 10 W of output dc power.

II. Synchronous Class-E Operation

Well-known class-E PA design equations for the maximum frequency of operation and the class-E load presented at the virtual drain of the device are given by [13]

$$f_{\max} = \frac{I_{\rm DS}}{2\pi^2 C_{\rm out} V_{\rm DS}} \tag{1}$$

$$Z_{\rm net} = \frac{0.28015 e^{j49.0524^\circ}}{\omega_s C_{\rm out}} \tag{2}$$

where $C_{\rm out}$ is the total output capacitance seen at the drain, ω_s is the input drive frequency (or switching frequency), and $I_{\rm DS}$ is the maximum dc current for a drain biasing voltage $V_{\rm DS}$. Using the estimated value of $C_{\rm out} = 2.7$ pF for the T2G6001528-Q3 pseudomorphic HEMT (pHEMT) from TriQuint Semiconductor, $V_{\rm DS} = 18$ V and $I_{\rm DS} = 1.4$ A in (1), a maximum switching frequency of approximately 1.5 GHz is obtained. In order to account for additional parasitic capacitance and operate the class-E PA without sacrificing too much output power while maintaining a high switching frequency, a more conservative operating frequency of 1.2 GHz is chosen. The impedance to be synthesized by the matching network is calculated to be $Z_{\rm net} = 9 + j10.4\ \Omega$ from [13]. As described in [14], the rectifier provides the correct value of $\Re\{Z_{\rm net}\}$ and the reactances presented to the amplifier and the rectifier can be combined into one, resulting in $j20.8\ \Omega$. To synthesize $Z_{\rm net}$ at f_s and provide an open circuit at $2f_s$ and $3f_s$, the approach of [8] is adopted. The parasitic capacitance of a series inductor L_1 in Fig. 2 provides an approximately open circuit at $2f_s$ and $3f_s$ when the self resonance (SRF) is between the two harmonics, while a series capacitor C_1 tunes the impedance at the fundamental.

To maintain a flat low circuit profile, only passive components with a maximum thickness of 2 mm are used. With this restriction, inductors from Coilcraft's 0603HP series and capacitors from ATC's 600L and 600S series are chosen. The inter-stage network is simulated using NI/AWR Microwave Office (MWO) with high-frequency models for the passive components provided by Modelithics. The design is implemented on a 30-mil Rogers RO4350B substrate, and a photograph of the prototype is shown in Fig. 3.

The converter is characterized as shown in Fig. 4. The PA is biased at a quiescent current of 10 mA for input voltages ranging from 12 to 27 V, and the rectifier is pinched off. $R_{\rm DC}$ is implemented using a BK Precision 8500 electronic dc load in a constant voltage mode enforcing output voltages ranging from 10 to 27 V. All the measurements are performed with $P_{\rm in} = 23$ dBm. The phase shift is adjusted for synchronous operation. Fig. 5 shows the efficiency and output power as a function of output voltage for 13, 17, and 27 V. The efficiency of the converter is defined as

$$\eta_{\rm DC-DC} = \frac{V_{\rm DCout} I_{\rm DCout}}{V_{\rm DCin} I_{\rm DCin}}. \tag{3}$$

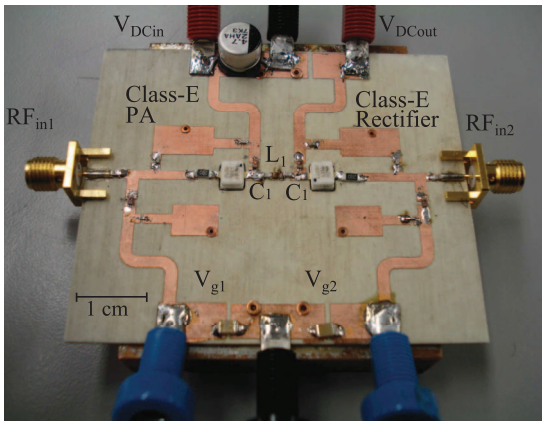


Fig. 3. Photograph of class-E^2 converter prototype. The left side of the circuit is the class-E inverter and the right side is a synchronous rectifier. They are coupled through the reactive network consisting of $L_1 = 1.8$ nH and $C_1 = 12$ pF.

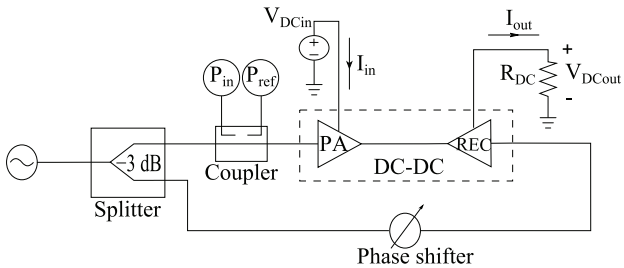


Fig. 4. Setup used to characterize the class-E^2 converter prototype. The output voltage is enforced by the electronic load while the current is allowed to be set by the converter itself.

As expected, the output power in Fig. 5 increases with input voltage, while the efficiency of the converter decreases with increasing input and output voltage.

III. Self-Synchronous Rectifier Analysis and Operation

A number of recent publications show experimentally that at microwave frequencies, a transistor rectifier can be operated without the need of an RF input, referred to as self-synchronous operation [15]–[18]. This is mainly enabled by the drain-to-gate feedback capacitance $C_{\rm gd}$. In a rectifier, the transistor operates in the third quadrant of its *I–V* curve [17], which is usually not taken into account in commercial nonlinear transistor models, making simulation impossible or unreliable.

A. Theoretical Analysis of Self-Synchronous Rectifier

The goal of this analysis is to determine the theoretical value of the gate impedance Z_g that satisfies self-synchronous class-E rectification. Fig. 6 shows a simplified intrinsic model for an HEMT transistor [19]. When the transistor is pinched off, the two diodes can be approximated as open circuits. This is true when the dynamic load line keeps $v_{\rm gs}$ and $v_{\rm gd}$ below the forward-bias knee value. To investigate a class-E self-synchronous rectifier, the idealized circuit shown in Fig. 7 is considered. It assumes a sinusoidal input current source driving an ideal switch. The input current includes a negative dc term representing the rectified dc output current.

The conditions for soft-switching class-E rectifier operation are $v_{\rm sw}(0) = 0$, $dv_{\rm sw}/dt(0) = 0$, and $v_{\rm sw}(T_s/2) = 0$. For simplicity, the class-E time-reversed waveform [14], [20] is assumed across the switch, which can be expressed using the formulation in [13] as

$$v_{\rm sw}(t) = \begin{cases} -\dfrac{I_{\rm dc}}{C_{\rm out}\omega_s}[a\cos(\omega_s t+\phi)+\omega_s t - a\cos(\phi)], \\ \qquad 0 \le t \le \dfrac{T_s}{2} \\ 0, \qquad \dfrac{Ts}{2} \le t \le Ts \end{cases} \tag{4}$$

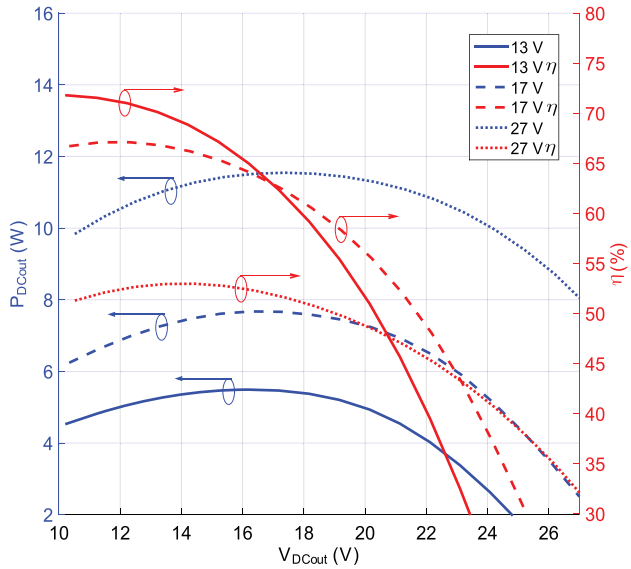


Fig. 5. Measured converter efficiency (red) and output power (blue) plotted as a function of output voltage for input voltages of 13, 17, and 27 V.

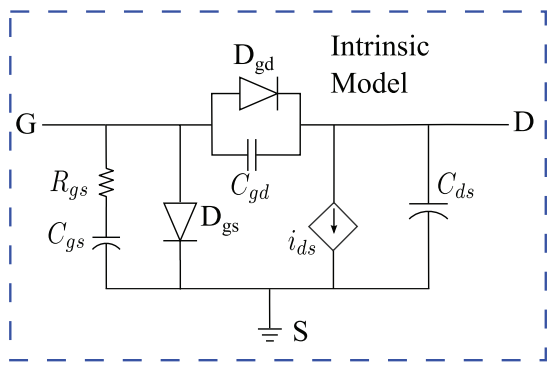


Fig. 6. Simplified intrinsic model of a GaN HEMT. Diodes $D_{\rm gd}$ and $D_{\rm gs}$ are modeled as open circuits for self-synchronous analysis.

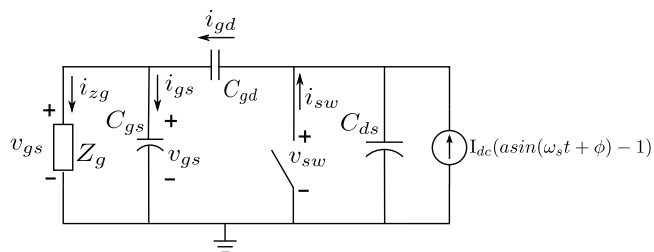


Fig. 7. Simplified switch model for class-E self-synchronous conditions. The switch is assumed to be ideal with $R_{\rm on} = 0$ and $R_{\rm off} = \infty$. $v_{\rm sw}$ is assumed to be an ideal class-E waveform and $v_{\rm gs}$ is approximated as a sinusoid. The unknown impedance Z_g is found under these conditions.

where $C_{\rm out}$ represents the equivalent output capacitance when the switch is off. The constants a and ϕ are found as in [13] to be 1.862° and 32.48°, respectively. In addition to the classic class-E boundary conditions, for the rectifier to operate self-synchronously, the voltage across $C_{\rm gs}$ should be less than the turn-off voltage of the transistor during the interval $0 \leq t \leq T_s/2$ and greater than the turn-on voltage of the transistor during the interval $T_s/2 \leq t \leq T_s$. A simple approximation for $v_{\rm gs}$ is the following:

$$v_{\rm gs}(t) = -V_0 \sin(\omega_s t) \tag{5}$$

where the switch is off for $v_{\rm gs} \leq 0$, and on for $v_{\rm gs} > 0$. From Fig. 7, the current $i_{\rm gd}$ through capacitor $C_{\rm gd}$ can be written as

$$i_{\rm gd}(t) = C_{\rm gd} d\frac{(v_{\rm sw} - v_{\rm gs})}{dt} = C_{\rm gd}\left(\frac{dv_{\rm sw}}{dt} - \frac{dv_{\rm gs}}{dt}\right). \tag{6}$$

Kirchoff's current law results in

$$i_{\rm gs} + i_{zg} = i_{\rm gd}. \tag{7}$$

When the switch is off, following (4)–(7), we obtain

$$i_{zg}(t) = C_{\rm gd}\Bigg[-\frac{I_{\rm dc}}{\omega_s C_{\rm out}}\{\omega_s - a\omega_s \sin(\omega_s t + \phi)\} + V_0\omega_s \cos(\omega_s t)\Bigg] + C_{\rm gs}V_0\omega_s \cos(\omega_s t). \tag{8}$$

When the switch is on, the voltage across the switch is 0, but the voltage across $C_{\rm gs}$ is not, hence the voltages across $C_{\rm gs}$ and $C_{\rm gd}$ are the same and (6) significantly simplifies. Following the previous procedure, during the interval $T_s/2 \leq t \leq T_s$, i_{zg} is found to be

$$i_{zg}(t) = (C_{\rm gd} + C_{\rm gs})\omega_s V_0 \cos(\omega_s t). \tag{9}$$

The unknown load Z_g can now be found from the voltage $v_{\rm gs}$ and i_{zg}. It is easier to start with the interval when the switch is on. Since the current $i_{zg}(t)$ from (9) lags the voltage from (5) by $\pi/2$, it is safe to assume that Z_g has to be inductive. To find the required equivalent inductance that imposes a class-E self-synchronous rectification, the current–voltage relationship is

$$v_{\rm gs}(t) = L_g(C_{\rm gd} + C_{\rm gs})\frac{d(\omega_s V_0 \cos(\omega_s t))}{dt} = -V_0 \sin(\omega_s t). \tag{10}$$

Solving for L_g,

$$L_g = \frac{1}{(C_{\rm gs} + C_{\rm gd})\omega_s^2} \tag{11}$$

which is the inductance required to resonate $C_{\rm gd}$ and $C_{\rm gs}$ in parallel. The L_g value in (11), however, would short the output capacitance during the OFF-state, leading to a zero voltage across the switch. Resonating $C_{\rm gs} + C_{\rm gd}$ at a slightly higher frequency would ensure a finite $C_{\rm out}$ and the desired class-E operation. Therefore, the idealized theoretical analysis gives the designer a starting point for choosing the gate termination for class-E synchronous rectification.

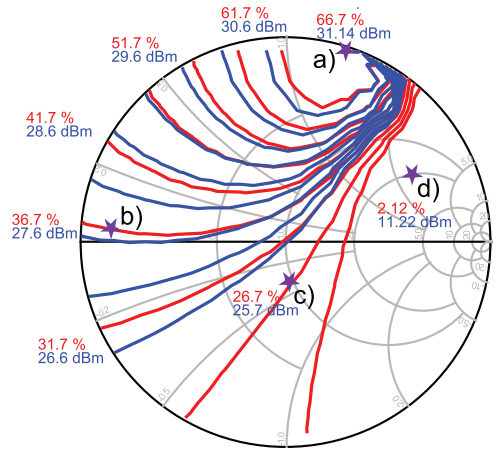


Fig. 8. RF–DC efficiency contours (red) and dc output power contours (blue) obtained in a load–pull simulation preformed at the gate port of a class-E self-synchronous rectifier using an improved nonlinear GaN HEMT model [21]. Results are obtained under a $V_{\rm gs} = -4$ V bias, $R_{\rm DC} = 90\ \Omega$, and an input power of 33 dBm (2 W). Impedance points a)–d) correspond to the impedance at the gate port for the dynamic load lines presented in Fig. 9.

B. Nonlinear Model Simulations

To validate the above simplified analysis, ADS simulations of a semi-ideal class-E rectifier using harmonic balance are performed. An improved 8×75 μm GaN HEMT model presented in [21] that accurately models $C_{\rm gs}$, $C_{\rm ds}$, $C_{\rm gd}$, and the third quadrant of the transistor's I–V curve is used in the simulations. The model used in the simulations does not correspond to the GaN HEMT used in the design of the class-E^2 converter shown in Fig. 3. The simulation involves ideal bias-tees and an ideal tuner presenting an open circuit at $5f_s$, $4f_s$, $3f_s$, and $2f_s$ and the impedance given by (2) at f_s for $C_{\rm ds} = 0.202$ pF and $f_s = 1.2$ GHz. The dc load $R_{\rm DC}$ is set equal to 90 Ω and the transistor is biased in pinch off with $V_g \approx -4$. V. A load–pull was performed at the gate port of the rectifier to find the impedance Z_g that achieves maximum RF–dc convertion efficiency and maximum output power for an input power of 33 dBm (2 W). The optimum impedance is found to be approximately $j89.46\ \Omega$, which represents the reactance of a 11.9-nH inductor at 1.2 GHz. Fig. 8 shows the dc output power (blue) and efficiency (red) contours resulting from the simulated load–pull. The maximum efficiency is 66.7% with a dc output power of 31.14 dBm. Fig. 9 shows the dynamic load line for the respective impedance points a)–d) marked in Fig. 8.

The contours and the dynamic load lines clearly illustrate how the performance of the rectifier diminishes as the equivalent reactance presented to the input of the GaN HEMT fails to approximately resonate $C_{\rm gs} + C_{\rm gd}$. Impedance a) in Fig. 8 is the optimum impedance that minimizes power dissipation by approximating an ideal diode, as shown in Fig. 9(a). When the transistor is off and the voltage $v_{\rm ds}$ swings positively, the transistor should block the voltage and operate on the $I_{\rm ds} = 0$ region along the V_d axis. To ensure this, $v_{\rm gs}$ swings deeper into the pinch-off region as $v_{\rm ds}$ increases. As $v_{\rm ds}$ decreases toward 0 due to the resonant nature of the output network, $v_{\rm gs}$ increases and approximates the operating (I–V) characteristics of an ideal conducting diode near the I_d axis in the third quadrant. As the

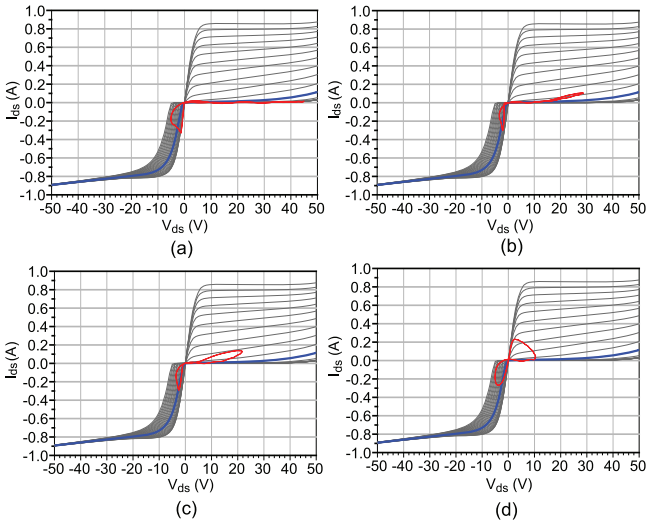


Fig. 9. Simulated dynamic load line (red) corresponding to impedance points a)–d) in Fig. 8. The blue line shows the *I*–*V* curves for the quiescent bias ($V_g = -4$ V).

impedance gets farther away from the equivalent reactance necessary to approximately resonate $C_{\rm gs}+C_{\rm gd}$, more power is dissipated because the transistor momentarily conducts when the switch should be off, as shown in Fig. 9(b)–(d). The performance degrades as the impedance resonates $C_{\rm gs}$ and $C_{\rm gd}$ below f_s, as in Figs. 8(d) and 9(d). Thus, the impedance presented to the gate should resonate at a slightly higher frequency than f_s, as discussed in Section III-A and (11), as well as to account for nonlinearities of $C_{\rm gs}$ and $C_{\rm gd}$.

For the simulated design, $C_{\rm gs}$ is highly nonlinear with a profile plotted in Fig. 10. $C_{\rm gd}$ also varies as a function of $v_{\rm gs}$ from a minimum of $\approx$ 0.17 pF at $v_{\rm gs} = -10$ V to a maximum of $\approx$ 0.47 pF at $v_{\rm gs} \approx 1$ V. Using the maximum value of those two capacitances and the equivalent inductor presented by the optimum impedance, the resonant frequency f_r is

$$f_r = \frac{1}{2\pi\sqrt{(0.47\ \text{pF}+0.95\ \text{pF})(11.9\ \text{nH})}} = 1.22\ \text{GHz} \quad (12)$$

which is only slightly larger than the switching frequency of 1.2 GHz. It is important to note that as the two nonlinear capacitances change with $v_{\rm gs}$, the presented impedance will always resonate at a higher frequency than the switching frequency.

Fig. 11 shows the time-domain waveforms at the intrinsic drain and at the intrinsic gate of the transistor for varying input powers (4–34 dBm) when the gate impedance is at point a) in Fig. 8. The waveforms show approximate class-E current and voltage waveforms at the intrinsic drain minimizing current and voltage overlap as well as the corresponding voltage and current across the input capacitor $C_{\rm gs}$. The voltage $v_{\rm gs}$ simulated in Fig. 11(a) approximates the sinusoidal voltage assumed in (5). Fig. 12 shows the dynamic load lines for the corresponding power levels of Fig. 11, which approximate behavior of an ideal diode.

C. Class-E^2 DC–DC Converter With Self-Synchronous Rectifier

In order to implement a self-synchronous rectifier in the class-E^2 converter, a load–pull is performed at the gate port

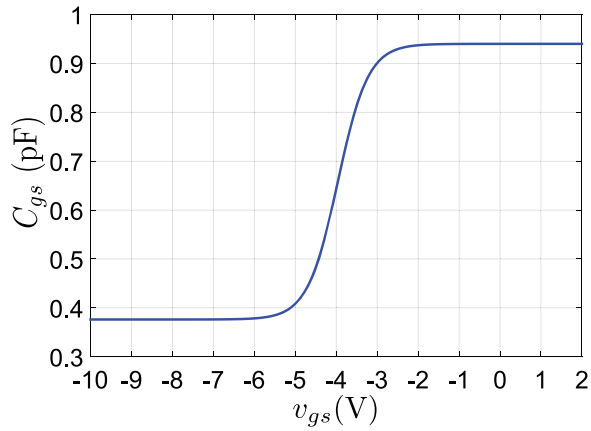


Fig. 10. Simulated nonlinear capacitance $C_{\rm gs}$ as a function of $v_{\rm gs}$ for the 8 × 75 μm GaN HEMT model [21] used in Section II.

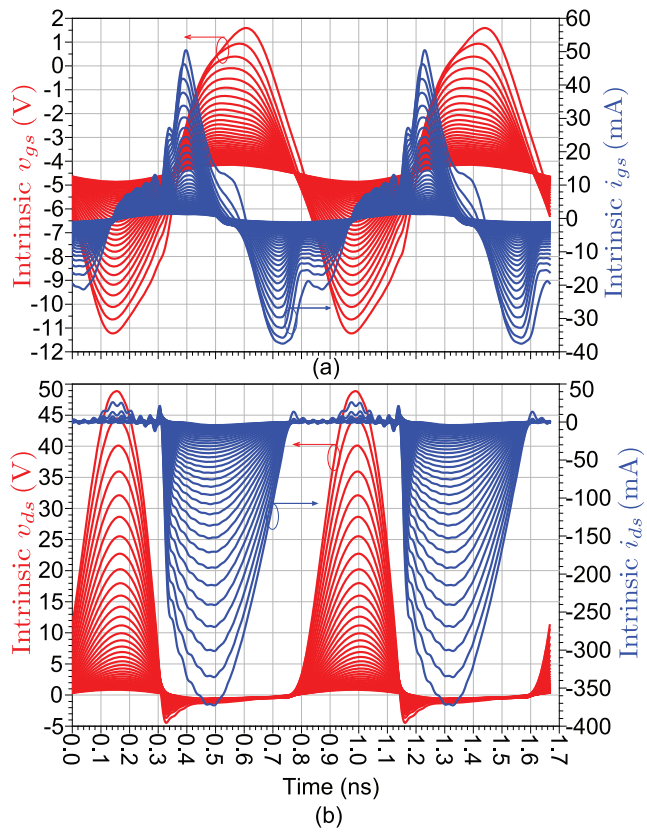


Fig. 11. Time-domain waveforms of class-E rectifier. Voltage and current waveforms at: (a) intrinsic gate and (b) intinsic drain. Waveforms are shown for input powers varying from 0 to 35 dBm in dB steps.

of the rectifier for maximum efficiency at an input voltage of 13, 17, and 27 V. The optimum impedance is not significantly affected by the output voltage. The results for 17 V are plotted in Fig. 13 with the optimum impedance found to be approximately $3.7 + j44.3\ \Omega$ at the connector reference plane.

A length of transmission line and an 8-pF shunt capacitor to ground are used to present this impedance to the transistor. The equivalent input capacitance of the transistor is estimated using a nonlinear model to be $\approx$ 8.5 pF. Following the theory presented in this paper, the impedance that the matching network

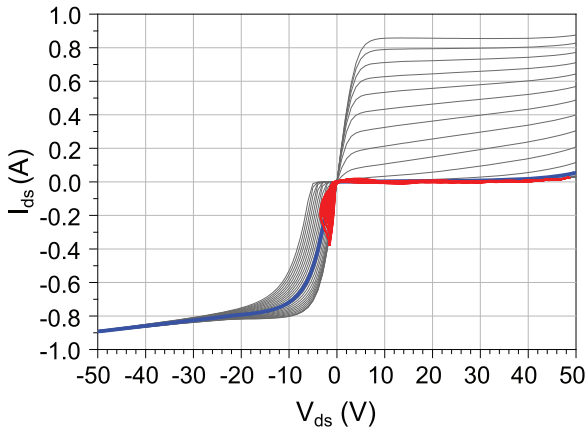


Fig. 12. Simulated dynamic load line (red) and *I–V* curves of quiescent bias (blue) for class-E self-synchronous rectifier for an input power range of 0–35 dBm with Z_g resonating equivalent input capacitance at 1.22 GHz. As expected, the transistor minimizes power dissipation and approximates an ideal diode.

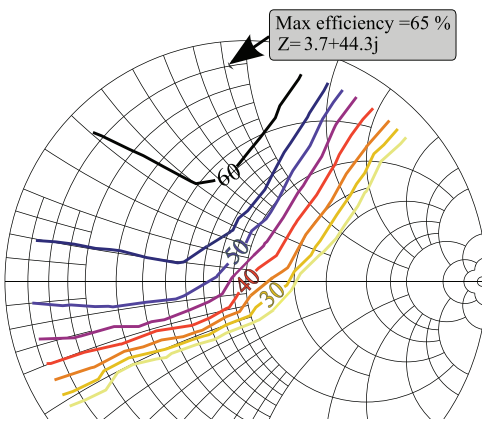


Fig. 13. Impedance constellation and efficiency contours produced by a load–pull performed at the gate port of the rectifier for maximum efficiency for a dc output voltage of 17 V. The Smith chart is normalized to 50 Ω.

of the rectifier presents to the input of the transistor should resonate the 8.5 pF a little bit above the switching frequency of 1.2 GHz. Fig. 14 plots an electromagnetic (EM) simulation of this impedance and the impedance of an ideal 2.07-nH inductor necesary to resonate the 8.5 pF at 1.2 GHz. Fig. 14 clearly shows the impedance of the matching network follows that of the inductor, supporting the theory.

A prototype of a self-synchronous converter is shown in Fig. 15. The converter is characterized following the previously described procedure without the need of a second RF driver for the rectifier. Fig. 16 shows the efficiency and output power as a function of output voltage for 13, 17, and 27 V. The results are improved compared to those of Fig. 5. The converter is the most efficient at 13-V input voltage and at lower output voltages in general, achieving an efficiency above 70% for output voltages ranging from 11 to 17 V, with a maximum efficiency of 75% and 4.6 W compared to the 72% efficiency of the converter from Section II. The improvement can be attributed to a shift in the value of the passive components used in the resonator, specifically the inductors that have a ±5% tolerance.

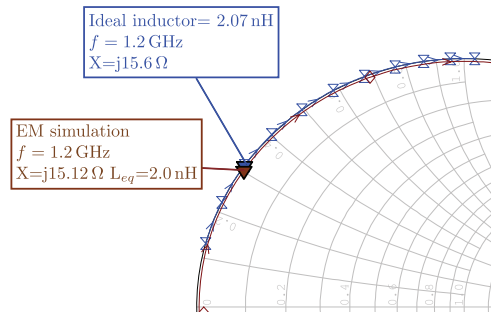


Fig. 14. Comparison between the impedance presented by the rectifier's input matching network EM simulated (brown) and the ideal 2.07-nH inductor (blue) required to resonate the 8.5-pF input capacitance of the T2G6001528 transistor model. The figure shows the impedance of the matching network closely follows the impedance of the ideal inductor around the switching frequency.

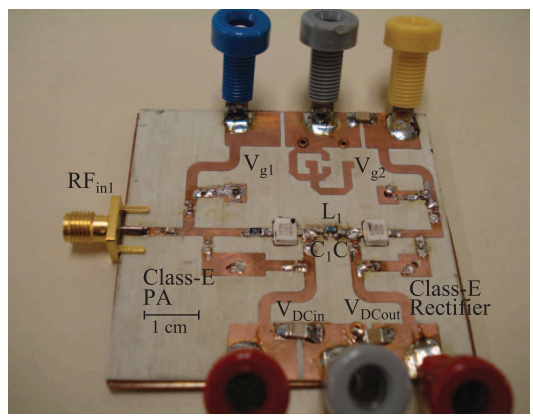


Fig. 15. Photograph of class-E^2 converter with the rectifier operating self-synchronously. The RF port at the gate of the rectifier is removed and the input matching network is modified to present the optimum impedance to the rectifier. The size of the circuit board is 5.6 cm × 6 cm.

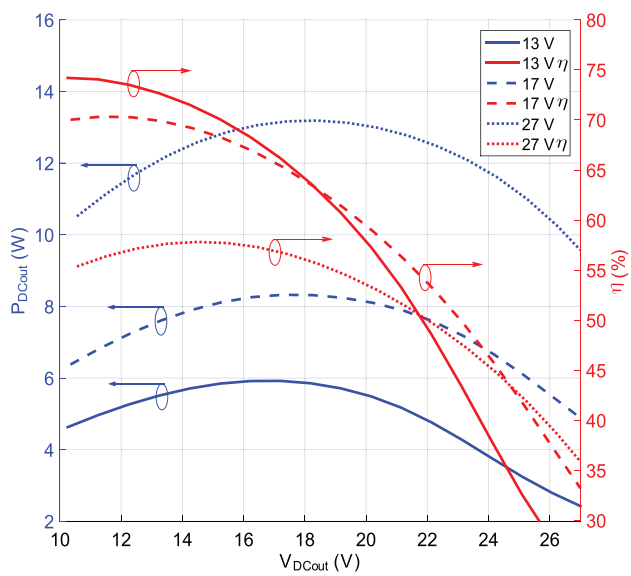
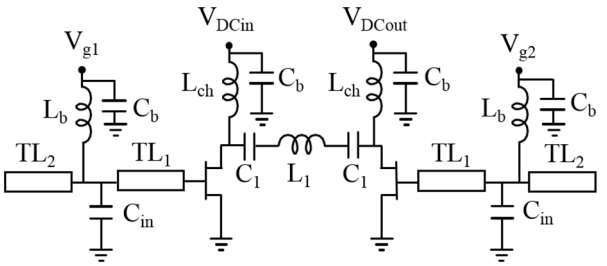


Fig. 16. Measured self-synchronous class-E^2 converter efficiency (red) and output power (blue) as a function of output voltage for input voltages of 13, 17, and 27 V.



C_{in}	L_{ch}	L_b	C_b	C_1	L_1	TL_1	TL_2
12 pF	12.5 nH	120 nH	27 pF	10 pF	8 nH	10 mm	18 mm

Fig. 17. Circuit schematic for self-oscillating self-synchronous class-E^2 dc–dc converter.

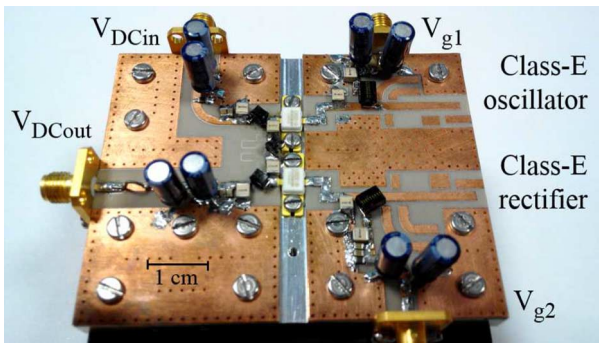


Fig. 18. Photograph of oscillating self-synchronous class-E^2 dc–dc converter.

IV. Oscillating Self-Synchronous Operation of Class-E^2 Converter

Turning the PA of the converter into a free-running power oscillator becomes a logical highly desirable step toward a self-driving microwave frequency resonant dc–dc converter, as in Fig. 1(c), eliminating the RF input. A similar MOSFET 2-MHz converter was published in [22] using a class-E oscillator design procedure introduced in [23]. The converter achieved 78.9% under 1.55-W output power using a feedback inductor to force the oscillation of the class-E inverter. In [10], a sub-watt 4.6-GHz class-E oscillator was demonstrated with a diode rectifier. In this section, we demonstrate the architecture of Fig. 1(c) in a class-E^2 GaN dc–dc converter operating around 900 MHz.

In Fig. 17, the circuit schematic for the implemented oscillating self-synchronous class-E^2 converter, based on the CGH35030F packaged GaN HEMT from Cree Inc., is presented. The change to a higher power device and lower frequency allows for higher output power and efficiency and demonstrates feasibility of the approach. The design procedure is very similar to the one described in Section I and is described in [9]. In order to interconnect the inverting and rectifying devices, an inductor L_1 and two capacitors C_1 are employed. Harmonic terminations at f_2 and f_3 are achieved as previously discussed through the self-resonance of L_1, while the choice of C_1 allows for reactance adjustment at the fundamental. An open-circuit stub (TL_2), a high-value capacitor to ground (C_{in}), and a length of transmission line (TL_1) are combined in order to synthesize the required gate impedance condition at the fundamental to operate the rectifier self-synchronously. The simplified theoretical analysis from Section III can be applied to the class-E oscillating inverter with some modifications. Substituting the current source in Fig. 7 by $I_{\mathrm{DC}}(1-a\sin(\omega_s t+\phi))$ to account for the dc current supplied to the inverter, (4) becomes

$$v_{\mathrm{sw}}(t)=\begin{cases}\dfrac{I_{\mathrm{dc}}}{C_{\mathrm{out}}\omega_s}[a\cos(\omega_s t+\phi)+\omega_s t-a\cos(\phi)], \\ \qquad 0\le t\le\dfrac{T_s}{2} \\ 0, \qquad \dfrac{Ts}{2}\le t\le Ts.\end{cases} \tag{13}$$

while (8) becomes

$$i_{zg}(t)=C_{\mathrm{gd}}\left[\frac{I_{\mathrm{dc}}}{\omega_s C_{\mathrm{out}}}\{\omega_s-a\omega_s\sin(\omega_s t+\phi)\}+V_0\omega_s\cos(\omega_s t)\right]+C_{\mathrm{gs}}V_0\omega_s\cos(\omega_s t). \tag{14}$$

The remaining equations remain unchanged. However, solving for a and ϕ results in 1.862° and -32.48°, respectively. These correspond to the time-reversed waveforms of the class-E rectifier as in [13]. Since (11) remains unchanged, the conclusions obtained from Section III apply to the class-E oscillator as well. Hence, the impedance presented to the gate of the transistor should correspond to an equivalent reactance capable of resonating $C_{\mathrm{gs}}+C_{\mathrm{gd}}$ at a frequency slightly above the switching frequency to ensure the desired class-E soft-switching operation. For that reason, a gate matching network mirroring that of the self-synchronous rectifier was implemented in Fig. 17. A photograph of the oscillating self-synchronous converter is shown in Fig. 18. The oscillator gate biasing voltage is used to initiate the oscillation by increasing the voltage above pinch-off. Once the oscillation starts, the voltage is lowered to a value approximately equal to that of the self-synchronous rectifier, where the maximum efficiency can be obtained [24].

The converter is characterized in a modified setup of the one shown in Fig. 4; the main difference is the absence of any RF input source. The electronic load providing a constant dc output voltage is changed to a passive 50-Ω load due to lower frequency oscillations produced by the electronic load. The rectifier was biased in pinch off ≈ -4.0 V, while the bias of the oscillator was increased until an oscillation is produced at around -3 V. Fig. 19 shows efficiency and dc output power for input voltages of 28, 22, and 17 V, as a function of output voltage. The oscillating self-synchronous converter can only operate as a buck converter since the oscillations subside when the output voltage becomes higher than the input voltage, and hence, more attention was given to higher input voltages. The converter is 79% efficient at an input voltage of 28 V and an output power of 12.8 W. As expected, output power is directly proportional to input voltage, but efficiency is maintained above 70% for an input voltage range of 11–28 V.

Output voltage control can be accomplished by frequency modulation (FM) through the oscillator's gate biasing voltage, due to the input capacitance C_{gs} variation with v_{gs} in a GaN

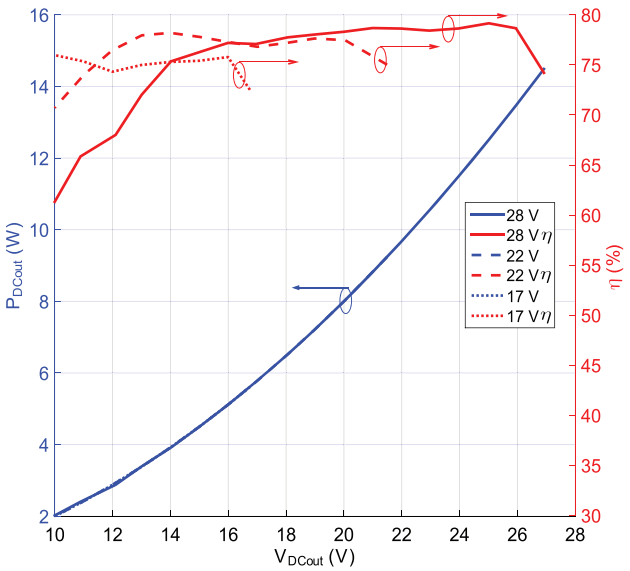


Fig. 19. Measured performance of oscillating self-synchronous class-E^2 dc–dc converter. Converter efficiency (red) and output power (blue) plotted as a function of output voltage for input voltages of 17, 22, and 28 V.

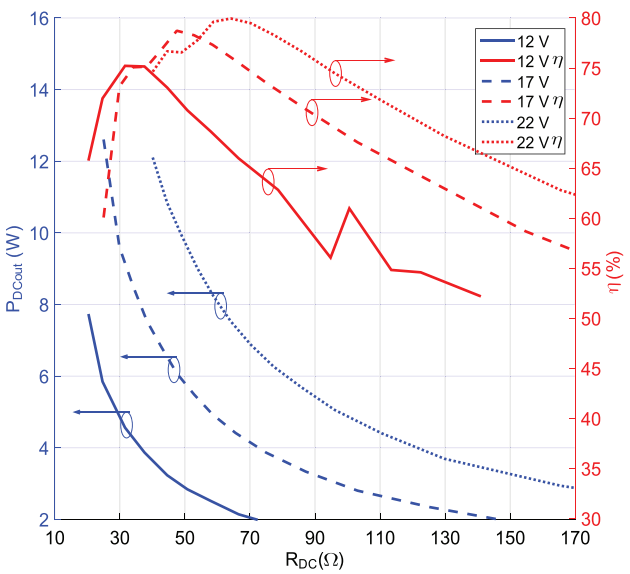


Fig. 20. Measured performance of $V_{\rm out}$ control through V_{g1} for oscillating self-synchronous converter. Input voltage is 28 V while output voltage is adjusted to 12, 17, and 22 V.

HEMT, as shown in Section III. This dependence can be exploited to control the output voltage of the converter for varying loads. When $V_{g1} = -3$ V, the frequency of oscillation starts around 920 MHz, and increases as the voltage decreases. At $V_{g1} = -6.4$ V, the oscillation disappears, reaching a frequency of 1040 MHz. The FM control is possible thanks to the detuning of the resonant interconnecting network, as is typical of class E^2 converters. Fig. 20 shows efficiency and output power as a function of $R_{\rm DC}$ when the output voltage is controlled through V_g to be 22, 17, and 12 V. FM presents a viable alternative for open or closed loop output voltage control, however, performance of the converter degrades at higher loads and lower voltages.

TABLE II
ESTIMATED LOSSES BASED ON SIMULATION

Total inverter transistor losses	49.0 %
OFF-ON tranistion	9.4 %
ON-OFF transition	10.4 %
Conduction losses	29.2 %
Total rectifier transistor losses	39.7 %
OFF-ON transition	11.3 %
ON-OFF transition	0.8 %
Conduction losses	27.6 %
Total passive components losses	8.4 %
Resonator	2.7 %
Inverter bias-T	3.1 %
Rectifier bias-T	2.6 %
Other losses	3.8 %

V. DISCUSSION AND CONCLUSION

In this paper, a series of microwave dc–dc converters that operate around 1 GHz switching frequency with efficiencies greater than 70% at greater than 5-W output power have been demonstrated. A loss budget for the oscillating self-synchronous converter has been given in Table II. The losses were estimated from simulations since it is difficult to measure the separate sub-circuits at gigahertz frequencies. The simulations were performed for $V_{\rm DCin} = 28$ V, $V_{\rm DCout} = 25$ V, a dc load of 24 Ω, and an operating frequency of 950 MHz. The converter was 80% efficient and the losses were distributed, as shown in Table II.

The biggest contributor to the dissipated power is the transistor's $R_{\rm ON}$ resistance for both the PA and the rectifier. Most of the losses in the passive elements came from power dissipated in the inductors. Estimated losses for the 1.2-GHz class-E^2 converter from Fig. 15 showed a similar distribution.

For the first time, an in-depth theoretical analysis of the operation of class-E self-synchronous transistor rectifiers has been derived. The idealized theoretical analysis has been validated with harmonic-balance simulations using an improved GaN HEMT nonlinear model. The procedure to design a self-synchronous rectifier by resonating the equivalent input capacitance slightly above the switching frequency provides the designer with a useful starting point for the design of a microwave dc–dc converter and self-synchronous rectifiers. The analysis has been validated for transistor rectifiers other than class-E, with some examples shown for a class-B circuit in [16] and a class F^{-1} circuit in [15]. Finally, the analysis has been extended to the design of a oscillating self-synchronous class-E^2 dc–dc converter. A oscillating self-synchronous Buck converter with no RF inputs has been demonstrated and characterized. The converter maintains an efficiency above 70% for input voltages of 11–28 V across a load of 50 Ω.

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