In-package Matching Network Validation for Improving Power Amplifier Performance

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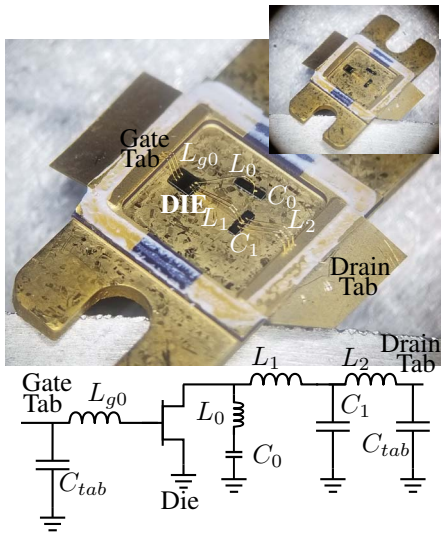
***Abstract*—The performance of RF and microwave transistors and MMICs can be significantly affected by parasitics presented by the package. This paper presents a technique to validate a package model by replacing the active device with a metal-oxide-semiconductor (MOS) capacitor of similar size and known value, allowing small-signal measurement of the full package. The technique is demonstrated with a 10-W Infineon LDMOS device at a fundamental frequency of 2.6 GHz, in a custom-designed package with both fundamental and 2^{nd} harmonic pre-match and termination impedances implemented within the package. Full-wave simulations allow accurate models of the passive elements above the 2^{nd} harmonic frequency.**

***Index Terms*—Package parasitics, LDMOS, harmonic terminations, matching network.**

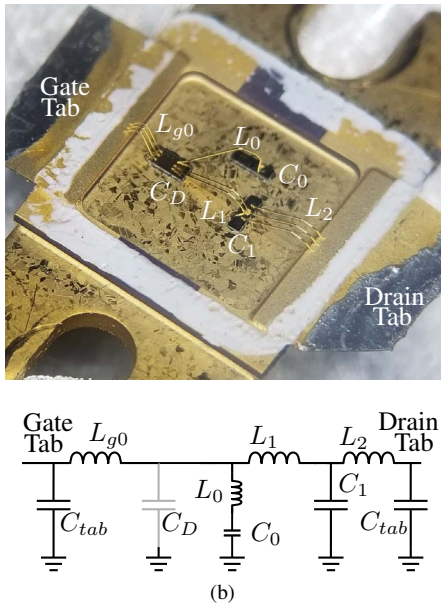
I. Introduction

Active microwave devices are often housed in metal-ceramic packages for better thermal dissipation, ease of circuit fabrication, power combining of multiple transistor cells (e.g. [1]), and mechanical and environmental ruggedness. However at RF and microwave frequencies, the package presents parasitic reactances that can adversely affect the electrical performance of the device, especially at harmonics of the intended operating frequency. Usually the package bond-wires and internal capacitors are designed for pre-matching or matching the device input and output at the fundamental frequency [2]. These impedance transformations, however, often do not consider and even significantly restrict harmonic impedances presented to the device. Bond-wires, MOS capacitors, and parasitics can be manipulated within the package to provide a more favorable 2^{nd} harmonic pre-match [3] or to provide a highly-reflective 2^{nd} harmonic termination [4] while also maintaining the appropriate fundamental pre-match. This requires accurate package modeling since bond-wire and MOS capacitor placement and geometry must be precise, as nicely addressed in [5–7].

Here we present a method for package model validation that includes harmonic frequencies. Fig.1a shows a standard package used by, e.g. Infineon, for a 10-W LDMOS transistor die. The circuit diagram shows three 50-μm diameter gold bond-wires at the input, which together with the tab capacitance provide some input pre-matching at the fundamental. On the output side, there are two MOS capacitors with bond wire connections, synthesizing a fundamental pre-match and a specific impedance at the harmonic. The transistor and package



(a)



(b)

Fig. 1. (a) Transistor package for an Infineon 10-W LDMOS device with a fundamental of 2.6 GHz. The package is custom designed for a fundamental pre-match and a 2^{nd} harmonic termination both internal to the package. (b) Passive validation package, where the active device is replaced by a capacitor of similar size and known value. Circuit diagrams are also shown, where the inductors represent bond-wires and the drain and gate tabs are represented by capacitors.

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together constitute a harmonically-terminated high-efficiency PA, where the PA performance is highly sensitive to the passive elements within the package [4].

Therefore, a multi-harmonic validation of the circuit component values in Fig.1a is necessary. In this paper, we demonstrate a validation method using a purely passive package, as seen in Fig.1b, where the transistor is replaced by a known capacitor.

An extensive broadband model for de-embedding a packaged transistor is validated by intrinsic and packaged device measurements in [1]. A validation method is discussed in [5], where the active device within the package is replaced by a pedestal, and small-signal measurements are compared with full-wave simulations. However, a pedestal constitutes a short to ground, presenting a highly-reflective impedance that limits the validation accuracy, particularly at higher frequencies (harmonics). In [8], the package environment is thoroughly modeled, not only electromagnetically but also thermally, and includes distributed effects. Although it is shown in [9] that distributed models more accurately represent in-package networks in small and large signal simulations, a lumped-element approach is adequate for the work presented here. This approximation is justified, since distributed effects along the transistor lateral dimension are minimal for the chosen 10-W die which consists of only a single unit cell.

II. In-Package Circuit Design

To determine the impedance that needs to be presented at the die reference plane for maximized power-added efficiency (PAE), a non-linear model of the device is used in harmonic balance simulations. The source and load impedances necessary to achieve a highly-efficient PA design at a fundamental of 2.6 GHz are shown in Fig. 2. The source impedance at the gate terminal is found to be $4.2 + j2.9\,\Omega$. The package consists of the parasitic tab capacitance (C_{tab}) and a source pre-match of $3 + j7.7\,\Omega$ is designed by placing the die edge 1 mm from the tab and using a set of three bond-wires (L_{g0}) with the shape and length shown in Fig. 1a. The simulated PAE loadpull contours at the fundamental and 2^{nd} harmonic are shown in Fig. 2, where the best PAE is achieved for a load impedance of $Z_L(f_0) = 4.4 + j11.7\,\Omega$, and $Z_L(2f_0) = 1.6 + j13.4\,\Omega$.

A lumped element circuit is next designed to achieve these desired impedances. The design constraints are: package size, parasitic tab capacitances, range and size of available MOS capacitors (0.3 to 15 pF), length of bond-wires corresponding to a range of 0.6 to 3 nH, minimum distance between two adjacent bond-wires (6 mil), and minimum distances from components to the walls of the package. The circuit topology with only shunt capacitances is next chosen to provide a termination at the 2^{nd} harmonic and enough degrees of freedom to obtain the loadpull impedance at the fundamental. An ideal circuit is then designed using available lumped element values, where inductances are obtained using full-wave simulations and adjusting bond-wire shape within manufacturing tolerances. After this initial matching circuit design, a full-wave HFSS

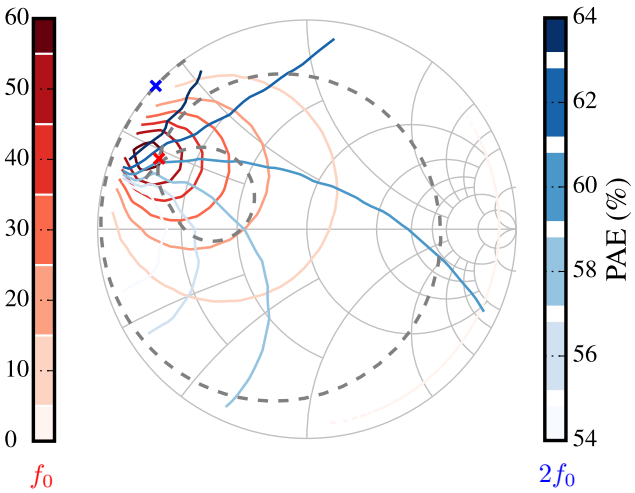

Fig. 2. Loadpull contours for constant PAE for varied fundamental (red scale) and 2^{nd} harmonic (blue scale) load impedance. The impedance presented to the device drain terminal by the in-package passive circuit from Fig. 1 over the 1 to 8 GHz frequency range is shown by the dashed gray trace, with the f_0 and $2f_0$ impedances indicated by the red and blue crosses, respectively.

simulation is performed to include mutual reactances, which in turn requires iteration in circuit element values.

During this process, the inductances are only placed in series (otherwise shorting DC current) and are tuned within a limited range since long bond-wires are difficult to realize. The circuit minimizes inductance since longer bond-wires present more resistive loss. Current handling of the package network must also be considered, therefore smaller series inductances are desired to allow multiple parallel bond-wires. The geometry of each bond-wire is manipulated along with the placement of the MOS capacitors and die within the package (considering manufacturing constraints) until full-wave simulations agree with the desired lumped-element model. The ANSYS HFSS full-wave simulated impedance presented at the device drain by the package design is shown in Fig.2 in dashed grey trace with the achieved impedances at the fundamental and second harmonic of $Z_L(f_0) = 6.4 + j11.2\,\Omega$, and $Z_L(2f_0) = 0.1 + j20\,\Omega$, within 95% of the values determined by load-pull.

A passive version of the in-package matching circuit is next designed with the active device replaced by a capacitor of similar size and known value (see Fig. 1b). A capacitance of 2.58 pF is chosen not only for its suitable dimensions but also because the resulting full-package S-parameters allow parasitics to become more noticeable. This is in contrast to e.g. a pedestal which presents effectively a short circuit and masks the effect of other reactances in the measured S_{21} and S_{11} of the circuit.

III. Full-Wave Simulations

Since the validation package is purely passive, the entire package can be simulated without the use of internal ports in Ansys HFSS, with the model shown in Fig.3. Wave ports

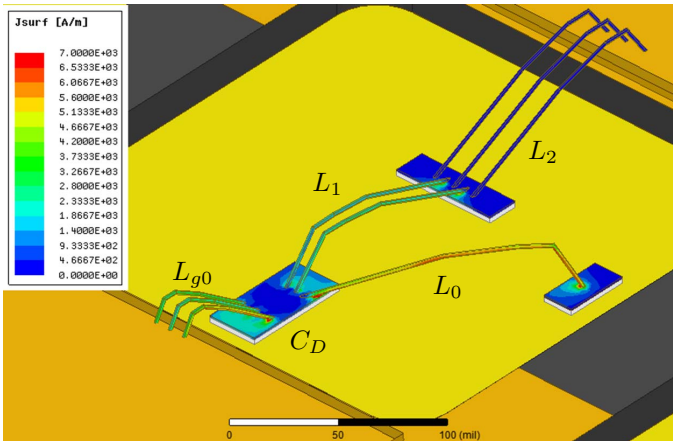

Fig. 3. HFSS model of the passive-only in-packaged matching circuit showing a plot of $2f_0$ of surface current magnitude along the bond wires and on the capacitor plates. The current along L_0 is pronounced (600 A/m), since it is responsible for the $2f_0$ drain termination. Notice that there is more current on the bond-wire closest to L_0 than the other bond-wire at that point in the network. This is due to mutual inductance.

are placed at the gate and drain tab edges and de-embedded to the package plane. The geometry is meshed relative to the electrical length at the 3^{rd} harmonic since the accurate knowledge of harmonic impedances is important for the design of an efficient PA. Full-wave simulations enable modeling of geometry effects such as angle between multiple connected electrically in parallel and varied lumped element and package heights

It is interesting to observe the surface current density magnitude at the second harmonic, shown in Fig. 3. The surface current density is high on the input bond wires to C_D, and progressively reduced in magnitude through the matching circuit. The current on the shunt inductor L_0 is pronounced since this is the second harmonic termination network, with a mean value of about 600 A/m for 10-W excitation at the input port (Gate). It also becomes obvious when looking at the asymmetric geometry of L_0 and L_1 that mutual inductance plays a role that cannot be neglected, especially at the second harmonic. The closer of the two wires of L_1 has a surface current mean value of about 250 while the further one is about 100 A/m, due to mutual inductance. Notice the practically negligible 2^{nd} harmonic current on L_2. The effect of mutual inductance and mutual capacitance is next taken into account when comparing with measured data.

IV. Experimental Validation

The passive package is placed into a microstrip fixture that tapers from the 280-mil wide lead to a 50 Ω environment, as shown in Fig.5. Thru-Reflect-Line (TRL) calibration is performed on the fixture to de-embed the measured S-parameters to the package plane. The simulated response of the circuit in Fig. 1b compared well with measurements at the fundamental but shows significant discrepancy at higher frequencies, pointing to the need of including mutual reactances. The most significant coupling is between bond-wires L_0 and L_1 as well

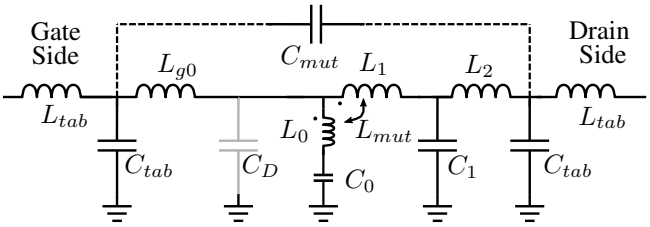

Fig. 4. Equivalent circuit model of passive package shown in Fig. 1b. The active device in Fig. 1a is replaced by a capacitor C_D of similar size and known value, represented by capacitor C_D in grey.

TABLE I
Circuit Model Element Values

L_0	L_{g0}	L_1	L_{mut}	L_{tab}	L_2
2.0 nH	1.1 nH	0.8 nH	0.31 nH	0.13 nH	1.4 nH
C_0	C_1	C_D	C_{mut}	C_{tab}	
0.78 pF	7.11 pF	2.58 pF	0.1 pF	5.6 pF	

as capacitive coupling between package tabs. The circuit was modified to include these mutual reactances as shown in Fig. 4, and L_{mut} and C_{mut} tuned to match measurement. Table I shows the resulting element values.

It is of interesting note that the mutual inductance L_{mut} between bond wire(s) L_0 and L_1 are significant since the coupling between them is a function of magnetic flux, which is in turn a function of the distance and angle between them. Therefore a mutual inductance between the two different sets of bond-wires is to be expected, since L_0 is large and is rotated 45° relative to L_1. The element C_{mut} is also not negligible.

Fig. 6 shows the results of measured example S-parameters compared to two simulations: the circuit model from Fig. 1b which does not include mutual reactances and the more complete circuit model from Fig. 4 obtained from full-wave simulations. The amplitude of the input reflection coefficient shows reasonable agreement with the simpler circuit up to

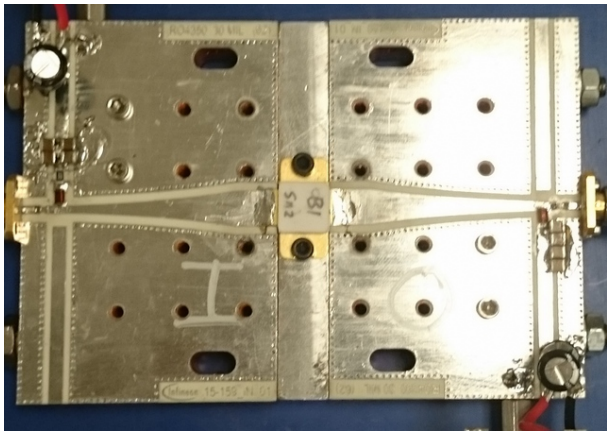

Fig. 5. Microstrip fixture used for TRL calibration and measurement of the validation package. The package is mounted on a 280-mil wide microstrip line and tapered to a 50 Ω environment. Bias-tees are integrated into the fixture anticipating large-signal measurements with the active package but are not necessary for the validation process.

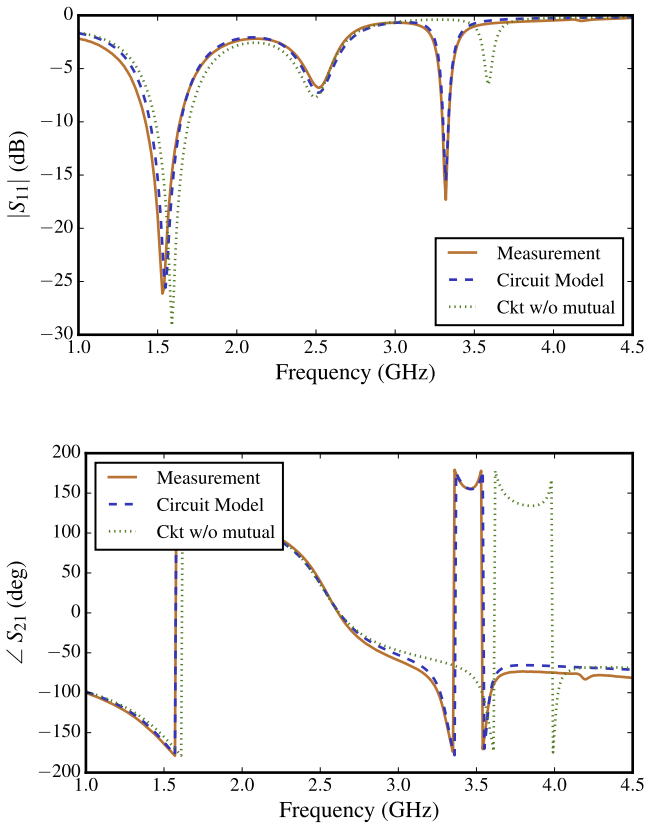

Fig. 6. Measured (solid line) vs. simulated (dashed line) S-parameters of the equivalent package circuit model from Fig.4. The elements C_{mut} and L_{mut} are omitted from this circuit model and also plotted (dotted line) to illustrate the distinct impact of these values on the impedance presented to the packaged device.

slightly above the fundamental frequency of 2.6 GHz while there is significant discrepancy above 3 GHz. Similarly, the phase of the transmission coefficient cannot be predicted with a simpler model above 3 GHz which will critically affect harmonically-terminated PA design.

V. Conclusion

In summary, this paper presents a technique to validate a transistor package model by replacing the active device with a metal-oxide-semiconductor (MOS) capacitor of similar size and known value, allowing small-signal measurement of the full package. Specifically, number, shape, and length of bondwires, specific values of shunt capacitors, and mutual reactances are determined to present precise complex impedance at the fundamental and 2^{nd} harmonic. The impedances are determined by transistor source and loadpull. The technique is demonstrated with a 10-W Infineon LDMOS device at a fundamental frequency of 2.6 GHz, in a custom-designed package with both fundamental and 2^{nd} harmonic pre-match and termination impedances implemented within the package. Full-wave simulations are shown to be essential to accurately model the passive elements above 3 GHz. The presented technique is an easy and straightforward experimental method that can be used to validate package design that performs more than just fundamental pre-matching.

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