Millimeter-Wave GaN Solid-State Arrays

by

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The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

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Millimeter-Wave GaN Solid-State Arrays

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Millimeter-wave applications above K_a-band have become increasingly important for both the military and commercial sector. With the overcrowded spectrum at lower microwave frequencies, more systems are demanding the use of unlicensed spectrum space at V-, W-band and beyond. Data communications for wireless links are requiring frequencies greater than 75 GHz to achieve high data rates up 80 Gbps. Scalable W-band phased arrays using silicon technology have been demonstrated for automotive radar, imaging and communication. Technologies such as Gallium-Nitride (GaN) have been pushing high-frequency performance with operating frequencies in the hundreds of GHz allowing the capability for solid-state high-power transmitters. General challenges for W-band high-power solid-state transmitters are achieving high effective radiated power (ERP) in a small footprint and with reasonable efficiency for space constrained applications. Recent advances in GaN technology with cutoff frequencies $f_t > 150$ GHz achieve power densities as high as 3 W/mm at W-band. For very high-power applications many amplifiers are required to be combined and fed into an array for spatially coherently power combining. The need for multiple levels of power combining provides a trade off in terms of combining efficiency, heat dissipation, volume and co-design from the transistor to the radiating aperture. Each power amplifier (PA) module can have varying levels of power combining including device level within a monolithic microwave integrated circuit (MMIC) amplifier, thin-film and waveguided power combining, and spatial power combining to achieve the desired ERP.

This thesis focuses on the design and analysis of millimeter-wave MMIC power amplifiers for high effective radiated power (ERP) using three GaN research processes in development by the industry. W-band PAs are presented and predict state-of-the-art output power. Analysis of power combining efficiency and degradation in power combiners and phased arrays caused by GaN-on-SiC semiconductor process variations is presented.

Dedication

Para Cecilia, Mauricio, y Catalina.

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Chapter 1

Introduction

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1.1 Background and Motivation

With the start of the Microwave and Millimeter-Wave Monolithic Integrated Circuits (MIMIC) Program funded through the Defense Advanced Research Project Agency (DARPA) in the late 1980's, extensive efforts began in the development of high-yield and low-cost III-V semiconductor technology, specifically GaAs monolithic microwave integrated circuits (MMIC) [8, 9]. Success in the program led to advancements in the infrastructure needed for MMIC computer aided design (CAD) software, integrated circuit fabrication, and testing up through 110 GHz. High performing 0.1 μm pseudomorphic InGaAs high electron mobility transistors (HEMT) process developed under the program allowed a path for millimeter-wave solid-state systems operating at W-band with various front-end MMICs [10, 11]. For example in [12], a passive millimeter-wave camera system demonstrated a first MMIC-based imaging system combining 1040 MMIC chips operating at 89 GHz with a $15^\circ \times 10^\circ$ field-of-view. These developments quickly found their place in

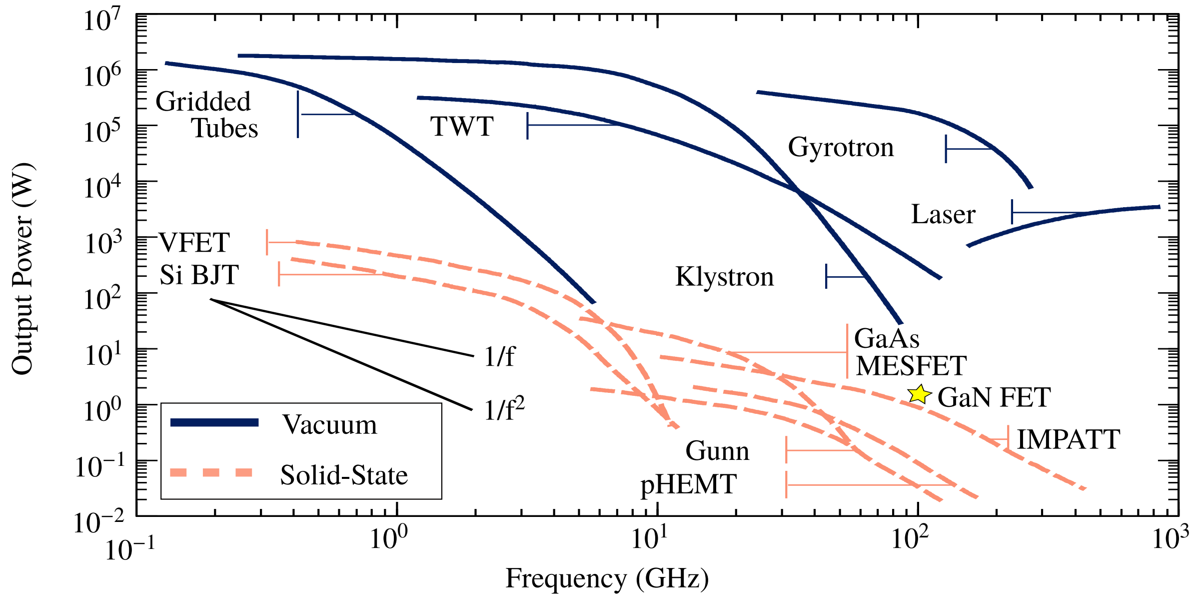

Figure 1.1: Output power for vacuum and solid-state sources versus frequency for various technologies. [2,3].

commercial and defense industry ranging from airborne and ground-based radars, satellite communications, to missile terminal guidance phase decoys, many of which still remain GaAs-based systems due to the robustness offered by the technology.

Due to the large success of the MIMIC Program, further government sponsorship led to the start of new programs targeting high transmitting solid-state power such as the Microwave and Analog Front-End Technology (MAFET) Program [13]. High-power microwave and millimeter applications requiring hundreds to thousands of watts required bulky vacuum tubes with the desire to close the power gap between vacuum and solid-state in Fig. 1.1. The program faced challenges in developing high-efficiency solid-state coherent power with reduced size, weight, power and cost (SWaP-C). The outcome brought forth new, innovative techniques in spatial power combining using GaAs technology where traditional binary corporate combining became limited by loss [14]. At 61 GHz, a 16×17 lens array using a total of 272 GaAs MMIC elements, achieved a total of 36 W [15].

1.1.1 Current Millimeter-Wave Applications

Millimeter-wave applications above K_a-band have become increasingly important for both the military and commercial sector. With the overcrowded spectrum at lower microwave frequencies, more systems are demanding the use of unlicensed spectrum space at V-, W-band and beyond, with for example V-band 5G allocations in the 57–64 GHz and 64–71 GHz unlicensed bands [16, 17]. High data rate communication systems operating at 92 GHz and achieving 6.5 Giga-bits-per-second (Gbps) with quadrature amplitude modulation (QAM)-128, have been demonstrated in [18]. Data communications for wireless links are requiring frequencies greater than 75 GHz to achieve high data rates up 80 Gbps with 16-QAM signals [19]. Scalable W-band phased arrays using silicon technology have been demonstrated for automotive radar, imaging and communication in [20–22], while a 3-D imaging 100-GHz MIMO FMCW radar is investigated in [23].

With the research interest at the turn of the century bringing wide band-gap semiconductor research into motion, technologies such as Gallium-Nitride (GaN) [4, 24, 25] and the continuing Indium-Phosphide (InP) [26, 27] have been pushing high-frequency performance with operating frequencies in the hundreds of GHz, and InP reaching a cutoff frequency of 1 THz [28].

Research efforts continue in reducing the SWaP-C of millimeter-wave systems for current commercial and military demands. Recent government sponsored programs such as DARPA's Compound Semiconductor Materials on Silicon (COSMOS) and Diverse Accessible Heterogeneous Integration (DAHI) aim to provide efforts in highly integrated front-ends to provide the most desirable qualities from each [1]. Integration between low-noise InP for receive, high-power density of GaN for transmit, and highly dense mixed-signal capabilities of Si technology would provide capability for high integration systems on a single platform.

1.1.2 High-Power Active Array Transmitters

The challenge of high power transmitters with efficient power combining faced in the GaAs era still remain today. The general challenges for W-band high-power solid-state transmitters are achieving high effective radiated power (ERP) in a small footprint and with reasonable efficiency. Ultra-high power vacuum tubes

have been demonstrated to generate several hundreds of kW at W-band [29, 30]. Producing comparable W-band power using solid-state is challenging the highest published solid-state W-band amplifier producing 20W. Recent advances in GaN technology with cutoff frequencies $f_t > 150$ GHz [24, 31–34], achieve power densities as high as 3 W/mm at W-band. Using these state-of-the-art large bandgap semiconductor processes, many front-end compatible W-band MMICs have been demonstrated, e.g. [35–39]. One of the most notable MMICs [40] demonstrated peak output power levels and efficiency of 3.6 W and 12%, respectively.

For very high-power applications, such as ground-based active denial systems, many amplifiers are combined and feed an array of antennas [41]. The transmitter spatially coherently combines 8,192 >1 W GaN-on-SiC HEMT MMIC PAs with PAE >20% around 93 GHz. The output powers of eight MMICs are combined into a greater than 7 W sub-module, and these are then combined into 100 W unit blocks, with an ultimate 6.8 kW output radiated power. This approach is modular and therefore scalable, with high demonstrated power-combining efficiency.

For a solid-state W-band high-power source, coherent power combining of thousands of individual MMIC PAs is required with several levels of circuit combining and final free-space combining in the antenna array. The need for multiple levels of power combining provides a trade off in terms of combining efficiency, heat dissipation, volume and co-design from the transistor to the radiating aperture. Figure 1.2 shows power combining progression of a planar active array. Each PA module can have varying levels of power combining including device level within a MMIC amplifier, thin-film and waveguided power combining, and spatial

Table 1.1: Material Properties and Circuit Maturity of Various Semiconductor Technologies [1]

Parameter	Why?	Unit	Si	GaAs	InP	GaN
Electron Mobility	Carrier Velocity	$10^3 \mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$	1.4	8.5	12	< 1
V_{peak}	Transit Time	10^7 cm/s	1	2	2.5	2.5
E_{BK}	Voltage swing	10^5 cm/sec	3	4	4	40
E_{g}	Charge Density	eV	1.12	1.42	0.74	3.4
K	Heat removal	$\mathrm{W/cm} \cdot \mathrm{K}$	1.3	0.5	0.68	3.7
Maturity	Circuit complexity	-	Excellent	Good	Adequate	Limited

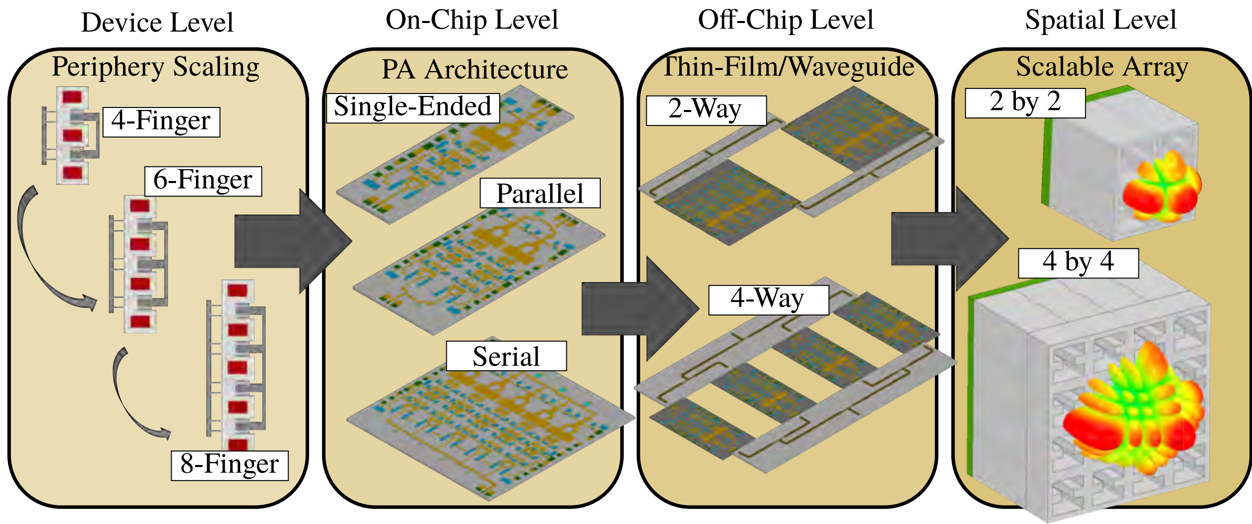

Figure 1.2: Various levels of power combining from device to spatial level.

power combining to achieve the desired ERP.

1.1.3 State-of-the-Art W-Band Power Amplifiers

Millimeter-wave transmitters in the 75-110 GHz W-band have to date been demonstrated extensively in silicon, where the output power is limited to tens of milli-watts with various stacked architectures used to increase the output power, e.g. [42]. InP can also produce this power level at W-band with over 40% power-added efficiency [43]. For higher output powers, GaN has shown record power densities of 6.5 W/mm^2 [44], with foundry processes demonstrating close to 1 W in a few GHz bandwidth, e.g. [45]. Figure 1.3 illustrates the current state-of-the-art published GaN MMIC PAs with performance summary given in Table 1.2.

1.2 Thesis Organization

The work presented in this thesis aims to answer what is achievable for wideband, high power W-band transmitters with the current state-of-the-art in millimeter-wave GaN-on-SiC semiconductor technology. Designs for various MMIC PAs are followed by an analysis of combining efficiency for high ERP transmitters, taking into account fabrication variations of GaN process in development. The content of each of the chapters are as follows:

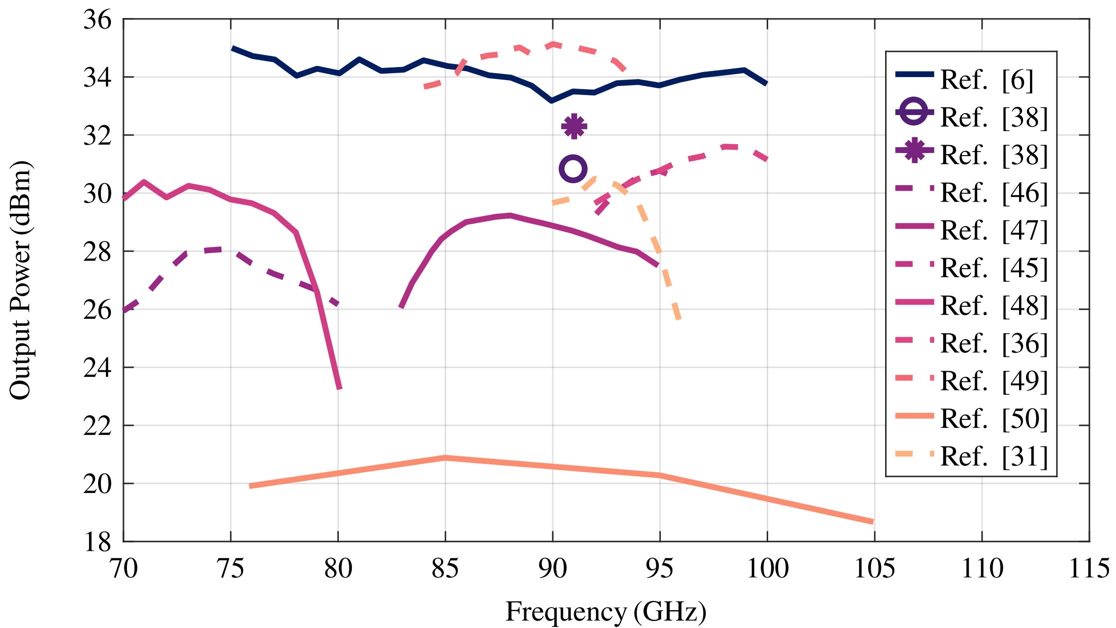

Figure 1.3: Output power versus frequency for state-of-the-art MMIC at W-band.

Table 1.2: Published GaN MMIC Power Amplifiers at W-Band

Reference	Peak Output Power (W)	Bandwidth (GHz)	*PAE* (%)	Chip Size (mm^2)
[6]	3	75-100	12	5.4 x 2.75
[38]	1.2	91	20	2.5 x 0.9
[38]	1.7	91	11	2.9 x 1.6
[46]	0.5	70-75	10	3.5 x 1.75
[47]	0.842	83-92	14.8	-
[45]	1.5	92-96	17.8	-

Chapter 2: Three state-of-the-art GaN-on-SiC millimeter-wave research processes are introduced; Qorvo's GaN09 90 nm V-band Γ-gate and W-band T-gate processes, and HRL's T3 40 nm process. Process metrics and performance based off of non-linear EEHEMT and Angelov transistor models for each process are presented. Steady-state thermal analysis for each of the processes will be summarized.

Chapter 3: Two W-band power amplifier designed in single-ended and balanced configuration are presented using Qorvo's GaN09 Γ-gate V-band process. The shortcomings in using transistor technology above

its designated operating frequency will be presented. Use of primary distributed matching techniques on a W-band MMIC design and compact biasing method will be shown in the designs.

Chapter 4: Two W-band power amplifier designs in balanced and serially configuration are presented using Qorvo's GaN09 T-gate W-band process. A look at the designs using state-of-the-art passive processing for the use of quasi-distributed MMIC designs to decrease MMIC footprint at W-band will be presented. An investigation of improved combining efficiencies through modeling of Lange couplers at millimeter-wave frequencies is presented. Additionally, stability design considerations in the design of millimeter-wave PAs is presented.

Chapter 5: The design of a full W-band MMIC power amplifier using HRL's T3 40 nm process will be presented. A unit power amplifier in balanced configuration predict the widest bandwidth and highest power using solid-state technology.

Chapter 6: With the need for power combining in high-power transmitter, an investigative look of power combining for on- and off-chip is done. The analysis of efficiencies distributed from the device level, on-chip reactive in-phase parallel combining, on-chip PA architecture, and off-chip corporate combining.

Chapter 7: A system level analysis for W-band spatial power combining is presented with the goal in achieving kW ERP at W-band. The analysis of combining efficiencies from Chapter 6 is extended to spatial power combining of variations presented in Chapter 6. Results of a 4×1 linear waveguide horn array at W-band is presented with analysis for a planar array.

Chapter 8: Finally, the thesis concludes with conclusions, thesis contributions, and recommendations for future work.

Chapter 2

State-of-the-Art GaN-on-SiC Millimeter-Wave Processes

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2.1 Introduction

Until recently, primary device technology of choice at millimeter-wave frequencies have been AlGaAs/InGaAs and InP HEMTs due to their decades of research and development resulting in process maturity. Government sponsored programs such as the DARPA's Nitride Electronic Next-Generation Technology (NEXT) program have brought forth high performing GaN devices with gate lengths down to 20 nm though aggressive device

scaling, achieving an f_T in excess of 300 GHz [24, 51, 52]. When placed on a SiC carrier substrate, GaN HEMT transistors provide capability for achieving high power, higher breakdown voltage, with the advantage of a high thermal conductivity.

This chapter presents three different research processes that are currently in development by the industry at Qorvo and HRL, for millimeter-wave operation. In Section 2.2, a brief background on GaN HEMT devices at millimeter-wave frequency is summarized. Section 2.3 introduces two Qorvo 90 nm GaN processes based off of the GaN09 Γ-gate and T-gate structure. Section 2.4 introduces HRL's 40 nm process based on T-gate structure. Section 2.5 presents a thermal analysis for GaN-on-SiC devices. Finally the chapter concludes with a summary of the processes presented.

2.2 GaN HEMT Devices

Due to GaN's wide band gap, it has been the chosen technology for power amplifiers from RF to millimeter-waves. The high breakdown voltage and high drain-source voltage allows for higher power densities to be achieved. In Fig. 2.1, a stack-up for a depletion-mode AlGaN/GaN HEMT transistor on SiC substrate is shown. The typical stack-up of HEMT transistor is formed by using 5 layers; cap, barrier, channel, barrier, and carrier substrate. Each provide specific function for the design of high performing HEMT devices. In many cases for III-V semiconductors, an additional thin layer placed between carrier substrate and barrier layer is used to provide lattice match to improve mechanical stability between the two.

2.2.1 Short-Channel HEMT Device Scaling

Efforts in improving transistor performance are achieved by investigating f_T and f_{max} for the device, given by,

$$f_T = \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)} \tag{2.1}$$

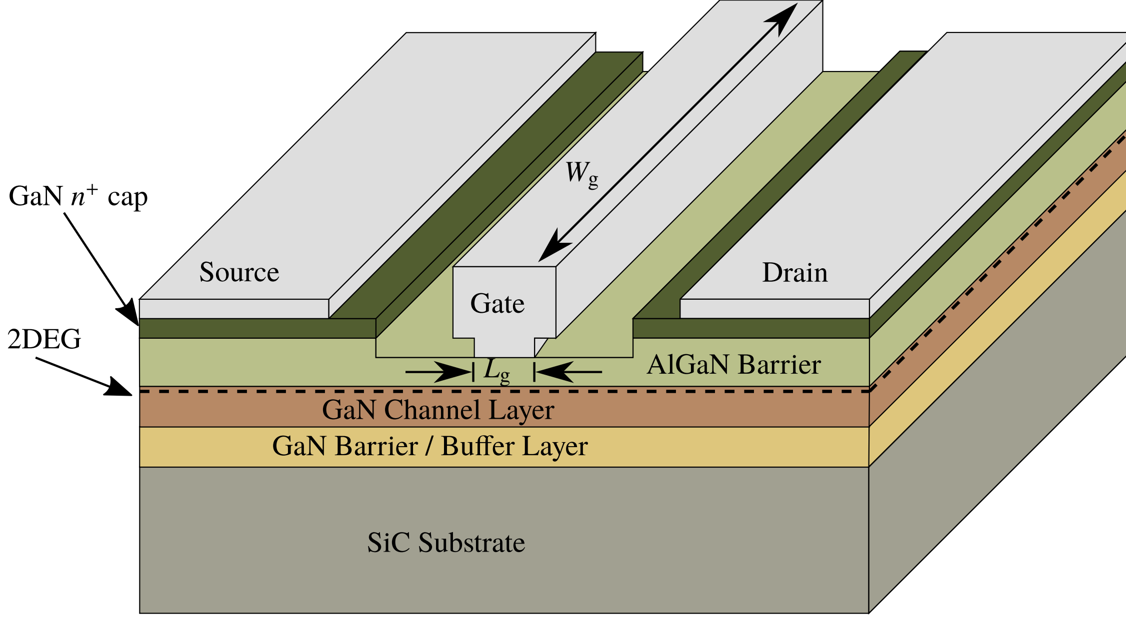


Figure 2.1: GaN HEMT transistor stack-up for D-mode device.

$$f_{\mathrm{max}} = \frac{f_{\mathrm{T}}}{\sqrt{4g_{\mathrm{ds}}\left(R_{\mathrm{in}} + \frac{R_{\mathrm{s}}+R_{\mathrm{g}}}{1+g_{\mathrm{m}}R_{\mathrm{s}}}\right) + \frac{4}{5}\frac{C_{\mathrm{gd}}}{C_{\mathrm{gs}}}\left(1 + \frac{2.5C_{\mathrm{gd}}}{C_{\mathrm{gs}}}\right)(1 + g_{\mathrm{m}}R_{\mathrm{s}})^2}} \tag{2.2}$$

For example, improving the the g_{m} and reducing parasitic capacitance of C_{gs} and C_{gd} will improve f_{T} and f_{max} [53]. Horizontal scaling provides a reduction in transit time across the channel between the source-drain which is important in increasing the frequency of operation of the transistor. The trade-offs with horizontal scaling are reduction in the breakdown voltage caused by the high field between the gate and drain terminals and an increase in the series resistance of the gate [53].

Advanced, heavily scaled HEMT transistors at millimeter-waves have been demonstrated in recent years [4, 24, 52]. From Eq. (2.2), reductions in device resistances at the source and drain provides improvements in f_{max}. Device scaling of L_{g} increases the R_{g} of the device which is mitigated by using a "cap" like structure on the gate contact which forms the "T" shape of the device. Gate recess into the AlGaN barrier additional helps improve charge control in the active region, increasing the modulation efficiency that is described in [54]. Additional reduction in R_{s} improves the f_{max} of the device. In [4] and [52], recessed ohmic contact regrowth for the GaN n^+ cap places the source and drain contact closer to the 2DEG region therefore reducing series

resistance at the S-D terminals.

2.2.2 GaN HEMT Models

One of the primary limitations on performance of GaN devices are the trapping effects that have become ubiquitous in literature and a field of research in itself. This limitation causes reduction in the maximum current that results in a reduction of output power of amplifiers and cause reduction in G_{m} over its DC value known as dispersion. This limitation is propagated to the accuracy of large-signal models that are used in the design of MMIC power amplifiers. On-going research for accurate modeling of GaN HEMT transistors continue with methods such as double-pulsed *I-V* measurements in [55]. The two most accepted models used are Keysight's EEHEMT model based on [56] and Angelov model [57], that will be used for Qorvo and HRL, respectively.

2.3 Qorvo GaN09 90 nm Process Technology

The W-band MMICs presented in Chapter 3 and Chapter 4 are designed in Qorvo's GaN09 90 nm Γ-gate and T-gate GaN-on-SiC HEMT research process. Over recent years, Qorvo's developments in active processing of HEMT devices have $f_T > 140$ GHz for V-band and W-band operation, that enable millimeter-wave PAs [31, 58]. Improvements in f_{T} for the Γ- and T-gates by reducing parasitics are shown in Fig. 2.2, with device parameters in Table 2.1. The Qorvo 90 nm technology uses an AlN/GaN epitaxial material growth structure in both Γ- and T-gate configuration. Scanning electron microscope (SEM) image for the Γ-gate is shown in Fig. 2.3 and gate structures for three generations of GaN09 are shown in Fig. 2.4.

The GaN HEMT technology utilizes internal-internal-source (ISV) and is processed on 50 μm SiC substrate. This transistor configuration provides advantages for stability, heat, and reduction in source inductance. The active technology is compatible with current state-of-the-art passive processing using the Qorvo 3-Metal-Interconnect (3MI) layer processing that provides tantalum-nitride (TaN) resistors and various metal-insulator-metal (MIM) silicon nitride (SiN) capacitor configurations. Most notably, the 3MI process provides capability for small capacitors-over-vias (COV), to be used for impedance matching at

Table 2.1: Qorvo GaN09 90 nm Process [Courtesy: Qorvo]

Parameter	Γ-Gate	T-Gate GEN I	T-Gate GEN II
C_{gs} (pF)	0.172	0.098	0.102
C_{gd} (pF)	0.029	0.016	0.016
DC G_m (mS/mm)	700	650	850
RF G_m (mS/mm)	628	441	673

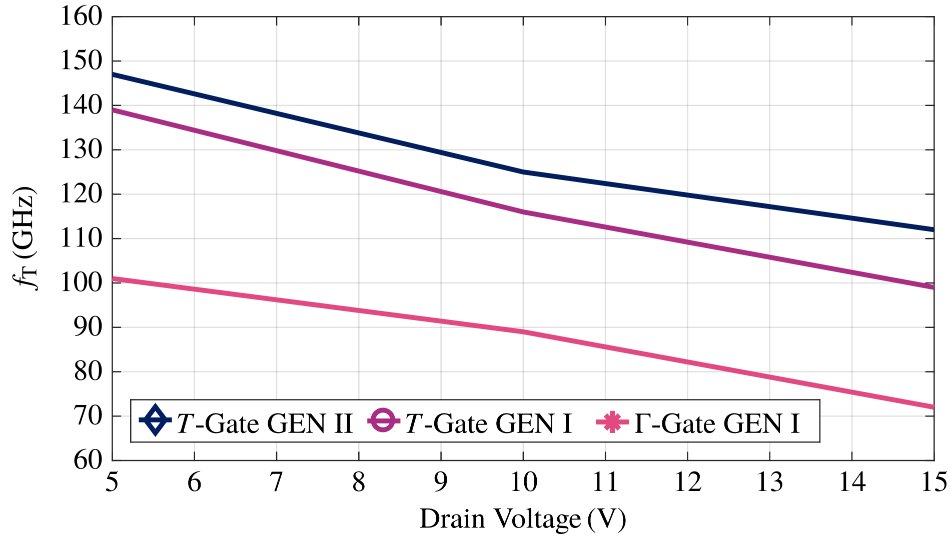


Figure 2.2: Cutoff frequency versus drain voltage for Qorvo GaN09. [Courtesy: Qorvo]

millimeter-wave frequencies. Further details on passive processing will be described in the following chapters.

2.3.1 GaN09 Γ-Gate Performance

The Qorvo GaN09 Γ-gate devices can operate at V-band. The device is modeled using a non-linear, EEHEMT model for a 4-finger, $N = 4$, and gate width, $W_G = 40\,\mu$m, 4×40 μm transistor. The I-V curves scaled for current density are plotted in Fig. 2.5. The device model was validated at 85 GHz which will be used as the frequency of analysis for subsequent non-linear performance. The device is intended to operate at a drain voltage, $V_{DS} = 15 - 18$ V with drain current density, $I_{DS,dens}$, of 200 mA/mm, corresponding to a drain

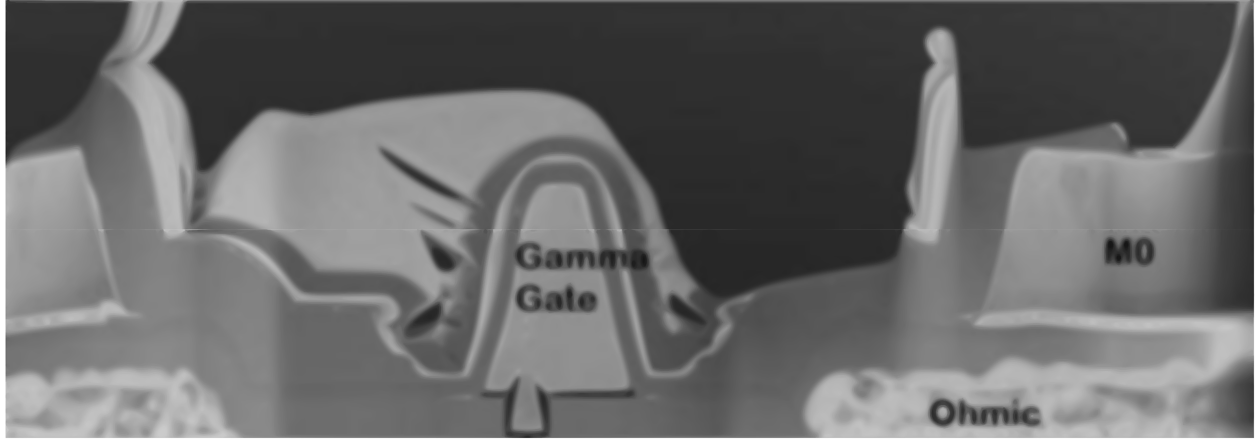
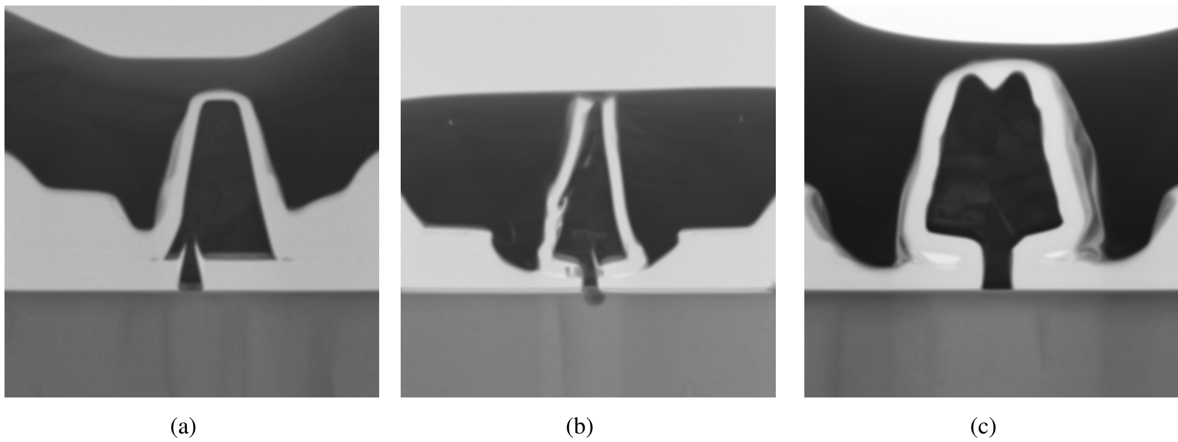


Figure 2.3: SEM for HEMT transistor structure on Qorvo GaN09 Γ-gate process.[Courtesy: Qorvo]



(a) (b) (c)

Figure 2.4: SEM images for Qorvo GaN09 process for (a) Γ-gate, (b) T-gate GEN I, and (c) T-gate GEN II. [Courtesy: Qorvo]

current I_D = 32 mA. Peak drain current density at the knee is shown to be 500 mA/mm.

Load-pull of non-linear devices is simulated using commercially available microwave CAD software, AWR's Microwave Office [59]. The procedure for load-pull is to first provide the source termination for gain match given by $\Gamma_{source} = \Gamma^*_{gate}$. For the 4×40 μm transistor, the reflection coefficient of conjugate gate impedance is $\Gamma_{source} = 0.82\angle 178°$. Once matched at the gate, load-pull for maximum output power and PAE is completed. Figure 2.6 and Fig. 2.7 show the load-pull results for maximum output power and PAE, respectively, $P_{out,max} = +25.54$ dBm at peak PAE with a $\Gamma_{opt} = 0.85\angle 123.3°$. The maximum PAE of the device is 27.3 % with a $\Gamma_{opt} = 0.83\angle 120.7°$.

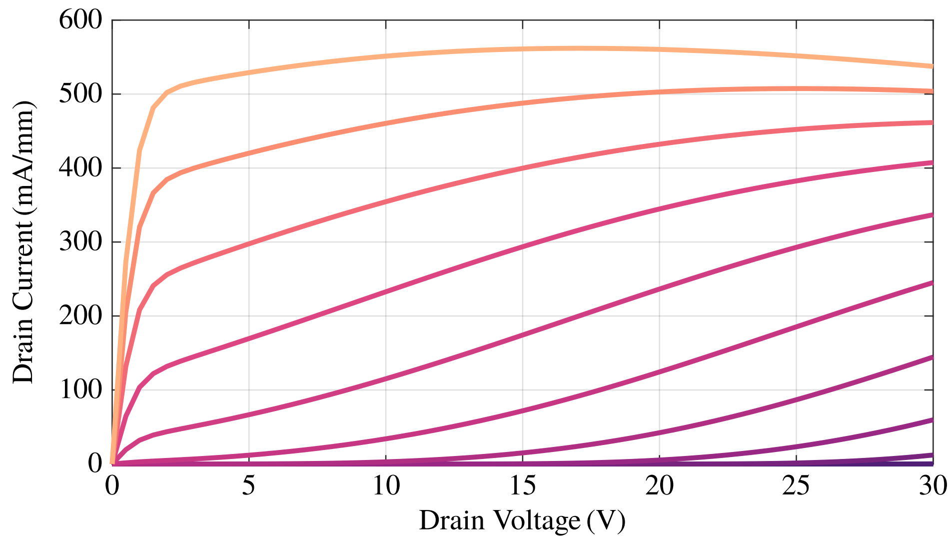


Figure 2.5: Simulated *I-V* curves for Qorvo GaN09 Γ-Gate 4×40 μm EEHEMT transistor. The peak drain current density is 500 mA/mm at a threshold voltage, V_{th} = 2 V.

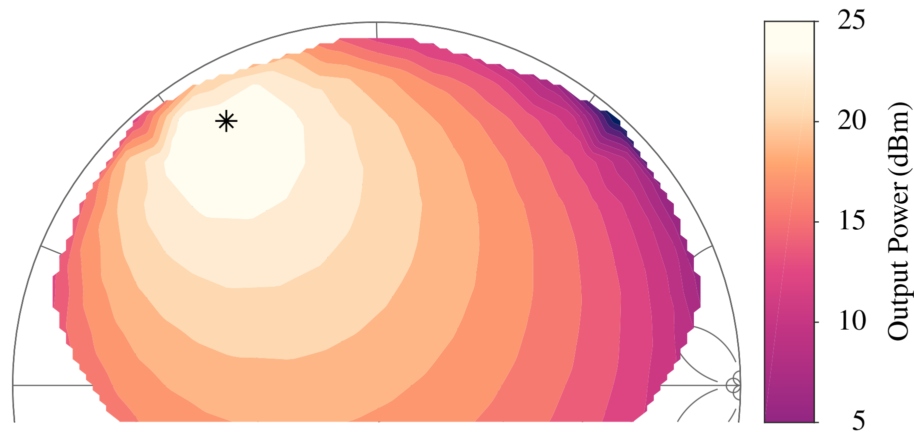


Figure 2.6: Simulated load-pull contour plots for maximum output power at 85 GHz using Qorvo GaN09 Γ-Gate 4×40 μm EEHEMT transistor. The source is terminated with the reflection coefficient of conjugate gate impedance, $\Gamma_{\text{source}} = 0.82\angle 178°$. The maximum output power is +25.54 dBm at peak PAE with a $\Gamma_{\text{opt}} = 0.85\angle 123.3°$

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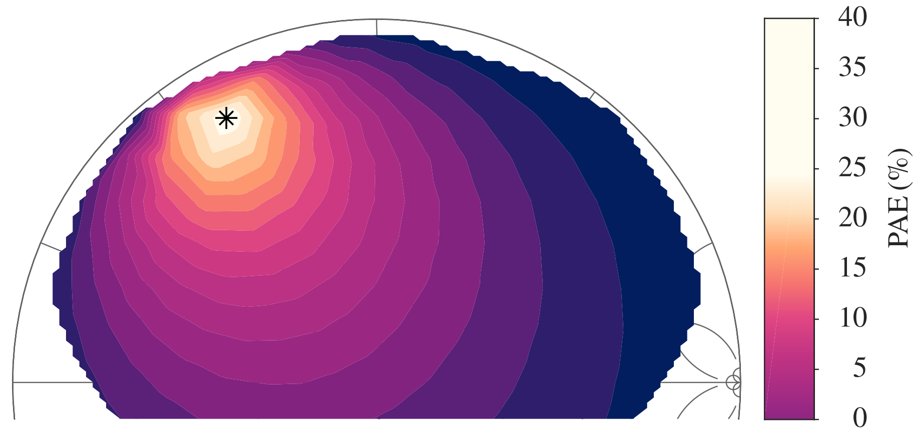


Figure 2.7: Simulated load-pull contours for maximum PAE at 85 GHz using Qorvo GaN09 Γ-Gate 4×40 μm EEHEMT transistor. The source is terminated with the reflection coefficient of conjugate gate impedance, $\Gamma_{source} = 0.82\angle 178°$. The maximum PAE is 27.3 % with a $\Gamma_{opt} = 0.83\angle 120.7°$.

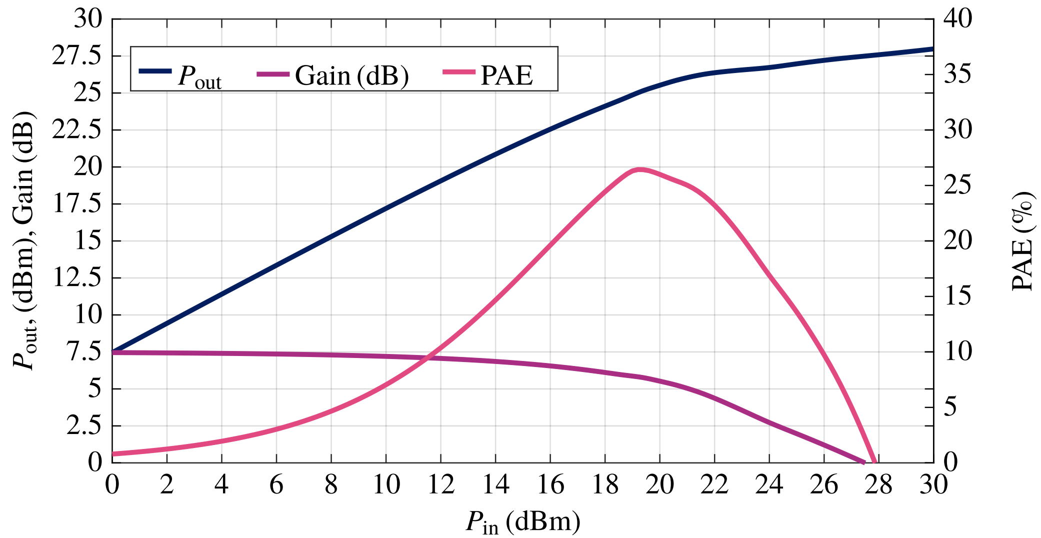


Figure 2.8: Simulated P_{out}, Gain, and PAE at 85 GHz for the Qorvo GaN09 Γ-Gate 4×40 μm EEHEMT transistor. The output power is +25.54 dBm at peak 26.3 % PAE with a gain of 5.69 dB.

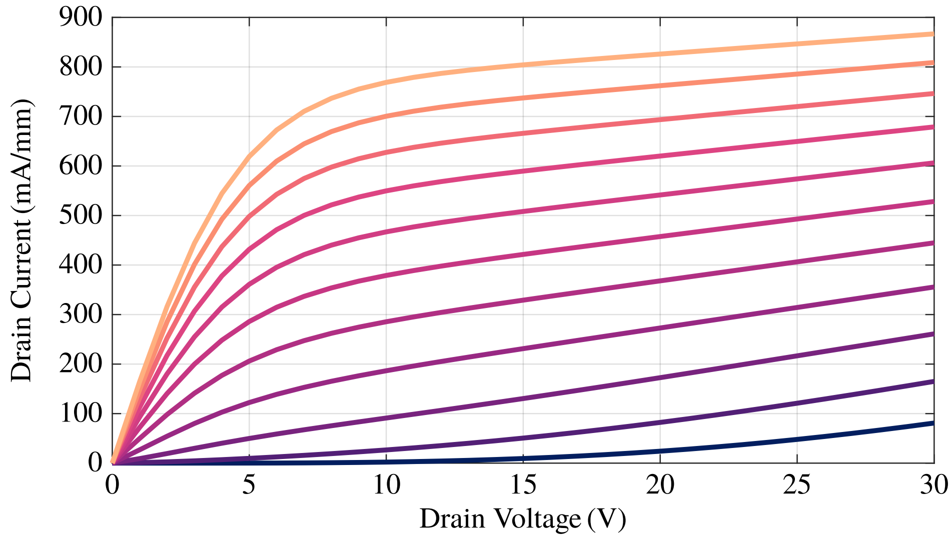


Figure 2.9: Simulated *I-V* curves for Qorvo GaN09 T-Gate 4×40 μm EEHEMT transistor. The peak drain current density is 737 mA/mm at a threshold voltage, V_{th} = 8 V.

2.3.2 GaN09 T-Gate Performance

While the Qorvo GaN09 Γ-gate is well suited for V-band PAs, the T-gate process is capable of W-band operation. Similar to the Γ-gate, the device is simulated using a non-linear EEHEMT model for a 4×40 μm transistor. The *I-V* curves scaled for current density are plotted in Fig. 2.9 showing peak drain current density at the knee of 700 mA/mm. The device model was validated at 95 GHz which will be used as the frequency of analysis for subsequent non-linear performance. The device is intended to operate at a lower drain voltage, V_{DS} = 13 V with a lower drain current density, $I_{DS,dens}$, of 150 mA/mm, corresponding to drain current of 24 mA for a 4×40 μm device. Though the T-gate device can operate at much higher frequencies, its lower breakdown voltage limits the output power of the device as will become evident with load-pull results.

Load-pull for the 4×40 μm are done with a source termination of $\Gamma_{source} = 0.77\angle 176.8°$. With the gate gain matched, load-pull for maximum output power and PAE is completed. Figure 2.10 and Fig. 2.11 show the load-pull results for maximum output power and PAE, respectively. The maximum output power is +22.24 dBm at peak PAE with a $\Gamma_{opt} = 0.75\angle 116.2°$. The maximum PAE of the device is 33.69 % with a $\Gamma_{opt} = 0.80\angle 118°$.

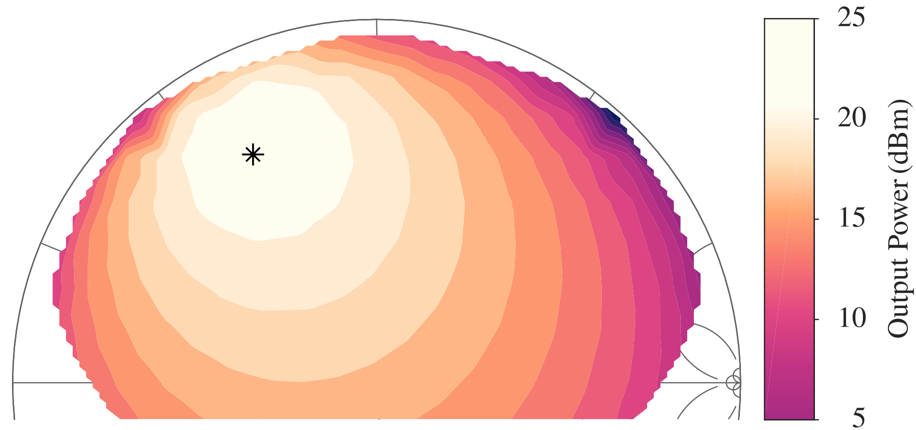


Figure 2.10: Simulated load-pull contours for maximum output power at 95 GHz using Qorvo GaN09 T-Gate 4×40 μm EEHEMT transistor. The source is terminated with the reflection coefficient of conjugate gate impedance, Γ_{source} = 0.77∠176.8°. The maximum output power is +22.24 dBm at peak PAE with a Γ_{opt} = 0.75∠116.2°.

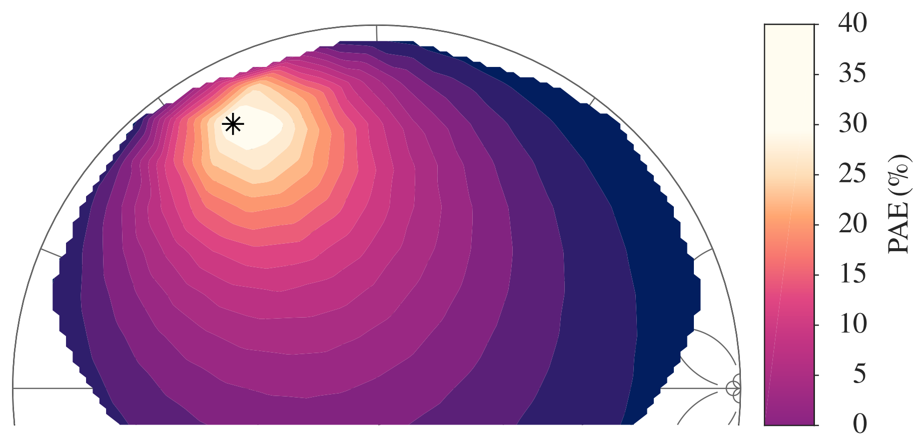


Figure 2.11: Simulated load-pull contours for maximum PAE at 95 GHz using Qorvo GaN09 T-Gate 4×40 μm EEHEMT transistor. The source is terminated with the reflection coefficient of conjugate gate impedance, Γ_{source} = 0.77∠176.8°. The maximum PAE is 33.69 % with a Γ_{opt} = 0.80∠118°.

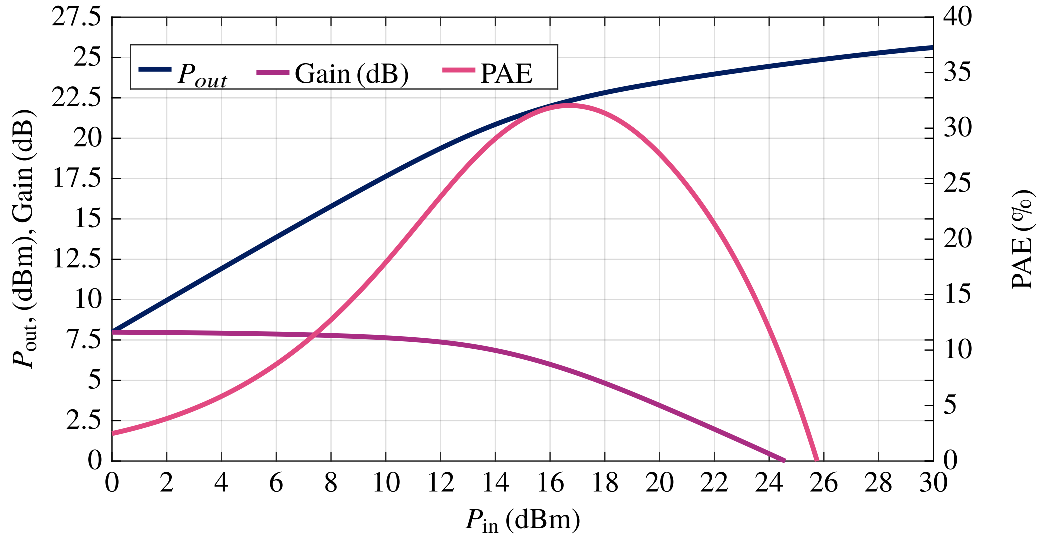
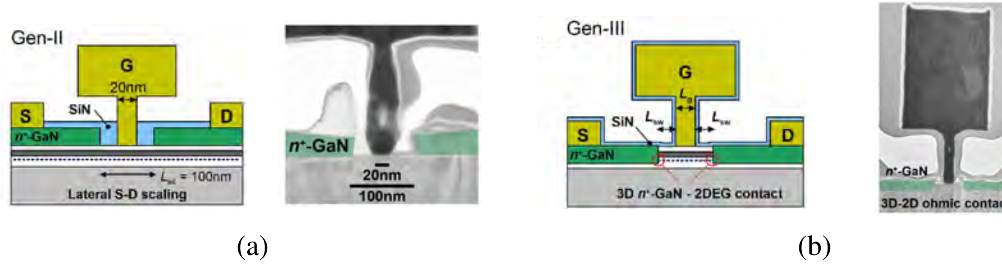


Figure 2.12: Simulated P_{out}, Gain, and PAE at 95 GHz for the Qorvo GaN09 T-Gate 4×40 μm EEHEMT transistor. The output power is +22.24 dBm at peak 32 % PAE with a gain of 5.67 dB.

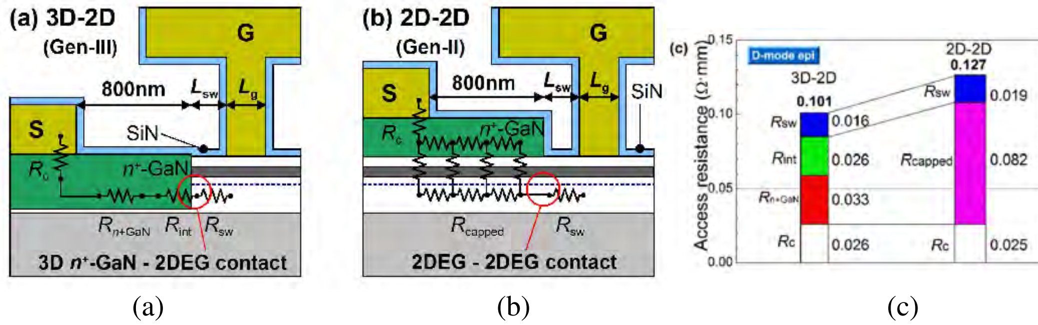


(a) (b)

Figure 2.13: HRL's technology for GEN-II (T2) and GEN-III (T3) [4]. SEM images for T2 and T3 which show different n^{+}-GaN cap configuration.

2.4 HRL T3 40 nm Process Technology

The HRL processes are well documented in the literature, e.g. [4, 24, 60–62]. This section will present the large-signal performance for the HRL T3 process. In Fig. 2.13, the evolution from the T2 to the T3 process shows the recessed n^{+}-GaN cap layer in direct contact with the 2DEG layer. As a result, reductions in the contact resistance from T2's 0.082 $\Omega \cdot$ mm to T3's 0.059 $\Omega \cdot$ mm is shown in Fig. 2.14. Transistor scaling for the T3 process achieves an $f_{\mathrm{T}}/f_{\mathrm{max}}$ of 200 GHz/400 GHz with a breakdown voltage, $V_{\mathrm{brk}} > 40$ V. The process is intended to operate at a drain voltage, $V_{\mathrm{DS}} = 12$ V with drain current density, $I_{\mathrm{DS,dens}}$, of 150 mA/mm, corresponding to $I_{\mathrm{D}} = 22.5$ mA for a 4×37.5 μm device.



(a) (b) (c)

Figure 2.14: Recessed n^{+}-GaN cap in T3 (a) provides reduction in contact resistance (b),(c), resulting in higher f_{T}. [4]

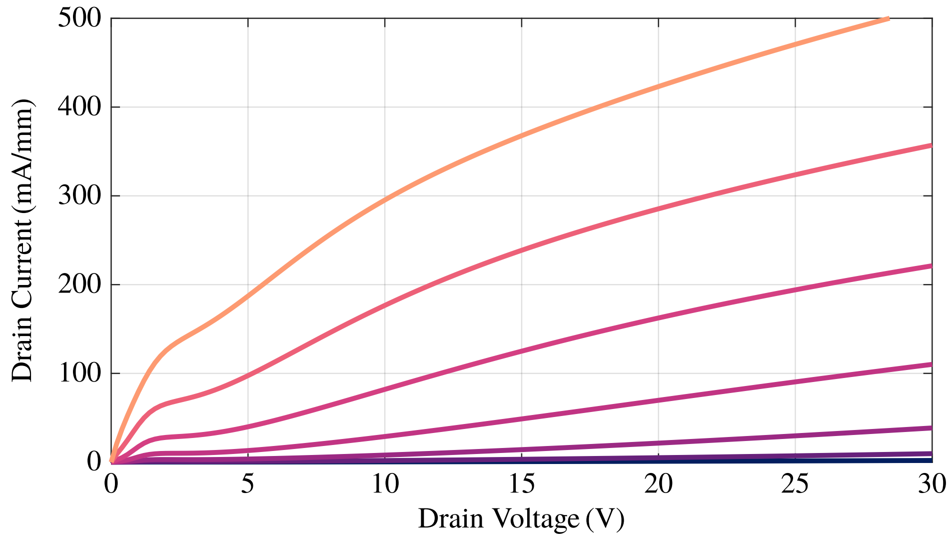


Figure 2.15: Simulated *I-V* curves for HRL's T3 4×37.5 μm Angelov transistor. The peak drain current density is 125.6 mA/mm at a threshold voltage, V_{th} = 2 V.

The device is modeled using a non-linear Angelov model for a 4×37.5 μm transistor. The *I-V* curves scaled for current density are plotted in Fig. 2.15 showing peak drain current density at the knee closer to 125 mA/mm. It is worth mentioning here Angelov's model to capture current collapse at the knee of the *I-V* curves over the EEHEMT behaviors in Fig. 2.5 and Fig. 2.9, that show a more pronounced "knee" behavior on the *I-V* curves. As a result, the Angelov is a better predictor of large-signal output power over the EEHEMT models.

Load-pull for the 4×37.5 μm are done source termination of Γ_{source} = 0.72∠174.6°. With the gate gain matched, load-pull for maximum output power and PAE is completed. Figure 2.16 and Fig. 2.17 show

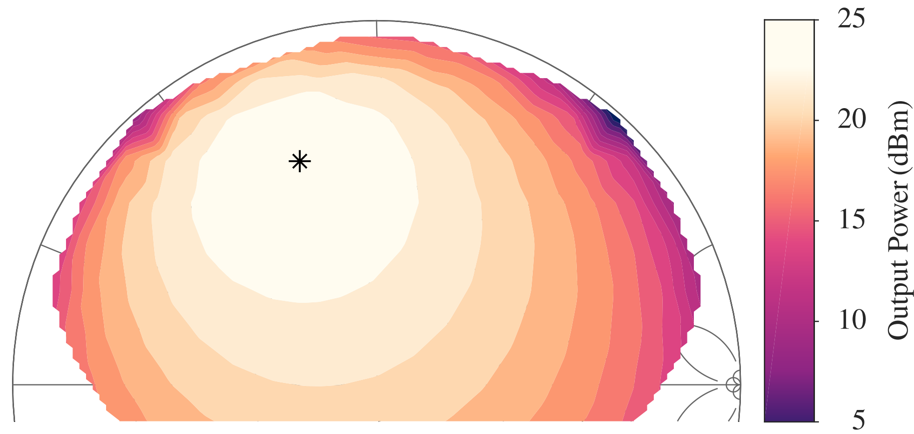


Figure 2.16: Simulated load-pull contour plots for maximum output power at 95 GHz using HRL's T-Gate transistor with an Angelov 4×37.5 μm transistor models. The source is terminated with a reflection coefficient of conjugate gate impedance, $\Gamma_{source} = 0.72\angle 174.6°$. The maximum output power of the device yields +23.94 dBm at peak PAE with a $\Gamma_{opt} = 0.65\angle 112°$.

the load-pull results for maximum output power and PAE, respectively. The maximum output power is +23.94 dBm at peak PAE with a $\Gamma_{opt} = 0.65\angle 112°$. The maximum PAE of the device is +27.22 % with a $\Gamma_{opt} = 0.80\angle 118°$.

2.5 Thermal Analysis of GaN HEMT Devices

Thermal analysis is important for GaN devices. Operating at high channel temperatures can decrease the mean time to failure (MTTF). Accurate measurements of channel temperature require techniques such as Raman spectroscopy and thermal microscopy, e.g. [63]. Analysis of channel temperature can be done with finite element (FEM) thermal solvers such as ANSYS Mechanical [64], and analytical approximation models for the thermal resistance based on transistor stack-up [65, 66].

In [65], accurate predictions of junction temperatures for AlGaN/GaN HEMT transistors were presented and validated with measurements in open literature, with improved accuracy over older models such as the Cooke model [67]. This section presents a thermal analysis based off the analytical approximation presented in [65] and steady-state FEM thermal analysis using [64] for feature sizes of state-of-the-art millimeter-wave

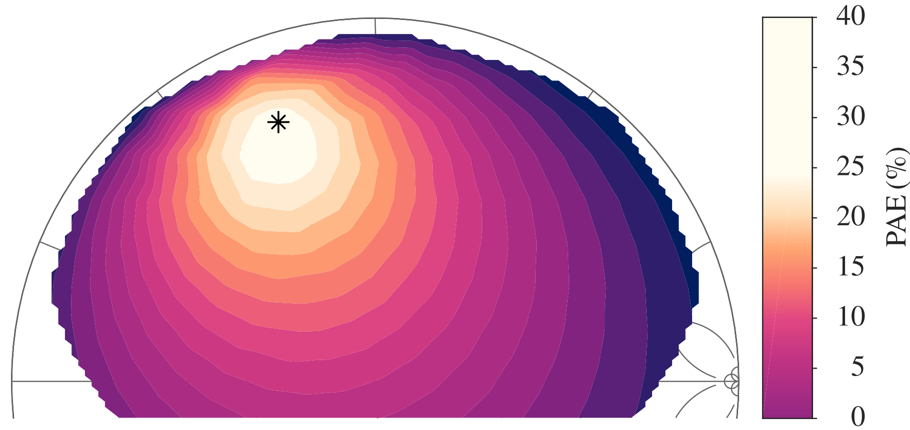


Figure 2.17: Simulated load-pull contour plots for maximum PAE at 95 GHz using HRL's T-Gate transistor using Angelov 4×37.5 μm transistor models. The source is terminated with a reflection coefficient of conjugate gate impedance, $\Gamma_{\text{source}} = 0.72\angle 174.6°$. The maximum PAE of the device is 27.22 % with a $\Gamma_{\text{opt}} = 0.73\angle 113°$.

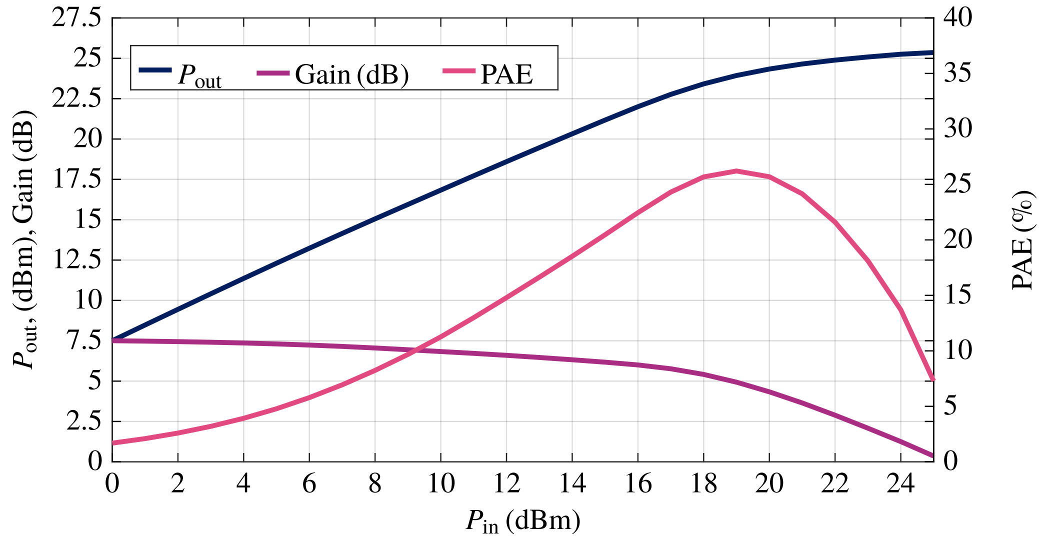


Figure 2.18: Simulated P_{out}, Gain, and PAE at 95 GHz for HRL's T3 T-Gate transistor performance using Angelov 4×37.5 μm transistor models, showing an output power of +23.94 dBm at peak 26.2 % PAE with a gain of 4.94 dB.

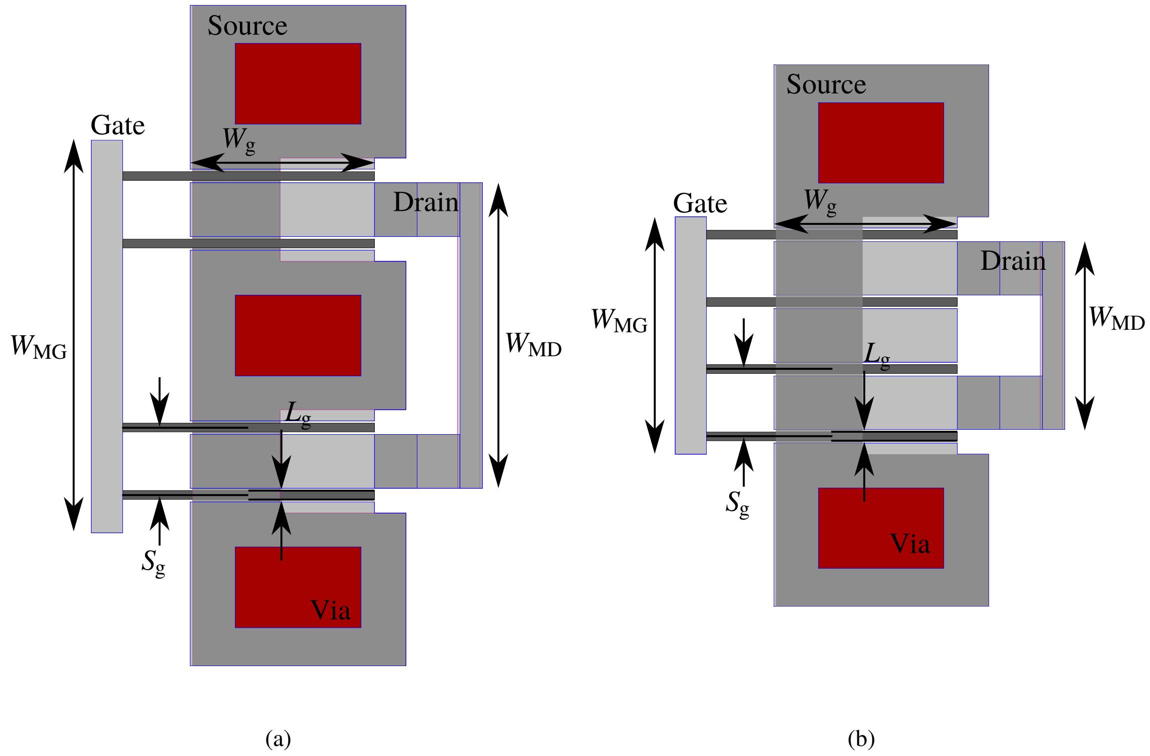


Figure 2.19: General layout of a 4-finger transistor device with internal source vias (ISV) in (a) and without ISV in (b).

processes such as those presented in Section 2.3 and Section 2.4. Figure 2.19 shows two typical layouts implemented for transistor layouts. In Fig. 2.19 (a), ISV are used for symmetrical operation of device at each finger. Alternatively, the configuration used in Fig. 2.19 (b) uses vias placed only externally at each ends are also used.

The stack up of a AlGaN/GaN on SiC device for the computation of the thermal resistance, Θ_{res}, is shown in Fig. 2.20. The thermal conductivity values used for SiC, GaN, and gold are $k_{\text{SiC}} = 3.3\,\text{W/cm}\cdot\text{K}$, $k_{\text{GaN}} = 1.5\,\text{W/cm}\cdot\text{K}$, and $k_{\text{Au}} = 315\,\text{W/m}\cdot\text{K}$, respectively. In Fig. 2.21, parameters substrate thickness, gate length (L_g), gate width (W_g), gate spacing (S_g), are scaled to solved for the thermal resistance of a device. Figure 2.21(a)-(d) shows scaling in gate width provides a faster drop off in thermal resistance over all other parameters. Unfortunately, increasing the gate width on the order of a 100 μm increases the input resistance of the device.

A comparison is presented here between analytical approximations and steady-state thermal analysis using

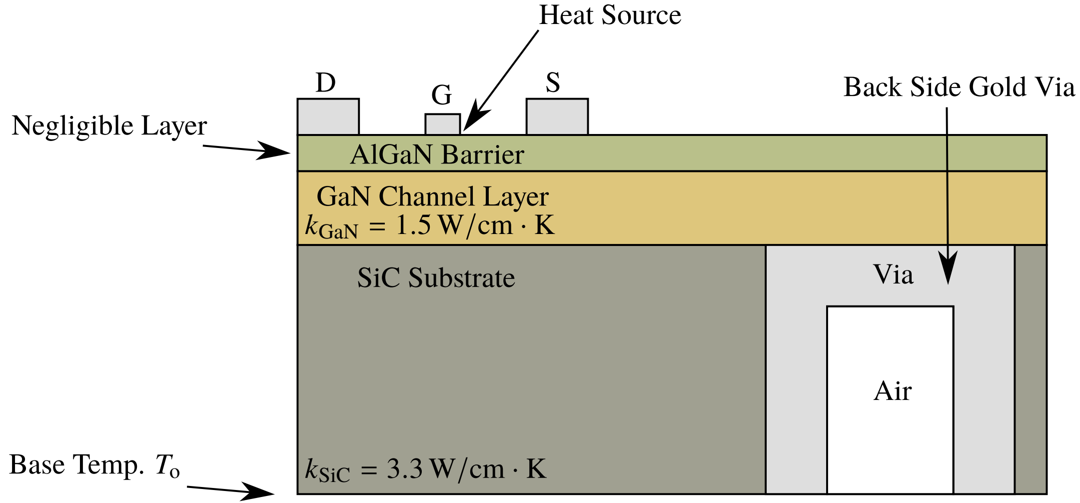


Figure 2.20: Cross-section stack up of a AlGaN/GaN on SiC device for thermal simulations. Thermal conductivity for SiC, GaN, and gold are $k_{SiC} = 3.3\,W/cm \cdot K$, $k_{GaN} = 1.5\,W/cm \cdot K$, and $k_{Au} = 315\,W/m \cdot K$, respectively.

geometry of a Qorvo GaN09 transistor with and without ISV. Figure 2.22 shows the lines of symmetry used for the adiabatic boundary conditions which restricts heat flux through the walls of the model. This boundary conditions forms a symmetry plane such that the two half fingers are operating in 4-finger environment. The base of the SiC substrate where the ground metallization will form thermal contact with packaging has the boundary conditions include a constant temperature of $T_o = 22\,°C$. Thermal excitation with an equivalent power flux of 0.12 W per finger are placed at the interface between the gate and GaN boundary. The 0.12 W per finger corresponds to DC conditions of $V_{DS} = 15\,V$ and $I_{DS,dens} = 200\,mA/mm$ for the Qorvo GaN09 Γ-gate. Thermal convection and radiation is assumed to be negligible and neglected at the top surface, as is typically assumed for stagnant air.

Figure 2.23 shows the steady-state thermal FEM simulation of a 4×40 μm device with and without ISV spacing. In Fig. 2.23(a), a single-finger model results in a $T_{max} = 62.69\,°C$. In Fig. 2.23(b) and (c), maximum thermal temperature is reduced from $T_{max} = 59.65\,°C$ to $T_{max} = 54.74\,°C$ for without and with ISV, respectively. Results of the FEM simulations compared to analytical approximation model in [65] are shown in Fig. 2.24, with results summarized in Table 2.2.

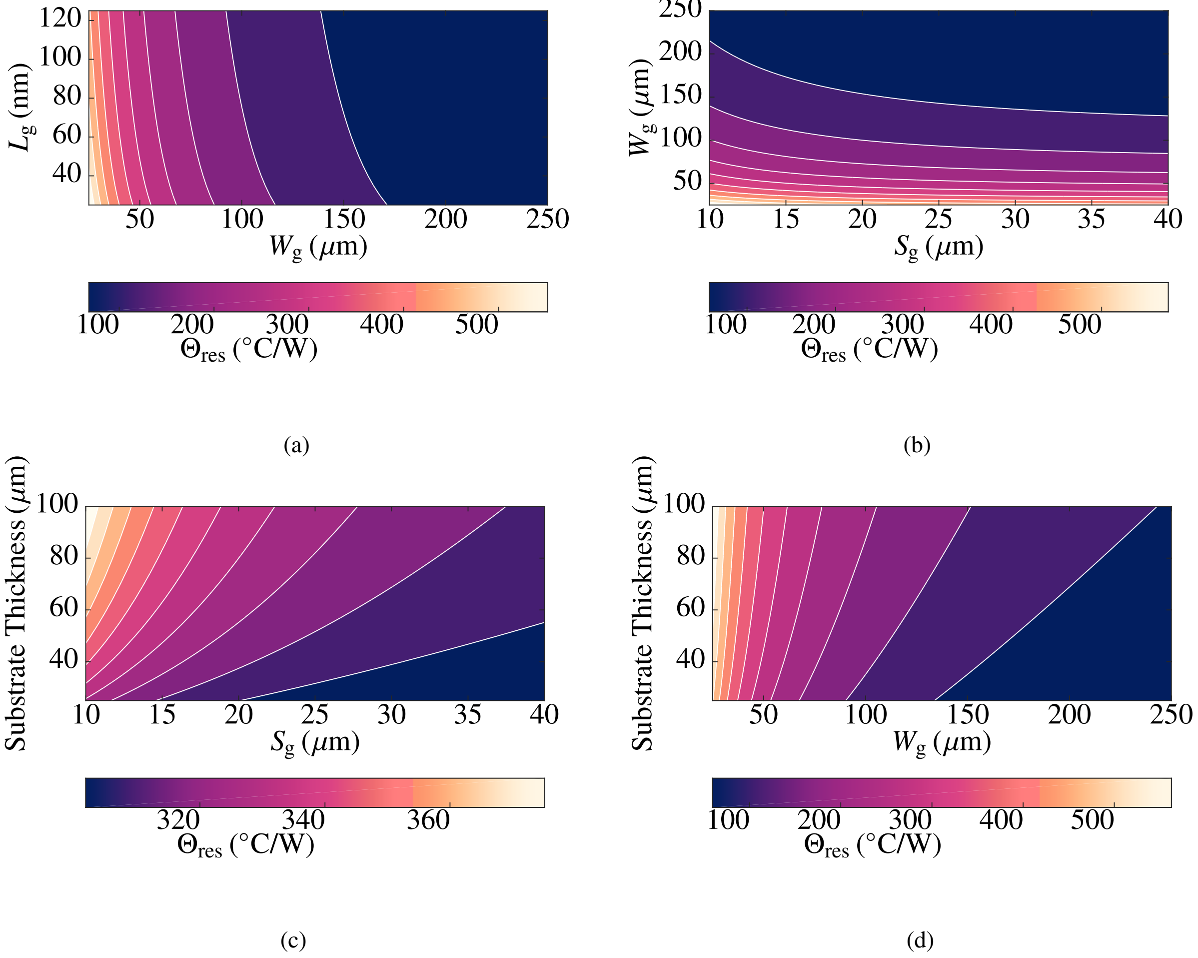


Figure 2.21: Thermal resistance value for various parameters based on modern semiconductor processes: (a) Swept parameters for gate length, L_g, and gate width, W_g, with gate spacing, $S_g = 15\,\mu$m, and substrate thickness, $t_{SiC} = 50\,\mu$m. (b) Swept parameters for gate spacing, S_g, and gate width, W_g, with gate length, $L_g = 40$ nm, and substrate thickness, $t_{SiC} = 50\,\mu$m. (c) Swept parameters for substrate thickness, t_{SiC}, and gate length, W_g, with gate spacing, $S_g = 15\,\mu$m, and gate length, $L_g = 40$ nm. (d) Swept parameters for substrate thickness, t_{SiC}, and gate spacing, S_g, with gate length, $L_g = 40$ nm, and gate width, $W_g = 40\,\mu$m.

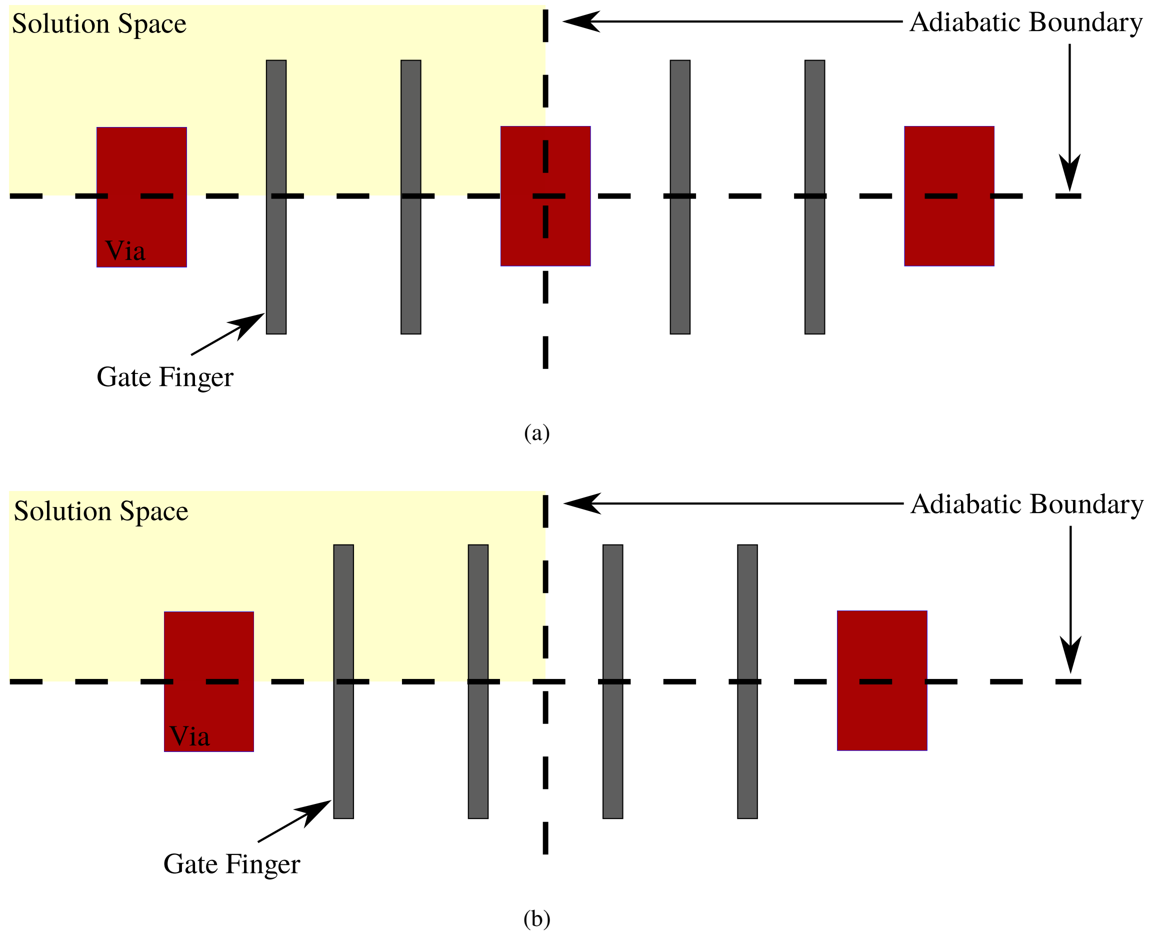


Figure 2.22: Cross section of FET transistor showing finite element simulation boundaries for ISV in (a) and external source vias in (b).

Table 2.2: Summary of Device Thermal Simulation

	Base Temp. (°C)	Channel Temp. (°C)	Thermal Resistance (°C/W)
Single-Finger	22	62.69	339
External Source Vias	22	59.65	314
Internal Source Vias	22	54.76	273

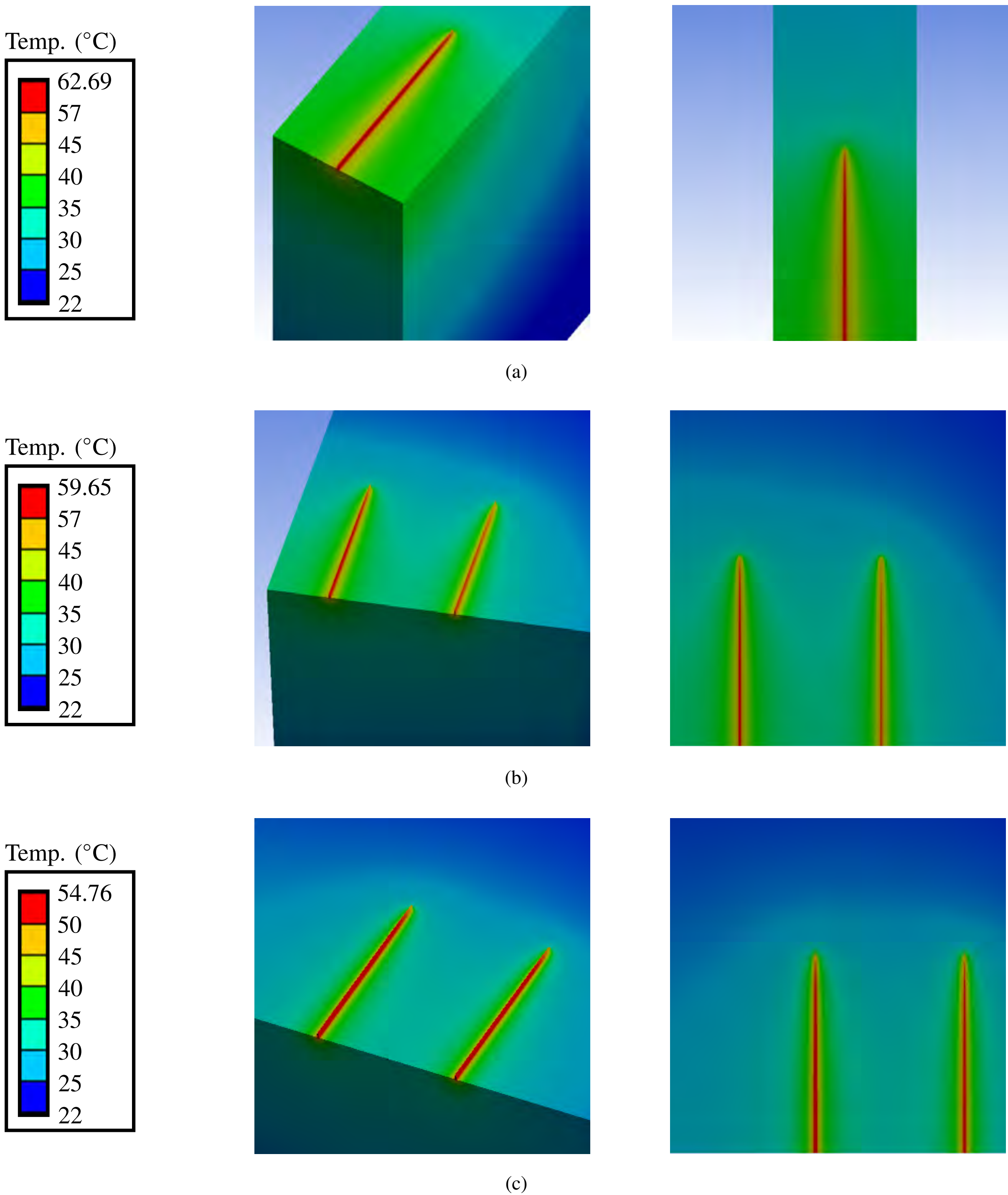


Figure 2.23: Finite element simulations for four-finger, $L_g = 40\,\mu$m device. Boundary conditions include: constant temperature of $T_o = 22\,°$C at the base of the SiC substrate, adiabatic boundaries on side walls of model, half plane at the middle of the finger, power flux of 0.06 W per half-finger corresponding to DC conditions of $V_{DS} = 15$ V and $I_{DS,dens} = 200$ mA/mm for the Qorvo GaN09 Γ-gate. Thermal convection and radiation is assumed to be negligible and neglected at the top surface.

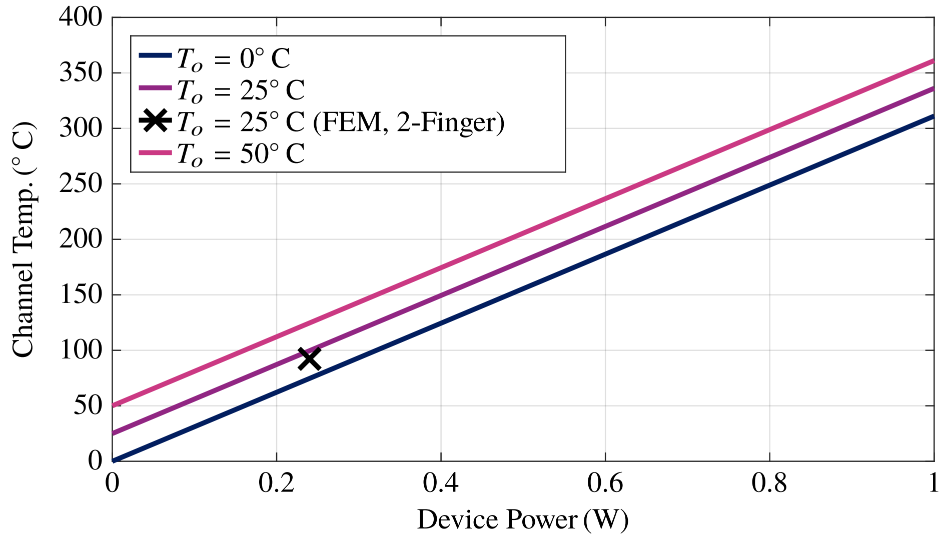


Figure 2.24: Channel temperature versus device power for various base temperatures.

2.6 Summary of Process Technology

A summary for the three processes described in this chapter is shown in Fig. 2.25, Fig. 2.26, and Fig. 2.27. Figure 2.27 shows the Qorvo GaN09 Γ-gate process having a higher power density over GaN09 T-gate and HRL's T3 for frequencies below 105 GHz. HRL's T3 process shows higher output power across all of W-band compared to the Qorvo GaN09 T-gate process, but the latter has improved gain over the band. A summary of optimum loads for output power and PAE are given in Table 2.4 with associated large-signal results given in Table 2.3.

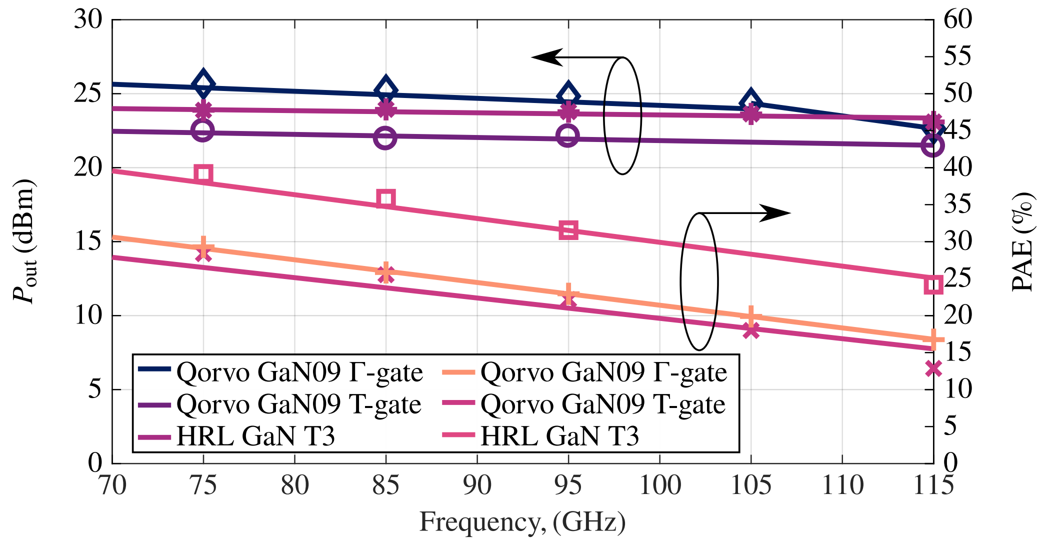


Figure 2.25: Output power, P_{out}, and PAE comparisons over W-band for Qorvo GaN09 Γ-gate and T-Gate, and HRL T3 processes.

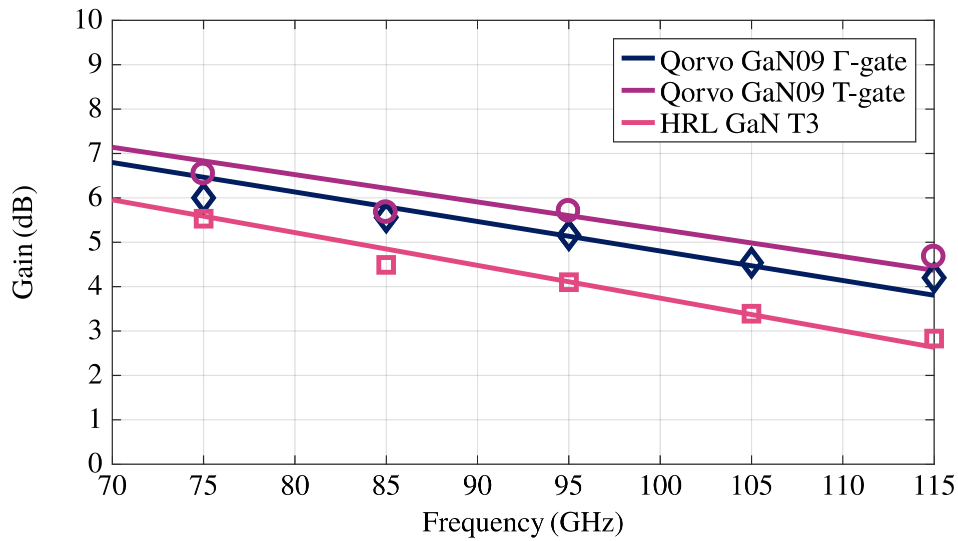


Figure 2.26: Large-signal gains at optimum power match and peak PAE comparisons over W-band for Qorvo GaN09 Γ-gate and T-Gate, and HRL T3 processes.

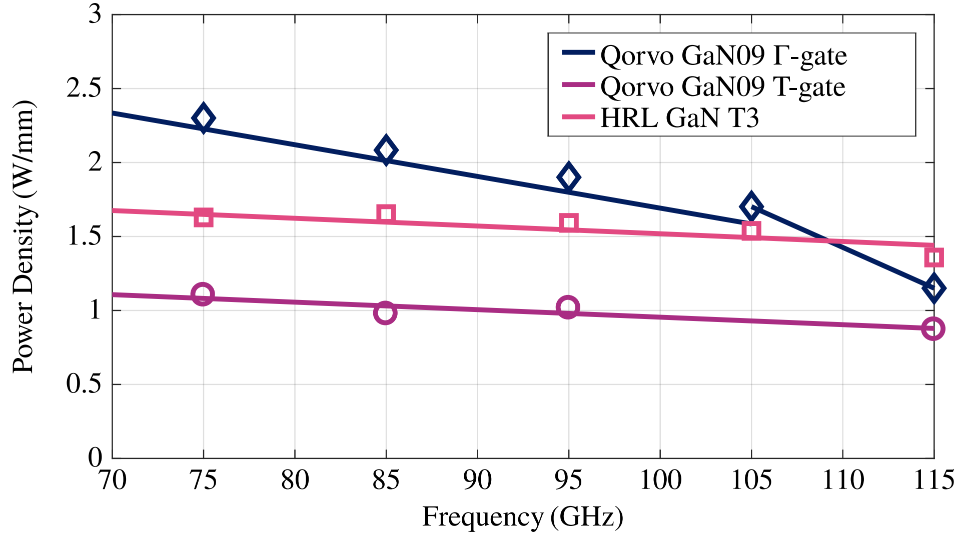


Figure 2.27: Power density at optimum power match and peak PAE comparison over W-band for Qorvo GaN09 Γ-gate and T-Gate, and HRL T3 processes.

Table 2.3: Summary of Millimeter-Wave Processes Optimum Source and Load Γ

Process	Maximum Gain Γ_{source}	Optimum Output Power Γ_{opt}	Optimum PAE Γ_{opt}
Qorvo GaN09 Γ-gate[1]	$0.82\angle 178°$	$0.85\angle 123.3°$	$0.83\angle 120.7°$
Qorvo GaN09 T-gate[2]	$0.77\angle 176.8°$	$0.75\angle 116.2°$	$0.80\angle 118°$
HRL T3 Process[3]	$0.72\angle 174.6°$	$0.65\angle 112°$	$0.73\angle 113°$

[1] P_{out}, PAE, and Gain based off 4×40 μm device model at 85 GHz.

[2] P_{out}, PAE, and Gain based off 4×40 μm device model at 95 GHz.

[3] P_{out}, PAE, and Gain based off 4×37.5 μm device model at 95 GHz.

Table 2.4: Summary of Millimeter-Wave Processes Large-Signal Metrics

Process	V_{DS} (V)	$I_{DS,dens}$ (mA/mm)	$P_{out,dens}$ (W/mm)	P_{out} (dBm)	PAE (%)	Gain (dB)
Qorvo GaN09 Γ-gate[1]	18	200	2.24	25.54	26.3	5.69
Qorvo GaN09 T-gate[2]	13	150	1.05	22.24	32	5.67
HRL T3 Process[3]	12	150	1.67	23.94	26.2	4.94

[1] P_{out}, PAE, and Gain based off 4×40 μm device model at 85 GHz.

[2] P_{out}, PAE, and Gain based off 4×40 μm device model at 95 GHz.

[3] P_{out}, PAE, and Gain based off 4×37.5 μm device model at 95 GHz.

Chapter 3

75-90 GHz W-Band MMIC PAs in Qorvo 90nm Γ-Gate Process

Contents

3.1 GaN09 Γ-gate Power Amplifier Single-Ended Design 32

3.2 GaN09 Γ-gate Power Amplifier Balanced Design 48

3.3 Conclusion 56

The W-band amplifiers summarized in Chapter 1 in Fig. 1.3 and Table 1.2 are considered currently the state-of-the-art for GaN millimeter-wave MMIC PAs. From Fig. 1.3, the benchmark for power density has been set by [6] using HRL's T2 process for highest power of 3 W peak power with broadest operating bandwidth. For highest W-band efficiency, the design presented in [38] show a peak PAE of >20% with a narrow frequency of operation at 91 GHz using Raytheon's GaN-on-SiC process.

This chapter presents two W-band power amplifiers designed in single-ended and balanced configurations using Qorvo's GaN09 Γ-gate research process that is designated for V-band (40 - 75 GHz) operation. The active devices presented in Section 2.3 are embedded into Qorvo's existing 3MI passive processing [31, 58] and summarized in Fig. 3.1. In Section 3.1, the unit solid-state PA (USSPA) is presented with

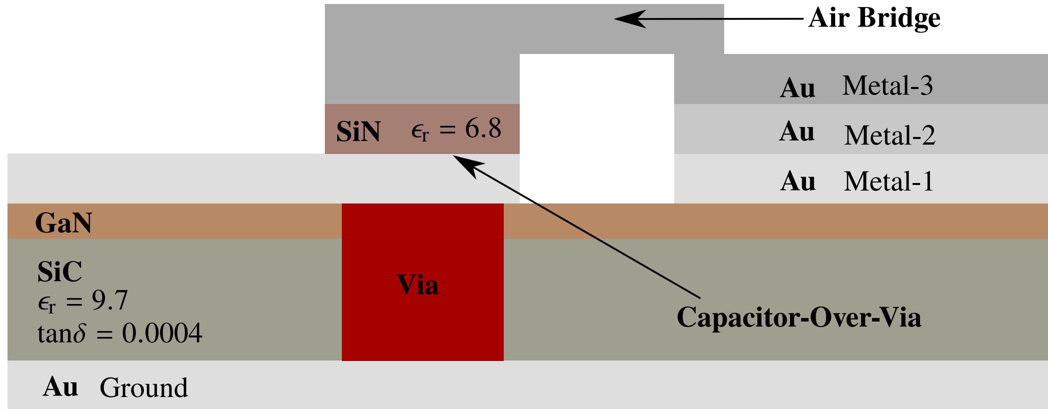


Figure 3.1: Qorvo 3MI process stack-up includes passive processing for microstrip operation containing three separate usable metallization. Process includes backside source vias, SiN dielectric layer for MIM capacitors, and TaN resistors. Additional capability for SiN processing over backside vias to form capacitors-over-vias. For GaN09, a SiC substrate thickness of 50 μm for millimeter-wave circuits is used. (Figure not to scale).

and subsequently used in two PA configurations. The design focuses on achieving maximal output power while using primarily distributed matching techniques and a compact biasing method in W-band. The shortcomings in using device technology above its designated operating frequency are presented and a brief discussion on linear stability analysis. On-wafer measurements of the USSPA in single-ended configuration are demonstrated. Section 3.2 presents the performance of the USSPA in balanced configuration with measured on-wafer results. Finally, the chapter concludes in Section 3.3 with a summary and comparison of the current W-band MMICs.

3.1 GaN09 Γ-gate Power Amplifier Single-Ended Design

3.1.1 Design and Layout

The designs presented here use the EEHEMT nonlinear models for a 4×40 μm devices that have been validated through measurements with performance given in Section 2.3.1 [68]. The device is load-pulled in simulation and the drain impedance chosen for maximum output power for the MMIC designs. From Fig. 2.8 in Section 2.3, the simulations for P_{out}, gain and PAE versus P_{in} at 85 GHz show a maximum output power of +25.54 dBm with corresponding PAE of 26.3 %. For initial network design procedures, the input

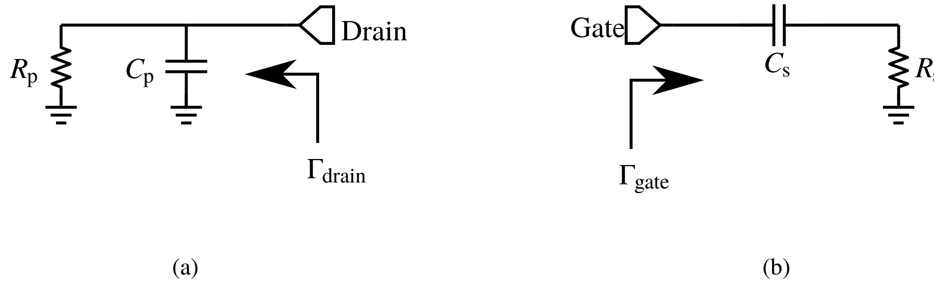


Figure 3.2: Approximate drain (a) and gate (b) equivalent circuits for device. This first-order approximation neglects bilateral effects is sufficient for preliminary network design in multistage amplifiers.

and output are modeled as parallel RC for equivalent drain model and series RC for equivalent gate model as shown in Fig. 3.2 (a) and (b), respectively. The optimal load reflection coefficient for maximum output power given in Section 2.3.1 is $\Gamma_{opt} = 0.85\angle 123.3°$ for 4×40 μm device, which corresponds to $R_p = 22.75\,\Omega \cdot \text{mm}$ and $C_p = 0.42\,\text{pF/mm}$. The source reflection coefficient for maximum gain is given by the conjugate of the gate reflection coefficient, $\Gamma_{source} = 0.82\angle 178°$, that corresponds to an R_s of 5 Ω and C_s of 2.55 pF. The gate values can also be given as densities, but as a note that though C_s scales with periphery, $N \cdot W_G$, R_s scales proportionally to W_G and inversely proportional to the number of fingers, N. For the 4×40 μm device, $R_s = 500\,\Omega/\text{mm}$ and $C_s = 15.94\,\text{pF/mm}$.

The overall output power is proportional by the output periphery of the amplifier given by,

$$P_{out} = \text{Periphery} \times P_{\text{device,dens.}} \times L_{\text{Combiner}} = N \times W_G \times P_{\text{device,dens.}} \times L_{\text{Combiner}} \tag{3.1}$$

where periphery is the number of fingers (N) times the transistor gate finger width (W_G), L_{Combiner} is the combiner loss, and $P_{\text{device,dens.}}$ is the output power density a technology is capable of achieving. Therefore, the choice of output periphery is dictated by output power requirements. For the USSPA design presented in this chapter, the primary design objective is to achieve state-of-the-art watt-level output power comparable to the MMICs summarized in Table 1.2. An output stage using four 4×40 μm devices will have a total periphery of 640 μm providing an output power greater than 1 W with a 2 W/mm power density of the GaN09 Γ-gate process.

The choice of the number of stages before the output power stage is dictated by the required gain for

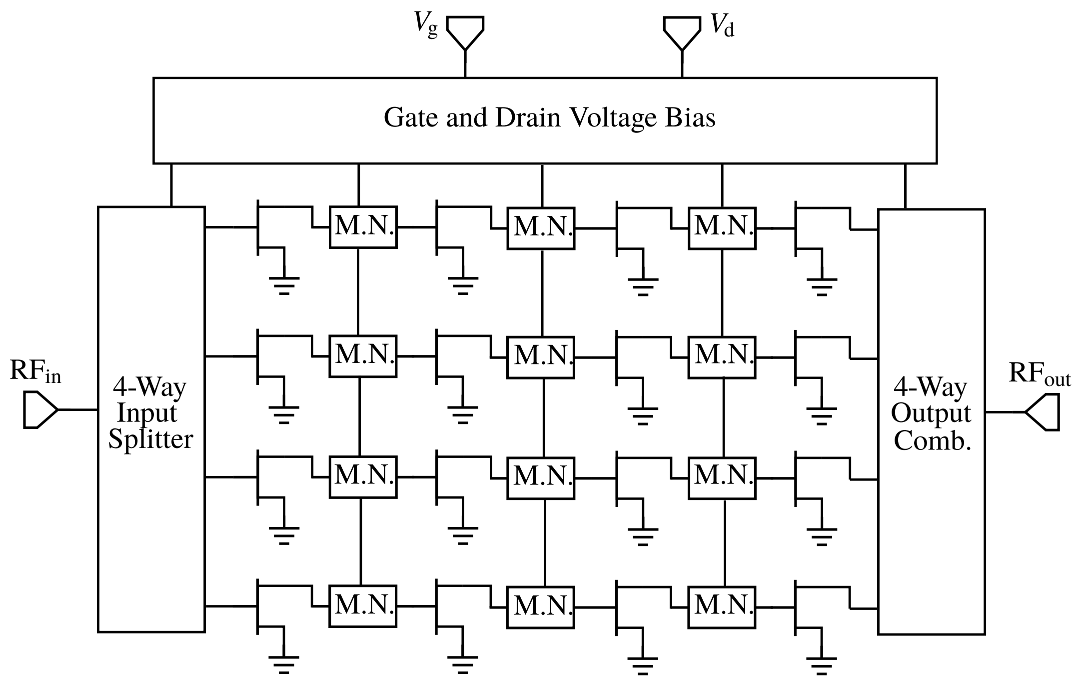


Figure 3.3: Schematic for USSPA of GaN09 Γ-gate single-ended power amplifier design. Design is a 4-stage, 4-way power combined architecture with 1:1:1:1 drive staging using 4×40 μm transistors.

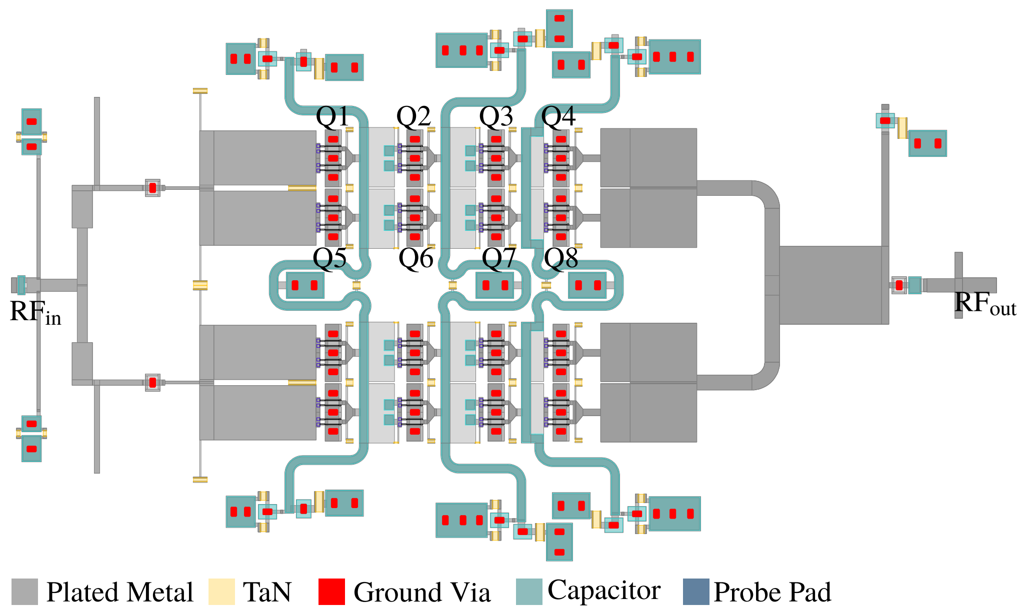


Figure 3.4: Qorvo GaN09 Γ-gate 4-stage, 4-way power combined USSPA design. The low impedance lines at input, interstages, and output combiner are used for matching.

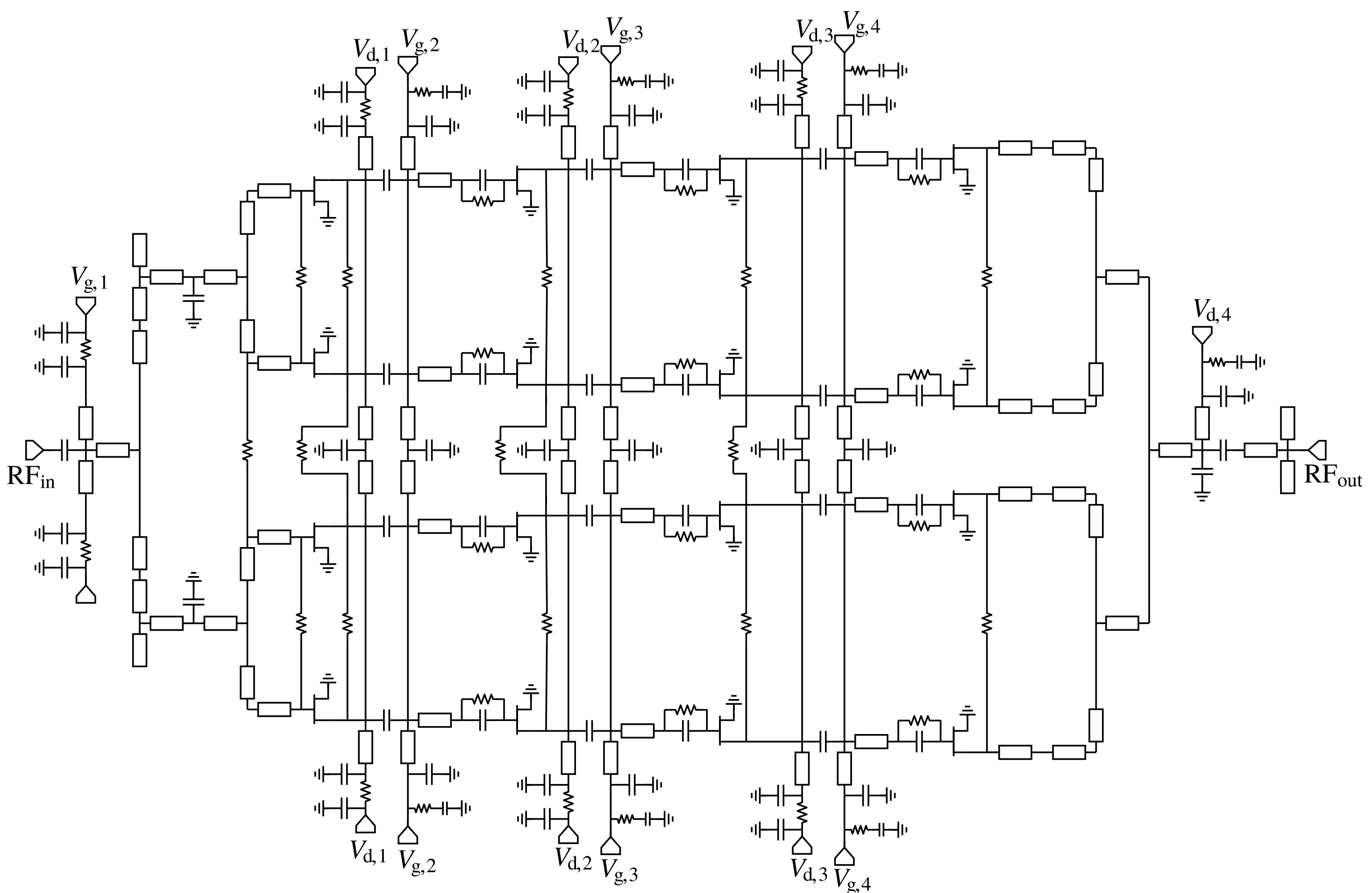


Figure 3.5: Schematic of the 4-stage, 4-way power combined USSPA design using Qorvo GaN09 Γ-gate, corresponding to the layout in Fig. 3.4.

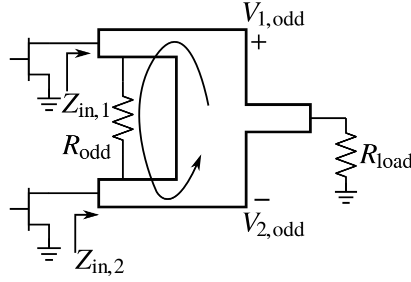


Figure 3.6: Schematic for two transistor combiner using odd-mode resistor. When $Z_{\text{in},1} \neq Z_{\text{in},1}$, a voltage differential occurs with $V_{1,\text{odd}}$ and $V_{2,\text{odd}}$, such that an oscillation may occur. Typically, R_{odd} is used to dissipate the odd-mode.

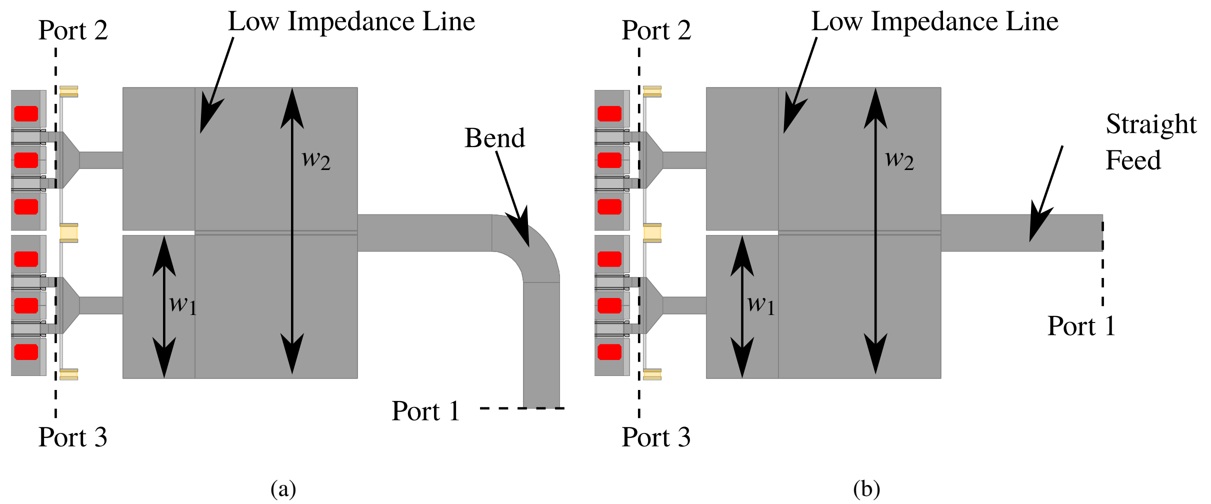
the amplifier. Since each stage prior to the output stage operates at a lower efficiency, additional gain stages contribute to the reduction in overall PAE. Therefore, it is desirable in many cases to limit the drive staging to reduce the overall DC consumption of the amplifier. The two primary issues faced with this approach for the GaN09 Γ-gate design are the following. First, since the transistor operates above the designated frequency range, the device gain is considerably lower, on the order of 2 dB, for a saturated transistor. This implies that the stage prior to the power stage will also be heavily compressed by using a 1:1:1:1 drive staging. Secondly, due to the limited availability of millimeter-wave load-pull measurements for non-linear device modeling, typical models are extrapolated from lower frequency load-pull measurements around a certain quiescent bias point and for a specific periphery. This implies that model validity is reduced when deviating from modeled periphery and bias conditions. For the GaN09 Γ-gate device, the transistor suffers from both of these disadvantages. Therefore, a four stage with 1:1:1:1 drive staging using the $4{\times}40\,\mu$m device at its modeled condition is used. The architecture, shown in Fig. 3.3, will increase the overall saturated gain and provide adequate compression of the output stage at the expense of PAE. The 1:1:1:1 drive staging offers the added benefit of achieving wider bandwidths within the interstage matching without further decreasing the periphery.

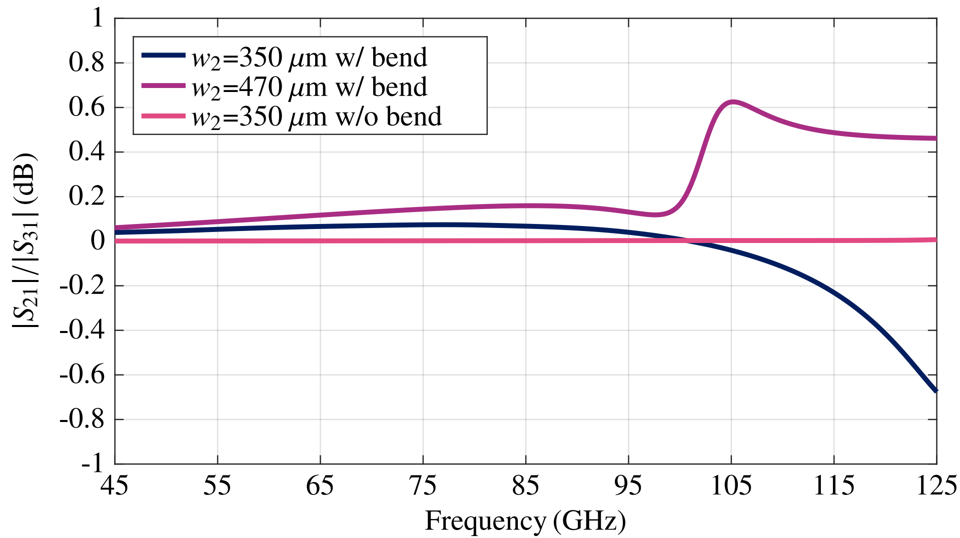
3.1.2 Network Design and Matching Topology

One of the most important objectives in power amplifier design is achieving low loss at the output matching and combining network. The combining efficiency are covered extensively in Chapter 6 and Chapter 7, but

here focuses on the on-chip reactive output combining. On MMIC, the primary role of the in-phase, parallel output combiner is to provide the reactive transformation from the optimum device impedance to 50 Ω with low loss and desired bandwidth. Millimeter-wave design methods for microstrip power combiners have been proposed in [69], but provide a narrowband solution. The challenge in the design of millimeter-wave power combiners is to obtain well-balanced impedance match at each of the combiner inputs for a broad frequency range. Changes in the reflection coefficient presented at the drain of the device become critical in maintaining even-mode operation of the combiner. Excessive imbalances at the input port place additional demands on the odd-mode resister placed between the transistors and contribute to added losses in the combiner. To make matters worse, undesired modes may get excited and further provide imbalances in the amplifier. An illustration is given in Fig. 3.6, for a two-way combiner.

An explanation on design issues for on-chip millimeter-wave power combiners is given next with performance shown for the GaN09 Γ-gate process. For the 4-way combiner used in the design, asymmetries on the quarter-symmetry plane cause unequal current crowding on curved microstrip segments that result in imbalances at the input of the combiner [70]. Current crowding compensation methods for MMIC designs in [5] are suitable for frequencies up to K_a-band, but these are ineffective above 50 GHz. In addition, the low-impedance transmission lines that provide low-Q matching desireable for bandwidth add complexity to the balance of the combiner. In W-band, asymmetries due to current crowding can excite undesired modes. In Fig. 3.7 (a) and (b), the first segment of the output combiner is shown with and without the bend placed after the combining node. The width, w_1, that is set to approximately half of w_2, is limited by the extraneous modes from the asymmetries caused by the bend in the structure. The magnitude balance shown over frequency presented in Fig. 3.7 (c), shows the extra mode being excited at approximately 100 GHz with $w_2 = 470\,\mu$m, that corresponds $w_2 = 0.47\,\lambda_g$. Reducing w_1 reduces the overall width of w_2 which increases the turn on frequency that is shown with the $w_2 = 350\,\mu$m curve. Therefore, while the highest characteristic impedance is set by fabrication processing and current handling, the lowest impedance usable in millimeter-wave MMICs is set by the width at which undesired modes can be excited. For output combiner presented here, this limit for usable microstrip transmission line impedance is $Z_o = [23, 67]\,\Omega$. The 4-way combiner performance is shown in Fig. 3.8 with a even-mode transmission parameter, T_e, between -2.2 dB





(c)

Figure 3.7: (a) Microstrip network for initial segment for the 4-transistor reactive combiner. (b) Microstrip network with port 1 moved passed the bend. (c) Imbalances in magnitude for splitters, $|S_{21}|/|S_{31}|$ for initial segment of combiner.

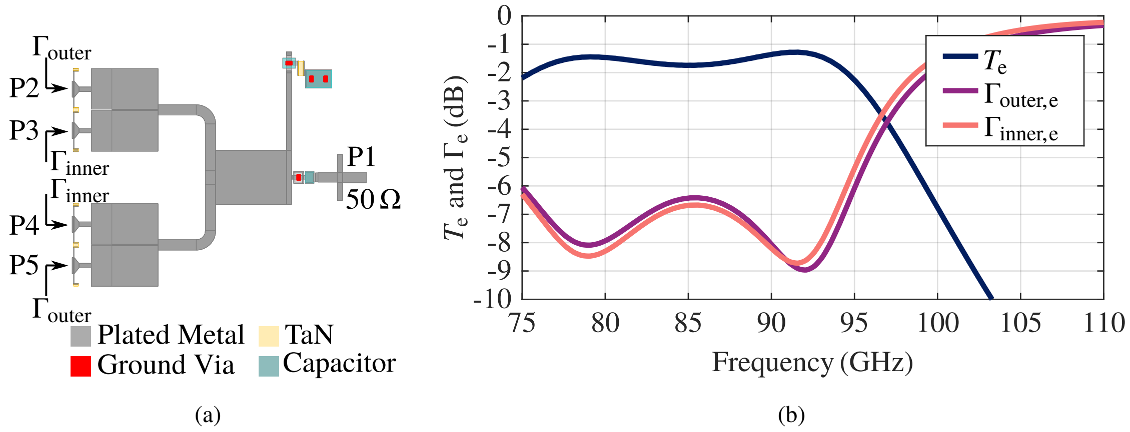


Figure 3.8: (a) Output combiner layout for with output at port P1 and sources at ports P2, P3, P4, and P5. Using symmetry, the input active even-mode reflection coefficients mirror about the center line such that $\Gamma_{2,e} = \Gamma_{5,e} = \Gamma_{outer,e}$ and $\Gamma_{3,e} = \Gamma_{4,e} = \Gamma_{inner,e}$. (b) Output combiner performance under even-mode operation such that the active transmission, T_e, and active reflection coefficient, Γ_e, are driven by synchronous sources.

and -1.29 dB for a frequency band 75-94.5 GHz. The active transmission parameter can be derived as in [71] for even- and odd-mode operation. For even-mode, $T_e = (S_{12} + S_{13} + S_{14} + S_{15})/2$, which assumes all sources on ports 2, 3, 4, and 4 are driven in-phase. Similarly, the active reflection coefficient can be calculated as $\Gamma_{outer,e} = S_{22} + S_{23} + S_{24} + S_{25}$ and $\Gamma_{inner,e} = S_{33} + S_{32} + S_{34} + S_{35}$. The output 4-way power combiner is optimized to achieve maximum output power and port balance by comparing the active reflection coefficient such that $\Delta\Gamma = |\Gamma_{outer} - \Gamma_{inner}|$ is minimized. A more rigorous approach to this method is continued in Chapter 6 for the analysis of combiners.

3.1.3 Bias Network Design

Biasing networks of multistage MMIC amplifiers can become space consuming. Large bypassing capacitors and close coupling microstrip lines can take up excessive wafer space and contribute to additional stability challenges. With a four-stage, four way amplifier, biasing gates and drains requires a total of 32 DC voltage paths.

The bias line topology used in the Γ-gate design utilizes multilayer MIM capacitors for voltage isolation between drains and gates. In addition, the capacitor is formed as a distributed multilayer transmission line that reduces the layout footprint. This topology with a single-sided chip biasing is compatible with the balanced

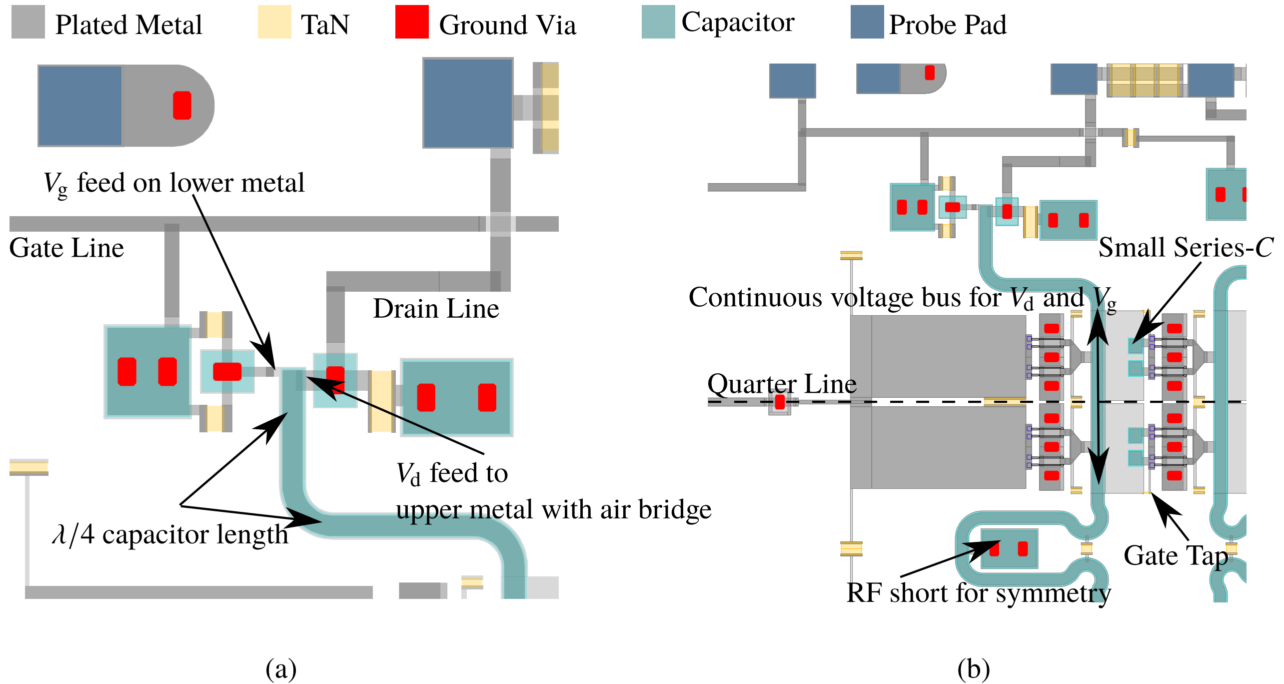


Figure 3.9: Compact biasing of a 4-stage power amplifier. Using Qorvo's 3MI process, a distributed capacitor transmission line $\lambda_g/4$ in length, provides isolation between gate and drain bias voltages with a bias bus to inner transistors. (a) Feed method at node of distributed capacitor which carries V_d on top metalization and V_g on lower metalization. The width of distributed capacitor is sized for current handling of drain current for all 4 transistors per stage. (b) The bias network topology provides RF at top and inner side of USSPA for symmetry while maintaining DC continuity.

configuration, presented in Section 3.2. Figure 3.9 shows the basic implementation for bias network design. Using the capability of the Qorvo 3MI process, the gate voltage, V_g, which carries negligible current, can be placed on the lower metalization level. The drain voltage, V_d, which carries the current for all 4 transistors per stage, can be placed on the thick top metalization. The length of the distributed multilayer transmission line is sized to provide an RF open at the interstage matching network. To achieve this, the distributed multilayer transmission line is approximately $\lambda/4$ in length, and its large capacitance provides an RF short between the two metal conductors while isolating both drain and gate voltages. The network is mirrored across the quarter-symmetry and thus provides RF half-symmetry across the center line of the MMIC. Though desirable in the space constrained MMIC design, this technique does provide some disadvantages. Due to the large series capacitance within the interstage, low frequency rejection for out-of-band gain is reduced and contributes to unwanted out-of-band low frequency gain, discussed further in Section 3.1.4. To provide

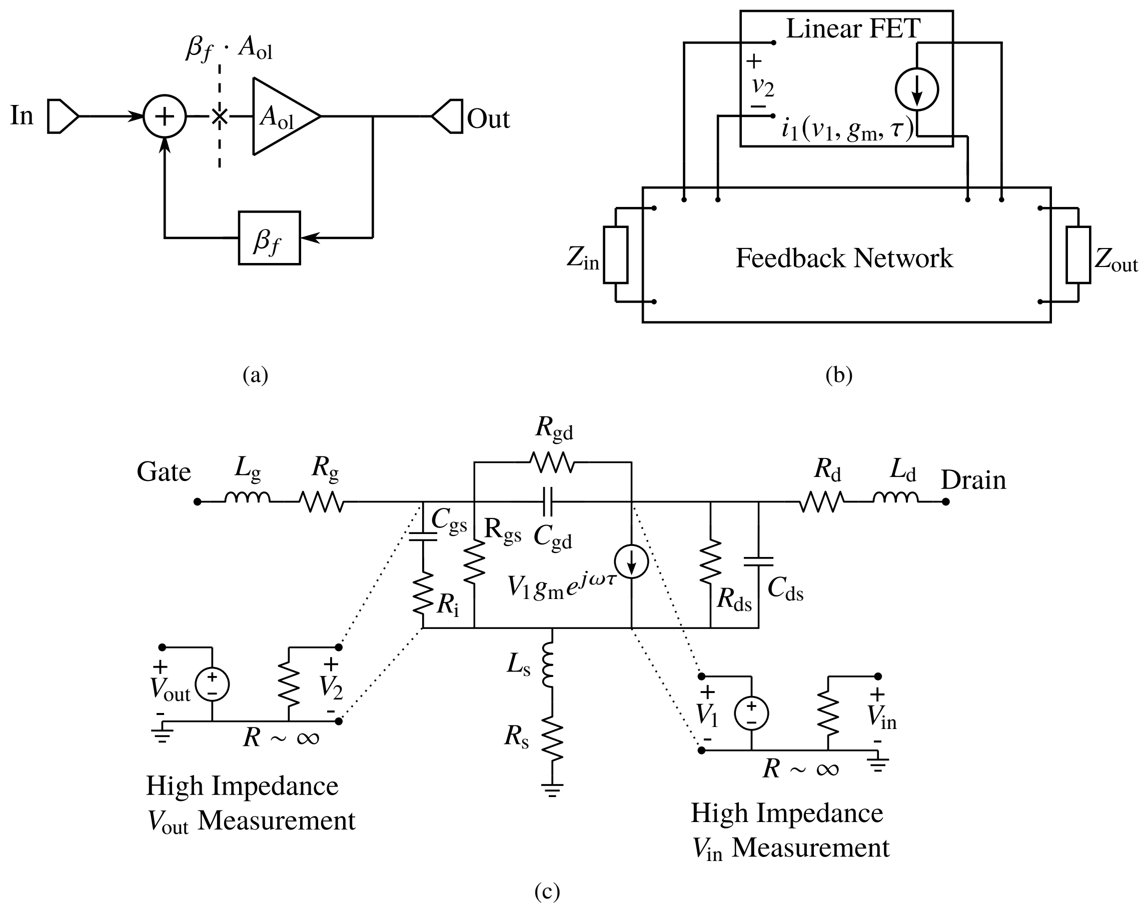


Figure 3.10: Method for stability using loop-gain is based on general feedback in (a) and calculation of the $\beta_f \cdot A_{ol}$ at the input of gain block, A_{ol}. The gain block can be represented as any linear FET device with a feedback network in (b) that includes; bias lines, other devices, matching network. A voltage controlled current source (VCCS) injects current i_1 in a small-signal model of linear FET device for calculation of $\beta_f \cdot A_{ol}$ [5].

some mitigation for this unwanted frequency response, small capacitors are place in series with the gates with a high RF impedance gate voltage tap to proved V_G to the device as shown in Fig. 3.9(b).

3.1.4 Method for Stability Analysis and Design Analysis

3.1.4a Stability Analysis Introduction

The methods for stability of MMIC power amplifiers are well documented in literature [72–77]. Applications of some of these methods to MMIC design, e.g. [78], are adopted for designs presented here and in Chapters 4 and 5. In the initial design phase, the amplifier is checked by using Rollet's stability criterion and observations

of the input and output reflection coefficents of the amplifier such that $|\Gamma_{\text{in,out}}| < 1$. This method is valid strictly only for single-stage amplifiers, observations for $K < 1$ provide good indications of possible instabilities where further stability analysis may be needed.

Further in the design phase, a more rigorous loop gain analysis based on classical feedback theory, defined by $A_{\text{cl}} = A_{\text{ol}}/(1 - \beta_f \cdot A_{\text{ol}})$ in Fig. 3.10(a) is used. The classical Barkhausen criterion designates that if $\beta_f \cdot A_{\text{ol}} = 1$, the necessary conditions for an instability may occur [79]. Implementation of the analysis is discussed in detail in [80] as return-ratio (RR), which is merely the inversion of $\beta \cdot A_{\text{ol}}$ such that $\text{RR} = -\beta_f \cdot A_{\text{ol}}$. The gain block in a MMIC can be represented as any single linear FET device with a feedback network that includes bias lines, other devices, matching networks, and any other path that can be lumped in a feedback network block as shown in Fig. 3.10(b). The benefit of this technique is that it does not require any a priori knowledge on the feedback configuration of the transistor, only proper simulation of suspected coupling mechanisms from output to the input [80]. As stated in [78], loop gain requires access to a single injection current source that involves fitting a non-linear transistor to its small-signal equivalent model. From Fig. 3.10(c), it is seen that this technique requires access to the dependent current source in the intrinsic model of the transistor. Additional circuit elements such as a lossy transmission line, provide further accurate modeling of the extrinsic parameters caused by the transistor manifolds of the gate and drain.

Internal Γ-probes at each of the gates and drains are used to further analyze Nyquist stability by non-invasive simulations of the amplifier [75, 81]. Using commercially available MMIC CAD software such as NI's AWR Microwave Office the Nyquist stability can be analyzed with built-in elements in the software. The Nyquist internal stability solves for $G_N = -\Gamma_1\,\Gamma_2$, which on a polar plot provides indication of instability with encirclement of -1 in a clockwise direction. The criterion is derived from one-port oscillation conditions of a component with impedance, Z_{in}, connected to a load with impedance, Z_{L}, with incident wave, a_{n}, such that the return wave is $a_{\text{L}} = a_{\text{n}}\Gamma_{\text{in}}/(1 - \Gamma_{\text{in}}\Gamma_{\text{L}})$. When $\Gamma_{\text{in}}\Gamma_{\text{L}} \geq 1$, the $1 - \Gamma_{\text{in}}\Gamma_{\text{L}}$ contributes to an unstable growing signal of a_{L}. While the example given presents instability with +1 encirclement, internal stability in NI's AWR Microwave Office uses a multiplication by -1 such that $G_{\text{N}} = -\Gamma_{\text{in}}\,\Gamma_{\text{L}}$, resulting in a negative -1 encirclement for Nyquist criterion of instability. For simplicity in analysis, the stability index, $SI = -\Re(G) = \Re(\Gamma_1\,\Gamma_2)$, will also be used that presents a possible instability of greater than zero within a

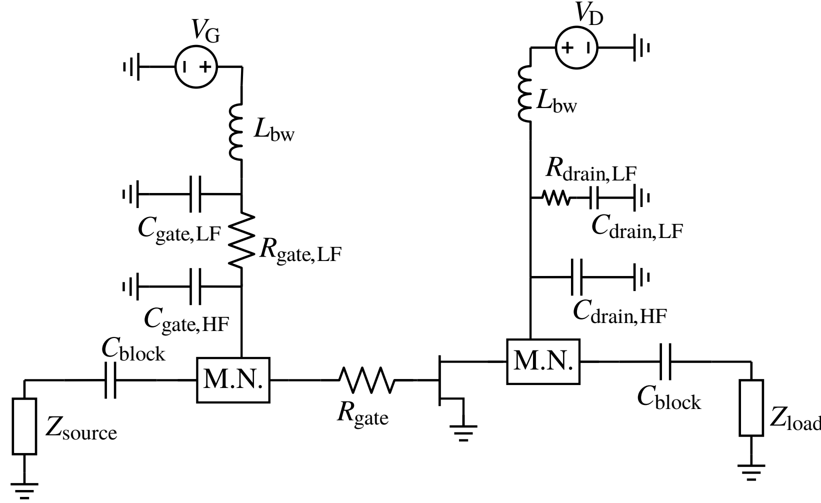


Figure 3.11: Stability circuits for millimeter-wave amplifier designs. $C_{gate,HF}$ before a large RC allows bypassing of in-band frequencies, while the series $R_{gate,LF} - C_{gate,LF}$ attenuates low frequencies. The drain line provides an equivalent function by removing $R_{gate,LF}$ for the drain current path to reduce the dissipative power on the bias line. Small DC blocking capacitors, C_{block}, are used to provide a high-pass response to further reject low-frequencies. For instabilities either in-band or close to the design band, a small series gate resistor, R_{gate}, stabilizes the transistor at the expense of gain.

90° phase margin.

3.1.4b Design for Stability and Results for Γ-gate USSPA

Up to now the discussion has only involved the techniques used in the analysis for stability of MMIC PAs. There are many circuit design techniques that are involved in ensuring amplifier stability. The high low-frequency gain of millimeter-wave devices causes challenges in both even- and odd-mode stability and must be addressed through careful design practices. The methods of analysis described in the previous section are performed to guide stabilization networks for in- and out-of-band stability targeting different instability issues. In addition, stability under process variations by increasing g_m by 30 %, decreasing C_{gs} by 30 % and increasing C_{gd} by 30 % must also be accomplished.

Figure 3.11 show various methods that are used for stabilization. On the main gate bias line, resistive bypassing is used to reduce low-frequency gain. Placing $C_{gate,HF}$ before a large RC bypasses the in-band frequencies with a non-resistive small capacitor, while the series $R_{gate,LF}C_{gate,LF}$ attenuates low frequencies. Similarly, on the drain line the equivalent while removing $R_{gate,LF}$ off the drain current flow path to reduce

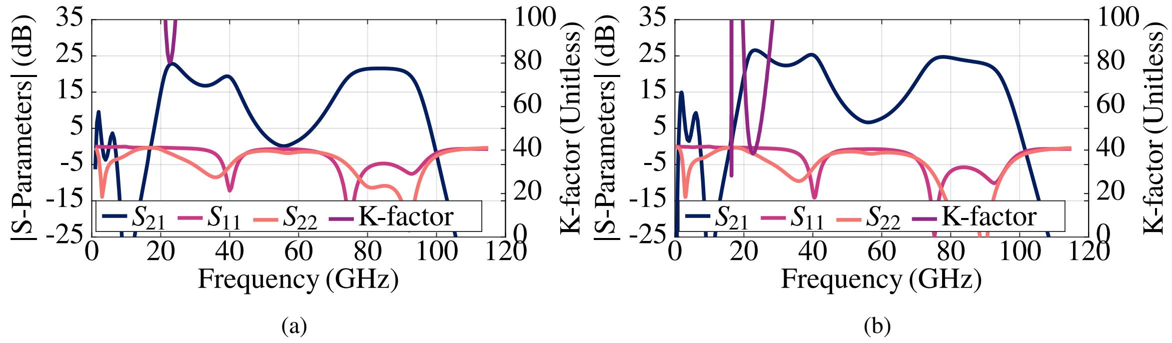


Figure 3.12: Simulated (b) g_{m} by 15 %, decreasing C_{gs} by 15 % and increasing C_{gd} by 15 %.

the dissipative power on the bias line. Small DC blocking capacitors, C_{block}, are used to provide a high-pass response to further reject low-frequencies. For instabilities either in-band or close to the design band, a small series gate resistor, R_{gate}, stabilizes the transistor at the expense of sacrificing gain.

In Fig. 3.12, the wideband frequency response from 0-115 GHz is shown for $|S_{21}|$, $|S_{11}|$, $|S_{22}|$, and K-factor. The K-factor for the complete amplifier is performed as initial stability analysis. Additionally, $|S_{11}|$ and $|S_{22}|$ are also analyzed across the whole wide band to ensure no frequencies have values greater than 0 dB. The amplifier is further simulated under process variations which show the limits of stability of the USSPA when increasing g_{m} by 15 %, decreasing C_{gs} by 15 % and increasing C_{gd} by 15 %. The additional stability metrics, Nyquist stability index and loop gain, are analyzed in Figs. 3.13 and 3.14 with and without process variation. Both metrics predict the USSPA to reach instability when increasing g_{m} by 15 %, decreasing C_{gs} by 15 % and increasing C_{gd} by 15 % at approximately 16 GHz.

The instability of the USSPA under process variations was alluded to earlier in the chapter in Section 3.1.3. The large series capacitance used for the bias lines within the interstage provided insufficient low-frequency rejection for out-of-band gain under the process variations. The wideband frequency response showed gain up to 20 dB at 16 GHz that proved to be a problematic region due to it being marginally stable without process variation. The results suggest that it may not be sufficient to obtain low frequency stabilization by only a few of the methods presented in Fig. 3.11, but require a composite of all to provide a band-pass response for the a design to ensure low-frequency stabilization even under process variations. Therefore, a design requiring significant out-of-band rejection requires the complete set of stability circuits shown in Fig. 3.11. The rigors

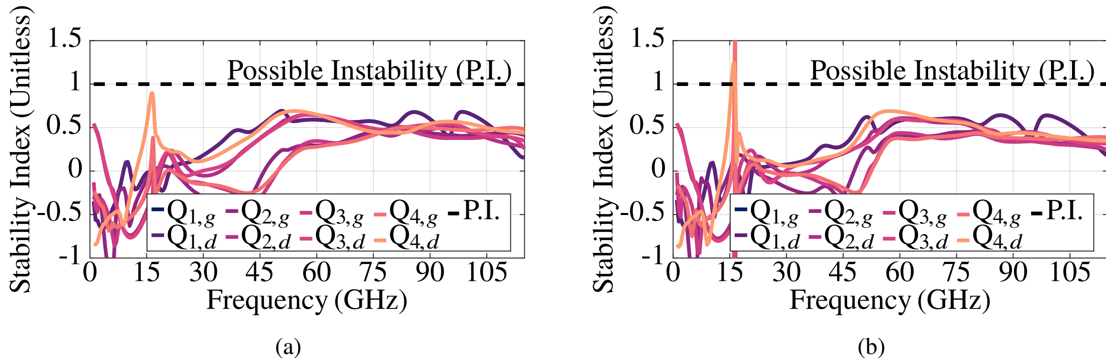


Figure 3.13: Nyquist stability index analysis for the USSPA without and with process variations in (a) and (b), respectively. (a) Marginal stability limits at $Q_{4,d}$ without process variations (b) Process variations are increased until stability index reaches greater than one. At g_m increased by 15 %, C_gs decreased by 15 % and C_gd increased by 15 %, the stability index is greater than one.

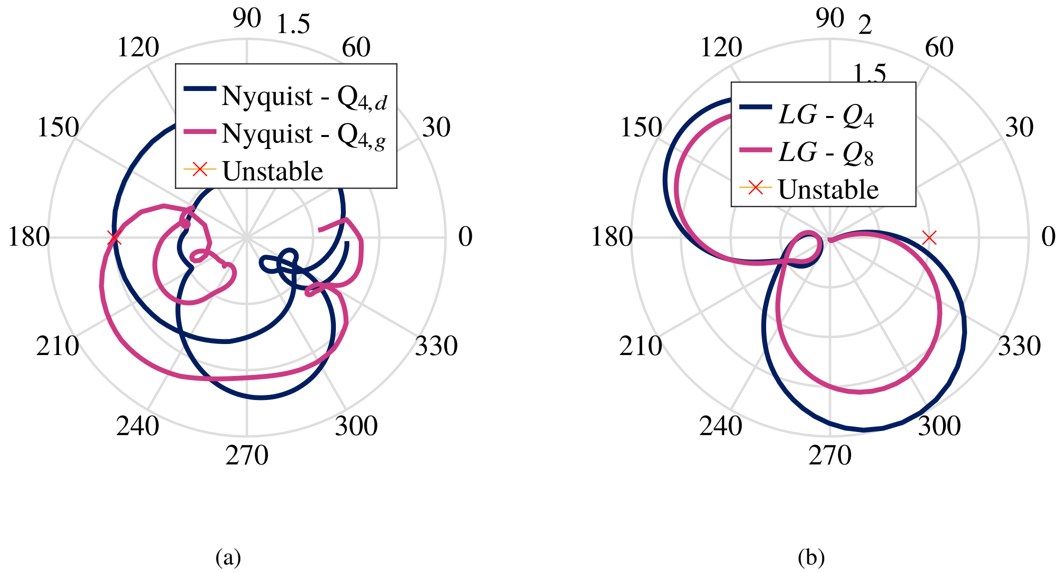


Figure 3.14: (a) Nyquist internal stability at Q_4 referenced to Fig. 3.4 with g_m increased by 15 %, C_gs decreased by 15 % and C_gd increased by 15 %. Both, gate and drain ports, show clockwise encirclement of -1 indicating instability with process variation. (b) Loop gain analysis at Q_4 and Q_8 with process variation show close encirclement of +1.

of this approach will be presented for the amplifier designs in Chapter 4 and Chapter 5.

3.1.5 Simulations for Single-Ended Design

The layout for the complete single-ended W-band MMIC amplifier is shown in Fig. 3.15. Additional bias routing to probe pads are placed on top side of the USSPA with resistors on the gate line at any crossover

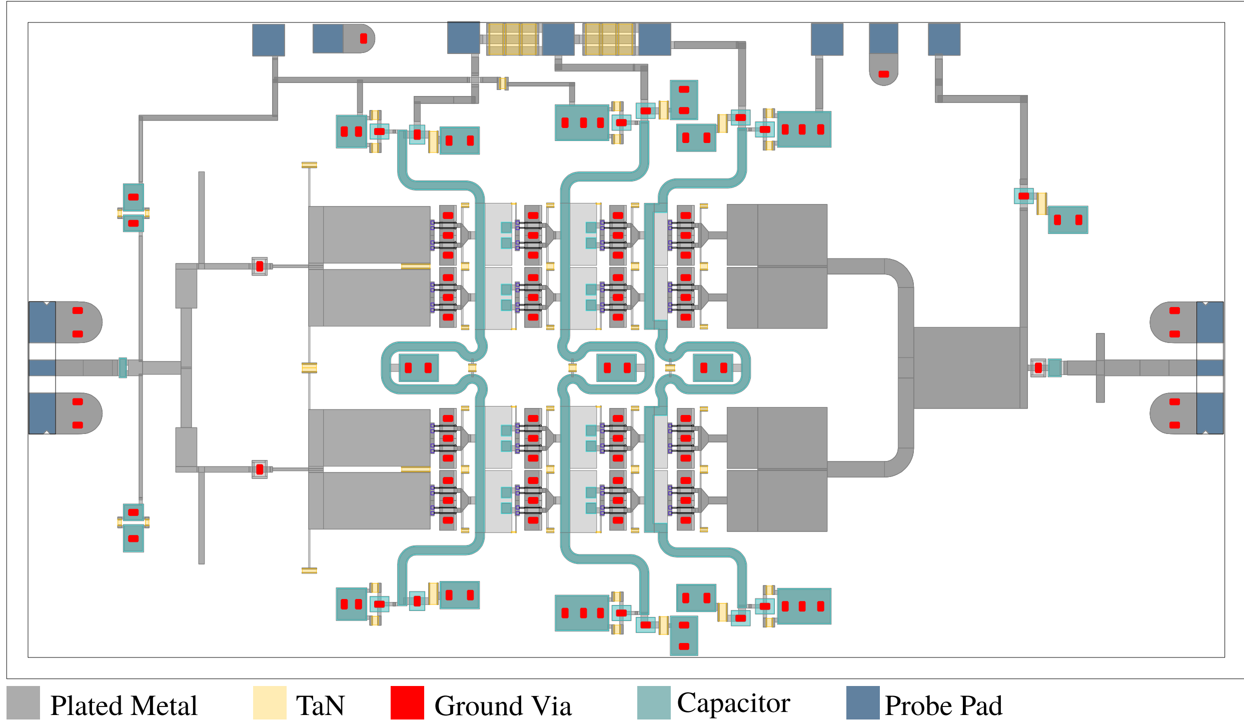


Figure 3.15: Layout for Qorvo GaN09 Γ-gate single-ended amplifier. Total chip size occupies 3.49×1.91 mm^2.

points [5]. The total chip size for the single-ended design occupies 3.49×1.91 mm^2. Simulation results for P_{out}, G_{sat}, and PAE over frequency response of the single-ended amplifier with +18 dBm RF input power are shown in Fig. 3.16, showing an output power of +29.6 dBm at 80 GHz and greater than +27 dBm over 76.6 GHz to 92.7 GHz. Results for P_{out}, G_{sat}, and PAE versus P_{in} at 85 GHz with +18 V drain supply and 200 mA/mm bias are shown in Fig. 3.17.

3.1.6 On-Wafer Measurements and Reverse Modeling

The fabricated single-ended amplifier is shown in Fig. 3.18. On-wafer small-signal measurements were taken across the wafer. Due to the developing process, low yield resulted in small-signal gain lower than predicted, by about 10 dB. A comparison of simulated versus on-wafer measurements for $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ are shown in Fig. 3.19. Good agreement of the shape of the frequency response is shown for $|S_{21}|$ and $|S_{11}|$. Reverse modeling is done using the small-signal FET model given Fig. 3.10(c) and the measured data with simulations shown in Fig. 3.20. Degradation in $|S_{21}|$ by approximately 10 dB show equivalent gain

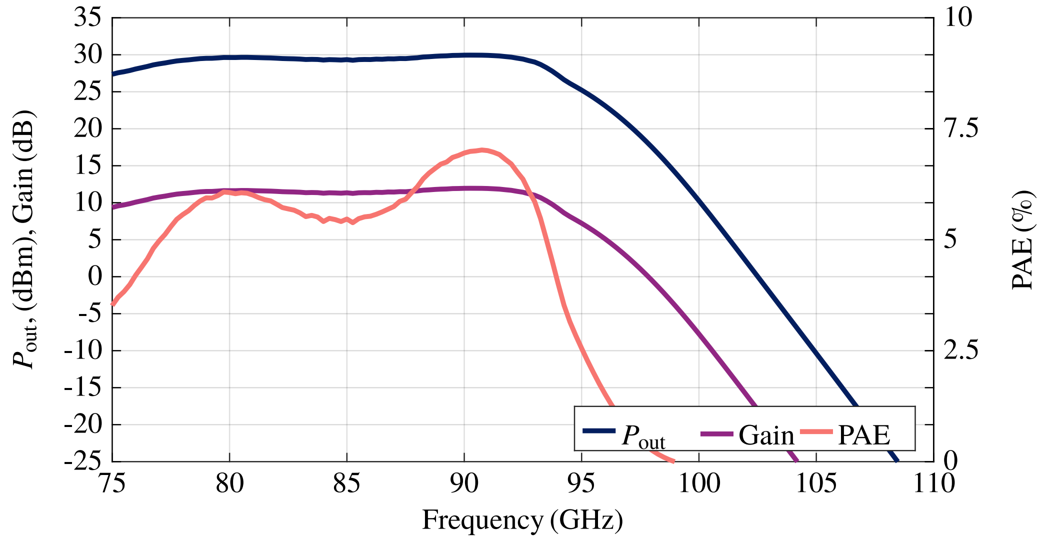


Figure 3.16: Simulated frequency response for the single-ended MMIC with P_{in} = +18 dBm under bias conditions (V_D, I_{DS})= (18 V, 200 mA/mm) for the 4×40 μm transistors.

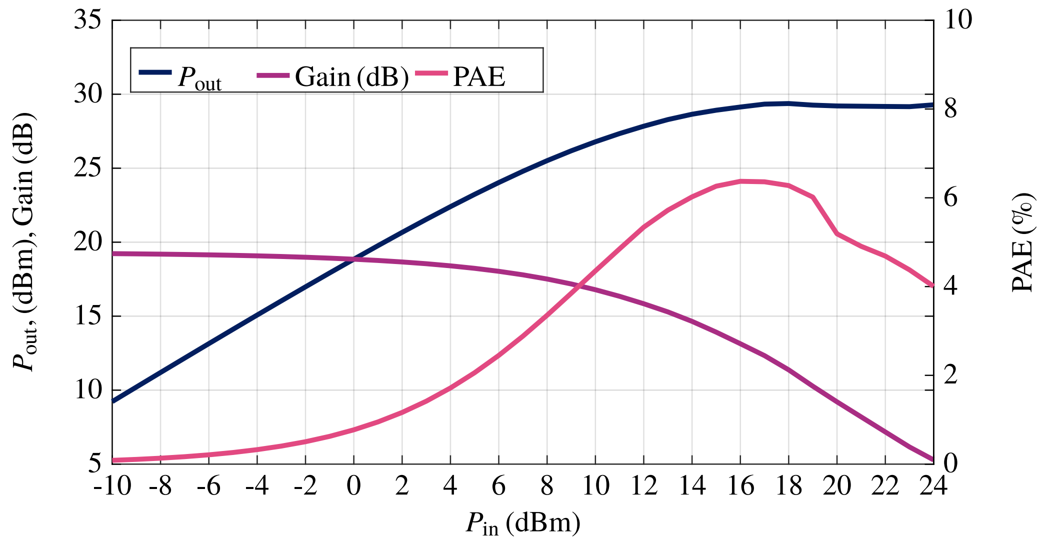


Figure 3.17: Simulated P_{out}, saturated gain and PAE versus P_{in} at 85 GHz of the single-ended MMIC design at a 18 V drain supply voltage with 200 mA/mm drain current.

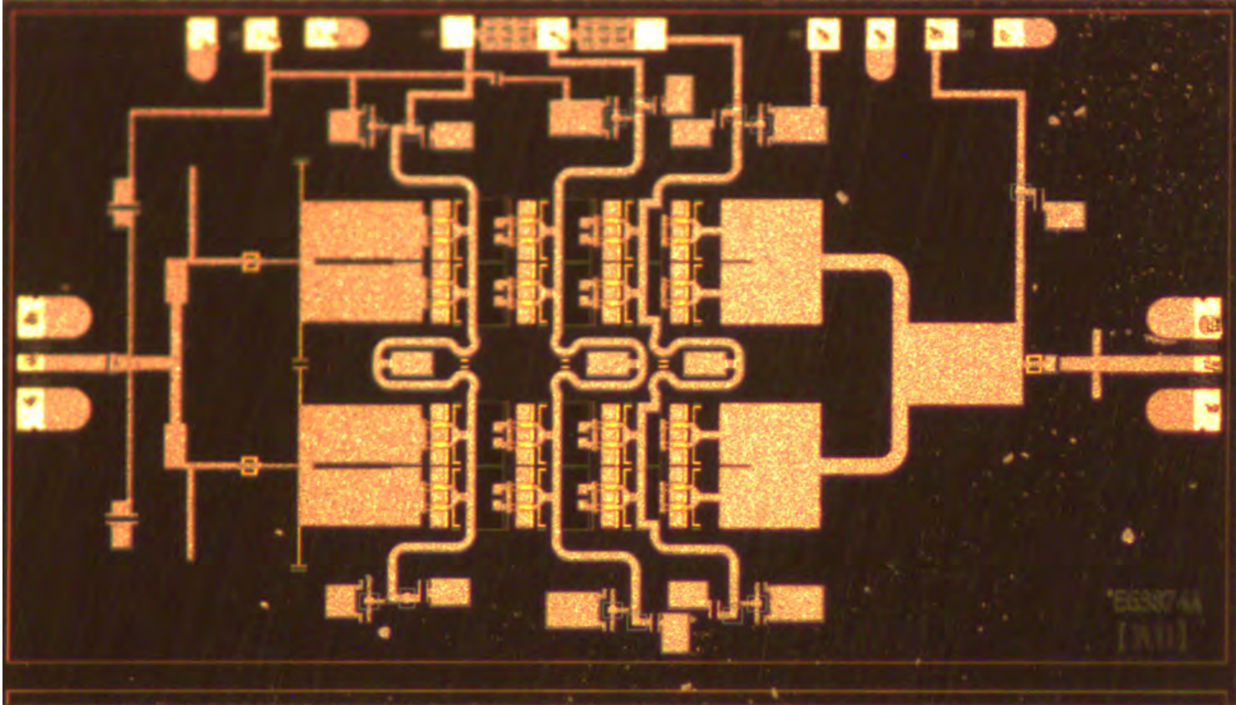


Figure 3.18: Photograph of Qorvo GaN09 Γ-gate single-ended amplifier for the layout shown in Fig. 3.15.

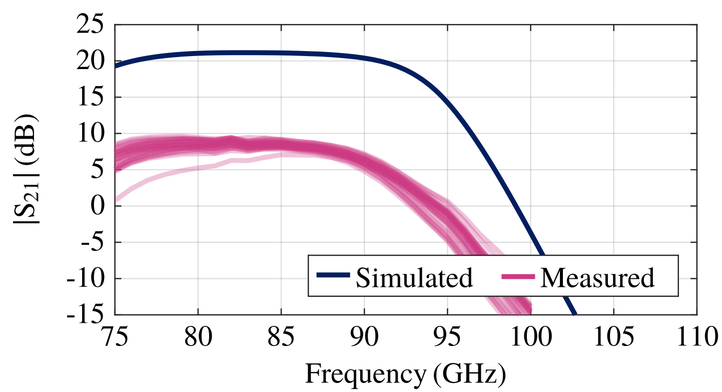
response by reducing the g_m by 45%.

3.2 GaN09 Γ-gate Power Amplifier Balanced Design

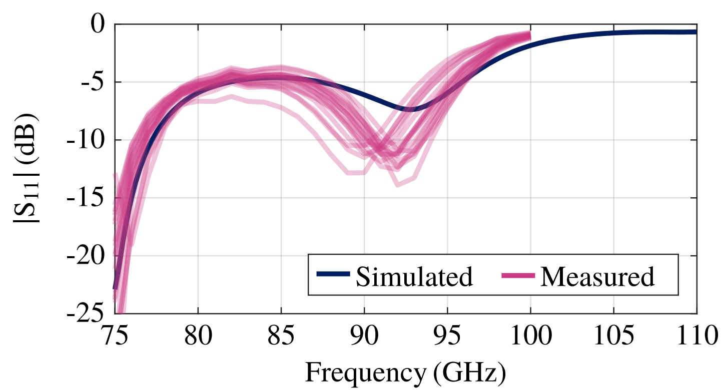
3.2.1 Design and Layout

One more level of power combining with Lange couplers in a balanced configuration increases the output power and improves input/output return loss for a second MMIC PA at the expense of doubling the layout area and DC consumption. The input and output return loss of the single-ended amplifier in Section 3.1 was sacrificed to extend the bandwidth. At worst case, the input $|S_{11}|$ reaches as high as -5 dB in simulation and measurement. In many cases it may be required to protect the PA from mismatched loads and a balanced amplifier accomplishes this. The general balanced amplifier architecture places the USSPA between two hybrid, 3 dB couplers shown in Fig. 3.21.

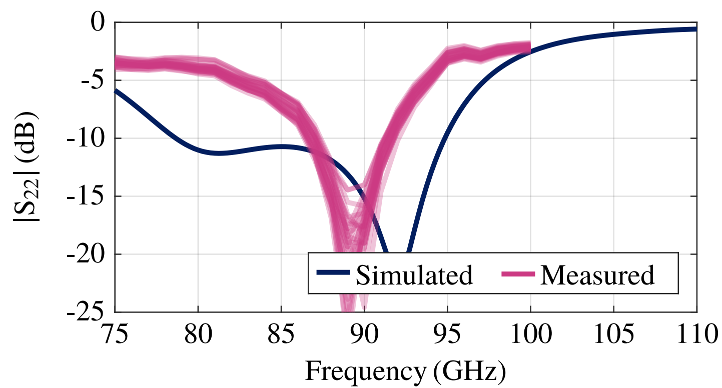
The single-ended amplifier is used for the the unit amplifier and placed between two Lange hybrid



(a)



(b)



(c)

Figure 3.19: Simulated versus measured for on-wafer Qorvo GaN09 Γ-gate single-ended amplifier for (a) $|S_{21}|$, (b) $|S_{11}|$, and (c) $|S_{22}|$.

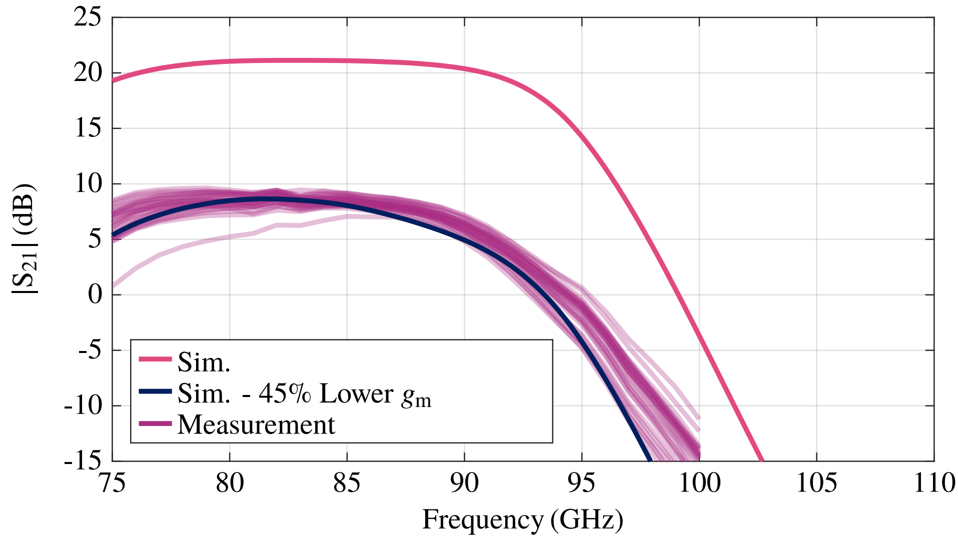


Figure 3.20: Reverse modeling for GaN09 Γ-gate single-ended amplifier. Simulation of $|S_{21}|$ with 45% lower g_m show more approximated fitting to on-wafer probe measurements.

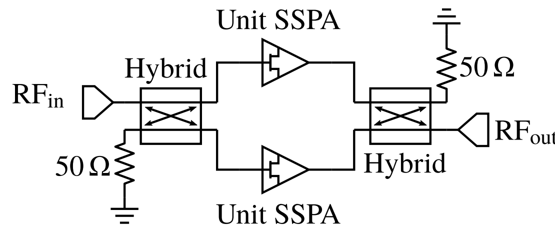


Figure 3.21: Block diagram for a USSPA in balanced architecture. Hybrid typically designed using 3 dB Lange couplers for bandwidth.

couplers. At W-band wavelengths a Lange coupler implemented with a length of 360 μm and finger width of 5 μm and finger spacing of 4 μm provides 3 dB coupling over the 75-110 GHz band. The isolated resistor for the output Lange combiner is sized to provide sufficient current handling under worst-case imbalanced operation. The MMIC layout of the balanced amplifier is shown in Fig. 3.22 with a footprint of 3.98×3.76 mm^2.

The simulated frequency response of the balanced amplifier with +21 dBm input power is presented in Fig. 3.23, with an output power of +29.6 dBm at 80 GHz and greater than +27 dBm over +28 dBm output power over 76.6 GHz to 92.7 GHz. The simulations predict greater than 1 W of power over 75 GHz to 93.5 GHz, with peak output power of 1.88 W at 79.75 GHz and peak PAE of 6% at 91.25 GHz. Input and

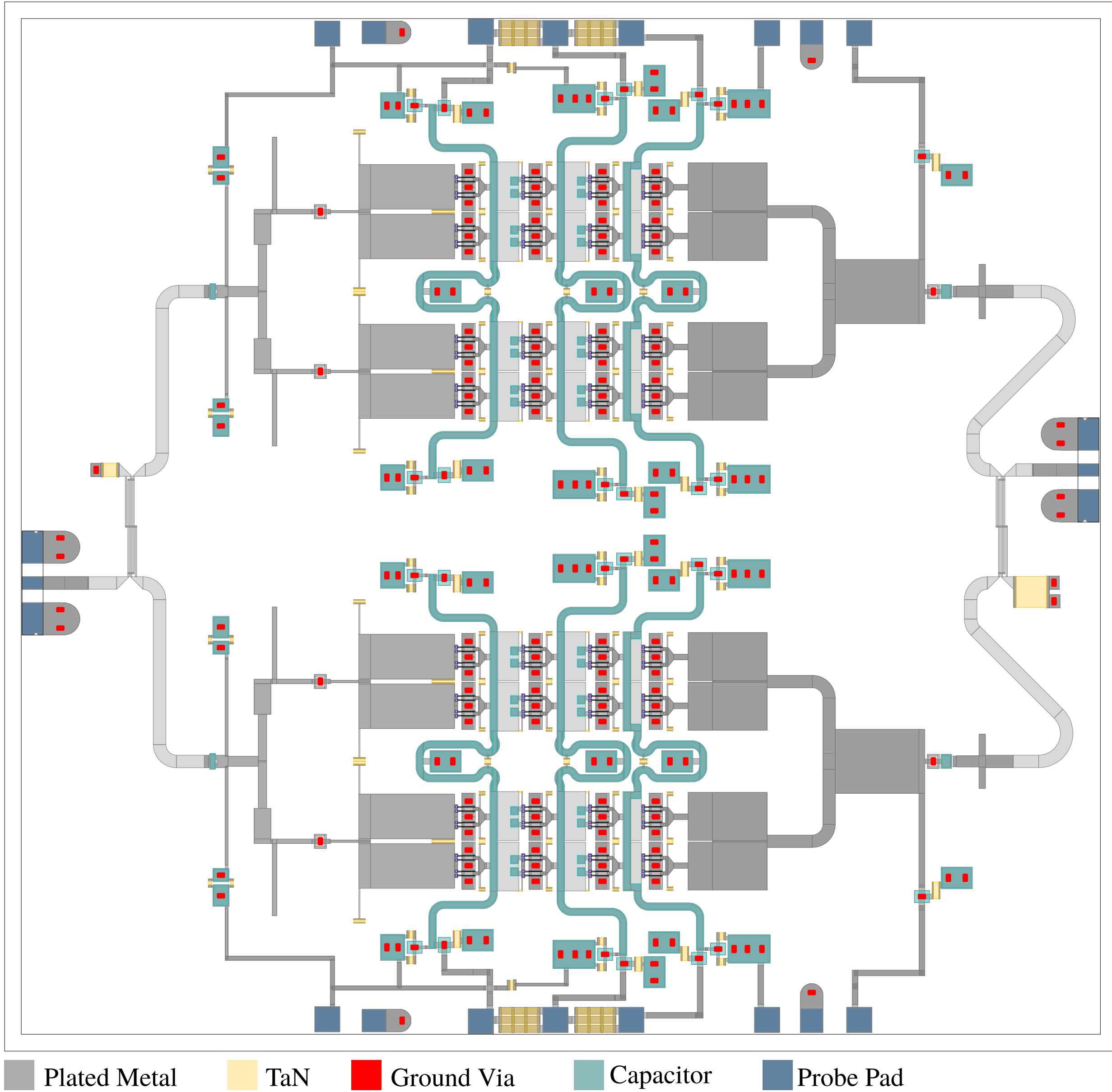


Figure 3.22: Layout for Qorvo GaN09 Γ-gate balanced amplifier. Total chip size occupies 3.82×3.68 mm^2.

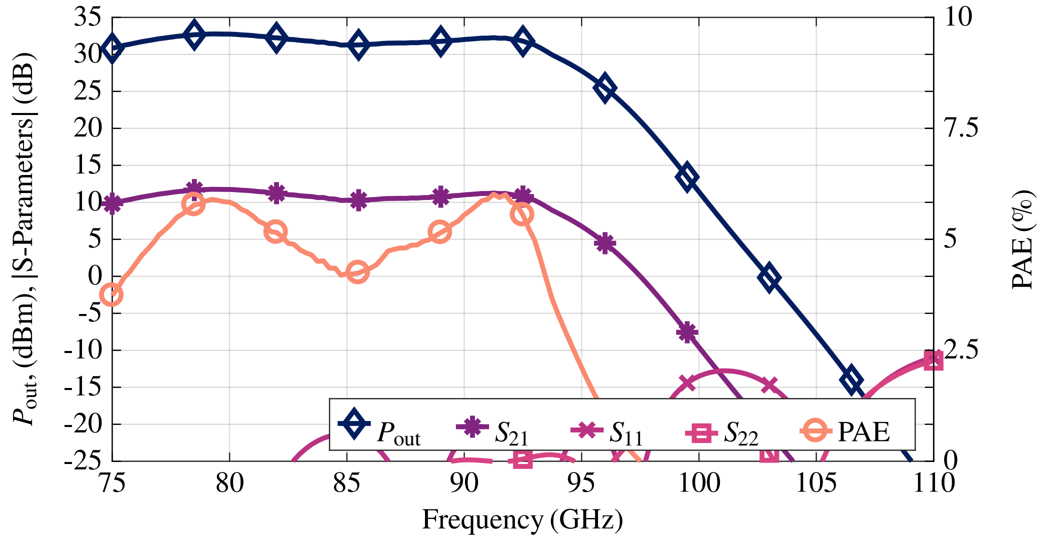


Figure 3.23: Simulated frequency response for the balanced MMIC amplifier with +21 dBm RF input power at (V_D, I_{DS})= (18 V, 200 mA/mm) for the 4×40 μm transistors.

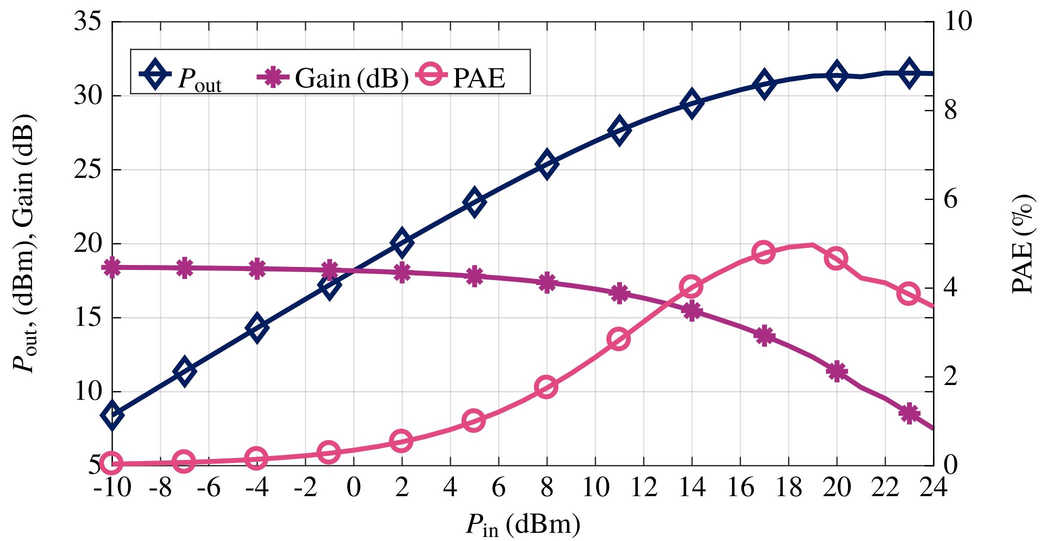


Figure 3.24: Simulated P_{out}, saturated gain and PAE vs. P_{in} at 85 GHz of the balanced MMIC design at a 18 V drain supply voltage with 200 mA/mm drain current.

output return loss is improved with worst case return loss of 19.44 dB. Simulation results for P_{out}, G_{sat} and PAE vs. P_{in} at 85 GHz of the balanced PA with 18 V drain supply and 200 mA/mm bias are shown in Fig. 3.24.

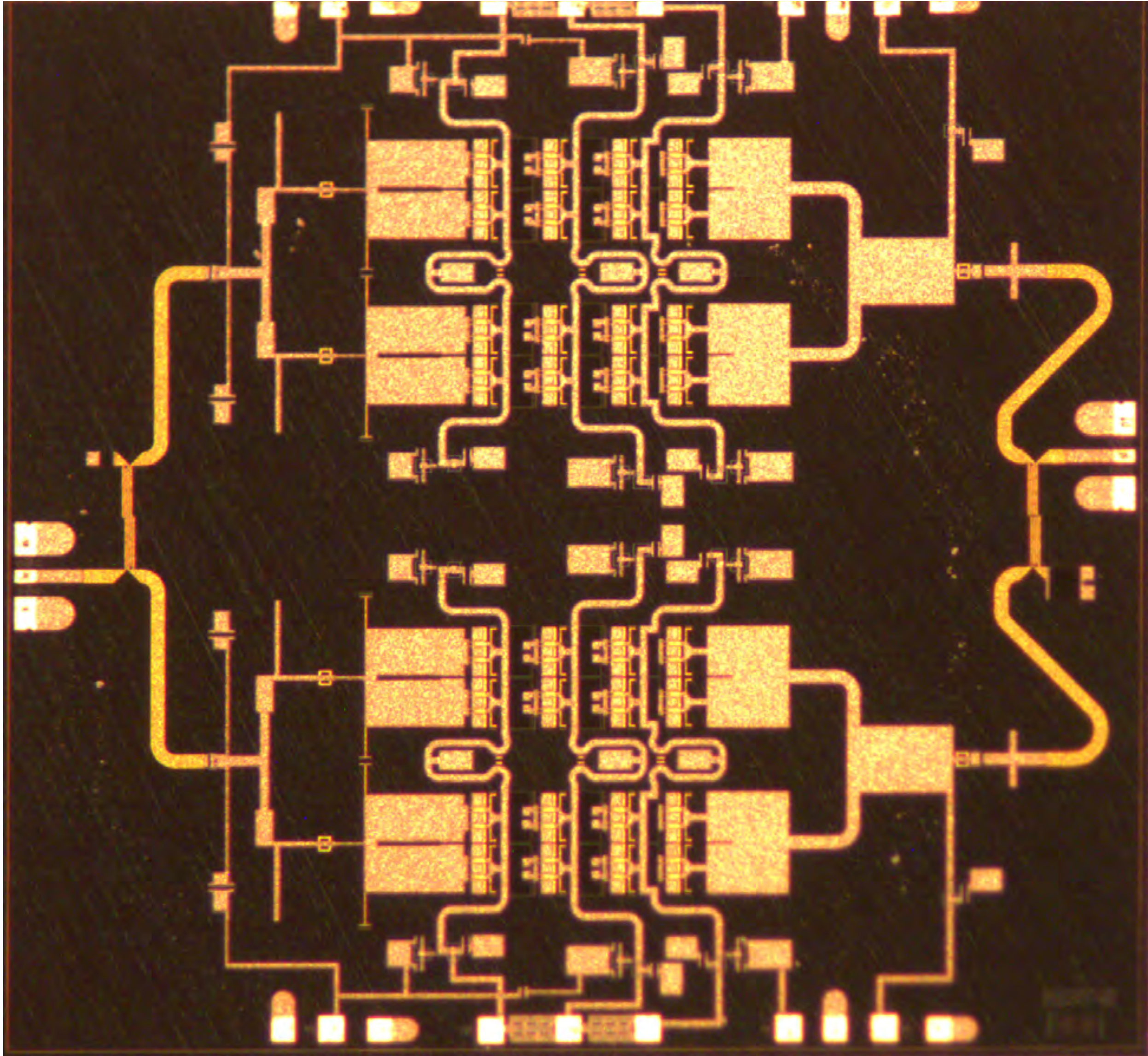
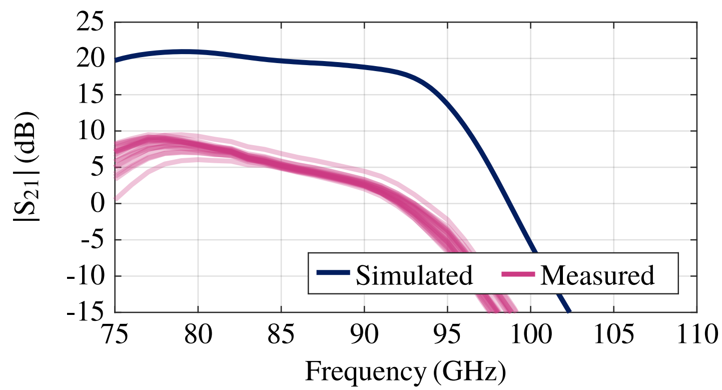


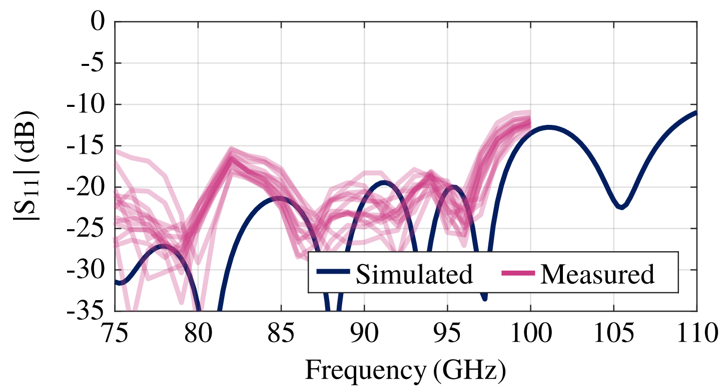
Figure 3.25: Photograph of Qorvo GaN09 Γ-gate balanced amplifier.

3.2.2 On-Wafer Measurements and Reverse Modeling

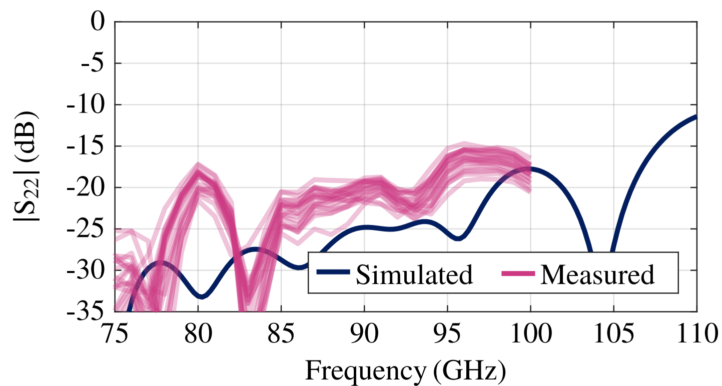
The fabricated balanced design is shown in Fig. 3.25 with on-wafer small-signal measurements taken across the wafer for $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ shown in Fig. 3.26. Similar to the single-ended amplifier, the reverse modeled balanced amplifier comparison using the small-signal FET model in Fig. 3.10(c) is shown in Fig. 3.27 with reduced g_m by 45%.



(a)



(b)



(c)

Figure 3.26: Simulated versus measured for on-wafer Qorvo GaN09 Γ-gate balanced amplifier for (a) $|S_{21}|$, (b) $|S_{11}|$, and (c) $|S_{22}|$.

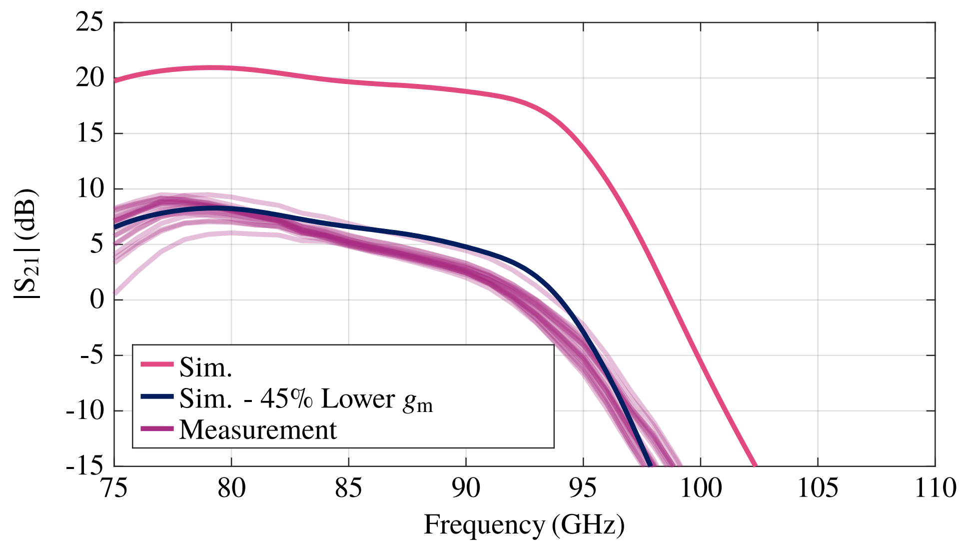


Figure 3.27: Reverse modeling for GaN09 Γ-gate balanced amplifier. Simulation of $|S_{21}|$ with 45% lower g_m show more approximated fitting to on-wafer probe measurements.

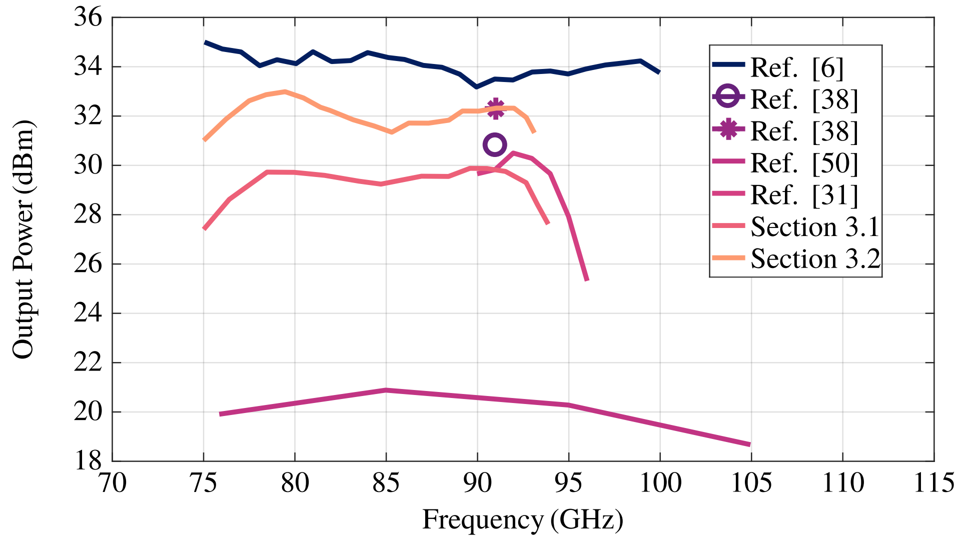


Figure 3.28: Output power versus frequency for state-of-the-art MMIC at W-band including Qorvo GaN09 Γ-gate designs presented in Sections 3.1 and 3.2.

3.3 Conclusion

The work presented in this chapter show the analysis and design of two W-band power amplifier using Qorvo's GaN09 Γ-gate process. Summary of performance compared to state-of-the-art are given in Fig. 3.28 and Table 3.1. In addition, a design method of a bias line topology that utilizes multilayer MIM capacitors as a distributed multilayer transmission line for voltage isolation is presented. The design method provides a reduction in MMIC layout footprint. The contributions of this chapter are presented in [82].

Table 3.1: GaN09 Γ-gate Compared to Published GaN MMIC Power Amplifiers at W-Band

Reference	Peak Output Power (W)	Bandwidth (GHz)	PAE (%)	Chip Size (mm^2)
[83]	3	75-100	12	5.4 × 2.75
[38]	1.2	91	20	2.5 × 0.9
[38]	1.7	91	11	2.9 × 1.6
[46]	0.5	70-75	10	3.5 × 1.75
[47]	0.842	83-92	14.8	-
[45]	1.5	92-96	17.8	-
Section 3.1 (single-ended)	0.979	76.6 - 92.7	5.8	3.5 × 1.91
Section 3.2 (balanced)	1.88	76.6 - 92.7	5	3.98 × 3.76

Chapter 4

75-108 GHz W-Band MMIC PAs in Qorvo 90nm T-Gate Process

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4.4 Conclusion 76

Recent published W-band amplifiers in [31] have showed promising capability with the Qorvo GaN09 T-gate process achieving 1.2 W at 95 GHz. With its high f_T > 145 GHz, high g_m > 1000 mS/mm, and integrated 3MI passives, the GaN09 T-gate process provides capability for state-of-the-art W-band power amplifiers.

This chapter presents the design of two MMIC PAs using Qorvo's GaN09 T-gate process and exploiting their state-of-the-art 3MI passive processing. In Chapter 3, the designs use distributed matching networks for impedance matching at the input, interstage, and output. Though desirable for millimeter-wave design, distributed matching networks require costly reticle space due to wide impedance lines needed. The designs

presented in this chapter take advantage of quasi-distributed matching techniques that provide reduction in overall MMIC design footprint and exploit state-of-the-art advanced passive processing of small capacitor-over-via (COV) presented in Fig. 3.1. This allows for the use of smaller valued capacitor for impedance matching, providing the capability to increase the amplifier's output periphery by up to 20% with equivalent die space to that of what was presented in Section 3.1.

To achieve larger bandwidths, a reduced output periphery over that presented previously in Section 3.1 is used. Moreover, to achieve higher output periphery with the USSPA, two MMIC amplifier topologies are shown: (1) balanced configuration similar to that of Section 3.2 and (2) a 5× combined amplifier using a serial combiner with total output periphery of 1600 μm. An extended analysis of on-chip Lange couplers at millimeter-wave frequencies for improved combining efficiencies is shown.

4.1 GaN09 T-gate Unit Power Amplifier for PA Architecture

4.1.1 Design and Layout of USSPA

The unit PA is a 3-stage, 2-way power combined topology with 1:1.5:2 drive staging, shown in Fig. 4.1(a). The output stage utilizes two 4×40-μm devices in parallel to provide a total periphery of 320 μm. In contrast to the design presented in Section 3.1, the output periphery is reduced by half to achieve larger bandwidths at the expense of output power. The layout of the 3-stage, 2-way power combined USSPA is presented in Fig. 4.1(b), with a compact total area of 2.75×0.64 mm^2. The complete schematic for the USSPA is shown Fig. 4.2.

With the inherently higher gain of the T-gate process, higher staging ratios can be chosen over the 1:1:1:1 presented in Chapter 3. Increased g_m of the device result in fewer gain stages, thus increasing the overall PAE of the amplifiers. Using non-linear EEHEMT models for 2×40 μm and 4×40 μm, a periphery for stage 1, 2, and 3 is chosen for 160 μm, 240 μm, and 320 μm, respectively. This drive staging corresponds to 1:1.5:2, allowing the drive stages to operate more efficiently. The bias conditions are kept at the modeled quiescent current, 150 mA/mm that corresponds to class-AB operation. For stage 1, 2, and 3, the drain current correspond to 24 mA, 36 mA, and 48 mA, respectively.

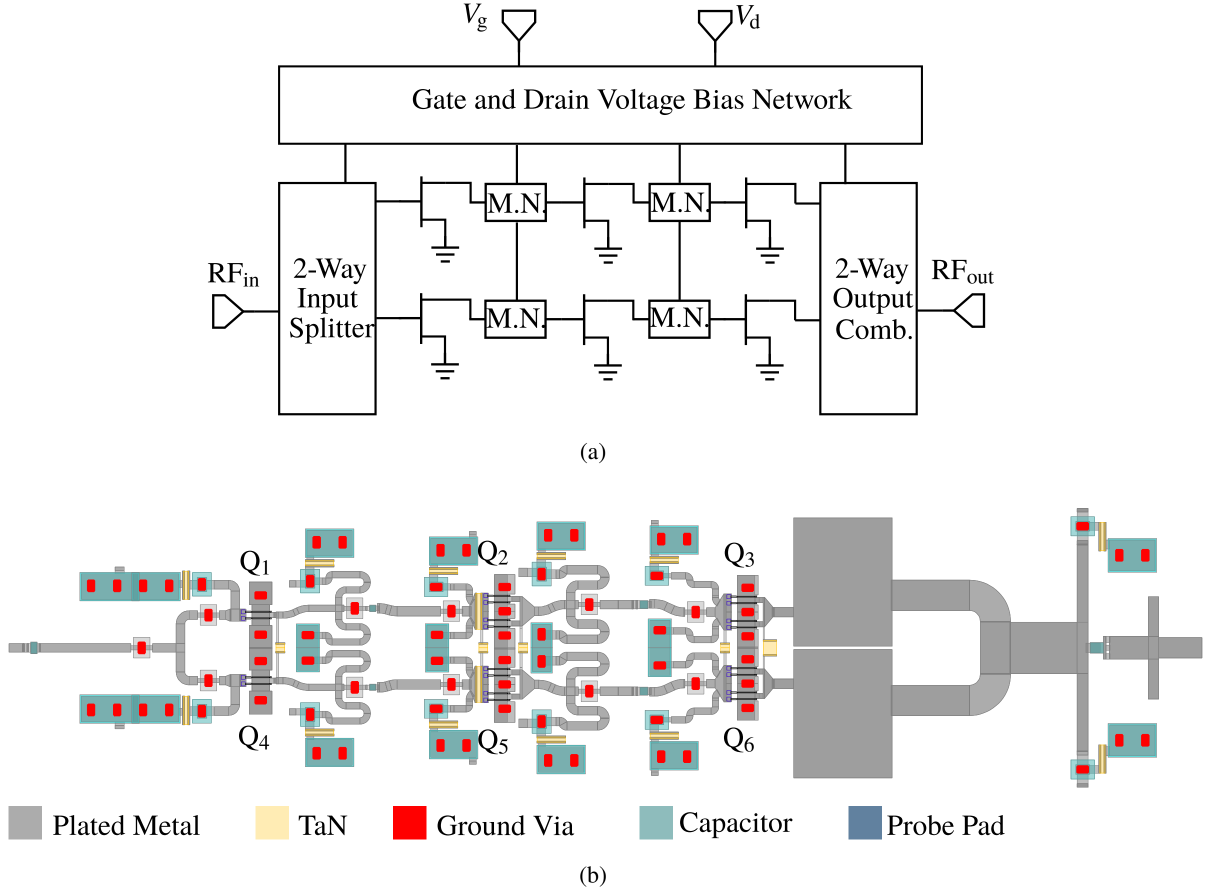


Figure 4.1: (a) Architecture for the GaN09 T-gate USSPA power amplifier design. The design is a 3-stage, 2-way power combined architecture with 1:1.5:2 drive staging using 2×40 μm, 4×30 μm, and 4×40 μm transistors for the first, second, and third stage, respectively. (b) Layout of the GaN09 T-gate MMIC USSPA with maximum dimensions of 2.75×0.64 mm^2.

4.1.2 Network Design and Matching Topology

The layout of the USSPA is presented in Fig. 4.1(b), showing the quasi-distributed matching techniques used for the input and interstages. To maintain low conduction losses at the output combiner, distributed matching techniques are used. As an initial design pass, each network is designed separately with equivalent *RC* circuits for gate and drain terminations. Similar to the procedure described in Chapter 3, the devices are approximated with series and parallel *RC* networks. Using the EEHEMT device models for the 2- and 4-finger transistors, their equivalent *RC* values are found. For the output power stage, the simulated load-pull value found in Section 2.3 for the 4×40 μm device is $\Gamma_{opt} = 0.75\angle 116.2°$, that corresponds to a $R_p = 104.7\,\Omega$ and $C_p = 0.05$ pF. The corresponding gate reflection coefficient, $\Gamma_{source} = 0.77\angle -176.8°$, can be represented

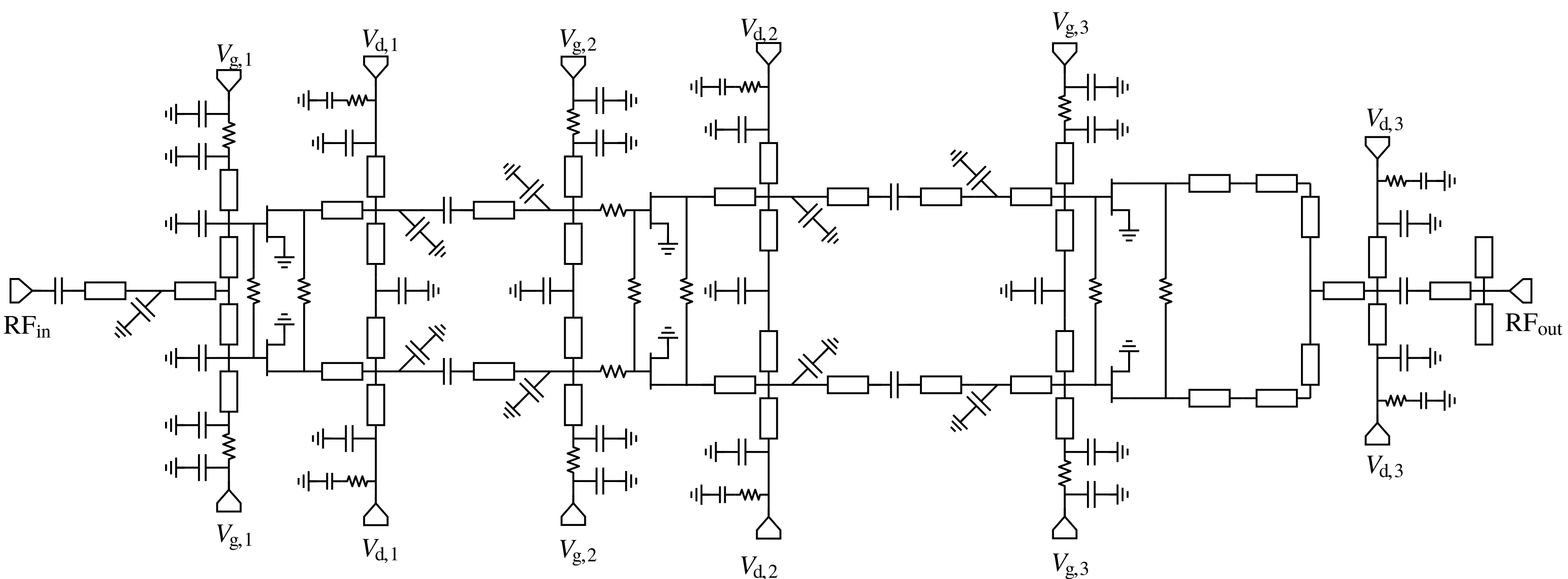


Figure 4.2: Schematic for the 3-stage, 2-way power combined USSPA design using Qorvo GaN09 T-gate corresponding to the layout in Fig. 4.1.

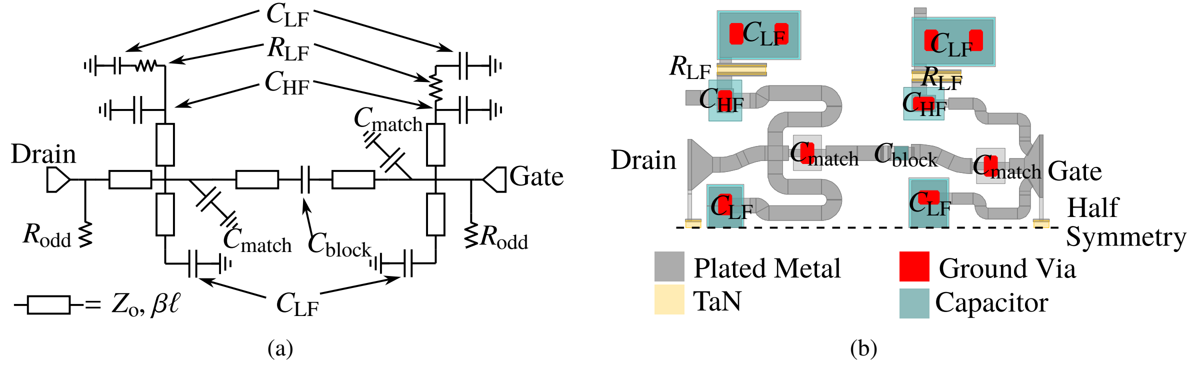


Figure 4.3: (a) Schematic for matching network topology used in each interstage. (b) Layout for half of the interstage showing half symmetry line. The quasi-distributed matching using tranmission lines, C_{match} and C_{block}, are shown.

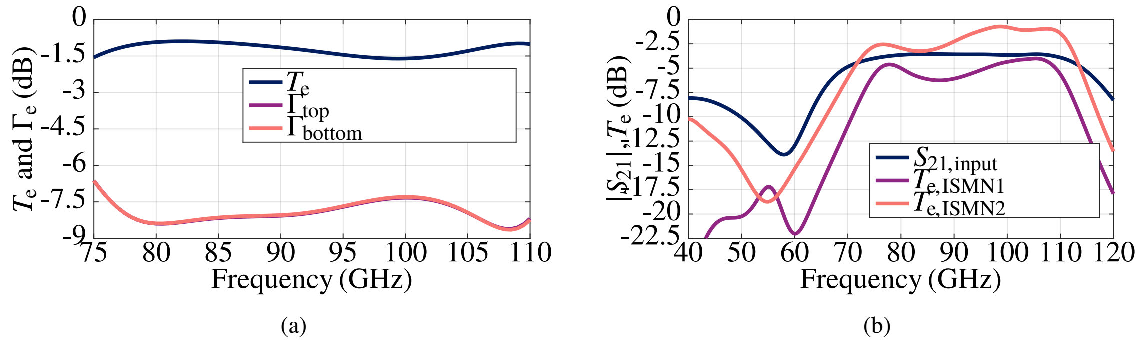


Figure 4.4: (a) The output 2-way combiner performance under even-mode operation such that the active transmission, T_{e}, and active reflection coefficient, Γ_{e}, are driven by synchronous sources. Perfect balance between both input ports due to symmetry of structure. Maximum and minimum insertion loss are 1.6 dB and 0.9 dB, respectively. (b) Frequency response for input network and interstages. Out-of-band rejection is 18.7 dB in V-band to reduce low-frequency gain for improved low-frequency stability.

with values R_{s} and C_{s} of 6.5 Ω and 0.122 pF.

For the first and second stages, the equivalent values are also found to achieve maximal gain for the drive stages. Using the 2×40 μm EEHEMT models, the input and output RC values can be represented as $(R_{\mathrm{s}}, C_{\mathrm{s}}) = (11.85\,\Omega, 0.223\,\mathrm{pF})$ and $(R_{\mathrm{s}}, C_{\mathrm{s}}) = (180\,\Omega, 0.02\,\mathrm{pF})$. Similarly, the scaled 4-finger EEHEMT model to a size of 4×30 μm can represented with $(R_{\mathrm{s}}, C_{\mathrm{s}}) = (5.8\,\Omega, 0.3\,\mathrm{pF})$ and $(R_{\mathrm{s}}, C_{\mathrm{s}}) = (134.7\,\Omega, 0.03\,\mathrm{pF})$.

The matching topology for the USSPA use quasi-distributed matching that is shown in Fig. 4.3. The quasi-distributed matching topology using tranmission lines, C_{match} and C_{block}, is enabled by the 3MI process and COV. The capacitor's direct contact to the top of substrate via reduces the overall inductance which

may cause the capacitor to self-resonate within W-band. Additionally, the thinned 50 μm over a 100 μm SiC substrate further reduce parasitic inductance.

The performance for the input, interstages, and output networks are shown in Fig. 4.4. Output, 2-way combiner performance shown in Fig. 4.4(a) under even-mode operation such that the active transmission, T_e, and active reflection coefficient, Γ_e, is optimized for wideband performance. Perfect balance between both input ports due to symmetry of structure is achieved as opposed to the 4-way design for the Γ-gate process presented in Chapter 3. Maximum and minimum insertion losses are 1.6 dB and 0.9 dB, respectively. The frequency response for input network and interstages in Fig. 4.4(b), shows good out-of-band rejection with reduction for low-frequency gain and improved low-frequency stability. Additional loss for the second interstage due to a series gate resistor is explained in the following section.

4.1.3 Stability of Millimeter-Wave Power Amplifiers

From Section 3.1, it is obvious that extensive efforts in MMIC design are placed into ensuring stability of the amplifier. It was observed that one of the more challenging tasks in the design of millimeter-wave amplifiers is ensuring stability at lower frequencies. The stability analysis techniques have already been presented in Section 3.1.4, therefore a stable design under process variation is presented in more detail for the T-gate design.

Due to the large transistor gains below millimeter-wave frequencies for high performing transistors, many of the difficulties in PA stabilization lie in stabilizing out-of-band regions. With GaN09 T-gate process having a larger g_m, the out-of-band stabilization becomes much more important to address. From Figs. 3.12 to 3.13 in Section 3.1.4, it is clear that due to the out-of-band gain response between 16-40 GHz, stability issues arose with changes in g_m, C_{gs}, and C_{gd} caused by process variation. Marginal stability issues under nominal model conditions quickly became problematic with process variations.

Reduction in low-frequency gain could not solely be accomplished through the low-frequency resistive bypassing circuits on the gate and drain line. Mitigation strategies in using parallel tanks in series at the gate to resonate at f_o would also provide narrowband solutions for the problem. A series-C small enough to be absorbed in the matching network while simultaneously providing significant rejection of low-frequencies

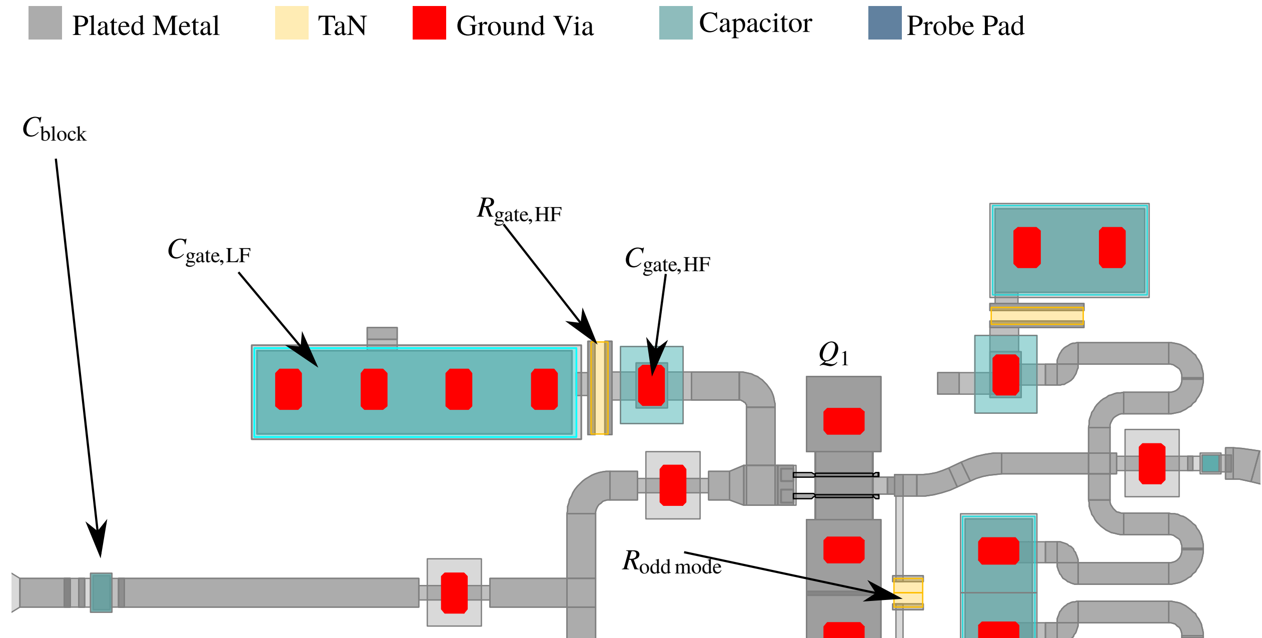


Figure 4.5: Stability design circuits for millimeter-wave power amplifier design using two methods. DC blocking capacitors placed at the input and interstages on the order of 0.03 pF for W-band provide a high-pass response. Resistive low-frequency bypassing with $\sim 5\,\Omega$ resistor at the gate and drain line for attenuation before and after the stage further provides suppression.

provides a viable solution for low-frequency rejection and wideband performance. The composite of the two design practices, low-frequency resistive bypassing and small-blocking capacitors, provide powerful techniques to ensure suppression of low-frequency gain.

Figure 4.5 shows the layout of the input and first interstage of the Qorvo T-gate unit PA as an example. The first approach provides a high pass response by using small DC blocking capacitors at the input and interstages. Typical values in W-band are on the order of 0.03 pF to ensure sufficient rejection at lower, microwave frequencies. The second approach is the implementation of resistive short at low-frequencies bias lines. Similar to the small blocking capacitors used throughout the multistage amplifier, small bypass capacitors provide bypass at frequencies in-band to the amplifier.

Further instabilities may be introduced closer to the frequency band of operation which may become more difficult to address due to changes of in-band frequency behavior of the matching networks. As previously stated, a typical initial diagnosis involves looking at the frequency response of the amplifier for |S-parameters| and K-factor. In Fig. 4.6, the wideband response of the USSPA is shown. Peaking gain response in, $|S_{21}|$,

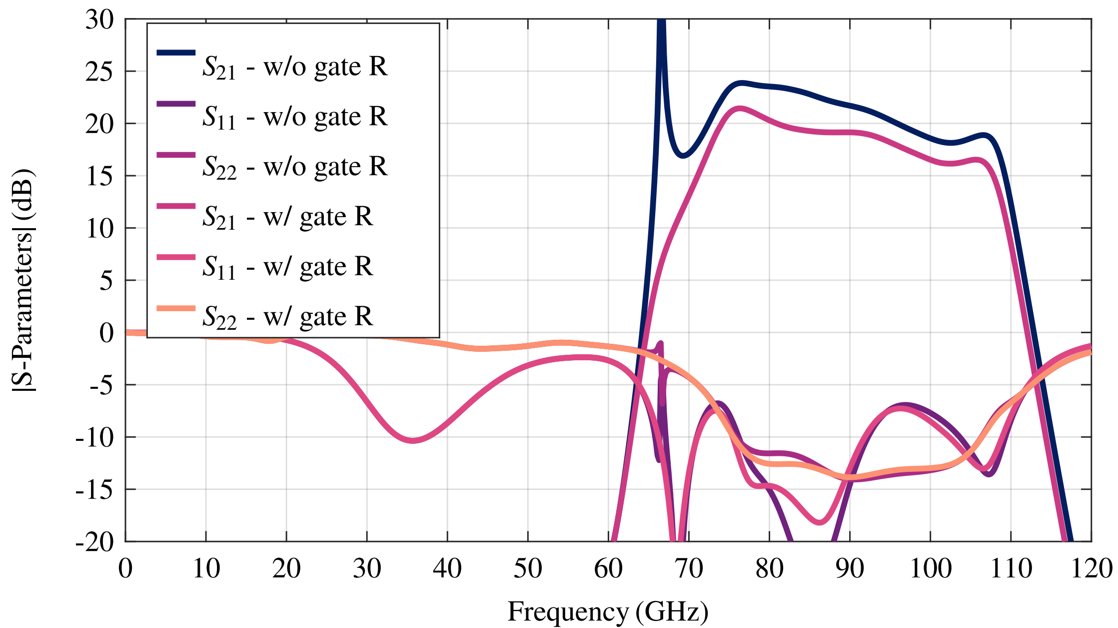


Figure 4.6: Wideband frequency response for USSPA with and without gate resistor on stage 2. Peaking gain response in, $|S_{21}|$, and output return loss in, $|S_{22}|$, show potential instability at 66 GHz without gate resistance.

and output return loss in, $|S_{22}|$, show potential instability at 66 GHz without a gate resistance placed at Q_2 and Q_5. Further analysis based on loop gain and internal Nyquist stability show instabilities caused by the second stage transistors, Q_2 and Q_5. The loop gain and internal Nyquist stability analysis for Q_2 with and without gate resistor are shown in Fig. 4.7 (a) and (b). Figure 4.7(c) show the internal reflection coefficients moving radially inward with increasing resistance contours on the Smith Chart, moving away from a point of outside the Smith Cart, showing the effectiveness of the gate resistance.

Though the gate resistor method provides an effective solution in stabilization, it comes at the expense of sacrificing gain which has previously been shown in Fig. 4.6 with the reduction of in-band gain by approximately 2 dB. The selection of the size of the gate resistance involves considering the stability under process variations that provides guidance in selecting the minimum about of resistance need for stability. In Fig. 4.8(a), the wideband response is shown with process variation using g_{m} increased by 30%, C_{gs} decreased 30%, and C_{gd} increased by 30%. Since the value of the resistor impacts the in-band performance of the amplifier, the value of R_{gate} is sized such that the stability is marginal at the extremes of process variation

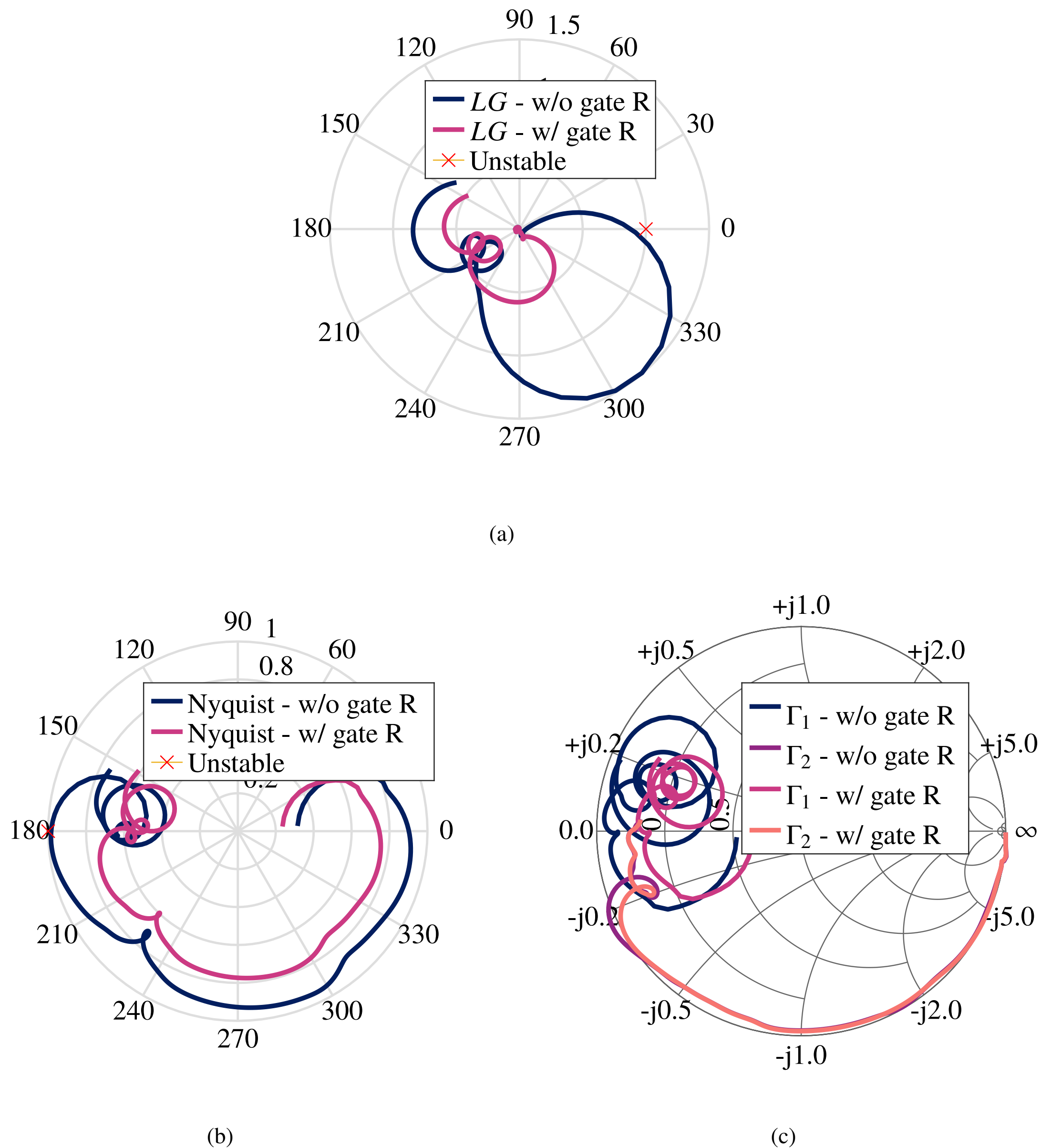


Figure 4.7: (a) Loop gain analysis for second stage Q_2 with and without gate resistor. (b) Internal Nyquist stability at the gate of the second stage, Q_2, with and without gate resistor. (c) Internal reflection coefficients with and without R with reference plane at the gate of Q_2 referenced to 50 Ω. Γ_1 is reflection coefficient into the interstage matching network and Γ_2 is reflection coefficient into of Q_2.

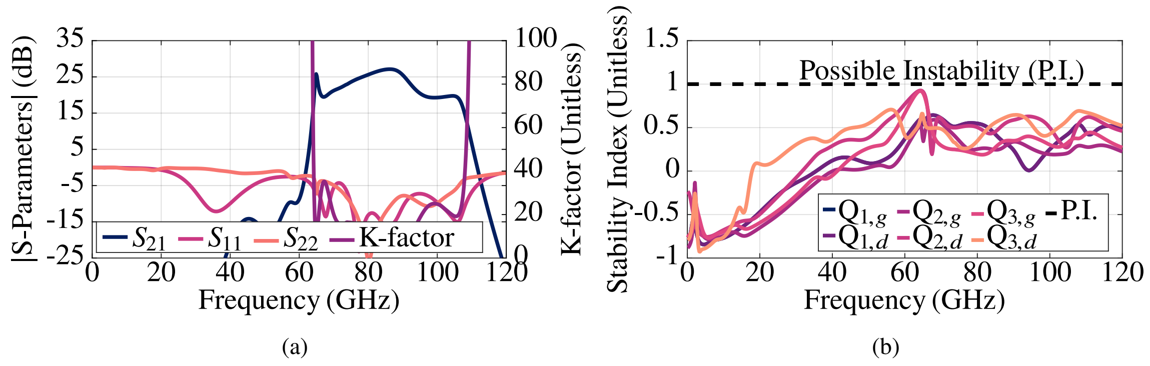


Figure 4.8: (a) Wideband frequency response of $|S_{21}|$, $|S_{11}|$, $|S_{22}|$ and K-factor for the USSPA. Performance shown with process variation using g_m increased by 30%, C_gs decreased 30%, and C_gd increased by 30%. (b) Wideband frequency response for Nyquist stability index for all devices in the USSPA. Stability index shows marginal stability at the worst case variation of the amplifier with stage 2 under process variation being the worst case. Stability index shown with process variation using g_m increased by 30%, C_gs decreased 30%, and C_gd increased by 30%.

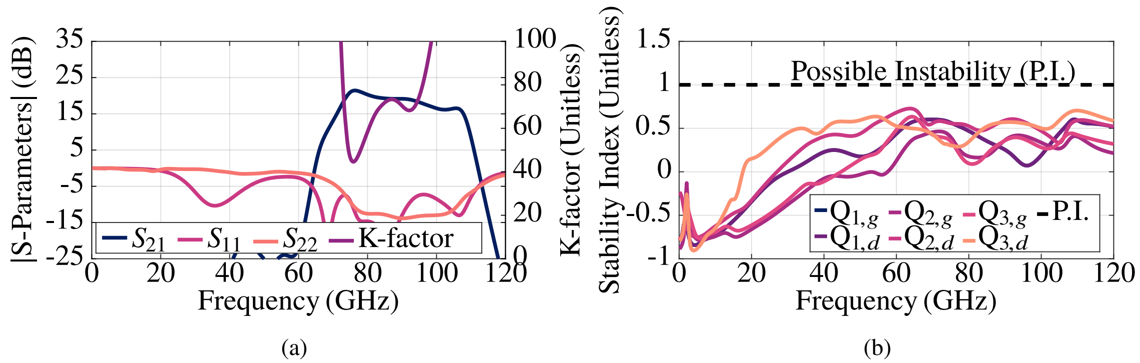


Figure 4.9: (a) Wideband frequency response of S_{21}, S_{11}, S_{22} and K-factor for the USSPA. Performance shown without process variation. (b) Wideband frequency response for Nyquist stability index for all devices in the USSPA without process variation.

shown with the Nyquist stability index in Fig. 4.8(b). A value of $5.5\,\Omega$ at the gates of Q_2 and Q_5 allows to achieve a marginal stability of stability index less than 1 and a loop gain with phase margin of 14.85° under $\Gamma = -1$ for source and load terminals. The resulting wideband frequency response and stability index of the stabilized USSPA is shown in Fig. 4.9 (a) and (b), respectively.

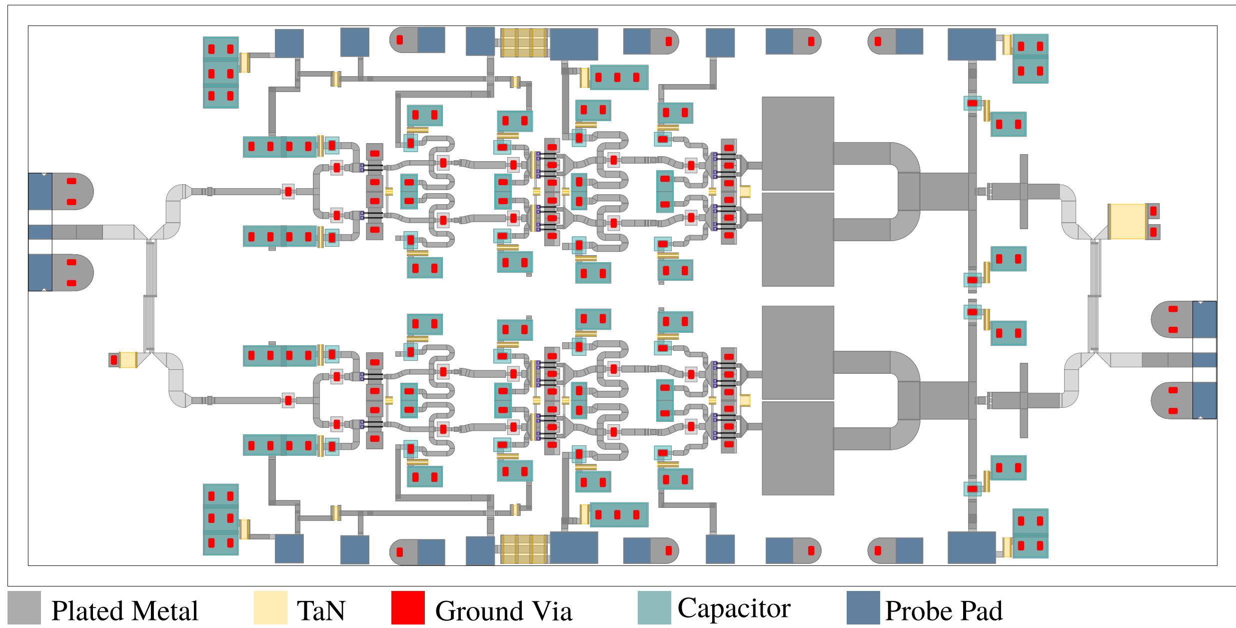


Figure 4.10: Layout for Qorvo GaN09 T-gate balanced amplifier. Total chip size occupies $3.9\times 1.84\,\mathrm{mm}^2$.

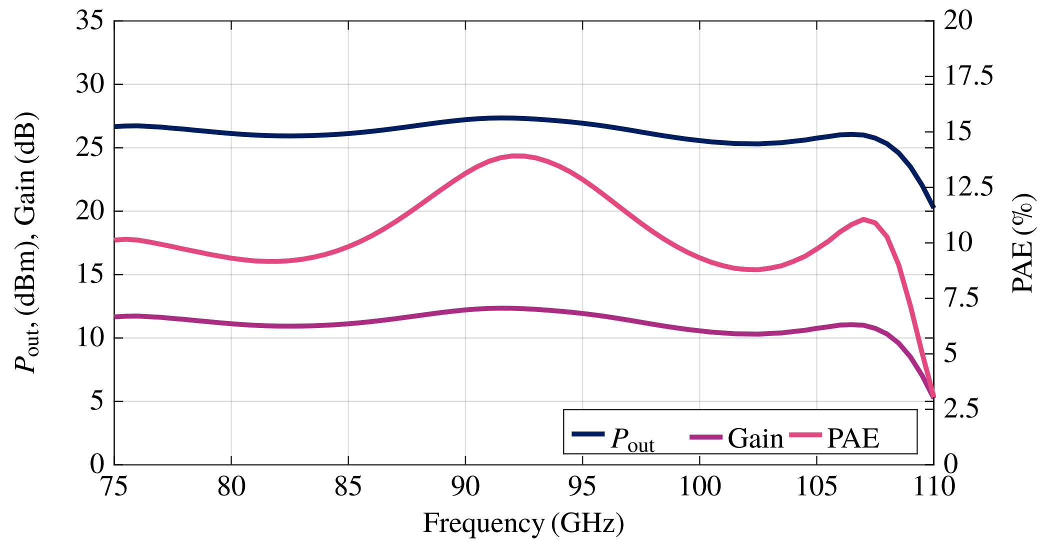


Figure 4.11: Simulated frequency response for the balanced MMIC with P_{in} = +15 dBm under bias conditions (V_d, I_{ds})= (+13 V, 150 mA/mm).

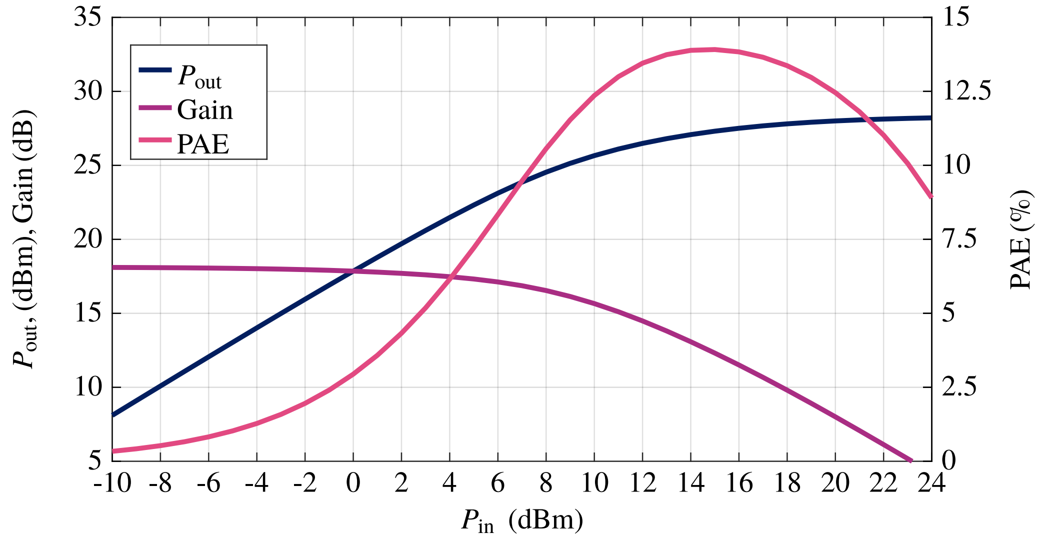


Figure 4.12: Simulated P_{out}, saturated gain and PAE versus P_{in} at 92.5 GHz of the balanced MMIC design at a +13 V drain supply voltage with 150 mA/mm drain current.

4.2 GaN09 T-gate Power Amplifier Balanced Design

4.2.1 Layout and Simulated Performance

Similar to Section 3.2, the USSPA design is used in a balanced architecture for power scaling. This allows to increase the output periphery from the 320 μm of the USSPA to 640 μm, which is equivalent to the GaN09 Γ-gate single-ended design presented in Section 3.1. The layout of the Qorvo GaN09 T-gate balanced amplifier is shown in Fig. 4.10 and occupies a total chip size occupies 3.9×1.84 mm^2. The simulated frequency response for the balanced amplifier is shown in Fig. 4.11. The bias voltage, V_d = +13 V, and quiescent bias current in class-AB, I_{ds} = 150 mA/mm, as modeled with the non-linear EEHEMT devices. The input power is set to +15 dBm, which corresponds to peak efficiency for the amplifier. The simulations predict and output power of +27.35 dBm (543 mW) at 91.5 GHz, with corresponding to a PAE of 13.8%. The balanced amplifier simulates a wideband frequency response achieving greater than 25 dBm over from 75-108 GHz. Predicted P_{out}, gain and PAE versus P_{in} at 92.5 GHz of the balanced amplifier at a +13 V drain supply voltage with 150 mA/mm drain current is shown in Fig. 4.12.

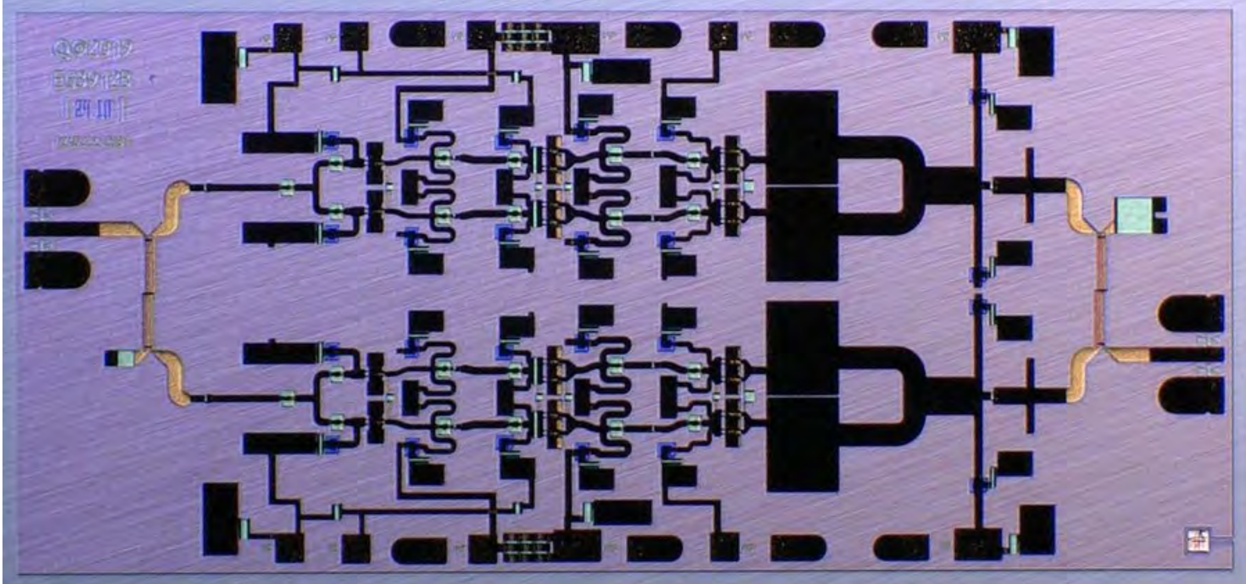


Figure 4.13: Photograph of Qorvo GaN09 T-gate balanced amplifier for the layout shown in Fig. 4.10.

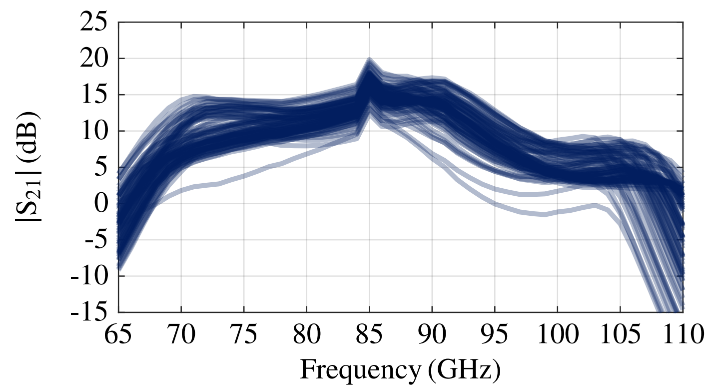
4.2.2 On-Wafer Measurements

The fabricated balanced design using the GaN09 T-gate process is shown in Fig. 4.13. The on-wafer small-signal measurements taken across the wafer for $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ shown in Fig. 4.14 for 65 to 110 GHz. The bias conditions of the small-signal measurements are $V_d = 13$ V with drain current, I_d, of 144 mA.

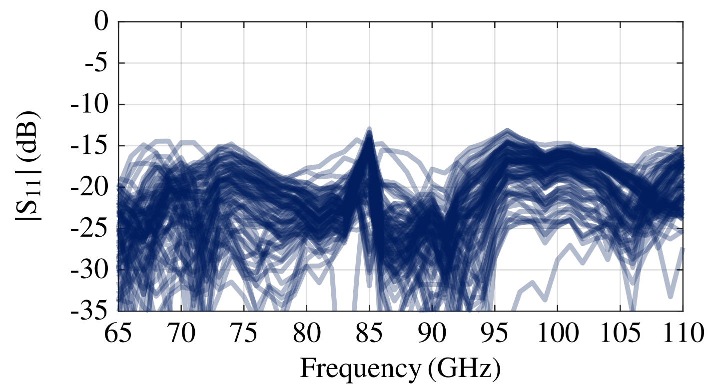
4.3 GaN09 T-gate Power Amplifier Serially Combined Design

4.3.1 Layout and Simulated Performance

Serial combining was first demonstrated using waveguides in [84] with promising MMIC performance demonstrated in [6]. The general architecture for a serially combined amplifier is shown in Fig. 4.15. The architecture offers scalability for power combining not limited to 2^N or $2N$ by corporate and balanced combiners, respectively. Similarly to a distributed or traveling-wave amplifier, power from the input signal of the amplifier gets coupled from the main propagation such that an equal amount of power is presented at the inputs of the USSPAs. Due to the required couplers needed for the architecture, monolithic integration becomes prohibitive at microwave frequencies. With the reduction of the guided wavelength at millimeter-



(a)



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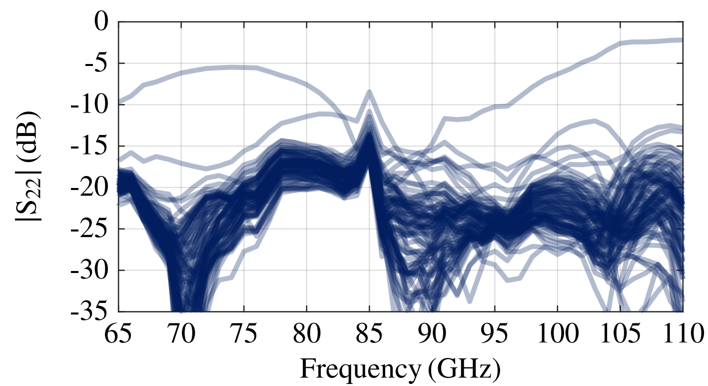


(c)

Figure 4.14: On-wafer measurements for Qorvo GaN09 T-gate balanced amplifier for (a) $|S_{21}|$, (b) $|S_{11}|$, and (c) $|S_{22}|$.

Thru

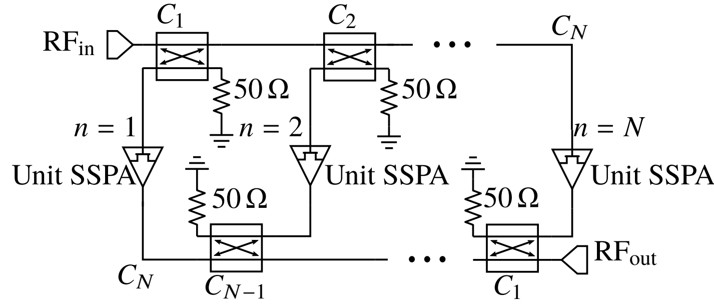
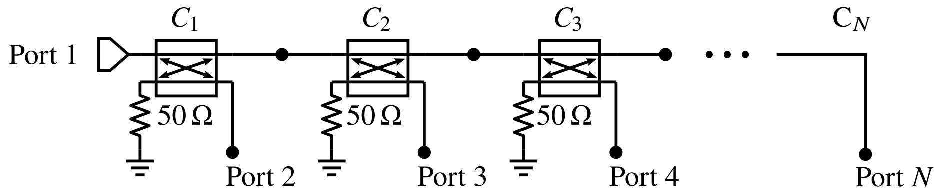
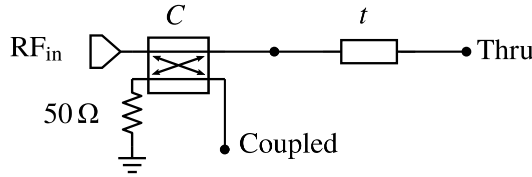


Figure 4.15: Schematic for a serially combined architecture combining a total of N identical USSPA.



(a)



(b)

Figure 4.16: (a) Schematic for N-way splitter section for serially combined architecture. Coupling coefficients are selected with Eqs. (4.1) and (4.2). (b) Equivalent coupler modeled with losses within the coupler modeled as losses on the thru path, t.

wave frequencies and state-of-the-art MMIC processing, serial combiners on-chip become feasible.

The coupling factors for the lossy serial combiner can be analyzed in splitting configuration shown Fig. 4.15(a) that is used at the input of the PA. Losses within the couplers can be modeled and lumped in addition to the losses in transmission line connecting each of the couplers as an element in series on the thru path. This approximation is shown in Fig. 4.15(b) with coefficients given from [6],

$$C_N^2 = 1 \tag{4.1}$$

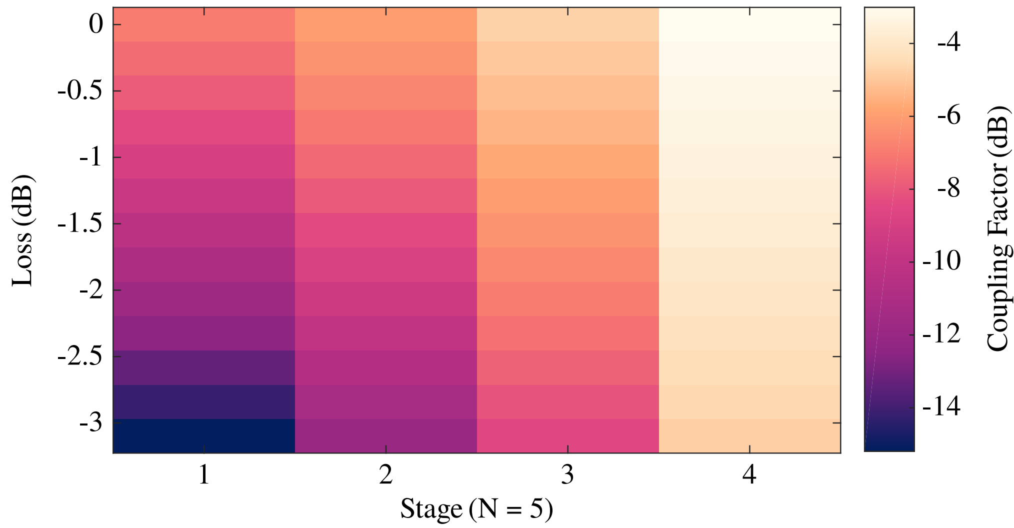


Figure 4.17: Required coupling factors per stage as a function of loss for $N = 5$.

$$C_i^2 = \frac{C_{i+1}^2 t_i^2}{C_{i+1}^2 t_i^2 + 1}. \tag{4.2}$$

A simple analysis of the coupling coefficients as a function of loss for N=5 are shown Fig. 4.17. The coupling coefficients are strongly dependent on the losses, t. As losses increase in the serial splitter, less coupling is required as the power propagates down the line to maintain equal powers at the ports. The choice of coupling factor for each becomes critical to provide equal input power presented at the inputs of each of the USSPAs. Similar to the limitations of a distributed power amplifier, unequal input powers presented at the input ports result in each amplifier being saturated at different levels and as a result, a reduction in overall output power and PAE of the amplifier.

Additionally, inadequate modeling result in unfavorable implementation of the splitter and combiner in the architecture. The synthesis of the couplers to ensure correct coupling coefficients at each stage requires careful EM modeling at millimeter-wave frequencies. To illustrate this, a closer analysis of the Lange coupler for the serial combining architecture will looked at for improvement in combining performance at the higher end of W-band where degradation in performance may occur. It has been shown in Chapter 3 that current crowding at millimeter-wave frequencies begins to affect circuit behavior and performance. For the Lange coupler, the coupling factor will differ for different feed variation therefore needing adjustments

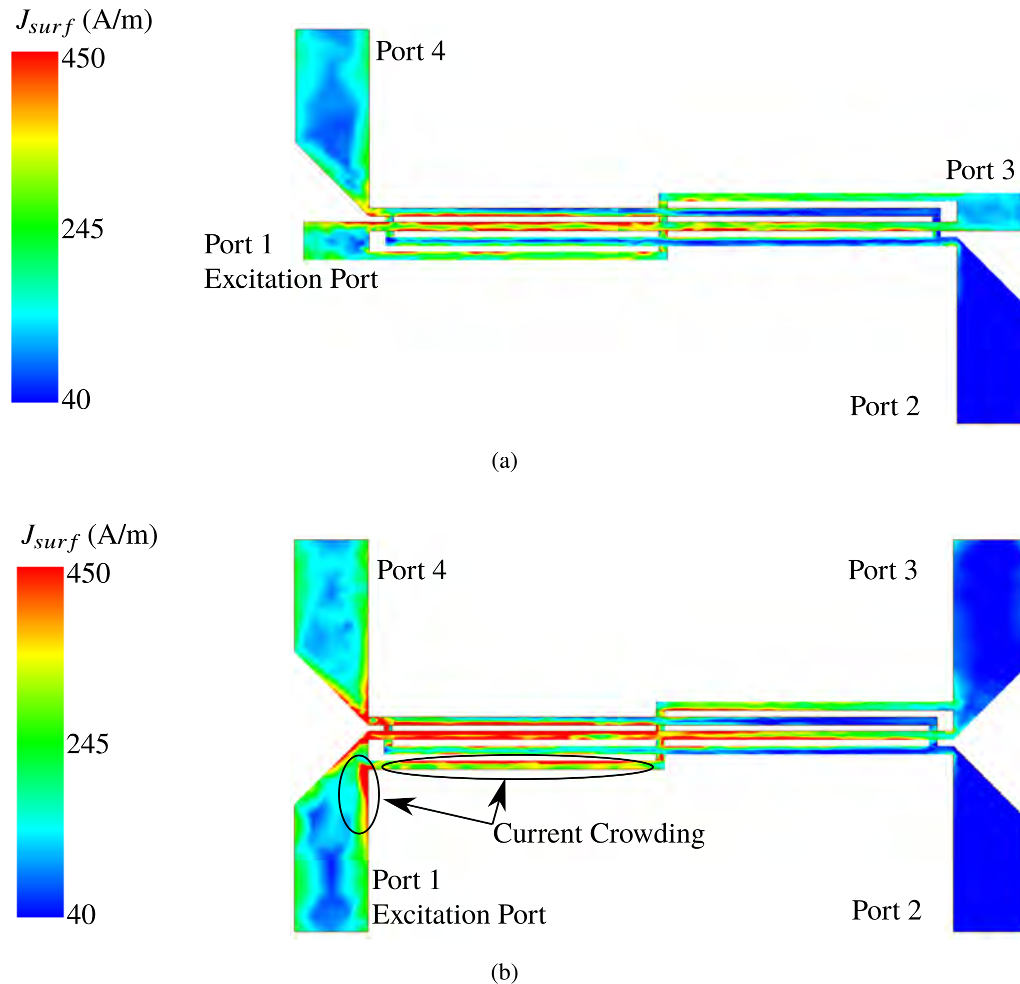
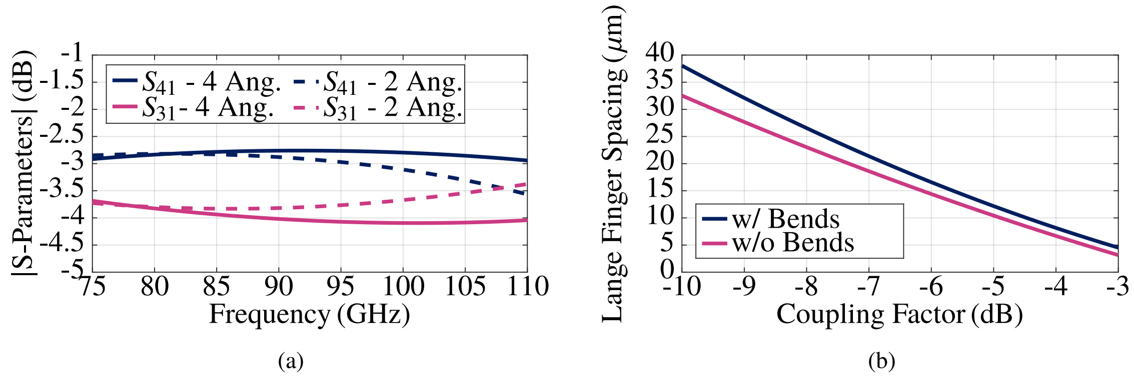


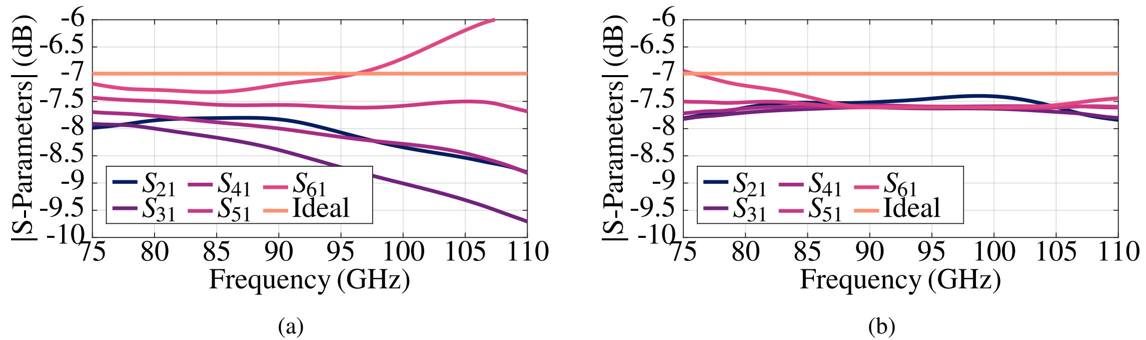
Figure 4.18: The surface current amplitude for 3 dB Lange couplers. (a) Manifold with two straight and two right angle feed that are used in serial combiners. (b) Manifold with four right angle feeds which commonly used for balanced amplifiers.

in finger spacing with a Lange coupler. Figure 4.18 show the current distributions for two Lange couplers being fed with 2-angled bends that are used for serial combiners in Fig. 4.18 (a) and 4-angled bends that are used for balanced amplifiers in Fig. 4.18 (b). A look at the current distributions for the fingers show current accumulation on the inside of the right angle bend in Fig. 4.18 (b), causing a difference in coupling performance. In addition, the Lange coupler shifts in center operating frequency shown in Fig. 4.19(a). Using a parametric EM simulation, coupling coefficient over finger spacing shown in Fig. 4.19(b). For coupling factors less than 3-dB, the resulting difference does not depend strongly on the manifold, but as the coupling factor decreases, larger variations in the coupling factor occur.



(a) (b)

Figure 4.19: (a) Frequency shift for Lange coupler two- and four-bend Lange manifold. (b) Lange coupling factor versus finger spacing at 92.5 GHz for two- and four-bend Lange manifold.



(a) (b)

Figure 4.20: (a) Serial Lange in splitter configuration showing dispersion across W-band. (b) Serial Lange configuration with feed compensation across W-band.

As it was alluded to earlier, the errors associated with the selection of improper coupling factors across the serial splitter impact the overall performance of the PA. In Fig. 4.20 (a), a design based on modeling using the traditional, 4-angled bend, Lange manifold show amplitude variation of up to 5 dB at the far end of the band, 110 GHz. Using a more accurate EM modeling, representative of how the Lange will be used for layout, the finger spacing as function of coupling factor can be investigated. As a results, the serial combiner can provide wideband improvement, more considerably at the high end of W-band where power is at a premium as shown in Fig. 4.20 (b). Improvements in the back-to-back loss are shown in Fig. 4.21.

The complete layout of the Qorvo GaN09 T-gate serially combined amplifier is shown in Fig. 4.22 and occupies a total chip size occupies 3.9×3.81 mm^2. The simulated frequency response for the serially combined amplifier is shown in Fig. 4.23. The bias voltage, V_d = +13 V, and quiescent bias current in class-AB, I_ds = 150 mA/mm, as modeled with the non-linear EEHEMT devices. The input power is set to

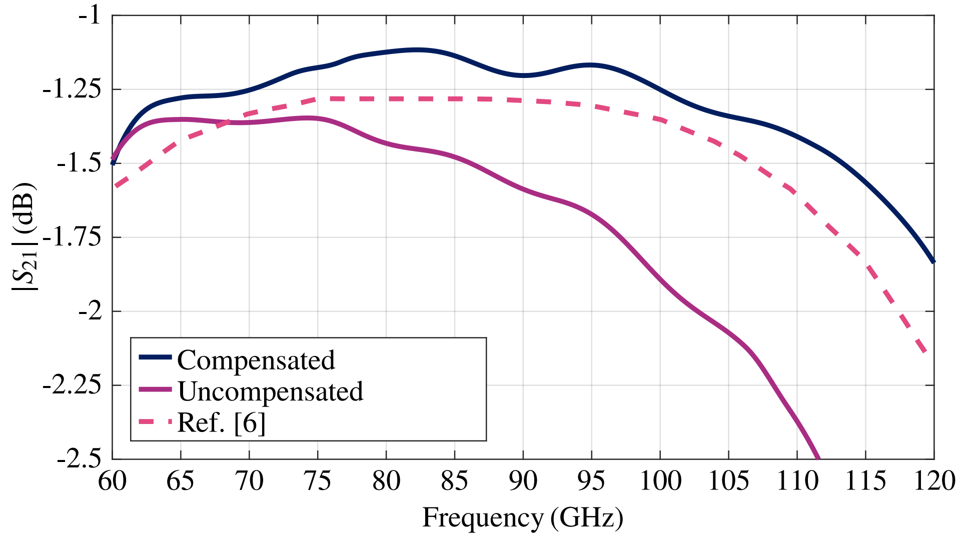


Figure 4.21: Improvements for back-to-back loss for improved EM modeling of Lange serial splitter/combiner are compared with [6].

+20 dBm, which corresponds to peak efficiency for the amplifier. The simulations predict an output power of +31.05 dBm (1.27 W) at 93.5 GHz, with corresponding to a PAE of 17.57%. The serially combined amplifier predicts a wideband frequency response achieving greater than 28.5 dBm over from 75-108 GHz. Predicted P_{out}, gain and PAE versus P_{in} at 92.5 GHz of the serially combined amplifier at +13 V drain supply voltage with 150 mA/mm drain current is shown in Fig. 4.24.

4.3.2 On-Wafer Measurements

The fabricated serial amplifier design using the GaN09 T-gate process is shown in Fig. 4.25. The on-wafer small-signal measurements taken across the wafer for $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ shown in Fig. 4.26 for 65 to 110 GHz. The bias conditions of the small-signal measurements are $V_{\text{d}} = 13$ V with drain current, I_{d}, of 360 mA.

4.4 Conclusion

In summary, this chapter presents the analysis and design of two W-band power amplifiers using Qorvo's GaN09 T-gate process. A summary of performance compared to state-of-the-art are given in Fig. 4.27

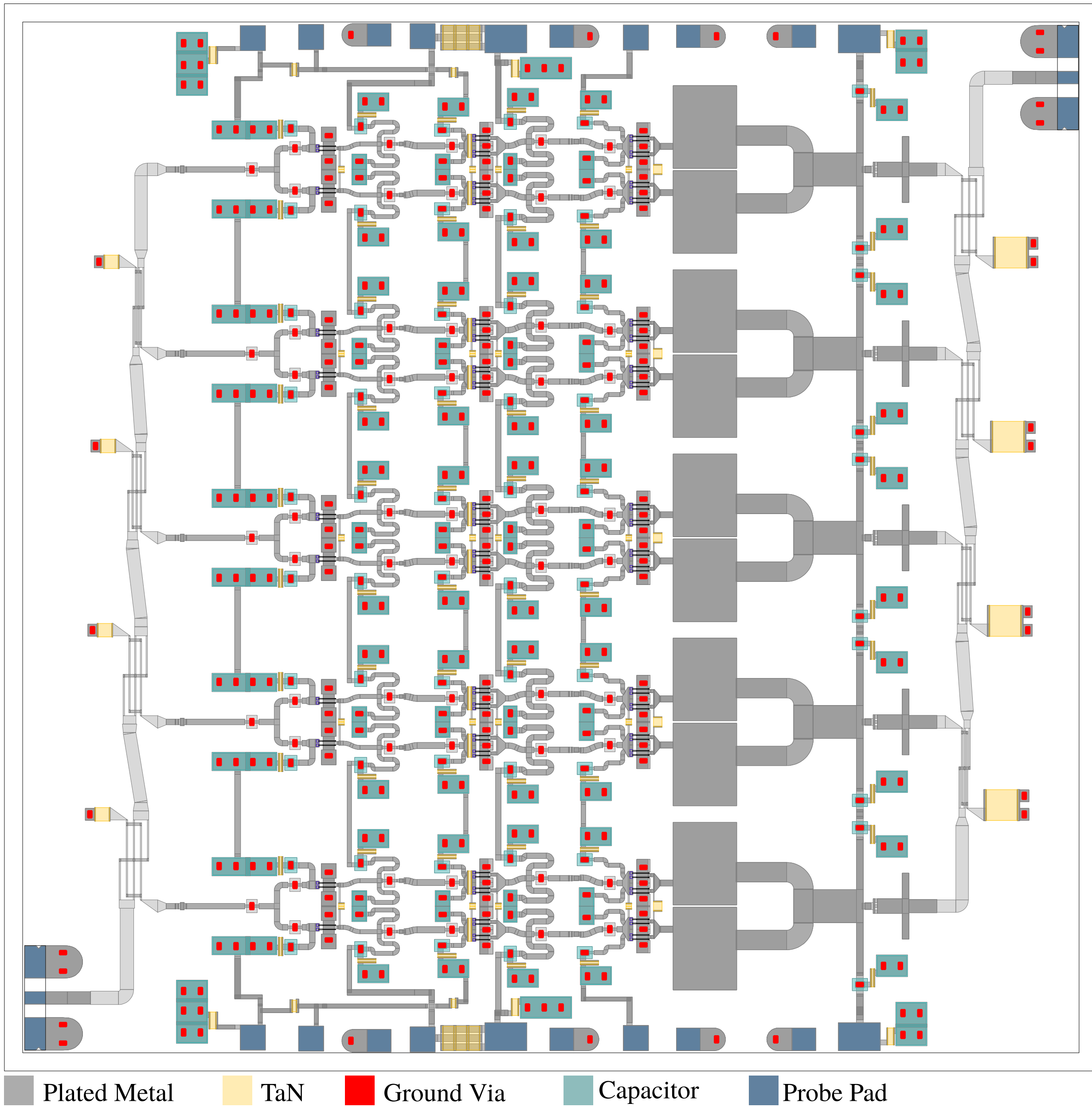


Figure 4.22: The layout for Qorvo GaN09 T-gate serially combined amplifier. The total chip size occupies $3.9{\times}3.81\ \mathrm{mm}^2$.

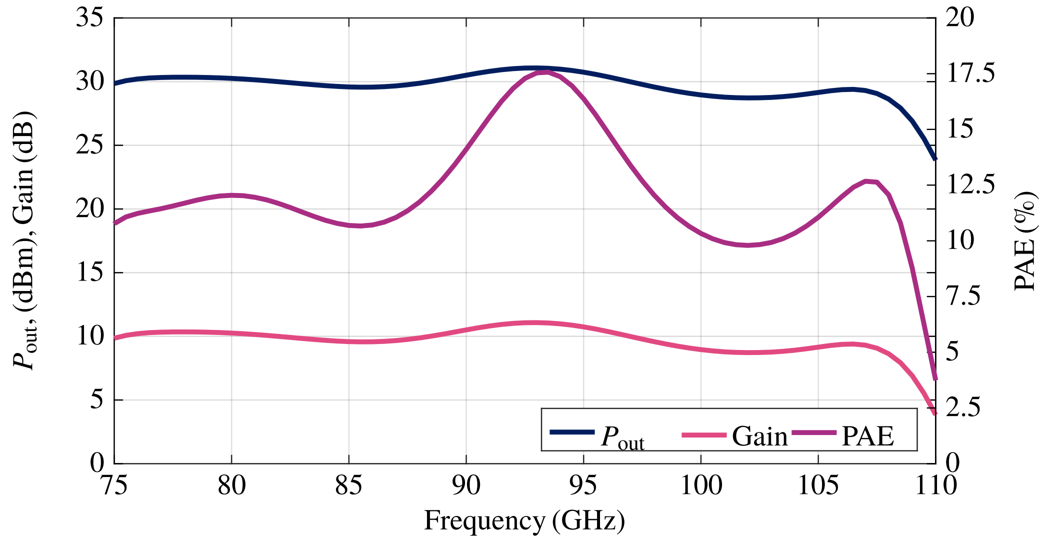


Figure 4.23: Simulated frequency response for the serially combined MMIC with P_{in} = +20 dBm under bias conditions (V_d, I_{ds})= (+13 V, 150 mA/mm).

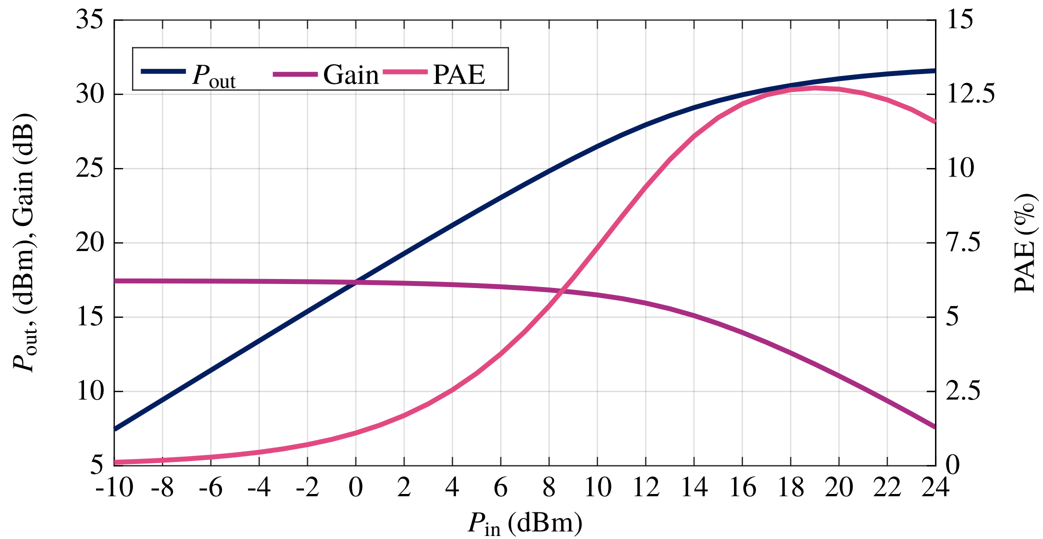


Figure 4.24: Simulated P_{out}, saturated gain and PAE versus P_{in} at 92.5 GHz of the serially combined MMIC design at a +13 V drain supply voltage with 150 mA/mm drain current.

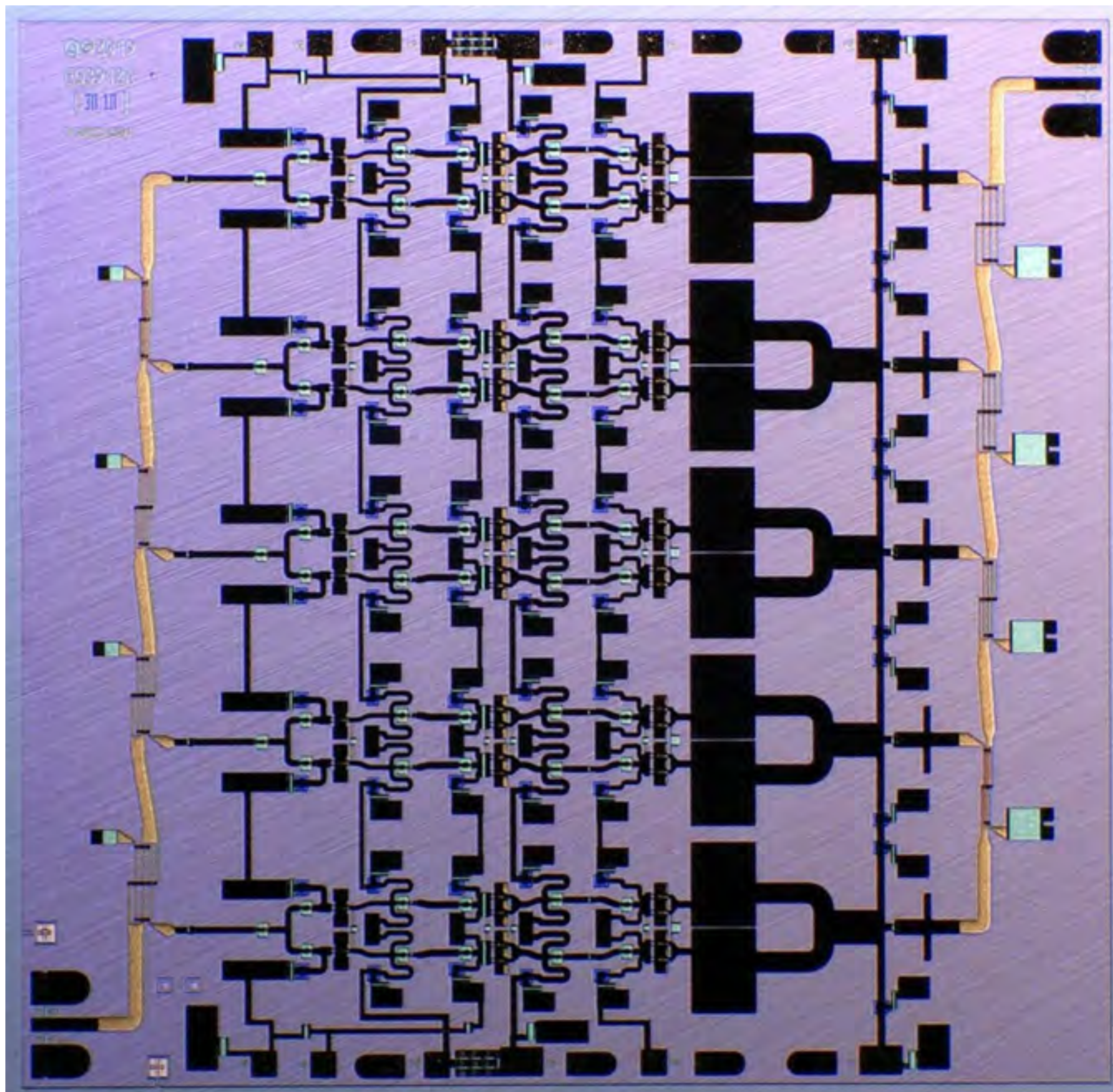
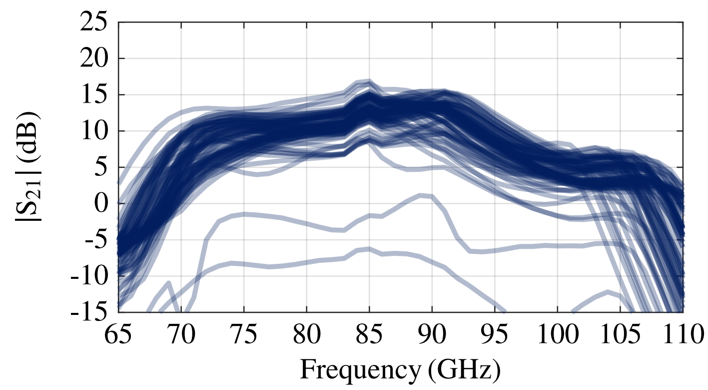
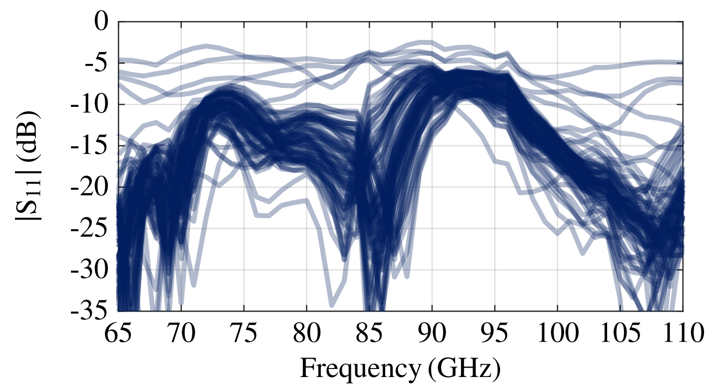


Figure 4.25: Photograph of Qorvo GaN09 T-gate serial amplifier for the layout shown in Fig. 4.22.



(a)



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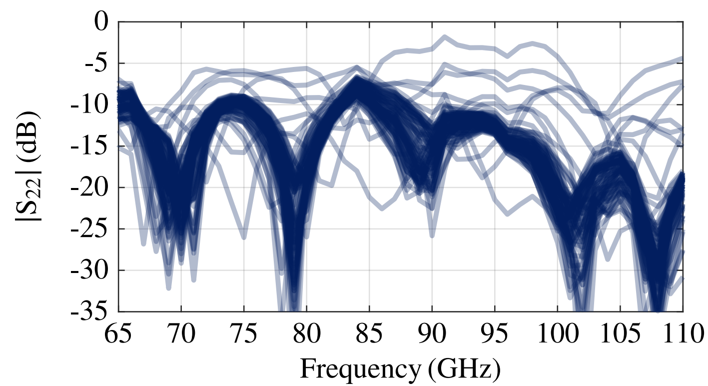

(c)

Figure 4.26: On-wafer measurements for Qorvo GaN09 T-gate serial amplifier for (a) $|S_{21}|$, (b) $|S_{11}|$, and (c) $|S_{22}|$.

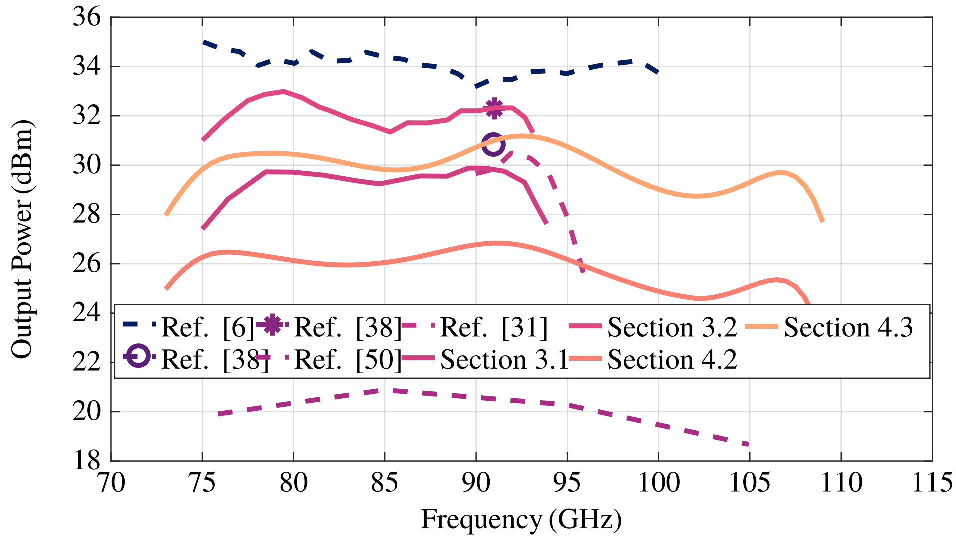

Figure 4.27: Output power versus frequency for state-of-the-art MMIC at W-band including Qorvo GaN09 Γ-gate and T-gate designs presented in Sections 3.1, 3.2, 4.2 and 4.3.

and Table 4.1. Both amplifiers produce over 0.5 W of output power at W-band, but the T-gate process shows higher frequency of operation covering 75-108 GHz while the Γ-gate process gives higher power in the lower W-band range. As a part of power combined architectures, an analysis method for the design of serial Lange combiners for improved combining efficiency is developed. The contributions from this chapter are presented in [85] where two T-gate W-band processes are compared in terms of amplifier performance, the Qorvo process discussed in this chapter and the HRL T3 process discussed in Chapter 5.

Table 4.1: GaN09 T-gate Compared to Published GaN MMIC Power Amplifiers at W-Band

Reference	Peak Output Power (W)	Bandwidth (GHz)	PAE (%)	Chip Size (mm^2)
[83]	3	75-100	12	5.4×2.75
[38]	1.2	91	20	2.5×0.9
[38]	1.7	91	11	2.9×1.6
[46]	0.5	70-75	10	3.5×1.75
[47]	0.842	83-92	14.8	-
[45]	1.5	92-96	17.8	-
Section 3.1 (single-ended)	0.979	76.6 - 92.7	5.8	3.5×1.91
Section 3.2 (balanced)	1.88	76.6 - 92.7	5	3.98×3.76
Section 4.2 (balanced)	0.543	75-108	8	3.9×1.84
Section 4.3 (serial)	1.27	75-108	8	3.9×3.81

Chapter 5

Full W-Band MMIC PAs in HRL 40 nm T3 Process

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5.1 T3 Power Amplifier Single-Ended Design 84

5.2 T3 Power Amplifier Balanced Design 89

5.3 On-Wafer Measurements 91

5.4 Conclusion 93

As introduced in Section 2.4, HRL processes are well documented with the processing techniques published in [4, 24, 60–62]. The success for high frequency performance from the evolution of the T2 to the T3 process are attributed to the recessed n^+-GaN cap layer in direct contact with the 2DEG layer. As a result, reductions in the contact resistance improve the f_T and f_{max} of the transistor. Transistor scaling for the T3 process achieves an f_T/f_{max} of 200 GHz/400 GHz with a breakdown voltage, $V_{brk} > 40$ V. The process is intended to operate at a drain voltage, $V_{ds} = +12$ V with drain current density, $I_{ds,dens}$, of 150 mA/mm, corresponding to $I_d = 22.5$ mA for a 4×37.5 μm device. The process is accompanied with passives that use three metalization layers to form transmission lines and air bridges. In addition, capacitors are formed with

a SiN layer and resistors formed with TaN layer. The actives and passives are processed on a 50 μm SiC carrier substrate.

Successful GaN W-band power amplifier designs using the T3 process have been published in [45, 47], but none yet have covered full W-band operation from 75-110 GHz. This chapter presents two wideband W-band PAs covering 75-110 GHz in HRL's T3 process. In Section 5.1, the design of a three stage USSPA with 1:2:3 drive staging is presented. In Section 5.2, the USSPA is placed in balanced configuration for additional level of power combining. Finally in Section 5.3, preliminary small-signal measurements for the USSPA is presented.

5.1 T3 Power Amplifier Single-Ended Design

5.1.1 Design, Layout, and Matching Topology of USSPA

The unit PA is a 3-stage, 2-way power combined topology with 1:2:3 drive staging, shown in Fig. 5.1(a). The output stage utilizes two 4×37.5 μm devices in parallel to provide a total output periphery of 300 μm. The primary objective of the design is to achieve full, W-band performance from 75-110 GHz, therefore similarly to the design presented in Chapter 4, the output periphery is kept small. The layout of the 3-stage, 2-way power combined USSPA is presented in Fig. 5.1(b), with a compact total area of 2.75×0.64 mm^2, with the complete schematic for the USSPA is shown Fig. 5.2.

The design uses the non-linear Angelov model for the 4×37.5 μm transistor. The modeled device is scaled to 4×25 μm for the first and second stage that boost the overall gain of the amplifier. The periphery for stage 1, 2, and 3 is chosen to be 100 μm, 200 μm, and 300 μm, respectively. The bias conditions are kept at the modeled quiescent current, 150 mA/mm that corresponds to class-AB operation for the output stage. For stage 1, 2, and 3, the drain current correspond to 15 mA, 30 mA, and 45 mA, respectively.

The matching topology used for the HRL T3 design use distributed matching due to lack of capacitor-over-vias (COV) available by the process. SiN capacitors is available to be used for DC blocking and bypassing functionality. Therefore, similarly to Chapter 3, low-impedance transmission lines and stubs are used for matching at the input, interstages, and output network. Parallel transistors use internally shared

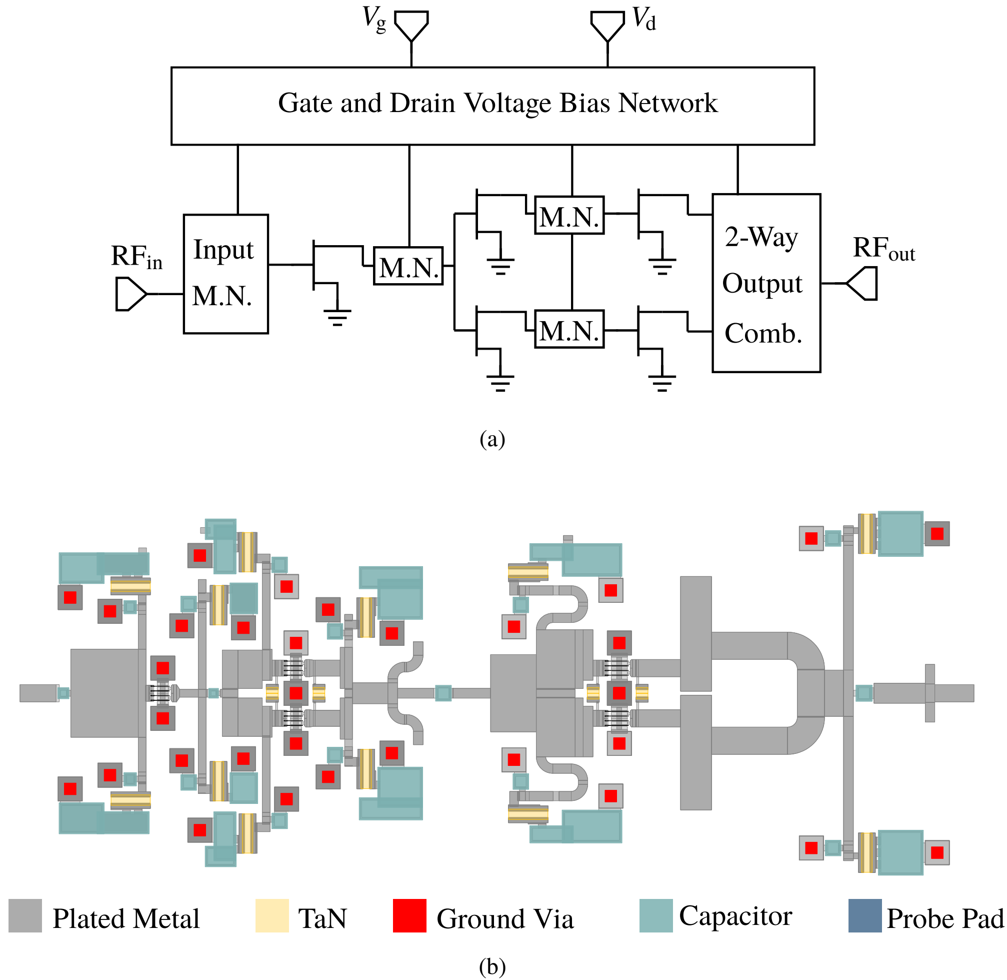

Figure 5.1: (a) Architecture for the HRL T3 USSPA power amplifier design. The design is a 3-stage, 2-way power combined architecture with 1:2:3 drive staging using 4×25 μm transistors for the first and second stage, and 4×37.5 μm, and 4×40 μm transistors the third stage. (b) Layout of the T3 MMIC USSPA with maximum dimensions of 2.43×0.927 mm^2.

vias to further reduce the distance between transistors and minimize effects from the placement of the odd-mode resistor between them. The design maintains half-symmetry with the bias lines to provide continuous biasing at either side of the USSPA to be compatible with balanced or serially combined architecture. As mentioned previously in Chapter 4, the half-symmetry design also provide sufficient balance between the parallel transistors of the amplifier, thereby reducing odd-mode occurrences. The complete design of the single-ended amplifier is shown in Fig. 5.4. Bias lines are kept compact with DC continuity for top and bottom side of design.

Stability techniques that have been presented in Section 3.1.4 and Section 4.1.3 are applied to the T3

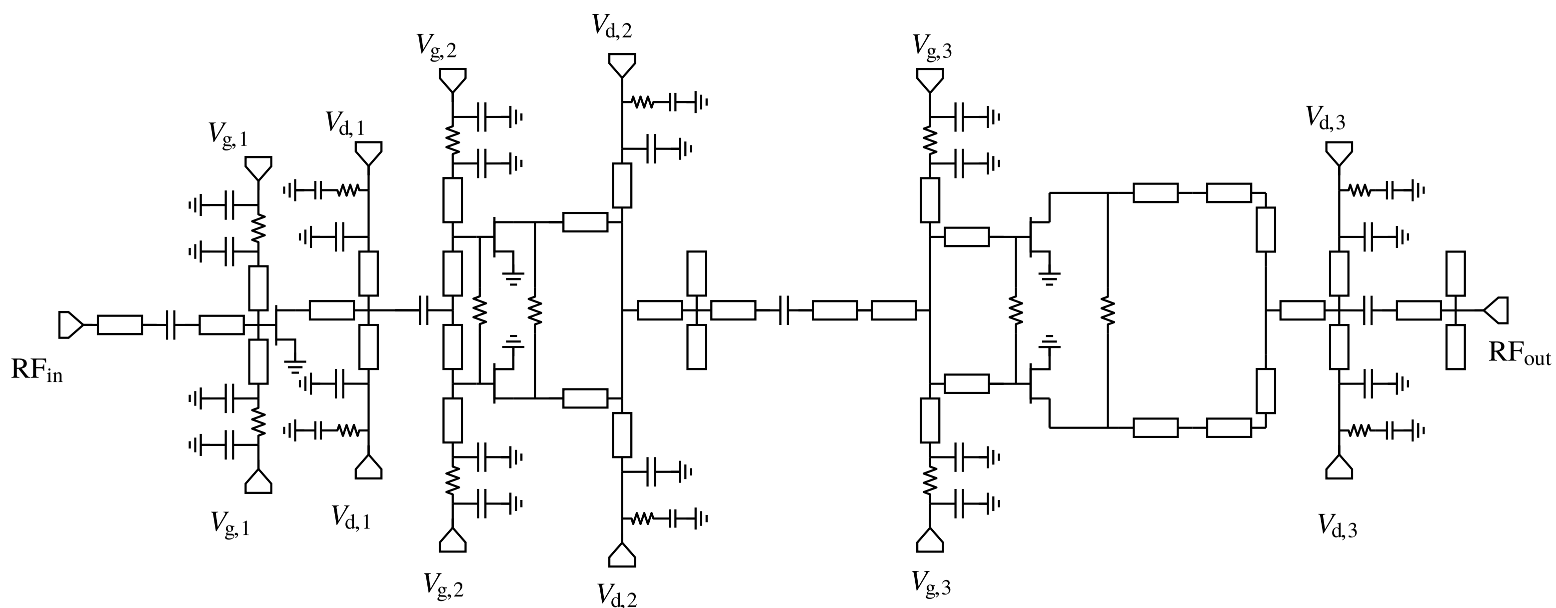

Figure 5.2: Schematic for the 3-stage, 2-way power combined USSPA design using HRL T3 process corresponding to the layout in Fig. 5.1(b).

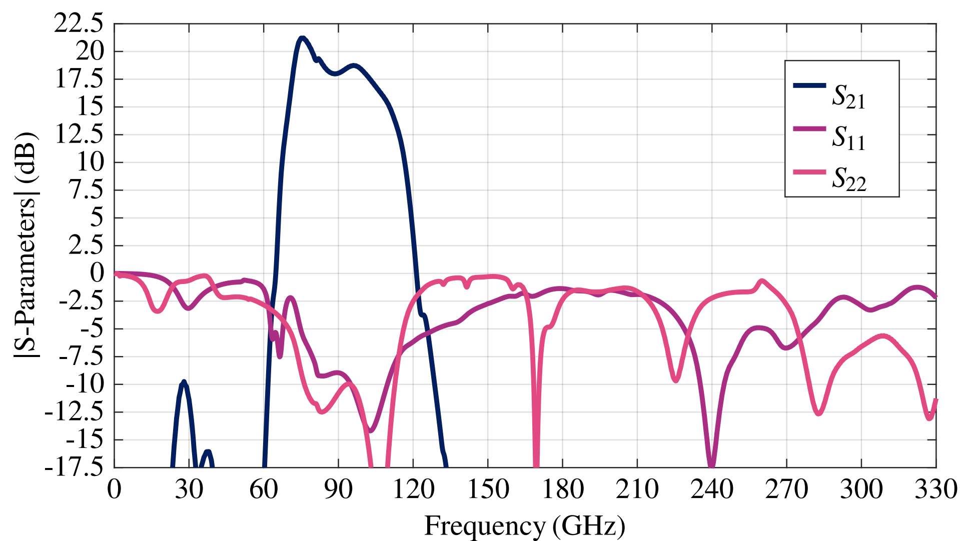

Figure 5.3: Wideband frequency response of $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ for USSPA from 0-330 GHz. Sufficient low-frequency gain suppression of approximately 10 dB provided at 30 GHz.

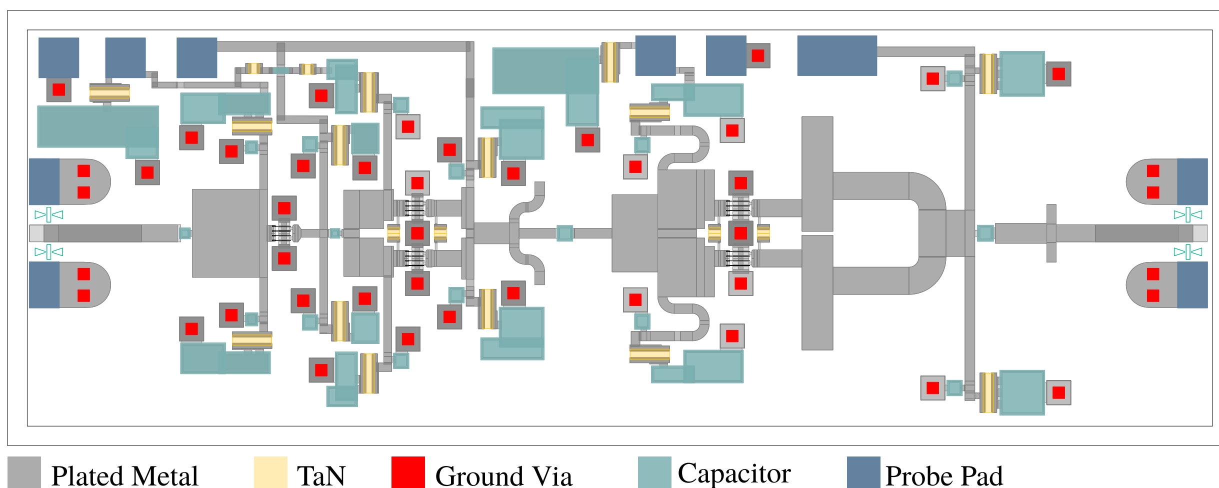

Figure 5.4: Layout for the single-ended amplifier with RF and bias pads. The total design occupies $3.12 \times 1.11\,\mathrm{mm}^2$.

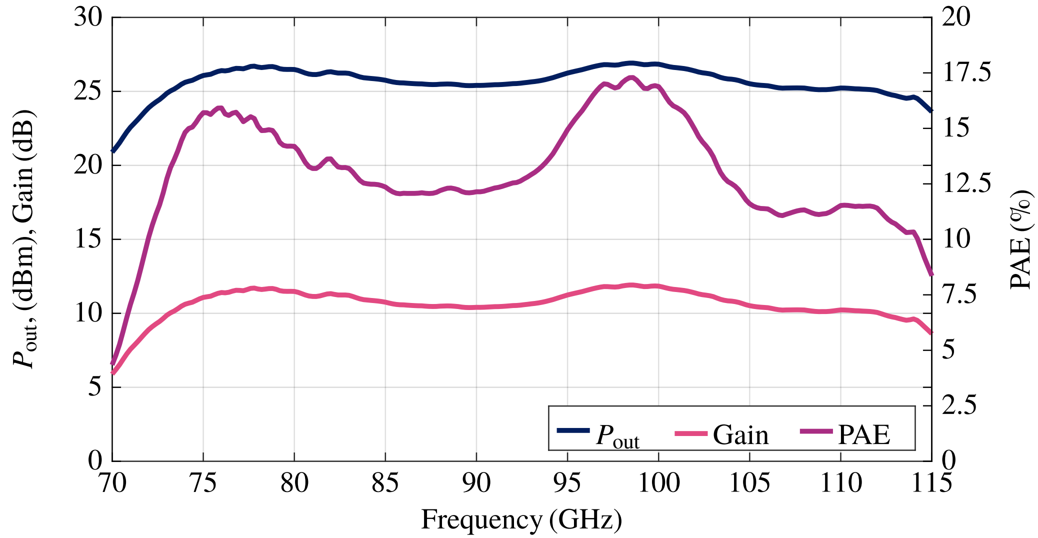

Figure 5.5: Simulated frequency response for the single-ended T3 process design with P_{in} = +15 dBm under bias conditions (V_d, I_{ds})= (+12 V, 150 mA/mm).

USSPA. Using small bypassing capacitors and low-frequency resistive bypassing, successful suppression of low-frequency gain is accomplished. Figure 5.3 shows the wideband frequency response of $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ for USSPA covering from 0-330 GHz. Simulations up to the third harmonic are required to establish convergence with the non-linear Angelov models. Sufficient low-frequency gain suppression with the minimum of approximately 10 dB provided at 30 GHz allows for stable results in K-factor, loop gain, and Nyquist criterion up to 330 GHz.

5.1.2 Simulated Performance for the Single-Ended Amplifier

The layout of the amplifier using the T3 process is shown in Fig. 5.4 and occupies a total chip size occupies 3.72×2.1 mm^2. The simulated frequency response for the single-ended amplifier is shown in Fig. 5.5. The bias voltage, V_d = +12 V, and quiescent bias current in class-AB, I_{ds} = 150 mA/mm, as modeled with the non-linear Angelov devices. The input power is set to +15 dBm, which corresponds to peak efficiency at the higher end of W-band (> 92.5 GHz) for the amplifier. The simulations predict an output power greater than 25 dBm over 75-110 GHz with a peak output power of 26.9 dBm at 98.6 GHz. Over W-band, a minimum PAE of 11% with 17% peak PAE at 98 GHz. A large-signal gain of > 10 dB is achieved over 75-110 GHz.

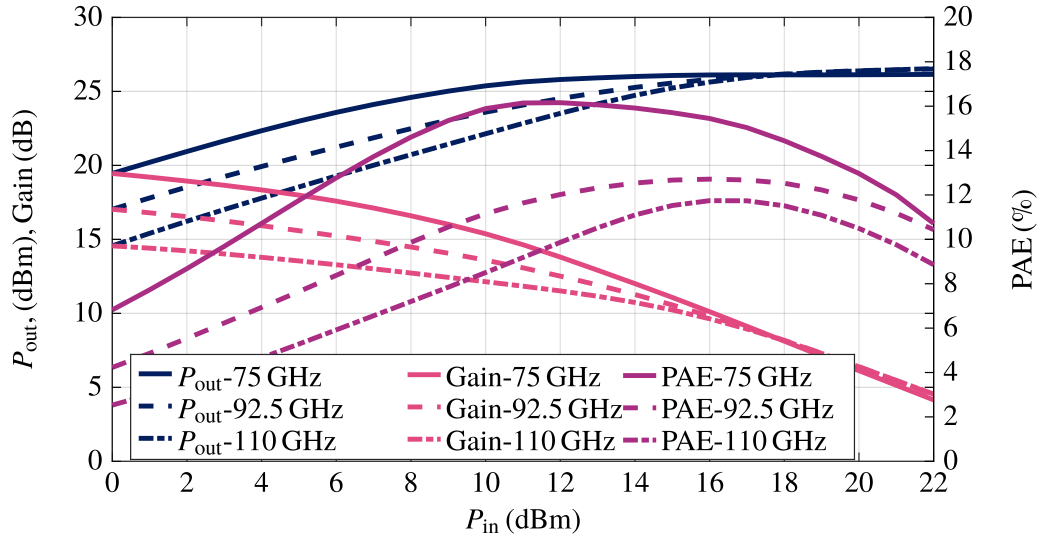

Figure 5.6: Simulated P_{out}, saturated gain and PAE versus P_{in} at 75 GHz, 92.5 GHz, and 110 GHz for the single-ended T3 process design at a +12 V drain supply voltage with 150 mA/mm drain current.

The simulated P_{out}, gain and PAE versus P_{in} at 75 GHz, 92.5 GHz, and 110 GHz curves for the single-ended amplifier biased at +12 V drain supply voltage with 150 mA/mm drain current are shown in Fig. 5.6.

5.2 T3 Power Amplifier Balanced Design

The USSPA design is used in a balanced architecture for further power scaling. The design's output periphery is increased from the 300 μm of the USSPA to 600 μm. The layout of the balanced amplifier using the T3 process is shown in Fig. 5.7 and occupies a total chip size occupies 3.72×2.1 mm^2. The simulated frequency response for the balanced amplifier is shown in Fig. 5.8. The bias voltage, V_d = +12 V, and quiescent bias current in class-AB, I_{ds} = 150 mA/mm, as modeled with the non-linear Angelov devices. The input power is set to +18 dBm, which corresponds to peak efficiency for the amplifier. The simulations predict an output power greater than 27.7 dBm over 75-110 GHz with peak output power of 29.4 dBm at 79 GHz. A minimum PAE of 9.6% is maintained over W-band with a 13.9% peak PAE at 77 GHz. A large-signal gain of > 9.3 dB is achieved over 75-110 GHz. The simulated P_{out}, gain and PAE versus P_{in} at 75, 92.5, and 110 GHz curves for the single-ended amplifier biased at +12 V drain supply voltage with 150 mA/mm drain current are shown in Fig. 5.9.

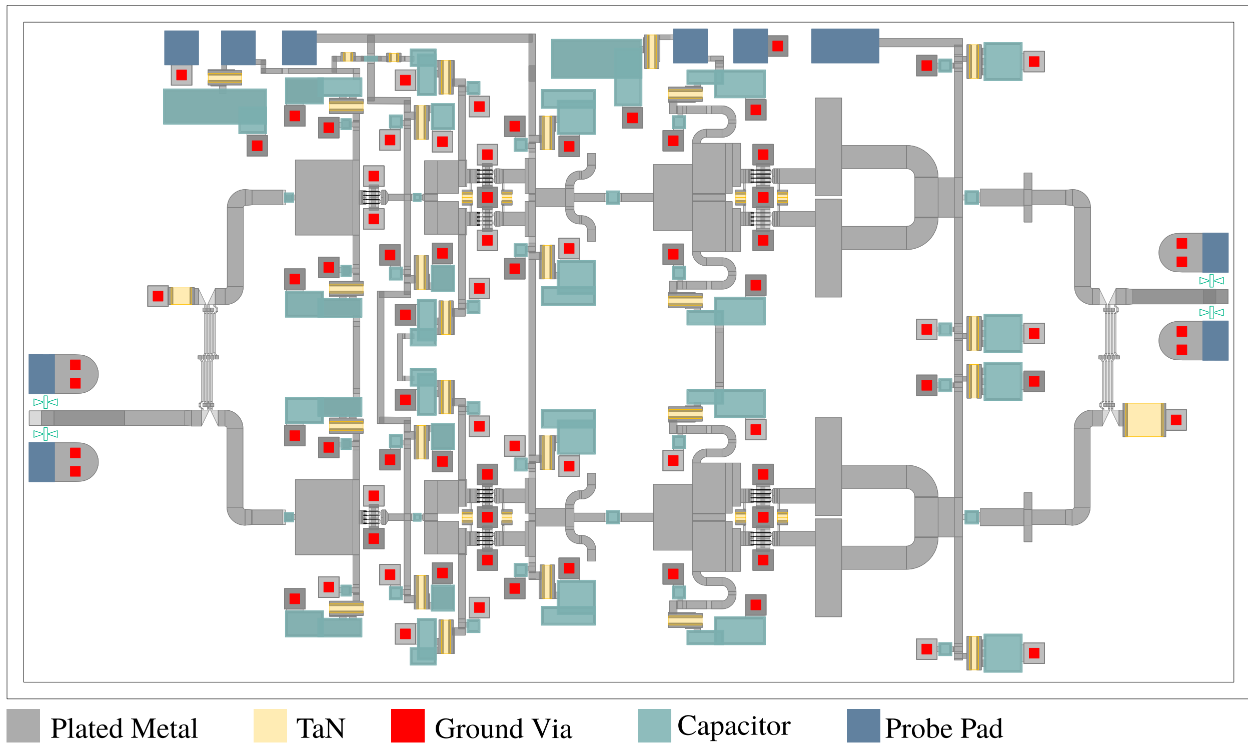

Figure 5.7: Layout for the balanced amplifier with RF and bias pads. The total design occupies $3.72 \times 2.1\,\mathrm{mm}^2$.

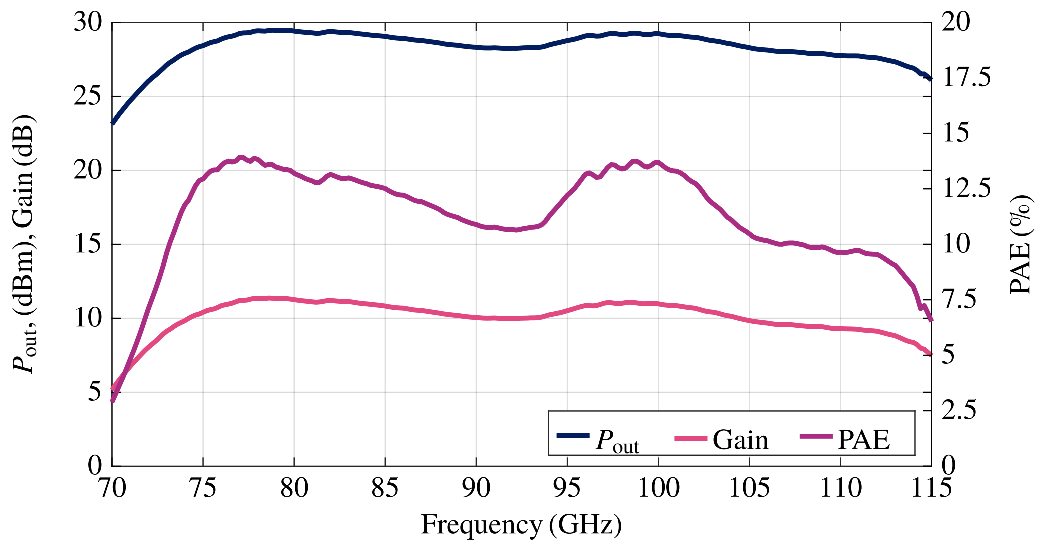

Figure 5.8: Simulated frequency response for the balanced configuration T3 process design with P_{in} = +18 dBm under bias conditions (V_{d}, I_{ds})= (+12 V, 150 mA/mm).

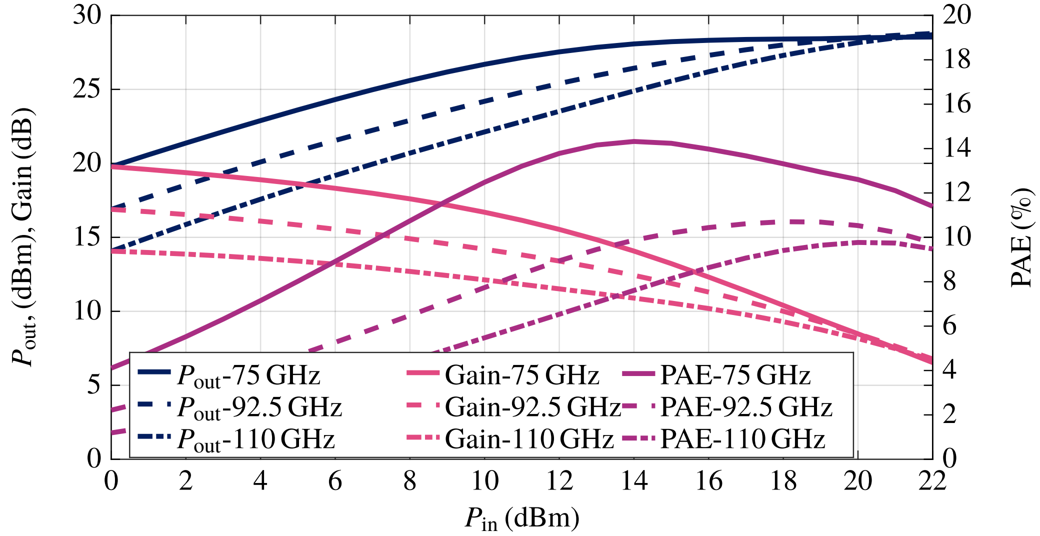

Figure 5.9: Simulated P_{out}, saturated gain and PAE versus P_{in} at 75 GHz, 92.5 GHz, and 110 GHz for the balanced configuration T3 process design at a +12 V drain supply voltage with 150 mA/mm drain current.

5.3 On-Wafer Measurements

The amplifiers were fabricated on a 3×5 mm^2 chip as shown in Fig. 5.7. The die includes additional test circuits for the process testing. For low-frequency bypassing and stability, the die was epoxied on a metal carrier plate with MIM capacitors placed close to the die to reduce bond wire inductance between chip and off-chip capacitors.

The small-signal measurements were taken on a single, stabilized single-ended amplifier. The on-wafer probing measurement station is shown in Fig. 5.11. The HP8510 with W-band frequency extenders is used for the network analyzer. WR-10-to-1 mm connectors are used at the output of the frequency extenders that connect to the GSG probes using 1 mm cable. Calibration standards are used to calibrate to the output of the GSG probe.

The bias conditions of the small-signal measurements are $V_{\text{d}} = 6$ V with drain current, I_{d}, of 139 mA. The measurements for $|S_{21}|$, $|S_{11}|$, and $|S_{22}|$ shown in Fig. 5.12 for 75 to 110 GHz and compared to simulated results.

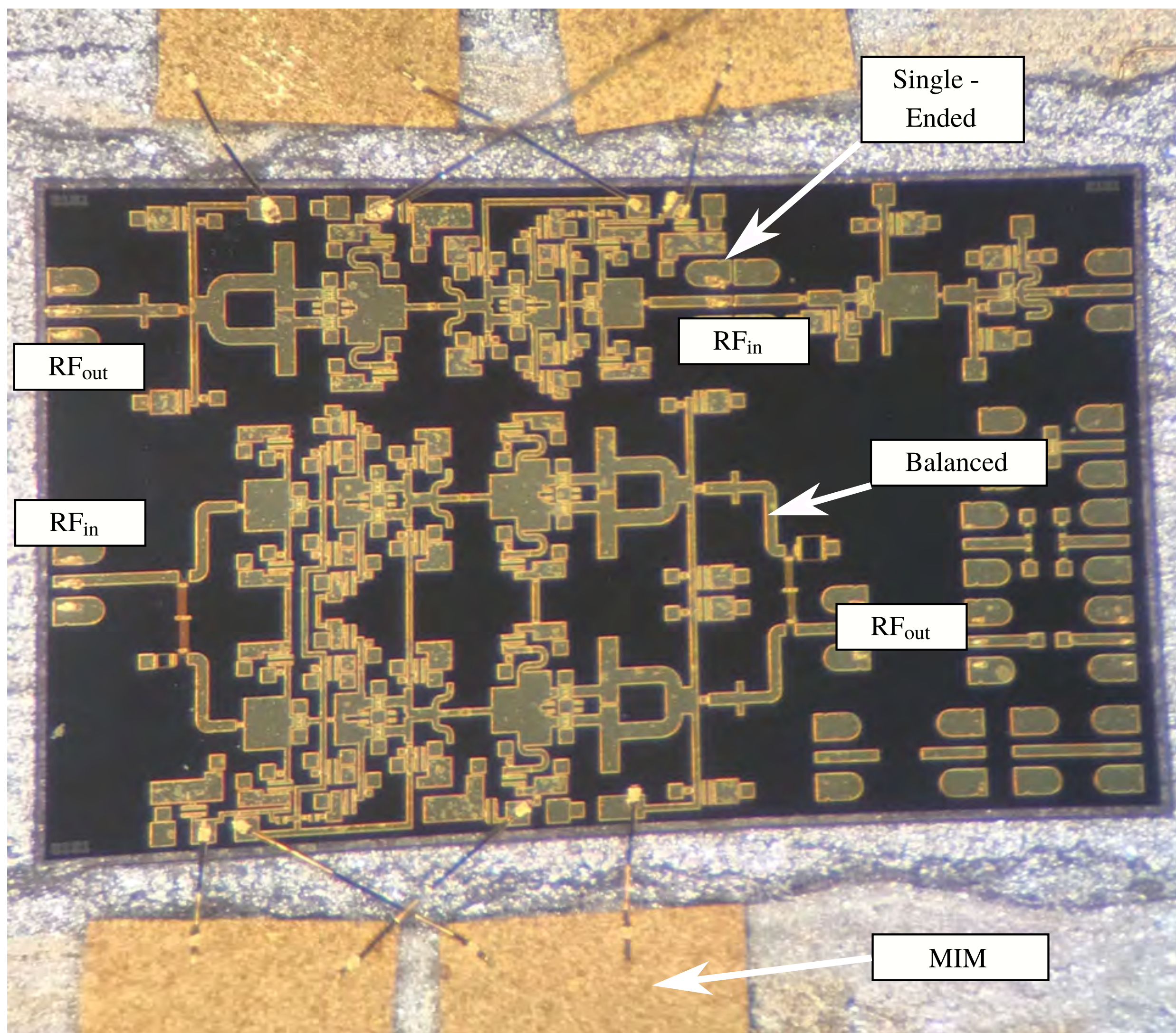

Figure 5.10: Photograph of the die that occupies $3 \times 5\,\text{mm}^2$ containing the multiple circuits with indications for circuits from Fig. 5.4 and Fig. 5.7.

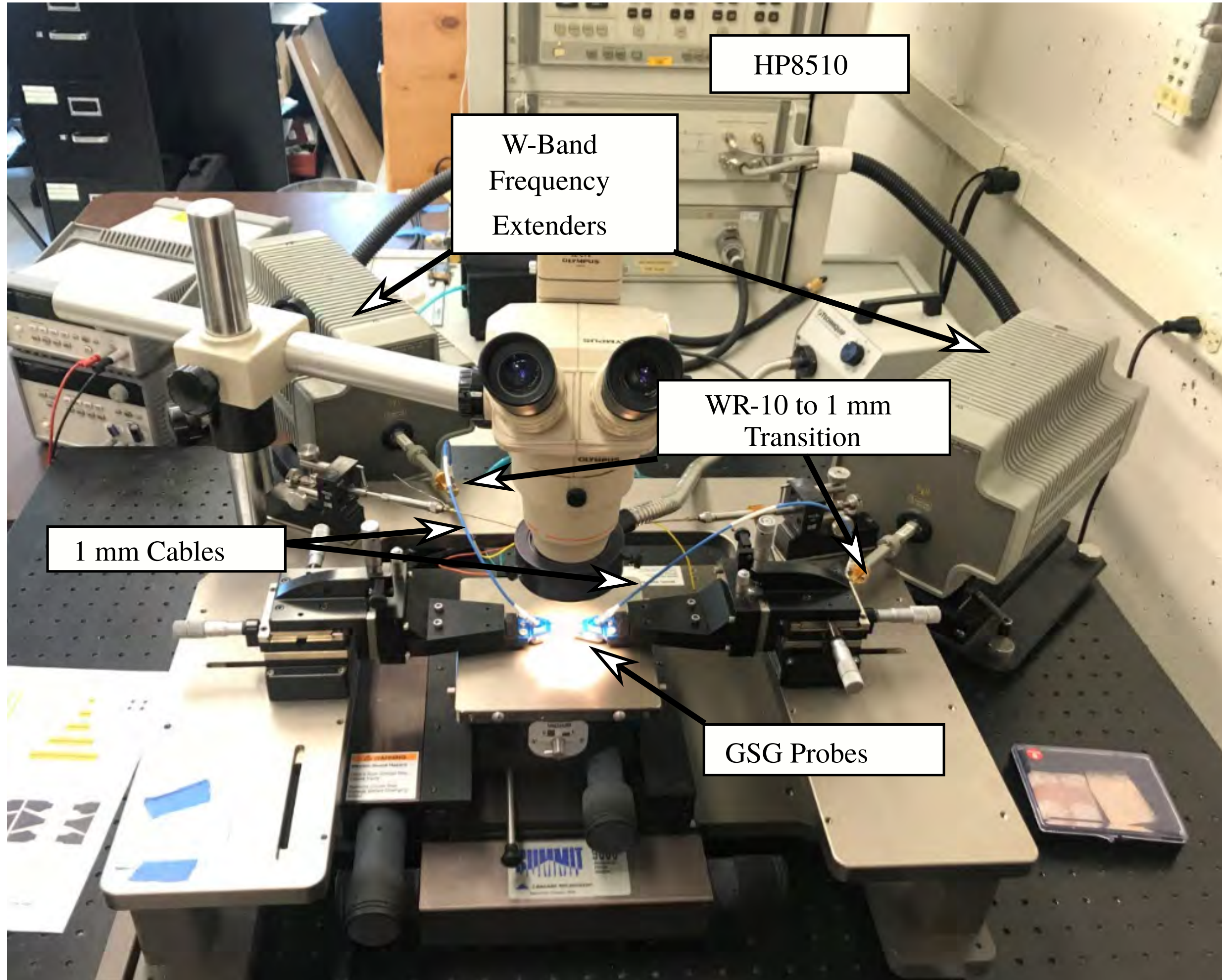

Figure 5.11: W-band on-chip measurement test station using HP8510 with W-band frequency extenders, WR-10-to-1 mm, 1 mm cable and GSG probes.

5.4 Conclusion

In summary, this chapter presents the analysis and design of two W-band power amplifiers using HRL's T3 T-gate process. Simulated results predict widest bandwidth with highest power covering the complete W-band, 75-110 GHz. The results are summarized in Table 5.1 with a comparison between published W-band GaN amplifiers and those presented in Chapter 3 and Chapter 4. The designs presented in this chapter used the knowledge gained from previous designs in Chapters 3 and 4, especially as it relates to combining structures and broadband stability. The contributions from this chapter are presented in [85] where the T3 T-gate W-band process is compared to Qorvo's T-gate process in terms of amplifier performance.

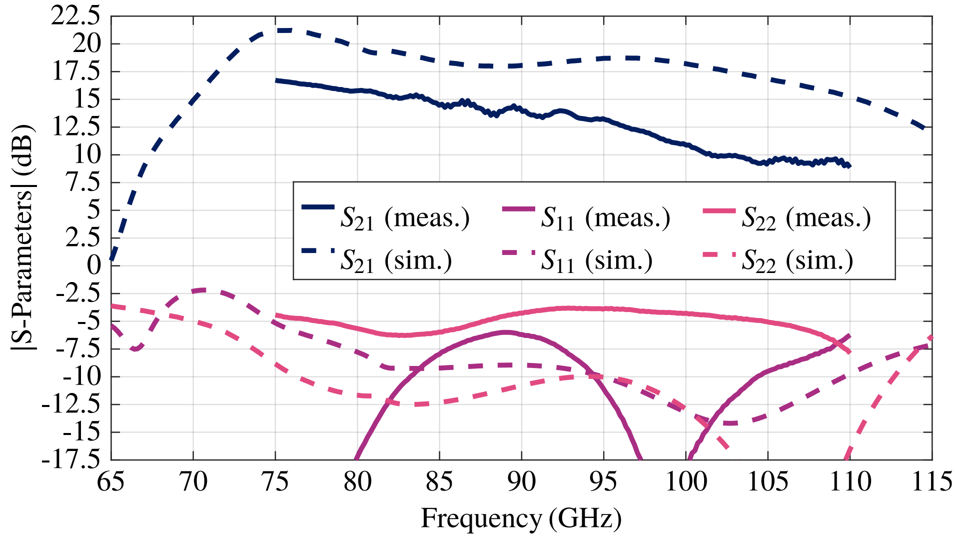

Figure 5.12: On-chip small-signal measurements for the single-ended amplifier shown in Fig. 5.10. The bias conditions are set to $V_{\mathrm{d}} = 6$ V with drain current, I_{d}, of 139 mA.

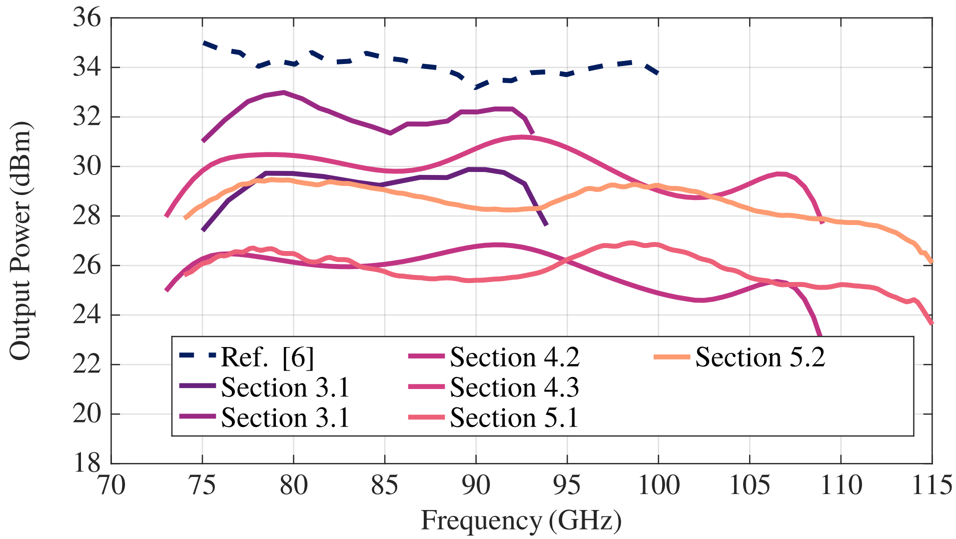

Figure 5.13: Output power versus frequency for state-of-the-art MMIC at W-band including Qorvo GaN09 Γ-gate and T-gate designs presented in Sections 3.1, 3.2, 4.2, 4.3, 5.1 and 5.2.

Table 5.1: T3 Compared to Published GaN MMIC Power Amplifiers at W-Band

Reference	Peak Output Power (W)	Bandwidth (GHz)	PAE (%)	Chip Size (mm^2)
[83]	3	75-100	12	5.4×2.75
[38]	1.2	91	20	2.5×0.9
[38]	1.7	91	11	2.9×1.6
[46]	0.5	70-75	10	3.5×1.75
[47]	0.842	83-92	14.8	-
[45]	1.5	92-96	17.8	-
Section 3.1 (single-ended)	0.979	76.6 - 92.7	5.8	3.5×1.91
Section 3.2 (balanced)	1.88	76.6 - 92.7	5	3.98×3.76
Section 4.2 (balanced)	0.543	75-108	8	3.9×1.84
Section 4.3 (serial)	1.27	75-108	8	3.9×3.81
Section 5.1 (single-ended)	0.49	75-110	11	3.12×1.11
Section 5.2 (balanced)	0.87	75-110	9.6	3.72×2.1

Chapter 6

Millimeter-Wave Power Combining

Contents

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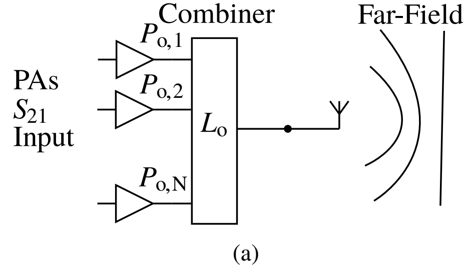
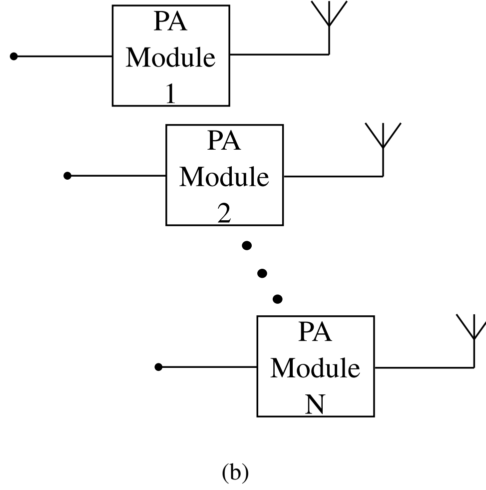
Power combining at millimeter-wave frequencies faces challenges that include high combiner losses, low available power per element, packaging tolerances, and heat removal due to low efficiency and small size of components. As briefly introduced in Fig. 1.2 there is a trade-off between different combining levels, especially between device and spatial ends. The goal of this chapter is to critically investigate this trade-off.

In Fig. 6.1(a), multiple amplifiers are combined into a combiner that has inherent ohmic losses and associated combining efficiency. The corporate-combined amplifiers are fed into a single antenna element, and then spatially combined through an array shown in Fig. 6.1(b). The design trade-offs in combining efficiencies between each level of combining range from thermal considerations at the device level as presented in Chapter 2, to space and weight considerations at the circuit and radiator level [3]. The issue presented in MMIC power combining is that the power amplifier designs do not scale linearly with wavelength.



(a)



(b)

Figure 6.1: (a)Combining of multiple PAs behind an antenna element. (b) Combining multiple active antennas for spatial power combining.

Therefore, the chip size becomes an increasing fraction of the unit call size of $\lambda/2$. In addition, for binary combiners placed after the MMIC and before the antenna, the number of combined elements quickly reaches the point of diminishing return due to insertion loss and size. This chapter focuses on circuit level while the analysis of spatial level upon radiation is discussed in Chapter 7.

For a multi-stage combiners considering K-binary stages, with L_{stage} loss per stage, and P_{o} output power per device, the total output power is given by [3]

$$P_{\text{out}} = P_{\text{o}}\, 2^K\, L_{\text{stage}}^K \tag{6.1}$$

which yields a total combining efficiency of the K-stage combiner,

$$\eta_{\text{comb}} = L_{\text{stage}}^K \tag{6.2}$$

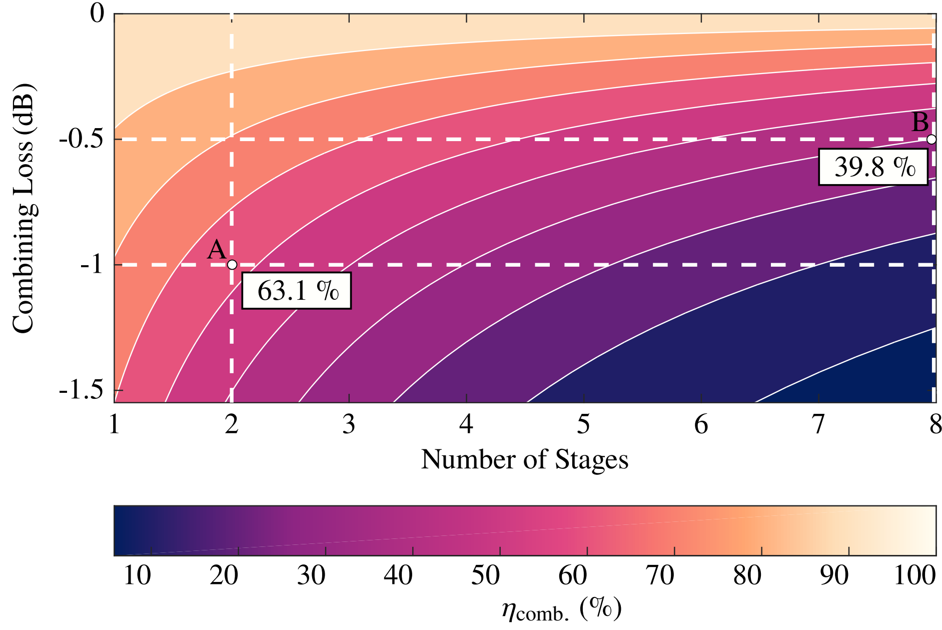


Figure 6.2: Combining efficiency, $\eta_{\text{comb.}}$, for multi-stage combining considering K-binary stages and L_{stage} loss per stage.

Figure 6.2 shows the combining loss as a function of number of stages, point to the rapid roll off in combining efficiency with number of elements combined. A 2-way combiner with a loss of 1 dB indicated by point A will achieve a combining efficiency of 63.1 %. Similarly, an 8-way combiner with lower loss of 0.5 dB shown by point B, will achieve a total combining efficiency of 39.8 %.

Analysis of power combined networks based on scattering parameters at the circuit and spatial levels has been explored in [86]. The results of [86] assume all input ports to be properly matched and all through paths to the output to be identical. The importance of this approach is that it provides the analysis of errors caused by variations in the PAs being combined. Even further, shifts in port impedances contribute to source-pulling between each of the ports which causes odd-mode operation within a non-isolated, in-phase combiner.

This chapter presents a more rigorous analysis of device and circuit level combing efficiency. In Section 6.1, a presentation of generalized scattering parameters is given with a further extension to active excitation of linear multiport networks. In Section 6.2, an analysis of combining efficiency for various on-chip combining architecture is given. Finally in Section 6.3, power combining using thin-film non-isolated

combiners and waveguide combiners is analyzed. The statistical W-band wafer data from the measured results in Chapter 3 is then used for numerical simulation for final circuit level combining efficiency.

6.1 General Scattering Parameters and Non-Symmetric N-Port Networks

The theory of generalized scattering parameters is presented in detail in [87–89]. In this section an extension for active scattering parameters is presented using the theory of multiple excited networks [71, 90], therefore providing a method for the analysis of combining networks with complex arbitrarily terminated port impedances and varying amplitude and phase. For example, a reactive in-phase power combiner on-chip provides a transformation from the optimal drain impedance to an external 50 Ω load, and can suffer from an impedance variation at the drain caused by potential device failure. The degradation in combining efficiency caused by asymmetrical impedance loading at the drain is further captured by this generalization.

Starting from a multiport scattering matrix, **S**, referenced to 50-ohms, a transformed scattering matrix referenced to an arbitrary complex impedance is given by

$$\mathbf{S}^{'} = \mathbf{\Lambda}^{-1} \left\{\mathbf{S} - \gamma^{*}\right\} \left\{\mathbf{U} - \gamma\mathbf{S}\right\}^{-1} \mathbf{\Lambda}^{*} \tag{6.3}$$

where $\boldsymbol{U}$ is the identity matrix, and $\mathbf{\Lambda}$ is the diagonal matrix with element values

$$\Lambda_j = \left(1 - \boldsymbol{\gamma}_j^{*}\sqrt{\frac{1 - \boldsymbol{\gamma}_j \boldsymbol{\gamma}_j^{*}}{\left(1 - \boldsymbol{\gamma}_j\right)\left(1 - \boldsymbol{\gamma}_j^{*}\right)}}\right). \tag{6.4}$$

with $\boldsymbol{\gamma}$ is a diagonal matrix computed as

$$\gamma_j = \frac{Z_j - R_{oj}}{Z_j + R_{oj}}. \tag{6.5}$$

When a multiport network described by $\mathbf{S}'$ is excited by multiple simultaneous sources, an active matrix **M** is used to describe the network behavior

$$\mathbf{M} = \frac{1}{\sqrt{\psi\psi^{\top}}} e^{j\vartheta} \psi^{\top}\mathbf{S}' \tag{6.6}$$

where ψ is a vector of incident wave amplitudes so that $\psi\psi^{\top}$ is the normalization power and ϑ is the vector consisting of phases of all the excitation waves. This formulation is used later in this chapter to analyze statistical variations between MMICs and their effect on amplitudes and phases at the outputs of multiport off-chip combiners. The results of Eq. (6.6) are used in subsequent sections for active excitation of networks with amplitude and phase errors.

6.2 On-Chip Combining

On-chip combining starts with device periphery scaling which was investigated in [91] and [92], while device-level modeling for scaling of MOS transistors were presented in [93] and [94]. Once the appropriate periphery is reached by device level scaling, on-chip power combining using reactive networks increases the power ideally by N, where N is the number of transistors as shown in Chapters 3 to 5. In reality, the combining efficiency is not 100 % and is given by $P_{\text{out}}/(N \cdot P_{\text{transistor}})$. Since this efficiency is limited by the loss of a corporate networks given by Eq. (6.2), additional power increase can be obtained in a balanced or serial architecture.

6.2.1 Corporate, Balanced, and Serial Combining

For reactive in-phase power combining, odd-mode operation can result in device failure. When this happens, the failed device will have some undetermined drain impedance causing the corporate output combiner to be asymmetrically loaded. Here the results are shown for open and short circuit loading extremes, but the approach is valid for any impedance values in terms of their effect on combining efficiency.

In Fig. 6.3 (a) and (b), two- and four-way combiners used in the designs in Chapters 3 to 5 are shown. The active even-mode transmission, T_{e}, for Qorvo Γ-gate, Qorvo T-gate, and HRL T3 MMIC PA designs presented in Sections 3.1, 4.1 and 5.1, respectively, are shown in Fig. 6.3 (c) with corresponding combining efficiency in (d). Degradation of the combiner under open and short loads are shown in Fig. 6.4 for each of the reactive combiners used in the various PA designs. The 4-way output combiner shows more graceful degradation over the 2-way combiner that suffers from approximately 40 % reduction under open load for

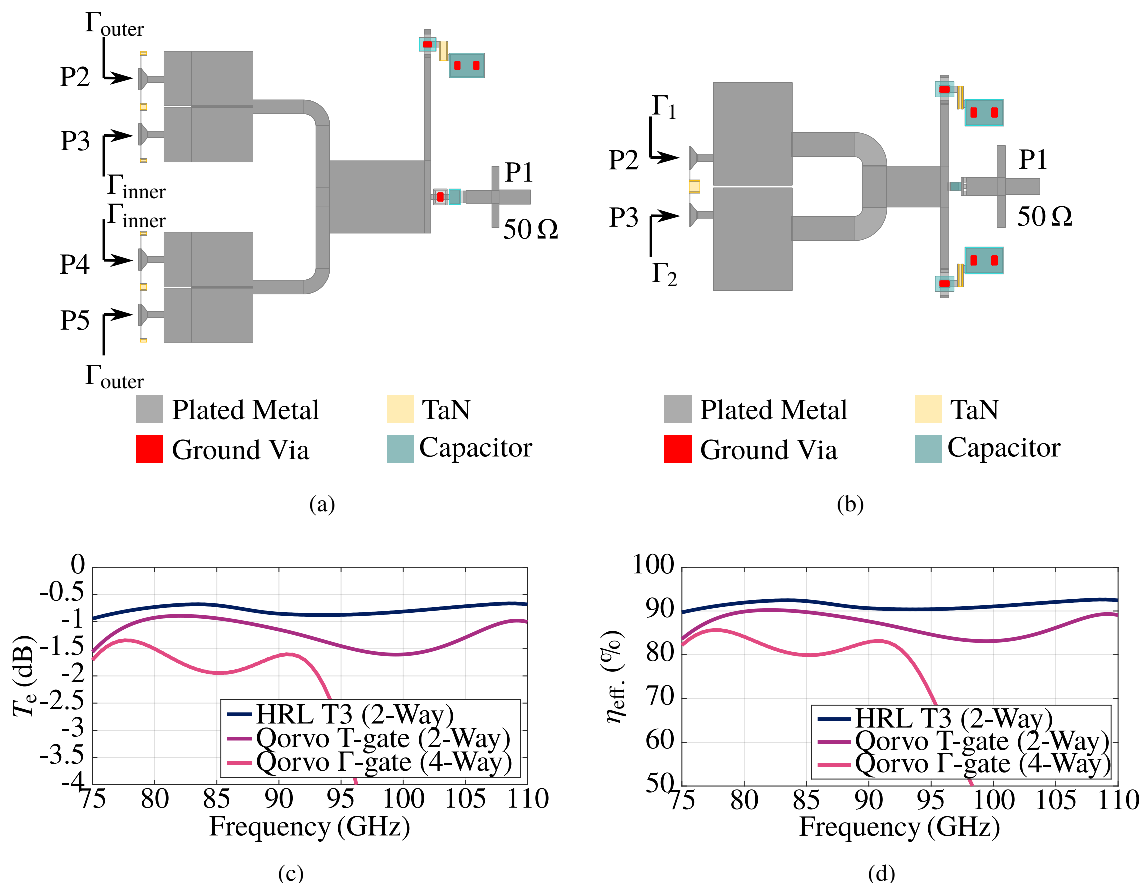


Figure 6.3: (a) 4-way reactive in-phase combiner from Section 3.1. (b) 2-way reactive in-phase combiner from Sections 4.1 and 5.1. (c) Active even-mode transmission, T_e, for Qorvo Γ-gate, Qorvo T-gate, and HRL T3 MMIC PA designs presented in Sections 3.1, 4.1 and 5.1, respectively. (d) Combiner efficiency, $\eta_{eff.}$, for Qorvo Γ-gate, Qorvo T-gate, and HRL T3 MMIC PA designs presented in Sections 3.1, 4.1 and 5.1, respectively.

the case of the Qorvo GaN09 T-gate MMIC.

As discussed in Chapters 3 to 5, after the reactive combiner, the next level of power combining includes architecture combining. Many of these architectures include the use of hybrid couplers. Using state-of-the-art MMIC processing, fabricating compact Lange couplers becomes feasible. Typical insertion loss of Lange couplers in the GaN-on-SiC process operating in W-band is on the order of 0.5 dB. As shown in Chapters 3 to 5, these Lange couplers can be used for both balanced and serially combined architectures shown in Fig. 6.5. The resulting combining efficiencies, given in Fig. 6.6, are calculated with S-parameters extracted from commercially available method of moments simulator, AWR's AXIEM [59]. The balanced

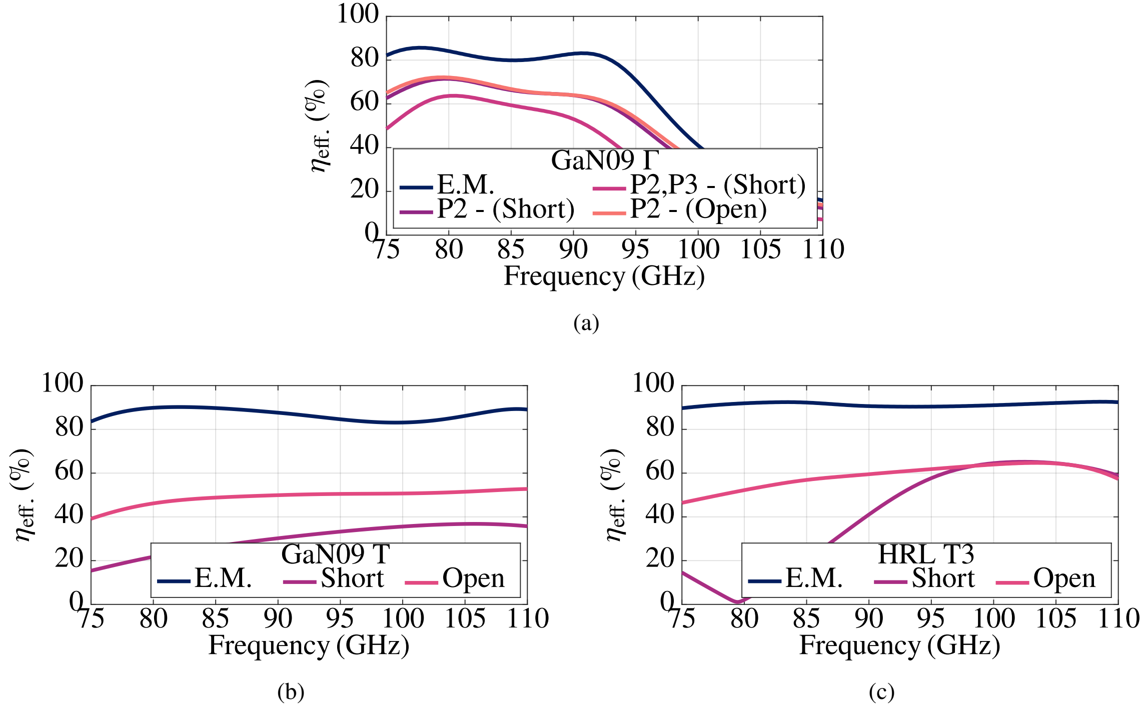


Figure 6.4: Combining efficiency for on-chip corporate in-phase reactive combiners.

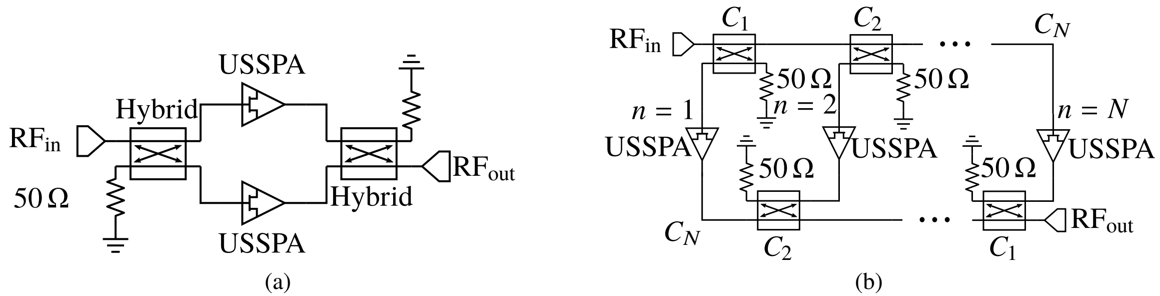


Figure 6.5: Simplified block diagram for a (a) balanced PA and (b) serially combined PA.

architecture that combines two amplifiers maintains higher combining efficiency. At the expense of additional wafer space, a serial combiner can be used to combine more than two power amplifiers, while achieving good combining efficiency.

6.3 Off-Chip Combining

Off-chip power combining can be implemented in either thin-film microstrip on alumina or quartz, or waveguide. Though thin-film provides the light weight alternative needed for space constrained systems,

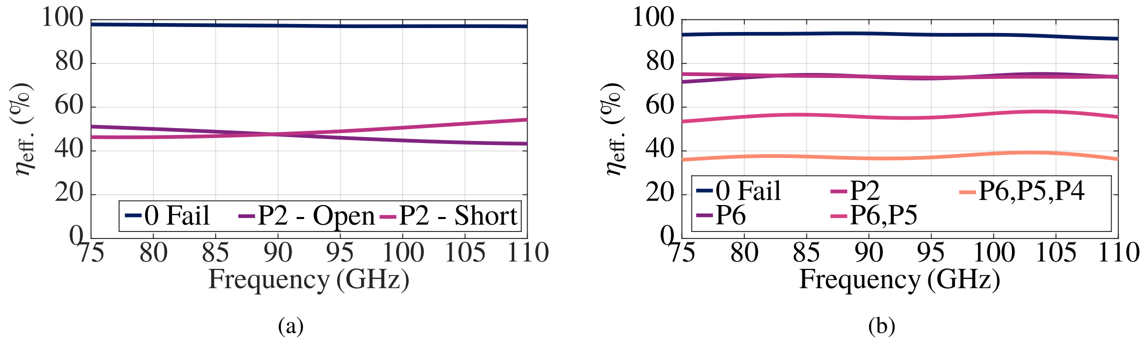


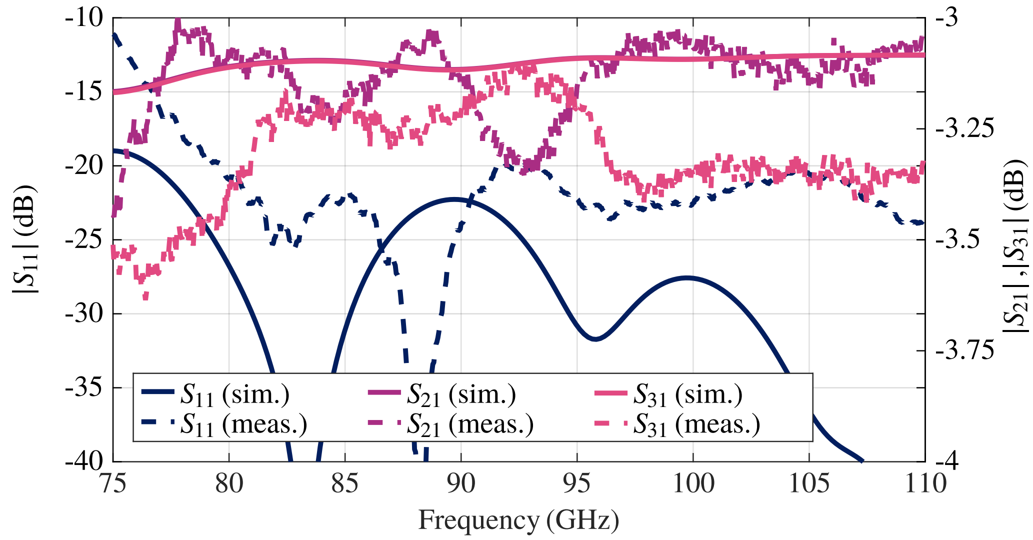
Figure 6.6: Combining efficiency for an on-chip balanced PA combiner in (a) and serially combiner in (b). Additional results showing degradation with port failures shown.

lower combining efficiency results due to conduction and dielectric losses caused by electrically large circuits needed to accommodate the MMICs. Recent interest in waveguide additive manufacturing (AM) at millimeter-wave frequencies is described in, e.g. [7, 95, 96], have provided additional means for waveguide fabrication. Combining efficiencies for standard split block manufacturing and measured AM results from [7] are compared. A comparison between thin-film and waveguide power combining for multiple levels of power combining is presented. In both cases, a non-isolated combiner is typically used. As the even-mode provides perfect isolation between the combined amplifiers, the odd-mode caused by manufacturing variations provides active load-pulling between them. Though desirable in some applications such as Doherty amplifiers, under even-mode, in-phase combining, this effect causes additional reductions in combining efficiency. Figure 6.7(a) shows the S-parameters of waveguide 2-way splitter manufactured with standard split block machining in aluminum with combining efficiency in Fig. 6.7(b). The results are compared to additive manufactured counterparts from [7]. The discrepancy is due to the inherent roughness of the latter.

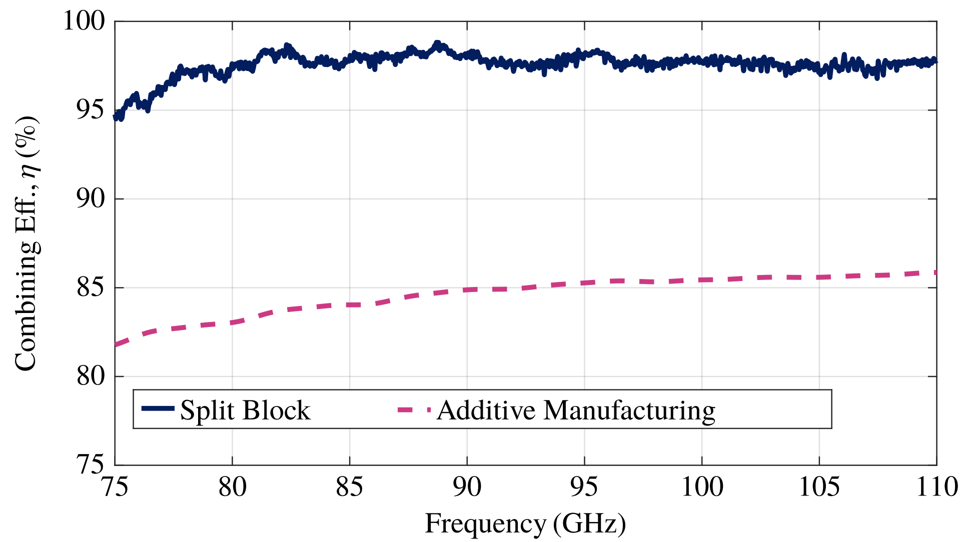
6.3.1 MMIC-to-Waveguide Transitions

In MMICs, the transmission line interconnects are typically microstrip, or coplanar waveguide (CPW) for circuits operating > 100 GHz. To interface to TE_{10} mode in a rectangular waveguide, a mode transition is needed. At millimeter-wave frequencies, parasitic packaging effects begin to dominate the performance of the mode conversion. Additionally, bond-wires detune the performance.

Quasi-Yagi in-line transitions at lower, $X-$band frequencies [97], demonstrated in-line compatible tran-



(a)



(b)

Figure 6.7: (a) S-parameters amplitudes of waveguide splitter manufactured with standard split block machining in aluminum. (b) Combining efficiency for two-way combiner compared to additive manufacturing in [7].

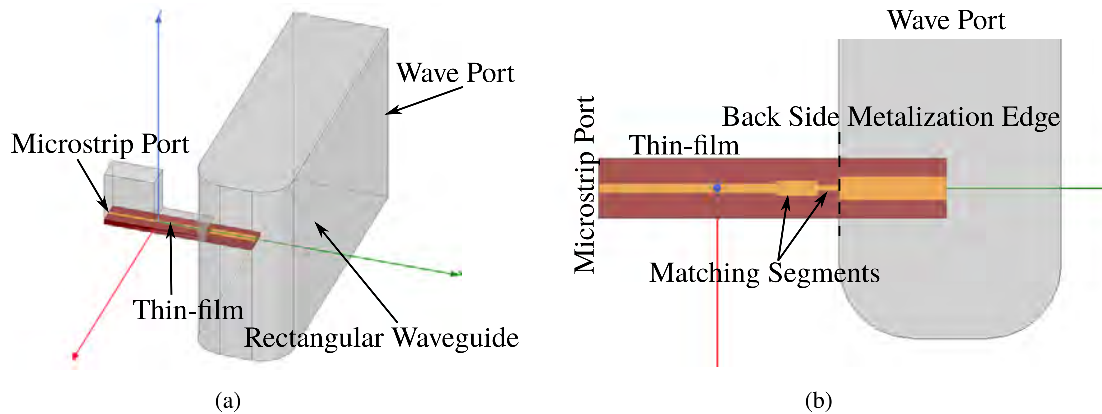


Figure 6.8: (a) A microstrip-to-waveguide transition showing placement of microstrip and waveguide ports. Thin-film alumina (or quartz) substrate interfaces peak E-field for the TE_{10} to the microstrip mode. (b) Top view of transition showing E-plane probe with matching segments. Backside metalization is extended up to the edge of rectangular waveguide.

sitions and have been adopted for flip-chip W-band receiver applications [98]. The issue presented by the flip-chip approach in power applications is the lack of thermal conduction to remove the heat away from the active region of the transistors.

With the first demonstrated on-chip transition from CPW-to-TE_{10} operating at G-band (110-300 GHz) in [99], many efforts continued with demonstrated success above 300 GHz, e.g. [100–102]. Additionally, direct MMIC-to-waveguide transitions using bond wires provide thermally viable solutions demonstrated at W-band in [18, 103]. This approach requires additional careful machining of molybdenum copper (CuMo) that provides excellent thermal conductivity perpendicular to the ground plane of the MMIC and laterally, therefore allowing greater spreading of the heat.

Limitations presented here for millimeter-wave frequencies for E-plane transitions include losses that result in degradation of combining efficiency with off-chip combiners. In Fig. 6.8, a conventional the general geometry of a microstrip-to-waveguide transition is shown. Transitions are typically fabricated on a thin-film alumina (or quartz) substrate that interfaces to the peak E-field for the TE_{10}. A top view of the transition showing an E-plane probe with matching segments is given in Fig. 6.8(b). Backside metalization is extended to the edge of the rectangular waveguide such that no backside metalization is below the E-plane probe section within the waveguide.

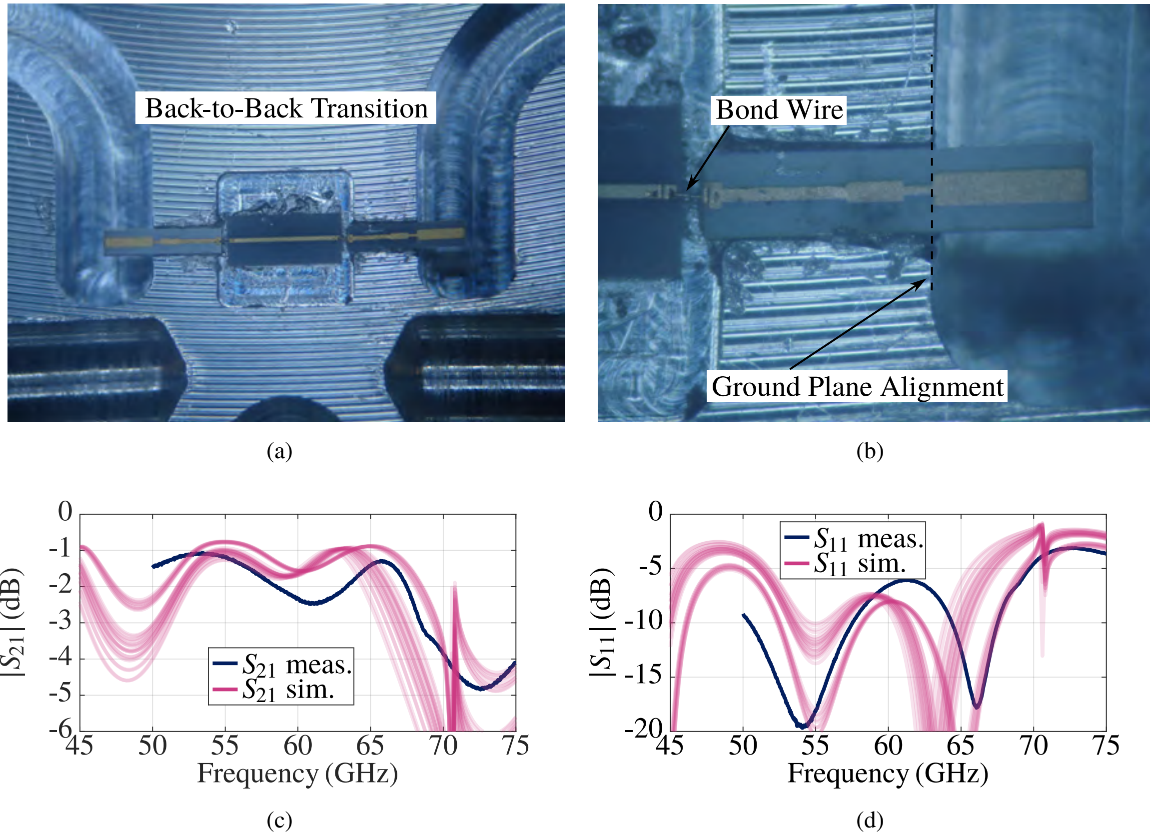


Figure 6.9: (a) Back-to-back transition of V-band transition of E-plane probes fabricated in split block machining using aluminum. (b) Single transition showing bond wire from 50 Ω microstrip line to transition segments. (c) $|S_{21}|$ measured and simulated results for parametric sweep varying bond wire length and spacing between 50 Ω microstrip segment to E-plane probe transition. (d) $|S_{11}|$ measured and simulated results for parametric sweep varying bond wire length and spacing between 50 Ω microstrip segment to E-plane probe transition.

In Fig. 6.9 (a) and (b), a back-to-back V-band (45-75 GHz) transition to E-plane probes fabricated in split block machining using aluminum is shown. A single transition showing a bond wire from 50 Ω microstrip line on SiC to a E-plane transition segment is measured and compared to simulated results for a parametric sweep varying bond wire length and spacing.

Figure 6.10(a) shows results for lower losses in a single transition in Fig. 6.10(b) by using a pedestal and minimizing distance between MMIC and thin-film substrate. The single E-plane W-band transition from 50 μm SiC substrate to 100 μm alumina substrate uses a 65 μm saw street typical for MMIC dicing. The SiC MMIC substrate is raised on a 50 μm pedestal to reduce length of bond wire transition. At worst case, $|S_{21}|$ results show a maximum loss of 1.5 dB.

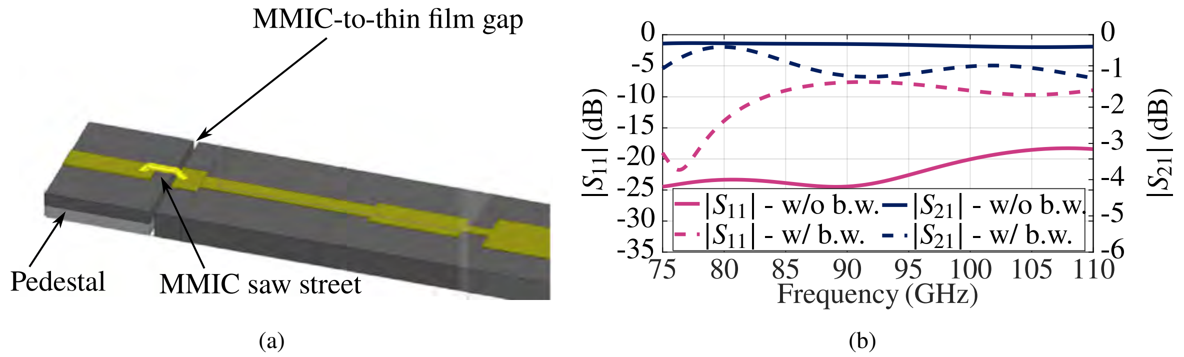


Figure 6.10: (a) Single E-plane W-band transition from 50 μm SiC substrate to 100 μm alumina substrate. A 65 μm saw street on MMIC used that is typical for MMIC dicing. The SiC MMIC substrate is raised by 50 μm pedestal to to reduce length of bond wire transition. (b) Simulations for microstrip-to-waveguide transition at W-band with and without bond wire.

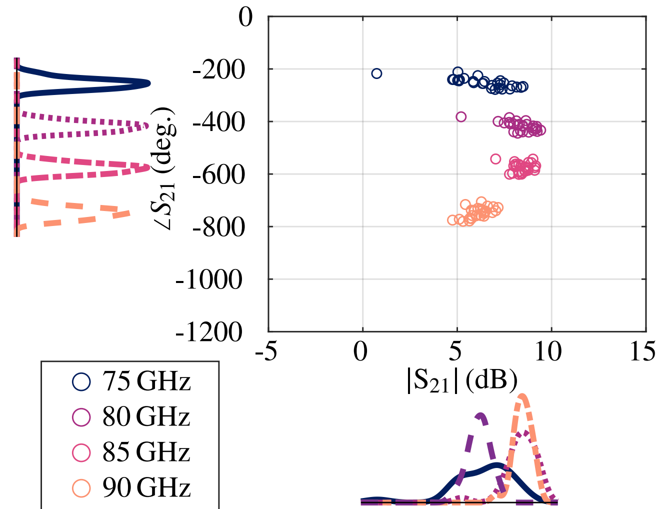


Figure 6.11: Scatter plot for various frequencies plotting magnitude and phase for on-wafer data of the Qorvo GaN09 Γ-gate single-ended design presented in Chapter 3.

6.3.2 Simulation Methods for Statistical Power Combining

Because of fabrication variations it is important to quantify the impact of both MMIC gain amplitude and phase spread across the wafer and fabrication tolerances of the passive combiners, as they all contribute to combining efficiency degradation. The measured data on a subset of approximately 38 MMICs is used to model a larger set, typically Gaussian or multi-modal fitting of arbitrary distributions. In Fig. 6.11, variations in amplitude and phase from a complex data set of S_{21} are shown for various frequencies. The measured

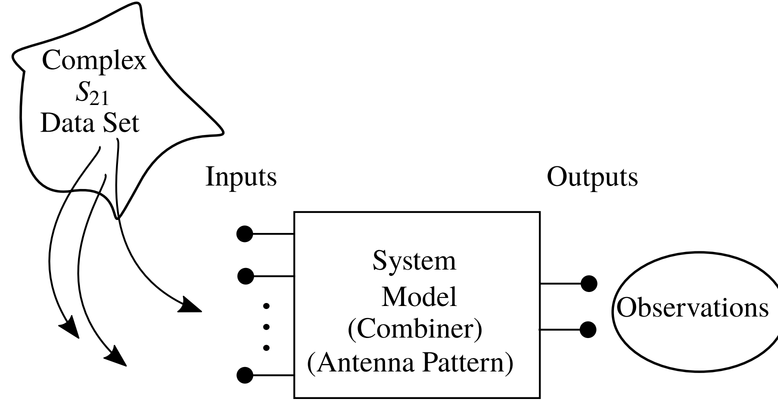


Figure 6.12: Statistical model for simulation in power combining. Variations in amplitude and phase from a complex data set of S_{21} are used for a system model of either combiners and arrays to approximate parameters such as combining efficiency and far-field patterns.

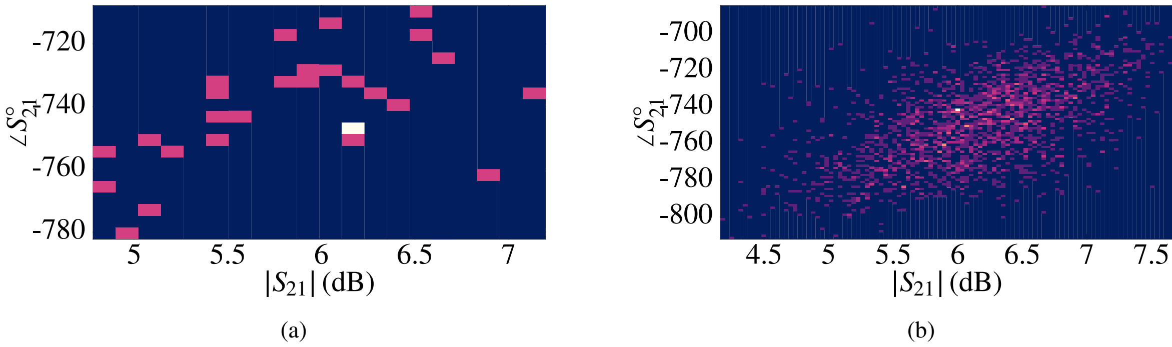


Figure 6.13: Histogram for $|S_{21}|$ versus $\angle S_{21}$ for on-wafer data in (a) and copula generated in (b) at 90 GHz.

data of the complex valued S_{21} use multivariate copula fitting to provide a larger sample set to be used in the simulation. This approach provides the ability to fit multidimensional (in frequency), multi-modal distributions [104]. In Fig. 6.13, an example of generated data using copula fitting is shown for on-wafer measured data. In addition, the measured data may be fitted to an uncorrelated Gaussian distribution for comparison.

Using the measured amplifier and non-correlated multi-modal distribution, a comparison between the two can be used to evaluate the combining efficiency for various K-stage non-isolated combiners. In Fig. 6.14, the simulated combining efficiency performance for 2-, 4-, 8- and 16-way combiners is shown for both thin-film alumina and rectangular waveguide. A comparison is performed between the measured data set and the uncorrelated multi-modal data set. Figure 6.15 shows the degradation in combining efficiency for

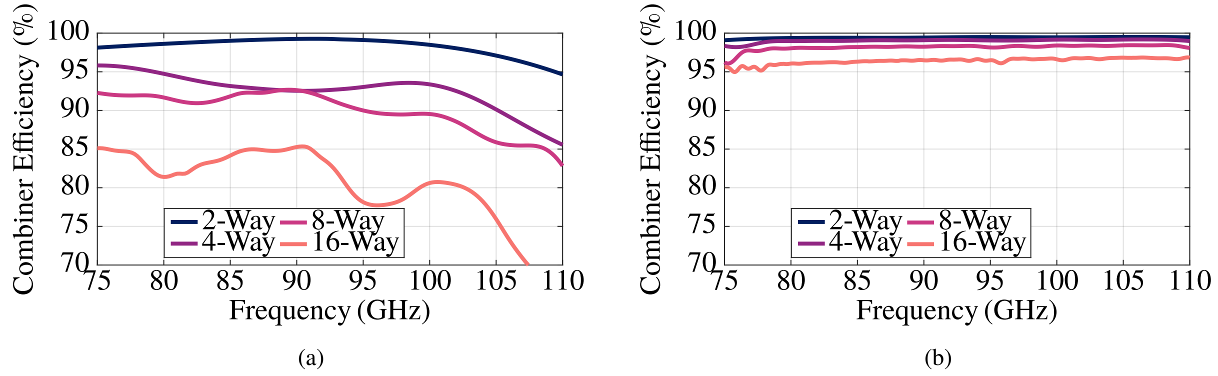


Figure 6.14: (a) Combining efficiency for thin-film alumina substrate for 2-, 4-, 8- and 16-way combiner. (b) Combining efficiency for aluminum waveguide for 2-, 4-, 8- and 16-way combiner.

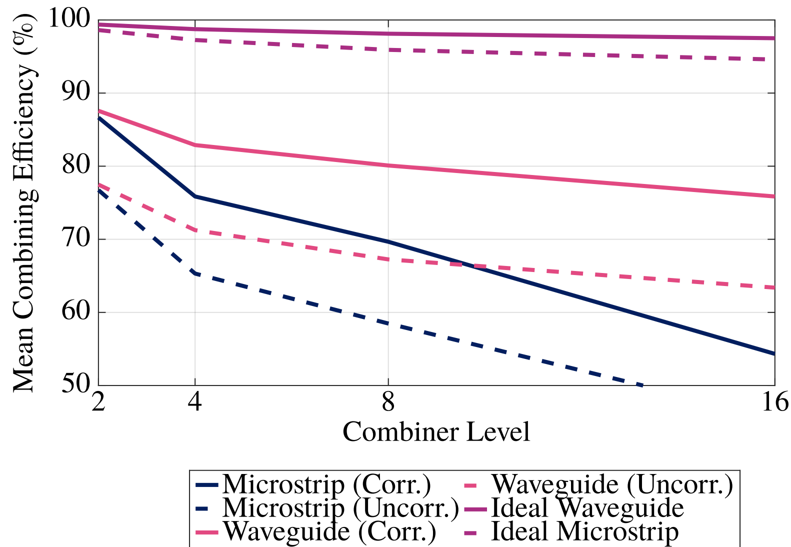


Figure 6.15: Simulation results for mean combining efficiency for 2-, 4-, 8- and 16-way combiner at 80 GHz using alumina thin-film and waveguide.

both cases. As expected the microstrip rapidly degrades in combining efficiency due to both conduction and dielectric losses of the substrate.

6.4 Conclusion

In summary, this chapter focuses on circuit level power combining starting from on-chip combining within a MMIC to off-chip thin-film or waveguide combining for multiple MMIC power scaling. The spread in gain between multiple MMICs on a single wafer is used to analyze degradation of combining efficiency

for off-chip for 2-, 4-, 8-, and 16-way combiners at W-band. Additionally, wire-bonded transitions from microstrip-to-waveguide are analyzed for the dominant mode in WR-10. The contributions are summarized in [105].

Chapter 7

Solid-State W-Band Spatially-Combined Arrays for High Effective Radiated Power

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The context of array pattern degradation based on random amplitude and phase errors was first discussed in [106] and followed by a classical paper of [107]. Traditionally, the analytical treatment for the impact of errors in the far field is considered to be Gaussian distributed with uncorrelated amplitude and phase. From Section 6.3, this is not always the case for sources of errors caused by MMIC amplifiers fabricated on the same wafer. State-of-the-art III-V semiconductor research-level processes can also provide large variations in both magnitude and phase of the transistor gain that may not always be Gaussian and uncorrelated. In

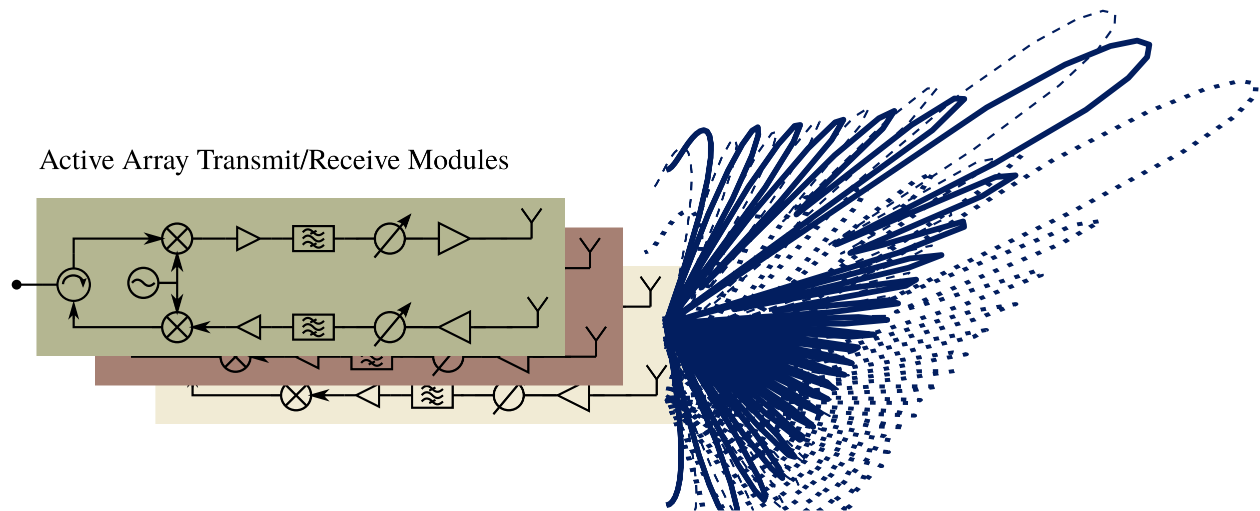


Figure 7.1: Block diagram for an active phased array using multiple transmit/receive modules. Ideal radiation pattern is shown in solid line while beam pointing errors and increased side-lobe levels are clearly seen in dashed line.

addition to affecting the combining efficiency, degradation in the far-field pattern affected by this variation translates to beam pointing errors and increased side lobe levels, affecting the overall performance of the array as shown in Fig. 7.1.

This chapter presents the continuation of the analysis for power combining at the spatial level to achieve high effective radiated power from the output of the active phased array. In Section 7.1, a design is presented of a horn to be scaled and used in linear and planar array configuration. Section 7.2 discusses this horn antenna element in a 4×1 linear array. Section 7.5 concludes the chapter concludes with the analysis of planar arrays for achieving 1.5 kW ERP based on the current state-of-the-art solid-state PAs presented in Chapters 3 to 5.

7.1 Antenna Element Design

For the antenna element, a metallic rectangular aperture is selected for compatibility with active waveguide modules for high power capability and low-conduction losses. The parameters of the horn shown in Fig. 7.2(a), are found through parametric sweep of the aperture dimensions of 1.27 mm by 3.81 mm, and filet radius of the feed to achieve a sufficient match across W-band.

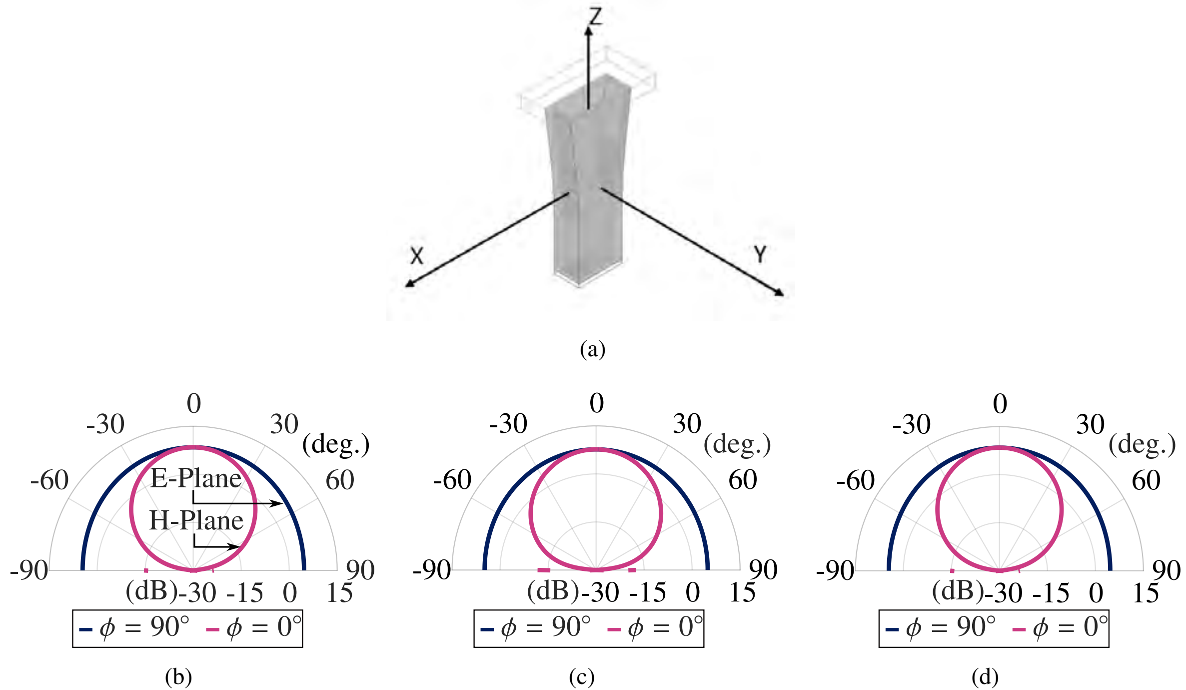


Figure 7.2: (a) Illustration horn antenna element with E-plane along Y-Z and H-plane along X-Z plane. The size of aperture is 1.27×3.81 mm^2 with a standard WR-10 feed of 1.27×2.54 mm^2. (b-d) Element patterns at 75, 92.5, and 110 GHz. The dark blue curves indicate E-plane cuts, and light purple curves indicate H-plane cuts.

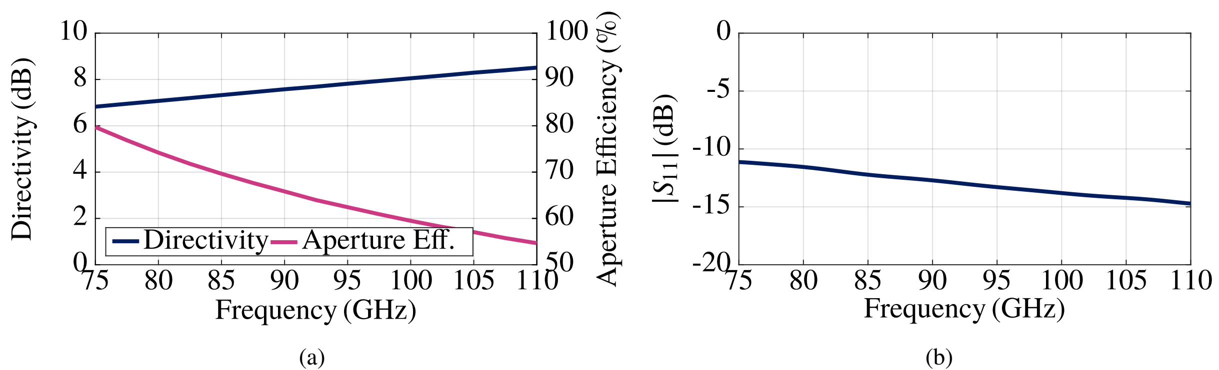


Figure 7.3: (a) Directivity and aperture efficiency versus frequency. The directivity over W-band simulates a minimum D_o = 6.8 dB at 75 GHz and maximum D_o = 8.5 dB at 110 GHz with an aperture efficiency of > 50% maintained across all of W-band. (b) Reflection coefficient versus frequency from 75-110 GHz.

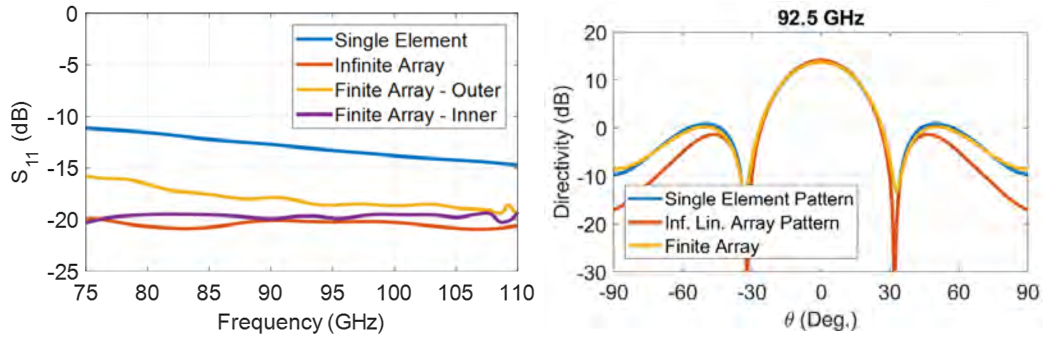


Figure 7.4: (a) Single element comparison to active element of $|S_{11}|$. (b) Single element pattern compared to active element pattern.

In Fig. 7.2(a), the geometrical orientation of the antenna is shown for the respective directivity plots in Fig. 7.2(b)-(d). The antenna element is simulated using commercially available finite element (FEM) electromagnetic solver, ANSYS HFSS [108]. The simulation setup includes perfect electric conductor (PEC) for the metallic structure, boundary integral (BI) to compute the far-field and reduce computational time for the simulations, infinite PEC ground plane in which the horn is flushed, and a wave port excitation to excite the TE_{10} mode. The resulting aperture size is $1.27\times3.81\,\text{mm}^2$ with a standard WR-10 feed of $1.27\times2.54\,\text{mm}^2$. Figure 7.2 (b)-(d) show the obtained antenna patterns. In Fig. 7.3(a), the directivity, D_o, and aperture efficiency, η_a, over W-band are plotted with the $|S_{11}|$ given in Fig. 7.3(b). As seen, typical E- and H-plane patterns are obtained with D_o = 6.8 dB at 75 GHz and D_o = 8.5 dB at 110 GHz. The aperture efficiency is calculated as the effective area, $A_\text{eff.} = D_\text{o}\lambda^2/4\pi$, divided by the physical aperture area, $A_\text{phy.}$, which includes the metallic wall thickness. An aperture efficiency of > 50% is maintained across the entire W-band.

7.2 4×1 Linear Array Design

For the design and analysis of arrays various methods can be used including commonly used element pattern multiplication, infinite array modeling, and finite arrays. Classical pattern multiplication analysis fails to account for mutual coupling that is caused by neighboring antenna elements in an array and assumes the element pattern is independent of the array spacing [109]. The importance of capturing mutual coupling in

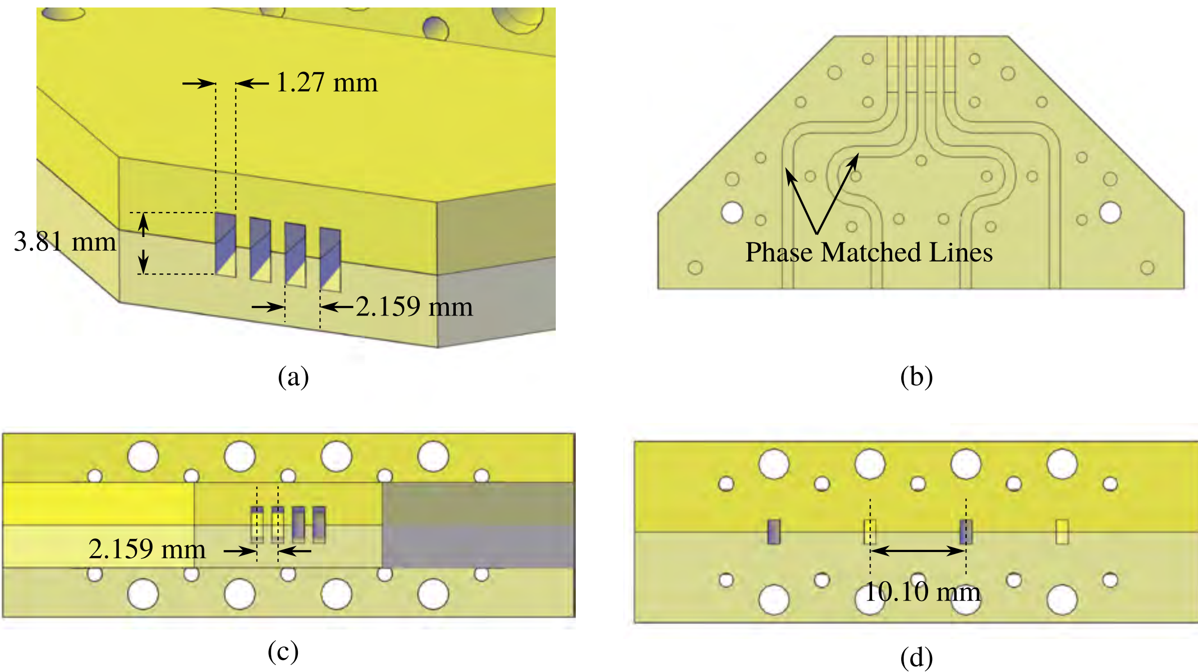


Figure 7.5: 4×1 linear array module with split machining configuration. (a) Radiator elements (b) Top view of half-way split showing phase matched lines for waveguide flange. (c) Front view of the antenna module. (d) Flange view of antenna module.

the analysis of arrays is to observe scan blindness caused by the excitation of surface waves across the array when steered from bore-sight for tightly coupled arrays.

The simulation of the single radiator in Section 7.1 over an infinite ground plane fails to account for mutual coupling. Additional computation of the active element pattern with an element simulated in infinite array conditions. In Fig. 7.4(a), $|S_{11}|$ of a single antenna element pattern over an infinite ground plane from Section 7.1 is compared to the active element reflection coefficient from an infinite array to the 4×1 finite array. As seen, the infinite array antenna has a closer comparison to that of the finite array.

Figure 7.5 shows the model of a 4×1 linear array that is designed to allow for split block fabrication. Phase matched lines shown in Fig. 7.5(b) are used to branch out from the 4×1 linear array input to be fed by a custom flange with overlapping alignment holes of a standard WR-10 waveguide flange. Front and rear views of the linear array split block module are shown in Fig. 7.5 (c) and (d), respectively. Limitations in the split block machining fabrication of the 4×1 linear array are reflected in the aspect ratio of the wall spacing between the array elements to the wall height. With typical machining for W-band device fabrication, the

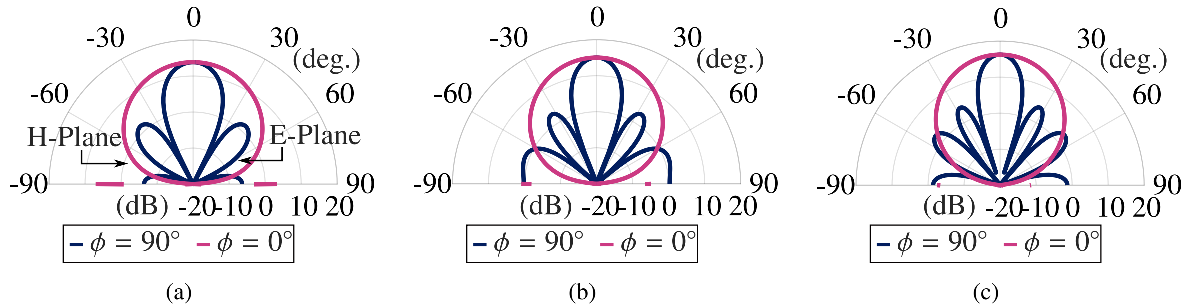


Figure 7.6: Simulated directivity patterns of the 4×1 linear array patterns for (a) 75, (b) 92.5, and (c) 110 GHz at zero scan angle. The dark blue curves indicate E-plane cuts, and light purple curves indicate H-plane cuts.

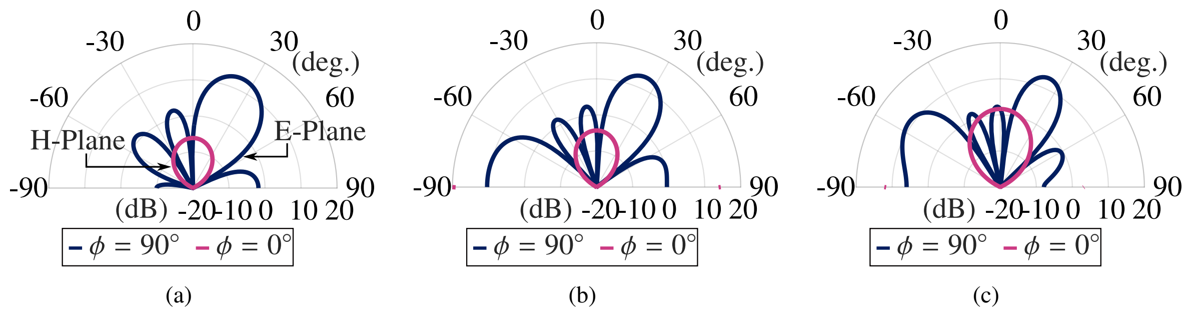


Figure 7.7: Simulated directivity patterns of the 4×1 linear array patterns for (a) 75, (b) 92.5, and (c) 110 GHz at a θ_o = 25° scan angle. The dark blue curves indicate E-plane cuts, and light purple curves indicate H-plane cuts.

aspect ratio is desired to be > 2:1 which reduces the risk in fracturing the wall during fabrication. The design of the array is set to a wall height and width of 1.91 mm and 0.89 mm, respectively, which results in an aspect ratio of 2.15.

The 4×1 linear array pattern is calculated first using the simulated active element pattern in an infinite array. In Fig. 7.6, the active array principal patterns for $\phi = 0°$ and $\phi = 90°$ at 75, 92.5, and 110 GHz are shown. The maximum directivity of the array is given by the highest frequency of operation at 16.3 dB at 110 GHz, 15.1 dB at 92.5 GHz, and 13.9 dB at 75 GHz. In Fig. 7.7, the array is scanned to $\theta_o = 25°$ with corresponding directivity of 13 dB, at 110 GHz, 13.3 dB at, 92.5 GHz and 13.3 dB at 75 GHz. It is worth remembering the directivity of the antenna varies over scan angle typically characterized with the scan loss given by [110]

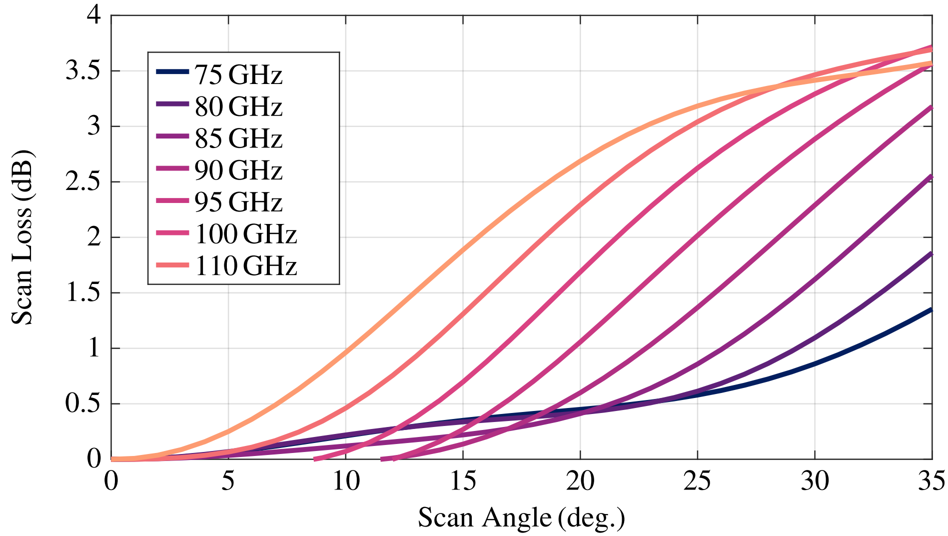


Figure 7.8: Scan loss versus scan angle for 4×1 linear array. Scan loss increases as frequency and scan angle increase due to the element pattern being more directive.

$$\text{Scan Loss (dB)} = 10 \log \left| \frac{D_{\text{o}}}{D(\theta_{\text{o}})} \right| \tag{7.1}$$

where D_{o} is the maximum directivity boresight and $D(\theta_{\text{o}})$ is the maximum directivity scanned at θ_{o}. In Fig. 7.8, the scan loss versus scan angle for 4×1 linear array is shown for various frequencies. At the maximum frequency the scan loss increases due to the element pattern directivity increasing as the electrical size of the aperture increases.

7.3 4×1 Linear Array Module

To allow experimental characterization of the 4×1 linear array, as shown in Fig. 7.9(a), four additional WR-10 components are integrated with the array. The linear array is corporate fed by two 2-way splitters used as a 4-way splitter. The performance of a single 2-way splitter (Section 6.3) shows low loss, as expected from a waveguide component. In addition to the splitters that are compatible with the custom waveguide flange on the antenna array, the array module can be configured with an optional delay line module to scan to $\theta_{\text{o}} = 25°$. The split block can be seen in Fig. 7.9(b). The fabricated module in Fig. 7.10 show various views of the antenna module. The module was fabricated by split block machining in aluminum. The input of the module

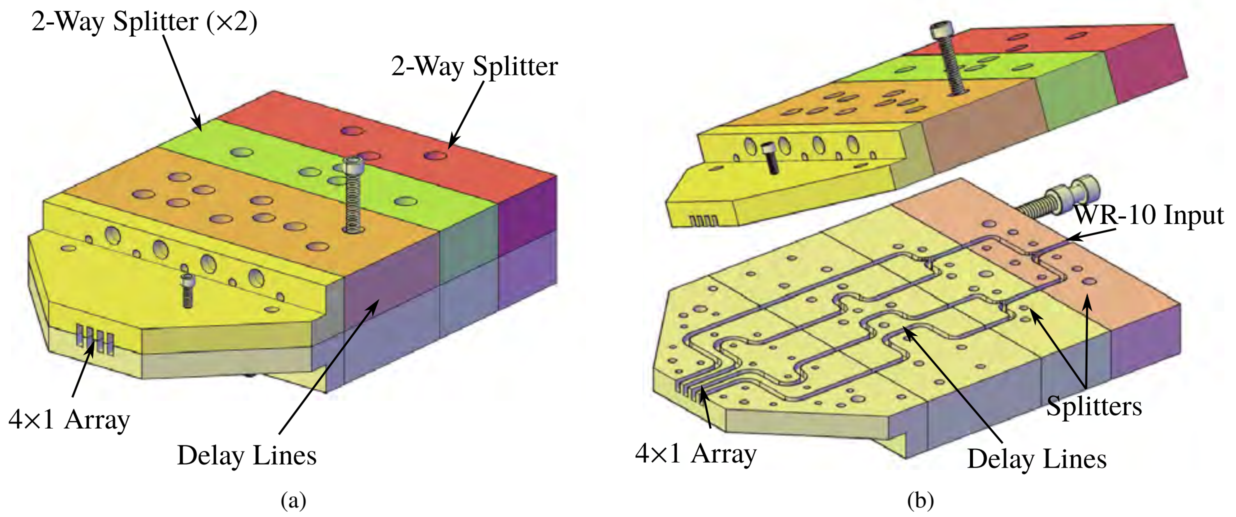
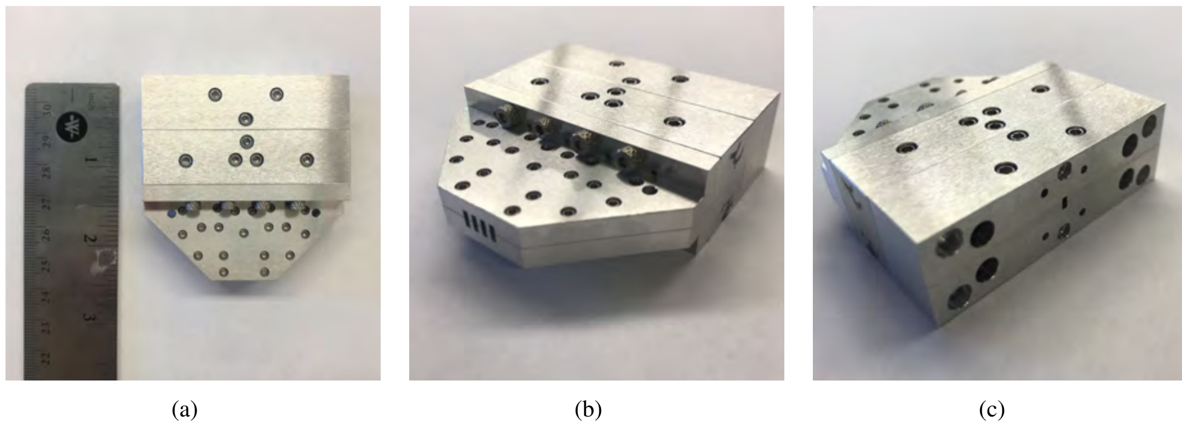


Figure 7.9: (a) Array module with split machining configuration. Module includes: array, delay lines, 2-way splitter (×2), and single 2-way splitter. (b) Split view of module showing inside waveguiding structures.

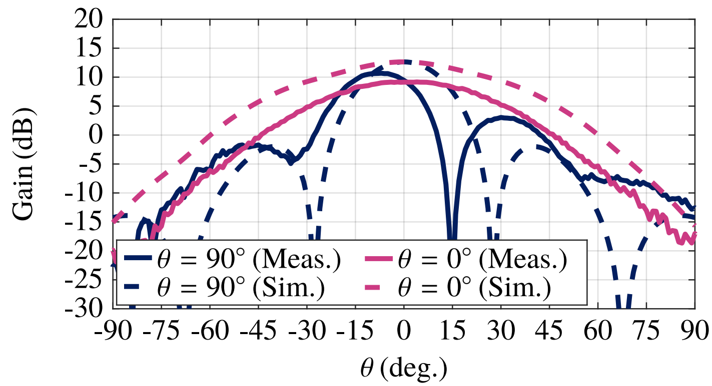


(a) (b) (c)

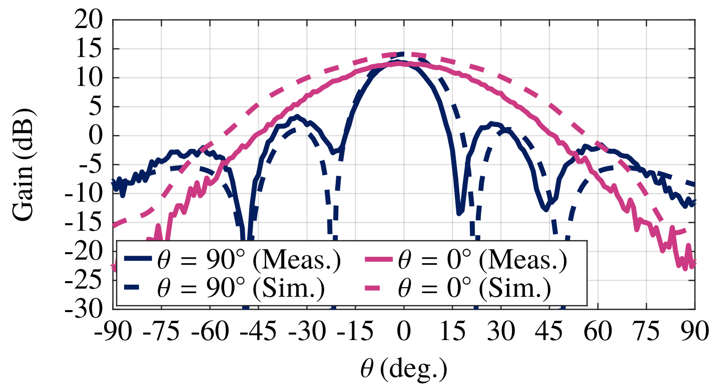
Figure 7.10: Fabricated array module with split block aluminum. (a) Top view of array module for sizing. (b) Front oblique angle of array module. (c) Rear angle showing single, WR-10 input.

contains a standard WR-10 flange.

Antenna gain measurements for the 4×1 linear array module are shown in Fig. 7.11 and are compared to simulated results. Reduction in the gain are due to the conduction losses in the module. Boresight gain versus frequency is shown in Fig. 7.12. Using the delay lines for a $\theta_o = 25°$ scan angle at 85 GHz behind the antenna array element, the measured scanned beam is shown in Fig. 7.13.



(a)



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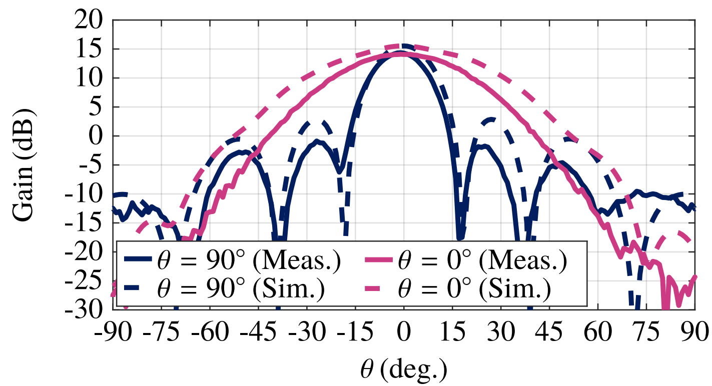


(c)

Figure 7.11: Measured and simulated gain patterns of the 4×1 linear array for (a) 75, (b) 92.5, and (c) 110 GHz at zero scan angle.

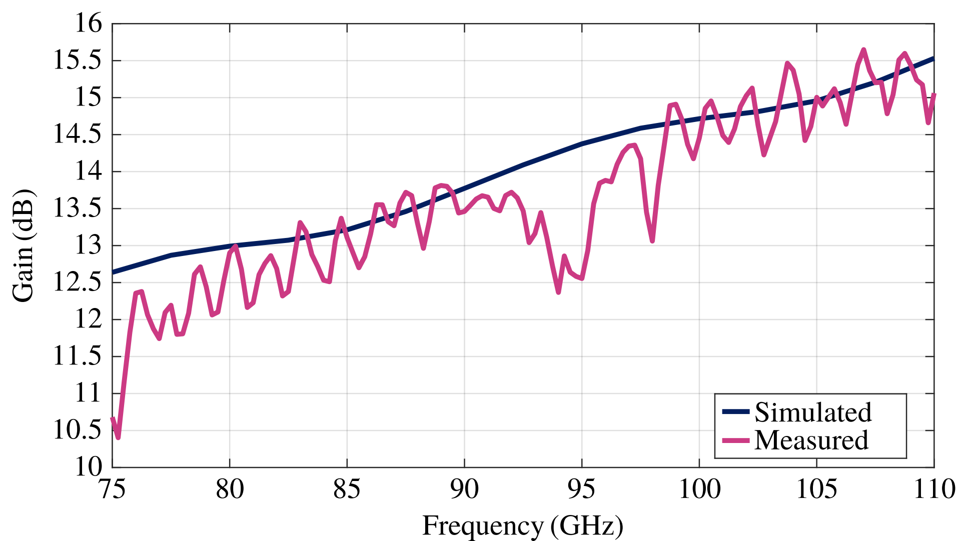


Figure 7.12: Measured and simulated gain boresight gain versus frequency of the 4×1 linear array.

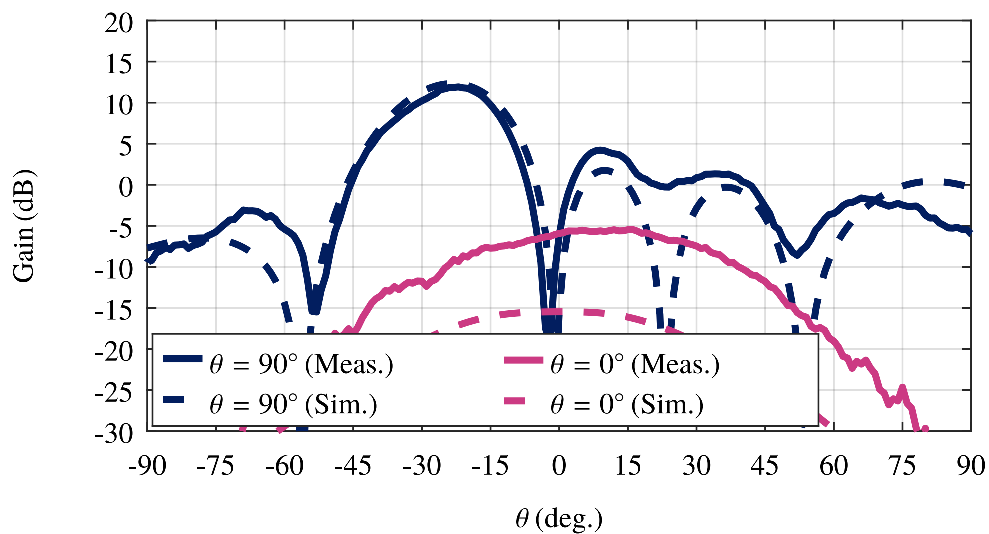
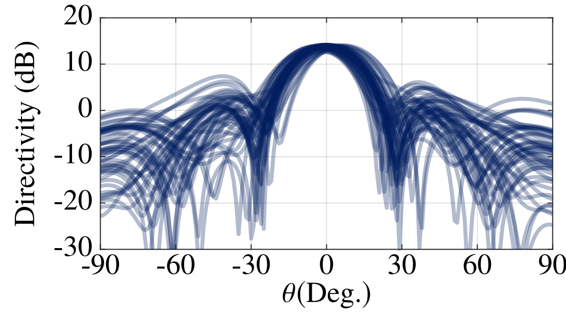
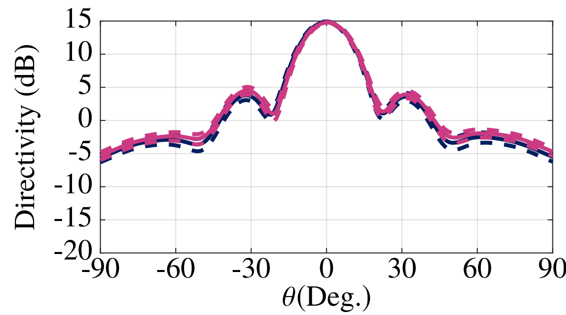


Figure 7.13: Measured and simulated gain pattern of the 4×1 linear array at 85 GHz at a $\theta_o = 25°$ scan angle.



(a)



(b)

Figure 7.14: (a) Antenna patterns for multiple simulated trials for a scan angle of $\psi = 0°$ at 92.5 GHz. (b) Mean patterns (solid) with 95% confidence intervals (dashed) for both the correlated and non-correlated.

7.4 Statistical Analysis of an Active Array using a 4×1 Linear Array

This section presents the analysis of linear array pattern degradation on random errors associated with variations in semiconductor processes. Any state-of-the-art III-V semiconductor research-level process can provide large variations in both magnitude and phase response of transistor gain across a wafer. It is well known that this affects beam pointing in the far-field, increased side lobe levels, affecting the overall performance of the array.

In continuation from Section 6.3.2 and model represented by Fig. 6.12, the simulation method using the variations in magnitude and phase of S_{21} that have been measured and shown previously in Fig. 6.13. For the following simulations, it is assumed that one amplifier is placed behind each radiating antenna element

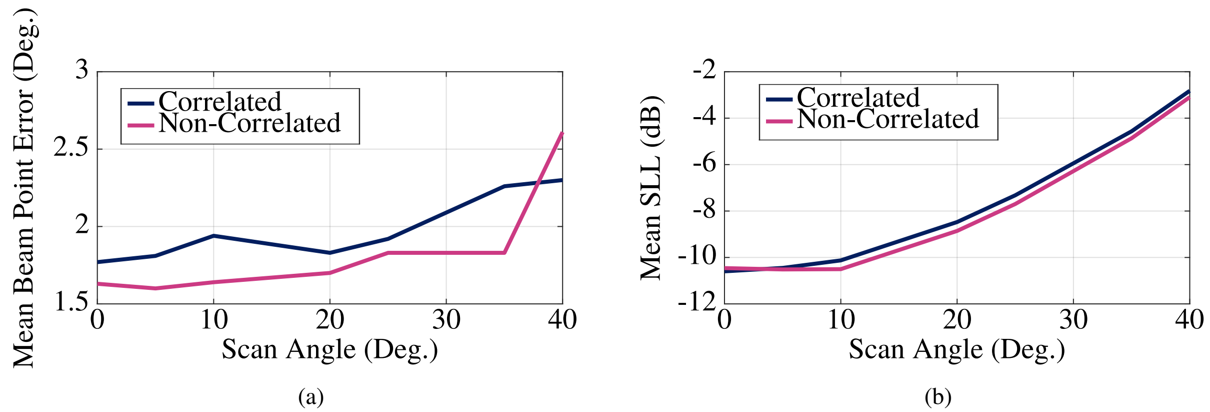


Figure 7.15: Comparison between non-correlated and correlated for beam pointing error and side lobe levels.

for the 4×1 linear array. The selection of the amplifier behind the antenna is uniformly distributed such that each amplifier is equally probable of being selected for the antenna element. The far-field simulation data for the antenna in Section 7.3, is also used in conjunction with on-wafer measurements.

Similar to Section 6.3.2, numerous iterative trials are ran such that the simulation reaches convergence in statistical far-field parameters. In Fig. 7.14(a), multiple antenna patterns are plotted for a scan angle of $\psi = 20°$ at 92.5 GHz. The mean patterns with 95% confidence intervals for both the correlated and non-correlated cases far-field patterns at $\psi = 0°$ are shown in Fig. 7.14(b).

In addition, simulations are ran over multiple scan angles for the 4×1 linear array. The scanned far-field simulation data is used for the statistical simulation. In Fig. 7.15, a comparison between correlated and non-correlated data for far-field parameters is shown over a scan angle of $\psi = 0° - 40°$. In Fig. 7.15(a), the mean beam pointing error is shown with approximately 1° difference between the two data sets. Figure 7.15(b) shows the mean side lobe levels between correlated and non-correlated cases.

7.5 Planar Phased Array for High ERP Applications

In this section the analysis is extended to planar phased arrays. Using the radiator element in Section 7.1 in planar configuration, an analysis is performed of the required array elements based on current state-of-the-art solid-state output power designed in GaN-on-SiC processes.

Figure 7.16 shows the contour plot for the ERP for number of array elements and element power at

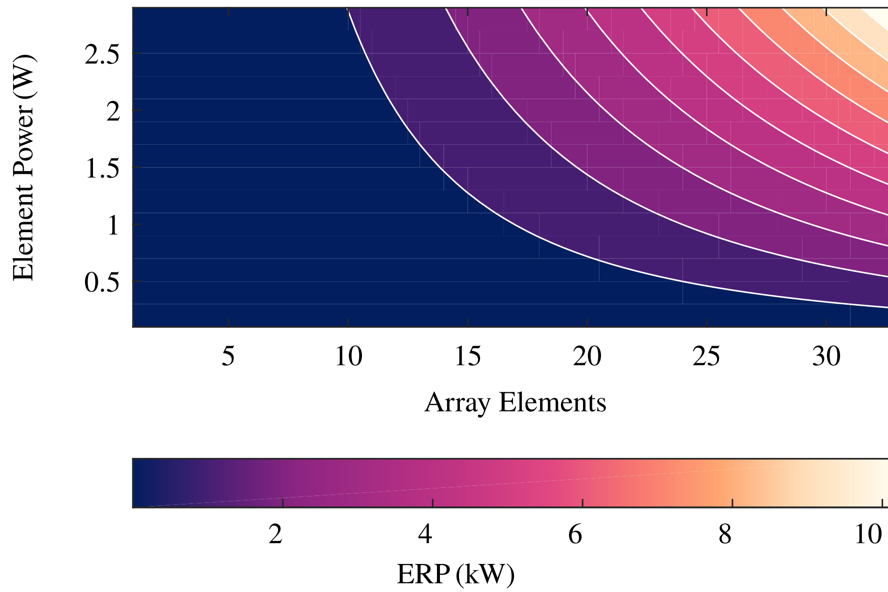


Figure 7.16: Contours for ERP given array element and element power the ERP is calculated at 92.5 GHz using 1 dB insertion loss for MMIC-to-waveguide transistions.

92.5 GHz given a 1 dB MMIC-to-waveguide loss and single element directivity of 7.66 dB. Corresponding DC power consumption of arrays given by an element amplifier with a gain of 12 dB and PAE of 10% and 20% are shown in Fig. 7.17 and Fig. 7.18, respectively.

The principal patterns for a design from each of Chapters 3 to 5 are shown in Fig. 7.19. The planar array is sized such that the it reaches kW-ERP. ERP is calculated at 92.5 GHz approximating a 1 dB loss for the MMIC-to-waveguide transition. The principal patterns are shown for a 5×4 planar array at 92.5 GHz using Qorvo GaN09 Γ-gate single-ended design in Section 3.1 operating at 0.979 W output power. For the Qorvo GaN09 T-gate serially combined design from Section 4.3, the patterns are shown for a 4×4 planar array at 92.5 GHz. HRL's single ended design from in Section 4.2 (c) uses a 5×5 planar array with the PA operating at 0.49 W output power.

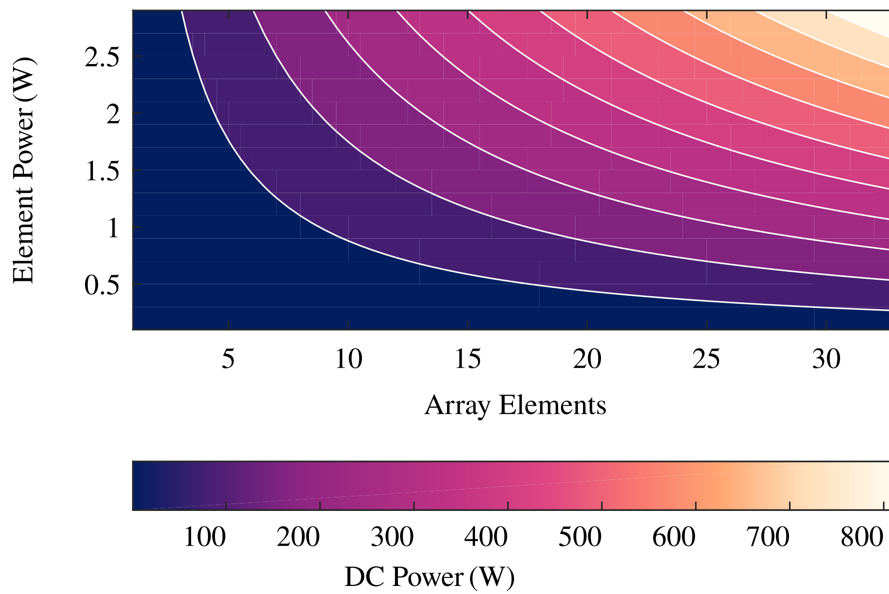


Figure 7.17: Contours for DC power given array element and element power. Calculation is based off of a 12 dB gain and 10% PAE amplifier.

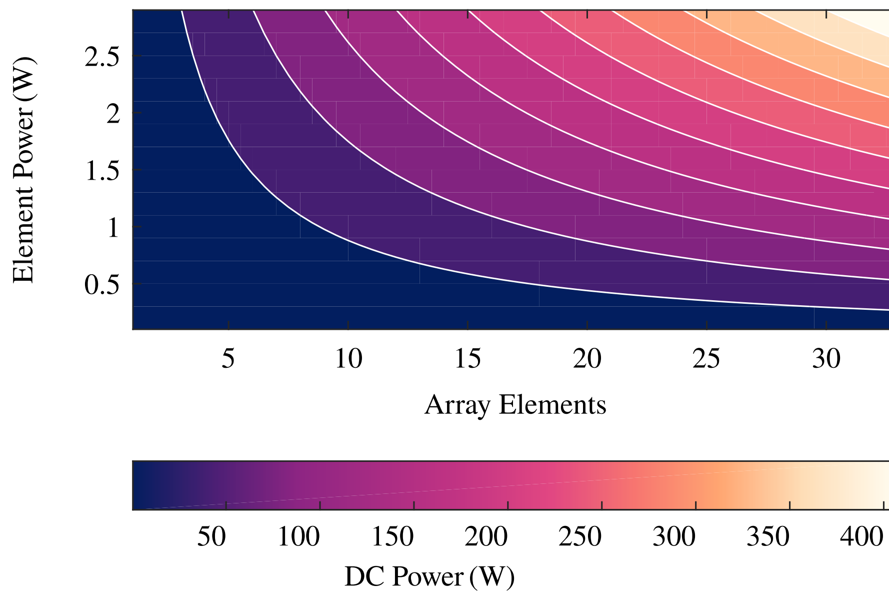
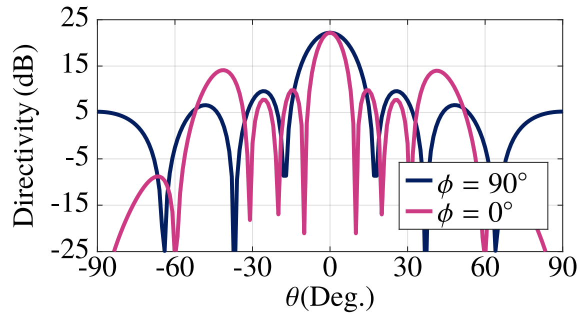
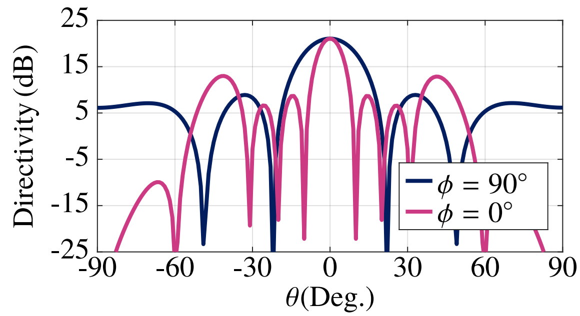


Figure 7.18: Contours for DC power given array element and element power. Calculation is based off of a 12 dB gain and 20% PAE amplifier.



(a)



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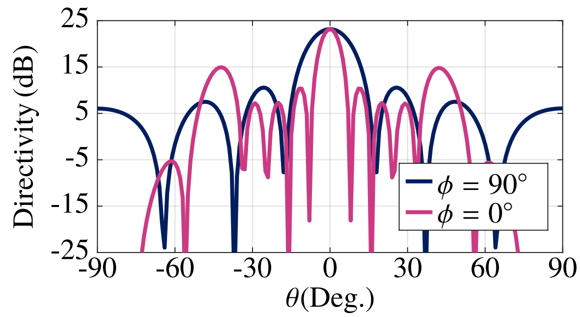

(c)

Figure 7.19: (a) Principal patterns for 5×4 planar array at 92.5 GHz. (b) Principal patterns for 4×4 planar array at 92.5 GHz. (c) Principal patterns for 5×5 planar array at 92.5 GHz.

7.6 Conclusion

In summary, this chapter focuses on the analysis of W-band arrays under statistical variations by using the design of a 4×1 linear array. Measurements of the designed 4×1 linear array module are presented at bore-sight and a scan angle of $\theta_o = 25°$. Statistical simulations are preformed using measured, on-wafer data and a 4×1 linear array to predict far-field patterns. In addition, an analysis for predicted results through simulation of the capability using state-of-the-art W-band amplifiers for high ERP applications is presented. The contributions of this chapter are summarized in [105].

Chapter 8

Conclusion and Future Work

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8.1 Summary

In summary, the focus of this thesis is the design and analysis of advanced millimeter-wave MMIC power amplifiers for high effective radiated power (ERP) aimed to fill the need of the increasingly important millimeter-wave applications above K_a-band in the military and commercial sector. Recent advances in GaN technology operating at millimeter-wave frequencies have brought forth W-band capable processes. The three different commercial GaN processes in development by Qorvo and HRL (Boeing/GM), are compared in terms of bandwidth, power, efficiency and gain of W-band power amplifiers: the Qorvo GaN09 90 nm V-band Γ-gate and W-band T-gate processes, and HRL's T3 40 nm process. Process metrics and performance based off of non-linear EEHEMT and Angelov transistor models for each process are presented and steady-state thermal analysis for each of the processes is summarized. Analysis of power combining efficiency and degradation in power combiners and phased arrays caused by GaN-on-SiC semiconductor process variations

is presented.

Specifically, the contributions of the research described in this thesis are as follows:

- In Chapter 3, two W-band power amplifier MMIC designs are presented in detail in single-ended and balanced configurations. Using Qorvo's GaN09 Γ-gate V-band process, high power is achieved up to 93 GHz and the shortcomings of using this technology above its designated operating frequency is presented. Simulation results predict 1 W and 2 W of output power from the single-ended and balanced amplifiers, respectively, with single digit efficiency. On-wafer measurements of the S-parameters match simulated performance trends with a reduction in gain due to processing issues which are currently being corrected by Qorvo. The results were communicated in [82, 105]. As of the writing of this thesis, we are expecting refabricated MMICs.

- In chapter 4, two W-band MMIC designs with improved bandwidth at the expense of output power are implemented in Qorvo's GaN09 T-gate process. The improvements in the designs compared to those of Chapter 3 include quasi-distributed elements that decrease MMIC footprint, and two power combined topologies (balanced and serial). An investigation of improved combining efficiencies through modeling of Lange couplers at millimeter-wave frequencies is presented. Additionally, stability analysis considerations under process variations is presented. The results from this chapter are presented in [105].

- In Chapter 5, the design of a full W-band MMIC power amplifier using HRL's T3 40 nm process will be presented. A unit power amplifier in balanced configuration predict the widest bandwidth and highest power using solid-state technology. This work supports DARPA's GaN maturation program which is viewed of critical importance to national security.

- In Chapter 6, an investigative look of power combining for on- and off-chip is discussed. The analysis of efficiencies distributed from the device level, on-chip reactive in-phase parallel combining, on-chip PA architecture, and off-chip corporate combining is shown. The results from this chapter are presented in [105].

- In Chapter 7, a system level analysis for W-band spatial power combining is presented with the goal in achieving kW ERP at W-band. The analysis of combining efficiencies from Chapter 6 is extended to spatial power combining of variations presented in Chapter 6. Results of a 4×1 linear waveguide horn array at W-band is presented with analysis for a planar array. The results from this chapter are presented in [105].

In addition to W-band solid-state transmitters, other relevant microwave and millimeter-wave components were investigated although they are not described in dissertation:

- Prior to the contributions in advanced W-band MMIC PA design, lower frequency 10 GHz GaN PAs for radar with increased spectral confinement were reported in [111].
- For microwave and millimeter-wave front-ends, isolation between transmitter is necessary. In addition to microstrip ferrite circulators design using commercially available ferrites with a new co-design approach, new types of integrated circulators in GaN MMIC processes are designed with self-biased iron-cobalt (FeCo) nano-wires. These are for the first time demonstrated at X-band frequencies. The results from this work are reported in [112–116].

8.2 Future Work

There are many areas of research where this work can be continued:

- First and foremost, additional large-signal measurements of the fabricated MMIC PAs presented in Chapters 3 to 5 are required. A thorough comparison of Qorvo millimeter-wave processes and HRL T3 process will further close the loop on the current state-of-the-art in W-band MMIC power amplifiers. In addition, the amplifiers presented in Chapter 5 considered the single-ended and balanced approach for the USSPA design. Further consideration for the USSPA design to be used in serial configuration to further boost is a consideration for the next MMIC fabrication run. An example of a ×3 serially combined layout is shown in Fig. 8.1.

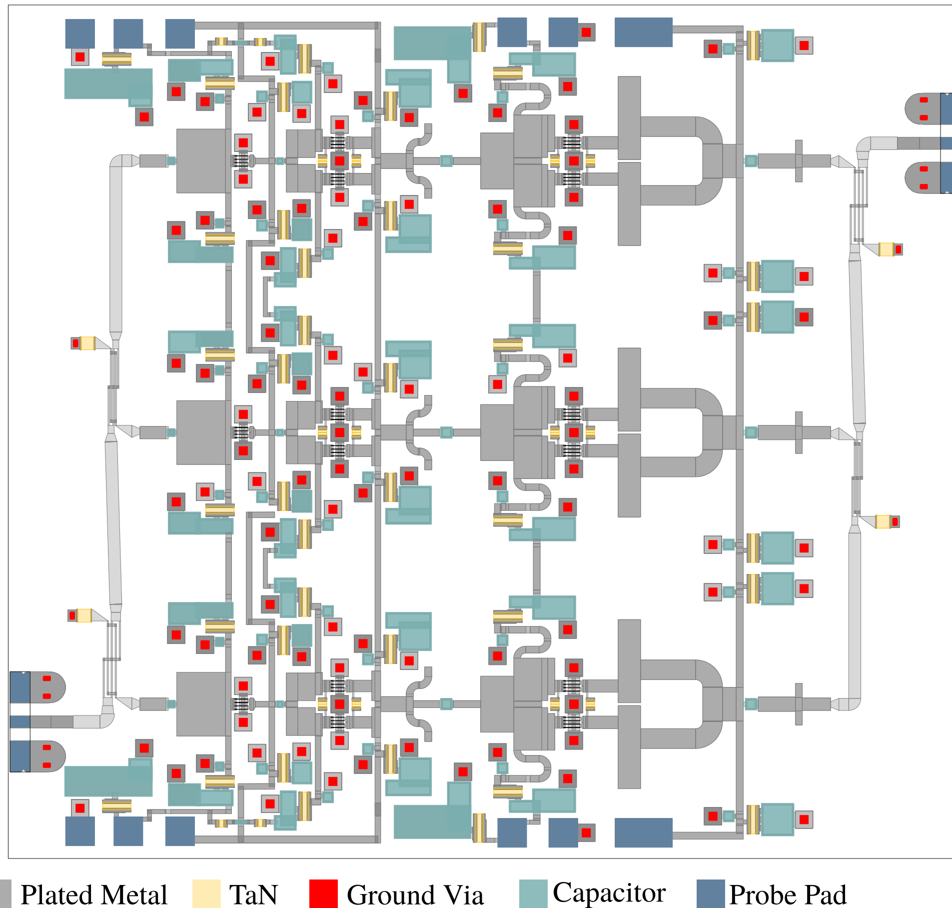


Figure 8.1: Example layout for a serially combined of the USSPA design from Chapter 5 using HRL T3's process.

- The next obvious step from a single MMIC PA is the develop the packaging associated with it. For space constrained applications, this includes addressing space limitations with a thermal solution for a phased array system. For a planar array, stringent space constraints are imposed for a stacked, linear array such as the one presented in Chapter 7.

- As designs from Chapters 3 to 5 continued to get refabricated, new spread of wafer data with more data and improved yield from GaN maturation and repeated analysis from Chapters 6 and 7 with hopeful improvements of both, power combining efficiency and far-field patter.

This thesis is primarily focused with the design of GaN technology PAs. The PA is only a single block in the transmitter front-end chain. The various other components of the transmitter such as oscillators,

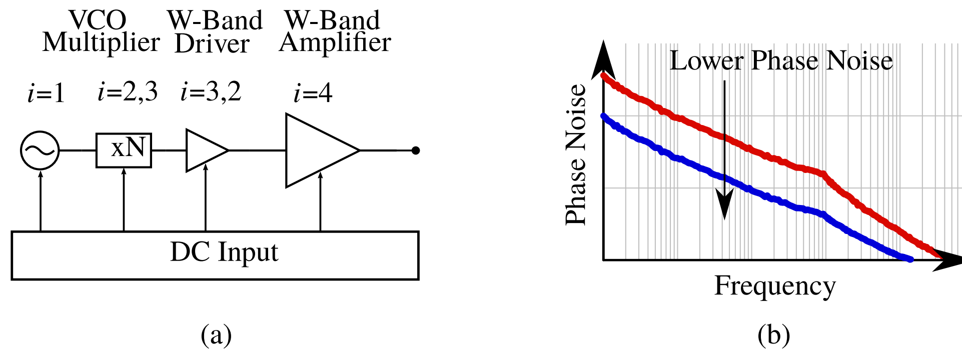


Figure 8.2: (a) A block diagram a multiplier high-source is shown. The diagram shows the various components needed for a high-power microwave variable microwave source. (b) Area for research includes which order of i to reduce phase noise in microwave sources.

multipliers, and mixers designed into millimeter-wave research processes are additional future works. For microwave sources requiring oscillators and multipliers, research in the MMIC design using state-of-the-art millimeter-wave process can be performed with research into the trade-offs. In Fig. 8.2, a block diagram for a multiplier high-source is shown. An investigation into several architectures in terms of (a) output power, (b) total conversion efficiency, (c) isolation, (d) phase noise and (e) wafer footprint, based on the order of the solid-state multiplier chain. The microwave power source MMICs would include voltage controlled oscillators (VCO) at W-band, as well as a VCO at a lower frequency with an active multiplier, with the multiplication factor determined by a trade-off study.

In addition to the multiplier, in order to investigate sub-harmonic LO isolation, a study of two configurations can be performed: multiplier followed by W-band PA, and lower-frequency driver followed by a multiplier, with equal output power levels sufficient to drive the final watt-level PAs. Alternatively, lower-frequency oscillators are followed with multipliers with the goal of higher chain efficiency.

One of the main objectives in the use of frequency multipliers at millimeter-wave frequencies is to separate the signal-generating from the amplification circuitry. This physical and electrical isolation reduces heating from the amplifier and improves stability. Although transistor frequency multipliers do not consume as much power as PAs, they are the primary cause of power dissipation in LO circuitry. In Fig. 8.3, the layout that is currently in fabrication with the HRL T3 process is shown. The multiplier topology uses a K/K_a-band class-C amplifier stage to generate harmonics and is cascaded with a class-AB W-band amplifier for further

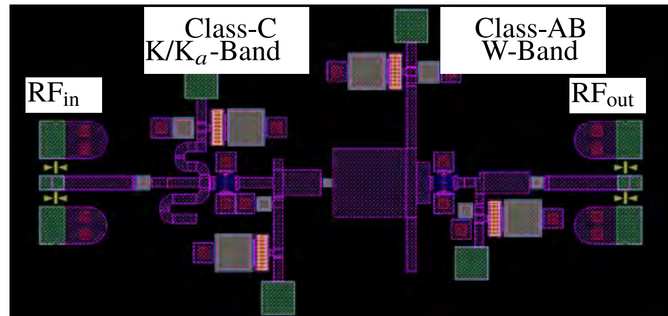
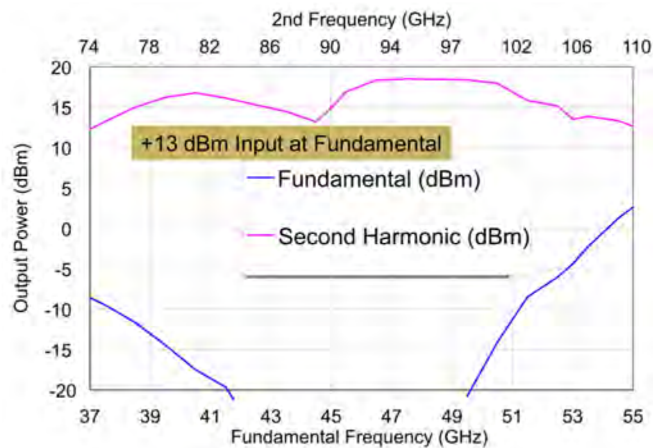
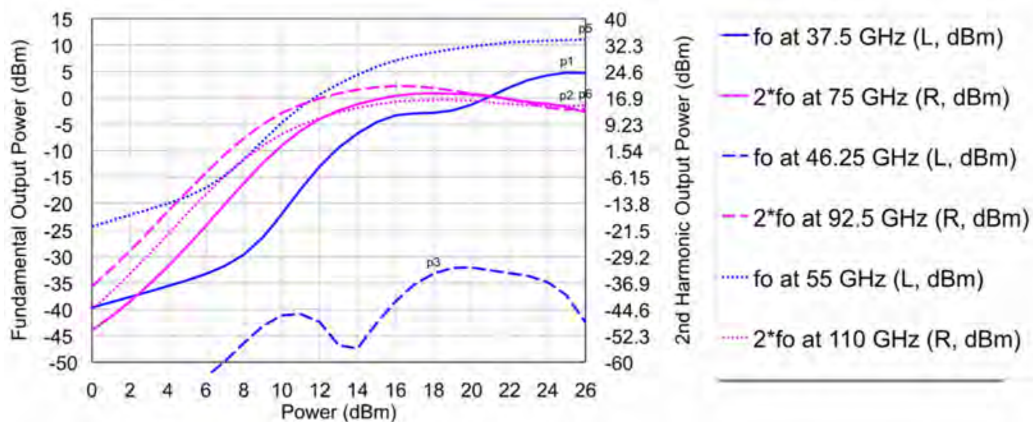


Figure 8.3: The layout of a multiplier currently in fabrication with the HRL T3 process. The multiplier topology uses a K/K$_a$-band class-C amplifier stage to generate harmonics and is cascaded with a class-AB W-band amplifier.

signal amplification. The simulated performance is shown in Fig. 8.4 showing greater than +10 dBm of output power across W-band, with a minimum of approximately 10 dB in fundamental frequency suppression.



(a)



(b)

Figure 8.4: (a) Frequency performance for the multiplier layout in Fig. 8.3 with +13 dBm fundamental input power. (b) Output power at the fundamental and second harmonic versus fundamental input power for the multiplier layout in Fig. 8.3.

Bibliography

[1] D. S. Green, C. L. Dohrman, J. Demmin, Y. Zheng, and T.-H. Chang, "A revolution on the horizon from darpa: Heterogeneous integration for revolutionary microwave\/millimeter-wave circuits at darpa: Progress and future directions," *IEEE Microwave Magazine*, vol. 18, no. 2, pp. 44–59, 2017. x, 3, 4

[2] M. A. Forman, "Active antenna arrays for power combining and communications," Ph.D. dissertation, University of Colorado at Boulder, 2001. xi, 2

[3] R. A. York and Z. Popović, "Quasi-optical power combining," in *Active and quasi-optical arrays for solid-state power combining*. Wiley, 1997, pp. 1–48. xi, 2, 96, 97

[4] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh *et al.*, "Scaling of gan hemts and schottky diodes for submillimeter-wave mmic applications," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 2982–2996, 2013. xii, 3, 10, 18, 19, 83

[5] C. F. Campbell, "MMIC Power Amplifier Design, What Mom Didn't Tell You," 2014. xv, 37, 41, 46

[6] J. M. Schellenberg, "A 2-w w-band GaN traveling-wave amplifier with 25-ghz bandwidth," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 9, pp. 2833–2840, 2015. xix, 6, 31, 56, 70, 72, 76, 81, 94

[7] S. Verploegh and Z. Popović, "V- and w-band two-way waveguide splitters fabricated by metal additive manufacturing," in *2018 Latin America Microwave Conference*. IEEE, 2018. xxi, 103, 104

[8] E. Cohen, “Mimic from the department of defense perspective,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 38, no. 9, pp. 1171–1174, 1990. 1

[9] E. D. Cohen, “The mimic program a retrospective,” *IEEE Microwave Magazine*, vol. 13, no. 4, pp. 77–88, 2012. 1

[10] K. Tan, R. Dia, D. C. Streit, T. Lin, T. Q. Trinh, A. Han, P. Liu, P.-M. Chow, and H. Yen, “94-ghz 0.1-mu m t-gate low-noise pseudomorphic ingaas hemts,” *IEEE electron device letters*, vol. 11, no. 12, pp. 585–587, 1990. 1

[11] T. Ton, B. Allen, H. Wang, G. Dow, E. Barnachea, and J. Berenz, “A w-band, high-gain, low-noise amplifier using phemt mmic,” *IEEE microwave and guided wave letters*, vol. 2, no. 2, pp. 63–64, 1992. 1

[12] L. Yujiri, H. H. Agravante, M. Biedenbender, G. S. Dow, M. R. Flannery, S. W. Fornaca, B. I. Hauss, R. L. Johnson, R. T. Kuroda, K. Jordan *et al.*, “Passive millimeter-wave camera,” in *Passive Millimeter-Wave Imaging Technology*, vol. 3064. International Society for Optics and Photonics, 1997, pp. 15–23. 1

[13] N. K. Das and H. L. Bertoni, *Directions for the next generation of MMIC devices and systems*. Springer Science & Business Media, 2013. 2

[14] J. Harvey, E. Brown, D. Rutledge, and R. York, “Spatial power combining for high-power transmitters,” *IEEE microwave magazine*, vol. 1, no. 4, pp. 48–59, 2000. 2

[15] J. J. Sowers, D. J. Pritchard, A. E. White, W. Kong, O. Tang, D. R. Tanner, and K. Jablinskey, “A 36 w, v-band, solid state source,” in *1999 IEEE MTT-S International Microwave Symposium Digest (Cat. No. 99CH36282)*, vol. 1. IEEE, 1999, pp. 235–238. 2

[16] S. Sun, T. S. Rappaport, M. Shafi, P. Tang, J. Zhang, and P. J. Smith, “Propagation models and performance evaluation for 5g millimeter-wave bands,” *IEEE Transactions on Vehicular Technology*, vol. 67, no. 9, pp. 8422–8439, 2018. 3

[17] P. M. Asbeck, N. Rostomyan, M. Özen, B. Rabet, and J. A. Jayamon, “Power amplifiers for mm-wave 5g applications: Technology comparisons and cmos-soi demonstration circuits,” *IEEE Transactions on Microwave Theory and Techniques*, 2019. 3

[18] K. Brown, A. Brown, T. Feenstra, D. Gritters, E. Ko, S. O’Connor, A. Pierce, A. Sanders, and M. Sotelo, “Ultra-compact high speed mmw transceiver using gan power amplifier technology,” in *2015 IEEE MTT-S International Microwave Symposium*. IEEE, 2015, pp. 1–3. 3, 105

[19] F. Boes, J. Antes, T. Messinger, D. Meier, R. Henneberger, A. Tessmann, and I. Kallfass, “Multi-gigabit e-band wireless data transmission,” in *2015 IEEE MTT-S International Microwave Symposium*. IEEE, 2015, pp. 1–4. 3

[20] X. Gu, A. Valdes-Garcia, A. Natarajan, B. Sadhu, D. Liu, and S. K. Reynolds, “W-band scalable phased arrays for imaging and communications,” *IEEE communications magazine*, vol. 53, no. 4, pp. 196–204, 2015. 3

[21] R. A. Alhalabi and G. M. Rebeiz, “A 77-81-ghz 16-element phased-array receiver with±50Âř beam scanning for advanced automotive radars [j],” *IEEE Transaction on Microwave Theory and Techniques*, vol. 62, no. 11, pp. 2823–2832, 2014. 3

[22] P. Schmalenberg, J. S. Lee, and K. Shiozaki, “A sige-based 16-channel phased array radar system at w-band for automotive applications,” in *2013 European Microwave Conference*. IEEE, 2013, pp. 1611–1614. 3

[23] D. Bleh, M. Rösch, M. Kuri, A. Dyck, A. Tessmann, A. Leuther, S. Wagner, and O. Ambacher, “A 100 ghz fmcw mimo radar system for 3d image reconstruction,” in *2016 European Radar Conference (EuRAD)*. IEEE, 2016, pp. 37–40. 3

[24] A. Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, D. Brown, A. Corrion, H. Moyer, S. Burnham, D. Regan, R. Grabar *et al.*, “Gan technology for e, w and g-band applications,” in *2014 IEEE compound semiconductor integrated circuit symposium (CSICS)*. IEEE, 2014, pp. 1–4. 3, 4, 9, 10, 18, 83

[25] M. Micovic, D. Brown, D. Regan, J. Wong, J. Tai, A. Kurdoghlian, F. Herrault, Y. Tang, S. D. Burnham, H. Fung *et al.*, “Ka-band lna mmic’s realized in fmax> 580 ghz gan hemt technology,” in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2016, pp. 1–4. 3

[26] R. Lai, X. Mei, W. Deal, W. Yoshida, Y. Kim, P. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange *et al.*, “Sub 50 nm inp hemt device with fmax greater than 1 thz,” in *2007 IEEE International Electron Devices Meeting*. IEEE, 2007, pp. 609–611. 3

[27] K. M. Leong, X. Mei, W. Yoshida, P.-H. Liu, Z. Zhou, M. Lange, L.-S. Lee, J. G. Padilla, A. Zamora, B. S. Gorospe *et al.*, “A 0.85 thz low noise amplifier using inp hemt transistors,” *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 6, pp. 397–399, 2015. 3

[28] W. Deal, X. Mei, K. M. Leong, V. Radisic, S. Sarkozy, and R. Lai, “Thz monolithic integrated circuits using inp high electron mobility transistors,” *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 25–32, 2011. 3

[29] B. G. Danly, M. Blank, J. Calame, B. Levush, K. T. Nguyen, D. E. Pershing, R. Parker, K. L. Felch, B. James, P. Borchard *et al.*, “Development and testing of a high-average power, 94-ghz gyroklystron,” *IEEE transactions on plasma science*, vol. 28, no. 3, pp. 713–726, 2000. 4

[30] K. Felch, M. Blank, P. Borchard, P. Cahalan, S. Cauffman, H. Jory, Y. Gorelov, and J. Lohr, “Operating experience on six 110 ghz, 1 mw gyrotrons for ech applications,” *Nuclear Fusion*, vol. 48, no. 5, p. 054008, 2008. 4

[31] S. Chen, L. Witkowski, and X. Gu, “Important recent advancement of gan technology and mmics for w-band applications,” *ECS Transactions*, vol. 80, no. 10, pp. 945–952, 2017. 4, 6, 11, 31, 56, 58, 81

[32] N. J. Kolias, “Recent advances in GaN mmic technology,” in *2015 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE, 2015, pp. 1–5. 4

[33] B. Romanczyk, S. Wienecke, M. Guidry, H. Li, E. Ahmadi, X. Zheng, S. Keller, and U. K. Mishra, "Demonstration of constant 8 w/mm power density at 10, 30, and 94 ghz in state-of-the-art millimeter-wave n-polar gan mishemts," *IEEE Transactions on Electron Devices*, vol. 65, no. 1, pp. 45–50, 2018. 4

[34] Y. Niida, Y. Kamada, T. Ohki, S. Ozaki, K. Makiyama, Y. Minoura, N. Okamoto, M. Sato, K. Joshin, and K. Watanabe, "3.6 w/mm high power density w-band inalgan/gan hemt mmic power amplifier," in *2016 IEEE Topical Conference on Power Amplifiers for Wireless and Radio Applications (PAWR)*. IEEE, 2016, pp. 24–26. 4

[35] A. Kurdoghlian, H. Moyer, H. Sharifi, D. F. Brown, R. Nagele, J. Tai, R. Bowen, M. Wetzel, R. Grabar, D. Santos *et al.*, "First demonstration of broadband w-band and d-band gan mmics for next generation communication systems," in *2017 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2017, pp. 1126–1128. 4

[36] B. Kim, T. Phan, and J. Schellenberg, "4w, w-band gan solid-state power amplifier," in *Gov. Microw. Appl. Crit. Technol. Conf.*, 2013. 4, 6

[37] A. Fung, L. Samoska, P. Kangaslahti, R. Lin, I. Mehdi, G. Sadowy, S. Tanelli, D. Esteban-Fernandez, A. Peralta, M. Soria, A. Brown, D. Gritters, S. O'Connor, and S. Lardizabal, "Gallium nitride amplifiers beyond w-band," in *2018 IEEE Radio and Wireless Symposium (RWS)*, Jan 2018, pp. 150–153. 4

[38] A. Brown, K. Brown, J. Chen, K. Hwang, N. Kolias, and R. Scott, "W-band gan power amplifier MMICs," in *2011 IEEE MTT-S International Microwave Symposium*. IEEE, 2011, pp. 1–4. 4, 6, 31, 56, 57, 81, 82, 95

[39] P. Harati, A. Tessmann, D. Schwantuschke, R. Henneberger, and I. Kallfass, "E-band transmitter with 29 dbm rf power for satellite communication," in *2016 46th European Microwave Conference (EuMC)*. IEEE, 2016, pp. 509–511. 4

[40] J. Schellenberg, B. Kim, and T. Phan, "W-band, broadband 2w gan mmic," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*. IEEE, 2013, pp. 1–4. 4

[41] K. Brown, A. Brown, T. Feenstra, D. Gritters, S. O'Connor, M. Sotelo, N. Kolias, K. Hwang, J. Kotce, and E. Robinson, "7kw gan w-band transmitter," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*. IEEE, 2016, pp. 1–3. 4

[42] K. Datta and H. Hashemi, "High-breakdown, high-f_{max} multiport stacked-transistor topologies for the w-band power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1305–1319, 2017. 5

[43] V. Radisic, C. Monier, K. Loi, and A. Gutierrez-Aitken, "W-band inp hbt power amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 9, pp. 824–826, 2017. 5

[44] S. Wienecke, B. Romanczyk, M. Guidry, H. Li, E. Ahmadi, K. Hestroffer, X. Zheng, S. Keller, and U. K. Mishra, "N-polar gan cap mishemt with record power density exceeding 6.5 w/mm at 94 ghz," *IEEE Electron Device Letters*, vol. 38, no. 3, pp. 359–362, 2017. 5

[45] M. Micovic, A. Kurdoghlian, A. Margomenos, D. Brown, K. Shinohara, S. Burnham, I. Milosavljevic, R. Bowen, A. Williams, P. Hashimoto *et al.*, "92–96 ghz gan power amplifiers," in *2012 IEEE/MTT-S International Microwave Symposium Digest*. IEEE, 2012, pp. 1–3. 5, 6, 57, 82, 84, 95

[46] D. Schwantuschke, B. Aja, M. Seelmann-Eggebert, R. Quay, A. Leuther, P. Brückner, M. Schlechtweg, M. Mikulla, I. Kallfass, and O. Ambacher, "Q-and e-band amplifier mmics for satellite communication," in *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*. IEEE, 2014, pp. 1–4. 6, 57, 82, 95

[47] M. Micovic, A. Kurdoghlian, K. Shinohara, S. Burnham, I. Milosavljevic, M. Hu, A. Corrion, A. Fung, R. Lin, L. Samoska *et al.*, "W-band gan mmic with 842 mw output power at 88 ghz," in *2010 IEEE MTT-S International Microwave Symposium*. IEEE, 2010, pp. 237–239. 6, 57, 82, 84, 95

[48] E. Ture, D. Schwantuschke, A. Tessmann, S. Wagner, P. Bruckner, M. Mikulla, R. Quay, and O. Ambacher, “High-gain algan/gan hemt single chip e-band power amplifier mmic with 30 dbm output power,” in *2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2015, pp. 1–4. 6

[49] W. Shaobing, G. Fangjin, G. Jianfeng, W. Weibo, L. Zhonghui, H. Nianning, and C. Tangsheng, “W-band algan/gan mmic pa with 3.1 w output power,” in *2017 14th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China (SSLChina: IFWS)*. IEEE, 2017, pp. 219–223. 6

[50] “BAL–WPA,” https://mmics.hrl.com/capabilities/mmics/GaNPA/pdf/BalancedPADataSheet.pdf, accessed: 2019-02-28. 6, 56, 81

[51] DARPA. (2019) DARPA nitride electronic next-generation technology. [Online]. Available: https://www.darpa.mil/program/nitride-electronic-next-generation-technology 9

[52] P. Saunier, “Gan for next generation electronics,” in *2014 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2014, pp. 1–4. 9, 10

[53] M. Golio, *RF and microwave semiconductor device handbook*. CRC press, 2002. 10

[54] T. Egawa, G.-Y. Zhao, H. Ishikawa, H. Umeno, and T. Jimbo, “Characterizations of recessed gate algan/gan hemts on sapphire,” *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 603–608, 2001. 10

[55] G. P. Gibiino, C. Florian, A. Santarelli, T. Cappello, and Z. Popović, “Isotrap pulsed iv characterization of gan hemts for pa design,” *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 8, pp. 672–674, 2018. 11

[56] Agilent Technologies. (2008) Ic-cap nonlinear device models, vol. 2. [Online]. Available: http://literature.cdn.keysight.com/litweb/pdf/iccap2008addon1/pdf/icmdlhf.pdf 11

[57] N. Angelov, H. Zirath, and A. Rorsman, "Validation of a nonlinear transistor model by power spectrum characteristics of hemt's and mesfet's," *IEEE transactions on microwave theory and techniques*, vol. 43, no. 5, pp. 1046–1052, 1995. 11

[58] S. Chen, L. Witkowski, and X. Gu, "Critical recent advancement of gan technology and mmics for millimeter-wave applications," in *Meeting Abstracts*, no. 29. The Electrochemical Society, 2017, pp. 1227–1227. 11, 31

[59] National Instrument. (2019) AWR microwave office. [Online]. Available: https://www.awrcorp.com/products/ni-awr-design-environment/microwave-office-software 13, 101

[60] K. Shinohara, A. Corrion, D. Regan, I. Milosavljevic, D. Brown, S. Burnham, P. Willadsen, C. Butler, A. Schmitz, D. Wheeler *et al.*, "220ghz f t and 400ghz f max in 40-nm gan dh-hemts with re-grown ohmic," in *2010 International Electron Devices Meeting*. IEEE, 2010, pp. 30–1. 18, 83

[61] M. Micovic, D. Brown, D. Regan, J. Wong, Y. Tang, F. Herrault, D. Santos, S. Burnham, J. Tai, E. Prophet *et al.*, "High frequency gan hemts for rf mmic applications," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016, pp. 3–3. 18, 83

[62] S. D. Burnham, R. Bowen, J. Tai, D. Brown, R. Grabar, D. Santos, J. Magadia, I. Khalaf, and M. Micovic, "Reliability characteristics and mechanisms of hrls t3 gan technology," *IEEE Transactions on Semiconductor Manufacturing*, vol. 30, no. 4, pp. 480–485, 2017. 18, 83

[63] J. L. Walker, *Handbook of RF and microwave power amplifiers*. Cambridge University Press, 2011. 20

[64] ANSYS. (2019) ANSYS structures. [Online]. Available: https://www.ansys.com/products/structures 20

[65] A. M. Darwish, A. J. Bayba, and H. A. Hung, "Thermal resistance calculation of algan-gan devices," *IEEE transactions on microwave theory and techniques*, vol. 52, no. 11, pp. 2611–2620, 2004. 20, 23

[66] ——, “Accurate determination of thermal resistance of fets,” *IEEE transactions on microwave theory and techniques*, vol. 53, no. 1, pp. 306–313, 2005. 20

[67] H. F. Cooke, “Precise technique finds fet thermal resistance,” *Microwaves*, vol. 25, pp. 85–87, 1986. 20

[68] S. Chen, private communication, Aug. 2017. 32

[69] K. W. Brown and A. K. Brown, “Millimeter-wave monolithic integrated circuit amplifier with opposite direction signal paths and method for amplifying millimeter-wave signals,” Jun. 28 2011, uS Patent 7,969,245. 37

[70] A. Weisshaar and V. K. Tripathi, “Perturbation analysis and modeling of curved microstrip bends,” *IEEE Transactions on Microwave theory and techniques*, vol. 38, no. 10, pp. 1449–1454, 1990. 37

[71] M. Roberg and C. Campbell, “A novel even & odd-mode symmetric circuit decomposition method,” in *2013 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*. IEEE, 2013, pp. 1–4. 39, 99

[72] W. Struble and A. Platzker, “A rigorous yet simple method for determining stability of linear n-port networks [and mmic application],” in *15th Annual GaAs IC Symposium*. IEEE, 1993, pp. 251–254. 41

[73] A. Platzker, W. Struble, and K. T. Hetzler, “Instabilities diagnosis and the role of k in microwave circuits,” in *1993 IEEE MTT-S International Microwave Symposium Digest*. IEEE, 1993, pp. 1185–1188. 41

[74] A. Platzker and W. Struble, “Rigorous determination of the stability of linear n-node circuits from network determinants and the appropriate role of the stability factor k of their reduced two-ports,” in *Third International Workshop on Integrated Nonlinear Microwave and Millimeterwave Circuits*. IEEE, 1994, pp. 93–107. 41

[75] K. Wang, M. Jones, and S. Nelson, “The s-probe-a new, cost-effective, 4-gamma method for evaluating multi-stage amplifier stability,” in *1992 IEEE MTT-S Microwave Symposium Digest*. IEEE, 1992, pp. 829–832. 41, 42

[76] L. Samoska, K.-Y. Lin, H. Wang, Y.-H. Chung, M. Aust, S. Weinreb, and D. Dawson, “On the stability of millimeter-wave power amplifiers,” in *2002 IEEE MTT-S International Microwave Symposium Digest (Cat. No. 02CH37278)*, vol. 1. IEEE, 2002, pp. 429–432. 41

[77] A. Suarez, “Check the stability: Stability analysis methods for microwave circuits,” *IEEE Microwave Magazine*, vol. 16, no. 5, pp. 69–90, 2015. 41

[78] C. Campbell, *Microwave Monolithic Power Amplifier Design*. John Wiley and Sons, Inc., 2013. [Online]. Available: http://dx.doi.org/10.1002/047134608X.W8180 41, 42

[79] G. Gonzalez, *Microwave transistor amplifiers: analysis and design*. Prentice hall New Jersey, 1997, vol. 2. 42

[80] P. R. Gray, *Analysis and design of analog integrated circuits*. John Wiley & Sons, 2009. 42

[81] C. Campbell and S. Brown, “Modified s-probe circuit element for stability analysis,” *White Paper from AWR*, 1994. 42

[82] M. Pinto, S. Manafi, G. Lasser, M. Al-Tarifi, D. Filipović, and Z. Popović, “W-band gan watt-level mmic pas,” in *2018 GOMACTech-18 Digest*, March 2018. 56, 128

[83] J. Schellenberg, “The evolution of power combining techniques: From the 60s to today,” in *2015 IEEE MTT-S International Microwave Symposium*, May 2015, pp. 1–4. 57, 82, 95

[84] M. Knox, R. Youmans, M. Kumar, L. Forker, H. Voigt, P. Brand, F. Marcotte, and A. Hughes, “400 w x-band gaas mmic cw amplifier,” in *Proceedings of 1995 IEEE MTT-S International Microwave Symposium*. IEEE, 1995, pp. 1605–1608. 70

[85] M. Pinto, S. Verploegh, T. Sonnenberg, and Z. Popović, “W-band gan mmic power amplifiers,” (Manuscript in Preparation). 81, 93

[86] D. B. Rutledge, N.-S. Cheng, R. A. York, R. M. Weikle, and M. P. De Lisio, "Failures in power-combining arrays," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 7, pp. 1077–1082, 1999. 98

[87] R. B. Marks and D. F. Williams, "A general waveguide circuit theory," *Journal of research of the National Institute of Standards and Technology*, vol. 97, no. 5, p. 533, 1992. 99

[88] K. Kurokawa, "Power waves and the scattering matrix," *IEEE transactions on microwave theory and techniques*, vol. 13, no. 2, pp. 194–202, 1965. 99

[89] M. Rafie, *Network scattering parameters*. World Scientific, 1996, vol. 2. 99

[90] S. R. Schafer, "Carrier and envelope frequency measurements for supply-modulated microwave power amplifiers," Ph.D. dissertation, University of Colorado at Boulder, 2016. 99

[91] J. Y. Hasani, "Three-port model of a modern mos transistor in millimeter wave band, considering distributed effects," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 9, pp. 1509–1518, 2016. 100

[92] B. Hassan, A. Cutivet, M. Bouchilaoun, C. Rodriguez, A. Soltani, F. Boone, and H. Maher, "Large periphery gan hemts modeling using distributed gate resistance," *physica status solidi (a)*, vol. 216, no. 1, p. 1800505, 2019. 100

[93] B. Razavi, R.-H. Yan, and K. F. Lee, "Impact of distributed gate resistance on the performance of mos devices," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 11, pp. 750–754, 1994. 100

[94] E. Abou-Allam and T. Manku, "A small-signal mosfet model for radio frequency ic applications," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 5, pp. 437–447, 1997. 100

[95] S. Verploegh, M. Coffey, E. Grossman, and Z. Popović, “Properties of 50–110-ghz waveguide components fabricated by metal additive manufacturing,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 12, pp. 5144–5153, 2017. 103

[96] B. Zhang and H. Zirath, “Metallic 3-d printed rectangular waveguides for millimeter-wave applications,” *IEEE Transactions on Components, Packaging and Manufacturing Technology*, vol. 6, no. 5, pp. 796–804, 2016. 103

[97] N. Kaneda, Y. Qian, and T. Itoh, “A broad-band microstrip-to-waveguide transition using quasi-yagi antenna,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 12, pp. 2562–2567, Dec 1999. 103

[98] W. T. Khan, A. L. V. LÃşpez, A. . Ulusoy, and J. Papapolymerou, “Packaging a *w* -band integrated module with an optimized flip-chip interconnect on an organic substrate,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 1, pp. 64–72, Jan 2014. 105

[99] S. Weinreb, T. Gaier, M. Barsky, Y. C. Leong, and L. Samoska, “High-gain 150-215-ghz mmic amplifier with integral waveguide transitions,” *IEEE Microwave and Guided Wave Letters*, vol. 9, no. 7, pp. 282–284, July 1999. 105

[100] K. M. Leong, W. R. Deal, V. Radisic, X. B. Mei, J. Uyeda, L. Samoska, A. Fung, T. Gaier, and R. Lai, “A 340–380 ghz integrated cb-cpw-to-waveguide transition for sub millimeter-wave mmic packaging,” *IEEE microwave and wireless components letters*, vol. 19, no. 6, pp. 413–415, 2009. 105

[101] L. Samoska, W. R. Deal, G. Chattopadhyay, D. Pukala, A. Fung, T. Gaier, M. Soria, V. Radisic, X. Mei, and R. Lai, “A submillimeter-wave hemt amplifier module with integrated waveguide transitions operating above 300 ghz,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 6, pp. 1380–1388, 2008. 105

[102] V. Hurm, A. Tessmann, H. Massler, A. Leuther, M. Riessle, M. Zink, M. Schlechtweg, and O. Ambacher, “Gaas microstrip-to-waveguide transition operating in the wr-1.5 waveguide band (500âĂŞ750 ghz),” in *2012 Asia Pacific Microwave Conference Proceedings*, Dec 2012, pp. 145–147. 105

[103] D. M. Gritters, K. W. Brown, A. K. Brown, M. A. Moore, P. J. Kocurek, and T. A. Hanft, "High frequency, high bandwidth, low loss microstrip to waveguide transition," Oct. 8 2013, uS Patent 8,552,813. 105

[104] S. Ross, *Simulation*, ser. Knovel Library. Elsevier Science, 2012. 108

[105] M. Pinto, S. Verploegh, G. Lasser, and Z. Popović, "Analysis of w-band gan power combined transmit arrays," (Manuscript in Preparation). 110, 126, 128, 129

[106] J. Howard, "Statistical patterns of a general array," *IEEE Transactions on Antennas and Propagation*, vol. 15, no. 1, pp. 60–65, Jan 1967. 111

[107] J. Ruze, "Antenna tolerance theory - a review," *Proceedings of the IEEE*, vol. 54, no. 4, pp. 633–640, April 1966. 111

[108] ANSYS. (2019) ANSYS high frequency structure simulator (hfss). [Online]. Available: https://www.ansys.com/products/electronics/ansys-hfss 114

[109] D. F. Kelley and W. L. Stutzman, "Array antenna pattern modeling methods that include mutual coupling effects," *IEEE Transactions on Antennas and Propagation*, vol. 41, no. 12, pp. 1625–1632, Dec 1993. 114

[110] A. K. Bhattacharyya, *Phased array antennas: Floquet analysis, synthesis, BFNs and active array systems*. John Wiley & Sons, 2006, vol. 179. 116

[111] A. Zai, M. Pinto, M. Coffey, and Z. Popović, "Supply-modulated radar transmitters with amplitude-modulated pulses," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 9, pp. 2953–2964, Sep. 2015. 129

[112] M. Pinto, L. Marzall, A. Ashley, D. Psychogiou, and Z. Popović, "Design-oriented modelling of microstrip ferrite circulators," in *2018 48th European Microwave Conference (EuMC)*, Sep. 2018, pp. 215–218. 129

[113] L. F. Marzall, M. Pinto, A. Ashley, D. Psychogiou, and Z. Popović, "Co-simulations of dc magnetic bias fields and rf performance for microwave ferrite circulators," in *2018 International Applied Computational Electromagnetics Society Symposium (ACES)*, March 2018, pp. 1–2. 129

[114] A. Ashley, L. F. Marzall, M. Pinto, Z. Popović, and D. Psychogiou, "Bandwidth design of ferrite-based circulators," in *2018 International Applied Computational Electromagnetics Society Symposium (ACES)*, March 2018, pp. 1–2. 129

[115] M. Pinto, L. F. Marzall, A. Ashley, D. Psychogiou, and Z. Popović, "A design approach for monolithically integrated broadband circulators," in *2018 International Applied Computational Electromagnetics Society Symposium (ACES)*, March 2018, pp. 1–2. 129

[116] L. Marzall, Y. Zhang, M. Pinto, A. Ashley, K. Gao, J. Hryn, D. Psychogiou, and Z. Popović, "Analysis of self-biased nano-composite microstrip circulators," in *2019 GOMACTech-19 Digest*, March 2019. 129