ROBUST DESIGN METHODOLOGY FOR

CLASS-E AMPLIFIERS FOR MICROWAVE

APPLICATIONS

by

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Robust Design Methodology for Class-E Amplifiers for Microwave

  Applications

Thesis directed by Prof. Zoya Popović

This thesis covers techniques for robust analysis, design, fabrication and characterization of ultra-high efficiency microwave switched-mode power amplifiers (PAs) in the range of 8–12 GHz, using different active device technologies and with efficiency in the 70% range with output power (P_{OUT}) 0.5–1 dB below the maximal power available from the device (P_{MAX}). Applications include spatial power combining, power control and linearization, tunable and reconfigurable PAs and multistage PA configurations. Three main methodologies for the PA design were explored: (1) a low–frequency class–E theory approach with linear model parameter extraction; (2) nonlinear simulations; and (3) the load-pull technique.

Using different paths of the established design methodology, a number of reliable X–band class–E PAs are designed and characterized. A class–E PA is applied as an element in a spatial combiner in order to solve the heat generation problem. A broadband radiating element and a uniform feeding/biasing network allow for an ultra–high amplification and power combining efficiency of an antenna array. This array represents a unique solution for efficient power combining in X–band frequency range.

Nonlinear active device modeling issues are also addressed and a comparison between simulation and measurement is performed. It is shown that existing nonlinear device models do not accurately predict switched–mode or ultra-linear PA behavior and cannot be used for dependable design. Therefore a load-pull based methodology is applied to high–power ultra linear amplifier design in commercial wireless communications. The same methodology is used for the development of highly efficient power amplifiers in the microwave range.

In order to improve the gain of a switched–mode microwave power amplifier, a two–stage amplifier is designed, fabricated, optimized and characterized, showing significant improvement in gain with minimal decrease in overall efficiency.

The most important component in a switched–mode PA is the active device itself, and its performance has the greatest impact on final PA characteristics. Three main active device technologies are compared for their suitability for switched mode microwave amplifier design. Using the methods presented in the previous chapters, several amplifiers were designed, fabricated and characterized. Results are organized in terms of relevant parameters and the benefits that each transistor family offers are studied.

The next topic focuses on the design of a tunable switched–mode microwave power amplifier, where a discrete MEMS tuner is integrated with a harmonically terminated active device. This cheap integrated load–pull system is used for power amplifier performance optimization, and serves as

a ground for reconfigurable amplifier design.

Future work is suggested for each of the topics along with a proposal for new work on an interstage matching tuner and application of large signal network analysis for microwave active device nonlinear characterization.

Dedication

To my family, friends in both countries, and a squirrel lost in the forest.

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Chapter 1

Introduction and Background

1.1 Introduction

The interest in highly–efficient switched–mode PAs for microwave applications has significantly increased after the work done by Thomas Mader et al. [1], mainly for class–E operating PAs. The class–E mode of PA operation is one of the variations of switched mode. Operating between cut–off and deep saturation, an active device at its output is forced to behave as a switch. Output voltage and current are shaped by a specially design output matching network, resulting in no dissipative and switching loss. This work established a connection between the classical approach of utilizing high–Q lumped element resonant circuitry for the class–E optimal matching and its equivalent distributed circuit using transmission lines. This opened the road for a major breakthrough in highly efficient class–E PAs, pushing the oper-

ation into the microwave ($\geq 2\,\mathrm{GHz}$) frequency range. At the same time, the rapidly growing wireless telecommunication industry imposed strong energy conservation requirements on transmitter front–ends, in order to extend the battery life of new–generation mobile hand sets, as well as to reduce the large power consumption in very dense networks of base stations. The systematic approach to the class–E microwave power amplifier (MPA) design and establishing a straightforward design procedure that reduces the development time is of great importance.

1.2 Thesis Organization

This thesis is divided into eight chapters, each demonstrating a different approach to high efficiency microwave power amplifier design. Encountered problems are highlighted and possible solutions are proposed. Most of the approaches are supported by a design example and a rigorous characterization of the amplifier. The Chapters are:

- Section 1.3 briefly reviews properties of the class–E mode, gives basic design equations and goes deeper in the discussion of microwave applications of class–E amplifiers.

- Chapter 1 presents realizations of class–E microwave PAs. The main nonidealities encountered during the microwave class–E on PA design are surveyed in this chapter. Encountered problems and their effects

PA characteristics are presented with possible solutions, some of which have been addressed in the literature for low–frequency class–E PAs. After an overview, a set of design methodologies developed and used throughout the rest of the thesis is presented. Available design tools are briefly addressed, as well as the current state of active–device nonlinear models.

- The topic of Chapter 3 is a spatial combiner of switched mode PAs. This chapter demonstrates an application of X–band class–E microwave PA designed using the analytical approach to solve the heat removal problem present in high–power active antenna arrays and quasi–optical combiners. Problems related to the connection between a highly efficient microwave PA and an antenna element (sensitivity to first–order parameter variations) are addressed. The resulting uniform 16–element active antenna array design, fabrication and characterization is detailed.

- Chapter 4 details the load–pull based design methodology. The load–pull technique is commonly used when no good nonlinear model is available for the design of a PA. A systematic procedure for active device characterization is developed, and augmented with a pretuning strategy. The goal is to eliminate extensive post–production tuning of the fabricated PAs. Two PAs are designed and characterized using this methodology: a high–power 2 GHz W–CDMA base–station PA and a

10–GHz 110–mW class–E PA.

- In Chapter 5 a two–stage class–E PA is presented. In order to achieve switch–acting of a microwave transistor an amplifier must operate with several dBs of gain compression. Available microwave active device gain is a precious resource and is often traded–off with efficiency. This chapter examines trade-offs between gain and efficiency in switched mode PAs. As a possible solution to gain improvement, directly coupled two–stage PAs are designed and characterized, in both hybrid and MMIC technology, using two different device technologies.

- Chapter 6 compares MESFET, HBT and HEMT hybrid class–E amplifiers. Three main technologies of active microwave devices are compared: Gallium-Arsenide Metal–Semiconductor Field Effect Transistor (GaAs MESFET), Indium–Phosphide Double Heterojunction Bipolar Transistor (InP DHBT) and Indium-Phosphide High Electron Mobility Transistor (InP HEMT). Amplifiers using devices from each of these families are designed, fabricated and characterized, and their characteristics compared in this chapter. This includes residual phase noise measurements performed for the first time at X–band class–E PAs.

- Chapter 7 presents related work using class–E microwave PA. First, an efficient way to control class–E PA output power by controlling the bias voltage is presented. As shown in Chapter 3, design of class–E PAs includes considerable postproduction tuning due to the numer-

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ous nonidealities and parasitics. The recent breakthrough in passive micro–electro–mechanic systems (MEMS) components (switches and varactors) allowed development of low–loss microwave tuning networks. A class–E MPA with an integrated MEMS tuner is designed and presented. A reconfigurable PA "intelligent" front–end is demonstrated using MEMS tuners integrated with the class–E PA. Depending on the applied modulation scheme, a single PA can be reconfigured between linear class–A mode of operation and switched, class–E mode. Initial steps in that design are presented in this chapter as well.

- Chapter 8 presents related and future work, categorized as follows:

  (1) Further improvements in tunable and reconfigurable class–E MPAs.

  (2) Design of tunable interstage matching networks using MEMS components, in order to simplify multistage high–efficiency PA design

  (3) Frequency extension of class–E MPAs. The highest frequency of operation achieved for class–E MPA so far is $12.5\,\mathrm{GHz}$. It is of interest to examine the possibility to design even higher frequency switched mode PAs, using new device technologies that are becoming available (HBT and HEMT). Pushing the power limit up is also of large importance, and becomes realistic especially with the breakthrough of new wide band–gap active devices.

  (4) Frequency bandwidth limitations of microwave class–E PAs.

(5) Further noise characterization of switched–mode class–E PAs. An integration of a noise–measurement with an automated load–pull system is proposed. The goal is to determine the optimal relationship between PA efficiency and phase noise.

(6) Application of large signal vector analysis (LSNA) for class–E PA development.

1.3   Class–E Microwave Power Amplifiers

The term "efficient amplification" means that the energy loss during the amplification process is small compared to the RF energy delivered to the load. A need for high efficiency RF and MW power amplification arises from the following facts:

(1) The DC energy supply is limited, particularly in hand–held systems (e.g. cell phone handsets), space-based systems, hazardous environment monitoring equipment, battlefield sensors, etc. Battery replacement in some of these applications is very difficult if not practically impossible.

(2) DC energy supply is expensive, in particular in high–power base–station networks due to the large number of transmit/receive cells involved. The cost of electrical energy for a single base station can achieve tens of thousands of dollars a year.

(3) Heat generated due to inefficient amplification can affect the performance or even damage an amplifying active device and therefore has to be removed. It is usually done using heat–sinks and, in the case of high–power application, forced cooling. Again, in the case of miniature hand–held devices it may become highly impractical to provide efficient cooling.

In a modern wireless communication system the transmitter contributes up to 50–75% of the total power consumption. The power requirements of the rest of a system (baseband processing and modulation parts) are already significantly reduced, using high–speed low–power CMOS circuits. Therefore, in order to further increase overal system efficiency, the PA front-end power consumption has to be optimized.

1.3.1 PA Energy Loss

The electric energy from the DC power supply that is lost during the amplification process consists of energy lost in: (1) the active device used to perform amplification (dissipative and switching loss); (2) lumped or distributed impedance matching and/or power combining networks; (3)unwanted harmonic and IMD products; (4) DC power supply lines, biasing and sensing networks; (5) linearization and control circuitry; and (6) radiation (transmission line discontinuities).

The loss external to the active device can be minimized following a set of

common design rules: for lower frequency high power applications, low loss (high–Q) lumped components (capacitors and inductors) should be used, in particular at the low–impedance points in matching networks, where high current densities are often encountered. In the higher frequency range, where the use of lumped components becomes unpractical, distributed lines on low–loss substrates are recommended. High–power combining networks (Wilkinson combiners, hybrid couplers etc.) can be designed with air as a dielectric, in order to eliminate dielectric loss. Excellent matching between amplifier halves in balanced configuration has to be enforced to minimize debalance loss in termination resistors. Use of high gain PA stages reduces the number of combining levels, and therefore minimizes insertion loss in dividing and combining networks. Reactive matching out of band of operation eliminates harmonic and some of IMD loss. Using large cross–section conductors for DC bias supply energy lost in supply circuits can be reduced.

However, in a typical high–power PA, more than 90% of the energy is lost in the active device. In order to closer examine the active device dissipative loss, let us consider a typical class–A biased linear PA shown in Fig. 1.1(a).

As long as the active device remains in its active regime, the output current is determined by the input electrode excitation (instantaneous value of input voltage or current that represents the input RF signal). Consequently, the output voltage is a response of the output circuit (load impedance) to the current of the current generator. The active device voltage and current waveforms are shown in Fig. 1.1(b). The power dissipated in the ideal con-
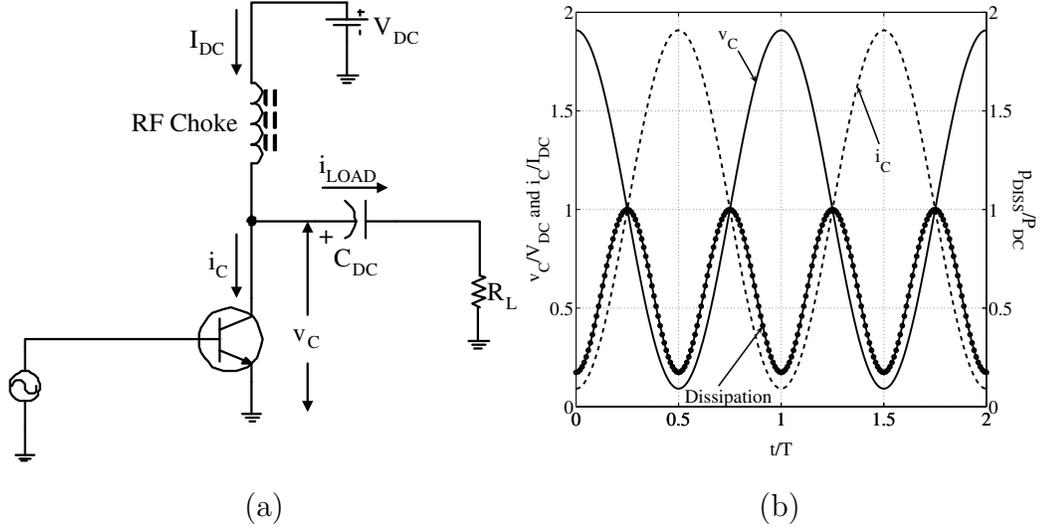
Figure 1.1: (a) Typical class–A power amplifier. (b) Normalized output voltage (solid), current (dashed) and instantaneous dissipated power (circles).

trolled current source $i_C(t)$ with voltage across it $v_C(t)$ can be calculated as

$$P_{DISS} = \frac{1}{T} \int_0^T v_C(t) \cdot i_C(t) \cdot dt, \tag{1.1}$$

for any arbitrary voltage/current waveshapes. Note that the loss is the characteristic of the current generator only. Loss also occurs in the resistive parts of the active device (ohmic resistances of bulk semiconductors, metallic electrodes etc.).

The dissipated power in Eq. 1.1 is proportional to time overlapping between output voltage and current waveshapes. If they are displaced in time (i.e. if there is no simultaneous existence of voltage and current on the ac-

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tive device), the dissipated power is entirely eliminated. This property is applied in any of switched mode techniques [2, 3, 4]. If switched mode is not applicable due to reasons that will be explained later, the dissipation on an active device still can be greatly reduced by decreasing the value of quiescent output current I_{CC} and reducing the conduction angle. This is a principle that lies behind the introduction of the numerous classes of operation with reduced conduction angle (A, B, AB, C) [3, 4]. The time overlapping between output voltage and current in those classes is significantly reduced, but not eliminated entirely (with the exception of zero P_{OUT} case with C–class of operation [4]).

1.3.2   Switched–mode of operation

From the discussion given in Subsection 1.3.1, it is clear that in order to eliminate power dissipation in an active device it is necessary to avoid simultaneous existence of voltage and current through it. In practice, it means that the concept of an active device acting as an ideal controlled current source has to be abandoned. The complete time displacement of voltage and current is naturally achieved on an ideal switch and power dissipation in such a component is entirely eliminated.

However, introducing a switch in an amplifying circuit has several implications:

- Contrary to an ordinary PA, in a switching PA both output voltage

and current are the transient response of a specially designed output matching network to a time variant circuit component (switch) and a constant DC source. Therefore, the ordinary rules for PA output matching design (load–line theory, [4]) do not apply to the case of a switched mode PA.

- The output voltage and current of a switching device are discontinuous and therefore rich in higher harmonic components. If not properly filtered out, these components are dissipated in the resistive load, limiting efficiency of such an amplifier (e.g. for a class–D amplifier, $\eta_{MAX} \approx$ 81%, [4]).

- Due to the discontinuous operation of reactive components (inductors and capacitors), increased voltage and current stress on the switching device is often present. This property limits the maximal output power to a level that can be considerably lower than a level achievable in linear classes of operation (A, B, AB) [1].

- In practice, an ideal switch is well approximated by an active device operating between cut–off and saturation (bipolar devices) or in triode regime (FETs). In that case any capacitance present between switch terminals is instantaneously discharged through the switch at the beginning of the ON–period, introducing *switching loss*. This mechanism further decreases maximal efficiency that can be achieved in switched mode of operation.

1.3.3 Class–E Mode of Operation

The output matching network in a class–E PA performs two important tasks:

(1) It shapes the voltage and current pulses in such a way that switching loss is minimized;

(2) It allows for the transistor's zero–voltage turn–on condition, reducing the equivalent input capacitance (due to the Miller effect). The result is increased switching speed;

(3) It performs harmonic filtering of the output current, therefore eliminating harmonic loss in the load.

This class of operation was introduced by Artym, Gruzdev, Popov, Kozyrev and Sokal [5, 6, 7, 8, 2] in early 70's. The latter gave first practical design formulas for output matching network components calculation. The breakthrough of class–E amplifiers in the microwave range was due to the work done by Mader and others [9]. However, the concept of voltage and current waveshaping in order to minimize switching loss is well known and applied in zero–voltage–switching (ZVS) resonant DC–DC converters [10].

The generic class–E circuit and ideal switch voltage and current waveforms are shown in Fig. 1.2(a). In [1] it is shown that switch voltage and current waveforms presented in Fig. 1.2 can be achieved under the following assumptions:
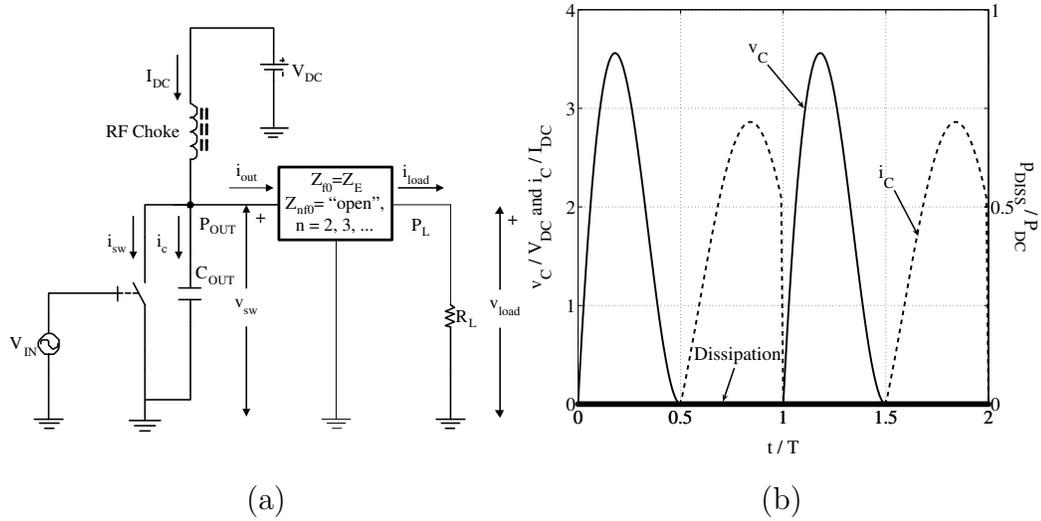
Figure 1.2: (a) Generic class–E power amplifier. The transistor is modeled as an ideal switch with a shunt capacitor C_{OUT}. (b) Output voltage (solid), current (dashed) and instantaneous dissipated power (thick solid).

- The active device operates as an ideal switch at ω_s, with 50% duty cycle (optimal for maximal P_{OUT} [11]);

- An ideal RF choke is used for drain voltage supply, maintaining constant collector (drain) supply current;

- "Open" termination at all higher harmonic frequencies (this corresponds to a sinusoidal output current assumption [2]), eliminating the harmonic power loss;

- At the fundamental frequency, the switch is terminated by a specific impedance given by:

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$$Z_E = \frac{0.28}{C_{OUT} \cdot \omega_S} e^{j49°} = R_E + jX_E, \tag{1.2}$$

where C_{OUT} is the total capacitance in shunt with the switch and ω_S is angular switching frequency.

In the case of a microwave PA, C_{OUT} is the output capacitance of active device. C_{OUT} is the main design parameter for class–E PAs (Eq. 1.2). In the case of lower frequency amplifiers ($\leq 1\,\mathrm{GHz}$) C_{OUT} is a part of the output matching network, and it is calculated as described in [2, 3, 4].

As shown in Fig. 1.2, due to the switching action, $i_{sw}(t)$ and $v_{sw}(t)$ are entirely displaced in time, eliminating the dissipation loss. The unique property of the class–E waveform can be observed in $v_{sw}(t)$ plot shown in Fig. 1.2(b): the switch closes when the voltage across C_{OUT} has a zero value. This means that the capacitor is "empty" at the moment when it gets shorted, thus avoiding the instantaneous discharge through the switch and eliminating the switching loss. In addition to that, the current through C_{OUT} also has zero crossing. This property contributes to a relatively insensitive class–E amplifier efficiency to the output impedance variation [12, 2]. The closed form time domain expressions for the transistor's voltage and current can be found by enforcing the following initial conditions [1]:

$$v_{sw}(t)\big|_{t=\frac{T_s}{2}} = 0; \qquad \frac{dv_{sw}}{dt}\Big|_{t=\frac{T_s}{2}} = 0 \tag{1.3}$$

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Performing Fourier transformation of these waveforms, the ratio between their fundamental components gives the optimal class–E output impedance, as given in Eq. 1.2.

The switch state is controlled by the input RF signal and that is the only information transfered between the input and the output of such an amplifier. This property makes class–E PAs particularly suitable for amplification of constant envelope signals (FM and ΦM). In order to further extend their applicability to signals with variable envelope, different techniques are available (EER, Chirex etc.).

1.3.4 Amplifier Efficiency Figures of Merit

For the PA efficiency characterization, three main figures of merit are commonly used: *drain (collector, DC–RF conversion) efficiency* (η), *power added efficiency* (PAE) and *overall efficiency* η_{ALL}, defined as:

$$\eta = \frac{P_{OUT}}{P_{DC}}, \tag{1.4}$$

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}}, \tag{1.5}$$

$$\eta_{ALL} = \frac{P_{OUT}}{P_{DC} + P_{IN}}, \tag{1.6}$$

where P_{OUT} is the power delivered to the load at the frequency of operation (power dissipated in the load at harmonic frequency is considered as a loss). P_{DC} is the power taken from the DC source, and P_{IN} is the input power. The drain (collector or DC–RF conversion) efficiency, Eq. 1.4 compares the output RF power with power taken from the DC source. In the case of bipolar active devices, both collector and base DC power consumption has to be taken into account. As part of a system, the PA is more often characterized by PAE (Eq. 1.5) which takes into account the input power in addition to the output and DC source power. Finally, if a PA is characterized as a "black box" using the power conservation principle, overall efficiency is commonly used (Eq. 1.6).

An important note has to be made with regard to the input power. In the case of an unconditionally stable, linear (small–signal) amplifier, the power available from the generator (P_{AV}) is equal to the power that enters the amplifier (P_{IN}) if the input of such an amplifier is conjugately matched to the source impedance [13]. However, if an amplifier is not unconditionally stable, it may not be possible to achieve complex–conjugate matching at the amplifier input. Similarly, PAs are often intentionally mismatched at their input (e.g. to achieve flat gain in wider frequency bandwidth, better linearity etc.). Even more practically, the input impedance of a PA usually is not known simply because high power measurement of the reflection coefficients require specialized and expensive equipment, and such measurements are power– and bias–dependent. In both cases, P_{IN} is always *smaller* than P_{AV}. In situations

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like these, PAE and η_{ALL} are both referred to the available power (P_{AV}). This convention is followed throughout this text because it gives more conservative results, and better corresponds to the fact that any PA is always part of a more complex system, with preceding and following parts usually independently designed. In practice, however, this potential ambiguity in efficiency figures of merit is avoided by the fact that PAs are always made to operate in matched condition, either by applying a nonreciprocal component (isolator) or a balanced configuration.

1.3.5 Class–E PA Dimensioning

The active device operating as a switch in a class–E PA is subjected to a considerable voltage and current stress. The peak current and voltage values exceed those of linear classes of operation and in a similar fashion they determine the maximal output power that can be generated at the output of such a PA. Consider an active device approximated as an ideal switch, assuming that all conditions given in Subsection 1.3.3 are satisfied. The switch voltage (equal to the transistor output voltage) during the "OFF" half–period is [1]:

$$v_{SW}(t) = \frac{I_{DC}}{C_{OUT} \cdot \omega_S}(\omega_S t - a \cdot (\cos(\omega_S t + \phi) - \cos \phi)) = v_T(t), \qquad (1.7)$$

while the switch current during the "ON" half–period is:

$$i_{SW}(t) = I_{DC}(1 - a \cdot \sin(\omega_S t + \phi)), \quad (1.8)$$

where a $= 1.862$ and $\phi = -32.48°$. The current flowing into the output matching network $i_{OUT}(t)$ is sinusoidal due to the "open" harmonic termination in its path:

$$i_{OUT}(t) = a \cdot I_{DC} sin(\omega_S t + \phi)), \quad (1.9)$$

while the current flowing into the switch/capacitor branch (corresponds to the drain or collector current) is:

$$i_T(t) = I_{DC} - i_{OUT}(t) = I_{DC}(1 - a \cdot \sin(\omega_S t + \phi)). \quad (1.10)$$

The peak values of switch voltage and transistor current values are therefore:

$$V_{T-MAX} = 1.134 \cdot \frac{I_{DC}}{\omega_S C_{OUT}}, \quad (1.11)$$

$$I_{T-MAX} = (1 + a)I_{DC}. \quad (1.12)$$

From the Eq. 1.9 the average power delivered to the matching network is

$$P_{OUT} = \frac{1}{2} R_E (a \cdot I_{DC})^2, \tag{1.13}$$

where R_E is the real part of the fundamental output impedance Z_E, Eq. 1.2. If the output matching network is lossless, then the power delivered to the network is equal to the power delivered to the load ($P_{OUT} = P_L$). From the Eq. 1.13 it can be inferred that higher output power P_L corresponds to a higher I_{DC}, resulting in the higher peak output voltage and current (Eq. 1.11 and Eq. 1.12).

Assume that the given active device has the maximal current range of I_{MAX} and the maximal voltage V_{MAX}. The first step in determining the maximal output power that can be generated using such a device is finding out whether the transistor voltage or the current limit is a critical one. This can be found if we first assume that the current limit is reached (i.e. $I_{T-MAX} = I_{MAX}$). From the Eq. 1.11 and Eq. 1.12, the corresponding maximal value of the transistor voltage is:

$$V_{T-MAX} = 1.134 \cdot \frac{I_{DC}}{\omega_S C_{OUT}} = \frac{1.134}{1+a} \cdot \frac{I_{T-MAX}}{\omega_S C_{OUT}} = 0.4 \cdot \frac{I_{MAX}}{\omega_S C_{OUT}}. \tag{1.14}$$

Two possible situations could occur:

(1) $V_{T-MAX} \leq V_{MAX}$. This means that the assumed current peak value is indeed the critical one. In that case, using Eq. 1.12 with substituted

$I_{T-MAX} = I_{MAX}$ the average transistor current I_{DC} can be found. Corresponding output power can be found using Eq. 1.13.

(2) $V_{T-MAX} > V_{MAX}$. This means that the initial assumption was not correct, and for the given transistor the voltage limit is more critical. Therefore, $V_{T-MAX} = V_{MAX}$ and then from Eq. 1.11 the average transistor current I_{DC} can be found. Then again, corresponding output power can be found using Eq. 1.13.

Finally, the required DC voltage supply can be calculated from the ideal efficiency assumption ($P_{DC} = P_{OUT}$):

$$V_{DC} = \frac{P_{OUT}}{I_{DC}} \tag{1.15}$$

As an example, a 10-GHz class–E PA using an active device with the following parameters will be dimensioned:

Table 1.1: Active device parameters for Class–E PA.

I_{MAX} [mA]	V_{MAX} [V]	C_{OUT} [pF]
140	10	0.107

I_{MAX} and V_{MAX} - transistor maximal output current and voltage ratings, C_{OUT} - output capacitance

These parameters correspond to an active device used for the class–E microwave PA design in Chapter 3. For the given output capacitance, using Eq. 1.2, the optimal class–E impedance is found. Following the described procedure the amplifier parameters are calculated and given in Table 1.2.

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Table 1.2: 10-GHz class–E PA parameters.

Z_E [Ω]	I_{T-MAX} [mA]	V_{T-MAX} [V]	P_{OUT} [mW]	V_{DC} [V]	I_{DC} [mA]
27.3+j35.1	140	8.25	113	2.32	48.9

Z_E - class–E optimal output impedance, I_{T-MAX} and V_{T-MAX} - transistor peak output current and voltage, $P_{OUT} = P_L$ - average load power, V_{DC} and I_{DC} - average transistor voltage and current.

Using a commercial harmonic–balance simulator (Agilent $ADS^{®}$), the idealized switch circuit from Fig. 1.2 is analyzed for the given voltage and current maximal rating and the output capacitance. The simulated response is shown in Fig. 1.3, confirming the calculated parameters.
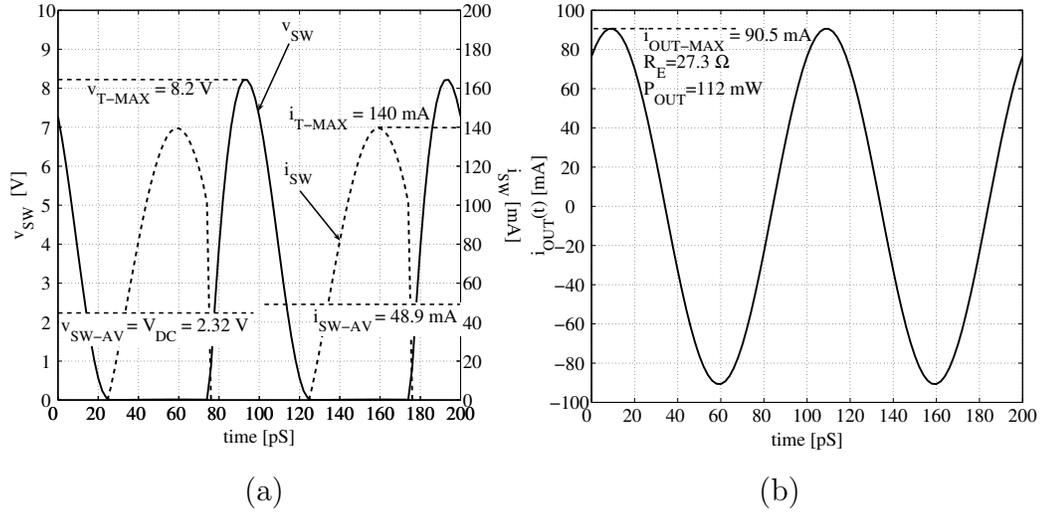
Figure 1.3: (a) Simulated ideal switch voltage (solid) and current (dashed) in class–E mode. (b) Output current through the optimal class–E impedance.

The previous calculation indicates that for the given active device, the

limitation is the maximal current rating (140 mA), while the voltage peak value is noticeably below the maximal voltage rating.

1.3.6 Output Power Control

An obvious disadvantage in using class–E mode of operation is its limitation to amplification of signals with constant envelope. Even if such signals are being used, in practical situations (e.g. dynamic wireless communication environment) the output power needs to be precisely controlled. The minimal output signal level is determined by required signal to noise ratio for achieving reliable transmission and reception) and it varies with variations in channel properties. Due to the effects on other users (which often share same or close carrier frequency (near–far problem)) and the energy requirements, it is not possible nor practical to constantly operate at the full power level. Because of that, in modern wireless communication systems the required average power level can change within a few seconds period in a range of few tenths of decibels. In practice, this task is performed through:

- Gain control. Using variable attenuators in an amplifier chain the input power to the final stage is regulated.

- Bias control. The bias of the output (or driver) stages is regulated limiting the output power to the desired level.

In order to maintain high efficiency and linearity these techniques are often combined.

Despite the constant envelope limitation, ideal class–E amplifiers are suitable for applying different bias control schemes, which in principle can be extended to bias modulation (e.g. Kahn's *Envelope Elimination and Restoration (EER)* [14]). This technique allows application of saturated PAs (such as class–E PA) to variable envelope modulation schemes that are used in most of the modern communication systems [15]. The reason for this is the principal independence of the class–E DC–RF conversion efficiency on variations in output bias voltage, as well as the linear proportionality between output and drain supply voltage.

The calculation presented in Subsection 1.3.5 is directed to determine optimal biasing condition for extracting maximal output power from a class–E PA. It can be easily extended to extract arbitrary output power below the maximum. If the DC supply voltage is provided through an ideal RF choke, the average value of the switch voltage has to be equal to the DC drain supply voltage V_{DC}. Using Eq. 1.7 it can be found:

$$V_{DC} = \frac{1}{T_S} \int_0^{T_S} v_S(t) \cdot dt = \frac{I_{DC}}{\pi \cdot \omega_S \cdot C_{OUT}}. \tag{1.16}$$

Substituting I_{DC} from Eq. 1.16 into Eq. 1.13, the power delivered to the matching network (Fig. 1.2) is:

$$P_{OUT} = \frac{1}{2} R_E \cdot (a \cdot \pi \cdot \omega_S \cdot C_{OUT})^2 \cdot V_{DC}^2. \tag{1.17}$$

The output matching network transforms load resistance R_L into the complex optimal impedance Z_E. If the network is lossless, power dissipated in R_E is actually power dissipated in R_L. Therefore, amplitude of the load voltage is:

$$V_L = \sqrt{2 \cdot P_L \cdot R_L}. \tag{1.18}$$

If the matching network is lossless $P_L = P_{OUT}$ and substituting P_{OUT} from Eq. 1.13 into Eq. 1.18, the relation between V_L and V_{DC} is

$$V_L = a \cdot \pi \cdot \omega_S \cdot C_{OUT} \cdot \sqrt{R_L R_E} \cdot V_{DD}. \tag{1.19}$$

By dynamically changing output supply voltage V_{DC}, the output voltage of the class–E PA can be modulated. If the phase information from the original input signal is preserved through the amplifier, the amplified version of the signal can be reconstructed at the output, through the bias modulation. Since the variation of the V_{DC} does not affect output voltage and current shape (except for the scaling factor), the optimal output impedances and other conditions for achieving such waveforms remain the same. Therefore, the optimal class–E impedance is not affected by the supply variation and the amplifier will still operate with ideal efficiency. An implementation of such system with a microwave class–E PA is presented in Chapter 7. Results of the performed analysis are also used in the design of two–stage class–E PA, Chapter 5.

Chapter 2

Realizations of Class–E Microwave PAs

2.1 Introduction

Depending on the operation frequency, there are three distinctive realizations of class–E PAs:

- For frequencies $< 0.5\,\mathrm{GHz}$, high–Q lumped elements are used in the output matching network, implemented as a series resonant circuit in combination with shunt capacitance across the device output terminals [2, 12]. The required termination at the fundamental frequency is provided by detuning the resonant circuit. The filtering of the harmonic components is performed by presenting a high impedance path to the output current [2]. The components of the matching networks are

directly calculated from the known C_{OUT}, power requirements and Q–factors of available components. Additional impedance transformation is usually required in order to transform the arbitrary load resistance into one required for class–E operation.

- For frequencies above > 2 GHz, a distributed realization of matching network is more appropriate, due to the increased loss in lumped elements and their parasitics. Microstrip or coplanar waveguides (CPW) on low–loss substrates are commonly used. The fundamental frequency impedance is generated by a single or a double shunt–stub matching network. The harmonic frequency termination at the device reference plane is provided by harmonic "traps" ($\lambda/4$ series/shunt open stub combinations). Due to the limited space and need for post–production tuning, usually no more than three harmonic frequencies are terminated [1, 9].

- For frequencies between 0.5 and 2 GHz, combined lumped–distributed realization is used in order to minimize the overall circuit size as well as the insertion loss.

Despite the simplicity of the ideal class–E mode, the practical design has several challenges, especially for PAs in the microwave frequency range. Some of the initial assumptions that underline basic design equations cannot be entirely satisfied in reality, resulting in degradation of P_{OUT}, efficiency, gain, bandwidth, maximal frequency of operation etc. Since the invention of

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class–E PAs, in the early 70's, considerable work has been done on analyzing different nonidealities and limitations and proposing possible improvements in class–E design as well as alternatives. An overview of main issues related to the practical implementation of class–E PAs follows.

2.2 Transistor and Circuit Nonidealities in Class–E Mode

As stated earlier, the switch in a class–E PA is an active device (transistor), operated between two extreme states - "OFF" (cut-off regime) and "ON" (saturation (BJT) or triode (FET) regime). The active device related non-idealities are:

- *Finite switching time.* The transition time between extreme active device states is mainly limited by the speed of the active device itself (carrier mobility, transistor regions dimensions and parasitic capacitances). For microwave transistors the transition time is related to f_{MAX} (maximal frequency of oscillation) and f_T (cut-off frequency) parameters [16]. During the transition time, output voltage and current are simultaneously present, resulting in dissipative loss. As long as the transition does not last for a considerable part of each RF cycle ($\leq 10\%$), the efficiency will be minimally affected as a result of current and voltage waveshaping. It is usually considered that transistors

intended to operate in class–E at frequency f_S should obey this rule: $f_S \leq (0.1 - 0.2) f_{MAX}$. The modified formulas for calculating P_{OUT} and efficiency are in case of finite switching speed are given in [17, 18].

- *Finite "ON" and "OFF" resistances.* During the "ON" state, a bipolar transistor is in saturation, behaving as a real voltage source with small but finite internal resistance as a result of the ohmic loss in the semiconductor and metal electrodes. During the "OFF" state, the resistance between output electrodes will be finite, due to the small current leakage through the substrate and reverse polarized junctions. The situation is similar in field–effect transistors. The finite resistances result in simultaneous output voltage and current at the transistor output during the entire RF cycle, increasing dissipative loss. The effects of finite resistances are addressed in [17, 19], by modifying the original set of class–E power equations.

- *Active device internal parasitics.* These are: inter-electrode capacitances, electrode pad parasitics, emitter (source) grounding via parasitics, parasitic substrate diodes, additional controlled current sources used to model substrate effects etc. One should keep in mind that in any active device model, the controlled current generator (described by transconductance g_m) is the main source of dissipative loss. Therefore, optimal load impedance has to be presented to its terminals. To describe operation of an active device numerous large–signal models

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that include lumped and distributed components are created. Their complexity might be tremendous and practical ways to handle these problem will be presented in Section 2.4 and detailed throughout the thesis.

- *Nonlinear output capacitance.* C_{OUT} used to calculate optimal class–E impedance is composed of several internal capacitances (e.g. for the simple FET model: C_{DS}, in parallel with a combination of C_{GD} and C_{GS}). This capacitance is dependent on the output voltage, due to the voltage dependence of C_{GD} and C_{GS}. Presence of such capacitances alters the output voltage and current shapes, affecting both the efficiency and maximal output power [1, 20, 21, 22].

- *Output supply voltage (V_{DC}) limitations.* As shown in Subsection 1.3.5, the maximal output power that can be extracted depends on the maximal ratings of the transistor, mainly on the breakdown voltage (V_{MAX}). However, this voltage is usually determined only at DC or very low frequency, because the existing equipment (e.g. curve–tracers) does not operate at microwave frequencies. V_{MAX} can differ significantly at the frequency of operation, so that maximal power handling can only be estimated or empirically determined. On the other hand, the minimal value of output supply voltage is determined by the "knee" in the transistor static characteristics. Namely, if the output supply voltage approaches the "knee" region, the transconductance of the de-

vice rapidly drops. This results in a significant power gain drop [1]. Therefore an active device has to be biased above the "knee" voltage to maintain considerable gain. This property determines the so called *maximal frequency of class–E operation* - f_{E-MAX} [1].

The external circuit nonidealities and limitations are:

- *Mounting parasitics.* At low frequencies the active device is usually one or more packaged semiconductor die, connected to the package pads by multiple bond–wires. The package is soldered to the external circuit. The packaging of the active device introduces parasitics (pad capacitances, bond wire inductances, etc.) that can at lower frequencies be characterized and embedded into the load impedance. However, at microwave frequencies, the influence of parasitic reactances becomes considerable and the use of packaged devices is avoided, with flip–chip bonding preferred over wire–bonding.

- *Finite quality factor (Q_L) of the output resonator.* Due to the finite realizable reactances in the output matching circuitry, the assumption of time–harmonic output current $i_{OUT}(t)$ is violated, affecting both the voltage and current waveshapes and allowing loss in load resistance at harmonic frequencies. This problem is treated in [23, 24, 19]. In the case of a microwave class–E PA output circuit, a number of harmonic stubs are necessary to approximate class–E waveforms [1].

- *Finite impedance of RF choke/bias lines.* This component plays a significant role in establishing proper class–E waveforms and its effects are thoroughly studied. The common approach is to include effects of the RF choke/bias lines into the output matching network and use it even to increase the available power from the active device [25, 26, 19, 27]. It can be done partially analytically, or using a nonlinear simulator with circuit optimization tools.

2.3 Input Matching

According to linear PA design theory, the input port of a PA has to be conjugately matched to the source generator impedance in order to achieve maximal power transfer between them. If the condition $Z_S = Z_{IN}^*$ [13] (Fig. 2.1) is satisfied, the following occurs:

- The entire available power from the source generator is delivered to the input port of the active device;

- Maximal power gain for the given load impedance is achieved;

- VSWR at the PA input port (normalized to the source impedance of the generator) is equal to 1, therefore, input of the PA is ideally matched to the generator.

For known load reflection coefficient Γ_L, and active device S–parameters the input reflection coefficient Γ_{IN} (that corresponds to Z_{IN} in Fig. 2.1) can

31
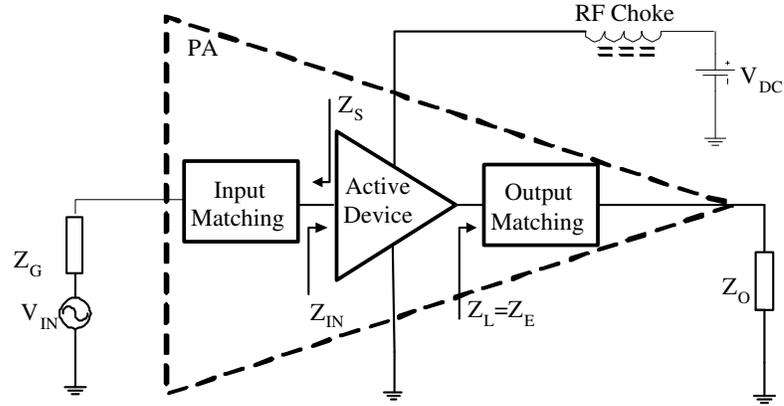
Figure 2.1: Class–E PA input and output matching schematic.

be found as [13]:

$$\Gamma_{IN} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L}. \tag{2.1}$$

A class–E PA operates with several dBs of gain compression so that linear theory does not apply. Without an accurate nonlinear model or large signal measurements at the PA input port it is not possible to *a priori* predict Z_{IN}. However, as will be shown in the following chapters, the linear approach provides an acceptable initial point for input matching design.

2.4   Class–E Microwave PA Design Methodology

Overview of numerous issues related to the practical implementation of a class–E microwave PA anticipates the difficulties that are encountered during the design and optimization of such an amplifier. It is worth noting that some of these nonidealities are common to the design of most large–signal PAs, irrespective of the class of operation, resulting in decrease in efficiency and output power. A class–E PA design procedure is presented in Fig. 2.2. The designer can take one of three different paths, depending on whether a nonlinear model for the selected active device and/or a harmonic load–pull system is available.

What follows is a brief explanation of these systematic approaches used to design a microwave class–E amplifier. PA design examples and applications are presented throughout the following chapters.

2.4.1   Analytical Approach

The analytic design procedure (Fig. 2.2) relies on an accurate active device output capacitance extraction based on small–signal S–parameter measurements and basic class–E theory presented in Chapter 1.

From the known C_{OUT}, an optimal load impedance $Z_L = Z_E$ can be determined (Eq. 1.2), as well as the optimal bias for the expected P_{OUT} (Chapter 1). A small signal S-parameter measurement provides an approximate

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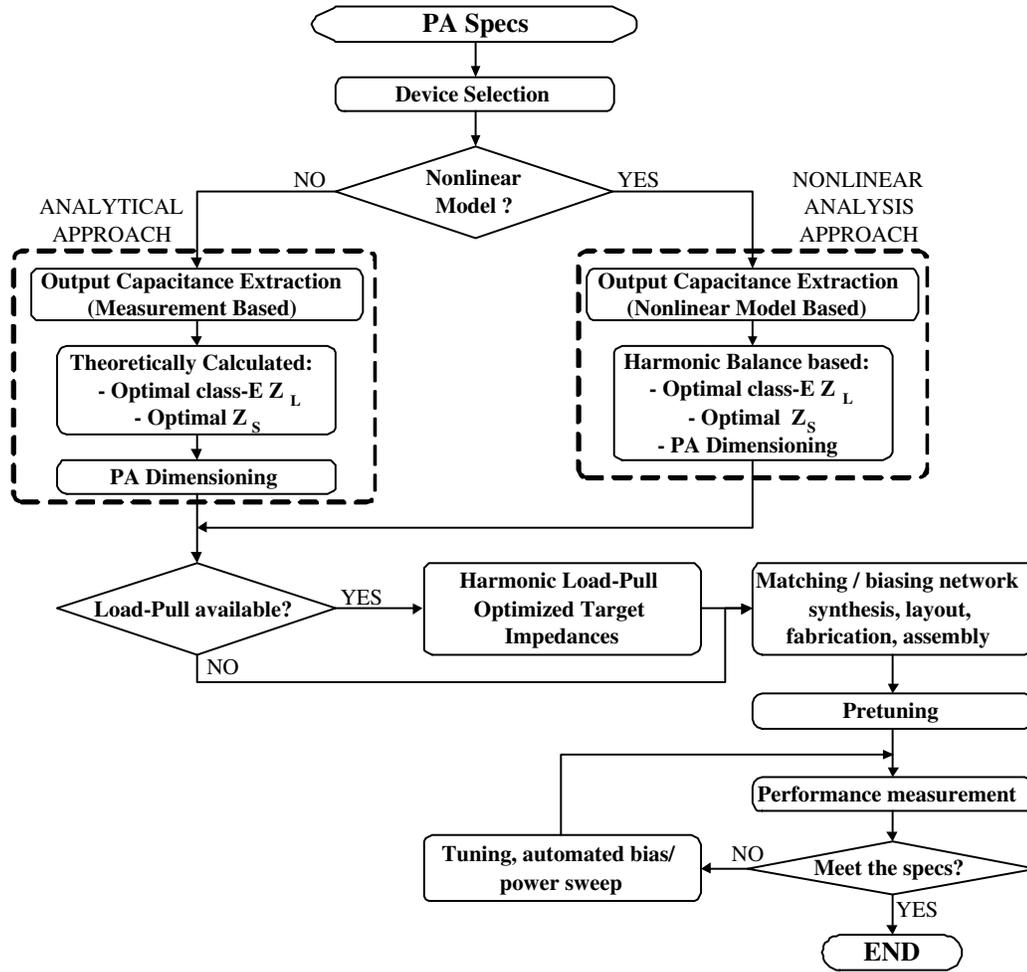
Figure 2.2: Microwave class–E PA design procedure.

input impedance Z_{IN}. Input and output matching networks with biasing components are then synthesized using a linear circuit simulator. Modeled or measured major parasitics (bond wire inductances, pad capacitances etc.) are embedded in the matching network. The basic set of design formulas can be augmented to include effects of nonlinear output capacitances, finite

DC feed impedances etc. However, in the case of microwave PAs, most of the effects are "masked" by the numerous internal and external active device parasitics. Due to the considerable idealizations and the finite accuracy in the parasitics modeling, this method provides only a good starting point for systematic post–production tuning (Chapter 3).

2.4.2 Nonlinear Circuit Simulation Approach

This approach is used if a good nonlinear model for the chosen active device is available. After C_{OUT} is determined (using measurements or nonlinear model) and an approximate optimal load impedance calculated, a nonlinear circuit simulator can be used to predict and optimize the PA performances. This is the most comfortable approach from a circuit designer viewpoint, that takes into account most of the active device nonidealities. However, nonlinear models that accurately predict performances of switch–acting microwave devices are not often available. Existing models can be used to a certain extent [28], mainly to predict trends and a moderate amount of post–production tuning with several design iterations can be expected.

In the following chapters, comparison between measured and simulated performances is presented in the cases where a nonlinear model for the active device was available. A nonlinear model is used to determine sensitivity of the class–E microwave PA on load impedance variations (Chapter 3).

2.4.3 Load–Pull Approach

Design of any PA, including class–E PA, starts with determining the optimal load and source impedances to achieve required characteristics (P_{OUT}, gain, efficiency, linearity etc.). The load–pull method is a systematic search throughout the load and source impedance planes, using passive (mechanical or electronic) or active (signal injection) tuners [4]. Once the optimal load and source impedances are found, they have to be accurately realized by appropriate matching networks. Using a developed systematic pretuning strategy, the input and output matching networks can be separately designed and optimized, before the final PA is assembled. From all presented methods, this one results in a minimal amount of post–production tuning. The main drawback is the high cost of the available accurate tuners for microwave frequencies and a relatively complicated calibration procedure. An application of the method is illustrated in Chapter 4.

2.4.4 Design Tools

Due to the high complexity of nonlinear phenomena within a class–E microwave PA and the need for an accurate modeling of passive matching networks, computer–based simulation and design tools are widely used. What follows is a brief description of the computer–aided engineering (CAE) methods used throughout this work.

If a nonlinear model for the selected active device is not available, pas-

sive PA components (input and output matching and biasing networks) are designed using a linear microwave circuit simulator (e.g. Agilent $ADS^®$ or Ansoft $Designer^®$). Target impedances (Z_S and Z_L) are determined using the analytical approach or the load–pull characterization. The simulator has the ability to accurately model microwave passive components (microstrip lines, stubs, lumped elements) as well as discontinuities (microstrip junctions, "open" and "short" line effects etc). Commercial linear simulators are supplemented by a wide variety of optimization tools that can be used to quickly determine matching circuit topology. Using measured S–parameters, a circuit optimizer can be used to extract the entire small–signal model of the transistor, including the C_{OUT}.

The next level in the use of linear simulation tools is adding a full–wave EM simulation capability. Using the Method of Moments (MoM) for planar circuit analysis, it is possible to accurately predict responses of the passive structures (matching and biasing networks), decreasing the amount of postproduction tuning. In addition, 3D full–wave methods (finite element method (FEM) for example) can be used to accurately model the discontinuities and parasitics around the active device mounting area. Modern linear simulators allow integration between circuit and EM solvers, allowing user to develop its custom library of EM simulation–based parameterized circuit components. This offers a better prediction of the final circuit performances with significantly decreased simulation time.

Finally, if a nonlinear model for active device is available, a nonlinear

circuit simulator can be used. Between many of the developed methods, the Harmonic–Balance (HB) is commonly used for simulation of strongly nonlinear PAs. HB is a frequency domain method that separates the circuit into two blocks. One block encompasses all nonlinear components, while the linear components and excitations (bias, source generators) are grouped into the second one. The two blocks are connected through new formed ports, with uniquely defined set of common voltages and currents. The solver determines port voltages at given fundamental and harmonic frequencies, using different optimization algorithms [29]. Once the port voltages are determined, the port currents can be directly found from admittance matrix, representing the linear portion of the circuit, or after a transformation in the time domain from the nonlinear part of the circuit.

The HB method allows the optimization of matching networks including most of the parasitics and nonlinearities of the applied active element. In addition, it allows the analysis of sensitivity to load impedance variations. Yield optimization and design–centering can be performed to produce robust and repeatable class-E PAs, such as the used for a 16–element spatial power combiner presented in Chapter 3. However, the HB method does not allow analysis of a transient circuit response.

2.4.5 Nonlinear Models for Switched–Mode Active Devices

Class-E PAs employ active devices operating under large signal conditions. This means that the amplitudes of the active device voltages and currents are comparable to the quiescent operating point values. Therefore, the basic linearity (small–signal) assumption is violated, the superposition principle does not hold and the well-developed linear microwave circuit design methodology (based on S–parameter circuit description [13]) cannot be applied.

Nonlinear circuit analysis tools, such as HB, rely on nonlinear models for active devices. Numerous large signal models for active devices are developed for different applications. They are based on either semiconductor physics or behavioral description of the active device [30, 16, 31]. The first group is commonly used by the active device designers, while the second group is used by circuit designers. Unlike small signal models, the large signal models include voltage–controlled nonlinear components (i.e. capacitors, resistors, current and voltage sources etc.).

In the case of behavioral large-signal models the nonlinear dependences of the capacitances and transconductances on circuit voltages are described using convenient mathematical representations, such as complex polynomial curves with parameters adjusted during the model extraction process. The extraction of large signal model parameters is usually done by performing a large number of small–signal (S–parameters) measurements, for an extensive

set of bias points, input power levels and frequencies. Using the obtained large set of measured data, unconstrained optimization methods [30] are applied in order to adjust the parameters of a selected nonlinear model. The optimization goal is to achieve good agreement between simulated response and measured bias/power dependent S–parameters.

Only large design houses can afford this complex and time-consuming task. Even in their case, the measurement is narrowed down to a range of bias points and power levels where the active device is going to be most likely used. Because of that, the available models can be satisfactory accurate only within that range. Here lays the main problem with nonlinear models for microwave transistors operating in switched mode–the usual parameter extraction do not cover the range of operation of active device in switched–mode (around the cut-off and in saturation). Moreover, switched mode PAs operate in deep compression with highly expressed nonlinearity. A single–frequency input voltage wave results in considerable harmonics in reflected and transmitted waves. These are not taken into account in ordinary vector network analyzers (that are measuring S–parameters one frequency at a time), significantly reducing the accuracy of such extracted models. Some attempts to derive nonlinear models for class–E operating active devices at lower frequencies have been undertaken [32, 33, 34].

From the reasons stated above, the present models have only limited use for predicting and optimizing parameters of class-E PAs in the microwave regime. This is the reason for using other methods of class-E PA design

and optimization, such as systematic postproduction tuning and load-pull methodology. A promising method in accurate switched–mode parameter extraction is the use of large signal network analysis (LSNA), where instead of fundamental frequency small signal S–parameters measurements, large signal voltage waves are simultaneously generated and measured at a number of harmonic frequencies, allowing for more realistic parameter extraction and nonlinear model validation [35, 36, 37].

2.4.6 C_{OUT} Determination

A common part of all of the methodologies presented above is the extraction of the output capacitance. The C_{OUT} of the active device can be extracted on several different ways. For lower–frequency operation ($\leq 2\,\text{GHz}$) and higher power active devices, the direct measurement of the capacitance can be performed. It can be done with a C-meter (e.g. bridge based), impedance analyzer or a vector network analyzer (VNA). The active device is biased in cut-off ($V_{IN} < V_T$ and $V_{OUT} = V_{DC}$). In order to separate the influence of parasitic bond–wire inductances (L_{bw}), the measurement has to be performed at a frequency considerably lower than the operating one. C_{OUT} can be measured at an anticipated bias point or the entire $C_{OUT}(V_{DC})$ profile can be acquired.

If the impedance analyzer or VNA is used, the measurement can be repeated at higher frequency, and using previously determined C_{OUT}, the parasitic L_{bw} and the series resistances can be easily determined. From mea-

sured static DC characteristics many other active device parameters can be estimated, such as the "ON" conductance of the switch (slope of the DC characteristics at the saturation (triode) range). A curve tracer operating in a pulsed mode can be used to determine the breakdown voltage V_{MAX} and the maximal current limitations I_{MAX}.

Lower frequency power devices have output capacitances of a few tenths to a few hundreds of pF (approximately: 1.5–2 pF per Watt of output power). For active devices operating in the microwave range, the output capacitances are significantly smaller, usually well below 0.5 pF. The corresponding reactance is comparable to parasitic reactances of the measurement setup and therefore more sophisticated methods have to be used. This involves a TRL–calibrated multifrequency S-parameters measurements. A general method suitable for extraction of the entire small–signal model of a microwave field effect transistor is presented in Appendix A.

Chapter 3

Spatial Combiner of Class–E Microwave Power Amplifiers

3.1   Introduction

Spatial power combining is a promising technique for efficient microwave power generation. In the microwave range (X–band and above) solid–state high–power active devices are not available, and with the current trends in active device development a single device with more power than a few Watts will not be achievable soon. Therefore, if higher power is required, different power combining techniques need to be employed. Power from the smaller active devices can be combined using corporate power combiners, such as transmission–line based binary combiners (e.g. the Wilkinson combiner, the hybrid coupler etc.) [38, 39, 40], N–way power dividers/combiners (N–line

junctions, radial N–way combiners etc.) [41], waveguide combiners [42, 43] and finally spatial combiners [40]. The most common way to combine power is to use a multilevel binary corporate combiner shown in Fig. 3.1(a).
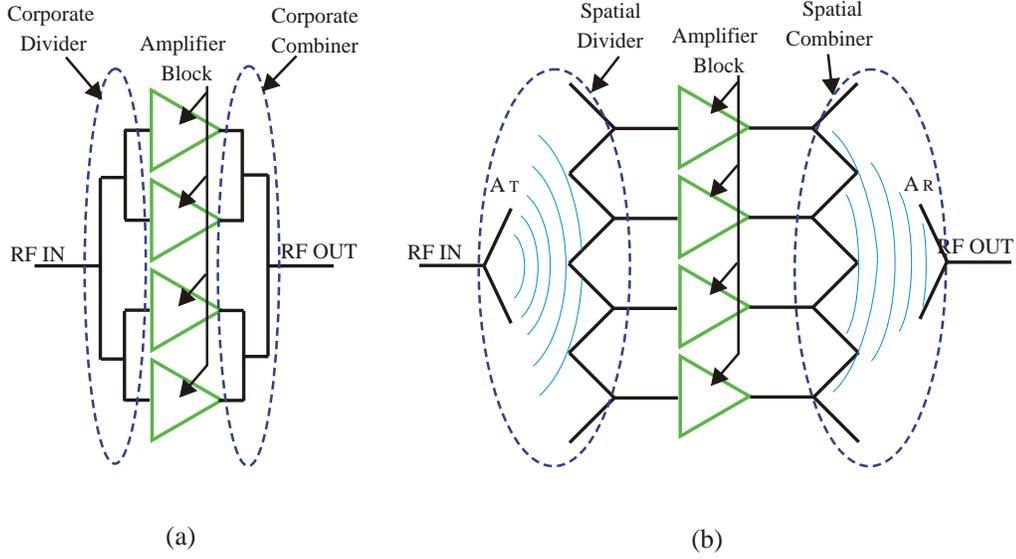
Figure 3.1: (a) Corporate power combiner using a multiple–level binary divider/combiner. (b) Spatial power divider and combiner.

Source power is equally divided between N identical amplifiers. After amplification, signals are coherently combined at the output using a combiner with the same topology as the divider. In order to combine N PAs using such a combiner, $n_c = \log_2 N$ combining stages are required. Each of the combining stages adds unavoidable insertion loss, while the total power gain ideally remains equal to the single amplifier gain. It is clear that the number of combining levels cannot be arbitrarily increased because the total insertion loss will ultimately reach the amplifier's gain. This problem can

be partially overcome using different N–way combiners, sacrificing isolation between stages and therefore introducing PA matching problems.

A spatial power combiner is generally a combination of a receiving and a transmitting antenna array, with a LNA/PA between each individual pair of antenna elements, Fig. 3.1(b). Input power transmitted from a common antenna (A_T) is collected by the elements in the receiving array and distributed among the large number of small size active devices. Small portions of the input power are amplified and coupled to the radiating elements on the transmitting array. The radiated RF power is coherently added in free space forming the antenna array radiation beam. Using a common receiving antenna (A_R) the power can be collected into a convenient wave–guiding system. The combining efficiency of such a combiner does not depend on the number of elements [40], as long as the entire radiated power can be collected. Therefore, in principal, any output power can be achieved by scaling N. A common figure of merit for spatial power combiners is *Power Combining Efficiency* (PCE), defined as:

$$PCE = \frac{P_{RAD}}{N \cdot P_{AVAIL}},$$ (3.1)

where P_{RAD} is the total radiated power from the combiner, P_{AVAIL} is the power available from a single amplifier in a circuit configuration, and N is the number of active elements in the spatial combiner.

This concept has several problems and this work is focusing on one of

the most challenging: the heat handling. Namely, the large number of active devices in the combiner generates a considerable amount of heat, mainly due to inefficient amplification. Because of 2–D combiner topology, it is hard to remove the generated heat from the combiner. If untreated, the generated heat in the most benign case will result in a negative temperature gradient between the PAs in the middle of the array and the PAs closer to the array edge [44]. Because PA gain is a function of temperature, this results in output power tapering between PAs within the combiner. In the case of PAs operating near compression, this is accompanied by a phase taper due to AM–PM conversion. Both of these properties affect the output radiation pattern, considerably decreasing the combining efficiency.

In order to solve this problem, a "tolerance–hardened" switched–mode class–E PA is designed, using previously described methodology. It is integrated with an antenna element and used as a building block for an active antenna array. The array has a corporate power divider on the input and combining antenna array at the output (Fig. 3.2).

This architecture is chosen due to the required input signal uniformity, necessary to achieve equal compression of the class–E PAs, maintaining the PA efficiency and PCE. Namely, the receiving side of a spatial combiner is usually placed in the near–field of a distributing antenna in order to minimize spill–over loss [40]. However, it is difficult to maintain amplitude and phase uniformity over the entire receiving surface. Use of a conventional corporate feed effectively solves this problem.
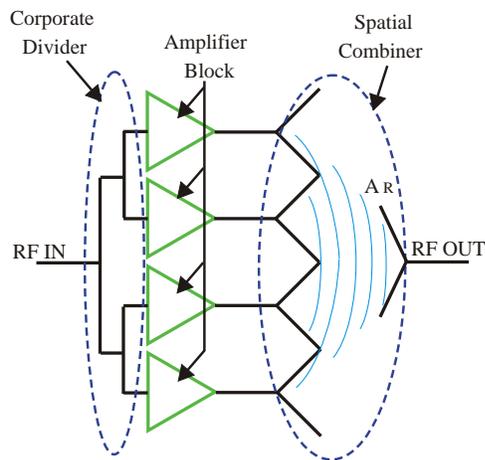
Figure 3.2: Active antenna array, with corporate feeding network, as a special case of spatial combiner [45].

This is the first successful X–band realization of a switched–mode active antenna array. With 16 corporately–fed antenna elements it achieves a very high average drain efficiency of $\approx 70\%$, with power combining efficiency of over 79%. The effective isotropic radiated power (EIRP) is $52\,\text{dBm}$ ($158\,\text{W}$) at $10.2\,\text{GHz}$.

3.2 Class–E PA for Spatial Power Combiner

The following material presents the design and characterization of a single class–E PA at $10\,\text{GHz}$. The basic sensitivity analysis of the PA was performed, determining the main contributor to the potential load impedance variations: the antenna element. According to the results of the analysis an

appropriate broadband antenna element was designed. After the characterization of an active antenna element, a corporate feed network was designed and finally the entire passive and active spatial combiner was fabricated and characterized.

3.2.1 Class–E PA Design

For the design of a class-E PA for a 10 GHz spatial combiner, a general purpose depletion–mode GaAs MESFET chip transistor fabricated by Alpha Industries, Inc. was selected. While operating in class–A the AFM04P2 MESFET, shown in Fig. 3.3(a) has the following properties:
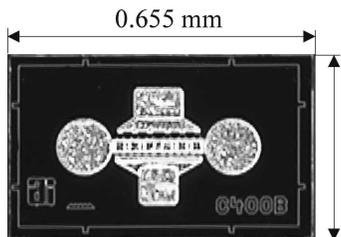
$f\,[GHz]$	$f_T\,[\mathrm{GHz}]$	$f_{MAX}\,[\mathrm{GHz}]$	$G\,[\mathrm{dB}]$
DC-40	30	60	9
$P_{1dB}\,[\mathrm{mW}]$	$V_{DS-MAX}\,[\mathrm{V}]$	$I_{D-MAX}\,[\mathrm{mA}]$	
126	6	140	

(a) (b)

Figure 3.3: (a) General–purpose millimeter-wave power GaAs MESFET AFM042P (Alpha Industries, Inc.) used for class–E PA design. The transistor is 0.1 mm thick. (b) Typical characteristics of the used MESFET: f - frequency of operation, f_T - cutoff frequency, f_{MAX} - maximal frequency of oscillation, P_{1dB} - output power at 1 dB compression point, measured at 18 GHz, G - power gain at 18 GHz, V_{DS-MAX} - maximal drain voltage, I_{D-MAX} - maximal drain current.

A simplified version of the parameter extraction method described in

Appendix A was used. From the given S-parameters measured at a class–A bias point ($V_{DS} = 5\,\text{V}$ and $I_{DQ} = 70\,\text{mA}$) at $10\,\text{GHz}$, with included bond–wires, the small–signal model parameters are determined. The extracted output capacitance of the MESFET is $C_{OUT} = 0.11\,\text{pF}$. This corresponds to the example used in Subsection 1.3.5 to illustrate class–E PA dimensioning, and the rest of the calculated parameters required for class–E PA design were summarized in Table 1.2.

The reverse transmission coefficient of the MESFET is small ($|S_{12}| = 0.073$) compared to the forward transmission coefficient ($|S_{21}| = 2.683$), so that the unilateral property can be assumed (forcing $S_{12} = 0$). Therefore, the optimal small–signal matching condition at the input is: $\Gamma_S = S_{11}^*$, with expected postproduction tuning at the input side.

Using a linear microwave circuit simulator (Agilent $ADS^{\circledR}$), narrowband single stub matching networks are designed and shown in Fig. 3.4. A second harmonic "open" termination is provided through a $\lambda/4$ long (at $20\,\text{GHz}$) "open" shunt stub with additional $\lambda/4$ series line ($TL1$ and $TL10$). Fundamental frequency matching to optimal class–E impedance (at $10\,\text{GHz}$) is achieved through second "open" shunt stub ($TL6$). The input matching was performed using a single series–"open" shunt stub configuration ($TL7$ and $TL4$).

The drain bias voltage is provided through a high–impedance $\lambda/4$ long transmission line $TL5$, terminated at $10\,\text{GHz}$ and $20\,\text{GHz}$ with two optimized radial stubs. Additional lower frequency RF decoupling is provided through
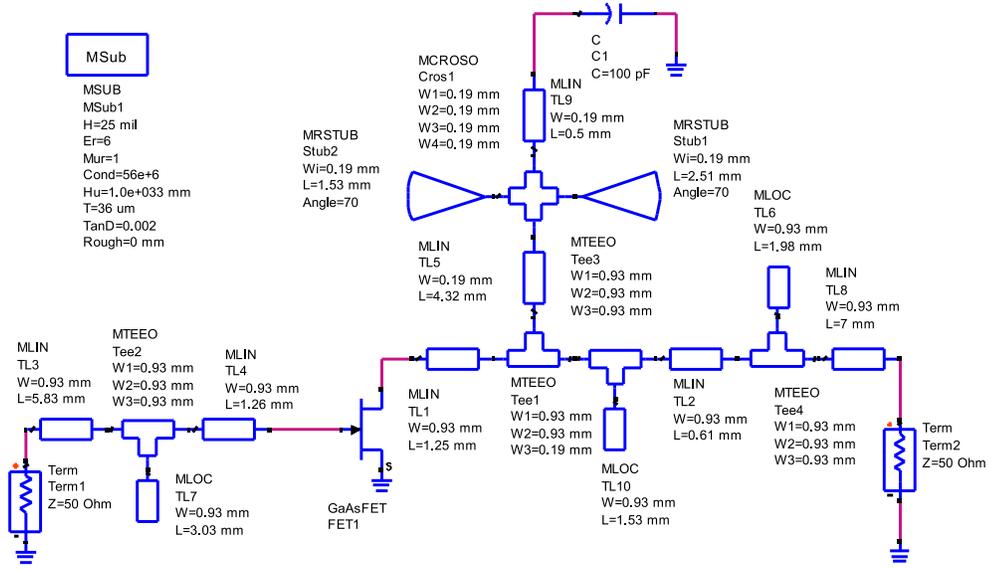
Figure 3.4: Schematic of the class–E microwave PA designed a for spatial power combiner. The drain bias line is included, while the gate bias is provided through an external bias–tee.

a 100 pF millimeter-wave shunt capacitor $C1$. This configuration of the bias network minimally affects the optimal load impedances at the fundamental and the second harmonic. At the same time, it prevents an unwanted leakage of RF power through the bias lines that could potentially cause amplifier instability. Additional RF decoupling is provided by winding the bias supply wire on a series of ferrite core beads. The gate bias is provided through an external commercial bias–tee (not shown in Fig. 3.4).

The PA was fabricated on 0.635 mm thick Rogers $TMM6^{®}$ substrate ($\epsilon_r = 6, \tan\delta = 0.0018$). This is a low–loss thermally stable substrate, slightly brittle, but with excellent machining properties, and is suitable for patterning
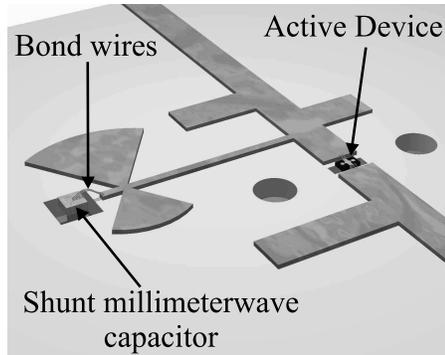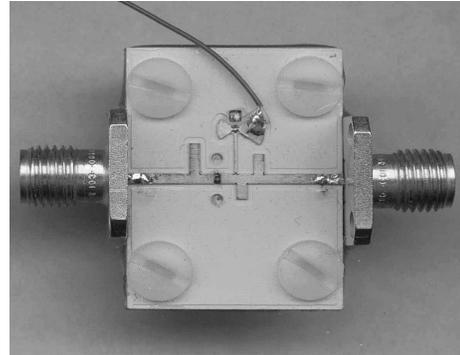
Figure 3.5: (a) Active device mounting method for class–E microwave PA. (b) Photograph of the fabricated class–E PA.

on a prototyping milling machine.

Mounting of the active device in a microstrip circuit (Fig. 3.5(a)) is a challenging task, due to the very small chip size (Fig. 3.3(a)). First, the thickness difference between the transistor and the substrate is overcome using a micro-machined cylindrical copper post, mounted on the common RF ground plane through a substrate hole. Then, the active device is mounted using silver epoxy on the copper post and aligned with the microstrip lines of the matching networks. A similar post is used for mounting of the shunt capacitors in the bias network. The active device and the capacitor are bonded to the matching network using two gold bond–wires per electrode, in order to replicate as closely as possible the environment in which the transistor's S–parameters are measured.

3.2.2   Class–E PA Characterization
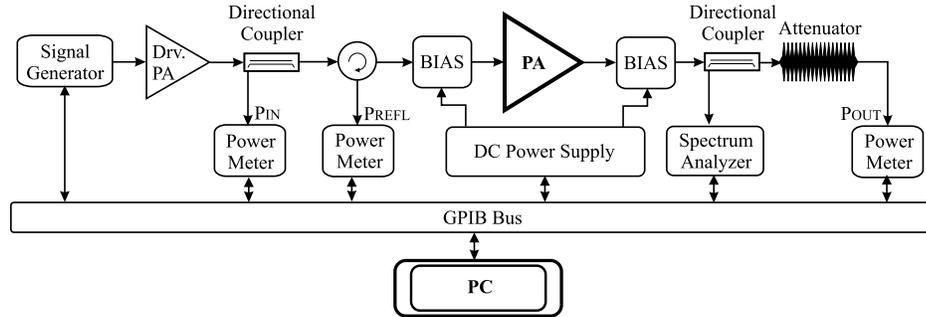
Figure 3.6: Schematic of the measurement setup used for automated class–E PA characterization. The signal generator provides a variety of required signals for PA characterization. All components of the system are controlled using a personal computer equipped with a GPIB card.

(a)   (b)
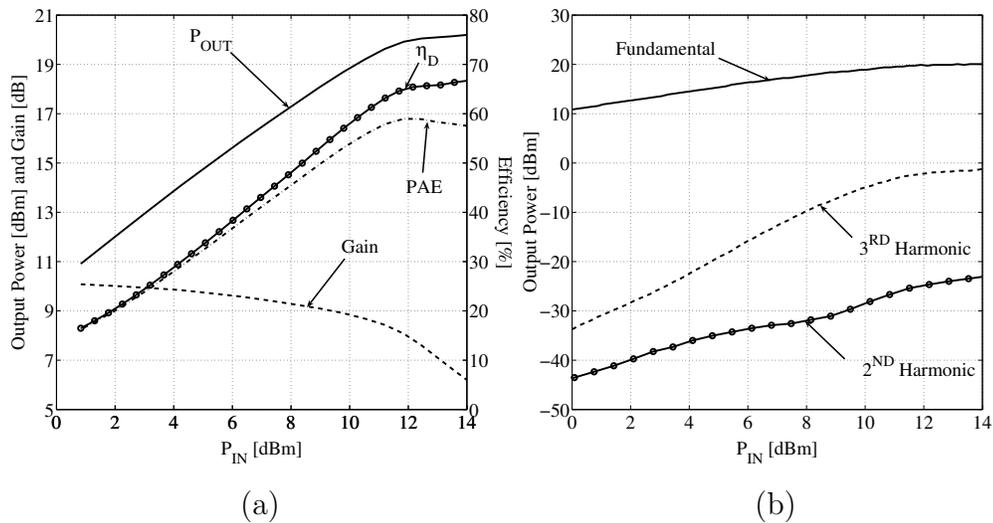
Figure 3.7: (a) Measured characteristics of the class–E PA at $10\,\text{GHz}$. Optimal bias point is found to be $V_{DS} = 4.2\,\text{V}$, and $V_{GS} = -1.4\,\text{V}$. (b) Measured second and third harmonic at the output of the PA. Significant suppression of the second harmonic is a consequence of the "open" termination.

The fabricated class–E PA was tested in a measurement setup shown in Fig. 3.6. In the postproduction tuning the second shunt stub in the output matching network was slightly changed, compensating for bond wire inductances and the transistor mounting parasitics. The optimal bias point is then found using a systematic search. Measured power–sweep characteristics of a typical PA referenced to SMA connectors are shown in Fig. 3.7.

(a)   (b)
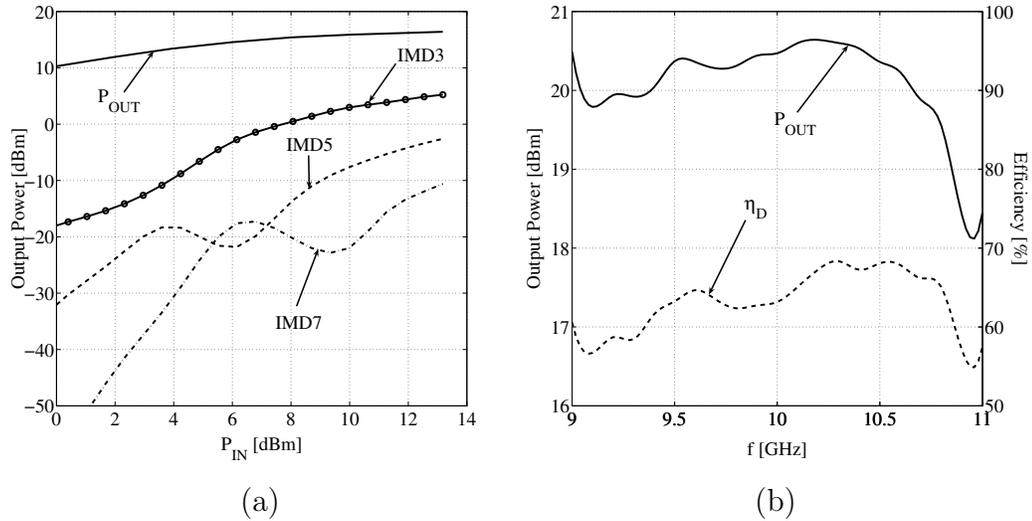
Figure 3.8: (a) Measured intermodulation products of the designed PA, for the two–tone input signal with $100\,\mathrm{kHz}$ spacing. (b) Frequency dependence of the PAs maximal P_{OUT} and η_D.

A considerable number of PAs were fabricated and consistency in the required tuning is observed. Several of the designed PAs achieved drain efficiencies above 72%, with output powers up to 20.7 dBm, which is contributed to the extremely high quality of the devices from the available semiconductor wafer (mainly lower parasitic resistances).

3.2.3   Class–E PA Sensitivity Analysis

In order to achieve high spatial combiner performances (i.e. PCE, effective isotropic radiated power (EIRP), overall efficiency, etc.) it is important to obtain uniform operation of all involved active elements. This is a difficult task due to the finite fabrication/mounting tolerances of such a complex structure and fabrication differences between individual active devices. Basic microwave class–E PA theory presented in Chapter 1 provides a single target impedance for achieving an ideal efficiency. However, it does not predict the behavior of such an amplifier upon the load impedance variations at the fundamental and the harmonic frequencies. What follows is a study of the sensitivity of a class–E PA performances to load impedance variations.

The active device fabrication tolerances are generally small, provided that all of the active devices used for the combiner design are coming from the same wafer. This property was experimentally verified for the given GaAs MESFET. After attempting different mounting approaches, the one that was finally adopted (Fig. 3.5(a)) has shown to be a very reproducible (transistor height and centering, bond wire length and shape can be precisely controlled, especially if all of the transistors are mounted in the same time). Therefore, this study is focused on the variations in the output matching network and an antenna element attached to it.

A general study of circuit variations on a class–E PA performances was performed by Raab [46]. It was done at low frequency, assuming that the

transistor behaves as an ideal switch, while the elements of the external circuit can vary. In the microwave frequency range, such simplified analysis is not applicable mainly because of the complexity of the nonlinear phenomena that occur in microwave active devices and the numerous included parasitics.
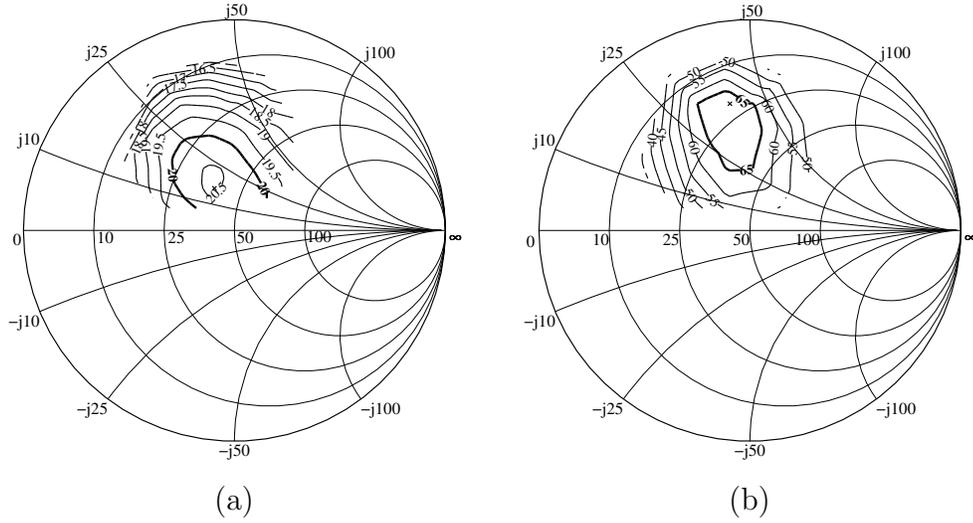
Figure 3.9: Simulated impedance contours of the constant P_{OUT} (a) and the constant η_D for the designed class–E PA (b). The contours are shown for constant $P_{IN} = 12\,\text{dBm}$.

In this work a commercial harmonic balance simulator is used to emulate a variable impedance environment. A nonlinear model for the selected GaAs MESFET (TOM2, developed by Triquint Semiconductor, Inc.) is slightly modified to achieve better agreement between measurement and simulation at power levels of interest, where the active device operates deeper in compression.

First, the load impedance of the active device is systematically varied and

simulated input power sweeps are performed for each of the impedance points. Higher harmonic terminations are kept ideal and the source impedance constant. The degradation of the main PA characteristics (i.e. P_{OUT}, gain and η_D) with deviation of the load impedance from the optimal one is shown in Fig. 3.9 in form of the constant P_{OUT}, and η_D contours.

As can be observed, PA characteristics are not extremely sensitive to the variations in the load impedance, which can be contributed to the specific active device output voltage and current shapes [2, 46]. The effects of small second harmonic termination variation on the fundamental impedance load–pull contours are generally small and are not considered here.

The next step is to determine the effect of expected fabrication variations of the output matching circuit and input impedance of an antenna element Z_L on the transistor's load impedance Z_{OUT}, Fig. 3.10.
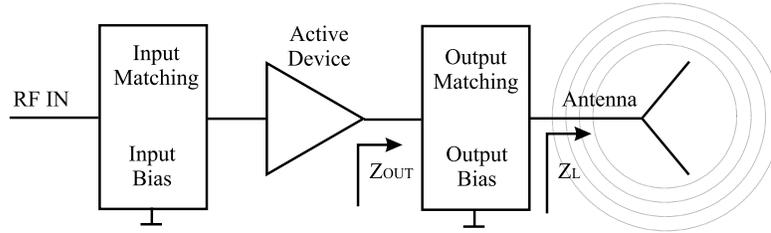
Figure 3.10: Schematic of the class–E PA integrated with an antenna element. The variations of matching network line dimensions are first analyzed assuming that Z_L is constant. Then, variations in the antenna geometry are considered.

Modern microwave substrate materials exhibit uniform dielectric constant as well the substrate thickness (all active antenna array elements, if possible,

should be fabricated on the same substrate board). Therefore, in the case of an entirely distributed matching network the main fabrication deviation is in the microstrip line and antenna dimensions.

(a)   (b)
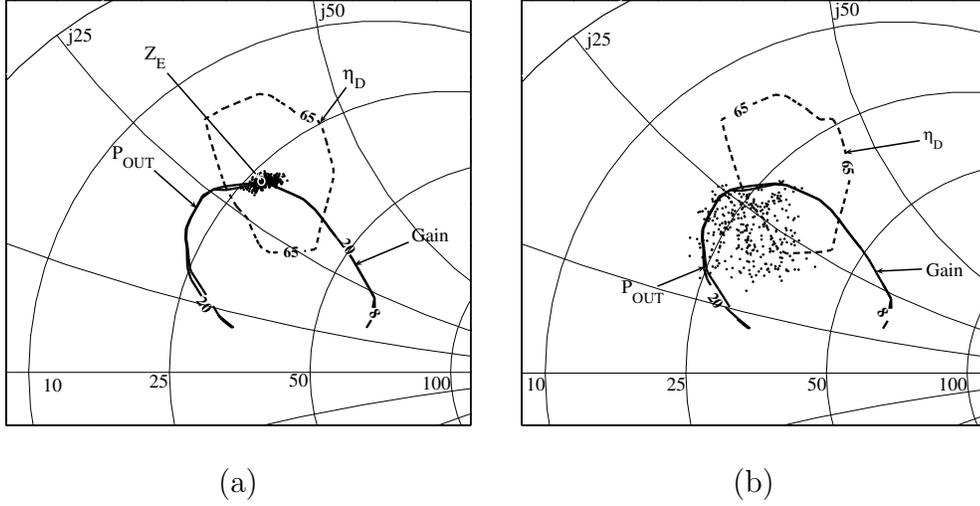
Figure 3.11: PA load impedance spreading due to the $\pm 50 \mu$m dimension variations in the output matching network with the constant antenna impedance (a) and with the antenna impedance variations (b).

For obtaining the impedance variations a statistical analysis is performed using Agilent $ADS^{®}$ simulator combined with MoM full–wave simulator (Agilent $Momentum^{®}$). Typical dimension tolerances of a laboratory prototyping PCB milling machine are $\pm 50 \mu$m. Assuming uniform probability distribution the expected spreading of the load impedances due to the variations in the output matching network only is shown in Fig. 3.11(a). Shown are contours for constant $P_{OUT} = 20 \, \text{dBm}$, $G = 8 \, \text{dB}$ and $\eta_D = 60\%$. The spreading of the load impedances is within the selected boundaries, Fig. 3.11(a).
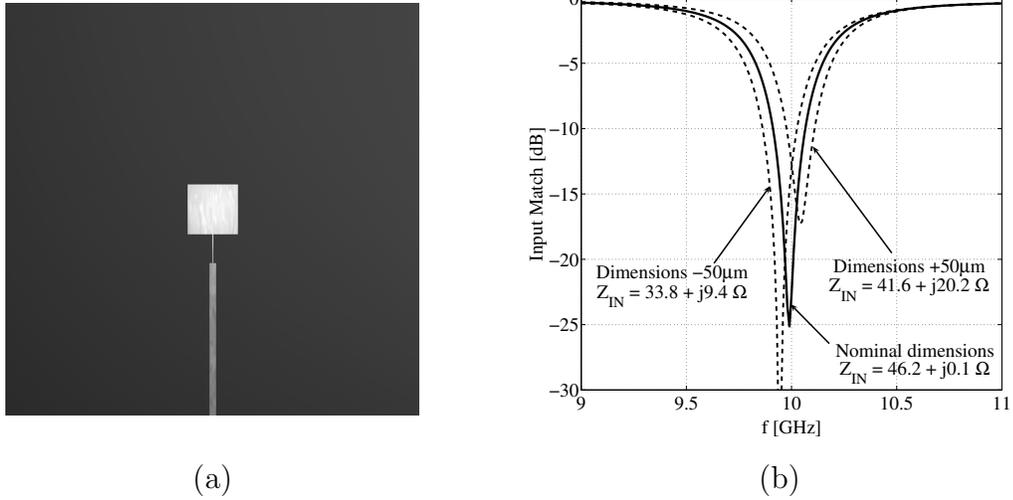
Figure 3.12: (a) Typical radiating side–fed X–band single layer patch antenna (9.69 mm x 9.69 mm with 0.2 mm x 5.49 mm wide impedance transformer). (b) The input return loss of the antenna with allowed $\pm 50 \mu$m dimension variations.

However, if a single layer microstrip patch antenna (Fig. 3.12(a)) is used instead of a constant 50-Ω load, the spreading of imedances becomes more significant (Fig. 3.11(b)). This is mainly due to a very narrow bandwidth of the patch antenna's input return loss: even small dimension variation leads to the shift in the antenna resonant frequency, which is followed by considerable impedance deviation from the initial value, as shown in Fig. 3.12(b).

From the given analysis it can be concluded that the main sources of load impedance uncertainty are the accuracy of the matching networks and the antenna element fabrication. In order to assure successful design of a high performance PA for spatial power combiner, the following guidelines are inferred:

(1) All active devices used for the array design should originate from the same wafer if possible;

(2) Device mounting height and position on the mounting stub need to be controlled. Bond wires with the same length, width and shape need to be used;

(3) In order to minimize deviation of the load impedance due to the matching network fabrication, the milling machine should be calibrated prior to use, with the typical line tolerances decreased to $\pm 10 \mu$m. An alternative is the use of a more expensive photo-lithographic process;

(4) A more broadband antenna element should be developed, in order to decrease sensitivity of the load impedance to the antenna fabrication variations.

3.3   16–Element Active Antenna Array Design

3.3.1   Broadband Active Antenna Element

Ordinary patch antenna shown in Fig. 3.12 suffers from high sensitivity of its resonant frequency to the parameter variations, as shown in Subsection 3.2.3, significantly affecting the load impedance presented to the active device. In order to achieve low side–lobe radiation from the array the antenna elements

need to be closely spaced (as close as possible to $\lambda/2$) [47]. This becomes difficult to satisfy if any kind of microstrip impedance transformer is used. Some other configurations of the antenna elements, such as inset–feed patch, or antenna with asymmetrically positioned feed at the radiating edge [48, 49, 50], can be used. However, the first one introduces fabrication difficulties at these frequencies, while the other affects the radiation pattern. Both of them are still highly sensitive to the fabrication tolerances.

A good alternative that was considered is a slot–coupled patch antenna [47, 38]. An open microstrip line couples EM energy to antenna element through the slot in the ground plane. An antenna with this structure would have a frequency bandwidth of more than 10%, therefore decreasing the sensitivity to the variations of the input impedance. A slot–fed patch antenna was designed, fabricated and characterized, showing expected frequency bandwidth and excellent radiation pattern over the frequency range. Although the designed element solves both of the mentioned problems, it was abandoned due to the bidirectional radiation of a slot in the ground plane. The unwanted radiation of the slot can be potentially coupled to the feeding network and can cause antenna array instabilites.

As an element of choice, a dual layer stacked–patch antenna is selected [51] and optimized for linear polarization at $10\,\mathrm{GHz}$, Fig. 3.13. The antenna consists of two patch elements, fabricated on two layers of low–cost Rogers *Ultralam 2000*® substrate ($\epsilon_r = 2.43, \tan\delta = 0.002$, thickness $0.508\,\mathrm{mm}$). The main patch is attached to the feed line through substrate vias, isolated

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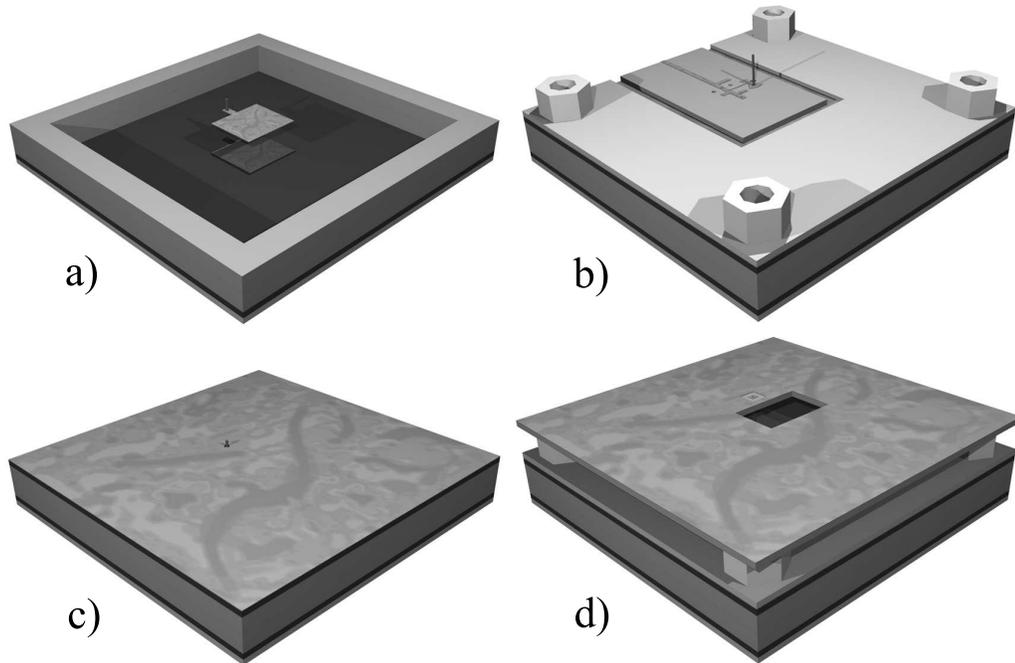
Figure 3.13: Single stacked patch antenna assembly. Inverted parasitic and main patch are separated by air, using FR4 frames (a). The main patch is connected with the active feed (PA output), using a set of ground planes vias (b). The active feed is placed on the opposite side of the ground plane (c) and connected to the DC biasing and a protective FR4 layer (d).

from the common ground plane. The common ground plane separates the radiating elements from the active feeding network, where the previously designed class–E PA is placed. This configuration prevents possible coupling between the active feed and the radiating elements, insuring the stability of the active array. The parasitic patch is inverted, radiating through its substrate. This substrate serves as a radome, enclosing and protecting the antenna elements. The dielectric between the active and parasitic patch is

air. The spacing between elements is set by FR4 spacer frames.

The antenna is designed using the Agilent *Momentum®*, a MoM software package. By optimizing the dimensions of both main and parasitic patch antenna as well as the spacing between them, a 50-Ω input impedance is achieved at the edge of the main antenna element, eliminating the need for a matching circuit.
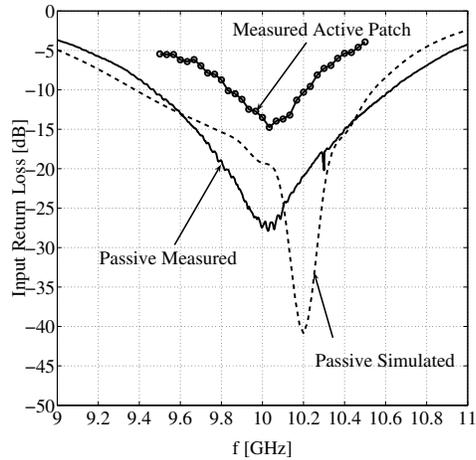
Figure 3.14: Simulated (dashed) and measured (solid) input return loss of the passive antenna element. Measured (circles) small–signal input return loss of the active antenna element.

Simulated and measured input return loss of the passive and active antenna element are shown in Fig. 3.14. Simulated and measured principal planes radiation patterns of the passive antenna element are shown in Fig. 3.15.

Measured radiation patterns of the active antenna element are very similar to the passive antenna ones. The designed patch antenna has a radiation
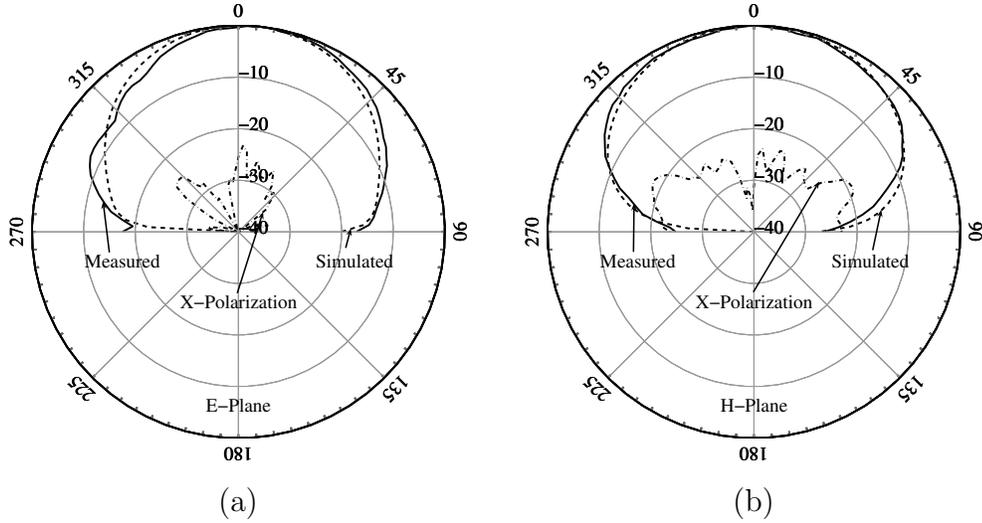
Figure 3.15: Measured and simulated E–plane (a) and H–plane (b) radiation patterns. Cross–polarization patterns are shown in black.

gain of 7.4 dBi and a back radiation level 15 dB below the maximal front radiation. The 2:1 VSWR frequency bandwidth of the antenna is 11.6% and the input return loss at 10 GHz is better than -27 dB. Using the radiation gain of a passive antenna element, performances of the PA in the active element are determined and summarized in Table 3.1.

Table 3.1: Measured 10-GHz active antenna performances

P_{OUT} [dBm]	G [dB]	η_D[%]	PAE[%]	V_{DD} [V]	I_D [mA]
19.8	7	61.4	49.1	4.2	37.8

P_{OUT} - power delivered to the antenna, G - power gain, η_D - drain efficiency, PAE - power added efficiency, V_{DD} - drain supply voltage, I_D - average drain current

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3.3.2 Active Antenna Array Design

For the input power distribution among the antenna elements, a 16-way divider is constructed using a Wilkinson divider as the main building block. Such a configuration provides uniform amplitude and phase distribution of the input signals as well as good isolation between amplifiers. A single 2-way divider is shown in Fig. 3.16(a).
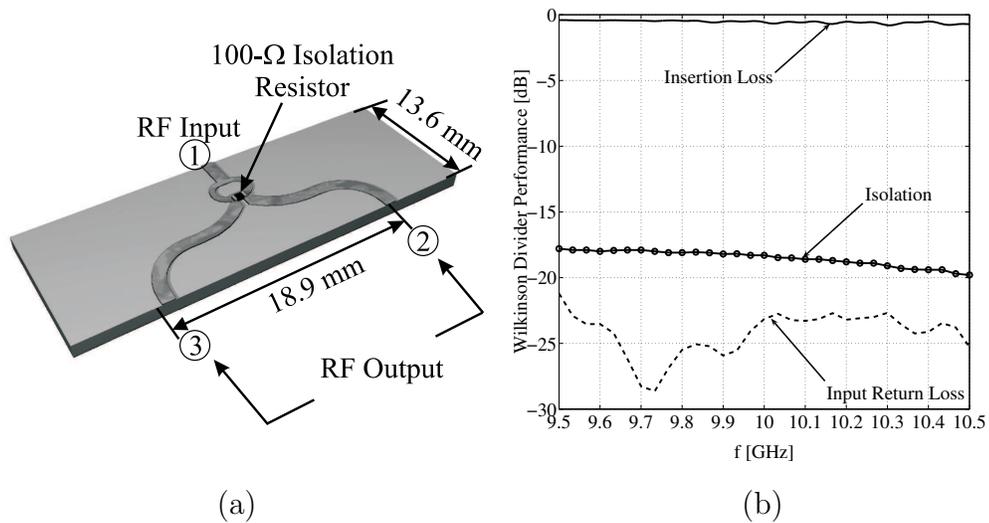
Figure 3.16: (a) Wilkinson divider used for 16–way power distribution. It is fabricated on Rogers *TMM6*® substrate. For the isolation between the output ports millimeter-wave thin–film resistors of $100\Omega/80$ mW were used. (b) Measured insertion loss (solid), return loss (dashed) and isolation of the designed Wilkinson divider (circles).

The measured frequency response of the divider is shown in Fig. 3.16(b). At 10 GHz, the divider has an insertion loss of 0.3 dB (calibrated at the SMA connectors), with isolation between ports better than 18 dB and the input

return loss better than -23 dB.

Using the main building blocks described in the previous sections - a class–E PA, broadband patch antenna and the 2–way low–loss Wilkinson divider, a 16–element active antenna array was designed. The array assembly is shown in Fig. 3.17. The spacing between antenna elements within the array is $0.6\lambda_0$ (18 mm). The overall size of the array is $116\,\text{mm}^2$. Details of the active feed are shown in Fig. 3.18(b).
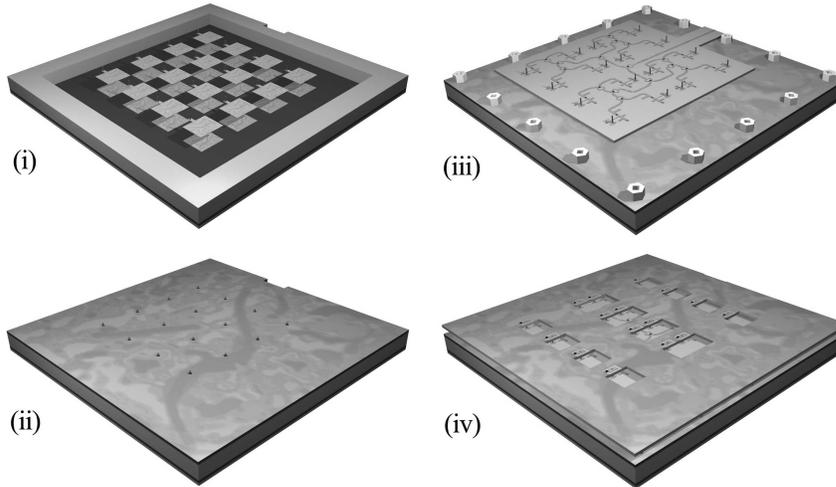
Figure 3.17: 16–element active antenna assembly. The parasitic and main patch arrays are separated by air, using FR4 frames (1). The main patch array is connected with the active feed, using set of ground planes vias (2). The active feed is placed on the opposite side of the ground plane (3) and connected with to the DC biasing and protecting FR4 layer (4).

Full–wave simulations of a passive sub–array showed the expected relative insensitivity of the antenna performances on dimension and alignment variations. The coupling between elements is analyzed as well using MoM. It
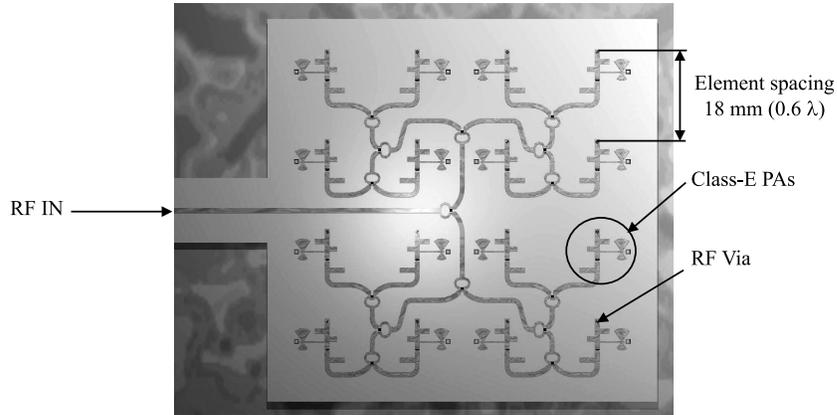
Figure 3.18: Details of the 16-element active feed. Feed size is 78 mm x 76 mm

remains below -35 dB between any adjacent antenna element. This property insures that the load impedance seen by a PA in a single active element will remain unchanged when such an element is placed into an antenna array.

Most of the array components are fabricated on a prototyping milling machine (LPKF *Protomat 93s*®). In order to maintain a uniform dielectric thickness of the fabricated substrates the antenna elements are only outlined using the milling machine. The rest of the copper is chemically etched. Alignment between antenna layers was performed through precisely drilled guiding holes using metal stubs that are removed after assembly. A photograph of the front and back side of the active array is shown in Fig. 3.19.

The antenna array is mechanically robust: its structure is very compact and reinforced using FR4 frames, while the substrate of the inverted parasitic array again serves as a radome. The active feed is protected by the DC supply layer, which in addition solves the problem of the DC bias voltage
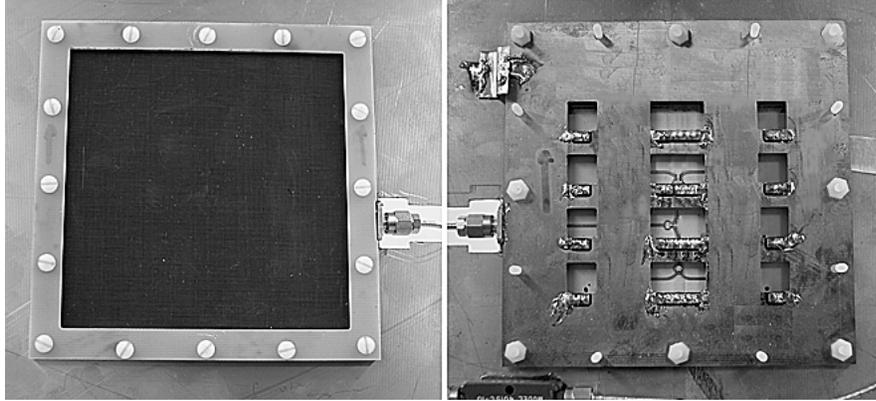
Figure 3.19: Photograph of the fabricated 16–element active antenna array, front side (left) and the back side (right).

taper, described in [52]. The gate biasing of the active devices is provided through the feeding network using an external bias-tee.

3.3.3 Characterization of the Active Antenna Array

Characterization of the active antenna array includes the active antenna radiation pattern measurements, combined with monitoring of input and DC power consumption. Of particular interest is determination of the drain efficiency of the class–E PAs within the array. Since the output ports of the PAs are not accessible, their output power has to be determined indirectly. If the radiation efficiency of the antenna is known, then in principle it is possible to determine the power delivered by PAs from the measured total radiated power [47]. However, both of these parameters are quite difficult to obtain.

In this work a comparative approach was used. First, a passive antenna array with the same geometry as the active one (with amplifiers replaced by 50-Ω "thru"–lines) is fabricated. Its radiation gain is determined using the anechoic chamber setup shown in Fig. 3.20.
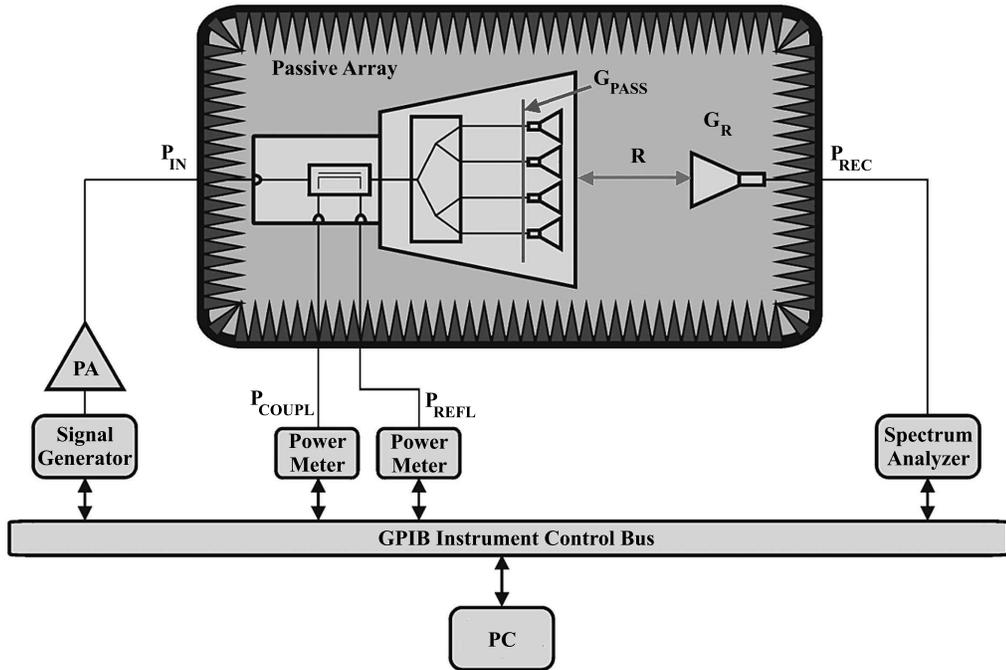
Figure 3.20: Anechoic chamber setup for passive antenna array measurement. The far-field distance between the array and the receiving horn is R. Gain of the receiving horn antenna is G_R. The input power is determined from measured P_{COUPL} and the known coupling coefficient of the directional coupler. The received power P_{REC} is measured with the spectrum analyzer.

The insertion loss of the feeding network is determined from a VNA measurement of the two back–to–back connected passive 16–way Wilkinson com-

biners, allowing radiation gain calculation of the antenna–part of the array:

$$G_{PASS} = \left(\frac{4\pi R}{\lambda}\right)^2 \cdot \frac{P_{REC}}{P_{IN}} \cdot \frac{1}{G_R} \cdot \frac{1}{A_F} \tag{3.2}$$

Finally, assuming that the passive and active antenna arrays have the same radiation gain the combined output power of the PAs, P_{OUT}, can be determined, using free–space measurement of the active antenna array (Fig. 3.21) and the Friis formula (Eq. 3.3).
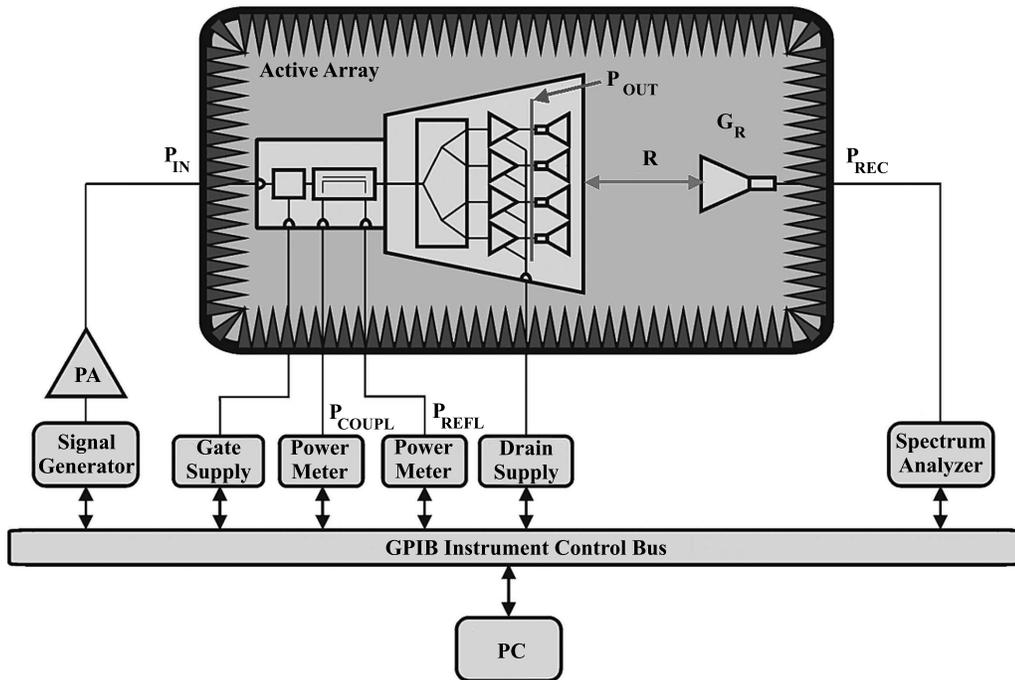
Figure 3.21: Active antenna array measurement setup. Gate bias is provided through RF feed using an external bias–tee (BT).

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$$P_{OUT} = \left(\frac{4\pi R}{\lambda}\right)^2 \cdot P_{REC} \cdot \frac{1}{G_R} \cdot \frac{1}{G_{PASS}} \qquad (3.3)$$

Although designed for 10 GHz, the optimal performance of the active array is achieved at 10.2 GHz. A possible cause of this are the fabrication tolerances and mutual coupling between antenna elements, resulting in a slight load impedance deviation.
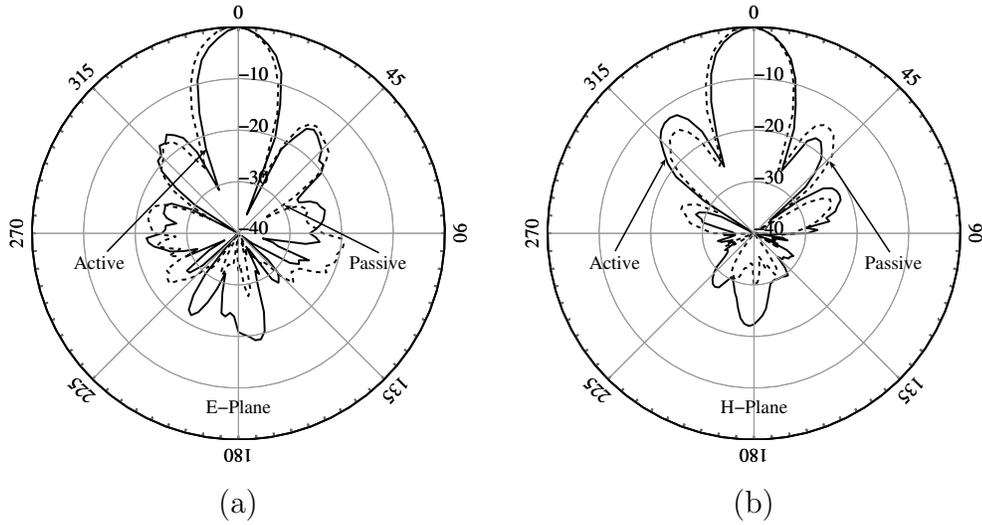
Figure 3.22: Measured E–plane (a) and H–plane (b) 16–element active (solid) and passive (dashed) antenna array radiation patterns at 10.2 GHz.

The measured radiation patterns of the passive and active arrays at 10.2 GHz are shown in Fig. 3.22, justifying the assumption that the radiation gains of the antennas is very similar due to the very uniform operation of all PA elements within the array. Simulations with different element spacing give a radiation gain uncertainty estimate of $\approx \pm 0.25$ dB.
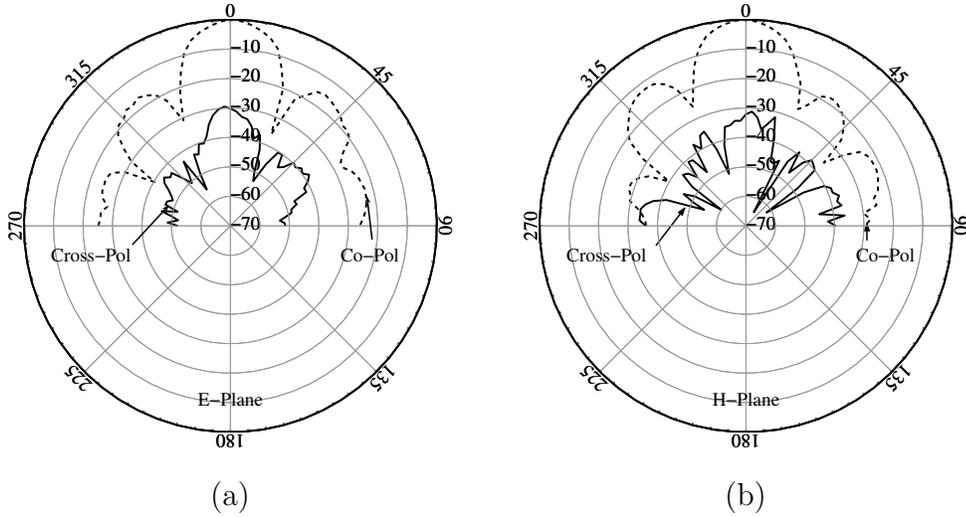
Figure 3.23: Measured E–plane (a) and H–plane (b) 16–element active cross–polarized radiation patterns at 10.2 GHz (solid). The dashed lines are the co–polarized radiation patterns of the active array.

Measured cross–polarized patterns of the 16–element active array are shown in Fig. 3.23. The 2nd and 3rd harmonic radiation patterns are measured and the level of the harmonic power is 45 dB below the broadside fundamental frequency power. The summarized antenna parameters are given in Table 3.2.

Table 3.2: Measured and simulated 10.2–GHz antenna performances of the active array.

G_{ANT} [dBi]	A_F [dB]	η_{RAD}[%]	X_{POL} [dB]	Harm [dB]	ρ_{IN} [dB]
19.8	1.4	90	-30	-45	< -13

G_{ANT} - radiation gain of the passive/active antenna array (feed loss excluded), A_F - feed insertion loss, η_{RAD} - simulated radiation efficiency, X_{POL} - cross–polarized radiation level, Harm - second and third harmonic radiation level, ρ_{IN} - input return loss.

After the antenna radiation is determined (the radiation gain), the PA stage of the array is characterized in a setup shown in Fig. 3.21, measuring received power and applying Eq. 3.3. Measured power–sweep characteristics of the amplifier stage are shown in Fig. 3.24(a).
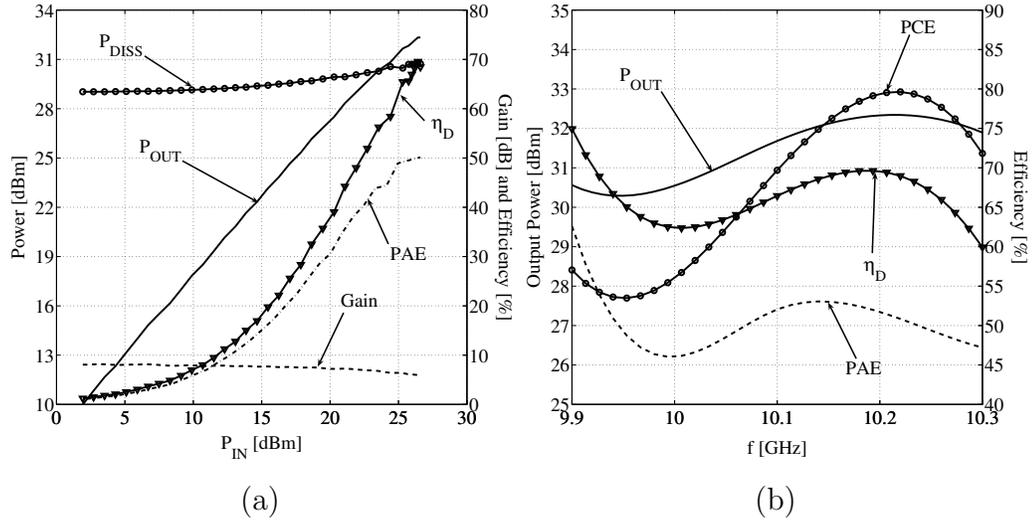
Figure 3.24: (a) Measured power sweep characteristics of the amplifier stage of the 16–element active antenna array at 10.2 GHz. The bias point is at $V_{DS} = 4.2$ V, and $V_{GS} = -1.4$ V. (b) Maximal P_{OUT} (solid), η_D (triangles), PAE (dashed) and PCE (circles).

The average efficiency of the PA stage is very close to the efficiency of the single PA in a circuit configuration, justifying the design approach. The array is further characterized at different operating frequencies. The measured maximal PA output power and PCE are shown in Fig. 3.24(b). Outside the presented frequency range, the discrepancy between passive and active antenna array radiation gain increases, and the accuracy of the output power

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estimation decreases. Summarized performance of the active antenna array is given in Table 3.3.

Table 3.3: Summarized characteristics of the 16–element active array

P_{OUT} [dBm]	G_{AMP} [dB]	η_D [%]	PAE [%]
32.3	5.9	70	52

P_{IN} [dBm]	P_{DC} [dBm]	P_{DISS} [dBm]
28	33.9	32

$EIRP$ [dBm]	P_{RAD} [dBm]	PCE [%]	G_{ARRAY} [dB]	PAE_{ARRAY} [%]
52.1	31.7	79	3.7	34

P_{OUT} - amplifier output power, G_{AMP} - amplifier gain, η_D - average drain efficiency, PAE - average power added efficiency of the active devices, P_{IN} - input power to the array, P_{DC} - DC power, P_{DISS} - total dissipated power in the array, $EIRP$ - effective isotropic radiated power, P_{RAD} - radiated power, G_{ARRAY} - power gain of the entire array and PAE_{ARRAY} - the power added efficiency of the entire array.

3.4   Conclusion

In the previous Sections, the design, fabrication and characterization of an X–band spatial combiner of switched–mode PAs was demonstrated as a unique solution for the heat generation problem at these frequencies. Fig. 3.25 presents a comparison of the power–loss budget with an equivalent array with PAs operating in class–A mode. Multi-fold reduction in the dissipated power is demonstrated.

A robust microwave class–E PA was designed with low sensitivity of op-
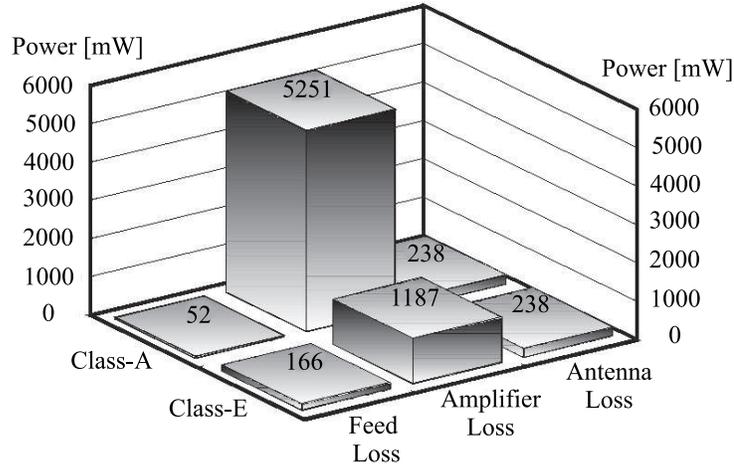
Figure 3.25: Power–loss budget for the 16–element power combiner and a comparable class–A array. The antenna loss is the same for both cases, while the feed loss is slightly higher for the class-E case because the gain of the PAs is lower.

timal load impedance to parameter variations. Additional impedance transformation between the broadband antenna element and the PA is eliminated, enabling efficient real–estate use and reduced EM coupling. The feeding and radiating sides of the array are electromagnetically separated for stability. Uniform signal distribution is provided through a symmetrical 16–way power divider, with isolation between each of the amplifier units. Finally, the problem of a nonuniform biasing is solved by applying a common low–resistance biasing layer for all of the array elements. The designed array exhibits PAs with one of the highest average operating efficiencies achieved at X–band, and an extremely high power combining efficiency of 79%.

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Chapter 4

Load–Pull Based Design Methodology

4.1 Introduction

Designing class–E power amplifiers at microwave frequencies is quite challenging. Nonlinear models that can be used for accurate simulation of the highly nonlinear switched–mode are not available, while existing models can only only provide a starting point for postproduction optimization. It is also difficult to extract internal and external parasitics surrounding the active device (mounting and connecting structures) that influence switched mode operation. The method used in the previous chapters utilized basic class–E theory combined with active device parameter extraction to obtain approximate target impedance for achieving high efficiency operation. The designed

PA had to be experimentally tuned after fabrication in order to compensate for numerous imperfections.

Load–pull is a well known technique used for the design of higher power amplifiers and oscillators. In this work the general load–pull method is applied and augmented with systematic pretuning of the input and output matching networks. Two design examples are presented:

(1) A 60 W ultra–linear PA for standard W-CDMA signals, operating in the 2.11–2.17 GHz range. An experimental uncharacterized LDMOS transistor is subjected to a systematic load–pull characterization on commercial high–power low–frequency commercial load–pull system.

(2) An X–band class–E PA with a commercially available GaAs MESFET transistor (same as the one used in Chapter 3). The load–pull is performed on a low–cost semi–automatic laboratory harmonic load–pull system developed by the author.

4.2   Load–Pull System Description

PA design consists of matching networks design for the determined optimal load and source impedances (Z_S and Z_L). The target impedances optimize PA operation with respect to the output power, gain, linearity, efficiency or more commonly, to the combination of these in some form of compromise. In the case of continuous classes of operation (A, AB, B, C, F) P_{OUT}

is optimized according to the load–line theory [4]. This theory gives an estimate of the optimal Z_L that would provide a maximal V_{OUT} and I_{OUT} swing achievable with the given active device, resulting in a maximal P_{OUT} and efficiency. The transistor's input is usually modeled as an RLC circuit and complex–conjugate matching is then performed in order to achieve optimal gain. Due to the theory simplifications involved, a considerable amount of postproduction tuning is almost always required, especially in the case of high–power low–impedance active devices. Unfortunately, in the case where linearity of the PA is a design parameter, a corresponding simple design theory is not available, especially if a parameter trade–off is required. If an accurate nonlinear model for the device is not available, the only systematic design approach is the use of a load–pull technique.
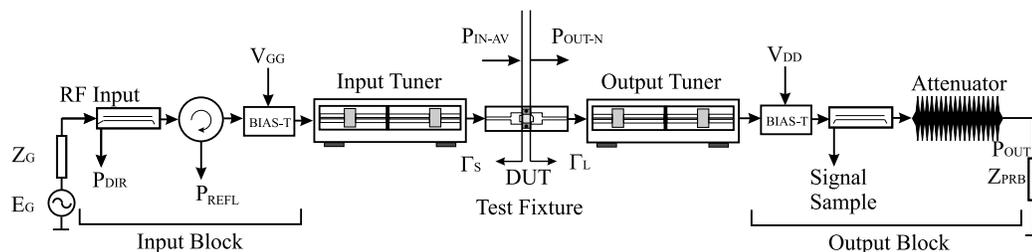
Figure 4.1: Schematic of a typical load–pull system with electromechanical prematched tuners.

A typical load–pull system is shown in Fig. 4.1. It consists of the following parts:

(1) Input block. This includes a directional coupler, circulator and biasing device. Its purpose is to provide biasing to the active device, input power measurement and finally to isolate the DUT from the driver PA. Two power meters are used to measure P_{DIR} at the directly–coupled port of the directional coupler and to monitor the reflected power P_{REFL} at the isolated port of the circulator.

(2) Input and output tuners that provide a set of precisely controlled, known and repeatable impedances. They can be mechanical, electrome-chanical or electronic. Active tuning is also possible [53, 54].

(3) Test fixture. This provides reliable active device mounting. It is a tran-sition between the tuner and input/output block coaxial system into the active device system that can be a microstrip (for packaged de-vices), CPW (for on–wafer measurements, when it includes the probes on a probe station), a waveguide, or a free–space. Often the test fixture performs an additional impedance transformation as well as the biasing of the DUT.

(4) Output block that consists of a directional coupler for signal sampling, an output biasing device and an appropriate attenuating device.

Existing electromechanical tuners are able to produce voltage standing wave ratios (VSWR) in the range between 1:100 at lower RF frequencies (ofter encountered with high power devices) and up to 1:20 in the higher microwave frequency range, with a 360° phase of the reflection coefficient. The high power tuners employ the prematching technique [55]: each of the tuners consists of two independent tuning sections in series. The tuner section closer to the DUT performs initial impedance transformation, selecting a range of interest in Smith chart, while the second stage performs accurate tuning within that range. In addition, an initial transformation of the source and load impedance is performed using a microstrip transformer on the test fixture (Fig. 4.1). Prematching is basically a trade-off between the tuning range and maximal possible VSWR. Special care has to be taken for the out–of–band tuner response. Ideally tuners should have a 50–Ω impedance out of their range of operation, in order to prevent possible DUT instability. Theoretical background for load–pull system calibration and measurement is given in Appendix B.

4.2.1   Pretuning Strategy

After careful load–pull characterization of the DUT, appropriate matching and biasing networks can be designed using a circuit simulator combined with planar EM simulator, in order to accurately model transmission–line discontinuities. Lumped elements of the matching networks (R, L and C) and their parasitics are modeled by different resonant circuits [38, 56]. Parasitics

of the lumped elements, if not provided by the manufacturer, have to be extracted from measurement. In some cases (e.g. high–power extremely low–impedance PAs), instead of the model extraction, a lumped element can be characterized in a specially designed and TRL–calibrated test fixture that replicates the actual position and mounting of the component in the PA [57].

In any case, postproduction tuning has to be expected, mainly due to the finite accuracy of the performed DUT measurements and component tolerances. The main PA performance (gain, P_{OUT} etc.) is monitored while varying the matching networks elements and positions, transmission line stubs length/position etc. This is a common experimental approach in PA design and a source of frustration for the engineer, questioning the entire load–pull approach. Namely, the applied DUT impedances can be so small and highly reactive that tuning becomes extremely difficult due to the finite tuning resolution achievable with variable components. Moreover, microwave active devices are considerably non–unilateral, making simultaneous tuning of input and output matching networks even harder and highly dependent on the engineer's intuition.

Here, a systematic approach is proposed. The PA circuit can be divided in two parts consisting of separate input and output matching/biasing networks. Using a TRL calibration is possible to measure impedance at the DUT reference plane and perform the pretuning of the networks prior to the PA assembling. Moreover, using a circuit/EM simulator it is possible to predict motion of the source and load impedance loci due to the tuning

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elements variations. This information can be used to guide the tuning, significantly decreasing the tuning time. After the input and output matching networks are pre–tuned, the PA can be assembled. In an example of this approach, presented in the Section 4.3, the empirical postproduction tuning is significantly decreased and simplified.

4.3   W–CDMA Base–Station PA
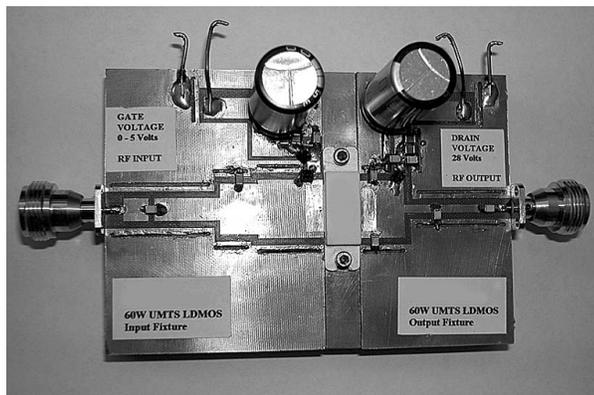
Figure 4.2: Photograph of the assembled 60–W 2.11–2.17 GHz W–CDMA PA.

The first example of the load–pull based PA design approach augmented by the pretuning strategy is the design of a Wideband Code–Division Multiple Access (W–CDMA) base station PA, operating at the 2.11-2.17 GHz range. An experimental uncharacterized LDMOS transistor with some internal prematching is used. The expected output power is 70 W (CW) with gain of 12 dB. The transistor operates at 28 V drain supply, with maximal drain

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voltage of 66 V and maximal drain current of 11 A. The high power transistor consists of two 42–parallel finger cells, resulting in a very low input and output impedances (increased to $\approx 3\Omega$–level after the internal matching).

The critical design parameter is linearity. W–CDMA base–station PA has to handle a complex QPSK modulated signal. The modulated carrier is generated by an I/Q modulator driven by a direct–sequence spread–spectrum multiplexed data channels (DS–CDMA) with a chipping rate of 3.84 MHz. An RF channel is therefore 3.84 MHz wide and consists of sixteen independent data channels modulating a single RF carrier. The test signal used for the measurement is a standard 3GPP Test Model 1, 16 Dedicated Physical Channels (DPCH) with 10 dB peak-to-average ratio, at 0.01% Complementary Cumulative Distribution Function (CCDF) [58], provided by an Agilent E4437B ESG–DP Series Signal Generator.

Due to the high linearity requirements and large signal peak–to–average ratio a power back-off by approximately 10 dB is expected. The linearity is characterized through the adjacent channel power ratio (ACPR), with the requirement of ACPR$\leq$ 45 dBc for the first adjacent channel (at ± 5 MHz from the channel center). The ACPR is measured using an Agilent E4406 VSA Series Transmitter Tester. The used test and measurement equipment including automatic high–power load–pull system is property of dBm Engineering, Boulder, CO.
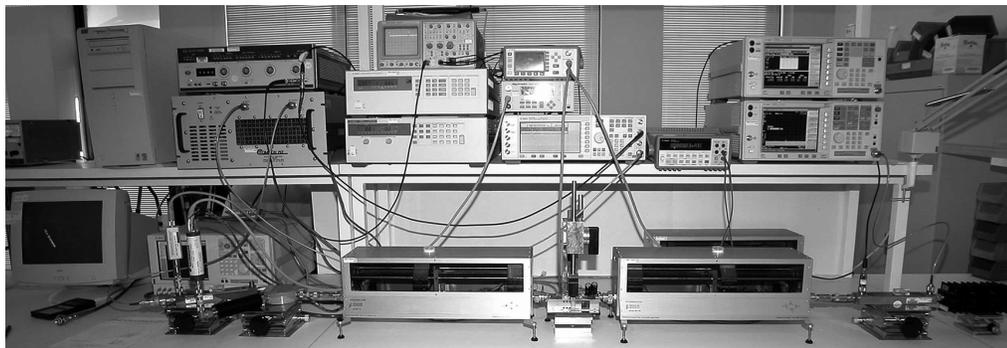
Figure 4.3: The commercial electromechanical load–pull system (Focus Microwaves) used for the DUT characterization. High–power tuners (bottom row) are with the prematching sections. Additional impedance transformation as well as the biasing is performed on the DUT test fixture. W–CDMA signal generator, DC power supplies, spectrum and signal analyzer are installed above the tuners (dBm Engineering, Boulder, CO).

4.3.1 Active Device Characterization

A commercial load–pull system with multiple prematching sections Fig. 4.3 is set up to measure ACPR for each of the load and source impedance points. For each of the selected impedances the input power is swept and the corresponding gain, P_{OUT}, efficiency and ACPR are measured. The output power and gain contours for constant ACPR=-45 dBc are shown in Fig. 4.4 and Fig. 4.5. Selected target impedances are the result of a compromise between P_{OUT} and gain. The optimal quiescent drain current is 700 mA with the gate bias voltage of 4.1 V, providing the flat gain vs. P_{OUT} characteristic.

Figure 4.4: Measured source (left) and load (right) impedance contours of the constant output power (dashed) and gain (solid) for the ACPR=-45 dBc at 2.11 GHz. 50–Ω charts are shown as insets for easier orientation. Impedances for the maximum output power (x) and maximum gain (+) are also shown. Selected target impedances (black circle) are : $Z_S = (8.5 + j0)\,\Omega$ and $Z_L = (1.5 - j3.25)\,\Omega$ at 2.11 GHz.

Figure 4.5: Measured source (left) and load (right) impedance contours of the constant output power (dashed) and gain (solid) for the ACPR=-45 dBc at 2.17 GHz (a) and at 2.17 GHz. Impedances for the maximum output power (x) and maximum gain (+) are also shown. Selected target impedances (black circle) are $Z_S = (7 + j0)\,\Omega$ and $Z_L = (1.5 - 3.0)\,\Omega$ at 2.17 GHz.

4.3.2   PA Design

Microstrip stepped–impedance transformers with shunt lumped capacitors are used for the impedance transformation.

Figure 4.6: Schematic of the W-CDMA power amplifier. The microwave Arlon substrate has $\epsilon_r = 2.5$ and is 0.787-mm thick. The parasitic inductance of the capacitors is 1 nH and the effective series resistance (R_S) is 100 mΩ. The biasing networks perform RF decoupling and transistor stabilization.

Table 4.1: W-CDMA PA distributed matching network dimensions.

	L1, L12	L2	L3	L4, L5
w [mm]	2.16	6.02	6.02	13.72
l [mm]	3.81	6.35	17.27	5.06

	L6, L7	L8	L9	L10	L11
w [mm]	15.75	15.75	15.75	2.16	2.16
l [mm]	6.02	3.81	8.64	8.89	13.97

w - microstrip line width, l - line length

DC supply voltages are provided through the lumped high–impedance bias lines, with resistive gate loading (in order to achieve low–frequency stability of the PA). The schematic is shown in Fig. 4.6. Each of the lumped

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elements (capacitors) is modeled as a series RLC circuit using the manufacturer's data. The microstip step–discontinuities are modeled using a method of moments code (Agilent *Momentum*®) and incorporated with (Agilent *ADS*®) circuit simulator. Microstrip stepped–transformer dimensions are given in Table 4.3.2.

4.3.3 PA Pretuning

(a)   (b)
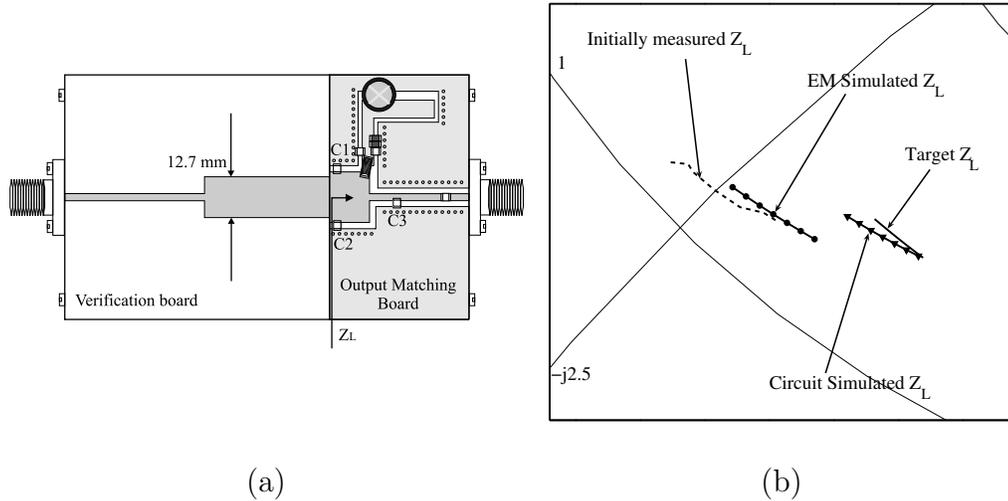
Figure 4.7: (a) Schematic of the verification board attached to the amplifiers output half-board, used for tuning. The Z_L arrow shows the position of the reference plane set for the load impedance measurement. (b) Measured initial output matching network response (dashed) for 2.11–2.17 GHz frequency range is compared to the response of the matching network with circuit (triangles) and EM (circles) modeled step–discontinuities. The target impedances are also shown (solid).

The matching network pretuning was performed separately, using the

individual input and output PA parts. A microstrip verification board is deembedded using a TRL calibration and applied to determine impedances presented at the DUT reference plane. It is designed to match the transistor lead width (12.7 mm). A schematic of the verification board attached to the output PA half–board is shown in Fig. 4.7(a). Compared responses of the output matching network are shown in Fig. 4.7(b). It reveals the importance of EM modeling of the distributed PA matching network components.

During the pretuning the initial impedance locus is aligned as much as possible with the target impedance locus. This is done in a systematic way, using the simulated response of the matching network to the shunt capacitance variation, as shown in Fig. 4.8. Final response of the pretuned matching networks is shown in Fig. 4.9. The assembled PA is shown in Fig. 4.2.
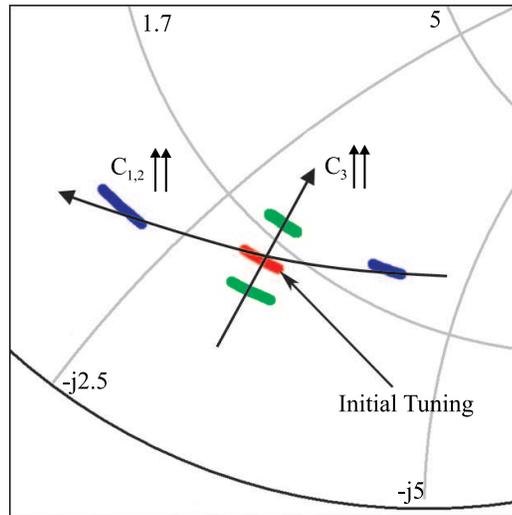
Figure 4.8: Pretuning guidance using simulated behavior of the output matching response to the variation in shunt capacitors values.
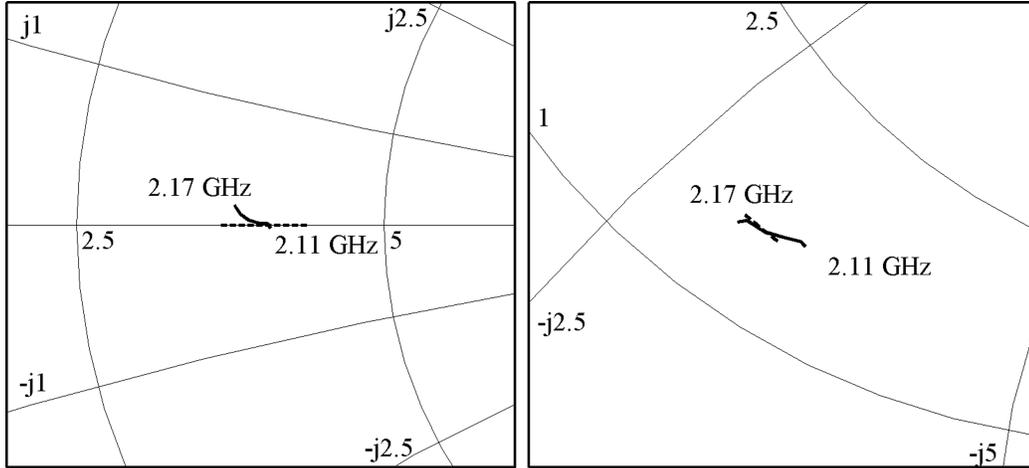
Figure 4.9: Pretuned input (left) and output (right) matching network response (solid) compared to the load–pull determined targets (dashed).

4.3.4 PA Characterization
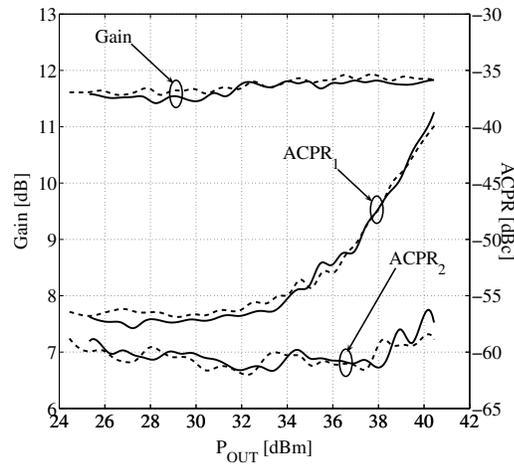
Figure 4.10: Measured gain and ACPR in the first two adjacent channels, 5 MHz (APR1) and 10 MHz (ACPR2) from the working channel. Power-sweep characteristics are shown at 2.11 GHz (solid) and at 2.17 GHz (dashed).

Measured characteristics of the PA are shown in Fig. 4.10. A minimal

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amount of postproduction tuning was performed by slightly adjusting the position of the output shunt capacitors in order to improve the gain and output power flatness over the operating frequency range.

4.3.5 Conclusion

The method described in this section is general and it was commercially used to successfully design a large number of PAs in the range between 800 MHz and 3.5 GHz, for powers up to 300W, for CW, pulsed and wireless modulations [57]. In addition, a harmonic characterization of the same LDMOS was performed, with the intent to improve the PA efficiency. Commercial second and third harmonic tuners were used. However, no effects on the efficiency were observed even with a constant envelope signal and highly compressed DUT. The reason for that is the low–pass internal output prematching network integrated within the device package. Its purpose is to increase the impedance levels, decrease the impedance Q-factors alleviating the external matching. The network effectively eliminates harmonic content in the output current, preventing external manipulation of the output voltage shape in order to increase the efficiency.

4.4 Load–Pull Based Class–E Microwave PA Design

As a second example of the load–pull design methodology a 10–GHz class–E PA is designed and characterized. Due to unavailability of an X-band commercial load–pull system with harmonic tuning, a laboratory system is developed.

4.4.1 Harmonic–Tuning

In the case of a high–efficiency PA design it is of interest to characterize DUT behavior with different terminations at the harmonic frequencies. Harmonic tuners with sliding resonators or multiple tuner sets separated by frequency multiplexers are commercially available. However, they are extremely expensive, in particular at higher microwave frequencies. In the case of the class–E PA, according to the theory presented in the Chapter 1, a high–impedance second harmonic termination practically satisfies the requirements. It can be realized as a fixed harmonic termination (e.g. microstrip shunt stub) on the DUT test fixture, with corresponding modification of the TRL calibration kit. The fundamental frequency load–pull characterization then can be performed in the same way as previously described.
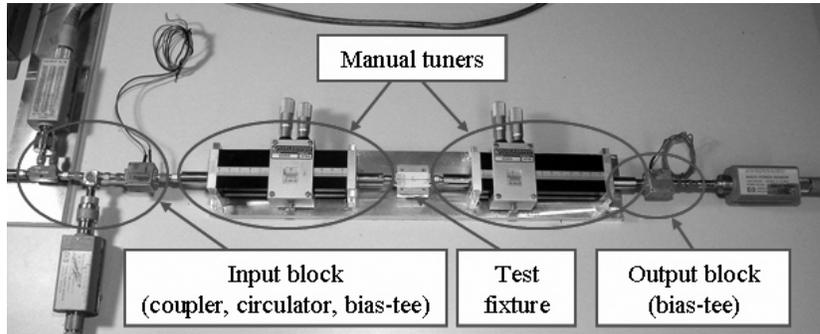
Figure 4.11: Photograph of X–band harmonically terminated load–pull system developed in–house. Mechanical tuners are used to adjust the source and load impedance. The fixed second harmonic termination is provided through the $\lambda/4$ series/shunt microstrip sections on the test fixture. Bias voltages are supplied through the tuner's central conductors from external bias tee-s.

4.4.2 X–Band Load–Pull System

The main components of the system are manual 6–18 GHz tuners (Maury Microwaves, Inc.). Measurement instruments and sources are controlled through a GPIB interface. Calibration and measurement software is developed in MathWorks *MATLAB*® using the theory presented in Appendix B. The X–band measurement system is shown in Fig. 4.11.

The test fixture for characterization of the GaAs MESFET transistor (AFM04P2, by Alpha Industries, Inc.) at 10 GHz as well as the appropriate TRL calibration kit, are showed in Fig. 4.12. The DUT reference plane is set 0.5 mm away from the actual wire bonding point. The bond wire inductances as well as the mounting parasitics to the DUT are thus included. Connectors at the fixture and the calibration kit are 3.5 mm type, sex matched, with very careful and accurate mounting on the base plate. The reason for that

is to minimize the calibration errors due to the connecting non–uniformities.

(a)   (b)
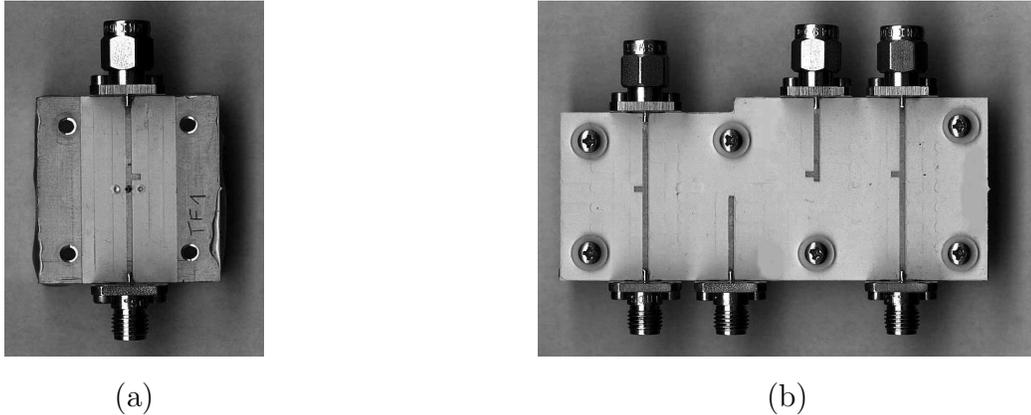
Figure 4.12: (a) A class–E load–pull test fixture, with fixed "open" termination at 20 GHz (shunt microstrip stub). (b) Corresponding TRL calibration kit ("Thru", two "Reflect" and a "Line" standards), with included second harmonic termination at each of them. Both test fixture and the calibration kit are fabricated on 0.635 mm thick Rogers $TMM6^{®}$ substrate ($\epsilon_r = 6, \tan \delta = 0.0018$).

The test–fixture S–parameters are deembeded using a gradient optimization method: the simulated responses of the four standards (Fig. 4.12(b)) are compared to the measured ones. Then, the S–parameters that correspond to the simulated responses are varied through the gradient optimization (Agilent $ADS^{®}$) until the satisfactory matching between simulated and measured responses were achieved.

Overall accuracy of the impedances presented to the DUT for the anticipated tuning range is verified by another TRL calibrated measurement as shown in Fig. 4.13. The insertion loss accuracy of the input and output load–pull blocks is verified measuring the "Thru" response of the entire sys-
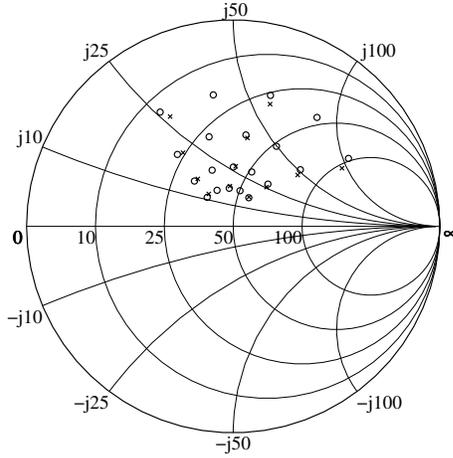
Figure 4.13: DUT impedance accuracy analysis. Calculated (circles) and measured (crosses) DUT input Γ_S for the selected input tuning range. Similar accuracy is observed with the load impedances.

tem, with active device replaced by the "Thru" line. In the 50-Ω position the measured and the calculated "Thru" response agree within $\pm 0.2\,$dB.

4.4.3 Load–Pull Characterization

Using the load–pull system described in the previous section, the active device is characterized. The tuning range for the load impedance is determined using the basic class–E theory and C_{OUT} determined in Chapter 3. The source impedance tuning range is set around the MESFET's S_{11}^* value and later slightly corrected. The 10–GHz source and load–pull contours for constant input power (12 dBm) are shown in Fig. 4.14. As can be observed, the source–pull contours are not closed due to the limited tuning range of the tuners. An additional impedance transformer between DUT and the input

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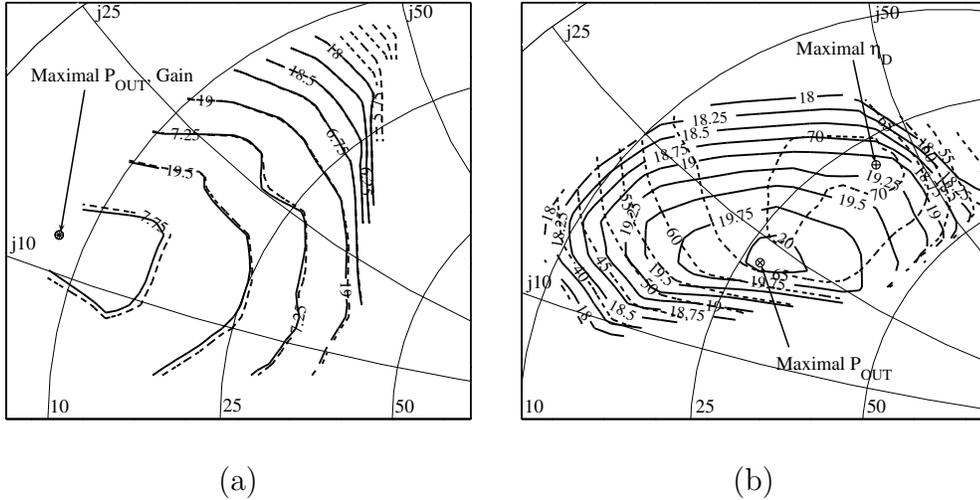
Figure 4.14: (a) Source–pull contours of constant P_{OUT} (solid) and gain (dashed). (b) Load–pull contours of the constant P_{OUT} (solid) and drain efficiency (dashed). P_{IN} is (12 dBm), bias point is $V_{GS} = -1.55$ V and $V_{DS} = 4.2$ V. All parameters are referenced to a plane 0.5 mm from the MESFET terminals.

tuner can expand the impedance coverage toward the edge of the Smith chart. The load–pull contours are closed around the optimal point, indicating that the tuning range of the output tuner is satisfactory. Impedances determined in the measurement are compared to the calculated ones, from Chapter 3, as shown in Table 4.2.

4.4.4 Load–Pull Based Class–E PA

Matching networks for the PA are designed using the target impedances summarized in Table 4.2. The second harmonic termination is provided in the same way as in the load–pull characterization by using $\lambda/4$ series–

Table 4.2: Comparison of load–pull and theoretical load and source impedances for the class–E PA.

$Z_{S-OPT}\,[\Omega]$	$Z_{S-DUT}\,[\Omega]$	$Z_{S-TH}\,[\Omega]$
7.7+j12	9.1+j24.4	5.2+j22.2

$Z_{L-OPT}\,[\Omega]$	$Z_{L-DUT}\,[\Omega]$	$Z_{L-TH}\,[\Omega]$
27.2+j25.8	35.9+j37	27.3+j31.5

Z_{S-OPT} - source–pull determined optimal source impedance, Z_{S-DUT} - source impedance at the DUT, Z_{S-TH} - small–signal source impedance, Z_{L-OPT} - load–pull determined optimal load impedance, Z_{L-DUT} - load impedance at the DUT and Z_{L-TH} - class–E theoretical load impedance.
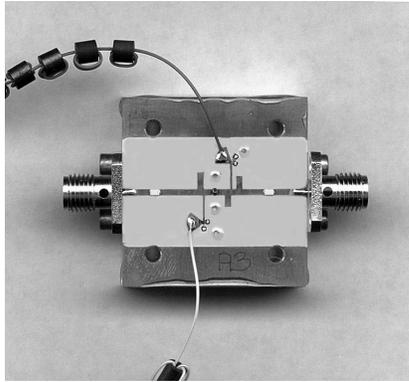
Figure 4.15: Photograph of the assembled load–pull based class–E PA

shunt stub combination. The PA is designed and verified without the bias lines and decoupling capacitors first. After the expected characteristics are achieved, high impedance bias lines are connected to the matching networks, and a series DC blocking microwave capacitor added. The photograph of the assembled PA is shown in Fig. 4.15.

Special care was taken in order to make the transistor mounting (position,

height, bond wire length) as similar as possible to those in the load–pull test fixture. In this particular case, bias lines are excluded from the load–pull characterization. Therefore, their inclusion in the final PA presents a difference that affects the PA performance. In principle, the bias lines can either be included within the DUT, by appropriately setting the reference plane, or they can be a part of the deembedding structures.

4.4.5 PA Characterization
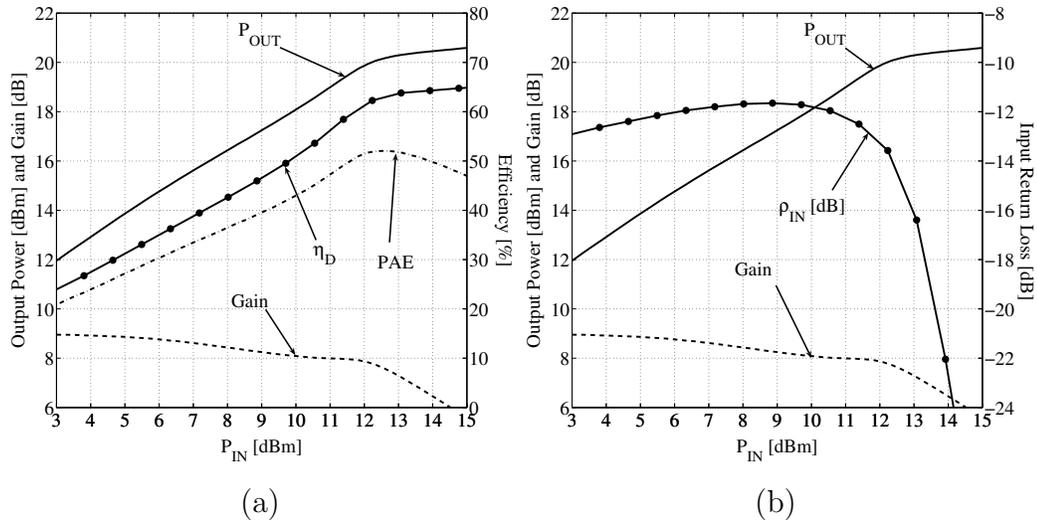
Figure 4.16: Load–pull based PA characteristics at 10 GHz. The bias point is: $V_{GS} = -1.55\,\mathrm{V}$ and $V_{DS} = 4.2\,\mathrm{V}$.

The load–pull based class–E PA is subjected to the standard set of power sweep measurements. The results are shown in Fig. 4.16. The same bias point used for the DUT load–pull characterization is applied. The measured

characteristics are within the expectations established by the load–pull and achieved without any postproduction tuning. Slight output power and efficiency degradation is mainly due to the insertion loss in the biasing/matching networks and SMA connectors (estimated to up to 0.35 dB). A slight matching network adjustment is attempted in order to compensate for the effects of the biasing network, but practically no improvement in characteristics was observed.

4.4.6 Conclusion

Table 4.3: Summarized characteristics of the load–pull based class–E PA at 10 GHz.

P_{OUT} [dBm]	$Gain$ [dB]	η_D [%]	PAE [%]	ρ_{IN} [dB]
20.3	7.8	64	53	-13

P_{OUT} - output power, η_D - drain efficiency, PAE - power added efficiency, ρ_{IN} - power reflection coefficient.

Using an inexpensive in–house developed load–pull system with a harmonic termination appropriate for class–E operation, a highly efficient microwave PA is designed and characterized. The PA operates with optimal characteristics without any required postproduction tuning. The PA's performances at 10 GHz are summarized in Table 4.3.

This approach has significantly reduced PA development time, by eliminating tedious postproduction tuning, that is particularly hard with the class–E PAs due to the need for simultaneous adjustments of the fundamen-

tal the second harmonic terminations. By setting the DUT reference plane apart from the physical bonding location, all parasitics are included within the DUT, eliminating a need for their extraction. The analytic approach presented in Chapter 3 can still be used in order to preselect the tuning range for the load–pull technique.

Chapter 5

Two–Stage Class–E Microwave PA

Due to deep compression required for the class–E mode of operation [9, 59] switched–mode power amplifiers (PAs) exhibit inherently low gain compared to other classes of operation. Improvement in the power gain while maintaining the efficiency can be achieved by cascading high–efficiency stages. In this chapter, trade-offs in high–efficiency two-stage PA design are examined, with the efficiencies, gains, biases and output powers of both stages as design parameters. First, the effect of driver–stage efficiency on overall two–stage PA performance is analyzed. Then a hybrid two–stage class–E PA based on identical GaAs MESFET driver and power stage is designed using load–pull methodology (Chapter 4). Using the bias control, class–E operation of the first stage is ensured for different output powers using the same active de-

vice. Finally, the achieved performance is compared to an X–band class–E InP DHBT MMIC two–stage PA, fabricated by Northrop Grumman Space Technology (NGST) and designed by Dr. Paul Watson at Sensor Directorate, Air Force Research Laboratory. In this amplifier a smaller periphery device is used for the driver stage operating in class–AB.

5.1   Two–Stage Performance Analysis
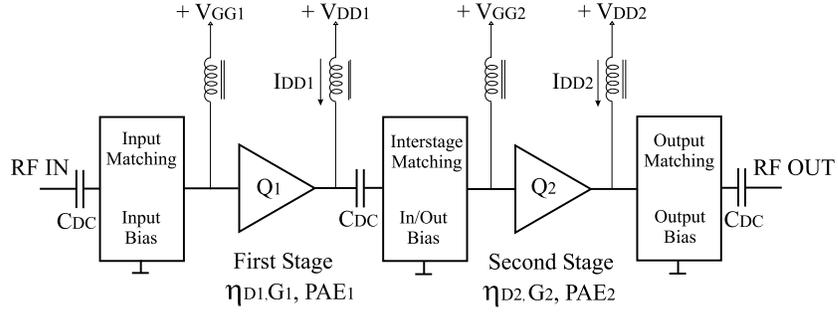
Figure 5.1: Directly–coupled two–stage switched mode PA. Interstage and output matching networks provide fundamental and harmonic frequency terminations for the first and second stage, respectively. Biasing is provided using high–impedance bias lines and series DC blocking capacitors C_{DC}.

The drain efficiency (η_D) of a two–stage PA, Fig. 5.1, can be expressed in terms of the drain efficiencies and gains of the individual stages, η_{D1}, G_1, η_{D2} and G_2:

$$\eta_D = \frac{\eta_{D1}\eta_{D2}}{\eta_{D1} + \frac{\eta_{D2}}{G_2}} \tag{5.1}$$

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The assumption used to derive Eq. 5.1 is that the two stages are perfectly isolated, so that their individual characteristics are maintained. Assuming high–efficiency operation of the second stage (class–E, for example), the overall drain efficiency is examined as a function of the mode of operation of the driver stage. Fig. 5.2 shows the two–stage η_D dependence on the input stage drain efficiency. The parameter in the plots is the second–stage gain G_2.
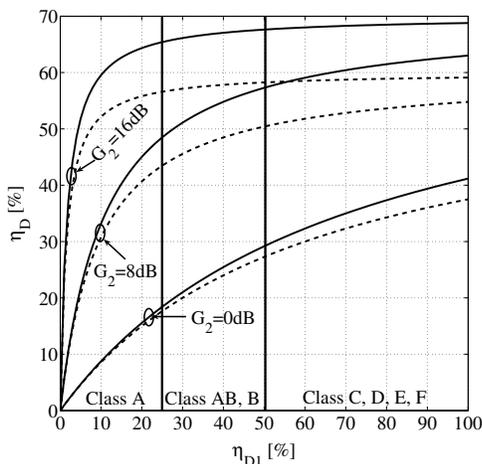
Figure 5.2: Two–stage drain efficiency versus input stage drain efficiency. The second stage drain efficiency is chosen to 70% (solid lines) and 60% (dashed lines). The parameter is the second–stage gain G_2. The vertical lines indicate approximate limits for PA efficiency in different classes of operation at microwave frequency.

For an X–band class–E PA in the second stage, e.g. [60], with a saturated power gain of 8 dB and $\eta_D = 70\%$, an increase of driver–stage efficiency from 20% (Class–A) to 70% (class–E) results in an increase in overall η_D from 45% to 61%. The direct consequences of the increase are:

- a 25% decrease in DC power consumption;

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- a 35% increase in battery lifetime (assuming constant battery characteristics over time);

- a 48% reduction in power dissipated to heat in the active device and

- a decrease in overall gain by the amount of gain compression of the first stage.

From the numerical example given above, it can be concluded that changing the class of operation of the first stage results in a considerable decrease in power dissipation and increase in battery life. However, as the second–stage gain reaches higher values (above $\approx 12\,\mathrm{dB}$), changing the mode of operation of the first stage results in a minor efficiency improvement (less then 8%). Since this is always followed by considerable decrease in the first stage gain due to compression, an increase in effciency by a few percent with sacrifying a few dBs of gain may not be justifiable.

Two–stage drain efficiency is independent of first–stage gain (Eq. 5.1), while the two–stage PAE is a function of drain efficiency and gain of both stages:

$$PAE = \frac{G_2 - \frac{1}{G_1}}{\frac{G_2}{\eta_{D2}} + \frac{1}{\eta_{D1}}}. \tag{5.2}$$

Since the increase in the first–stage drain efficiency affects the gain of the first stage, it is more convenient to analyze PAE by defining the reduction of

PAE due to the addition of a driver stage as:

$$\Delta PAE = PAE_2[\%] - PAE[\%]. \qquad (5.3)$$

Combining Eq. 5.2 and Eq. 5.3, a relationship between required driver–stage PAE and the reduction of the output–stage PAE can be expressed as [61]

$$PAE_1 = \frac{(PAE_2 - \Delta PAE) \cdot (G_1 - 1) \cdot PAE_2}{[\Delta PAE \cdot (G_2 - 1) + PAE_2] \cdot G_1 - PAE_2}, \qquad (5.4)$$

where PAE_1, G_1, PAE_2, and G_2 are the efficiency and gain values of the driver and output stages, respectively. This dependence is shown in Fig. 5.3, for two different cases: a higher–gain high–efficiency second stage ($PAE_2 = 55\%$, $G_2 = 11\,\mathrm{dB}$), and a lower–gain high–efficiency second stage ($PAE_2 = 55\%$, $G_2 = 7\,\mathrm{dB}$), with the gain of the first stage ($G_1 = 8, 11, 14$ and $17\,\mathrm{dB}$) as a parameter.

These are typical gain values for different classes of operation of microwave active devices, from deeply saturated class–E to linear class–A, respectively. To maintain the PAE of the two–stage amplifier very close to the second–stage PAE (e.g. $\Delta PAE \leq 2\%$) the PAE of the first stage has to be above 36%. This can be easily achieved if the first stage operates in AB class, resulting in minimal gain reduction. However, if the second stage has a smaller gain but higher efficiency, in order to maintain PAE reduction at the same value (less than 2%) the efficiency of the first stage has to be around

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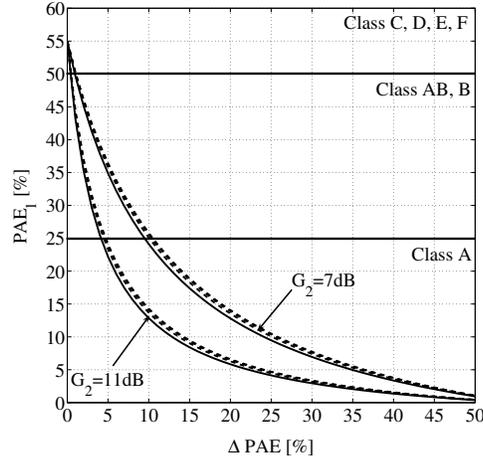
Figure 5.3: PAE_1 as a function of ΔPAE for G_1 equal to 8, 11, 14 and 17 dB. PAE_2 is 55% in both cases and G_2 is either 7 dB (upper curve set) or 11 dB (lower curve set). The approximate limits for microwave PA efficiency of different classes of operation are indicated with vertical lines.

50%. This can be achieved by operating the first stage PA in deeper AB or B class of operation, or class–E, as applied in the following work.

The PAE plot in Fig. 5.3 reveals another property of two–stage amplifiers: the overall PAE can actually be equal or even greater than the second stage PAE. For example, for a low–gain, high–efficient second stage ($G_2 = 7$ dB, $PAE_2 = 55\%$, $\eta_{D2} = 69\%$), if the PAE of the first stage is the same as the second stage PAE, the overall PAE will remain the same. This is very convenient property, since the efficiency of the commercial PAs is commonly characterized by PAE, instead of drain (collector) efficiency.

PA stages can be cascaded as follows:

(1) by using two balanced amplifiers. This provides isolation between

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separately–designed stages due to the matching provided by directional couplers;

(2) by inserting a non–reciprocal element (isolator) between stages;

(3) by directly connecting of the driver and output stages with an interstage matching network.

In this work the latter approach is followed. It eliminates the loss due to couplers/isolators, reduces the required real–estate, and allows a monolithically integrated circuit. The price is the relative difficulty of the interstage matching network design.

5.2   Hybrid Two–Stage High–Efficiency PA Design

Based on the trade–off analysis presented in the previous section, it can be concluded that the efficiency of the second stage should be maximized. Class–E operation is chosen since it requires slower devices than other switched modes and it is relatively insensitive to parameter variations [2, 46]. As the output stage, a class–E PA described in the Chapter 4 is used.

5.2.1 The High–Efficiency Driver Stage

Fig. 5.2 shows the efficiency trade–offs in drive stage operating mode choice. A class–E driver stage is chosen, using the same GaAs MESFET as the output stage, operating at a lower output power level, required for driving the output stage. However, a decrease in input power will cause a rapid drop in the amplifier efficiency [3, 4]. This is a common problem for all high–efficiency classes of operation. Nevertheless, based on the derivation presented in Chapter 1, Subsection 1.3.6, the output power of a class–E PA can be varied by varying the bias with the following properties:

- the power can theoretically range between zero and maximal available power;

- for a realistic transistor, the drain bias should be kept above threshold to avoid significant power gain degradation [1], giving a lower limit to the power range;

- the upper power range limit is given by the max V/I peak handling capability of the device, which also depends on the nonlinearity of the output capacitance [1];

- the optimal (ideal) efficiency is not affected when the bias is varied. Namely, the transistor voltage and current amplitudes change with bias voltage, but not their shape in time domain. Since the waveform shape is responsible for the high efficiency in class-E mode, the efficiency

remains the same;

- for the same reason, the optimal class–E load impedance remains the same.

The lower power limitation is a practical constraint that can be avoided by using a smaller–periphery device for the driver stage amplifier, which was not commercially available for the MESFET used in this work. However, this method is used in the monolithic PA presented in the next section, while the bias–controlled power method is used for the hybrid PA.
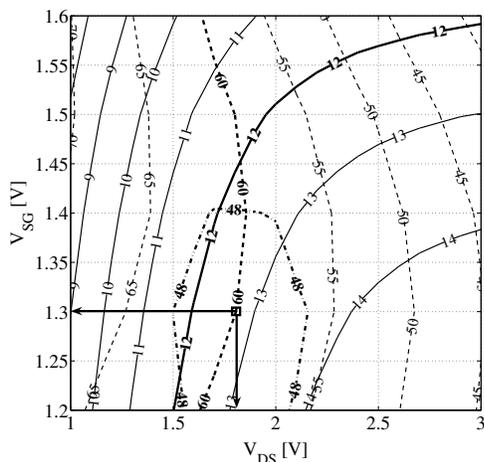
Figure 5.4: Bias/power sweep contours of the designed class-E PA for input power of 5 dBm at 10 GHz. Shown are contours of constant P_{OUT} (solid) and η_D (dashed). Gain contours are omitted from the plot for the clarity and can be inferred from the P_{OUT} and P_{IN}. As a result of a compromise between these three parameters the bias point for the driver stage is selected (arrows): $V_{GS} = -1.3\,\text{V}$ and $V_{DS} = 1.8\,\text{V}$, resulting in expected $G \approx 7.5\,\text{dB}$, $P_{OUT} \approx 12.5\,\text{dBm}$ and $\eta_D \approx 60\%$.

In order to select an optimal bias point an automatic bias/power sweep measurement is performed. The required output power of the driver stage is between 12 dBm and 13 dBm. The constant P_{OUT}, G and η_D contours for $P_{IN} = 5$ dBm are shown in Fig. 5.4. This approach assumes that the C_{OUT} is not a function of bias voltage. Although the C_{GD} component of C_{OUT} varies with drain bias [30] these variations are small in the range of voltages chosen for the measurements in Fig. 5.4, and efficiency remains high even for low drain bias voltages.

5.2.2 The Two–Stage Switched–Mode PA

The block diagram of the directly–coupled two–stage amplifier is shown in Fig. 5.1. The interstage matching network shown in Fig. 5.5 transforms the input impedance of the output stage into the optimal class–E impedance for the first stage, and in the same time provides the second-harmonic termination as well as the biasing.

For the initial interstage matching network design, the complex–conjugate of Z_S is used $(9.1 - j24.4\Omega)$, determined from the source–pull characterization of the DUT and observed small reflected power from the DUT (Fig. 4.16(b)). The fabricated two-stage hybrid amplifier is shown in Fig. 5.6.

Results of power–sweep characterization of the optimized two–stage PA are shown in Fig. 5.6(b). The data is measured for a connectorized amplifier. During the optimization process, the fundamental frequency load impedance of the first stage is slightly changed from the initial class–E value. Therefore,

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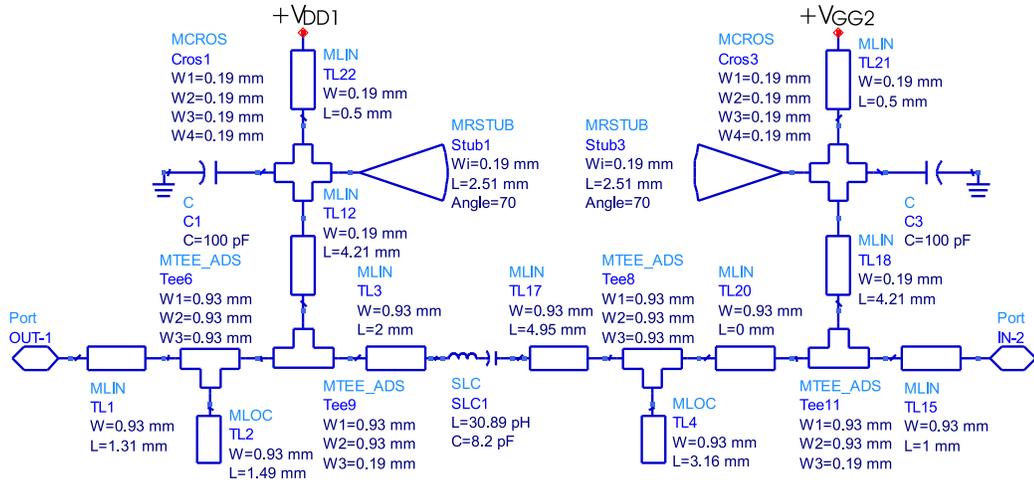
Figure 5.5: Schematic of the interstage matching network.
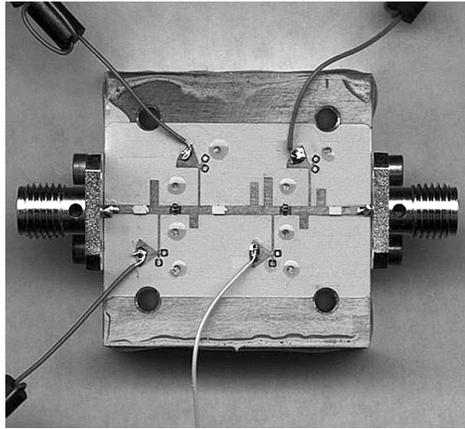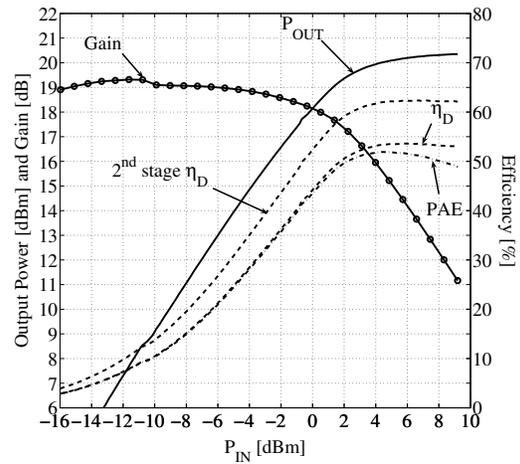
(a)   (b)

Figure 5.6: (a) Photograph of the hybrid two–stage class–E PA after interstage matching network tuning. (b) The measured power–sweep of the two–stage switched–mode PA at $10\,\mathrm{GHz}$. The bias point for the first stage is $V_{GS1} = -1.3\,\mathrm{V}$ and $V_{DS1} = 1.8\,\mathrm{V}$ while the second stage is biased at $V_{GS2} = -1.55\,\mathrm{V}$ and $V_{DS2} = 4.2\,\mathrm{V}$.
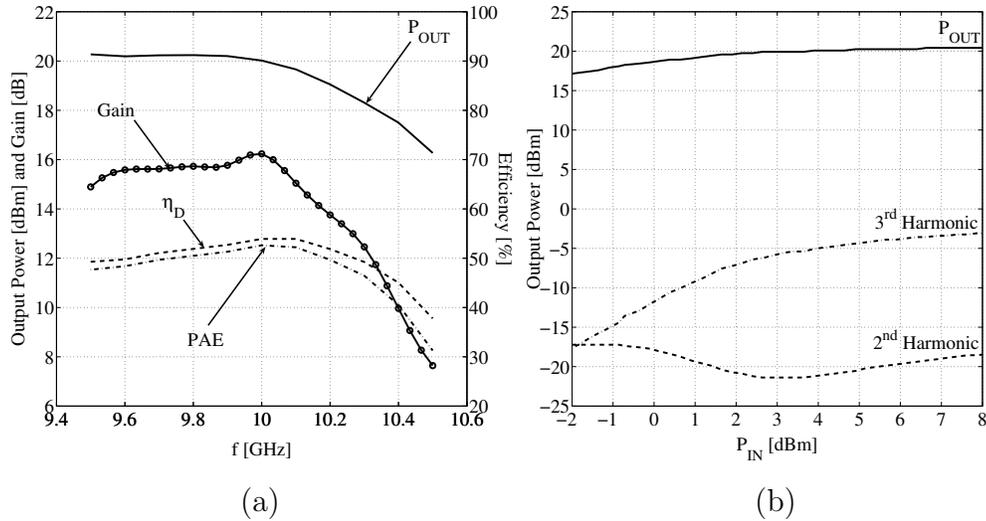
Figure 5.7: (a) Frequency sweep of the two–stage amplifier characteristics. The P_{IN} is adjusted to maintain the maximal PAE at each frequency point. (b) Measured second and third harmonic power sweep of the two–stage PA.

the first stage operates in an alternative class–E mode, or perhaps in a deeply saturated AB class, with an "open" termination at the second harmonic frequency. The two–stage amplifier has an excellent input return loss of -18 dBc at the nominal input power level of 4 dBm. The frequency sweep of amplifier parameters for maximum PAE is shown in Fig. 5.7(a). The second and third harmonic levels are -41 dBc and -25 dBc, respectively, (Fig. 5.7(b)). High suppression of the second harmonic in the output signal is a result of the harmonic traps applied in both amplifier stages. The intermodulation products are measured with a two–tone test signal at 10 GHz with 100 kHz frequency spacing. As expected, the class–E PA is nonlinear with third, fifth and seventh order products of -11 dBc, -19.7 dBc and -32 dBc, respectively.

The linearity of the PA can be significantly improved by implementing the EER linearization scheme, as presented in [62]. In this case, both stage bias voltage can be regulated by a fast bias controller in order to reconstruct amplitude modulation at the PA output. Initial set of static measurements is performed on the designed two–stage PA. These measurements are required for FPGA look–up table generation, as described in [62]. AM–AM and AM–PM characteristics of the PA are shown in Fig. 5.8.
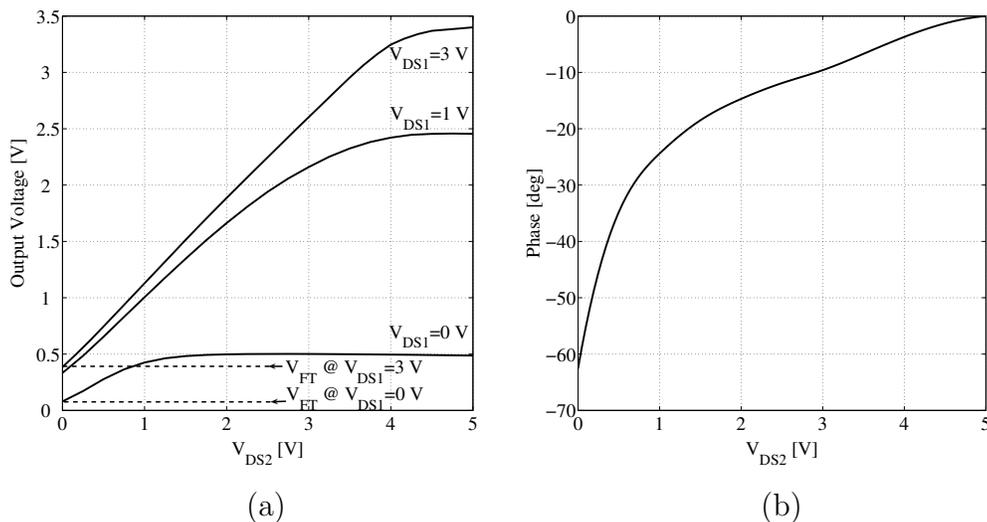
Figure 5.8: (a) Measured AM–AM characteristics of the two–stage PA. Gate voltages of both stages are kept constant ($V_{GS1} = -1.3\,\text{V}$ and $V_{GS2} = -1.55\,\text{V}$, as well as the $P_{IN} = 4\,\text{dBm}$. Parameter of the curves is V_{DS1}. Output voltage is calculated for load impedance of $50\,\Omega$. Feed–through voltage is shown on the plot (V_{FT}) for two different V_{DS1} values. (b) Measured AM–PM characteristics are shown for nominal bias of the first stage.

An interesting property of the two–stage PA is possibility to reduce feed–through voltage (V_{FT}) by decreasing the drain voltage of the first stage. A

Table 5.1: Measured hybrid two–stage class–E amplifier performances.

P_{OUT} [dBm]	G [dB]	η_D [%]	PAE [%]	η_{D2} [%]	ρ_{IN} [dB]
20	16	53	52	62	< -18

P_{OUT} - output power, G - gain, η_D - two-stage drain efficiency, PAE - two-stage power added efficiency and ρ_{IN} - input reflection coefficient.

Table 5.2: Separately–measured 1st and 2nd stage performances compared to integrated hybrid two-stage PA performances.

	P_{OUT1} [dBm]	G_1 [dB]	η_{D1} [%]	PAE_1 [%]
Separated stages	12.5	7.5	61	50
Connected stages	≈ 12	≈ 8	≈ 60	≈ 50

	P_{OUT2} [dBm]	G_2 [dB]	η_{D2} [%]	PAE_2 [%]
Separated stages	20.3	7.8	64	53
Connected stages	20	8	62	52

P_{OUT1} - first stage output power, G_1 - first stage gain, η_{D1} - first stage drain efficiency, PAE_1 - first stage power added efficiency, P_{OUT2} - second stage output power, G_2 - second stage gain, η_{D2} - second stage drain efficiency and PAE_2 - second stage power added efficiency.

minimal value of V_{FT} is required for an EER transmitter since it affects overall linearity of the PA ([62]). In a single stage PA V_{FT} can be reduced by inserting an attenuator in the input signal path. This reduces efficiency of the entire system due to the small but finite insertion loss of the attenuator during the portion of the envelope cycle when its action is not needed. In the case of the two–stage class–E PA, the first stage with bias control can be used to achieve the same goal.

Table 5.1 summarizes the measured performance of the two-stage PA. The

performance comparison of the two stages when characterized separately is given in Table 5.2. The output power of the first stage is estimated.

From the given data it can be concluded that the main amplifier parameters of both stages are preserved after direct connection.

5.3   Monolithic Broadband Two–Stage PA

For comparison purposes, monolithic single and two–stage PAs are designed by Dr. Paul Watson et al. [63, 64, 65] shown in Fig. 5.9.
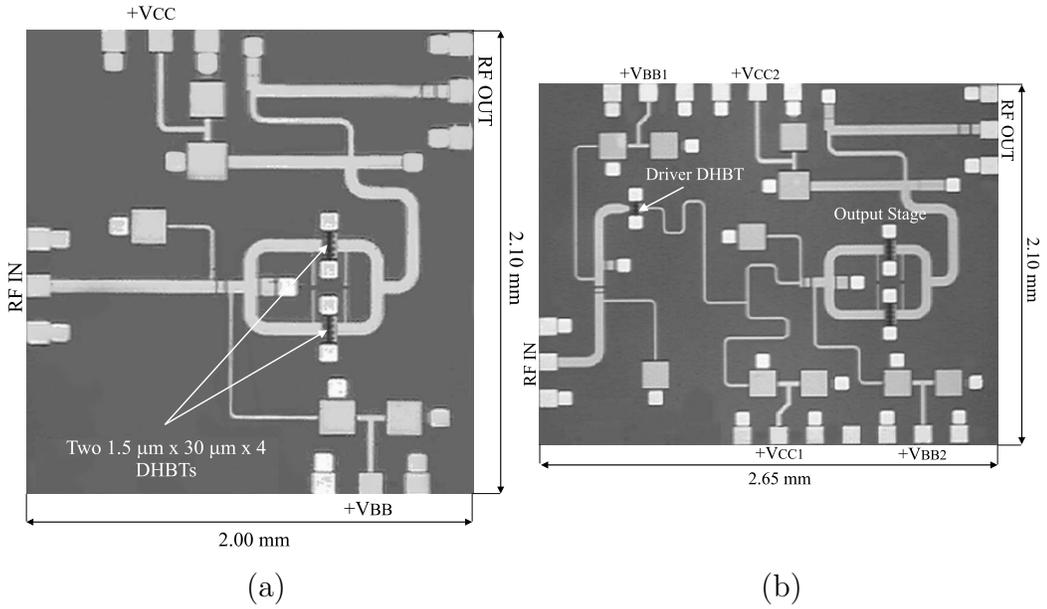
Figure 5.9: Photograph of the monolithic InP DHBT class-E output stage (a) and the entire two–stage MMIC PA (b). The input stage consists of a single 1.5 μm x 30μm x 2 finger device. The output stage consists of two 1.5 μm x 30 μm x 4 finger devices combined in parallel, resulting in a total emitter area of 360 μm^2.

The two–stage PA is designed with a class–AB input stage, and an alternative class–E as a second stage. InP DHBT active devices with different peripheries for input and output stages are used. The device technology utilized for the MMIC class–E amplifier has been detailed in [63, 64]. The amplifier is designed for radar applications with amplitude flatness over a relatively broad frequency range (8-10 GHz). The design is performed using available scalable nonlinear models for the InP DHBTs. Summarized characteristics of the MMIC PA are given in Table 5.3.

Table 5.3: Comparison of monolithic output stage class-E PA and monolithic two-stage class-E PA at 8 GHz.

	P_{OUT} [dBm]	G [dB]	η_D [%]	PAE [%]	BW [GHz]
Output stage PA	24.7	11.7	59	55	7.4-10.1
Two-stage PA	24.6	24.6	52.2	52	7.7-10.5

P_{OUT} - output power, G - gain, η_D - two-stage drain efficiency, PAE - two-stage power added efficiency and BW - frequency bandwidth for PAE $\geq$ 40%.

5.4 PA Performance Comparison

The hybrid and MMIC PAs are compared in Table 5.4 with the following conclusions:

(1) Both PAs demonstrate around 52% PAE and well-preserved individual–stage characteristics. The compressed gain of the monolithic PA is higher due to the higher linear gain of the HBT compared to the MESFET.

Table 5.4: Comparison of hybrid and MMIC two–stage class–E PAs.

	1ST Stage	2ND Stage	f [GHz]	f_T [GHz]
Hybrid PA	GaAs MESFET	GaAs MESFET	10	30
MMIC PA	InP DHBT	2 x InP DHBT	8	80

	G [dB]	P_{OUT} [dBm]	η_D [%]	PAE[%]	BW [GHz]
Hybrid PA	16	20	53	52	9-10.4 (14%)
MMIC PA	24.6	24.6	52.2	52	7.7-10.5 (31%)

f - frequency of operation, f_T - cutoff frequency, G - power gain, P_{OUT} - output power, η_D - drain efficiency, PAE - power added efficiency, BW - frequency bandwidth for $PAE \geq 40\%$.

(2) Due to the larger f_T, InP DHBTs are well-suited for this mode of operation;

(3) The monolithic PA is designed using harmonic balance simulations to have a PAE $\geq 40\%$ with minimal gain and power variations over 31% bandwidth. In contrast, the hybrid PA is designed using basic theory augmented by load–pull at a single frequency. Although not designed to be broadband, it exhibits a 15% bandwidth for $PAE \geq 40\%$;

5.5 Conclusion

In the previous sections the first successful realization of a two–stage efficiency–optimized PA at X–band is presented. The following general conclusions can be drawn:

(1) Although the driver stage consumes less power than the output stage,

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it is important to optimize its efficiency, as it directly determines the total PAE;

(2) The class of operation of the driver stage should be determined by the gain requirement: for higher gain, class–AB will give optimal overall efficiency performance, while for highest overall efficiency, class–E is recommended;

(3) If different periphery devices are not available, it is possible to achieve very high total efficiency by bias adjustment of the driver stage, due to the unique properties of the class–E mode of operation;

(4) Efficiency is optimized when the two amplifier stages are directly cascaded with an interstage network. The design of this network is not straightforward due to the bilateral character of both stages;

(5) Hybrid and monolithic versions with different device types (e.g. MESFET and HBT in this work) can give comparable efficiency results if all parasitics in the hybrid design are modeled appropriately;

(6) The efficiency–optimized two–stage PA is nonlinear. Well–known linearization techniques, such as Envelope Elimination and Restoration (EER) [62], can be modified to apply to two stages.

Chapter 6

Transistor Technologies for High–Efficiency Microwave PAs

6.1 Introduction

Currently, microwave power and low–noise transistors are commercially available in five distinctive technologies: Bipolar Junction Transistors (BJT), Metal–Oxide–Semiconductor Field–Effect Transistors (MOSFET), MEtal–Semiconductor Field–Effect–Transistors (MESFET), Heterojunction Bipolar Transistors (HBT) and High Electron Mobility Transistors (HEMT).

The first two technologies are commonly used in low–frequency analog and digital electronics, although recent fabrication precess advance have made these transistor technologies available in the microwave range ($\leq 8\,\mathrm{GHz}$). The other three technologies are dominant in the medium and high mi-

crowave frequency range ($\geq 3\,\text{GHz}$) due advances in three fabrication processes: Molecular Beam Epitaxy (MBE), Metal Organic Chemical Vapor Deposition (MOCVD) and Ion Implantation. A very comprehensive overview of microwave transistor technologies is given in [16, 30, 31] and here a brief overview of the operation principles and the current state of these three technologies is presented in context of switched mode PAs.

6.1.1 MESFETs

The operation of a MESFET is very similar to the operation of a MOSFET, with the main difference in the gate, which forms a Schottky contact with the applied semiconductor. This eliminates gate MOS capacitance allowing for higher operating frequencies. MESFETs are usually fabricated in GaAs. Significantly larger low–field electron mobility of the GaAs ($8625\,\text{cm}^2/\text{Vs}$, compared to $1430\,\text{cm}^2/\text{Vs}$ for n–type Si) directly improves the maximal frequency of operation (Eq. 6.3). In addition to electrons having higher mobility compared to holes, it is difficult to obtain p–type GaAs. For a n–type MESFET source and drain electrodes are ohmic n^+ connects. Semiconductor n–type active layer is epitaxially grown on a semi–insulating GaAs substrate. A common dopant for the GaAs is Si. The drain current is controlled by the gate–source voltage, with modes of operation identical to the MOSFET (triode, saturation and cutoff [71, 72, 16]).

A small–signal model of a MESFET transistor is shown in Fig. A.1 (Appendix A). The f_T and f_{MAX} of such a transistor are related to the model

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parameters as [16]:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})(1 + g_{DS}R_S) + C_{GD}g_m R_S}, \qquad (6.1)$$

$$f_{MAX} = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \frac{1}{\sqrt{(4g_{DS}(R_i + R_S + R_G) + 4g_m R_G \frac{C_{GD}}{(C_{GS} + C_{GD})}}}, \qquad (6.2)$$

where C_{GS}, C_{GD}, R_S, R_G, R_i and g_m are the elements of small signal model shown in Fig. A.1. A common approximation for f_T is:

$$f_T \approx \frac{g_m}{2\pi C_{GS}} = \frac{v_S}{2\pi L} \qquad (6.3)$$

where v_S is the saturation velocity and L is the channel length. Therefore, the cutoff frequency of a MESFET can be maximized by increasing the transconductance, or more importantly by decreasing the parasitic capacitances (resistances), mainly C_{GS}. From the device design standpoint that means increase in the saturation velocity with decrease in channel length.

The MESFET gate–drain breakdown voltage can be approximately found from an empirical formula [16]:

$$BV_{GD} \approx \frac{9 \cdot 10^9 L_{EFF}}{N_D a}, \qquad (6.4)$$

where L_{EFF} is the effective gate length, N_D is the doping concentration and a is the active layer thickness. The typical BV_{GD} for MESFETs is 20–30 V, and maximal current densities are 300–400 mA/mm. It can be concluded from Eq. 6.1 and Eq. 6.4 that the design requirements for high f_T and breakdown voltage are contradicting.

The MESFET technology is in a very mature state, with a maximal published f_T of 168 GHz for a low–noise device. Power MESFETs are able to deliver more than 10 W per single die at 14 GHz [73]. Further increase in output power is achieved with new wide–bandgap material MESFETs, such as SiC and GaN MESFETs. These transistor have extremely high breakdown voltages (up to 150 V) while the cutoff frequencies currently reach 22 GHz [74].

6.1.2 HBTs

The structure of a HBT is very similar to a standard BJT transistor. It can be NPN or PNP type, with the main difference in heterojunction between emitter and base: the energy band-gap of the base material is smaller than the band–gap of the material used for emitter. Due to the bending of the energy levels at the junction of two distinctive materials, after the initial carrier diffusion the energy barriers imposed to the electrons moving from the N–type material (emitter) to the P–type (base) remains much smaller then the barrier imposed to holes traveling in the opposite direction. After forward bias is applied, electrons with sufficient energies are able to cross

the junction from N to P crystal by thermionic field emission [16]. The hole current from the P to the N crystal is effectively suppressed, due to the higher energy barrier. This property allows for a high doping concentration of the base, in order to reduce base resistance and increase f_{MAX}, Eq. 6.6. The rest of the HBT operation is similar to homojunction BJT. If the collector–base junction also consists of materials with different band-gaps, the transistor is called Double Heterojunction Bipolar Transistor (DHBT). Vertical current flow in a HBT relaxes requirements for photolitographic accuracy and MBE layer control determines the main transistor parameters.

The materials that are forming the junctions allow again for significantly higher electron mobilities compared to Si, resulting in a much higher f_T and f_{MAX} compared to BJTs. The cut–off frequency of a HBT can be calculated as:

$$f_T = \frac{1}{2\pi\tau_{EC}}$$
(6.5)

where τ_{EC} is the total emitter–collector transit time [16]. The most critical component of τ_{EC} is the base transit time. This parameter is quadratically proportional to the base thickness. Therefore thinning the base body results in a rapid increase in f_T. However, as in BJTs, the base cannot be arbitrarily thin due to the breakdown (base punch-through). The maximal frequency

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of oscillation for an HBT can be calculated as:

$$f_{MAX} = \sqrt{\frac{f_T}{8\pi R_B C_{CB}}} \tag{6.6}$$

where R_B and C_{CB} are the total base resistance and the collector–base capacitance, respectively [16]. As can be concluded from Eq. 6.6, the f_{MAX} can be increased by decreasing both R_B and C_{CB}. Collector–emitter breakdown voltage of HBTs is typically around 15–20 V.

HBT technology is relatively young and modern HBTs suffer from several problems, such as self–heating, current gain collapse, V_{CE} voltage–offset etc. However, the performance of experimental HBTs is very impressive: f_{MAX} ranges from 40–350 GHz for GaAs–based HBTs and up to 300 GHz for for InP–based HBTs. The highest f_{MAX} of 1080 GHz (with gain of 21 dB at 100 GHz) is achieved with an InP–based transferred–substrate HBT [75]. SiGe HBTs reach a f_{MAX} of 300 GHz [76]. The output power capability of HBTs currently reaches 1 W at 35 GHz. One of the very convenient properties of HBTs is their neutral or slightly negative current gain temperature coefficient. It simplifies the bias network design compared to ordinary BJTs, eliminating the need for sensing and current control network.

6.1.3   HEMTs

A typical GaAs HEMT is very similar to a MESFET, with the main difference in materials used in the active channel (InGaAs) and AlGaAs barriers

surrounding the channel. These two materials have different band–gaps, forming a heterojunction between them. Due to the bending of the energy bands after such materials are contacted, the electrons from the AlGaAs layer are forced to migrate in an extremely thin layer between AlGaAs and GaAs layers, where they remain confined in a so–called two dimensional electron gas. These electrons are the main carriers that form the drain current. The density of the electron cloud (and therefore the drain current intensity) is modulated by the gate voltage and the Schottky barrier formed underneath the gate. The rest of operation is very similar to that of a MESFETs. Since the electrons are spatially separated from their donors their motion is not affected by the ionized impurities, therefore resulting in enhanced mobility compared to that one in bulk GaAs. This improvement is by one or more orders of magnitude at lower temperatures, compared to MESFETs.

Performance achieved by AlGaAs/GaAs HEMTs is a: f_{MAX} of 151 GHz [77], power densities of 0.5–1.5 W/mm (Watts per gate width) ([16] with 60 W per die at 2.14 GHz. AlGaAs/InGaAs pHEMTs achieve f_{MAX} of 290 GHz, with power density of 1.6 W/mm at 2 GHz with over 35 W per transistor die. The power pHEMTs operate up to 94 GHz. GaAs mHEMTs achieve f_{MAX} of 400 GHz and power densities of 0.92 W/mm at 35 GHz. The major improvement is achieved in InP HEMTs: f_{MAX} of 600 GHz are reported, with a useful output power up to 100 GHz. Breakdown voltage of GaAs and InP HEMTs is in 10–20 V range. Finally, wide–bandgap HEMTs (AlGaN/GaN) exhibit f_{MAX} of 155 GHz. These HEMTs have an extremely high breakdown

voltage of up to 248 V [78] allowing for power densities of 10.7 W/mm at 10 GHz A single transistor delivers 51 W at 6 GHz [79]. With the exception of the AlGaAs/GaAs HEMTs all of the mentioned types are in the development phase and they are not yet commercially available.

6.2 Class–E PA Comparison

The most important parameter for class–E PA active device selection is the cutoff frequency (f_T) as well as the maximal frequency of oscillation (f_{MAX}), defined in Chapter 1. The switching speed is directly proportional to these parameters and therefore to first order limits the high–efficiency operation (Chapter 1). Furthermore, microwave transistors exhibit the well known unilateral gain frequency roll–off of ≈ -20 dB/dec:

$$U(f) \approx -20 \log(f) + 20 \log(f_{MAX}) \tag{6.7}$$

It can be expected that a transistor with the larger f_{MAX} will exhibit larger unilateral gain at the a certain operating frequency than a transistor with smaller f_{MAX}. Higher cutoff frequency implies lower extrinsic parasitics of such a device (Eq. 6.1), anticipating a higher achievable efficiency.

As in linear classes of operation, the maximal transistor output voltage is limited by breakdown, while the current limit is related to the maximal current density achievable by the device. These parameters determine the maximal power that can be extracted from a given device (Chapter 1).

Power amplifiers operating in class–E switched mode in the C–X band range have been implemented with MESFETs [60] HBTs [63, 80], and HEMTs [81, 82]. In this work three hybrid X–band class–E PAs using GaAs MESFET, InP DHBT and GaAs pHEMT active devices are designed and characterized. Their characteristics are compared, particularly with respect to their saturation properties, AM–AM, AM–PM, feed–through and supply–to–load voltage transfer characteristics. The main parameters are examined over a frequency range in order to compare suitability of these high efficiency PAs for wide–bandwidth EER [62]. This is the first comparative study of the transistor technologies for class–E PA design performed so far.

For the study, only the GaAs MESFET transistor was commercially available (AFM04P, by Alpha Industries, Inc). The DHBT transistor is provided by Northrop Grumman Space Technologies (Dr. Wendy Lee), while the GaAs HEMT is provided by Raytheon (Dr. Katherine Herrick). All three transistors are with similar physical dimensions, and the class–E PAs operate with similar output bias voltages. The active devices are mounted as described in Chapter 3. Each of the PAs is designed for a 10–GHz operating frequency, using similar matching network design approach. Initial target impedances, harmonic terminations and bias points are chosen for class–E operation. However, these values are later optimized through load–pull and automated bias sweep in order to achieve the best compromise between P_{OUT}, gain and efficiency.

6.2.1 GaAs MESFET PA Design

The MESFET PA used for the comparison is the same one used in Chapter 4. The 6–finger device has a gate length of $0.25\,\mu$m, with a total gate periphery of $400\,\mu$m. Estimated f_T and f_{MAX} are $30\,$GHz and $50\,$GHz, respectively [16]. The PA is designed using class–E theory, augmented with the load–pull technique. For this transistor the TOM2 nonlinear model is available and the simulated and measured performances using (Agilent $ADS^\text{®}$ harmonic balance are compared in Fig. 6.1. Convergence problems were encountered during the harmonic balance simulation. The PA exhibits relatively good input match of -13 dB.
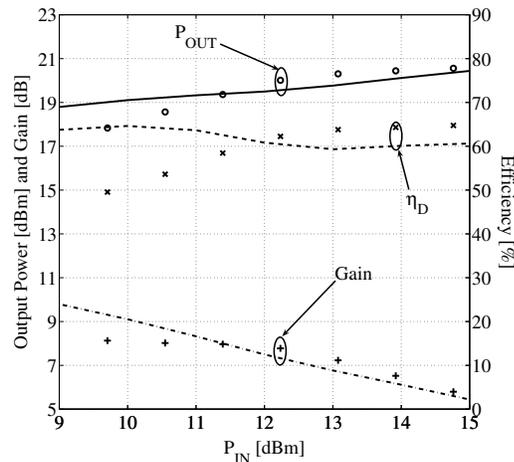
Figure 6.1: Measured (symbols) and simulated (lines) MESFET PA characteristics at $10\,$GHz. Bias point is $V_{GS} = -1.55\,$V and $V_{DS} = 4.2\,$V. The available TOM2 model parasitic inductances are slightly decreased in order to achieve better agreement between measurement and simulation at the operating power level ($P_{IN} \approx 12 - 14\,$dB.)

6.2.2 InP DHBT PA Design

The second PA uses a InAlAs/InGaAs DHBT on InP substrate fabricated by NGST [63]. The transistor has a $1.5\,\mu$m x $30\,\mu$m x 4 emitter finger unit cell and is capable of delivering $22\,$dBm of output power with a gain of $16\,$dB at $20\,$GHz. This is considerably higher gain than in the GaAs MESFET case, mainly due to the larger f_T and f_{MAX} values of $80\,$GHz and $150\,$GHz, respectively. The class–E impedance is determined from the measured output capacitance of $0.19\,$pF, which gives an optimal $Z_L = (16 + j18)\Omega$. The actual unpackaged device has an integrated microstrip launch line that was taken into account at the fundamental and harmonic frequency. As the initial source impedance, a value for a MMIC PA design with the same device [80] was used: $Z_S = (1.12 + j2.96)\Omega$. A schematic of the HBT PA is shown in Fig. 6.2 and the photograph of the fabricated and tuned PA is shown in Fig. 6.3.
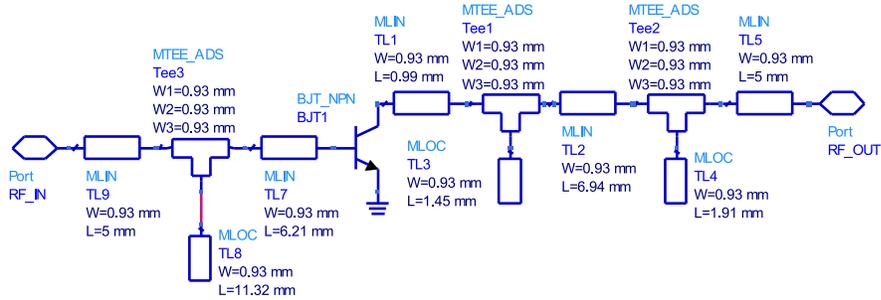
Figure 6.2: Schematic of the DHBT class-E PA. The PA is fabricated on $0.635\,$mm thick Rogers $TMM6^{®}$ substrate ($\epsilon_r = 6, \tan\delta = 0.0018$), with external bias–tees.
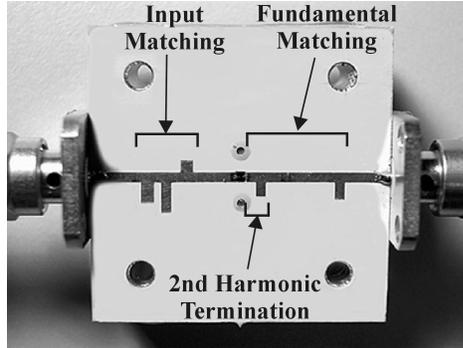
Figure 6.3: Photograph of the DHBT hybrid PA, with tuned input matching network.

(a)

(b)
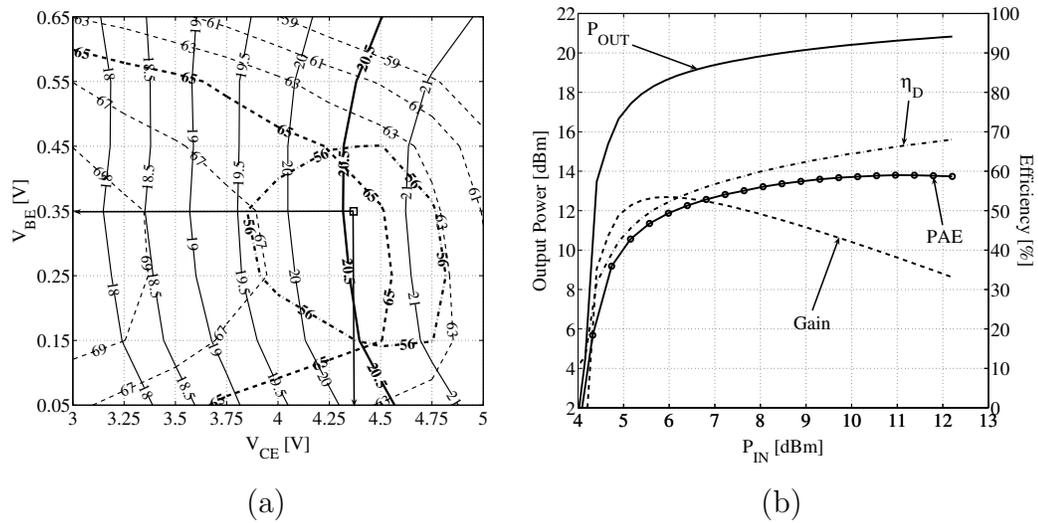
Figure 6.4: (a) Constant P_{OUT} (solid), η_D (dashed) and PAE (dot–dashed) contours of obtained through the automated bias/power sweep. Selected bias point is $V_{CE} = 4.35\,V$ and $V_{BE} = 0.35\,V$. (b) Measured DHBT class–E power amplifier characteristics.

A low–frequency oscillation were detected with the device. A possible cause of oscillations is the very high gain at low frequencies. Due to the very limited number of available devices, stabilization was not attempted and the

integration of narrowband bias line with the PA was omitted. Instead, the external broadband bias–tees were used. In addition, the output biasing range of the transistor was limited up to 5 V. The optimal bias point is found through an automated bias–sweep measurement (Fig. 6.4(a)). The power–sweep characteristics of the PA are shown in Fig. 6.4(b). The PA exhibits a relatively good input match of -12 dB.

6.2.3   GaAs pHEMT PA Design

The HEMT PA uses a Raytheon AlGaAs/InGaAs/GaAs pseudomorphic HEMT [83]. From the measured DC static characteristics, maximal current and voltage ratings are estimated to be: $V_{DS-MAX} = 14$ V and $I_{D-MAX} = 250$ mA, which corresponds to approximately 440 mW (26.4 dBm) of the available class–A output power. The approximate C_{OUT} is 0.25 pF. Using the load–pull setup described in Chapter 4 the optimal source and load impedances were found. The measured load and source pull contours for the selected bias point and constant input power are shown in Fig. 6.5.

A schematic of the hybrid HEMT PA with integrated bias lines is shown in Fig. 6.6, and the photograph of the tuned PA is shown in Fig. 6.7.

The optimal bias point was found through a systematic bias/power sweep (Fig. 6.8(a)). Measured power sweep of the tuned PA is shown in Fig. 6.8(b). The PA exhibits a moderate input match of -9.7 dB.

Some amount of postproduction tuning was performed. The reason for this is a relatively low input impedance, and a lower load–pull accuracy at
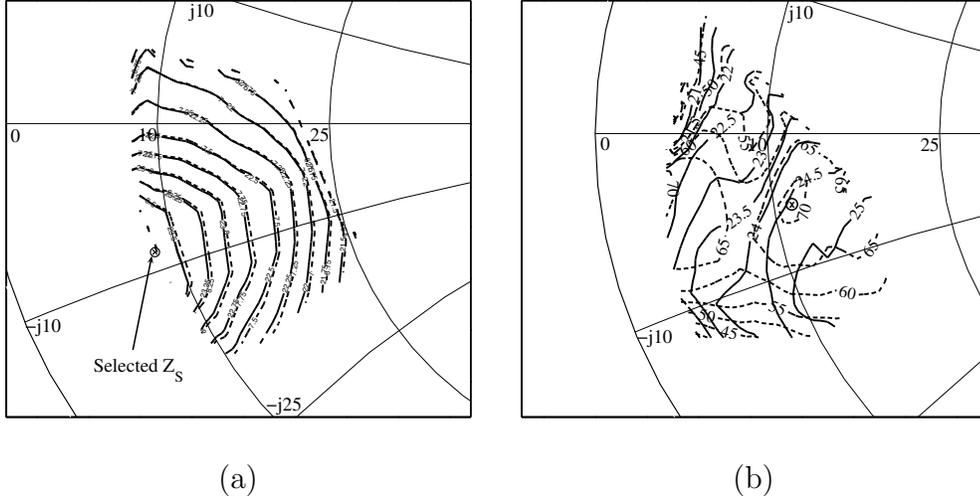
Figure 6.5: (a) Constant P_{OUT} (solid) and gain (dashed) source–pull contours for P_{IN}=16 dBm. (b) Constant P_{OUT} (solid) and η_D (dashed) load–pull contours for $P_{IN} = 16$ dBm. The measurement is performed at $V_{DS} = 5$ V and $V_{GS} = -0.35$ V. The optimal source and load impedances are shown (cross).
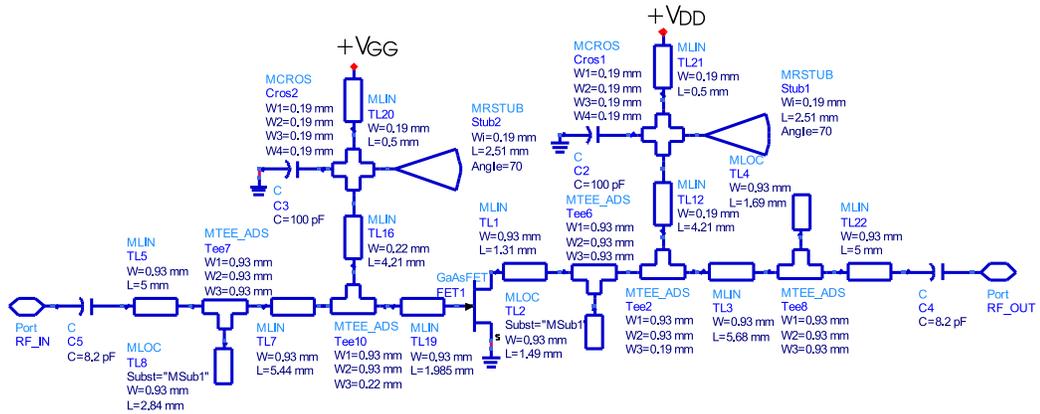
Figure 6.6: Schematic of the hybrid HEMT class-E PA. The PA is fabricated on 0.635 mm thick Rogers *TMM6®* substrate ($\epsilon_r = 6, \tan \delta = 0.0018$), with integrated bias–tees.
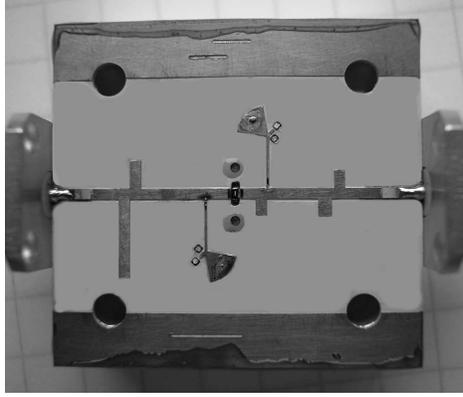
Figure 6.7: Photograph of the hybrid HEMT PA after postproduction tuning. Additional stubs are added in both input and output matching networks.

(a)

(b)
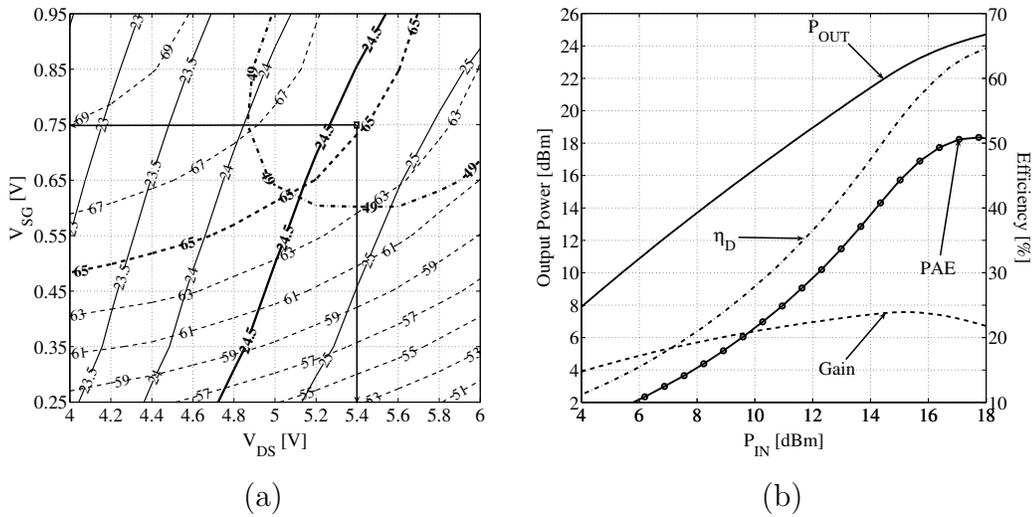
Figure 6.8: (a) Constant P_{OUT} (solid), η_D (dashed) and PAE contours of obtained through the automated bias/power sweep. Optimal bias point is set at $V_{DS} = 5.4\,\text{V}$ and $V_{GS} = -0.75\,\text{V}$. (b) Measured HEMT class–E power amplifier characteristics.

the edge of the tuning range of the available tuners. The addition of the bias lines slightly affects the characteristics of the HEMT and that also requires

compensation. However, the final load and source impedances do not differ significantly from the design, as shown in Table 6.1.

6.2.4 Performance Comparison

Table 6.1 summarizes final load and source impedances, C_{OUT} and bias points of each of the designed PAs. Relevant characteristics of the applied active devices are summarized in Table 6.2. HEMT and DHBT transistors dominate with available P_{OUT} and f_T and f_{MAX} characteristic frequencies over the MESFET. The measured P_{OUT}, gain, η_D (η_C) and PAE of the designed PAs are compared in Fig. 6.9 and Fig. 6.10 for varying input power. Since the HBT PA uses external biasing while HEMT and MESFET PAs have integrated bias lines, the loss in the biasing network and connectors is calibrated out in the following comparison.

Each of the PAs achieves optimal PAE at different power levels. The HBT PA dominates in gain, while the HEMT provides the highest P_{OUT}. Efficiencies of all three devices are comparable, reaching a 70% range. Table 6.3 shows the main paramaters of the DUT determined from the load–pull measurement and the actual PA characteristics compared at the corresponding input power levels. Again, insertion loss of the connectors, bias lines and the decoupling capacitors are calibrated out.

Frequency dependence of maximal output power P_{OUT} and drain (collector) efficiency is shown in Fig. 6.11. The MESFET PA exhibits the largest frequency bandwidth in both P_{OUT} and η. Namely, the optimal load impedance

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Table 6.1: Summarized PAs optimal load and source impedances and bias–points.

	Z_S [Ω]	Z_L [Ω]	Z_E [Ω]	C_{OUT} [pF]
MESFET	9.1+j24.4	35.9+j37	27+j31	0.11
DHBT	15.1-j0.5	15.8+j18.2	16+j18	0.185
HEMT	6.8-j2.14	11.3-j1	12.2+j14	0.24

	V_{IN} [V]	V_{OUT} [V],	I_Q [mA]
MESFET	-1.55	4.2	4
DHBT	0.35	4.35	0
HEMT	-0.75	5.4	0

Z_S and Z_L source and load impedances, respectively, after the postproduction tuning, Z_E - optimal class–E impedance based on C_{OUT} estimation. V_{IN} and V_{OUT} - optimal input and output electrode bias voltages, I_Q - quiescent output current.

Table 6.2: Compared active device performances relevant for high efficiency operation.

	f_T [GHz]	f_{MAX} [GHz]	V_{MAX} [V]	I_{MAX} [mA]	P_{O-A} [dBm]
MESFET	30	60	6	140	21
DHBT	80	150	18	200	26.5
HEMT	28	86	14	250	26.4

f_T–cutoff frequency, f_{MAX}–maximal frequency of oscillation, V_{MAX} and I_{MAX} - voltage and current maximal ratings, P_{O-A}–output power available in class–A.

being closer to 50Ω requires smaller output matching network transformation ratio, allowing for larger frequency bandwidth.

Harmonic levels and 2–tone IMD levels (1 MHz carrier spacing) are listed in Table 6.4 for the optimal output power levels for each of the PAs. The high suppression of the second harmonic in the output signal is due to harmonic
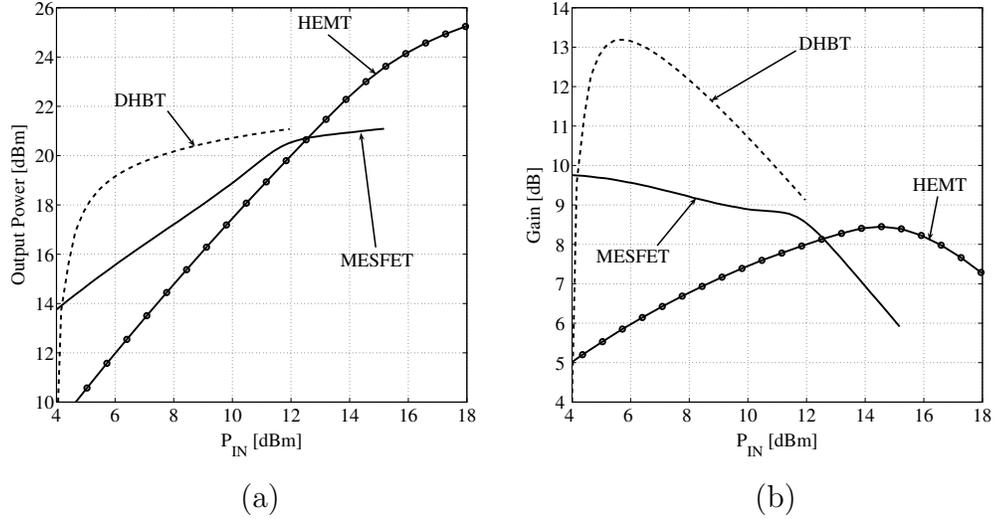
Figure 6.9: Comparison of measured P_{OUT} (a) and gain (b) of the hybrid high–efficiency PAs with MESFET (solid), DHBT (dashed) and HEMT (circles) active device. Presented characteristics are measured at the optimal bias points for each of the PAs.

Table 6.3: Compared load–pull and actual PAs performances.

	P_{OUT} [dBm]	G [dB]	η_D [%]
MESFET	20/20.8	8.05/7.9	70/71
DHBT	-/20.9	-/10	-/67.5
HEMT	24.5/24	8.75/8.2	70/65

P_{OUT} - output power from load–pull / actual PA output power, G - gain from load–pull / actual PA gain, η_D - efficiency from load–pull / actual PA efficiency.

traps in output matching networks. The summarized general characteristics are given in Table 6.4.

Harmonic and intermodulation levels of the HEMT PA are not measured due to the active device failure.

The linearity of the PAs can be improved if the amplitude and phase
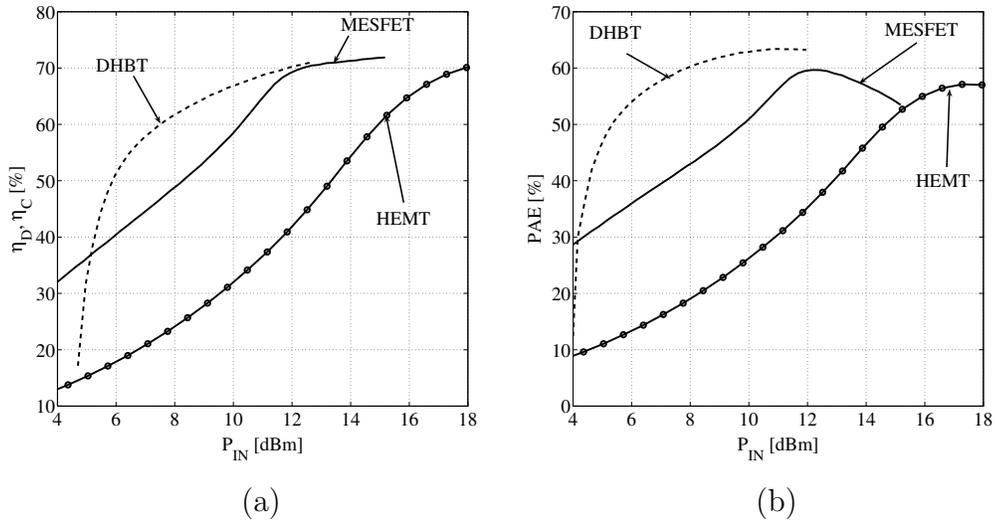
Figure 6.10: Compared η_D (a) and PAE (b) of the designed hybrid high–efficiency PAs.
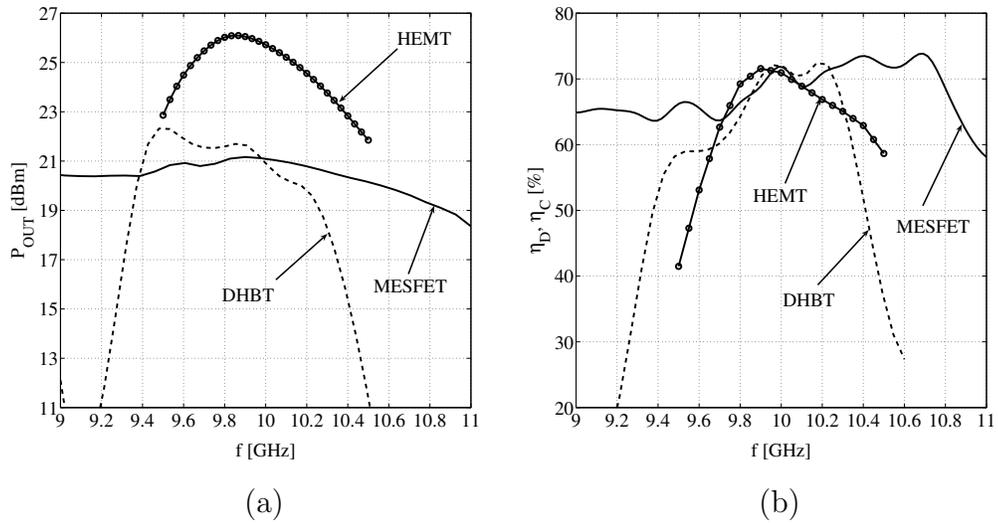
Figure 6.11: Measured frequency dependence of: (a) P_{OUT} and (b) η_D. Maximal values at each frequency are shown.

Table 6.4: General characteristics of 10–GHz high–efficiency hybrid PAs.

	P_{OUT} [dBm]	G [dB]	η [%]	PAE [%]	BW [GHz]
MESFET	20.6	8.3	70.1	59.6	8.75–10.95
DHBT	20.9	10	68.8	63.4	9.69–10.35
HEMT	25.2	7.3	70.1	57	9.67–10.47

	$2f_0$ [dBc]	$3f_0$ [dBc]	$IMD3$ [dBc]	$IMD5$ [dBc]	CD [dB]
MESFET	-49.7	-23.5	-11	-16.5	1.5
DHBT	-32.8	-26.9	-13	-21	3.3
HEMT	-	-	-	-	1.2

P_{OUT}–output power, G–power gain, η–drain/collector efficiency, PAE–power added efficiency, ρ_{IN}–input reflection, BW–frequency bandwidth for $\eta \geq 60$ [%] and $2f_0$ and $3f_0$ - harmonic levels relative to the carrier, $IMD3$ and $IMD5$ - third and fifth order intermodulation product levels, CD - compression depth at optimal P_{OUT}.

of the input signal are provided through the bias and the drive of the PA, respectively (Envelope Elimination and Restoration (*EER*) [14, 62]). In an ideal class–E PA the dependence of output voltage on DC supply voltage ($V_{LOAD}(V_{DC})$) is a straight line through the origin, and the carrier phase at the output tracks the carrier phase at the input. In a realistic PA, a relevant nonideality is the deviation of $V_{LOAD}(V_{DC})$ from a straight line. This is described with AM–AM measurements which can be used to correct for the nonideality. In addition, for $V_{DC} = 0$ V there is a nonzero output voltage, referred to as "feed-through". Furthermore, the output carrier phase is dependent on the DC supply voltage and therefore does not track the input phase exactly. This is described with AM–PM measurements which, if known *a priori* can also be used to improve performance. Fig. 6.12 shows the AM–

AM and AM–PM measured characteristics of the MESFET and HBT class–E
PAs for optimal levels of P_{IN}.

(a)   (b)
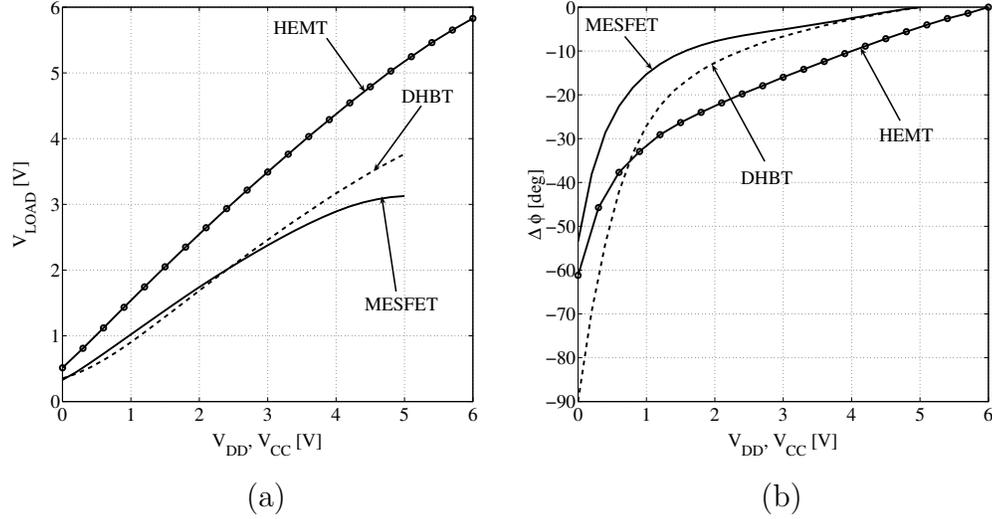
Figure 6.12: (a) Load voltage dependence on drain (collector) voltage; (b)
Relative phase dependence on drain (collector) voltage. Input power is kept
constant, for MESFET at 12.4 dBm, for HBT at 11.4 dBm and for HEMT
at 18 dBm. The measurements are performed at 10 GHz, with constant gate
voltage.

For each amplifier, the corresponding four–dimensional data sets (V_{LOAD},
V_{DC}, $\Delta\phi$ and P_{IN}) can be pre–loaded into FPGA lookup tables to control the
fast DC–DC converter in the biasing circuit [62]. In *EER* mode of operation,
a transfer characteristic from the bias supply voltage to load voltage (G_{EER})
is a relevant parameter, defined as

$$G_{EER} = 20\log(\frac{V_{LOAD}}{V_{DC}}) \tag{6.8}$$

where V_{LOAD} is the voltage across a 50-Ω load resistance and V_{DC} is the drain (collector) DC supply voltage. The frequency dependence of G_{EER} is shown in Fig. 6.13. The EER characterization was done with Ms. Narisi Wang at the University of Colorado and the details will be presented in her doctoral thesis.
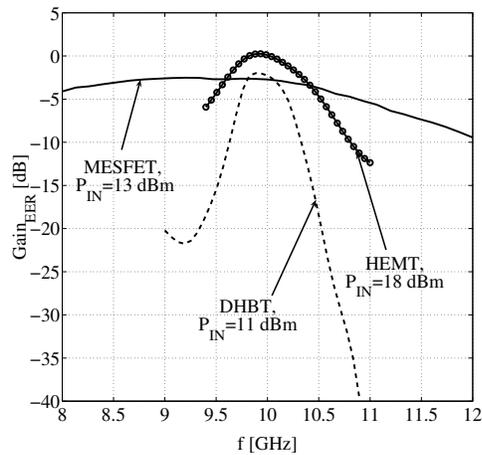
Figure 6.13: The G_{EER} for MESFET (solid), HBT (dashed) and HEMT Class–E PA (circles) at nominal bias point and optimal P_{IN}.

6.2.5 Discussion

All three implemented high–efficiency PAs reach expected saturated power levels with efficiencies above 65%, exhibiting relatively high power gain and good input matching conditions. Due to the higher f_T and f_{MAX}, the HBT PA has approximatelly 1.7 dB higher gain, resulting in a higher PAE than other PAs. However, since at 10 GHz all three PAs are operating considerably below their f_{MAX}, the effect of the transistor speed (proportional to f_{MAX})

on the PA efficiency is not very distinct. This confirms the "rule–of–thumb" that $f \leq \frac{f_{MAX}}{6}$, mentioned in Chapter 2. The higher I_{MAX} values and larger output breakdown voltage allow HBT and HEMT PA operation at higher P_{OUT}, although in this study the output voltage is kept in the safe range in order to avoid possible device damage. The consequence is that the HBT PA operates considerably below its actual power limits. This study confirms that the HEMT and HBT transistor technologies offer better performances (potentially higher P_{OUT} and gain) than MESFET for high–efficiency PAs in the higher microwave range.

Another difference between the PAs is in the shape of power–sweep characteristics. The MESFET PA shows typical high–gain behavior for small signal levels, monotonically compressing as the input power increases. Contrary to that, the gain of the HBT and HEMT PA exhibits considerable gain expansion for small signal levels, followed by a similar steady compression. The reason for that is that for optimal efficiency the HBT and HEMT PA need to be biased slightly below their thresholds. Due to the lower source and load impedances of the HBT and HEMT PAs, the efficiency and power bandwidths are considerably lower than for the MESFET.

Finally, the HBT PA exhibits the largest AM–PM conversion of all three PAs, with similar feed–through voltage into a 50–Ω load. The *EER*–related parameters are compared in Table 6.5, from which it can be concluded that the MESFET class-E PA is the most amenable to broadband EER operation.

Table 6.5: Compared EER characteristics of 10–GHz high efficiency hybrid PAs.

	P_{IN} [dBm]	V_{LOAD} [V]	V_{F-T} [V]	$\Delta\phi[°]$	EER_{BW} [GHz]
MESFET	12.4	0.33–3.13	0.33	-53	8.1–10.5
DHBT	11.4	0.35–3.77	0.35	-105	9.8–10.1
HEMT	18	0.51–5.83	0.51	-61	9.7–10.2

P_{IN}–input power for maximal V_{LOAD} range, V_{LOAD}–range of load voltage, V_{F-T}–"feed-through" voltage for optimal P_{IN} at 10 GHz, EER_{BW}–frequency bandwidth for $G_{EER} > -1$ dB.

6.2.6   PA Phase Noise Measurement

Phase noise is a random fluctuation of an oscillator or amplifier output signal phase caused by many different effects that occurs within the active device it self, such as for example up-converted flicker noise. Insufficiently filtered bias supply also contributes to the flicker noise. Although local oscillators are the main sources of the phase noise, it occurs in amplifiers as well. In modern communication systems with multilevel amplitude/phase modulation (QPSK, M–QAM, M–PSK) the transmitted information is encoded in both phase and amplitude of the carrier. While amplitude noise affects amplitude detection, the phase noise affects carrier phase detection required for coherent demodulation [15]. The presence of phase noise practically limits the data rate that can be achieved using such a transmitter for the predetermined bit–error–rate (BER). Another negative effect is frequency bandwidth spreading due to unwanted phase modulation of the carrier caused by noise. The transmitted signal can occupy larger bandwidth than allowed, possible

affecting the transmission in the neighboring channels. The phase noise has probably the largest impact in Doppler radar systems where the received signal from the moving objects can be entirely covered by the phase–noise induced spectral skirts of the clutter signal.

It is well known that phase noise of an oscillator can be reduced by operating the active device in a quasi linear regime, avoiding deep gain compression. Similar holds for PAs. As explained in Chapter 1, class–E PAs require operation in deep compression (3–5 dB). Hence, it is interesting to examine degradation of the phase noise of microwave PAs due to operation in switched mode. So far there has been only one study of such phenomenon [84], performed on a MESFET PA, operating at a lower microwave frequency. The following study offers a comparison of measured phase noise of PAs designed with different device technologies, operating at 10 GHz. The MESFET and HBT PA described in the previous section are used as class–E representatives. In addition, a class–A MESFET PA is also designed using a small signal approach [13]. Single sideband (SSB) phase noise is measured using a discriminator method [85]. The preliminary results are shown in Fig. 6.14.

As expected, the deeply compressed operation of both class–E PAs results in increased phase noise. The DHBT PA has lower close–to–carrier noise (contribution of the 1/f noise) than the MESFET, which is a typical characteristic of bipolar devices.

The gain compression of the active devices for class–E operation is unfortunately unavoidable. In applications where the efficiency and the phase

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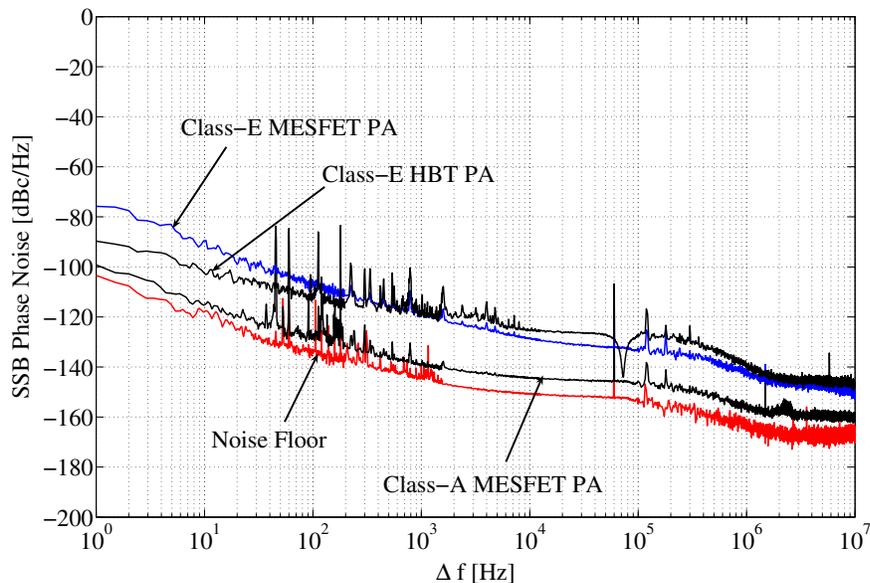
Figure 6.14: Measured SSB phase noise of the MESFET and DHBT class–PAs. The noise floor of the measurement system is shown in gray. Spikes visible in the spectral density are results of power grid interference (60 Hz and harmonics), requiring better EM isolation of the measurement system and the PAs which includes use of a battery or linear power supply.

noise are both important a trade-off between them has to be performed. As a proposal for future work, a PA phase noise measurement system can be embedded within a harmonic load–pull system. Using simultaneous measurements of the phase noise, P_{OUT} and efficiency, the contours of constant parameters can be found and used to perform required trade-offs in the design.

Chapter 7

Related Work

Class–E microwave PAs designed using the presented methodology were used for different applications. First, an amplifier designed using the analytic approach (Chapter 1) took part in the implementation of a bias/power control circuitry. As predicted in Subsection 1.3.6, the high efficiency of the PA is maintained over a broad range of output powers by varying the output bias voltage [86]. A similar PA is used in a prototype PA with implemented EER technique, through which the linearity of the highly compressed class–E PA is improved [62].

In order to entirely eliminate the need for manual tuning of a designed class–E PA, integration of a MEMS–based tunable output matching network with such a PA is attempted. The initial results of the tunable class–E PA are presented, showing that extremely low loss tuning networks could benefit high efficiency PA tuning. Finally, a mode–tuned PA that switches

between E and A classes of operation depending on the signal parameters is demonstrated.

7.1 PA Output Power Control

In a wireless communication system the average output power of a front–end needs to be controlled. Modern systems are able to vary the average power level on a slow time scale (on the order of milliseconds) to compensate for variable channel propagation properties (presence of other user signals, distance to the base station, multipath environment, etc). Output power is typically controlled by an automatic gain control loop (AGC). Power is sensed at the PA output and compared with the reference signal. The error signal is used to control a variable attenuator in the RF signal path, thereby varying the drive to the main output PA. The problem with this approach is the well known decrease of PA efficiency on the deviation as the output power level varies [4]. This is also true for output stages with class–E PAs [4, 86].

An alternative approach commonly encountered in the case of linear PAs used in communication handset is bias control. As shown in Section 1.3, if the PA operates in class–E it is also possible to control its output power level by varying the output bias voltage, without affecting the efficiency. The reason for this is that load voltage is linearly proportional to the drain supply voltage in ideal class–E PA, while the optimal load impedance is not

a function of the power level. Using an X–band class–E MESFET PA, a power control system is implemented as shown in Fig. 7.1.
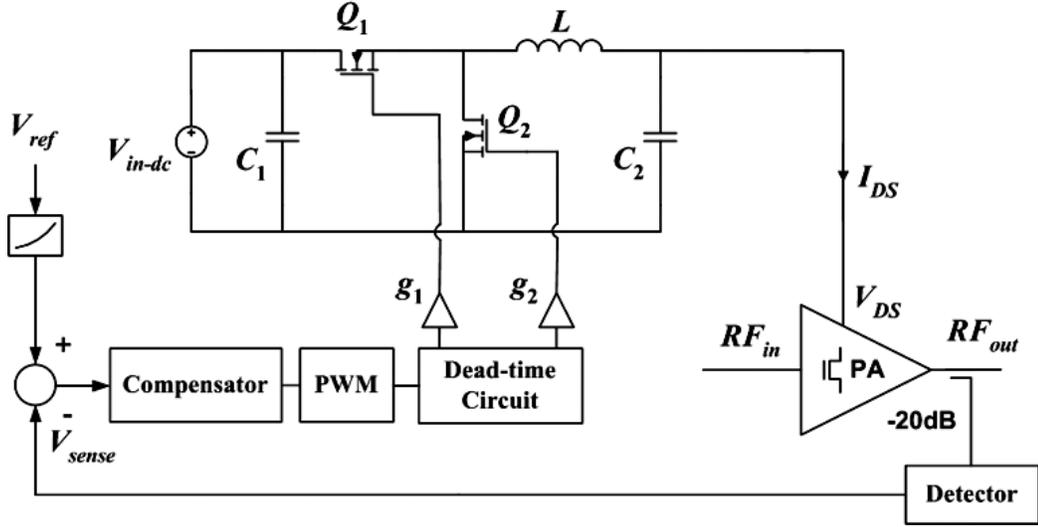
Figure 7.1: Block diagram of the class–E PA output power control system.

Drain bias voltage of the PA is adjusted by an extremely efficient Buck DC–DC converter (95% conversion efficiency at 200 kHz switching frequency [86]). The MESFET's output bias is controlled by a feedback loop closed around the PA, the compensator and the convertor. The error signal that controls the convertor's duty cycle is provided by comparing the reference voltages V_{REF} and V_{SENSE}. The feedback loop tracks the variations in reference signal and sets the output PA power accordingly.

V_{SENSE} is proportional to the output signal envelope and is provided by a microwave detector circuit. The detector is integrated with a class–E PA, designed using the extracted C_{OUT}. The PA is very similar to the one used in

Chapter 3 (Fig. 7.2(a)), with the addition of the bias lines and DC decoupling capacitors. A low–loss 20–dB directional coupler samples the output power. A matched Schottky diode detector rectifies the signal and generates a DC voltage proportional to the PA's output power.

| (a) | (b) |
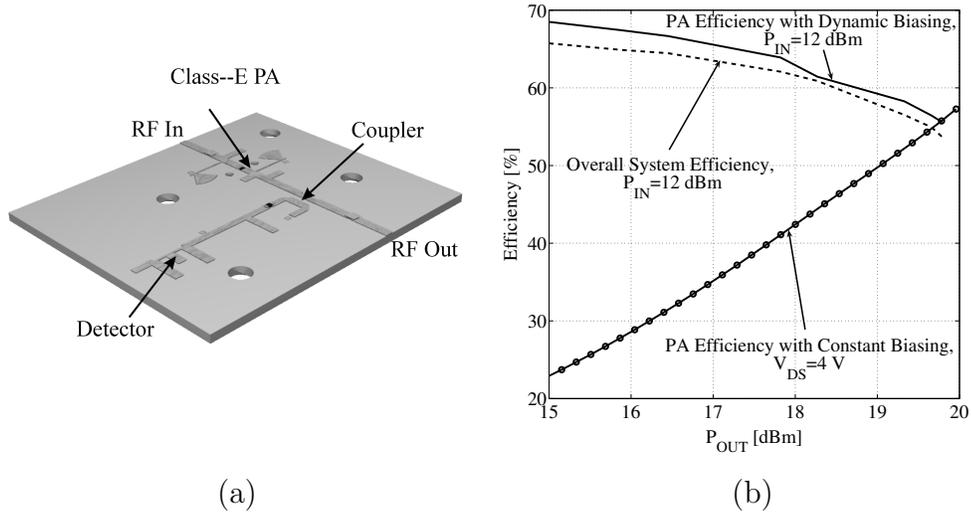
Figure 7.2: (a) Schematic of the integrated class–E PA and microwave detector circuitry. Class–E PA is with bias lines and DC decoupling capacitors. (b) Measured efficiency for the PA with constant drain bias of $V_{DS} = 4\,\text{V}$ (circles), the PA with manual drain bias control (solid line) and the entire closed loop system when the connector loss and coupler loss is calibrated out (dashed line) [86].

The effect of power control on the PA drain efficiency is demonstrated in Fig. 7.2(b). Without the control, the PA exhibits a steep efficiency drop with a decrease in P_{OUT}, resulting in an average efficiency of 41.2%. With bias control applied, the drain efficiency of the PA remains almost constant with P_{OUT} decrease, at the average level of 62%. If the loss in DC–DC

convertor and controling circuitry is included, the average power efficiency of the system remains above 60.4% [86]. The bandwidth of the system is currently limited by the DC–DC convertor bandwidth of 12 kHz, which is sufficient for output power regulation for most of existing systems [58].

An implementation of a class–E PA with EER linearization that expands the power control principle to allow amplification of variable envelope signals can be found in [62]. It utilizes the same PA developed for this Section.

7.2   Tunable Class–E PA

The methodology for systematic microwave class–E PA design presented in the previous chapters allows for significant reduction in PA design time even in the case when the nonlinear models for the active devices are not available. However, in any of the proposed design paths some amount of the postproduction tuning is almost always necessary. The reason for this is primarily the active device characteristics spreading, as well as the finite matching/biasing networks fabrication and mounting tolerances. On the other hand, a careful load–pull approach followed by pretuning requires a considerable investment in hardware (load–pull system), software for the measurement system control and time required to follow the proposed procedures.

As explained in Chapter 1, PA development is reduced to matching networks design and tuning, based on data provided by the device characterization. An alternative to this approach is the integration of tunable low–loss

matching networks within the PA [87, 88, 89]. This approach became feasible after the recent progress in MEMS devices, such as RF switches and variable capacitors. These devices enable variable matching networks that can produce a discrete (MEMS switches) or continuous (MEMS capacitors) set of the impedances. Initial work has been done on this subject resulting in an integrated class–E PA with a discrete–impedance MEMS tuners. The work is done in collaboration with Prof. John Papapolymerou's group at Georgia Institute of Technology (GIT).

The main limiting factor for this application is the tuner insertion loss IL, that can be calculated as:

$$IL = \frac{P_{IN}}{P_{OUT}} = \frac{1 - |\Gamma_{IN}|^2}{|S_{21}|^2} \frac{|1 - S_{22}\Gamma_L|^2}{(1 - |\Gamma_L|^2)} \tag{7.1}$$

In this equation Γ_L is the power probe input reflection coefficient, Γ_{IN} is the input reflection coefficient of the matching network with integrated tuner and S_{21} and S_{22} are the S–parameters of the matching network.

If the active device operates with a drain efficiency η_D, the overall drain efficiency (η_{D-TOT}) that includes loss in the output matching network is:

$$\eta_{D-TOT} = \frac{\eta_D}{IL} \tag{7.2}$$

An allowed insertion loss (in decibels) that causes an efficiency reduction of $\Delta\eta = \eta_D - \eta_{D-TOT}$ of the active device with η_D efficiency can be calculated

as:

$$IL_{MAX}[dB] = -10\log(1 - \frac{\Delta\eta}{\eta_D})\tag{7.3}$$

For a typical class–E PA operating at X–band, η_D is 70% (Chapter 6). If the reduction in drain efficiency of 5% is tolerable, the maximal insertion loss of the output matching network is 0.32 dB. As can be seen in the class–E PA sensitivity analysis (Fig. 3.9, Chapter 3) this corresponds to a relatively large range of allowed impedances. Therefore, if the tuner loss is larger than this value it is not justifiable to replace a fixed matching network having even a relatively large fabrication tolerances with such a tuner.

A schematic of the designed class–E PA with an integrated tuner is shown in Fig. 7.3(a). Based on the simple class–E theory and extracted C_{OUT}, target load impedance for the chosen MESFET (AFM042P by Alpha Industries, Inc.) is calculated to be $Z_E = (27 + j31)\Omega$. The PA input matching, second harmonic output termination and the bias are designed on a 0.635–mm thick Rogers TMM6 ® substrate ($\epsilon_r = 6$, $\tan\delta = 0.0018$). An output tuner is designed and fabricated on a silicon substrate ($\epsilon_r = 11.7$, $400\,\mu$m thick). The tuner (Fig. 7.3(b)) consists of a main 50–Ω RF transmission line with the six different–length microstrip shunt stubs and MEMS switches attached to their ends. When the switch membrane is lowered down (by applying a DC potential difference between the membrane and an isolated electrode underneath) it establishes the RF contact between the microstrip stub and

<div align="center">(a)   (b)</div>
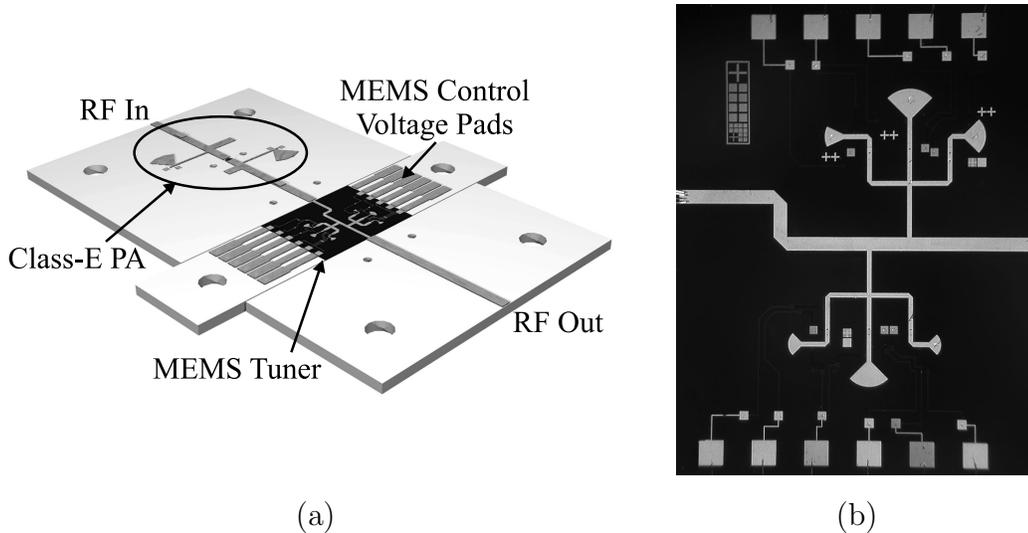
Figure 7.3: (a) Class–E PA integrated with the discrete MEMS tuners. (b) Fabricated MEMS tuner on high–resistivity silicon. Biasing of the PA is provided through integrated bias lines, while the MEMS actuation voltage is provided through high–resistivity bias lines integrated with tuner. PA's 50–Ω RF line serves as the actuation DC voltage reference, DC–decoupled from PA drain supply by a millimeter–wave DC capacitor of $8.2\,\mathrm{pF}$.

the appropriate radial stub acting as an RF ground. There are 64 possible states that spans the tuner impedance coverage around the target class–E impedance as shown in Fig. 7.4.

An expected MEMS actuation voltage is $\approx 30\,\mathrm{V}$. Since the electrodes are DC isolated and the charging and discharging capacitances are on the order of femto Farads, the required supply current is negligible. Therefore, tuner switches in principle do not contribute to the decrease in efficiency of the entire system, providing that highly efficient DC–DC switching converter is available.
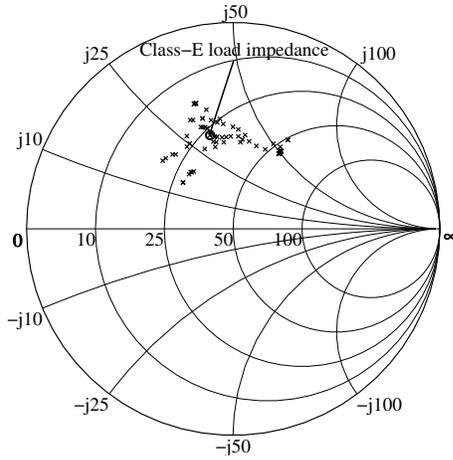
Figure 7.4: Simulated tuning range of the output matching network. S–parameters of the MEMS tuner are obtained using Agilent *Momentum*® simulation of the tuner structure.

The fabricated tuner was mounted on a TRL–calibrated test fixture using silver epoxy. It was wire–bonded to the PA's RF output and the actuation voltage pads. The measured S–parameters of the tuner are combined with the output matching network response and shown in Fig. 7.5 [90].

The measurements of the prototypes revealed several fabrication problems resulting in relatively poor initial performance:

- Several switches were nonoperational, reducing the available tuning range. Some of the switches showed a tendency toward being stuck at the "short" position, requiring application of a high DC voltage for forced release, or a time interval of several minutes in order to discharge the switch and other capacitances and return to the initial position;

- Considerably larger than expected voltage for switch actuation is re-
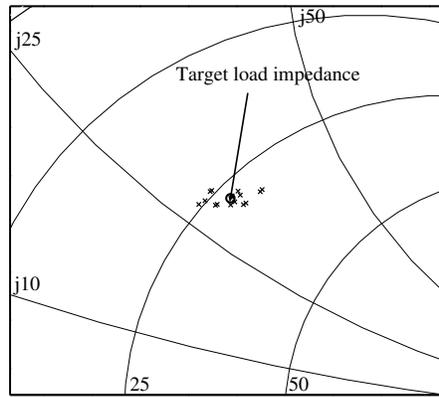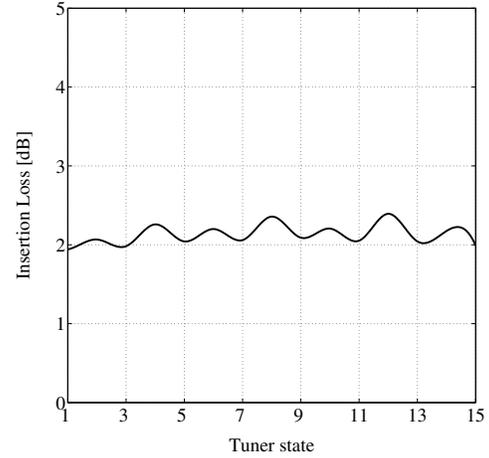
<div align="center">(a)   (b)</div>

Figure 7.5: (a) The tuning range of the output matching network with measured integrated MEMS tuner. Only 4 of 6 switches were operational, resulting in 16 possible tuner states. (b) The calculated insertion loss of the output matching network. Most of the loss is contributed to the MEMS tuner.

quired (80–100 V), due to the higher mechanical stiffness of the switch membrane and thicker DC isolation layer underneath;

- The actual tuner impedance range is different than the simulation predicts, and sensitive to fabrication tolerances. An additional fixed pre–matching stub is required on the PA substrate to correct for this. A possible cause is inaccurate modeling of the MEMS switch as pure "open" and "short" circuits;

- The insertion loss of the tuner at some of the switch–states exceeds a level of 2 dB, which is significantly above the expectation. A possible

cause for this is the loss in MEMS switches due to the impurities in the used materials and a degradation of the switch characteristics due to exposure to the atmosphere. This is related to a problem encountered with application of the silver epoxy for the tuner attachment. Namely, it was found that the out-gassing of the epoxy components during the curing interval deposits an unwanted layer on adjacent MEMS structures, affecting good contact between switch plates. Another possible reason is RF loss in high resistance DC bias lines used to provide DC actuation voltage. Some indications that the insertion loss is sensitive to the position of the switches within the tuner are observed;

- Since they are unpackaged, the tuners are sensitive to the general transportation and handling conditions. They need to be kept in a pressurized nitrogen chamber in order to avoid a quick aging process.

Currently, improvements in the MEMS tuner fabrication and storing are expected. The epoxy outgassing problem can be eliminated if the tuners are packaged. The silver epoxy attachment can also be eliminated by using, for example, indium soldering or a pure mechanical attachment.

7.3 Reconfigurable Microwave PA

A reconfigurable microwave PA can be viewed as a component of an "intelligent front–end". It is the core of a system that is able to adapt its operation

to the properties of the transmitted signal. This PA is a further extension of the tunable PA presented earlier. A block diagram of the system is shown in Fig. 7.6.
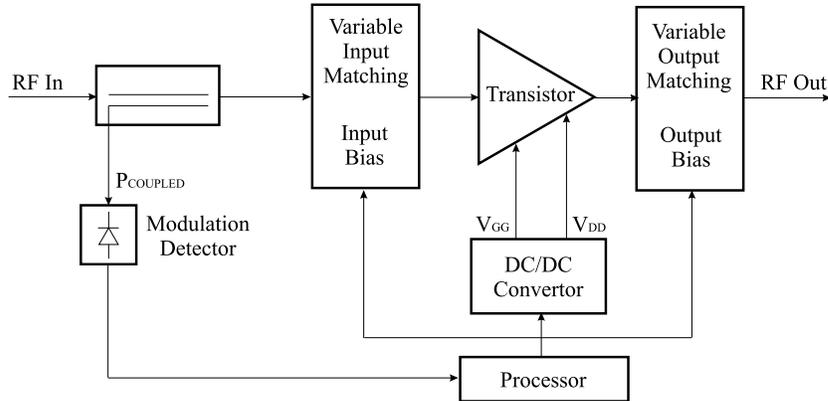
Figure 7.6: Block diagram of the intelligent front-end PA. The PA is integrated with MEMS–based variable matching networks.

The input signal is sampled by a directional coupler and its envelope is detected using a microwave detector, similar to one used in Section 7.1. If the variations in the input signal envelope are detected, the active device bias point, source and load impedances are set to the optimal linear (class–A) matching/biasing condition. In the case of a constant envelope input signal the bias and active device source and load impedances (at fundamental and second harmonic frequency) are reconfigured to the values optimal for class–E operation.

A 10–GHz prototype PA with reconfigurable matching networks that is able to switch between different classes of operation is designed together with Patrick Bell (Ph.D. candidate at the University of Colorado). The networks

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incorporate microwave MEMS switches developed by Sandia National Laboratories, where the tuner prototype is fabricated. The active device used for the PA design is GaAs MESFET AFM04P2 (Alpha Industries, Inc.). The optimal impedances for class–A and class–E are determined using the load–pull and summarized in Table 7.1.

Table 7.1: Source and load impedances for the reconfigurable PA.

$Z_S\,[\Omega]$	$Z_{L-A}\,[\Omega]$	$Z_{L-E}\,[\Omega]$
9.1+j24.4	26.6+j15.3	35.9+j36.6

Z_S - source impedance, Z_{L-E} - class–E load impedance, Z_{L-A} - class–A load impedance.

The active device is attached to the via–grounded pad using silver epoxy and wire–bonded to the input and output matching networks. The load–pull characterization is performed on the active device mounted on a similar test fixture, in order to include bond–wire and mounting parasitics.

A schematic of the reconfigurable output matching network is shown in Fig. 7.7(a). Shunt stubs are loaded with integrated MEMS switches. Switch in the "down" position effectively extends the shunt "open–circuit" stubs. With both switches "down", a class–A optimal load impedance is presented to the active device. When both switches are "up", a class–E load impedance is presented, as well as the proper second harmonic termination. Source impedance for both classes of operation is very similar so that the tuning of the input matching network is not required. A photograph of the reconfigurable PA is shown in Fig. 7.7(b).
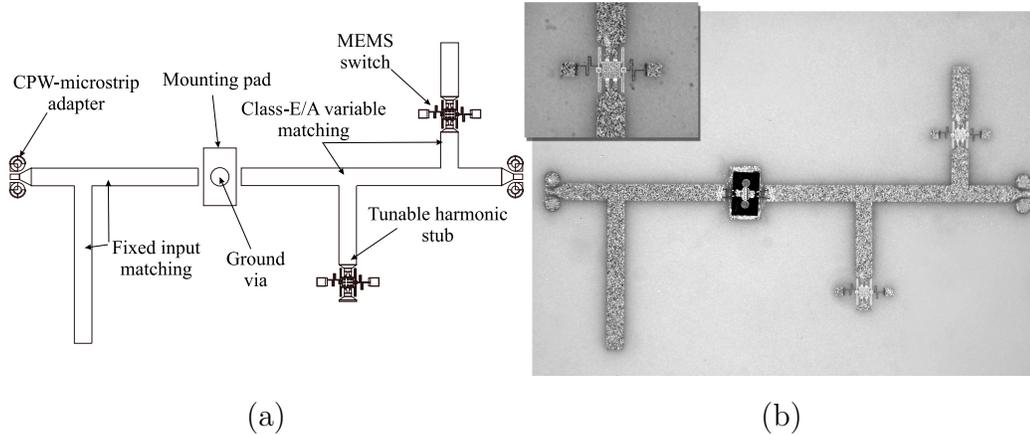
Figure 7.7: (a) Schematic of the reconfigurable output matching network with integrated MEMS switches. The network is fabricated on Alumina substrate ($\epsilon_r = 9.8$, 0.508 mm thick). (b) Photograph of the designed Class–A/E PA with integrated MEMS tuner. Detail of the MEMS switch is shown in the inset.

The simulated and measured impedances of the input and output matching networks at 10 GHz are shown in Fig. 7.8(a). Measured insertion loss of the output matching network is 0.16 dB and 0.28 dB for class–A and class–E load impedances, respective, while the simulated insertion loss is 0.06 dB and 0.17 dB, respectively.

Although a different process was used for the reconfigurable PA fabrication, the resulting tuner suffers from similar problems as the tuner presented in Section 7.2. Initial measurements reveal correct impedance states achieved by the output matching network. The insertion loss of the tuner is considerable lower that in the case of the tuner used for the tunable PA, indicating a more mature fabrication process. However, the MEMS switches are however

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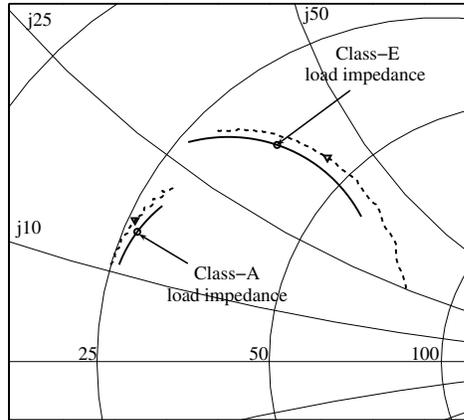
Figure 7.8: Measured (dashed) and simulated (solid) load impedances for class–A and class–E [91].

sensitive to the silver epoxy outgassing, quickly degrading and increasing the insertion loss. Power measurements of the entire PA are a part of future work.

Chapter 8

Conclusion and Future Work

8.1 Thesis Summary

The core of the work presented in this thesis is the established methodology applicable for the design of any kind of harmonically terminated microwave PAs, in particular for class–E PAs. The proposed approach considerably minimizes PA development time and assures that the selected load and source impedances result in an optimal relationship between the output power, gain and efficiency.

In the first two chapters the elementary class–E theory was reviewed, with addition of a simple set of formulas useful for PA dimensioning. A theoretical basis for class–E PA output power control through bias variation is presented. It also serves as a background for the EER linearization. The main nonidealities of a real microwave active device are addressed including mounting and

wire–bonding parasitics. A useful small signal model extraction algorithm supported by optimization is outlined in Appendix A.

In Chapter 3, the design of a spatial combiner of 16 switched mode PAs with a high element and high PCE is presented. Most of the problems encountered in the previous design attempts (heat removal, uniform input signal and bias distribution, stability, sensitivity to the antenna parameter variations [52, 44, 92]) are addressed and successfully solved. This chapter also includes a realistic microwave class–E PA fabrication tolerance analysis, based on a modified large signal model of the applied GaAs MESFET.

A load–pull design methodology augmented with a pre–tuning strategy is presented in Chapter 4. A self–contained set of equations that the load–pull method is based on is given in Appendix B. Two example PAs are designed, fabricated and characterized: a 60–W W–CDMA base station PA and an X–band class–E PA.

After a cost/benefits study of cascading high–efficiency PA stages (Chapter 5), a 10–GHz two stage class–E PA is successfully designed, optimized and characterized. The class–E microwave PA power gain is doubled while maintaining output power level and high efficiency operation. A basic characterization of the PA for EER linearization scheme is also performed. A possibility for feed–through voltage cancellation using such an amplifier is proposed.

Representatives of the three main active device technologies (GaAs MESFET, InP DHBT and GaAs pHEMT) are used for class–E PA design and

their performances are compared in the Chapter 6. This includes EER characterization, as well as phase–noise measurements, for the first time considered at these frequencies.

The output power control of a microwave class–E PA is demonstrated in Chapter 7. As the equations presented in the Chapter 1 predict, it is possible to maintain high efficiency of a class–E PA over a wide range of output power levels. This work served as an initial point for full EER linearization system implementation, described in detail in [62].

In order to entirely eliminate the somewhat tedious load–pull methodology and postproduction tuning of class–E microwave PAs a concept of a tunable microwave PA is presented. It is based on an integrated MEMS–based tunable matching network. In the last part of the chapter design and initial measurements of a reconfigurable class–E/class–A PA are presented as a part of an "intelligent front end".

8.2   Original Contributions

The author's original contributions presented throughout this work are:

- Established and verified a systematic load–pull based design procedure for class–E microwave PA design. The procedure considerably decreases the time for development of class–E and other types of PAs. With the addition of a proposed pretuning strategy accompanied with EM modeling of the circuit discontinuities, high–power amplifier design for

any purpose is considerably shortened;

- Solved the heat generation/removal problem in X–band 2–dimension active antenna array by integrating robust switched–mode class–E microwave PAs with an optimized broadband stacked–patch antenna element, minimizing fabrication tolerances. The array exhibits the record average amplifier efficiency and very good power combining efficiency. Solved uniform amplifier feed / biasing problem by implementing a corporate feeding network and a common drain–biasing layer;

- Developed the first two–stage class–E microwave PA, doubling the power gain while maintaining high efficiency of operation;

- Presented the first comparative study of three main active device technologies for class–E PA design, in particular for EER applications. This includes the first phase–noise measurements of the highly compressed PAs at these frequencies;

- Developed (in collaboration with Patrick Bell, University of Colorado) and initially characterized the first tunable and reconfigurable 10–GHz class–E PAs.

8.3   Proposed Future Work

The most important part of the proposed future work is further improvement in tunable and reconfigurable PAs. The idea of possible elimination of

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the load–pull, postproduction tuning or even a very approximate microwave device characterization (required for first–pass class–E PA design) is very attractive.

In the case of the tunable PA, better modeling of the MEMS switches is required. Probably the best way would be to perform TRL–calibrated measurements on a single shunt microstrip stub with a single MEMS switch attached (this includes corresponding radial stub and high resistance bias lines). The switch and adjacent components can then be modeled by a single–port S–parameter data block in Agilent $ADS^®$. The parameters of the data block can be determined through optimization and included in a circuit simulator.

Further testings of the tuner insertion loss, power handling capability and reliability are of great interest. If a required improvement in the tuner insertion loss (determined by Eq. 7.3) cannot be achieved, the tuner still can be used for initial PA characterization as a cheap short–term alternative to a commercial load–pull system. After that it can be replaced by a fixed matching network. In addition, a MEMS tuner can be used in the systems where PA's load impedance significantly varies. This is the case of an antenna in a wireless communication handset or in a spatially oversampled steerable antenna array.

It is well known from low RF frequency high–power PAs design practice that the position of lumped components in both input and output matching networks greatly influences the insertion loss. The corresponding study of the

MEMS tuner topologies (in order to determine optimal position for the tuning elements) has not been performed so far. Such a study can be potentially very interesting in order to further minimize insertion loss of the microwave tuners.

In the case of a reconfigurable PA, power measurements need to be performed in order to verify the PA operation, as well as the tuner RF power handling capability. Part of the future work is integration with a highly efficient bias controller and the modulation detector, followed by stand–alone system testing.

Future work related to tunable and reconfigurable PAs also includes design of an interstage matching MEMS tuner, in order to simplify the tuning procedure for multistage PA design (Fig. 8.1(a)). As explained in Chapter 5 the input impedance of the second stage is generally not known. In absence of a good nonlinear model or equipment for large signal network analysis it is difficult to perform *a priori* design of the interstage matching network. *A posteriori* optimization of a two–stage PA is also an involving task due to active devices nonunilaterality.

However, a variable tuning network can be designed to perform the transformation of the estimated second stage input impedance range into impedance range centered around the optimal load impedance required by the first stage, as shown in Fig. 8.1(b).

After such a PA is assembled, an automated impedance search (similar to load–pull supported by a gradient optimization) can be performed on
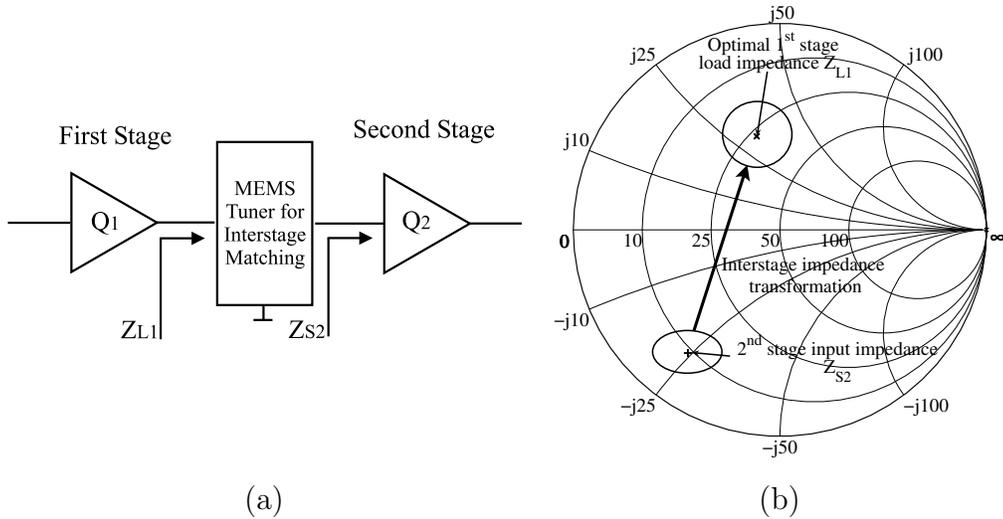
Figure 8.1: (a) Schematic of the interstage matching network with integrated MEMS tuner (b) Range transformation between the second stage input impedance and the first stage load impedance.

the integrated variable interstage matching network, in order to find the optimal transformation state. Then, a fixed interstage matching network with minimal insertion loss can be designed to replicate the tuner impedance transformation property.

The interstage tuner can be realized with varactor diodes or MEMS variable capacitors for a continual tuning range, or with MEMS switches for a discrete range. It is clear that a single tuner cannot perform arbitrary impedance transformations between points in the tuning ranges shown in Fig. 8.1(b). Different tuner topologies will be required and this can be the subject of further study. In addition, the interstage tuner in principle can be used to control harmonic content of the signal that propagates between the

first and the second stage. This can be achieved by presenting controllable impedances at the higher harmonics, both to the first and the second stage. This opens a new field of research in harmonic interstage optimization and wave–shaping.

In the general area of microwave class–E PAs, further research of frequency limits is needed. Currently, the class–E PA's are successfully designed up to 12.5 GHz, using the methodology described in this work. With the availability of new active technologies (in particular InP HEMTs and HBTs), this boundary can be pushed farther. The same is true for power increase, with the availability of wide band–gap microwave active devices.

A preliminary investigation of the frequency bandwidth of microwave class–E PAs is performed by Narisi Wang (University of Colorado) and the author. It reveals that harmonic reactance presented to the PA affects optimal class–E impedance, as well as the maximal output power. This has significant impact on a potential broadband class–E matching network design. It is also very interesting to investigate bandwidth limitations of the current class–E PA topologies on a frequency or phase–modulated input signal. This would also include distortion analysis, usually neglected in class–E PAs.

Further extensions in phase noise measurements is another topic that can be suggested. The developed PA phase noise measurement system can be embedded within a harmonic load–pull system. Using simultaneous measurements of the phase noise, P_{OUT} and efficiency the contours of constant

parameters can be used to perform required trade-offs among them.

Finally, a microwave class–E related research area with a great potential is the application of large signal network analysis (LSNA) [35, 36, 37] in the characterization and modeling of microwave active devices operating in the switched mode. The LSNA can be used to obtain the actual voltage and current waveshapes at the active device ports, under controllable fundamental and harmonic terminations. An insight to actual microwave device I/V curves at the operating frequency is a privilege to any designer, allowing to manipulate them directly, by controlling harmonic content in both input and output signals. Moreover, the simultaneous acquisition of power/bias dependent wave variables several harmonic frequencies gives a unique versatility that is currently missing in standard S–parameter based large signal model extraction methods. This means that accurate active device models for microwave transistors operating in highly nonlinear switched–mode may soon become available, assuring a very comfortable design environment.

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Appendix A

Small–Signal Parameter

Extraction
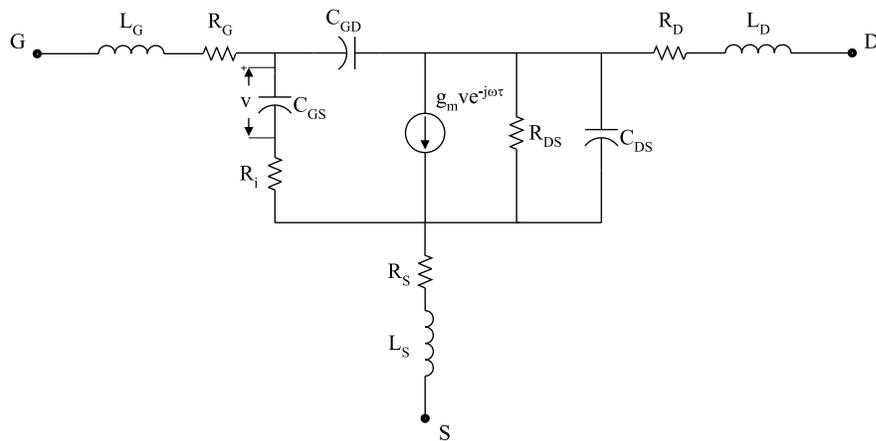
Figure A.1: Small–signal equivalent schematic of a MOSFET, MESFET and HEMT.

The small signal model of a microwave MESFET is shown in Fig. A.1.

The model parameter extraction is based on a method described in [30] with application of a gradient optimization procedure instead of simple error function evaluation and re–iteration. Modifications of the method can be used to extract small signal parameters of other types of microwave active components that can be used as switch–acting devices in a class–E PA (BJTs, HBTs).

The first step is the determination of approximate series contact resistances of electrodes R_G, R_S and R_D. Performing a set of three DC measurements of a forward biased gate current with: a) source grounded, b) drain grounded and c) both source and drain grounded, yields three input resistances R_a, R_b and R_c. The electrode resistances can be directly calculated as:

$$
\begin{aligned}
R_G &= R_c - \sqrt{R_c^2 - R_c(R_a + R_b) + R_a R_b} \\
R_D &= R_b - R_G \\
R_S &= R_a - R_G
\end{aligned}
\tag{A.1}
$$

These values are slightly dependent on the forward bias conditions, and will differ from the values at frequency of operation, due to the skin effect. However, these values are good initial estimates for the later optimization.

The next step is the determination of the intrinsic device elements. This is done throughout the following iterative procedure, based on a set of measured 2–port S–parameters, given at N discrete frequency points. Initially, para-

sitic inductances are assumed to be zero. Converting measured S–parameters S_{ij_m} into Z–parameters Z_{ij_m}, previously determined resistances are easily deembeded, resulting in Z–parameters of the intrinsic active device - z_{ij_m}:

$$
\begin{aligned}
z_{11m} &= Z_{11m} - (R_G + R_S), \\
z_{12m} &= Z_{12m} - R_S, \\
z_{21m} &= Z_{21m} - R_S, \\
z_{22m} &= Z_{11m} - (R_D + R_S) \\
D &= 1 + \omega^2 C_{GS}^2 R_i^2.
\end{aligned}
$$

$$(A.2)$$
$$(A.3)$$

In order to extract component values of the intrinsic device, it is convenient to transform its Z–parameters to Y–parameters. Then, by solving the intrinsic circuit for its Y–parameters and equating them to the previously determined ones, a set of equations is obtained:

$$
\begin{aligned}
y_{11} &= R_i (C_{GS}\omega)^2 / D + j\omega(C_{gs}/D + C_{GD}), \\
y_{12} &= -j\omega C_{GD}, \\
y_{21} &= g_m e^{-j\omega\tau} / (1 + j\omega R_i C_{GS}) - j\omega C_{GD}, \\
y_{22} &= g_{DS} + j\omega(C_{DS} + C_{GD}).
\end{aligned}
$$

$$(A.4)$$

From the measured set of intrinsic Y–parameters over frequency, the capacitances of the active device can be extracted. First, C_{GD} and C_{DS} can be found from:

$$C_{GD} = -m_{y12},$$

$$C_{DS} = m_{y22} - C_{GD}, \qquad (A.5)$$

where m_{y12} and m_{y22} are the slopes of the regression lines to the corresponding imaginary parts of the measured intrinsic Y–parameters (Eq. A.5). Finally, using a low frequency approximation ($\omega C_{GS} R_i << 1$), the first of Eq. A.5 gives

$$C_{GS} = m_{y11} - C_{GD}. \qquad (A.6)$$

The output capacitance of the active device can be calculated as:

$$C_{OUT} = C_{DS} + \frac{C_{GD}C_{GS}}{C_{GD} + C_{GS}} \qquad (A.7)$$

The rest of the intrinsic active device model (g_m, g_{DS}, τ and R_i can be determined following the procedure given in [30]. After that, from the difference between measured and modeled Z–parameters of the intrinsic device with included previously determined electrode resistances, the metalization and bond inductances can be estimated. Finally, modeled S– parameters of the entire circuit can be determined, and compared to the measured ones. An error term for each S–parameter can be established as:

$$E_{i,j} = \frac{1}{N} \sum_{k=1}^{N} \frac{\left| S_{ij-meas}^{k} - S_{ij-model}^{k} \right|}{\left| S_{ij-meas}^{k} \right|}. \qquad (A.8)$$

Now, the entire process can be repeated, starting from the measured S–parameters and deembeding the resistances and parasitic inductances found in the previous iteration. Stepping through the described algorithm, a more accurate set of intrinsic model components can be determined. The iterations end when the error terms drop below specified tolerances.

The proposed modification eliminates the iterations of the described procedure. Instead, after the initial extraction step, the obtained model parameters are varied through a gradient optimization routine available in most circuit simulators, until satisfactory agreement between measured and modeled S–parameters is achieved.

Appendix B

Load–Pull Background

B.1   Load–Pull System Deembedding

The deembedding of a load–pull system [93] is measurement of S–parameters
of each of the system blocks, using a VNA and their deembeding during the
DUT characterization.

Through this process all impedances and powers are referenced to the
DUT reference plane. A "Short–Open–Load–Thru" (SOLT) calibrated VNA
determines the following sets of S–parameters (Fig. B.1):

- Driver stage (signal generator and pre–amplifier) output reflection co-
  efficient, Γ_{DRV} (input of the driver PA is terminated by 50Ω);

- Output power–probe input reflection coefficient, Γ_{PRB};

- Input block 2–port parameters with coupled and isolated port on the
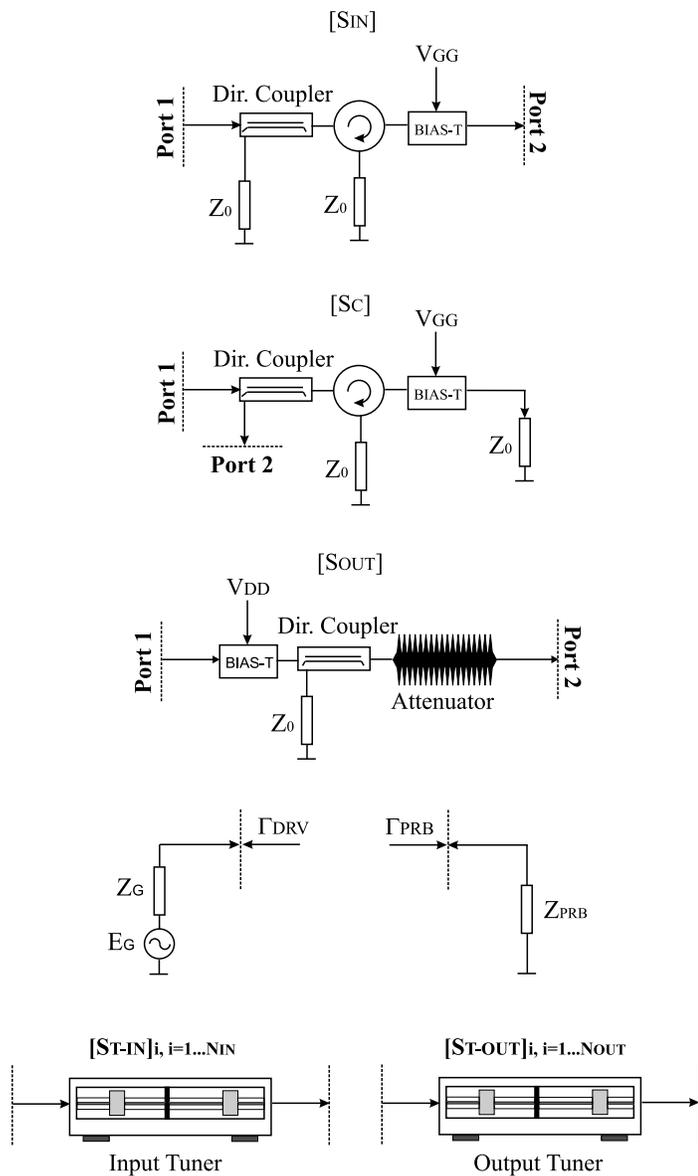
Figure B.1: Deembedding of the input and the output blocks, the driver stage and the output power probe. The input and output tuner S–parameters are measured for each of the tuner's position.

directional coupler and circulator terminated with the matched load, S_{IN};

- Input block 2–port parameters between the input and the coupled port with the output and the isolated port terminated with the matched load, S_C;

- Output block 2–port parameters, S_{OUT};

- Input and the output tuner S–parameters for the range of impedances of interest: $S_{T-IN}(i)$, and $S_{T-OUT}(j)$ where $i = 1...N_{IN}$ and $j = 1...N_{OUT}$. N_{IN} and N_{OUT} are the number of calibration points for the input and the output tuner.

Finally, the S–parameters of the input and output fixture halves (S_{F-IN} and S_{F-OUT}) have to be determined. In the case of a non–coaxial DUT this is a well known problem of determining the S–parameters of a 2–port element (test fixture half) with different port types (e.g. coaxial on one side and microstrip on the other). A SOLT calibrated VNA can be used to measure a set of S–parameters of the following transmission–line standards inserted between test fixture halves [94, 95, 96]: "Thru", "Reflect" (usually a line short, equal for both ports) and one or more "Line" standards, as shown in Fig. B.2.

The characteristic impedance of all lines is equal to Z_0, determined by substrate dielectric constant and line width. Using the set of measured S–parameters, the actual S–parameters of the test fixture can be estimated.
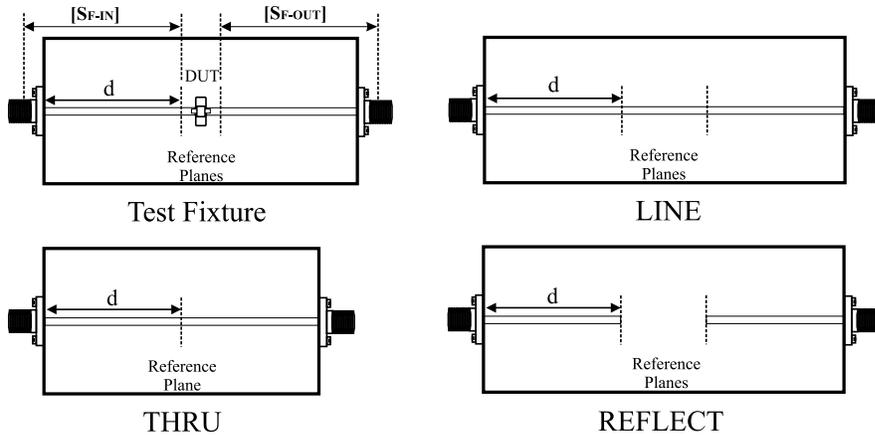
Figure B.2: Test fixture (microstrip) with the reference plane set so that mounting parasitics are included into the DUT. "Zero–length" "Thru" standard, followed by a single (or multiple) "Line" standard, and finally "Reflect" standard, usually "open" circuit for microstrip or "short" circuit for CPW.

For that task an analytic procedure given in [97] can be used, or commercial calibration software, such as *MultiCAL*® [95, 96] in a "two–tier mode", can be applied.

The standards are fabricated on the same substrate as the test fixture, using the transmission lines with the known characteristic impedance. For low-loss lines in order to properly denormalize obtained S–parameters only the capacitance per unit length has to be accuratelly known. The main assumptions in this method are that all transmission lines (calibration standards and test fixture lines) have the same characteristic impedance and the same exact connections. If coaxial system is used in the rest of the system all of the applied connectors have to be identical, consistently mounted on the test fixture and the standards. The reference plane is set by the center

of the "Thru" standard. In order to ascribe the mounting/bonding para-sitics to the DUT the reference plane needs to be set "far enough" from the point where the DUT is physically connected to the test fixture (Fig. B.2). This is approximately a substrate thickness apart from the DUT connection, depending on the transmission line geometry.

B.2 Load–Pull Measurement

After the performed calibration, the measured S–parameters of the individual system blocks are known. Entire input and output part of the system can now be modeled by a pair of 2–port S–parameters matrices for each of the tuner position, as shown in Fig. B.3.
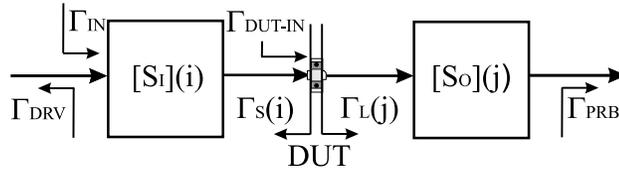
Figure B.3: Model of the load–pull system shown in Fig. 4.1. For each of the tuner positions, the input and the output block are replaced by the equivalent 2–port S–parameter matrices. Indexes i and j correspond to the individual tuner positions.

The reflection coefficient at the DUT reference plane can be easily calcu-lated for each of the tuner position as:

$$\Gamma_S(i) = S_{I22}(i) + \frac{S_{I21}(i) \cdot S_{I12}(i) \cdot \Gamma_{DRV}}{1 - S_{I11)}(i) \cdot \Gamma_{DRV}}. \tag{B.1}$$

$$\Gamma_L(j) = S_{O11}(j) + \frac{S_{O21}(j) \cdot S_{O12}(j) \cdot \Gamma_{PRB}}{1 - S_{O22}(j) \cdot \Gamma_{PRB}}. \tag{B.2}$$

where $i = 1...N_{IN}$ and $j = 1...N_{OUT}$. N_{IN} and N_{OUT} are the input and output tuner positions respectively. Γ_{DRV} and Γ_{PRB} are reflection coefficients of the driver and the output power probe respectively.

Using the determined S–parameters of the input block and measured power at the input directional coupler coupled port (P_{DIR}) it is possible to calculate the power available at the DUT input reference plane (P_{IN-AV}). First, the power incident at the input port of the directional coupler is:

$$P_{G-INC} = \frac{P_{DIR}}{C_{DIR}}. \tag{B.3}$$

C_{DIR} is the input coupler power coupling coefficient defined as:

$$C_{DIR} = \left|S_{C(21)}\right|^2 \tag{B.4}$$

where $S_{C(21)}$ is the forward transmission coefficient of the input block (Fig. B.1). The power that enters the input block is:

$$P_{IN} = P_{G-INC}(1 - |\Gamma_{IN}|^2) \tag{B.5}$$

where Γ_{IN} is the input reflection coefficient of the entire load–pull system.

In principal, Γ_{IN} can be calculated as:

$$\Gamma_{IN} = S_{I11} + \frac{S_{I21} \cdot S_{I12} \cdot \Gamma_{DUT-IN}}{1 - S_{I22} \cdot \Gamma_{DUT-IN}} \tag{B.6}$$

for each of the input tuner positions.

Unfortunately, Γ_{DUT-IN} of a nonlinear DUT is not known in most cases, as explained earlier. Although it could be measured using a modified VNA [98], the Γ_{DUT-IN} is dependent on the input power level as well as the DUT bias point. It is clear from Eq. B.6 that without knowing Γ_{DUT-IN} it is not possible to determine the power entering the input block of the system (Eq. B.6, Eq. B.5). This problem can be overcome by using a circulator/isolator in the input block. If the isolator offers high isolation in the reverse direction, the resulting reverse transmission parameter (S_{I12}) of the input block can be neglected. From the Eq. B.6 follows:

$$\Gamma_{IN} \approx S_{I11}. \tag{B.7}$$

With this approximation, the input power P_{IN} can now be calculated from the measured P_{DIR} using Eq. B.5. Next, the power available from the driver PA (P_{DRV-AV}) can be found as [13]:

$$P_{DRV-AV} = P_{IN} \frac{|1 - \Gamma_{DRV}\Gamma_{IN}|}{(1 - |\Gamma_{DRV}|^2)(1 - |\Gamma_{IN}|^2)}. \tag{B.8}$$

This assumes that the available power consists of fundamental frequency component only.

Finally, the power available at the DUT input reference plane is:

$$P_{IN-AV}(i) = P_{DRV-AV} \frac{1 - |\Gamma_{DRV}|^2}{|1 - S_{I11}(i)\Gamma_{DRV}|^2} \frac{|S_{I21}(i)|^2}{(1 - |\Gamma_S(i)|^2)}. \tag{B.9}$$

The available DUT power is used instead of DUT input power because it is independent of the DUT input reflection coefficient. However, the P_{IN-AV} depends on the input tuner position (Eq. B.9). In practice, the source–pull characterization of the power active device is performed with a constant P_{IN-AV}. Therefore, in order to maintain this power constant it is necessary to correct the driver PA output power for each of the input tuner positions, applying the Eq. B.9. This is an easy task since the input block is fully characterized with its S–parameters and the P_{AV-DRV} do not depend on the Γ_{IN}.

The power that the DUT delivers to the output block (P_{OUT-N}) can be calculated from the measured output power (P_{OUT}) and measured S–parameters of the output block as:

$$P_{OUT-N}(j) = P_{OUT}(j) \frac{1 - |\Gamma_L(j)|^2}{|S_{O21(j)}|^2} \frac{|1 - S_{O22}(j)\Gamma_{PRB}|^2}{(1 - |\Gamma_{PRB}|^2)} \tag{B.10}$$

Finally, from the known input available power and power delivered to the output block, the transducer gain of the DUT can be found for any position of the input and output tuner as:

$$G_T(i,j) = \frac{P_{OUT-N}(j)}{P_{IN-AV}(i)} \qquad \text{(B.11)}$$

From the obtained output power, gain and measured DC power consumption, the efficiencies can be calculated for each of the impedances presented to the DUT using Eq. 1.4-Eq. 1.5. Harmonic power or intermodulation products can be measured using an additional coupler at the output, and compared to the power at the fundamental frequency. This measurement shows the DUT distortion dependence on the input and output impedances. Contours of constant DUT parameters are a common way for representing load dependence of the parameters in a Smith chart and performing the DUT performance trade–off.