MEMS-Reconfigurable Microwave Power Amplifiers

by

Patrick J. Bell

B.S., University of Virginia, 2001

M.S., University of Colorado at Boulder, 2003

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Zoya Popovic

Christopher Dyck

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MEMS-Reconfigurable Microwave Power Amplifiers

Thesis directed by Prof. Zoya Popovic

In recent years, there has been a great deal of interest in MEMS reconfigurable circuits for applications in miniaturized multifunctional microwave systems. RF-MEMS switches have demonstrated low loss, linear operation and low static power consumption, making them suitable components in a high-performance, reconfigurable circuit.

A principle component in a reconfigurable power amplifier is an impedance tuner. Although a number of universities have published tuners with impedance constellations covering large percentages of the Smith Chart, adoption of these tuners into front-end circuits has been slow. Current demonstrations of reconfigurable power amplifiers are limited to very simple circuits to enable frequency hopping.

This thesis analyzes this trend and determines the criteria for integrating a tuner with a power amplifier, design of impedance tuners to meet amplifier specifications, and a performance analysis of a 10 GHz power amplifier that reconfigures from a high-linearity class-A mode to a high-efficiency class-E mode. This reconfigurable amplifier is compared to conventional non-reconfigurable class-A and class-E amplifiers. It is shown that a simple reconfigurable power amplifier can be designed with less than 5% degradation in power-added efficiency.

This thesis also presents the design of a low-loss 80-state impedance tuner and a generalized analysis of impedance tuners, including constellation density, bandwidth, redundant coverage, insertion loss, and failure degradation, using a MEMS-switched double-slug tuner as an example. A high-performance micromachined inductor, compatible with flip-chip integration in hybrid circuits, is also designed and characterized for use in miniaturized biasing circuits.

Dedication

To my parents and grandparents, for being with me each step of the way.

Acknowledgements

I would like to thank Prof. Zoya Popovic and her research group for their guidance and assistance in this work. In particular, I'd like to thank Nestor Lopez, my office-mate and amplifier brother, who was both instrumental in exploring the world of power amplifiers with me and a terrific friend - thanks for good times and the laughs; Nils Hoivik for introducing me to the world of MEMS and for his encouragement throughout the years; and Ken Vanhille for his friendship and perspective. I would also like to thank Alan Brannon, Jacques Loui, Srdjan Pajic, Negar Ehsan, and Rachael Tearle.

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Introduction

In recent years, there has been a great deal of interest in MEMS reconfigurable circuits for applications in miniaturized multifunctional microwave systems. Multifunctional systems reconfigure a single signal path to perform multiple functions, such as communication with multiple networks with different operating frequencies and modulation schemes [1]. RF-MEMS switches have demonstrated low loss, linear operation and low static power consumption, making them suitable components in a high-performance, reconfigurable circuit.

Early MEMS reconfigurable circuits primarily focused on phase shifters and filters. RF MEMS phase shifters are a low-loss, high-linearity alternative to p-i-n diode, FET transistor, or ferrite material based phase shifters, which introduce high losses and nonlinearity in the front end [2]. Demonstrated MEMS-based phase shifters have been based largely on established designs with a replacement of the solid-state component with a MEMS component in switched [3–10] or distributed networks [11–16]. Reconfigurable and tunable MEMS-based filters have higher quality factor than varactor diode-based filters [17–27].

In addition to phase shifters and tunable filters, a reconfigurable power amplifier is a critical component in a multifunctional signal path. A conventional microwave power amplifier (PA) is optimized to operate with a particular frequency, gain, power level, and bandwidth. A reconfigurable power amplifier (RPA) would be required to operate

in multiple or changing operating conditions, such as diverse frequency or signal modulation schemes, and environmental conditions. RPAs could also enable a single terminal to function for both communication and radar applications, which is not feasible with conventional amplifiers since these applications have very different requirements on the amplifier.

Implementing an RPA requires reconfigurable impedance matching networks and bias supplies, with a controller algorithm to optimize the amplifier based either on external configuration commands or by sensing changes in performance. Both the impedance matching networks and the sensors must have low insertion loss to ensure efficient amplifier operation, which is essential in any mobile application. A block diagram of an RPA is shown in Figure 1.1, which includes tunable impedance matching networks at the input and output of the transistor, a reconfigurable bias supply, a controller, and high impedance RF chokes. This work focuses primarily on the combination of a transistor and a reconfigurable output-matching network and the design of the output network, indicated in Figure 1.1. Design and measurement of miniature inductors for RF chokes is also included.

Although a number of impedance tuners with impedance constellations covering large percentages of the Smith Chart (discussed in detail in Section 1.1) have been published since 2001, demonstration of these tuners in front-end circuits has been slow to occur, nor have any performance trade-offs been established to weigh the benefits of the increased complexity of an RPA. Current demonstrations of RPAs are limited to very simple circuits to enable frequency hopping.

This thesis determines the criteria for integrating a tuner with a power amplifier, design of low-loss impedance tuners to meet amplifier specifications, and a performance analysis of a power amplifier that reconfigures from a high-linearity Class-A mode to a high-efficiency Class-E mode. This thesis also presents a generalized method of analysis of impedance tuners, including constellation density, bandwidth, redundant coverage,

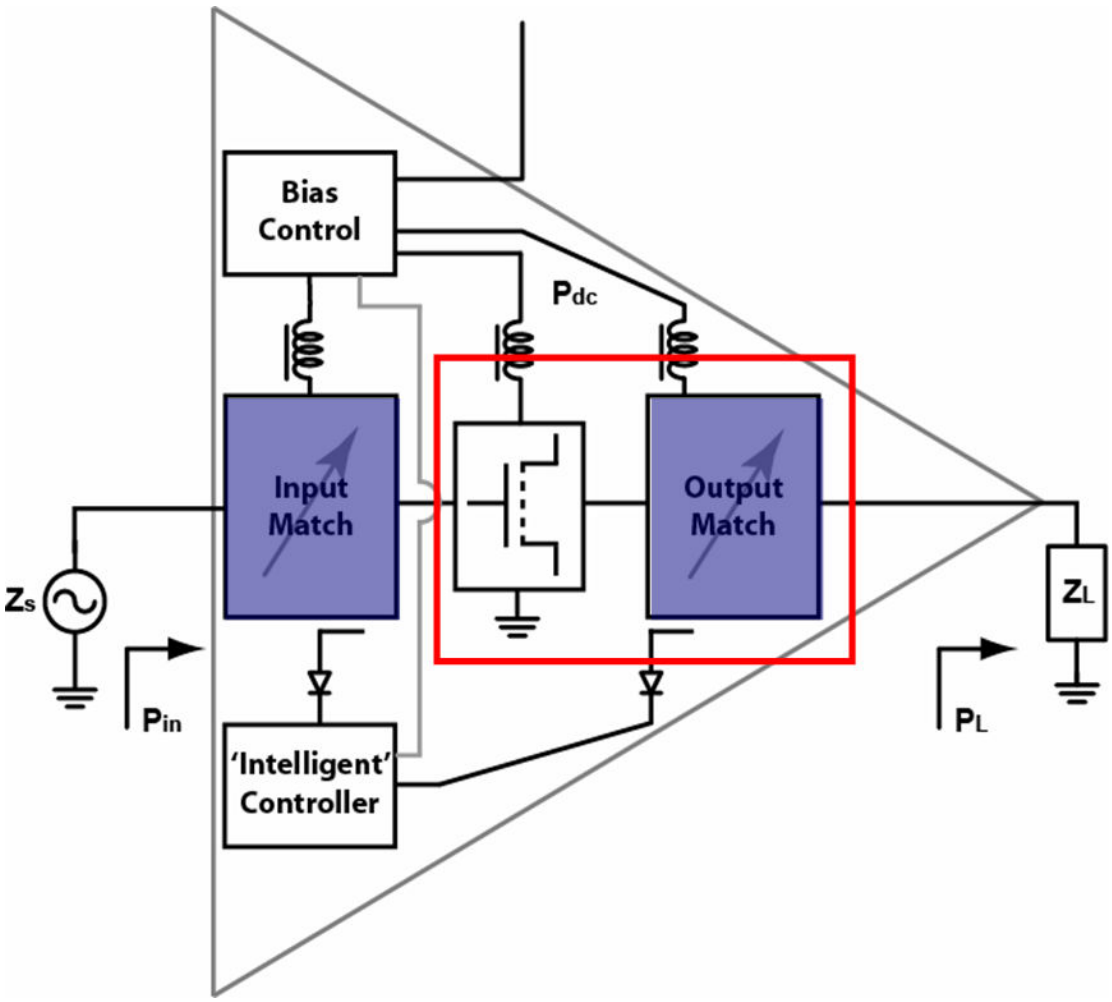


Figure 1.1: A block diagram of a reconfigurable power amplifier (RPA), with tunable matching networks at the input and output of the transistor, a reconfigurable bias supply, sensors and a controller processor, and high impedance RF chokes. This work focuses on the combination of a transistor and a reconfigurable output-matching network, indicated by the red box. Design and measurement of miniature inductors for RF chokes is also included.

insertion loss, and failure degradation, using a MEMS-switched double-slug tuner as an example.

1.1 Literature Review

1.1.1 Solid-State Tuners

Early impedance tuners relied on solid-state technology to reconfigure the circuit. One of the earliest tuners used high electron mobility transistors (HEMTs) to switch shunt capacitors along a transmission line [28]. This tuner was designed for integration with an amplifier to compensate for process deviations affecting the small signal parameters of the amplifier. Small gate widths were used in the HEMTs to allow close spacing of the shunt capacitors. Simulations showed small gain variations (0.3 dB) in the amplifier at 25 GHz. Insertion loss and intermodulation distortion (IMD) are not discussed.

Another solid-state tuner, published in 1996, used HEMTs as switches in a series-shunt configuration [29]. These transistors had large gate areas to minimize the on-state resistance, which came at the cost of decreased off-state isolation. To solve this, inductors were placed in parallel with the transistors that were resonant with the off-state capacitance. The eight series-shunt switches allowed four lengths of line to be switched independently to become either an open or a shorted stub. This tuner produced 50 discrete points at 18 GHz with a maximum reflection coefficient ($|\Gamma|_{max}$) of 0.85. This work was later expanded in [30] to test series, shunt, and series-shunt configurations of the HEMT switches. The shunt and series-shunt configurations both covered $|\Gamma|_{max} = 0.85$ with a minimum insertion loss of 10 dB and 6 dB respectively.

In 1997, another solid-state approach used varactor diodes to create a variable capacitor-inductor-capacitor Pi-network [31]. This tuner was intended for general tuning applications, both characterization and integration in a circuit. The impedance inverters

used to create the variable inductance limited the bandwidth to 10% at 2.25 GHz. The authors intended this tuner for 15–25-dBm applications, and gave no discussion of IMD.

In 2004, the first tuner integrated into a system was designed to compensate a changing antenna load in the 380–400 MHz range for 40 dBm power levels [32]. Initially, the authors used low-pass Pi-matching networks using varactor diodes and impedance inverters, but this design was later changed to p-i-n diodes with fixed capacitors to increase the power handling capability. The capacitor values were selected in binary increments to achieve 2^N capacitance combinations for N capacitors. The p-i-n diodes introduced additional intermodulation products into the system, which were measured to be -42 dBc (IMD3) for 35 dBm input power.

1.1.2 MEMS-Based Tuners

The promise of compact size, reduced loss, and high linearity led to the integration of MEMS switches and variable capacitors into impedance tuners beginning in 2001. Using variable capacitors in resonant unit cells, a large impedance change for a small change in capacitance (30%) was shown in [33]. The constellations in [33] showed 49 points with maximum standing wave ratios (SWRs) of 14, 21, and 32 for the three types of tuners reported at 29, 25, and 30 GHz respectively. The authors claimed this type of tuner was suitable for power amplifier applications, but loss was not discussed.

The earliest switch-based impedance tuner was also reported in 2001, which was a hybrid assembly using switched capacitor banks (fabricated on silicon) to terminate mircostrip stubs on an alumina substrate [34]. This work was later expanded in 2003 to include 10 GHz and 20 GHz tuners [35].

Switch-based tuners fabricated on a single glass substrate were reported in 2004 [36, 37]. Both used the same MEMS switch process. The first was a capacitor-loaded coplanar waveguide (CPW) line, which produced constellations from 20–50 GHz with eight switches for a total of 256 states [36]. The constellations were approximately cir-

cular, but the coverage areas changed with frequency. Loss was not quantified. The second circuit was a capacitor-loaded triple-stub circuit in CPW, which produced constellations from 6–20 GHz with 11 switches for a total of 2048 states [37]. Again, the constellation shape and area changed dramatically across frequency, and loss was not discussed.

A scaled version of [36] was reported in 2004, producing constellations from 4–18 GHz with eight switches and 256 states [38]. [38] gave extensive treatment to the linearity of the tuner, although the loss reported was not insertion loss (see Section 4.1). The coverage area across the 4–18-GHz frequency range was inconsistent.

Another variable-capacitor based tuner on silicon was reported in 2005 [39], which used variable capacitors and impedance inverters to create a capacitor-inductor-capacitor Pi-network as in [31]. Since the variable capacitors are contact-less devices, they handled higher power, up to 3.5 W. This tuner covered a large region of the Smith Chart at 30 GHz. The loss reported in [39] was not insertion loss.

Due for publication in 2006 is a MEMS implementation of the classical "double slug" impedance tuner [40]. This tuner produces circular constellations from 10–30 GHz. One major advantage of this tuner design is its regular coverage area across most of its frequency band. Insertion loss is reported correctly.

Other tuners have been reported in the 20–50 GHz [41] and W-band range [42] for load-pull and noise characterization.

1.1.3 Integrated Tuners and Amplifiers

While several stand-alone MEMS tuners have been reported and claim suitability for power amplifier applications, very few have been integrated with amplifiers.

[43] used variable capacitors in tunable input and output matching networks to optimize a class-AB amplifier for 6 and 8 GHz operation. The tuner was a capacitor loaded double-stub CPW configuration, though details of the tuner impedance and loss

are not reported. The amplifier achieved 26% PAE at 6 GHz and 17% PAE at 8 GHz. [43] showed good agreement between measurement and simulation, but it is unclear whether this design achieves class-AB with such low efficiencies.

[44] used a single switch in the input and output matching networks to create a two-state amplifier that switches from 900 MHz to 1.9 GHz. The amplifier delivered 31 dBm in both states and has a saturated PAE of 62% at 900 MHz and 46% at 1.9 GHz. This technique was extended in [45] to include 900 MHz, 1.5 GHz and 2.0 GHz. The tuner in [45] used two switches in the input and output matching circuits for the three states. At the three frequencies, the amplifier achieved 60%, 61%, and 62% PAE respectively for a saturated output power of 30 dBm.

A fully adaptable system, complete with feedback controllers for the reconfigurable input and output matching networks was demonstrated in [46] from 8–12 GHz. The amplifier maintained 25–27 dBm of output power across X-band and converged to an optimal solution in approximately 20 iterations for a completely unknown input frequency. Efficiency was not reported.

1.2 Motivation for This Work

This thesis examines the gap between the tuners demonstrated in [33, 35–40], which have large constellations and hundreds of states, and the integrated amplifiers demonstrated in [44–46], which have much simpler tuner implementations and only a few states. Section 1.2.1 uses a 10 GHz high-efficiency amplifier as an example to demonstrate the effect adding a tuner network from [37, 38, 40, 47] has on efficiency. (Note that [47] is a 10 GHz design based on [39].) These networks are chosen as case studies because they claim suitability for power amplifier applications and produce constellations at 10 GHz.

1.2.1 Effect of Insertion Loss on Efficiency

A matching network with MEMS switches will have a slightly higher insertion loss than a network without MEMS due to the incremental loss of the switch contacts. If the output power and efficiency of a conventional amplifier are known, the additional loss of the MEMS network (ΔIL) can be used to determine the effect on output power and efficiency if this reconfigurable network is included in the system.

The output power of a conventional amplifier, $P_{out,conv}$, is scaled by the additional insertion loss ΔIL of the MEMS network. Power-added efficiency is determined by:

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}}, \tag{1.1}$$

where P_{in} is the input power, and P_{dc} is the dc power [48]. This equation can be modified to determined the PAE of an RPA (PAE_{recon}), assuming $P_{out,conv}$, P_{dc}, and ΔIL are known:

$$PAE_{recon} = \frac{(P_{out,conv} \cdot \Delta IL) - P_{in}}{P_{dc}}. \tag{1.2}$$

Figure 1.2 shows the effect of an increasing ΔIL on the efficiency of the reconfigurable amplifier, PAE_{recon}, for different initial efficiencies. The red line is a 55% PAE class-E amplifier used as an example in this study, which has 8 dB gain [49]. The blue dashed lines are estimations of the efficiency effect as the initial efficiency changes. These curves are estimated by increasing or decreasing P_{dc} and assuming the 8 dB gain of the amplifier remains constant. In practice, gain will change for the various amplifier classes [50–53], however this assumption will suffice for this discussion.

As the loss at the output of the amplifier increases, the output power and efficiency decrease. At 8 dB of insertion loss, the efficiency drops to 0 for all cases. PAE can be re-expressed to show its dependence on gain as

$$PAE = \frac{P_{out}}{P_{dc}} \left(1 - \frac{1}{G}\right) \tag{1.3}$$

[48]. It follows that an amplifier with 8 dB gain amplifier (with a lossless output)

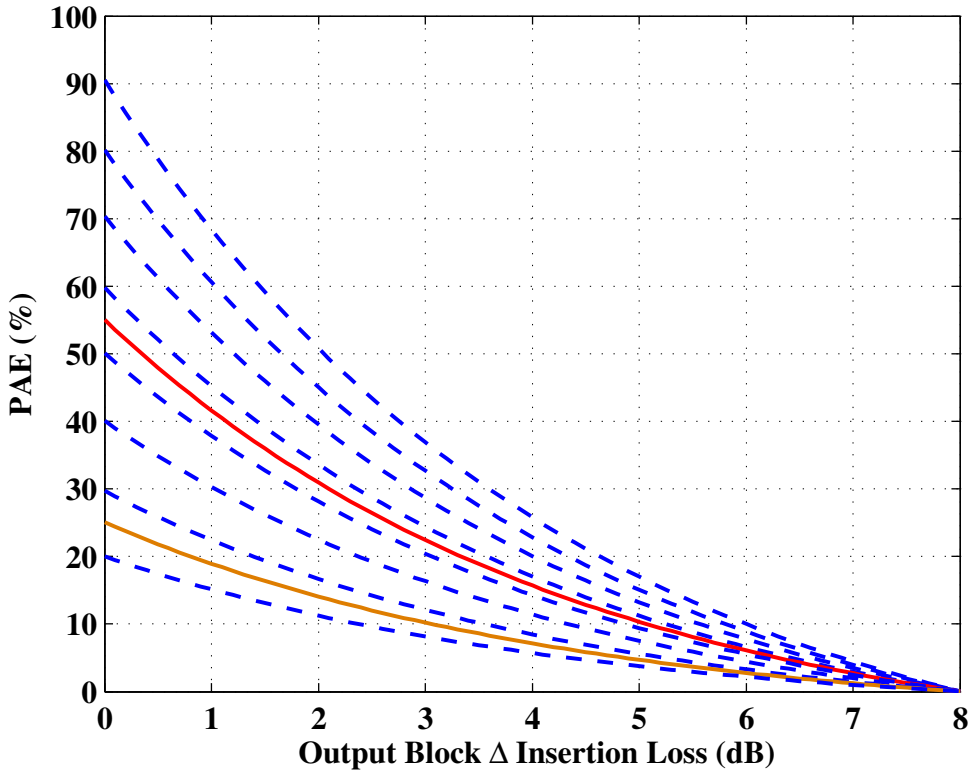


Figure 1.2: The effect of increasing the insertion loss in the output network of an amplifier is a decrease in output power and power-added efficiency. Higher-efficiency amplifier modes are more sensitive to increased loss than low-efficiency modes. A typical 10-GHz class-E PA has 55% PAE [49], and the solid red line indicates how the PAE of this PA would decrease as loss in the output network increases.

combined with an output network with 8 dB of loss would have unity gain and no power-added efficiency.

Mentioned earlier in the introduction, loss is often not reported correctly as insertion loss (negative power gain). However, [37,38,47] provide measured s-parameters for cases where all the MEMS devices are in an open state or a closed state, which can be used to determine the approximate minimum and maximum loss of the tuner. Insertion loss (in dB) is determined from the published s-parameters by $IL = 10\log(|S_{21}|^2/(1 - |S_{11}|^2))$ for a matched load. [40] reports loss correctly, and so those loss measurements are used directly. Figure 1.3 marks the locations of the minimum and maximum insertion loss for the published tuners used in this case study. These results are summarized in Table 1.1.

Table 1.1: Published Tuners and Insertion Loss at 10 GHz

Label in Figure 1.3	Reference	Insertion Loss (dB)	55% PAE Degradation
A	[37]	?-9*	?
B	[38]	0.5–4	48%–18%
C	[47]	1.8–3.5	33%–20%
D	[40]	1.5–4	35%–18%

Case A only reports the s-parameters for all switches in the closed position, so the minimum insertion loss is unknown. The maximum loss is also greater than the gain of this amplifier, so a combination of the amplifier with this tuner would have no power-added efficiency. Case B shows that the addition of the tuner would drop the efficiency of the amplifier from 55% to 48% immediately. As the tuner configures to its various states, assuming the transistor can always be matched to its ideal operating impedance, the loss of tuner degrades the PAE to as low as 18%, depending on state. Case C would have an efficiency range from 33% to 20%, and Case D from 35% to 18%.

Such a large degradation in output power and efficiency is undesirable. Microwave power amplifiers are the most costly elements in any wireless or radar system, so their performance is critical, from both a system and monetary perspective. This thesis aims

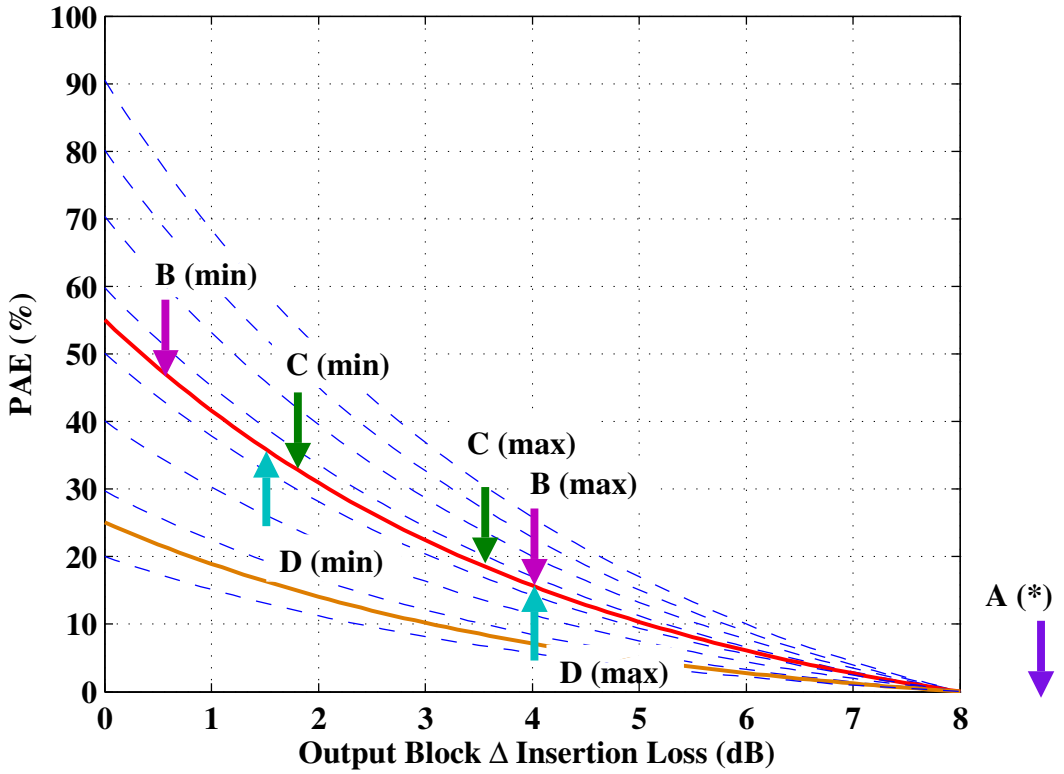


Figure 1.3: Locations of the minimum and maximum insertion loss for the 10 GHz tuners reported in [37, 38, 40, 47], showing the degradation in efficiency for an amplifier that is initially 55% efficient. These results are summarized in Table 1.1.

to determine if it is possible to design a reconfigurable network with less than 0.5 dB of maximum insertion loss, such that the amplifier efficiency would degrade no more than 5%. Once a simple network is demonstrated in Chapter 2, a more complex network is designed in Chapter 3 with less than 0.7 dB of maximum insertion loss.

1.3 Sandia Ohmic MEMS Switch

The MEMS device used throughout the experiments in this thesis is the Sandia ohmic switch, designed and fabricated at Sandia National Laboratories, Albuquerque, NM. The circuits under test are designed and tested by the author.

The RF-MEMS switches in these networks consist of a metal plate with four contacts suspended above a transmission line layer. The plate is held at the same potential as the line through a resistor layer connection to a bond pad. In the blocking state, RF isolation is accomplished by the air gap between the switch plate and the transmission line and is typically 30 dB at 10 GHz. The switch is pulled down by applying a potential between the switch plate and an electrode underneath the plate. The switch contacts and plate bridge the transmission line gap forming a low resistance path that adds less than 1 Ω of series resistance when compared to an equivalent length of transmission line. The transition speed from the blocking state to the passing state ranges from 12-25 μs, including bounce, and depends on the type of drive signal used [54]. Cold-switching reliability testing of switches using Au-Au metal contacts has resulted in median lifetime values of greater than 50 million cycles.

Figure 1.4 shows a photograph of a Sandia switch.

1.3.1 Switch Equivalent Circuit

An equivalent circuit for the switch is provided by Sandia National Laboratories. The equivalent circuit is defined between the two reference planes indicated in Figure 1.4.

In the open state, the switch behaves as a small transmission line in series with

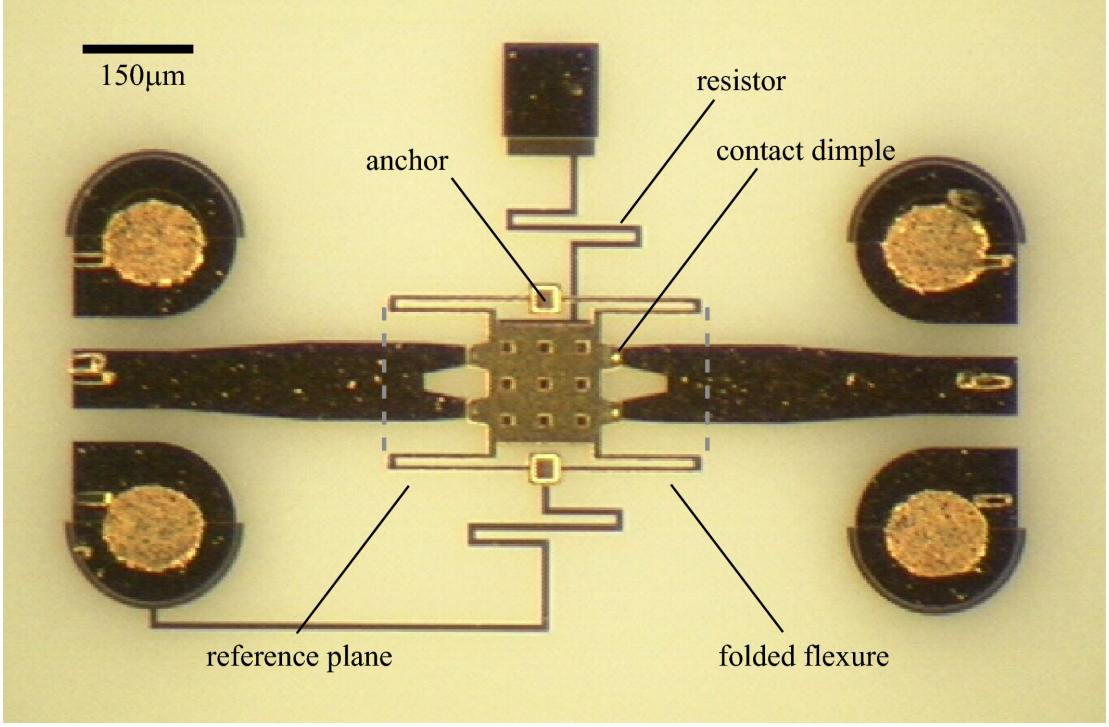


Figure 1.4: A photograph of the Sandia Ohmic MEMS Switch on an alumina (Al_2O_3) substrate. The switch plate is solid gold, 140 μm wide and 150 μm long. Contact is made with the transmission line through contact dimples, which are 10 μm wide, 5 μm long, and extend 1 μm below the plate. The plate thickness is 6 μm. In the center of the plate are 9 etch holes for the release of the plate; each are $16 \times 16\, mu$m. The plate is anchored to the substrate through 4 folded flexures, which are each 5 μm wide. Actuation occurs through a voltage applied through a 0.1-μm thick resistive layer to an electrode beneath the switch plate. The reference planes for the equivalent circuits shown in Figures 1.5 and 1.6 are indicated. The CPW-to-microstrip transitions have through wafer Cu-W filled vias, which present 40 pH for a 100 μm diameter via.

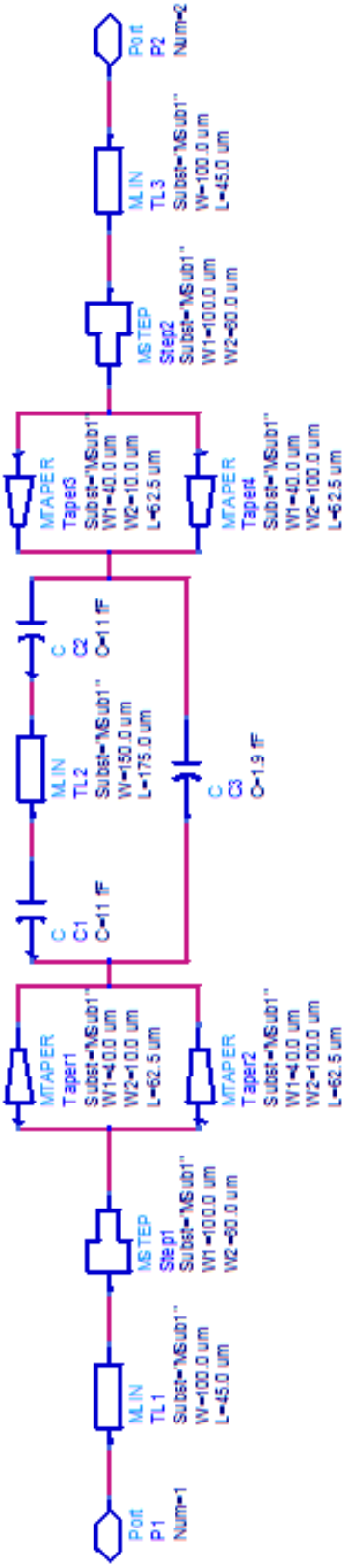


Figure 1.5: Equivalent circuit model of the Sandia ohmic MEMS switch in the open position. This model is accurate up to 20 GHz.

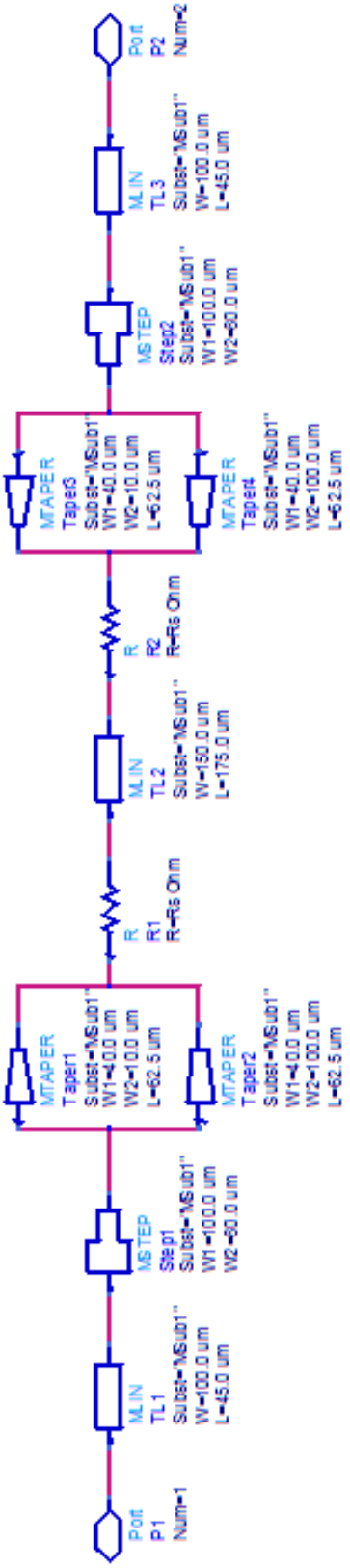


Figure 1.6: Equivalent circuit model of the Sandia ohmic MEMS swtich in the closed position. This model is accurate up to 20 GHz.

11-fF capacitors. The feed-through capacitance of the switch is approximately 1.9 fF, shown in Figure 1.5.

In the closed state, the 11-fF series capacitors are replaced with 0.6-Ω resistors, shown in Figure 1.6. The resistance varies from run to run, and so this value may be adjusted.

1.4 Organization of the Thesis

Having established the effect that current published impedance tuners would have on amplifier efficiency in Section 1.2.1, this thesis first examines a very simple reconfigurable amplifier with only two states. This amplifier is used to determine whether the efficiency degradation can be limited to 5%. To differentiate from other published reconfigurable amplifiers, the amplifier in this work demonstrates a different kind of reconfigurability - from a high linearity class-A mode to a high-efficiency class-E mode at 10 GHz. The each state of the RPA is compared to a standard class-A or class-E PA to determine the effect of the MEMS output circuit. Design and measurements of this amplifier are presented in Chapter 2.

Once it is established that a two-state reconfigurable power amplifier can meet the specified efficiency requirements, a more complex tuner is designed in Chapter 3. This "double slug" type tuner produces concentric circles of impedances on the Smith Chart, making it ideal for correcting a dynamic load due to a changing antenna impedance. The particular tuner chosen in this design produces a constellation of 80 impedance points on the Smith Chart within an 4:1 SWR circle. Chapter 3 takes the design from network theory through the optimization of the physical layout.

A means of quantitatively analyzing and comparing tuner designs for power amplifier applications is absent in the literature. Chapter 4 proposes a method of such analysis through determination of the coverage area to specified SWR requirements, insertion loss and effects on output power, redundancy due to overlapping coverage re-

gions and choice of state for maximum output power and efficiency, and the degradation of the tuner coverage area as devices begin to fail in the tuner.

Chapter 5 presents the design and measurement of a micromachined air-suspended inductor for use in high-frequency bias circuitry - a necessary component as amplifier complexity increases dramatically with the addition of impedance tuning circuitry.

Chapter 6 concludes with summary, discussion, and future work.

Chapter 2

MEMS-Reconfigurable Class-A-to-E Power Amplifier

In order to determine what constraints amplifier integration places on the design of the tuner, a simple two-state tuner is examined. Unlike the frequency-agile amplifiers demonstrated in [44–46], this work demonstrates a tuner which enables a different kind of multifunctionality: a power amplifier (PA) that can operate in either a linear class-A or high-efficiency class-E [55] mode, depending on the type of input signal that modulates the same carrier frequency. This type of reconfigurable PA (RPA) would allow a transmitter to switch between a frequency modulated signal (such as a chirp) or other constant-envelope modulation schemes, and an amplitude modulated signal with zero-crossings in the envelope (such as spread-spectrum) [56]. This chapter discusses:

(1) the target impedances and insertion loss of a PA tuner;

(2) the tuner design, including the optimal position of the MEMS switches in the microstrip circuit for low loss;

(3) measured comparison of the two states of the tuner to equivalent circuits without MEMS; and

(4) measured performance of the class-A and -E states of the PA at 10 GHz with comparison to conventional class-A and -E amplifiers made on the same substrate without MEMS.

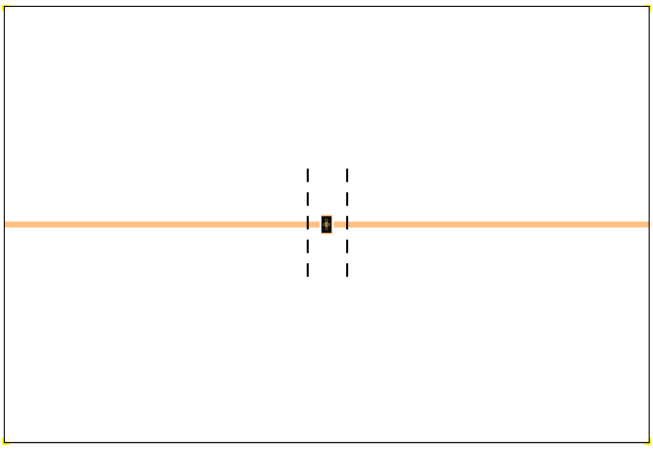
2.1 Design

A class-A-to-E switched-mode amplifier design involves simultaneous consideration of the class-A and -E source and load impedances, determination of the acceptable insertion loss in the MEMS-switched output network, and design of the switched network that satisfies the previous two criteria. This section presents details of the amplifier and MEMS network designs.

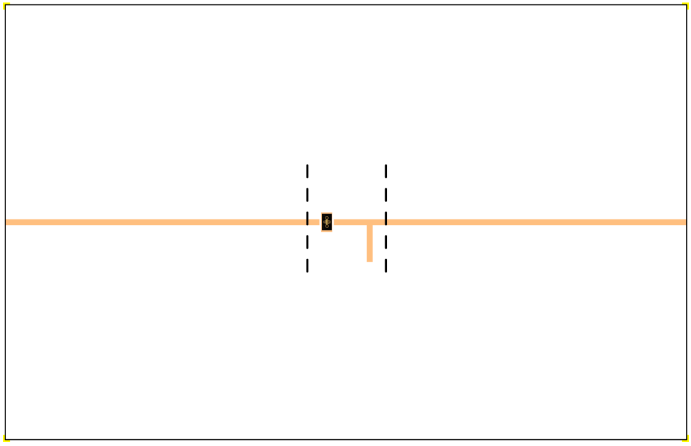
2.1.1 Amplifier Design

A Skyworks/Alpha GaAs MESFET is characterized by source and harmonic load-pull measurements at 10 GHz to determine impedance contours for output power (P_{out}) and power-added efficiency (PAE) in both modes. For this particular device, it is possible to choose identical input impedances for both modes. This common input network greatly simplifies the complexity of the circuit while allowing both modes to achieve 20 dBm of output power. Load-pull contours are measured using the fixtures shown in Figure 2.1. Note that the output reference plane on the class-E fixture (Figure 2.1(b)) is located past the second harmonic stub. The Z_E impedance is typically given at the transistor reference plane, so these measurements are transformed through the stub and transmission line network to determine the Z_E impedance. From the load-pull measurements of the MESFET, shown in Figure 2.2, the output network impedances are chosen to be $Z_E = 36.1+j36.9\,\Omega$ for class-E and $Z_A = 27.2+j15.1\,\Omega$ for class-A. The corresponding quiescent bias points are (V_{DS}=4.2 V, I_{DS}=20 mA)$_E$ and (V_{DS}=5 V, I_{DS}=70 mA)$_A$.

Under these operating conditions, the amplifier performance will configure into one of the states shown in the power sweep in Figure 2.3 and the two-tone intermodulation plots in Figure 2.4. These figures show measured data for two prototype amplifiers used in the design of the RPA. Both states are designed to give similar output power

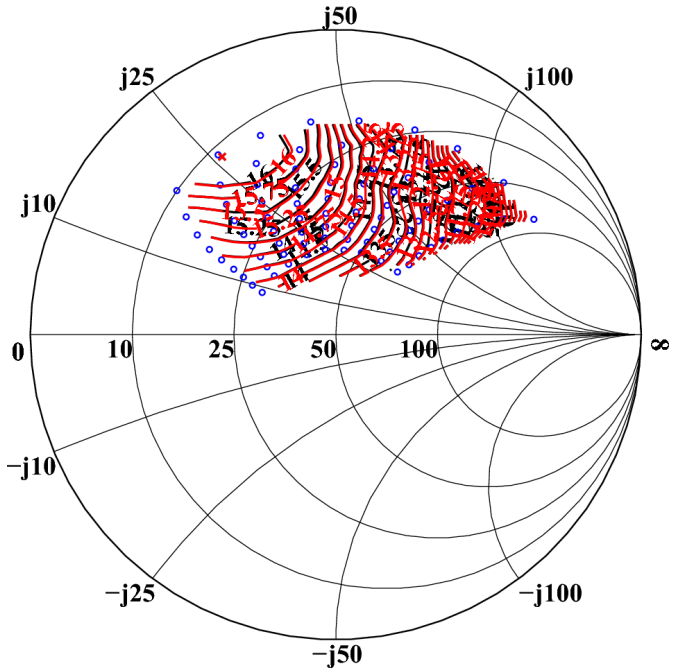


(a) Class-A Load-Pull Fixture

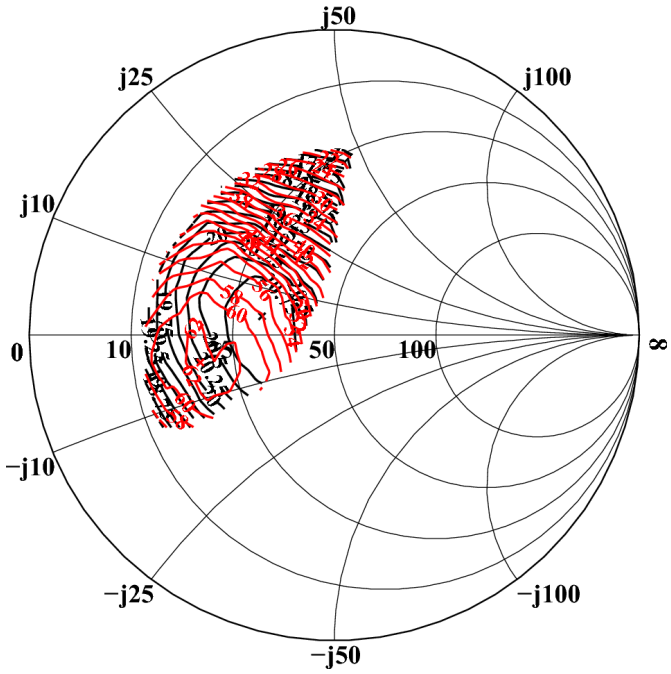


(b) Class-E Load-Pull Fixture

Figure 2.1: Fixtures for load-pull measurements. The reference planes are indicated. Note that the reference planes in the class-E fixture are located beyond the second harmonic stub. These impedance contours must be transformed through the shunt stub and series line (and tee-parasitics) in order to determine the Z_E at the transistor output. The resulting class-E impedance is $36.1+j36.9\,\Omega$.



(a) Class-A Load-Pull



(b) Class-E Load-Pull

Figure 2.2: Load-pull contours for class A and class E. The class-A impedance is chosen at $Z_A = 27.2+j15.1\,\Omega$ such that the input network for both configurations can be identical. After the reference plane transformation indicated in Figure 2.1, the resulting class-E impedance is $Z_E = 36.1+j36.9\,\Omega$. These measurements and figures are courtesy of Srdjan Pajic.

for comparison, shown in Figure 2.3, but the linearity and efficiency are quite different. Figure 2.3 shows that the class-E amplifier reaches a peak drain efficiency (η_D) at 70% and peak power-added efficiency (PAE) at 60%. The class-A amplifier reaches 30% drain efficiency at the 1 dB compression point and 28% PAE. If the class-A amplifier is overdriven, it is capable of achieving 45% drain efficiency and 40% PAE. The linearity differences between these two amplifiers are evident in the third and fifth order intermodulation products, IMD3 and IMD5 respectively, as shown in Figure 2.4. Both IMD3 and IMD5 are much lower for the class-A amplifier (indicated by the dotted lines), which is indicative of better linearity in the amplifier. Upper and lower intermodulation products are indicated by the blue and red lines respectively. Also typical of these two amplifier classes, the class-A amplifier is symmetrical in upper and lower products, while the class-E amplifier (indicated by the solid lines) is asymmetrical, most likely due to memory effects in the transistor [53].

Adding switches to the output matching network introduces loss at the output of the amplifier, reducing the output power and therefore, the efficiency of the amplifier. This loss determines the cost of reconfigurability, that is, how the ability to reconfigure reduces the performance of each state when compared to non-reconfigurable amplifiers, as discussed in Section 1.2.1.

2.1.2 MEMS Output Network Design

One method of changing the impedance of a network is to change the length of a shunt stub (see further discussion in Section 3.1). Placing a MEMS switch along a stub line results in two impedances, depending on whether the switch is in the open on closed position. The loss of a stub network with a switch changes depending on the location of the switch in the stub. Figure 2.5 shows a switch located at three different positions in the stub. The stub is 54° in length at 10 GHz, and each circuit has an input impedance of 20-$j10\,\Omega$ when the switch is in the closed state.

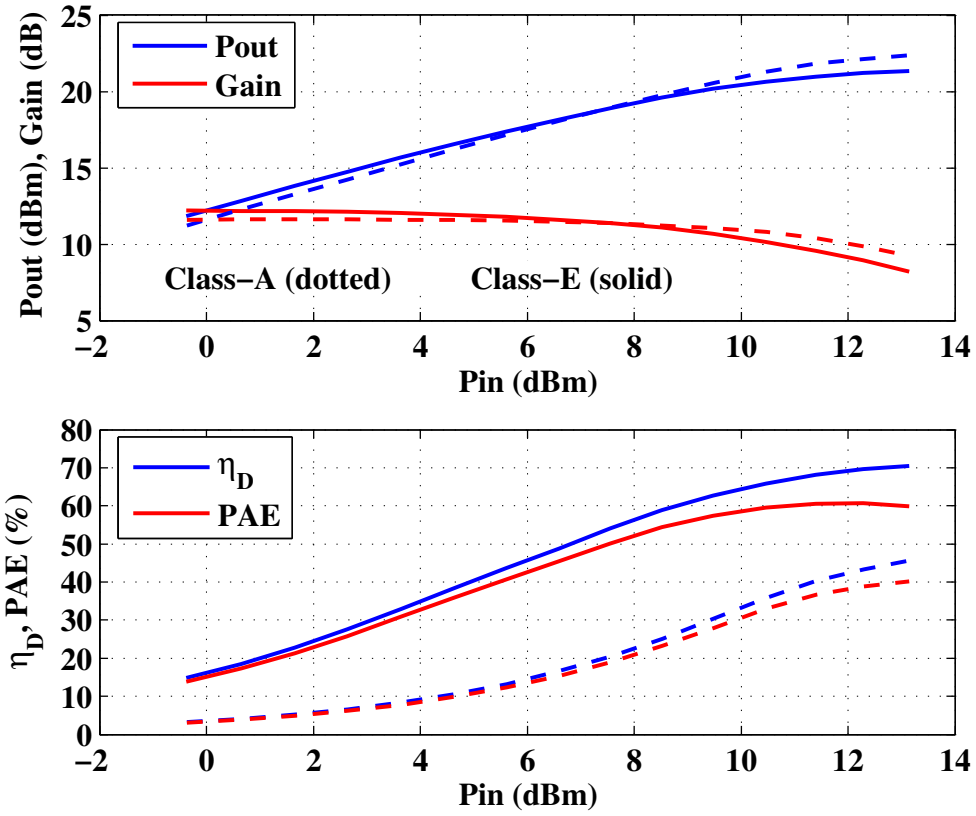


Figure 2.3: Measured power sweep comparison of class-A (dotted) and class-E (solid) amplifiers. The amplifiers are designed to deliver nearly the same output power, but have very different efficiencies.

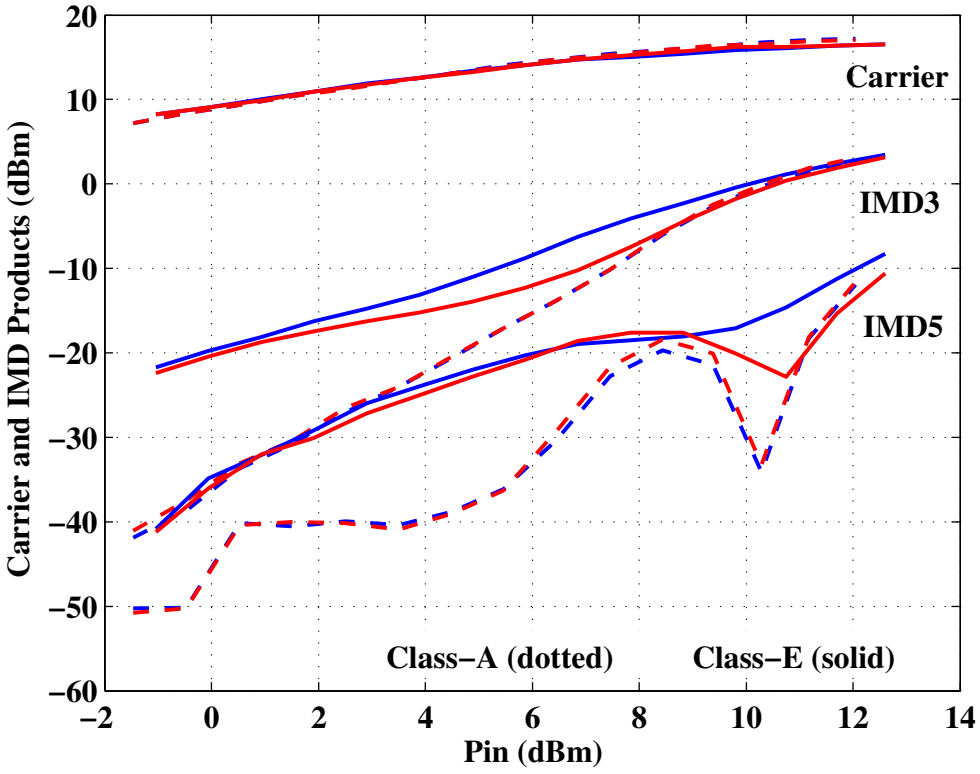


Figure 2.4: Measured two-tone analysis comparison of class-A (dotted) and class-E (solid) amplifiers, with 5 MHz tone separation at 10 GHz. The amplifiers have very different linearity characteristics, evident in the IMD3 and IMD5 products. Upper and lower intermodulation products are indicated in blue and red respectively.

As the switch is moved in the stub from a location in high current density (Base), shown in Figure 2.6, to a location of moderate current density (Middle), shown in Figure 2.7, to a location of low current density (End), shown in Figure 2.8, the insertion loss decreases. Table 2.1 shows the measured insertion loss at 10 GHz for each location and compares the loss to a microstrip line of equivalent length on alumina with gold conductors. These measurements are calibrated using a thru-reflect-line (TRL) method with a 0.01-dB thru-line ripple in S_{21} after calibration.

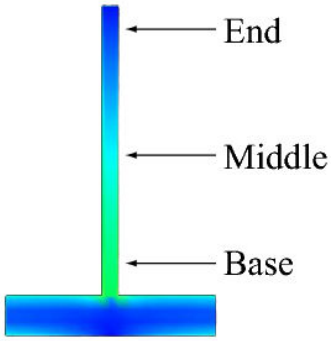
Table 2.1: Measured Effect of Position on Loss at 10 GHz

Position	IL (no MEMS)	IL (with MEMS)
Base	0.08 dB	0.18 dB
Middle	0.08 dB	0.10 dB
End	0.08 dB	0.08 dB

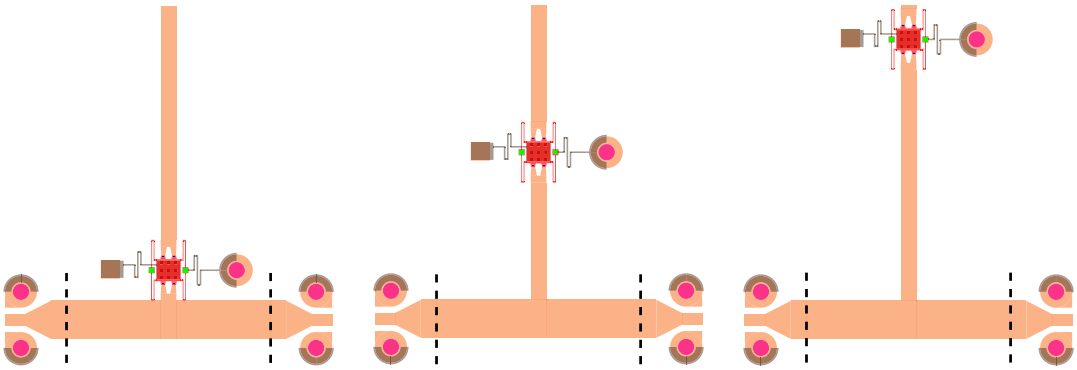
This study shows that two effects occur simultaneously as switch location is varied: impedance change, and loss change. Since the realization of impedance matching networks is not limited to a single solution, different networks can produce the same input impedance and have very different losses.

As an example, the high isolation of the MEMS switches could lead to the conclusion that the states of a reconfigurable network can be designed independently. Figure 2.6(b) shows that when the switch is located at the base of the stub, in the open position it "turns off" the stub quite effectively and the line becomes 50 Ω. However, this location has very high insertion loss due to the currents in the switch, which makes this solution undesirable.

For this reason, the states of the output network for the Class-A-to-E circuit are designed concurrently in a double-stub configuration. Full-wave EM simulations show that this configuration has lower loss than a circuit with switches at the bases of the stubs. When both switches are in the open state, the output network presents the class-A impedance to the transistor. When both switches are in the closed state, the

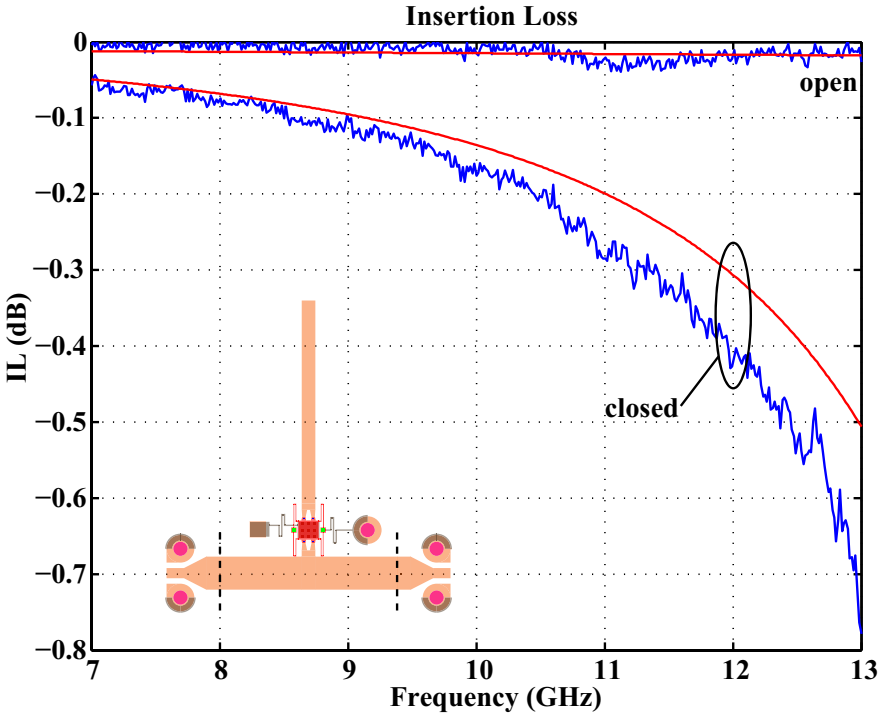


(a) Current Standing Wave (maximum magnitude at the Base point)

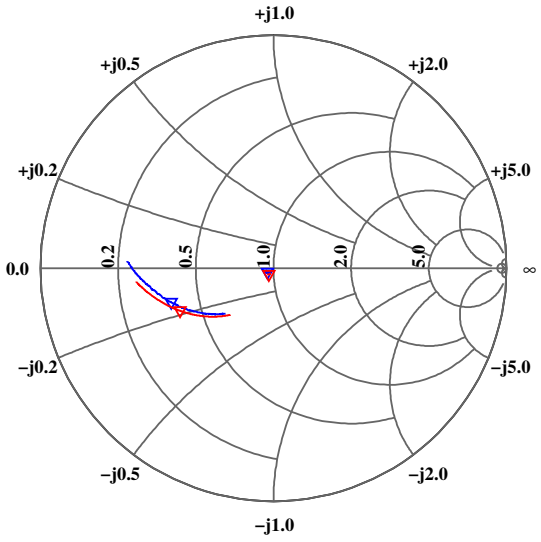


(b) Base (c) Middle (d) End

Figure 2.5: A circuit with an input impedance of 20-$j10\,\Omega$ is tested with a switch located in different positions to determine the effect of position on loss. (a) shows the current standing wave, which is at its highest (green) at the intersection of the stub and the line and at its lowest (blue) at the open end of the line. The measured insertion losses of these circuits ((b), (c), and (d)) are shown in Table 2.1 and compared to an equivalent stub without MEMS on the same substrate. Reference planes are indicated by the dashed line.

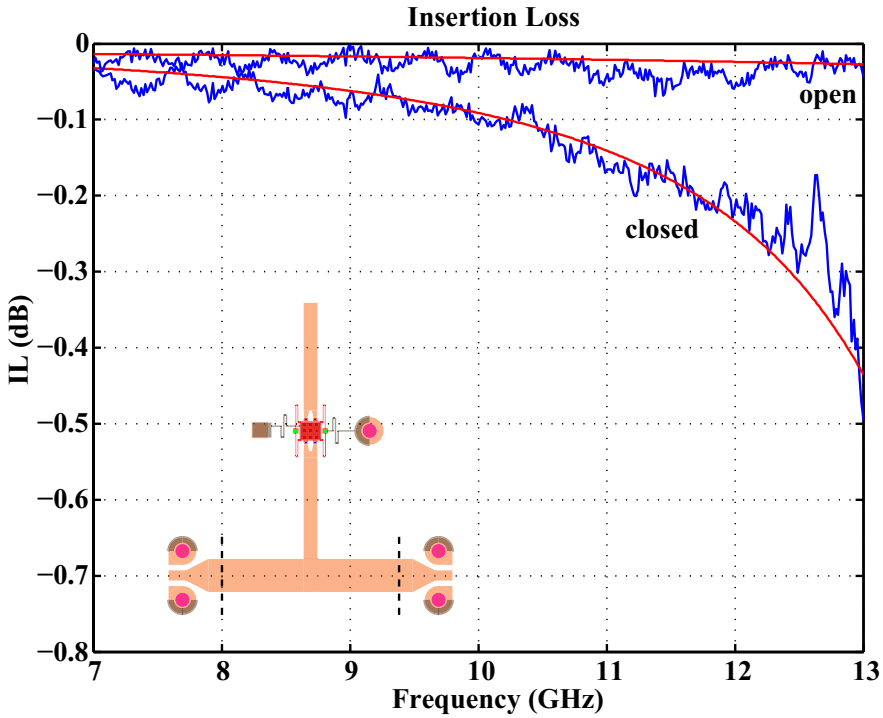


(a) Measured (blue) and simulated (red) insertion losses of a 70-Ω stub with switch at the base.

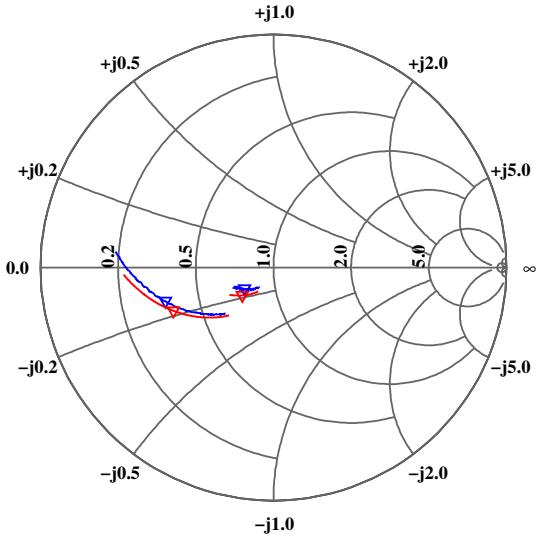


(b) Measured (blue) and simulated (red) impedances of a 70-Ω stub with a switch at the base from 7–13 GHz. The 10-GHz impedances are indicated by the ▽ markers.

Figure 2.6: Simulated and measured insertion loss (a) and impedance (b) of a 70-Ω stub with a switch at the base of the stub. The red line shows the simulated response from ADS using an equivalent circuit model for the switch, and the blue line shows the measured response.

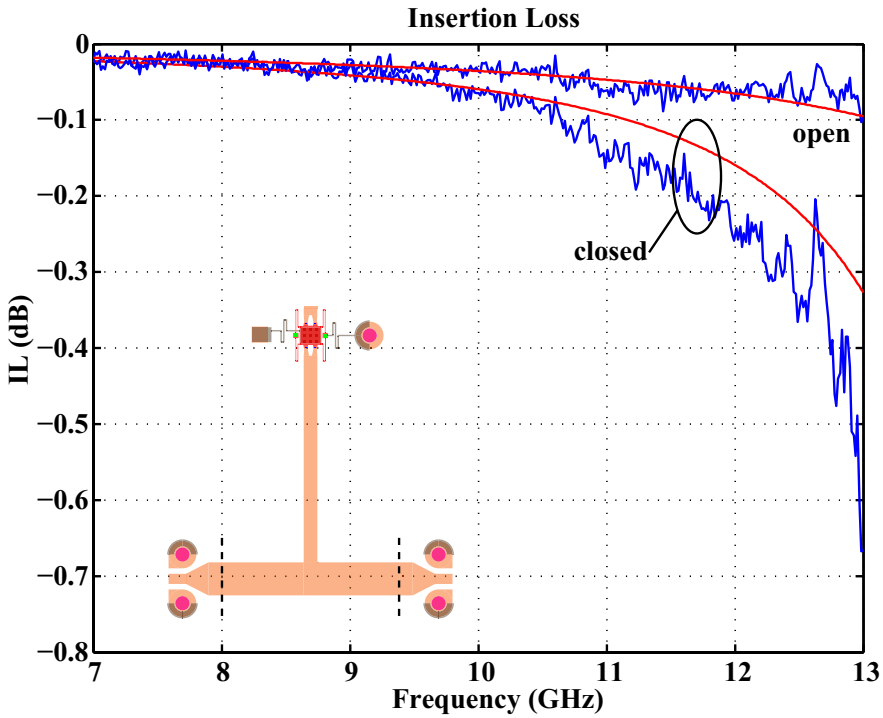


(a) Measured (blue) and simulated (red) insertion losses of a 70-Ω stub with a switch at the middle point.

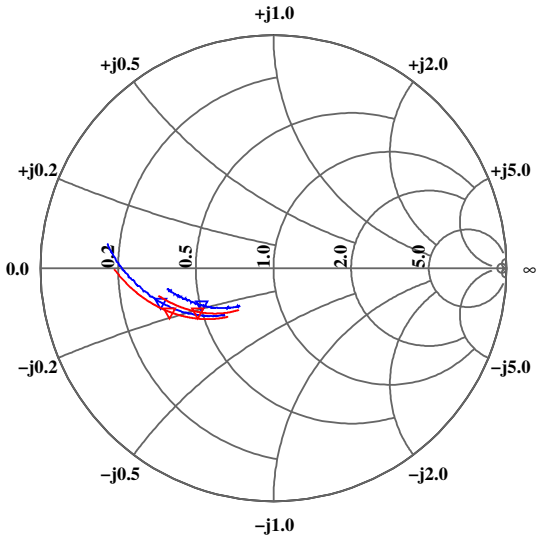


(b) Measured (blue) and simulated (red) impedances of a 70-Ω stub with a switch at the middle point from 7–13 GHz. The 10-GHz impedances are indicated by the ▽ markers.

Figure 2.7: Simulated and measured insertion loss (a) and impedance (b) of a 70-Ω stub with a switch in the middle of the stub. The red line shows the simulated response from ADS using an equivalent circuit model for the switch, and the blue line shows the measured response.



(a) Measured (blue) and simulated (red) insertion losses of a 70-Ω stub with a switch at the end.



(b) Measured (blue) and simulated (red) impedances of a 70-Ω stub with a switch at the end from 7–13 GHz. The 10-GHz impedances are indicated by the ▽ markers.

Figure 2.8: Simulated and measured insertion loss (a) and impedance (b) of a 70-Ω stub with a switch at the end of the stub. The red line shows the simulated response from ADS using an equivalent circuit model for the switch, and the blue line shows the measured response.

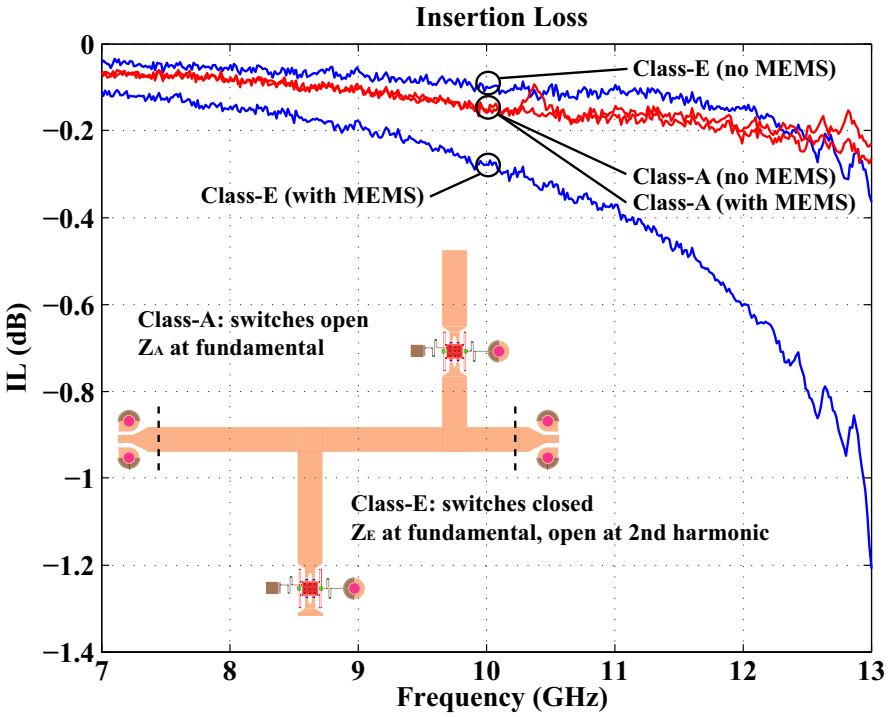
network presents the class-E fundamental impedance and an open circuit at the second harmonic.

A schematic of the output network is shown inset in Figure 2.9(a). For comparison, insertion loss of the tuned network in Figure 2.9(a) is shown along with the insertion loss of an equivalent microstrip network without MEMS for each state. Figure 2.9(b) shows the measured impedance of the network compared to the designed impedance. S-parameters are measured from 7–13 GHz using an Agilent 8510C network analyzer and a Cascade Summit 9000 probe station with 150 μm pitch ground-signal-ground (GSG) probes. A TRL calibration is included on the alumina substrate with the same CPW-to-microstrip transitions as the tuner and amplifier circuits. In the class-A state, the simulated impedance of the output network is $Z_A = 26.59+j15.34\,\Omega$ at 10 GHz, and the measured impedance is $Z_A = 25.81+j16.5\,\Omega$. The measured class-E impedance at $Z_E = 44.05+j41.9\,\Omega$ is off from the designed impedance of $Z_E = 35.94+j36.65\,\Omega$, but this difference does not adversely affect the amplifier performance based on the load-pull data. In general, class-E amplifiers are not extremely sensitive to the output match [57].

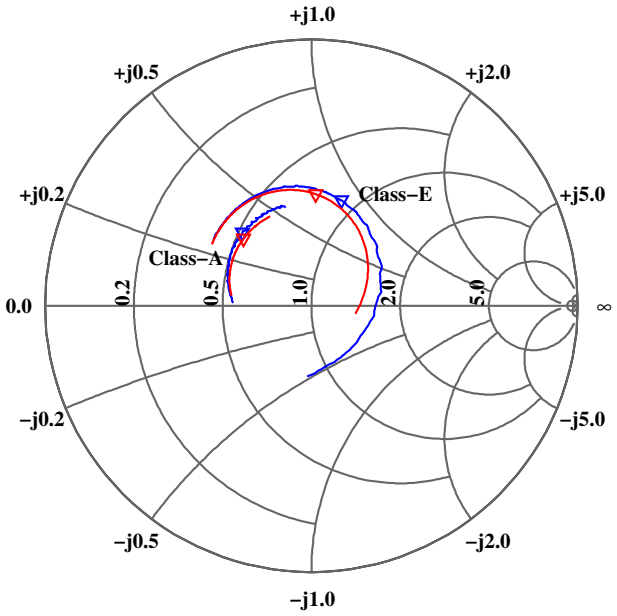
The measured insertion loss of the network in class-A mode is 0.15 dB at 10 GHz. An equivalent microstrip network for the class-A impedance also has 0.15 dB of measured insertion loss. Since the switches are in the open position for the class-A impedance, it follows that there is no distinguishable change in loss between the circuits with and without MEMS switches. The class-E mode has a measured insertion loss of 0.27 dB, and an equivalent microstrip circuit has a loss of 0.1 dB. Therefore, the reconfigurable network contributes an additional 0.17 dB of loss in the class-E mode, and no additional loss in the class-A mode.

2.2 Amplifier Characterization

In the class-A state, with the switches in the open state, the biases of the transistors in the RPA and the conventional PA are set to the class-A quiescent point from



(a) Insertion loss of the reconfigurable output circuit.



(b) Measured (blue) and simulated (red) impedances of the reconfigurable output circuit from 7–13 GHz. The 10-GHz impedances are indicated by the ▽ markers.

Figure 2.9: Measured insertion loss and input impedance of the output network in class-A (open) and class-E (closed) states, compared to networks without switches.

Section 2.1.1. Figure 2.10 shows the output power, gain, drain efficiency η_D, and PAE as a function of input power P_{in}.

This class-A design achieves 20 dBm of output power if overdriven, but the 1 dB compression point limits P_{out} to 19.7 dBm. Drain and power-added efficiencies are typical for class-A amplifiers at 10 GHz. Table 2.2 gives the performance parameters of both PAs at the 1 dB compression point.

In the class-E state, the switches are in the down state, and the biases of the transistors in the RPA and the conventional PA are set to the class-E quiescent point from Section 2.1.1. Figure 2.11 shows an input power sweep from -1.5 to 12.5 dBm.

The class-E design achieves 20 dBm of output power in both the conventional and reconfigurable amplifiers. Drain and power-added efficiencies are typical for class-E amplifiers at 10 GHz [49], with a 4% reduction in efficiency in the reconfigurable amplifier, consistent with expectations from Figure 1.2. The performance parameters of both PA types are summarized in Table 2.2.

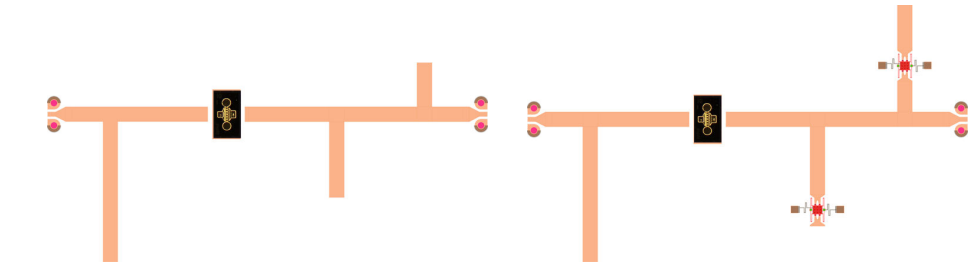
Table 2.2: Amplifier Performance Comparison

Class-A			Class-E		
Param.	Standard	Reconfig.	Param.	Standard	Reconfig.
$P_{out,1\,\mathrm{dB}}$	20.3 dBm	19.7 dBm	$P_{out,\max}$	20.7 dBm	20.6 dBm
Gain	10 dB	10 dB	Gain	7.9 dB	7.8 dB
$\eta_{D,1\,\mathrm{dB}}$	27.5%	26.6%	$\eta_{D,\max}$	61.9%	58.3%
$PAE_{1\,\mathrm{dB}}$	25.3%	24.1%	$PAE_{\max}$	53.2%	49%

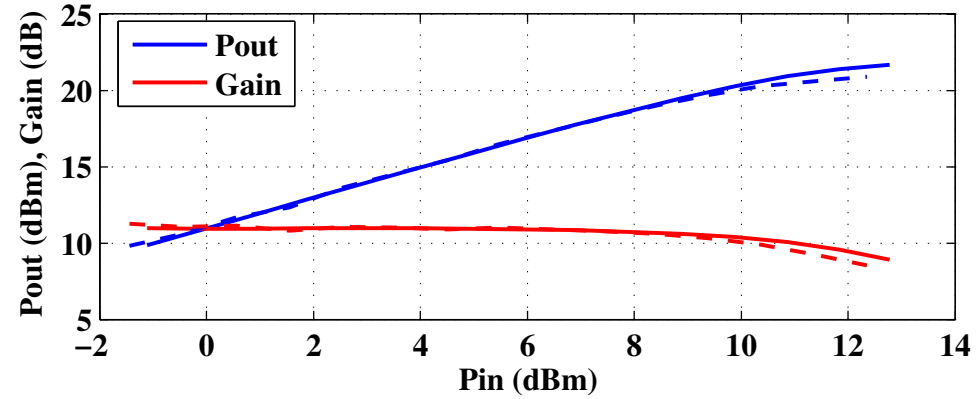
2.2.1 Two Tone Analysis

A two-tone analysis is performed on both states of the reconfigurable amplifier and on the standard class-A and class-E amplifiers for comparison. The tones are separated by 5 MHz at 10 GHz (0.05% bandwidth) and are calibrated to have equal input power.

Both the class-A and class-E cases, shown in Figures 2.12 and 2.13, show similar



(a) Standard (solid line) (b) Reconfigurable (dotted line)



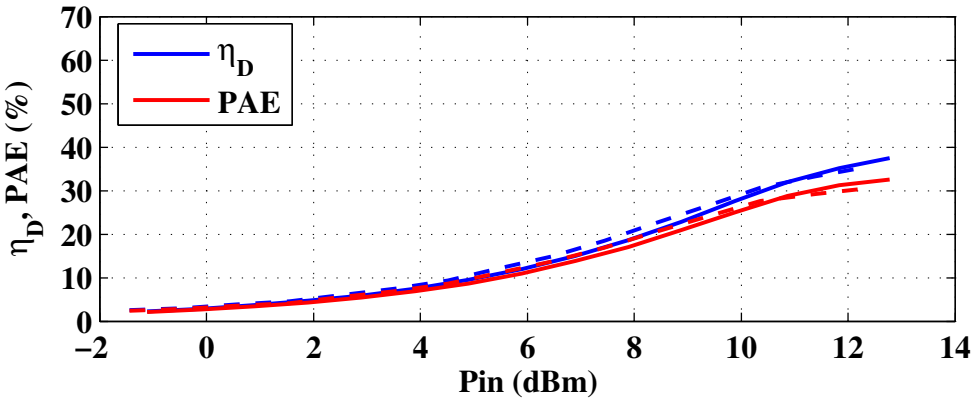
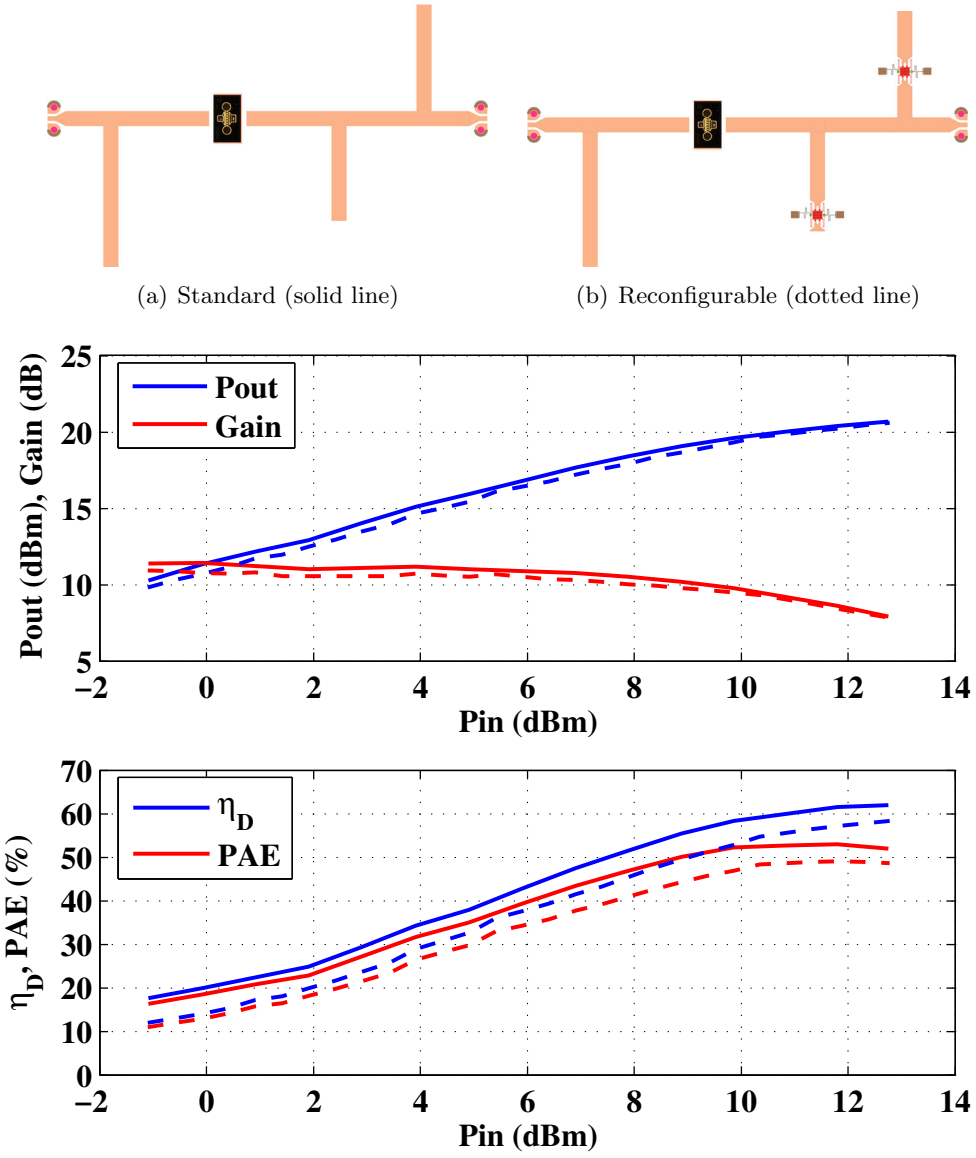


Figure 2.10: Output power (blue), gain (red), drain efficiency (blue), and PAE (red) comparison of a standard class-A PA from (a) (solid) and the reconfigurable PA in class-A mode from (b) (dotted). The switches are open in (b), and the performance of the two amplifiers is nearly identical.



(a) Standard (solid line) (b) Reconfigurable (dotted line)

Figure 2.11: Output power (blue), gain (red), drain efficiency (blue), and PAE (red) comparison of a standard class-E PA from (a) (solid) and the reconfigurable PA in class-E mode from (b) (dotted). The switches are closed in (b), and the additional insertion loss of the MEMS switches lowers the efficiency of the reconfigurable amplifier.

behavior when the intermodulation products of the standard PA (solid) and the reconfigurable PA (dotted) are compared. The upper and lower intermodulation products are indicated in blue and red respectively.

2.2.2 Class-AB Case

Changing the load impedance of an amplifier is not the only means of changing the amplifier class of operation. Reducing the conduction angle of a class-A amplifier into a a class-AB mode (by decreasing the quiescent drain current) [53] results in an increase in efficiency from the class-A state, even if the amplifier is not optimized for class-AB operation as is the case here. Figure 2.14 shows a power sweep of the two amplifiers under test: the reconfigurable amplifier in its class-E state, and the standard class-A amplifier given an AB bias. The class-AB amplifier (solid) has similar output powers to the class-E amplifier (dotted), and is capable of achieving similar drain and power-added efficiencies if driven into compression. Figure 2.15 shows a two-tone analysis of both amplifiers, showing that they have similar linearity characteristics in IMD3 and IMD5. Table 2.3 shows a comparison of the output power, gain, and efficiencies of the class-AB and class-E cases when driven at maximum input power.

Table 2.3: Amplifier Performance Comparison, Class-AB and Class-E

Class-AB		Class-E		
Param.	Standard	Param.	Standard	Reconfig.
$P_{out,\max}$	21.1 dBm	$P_{out,\max}$	20.7 dBm	20.6 dBm
Gain	8.5 dB	Gain	7.9 dB	7.8 dB
$\eta_{D,\max}$	57.2%	$\eta_{D,\max}$	61.9%	58.3%
$PAE_{\max}$	49%	$PAE_{\max}$	53.2%	49%

With the same input power, the class-AB amplifier has higher output power, higher gain, and efficiencies within 1% of the reconfigurable class-E amplifier. This indicates that similar performance can be achieved by a standard amplifier with only a

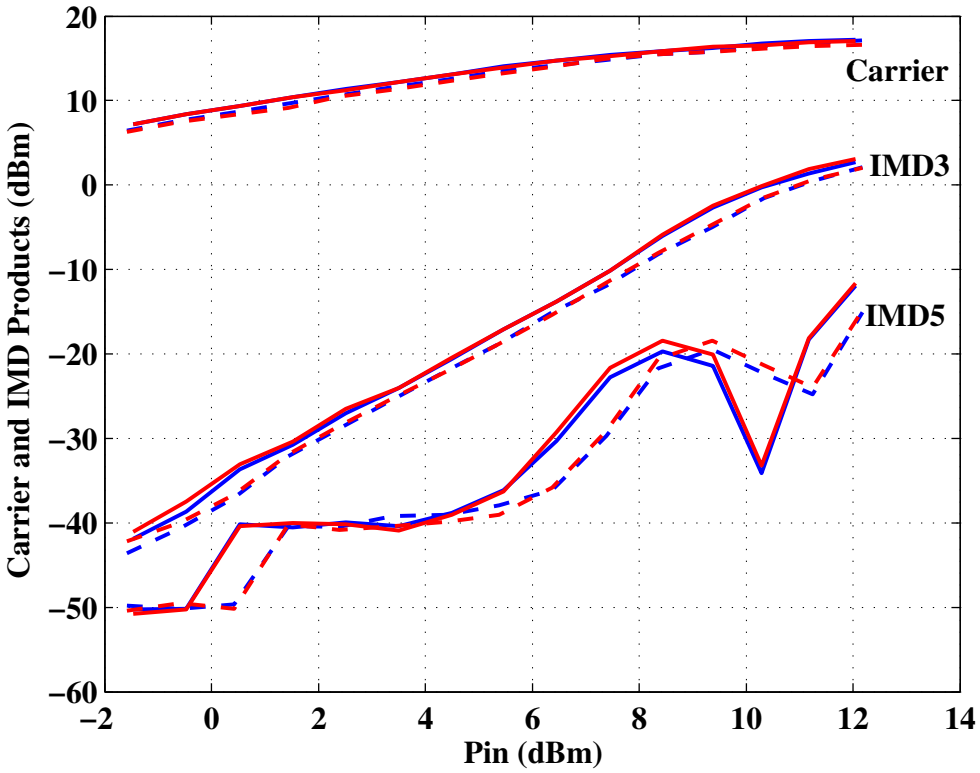


Figure 2.12: Comparison of a two-tone analysis with 5 MHz tone separation between the reconfigurable PA in class-A mode (dotted) with a standard class-A PA (solid). The upper product is in blue and the lower product is in red.

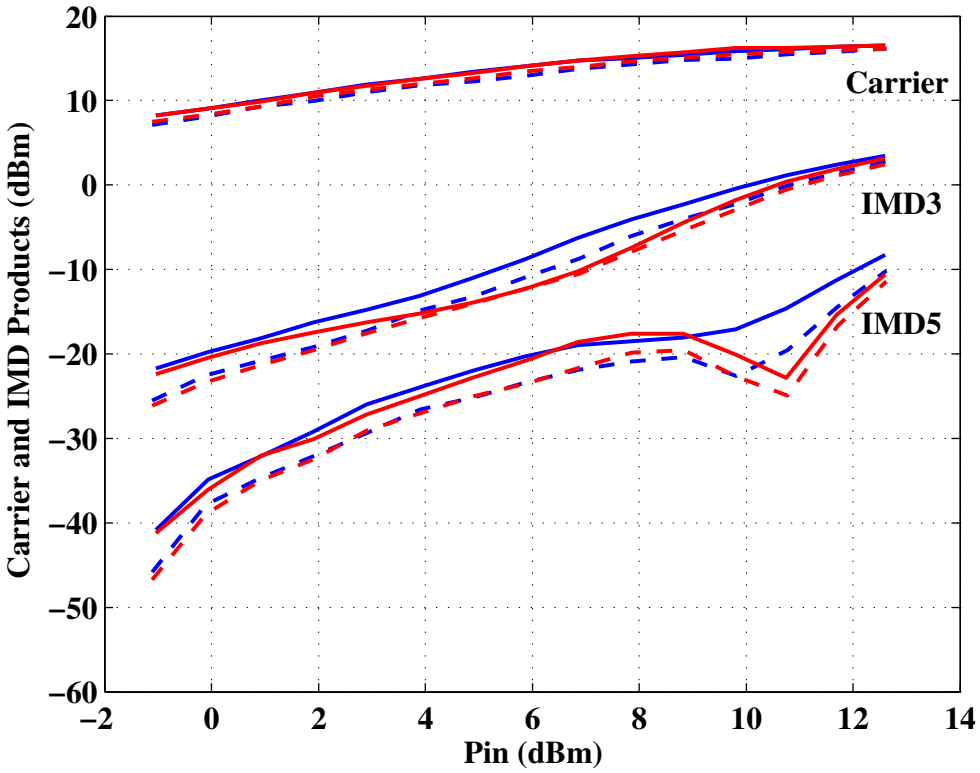
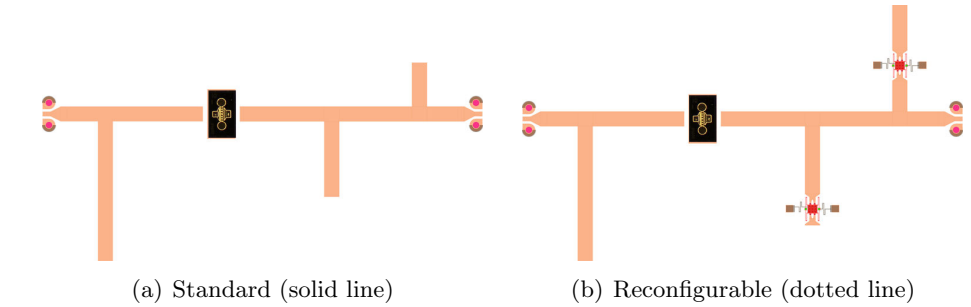
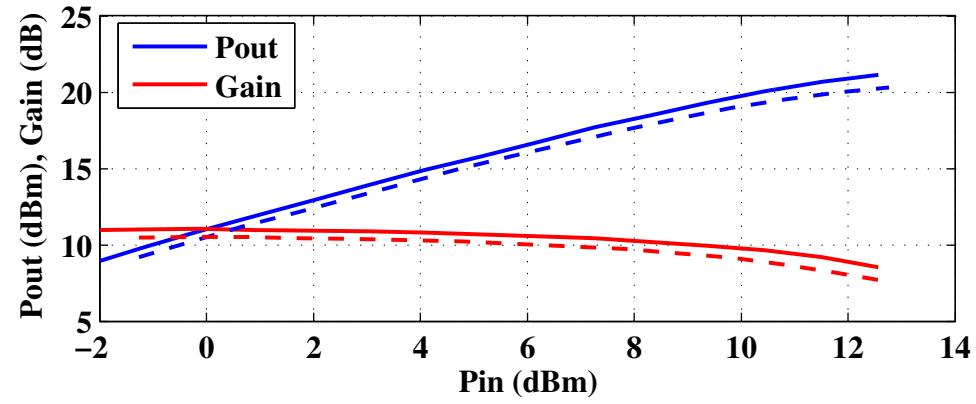


Figure 2.13: Comparison of a two-tone analysis with 5 MHz tone separation between the reconfigurable PA in class-E mode (dotted) with a standard class-E PA (solid). The upper product is in blue and the lower product is in red.



(a) Standard (solid line) (b) Reconfigurable (dotted line)



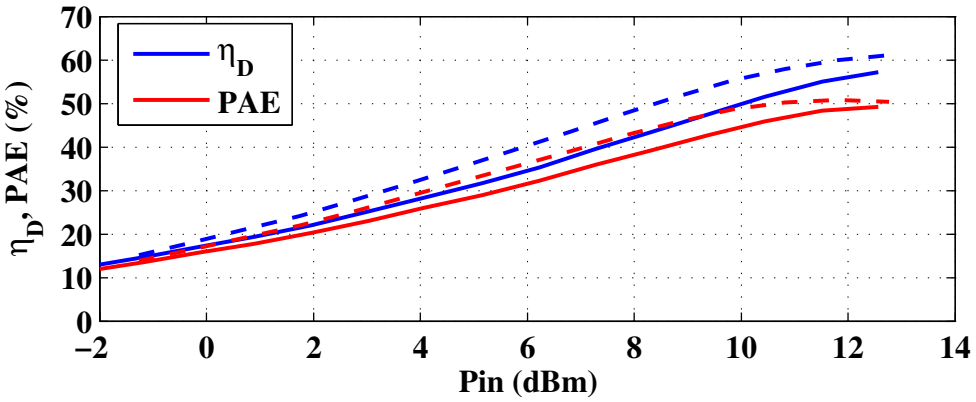


Figure 2.14: Output power (blue), gain (red), drain efficiency (blue), and PAE (red) comparison of a non-optimized class-AB PA from (a)(solid) and the reconfigurable PA in class-E mode from (b) (dotted). The switches are closed in (b), and the performance of the two amplifiers is very similar. This indicates that nearly the same output power and efficiencies could be met by changing the bias alone, without the additional complexity of the MEMS in the output network.

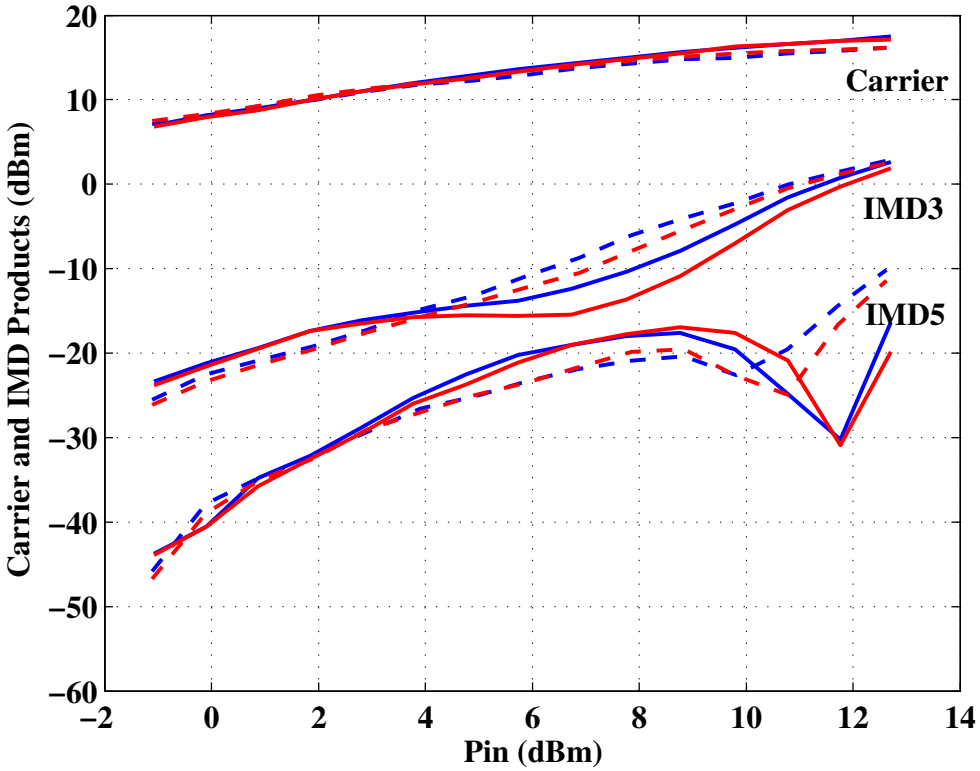


Figure 2.15: Comparison of a two-tone analysis with 5 MHz tone separation between the reconfigurable PA in class-E mode (dotted) and the standard amplifier with a class-AB bias (solid). The upper product is in blue and the lower product is in red.

reconfigurable bias, and no MEMS devices in the output network.

One reason the class-E and class-AB cases are so similar, even though class-E is theoretically capable of much higher efficiencies, is that the reconfigurable network adds loss which decreases the power-added efficiency of the class-E amplifier. This experiment demonstrates the necessity of designing the amplifier state with the highest efficiency to have the lowest loss. If the reconfigurable amplifier could obtain the class-E state with the MEMS switches in the open position, it would not have the 4–5% reduction in efficiency from the standard amplifier, which would separate the class-AB and class-E efficiencies by 5%. This improvement in efficiency could possibly justify the added complexity of a reconfigurable output network. Figure 1.2 shows the effect of increasing insertion loss on an amplifier with a starting efficiency of 25% in orange, in comparison to an amplifier with a starting efficiency of 55%, which is shown in red.

Chapter 3

Theory and Design of Tunable Impedance Transformation Networks

In Chapter 2, it is established that a simple two-state class-A-to-E reconfigurable power amplifier (RPA) could be designed with less than a 5% degradation in power-added efficiency (PAE) from its conventional equivalents. In this chapter, a more complex output network is designed to enable "tuning" of an amplifier.

A reconfigurable amplifier can switch between multiple pre-defined states, as is shown in Chapter 2, and in [44–46]. A tunable amplifier can adjust to optimize for changes in the operating conditions.

In order to design a tunable output matching network, the classical lumped-element, shunt-stub, and series-slug matching networks are examined first, noting what elements are required to tune in order to produce a constellation of impedance points on the Smith Chart. The double-slug network is chosen for the final design, and this chapter details its implementation using the Sandia ohmic MEMS switch.

3.1 Impedance Transformation Networks

Impedance matching networks can be divided into three categories: lumped-element, shunt-stub, and series-slug. Each of these networks have a range of impedances that they can match, and a forbidden region where they cannot match. In the following section, each of these classes are examined to determine the forbidden regions and what elements must vary in order to produce a constellation. Additional information may be

found in [58, 59].

Each network in the following sections is analyzed with respect to Z_{in}, the input impedance of the network, assuming a 50-Ω load ($Z_L = Z_0 = 50\,\Omega$). The constellations shown are the constellations of points that the network can produce; in order to match, these impedances must be the complex conjugate of the source - the transistor output in this case. (Note that in [58], and arbitrary load is matched to Z_0. In the cases below, a $Z_L = Z_0$ load is transformed through the network to show the possible Z_{in} points that can be matched to Z_0, which is opposite from [58].)

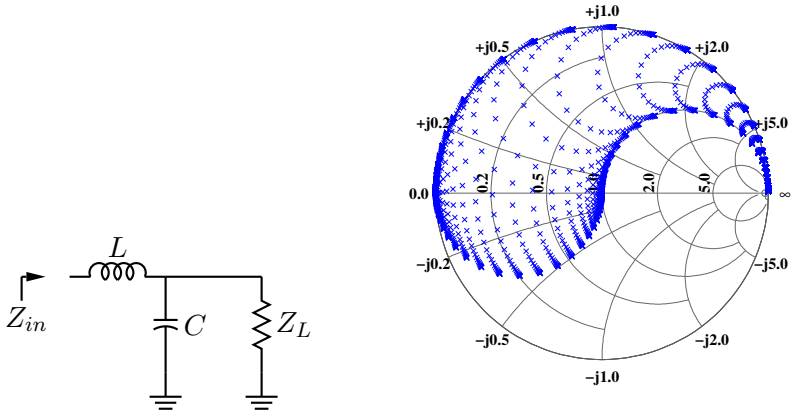
3.1.1 Lumped-Element Networks

The simplest lumped-element matching networks are the L-type. There are eight variations of the L-type network, depending on the order of the elements and whether they are in series or in shunt.

Figure 3.1 shows a series inductor and a shunt capacitor, which is capable of matching half of the Smith chart. The values of L_s and C_p are allowed to vary logarithmically from 10^{-4} to 10^4 to give the full range of constellation. Both L_s and C_p must vary in order to produce a constellation of points. Variable inductors are difficult to realize. A series variable inductor is often approximated using a shunt variable capacitor and an impedance inverter, but these solutions are inherently narrowband.

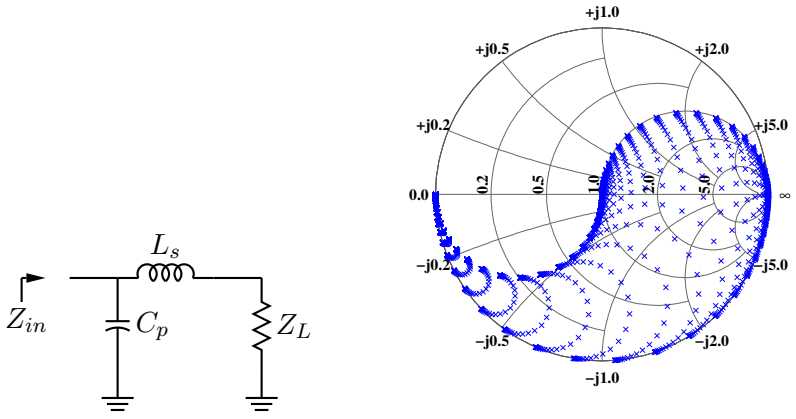
Similarly, changing the position of the elements in Figure 3.1 yields coverage of half of the Smith Chart, however the constellation is the complement of the one in Figure 3.1(b), as shown in Figure 3.2(b). As before, both L_s and C_p must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on L_s and C_p are in place. Realizing a variable inductor with a variable capacitor and impedance inverter gives a narrowband solution.

Additionally, the configuration of a series capacitor and shunt inductor can cover over half of the Smith Chart, as shown in Figure 3.3. Both C_s and L_p must vary in



(a) (b)

Figure 3.1: A series inductor and shunt capacitor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). In this case, both L_s and C_p must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on L_s and C_p are in place.



(a) (b)

Figure 3.2: A shunt capacitor and series inductor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). In this case, both C_p and L_s must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on C_p and L_s are in place.

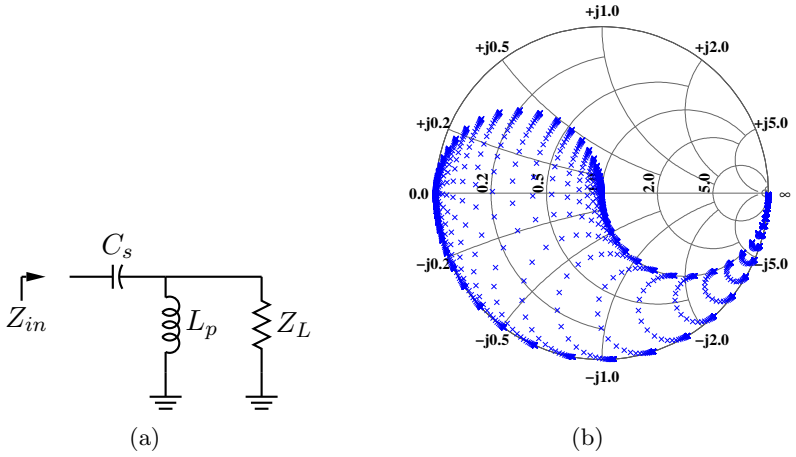
order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on C_s and L_p are in place. Realizing a variable inductor with a variable capacitor and impedance inverter gives a narrowband solution. One significant disadvantage of this type of network is in biasing, since the shunt inductor will provide a short circuit at dc. This network, and its complement shunt inductor and series capacitor network shown in Figure 3.4 are not often used in active applications for this reason.

If the series and shunt elements are the same, the L-networks can match a smaller are of the Smith Chart, as shown in Figures 3.5 and 3.6. In these cases, the order of the elements does not affect the matching region. Both elements must vary in order to produce a constellation. The inductor network has the problem of being a dc short for biasing as discussed in Figures 3.3 and 3.4.

Expanding the concept of the L-network to include one additional element, forming a Pi-network (or equivalently, a T-network), allows coverage of the entire Smith Chart. This network is shown in Figure 3.7 in the shunt capacitor-series inductor-shunt capacitor configuration, which does not have the biasing problems associated with the shunt inductor networks. All three elements must vary in order to produce a constellation. This type of network is used in [39, 43, 47], as discussed in Chapter 1. A 10-GHz varactor diode implementation was tested at the University of Colorado for use with class-E power amplifiers in a array [60].

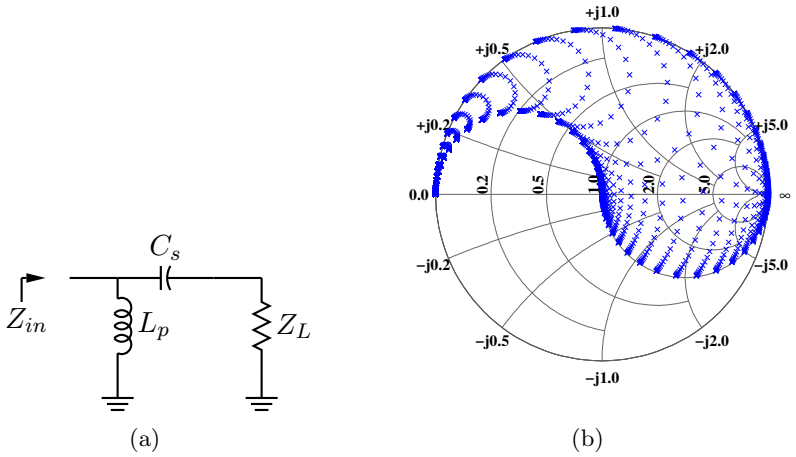
3.1.2 Shunt-Stub Networks

A second class of matching networks are the shunt-stub networks (the series-stub networks are not readily realizable in many physical layouts and are not discussed here). Shunt stubs are a common form of microstrip matching network, since all the lines and stubs are of the same characteristic impedance. Shunt stubs can be divided into two sub-classes: open stub and shorted stub. In this section, only open stubs are considered



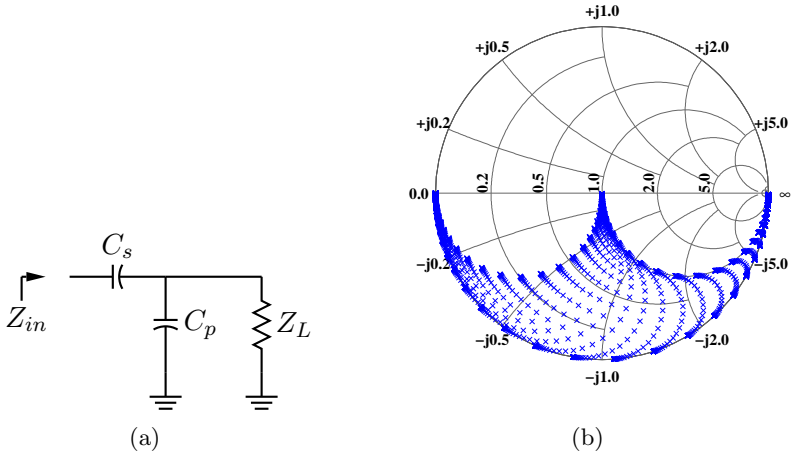
(a) (b)

Figure 3.3: A series capacitor and shunt inductor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). In this case, both C_s and L_p must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on C_s and L_p are in place.



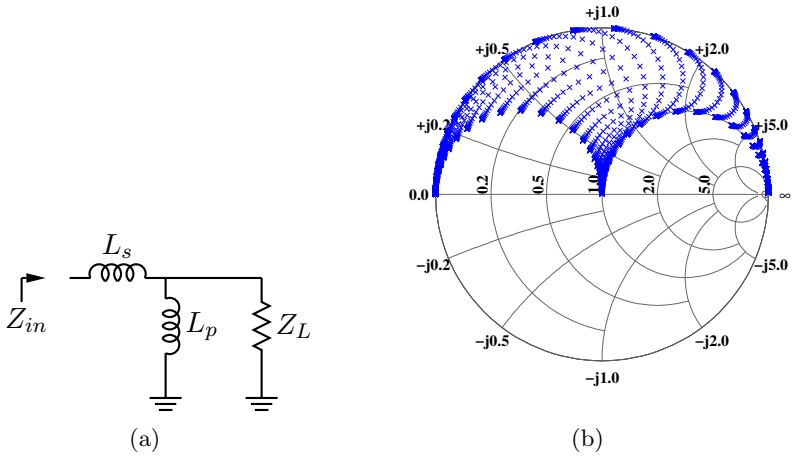
(a) (b)

Figure 3.4: A shunt inductor and series capacitor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). In this case, both L_p and C_s must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on C_s and L_p are in place.



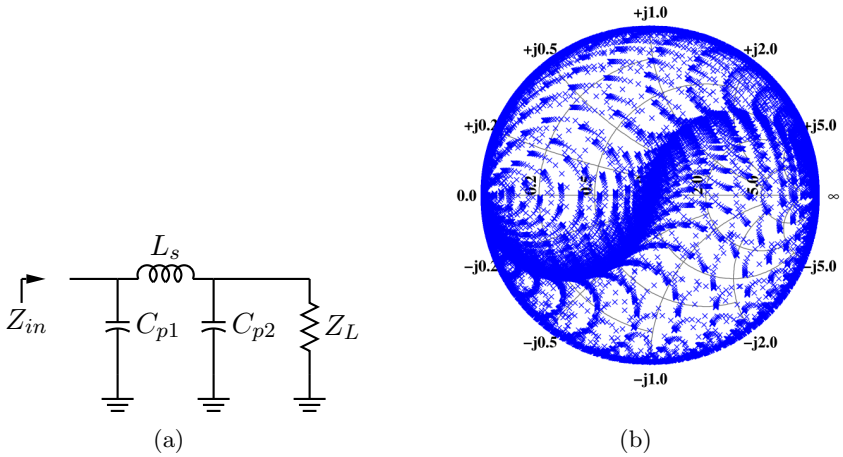
(a) (b)

Figure 3.5: A series capacitor and a shunt capacitor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). Both C_s and C_p must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on C_s and C_p are in place.



(a) (b)

Figure 3.6: A series inductor and a shunt inductor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). Both L_s and L_p must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on L_s and L_p are in place.



(a) (b)

Figure 3.7: A shunt capacitor-series inductor-shunt capacitor lumped-element matching network. The equivalent circuit is shown in (a), and the constellation of Z_{in} which can be matched to $Z_L = Z_0 = 50\,\Omega$ is given in (b). In this case, all three elements, C_{p1}, L_s, and C_{p2} must vary in order to produce a constellation of points, typically a subset of the region shown in (b) once practical limitations on L_s, C_{p1}, and C_{p2} are in place. This type of network is used in [39, 43, 47], as discussed in Chapter 1. A 10-GHz varactor diode implementation was tested at the University of Colorado for use with class-E power amplifiers in a array [60].

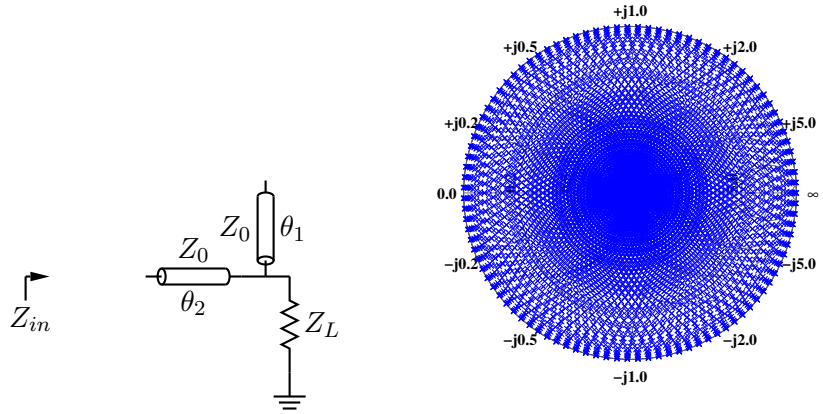
(the most readily realizable in microstrip layouts), however the same principles apply to shorted stubs.

A single stub allowed to vary from 0–180° in electrical length placed at a distance between 0–180° from impedance the network is to match is capable of covering the entire Smith Chart. This configuration is shown in Figure 3.8. However, making this configuration tunable would require both the length of the stub (θ_1) to change (which could be possible with shorting switches or adding incremental lengths, albeit the latter solution would be very lossy), and the position of the stub (θ_2) to change. Changing the position of the stub is not possible, though a loaded transmission line could be capable of altering θ_2 to a small degree. A true-time delay phase shifter could also change θ_2, though such an implementation would add significant complexity to the circuit.

Alternatively, a double-stub configuration fixes the length between the two stubs, θ_2, shown in Figure 3.9(a). In this implementation, all stubs and lines have a constant characteristic impedance Z_0, and only θ_1 and θ_3 vary. This configuration is common in microstrip applications where manual "tweaking" of the impedance is required, since the stubs can be trimmed or lengthened easily.

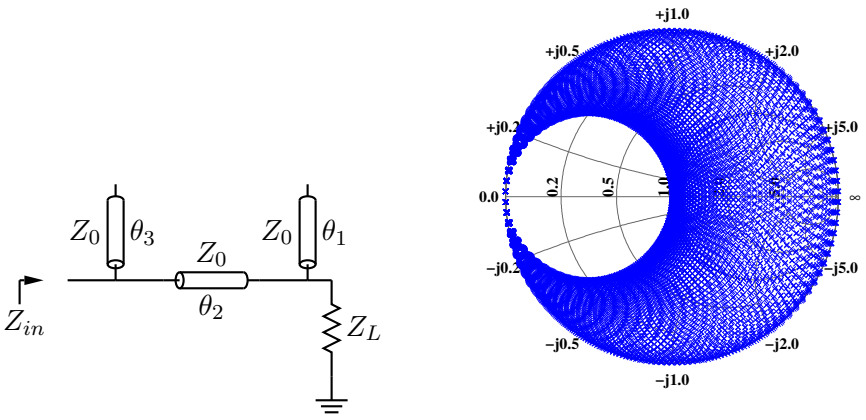
One drawback of the double-stub configuration is the forbidden region, which is within the $g = 1$ circle in Figure 3.9(b). The size of this forbidden region depends on θ_2. The region is at a maximum (shown here) when $\theta_2 = 90°$, and decreases as θ_2 becomes smaller or larger. However, the decreased area of the forbidden region comes at the cost of increased sensitivity to θ_1 and θ_2 to the point where it can be impractical to realize the circuit. In the case of the open stubs, shown in Figure 3.9, the forbidden region is on the open-circuit side of the Smith Chart. Shorted stubs have a forbidden region on the short-circuit side. The forbidden region may also be rotated to a "convenient" location on the Smith Chart with the addition of another series transmission line between Z_{in} and the θ_3 stub.

A triple-stub network, not shown, can cover the entire Smith Chart with a fixed



(a) (b)

Figure 3.8: A single shunt stub matching network (with an open-circuit termination in this example) with a length θ_1 between 0–180°, placed at a position θ_2 between 0–180° from the impedance the network is to match is capable of covering the entire Smith Chart. A circuit representation is shown in (a), with the Smith Chart coverage shown in (b). The characteristic impedance Z_0 remains constant throughout the circuit, but both the length of the stub and the position of the stub must vary in order to produce a constellation. While the length of the stub could be modified using switches to short the line or incrementally increase its length in order to vary θ_1, it is impossible to vary θ_2.



(a) (b)

Figure 3.9: A double shunt stub matching network (with open-circuit terminations in this example) requires only θ_1 and θ_3 to vary from 0–180°. The distance between the stubs, θ_2, is fixed. The characteristic impedances of all the lines and stubs remains constant at Z_0. This configuration is more suitable to tuner applications, however it has a forbidden region. The size of this forbidden region depends on θ_2 and the solution becomes increasingly sensitive to θ_1 and θ_3 as the forbidden region becomes smaller.

distance between the three stubs and requiring only the lengths of the stubs to vary.

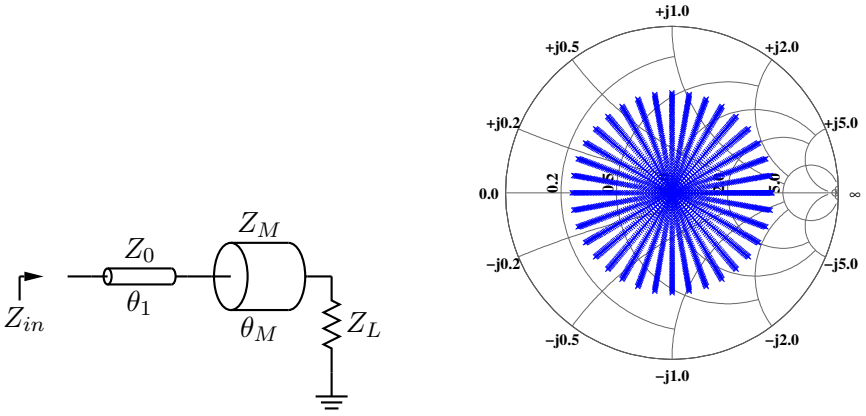
3.1.3 Series-Slug Networks

A third class of matching networks is the series-slug network. These slug networks are most often implemented mechanically, with dielectric blocks called slugs that are mechanically positioned in the transmission line between the center conductor and ground to change its characteristic impedance from Z_0 to Z_M. In this case, the slug has a fixed electrical length, typically 90° at the operating frequency.

The single slug has a common microstrip realization, the quarter-wave transformer. A quarter-wave transformer can match any real impedance to any other real impedance. By addition of a transmission line of length θ_1 between the 90° slug section and the impedance to be matched (shown in Figure 3.10(a)), a circular region of the Smith Chart is covered. This region is shown in Figure 3.10(b). The radius of the region is determined by the maximum value of Z_M, which must be allowed to vary in order to produce a constellation. θ_1 must also vary. It may be possible to design this type of network with a discretized transmission line loaded with variable capacitors. As the capacitance changes, the characteristic impedance changes. However the phase of each discrete section also changes, which creates difficulty in achieving a consistent constellation.

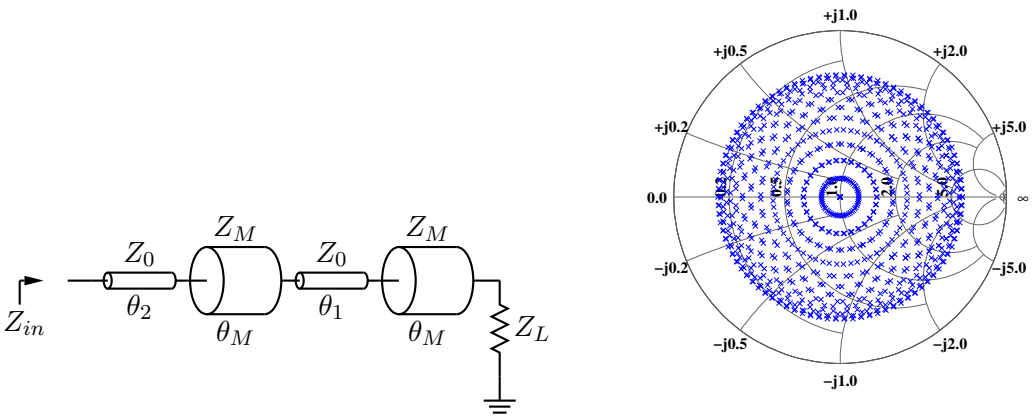
A double-slug configuration has slugs with constant Z_M and constant length $\theta_M = 90°$. The position of the slugs, θ_1 and θ_2 must vary in order to give the constellation shown in Figure 3.11(b). The radius of the coverage region depends on the value of Z_M. Again, a discretized transmission line may be used to implement this configuration. In this case, the transmission line could be loaded with switches to change the characteristic impedance from Z_0 to Z_M. Since the impedances are both constant values, it is easier to control the phase of each discrete section.

Since the double-slug tuner requires a straightforward operation (changing from



(a) (b)

Figure 3.10: A single series slug matching network (a) can match impedances within a circle on the Smith Chart (b). The radius of the region is determined by the maximum value of Z_M, which must vary along with θ_1 in order to produce this constellation.



(a) (b)

Figure 3.11: A double series slug matching network (a) has constant slug impedances, Z_M, with constant lengths, θ_M. This configuration also produces a circular constellation on the Smith Chart, with an outer radius defined by Z_M. The lengths of line between the slugs and from the slugs to Z_{in} must vary to produce this constellation.

one impedance to another in discrete segments of a transmission line) and produces a circular constellation, this network is chosen for the impedance tuner design. The circular constellation will be beneficial in integrating the tuner with a larger circuit, since the constellation will not be sensitive to the length of transmission line between the tuner and the other components of the circuit.

3.2 Theory of the Double-Slug Network

A double-slug tuner consists of two sections of transmission line with fixed characteristic impedances (Z_M) and electrical lengths (θ_M) connected in series with a variable-length transmission line of a different characteristic impedance (Z_0) as shown in Figure 3.12. The slugs are typically one-quarter wavelength long. Their position is allowed to vary by varying the length of θ_1 and θ_2 between 0 and 180°. This tuner is capable of eliminating standing waves up to a value dependent on Z_M, and the criteria for designing the tuner are described in this section. For completeness, a third section of Z_0 transmission line of length θ_3 is included such that the overall length of the tuner is constant. In this analysis, referring to Figure 3.12, $Z_S = Z_L = Z_0$.

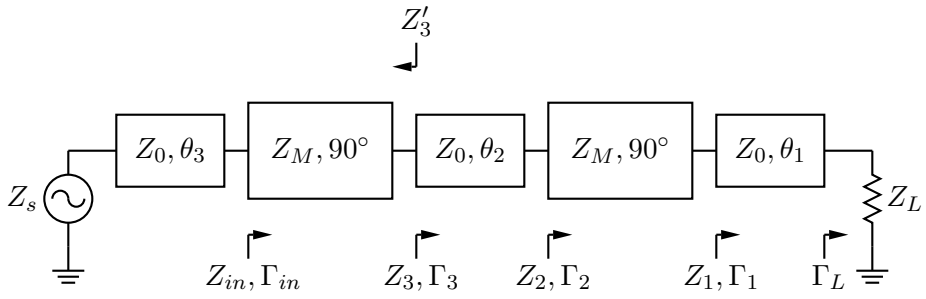


Figure 3.12: A double slug tuner consists of two 90° matching slugs with impedance Z_M in series with a transmission line of impedance Z_0. The position of these slugs is allowed to vary by varying the length of θ_1 and θ_2 between 0 and 180°. For completeness, a third section of Z_0 transmission line of length θ_3 is included such that the overall length of the tuner is constant.

The tuner analysis is divided into sections as indicated in Figure 3.12. The input

impedances and reflection coefficients at each of the sections are as follows:

$$Z_1 = Z_0\frac{1+\Gamma_L e^{-2j\theta_1}}{1-\Gamma_L e^{-2j\theta_1}}, \qquad \Gamma_1 = \frac{Z_1 - Z_M}{Z_1 + Z_M}, \tag{3.1}$$

$$Z_2 = Z_M\frac{1-\Gamma_1}{1+\Gamma_1}, \qquad \Gamma_2 = \frac{Z_2 - Z_0}{Z_2 + Z_0}, \tag{3.2}$$

$$Z_3 = Z_0\frac{1+\Gamma_2 e^{-2j\theta_2}}{1-\Gamma_2 e^{-2j\theta_2}}, \qquad \Gamma_3 = \frac{Z_3 - Z_M}{Z_3 + Z_M}, \tag{3.3}$$

$$Z_{in} = Z_M\frac{1-\Gamma_3}{1+\Gamma_3}, \qquad \Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0}. \tag{3.4}$$

Since Z_M is a quarter-wave line,

$$Z_3' = \frac{Z_M^2}{Z_0}. \tag{3.5}$$

Likewise, substituting Γ_2 from Eq. 3.2 into Z_3 from Eq. 3.3 gives

$$\begin{aligned} Z_3' &= Z_0\frac{(Z_2+Z_0)+(Z_2-Z_0)e^{-2j\theta_2}}{(Z_2+Z_0)-(Z_2-Z_0)e^{-2j\theta_2}} \\ &= \frac{Z_0Z_2(1+e^{-2j\theta_2})+Z_0^2(1-e^{-2j\theta_2})}{Z_0(1+e^{-2j\theta_2})+Z_2(1-e^{-2j\theta_2})} \end{aligned} \tag{3.6}$$

The maximum of this equation occurs at $\theta_2 = \pi/2$. Then substituting Γ_1 from Eq. 3.1 into Z_2 in Eq. 3.2 gives

$$Z_3 = \frac{Z_0^2}{Z_2}, \tag{3.7}$$

$$\text{and } Z_2 = Z_M\frac{(Z_1+Z_M)-(Z_1-Z_M)}{(Z_1+Z_M)+(Z_1-Z_M)} = \frac{Z_M^2}{Z_1}.$$

Therefore $Z_3 = Z_0^2/Z_M^2$. All that remains in determining Z_3 is to determine Z_1. If θ_1 is chosen such that Z_1 is real, $|\Gamma_L|$ remains the same, and

$$Z_3' = Z_3 = \frac{Z_M^2}{Z_0} = \frac{Z_0^3(1+|\Gamma_L|)}{Z_M^2(1-|\Gamma_L|)}. \tag{3.8}$$

Therefore, the maximum voltage standing wave ratio and maximum Γ_L the tuner can match to Z_0 are

$$VSWR = \frac{1-|\Gamma_L|}{1+|\Gamma_L|} = \left(\frac{Z_M}{Z_0}\right)^4, \tag{3.9}$$

$$\text{and } |\Gamma_L| = \left|\frac{Z_M^4 - Z_0^4}{Z_M^4 + Z_0^4}\right|. \tag{3.10}$$

3.3 Design of an Electrically Reconfigurable Double-Slug Network

The double-slug network requires transmission lines with two impedances, the slug impedance, Z_M, and the line impedance, Z_0. The slug impedance has a fixed electrical length (90°), however the electrical length of the line section must vary from 0–180° in length to complete the double-slug solution. In a mechanical realization of this network, the slugs physically move along the transmission line to vary θ_1 and θ_2.

An electrical realization using MEMS devices requires discretization of the transmission line, as shown conceptually in Figure 3.13. Both Z_M and Z_0 sections of transmission line are separated into θ_M and θ_0 segments. The Z_M sections must total 90° (which in this example requires two θ_M sections), and the Z_0 sections must total θ_1, θ_2, and θ_3.

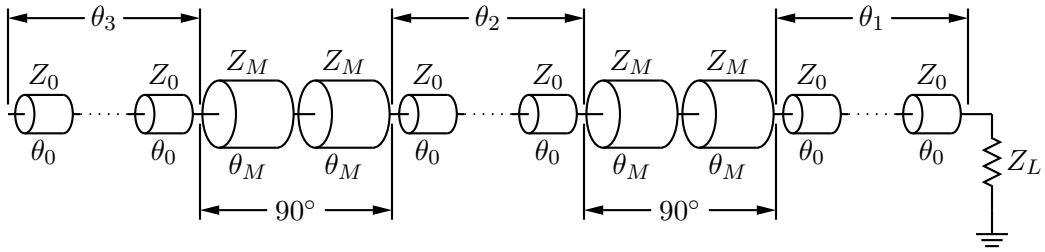
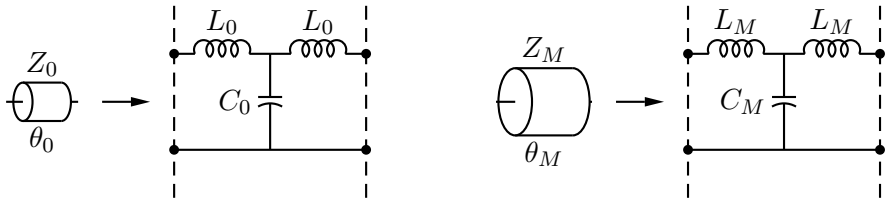


Figure 3.13: Sections of Z_0 and Z_M transmission line separated into segments of length θ_0 and θ_M respectively. A variable element is required to change the characteristic impedance from Z_0 to Z_M such that the slug sections (Z_M) can move in steps of θ_0.

Each section of transmission line is represented by an equivalent circuit of inductors and capacitors. For the purposes of symmetry, a T-network is used, as shown in Figure 3.14.

Both networks shown in Figure 3.14 can be modeled as cascaded matrices. A transmission line segment of impedance Z and length θ is described by

$$[A]_{tline} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ\sin\theta \\ j1/Z\sin\theta & \cos\theta \end{bmatrix} \tag{3.11}$$



(a) Z_0 section (b) Z_M section

Figure 3.14: An equivalent circuit representation of a Z_0 (a) and Z_M (b) transmission line segments.

and the T-equivalent circuit segment is modeled as

$$[A]_{EC} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ jB_C & 1 \end{bmatrix} \begin{bmatrix} 1 & jX_L \\ 0 & 1 \end{bmatrix}$$
$$= \begin{bmatrix} 1 - X_L B_C & jX_L(2 - X_L B_C) \\ jB_C & 1 - X_L B_C \end{bmatrix} \tag{3.12}$$

Equating like parts, the following results:

$$B_C = \frac{1}{Z \sin\theta},$$
$$\text{therefore } C = \frac{\sin\theta}{\omega Z}, \tag{3.13}$$
$$\text{and } X_L = \frac{Z(1 - \cos\theta)}{\sin\theta},$$
$$\text{therefore } L = \frac{Z(1 - \cos\theta)}{\omega \sin\theta}. \tag{3.14}$$

Minimizing the number of MEMS switches required in the reconfigurable circuit requires minimizing or eliminating any switches in series with the inductors or capacitors. By constraining $L = L_0 = L_M$ of the inductor, and using a parallel combination of capacitors C_0 and C_1 to equal C_M, only one switching device is required in each transmission-line segment. Since one state occurs when the switch is in the open position, this state has much lower loss than the closed-position state. Such a configuration is highly desirable in a double-slug tuner, since in the "all zero" state, where all switches are open, the tuner becomes a low-loss 50-Ω line that contributes minimally to the rest

of the system. A schematic of this reconfigurable segment is shown in Figure 3.15.

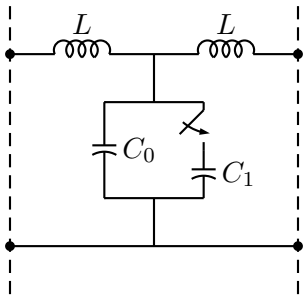


Figure 3.15: A reconfigurable transmission line segment. The inductor L is constrained such that $L = L_0 = L_M$. The parallel combination of C_0 and C_1 is equivalent to C_M.

Constraining the two states to have the same inductance leads to a reduction in the degrees of freedom in the double slug implementation. The ideal double-slug solution has four degrees of freedom, namely, the two impedances Z_0 and Z_M and the two electrical lengths θ_0 and θ_M. By constraining L, Z_M becomes dependent on Z_0 and θ_0. Further constraints on the network are that $Z_0 = 50\,\Omega$ in the open state, and that θ_M be an integer factor of 90° such that an integer number of switches close to create the Z_M section. The θ_0 sections do not necessarily need to be an integer multiple of 180°, since the 0 and 180° solutions of θ_1 and θ_2 are redundant. With these constraints, the section design may be divided into the following steps:

(1) Choose θ_0.

(2) Determine C_0 and L by

$$C_0 = \frac{\sin\theta_0}{\omega Z_0} \tag{3.15}$$

$$\text{and } L = \frac{Z_0(1-\cos\theta_0)}{\omega \sin\theta_0}. \tag{3.16}$$

(3) Choose θ_M as an integer factor of 90°.

(4) Determine C_M and Z_M by

$$C_M = \frac{1 - \cos\theta_M}{\omega^2 L} \tag{3.17}$$

$$\text{and } Z_M = \frac{\omega L \sin\theta_M}{1 - \cos\theta_M} \tag{3.18}$$

Once Z_M is known, it is possible to calculate $|\Gamma|_{max}$ from Eq. 3.10.

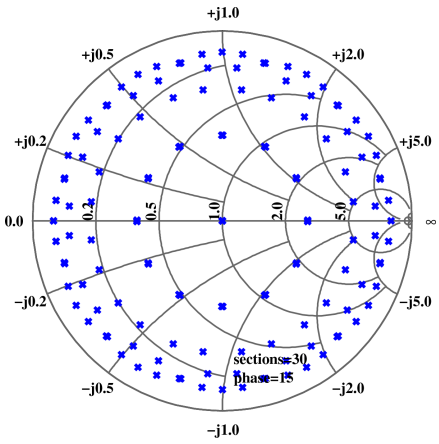
Z_M is now linked to the choice of θ_0 and θ_M, and only certain constellations are possible, shown in Figures 3.16 and 3.17. In each figure, the phase of Z_M (θ_M) is set to 30° in Figure 3.16 and 45° in Figure 3.17. The phase of Z_0 (θ_0) is then varied from 15° to 26° in 1° steps.

In the ideal tuner, there is infinite control over the phase of θ_1 and θ_2, and the tuner can create all impedances within the $|\Gamma|_{max}$ circle. However, since this electronic implementation is limited to discrete steps in phase, a constellation of impedance points is formed. What cannot be determined by the formulas is how the constellation points are distributed.

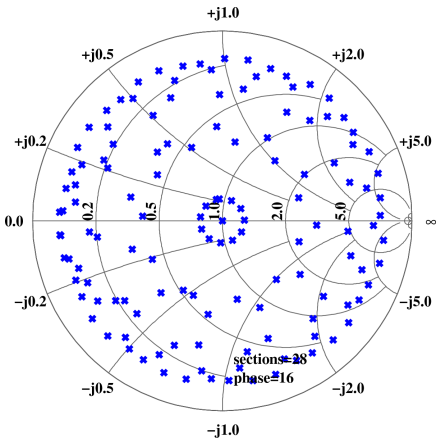
Figure 3.16 shows possible constellations when $\theta_M = 30°$. This would require 3 switches to be in the closed position in order to create the 90° section at 10 GHz.

In Figure 3.16 (a), there are very few points in the central region of the Smith chart, with most of the constellation lying on the perimeter of the chart. Figure 3.16 (a) also shows that several points are redundant. Depending on the application, this redundancy may be desired in order to make the circuit robust; however, from a minimization perspective, the redundancy is undesirable. It is equally undesirable to have points in close proximity to each other, as in Figure 3.16 (f) or (i).

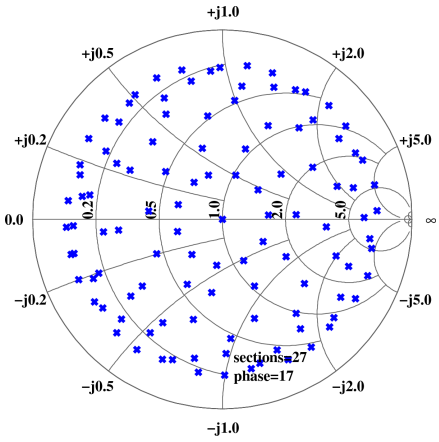
Another factor to consider is that in the implementation of these inductances and capacitances, it becomes increasingly difficult to optimize the reconfigurable circuit simultaneously as the two impedance states (and phases) become increasingly separated. The exact values of inductance and capacitance calculated from (3.15), (3.16), and (3.17) are shown in Table 3.1, along with the slug impedance calculated from (3.18) and the



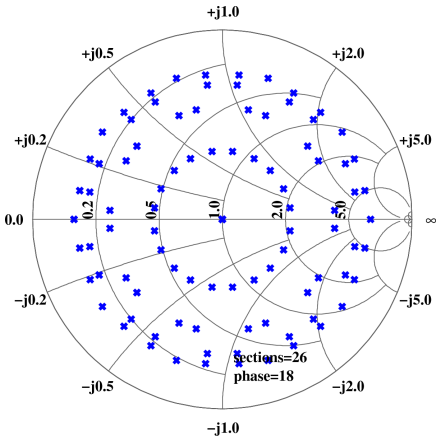
(a) θ_0=15°, Z_M=24.5 Ω, $|\Gamma|_{max}$=0.88, required devices=30



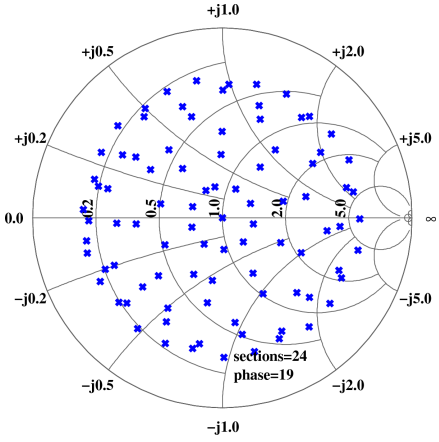
(b) θ_0=16°, Z_M=26.2 Ω, $|\Gamma|_{max}$=0.86, required devices=28



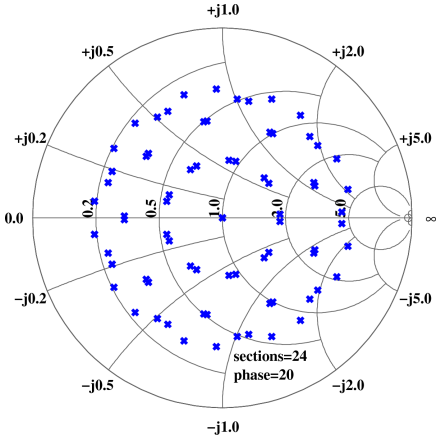
(c) θ_0=17°, Z_M=27.9 Ω, $|\Gamma|_{max}$=0.82, required devices=27



(d) θ_0=18°, Z_M=29.6 Ω, $|\Gamma|_{max}$=0.78, required devices=26

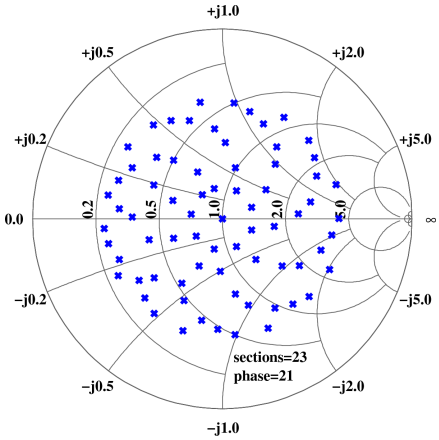


(e) θ_0=19°, Z_M=31.2 Ω, $|\Gamma|_{max}$=0.74, required devices=24

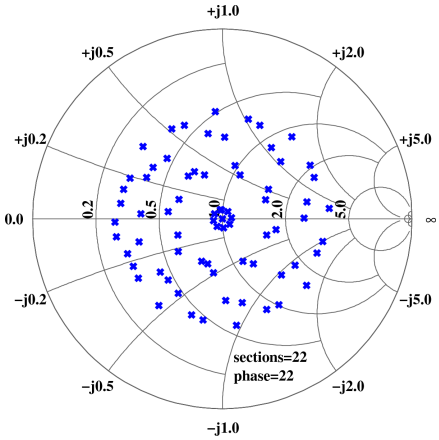


(f) θ_0=20°, Z_M=32.9 Ω, $|\Gamma|_{max}$=0.68, required devices=24

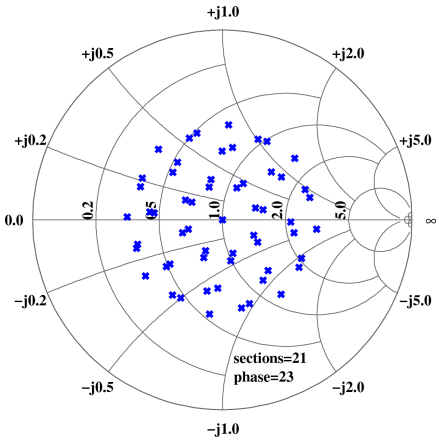
Figure 3.16: Possible 10-GHz tuner constellations, θ_M=30° for θ_0=15–20°.



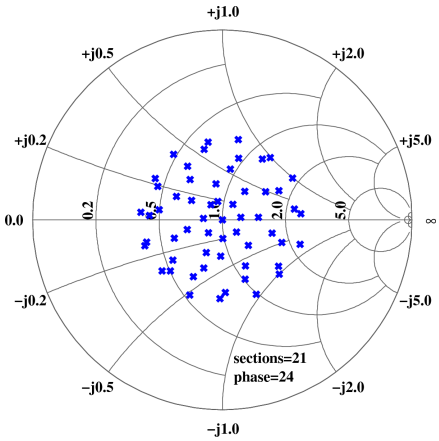
(g) θ_0=21°, Z_M=34.6 Ω, $|\Gamma|_{max}$=0.63, required devices=23



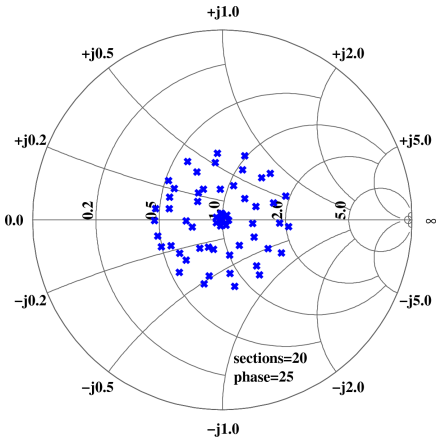
(h) θ_0=22°, Z_M=36.3 Ω, $|\Gamma|_{max}$=0.57, required devices=22



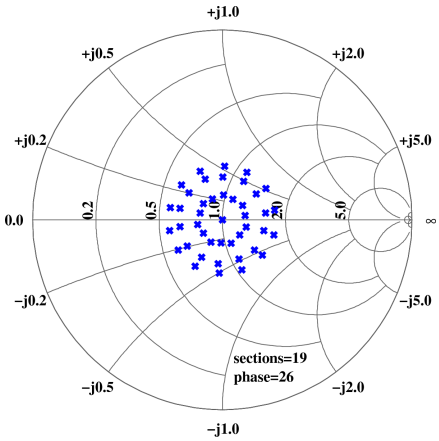
(i) θ_0=23°, Z_M=37.9 Ω, $|\Gamma|_{max}$=0.50, required devices=21



(j) θ_0=24°, Z_M=39.7 Ω, $|\Gamma|_{max}$=0.43, required devices=21



(k) θ_0=25°, Z_M=41.4 Ω, $|\Gamma|_{max}$=0.36, required devices=20



(l) θ_0=26°, Z_M=43.1 Ω, $|\Gamma|_{max}$=0.29, required devices=19

Figure 3.16: Possible 10-GHz tuner constellations, θ_M=30° for θ_0=21–26°. (cont.)

maximum Γ calculated from (3.10). Thus, for the case of $\theta_M = 30°$, Figure 3.16 (g) represents the best compromise. The points in the constellation are separated, the impedance of $34.6\,\Omega$ is close enough to $50\,\Omega$ and phase of 21° is close enough to 30° to allow simultaneous optimization of the reconfigurable element (Section 3.4 contains the details of this process), while maintaining a reasonably large coverage area of $|\Gamma|_{max} = 0.63$ (a 4:1 SWR).

As θ_0 approaches θ_M, the constellation reduces to a single point where $\theta_0 = \theta_M$. This trend is evident in Figure 3.16.

Similarly, Figure 3.17 shows the possible constellations when $\theta_M = 45°$, requiring only 2 switches in the closed position to create the 90° section. The exact inductance and capacitance values are shown in Table 3.1.

Figure 3.17 (a) is even more exaggerated than Figure 3.16 (a) in having no points in the central region of the Smith chart and all concentrated around the perimeter. Again, there are solutions which place impedance points in close proximity, such as Figure 3.17 (f) and (l). Figure 3.17 (g) or (j) produce the best compromises in impedance, phase, constellation density, and coverage area and would be suitable for applications requiring high VSWR coverage, though the large separation between the C_0 and C_M values shown in Table 3.1 would make implementation more difficult.

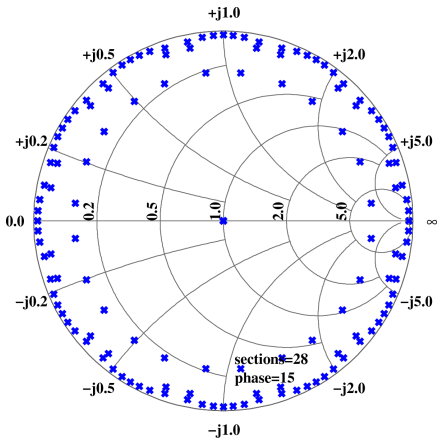
For the purposes of this work, Figure 3.16 (g) is selected as the target constellation, providing a balance between all parameters of interest. Section 3.4 details the implementation of the reconfigurable transmission line section to produce this constellation. In principle, the same design methodology may be followed to produce a tuner with a constellation from Figure 3.17 (g) or (i).

3.4 Implementation of the Reconfigurable Line Section

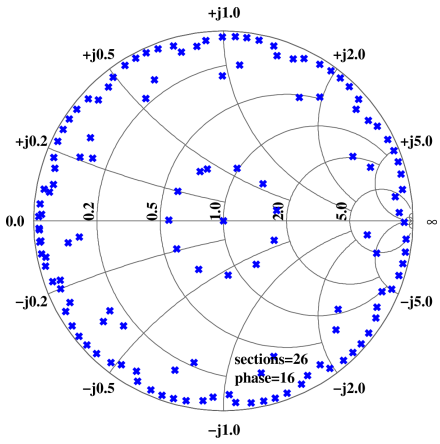
Implementing the constellation in Section 3.4 (g) requires loading the transmission line with the necessary inductance and capacitance. These elements are first considered

Table 3.1: Capacitance and Inductance Values for $\theta_M = 30°$ and $\theta_M = 45°$

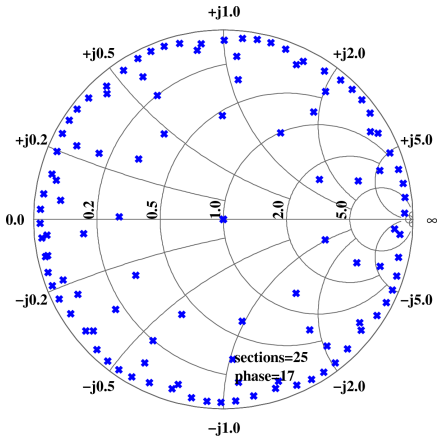
θ_0	C_0 (fF)	L (pH)	$C_{M,30°}$ (fF)	$Z_{M,30°}$ (Ω)	$\lvert\Gamma\rvert_{max,30°}$	$C_{M,45°}$ (fF)	$Z_{M,45°}$ (Ω)	$\lvert\Gamma\rvert_{max,45°}$
15°	82.4	104.8	323.9	24.5	0.88	708.2	15.9	0.98
16°	87.7	111.8	303.4	26.2	0.86	663.4	17.0	0.97
17°	93.0	118.9	285.3	27.9	0.82	623.8	18.0	0.97
18°	98.4	186.0	269.3	29.6	0.78	588.6	19.1	0.96
19°	103.6	133.2	254.8	31.2	0.74	557.1	20.2	0.95
20°	108.8	140.3	241.9	32.9	0.68	528.7	21.3	0.94
21°	114.1	147.5	230.1	34.6	0.63	503.0	22.4	0.92
22°	119.2	154.7	219.4	36.3	0.57	479.6	23.5	0.91
23°	124.4	161.9	209.6	37.9	0.50	458.3	24.6	0.89
24°	129.5	169.1	200.6	39.7	0.43	438.6	25.7	0.87
25°	134.5	176.4	192.4	41.4	0.36	420.5	26.8	0.85
26°	139.5	183.7	184.7	43.1	0.29	403.8	27.9	0.82



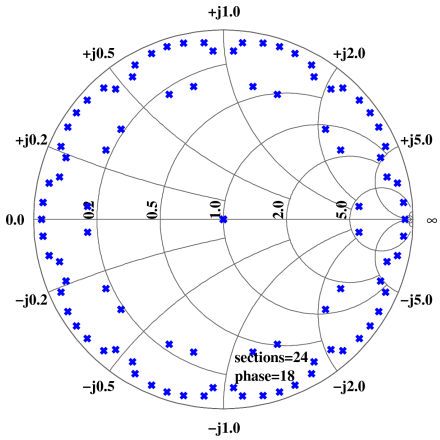
(a) θ_0=15°, Z_M=15.9 Ω, $|\Gamma|_{max}$=0.98, required devices=28



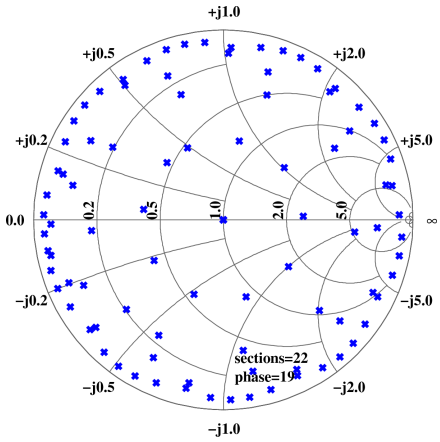
(b) θ_0=16°, Z_M=17.0 Ω, $|\Gamma|_{max}$=0.97, required devices=26



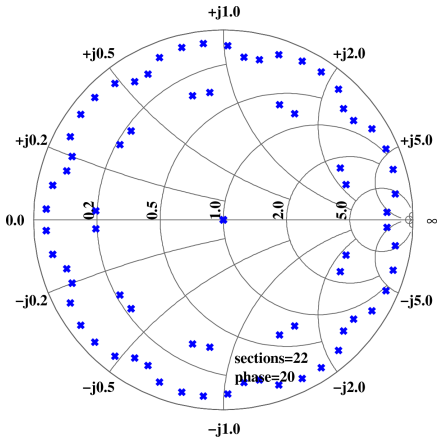
(c) θ_0=17°, Z_M=18.0 Ω, $|\Gamma|_{max}$=0.97, required devices=25



(d) θ_0=18°, Z_M=19.1 Ω, $|\Gamma|_{max}$=0.96, required devices=24

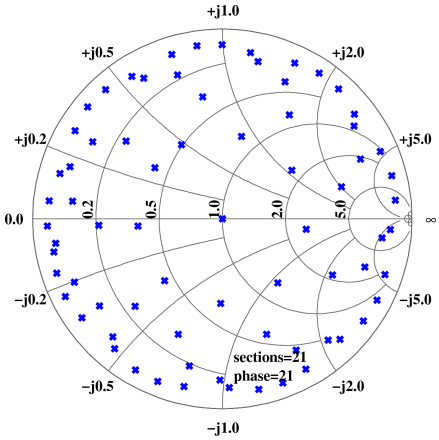


(e) θ_0=19°, Z_M=20.2 Ω, $|\Gamma|_{max}$=0.95, required devices=22

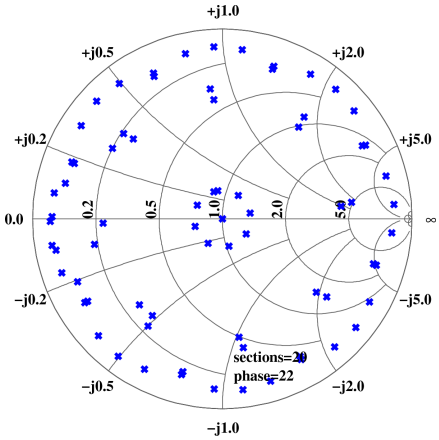


(f) θ_0=20°, Z_M=21.3 Ω, $|\Gamma|_{max}$=0.94, required devices=22

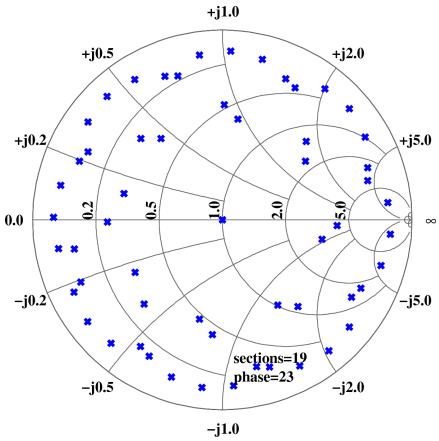
Figure 3.17: Possible 10-GHz tuner constellations, θ_M=45° for θ_0=15–20°.



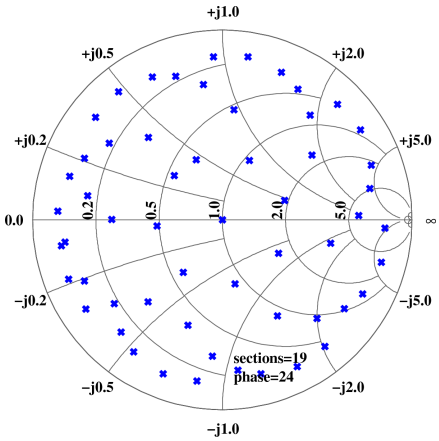
(g) θ_0=21°, Z_M=22.4 Ω, $|\Gamma|_{max}$=0.92, required devices=21



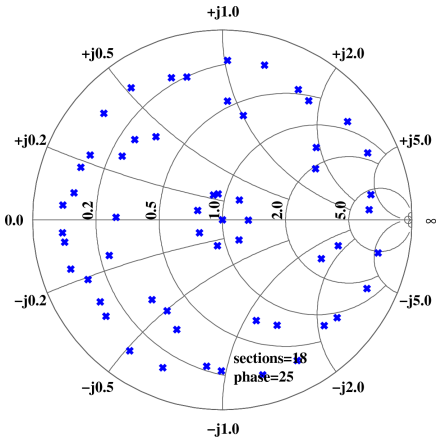
(h) θ_0=22°, Z_M=23.5 Ω, $|\Gamma|_{max}$=0.91, required devices=20



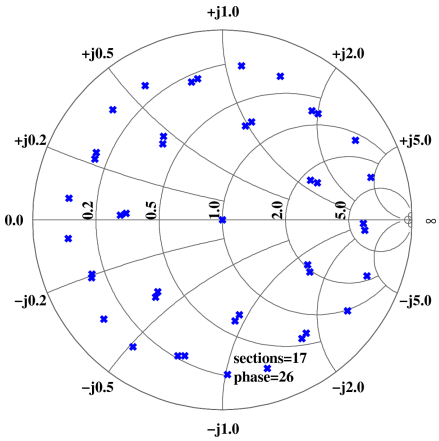
(i) θ_0=23°, Z_M = 24.6 Ω, $|\Gamma|_{max}$=0.89, required devices=19



(j) θ_0=24°, Z_M=25.7 Ω, $|\Gamma|_{max}$=0.87, required devices=19



(k) θ_0=25°, Z_M=26.8 Ω, $|\Gamma|_{max}$=0.85, required devices=18



(l) θ_0=26°, Z_M=27.9 Ω, $|\Gamma|_{max}$=0.82, required devices=17

Figure 3.17: Possible 10-GHz tuner constellations, θ_M=45° for θ_0=21–26°. (cont.)

independently, then combined and optimized to produce a "unit cell" with impedance Z_0 and phase θ_0 in the open state, and impedance Z_M and phase θ_M in the closed state.

3.4.1 Design of the Loading Capacitor

A transmission line may be loaded with a shunt capacitance by: a lumped capacitor, a subquarter-wavelength open stub, a radial stub, or an interdigital capacitor. Surface mount capacitors are far too large at 10 GHz to be suitable, and monolithic capacitors such as metal-insulator-metal (MIM) or metal-air-metal (MAM) capacitors are untested in the current fabrication process, and so use of a lumped capacitor is unsuitable.

Of the remaining options, a 100 fF capacitor is designed as a test case on 254-μm thick alumina (Al_2O_3, $\epsilon_r = 9.8$). An open shunt stub 100 μm in width must be approximately 755 μm in length. A radial stub of equal width at the junction with the transmission line must be 345 μm in length for a 70° angle. Both solutions show good agreement with an ideal shunt capacitance up to 15 GHz. Both of the solutions, however, present a high potential for coupling between the elements, since the tuner will require 22 sections placed in close proximity.

By comparison, a 100-pF interdigital capacitor with 3 pairs of fingers, 20 μm finger widths and 22 μm gaps must be 250 μm in length. Smaller gap widths allow the capacitor to be further reduced in size. The element has good agreement with an ideal shunt capacitance up to 20 GHz. Since this element is very compact, it will be the most suitable for this particular application.

Figure 3.18, from the Agilent ADS documentation [61], shows the design parameters of an interdigital capacitor. W is the width of the fingers, G is the gap space between the fingers, G_e is the gap space at the ends of the fingers, L is the length of the fingers, W_t is the width of the finger interconnect, and W_f is the width of the connecting feed line. Additionally, the number of finger pairs, N_p, is required.

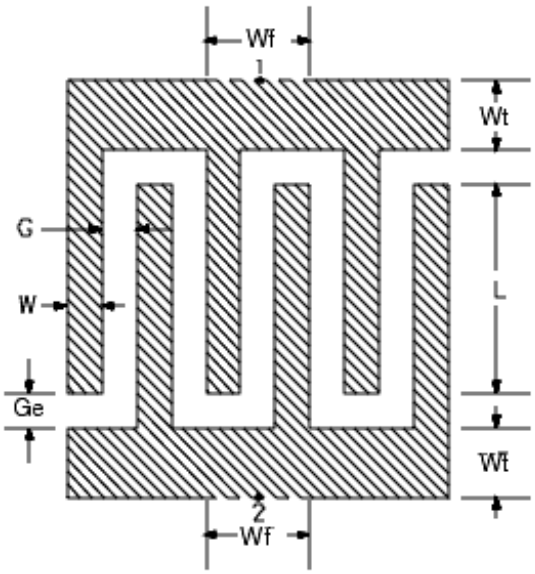


Figure 3.18: Specifications for an interdigital capacitor in Agilent ADS from [61]. G is the gap spacing, W is the finger width, G_e is the end gap spacing, L is the length of the fingers, W_t is the width of the interconnect, and W_f is the width of the connecting feed line. Additionally N_p, the number of finger pairs, must be specified.

The interdigital capacitor has an equivalent circuit as shown in Figure 3.19. The "intended" capacitance is labeled C_i, and the other elements are parasitic. The series parasitic elements due to the capacitor are L_{Cs} and R_{Cs}, and the shunt elements are C_{Cp}. To first order, the capacitance C_i may be estimated based on the geometry of the capacitor (W, G, and L in microns) [62]:

$$C_i(\text{pF}) = \frac{\epsilon_{re}10^{-3}}{18\pi}\frac{K(k)}{K'(k)}(2N_p - 1)L \tag{3.19}$$

where

$$k = \tan^2\left(\frac{a\pi}{4b}\right), a = \frac{W}{2}, b = \frac{W+G}{2},$$

and

$$\frac{K(k)}{K'(k)} = \begin{cases} \frac{1}{\pi}\ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right), & \text{for } 0.707 \leq k \leq 1; \\ \frac{\pi}{\ln\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)}, & \text{for } 0 \leq k \leq 0.707; \end{cases}$$

$$k' = \sqrt{1-k^2}.$$

However, accurate determination (and reduction) of the parasitic elements is not straightforward. Equations for the parasitic elements may be found in [61], but it is left to an optimization routine, discussed in Section 3.5, to determine the final geometry which best fits the design specifications.

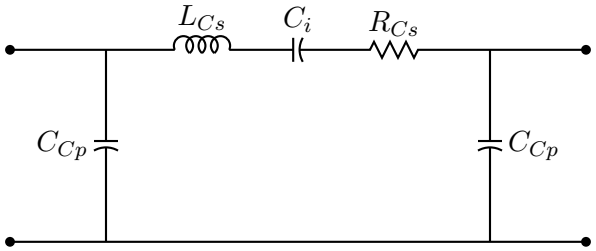


Figure 3.19: Equivalent circuit for an interdigital capacitor.

3.4.2 Design of the Loading Inductor

A series inductance in a transmission line may be created by a thin "strip" inductor, or a thin loop inductor [62]. Since loss is a primary concern in these circuits, long sections of thin line are undesirable.

Instead, a transverse notch in the microstrip line is used to create a small inductance. Figure 3.20 shows a notch as specified in Agilent ADS [61]. W is the width of the microstrip line containing the notch, L is the length of the notch, and D is the depth of the notch into the line.

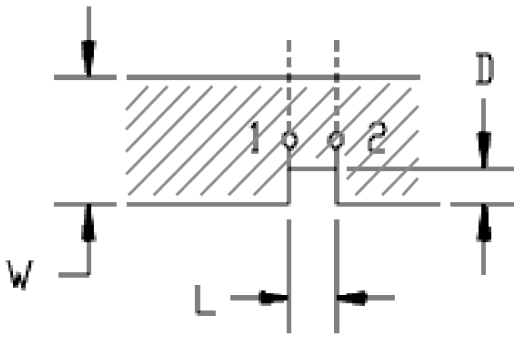


Figure 3.20: Specifications for a microstrip notch in Agilent ADS from [61]. W is the width of the microstrip line, D is the depth of the notch, and L is the length of the notch.

Figure 3.21 shows an equivalent circuit for the notch inductor, where L_i is the "intended" inductance, C_{Ls} is the series parasitic capacitance, and C_{Lp} are the shunt parasitic capacitances. The "intended" inductance L_i can be estimated to first order by [62]:

$$L_i \text{ (nH)} = \frac{\mu_0 \pi h}{2} \left(1 - \frac{Z_0}{Z_0'} \sqrt{\frac{\epsilon_{re}}{\epsilon_{re}'}}\right)^2, \tag{3.20}$$

where h is the thickness of the substrate in millimeters, Z_0 and ϵ_{re} are the characteristic impedance and the effective relative dielectric constant of the microstrip line of width W, and Z_0' and ϵ_{re}' are the impedance and dielectric constant of a microstrip line of width $W - D$.

As in the case of the interdigital capacitor, equations exist in [61] to determine the parasitic elements in Figure 3.21, however an optimization routine is used to best fit the geometry to the electrical specifications, which Section 3.5 discusses in detail.

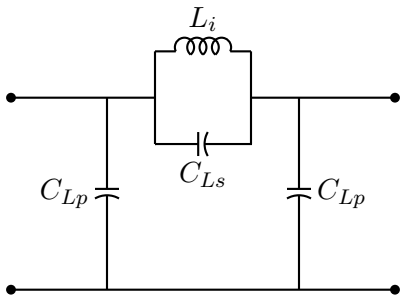


Figure 3.21: Equivalent circuit for a microstrip notch.

3.4.3 Combination into a "Unit Cell"

The capacitor and inductor elements from the previous sections are combined into what will be the "unit cell" of the reconfigurable transmission line, such that in the different states, the cell will have the configurations from Figure 3.14. Ideally, the unit cell would have the configuration shown in Figure 3.22, where L_i and C_i are the intended inductance and capacitance of the cell components (from Figure 3.14(a) or (b)), void of any parasitic components.

In actuality, the microstrip interdigital and notch components have parasitic reactances and losses, shown in Figures 3.19 and 3.21, which makes the actual equivalent circuit closer to the one shown in Figure 3.23. The physical dimensions of the notch and interdigital components are varied through optimization routines such that the full equivalent circuit in Figure 3.23 most closely matches the ideal circuit in Figure 3.22.

The unit cell must also switch between the two impedance states of Figure 3.14 in the manner shown in Figure 3.15. This means inclusion of the MEMS switch into the unit cell, which has additional parasitic components (namely capacitance in the open state and resistance and a small electrical length in the closed state). The equivalent

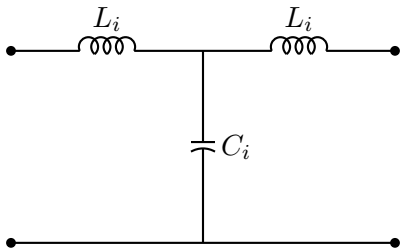


Figure 3.22: Ideal equivalent circuit for the transmission line section.

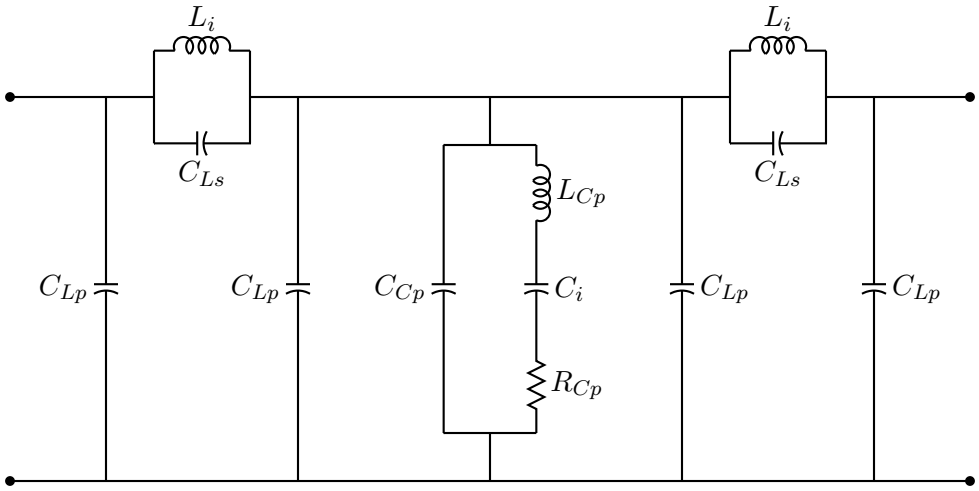


Figure 3.23: Full equivalent circuit for the transmission line section, including parasitic elements.

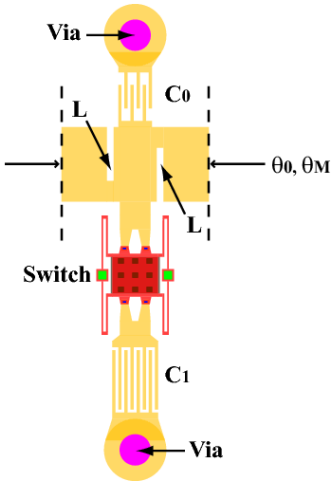
circuit model of the switch is detailed in Section 1.3.1 and shown in Figures 1.5 and 1.6.

An additional constraint on the unit cell is that the MEMS devices cannot be arbitrarily close to one another. Each device includes flexures, anchors, and a resistive network to provide the actuation bias, as shown in Figure 1.4. Without any change to the bias network design, the switches may be no closer on the same side of the transmission line than approximately 500 μm (measured as the distance between the junction edges). Redesigning the bias network could potentially allow the switches to be as close as 200 μm on the same side of the transmission line. If the switches are staggered along the transmission line, the distance between the cell junction edges reduces to 200 μm for no change in the bias network (since the transmission line joining each cell is 100 μm in length on either size of the switch). With a redesigned, staggered bias network, the switches could possibly be as close as 50 μm.

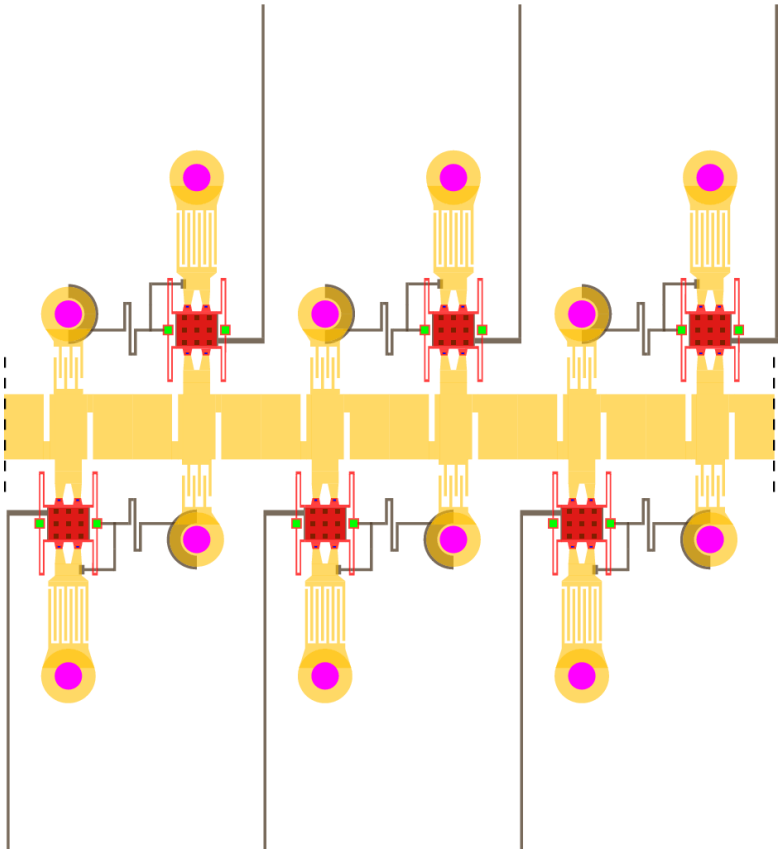
With the inclusion of 100 μm diameter plated vias along the line (surrounded by a 200 μm diameter microstrip pad, shown in Figure 3.24(a)) and to minimize coupling between the cells, the switches are staggered along the line with the junctions separated by 360 μm, shown in Figure 3.24(b). This allows 300 μm of separation between each switch and the nearest via, and 810 μm of separation between adjacent switches on the same side of the transmission line. Note, these values were chosen subjectively, based on ease of fabrication (particularly the release step) and of a suitable separation to reduce coupling while minimizing the overall circuit size. Since the circuit is a loaded transmission line with a phase of 21°, the length of an unloaded, straight section of line of equal length to the unit cell must be much less than 21°.

3.5 Optimization of the Unit Cell

Figure 3.25 shows the schematic in Agilent ADS used to optimize the unit cell. Since the desired unit cell is in a configuration shown in Figure 3.15, the optimization occurs in two steps:



(a) Unit Cell



(b) 6 Staggered Cells

Figure 3.24: The unit cell layout (a) with each component labeled according to the corresponding component in Figure 3.15. Each unit cell is staggered (b) such that the switches and larger capacitors are separated sufficient distance for fabrication and reduction of coupling.

(1) The physical dimensions of the notch and interdigital components which produce the common inductance and capacitance C_0 are optimized with the switch in the open position.

(2) The optimization parameters from step (1) are disabled, and the physical dimensions of the interdigital capacitor which produces capacitance C_1 are optimized with the switch in the closed position.

Since the two states of the MEMS switch have different equivalent circuit models, a nested approach is used whereby the models for the open and closed state are inserted into the unit cell schematic as two separate blocks. These blocks are selected using an ADS component known as a "path selector", shown in the lower branch of Figure 3.25, which uses a state variable to determine the path. This component provides an ideal "thru" connection, perfect isolation, no phase change and no loss.

3.5.1 First Optimization Step

The unit cell is symmetric about the center cross element, since the left and right inductances are equal. This inductance is produced by the notch element located between two transmission line elements. The position of the notch is allowed to vary by varying the lengths of the two transmission lines, such that their total length sums to a constant. The notch has two parameters that are allowed to vary: its length L and its depth D, according to Figure 3.20.

The upper branch of the circuit contains the interdigital capacitor that will create C_0 from Figure 3.15. Since this capacitance is small, the number of finger pairs N_p is set to 3. The gap width G and finger width W from Figure 3.18 are fixed to $10\,\mu$m, which approaches the limit of the fabrication capabilities without significantly affecting the yield. The width of the interconnect, W_i, and the width of the feed line, W_f, are fixed to $100\,\mu$m and $20\,\mu$m respectively. The gap at the end of the finger, G_e, and the

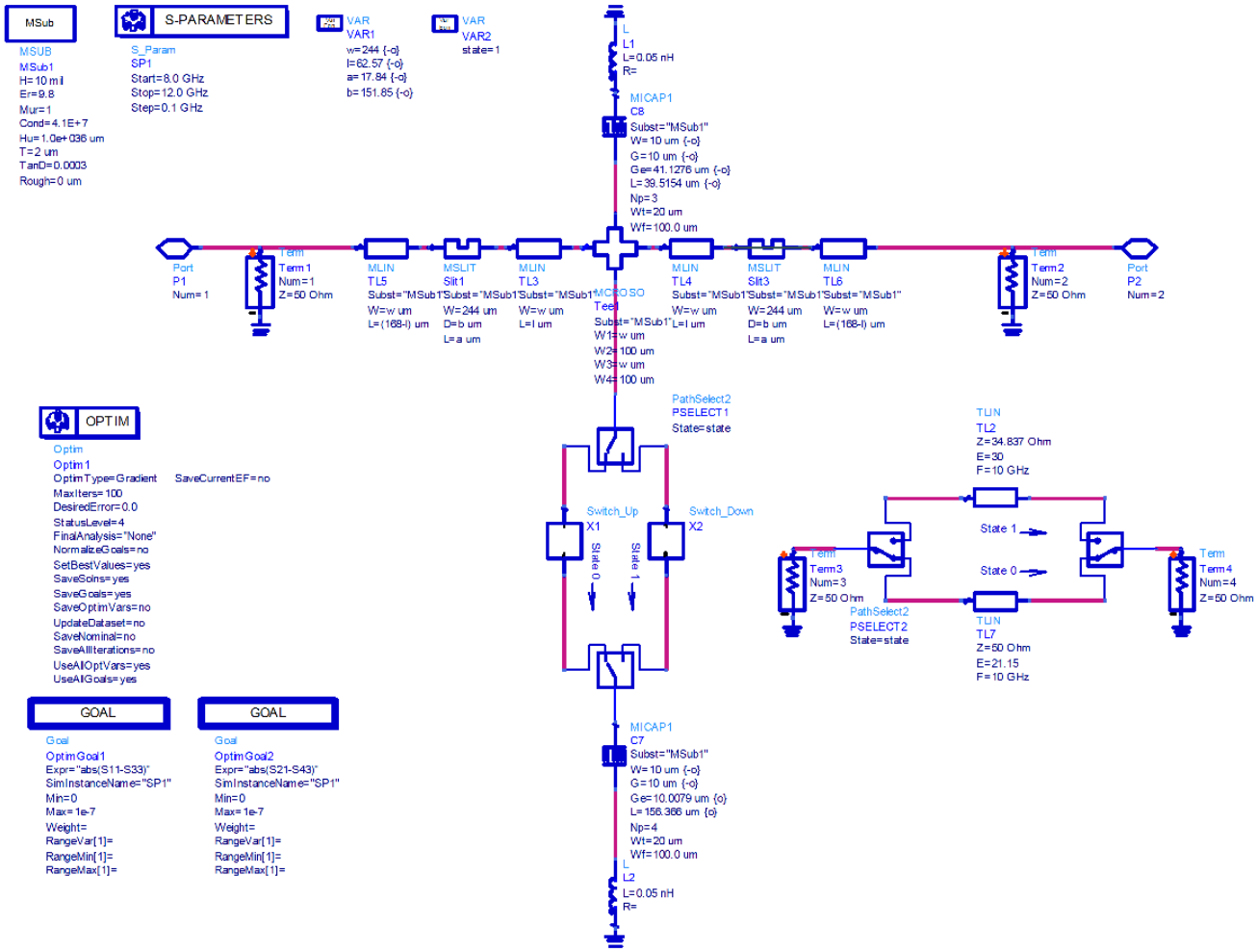


Figure 3.25: A schematic of the unit cell used for optimization of the physical dimensions of the notches and interdigital capacitors.

finger length, L, are allowed to vary. The capacitor is connected to ground through a series inductance of 0.05 nH, which is the inductance of the 100 μm diameter via.

The path selector is set to use the open state equivalent circuit model for the switch.

These values are optimized with two goals:

(1) Minimizing the magnitude of the difference between S_{11} in the unit cell and an ideal transmission line of impedance Z_0 and phase θ_0, and

(2) minimizing the magnitude of the difference between S_{21} in the unit cell and the ideal transmission line.

Optimization is first run using the "random" optimization type to reduce the two goals to within 10^{-3}. This ensures that the optimizer locates a global minimum over the entire search space. The optimization is then performed again using a gradient method to reduce the two goals to within 10^{-7}. The frequency range of optimization is set from 8–12 GHz, covering X-band.

3.5.2 Second Optimization Step

In the second optimization step, all values optimized in step (1) are disabled. The path selector is set to use the closed-state equivalent circuit model.

The lower branch of the circuit contains the interdigital capacitor that will create C_1 from Figure 3.15. Since this capacitance is larger than C_0, the number of finger pairs, N_p, is set to 4. The gap width, G, and finger width W from Figure 3.18 are fixed to 10 μm, which approaches the limit of the fabrication capabilities without significantly affecting the yield. The width of the interconnect, W_i, and the width of the feed line, W_f, are fixed to 100 μm and 20 μm respectively. The gap at the end of the finger, G_e, and the finger length, L, are allowed to vary. The capacitor is connected to ground

through a series inductance of 0.05 nH, which is the inductance of the 100 μm diameter via.

These values are optimized with two goals, similar to step (1):

(1) Minimizing the magnitude of the difference between S_{11} in the unit cell and an ideal transmission line of impedance Z_M and phase θ_M, and

(2) minimizing the magnitude of the difference between S_{21} in the unit cell and the ideal transmission line.

Again, optimization is first run using the "random" optimization type to reduce the two goals to within 10^{-3}, then run again using a gradient method to reduce the two goals to within 10^{-7}.

3.5.3 Full-Circuit Verification

Once optimization is complete, the unit cells are cascaded and nested into a larger circuit, which contains all 22 switches, shown in Figure 3.26.

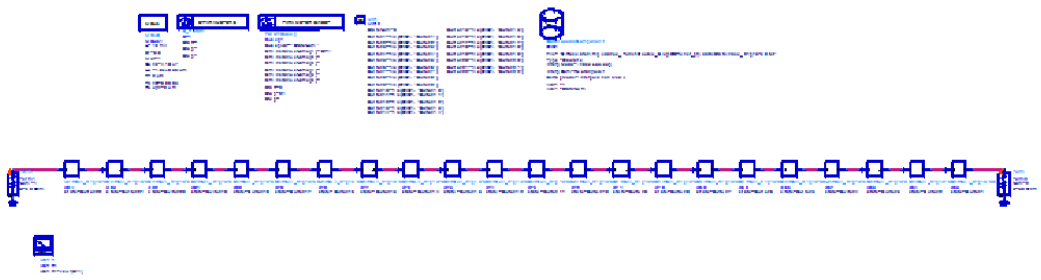


Figure 3.26: Unit cells are nested in a larger simulation of the full 22-switch circuit to determine the impedance constellation and loss. Each box contains the circuit shown in Figure 3.25, i.e. one reconfigurable line section.

The state of each unit cell's path selector is passed as a variable from the top level circuit into each cell. This state is determined from a data access component (DAC), which contains arrays of ones and zeros representing whether the unit cell switch is in the closed or open respectively. The columns of the array represent the value of

a particular switch. Each array represents one impedance point on the 10 GHz Smith Chart, referred to as one "state" of the tuner. These arrays are indexed. The parameter sweep component in ADS steps through all the indices required to create double slug operation centered at 10 GHz. Since three closed switches are necessary to create a 90° section with impedance Z_M, shown in Figures 3.12 and 3.13. The two groups of three ones in Table 3.2 represent the slugs.

The slugs start adjacent to each other (state j), creating a 180° section and an impedance point at 50 Ω on the Smith Chart. The slugs are then separated one cell length at a time (θ_0 from Figure 3.13) in states j+1 through j+7. The total separation distance is θ_2 from Figures 3.12 and 3.13. Table 3.2 does not show the complete state matrix, only a subset for one cycle of the slugs (i.e. once the slugs are separated by at least 180°, the impedance pattern repeats itself). The matrix shown in Table 3.2 is followed by zeros beyond switch S_{i+12}, which represent θ_1 from Figures 3.12 and 3.13. The complete tuner has sufficient switches such that θ_1 can vary from 0–180°. The matrix is also preceded by zeros for all switches before S_i, which represent θ_3 from Figures 3.12 and 3.13.

An s-parameter simulation is performed to verify the complete circuit. Figure 3.27 shows a comparison between the ideal 10-GHz constellation from Figure 3.16(g) as calculated in MATLAB and the constellation calculated in ADS. The ideal impedance points are indicated by the blue x symbols, and the model points are indicated by the red o symbols. While it is impossible to match the ideal constellation perfectly once parasitics, losses, and physical limitations are included in the ADS model, the constellations nonetheless have good agreement in range and distribution of points.

The ADS simulation allows a first estimate of the insertion loss of the tuner, based on the physical models of the components. Figure 3.28 shows the insertion loss as it depends on the state of the tuner (i.e. the loss at each impedance point). The symbols indicate the loss at each discrete state of the tuner. The special "0" state is not

Table 3.2: State Matrix

State		S_i	S_{i+1}	S_{i+2}	S_{i+3}	S_{i+4}	S_{i+5}	S_{i+6}	S_{i+7}	S_{i+8}	S_{i+9}	S_{i+10}	S_{i+11}	S_{i+12}	
j	...	0	0	0	0	0	0	0	1	1	1	1	1	1	...
$j+1$	...	0	0	0	0	0	0	1	1	1	0	1	1	1	...
$j+2$	...	0	0	0	0	0	1	1	1	0	0	1	1	1	...
$j+3$	...	0	0	0	0	1	1	1	0	0	0	1	1	1	...
$j+4$	...	0	0	0	1	1	1	0	0	0	0	1	1	1	...
$j+5$	...	0	0	1	1	1	0	0	0	0	0	1	1	1	...
$j+6$	...	0	1	1	1	0	0	0	0	0	0	1	1	1	...
$j+7$	...	1	1	1	0	0	0	0	0	0	0	1	1	1	...

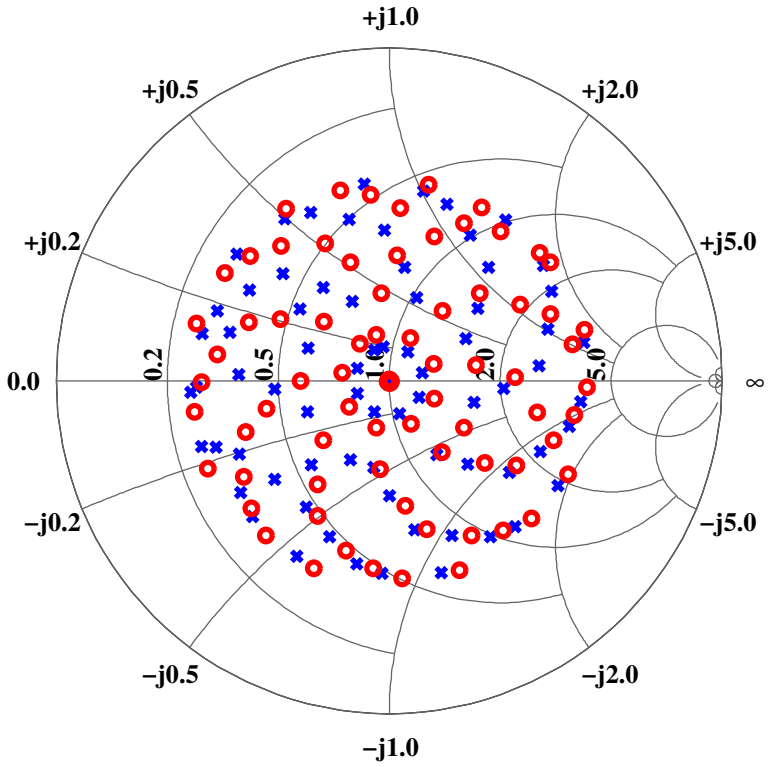


Figure 3.27: A comparison of the 10-GHz ideal tuner constellation (blue x) with the full circuit simulation from ADS (red o), which includes losses. The constellations are similar in range and distribution.

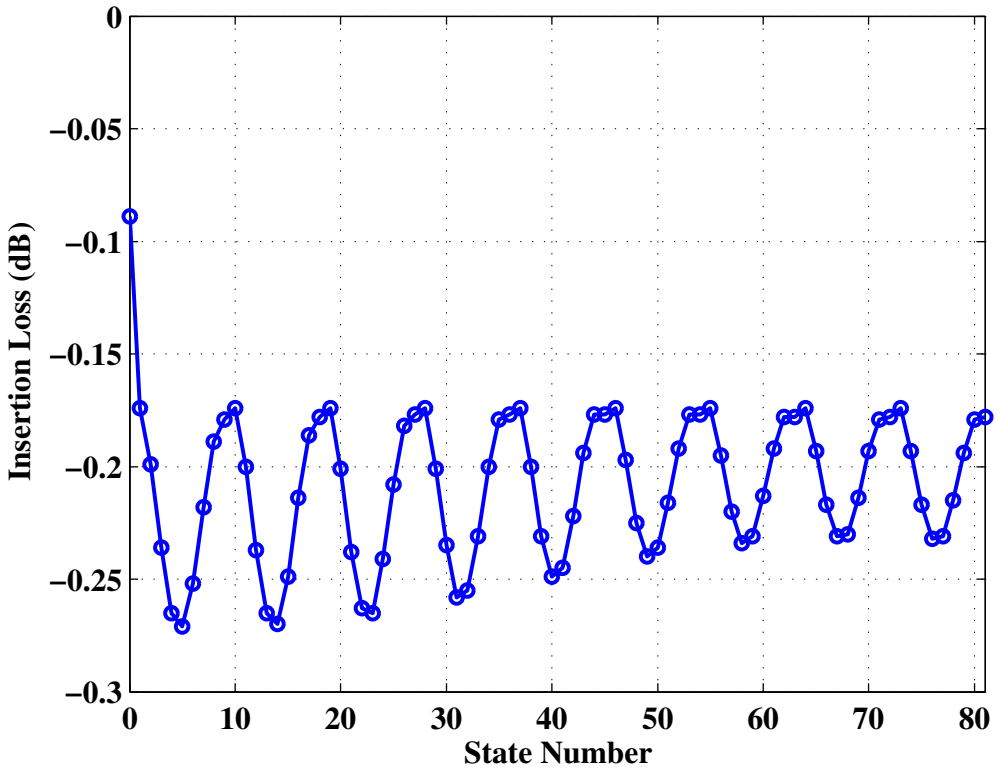


Figure 3.28: Simulated insertion loss in each state of the tuner. The "0" state is when all switches are open and has an insertion loss of 0.08dB. The other states have losses ranging from 0.17–0.27 dB.

part of the normal double slug configuration, and is when all switches are in the open position. In this position, the circuit is in its lowest loss configuration and becomes a 50 Ω line approximately 1.3λ in length at 10 GHz. This state effectively turns off the tuner entirely and has an insertion loss of 0.08 dB. This loss is higher than a microstrip line of equal length, but much less than any other 50 Ω state of the tuner.

The other states of the tuner have insertion losses ranging from 0.17 dB to 0.27 dB as the impedance position ranges from lowest VSWR (50 Ω) to highest VSWR (approximately 4:1) respectively.

3.5.4 Full-Wave Verification

Since the full circuit is densely packed, the last verification step is a full-wave method-of-moments analysis (Ansoft Designer) to determine the effects of coupling between the elements. Simulating the entire structure would be extremely time consuming, so some simplifications are made:

(1) Switch flexures , anchors, and etch holes are eliminated

(2) Six switches are simulated together, instead of all 22 (as shown in Figure 3.24(b))

(3) Switches are either all open or all closed to eliminate complex layer assignments to account for the different heights in each state

(4) Vias are used to connect the switch layer to the microstrip layer, which are the size of the contact dimple

(5) All metal layers are infinitely thin

(6) In the closed position, the switch is at a height of 1 μm

(7) In the open position, the switch is at a height of 3.5 μm

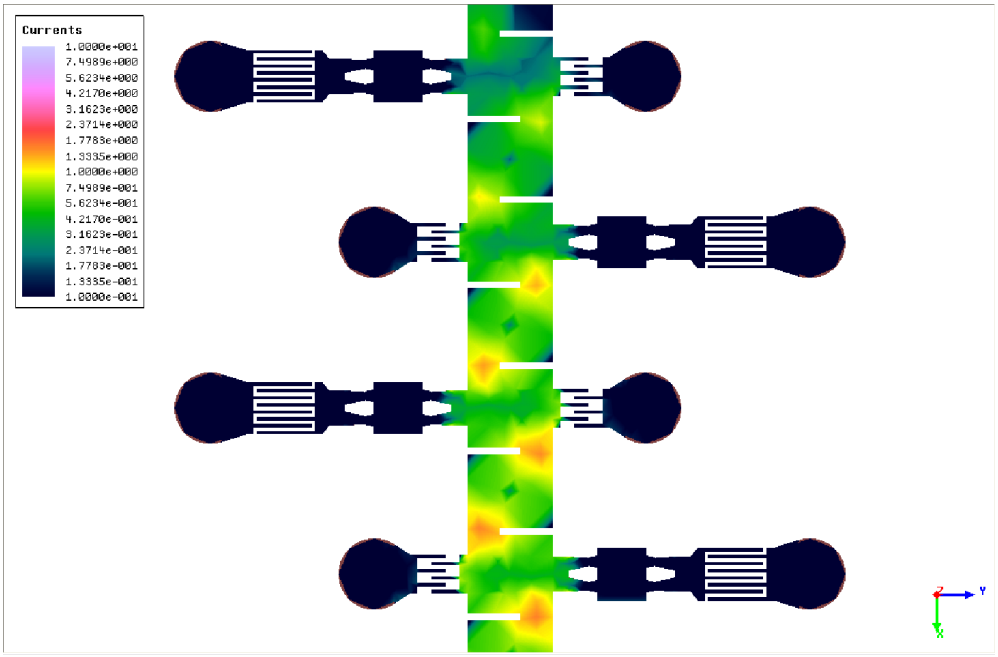
Figure 3.29 shows the surface currents for the cases when all switches are open (a) and all are closed (b). The current color scales are logarithmic from 0.1 to 10 and are the same in both (a) and (b). The isolation of the switches is apparent in (a), since no currents are present in the switch or the capacitor and via behind the switch. When the switches are closed, moderate current densities are present in the switch membrane (approximately 0.5).

The phase of the circuit in the full-wave simulation was electrically smaller than the schematic simulation by a few degrees, possibly due to coupling between the elements. Each cell is designed to have a phase of 21.2°. The phase of the unit cell was determined by examining the phase of S_{21} of the complete circuit and dividing by the number of switches. The phase of each unit cell reached convergence for six or more switches. To compensate for the phase variation, the unit cell in the ADS schematic was re-optimized to be a few degrees longer, the new physical dimensions exported in a layout, and re-simulated in the full-wave simulator. Unfortunately, no correlation exists to verify the accuracy of Ansoft Designer with measured results. At this stage, the full-wave simulation exists as a best estimate. A six-switch test circuit is included on the wafer to verify the full-wave all-open or all-closed scenario. From this circuit, the phase of the unit cell will also be determined.

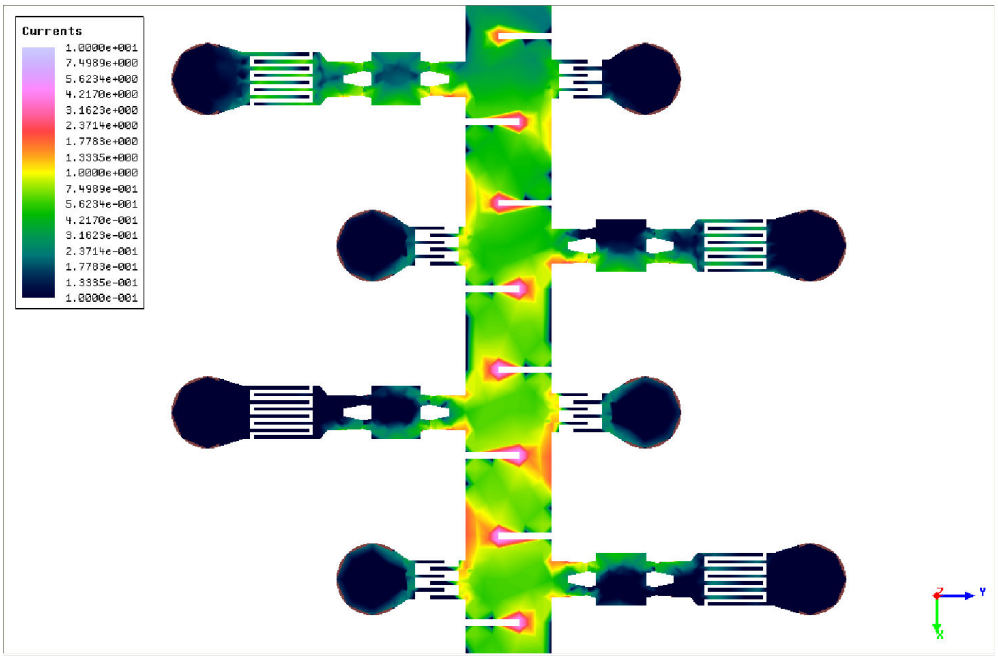
Table 3.3 shows how the phase and input match changed from the physical dimensions initially determined by the optimization routine to the final values used in the design after compensating the dimensions. Ideally, the six-switch test circuit should be well matched in both the open and closed states, and have phase of 21.2° in the open state and 30° in the closed state.

3.6 Complete Circuit

The final required elements in the tuner implementation are the resistive elements necessary for actuating the switch. The resistive layer has a resistivity of $3\,\mathrm{k}\Omega/\square$. This



(a) All Switches Open



(b) All Switches Closed

Figure 3.29: Method of Moments (MoM) simulation of 6 switches (as shown in Figure 3.24(b)) with all switches in the open state (a) and closed state (b). Only 4 switches are shown for clarity. The current color scale is logarithmic from 0.1 to 10. The isolation provided by the switches is evident in (a), and when the switches are closed they are in regions of moderate current density (the maximum is approximately 0.5), shown in (b).

Table 3.3: Initial and Final S-Parameter Values from Full-Wave Simulation

	Switch Open		Switch Closed	
Parameter	Initial	Final	Initial	Final
S_{11} (6 cells)	-33.7 dB	-34.6 dB	-15.8 dB	-34.5 dB
S_{21} (6 cells)	-0.12 dB	-0.14 dB	-0.30 dB	-0.24 dB
phase(S_{21}) (1 cell)	18.9°	21.4°	25.6°	29.6°

highly resistive material has a very small effect on the microwave performance (according to full-wave simulations that include the resistive layer) and is therefore neglected during the optimization. Since the actuation lines are gathered to a 12-pin DC probe pad, different lengths are required for each switch. In order to not have different resistances associated with each switch, the resistive lines are kept at a constant length, and then gold traces are used to connect the lines with the DC bias pads, shown in Figure 3.30. The actuation resistor R_A is 400 kΩ.

Additionally, it is essential that the switch plate be at the same potential as the lines it touches when it makes contact. The center RF line is at DC ground, so the switch plate is connected through a resistor R_D to a via in an adjacent cell. The switch makes contact with one side of the interdigital capacitor, so these two surfaces are kept at equal potentials through the equalization resistor R_E, which is 100 kΩ. Both the switch plate and the interdigital capacitor are discharged through the discharge resistor $R_D = 200\,\text{k}\Omega$. These resistor values are summarized in Table 3.4.

Table 3.4: Resistor Values

Resistor Line	Total Resistance
R_A	400 kΩ
R_E	100 kΩ
R_D	200 kΩ

The final circuit layout is shown in Figure 3.31, including all 22 switches, RF and DC probe pads, and all bias resistors. The overall dimensions are 5 mm by 11.5 mm.

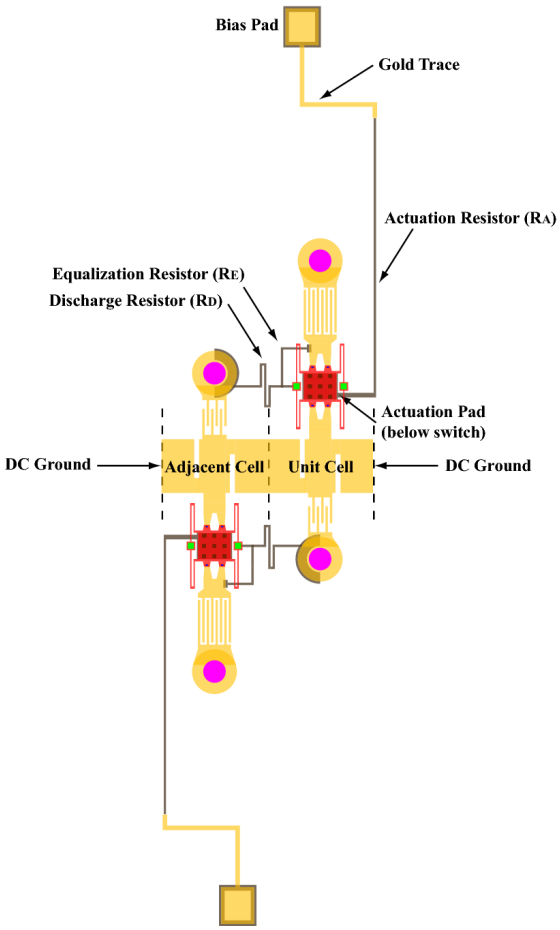


Figure 3.30: Resistor layout for actuation and discharge of the MEMS switch.

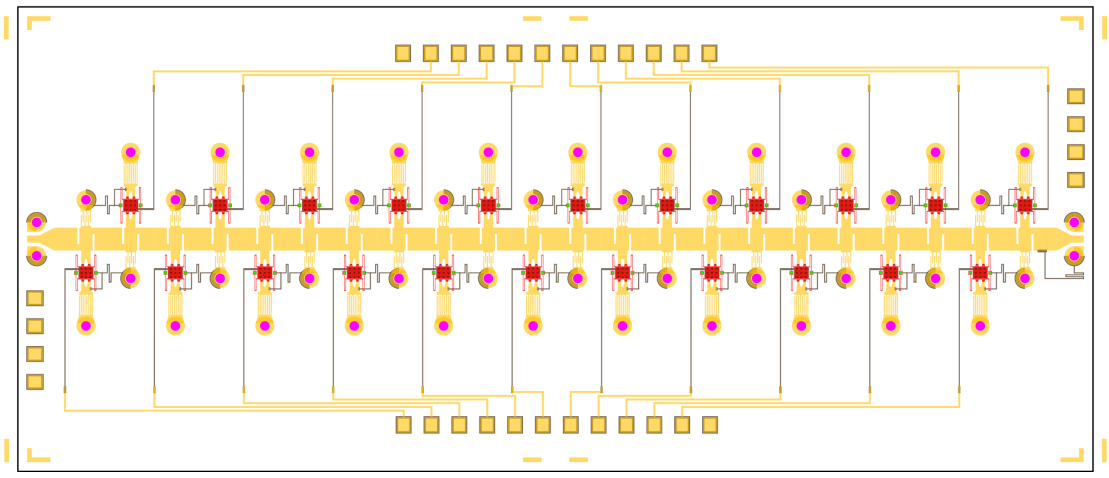


Figure 3.31: The complete circuit layout, which includes all 22 switches, RF and DC probe pads, and actuation and discharge resistors. The outer dimensions of the circuit are 5 mm by 11.5 mm.

Chapter 4

Performance Analysis of Tuner Networks

Determining how well a tuner network is performing involves several steps. The insertion loss of the network is of primary importance, especially in amplifier systems where output power and system efficiency are at stake. As discussed in previous chapters, the aim of reducing the loss of the network led to the design of a tuner with an impedance constellation much less dense than other tuners in the literature. This chapter examines the tuner in a quantitative manner and provides a means of comparison between different tuner designs.

Since insertion loss is of highest importance in these designs, the definition of loss is reviewed in Section 4.1. There are major discrepancies in the literature, particularly in the case of MEMS-based impedance tuners, about the determination of insertion loss from s-parameters. The alternative s-parameter method used in the MEMS literature and the standard method are compared with respect to the definition of insertion loss, and the limitations of the alternative method are discussed.

Often circuit components do not require a perfect match, but are specified to a certain standing-wave ratio (SWR). Since low-density impedance constellations cannot match all impedances, Section 4.2 shows how a specified SWR can be mapped into circles around the various impedance points at the input of the tuner. This mapping determines regions in which impedances can be mapped to within the specified SWR. Section 4.3 shows how the area of these regions may be numerically integrated such that

the coverage area of the tuner (Section 4.4) and the overlap of the regions (Section 4.5) are quantified. This quantification allows a "bandwidth" to be determined for the amplifier, i.e. a frequency range over which the impedance constellation is capable of matching a specified range of impedances to within a specified SWR.

The output power of the RPA is a combination of the output power of the amplifier (with a lossless output), the loss of the tuner state, and the mismatch of the state. This concept is illustrated in Section 4.6.

In critical applications, it is important that the tuner degrade gracefully as devices fail. Section 4.7 examines the methods of failure in the tuner, and shows how many devices may fail before the tuner is no longer capable of meeting coverage specifications.

4.1 Insertion Loss

What is termed "insertion loss" in the characterization of MEMS switches [63] leads to significant error when calculating the loss of MEMS-based impedance tuners, using loss as a negative power gain. This section aims to clarify the conditions under which this formula is valid, and how this formula relates to the standard definition of insertion loss.

The standard definition of insertion loss is

$$IL = \frac{P_L}{P_{in}}, \tag{4.1}$$

where P_L is the power delivered to the load and P_{in} is the power inserted into the system $[S]$ after any mismatch reflections, shown in Figure 4.1. The operating power gain of a network is also defined as P_L/P_{in}. In this sense, loss is equivalent to negative power gain.

Using a signal-flow diagram to relate the insertion loss to the s-parameters of $[S]$, Eq. 4.1 may be expressed with no assumptions made about the load Z_L by [64]

$$IL = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2}. \tag{4.2}$$

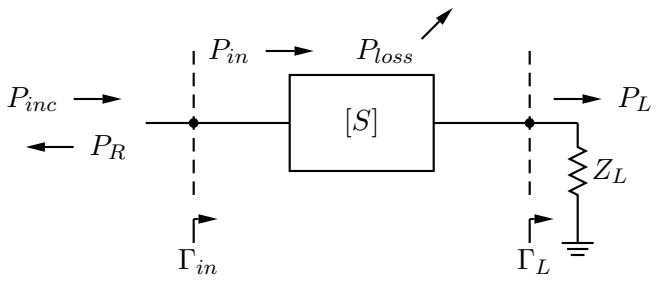


Figure 4.1: Power waves in a two-port lossy system $[S]$. P_{inc} is the incident power available from the source, and P_R is the reflected power due to impedance mismatch characterized by Γ_{in}. P_{in} is the input power of the system $[S]$, P_{loss} is the power lost in the system, and P_L is the power delivered to the load, Z_L.

When the load Z_L is matched ($\Gamma_L = 0$), Eq. 4.2 reduces to

$$IL = 10 \log \left(\frac{|S_{21}|^2}{1 - |S_{11}|^2} \right), \tag{4.3}$$

including a conversion to decibels, in which insertion loss is typically expressed.

The alternative definition of insertion loss in terms of s-parameters in [63] is

$$1 - |S_{11}|^2 - |S_{21}|^2 = Loss, \tag{4.4}$$

where $Loss$ is the percentage power loss. $Loss$ is converted to decibels [65] using

$$IL = 10 \log \left(1 - Loss\right). \tag{4.5}$$

The following section will show that the insertion loss in Eq. 4.5 defined by the percentage power loss in Eq. 4.4 is valid only in the case where the device under test ($[S]$) is matched to the source. These cases include a single switch under test, and most tunable filter and phase shifter applications. However, in the case of a matching circuit at the output of an amplifier, the matching circuit must be characterized in order to determine the insertion loss of the matching block alone. In this case, a matching circuit measured in a $50\,\Omega$ system is not matched. This mismatch, however, should not affect the loss characteristics of the matching block provided the load remains the same.

4.1.1 Validity Conditions

The argument for the validity of Eq. 4.4 and Eq. 4.5 comes from power conservation principles [65, 66]. In Figure 4.1, when the load Z_L is matched (all power available from system $[S]$ is delivered to the load as P_L), the power conservation equations states

$$P_{inc} - P_R - P_{loss} - P_L = 0. \tag{4.6}$$

These power waves may be related to the s-parameters of $[S]$ (again, when Z_L is matched) by:

$$P_R = P_{inc}|S_{11}|^2, \tag{4.7}$$

$$P_L = P_{inc}|S_{21}|^2, \tag{4.8}$$

$$P_{in} = P_{inc}(1 - |S_{11}|^2) = P_{inc} - P_R. \tag{4.9}$$

Through substitution into Eq. 4.6

$$P_{inc} - P_{inc}|S_{11}|^2 - P_{inc}|S_{21}|^2 - P_{loss} = 0$$

$$P_{inc}(1 - |S_{11}|^2 - |S_{21}|^2) = P_{loss}.$$

What is termed percentage loss ($Loss$) in Eq. 4.4 is actually the ratio of the lost power P_{loss} to the incident power P_{inc}:

$$(1 - |S_{11}|^2 - |S_{21}|^2) = Loss = \frac{P_{loss}}{P_{inc}}. \tag{4.10}$$

Substituting into Eq. 4.5 gives

$$\begin{aligned} IL &= 10\log\left(1 - \frac{P_{loss}}{P_{inc}}\right) \\ &= 10\log\left(\frac{P_{inc} - P_{loss}}{P_{inc}}\right). \end{aligned} \tag{4.11}$$

By re-examining the power conservation equation, Eq. 4.6, the numerator can be re-expressed as $P_R + P_L$. Also, the denominator is equivalently $P_{in} + P_R$ from (4.9). Therefore, Eq. 4.11 is equivalently

$$IL = 10\log\left(\frac{P_R + P_L}{P_{in} + P_R}\right). \tag{4.12}$$

Under the condition that the system $[S]$ is perfectly matched ($P_R = 0$), then this formula reduces to the standard definition of insertion loss in Eq. 4.1. However, when the system $[S]$ is not perfectly matched, using Eq. 4.4 and Eq. 4.5 to calculate insertion loss is no longer valid, and becomes increasingly inaccurate as reflected power increases. This invalidity occurs because Eq. 4.4 and Eq. 4.5 are dependent on the incident power. However, the definition of insertion loss is dependent only on the input power, that is, the power inserted into the network. Regardless of the reflected power due to a mismatch of system $[S]$ to the source, the loss of system $[S]$ alone should remain the same.

Insertion loss is universally defined in Eq. 4.1, and may always be computed from s-parameters using Eq. 4.2. In the case of a matched load, Eq. 4.2 reduces to Eq. 4.3. The formulas in Eq. 4.4 and Eq. 4.5 are only valid when P_R is zero. Most MEMS circuits to-date [63], namely phase shifters and filters, are intended to be well matched, and so Eq. 4.4 and Eq. 4.5 are relatively accurate (though the reflected power in these circuits is not absolutely zero, which leads to slight inaccuracies). A matching circuit block consisting of MEMS impedance tuners is intentionally not matched in a $50\,\Omega$ measurement system, and so for the first time the discrepancies in Eq. 4.4 and Eq. 4.5 become apparent. In conclusion, the most general formula in Eq. 4.2 is always valid and the best means of calculating of insertion loss. In addition, if a tuner circuit is characterized alone, into $50\,\Omega$ ports, Eq. 4.2 best describes the measurement used to determine insertion loss.

4.2 Constellation Density Based on Acceptable SWR

Most systems are specified to a particular SWR, indicating how well the system must be matched. Often, a perfect match is not required and a final SWR in the range of 1.1–1.5 is acceptable. In order to determine how this range affects the design of the tuner, the SWR must be translated into a range of impedances and mapped

through the network to a range of impedances at the input of the tuner. This requires operations in several mathematical domains. These domains occur in complex planes in the locations indicated in Figure 4.2. The Z plane and its corresponding Γ plane are located between the tuner and the load. Impedances and reflection coefficients in these planes are mapped through the network to new impedances and reflection coefficients on the Z' and Γ' planes respectively. The tuner block contains the double-slug tuner network designed in Chapter 3, repeated as a block diagram here for clarity.

A conventional amplifier is connected directly to the load, and an SWR is specified at the Z plane, as shown in Figure 4.2(a). In the case of a reconfigurable amplifier, the goal is to determine what impedances in the Z' plane for a variable load Z_L, shown in Figure 4.2(b) can the tuner correct to the same SWR at the amplifier (in the Z plane).

From a specified SWR and a load of $Z_L = 50\,\Omega$, the magnitude of the reflection coefficient which produces this SWR can be found by:

$$|\Gamma| = \frac{SWR - 1}{SWR + 1}. \tag{4.13}$$

This produces a circle Ψ in the complex Γ plane of radius $|\Gamma|$, defined by

$$\Gamma_\Psi = |\Gamma| e^{j\phi}, \tag{4.14}$$

where ϕ in the domain 0–2π. The corresponding impedance in the Z plane is found by

$$Z_\Psi = Z_0 \frac{1 + \Gamma_\Psi}{1 - \Gamma_\Psi}. \tag{4.15}$$

A load impedance Z_L may be represented in chain matrix form as the product of a shunt admittance $Y = 1/Z_L$ and an open circuit, where the voltage is 1 and current is 0:

$$[A_L] = \begin{bmatrix} 1 & 0 \\ 1/Z_L & 1 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} = \begin{bmatrix} 1 \\ 1/Z_L \end{bmatrix}.$$

In this case, however, the impedance in the Z plane is not Z_L, but rather a domain of

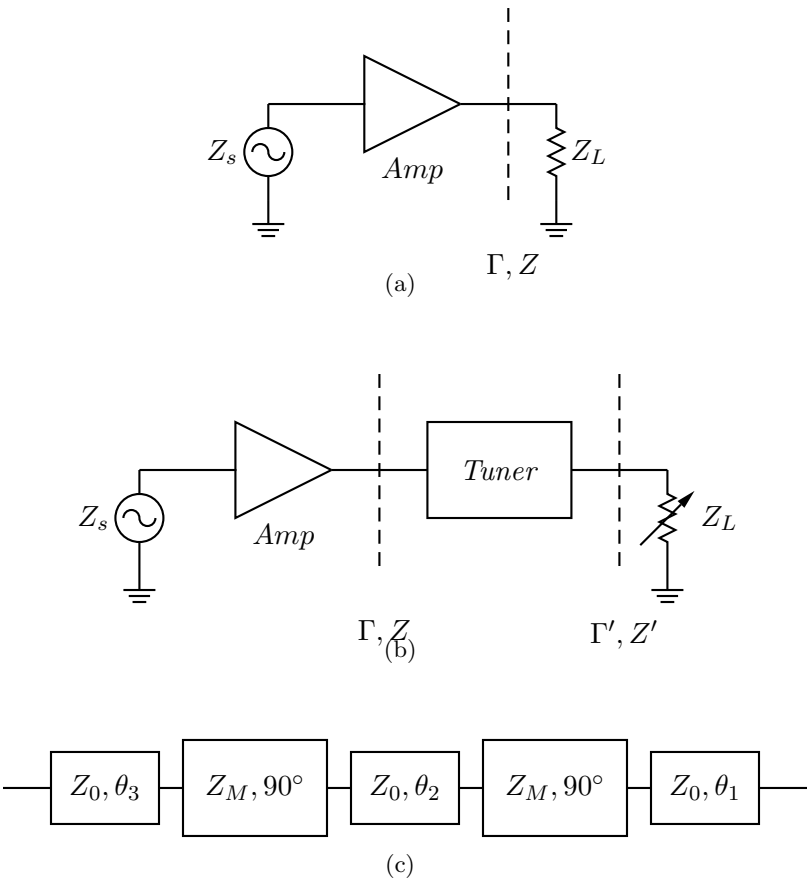


Figure 4.2: An amplifier connected to a fixed load (a) is typically specified to an SWR at the Z plane. With a variable load (b), the tuner must correct the impedance at the Z' plane within the same SWR specification as (a) at the Z plane. Thus, a variable load results in no change in the amplifier performance. The tuner block in (b) is expanded in (c) and consists of the double-slug network from Chapter 3, Figure 3.12 as an example.

impedances Z_Ψ

$$[A_\Psi] = \begin{bmatrix} 1 & \\ & 1/Z_\Psi \end{bmatrix}.$$

The tuner network may also be defined as a chain matrix

$$[A_{T_s}] = \begin{bmatrix} A_s & B_s \\ C_s & D_s \end{bmatrix},$$

where s is the particular impedance state of the tuner.

Cascading the tuner with the complex load domain gives the state-dependent chain matrix at the input of the tuner:

$$[A_{in,s}] = [A_{T_s}]\,[A_\Psi] = \begin{bmatrix} A_s & B_s \\ C_s & D_s \end{bmatrix} \begin{bmatrix} 1 & \\ & 1/Z_\Psi \end{bmatrix} = \begin{bmatrix} A_s Z_\Psi + B_s \\ C_s Z_\Psi + D_s \end{bmatrix}.$$

The input impedance of the tuner in the Z' plane is given by V/I,

$$Z'_{\Psi,s} = \frac{A_s Z_\Psi + B_s}{C_s Z_\Psi + D_s}. \tag{4.16}$$

Eq. 4.16 represents a bilinear transformation [67–69] of impedances from the Z plane to the Z' plane. Typically, this transformation is used to determine the input impedance Z_{in} looking into a network with a fixed load Z_L at the output of the network:

$$Z_{in} = \frac{AZ_L + B}{CZ_L + D}.$$

However, since the bilinear transformation is a conformal mapping, the concept of mapping a single point of impedance may be generalized to a mapping of a domain of complex load impedances at the output, Z_Ψ, to a domain of complex input impedances, $Z'_{\Psi,s}$. Each state s of the tuner has a different chain matrix, so the resulting $Z'_{\Psi,s}$ is a state-dependent mapping of Ψ.

It is customary to view impedance constellations on the Smith Chart, so $Z'_{\Psi,s}$ is mapped from the Z' plane to the Γ' plane

$$\Gamma'_{\Psi,s} = \frac{Z_{\Psi,s} - Z_0}{Z_{\Psi,s} + Z_0}.$$

Figure 4.3 shows $Z_L = 50\,\Omega$ surrounded by circle of SWR = 1.5 defined by Z_Ψ, which is mapped using the method described above to a particular state of the tuner Z_s and a new region of impedances $Z_{\Psi,s}$.

Additionally, the region of impedances enclosed by the boundary Z_Ψ in the Z plane is mapped and enclosed by the boundary $Z'_{\Psi,s}$ in the Z' plane. This principle is demonstrated in Figure 4.4, where concentric SWR circles ranging from 1.1–1.5 are mapped from the Z plane to the Z' plane for state s. Each SWR circle is indicated in a different color.

Figure 4.4 demonstrates that given a maximum SWR acceptable to the amplifier, the tuner is capable of covering an area of the Smith Chart. The coverage areas for SWRs from 1.1–1.5 are shown in Figure 4.5. This figure also shows that the area enclosed by the $|\Gamma|_{max} = 0.61$ circle is completely covered for SWR = 1.5 and 1.4. At SWR = 1.3 small gaps begin to appear in the coverage region, and the coverage area continues to reduce as the SWR approaches 1.1. Section 4.3 discusses a numerical method of determining the area of these regions, and Section 4.4 discusses how the area of these regions changes with frequency, which is used to determine a tuner bandwidth.

Additionally, these regions overlap, as shown in Figure 4.6. For clarity, the only a partial constellation is shown. Several impedance regions are overlapped by two states, such as the one indicated by the "Double Overlap Area" arrow. In this example, there are two regions which are covered by three states, such as the one indicated by the "Triple Overlap Area" arrow. Section 4.5 uses the numerical integration technique from Section 4.3 to determine how many states cover a particular impedance.

In the case of a double overlap (in the region indicated by the arrow in Figure 4.6), impedances in the overlap region are mapped to within the specified SWR by either state A or state B would map the impedance to within the specified SWR. However, the loss of the tuner is dependent on the state. Section 4.6 discusses the trade-off between mismatch and loss, and how the appropriate tuner state is determined such that the

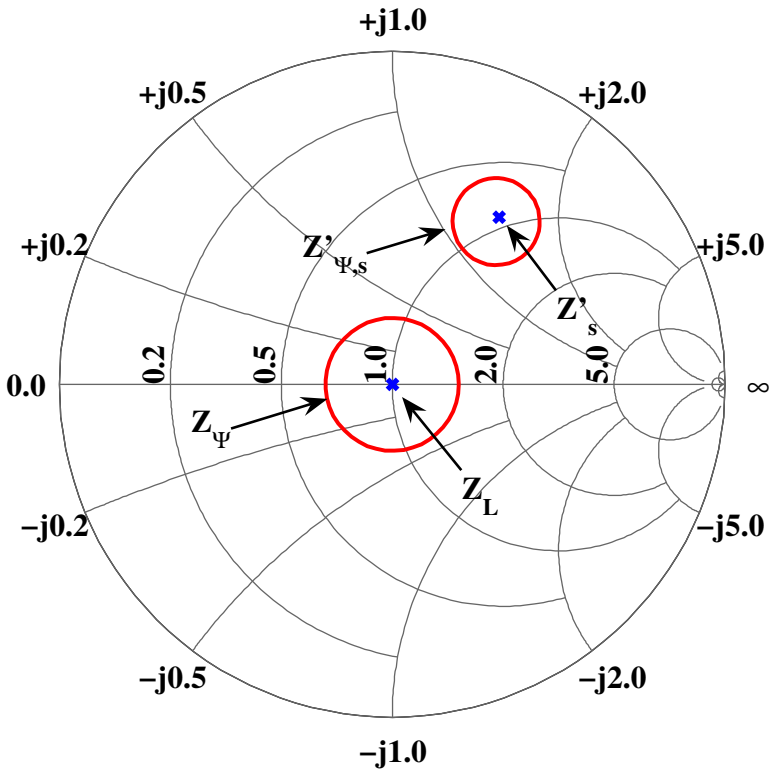


Figure 4.3: Impedance Z_L is mapped through the tuner network to a particular state Z_s. Likewise, a domain of impedances Z_Ψ around Z_L defined by SWR = 1.5 is mapped to a new domain of impedances $Z'_{\Psi,s}$ corresponding to the state of the tuner.

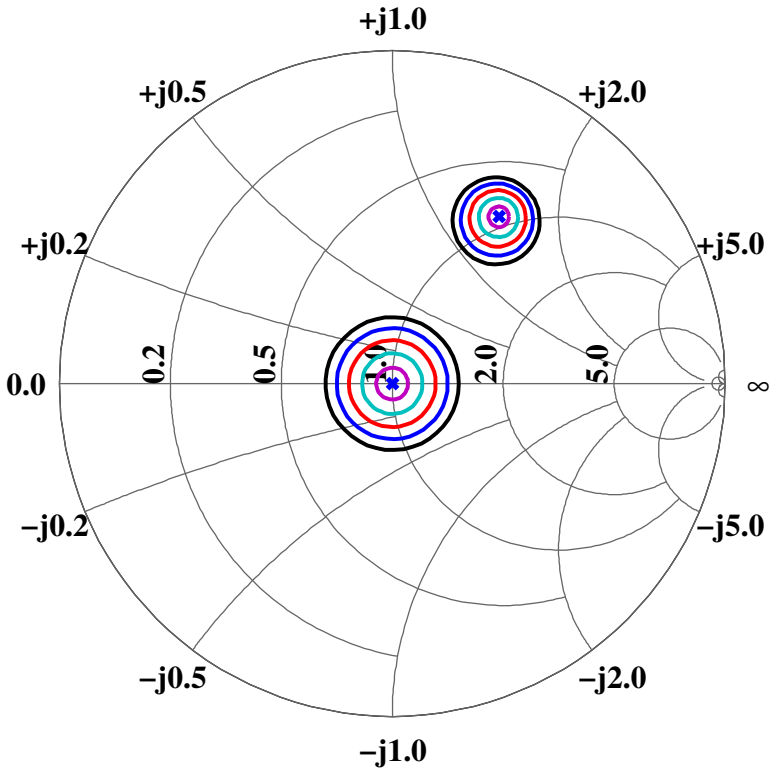
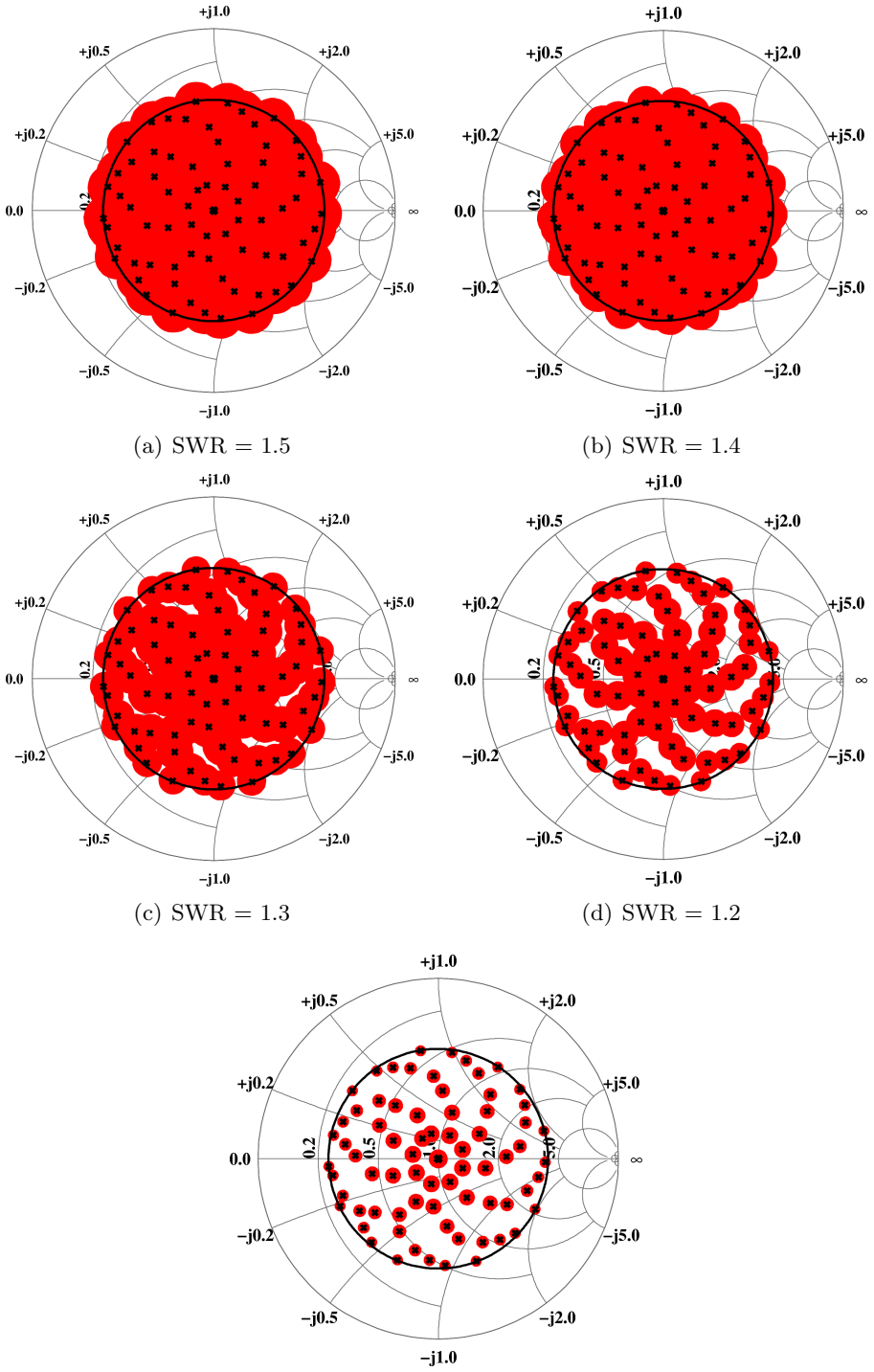


Figure 4.4: A mapping of concentric SWR circles. Concentric circles in the Z plane map are mapped to concentric circles in the Z' plane for state s. This indicated that the entire region enclosed by the boundary Z_Ψ in the Z plane is mapped to the Z' plane and enclosed within the boundary $Z'_{\Psi,s}$. Each SWR circle from 1.1–1.5 is indicated in a different color.



(a) SWR = 1.5

(b) SWR = 1.4

(c) SWR = 1.3

(d) SWR = 1.2

(e) SWR = 1.1

Figure 4.5: Regions covered by specified SWR from 1.5 to 1.1. The $|\Gamma| = 0.61$ circle is also shown, which is the maximum $|\Gamma|$ of all the tuner states.

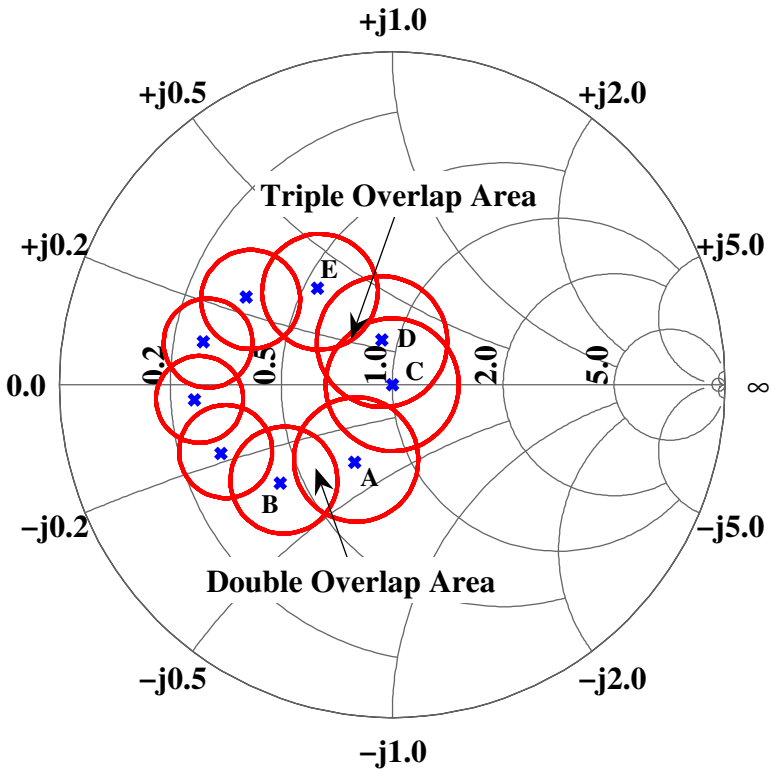


Figure 4.6: An example of overlapping SWR regions in a two slug tuner. In this case, there are several regions of the Smith Chart where two regions overlap, meaning that both states could match an impedance within that region to within the specified SWR. In this case, other criteria should be used to determine the proper choice of state, such as which state has the lowest loss or produces the highest output power. There are two small regions in this example that are overlapped by three states.

RPA has the largest output power (which will simultaneously provide the conditions for highest gain and efficiency). The importance of determining the best state is evident in the case of the triple overlap region (indicated by the arrow). For this region, there are three states which all map the impedance to within the specified SWR: C, D, and E. However, even though state D is closest to any impedance within the overlap region, because state C can be produced by turning all switches in the tuner off (state 0, which has the lowest insertion loss of all possible states from Figure 3.28), it is possible that the mismatch caused by using state C would decrease the overall output power a smaller amount than the combined mismatch and loss of state D. Section 4.6 discusses this hypothesis in greater detail.

4.3 Numerical Determination of Constellation Area

While the area of the regions in each state could be calculated analytically, it would not be possible to calculate the area of all the combined states due to the overlap of the regions, as shown in Figure 4.6. Instead the area of these regions is calculated numerically by defining the boundary of the region as a polygon, and using the "in-polygon" function built into MATLAB. This function returns a 1 if point is inside a polygon or on the boundary, or a 0 if the point is outside the polygon.

To create test points, a mesh is created in the Smith Chart. The Smith Chart is a unit circle in the Γ plane. For the purposes of simplicity, rather than containing the quantization to the unit circle boundary, the quantization matrix extends from -1 to 1 and -j to j in the Γ plane, as shown in Figure 4.7. Selecting points A–H demonstrate how the Γ position translates to a matrix index, shown in Table 4.1, which follows these equations:

$$r_i = (1 + x_p)\,\frac{N}{2} \tag{4.17}$$

$$c_i = (1 - y_p)\,\frac{N}{2}, \tag{4.18}$$

where r_i and c_i are the row and column matrix index, and x_p and y_p are the x (real) and y (imaginary) positions in the Γ plane. N is the size of the matrix, which is NxN. In this analysis, $N = 200$, such that moving one index in the matrix in any direction is equivalent to a change of 0.01Γ.

Table 4.1: Quantization of Γ

Point	Γ Coordinate (x_p, y_p)	Matrix Index $[r_i, c_i]$
A	$(-1, 1)$	$[1, 1]$
B	$(0, 1)$	$[1, N/2]$
C	$(1, 1)$	$[1, N]$
D	$(1, 0)$	$[N/2, N]$
E	$(1, -1)$	$[N, N]$
F	$(0, -1)$	$[N, N/2]$
G	$(-1, -1)$	$[N, 1]$
H	$(-1, 0)$	$[N/2, 1]$

In order to decrease the computation time, the search matrix is limited to a subset, m, of the full NxN matrix, M. This search matrix m is determined by determining the floor and ceiling of the polygon in the x and y directions, which rounds the actual value to the next lowest or next highest integer respectively. To ensure completeness, the search matrix is extended by one index in both directions.

To demonstrate, the dashed region of Figure 4.7 is shown in detail in Figure 4.8. Two overlapping boundaries are indicated, the first in red and the second in blue. For the red boundary, a search space is determined using the floor to ceiling plus one method described above, which defines the red square. Nodes inside the square are tested using the "inploygon" function, also described above. In Figure 4.8, nodes that are inside the polygon or on the boundary return a 1, indicated by the red circles. Once the search is complete, the second blue region is tested. Again, a search space is defined around the region, indicated by the blue square, and nodes are tested in a similar manner, returning a 1 inside the region and on the boundary, indicated by the blue squares. Note that for efficiency of the following operations on the two matrices, M and m are the same size;

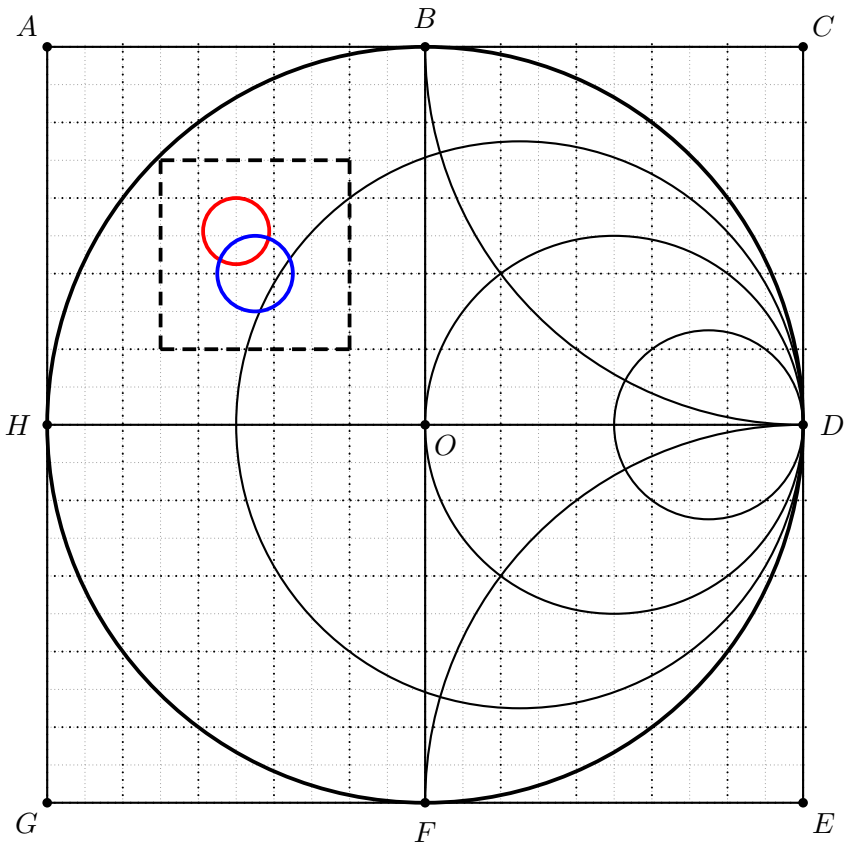


Figure 4.7: The quantization of the Smith Chart for numerical analysis. The conversions of points A–H and O from the Γ plane into matrix indices are shown in Table 4.1. In the following analysis, the matrix is 200x200 such that each node is a 0.01 change in Γ.

m is simply indexed using the floor to ceiling plus one method such that a subset of the matrix is tested in the "inpolygon" function. The rest of matrix m is padded with zeros.

When each search is complete, the resulting matrix m is combined with the full matrix M using an OR operation to ensure that the overlap region, indicated by the magenta triangles, is not counted twice:

$$M = M \vee m. \tag{4.19}$$

The area of the region is computed by performing a two-dimensional sum over the NxN matrix, which counts the number of nodes that lie inside the boundary, and multiplying the result with the area of the mesh grid, which is $(N/2)^2$:

$$Area = \sum_{r_i=1}^{N} \sum_{c_i=1}^{N} M\left[r_i, c_i\right] \cdot \left(\frac{N}{2}\right)^2. \tag{4.20}$$

This method is used to compute the coverage area of the tuner, discussed in Section 4.4.

Alternatively, it is possible to determine the number of regions in which a node lies by combining the search space with the NxN matrix using an ADD operation. This would result in the magenta triangles returning a value of 2, and both the red circles and blue squares returning a value of 1.

$$M = M + m \tag{4.21}$$

The area of the region that is covered by at least n tuner states is computed by:

$$Overlap_n = \sum_{r_i=1}^{N} \sum_{c_i=1}^{N} \left(M\left[r_i, c_i\right] \geq n\right) \cdot \left(\frac{N}{2}\right)^2. \tag{4.22}$$

This method is used to compute the coverage redundancy, discussed in Section 4.5.

4.4 Performance Analysis #1: Coverage Area vs. SWR

One means of gauging the performance of an impedance tuner is by specifying a desired coverage range and measuring how well the tuner covers that range. At 10 GHz,

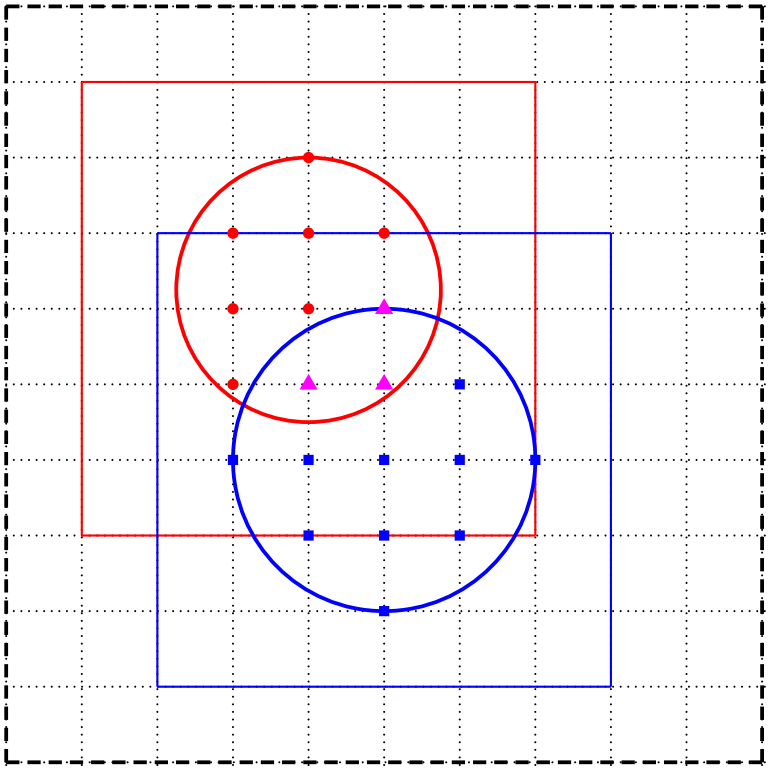


Figure 4.8: An example of how the area of the SWR regions is determined numerically. This is an enlarged view of the dashed region indicated in Figure 4.7. In the case of the red circle region, a search space is define around the region to limit computation time, indicated by the red square. Nodes within the square are tested and return a 1 if the node lies within or on the boundary of the polygon that describes the region. In the case of the red region, nodes which return a 1 are indicated by the red circles and magenta triangles. The process is repeated for the blue region, with a new search space defined by the blue square. Nodes returning a 1 are indicated by the blue squares and the magenta triangles. When the regions are combined together, the region with the magenta triangles was covered by both the red and blue regions. This region could be counted only once using an OR operation to determine the total area enclosed by the two regions (Section 4.4), or it could be summed to determine how many regions cover a particular node (Section 4.5).

the tuner is designed to generate impedance states out to a maximum Γ of 0.61. Setting $|\Gamma|_{max} = 0.61$ defines a circle as shown in Figure 4.5. Figure 4.5 also shows that for SWR > 1.4, the range is completely covered.

The coverage area is calculated numerically by applying a mask to the numerical area calculation from Section 4.3. This mask contains 0s outside the specified $|\Gamma|_{max} = 0.61$ circle and 1s in the interior. Matrix M is combined with the mask through an OR operation to eliminate all points outside the $|\Gamma|_{max} = 0.61$ circle. Table 4.2 shows the percent coverage of the tuner at 10 GHz for specified SWR values.

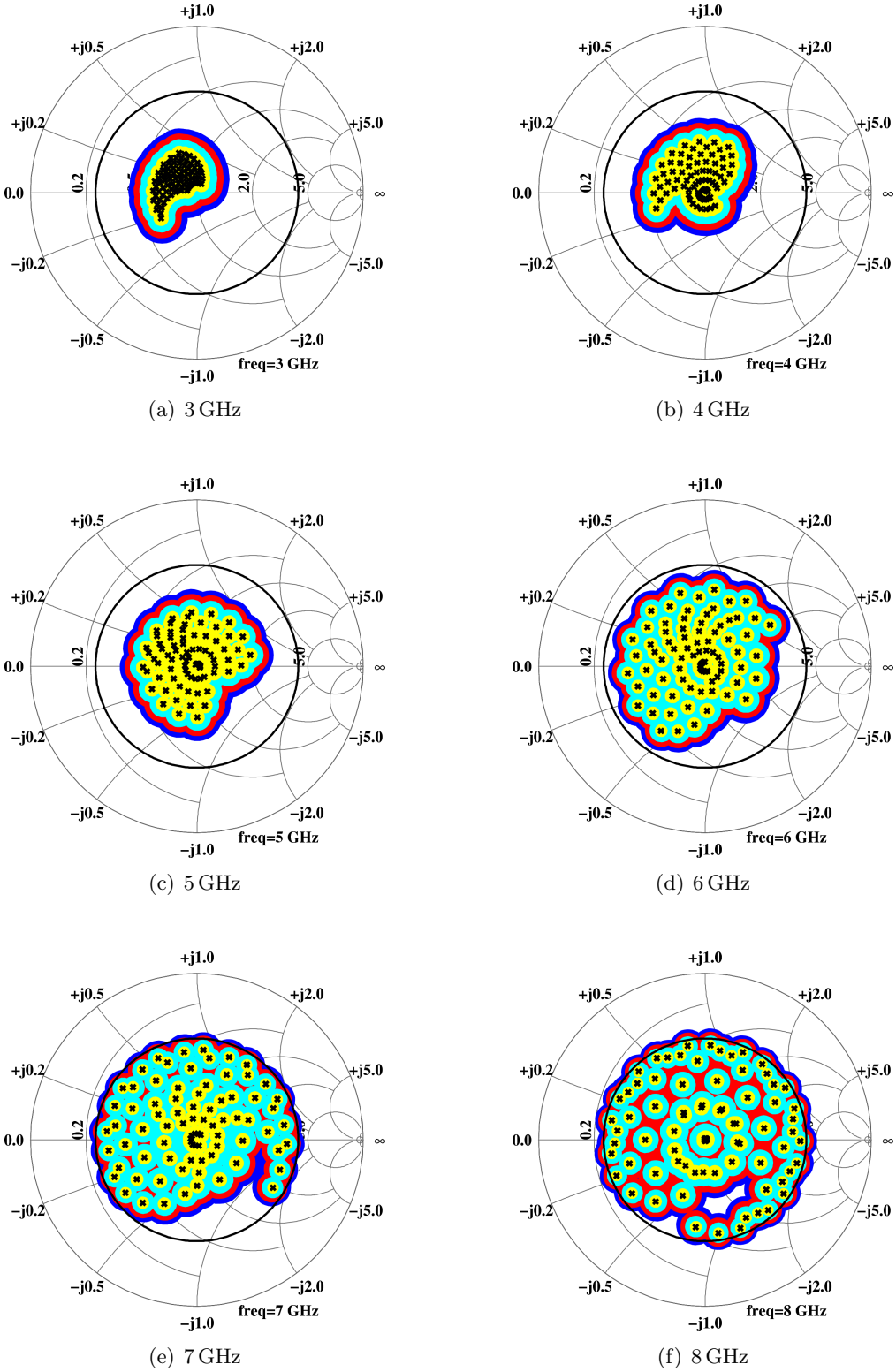
Table 4.2: Percent Coverage at 10 GHz

SWR	Coverage (%)
1.5	100
1.4	100
1.3	95
1.2	71
1.1	24

To interpret Table 4.2, a signification portion of the desired coverage area (71%) can be matched to SWR=1.2 or better. Of the 29% of the desired range that cannot be matched to 1.2, 82% of those impedances can be matched if the specification is relaxed to SWR=1.3, bringing the total coverage area to 95% of the desired range. The remaining 5% can be covered if the specification is further relaxed to SWR=1.4.

To determine a coverage bandwidth for the tuner, this analysis is extended over frequency. Figure 4.9 shows the changes in the tuner constellation as frequency is swept. Overlaying SWR regions are shown in color, with SWR = 1.1 in yellow, 1.2 in cyan, 1.3 in red, and 1.4 in blue. The true impedance points are indicated by the black x, and the desired coverage range is indicated by the black circle.

Figure 4.9 shows that the tuner does not begin to cover the specified range until close to 8 GHz (Figure 4.9(f)). The range that is not covered in Figure 4.9(f) by an SWR of 1.4 is covered by 1.5. X-band is shown in detail in Figure 4.9(f)–(m), with good

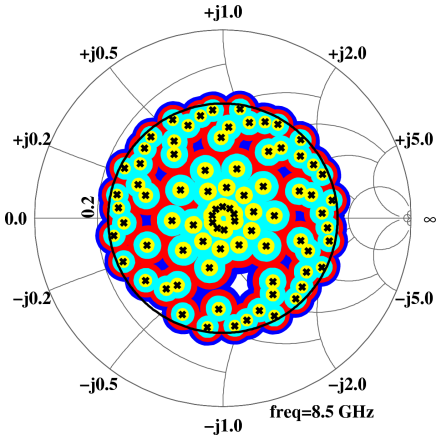


(a) 3 GHz (b) 4 GHz

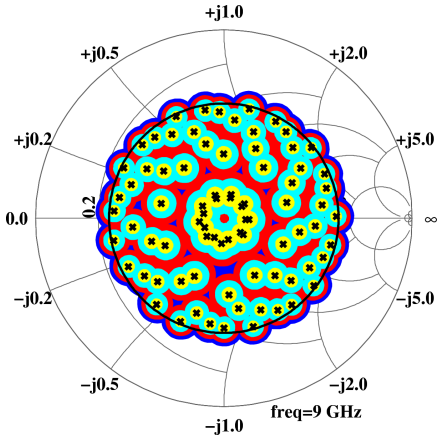
(c) 5 GHz (d) 6 GHz

(e) 7 GHz (f) 8 GHz

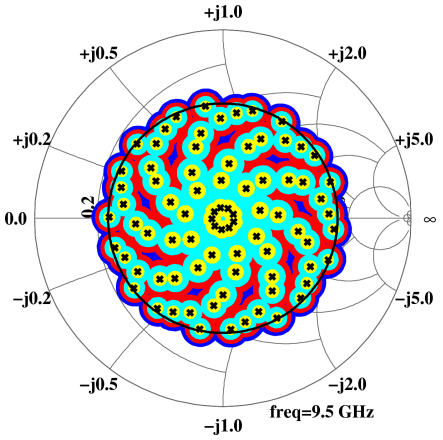
Figure 4.9: SWR regions from 3–8 GHz. The states (black x) are enclosed by regions of increasingly smaller SWR at the output; SWR = 1.4 (blue), SWR = 1.3 (red), SWR = 1.2 (cyan), and SWR = 1.1 (yellow). $|\Gamma|_{max} = 0.61$ is also shown.



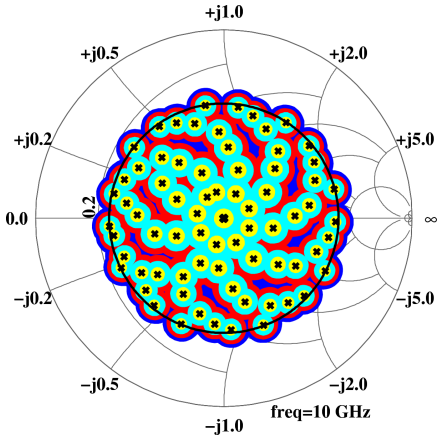
(g) 8.5 GHz



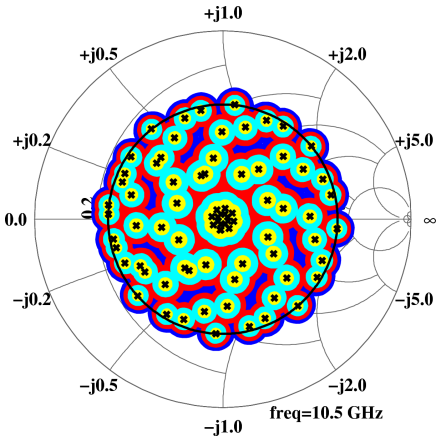
(h) 9 GHz



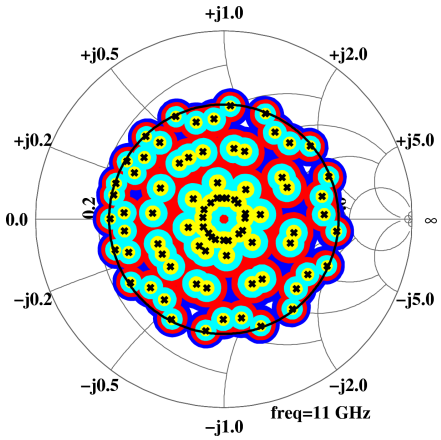
(i) 9.5 GHz



(j) 10 GHz

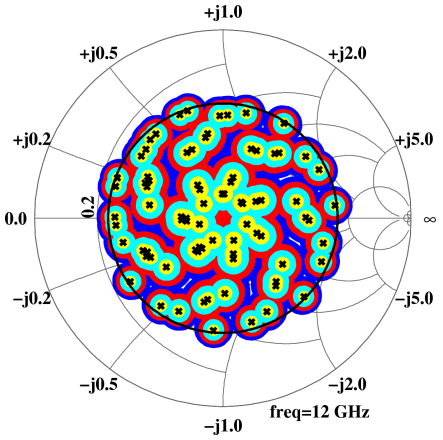


(k) 10.5 GHz

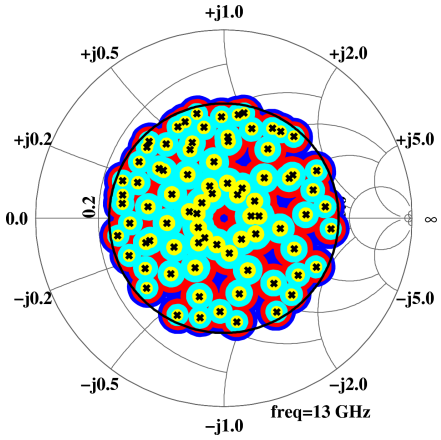


(l) 11 GHz

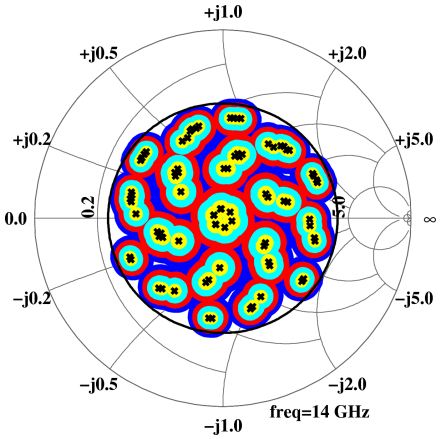
Figure 4.9: SWR regions from 8.5–11 GHz. The states (black x) are enclosed by regions of increasingly smaller SWR at the output; SWR = 1.4 (blue), SWR = 1.3 (red), SWR = 1.2 (cyan), and SWR = 1.1 (yellow). $|\Gamma|_{max} = 0.61$ is also shown. (cont.)



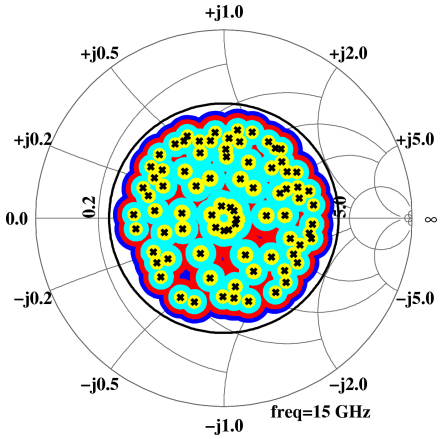
(m) 12 GHz



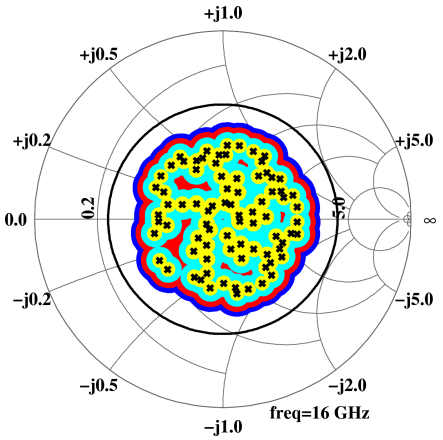
(n) 13 GHz



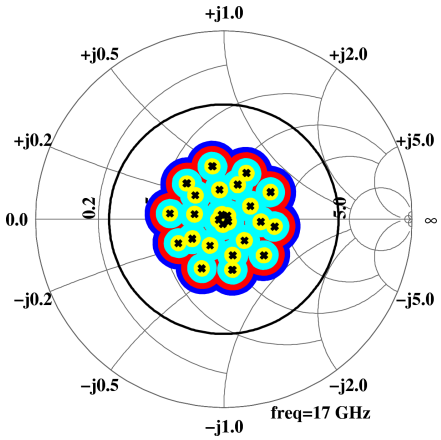
(o) 14 GHz



(p) 15 GHz



(q) 16 GHz



(r) 17 GHz

Figure 4.9: SWR regions from 12–17 GHz. The states (black x) are enclosed by regions of increasingly smaller SWR at the output; SWR = 1.4 (blue), SWR = 1.3 (red), SWR = 1.2 (cyan), and SWR = 1.1 (yellow). $|\Gamma|_{max} = 0.61$ is also shown. (cont.)

coverage of the specified circle. The coverage region begins to reduce around 15 GHz, shown in Figure 4.9(p)–(r).

The percent coverage is plotted for SWR = 1.1–1.5 in Figure 4.10 in order to determine an exact coverage bandwidth. The coverage area of the tuner is greater than 99% for an SWR of 1.5 from 8.0 GHz to 14.4 GHz. Coverage is greater than 99% for an SWR of 1.4 from 8.4–12 GHz and from 12.6–13.4 GHz.

Between 12 and 12.6 GHz, the tuner impedance states cluster together, which prevents those frequencies from being covered to an SWR of 1.4, but those regions are covered to an SWR of 1.5.

Should coverage at a higher SWR be required, the tuner would need to provide a denser constellation. As shown in Figure 4.10, coverage at and SWR of 1.3 is averages 93% across X-band (95% at 10 GHz), and coverage at 1.2 is averages around 65% (70% at 10 GHz).

This method of coverage analysis provides a useful tool in determining the best tuner configuration to meet design specifications. In this study, this particular tuner was chosen for demonstration purposes for having a moderately dense constellation that covered a $|\Gamma| = 0.6$ circle. This analysis shows that this particular tuner is capable of covering the entire region to an SWR of 1.4 across X-band. However, in a true design scenario, the coverage region, bandwidth, and SWR would be specified at the beginning of the tuner design. Design options from Figures 3.16 and 3.17 could be tested with this method in order to choose suitable configuration options. These options could then be tested again other criteria, including coverage redundancy (Section 4.5) and insertion loss to determine the best network design for a given application. It is likely that the least complex option (i.e. the fewest switches in the network) would provide the lowest loss, however a full circuit model is required to determine loss.

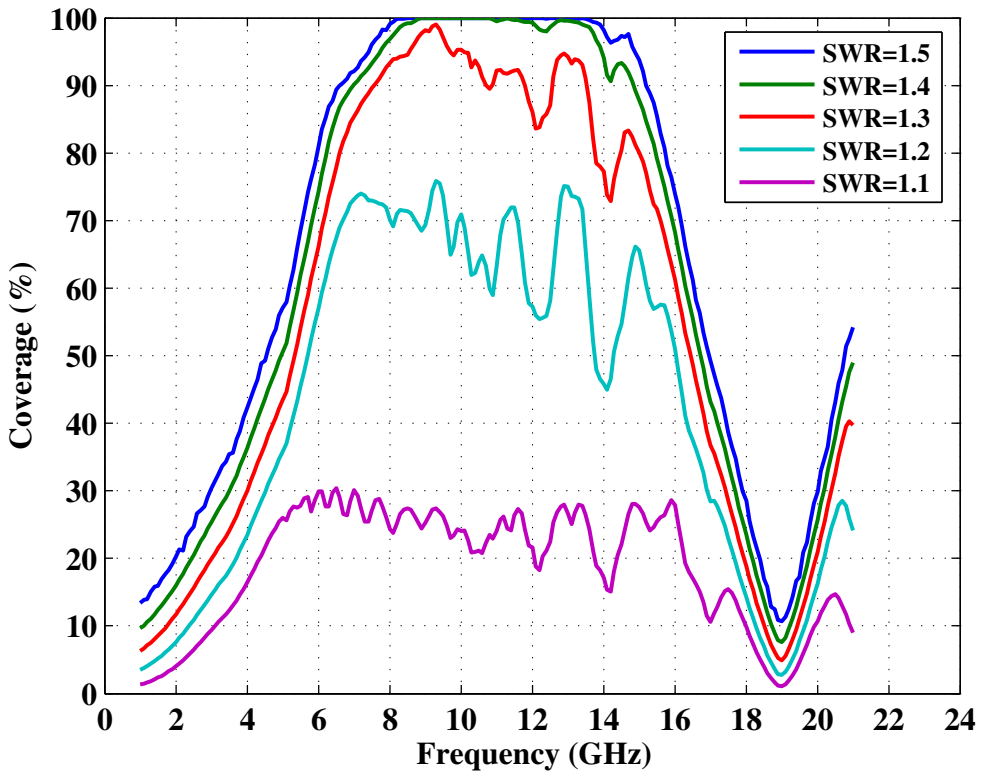


Figure 4.10: The coverage area bandwidth of the tuner, shown for SWR = 1.1–1.5. The coverage area of the tuner is greater than 99% for an SWR of 1.5 from 8.0 GHz to 14.4 GHz. Coverage is greater than 99% for an SWR of 1.4 from 8.4–12 GHz and from 12.6–13.4 GHz.

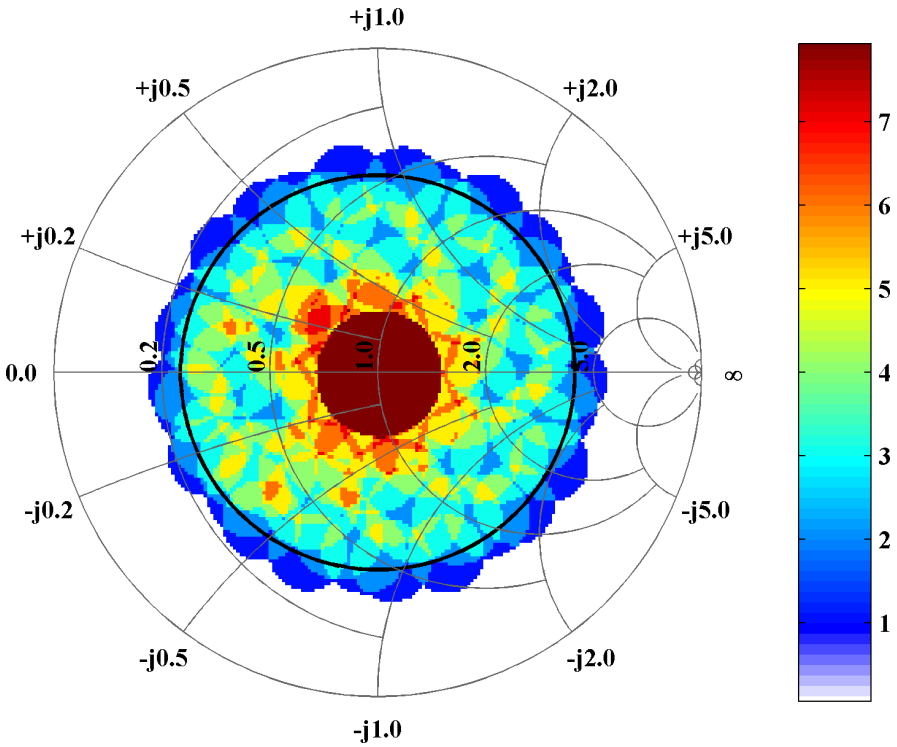
4.5 Performance Analysis #2: Coverage Redundancy vs. SWR

A second means of analyzing the performance of the tuner is through examination of the coverage redundancy. Specifying a desired SWR generates regions around the impedance states, as shown in Section 4.2. As the density of the constellation increases, these regions begin to overlap. In the area of overlap, multiple states can match the impedances to the specified SWR and so a second criterion may be used to determine the best state. This choice must consider which state provides the highest output power (which in turn gives the highest amplifier efficiency), given the mismatch of the state and the insertion loss. This procedure is discussed in detail in Section 4.6.

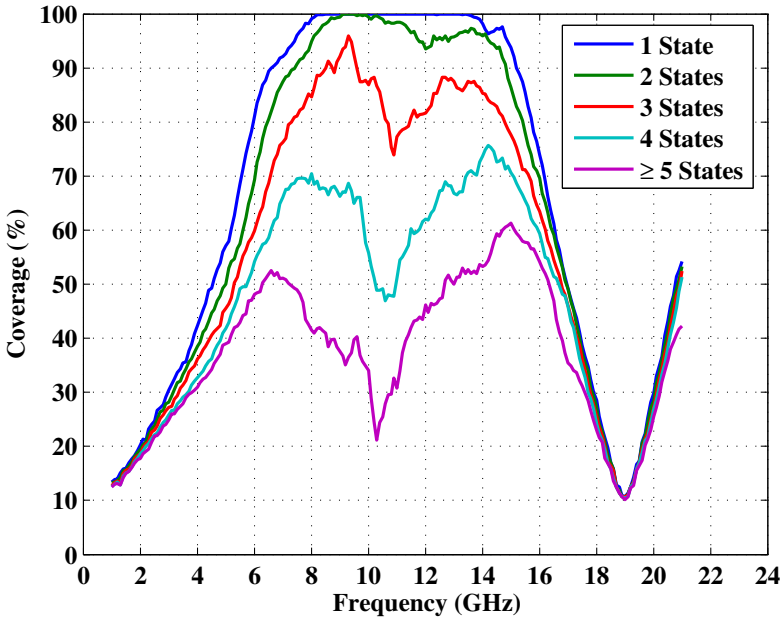
The coverage redundancy is also a means of determining whether the network has been sufficiently minimized for the given specifications. A perfectly minimized network would have complete coverage of the specified area to a particular SWR with minimal overlap between the regions.

Continuing to use the same network as an example, Figure 4.11 through Figure 4.15 show how the regions overlap each other, for each given SWR. The overlap is determined using the method described in Section 4.3, where points inside the Smith chart are counted each time they lie within an SWR circle, resulting in a total number of states which cover a particular impedances for each test point in the quantized Smith chart.

Figure 4.11(a) shows an overlap plot of SWR = 1.5 regions, with the color indicating the number of tuner states that cover a particular region. The highest color (red) indicates that the region is covered by 8 or more impedances. In Figure 4.11, the specified coverage region is covered entirely by at least two tuner states. This redundancy could be used to optimize for tuner loss, or may indicate that the tuner is not sufficiently optimized for this SWR. Figure 4.11(b) shows a frequency sweep of the coverage percentage. When this percentage is calculated, the area is limited to the area

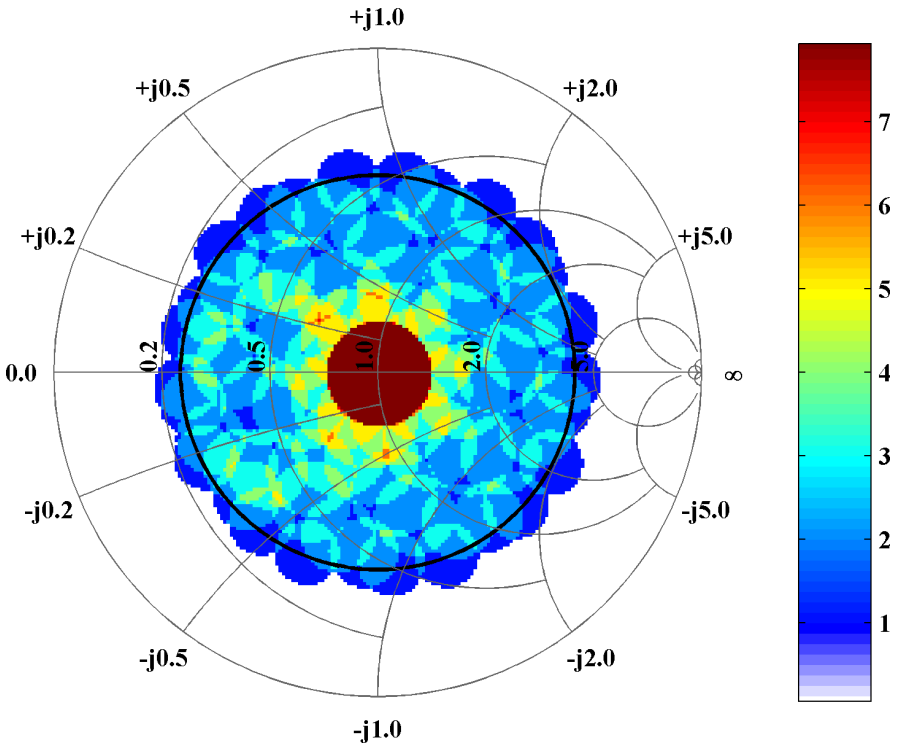


(a) Overlap regions at 10 GHz

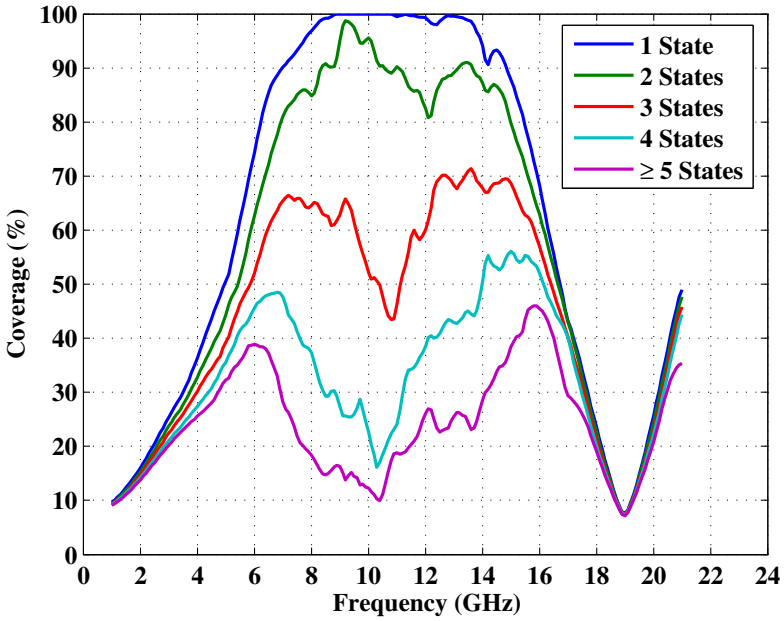


(b) Coverage Area vs. Frequency

Figure 4.11: Overlap of SWR = 1.5 regions at 10 GHz (a) and across the frequency range from 1–21 GHz (b). The number of states that cover a particular region of impedances is indicated by the color.

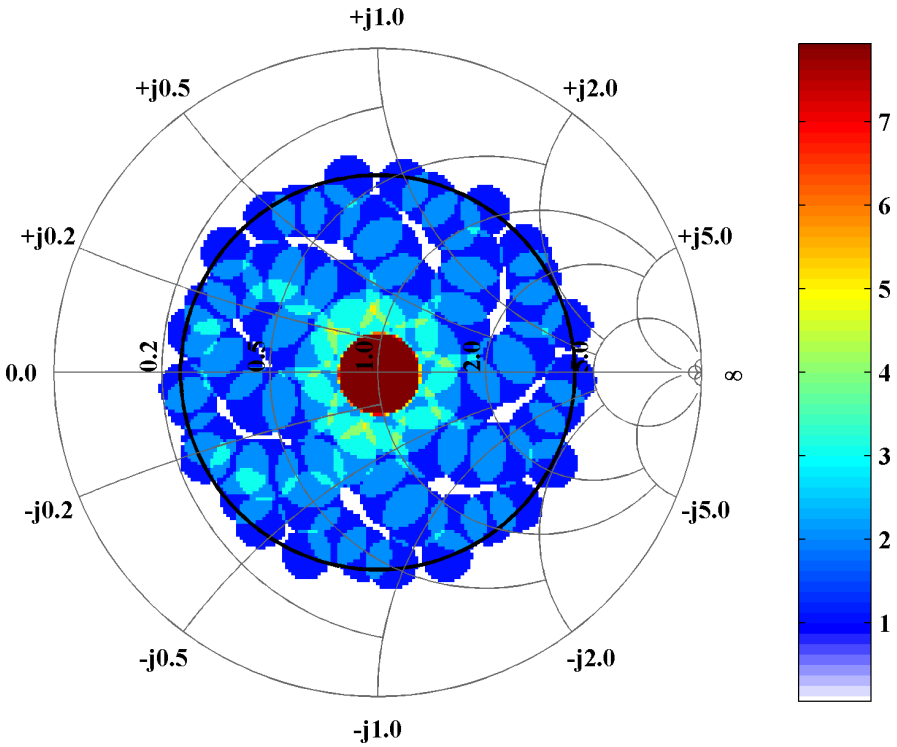


(a) Overlap regions at 10 GHz

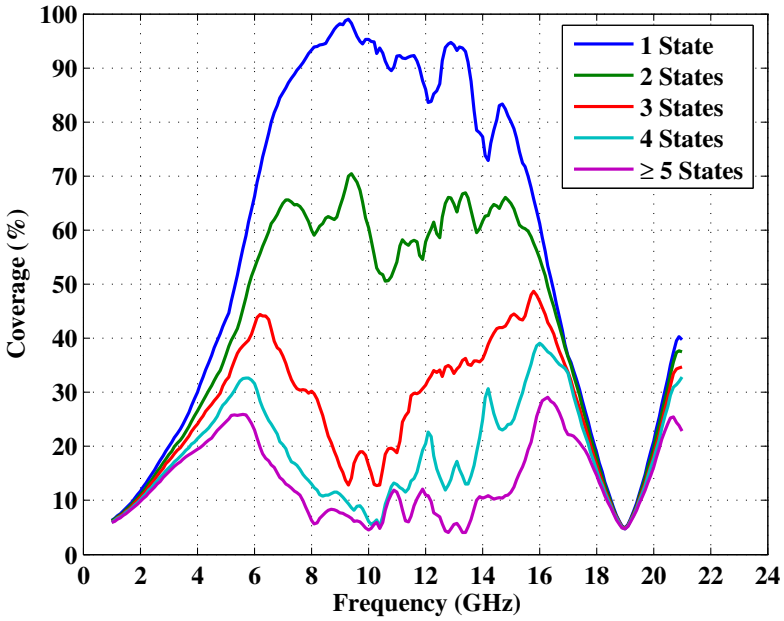


(b) Coverage Area vs. Frequency

Figure 4.12: Overlap of SWR = 1.4 regions at 10 GHz (a) and across the frequency range from 1–21 GHz (b). The number of states that cover a particular region of impedances is indicated by the color.

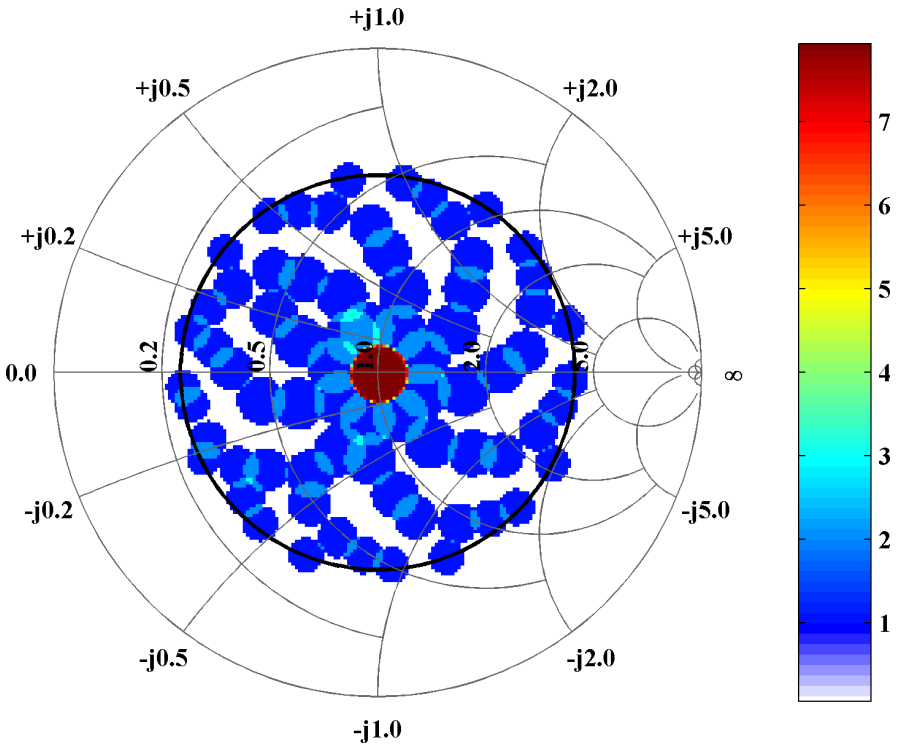


(a) Overlap regions at 10 GHz

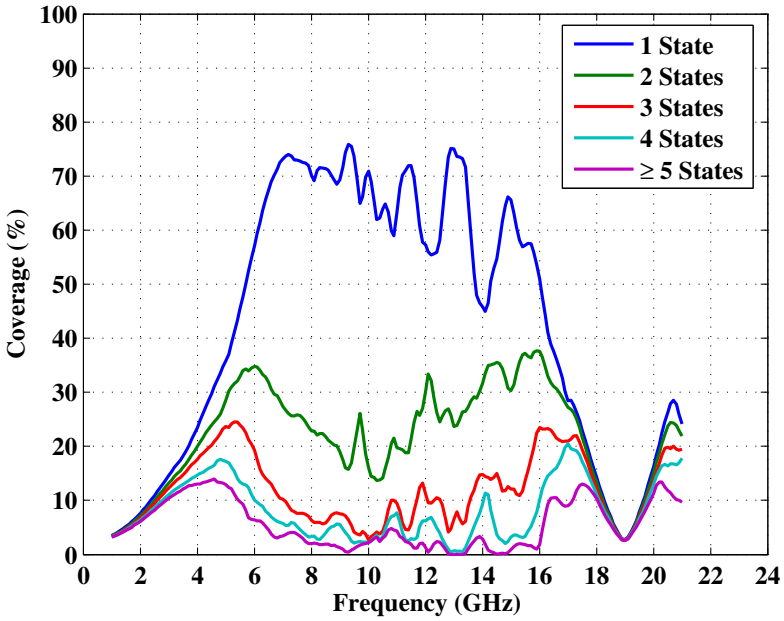


(b) Coverage Area vs. Frequency

Figure 4.13: Overlap of SWR = 1.3 regions at 10 GHz (a) and across the frequency range from 1–21 GHz (b). The number of states that cover a particular region of impedances is indicated by the color.

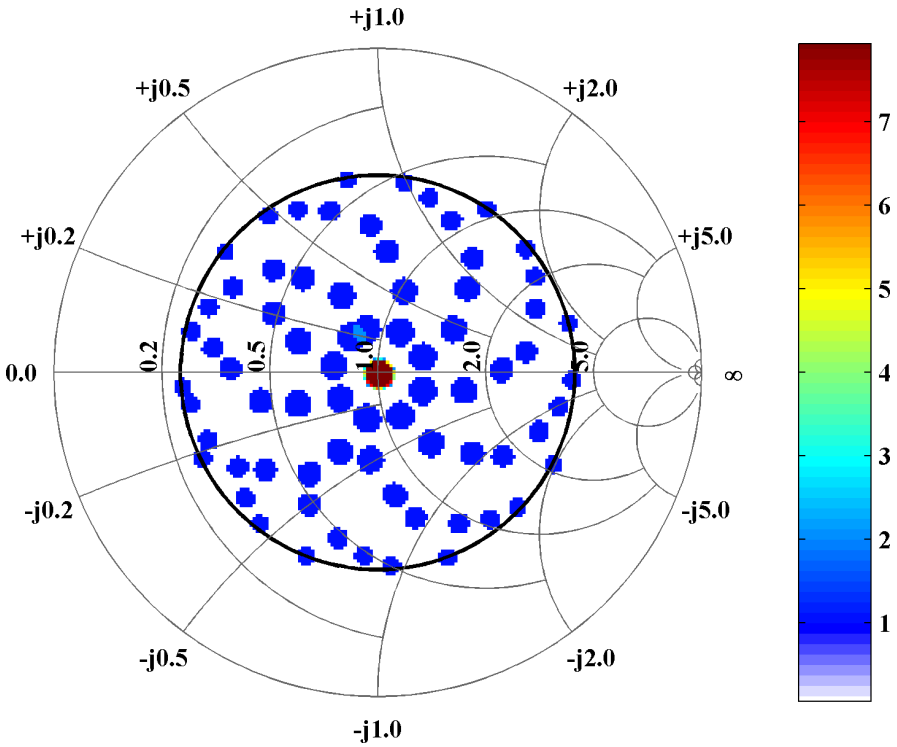


(a) Overlap regions at 10 GHz

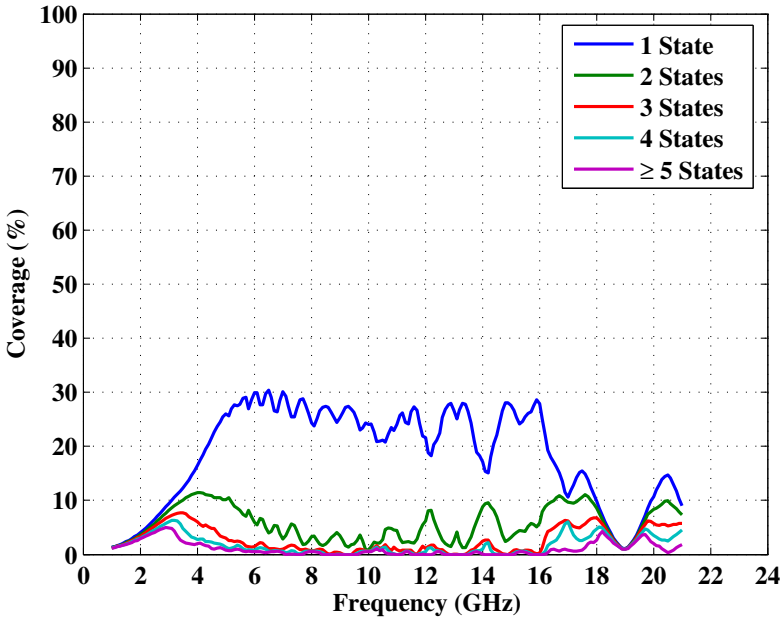


(b) Coverage Area vs. Frequency

Figure 4.14: Overlap of SWR = 1.2 regions at 10 GHz (a) and across the frequency range from 1–21 GHz (b). The number of states that cover a particular region of impedances is indicated by the color.



(a) Overlap regions at 10 GHz



(b) Coverage Area vs. Frequency

Figure 4.15: Overlap of SWR = 1.1 regions at 10 GHz (a) and across the frequency range from 1–21 GHz (b). The number of states that cover a particular region of impedances is indicated by the color.

within the circle indicated, as described in Section 4.3 and used in the coverage area analysis in Section 4.4. 85% of the area is covered by at least 3 states, 56% by 4 states, and 34% by at least 5 states.

A tuner that is optimized to minimize overlap will have 100% coverage at the specified SWR a single time for entire constellation, while all other multiple coverage curves would be minimized. Figure 4.11(b) shows this minimization notch occurring near 11 GHz. The design could be optimized to bring this notch to 10 GHz, but it is not likely that such design alterations would reduce the circuit size by more than 1 switch.

Figure 4.12 shows the overlap regions for SWR = 1.4. The tuner is better optimized for this SWR, with 95% of the area covered by at least 2 states, 51% covered by 3, and greater than 4 overlapping states are minimized. Figure 4.13 shows that the tuner is also well optimized for an SWR of 1.3 with 95% coverage at least once, 60% coverage by 2 states, and coverage by more than 3 states are minimized. Figures 4.14 and 4.15 show similar analysis for SWRs of 1.2 and 1.1, although the total coverage area is insufficient at these SWRs.

4.6 Performance Analysis #3: Output Power vs. SWR Mismatch and Tuner Loss

The critical parameter to all amplifier design is the output power delivered to the load (P_L). This parameter affects gain and PAE if input power is constant. Determining the output power of the combined amplifier-tuner network requires the mismatch between the required amplifier impedance, Z_{amp} and the impedance of the tuner state, $Z_{in,tuner}$, and the insertion loss of that state (from Figure 3.28).

In the case where the amplifier is matched to the nominal load (50 Ω) and a tuner is inserted into the network to correct for load variations, as shown in Figure 4.16, the 50 Ω point is located at the plane between the amplifier and the tuner. The tuner is able to correct for load variations according to its constellation. In this case, load variations

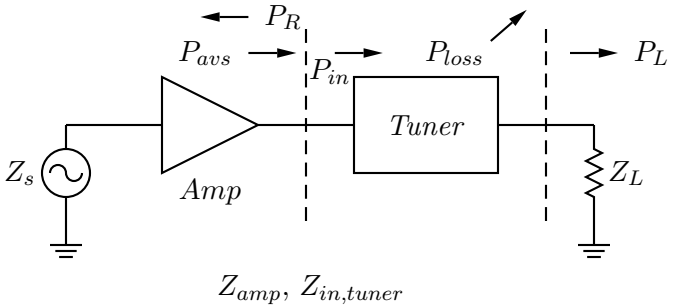


Figure 4.16: Power flow for total output power calculation in an amplifier-tuner combination.

up to an SWR of 4 ($|\Gamma|_L = 0.61$) can be re-matched to the amplifier. However, the amplifier will deliver a decreased power to the load due to the insertion loss of the tuner.

The size of the SWR regions is determined by load-pull contours. In essences, it will depend on the sensitivity of the amplifier match. If the amplifier is not sensitive to changes within a given SWR, then only the insertion loss of the tuner in a particular state is required. For completeness, however, the amplifier can be considered as a source. The nominal output power of this source, P_{avs} in Figure 4.16, must be reduced by the reflected power due to the residual mismatch between the source and the tuner, P_R. This determines the power inserted into the tuner network, P_{in}, which must then be reduced according to the insertion loss of the network, P_{loss}, in order to determine the final power delivered to the load, P_L.

A required metric for tuner performance is whether the output power after the residual mismatch and tuner loss is higher than the output power due to the mismatched load alone.

4.7 Performance Analysis #4: Failure and Degradation of the Constellation

The reliability of MEMS devices has long been an issue for this technology. It is beneficial to consider reliability in MEMS tuner design, such that the tuner will degrade gracefully as devices fail.

In Section 4.7.1, example constellations are shown as greater numbers of switches fail. Section 4.7.2 shows a statistical study of the failures.

4.7.1 Constellation Degradation

In order to generate constellations as the number of failures increases:

(1) it is necessary to assume that the switches will fail in either the open state or the closed state;

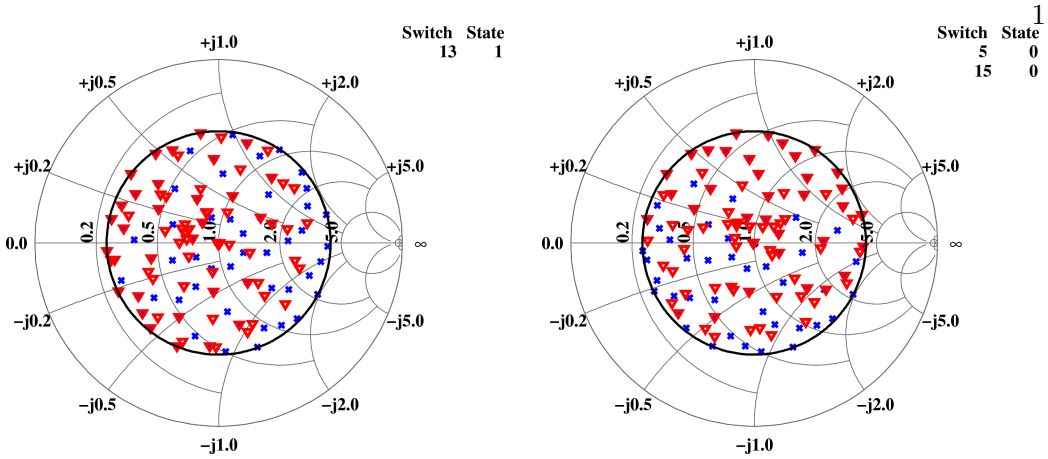
(2) the number of switch failures is specified;

(3) the location of the switch chosen at random;

(4) and the state of the failure is chosen at random.

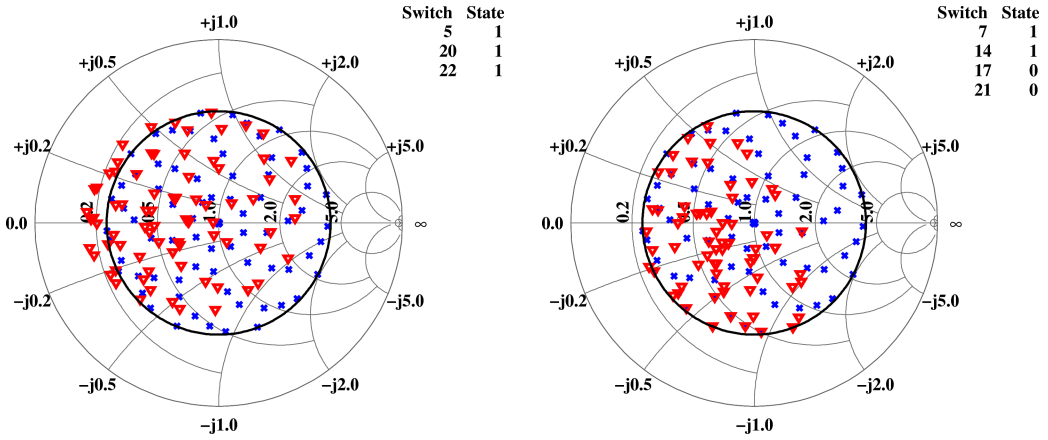
The new constellation is plotted with the red $\triangledown$ indicating the states of the tuner, while the original states are plotted by the blue x. The original range of the tuner, $|\Gamma|_{max} = 0.61$, is also indicated. The plots in Figure 4.17 are chosen at random from the large number of possible failure combinations for the purpose of illustration. The location of the switch that failed, and the state in which it failed are displayed in each plot.

Figure 4.17(a)–(c) show that with 1–3 switch failures, the constellation remains well dispersed through the specified area. At 4 failures, Figure 4.17(d), the constellation begins to show clustering, which would leave some regions uncovered. Another factor



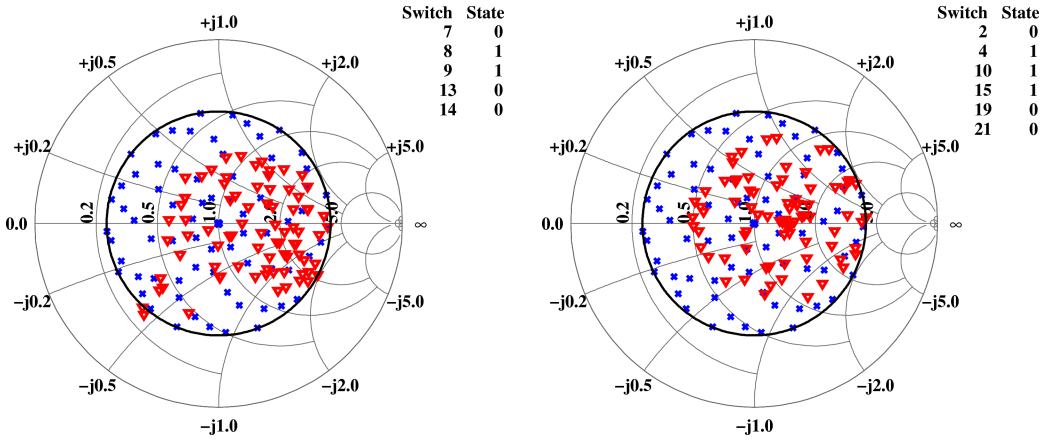
(a) 1 Failure

(b) 2 Failures



(c) 3 Failures

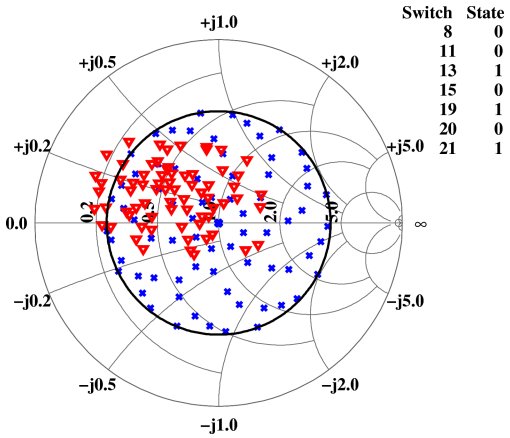
(d) 4 Failures



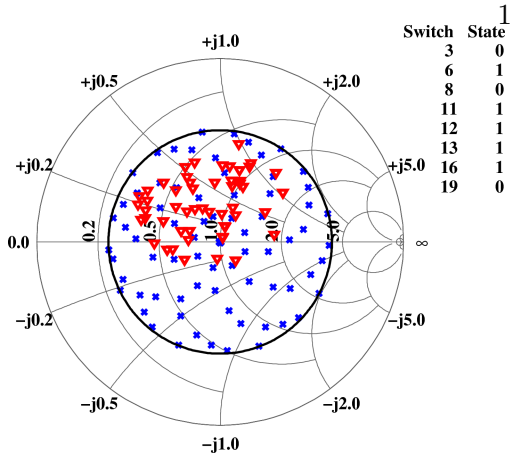
(e) 5 Failures

(f) 6 Failures

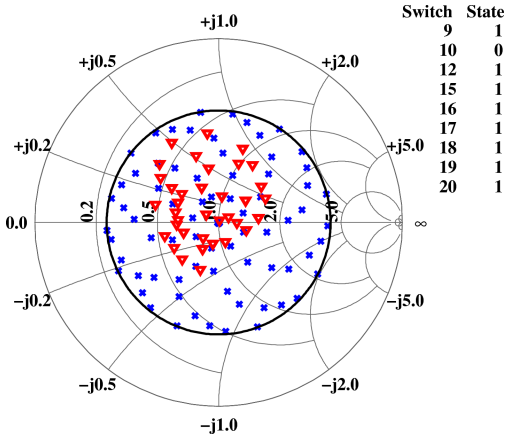
Figure 4.17: Failure constellations for 1–6 switch failures. Failure locations and states are chosen at random and indicated. The failure constellation is indicated by the red ▽. The original constellation is shown by the blue x and the specified coverage circle of $|\Gamma|_{max} = 0.61$ is indicated.



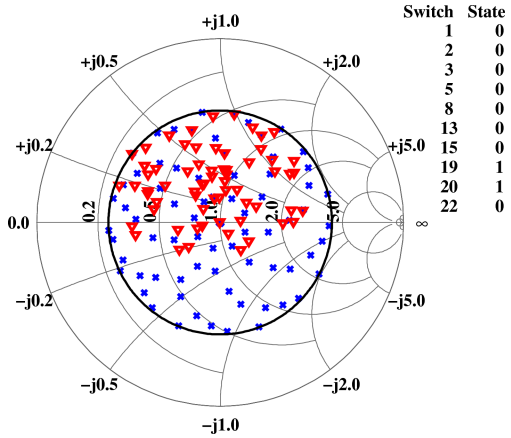
(g) 7 Failures



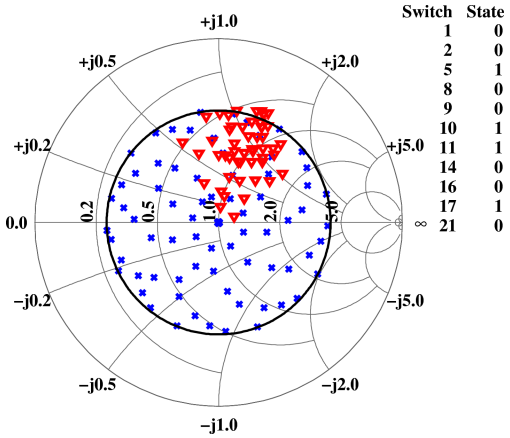
(h) 8 Failures



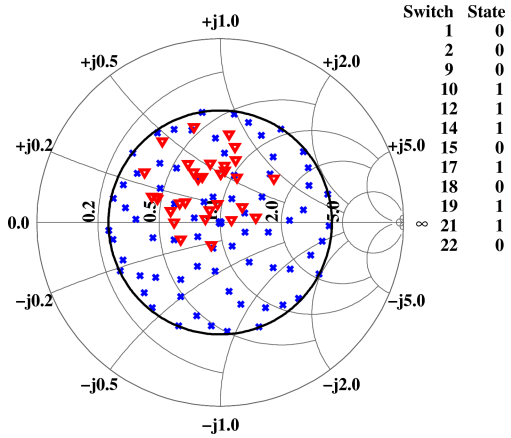
(i) 9 Failures



(j) 10 Failures

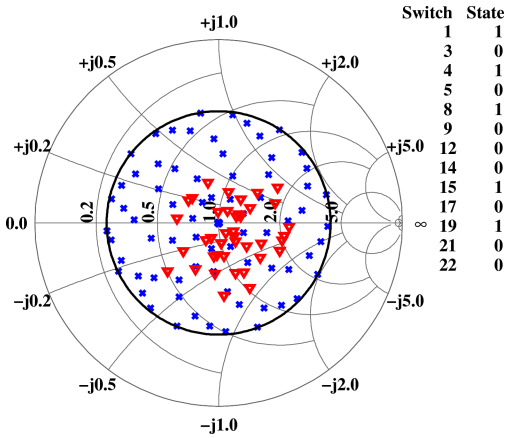


(k) 11 Failures

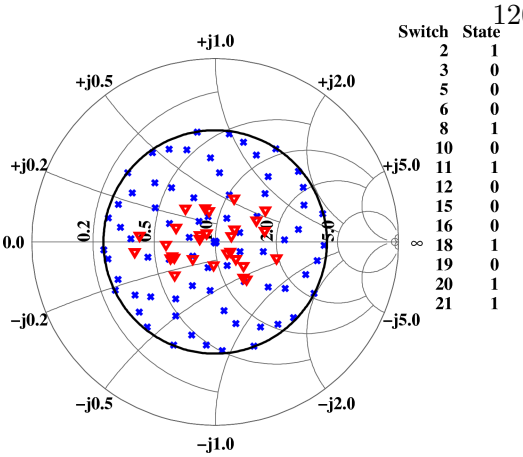


(l) 12 Failures

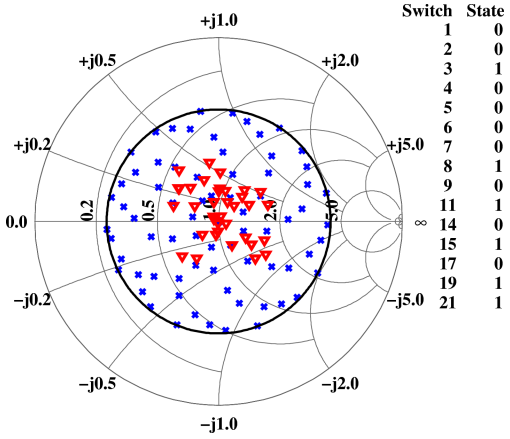
Figure 4.17: Failure constellations for 7–12 switch failures (cont.). Failure locations and states are chosen at random and indicated. The failure constellation is indicated by the red ▽. The original constellation is shown by the blue x and the specified coverage circle of $|\Gamma|_{max} = 0.61$ is indicated.



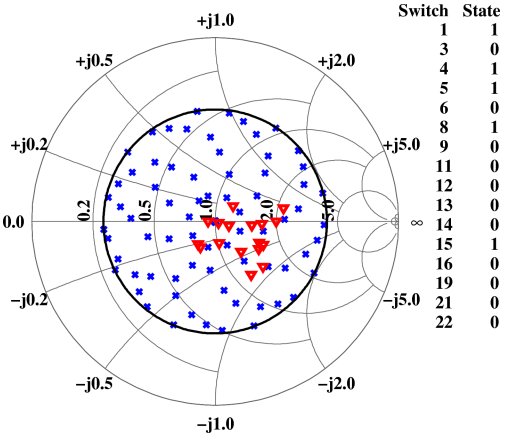
(m) 13 Failures



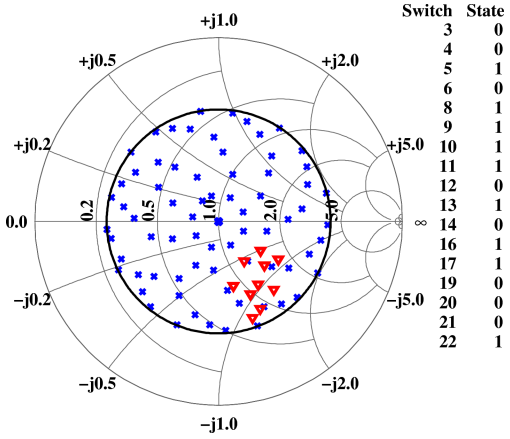
(n) 14 Failures



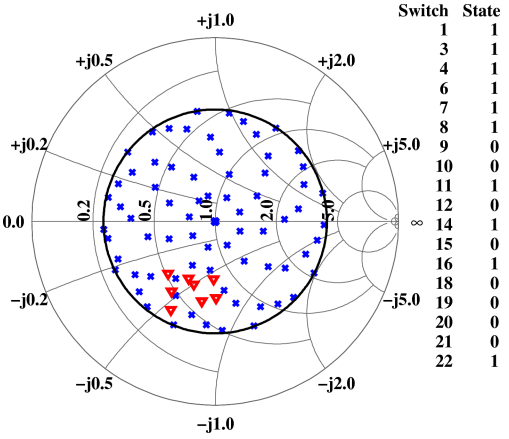
(o) 15 Failures



(p) 16 Failures

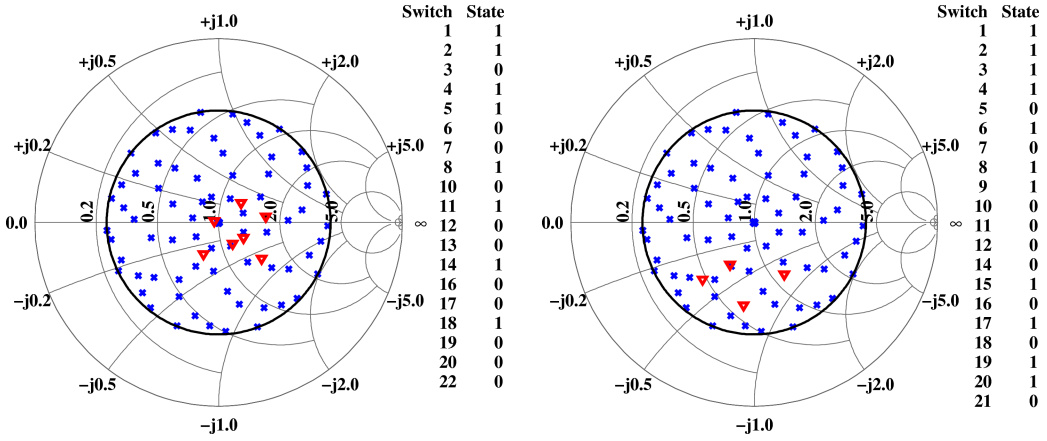


(q) 17 Failures



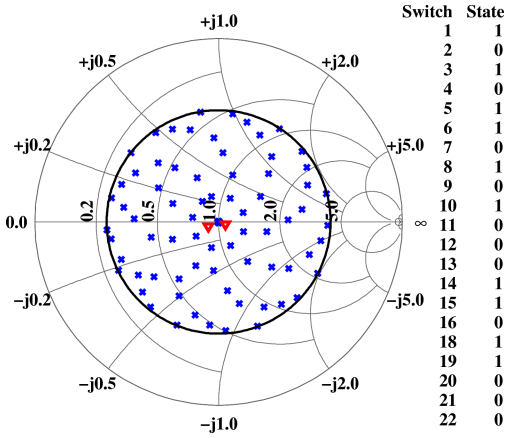
(r) 18 Failures

Figure 4.17: Failure constellations for 13–18 switch failures (cont.). Failure locations and states are chosen at random and indicated. The failure constellation is indicated by the red ▽. The original constellation is shown by the blue x and the specified coverage circle of $|\Gamma|_{max} = 0.61$ is indicated.

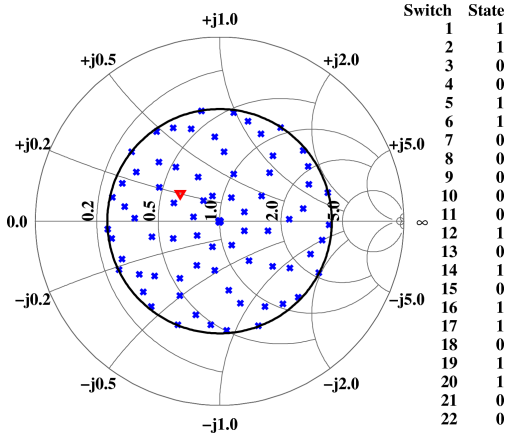


(s) 19 Failures

(t) 20 Failures



(u) 21 Failures



(v) 22 Failures

Figure 4.17: Failure constellations for 19–22 switch failures (cont.). Failure locations and states are chosen at random and indicated. The failure constellation is indicated by the red ▽. The original constellation is shown by the blue x and the specified coverage circle of $|\Gamma|_{max} = 0.61$ is indicated.

is that switch failures mean that the tuner is not capable of producing as many states, which further reduces the size of the constellation.

The failing tuner is able to cover approximately 50% of the area up to approximately 10 failures, Figure 4.17(j). Figure 4.17(k)–(o) show approximately 25% coverage for 11–15 failures. Above 16 failures, Figure 4.17(p)–(v), the tuner produces very few states and extremely limited coverage.

These constellations were chosen at random for the purpose of illustration the constellation changes, however, failure may be more exhaustively studied through a statistical analysis, presented in Section 4.7.2.

4.7.2 Statistical Failure Analysis

To statistically analyze the failure of the tuner, the process described in Section 4.7.1 is repeated, and the percent coverage area is calculated for each failed constellation:

(1) it is necessary to assume that the switches will fail in either the open state or the closed state to simplify the analysis, though in general this is not necessarily true;

(2) the number of switch failures is specified;

(3) the location of the switch chosen at random;

(4) the state of the failure is chosen at random;

(5) and the tuner is then analyzed for percent coverage area as in Section 4.4.

One item of interest is whether there is any difference between failures in the open state and failures in the closed state. From a loss perspective, it is desirable to have switches fail in the open state, since the unit cell in the open state has lower loss than the unit cell in the closed state. To determine the effect of the fail state on the coverage

area, the color of the scatter point in Figure 4.18 represents the number of switches that failed in the closed position. 100 tests are performed on each specified number for switch failures. The average coverage area of all tests is indicated by the red line.

To determine the statistical significance of the data, a box-and-whisker plot is shown in Figure 4.19. The horizontal red bar indicates the median of the data, and the box extents show the upper and lower quartiles. The average line from Figure 4.18 is also shown. The median and average values of the data are close in all fail cases.

Although Figures 4.18 and 4.19 show that the coverage area decreases as the number of failures increases (consistent with the constellation findings from Section 4.7.1), it is inconclusive how the number of switches which fail in the closed position affects the coverage area. Another analysis is run, where instead of choosing the fail state at random, the fail state is always set to open. This scatter plot is shown in Figure 4.20, and the box-and-whisker plot is shown in Figure 4.21. Similarly, another test is run where the switches are set to always fail in the closed state, shown in Figures 4.22 and 4.23.

These results are combined in Figure 4.24 to show the random failures from Figure 4.22 in black, the failures all in the open state from Figure 4.22 in blue, and the failures all in the closed state from Figure 4.22 in red. Note that the scatter points are offset slightly for clarity. From the corresponding average lines, it is evident that there is a weak correlation between the number of failures in the closed state to decreased coverage area, though the large standard deviation of these tests indicate that this is not independent of location.

These figures suggest that up to 4 failures, the tuner performs reasonably well, with coverage averaging above 90%. At 4 failures, the lower quartile is at 85% coverage, the upper quartile is at 95% coverage, with median and average values at approximately 90%. This point could be considered the break point where further failures are no longer able to consistently cover the specified area.

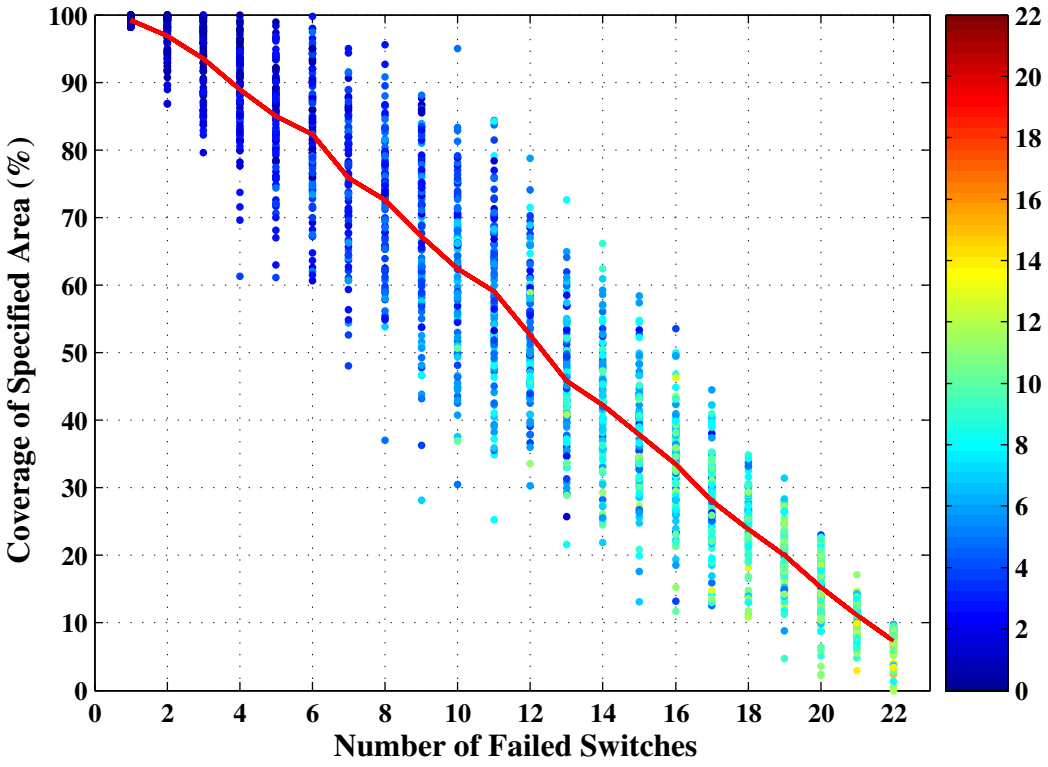


Figure 4.18: Degradation of the coverage area as switch failures increase. The failure locations and fail states are chosen at random. The number of switches that failed in the closed state are indicated by the color of the point. For each specified number of switch failures, 100 test cases are run. The average coverage area is indicated by the red line.

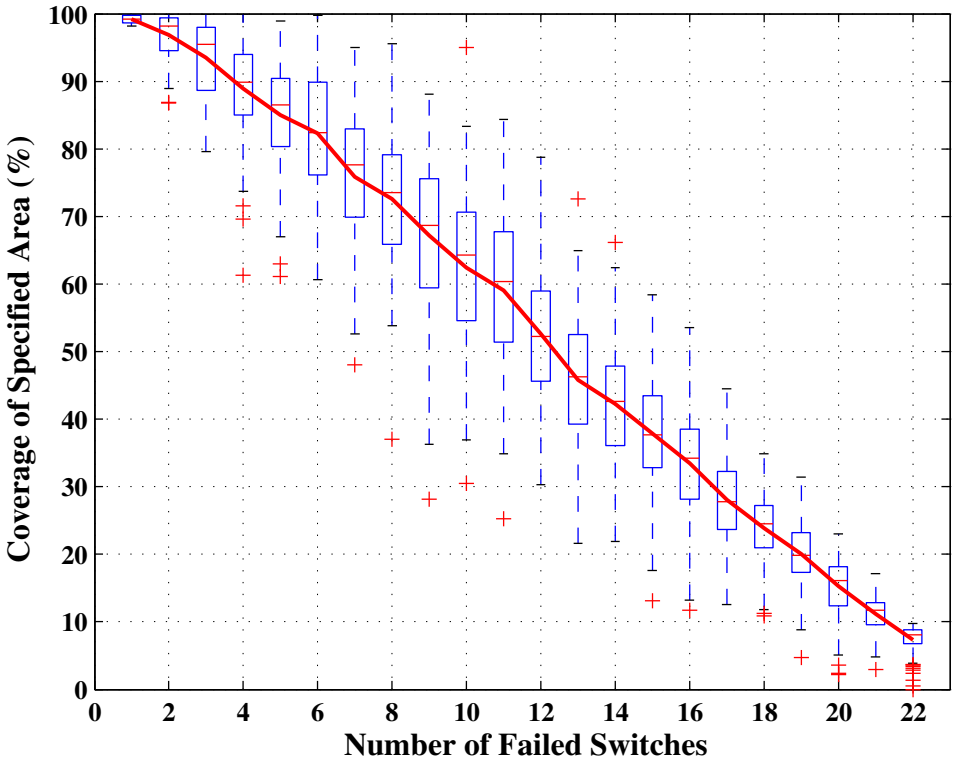


Figure 4.19: Box and whisker plot showing the degradation of the coverage area as switch failures increase. Switch locations and fail states are chosen at random, for 100 tests per specified number of switch failures. The horizontal red bar indicates the median of the data, and the box extents show the upper and lower quartiles. The average line from Figure 4.18 is also shown. The median and average values of the data are close in all cases.

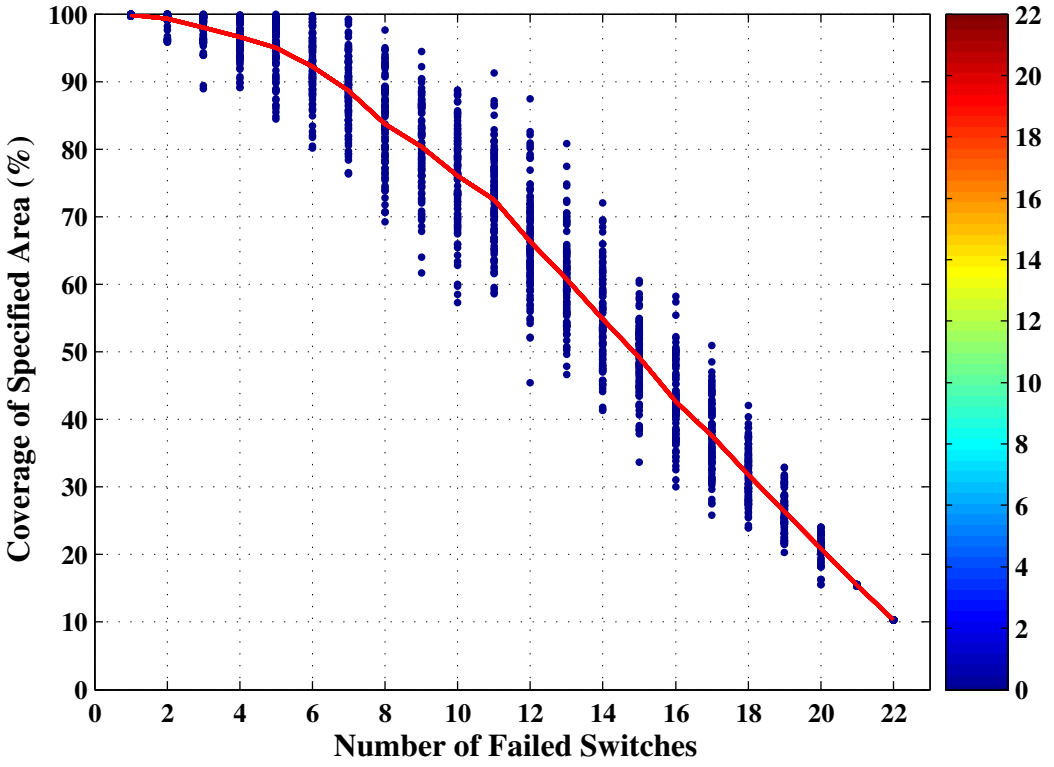


Figure 4.20: Degradation of the coverage area as switch failures increase. The failure locations are chosen at random, but the fail state is always open. The number of switches that failed in the closed state are indicated by the color of the point as in Figure 4.18, which are all 0 in this case. For each specified number of switch failures, 100 test cases are run. The average coverage area is indicated by the red line.

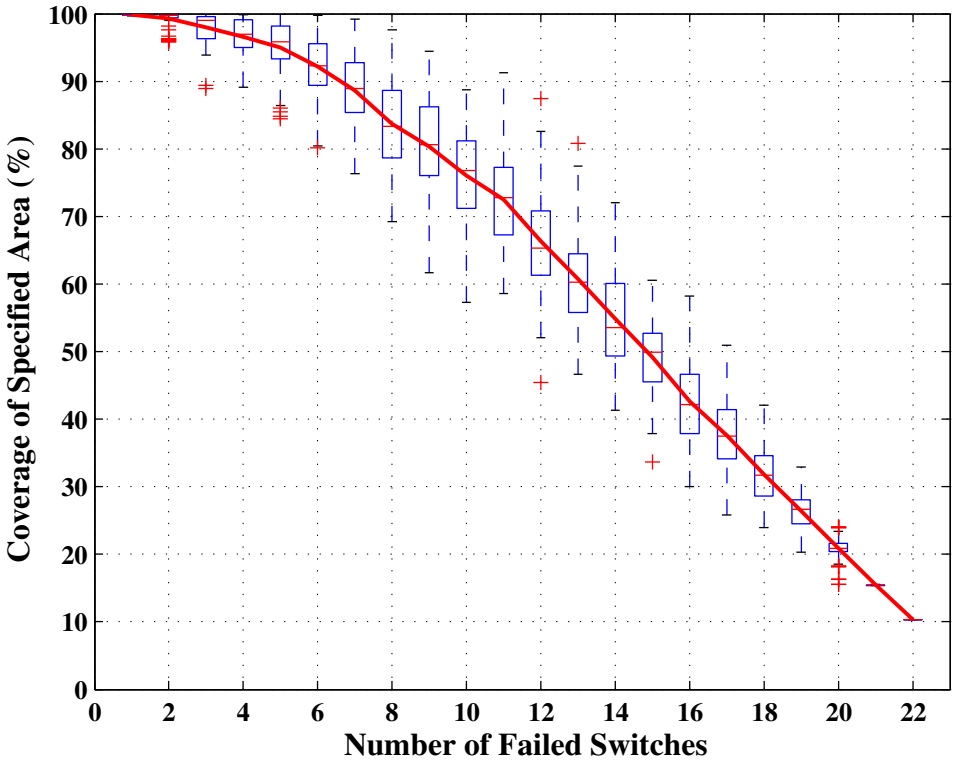


Figure 4.21: Box and whisker plot showing the degradation of the coverage area as switch failures increase. Switch locations are chosen at random for 100 tests per specified number of switch failures, but the fail state is always open. The horizontal red bar indicated the median of the data, and the box extents show the upper and lower quartiles. The average line from Figure 4.20 is also shown. The median and average values of the data are close in all cases.

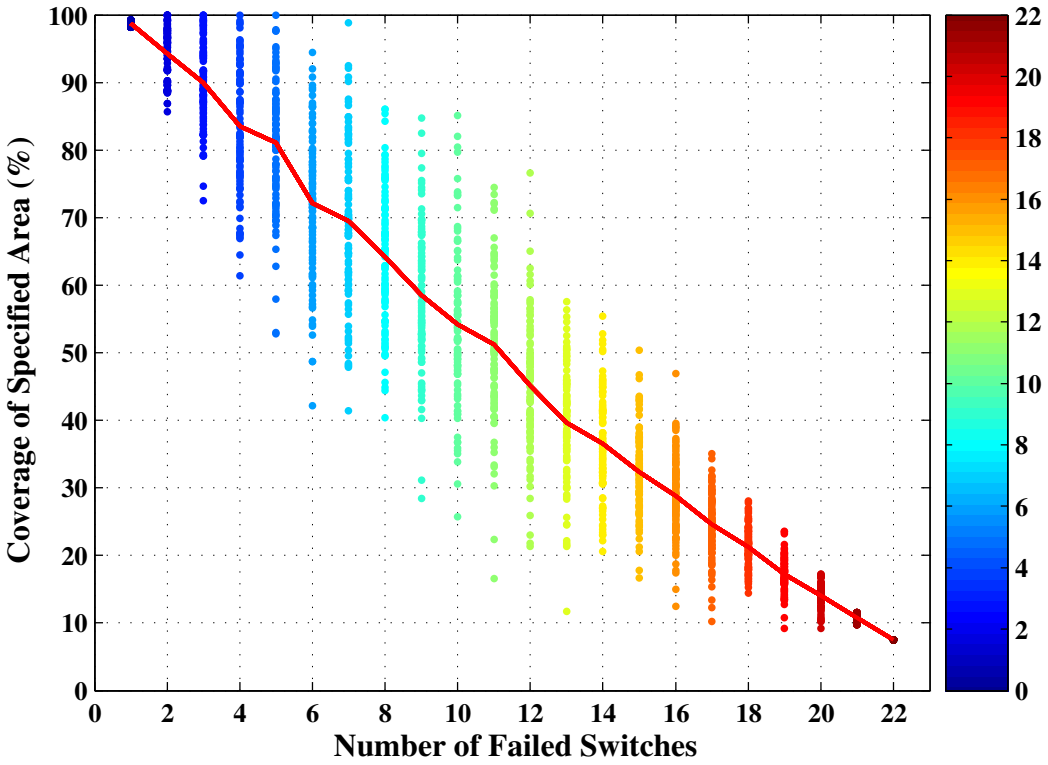


Figure 4.22: Degradation of the coverage area as switch failures increase. The failure locations are chosen at random, but the fail state is always closed. The number of switches that failed in the closed state are indicated by the color of the point as in Figure 4.18, which in this case equals the number of switches allowed to fail. For each specified number of switch failures, 100 test cases are run. The average coverage area is indicated by the red line.

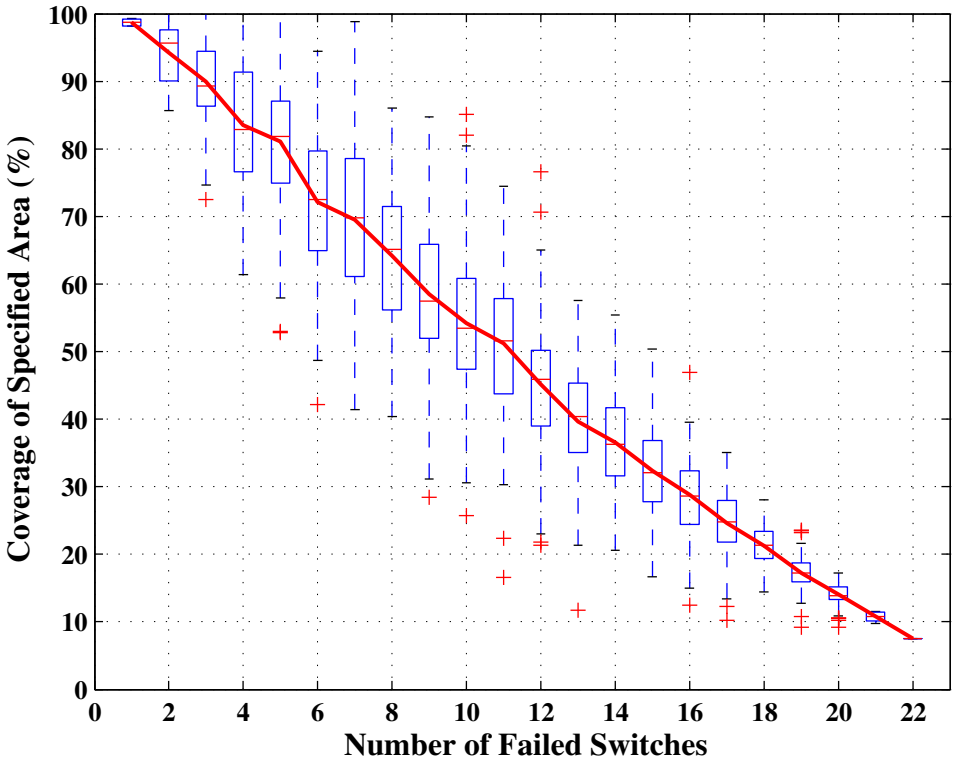


Figure 4.23: Box and whisker plot showing the degradation of the coverage area as switch failures increase. Switch locations are chosen at random for 100 tests per specified number of switch failures, but the fail state is always closed. The horizontal red bar indicated the median of the data, and the box extents show the upper and lower quartiles. The average line from Figure 4.22 is also shown. The median and average values of the data are close in all cases.

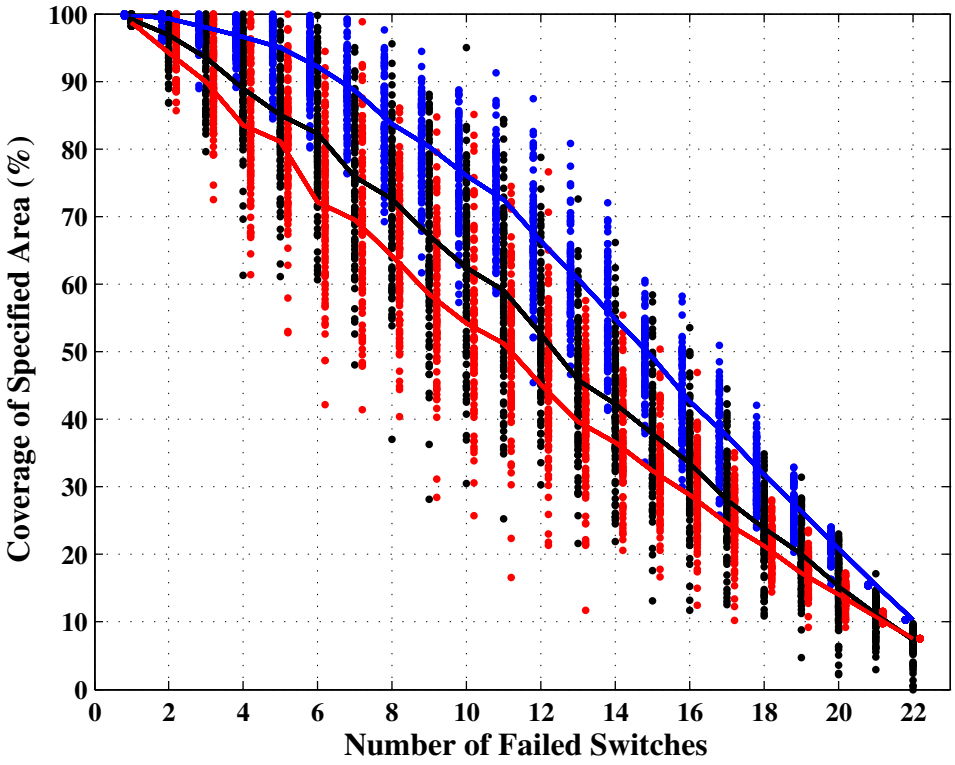
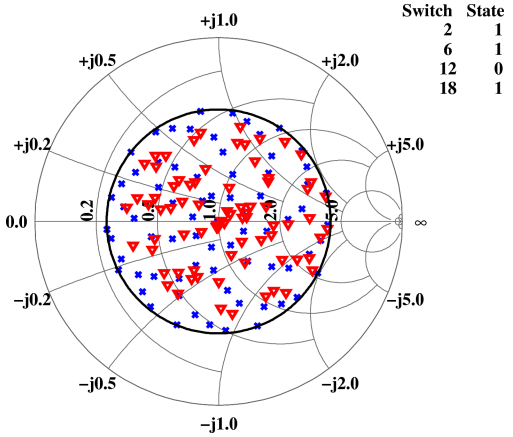
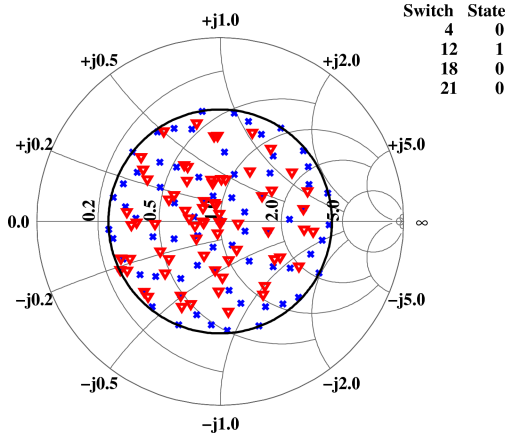


Figure 4.24: A combination of random failures (Figure 4.22 - black), failures all in the open state (Figure 4.22 - blue) and failures all in the closed state (Figure 4.22 - red). The averages are indicated in the corresponding color. Note that the scatter points are offset slightly for clarity. There is a weak correlation between failure state and coverage area, indicating that failures in the open state are less significant than failures in the closed state. However, the dependence of coverage area on fail state is not independent of failure location, as indicated by the large standard deviation in each scatter plot.

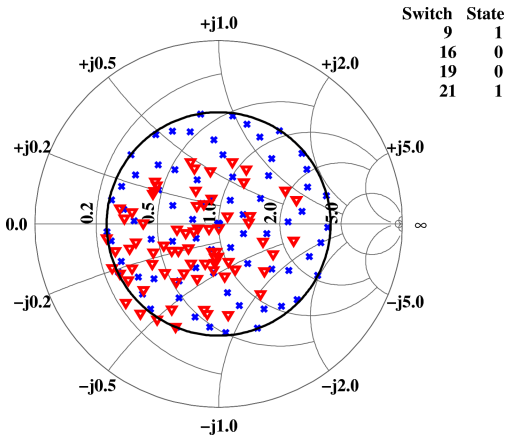
A few examples of failure constellations that represent good, moderate, and poor coverage at 4 failures are shown in Figure 4.25.



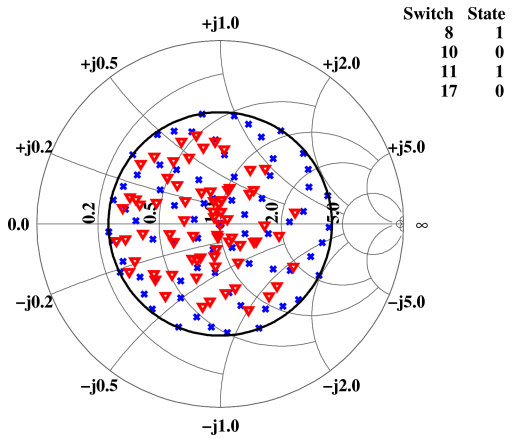
(a) 4 Failures, Good Coverage



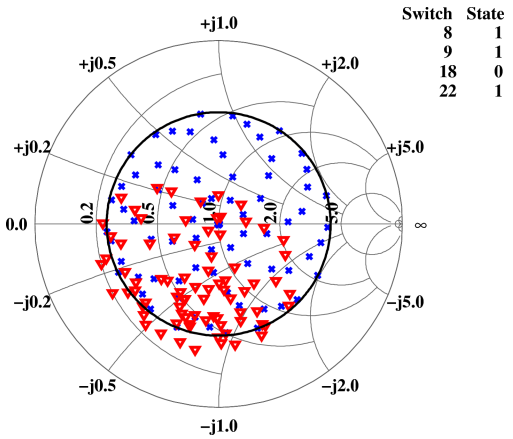
(b) 4 Failures, Good Coverage



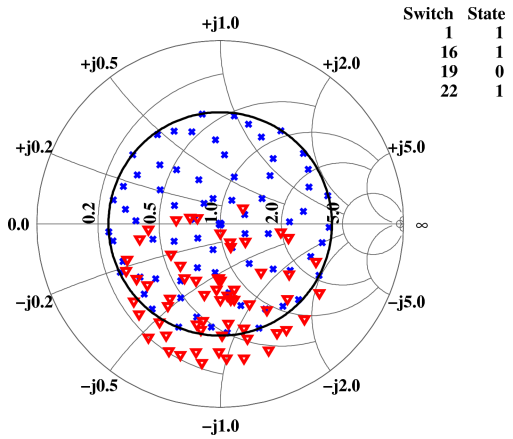
(c) 4 Failures, Moderate Coverage



(d) 4 Failures, Moderate Coverage



(e) 4 Failures, Poor Coverage



(f) 4 Failures, Poor Coverage

Figure 4.25: Example failure constellations for 4 failures, showing that it is possible to have good, moderate or poor coverage at 4 failures, depending on the location of the failures and the fail states.

Chapter 5

Surface Micromachined Flip-Chip Assembled Inductor

As the complexity of amplifiers increases to include multiple and multi-functional, the size of the biasing components becomes increasingly critical to integration. Ideally, the RF choke in the bias circuitry would be an inductor, passing low-frequency and DC components while presenting a high impedance to the RF. Limitations in quality factor, current handling, and inductance often prohibit the use of lumped inductors in microwave hybrid-circuit applications at frequencies above C-band. However, monolithic inductors are commonly used in applications up to K-band.

The goal of this work is to bridge the gap between surface mount and monolithic inductor performance. The inductors presented here are micromachined on an inexpensive host substrate using lithographic techniques and then transferred to a high-quality microwave substrate via a low-temperature flip-chip assembly process. The result is a lumped inductor hybrid circuit with performance characteristics comparable to those of monolithic inductors. A rendered image of final assembled structure is shown in Figure 5.1. This work builds on the rectangular flip-chip inductor developed at the University of Colorado at Boulder [70, 71] to test different inductor geometries, optimized for microwave performance.

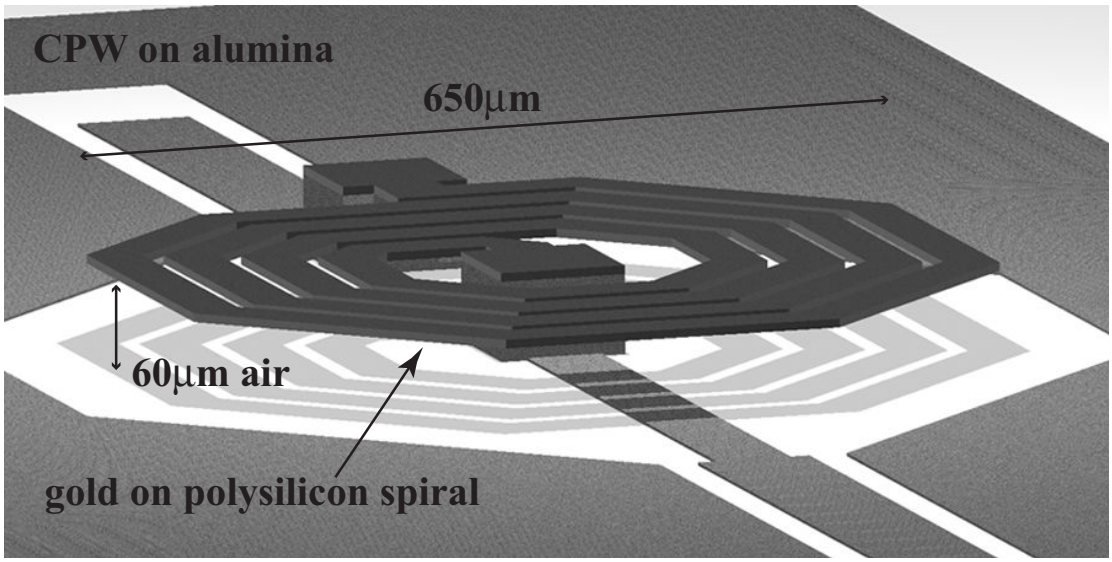


Figure 5.1: A rendering of a micromachined inductor after completion of the release and flip-chip assembly in a CPW 50-Ω test line. The inductor is suspended 60 μm above the microwave substrate on gold posts (100 μm·100 μm).

5.1 Background

Substrate effects are the dominant limitation of planar inductors on both high-resistivity substrates like GaAs and low-resistivity CMOS-grade silicon. Resistive losses degrade the quality factor. High substrate permittivity increases the parasitic capacitance, which reduces the self-resonant frequency.

These issues have been addressed in the past by fabricating the inductor on low-K dielectrics, such as polyimide [72–74] or benzocyclobutene (BCB) [75, 76]. With these methods, resonant frequencies between 12 and 14 GHz for inductances around 2 nH and quality factors between 30 and 50 have been demonstrated [72].

Another option is to bulk etch the substrate surrounding the inductor, suspending the inductor structure in air. First demonstrated on silicon in [77], substrate removal increased the resonant frequency from 800 MHz to 3 GHz. Similarly on bulk-etched GaAs [78], substrate removal increased the resonant frequency of a 5-nH inductor from 10 to 17 GHz with an increase in quality factor from 11.5 to 18.9. A third method utilizes microelectromechanical system (MEMS) fabrication techniques to create air-suspended inductors without bulk substrate etching. Stacked planar microstructures may be built using either photoresist [79, 80] or polyimide [81] as sacrificial layers. The surface micromachining approach in [79] demonstrates a 2.7-nH inductor with a self-resonant frequency of 15 GHz and a Q-factor of 40.

5.2 Goals of This Work

This work aims to bridge the performance gap between surface mount and monolithic inductors. The inductor coil is surface micromachined on a silicon host substrate in the same ways as monolithic inductors are fabricated. Integrated with this inductor is a tethered assembly mechanism [82] which allows flip-clip transfer of the inductor from the silicon substrate to a more suitable microwave substrate. This assembly process is

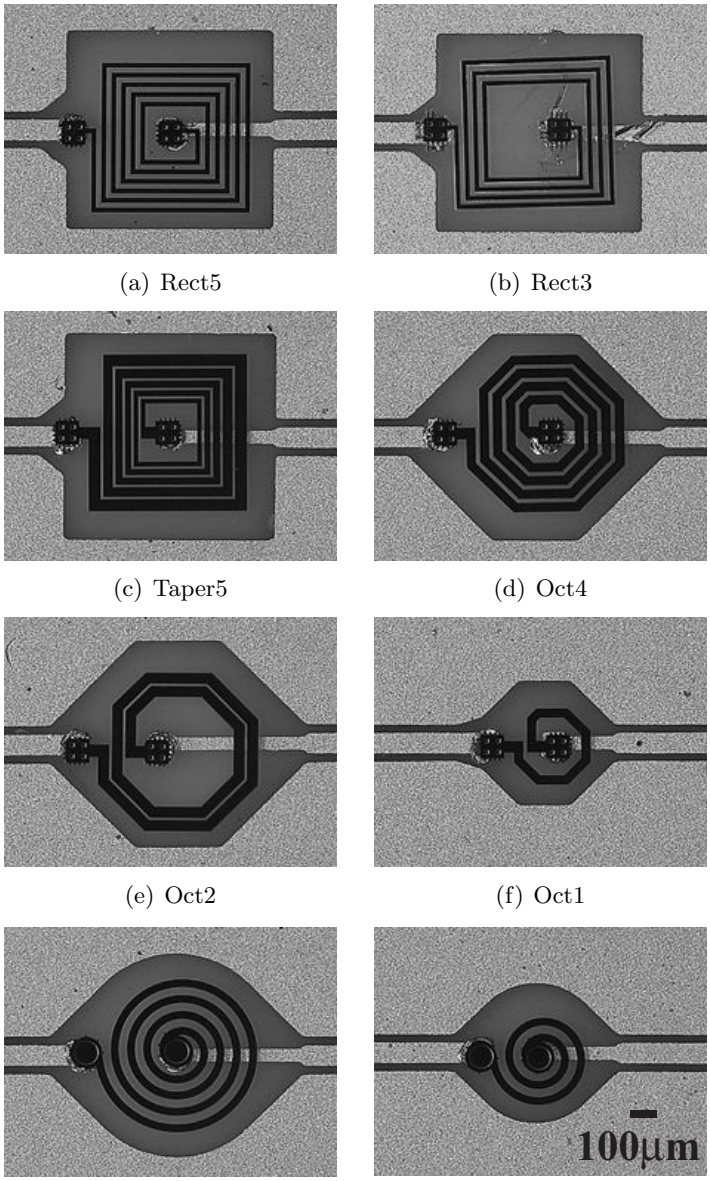
compatible with other surface mount methods allowing integration of a monolithic-like inductor in a hybrid circuit for the first time. No surface or bulk etching is required on the microwave substrate.

These inductors are designed using standard design formulas for monolithic inductors available in the literature. The inductance values range from 0.65–16 nH, with self-resonant frequencies from 5–35 GHz and quality factors from 45–100. Standard inductor shapes (rectangular, octagonal, circular, and rectangular tapered), shown in Figure 5.2, are used to demonstrate the flexibility of this assembly technique. The inductor labels in Figure 5.2 are used throughout this paper in reference to each particular inductor type.

Circuit applications are also demonstrated in this work. In [71], the inductor type shown in Figure 5.2(a) (Rect5) was demonstrated as a high-impedance RF choke in a miniaturized bias-tee. The impedance of these inductors remains high well beyond the self-resonant frequency (over 100 Ω from 1–15 GHz), extending the bandwidth of a bias-tee network. Below the resonant frequency, the inductors can be used as high-quality lumped elements. An example is a miniaturized Wilkinson divider at 1.72 GHz [83] with a footprint of 0.96 cm^2.

5.3 Design

Design of flip-chip micromachined inductors begins with selection of silicon surface micromachining process layers, which must provide adequate structural support and low conductor losses. After selection of the metalization layers, the geometry of the planar coil is chosen for desired values of inductance and resonant frequency. Equations based on geometric considerations accurately predict the inductance, however, full-wave simulations are required for accurate determination of the self-resonant frequency.



(a) Rect5 (b) Rect3

(c) Taper5 (d) Oct4

(e) Oct2 (f) Oct1

(g) Circ4 (h) Circ2

Figure 5.2: Photographs of the flip-chip assembled suspended inductors. This assembly technique was tested for several geometries, including a 5.5-turn rectangular (a) and an open-center 3.5-turn rectangular (b), a 5-turn tapered rectangular (c), 4- 2- and 1-turn octagonal (d), (e) and (f), and 4- and 2-turn circular inductors (g) and (h). The labels in this figure will be used throughout this paper in reference to a specific geometry. The coplanar waveguide lines have $90\,\mu$m signal line and $30\,\mu$m slot widths for $50\,\Omega$ on an alumina substrate ($\epsilon_r = 9.8$).

5.3.1 Micromaching and Mechanical Considerations

Early experimentation with 2-μm thick solid gold suspended inductors was unsuccessful [70]. The highly malleable gold structure does not provide adequate structural support, since the diameter-to-thickness aspect ratio is large for useful inductor values (about 100:1). This problem is addressed using a multilayer structure of polysilicon and trapped silicon dioxide to provide additional stiffness. The worst-case sagging at the extreme edges is less than a single turn thickness (2 μm) due to internal stress, simulated using finite-element analysis (Coventorware). The advantage of a multilayer structure comes at the cost of a coefficient of thermal expansion (CTE) mismatch. A detailed thermal analysis of released gold/polysilicon structures is given in [84]. Tests from 25°C to 120°C show little variation in the electrical properties of the inductors presented in this work.

A polysilicon surface micromachining multi-user MEMS process (PolyMUMPs) foundry service is commercially available through the MEMSCAP Corporation. This process has three available polysilicon deposition layers with intermediate phosphosilicate glass (PSG) layers and a thin gold metal layer. These micromachining layers are deposited through low-pressure chemical vapor deposition (LPCVD) on a 100 mm n-type (100) silicon wafer with 1–2 Ω-cm resistivity, which is then heavily doped with phosphorous through diffusion. Following deposition of the polysilicon layers and a PSG hard mask, the wafer is annealed at 1050°C for 1 hour, which dopes the silicon with phosphorous from the PSG and significantly reduces the net stress in the layer. Deposition of a 0.5 μm layer of gold completes the fabricate process in the MUMPs foundry [85]. The process layers used in these inductors are 2.0 μm of polysilicon (POLY1), 0.75 μm of PSG oxide (OXIDE2), 1.5 μm of polysilicon (POLY2), and 0.5 μm of gold (METAL).

MUMPs is intended to be a self-contained MEMS process, however, the low resistivity of the silicon wafer is unsuitable for microwave circuits and components, and

the gold metalization is thinner than a skin depth up to 25 GHz. These issues are addressed by a maskless electroplating process, plating 2 μm of additional gold (shown in the ELECTRO layer of Figure 5.3), and removing the silicon substrate. Substrate removal is accomplished by designing the entire inductor structure above the first PSG oxide layer. A timed hydrofluoric acid (49% HF) pre-release step then dissolves the sacrificial PSG oxide and suspends the inductor in air.

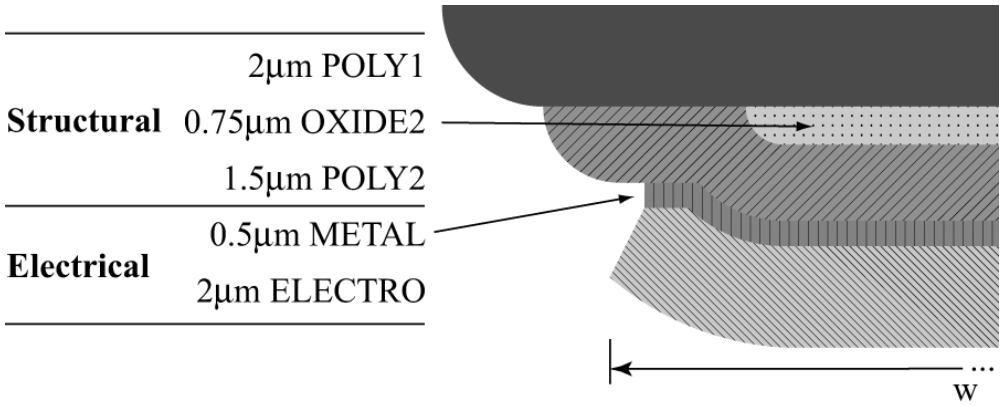


Figure 5.3: The cross-section of the edge of one turn in the inductor coil, showing the PolyMUMPs micromachining layers [85], which are inverted after flip-chip bonding. The vertical dimension is to scale. The turn width w is much larger than the total thickness (24–40 μm).

Tethering structures around the inductor bond pads anchor the suspended pre-released inductor structure to the silicon wafer. A flip-chip thermo-compression bonding process bonds the pads on the top electroplated gold layer to pedestals on a receiving microwave substrate. The compression force of this flip-chip process breaks the tethering structure at predefined points, releasing the inductor from the silicon entirely. The pedestals support the inductor structure 60 μm above the microwave substrate.

Realizing the inductor diameter-to-metal thickness aspect ratio is quite large (about 100:1 for the largest inductors), two polysilicon layers with a trapped oxide layer are used for structural support. The 2 μm POLY1 and 1.5 μm POLY2 layers are anchored together through 2 μm-wide perimeter around the inductor coil. These an-

chors through the second PSG oxide layer trap a 0.75 μm layer of PSG, which is not exposed during the HF pre-release. This polysilicon-trapped oxide layers provide mechanical stiffness to the inductor, while the 2.5 μm thick metal layer provides a low-loss conduction path for microwave signals. Sagging at the extreme edges of the inductor structure is negligible. One disadvantage of this multilayer stacking is the difference in the coefficients of thermal expansion (CTE), which will cause warpage as temperature varies. A detailed thermal analysis of released gold/polysilicon MUMPs structures is given in [84]. An optimal foundry process would provide thick metal layers with less CTE mismatch between the layers, providing both stiffness and allow a wider range of operating temperatures. Tests from 25°C to 120°C show little variation in the electrical properties of the inductors presented in this work.

5.3.2 Electrical Considerations

Electrical design of the inductors can be divided into three categories: the inductance of the coil, the series resistance of the coil, and the design of the coplanar waveguide test circuit for each inductor type.

5.3.2.1 Inductance

The inductance of a planar coil is dependent on: the total number of turns n, turn width w, turn spacing s, outer diameter D_o, inner diameter D_i, and the geometry of the spiral, as shown in Figure 5.4.

While Greenhouse formulas for inductance are very accurate [86], they are difficult to use in the design process. By instead approximating the sides of the inductor spiral as symmetrical current sheets [87], inductance may be calculated from the parameters described above by:

$$L = \frac{\mu n^2 d_{\text{avg}} c_1}{2} \left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2 \right], \tag{5.1}$$

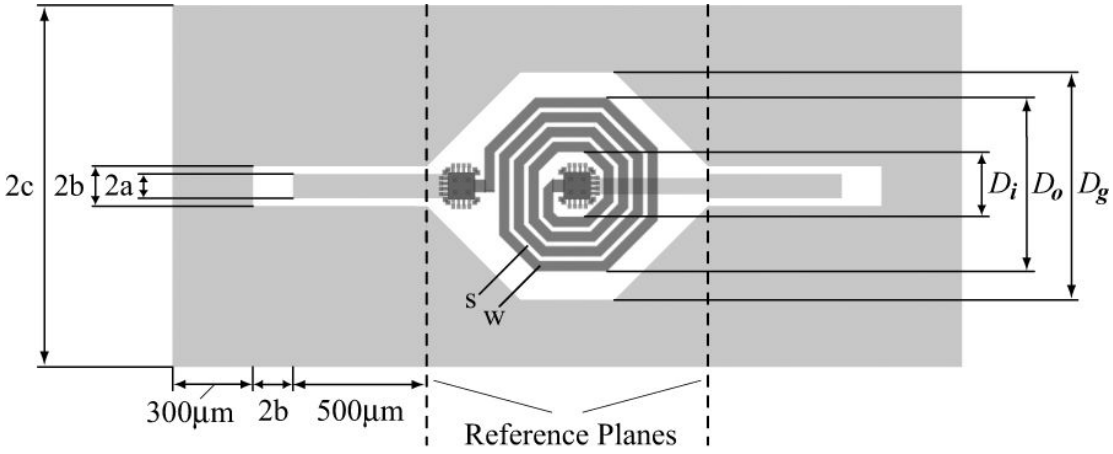


Figure 5.4: Critical dimensions of the inductor test substrate include the finite ground CPW dimensions ($2a$, $2b$, $2c$), the inner and outer diameters of the inductor (D_i and D_o), the turn width (w) and spacing (s) between turns, the diameter of the ground slot around the inductor (D_g), the distance of the CPW launch from the probe pads to the reference plane ($500\,\mu$m), the open-circuit end-gap distance ($2b$), and the width of the backshort ($300\,\mu$m). The CPW dimensions, backshort, and launch remain constant for all tested inductor types. The ground slot diameter is consistently $D_o + 200\,\mu$m. D_i, D_o, s, and w are varied in each inductor type.

where μ is the magnetic permeability, the fill factor $\rho = (D_o - D_i)/(D_o + D_i)$, and the average diameter $d_{\text{avg}} = (D_o + D_i)/2$. The coefficients c_i are dependent on the geometry of the spiral, and are summarized in Table 5.1, repeated here for completeness.

Table 5.1: Coefficients for Current Sheet Expression

Geometry	c_1	c_2	c_3	c_4
Rectangular	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circular	1.00	2.46	0.00	0.20

As the ratio of s/w becomes large, the accuracy of these expressions degenerates [87], however, most spirals are designed with $s \leq w$ to increase the inter-winding magnetic coupling and reduce the overall component footprint. Other considerations include: open space in the center of the spiral for flux lines to increase the stored energy, and a maximum diameter less than $\lambda/30$ to avoid distributed effects [48]. Tapering the traces can increase the quality factor by balancing the effects resistive losses of thin windings with the induced eddy current losses of wide windings [88]. Table 5.2 gives a summary of the design parameters for the inductors in this work, referring to dimensions in Figure 5.4 and the labels from Figure 5.2. A tapered inductor is included in this work, however the tapers presented here are not optimized.

5.3.2.2 Resistance

The DC resistance of the inductor coil is given as:

$$R_{\text{DC}} = \frac{l}{wt\sigma} = \frac{l}{w} R_s, \tag{5.2}$$

where l is the total length of the inductor coil, σ is the metal conductivity, w is the turn width, and t is the thickness of the conductive layer [89] (2.5 μm for the METAL + ELECTRO layers in this case, approximating the cross-section as rectangular). The

Table 5.2: Inductor Design Parameters with Estimates of Inductance, DC Resistance, and Self-Resonant Frequency

			(μm)		(nH)	(Ω)	(GHz)
Type	n	w/s	l	D_o/D_i	L_s calc	R_s calc	f_{res} sim
Rect5	5.5	24/16	9395	650/205	16	3.82	5.0
Rect3	3.5	24/16	7112	650/367	10.4	2.89	6.3
Taper5*	5	na/10	8077	650/240	$\sim$10	1.89	5.5
Oct4	4	40/15	5722	650/240	8.1	1.40	7.5
Oct2	2	40/15	1974	650/460	4.0	0.48	11.0
Oct1	1	40/15	955	320/240	0.5	0.23	30.0
Circ4	4	24/16	4575	600/136	5.8	1.86	8.6
Circ2	2	24/16	1503	392/136	1.14	0.61	21.7

* Note the inductance of the tapered inductor (Taper5) cannot be calculated using (5.1); this inductance is estimated using full-wave simulation and matching the s-parameter response with a simple circuit model.

sheet resistance is given by $R_s = 1/(t\sigma)\ \Omega/\square$.

At high frequencies, the skin effect must be included in (5.2). For conductors of finite thickness, calculating the skin depth requires integration of the exponentially decaying current from the surface to the finite thickness t, with a surface current density of unit magnitude;

$$\begin{aligned} I_{\text{total}} &= \int_0^t e^{-x/\delta_s}\, dx \\ &= \delta_s \left[1 - e^{-t/\delta_s}\right]. \end{aligned} \tag{5.3}$$

From (5.3), the skin depth δ_s is scaled by $(1 - e^{-t/\delta_s})$ for a finite thickness of metal [90]. This scaling factor modifies the sheet resistance R_s in (5.2) to give the high frequency resistance:

$$R_{\text{RF}} = \frac{l}{w\delta_s(1 - e^{-t/\delta_s})\sigma}. \tag{5.4}$$

Since only an estimation of the series resistance is required, proximity effects are not considered.

MEMSCAP reports the sheet resistances of each of the MUMPs layers. The corresponding conductivities using the nominal layer thicknesses are $5.00{\cdot}10^4$ S/m for POLY1, $3.33{\cdot}10^4$ S/m for POLY2, and $3.33{\cdot}10^7$ S/m for the gold METAL layer. The gold ELECTRO layer conductivity is $4.1{\cdot}10^7$ S/m. In the flip-chip process, the ELECTRO layer is bonded directly to the pedestals on the circuit, providing a gold-to-gold connection. Considering the resistances of the POLY1, POLY2, and combined METAL+ELECTRO layers as three resistors in parallel, the substantially larger sheet resistance of the parallel polysilicon layers above the gold layer has a negligible contribution to the overall resistance of the inductor.

Figure 5.5 shows the resistance per unit length of the inductor coil for various conductor thicknesses from 0.5–4.5 μm. Thicknesses above 2.5 μm have insignificant effect on the RF resistance due to the skin effect, except at low frequencies. The unit length resistance in Figure 5.5 is calculated for a 40 μm turn width, but the linear

dependence on width allows scaling for the other widths used in this work. From Figure 5.5, total conductor thickness is chosen at 2.5 μm, with the DC resistance of the various types included in Table 5.2. Note that the resistance of the tapered inductor (Taper5*) must be calculated in segments, since width w changes for each inner turn.

5.3.2.3 Coplanar Waveguide

A common finite-ground coplanar waveguide (FG-CPW) structure is used for all inductors in Figure 5.2. Equations for the characteristic impedance of a FG-CPW line based on a, b, and c from Figure 5.4 are derived in [91]. Using [91] and [92] as guidelines for FG-CPW dimensions that maintain a single CPW mode, the lateral dimension $2c$ is constrained to

$$8b < 2c < \lambda_g/2. \tag{5.5}$$

It is desired that $2c$ also be larger than the diameter of the slot in the ground plane beneath the inductor D_g, which is 200 μm larger than the outer diameter of the inductor D_o. Since the largest inductor in the study has an outer diameter of 650 μm, $2c$ must be greater than 850 μm.

Using the quasi-TEM expressions in [91] to determine an initial estimate of the geometry (a, b, and c), the lateral dimension $2c$ is set to 1350 μm. This value of $2c$ gives at least 250 μm of ground plane around the inductor, and sets a maximum λ_g at 47.8 GHz from (5.5) before the excitation of higher modes. The slot width on the 635-μm thick alumina (Al_2O_3, $\epsilon_r = 9.8$) substrate is chosen to be 30 μm such that the ratio $(b-a)/h > 20$. The signal line width $2a$ of the CPW line for a 50 Ω structure is 90 μm. Although these values result in an impedance slightly less than 50 Ω from [91], they are the final adjusted values verified with a method-of-moments simulation (Agilent Momentum) to achieve 50 Ω. This transmission structure was also verified experimentally using a TRL calibration and exhibited a maximum attenuation < 0.16 dB/mm at 45 GHz.

To set the phase reference planes at the edge of the inductor, TRL calibration

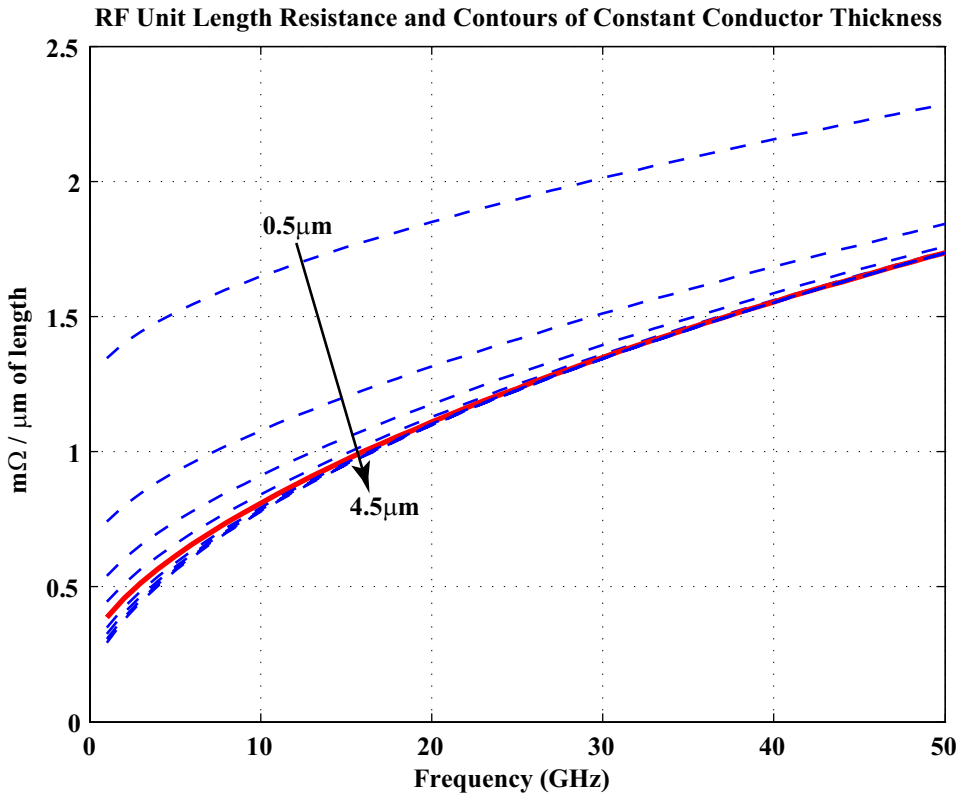


Figure 5.5: RF resistances per unit length as a function of frequency, parameterized by contours of constant thickness between 0.5 μm and 4.5 μm. Conductor thicknesses above 2.5 μm (indicated by the solid line) have significant effect on the RF resistance only at low frequencies due to the skin effect.

standards are designed with 500 μm launches. The open circuit is created with a gap from the end of the signal line to the edge of the ground plane equal to $2b$ to minimize the capacitance at the end of the line [93]. This gap is also at the ends of the transmission lines on each test structure with 300-μm backshorts. The test structures are spaced on the test wafer such that coupling between the structures is below -40 dB and verified by full-wave simulation.

5.3.3 Full-Wave Analysis

Full-wave simulations of each inductor geometry are required to determine the resonant frequency, f_{res}, at which parasitic capacitances cause the reactive component of the impedance to become zero and the phase of the impedance is zero.

Each geometry is simulated using Agilent Momentum. A few simplifications greatly decrease the simulation time:

(1) the alumina substrate is thick compared to the slot width, therefore the substrate is assumed to be infinite;

(2) the finite ground planes extend far enough to cause little deviation in impedance from the case of the ideal CPW with infinite ground planes, therefore the ground is assumed to be infinite and only the slot is meshed; and

(3) the backshort in the ground plane has little effect on the circuit, therefore it can be ignored.

A simulation of the exact finite-ground/finite-substrate structure was compared to the simplified model and validates convergence of these assumptions from 1–50 GHz.

Table 5.2 summarizes the results of the simulations, showing the resonant frequency for the various inductor types.

5.4 Hybrid Assembly

One of the primary goals of this work is to bring the advantages of compact, planar inductors to hybrid circuits. Hybrid integration in this case involves transfer of the inductor from the silicon wafer to the circuit, and elimination of the lossy [85] silicon wafer.

In earlier inductor assemblies, the thermo-compression bonding to gold bumps on an alumina (Al_2O_3) substrate occurred first, followed by a timed 49% hydrofluoric acid (HF) etch of the sacrificial PSG layer. While HF does not attack alumina, not all microwave substrates and components are HF resistant. Providing greater versatility requires a pre-release assembly mechanism to be integrated with the inductor, allowing the HF release to occur before the thermo-compression bond to the microwave substrate.

To facilitate a "pre-release" of the inductor before bonding, the inductor structure is anchored through the sacrificial PSG to the silicon wafer by tethers around the bond pads [82], illustrated in Figure 5.6. With these polysilicon tether structures, the timed HF release occurs first, leaving the inductor suspended in air while anchored through the tethers to the silicon wafer. The receiving microwave substrate has pedestals (gold bumps) that align with the two bond pads on the inductor. The pressure applied to the pad during bonding causes the tethers to break at the designed notches in the polysilicon, indicated in Figure 5.6, which free the inductor from the host silicon. The final structure is a metal spiral suspended 60 μm in air above the microwave substrate. Figure 5.7 shows a conceptual schematic of the complete transfer process, and Figure 5.8 shows photographs taken during the process. In addition, a locking mechanism in the bond pad using the POLY0 layer of the PolyMUMPs process guides and hold the inductor in position during the bonding process. These locking structures are shown in Figures 5.6 and 5.7(c).

This hybrid assembly has been demonstrated on both alumina and Rogers TMM6

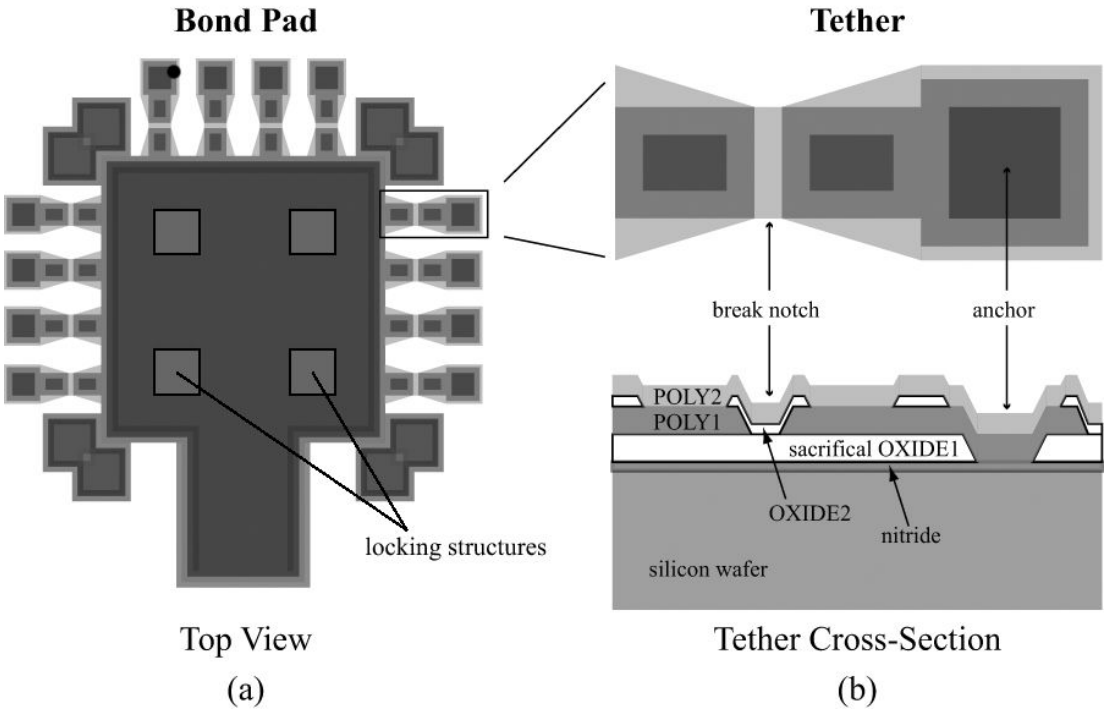
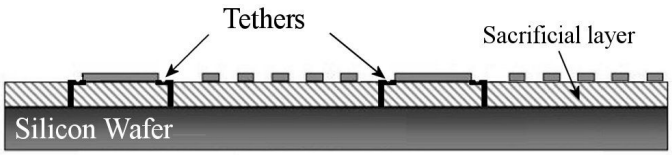
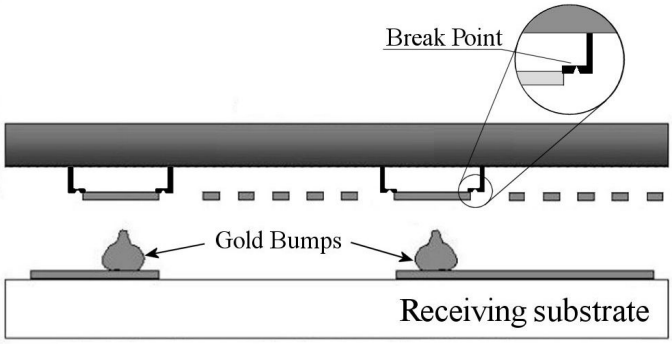


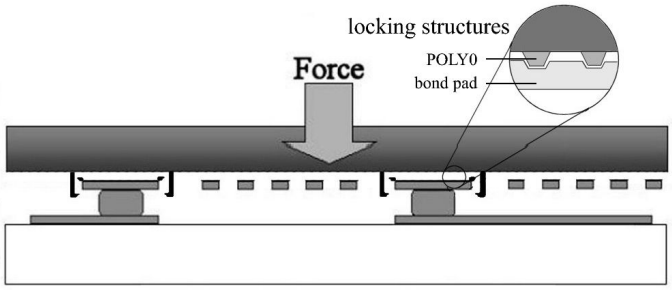
Figure 5.6: Layout of the assembly tethers surrounding a bond pad (a) and an enlarged top and cross sectional view of a single tether (b). The notch is located at a predetermined breaking point.



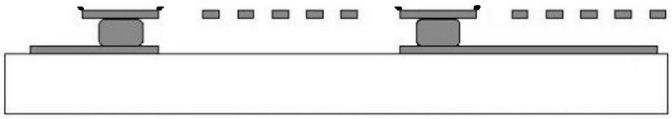
(a) A micromachined inductor on the silicon wafer before the pre-release etching of the sacrificial oxide.



(b) A pre-released device flipped and aligned with the bond pads on the receiving substrate. The inductor is anchored to the silicon wafer by the tethers surrounding the bond pads.

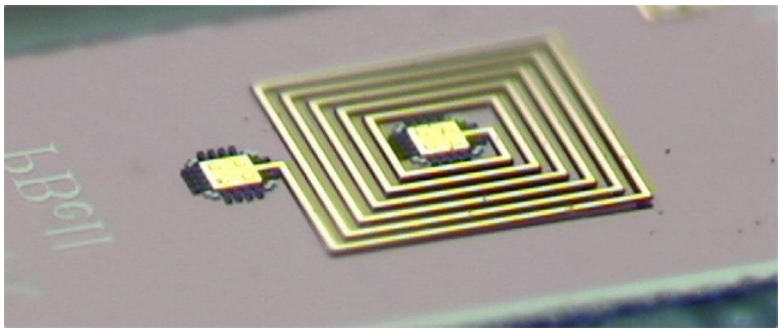


(c) Thermo-compression bonding breaks the tether structures to completely release the inductor.

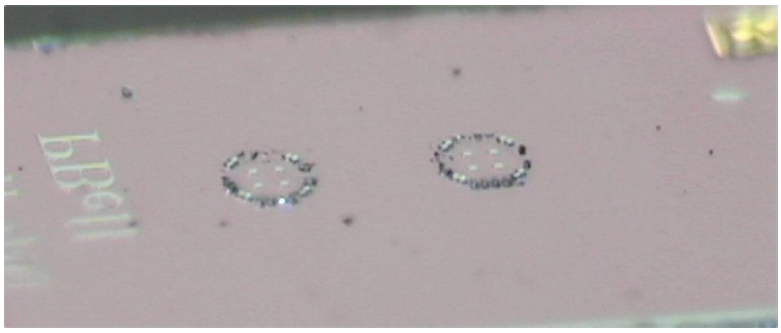


(d) A released inductor suspended in air above the microwave substrate.

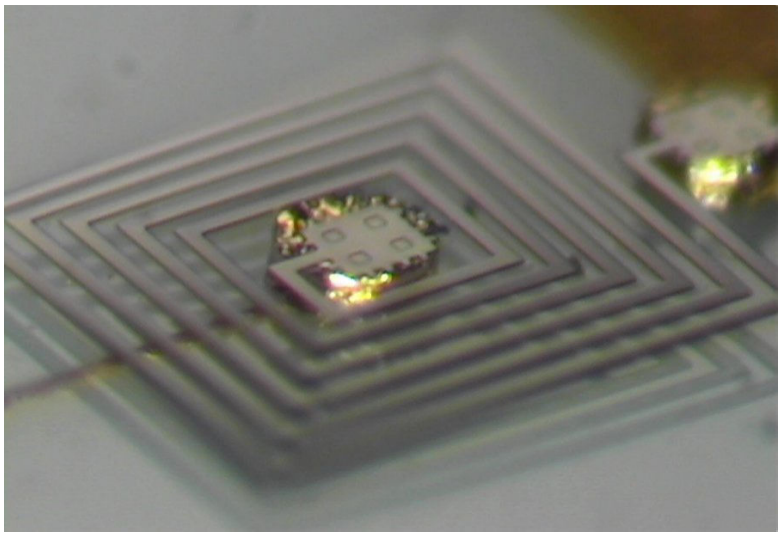
Figure 5.7: A cross-sectional illustration of the pre-release and flip-chip transfer process of the tethered inductor. The sacrificial oxide layer of the host wafer with micromachined inductor features (a) is etched, leaving the inductor structure anchored to the host substrate by the tethers. The inductor-host substrate combination is then flipped and aligned (b) with the gold bumps on the receiving substrate. Thermo-compression bonding (c) joins the inductor bond-pads to the gold bumps and simultaneously breaks the tethers at designed points. The inset in (c) shows an interlocking structure to hold the inductor in place during the bonding process. After flip-chip transfer, the resulting structure is a released device (d). This conceptual drawing is not to scale.



(a) A pre-released inductor anchored by tethers to the host silicon substrate.



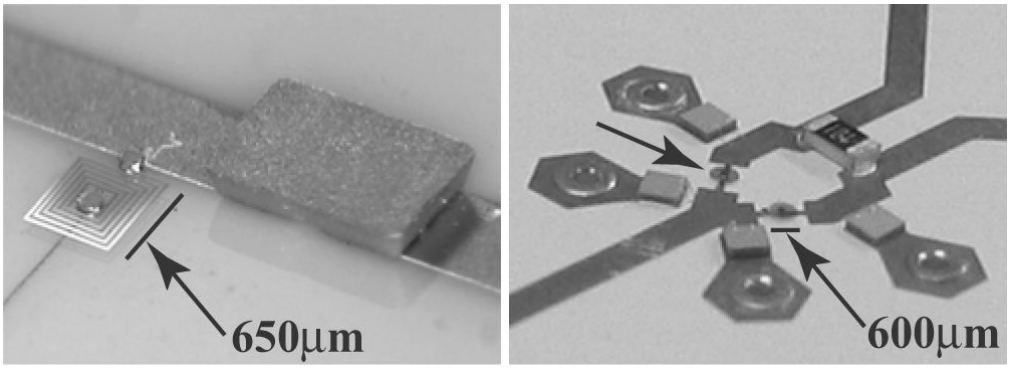
(b) Broken tethers remaining on the host substrate after flip-chip assembly.



(c) Final integrated inductor assembly.

Figure 5.8: The micromachined inductor on the host silicon wafer after pre-release (a). The gold layer is visible on the surface of the inductor. After flip-chip bonding, the tethers break away from the inductor structure and remain attached to the host wafer (b). The final structure is a suspended inductor (c). The top layer visible on the inductor in (c) is polysilicon. The gold layer is now underneath the flipped device.

substrates [71, 83], shown in Figure 5.9, and is compatible with any flat substrate. No sacrificial material is required on the circuit substrate, and this method can integrate inductors with existing microwave circuitry.



(a) Bias Tee (b) Wilkinson Divider

Figure 5.9: Inductors from this work hybridly integrated with surface-mount capacitors and resistor in a miniature bias tee on alumina [71] and a miniature low-loss Wilkinson power divider on Rogers TMM6 [83]. The scale and inductors are indicated. The bias-tee has an insertion loss of 0.5 dB from 1–15 GHz. The 1.72-GHz 3-dB divider has a 0.96-cm^2 footprint, with S_{11}=-20 dB, S_{23}=S_{32}=-26 dB, and insertion loss of 0.2 and 0.8 dB at ports 2 and 3 respectively.

5.5 Measured Performance

Three copies of the eight inductor types were characterized to verify basic repeatability. S-parameters were measured on a 50-GHz Agilent 8510C network analyzer and a Cascade Summit 9000 probe station with 250-μm pitch air coplanar (ACP) ground-signal-ground (GSG) probes. A thru-reflect-line (TRL) calibration was performed with reference planes at the edge of the inductor, Figure 5.4.

Depending on the intended application, different parameters are relevant. Inductors in matching circuits and filters operate below the resonant frequency, and so resonance and quality factor are critical parameters. RF chokes for bias lines require a high impedance, in which case the inductor can operate beyond the resonance frequency. This section summarizes measured results in terms of phase, quality factor, and input

impedance.

5.5.1 Equivalent Circuit Model

Using the measured s-parameters, the equivalent circuit model often accepted in the literature [89], Figure 5.10, is fit to the experimental data using the optimization routines in Agilent ADS. A gradient method is used to fit the model to the magnitude and phase of the impedances of the experimental data from 1 GHz to the self-resonant frequency. L_s, C_s and R_s are the series inductance, capacitance and resistance. The shunt capacitance C_p and resistance R_p are due to substrate losses. Typically the shunt resistance for insulating substrates is assumed to be infinite [72, 78], however, without this component the equivalent model does not converge to the measured Q factor. For best accuracy in the model, R_p cannot be assumed to be infinite. Table 5.3 shows typical component values for all inductor types, where R_p is in the range of 10–50 kΩ.

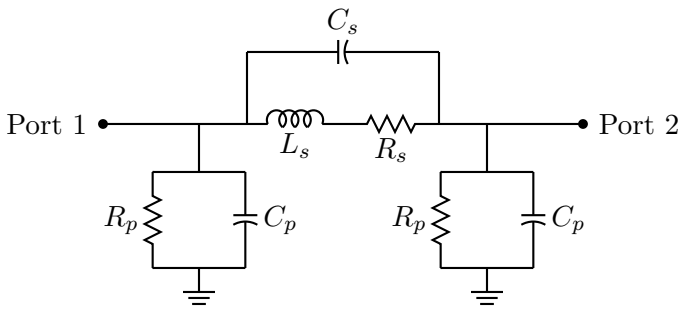


Figure 5.10: A pi-equivalent circuit model of the inductor, where L_s, C_s and R_s are the series inductance, capacitance and resistance. The substrate effects are included in C_p and R_p. This model is accurate up to the resonant frequency.

5.5.2 Self-Resonant Frequency

The self-resonant frequency is most visible in the phase of the input impedance of the inductor Z_{in} with a short circuit termination at port 2 of Figure 5.10. The resonance occurs when the phase changes abruptly from 90° to -90°.

Table 5.3: Extracted Equivalent Circuit Parameters and Measured Performance

Parameter	(nH) L_s model	(Ω) R_s model	(fF) C_s model	(fF) C_p model	(kΩ) R_p model	(GHz) f_{res} meas	(GHz) f_{Qmax} meas	Q meas
Rect5	16.1	1.95	4.7	58.2	20.3	5.0	1.6	45
Taper5	12.7	0.47	4.14	57.0	20.9	5.8	1.2	100
Rect3	11.84	1.1	1.1	48.5	41.8	6.8	2.3	82
Oct4	7.84	1.65	1.4	47.6	22.5	8.2	2.9	50
Circ4	5.56	1.74	2.32	40.1	46	10.4	5.9	57
Oct2	4.12	0.88	0.48	42.2	50	11.6	5.5	88
Circ2	1.14	0.61	8.6	20.0	19.3	27.7	11.2	76
Oct1	0.65	0.28	5.98	25.2	5.1	34.8	8.5	64

Figure 5.11 shows the phase of each of the eight inductor types. The solid lines represent the equivalent circuit models, with the symbols at the measured data points showing the close agreement of the models. The measured resonant frequency is also included in Table 5.3, The resonance frequency obtained with full-wave simulation is in Table 5.2.

5.5.3 Input Impedance

The magnitude of Z_{in} is critical to RF chokes in bias lines. Figure 5.12 shows the magnitude of Z_{in} for the 8 types of inductors. The maximum impedance for each of the inductors occurs at the resonant frequency, which is where the impedance crosses the real axis of the Smith chart. Beyond this resonance, although on the capacitive side of the Smith chart, the impedance remains high. For added clarity, the measured data is cut after the first minimum of Z_{in} (around $20\,\Omega$), beyond which the inductor alternates between series and parallel resonances and would be quite difficult to use in an RF choke design. In the case of the Rect5 inductor, which is demonstrated in a miniaturized bias-tee in [71], the impedance is above $100\,\Omega$ from 1 to 15 GHz. This high impedance range corresponds to the operating range of the bias-tee, where losses between the RF ports are minimized.

5.5.4 Quality Factor

This section describes the method used in this work to calculate the quality factor from measurement. The equations listed in this section are given for completeness. In its most general form, the quality factor is a ratio of energy stored to the power dissipated per cycle:

$$Q = \omega \frac{W_s}{P_d}. \tag{5.6}$$

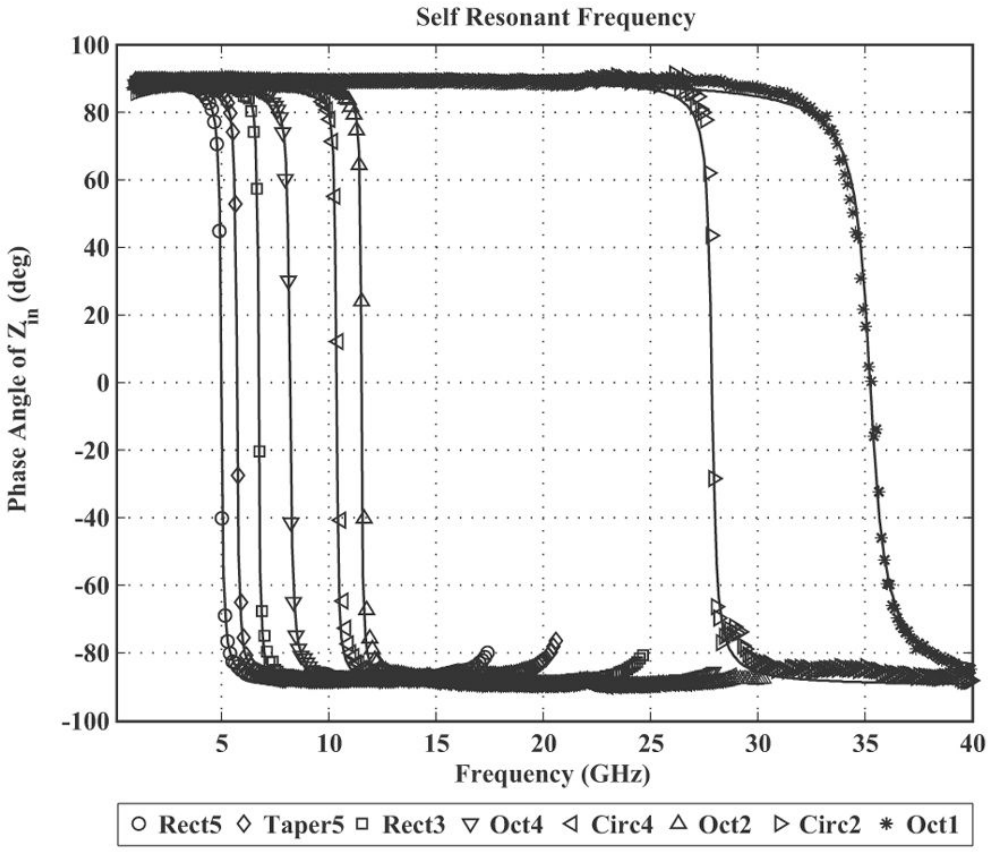


Figure 5.11: Measured (symbol) and modeled (solid line) phase of the eight inductors from Figure 5.2. The self-resonant frequency occurs where the phase crosses zero. The legend shows the order of the self-resonance frequency from left to right. A summary of the measured resonant frequencies is included in Table 5.3

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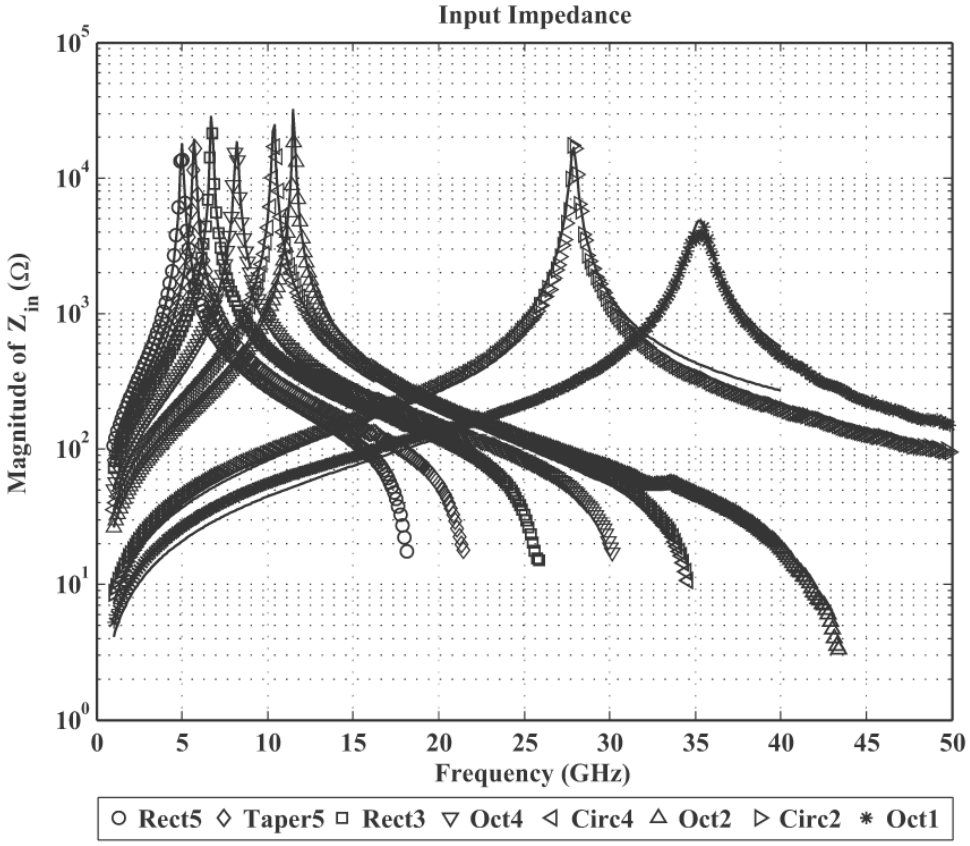

Figure 5.12: Measured (symbol) and modeled (solid line) input impedances for all types of inductors. The maximum impedance occurs at the resonant frequency. The legend shows the order of the impedance peak from left to right. For clarity, only the impedances up to the first minimum are shown.

At low frequencies ($f \ll f_{\text{res}}$), the stored energy is in the reactance and is primarily inductive, so the Q-factor is defined as:

$$Q = \omega \frac{\frac{1}{2}Li^2}{\frac{1}{2}Ri^2} = \frac{\omega L}{R}, \tag{5.7}$$

where i is the rms current [89]. At microwave frequencies and close to the self-resonant frequency, the effects of additional parasitic reactances must be included:

$$Q = \frac{\text{Im}\,[Z_{in}]}{\text{Re}\,[Z_{in}]} = \frac{X}{R}, \tag{5.8}$$

where Z_{in} is the input impedance with a short circuit termination at port 2 of Figure 5.10.

The inductive and capacitive reactances become equal at the self-resonant frequency (f_{res}), and the imaginary part of Eq. 5.8 becomes zero. Since quality factor is normally associated with resonators, where peak Q is achieved at the resonance frequency, the zero condition of the inductor quality factor at resonance is unusual. However, regardless of its discrepancies with resonator quality factors, this definition is generally used as a quantitative descriptor of inductor performance.

Figure 5.13, Figure 5.14, and Figure 5.15 show the measured Q-factor (symbols) and the Q-factor of the equivalent circuit model (solid line). The maximum Q (Q meas) and the frequency at which this value occurs (f_{Qmax} meas) are included in Table 5.3.

The s-parameter method of calculating quality factor is very sensitive, most evident in Figure 5.15 for high values of Q at high frequencies. Similar behavior is noticed in [78] and [74]. A different measurement and extraction method will be needed as higher-frequency inductors become more available. The models for Circ2 and Oct1 are fit to the data at lower frequencies (1–8 GHz) and at the self-resonant frequency, resulting in conservative peak-Q values compared to the data.

The trends in Figure 5.13–5.15 suggest three methods of quality factor improvement. First, the quality factor at frequencies up to 5 GHz may be enhanced by thicker

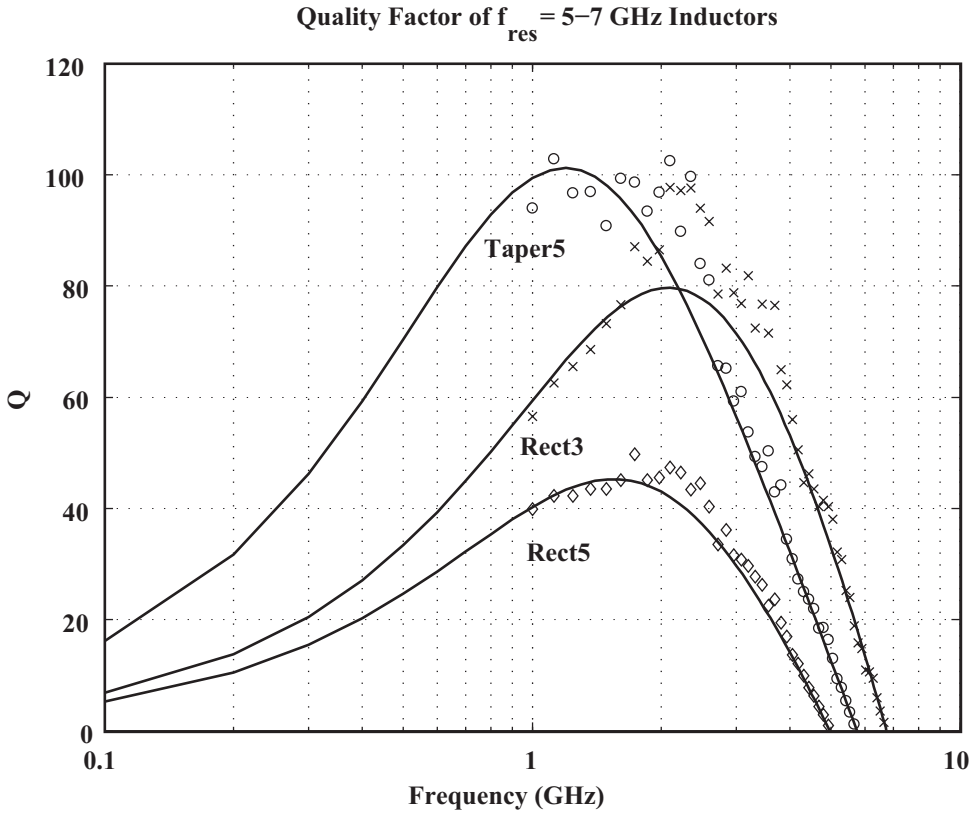

Figure 5.13: The quality factors of inductors with resonant frequencies between 5 and 7 GHz. Rect5 ($\diamond$) and Rect3 ($\times$) have maximum Q of 45 and 80 respectively. Maximum Q of 100 is achieved by the tapered design Taper5 ($\circ$). The solid lines indicate the calculated Q responses of the equivalent circuit models for each type.

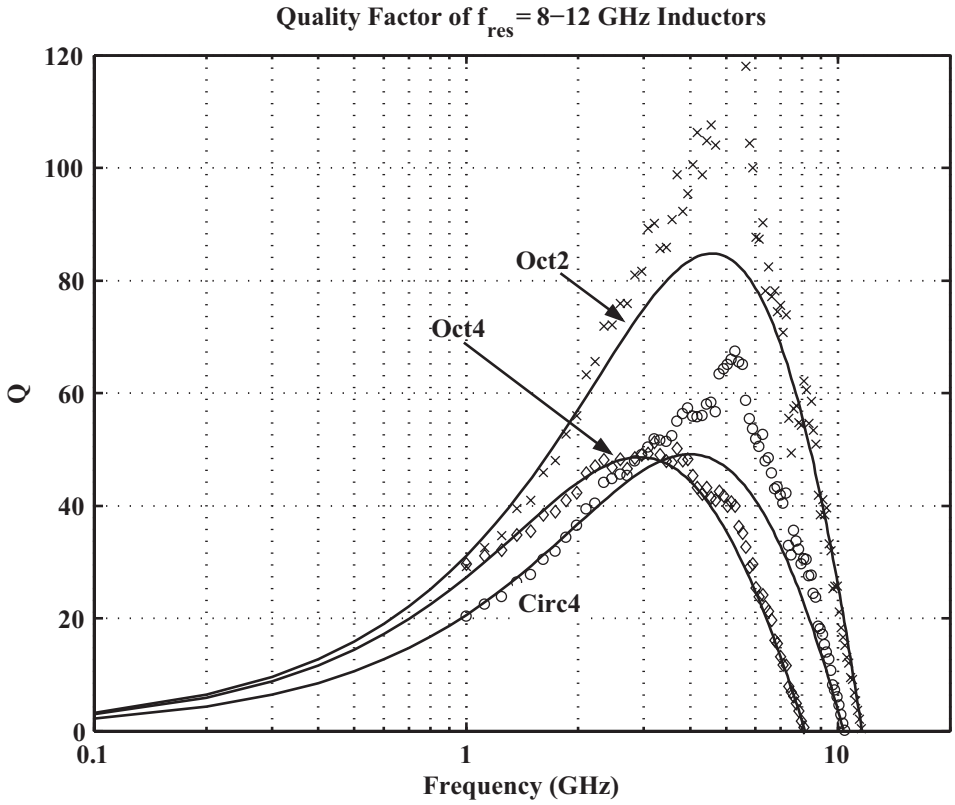

Figure 5.14: The quality factors of inductors with resonant frequencies between 8 and 12 GHz. Oct4 ($\diamond$) and Circ4 ($\circ$) have a Q maximum of 50, and Oct2 ($\times$) has peak quality factors of 85. The solid lines indicate the calculated Q responses of the equivalent circuit models for each type.

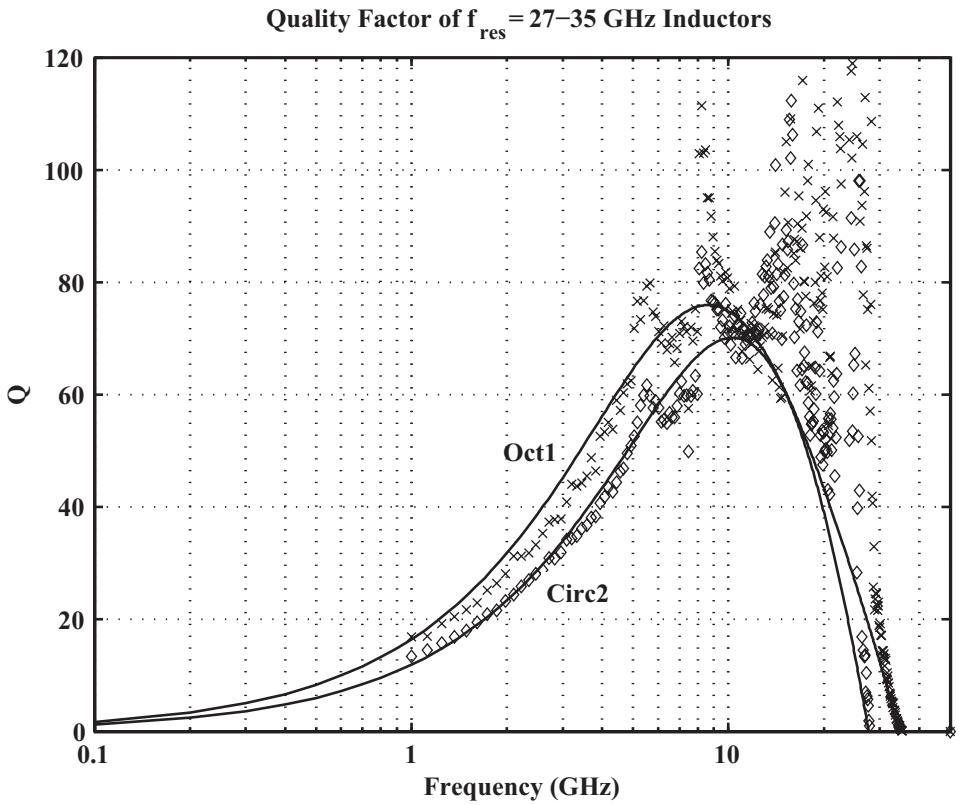

Figure 5.15: The quality factors of inductors with resonant frequencies between 27 and 35 GHz. Circ2 ($\diamond$) has a maximum Q of 70, and Oct1 ($\times$) a maximum Q of 75. The solid lines indicate the responses of the equivalent circuit models for each type. Sensitivity of the measurement between 10 and 12 GHz makes it difficult to achieve a high degree of convergence over the entire measurement and adds some uncertainty. The maximum Q is taken from the model, which converges with the measured data except between 10 and 12 GHz.

metalization. Second, reducing the potential for conductor and induced eddy current loss in the inner turns by eliminating them in the open core Rect3 and Oct2 inductors improved the quality factor significantly, although these configurations do not achieve the maximum inductance for the area occupied by the inductor. Additionally, tapering the turn widths to balance the effects of conductor losses in the longer outer turns and the eddy current losses for the inner turns in the presence of stronger magnetic fields dramatically enhances the quality factor, verifying the results of [88]. Essentially, these inductors exhibit the same traits as their monolithic planar spiral counterparts.

5.6 Summary and Discussion

This chapter presents design, assembly, modeling, and measurements of high Q inductors with measured resonant frequencies through Ka-band. An important additional parameter is current handling, particularly for applications in bias lines. Heating at high currents warps the inductor structure due to the CTE mismatch of the stacked structure long before it reaches a catastrophic meltdown. Warpage is considered the mode of failure, since the high heat will change the metal properties and the plastic deformation permanently changes the inductance. Since these tests are destructive, only the 5.5-turn rectangular inductor has been tested. It has the highest series resistance R_s of all the inductors in this work. Visual warpage occurred around 120 mA, with catastrophic meltdown around 300 mA for the three Rect5 inductors tested. This indicates that the maximum current handling capacity is approximately $2\,\mathrm{mA}/\mu\mathrm{m}^2$ of cross-sectional area, less than gold alone (silicon-gold alloys melt at a lower temperature than pure gold). Inductors with larger cross-sectional areas (such as the octagonal type) support approximately 200 mA before the onset of warpage. A thicker metal layer would also increase the current handling proportionally.

Susceptibility to shock and vibrations are also concerns with suspended inductors. Using the 4-turn octagonal inductor as an example, finite-element simulations

show the first three modes of mechanical resonance occurring between 9.2 and 10.8 kHz. Similar mechanical resonant frequencies for suspended inductors are reported in [74]. The multilayer structure in this work also increases the stiffness of the inductor when compared to all-metal inductors. Simulations indicate a maximum deformation at the outer edges of the inductor of 0.04 μm (<1% of the inductor coil thickness) for acceleration of 100 G. At 10,000 G, the maximum deformation is 9 μm (1.3 coil thicknesses and 15% of the total inductor height).

In summary, the inductors demonstrated in this work have inductance values ranging from 0.65–16 nH, with self-resonant frequencies from 5–35 GHz, and quality factors ranging from 45–100. The high impedance of the inductors even beyond the resonant frequency makes these inductors particularly useful as high-impedance RF chokes in bias-tees. Below resonance, the low-loss and high-Q properties of these flip-chip assembled inductors make them suitable for lumped-element circuits and impedance matching in the 1–5 GHz frequency range, where distributed matching circuits are quite large and surface-mount inductors are not readily available. This flip-chip assembly method can be used to create lumped-element inductors on hybrid circuits with frequency and quality-factor characteristics comparable to their monolithic counterparts.

Chapter 6

Summary and Conclusions

In summary, this work shows the constraints of integrating a MEMS tuner with a microwave power amplifier. In Chapter 1, current MEMS tuners from the literature are evaluated to determine their suitability for integration, and it is shown that in all cases the insertion loss of the tuner is too high to be practical.

Chapter 2 details the design and measurement of a simple reconfigurable power amplifier that can change from a linear class-A mode to a high-efficiency class-E mode, depending on the signal environment of the amplifier. Other reconfigurable amplifiers in the literature enable frequency hopping, and the ability to change operating class differentiates the amplifier in this work.

The output network in the class-A-to-E reconfigurable power amplifier is designed to have less than 0.3 dB of insertion loss. Figure 6.1 shows a comparison of the output network from Chapter 2 with other reconfigurable output networks from the literature (from Figure 1.3) and how these networks out affect the efficiency of a 55% class-E amplifier. The losses of this tuner are much lower than those in the literature, however, it is a very simple two-state tuner, whereas cases A–D have hundreds of states.

Once it is established that a two-state reconfigurable amplifier can meet our desired efficiency specifications, Chapter 3 details the design of a more complex impedance tuner, comparable to cases A–D from the literature. The double-slug type design provides 80 states within a 4:1 SWR circle with very low loss. Figure 6.2 shows a comparison

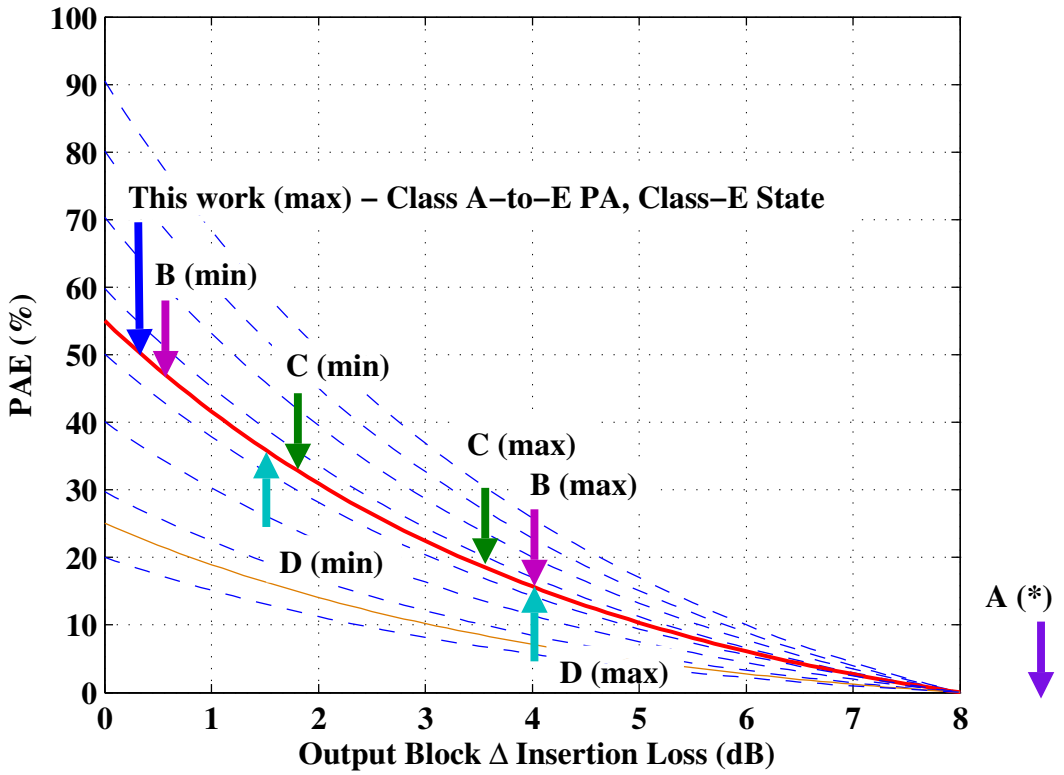

Figure 6.1: Insertion loss and efficiency performance of the reconfigurable power amplifier presented in this work compared to tuners in the published literature. The effect of additional insertion loss on the power-added efficiency is shown for a 55% efficient 10 GHz amplifier with 8 dB of gain. Loss ranges from cases A–D in the published literature are repeated from Figure 1.3. The maximum insertion loss of the reconfigurable power amplifier demonstrated in Chapter 2 is indicated.

of the designed tuner network from Chapter 3 with other reconfigurable output networks from the literature (from Figure 1.3) and how these networks out affect the efficiency of a 55% class-E amplifier. In this comparision, the tuner designed in this work has a clear improvement over current tuner networks.

Chapter 4 provides the most significant contribution of this work: a generalized method of analyzing and comparing tuner performance. Amplifier performance specifications such as output SWR are translated into tuner specifications in order to determine the necessary density of points in the impedance constellation. A specified final SWR can be used to determine the coverage area of the tuner, via a numerical analysis. This numerical analysis can determine either the total coverage of the tuner, or how many states can match a particular impedance to the specified SWR. Extending this analysis across frequency gives a tuner bandwidth. As discussed in Chapter 1, the bandwidth specified in the literature often does not mean that the tuner covers the same area over that bandwidth. Linking the tuner bandwidth to its coverage area is a more practical specification for amplifier design.

The total efficiency of the amplifier-tuner system is determined in Chapter 4 from the nominal efficiency of the amplifier, the loss of the tuner in its determined state, and the mismatch of the tuner and amplifier (determined by the density of the impedance constellation).

Chapter 4 also shows how the tuner behaves as increasing numbers of devices fail in either the open or closed states. A trend is evident that the tuner coverage area degrades more gracefully if the devices fail in the open position, which is also beneficial from a loss perspective.

Chapter 5 looks ahead to the problem of very small biasing networks that will be required in highly-integrated systems. Very small high-performance micromachined inductors are designed and measured. These inductors have the unique feature of a planar "monolithic-like" design that is integrable with hybrid circuits through a flip-

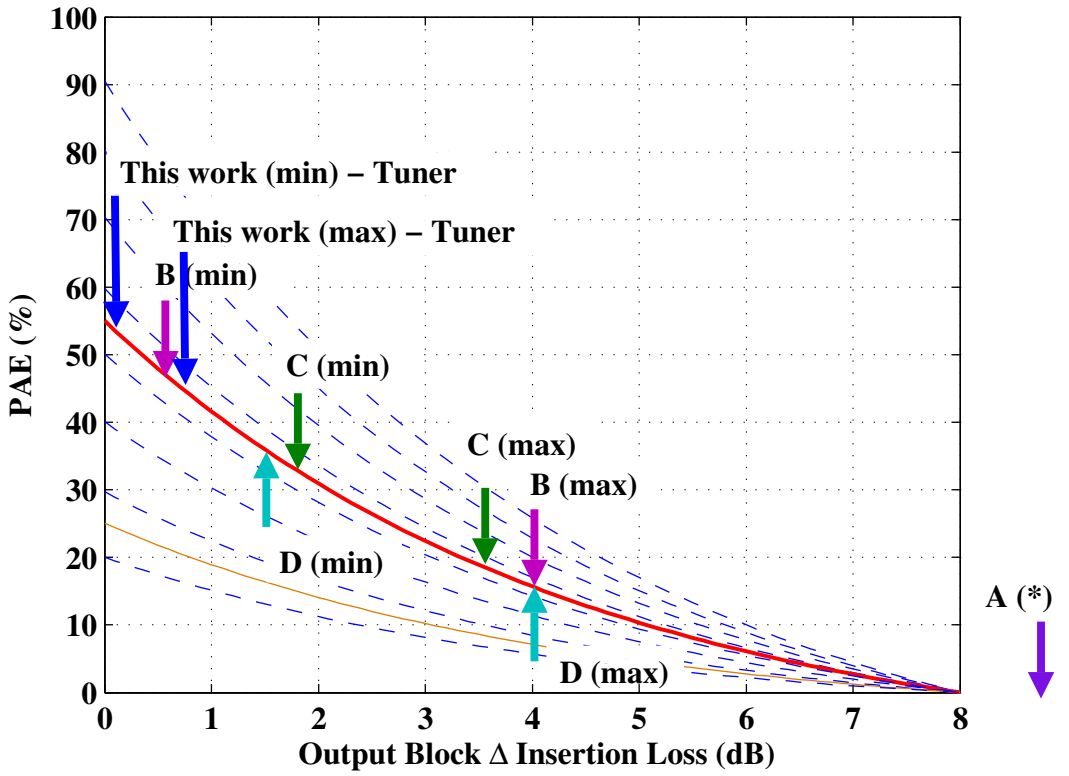

Figure 6.2: Insertion loss and efficiency performance of the double-slug impedance tuner presented in this work compared to tuners in the published literature. The effect of additional insertion loss on the power-added efficiency is shown for a 55% efficient 10 GHz amplifier with 8 dB of gain. Loss ranges from cases A–D in the published literature are repeated from Figure 1.3. The minimum and maximum insertion loss of the tuner designed in Chapter 3 is indicated.

chip assembly process.

6.1 Future Work

Future work will include verification of the circuits designed in Chapter 3 and the analysis methods in Chapter 4. Due to factors beyond the control of the author, fabrication of the tuner circuits at Sandia National Laboratories was not complete as of July 2006. Testing of these circuits will be conducted by another student at a later date.

Once these circuits are ready for testing, they should enable further testing of several multifunctional system concepts: adapting for a variable load presented by an antenna in a mobile environment; chip-scale load-pull of a transistor; adaptation of the output matching impedance for changing transistor characteristics, such as temperature and bias compensation; and interstage load/source pull for multistage power amplifiers.

In conclusion, through the examination of design constraints and performance requirements, the work in this thesis should aid in the future integration of power amplifiers and MEMS impedance tuners. Through the demonstrations of the class-A-to-E reconfigurable amplifier, and the detailed design and analysis of the MEMS double-slug tuner with the Sandia ohmic MEMS switch, it is the hope of this author that this work will help provide a bridge between amplifier designers and MEMS circuit designers in order to bring the two technologies together and enable multifunctional reconfigurable power amplifiers in the future.

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Appendix A

Transistor Data Sheet

The data sheet for the Skyworks/Alpha transistor used in Chapter 2 is included for reference in Figure A.1.

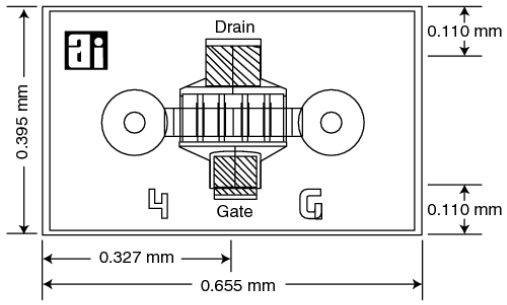
Ka Band Power GaAs MESFET Chip

Alpha

AFM04P2-000

Features

- 21 dBm Output Power @ 18 GHz
- High Associated Gain, 9 dB @ 18 GHz
- High Power Added Efficiency, 25%
- Broadband Operation, DC–40 GHz
- 0.25 μm Ti/Pd/Au Gates
- Passivated Surface
- Through-Substrate Via Hole Grounding



Chip thickness = 0.1 mm.

Description

The AFM04P2-000 is a high performance power GaAs MESFET chip having a gate length of 0.25 μm and a total gate periphery of 400 μm. The device has excellent gain and power performance through 40 GHz, making it suitable for a wide range of commercial and military applications in oscillator and amplifier circuits. It employs Ti/Pd/Au gate metallization and surface passivation to ensure a rugged, reliable part. Through-substrate via holes are incorporated into the chip to facilitate low inductance grounding of the source for improved high frequency and high gain performance.

Absolute Maximum Ratings

Characteristic	Value
Drain to Source Voltage (V_{DS})	6 V
Gate to Source Voltage (V_{GS})	-4 V
Drain Current (I_{DS})	I_{DSS}
Gate Current (I_{GS})	1 mA
Total Power Dissipation (P_T)	700 mW
Storage Temperature (T_{ST})	-65 to +150°C
Channel Temperature (T_{CH})	175°C

Electrical Specifications at 25°C

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Saturated Drain Current (I_{DSS})	V_{DS} = 2 V, V_{GS} = 0 V	90.0	140.0	190.0	mA
Transconductance (gm)		60.0	80.0		mS
Pinch-off Voltage (V_P)	V_{DS} = 5 V, I_{DS} = 1 mA	1.0	3.0	5.0	-V
Gate to Drain Breakdown Voltage (V_{bgd})	I_{GD} = -400 μA	8.0	12.0		-V
Output Power at 1 dB Compression ($P_{1\ dB}$)	V_{DS} = 5 V, I_{DS} = 70 mA, F = 18 GHz		21.0		dBm
Gain at 1 dB Compression ($G_{1\ dB}$)			9.0		dB
Power Added Efficiency (ηadd)			25.0		%
Output Power at 1 dB Compression ($P_{1\ dB}$)	V_{DS} = 5 V, I_{DS} = 70 mA, F = 30 GHz		20.0		dBm
Gain at 1 dB Compression ($G_{1\ dB}$)			5.0		dB
Power Added Efficiency (ηadd)			15.0		%
Thermal Resistance (Θ_{JC})	T_{BASE} = 25°C			250.0	°C/W

Figure A.1: Transistor data sheet, page 1

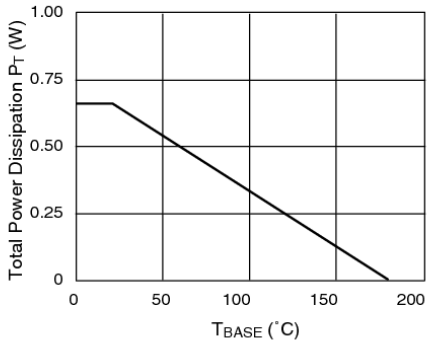
Typical S-Parameters (V_{DS} = 5 V, I_{DS} = 70 mA)

Freq. (GHz)	S_{11}		S_{21}		S_{12}		S_{22}		k	MAG (dB)
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.		
2	0.969	-37.191	5.040	153.579	0.029	68.605	0.550	-18.296	0.100	22.364
3	0.958	-54.069	4.740	141.521	0.041	59.064	0.533	-26.529	0.150	20.613
4	0.935	-69.318	4.398	130.518	0.051	50.587	0.514	-33.959	0.200	19.278
5	0.913	-82.889	4.050	120.568	0.058	43.171	0.497	-40.630	0.250	18.247
6	0.893	-94.881	3.719	111.573	0.064	36.722	0.482	-46.663	0.299	17.658
7	0.877	-105.468	3.415	103.398	0.068	31.107	0.471	-52.183	0.349	17.104
8	0.863	-114.843	31.420	95.911	0.071	26.196	0.462	-57.310	0.398	16.464
9	0.852	-123.189	2.898	88.991	0.073	21.873	0.456	-62.138	0.447	15.986
10	0.843	-130.670	2.683	82.540	0.074	18.042	0.453	-66.738	0.496	15.566
11	0.836	-137.422	2.492	67.477	0.075	14.624	0.452	-71.161	0.544	15.193
12	0.831	-143.563	2.322	70.736	0.076	11.558	0.453	-75.442	0.593	14.858
13	0.826	-149.188	2.171	65.267	0.076	8.796	0.455	-79.606	0.641	14.447
14	0.823	-154.374	2.036	60.027	0.076	6.302	0.459	-83.671	0.688	14.285
15	0.821	-159.187	1.914	54.985	0.065	4.047	0.464	-87.648	0.735	14.037
16	0.819	-163.679	1.805	50.114	0.074	2.007	0.470	-91.546	0.781	13.811
17	0.818	-167.895	1.605	45.393	0.074	0.167	0.477	-95.372	0.827	13.063
18	0.817	171.872	1.615	40.805	0.073	-1.486	0.484	-99.129	0.872	13.412
19	0.817	-175.369	1.532	36.335	0.072	-2.961	0.492	-102.821	0.916	13.235
20	0.817	-179.221	1.456	31.973	0.071	-4.266	0.501	-106.451	0.959	13.071
21	0.818	177.359	1.386	27.760	0.060	-5.405	0.510	-110.021	1.001	12.753
22	0.819	174.083	1.321	23.535	0.069	-6.382	0.520	-113.533	1.041	11.534
23	0.820	170.936	1.261	19.445	0.068	-7.201	0.530	-116.989	1.069	10.915
24	0.821	167.905	1.205	15.343	0.067	-7.863	0.540	-120.389	1.116	10.431
25	0.822	164.969	1.512	11.498	0.066	-8.371	0.551	-123.737	1.150	10.024
26	0.824	162.148	1.103	6.633	0.065	-8.728	0.561	-127.031	1.181	9.671
27	0.825	159.403	1.057	3.836	0.064	-8.937	0.572	-130.275	1.210	9.358
28	0.826	156.737	1.013	0.105	0.063	-9.004	0.583	-133.468	1.235	9.080
29	0.829	154.144	0.972	-3.563	0.062	-8.937	0.594	-136.612	1.256	8.830
30	0.831	151.618	0.922	-7.169	0.062	-8.740	0.605	-139.606	1.273	8.604
31	0.833	149.155	0.895	-10.714	0.061	-8.427	0.616	-142.754	1.285	8.403
32	0.835	146.649	0.860	-14.200	0.061	-8.010	0.627	-145.754	1.292	8.222
33	0.836	144.398	0.826	-17.627	0.061	-7.502	0.638	-148.608	1.294	8.061
34	0.838	142.097	0.794	-20.996	0.061	-6.920	0.648	-151.615	1.291	7.920
35	0.840	139.845	0.764	-24.308	0.061	-6.281	0.659	-154.477	1.283	7.797
36	0.842	137.637	0.734	-27.563	0.061	-5.604	0.670	-157.293	1.270	7.694
37	0.844	135.472	0.706	-30.761	0.061	-4.907	0.680	-160.065	1.251	7.611
38	0.846	133.347	0.679	-33.903	0.061	-4.209	0.690	-162.693	1.228	6.550
39	0.848	131.261	0.653	-36.988	0.062	-3.525	0.700	-165.477	1.202	7.513
40	0.850	129.211	0.628	-40.017	0.063	-2.874	0.710	-168.117	1.171	7.504

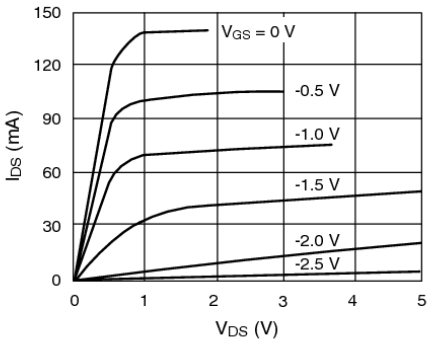
S-Parameters include the effects of two 0.8 mil diameter bond wires, each 10 mil long, to each of the gate and drain terminals.

Figure A.1: Transistor data sheet, page 2 (cont.)

Typical Performance Data



Power Derating



I-V

TOM-2 Model Parameters

Parameter	Description	Unit	Default
BETA	Transconductance Coefficient	A/V^2	0.09464
V_{PO}	Pinch-off voltage	V	-1.8760
U	Mobility degradation fitting parameter	/V	0.3599
GAMA	Slope parameter of pinch-off voltage		0.03458
Q	Power law parameter		1.6560
NG	Subthreshold slope gate parameter		0.6025
ND	Subthreshold slope drain parameter		0.6050
DELT	Slope of drain characteristics in the saturated region	/A, V	0.5633
ALFA	Slope of drain characteristics in the linear region	/V	1.9400
T	Channel transmit-time delay	pS	6.4330
C_{GSO}	Gate-source Schottky barrier capacitance at V_{GS} = 0	pF	0.4232
C_{GDO}	Gate-drain Schottky barrier capacitance at V_{GS} = 0	pF	0.03138
V_{BI}	Built-in barrier potential	V	1.200
IS	Diode saturation current	A	0.563e-12
N	Diode ideality factor		1.1000
IBO	Breakdown saturation current	A	1.000e-16
NR	Breakdown ideality factor		10.0
V_{BD}	Breakdown voltage	V	20.00
RG	Gate terminal resistance	Ω	1.0000
RD	Drain terminal resistance	Ω	2.0000
RS	Source terminal resistance	Ω	0.8000
LG	Gate lead inductance	nH	0.5572
LD	Drain lead inductance	nH	0.2279
LS	Source lead inductance	nH	0.03532
CDS	Drain-source capacitance	pF	0.1555
RDSD	Channel trapping resistance	Ω	107.99
CDSD	Low frequency trapping resistance	nF	12.03
CGE	Gate-source electrode capacitance	fF	7.7240
CDE	Drain-source electrode capacitance	fF	9.4390

Figure A.1: Transistor data sheet, page 3 (cont.)

Appendix B

Wafer Under Test

When testing systems with multiple MEMS devices, a non-intrusive means of determine the state of a switch (whether the switch was actuating under the applied voltage). A laser was used to illuminate the switch from the side, while the wafer is on the probe station under a microscope. As the switch actuates, the speckle pattern caused by reflections off the edge of the device changes and is noticeable through the microscope. A photograph of this setup is shown in Figure B.1.

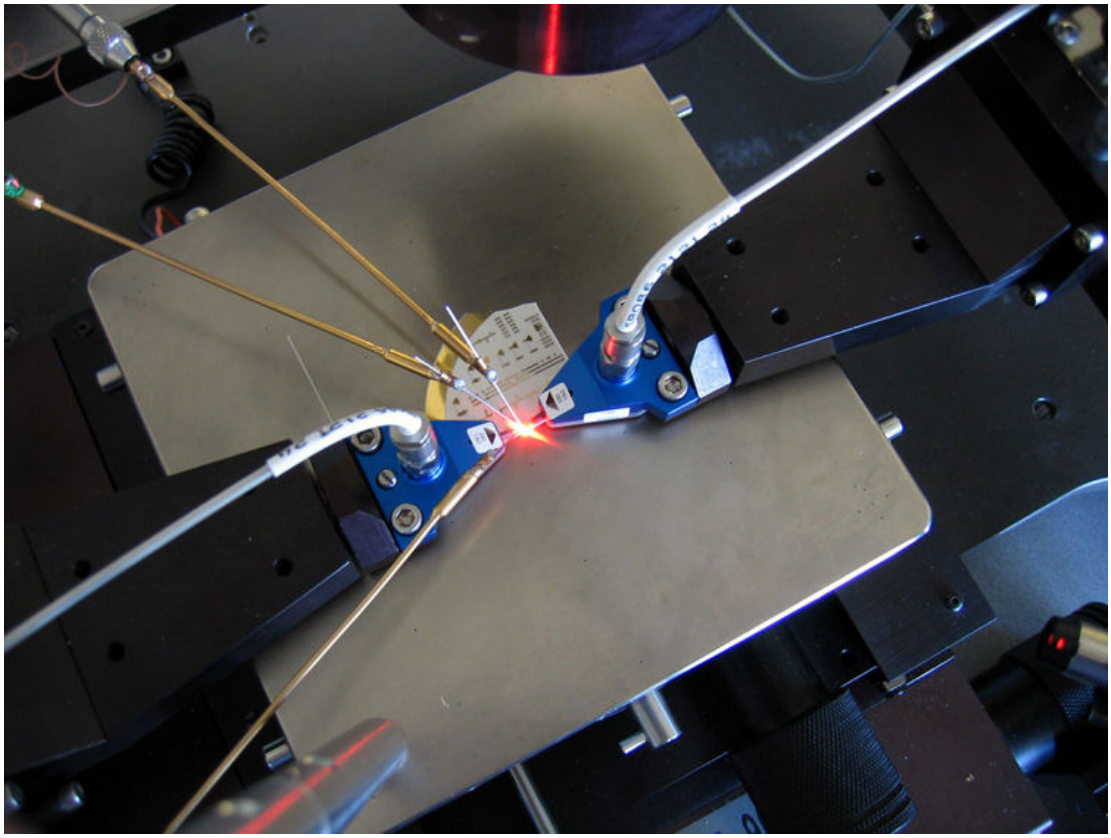


Figure B.1: A laser was used to illuminate the switch from the side, while the wafer is on the probe station under a microscope. As the switch actuates, the speckle pattern caused by reflections off the edge of the device changes and is noticeable through the microscope.