Broadband Microwave Lithographic 3D Components

by

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written by Negar Ehsan

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Zoya Popović

Dejan Filipović

Date ____________________

The final copy of this thesis has been examined by the signatories, and we

Find that both the content and the form meet acceptable presentation standards

Of scholarly work in the above mentioned discipline.

Ehsan, Negar (Ph.D., Electrical and Computer Engineering)

Broadband Microwave Lithographic 3D Components

Thesis directed by Professor Zoya Popović

The theme of this thesis is the design and characterization of rf front-end broadband components implemented in a new technology. Every radar and wireless communication system contains components such as amplifiers, antennas, filters, and dividing/combining networks. Active components usually occupy a small percentage of the total footprint, while the rest is occupied by passive microstrip or co-planar-waveguide components. For multi-functional systems that operate over different frequency ranges it is desirable to have a single broadband PA that replaces individual amplifiers for each band. Thus it is beneficial in terms of real estate and simplicity to utilize passive components that are both compact and broadband.

In this thesis, conventional dispersive transmission lines are replaced with PolyStrata micro-coaxial lines that exhibit loss around 0.1 dB/cm at 40 GHz and isolation of > 60 dB for neighboring lines sharing a common wall. The characteristic impedance of the lines is constant over a broad range of frequencies, as the TEM mode is dominant up to around 450 GHz. The design, implementation, and characterization of micro-coaxial broadband (2–20 GHz) passive components such as matching networks (impedance transformers) and divider/combiner networks are presented. Although these components were designed around 2–20 GHz, with a re-design they can operate at much higher frequencies due to the micro-coaxial lines' capabilities.

An example of a system operating at higher frequencies is NASA/JPL's Mars Science Laboratory (MSL) landing radar system, which will operate at either W-band or G-band. Size and weight constraints motivate the transition to these frequency bands. The nature of the PolyStrata fabrication process lends itself to the fabrication of rectangular waveguides above 90 GHz, making it an option for the frequency-scanned antenna array on the MSL. Results are presented in which both traveling-wave slotted-waveguide and slotted-coaxial antenna arrays at 100 GHz and 150 GHz were investigated for the MSL landing system.

Dedication

To Ali, Roya, and Bahar Ehsan.

Professional Acknowledgments

It is my pleasure to thank those who made this thesis possible.

I owe my deepest gratitude to my advisor, Professor Zoya Popović, who encouraged me to continue on my graduate studies. Not only did she always provide guidance, motivation, support, an amazing research group and lab, but she also was a great example in life. She has been always more than an advisor to me.

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Chapter 1

Introduction

Wisdom is the guide and is the heart's enlivener;

wisdom is your helper in both worlds.

From it comes happiness and all human welfare;

from it you gain increase and without it you experience loss.

—Hakim Abol-Ghasem Ferdowsi

Wisdom begins in wonder.

—Socrates

Contents

1.1 Scope of this thesis

The topic of this thesis is design and characterization of rf front-end broadband components implemented in a new technology. Every radar and wireless communication system contains rf/microwave components such as amplifiers, antennas, filters, *et cetera*. In many cases the transmitter's final stage power amplifier (PA) is the largest power consumer of the front-end [1], e.g. the power amplifier in a satellite transmitter consumes about 40% of the total power. For multi-functional systems that operate over different frequency ranges it is desirable to have a single broadband PA that replaces individual amplifiers for the different bands [2, 3].

Solid-state high power amplifiers (typically 10 W and above) are designed around discrete devices or monolithic microwave integrated circuits (MMICs) in materials such as gallium arsenide (GaAs) based heterostructures, gallium nitride (GaN), and silicon at lower microwave frequencies. MMIC PAs are usually pre-matched to 50 Ω input and output. The input and output impedances of power transistors are very low (sub-ohm for 100 W devices) and when impedance matching them to 50 Ω the design usually sacrifices bandwidth, efficiency, and/or power. Finally, in a MMIC, if one of the active devices fails, the entire PA sub-assembly is lost. It would be potentially more cost efficient if the active components could be singulated and then assembled with the rest of the components, in turn facilitating simple replacement of a failed active component.

Passive components such as transmission lines, matching networks, filters, combiners/dividers that are made in microstrip, coplanar waveguide (CPW) transmission line media, and/or waveguide usually suffer from high loss, dispersion, large component size and high coupling between the adjacent lines. In a MMIC non-uniformly-distributed-power-amplifier (NDPA) as shown in Figure 1.1, active components usually occupy less than 5 % of the total physical footprint [4], while the rest is occupied by microstrip/CPW lines and filters, matching networks, etc. It is not cost effective to use GaAs/GaN wafer real estate for passive components that do not require such expensive substrates.

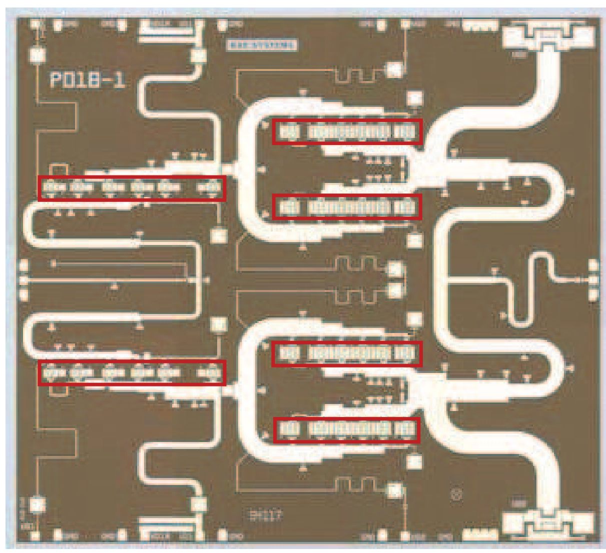


Figure 1.1: NDPA MMIC amplifier; the active transistor area, outlined by the four red boxes, occupies less than 5 % of the entire MMIC real estate.

The approach discussed in this thesis is to use non-50 Ω MMICs hybridly integrated with PolyStrata micro-coaxial lines which replace conventional guiding media. These micro-coaxial lines have loss as low as 0.1 dB/cm (0.08 dB/λ) at 38 GHz [5], and isolation of 60 dB at Ka band for neighboring lines sharing a common ground wall [6]. The characteristic impedance of the lines is constant over a broad range of frequencies, since the TEM mode is dominant up to around

450 GHz depending on the line geometry [7, 8]. Table 1.1 compares some of the properties of micro-coaxial lines, microstrip lines, coplanar waveguides, and hollow metallic waveguides. The low dispersion, accompanied by low loss and high isolation, makes the PolyStrata process uniquely suitable for ultra-broadband (2–20 GHz) miniaturized components necessary for rf front-ends.

Table 1.1: General characteristics of different media

	Microstrip	CPW	Waveguide	Micro-coax
Mode	Quasi-TEM	Quasi-TEM	TE or TM	TEM
Dispersion	High	High	Very high	Very low
Impedance Range (Ω)	15–100	25–100	Fixed	5–140
Loss at 40 GHz	1 dB/cm	1 dB/cm	0.013 dB/cm	0.08 dB/cm
Component size	Small	Small	Large	Very small
Isolation at 40 GHz	−25 dB	−30 dB	Very high	−60 dB
Manufacturing cost	Low	Low	High	Medium

Figure 1.2 shows a system-level block diagram of a typical rf front-end. This thesis focuses on the transmit path of the front-end and in particular on the design, implementation, and characterization of broadband passive components such as the matching networks (impedance transformers), divider/combiner networks, and the antenna or the antenna array. Using micro-coaxial or other PolyStrata components instead of traditional guiding media has a potential to be both cost efficient and offer improved performance compared to more traditional approaches.

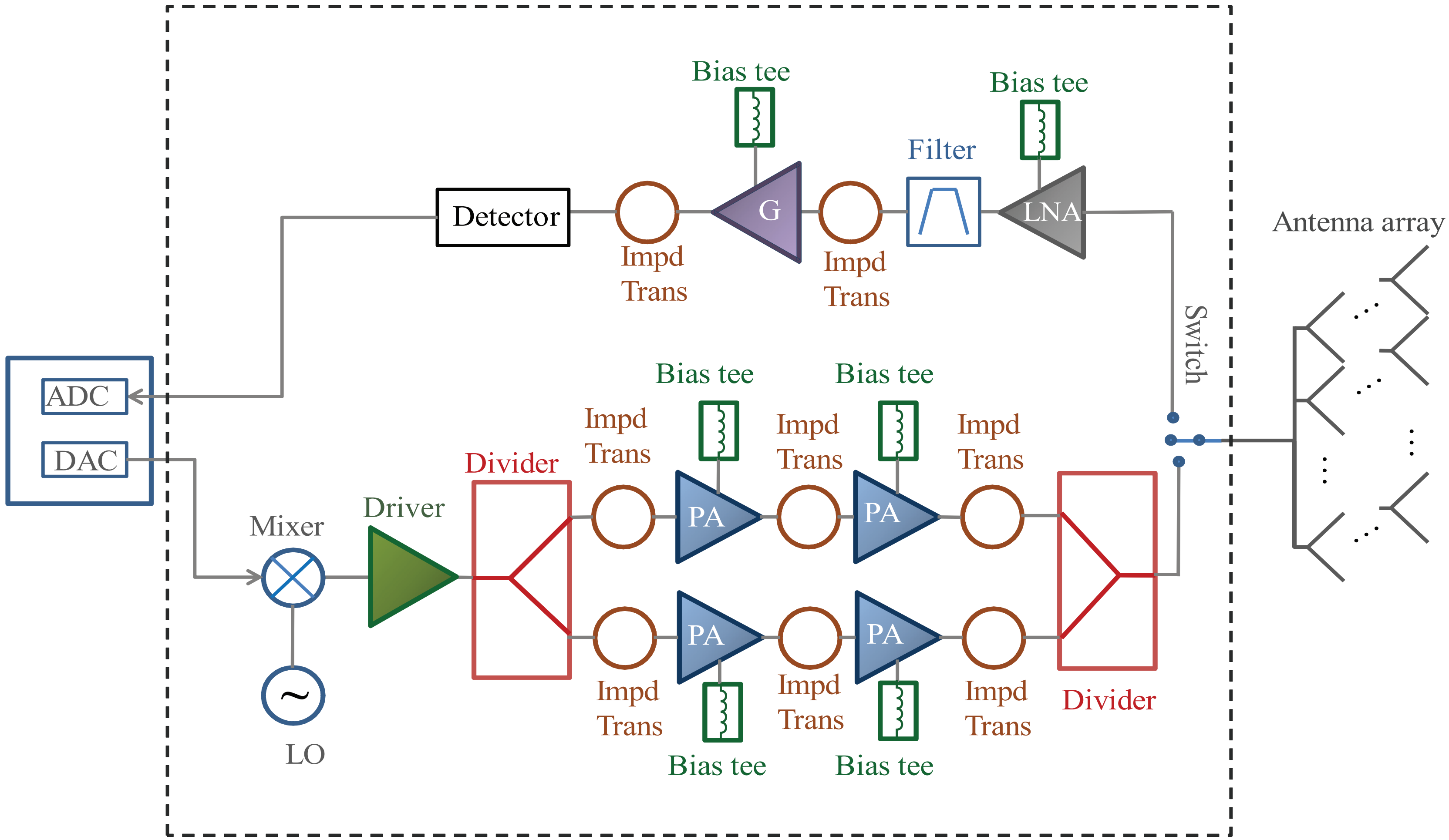


Figure 1.2: Block diagram of a generic communication/radar system. This diagram consists of three sections: analog to digital and digital to analog converters, passive and active rf circuitry, and the antenna(s). Note: the switch in front of the antenna can be replaced by a circulator or duplexer, depending on the application.

1.2 PolyStrata process

The PolyStrata process involves sequential deposition of copper layers and photoresist on a silicon wafer. Copper layer thicknesses range from 10 µm to 100 µm, with gap-to-height and width-to-height aspect ratios of 1:1.2 and 1:1.5, respectively. The inner conductor is supported by 100 µm long dielectric straps with periodicity of 700 µm. After the desired layers are deposited, the photoresist filling all space unoccupied by copper and dielectric straps is rinsed away ("released") through 200 µm × 200 µm release holes. Figure 1.3 depicts this process graphically.

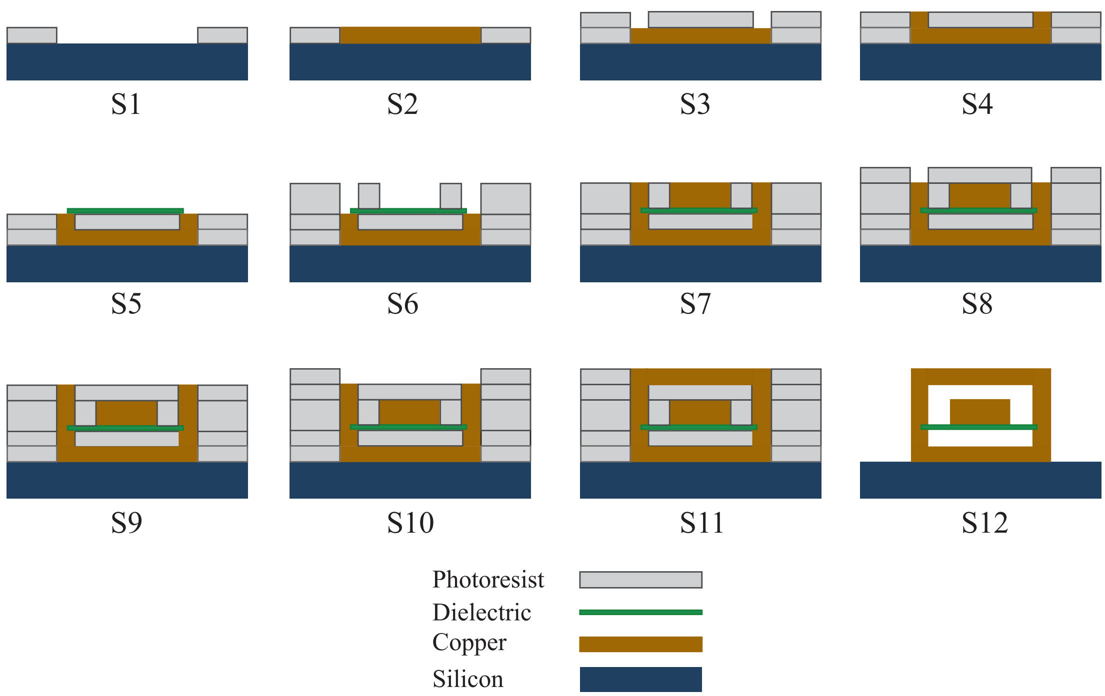


Figure 1.3: Graphical explanation of the PolyStrata process for a 5-layer micro-coaxial line. In the first step photoresist is applied and patterned on the silicon wafer with a mask. Next, a uniform copper layer is electroplated on the wafer and then planarized. The same steps are repeated to grow the structure. In order to support the inner conductor, dielectric straps are embedded into the sidewalls through photopatterning. Steps 1–5 are repeated to complete the structure. With this method up to 15 independent layers can be made. The last step is releasing the photoresist to complete the fabrication of an air-filled micro-coaxial line [9].

1.3 Previous work

In this section a review is presented of some of the previous research done in theoretical analysis of both generic rectangular coaxial lines and micro-coaxial lines in the PolyStrata process. Components previously designed and implemented in this technology are summarized.

1.3.1 Theoretical analysis

The early studies of lossless rectangular coaxial lines go back to the calculation of characteristic impedance Z_c:

$$Z_c = \sqrt{\frac{L}{C}} = \frac{1}{\upsilon C}, \tag{1.1}$$

where L is the inductance per unit length, C is the capacitance per unit length, and the propagation velocity υ is given by

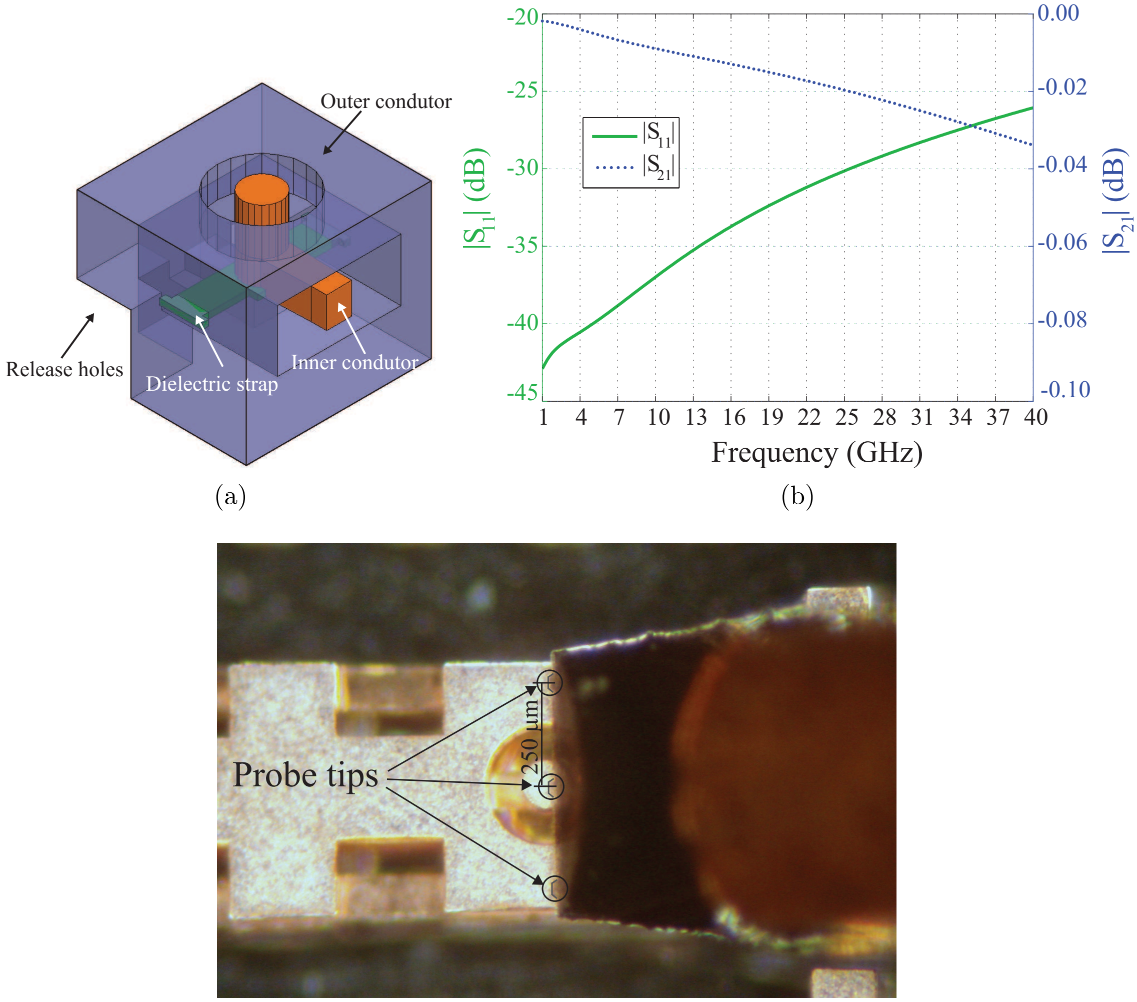
$$\upsilon = \sqrt{\frac{1}{\varepsilon\mu}} = \sqrt{\frac{1}{LC}}. \tag{1.2}$$

Various conformal mapping techniques were used to calculate the inductance and capacitance per unit length and characteristic impedance of the rectangular coaxial lines. Chen [10] calculated characteristic impedance for different cases such as various inner conductor heights compared to outer conductor heights‘, symmetrical and eccentric rectangular coaxial lines and rounded inner conductor edges. Costamagna [11] found the characteristic impedances of several symmetrical and eccentric rectangular coaxial lines by means of numerical inversion of the Schwarz-Christoffel conformal mapping. His analytic results agreed very closely with his own experiments, Chen's calculations, and other existing results. Theoretical expressions for conductor loss in rectangular coaxial lines based on Wheeler's rule were presented by Lau [12].

Lukić *et. al* [7] performed a comprehensive study of the effects of imperfections in the manufacturing of PolyStrata micro-coaxial lines. A quasi-analytical modeling approach based on two numerical implementations of the Schwarz-Christoffel conformal mapping technique was used for analyzing these lines. Non-idealities of the micro-coaxial lines due to fabrication were studied and their effects on characteristic impedances, attenuation, bandwidth, and power handling were presented. 3D surface roughness effects on attenuation in the PolyStrata micro-coaxial lines were also presented in [13]. In order to measure PolyStrata components with standard non-micro-coaxial measurement equipment such as CPW probes, Vanhille [6] designed several transitions called "launches." The launch is a robust structure that allows repeatable and accurate measurements. Figure 1.4 shows an HFSS model of a launch, of which the same launch topology is used on most of the components discussed throughout this thesis. An example of a 250-μm-CPW probe connected to the launch is shown in Fig. 1.4 c.

Some of the properties of PolyStrata micro-coaxial lines that have been designed and measured are summarized as:

- loss as low as 0.1 dB/cm at Ka band [5]
- Isolation of better than 60 dB between two micro-coaxial lines sharing a common ground wall [8, 14]
- Constant characteristic impedances due to dominant TEM mode up to 450 GHz (geometry dependent)

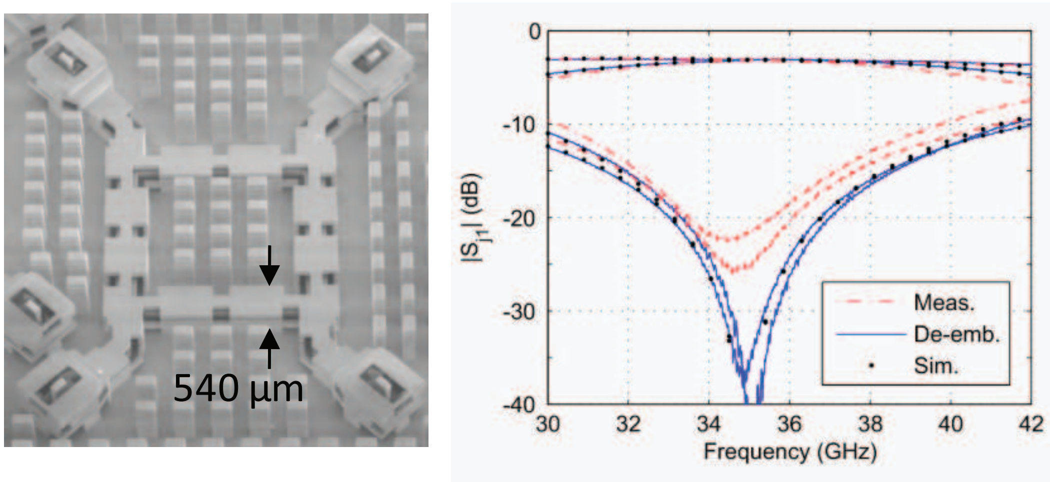


(c)

Figure 1.4: (a) HFSS model of a launch that transitions between a 250 µm pitch CPW probe and a 50 Ω line designed for 5-layer PolyStrata process. (b) S-parameter simulation results for the launch. (c) Photograph of a Cascade Microtech CPW 250-µm-pitch probe landing on a Launch.

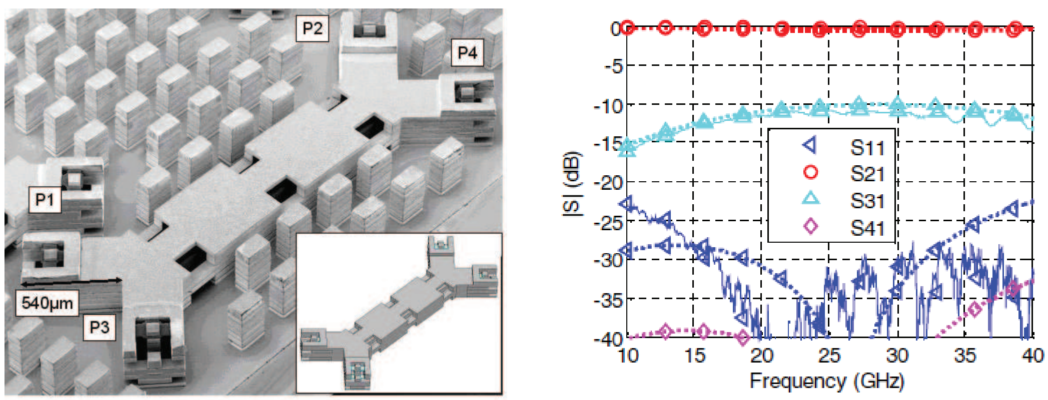
1.3.2 Components

A number of millimeter-wave components such as resonators [15, 16, 17], hybrids [18], directional couplers [19], cavity-backed patch antennae and antenna arrays [20, 21, 22, 23], log periodic antennae [24, 25], and narrowband dividers [26] have already been demonstrated with the PolyStrata process. Figures 1.5–1.9 show some of these devices.



(a) (b)

Figure 1.5: (a) SEM image of a micro-coaxial hybrid. (b) Measured and simulated s-parameter results [18]



(a) (b)

Figure 1.6: (a) SEM image of a micro-coaxial 10 dB directional coupler designed for operation centered around 26 GHz. (b) Simulated (dotted) versus measured (solid) s-parameters for a 10 dB [19].

A micro-machining process called EFAB™has been widely used to implement rectangular coaxial components [27, 28]. Several components such as band-pass filters [29, 30], resonators [31], and couplers [32, 33, 34] were designed using this technology. Figure 1.10 shows a 6-port 60 GHz coupler implemented with EFAB technology.

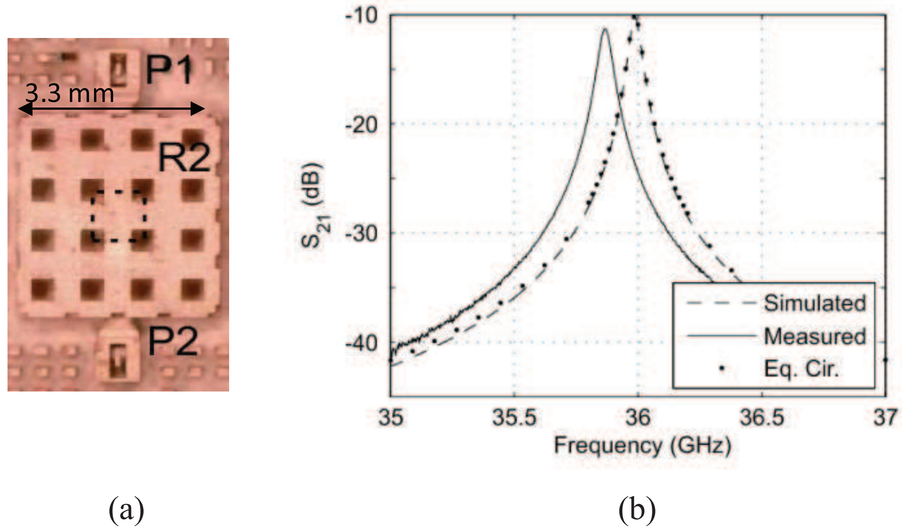


Figure 1.7: (a) A photograph of a quasi planar resonator designed for 36 GHz (b) FEM and circuit simulation results and measurement result of the resonator. The measured unloaded quality factor is 830 [15].

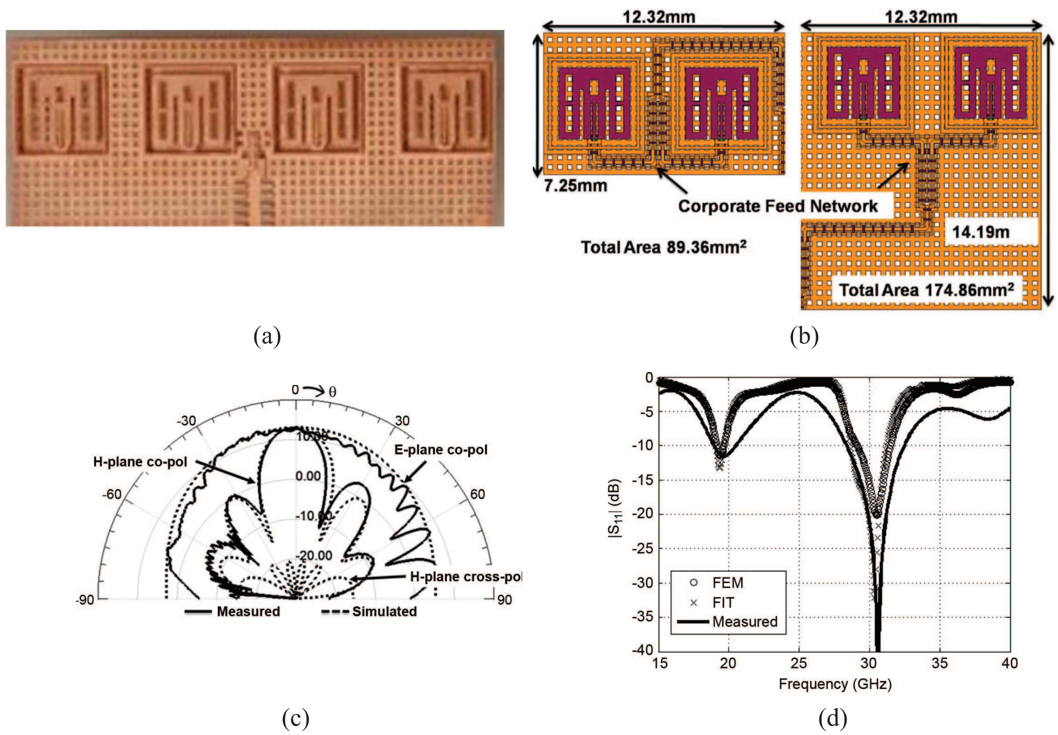


Figure 1.8: (a) Photograph of a fabricated 4×1 corporate feed cavity backed patch array with integrated micro-coax based power dividers. (b) Two corporate feed layouts: network routing between antenna patch elements (left) and a conventional configuration (right). (c) Radiation patterns at 30.23 GHz for E-plane and H-plane [26], and (d) measured and simulated S_{11} result.

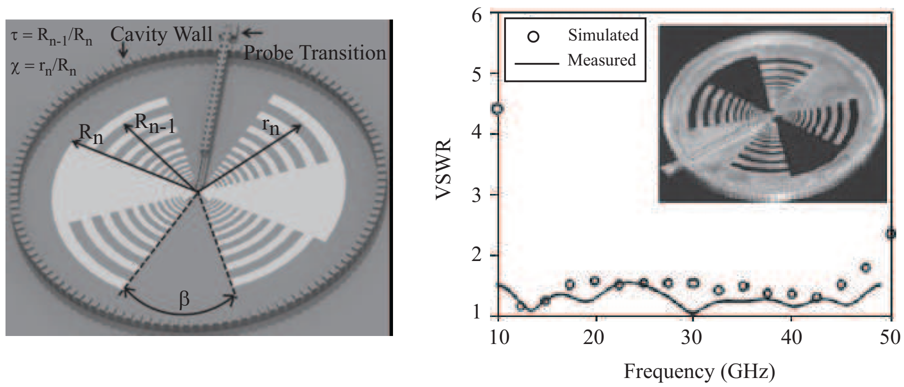
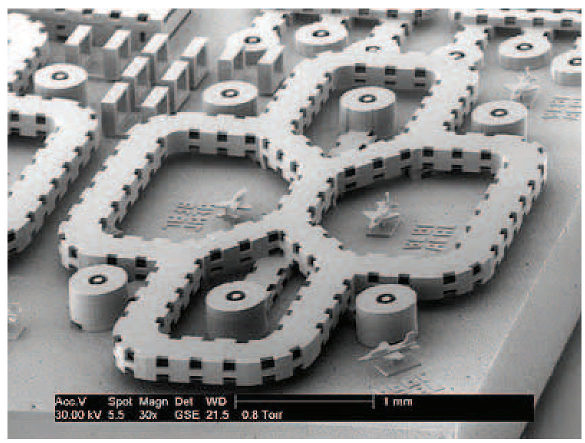
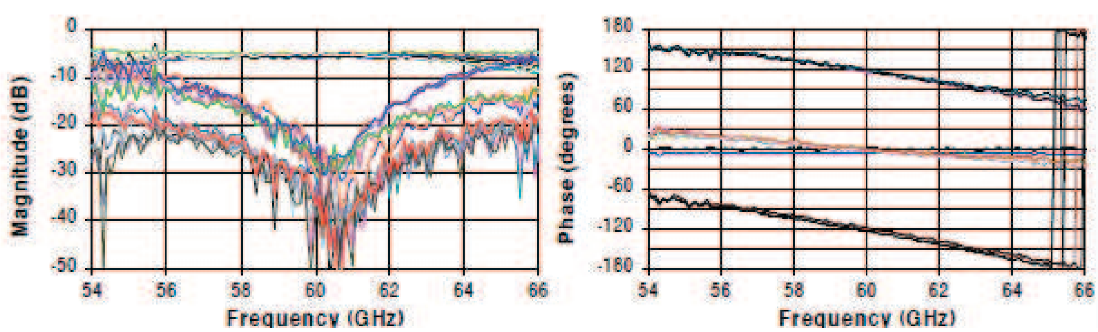


Figure 1.9: (a) Drawing of a two octave bandwidth log-periodic antenna integrated into PolyStrata. (b) Measured and simulated VSWR of the antenna [25].



(a)



(b)

Figure 1.10: (a) SEM photograph of 60 GHz 6-port coupler implemented in micromachined (EFAB) rectangular coaxial line. At 60 GHz, all signal paths of the coupler have a measured insertion loss less than 1.14 dB and a phase error of less than 3.8°. (b) Magnitude and phase s-parameter measured results [32]

1.4 Organization of this thesis

This thesis is divided into chapters as follows:

- Chapter 2 addresses fundamental properties of micro-coaxial lines for microwave broadband hybrid-monolithic integration with active and passive devices. In this chapter possible impedance ranges for different micro-coaxial cross-sections defined by processing parameters are determined. Also, calibration methods for micro-coaxial component measurements, and dc and rf power handling capabilities of micro-coaxial lines and components are presented.

- Chapter 3 demonstrates broadband Wilkinson dividers implemented in wafer-scale PolyStrata technology, which provides both low loss and small footprints simultaneously. In this chapter a comprehensive discussion of these components including full-wave design and analysis, characterization methods and measurement results are presented.

- Chapter 4 outlines the characteristics of a 4:1 Guanella transformer and its bandwidth capabilities. In particular the design procedure, and full-wave electromagnetic implementation of this transformer in the 2–24 GHz range are explained. This chapter presents the 4:1 impedance transformer performance in three different environments: air, air-filled metallic cavity, and on silicon. It also demonstrates a 2.25:1 impedance transformer, its design procedure, full-wave analysis and implementation.

- Chapter 5 presents an extension of the PolyStrata-based designs to millimeter-wave antenna arrays with frequency scanning for planetary landing systems.

An overview of scanned arrays and requirements on feed networks and antenna elements, followed by specific designs in PolyStrata technology for 1D 10–20 element slotted waveguide arrays at both W-band and G-band are presented.

- Finally, Chapter 6 summarizes the contributions of the thesis and presents some suggestions for future work. In particular, preliminary PolyStrata broadband power amplifier results are analyzed and possible improvements are suggested. Additional broadband components that can be envisioned in the PolyStrata technology are also discussed. Finally, extensions to the work on the W-band and G-band frequency-scanned arrays are presented.

Chapter 2

Micro-Coaxial Design Environment

Whatever you can do, or dream you can do begin it. Boldness has genius, power, and magic in it.

—Johann Wolfgang von Goethe

Progress lies not in enhancing what is, but in advancing toward what will be.

—Gibran Khalil Gibran

Contents

2.1 Introduction

This chapter addresses fundamental properties of micro-coaxial lines for microwave broadband hybrid-monolithic integration with active devices. In order to design, e.g., a broadband solid state power amplifier, matching circuits might require a broad range of characteristic impedances that can handle tens of watts of power with low loss.

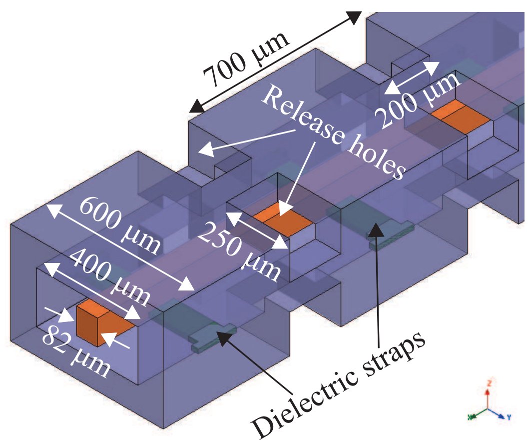


Figure 2.1: Physical geometry of a 50 Ω rectangular micro-coaxial line. The inner conductor is supported in air by periodic dielectric support straps that take up a very small percentage of the total volume, resulting in very low loss [7]. The outer conductor contains holes that serve to drain the photoresist in the last fabrication step. The aspect ratio and relative dimensions of the inner and outer conductor determine the characteristic impedance.

A section of a 50 Ω rectangular micro-coaxial line is shown in Figure 2.1 with its physical dimensions indicated. As described in 1 the Cu inner conductor is supported in air by periodic dielectric support straps. The outer conductor contains release holes that serve to drain the photoresist in the last step of the fabrication. The rf designs are constrained by fabrication requirements, which include the number of Cu layers that comprise the coaxial line, dielectric support thermal properties, aspect ratio and thickness of Cu layers and air gaps, position of release holes, and wafer/circuit layout for footprint reduction. In addition, incorporating active devices into a coaxial environment poses issues related to both monolithic and hybrid integration techniques, and the interconnects and assembly structures become a core component of the monolithic PolyStrata™ design.

2.2 Characteristic impedances available with micro-coaxial lines

As discussed in the previous chapter, the PolyStrata™ process is a sequential deposition fabrication process with Cu layers that each can vary from 10 µm–100 µm in thickness. Increasing the number of layers provides additional design flexibility, but fabrication time is directly proportional to the number of layers.

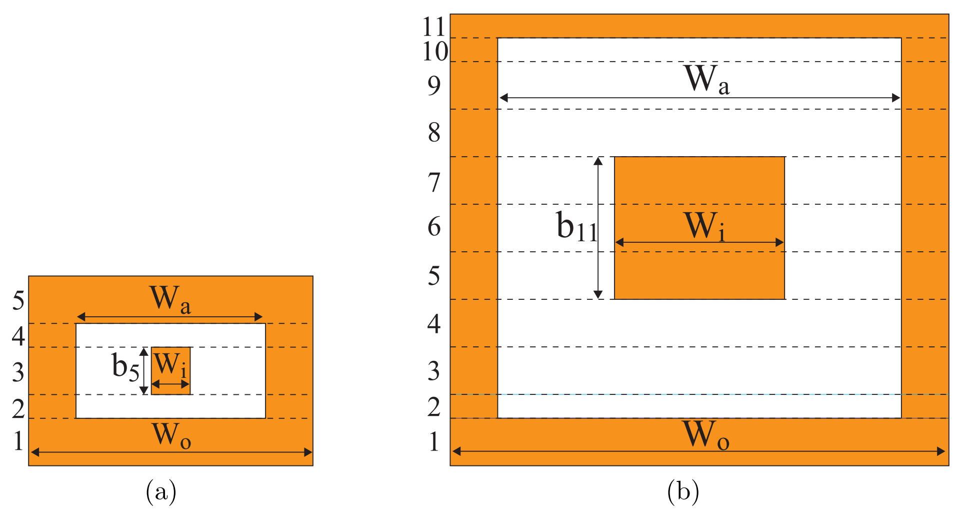


Figure 2.2: (a) Cross-section of the five-layer micro-coaxial line. The height of layers 1, 3, and 5 is 100 µm, and layers 2 and 4 are 50 µm tall. (b) Cross-section of the eleven-layer micro-coaxial line; the height of layers 2, 10, and 11 is 50 µm; all other layers are 100 µm tall.

This chapter discusses both a five-layer process that is fast and reliable, and an eleven-layer process that allows for higher power levels and more design flexibility, with cross-sections shown in Figure 2.2. The available characteristic impedances versus inner conductor widths of the two configurations are calculated using the method from [7] and are shown in Figure 2.3. The design variables b_{11} and b_5 indicate the heights of the inner conductors for the eleven-layer and the five-layer lines, respectively. The inner width of the outer conductor W_a in Figure 2.2 (b) is 1350 µm wide for the traces labeled b_{11}, and the inner width of the outer conductor W_a in Figure 2.2 (a) is 1200 µm for the trace labeled b_5.

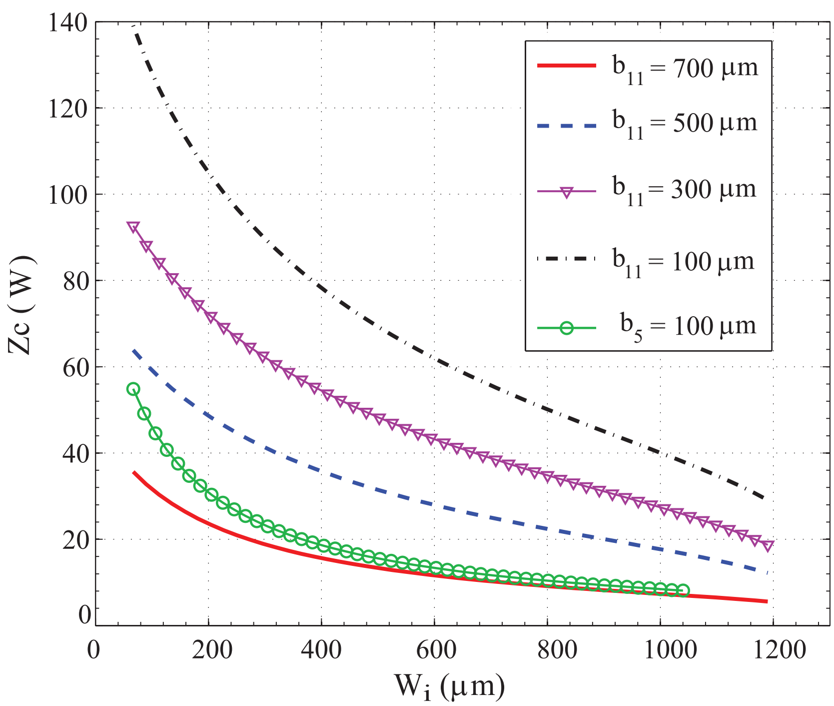


Figure 2.3: Possible characteristic impedances for the eleven-layer and five-layer micro-coaxial lines versus inner conductor widths of the eleven-layer and five-layer lines. Variables b_{11} and b_5 indicate the height of the inner conductor for the eleven-layer and five-layer lines, respectively. The traces labeled b_{11} correspond to $W_a = 1350$ µm, and the traces labeled b_5 are for $W_a = 1200$ µm.

The eleven-layer line enables greater design flexibility since the inner conductor

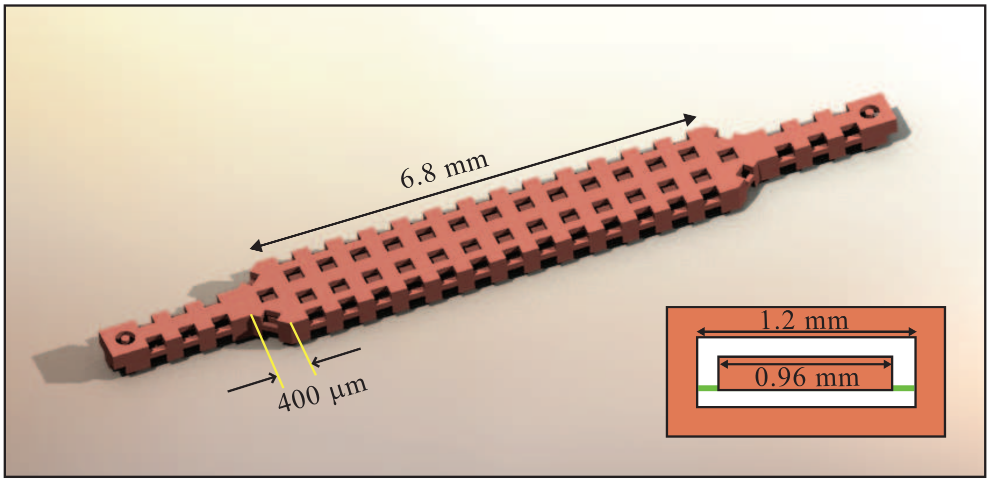


Figure 2.4: Rendered picture of an 8 Ω line connected to 50 Ω lines through 400 μm geometrical tapers. The micrograph on the bottom right shows the cross-sectional geometry of the 8 Ω line.

can be fabricated with between one and seven layers, for a total height from 100 μm to 700 μm. The resulting dimensions correspond to characteristic impedances from 6 Ω to 140 Ω. The impedance range for a five-layer line with dimensions shown in Figure 2.2 (a) with a single-layer inner conductor is 8 Ω–55 Ω.

In order to confirm the low characteristic impedances of the rectangular coaxial lines shown in Figure 2.3, an 8.8 Ω line ($W_i = 960$ μm, and $W_a = 1200$ μm) was implemented in the five-layer process. Figure 2.4 shows the rendered picture of this line connected to two 50 Ω lines through 400 μm geometrical tapers. Figure 2.5 shows the simulated vs. measured S-parameter results of the 8 Ω line terminated in 50 Ω input and output ports. This line was analyzed with Ansoft High Frequency Structure Simulator (HFSS™), a full-wave FEM simulation tool. The measurement was performed using an HP8510C network analyzer with a probe station. The calibration was performed with an on-wafer TRL calibration standard set shown in Figure 2.6 with two line lengths for the required bandwidth. Figure 2.7 (a) and (b) show the low- and high-frequency line measurements from 2 to 20 GHz. The lengths

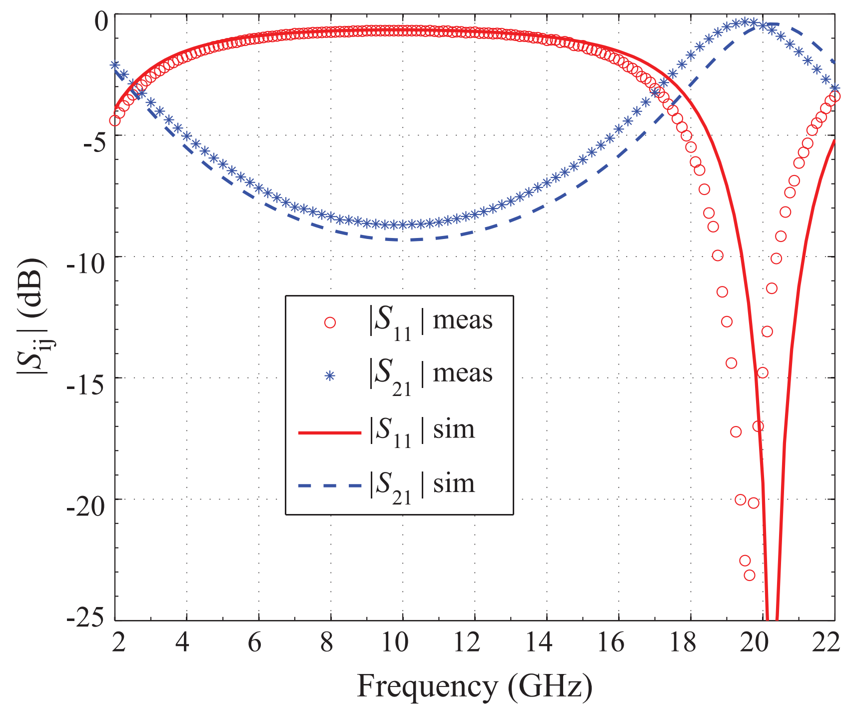


Figure 2.5: Simulation and measurement results of an 8 Ω line with 50 Ω input and output ports. These results include 50 Ω line connected through a 400 μm taper.

of the two lines are 16.8 mm and 4.9 mm, respectively.

In order to test some other characteristic impedances available with the 5-layer configuration a bandpass filter shown in Figure 2.8 was designed. This filter was first designed in Ansoft Designer and then it was implemented into micro-coaxial environment utilizing HFSS. In this design four impedances (50 Ω, 40 Ω, 35 Ω, and 30 Ω) were used. The simulated and measured result of the filter is shown in Figure 2.9.

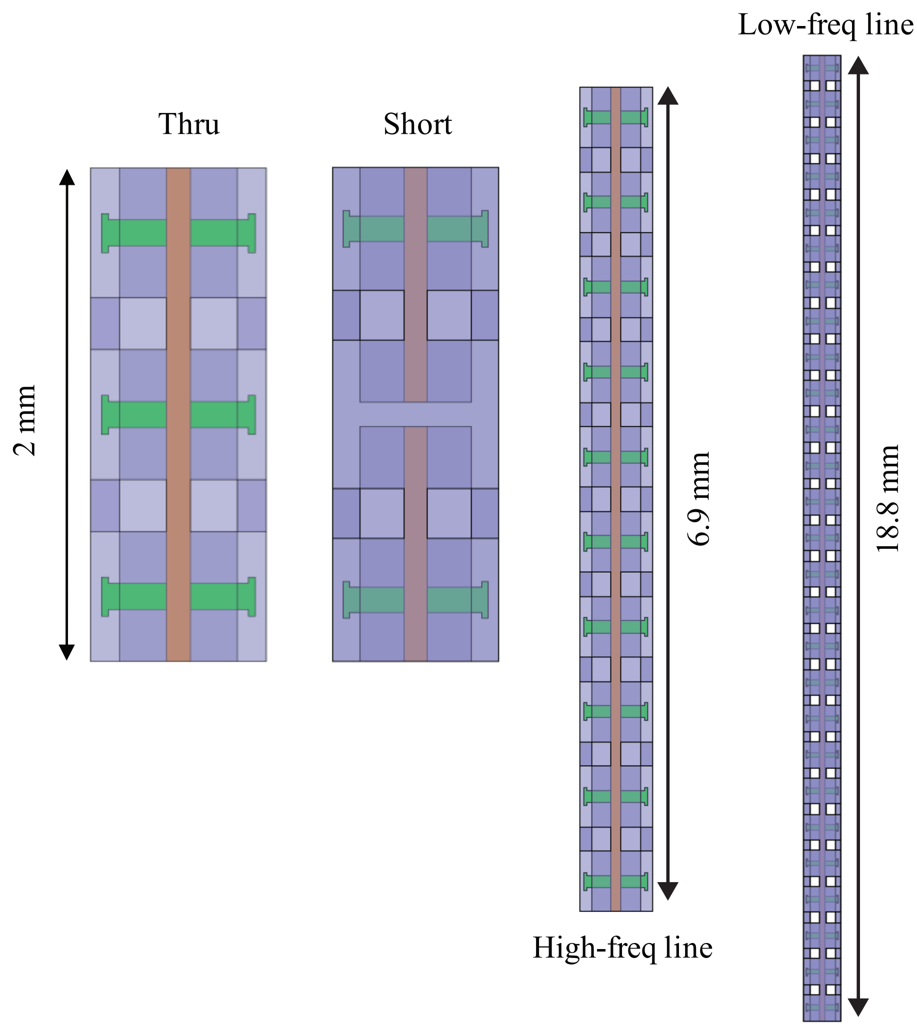
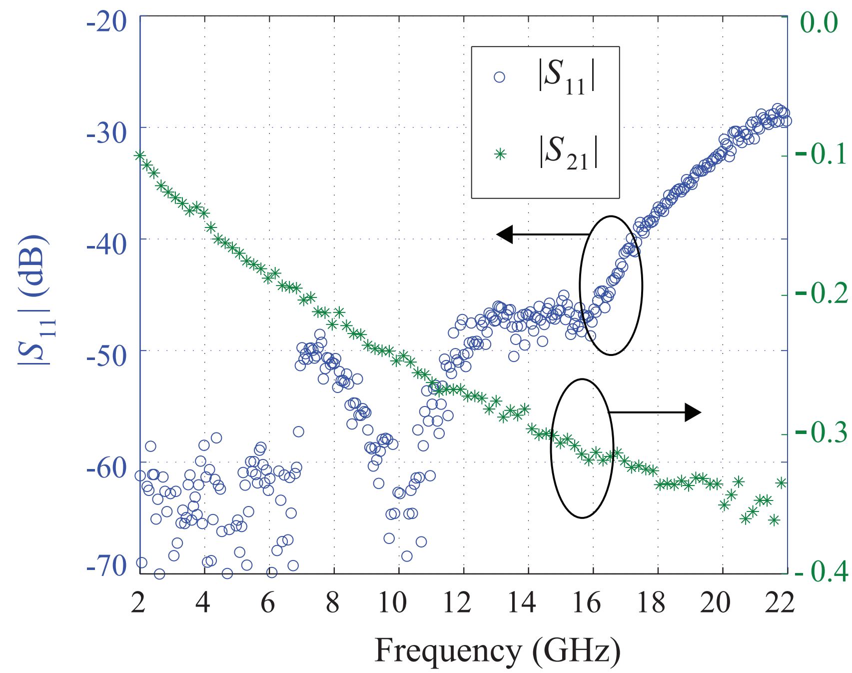
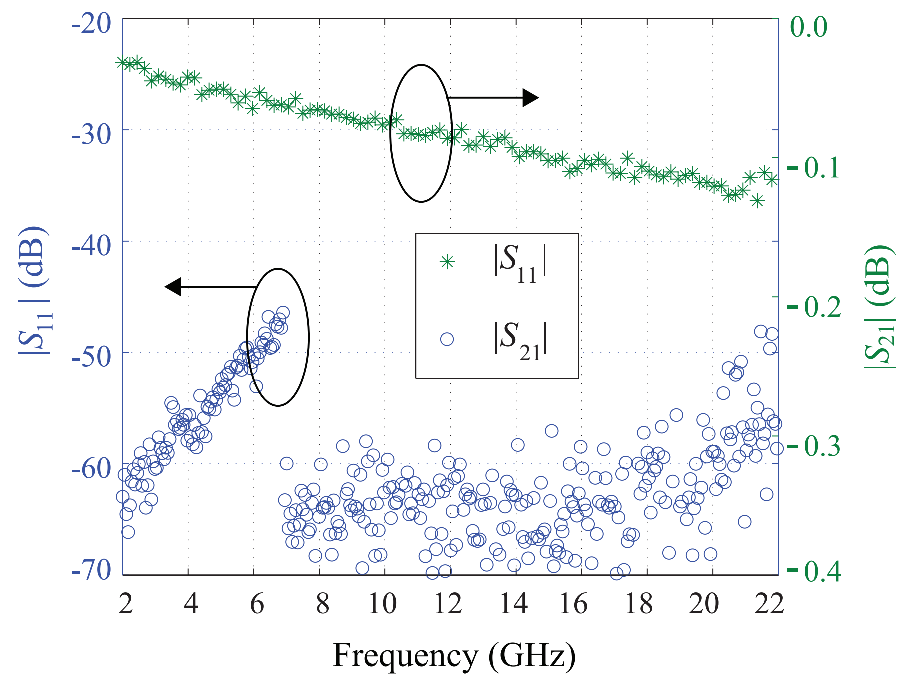


Figure 2.6: TRL standards implemented in HFSS. These standards include thru, shorts, low-frequency line, and high-frequency line. These standards are designed for frequencies between 2–22 GHz.

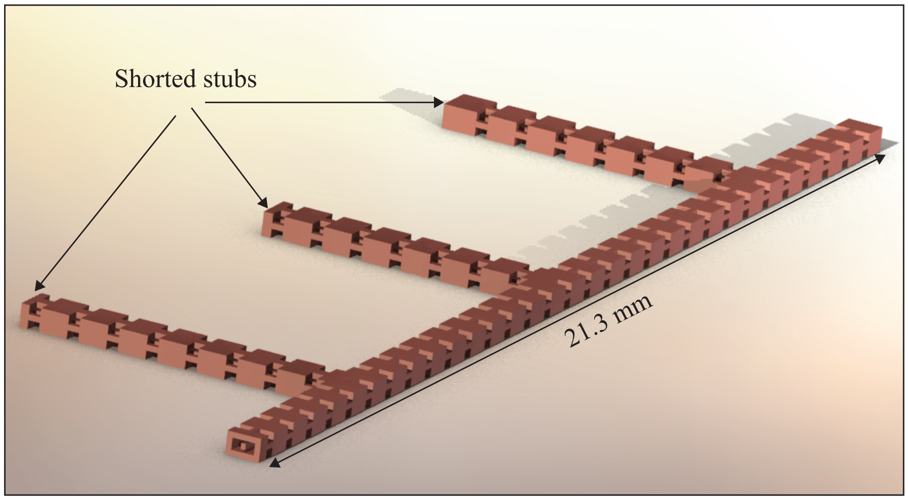


(a)

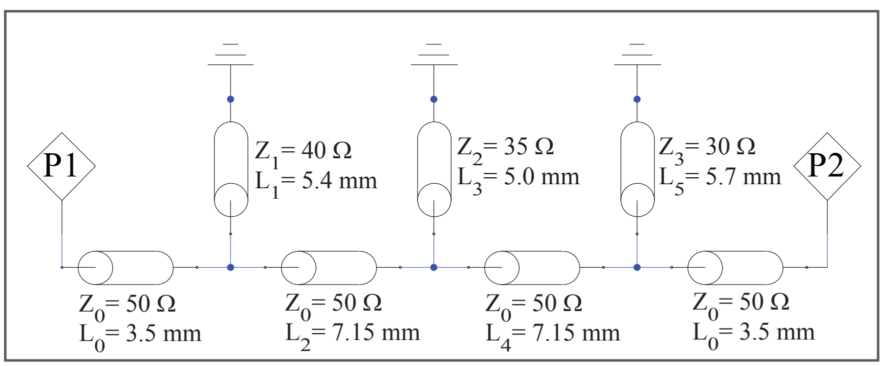


(b)

Figure 2.7: (a) Measured validation of the low-frequency TRL standard. The design frequency of this standard is 2 GHz–7 GHz. (b) Measured validation of the high-frequency TRL standard. The design frequency of this standard is 7 GHz–22 GHz.



(a)



(b)

Figure 2.8: (a) rendered picture of a band pass filter implemented in the 5-layer configuration. (b) circuit model of the filter. This filter includes three shorted stubs with three different impedances as indicated in the figure.

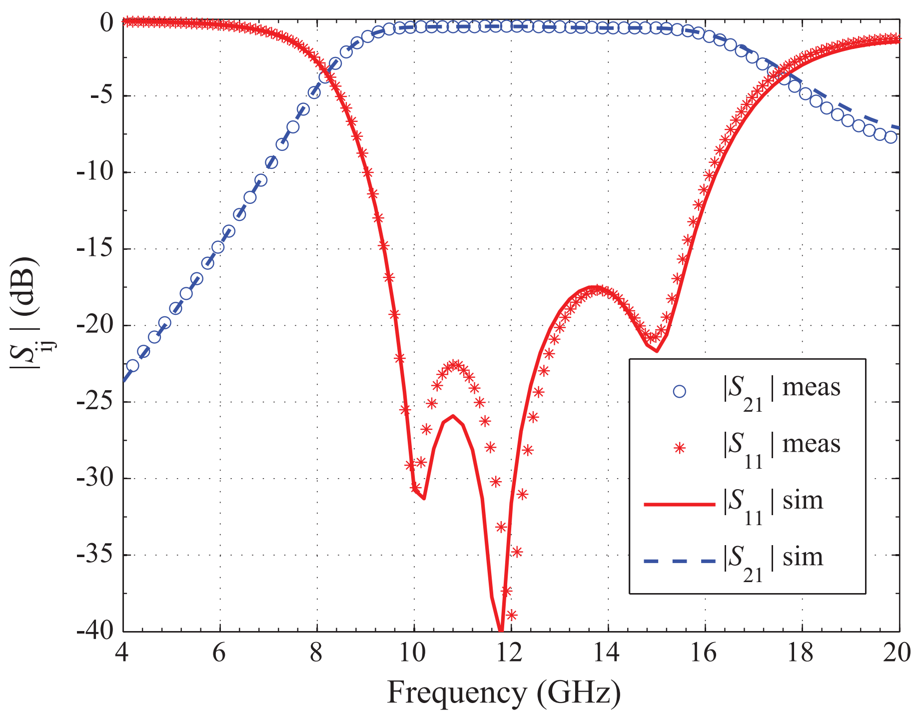


Figure 2.9: Simulated and measured s-parameter results of the filter shown in Figure 2.8.

2.3 Power handling

For biasing active components, it is critical to determine the minimum cross-section of the inner conductor that can handle the required dc current. Ohmic loss calculations show that 2.5 A of dc current necessitates an inner conductor cross-section $\geq 65\,\mu\mathrm{m}^2$, so the 100 µm minimum height shown in Figure 2.2 includes a reasonable margin of safety. The main limitations for both dc and rf power handling are the 200 °C glass-transition temperature of the dielectric straps, and electric field breakdown around sharp metal edges.

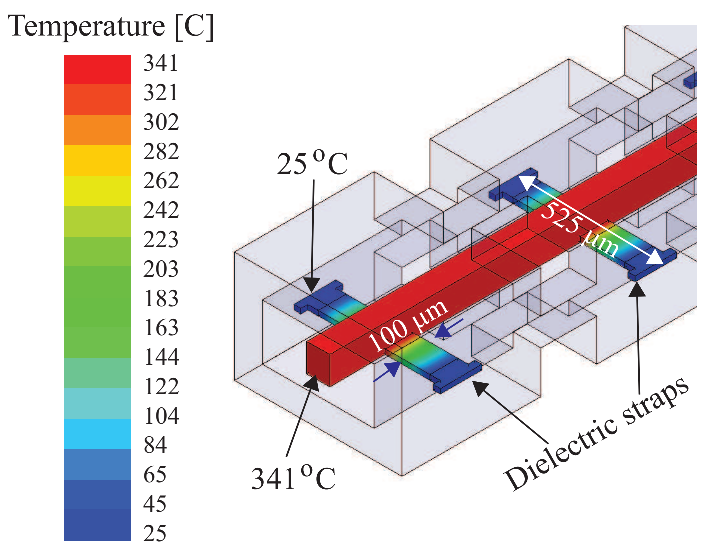


Figure 2.10: This figure shows the static thermal simulation result of the five-layer low-frequency TRL line standard. The simulation is performed with Ansoft ePhysics™ for input power of 20 W. The temperature of the inner conductor increases to 341 °C, while the outer conductor temperature is kept at 25 °C.

Static thermal simulations are performed using Ansoft ePhysics™ FEM software, assuming the temperature of the outer conductor is fixed at 25 °C and the structure is placed in an air boundary box with a fixed temperature of 25 °C. The line was first simulated at 20 GHz using HFSS™ in order to extract the conductor and dielectric losses. The plot of the temperature profile for the five-layer 50 Ω low-frequency TRL line standard is shown in Figure 2.10. The line is simulated with 100 µm wide periodic dielectric support straps that are 700 µm apart, and with release holes as shown in Figure 2.1. A comparison of maximum temperatures for the lines from Figure 2.2 is given in Table 2.1 for both 10 W and 20 W of incident power from a matched generator. Note that these are worst-case temperatures, since there is no additional heatsinking, no radiative heat transfer is taken into account, and it is assumed that there are no thermally-conductive interconnects at the two ends of the line.

Table 2.1: Static thermal analysis of 50 Ω lines at 20 GHz

Line	Power [W]	Temp [°C]
Five-layer 50 Ω	10 / 20	183 / 341
Eleven-layer 50 Ω	10 / 20	72 / 120

Electric field breakdown was estimated based on HFSS™ simulations of the electric field distribution, which show that the transverse field distribution in the case of the 8 Ω line is the strongest in the narrow air gaps, while for the 50 Ω line the field is the strongest at the inner conductor corners. Figure 2.11 shows the simulated electric field distribution at 20 GHz for the 11-layer 50 Ω and 8.8 Ω lines and 5-layer 50 Ω and 8.8 Ω lines cross-section.

For the 11-layer configuration the maximum electric field for both 8.8 Ω line and 50 Ω line are comparable. However for the 8.8 Ω line the field is concentrated between the inner and outer conductor narrow gaps, and for the 50 Ω line the field is more concentrated at the inner conductor corners. Since exact corners are not manufacturable, field break down is less likely to happen for the 50 Ω line at the same power level compare to the 8 Ω line. Due to the high concentration of the field at the narrow gaps for the 8 Ω line any manufacturing error like a flake can

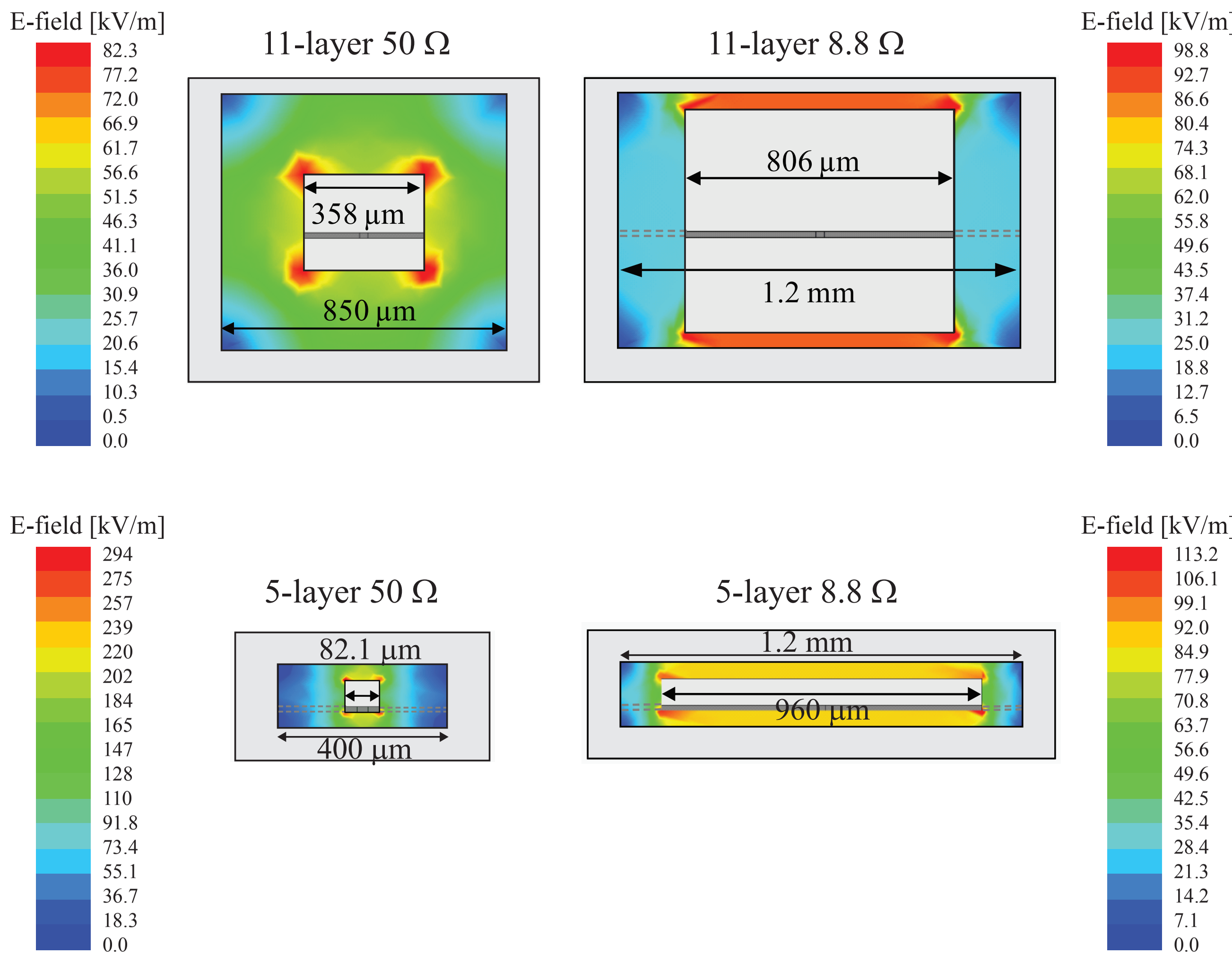


Figure 2.11: Electric field distribution at 20 GHz for 50 Ω 5-layer and 11-layer lines, and 8 Ω 5-layer and 11-layer lines.

cause electric field break down at high power level for this line.

For the 5-layer configuration although the fields are more concentrated on the vertical gaps of the 8 Ω line, the maximum of electric field distribution is much higher for the 50 Ω line, as a result the 50 Ω line will be subjected to field break down with much less input power.

Table 2.2 gives the calculated maximum electric field magnitudes for 1 W of input power from a matched generator, indicating that the low-impedance lines and smaller lines are more sensitive to breakdown. For higher power levels, $|E_{\max}|$ can be obtained by multiplying the results in the table by $(P_{\text{in}}/1\,\text{W})^{1/2}$. The maximum field for the 5-layer 50 Ω line with 120 W of input power is 3220 kV/m; based on Woo's chart [35], we expect to observe field break down for this line at this power level.

Table 2.2: Calculated maximum electric field, $P_{\text{in}} = 1\,\text{W}$

Line	5 layer 8 Ω	5 layer 50 Ω	11 layer 8 Ω	11 layer 50 Ω
$\lvert E_{\max}\rvert$ [V/m]	$1.13 \cdot 10^5$	$2.94 \cdot 10^5$	$0.99 \cdot 10^5$	$0.82 \cdot 10^5$

The power handling capability measurements for multiple lines were performed at BAE Systems. The results are added to this chapter for completeness and for confirmation of the simulation results.

Power handling at 2 GHz was tested on a 15 mm long 50 Ω five-layer open-ended line, connected with a bond wire to a 0.085" (2.16 mm) diameter semi-rigid coaxial cable. Up to 12.6 W of CW power, resulting in 78 V estimated at the open end was input to the line for 45 min with no observed degradation.

Up to 300 W of 10 % duty cycle 10 ms period pulsed power was input into a 15 mm line using the test setup shown in Figure 2.12. These measurements

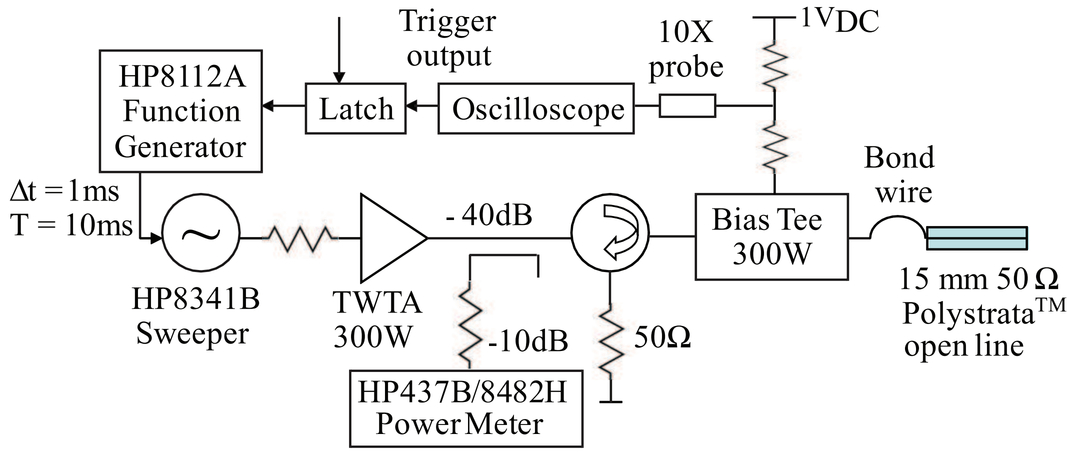


Figure 2.12: Measurement setup for rf field breakdown; testing performed with an open-ended 50 Ω line with up to 300 W of input power at 10 % duty cycle (1 ms duration pulses). Ionization provides a dc path through the bias tee. The detection of arcing automatically turns off the rf source, protecting the micro-coaxial line and allowing multiple tests.

reduce thermal stress on the open-ended micro-coaxial line, while enabling rf field breakdown testing up to 18 GHz. When voltage breakdown occurs, ionization creates a path for dc current to flow through the bias tee choke, creating a voltage drop measured by the oscilloscope with trigger set on a falling edge. When the oscilloscope triggers, the latch output resets, turning off the pulse generator. When the modulation is not present, the sweeper turns off, thus detecting breakdown and protecting the micro-coaxial line from damage. No arcing was detected at the test frequency of 2.5 GHz for power levels below 53 W, the level when a single arc occurred. Multiple arcs were observed at 120 W and 150 W, and arcing at 300 W resulted in catastrophic failure. Based on simulations and previous work by Woo [35], breakdown will likely not occur for an ideal micro-coaxial line until 120 W. The lower power level at which breakdown occurred is presumably due to an imperfect conductor surface.

In summary, this chapter demonstrates properties of TEM micro-coaxial lines, including wide impedance range, dc current handling, CW and pulsed rf power handling [4, 36]. These results open the possibility for PolyStrata™ integration with high power active devices for broadband hybrid-monolithic ultra-compact solid-state power amplifiers.

Chapter 3

Broadband Micro-Coaxial Wilkinson Power Dividers/Combiners

Genius is one per cent inspiration, ninety-nine per cent perspiration.

—Thomas A. Edison

Free thinkers are those who are willing to use their minds without prejudice and without fearing to understand things that clash with their own customs, privileges, or beliefs.

—Leo Nikolayevich Tolstoy

Contents

3.1 Introduction

The Wilkinson power divider was first introduced in 1960 as a distributed N-way circuit with $N-1$ lumped resistors [37]. Various distributed and lumped extensions of this in-phase high-isolation divider have been researched to date [38, 39, 40]. For a single-section two-way divider the bandwidth is around 3:1 for a VSWR of 2:1. Several methods have been developed to increase the bandwidth of such dividers. In 1968, Cohn introduced a multi-section divider, containing M pairs of equal-length transmission lines in series and M shunt resistors between the pairs [41]. Figure 3.1 shows this general multi-section divider. Cohn found the reflection and transmission coefficients based on even and odd modes analysis. Figure 3.2 shows the even and odd mode circuits for the general multi-section divider. For the even mode two waves with equal amplitude and phase are incident to ports 2 and 3 resulting in no current flow through the resistors [42, pages 319–321]; thus we can bisect the circuit of Figure 3.1 with open circuits in the middle to obtain the circuit shown in Figure 3.2 (a). For the odd mode two waves with equal amplitude and 180° phase difference are incident to ports 2 and 3 which resulting a voltage null along the middle of the circuit in Figure 3.1. Thus we can bisect the circuit to the circuit shown in Figure 3.2 (b).

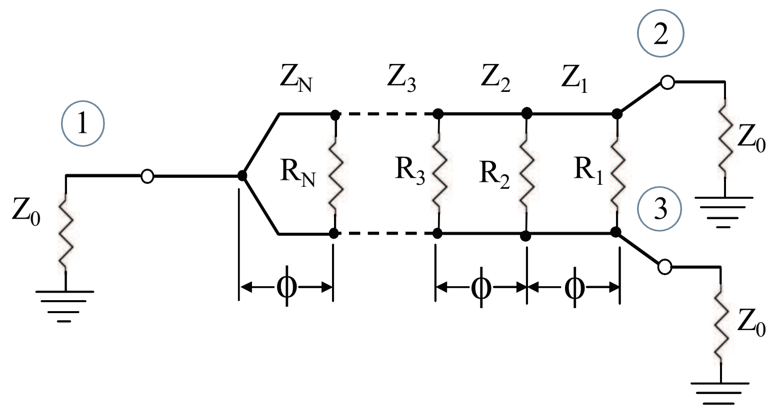


Figure 3.1: General multi-section broadband divider [41].

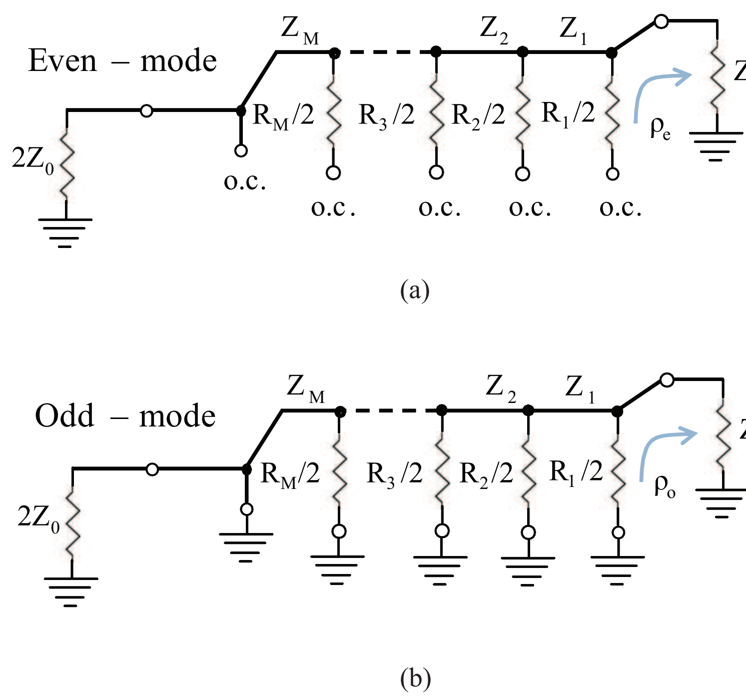


Figure 3.2: Bisection of the circuit shown in Figure 3.1. (a)Even mode and (b) odd mode excitations.

The following characteristics are realized for reflection and transmission coefficients of the general multi-section divider with respect to even mode reflection (ρ_e) and odd mode reflection (ρ_o) [41]:

$$|\rho_1| = |\rho_e|, \tag{3.1}$$

$$t_{12} = t_{13}; |t_{12}| = |t_{13}| = \sqrt{\frac{1}{2}(1 - \rho_e^2)}, \tag{3.2}$$

$$\rho_2 = \rho_3 = \frac{1}{2}(\rho_e + \rho_o), \tag{3.3}$$

$$t_{23} = \frac{1}{2}(\rho_e - \rho_o) \tag{3.4}$$

where ρ_1, ρ_2, and ρ_3 are reflection coefficients at port 1, port 2, and port 3, respectively; and t_{12}, t_{13}, and t_{23} are transmission coefficients between ports 1&2, 1&3, and 2&3, respectively. Cohn wrote an algorithm to optimize ρ_1, ρ_2, ρ_3, and t_{12} for equal-ripple Tchebychev behavior. This divider can theoretically achieve 10:1 bandwidth with $M = 7$, with a characteristic impedance range of 90 Ω–50 Ω and resistor values of 100 Ω–600 Ω. High isolation can be maintained between output ports over a broad bandwidth.

Other broadband Wilkinson-type dividers are designed mostly in microstrip [43]. Algorithms to find the correct number of sections, characteristic impedances and lumped resistor values are given for ideal components [44, 45]. The greatest experimentally demonstrated bandwidth with the Wilkinson divider to the best of the authors' knowledge is 4:1 (3–12 GHz) using a strip-line configuration with four sections [44].

The goal of this chapter is to demonstrate broadband Wilkinson dividers implemented in wafer-scale PolyStrata technology, which provides both low loss and small footprints simultaneously; the latter is illustrated in Figure 3.3. The low dispersion, low loss and high isolation properties of micro-coaxial lines as discussed in Chapter 2, makes the PolyStrata process uniquely suitable for ultra-broadband

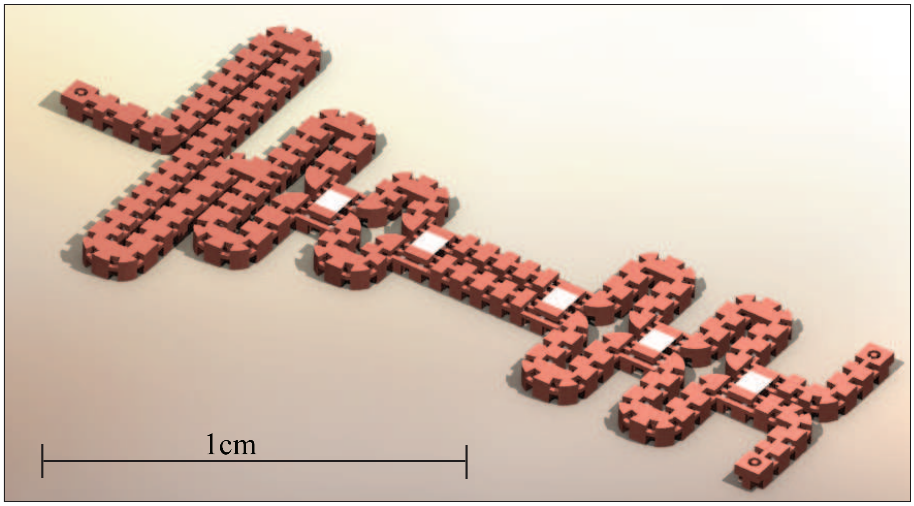


Figure 3.3: Rendering of the miniaturized 2–22 GHz Wilkinson divider implemented in the five-layer fabrication process described in Chapter 2.

miniaturized components, such as the 11:1 bandwidth Wilkinson divider/combiner presented here.

Since a Wilkinson divider requires resistors, in this work we demonstrate for the first time specially designed three-dimensional surface mount pads for hybrid integration of 0402 and 0303 standard packaged resistors. This hybrid assembly method can be extended to other lumped passive and active components. The dividers utilize the available discrete values of surface-mount broadband resistors, and follow the constraints of the PolyStrata fabrication rules, which determine the achievable characteristic impedances and the overall size of the circuit.

3.2 Design Procedure

As mentioned in Section I, a general broadband Wilkinson divider consists of M pairs of transmission lines with shunt resistors between them [41]. The number of sections, characteristic impedances, and resistor values determine the bandwidth.

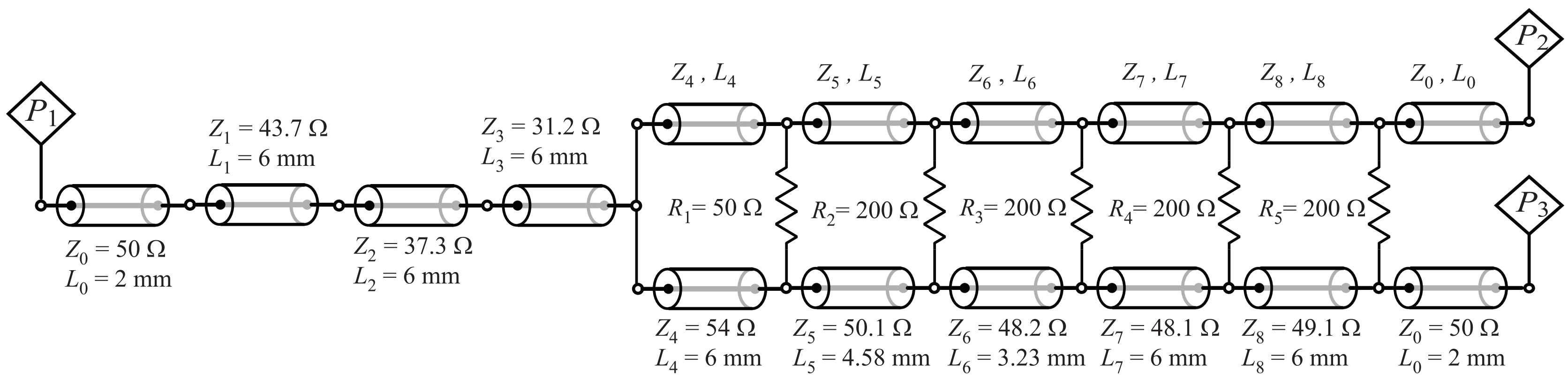


Figure 3.4: Circuit schematic of the broadband Wilkinson divider with indicated characteristic impedances, lengths, and resistor values. This model consists of five pairs of transmission lines with five resistors between each pair. The input transmission line is composed of four sections.

Since Cohn's basic design of a 50 Ω Wilkinson requires impedances greater than those available with the layer configuration shown in Figure 2.2 (a), we chose to transform the input impedance of 50 Ω to a lower impedance at the point of the division. Port one is therefore composed of several sections of line with impedances varying from 50 Ω to approximately 30 Ω. A constraint of 54 Ω was placed on the maximum allowable impedance for all transmission line sections in Figure 3.4, and Ansoft Designer was used to optimize the divider with $Z_0 = 50\,\Omega$ input and output ports. Figure 3.4 shows the circuit model, in which the characteristic impedances and the lengths of the transmission lines are chosen from the results of the optimization process, and the resistors in between them are chosen based on the availability of resistor values in 0402 and 0303 packages. Due to the impedance constraint, six transmission line sections were required to achieve the desired return loss and isolation over the desired bandwidth.

The circuit from Figure 3.4 was modeled in Ansoft High-Frequency Structure Simulator (HFSS) for the five-layer process and in a straight geometry (unlike

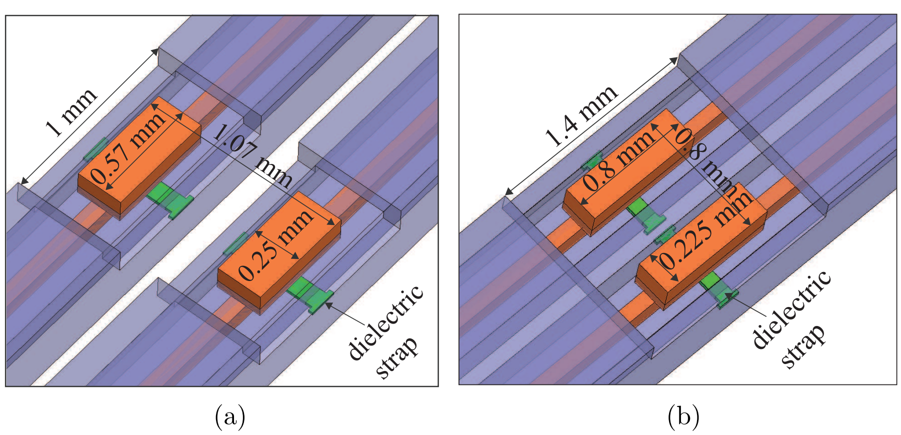


Figure 3.5: Full-wave simulation model of two passive sockets designed for a shunt (a) 0402 and (b) 0303 chip resistor package. The lumped resistor is connected between the two pads; for (b) the two micro-coaxial lines share an outer conductor wall.

the reduced-footprint version shown in Figure 3.3). The cross-sections of each transmission line section are calculated using the method from [7]. In order to place surface mount resistors in shunt between transmission line sections, 3D assembly pads, referred to as "passive sockets," are designed for both 0303 and 0402 standard packages, as shown in Figure 3.5. The design of the passive sockets depends on the cross-sectional geometry of the transmission lines at the location where the socket is placed. If the field distribution is concentrated in the upper gap (layer 4), designing the sockets becomes more difficult due to field leakage from the open area of the outer conductor. Since the fields were not very concentrated in the upper gap layer, there was not much difficulty in this design. This issue will be discussed in more detail for a divider with input and output ports of $12.5\,\Omega$ in Chapter 6.

In the Finite Element Method (FEM) simulation, the resistors are modeled as purely resistive impedance sheets. Figure 3.6 shows the comparison between circuit simulations and the FEM results with the 0303 resistor packages. For the circuit model, ideal transmission lines and resistors are used; however, in the HFSS model, the conductor losses, as well as parasitics due to the "passive sockets" and resistors are taken into account, resulting in increased insertion loss. This device has a VSWR better than 2:1 from 2–22 GHz, and a better than 20 dB return loss and isolation from 4–18 GHz.

3.2.1 Miniaturization

In order to reduce the footprint of the straight Wilkinson divider, we miniaturized it by bending the transmission lines as shown in Figure 3.3 (a). The length of

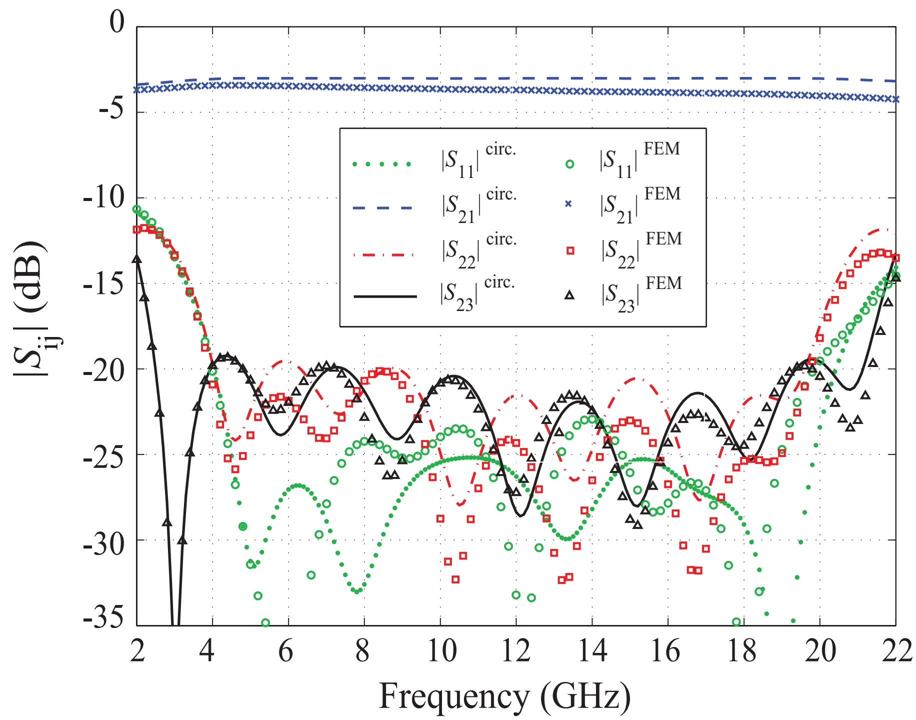


Figure 3.6: FEM and circuit simulation comparison. $|S_{21}|^{\text{circ.}}$ and $|S_{21}|^{\text{FEM}}$ are $-3.02\,\text{dB}$ and -3.70 dB at 12 GHz respectively. Conductor losses are not taken into account in the circuit simulator.

the miniaturized divider is 18 mm, significantly less than the 48 mm long straight divider. This is facilitated by the high isolation between adjacent micro-coaxial lines [8] and judicious EM design of the tight bends. The difficulties encountered during the design of the miniaturized Wilkinson divider include maintaining the characteristic impedances of the transmission lines through the curves and careful design of the passive sockets.

3.3 Prototype Performance

Figure 3.7 contains photographs of a fabricated straight Wilkinson divider, a passive socket for 0303 package surface mount component, and a miniaturized Wilkinson divider. The dividers were measured with an Agilent E8364B PNA four-port

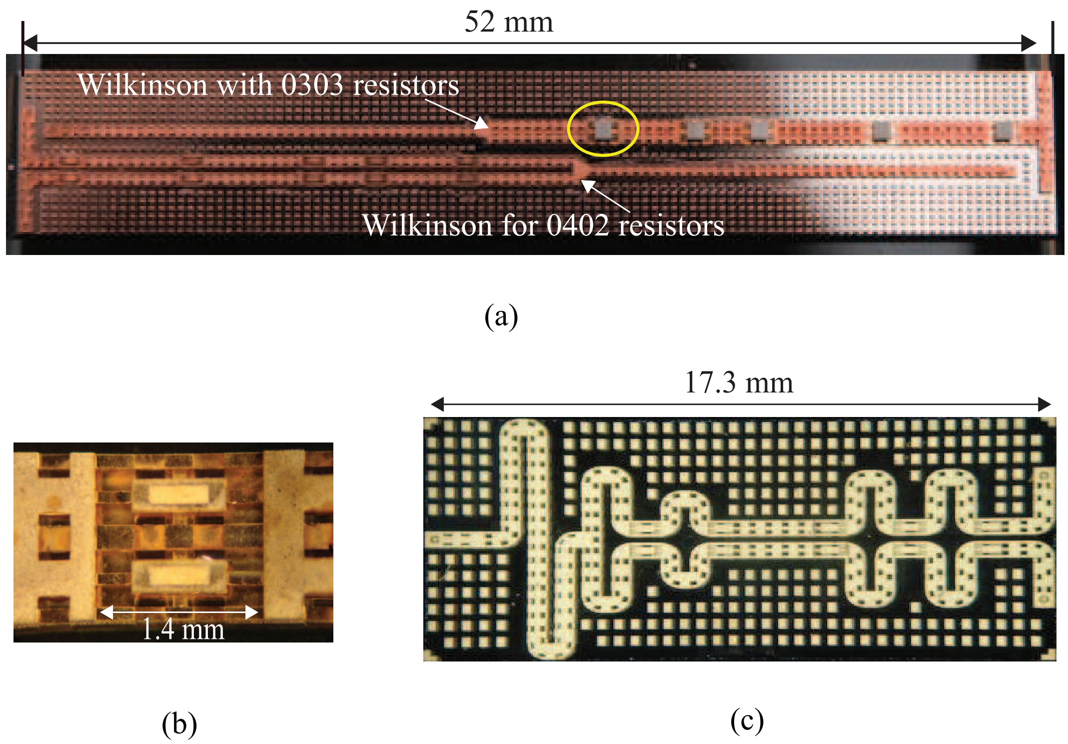
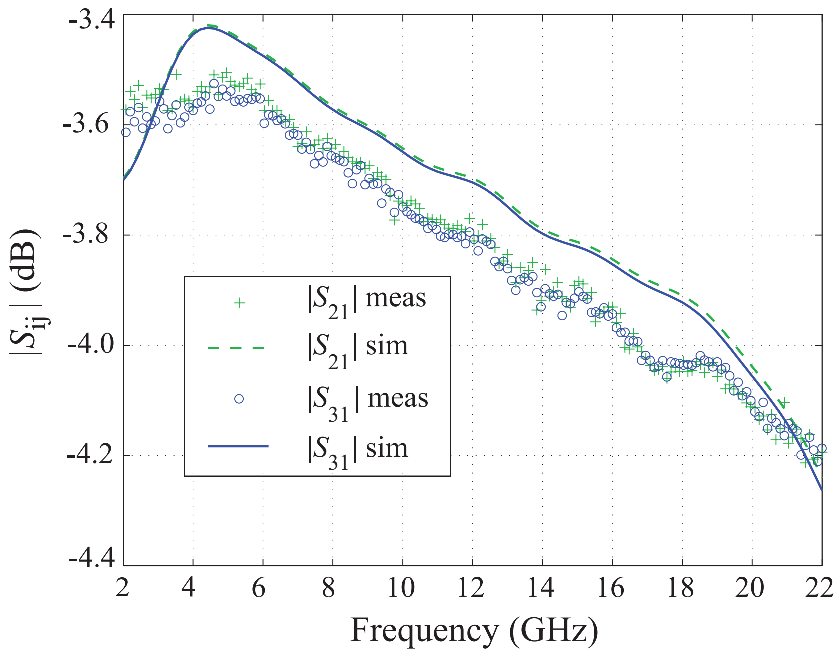
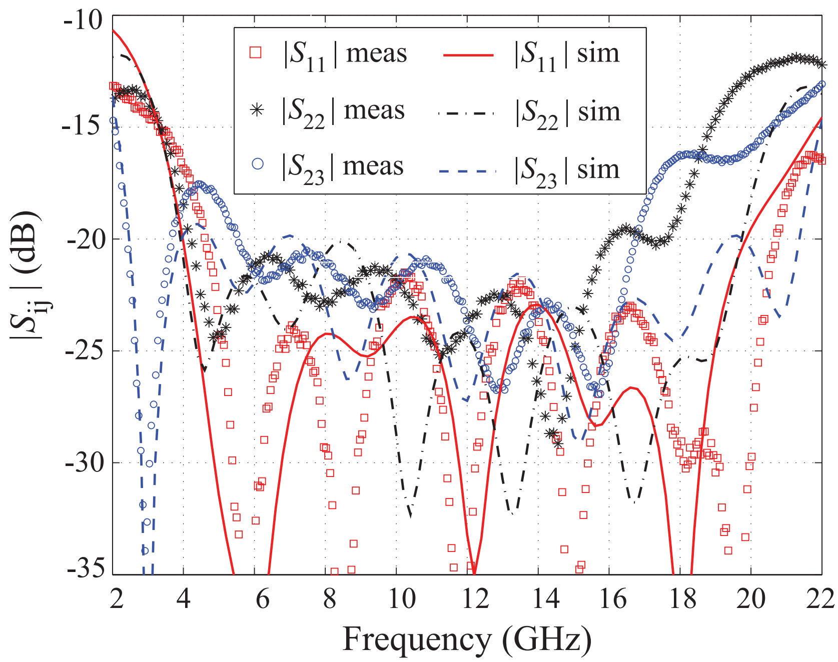


Figure 3.7: (a) Photograph of the fabricated straight Wilkinson divider for both 0402 and 0303 sockets. Resistors are mounted on the divider with 0303 passive sockets. (b) Photograph of an 0303 passive socket with no resistor. (c) Photograph of the fabricated miniaturized Wilkinson divider.

network analyzer, Cascade Microtech 250-µm pitch CPW microwave probes, and a Cascade Summit 9000 probe station. Two calibration methods were performed; the first was a three-port short-open-load-through (SOLT) implemented in CPW on an alumina substrate. This calibration method removes the effect of the cables and probes up to the probe tips. The straight Wilkinson divider was measured with this calibration method; Figure 3.8 (a) and (b) show the comparison between s-parameter simulation and measurement results of this divider. One possible reason for the reduced performance in measured $|S_{23}|$ and $|S_{22}|$ above 16 GHz is imperfection in the manual mounting and positioning of the resistors in the sockets.



(a)



(b)

Figure 3.8: ((a) $|S_{21}|$ & $|S_{31}|$ and (b) return loss & isolation for the straight divider.

A broadband Wilkinson divider ideally has no amplitude or phase imbalance due to perfect symmetry [41]. In the actual circuit, however, due to fabrication imperfection the symmetry is broken and the measured amplitude and phase imbalance are calculated from

$$\Delta|S| = |S_{31}| - |S_{21}| \qquad \text{[dB]}, \tag{3.5}$$

and

$$\Delta\phi = \angle S_{31} - \angle S_{21} \qquad \text{[deg]}. \tag{3.6}$$

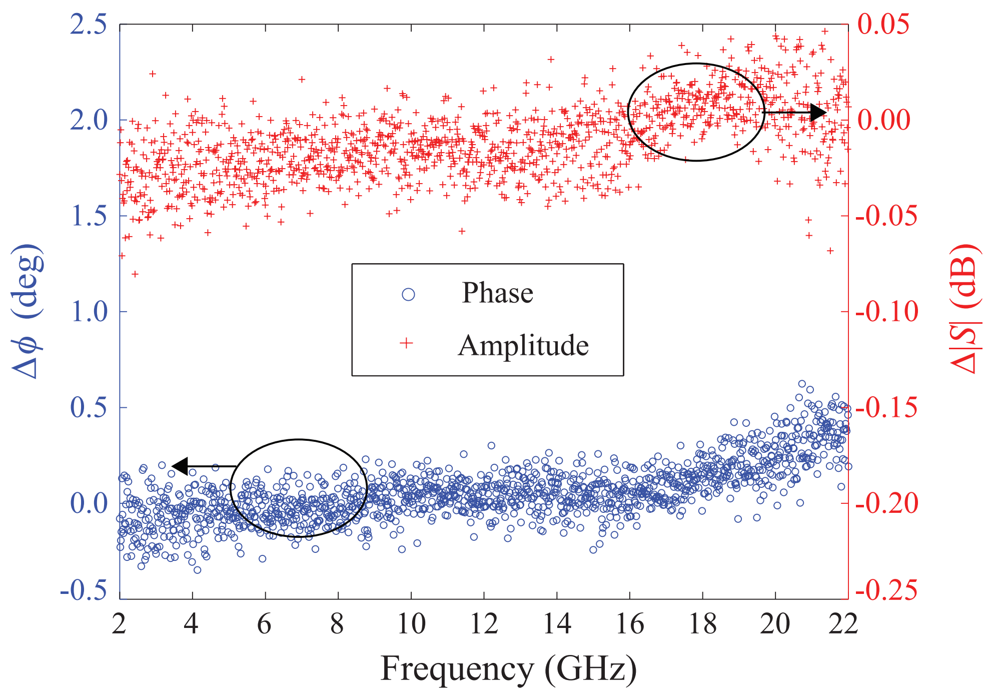


Figure 3.9: Measured phase and amplitude imbalance for straight divider; note that the scale covers 1° in phase and 0.1 dB in amplitude.

Figure 3.9 shows the measured amplitude and phase imbalance of the straight Wilkinson divider. The phase imbalance is better than 1° and the amplitude imbalance is better than 0.1 dB.

The second calibration method is performed via an on-wafer PolyStrata TRL calibration standards that were designed exclusively for the miniaturized Wilkinson divider. The bent TRL standards, include short, thru, and two lines to cover the desired bandwidth as shown in Figure 3.10, and their mirrored version for three port calibration. This calibration method creates the error boxes A, B, and C that are shown in Figure 3.11. TRL calibration method removes the effect of the cables, probes, and probe to PolyStrata transition. The three-port TRL calibration method, is performed like two TRL calibrations. One calibration is done between port 1 and 2 to create error boxes A and B. The second calibration is done between port 1 and 3 to create error box C. The miniaturized Wilkinson divider was calibrated through this method; specifically, the divider was measured with the PNA using the three-port TRL calibration and three 250-μm pitch CPW microwave probes. Figure 3.12 shows the comparison between simulated and measured results of the miniaturized Wilkinson divider. Measured amplitude and phase imbalance, from (3.5) and (3.6), are $< 0.1\,\text{dB}$ and $< 1^{\circ}$, respectively.

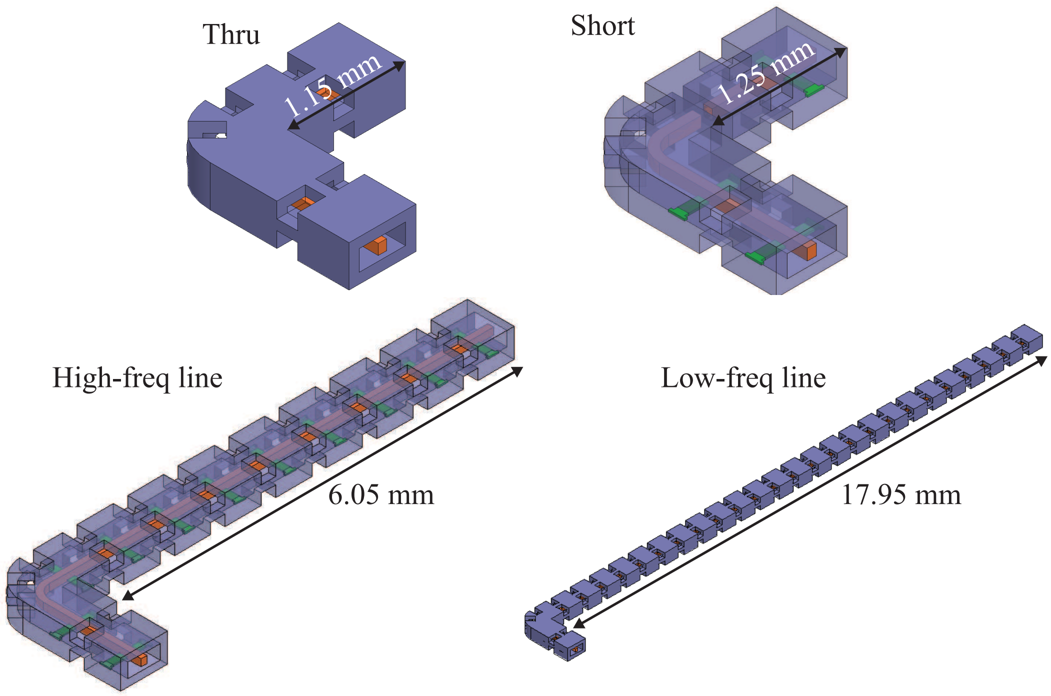


Figure 3.10: Bent TRL standards designed for miniaturized Wilkinson divider, for three-port measurement. Each standard has mirrored version as well, which is not shown in this figure.

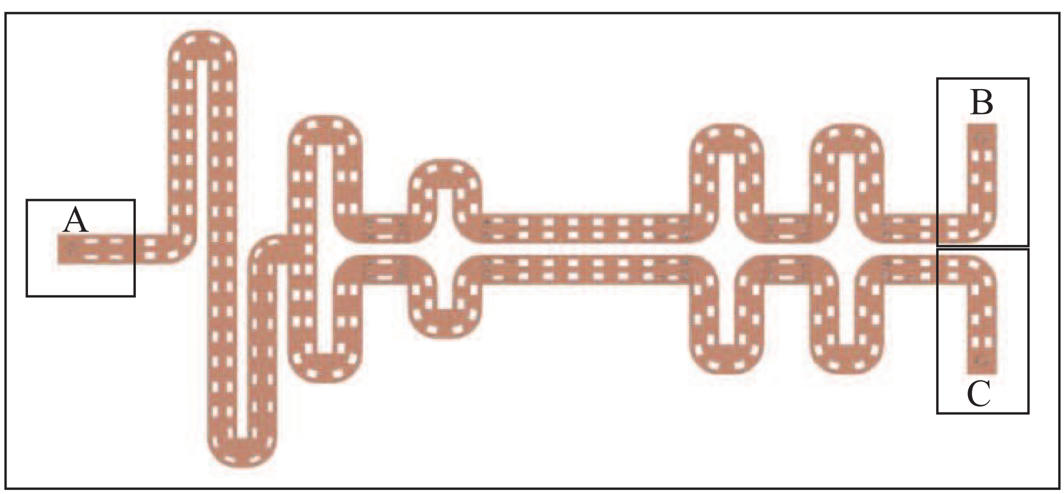


Figure 3.11: Error boxes created with the bent TRL standards. The three-port TRL calibration method, is performed like two TRL calibrations. One calibration is done between port 1 and 2 to create error boxes A and B. The second calibration is done between port 1 and 3 to create error box C.

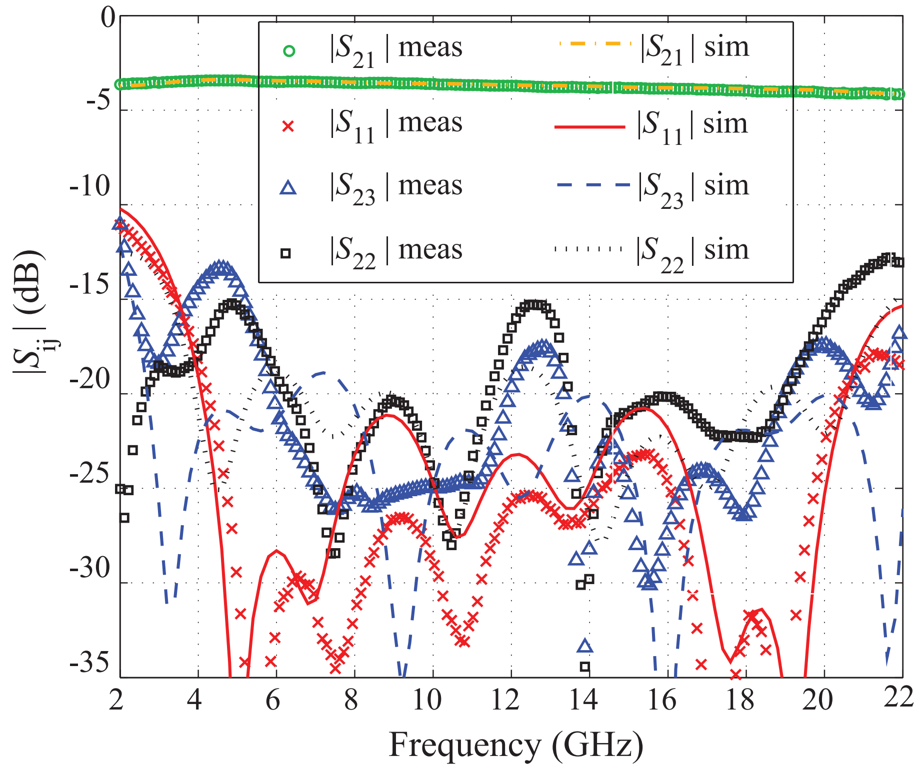


Figure 3.12: Simulated and measured s-parameter results of the miniaturized Wilkinson divider with 0402 resistors. Measured $|S_{21}|$ at 12 GHz is −3.71 dB.

3.4 Power Considerations

3.4.1 Effect of Mismatched Loads

In an ideal Wilkinson power divider, the current in the resistors is zero. However, this is not the case when there are slight mismatches at the output ports, or in the worst case, when a device or line at an output port fails as short or open. It is important to know how much current can flow through the resistors for specific mismatches, in order to select a resistor with appropriate power handling characteristics. Both the output port mismatches and the current flow in the resistor are investigated for the ideal broadband divider shown schematically in Figure 3.4. Table 3.1 gives the RMS current in each resistor for different output port impedances ranging from 40 Ω to 60 Ω, with 1 W of input power at 10 GHz. The maximum current in the resistors for 60 Ω and 40 Ω loads at the two ports is 4.71 mA, in $R_1 = 50\,\Omega$. Figure 3.13 shows the simulated transient response of the current flow in each resistor for this case. The transient analysis was performed with a circuit simulator for 2 ns duration in 0.1 ps steps. Note that R_5 is the first resistor into which the current flows, since this resistor is closest to the mismatched output ports. The selected 0402 (USMRG2040AN) and 0303 (USMRG3000AN) resistors can dissipate 3.45 W and 3.89 W, respectively, providing a significant safety margin.

3.4.2 RF Power Handling

The power handling capability of the dividers in this chapter is limited primarily by the transmission lines' thermal and electrical breakdown limits as discussed in detail

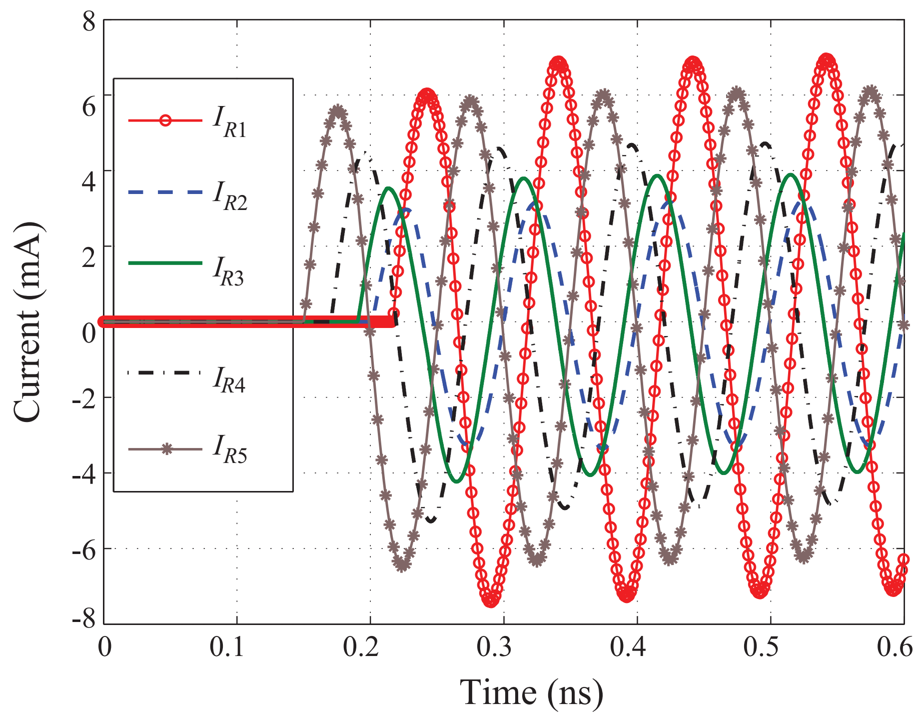


Figure 3.13: Transient response simulation from $t = 0$ ns to $t = 0.6$ ns of current in each resistor. Ports 2 and 3 are connected to 40 Ω and 60 Ω loads, respectively. The analysis was performed for 2 ns duration with 0.1 ps steps.

Table 3.1: RMS current through resistors for 1 W input power and various load mismatches

$R_{L(2,3)}$ [Ω]	40,50	45,50	40,55	45,55	40,60	45,60
I_{R1} [mA]	2.60	1.23	3.71	2.34	4.71	3.33
I_{R2} [mA]	1.19	0.56	1.71	1.08	2.17	1.54
I_{R3} [mA]	1.46	0.69	2.08	1.31	2.64	1.87
I_{R4} [mA]	1.79	0.85	2.56	1.61	3.25	2.30
I_{R5} [mA]	2.32	1.09	3.31	2.08	4.20	2.98

previously in Chapter 2. In that work, it was concluded that the electrical breakdown limit of 120 W for the five-layer 50 Ω line is significantly above the thermal limits. Micro-coaxial lines with larger cross-sections allow greater power handling capability, increased design flexibility, and lower insertion loss. Figure 2.2 (b) shows the cross-section of such a line, with eleven layers. The available characteristic impedances for micro-coaxial lines with the eleven-layer configuration range from 6 Ω to 140 Ω.

A broadband miniaturized micro-coaxial Wilkinson divider was designed and fabricated with this larger cross-section line. Figure 3.14 shows the circuit schematic of this divider, which consists of four parallel transmission lines and four resistors in the divider section, and three transmission lines sections in the input line; Table 3.2 shows their values.

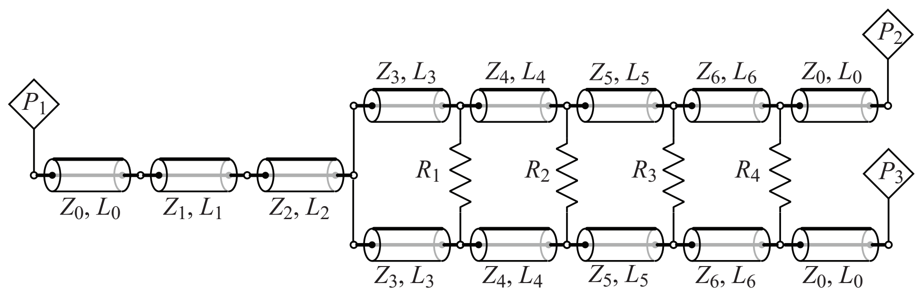
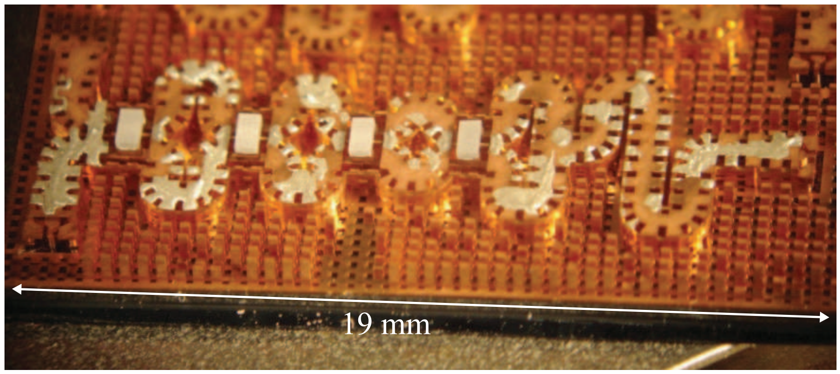


Figure 3.14: Circuit schematic of the broadband Wilkinson divider designed for the eleven-layer process. The values of characteristic impedances, resistors and length of each section are given in Table 3.2.

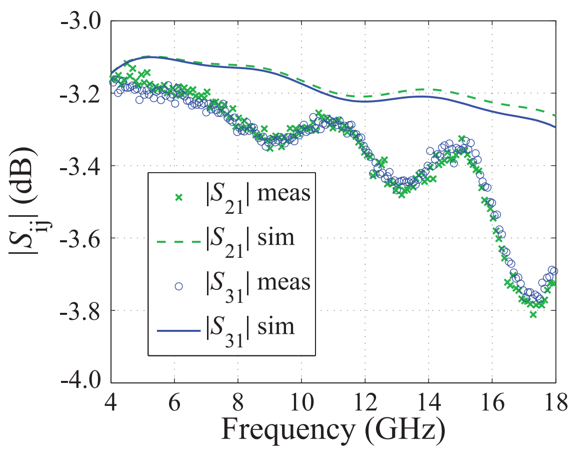
Table 3.2: Eleven-layer 50 Ω Wilkinson parameters

Section	0	1	2	3	4	5	6
Z [Ω]	50	46	41	70	66	61	55
l [mm]	1	6.3	6.3	5.4	4.0	5.1	5.8
R [Ω]	—	50	200	200	200	—	—

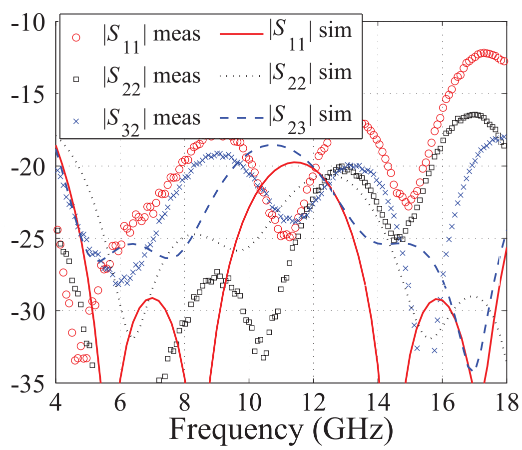
Although fewer transmission line sections are used in this design, the resulting bandwidth is still 2–22 GHz. This is due to the greater range of characteristic impedances available with the eleven-layer process compared to the five-layer line. This divider was modeled in HFSS and then fabricated in the PolyStrata process. Figure 3.15 (a) shows the fabricated picture and Figure 3.15 (b) and (c) show the simulated and measured results of this divider. Due to a process error that has subsequently been identified and corrected, the top layer, 11, was not completely in intimate contact with the rest of the device. This seam was filled using conductive epoxy. Despite this problem, the transmission coefficient $|S_{21}|$ in the eleven-layer divider is approximately 0.4 dB better than the five-layer dividers due to the larger cross-section of the transmission lines.



(a)



(b)



(c)

Figure 3.15: (a)Photograph of the 11-layer Wilkinson divider. Conductive epoxy was spread on the outer conductor to fill out the cracks on the outerconductor. (b) Simulated and measured $|S_{21}|$ and $|S_{31}|$ for the eleven-layer Wilkinson divider. (c) Return loss, isolation, and match at the output ports.

3.5 Chapter Summary

In summary, 11:1 bandwidth Wilkinson dividers implemented in micro-coaxial lines have been designed, fabricated, and characterized with measured performance agreeing closely to simulations. The measured isolation between the output ports is better than 11 dB for 2–22 GHz, and the return loss is better than 13 dB over that range. The measured insertion loss varies from less than 0.2 dB at 4 GHz to 0.7 dB at 18 GHz, due to the increase from the skin effect loss in the copper. Several coaxial geometries for different power handling capabilities were considered. The power loss through the resistors was determined for ±20 % mismatch in the magnitude of the load impedances with at most 3.2 mW power dissipation in a 200 Ω resistor for 1 W of input power. The PolyStrata process enables hybrid integration of standard surface mount components such as 0402 and 0303 standard package resistors in the Wilkinson dividers. This type of hybrid integration can be extended to active devices for a PolyStrata power combined amplifier. It is also possible to detach the coaxial copper structure from the silicon substrate and integrate it with circuits made in different technologies.

Chapter 4

Broadband Micro-Coaxial Impedance Transformers

A window is enough for me, a window to the instance of insight, sight, and peace.

—Forough Farokhzad

If you would be a real seeker of the truth, it is necessary that at least once in your life you doubt, as far as possible, all things.

—René Descartes

Contents

4.1 Introduction

As discussed in Chapter 1, it is necessary to design a broadband matching network in order to match the input and output impedances of a broadband amplifier. Conventional broadband matching networks such as linear, exponential, and Klopfenstein tapers are very long (greater than 6 cm) for frequencies above 2 GHz with return loss better than 14 dB. In this chapter miniaturized transmission line transformer matching networks from 2–24 GHz are discussed.

A transmission-line transformer (TLT) with frequency-independent characteristics was first introduced in 1944 by Guanella [46]. These devices transform current, voltage and impedance similarly to conventional wire-wound transformers, but are implemented with interconnected transmission lines [47]. Figure 4.1 (a) shows the transmission-line model of a 4:1 impedance transformer, where two equal-length equal-delay lines are connected in a way that imbalances currents in the outer conductors so that energy is transmitted via a transverse transmission-line mode [48, 49]. Because the shield of one line is connected to the inner conductor of the other equal length line, the currents add in phase at the low-impedance end. As a result of the equal delay, the transformation becomes theoretically independent of the line length, and therefore frequency independent. In 1959, Ruthroff introduced

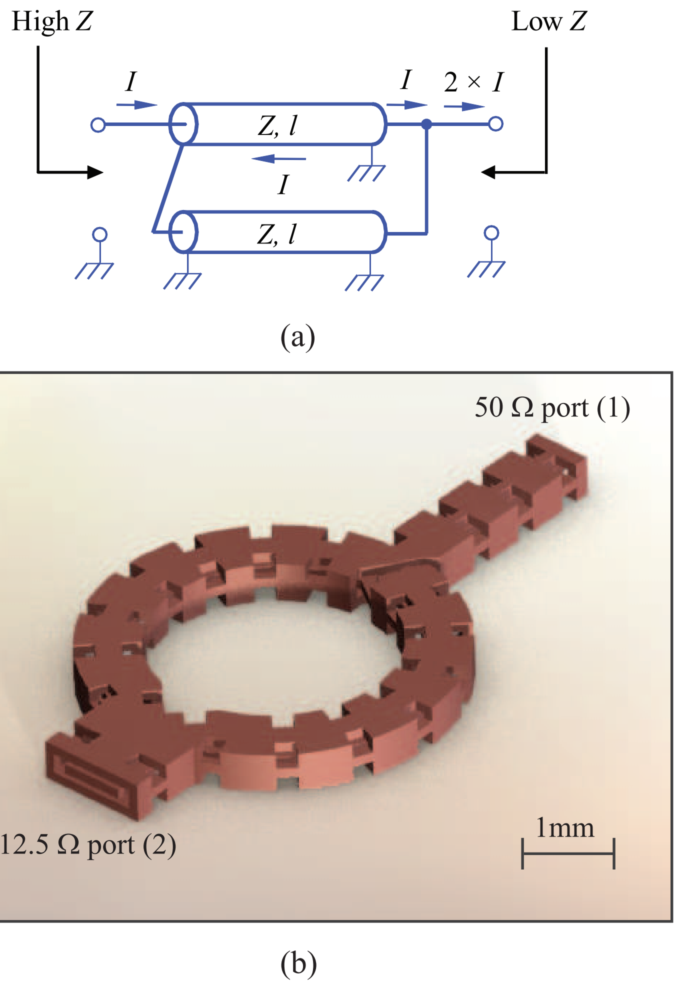


Figure 4.1: (a) Transmission line model of a 4:1 Guanella transformer. (b) Rendering of the 4:1 Guanella transformer implemented in the five-layer PolyStrata environment.

a new class of TLTs that uses only one transmission line and thus is considerably smaller than the Guanella transformer. However, it is not theoretically frequency independent [47].

Coaxial TLTs are widely used as impedance matching networks for broadband power amplifiers in the UHF and VHF ranges [48]. For frequencies under 100 MHz, transformers are constructed from pairs of wire wound around a ferrite core. At UHF and low microwave frequencies, coaxial lines are used in transformer implementation. They are commonly loaded with ferrites to increase the inductance, thereby increasing the electrical length of the transmission lines and extending the low-frequency cutoff. At microwave frequencies, planar configurations with multilayer PCBs and MMIC structures have also been demonstrated [48, 50, 51].

This chapter is organized in the following manner:

- Section 4.2 discusses the fabrication process and outlines the characteristics of 4:1 Guanella transformer and its bandwidth capabilities. In particular we explore the design procedure, and full-wave electromagnetic simulations of this transformer in the 2–24 GHz range.
- Section 4.3 presents the 4:1 impedance transformer performance in three different environments air, air-cavity, and silicon.
- Finally, Section 4.4 demonstrates a 2.25:1 impedance transformer, its design procedure, full-wave analysis and implementation. The prototype performance is compared with full-wave simulation results.

4.2 4:1 Impedance Transformer Design Procedure

The Guanella-type transformer as shown in Figure 4.1 (a) consists of two transmission lines with a series connection at the high-impedance end and parallel connections at the low-impedance end. For a 4:1, 50 Ω to 12.5 Ω transformer, the impedance of the transmission line sections is $\sqrt{Z_{low} \cdot Z_{high}} = 25\,\Omega$. Such a device is chosen to match the approximately 10 Ω input and output impedances of a broadband GaN traveling-wave amplifier discussed in Chapter 1.

An ideal transformer, as described in Section 4.1, has infinite bandwidth, regardless of the length of the transmission lines and the geometry of the interconnects. However, in practice, the design of a TLT for microwave frequencies between 2 and 24 GHz requires careful full-wave electromagnetic (EM) simulations; Ansoft's High-Frequency Structure Simulator (HFSS) is used in this study. Figure 4.1 (b) shows the 4:1 micro-coaxial transformer designed to be implemented in the five-layer PolyStrata process described in Chapter 2. The important design features are the lengths of the lines, and the geometrical detail of the interconnections between the transmission lines at the series and parallel junctions. The lengths of the transmission lines contribute to both the lower and upper frequency limits. The lower frequency limit is directly proportional to the reactance associated with the inductance of the middle section transmission lines. For a given transformer design that operates between f_1 and f_2, in order to extend the low-frequency limit to $(f_1 - \Delta f_1)$, the electrical lengths of the transmission lines should be increased. However, this will also result in a shift in the high-frequency limit to $(f_2 - \Delta f_2)$. For example, if $f_1 = 2\,\text{GHz}$ and $f_2 = 24\,\text{GHz}$, to change the lower frequency limit from f_1 to $f_1 - \Delta f_1 = 1\,\text{GHz}$, we would increase the length of the two transmission lines to $[f_1/(f_1 - \Delta f_1)]\, l$ in order to maintain the same electrical length at $f_1 - \Delta f_1$. However, this would shift f_2 down by some Δf_2, where $\Delta f_2 > \Delta f_1 = 1\,\text{GHz}$. In order to maintain the high-frequency limit at f_2, the junctions need to be re-optimized. For the design presented here, a length of $l \approx 5\,\text{mm}$ is chosen for the desired bandwidth of at least 2–24 GHz. The second important factor that sets the upper frequency limit is the parasitic reactance associated with each transmission-line junction.

Figure 4.2 (a) shows the series interconnection between the middle section transmission lines and the 50 Ω transmission line. This region is designed such that it produces the lowest possible inductance and capacitance parasitics with the given PolyStrata design rules for gaps between the conductors and widths of the conductors. Figure 4.2 (b) shows the parallel interconnection between the middle section transmissions lines and the 12.5 Ω transmission line. The chamfer at the junction of this interconnection is designed such that it creates a smoother transition from the two 25 Ω lines to the 12.5 Ω line; as a result the upper frequency limit increases.

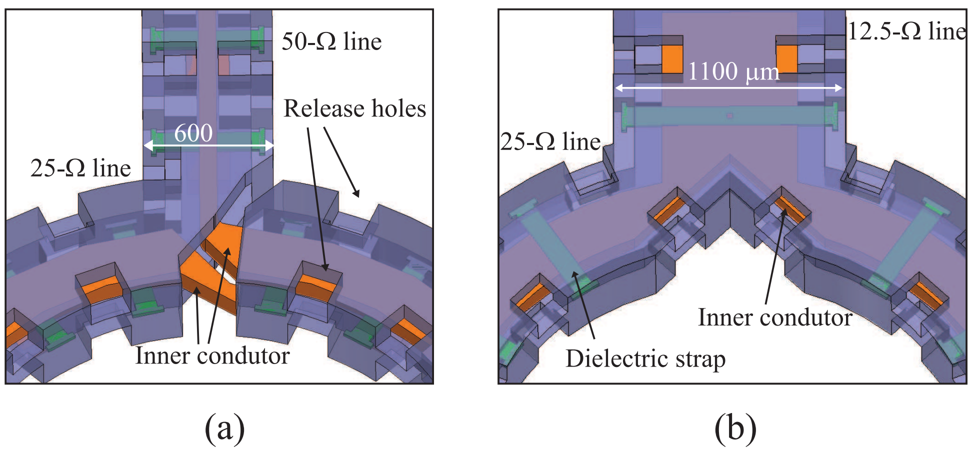


Figure 4.2: (a) Series interconnection between the 25 Ω line and 50 Ω line; (b) Parallel interconnection between the 25 Ω line and 12.5 Ω line

To illustrate the importance of full-wave analysis and interconnect optimization, Figure 4.3 shows simulation results when the transmission line interconnections are not optimized, for two obvious rectangular and circular geometries. The circular geometry improves the performance even without optimized junctions, since it contains fewer discontinuities, and reduces coupling. Figure 4.4 shows the simulation results of a transformer with the circular geometry after extensive simulations to minimize parasitics. $|S_{21}|$ for the optimized circular geometry transformer at

17 GHz is about 0.25 dB, where for the un-optimized circular and rectangular geometries it is 0.5 dB and 1.25 dB, respectively.

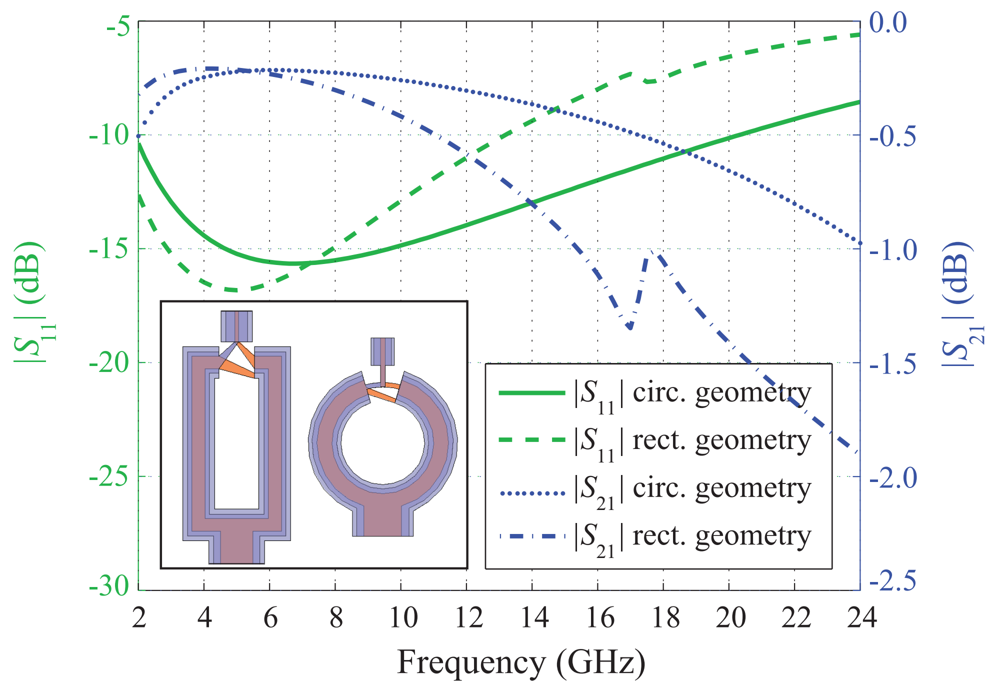


Figure 4.3: S-parameter simulation results for two un-optimized 4:1 impedance transformers with circular and rectangular geometries. These simulations do not include release holes or dielectric straps.

4.3 4:1 Impedance Transformer Characterization

Because the currents on the outer conductors of a TLT are not equal, and there is an opening in the outer conductor at the transmission-line connection, the environment around the TLT significantly affects its performance. The initial design discussed in the previous section is for the case of a transformer in air. However, in order to integrate the transformer with other components in a system, mechanical stability requires integration with a substrate or package. For this reason, we investigate an

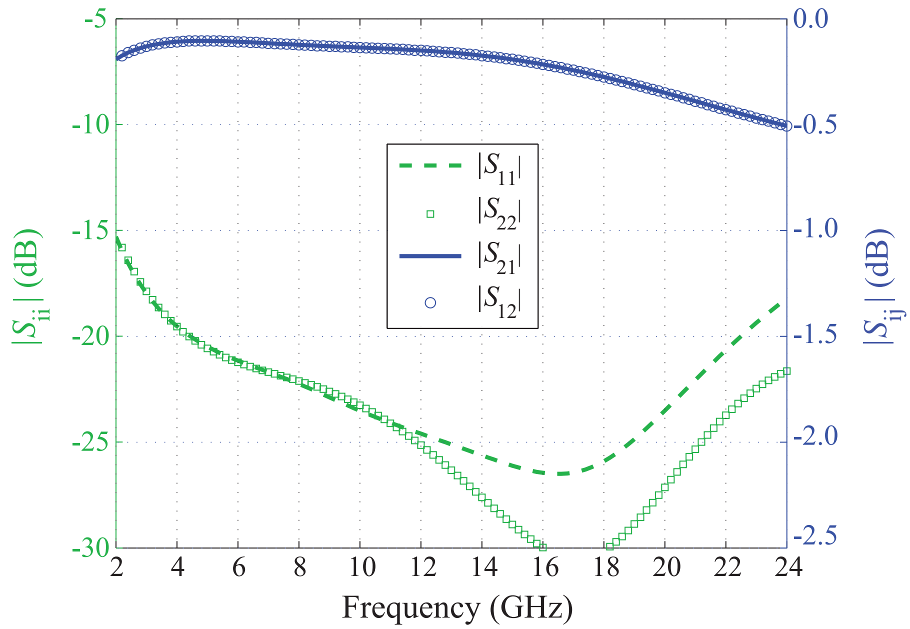


Figure 4.4: Simulation results of the 4:1 circular impedance transformer, where the intraconnections are fully optimized for the lowest possible parasitics. This simulation takes into account all the fabrication design rules including release holes or dielectric straps.

air-filled metal cavity designed to function as a support for the transformer, as well as the native substrate for PolyStrata fabrication, silicon.

In this section, characterization of fabricated transformers in air (on foam, $> 99\,\%$ air), air-filled metal cavity, and on a silicon substrate, is presented. In order to measure the transformer in a $50\,\Omega$ system, we considered two measurement methods: (1) a back-to-back structure; and (2) a geometrical taper to connect the $12.5\,\Omega$ side of the transformer to a $50\,\Omega$ port. The former is done for a TLT designed in air and measured on foam and for a TLT designed and measured on a brass fixture with an air-filled cavity beneath the intraconnections. The latter is discussed for the TLT designed and measured on a silicon substrate.

4.3.1 Micro-coaxial Transformer in Air

Back-to-back transformers fabricated on a high resistivity silicon substrate, connected to each other at their 12.5 Ω ports as shown in Figure 4.5, allow measurements to be made in a 50 Ω system. The circuit can be detached from the wafer and used as a free standing device. A 5 mm thick piece of foam ($\epsilon_r \approx 1.005$ at rf) is used as mechanical support. Measurements are performed with an Agilent E8364B PNA four-port network analyzer, Cascade Microtech 250-μm-pitch CPW microwave probes, and a Cascade Summit 9000 probe station. Calibration is performed with a set of on-wafer TRL calibration standards including two line lengths in order to cover the bandwidth [36].

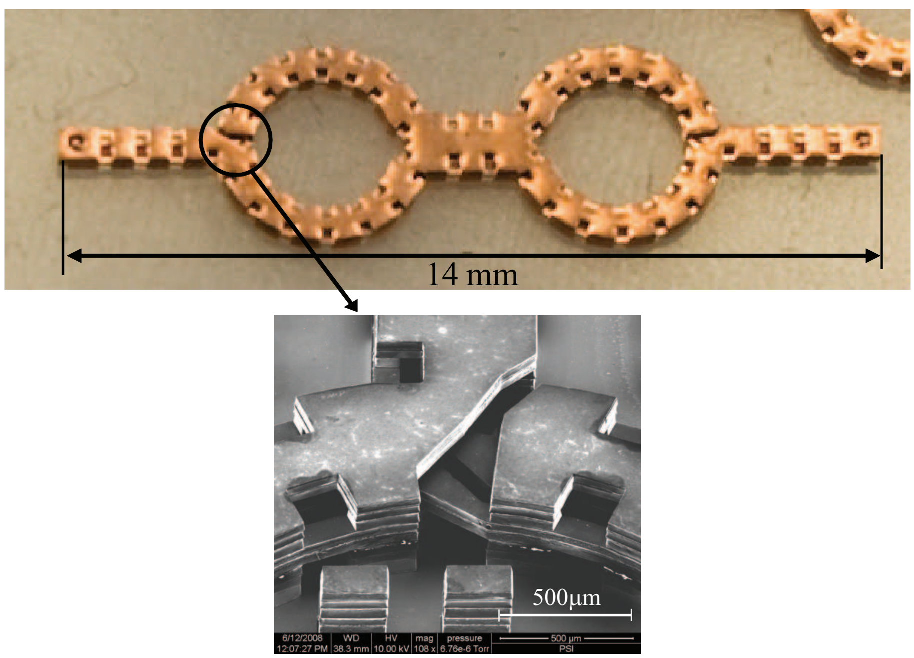


Figure 4.5: Photograph of the 4:1 impedance transformer, fabricated in the PolyStrata. The micrograph on the bottom shows the fabricated photo of the intra-transformer connections between the 50 Ω and 25 Ω lines.

Figure 4.6 shows the measured and simulated results of the back-to-back transformers measured on foam. The small dip at 7 GHz is due to calibration, since the transition frequency between the two line standards is 7 GHz. The dip at 15 GHz, however, is due to a slight difference in electrical length of the two lines of each transformer.

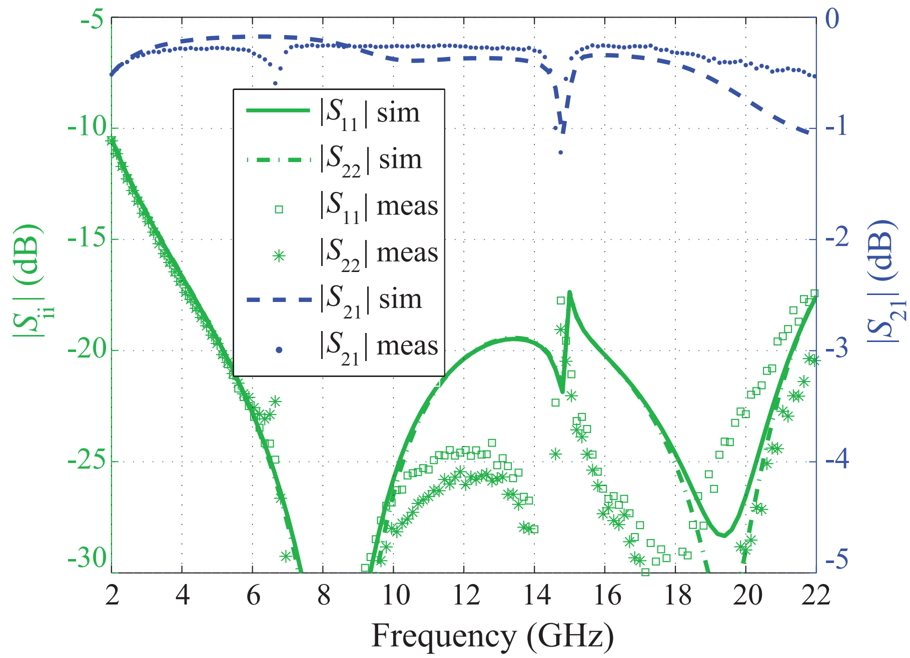


Figure 4.6: Simulated and measured results of the back-to-back 4:1 impedance transformer.

Figure 4.7 shows circuit simulations (Ansoft Designer) for a 100 μm length difference corresponding to the bend of the lefthand line in Figure 4.2 (a). These results point to the importance of careful design of the connection between the transmission lines, where in addition to parasitics, any effective length differences need to be compensated. Specifically, in the inset circuit of Fig. 4.7, the two 25 Ω transmission lines create a $\lambda/2$ resonator beginning at the 50 Ω line, shorted to the outer conductor of the upper 25 Ω line, causing a resonance at 14.8 GHz. In FEM simulations, this effect might not be obvious since it depends on meshing, so the mesh should be varied to check for this effect, or one might choose to validate against a different full-wave simulator.

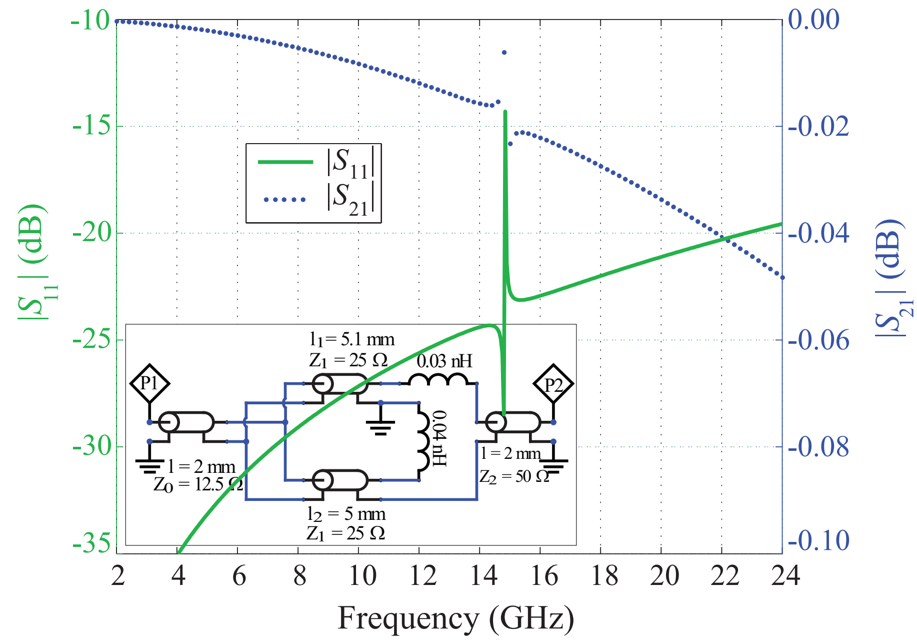


Figure 4.7: Circuit simulation results for a 4:1 transformer with 100 µm length difference between the two transmission lines. The micrograph on the bottom left shows the circuit model that includes the parasitics at the 50 Ω junction. The coaxial transmission lines in this circuit model are ideal, so there is no limitation on the low frequency limit. The difference in line length causes the resonances at 15 GHz.

4.3.2 Cavity-Backed Micro-coaxial Transformer

For a TLT in air, a brass frame is designed for support as shown in Figure 4.8. Since a micro-coaxial TLT operates based on current flow on the outer conductor as well as the inner conductor of the coaxial line, the surrounding frame could interfere with the operation of the transformer and degrade the performance. The perimeter and the depth of the structural support were simulated in HFSS to find the optimal dimensions, where the depth of each cavity is approximately 2.5 mm ($\lambda/60$ at 2 GHz), and the sides are 7 mm and 7.4 mm in length.

Figure 4.9 shows the simulated and measured results of the 4:1 back-to-back transformers placed on the brass structure, calibrated with a two-port short-open-load-through implemented in CPW on an alumina substrate, in the absence of

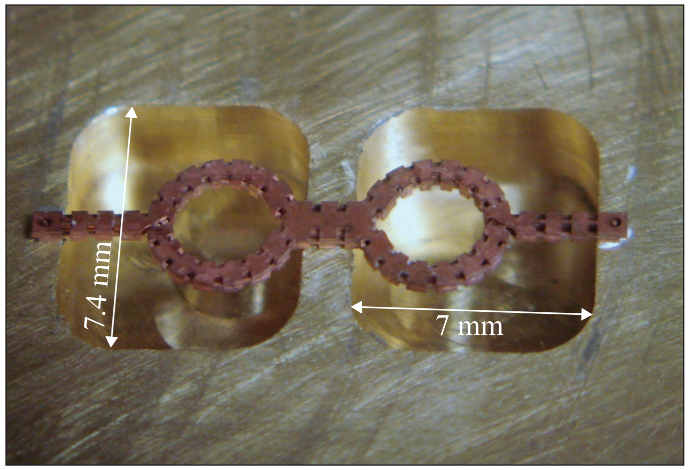


Figure 4.8: Photograph of the back-to-back 4:1 transformer epoxied on the brass fixture. The depth of the cavities is 2.5 mm.

an appropriate TRL calibration standard. This calibration method removes the effects of the cables and probes up to the probe tips. As shown in Figure 4.9 the performance of the device is very similar to the one measured on foam. The only difference is that the standing wave shown in $|S_{11}|$ is slightly shifted to the left, due to calibration difference.

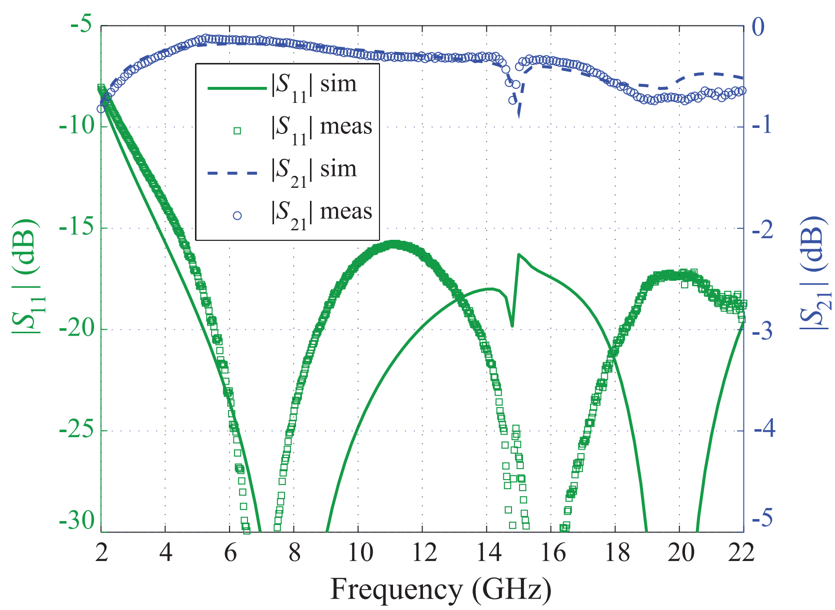


Figure 4.9: Simulation and measured results of the back-to-back 4:1 impedance transformers on the brass fixture of Figure 4.8.

4.3.3 Micro-coaxial Transformer on Silicon

As mentioned in Section 4.1, in order to enhance the lower frequency limit of TLTs, ferrite-loaded transmission lines or ferrite cores are commonly used. The ferrites increase the distributed inductance of the lines, and as a result, they are effectively longer and thus reduce the lowest operation frequency. In this case, the silicon substrate has a similar effect as ferrites; it reduces the lowest operation frequency at the cost of greater insertion loss. The dielectric increases the distributed capacitance between the two shield conductors in proportion to ϵ_r, and so their electrical length increases. The additional loss is due to coupling to substrate modes which are most likely excited at the transmission-line intra-connections at the $50\,\Omega$ junction.

In the previous section the simulation and measured results of a back-to-back transformer are presented and show good agreement. However, the back-to-back structure does not show the transformation of $50\,\Omega$ to $12.5\,\Omega$. In order to demonstrate the 4:1 transformation for a single transformer on silicon, a linear geometrical taper at the $12.5\,\Omega$ port was added to connect a $12.5\,\Omega$ line to a $50\,\Omega$ line. Figure 4.11 (a) shows the fabricated transformer with a geometrical taper on silicon, and (b) shows a sketch of the taper. The geometrical taper only allows us to measure the transformer with the same micro-coax to CPW transition and 250-μm-pitch probes, and since its length is very short, it does not actually transform $12.5\,\Omega$ to $50\,\Omega$. An estimate of the input impedance of the taper looking from the $50\,\Omega$ side at 12 GHz is given by

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} = 12.68 + j5.9\,\Omega, \tag{4.1}$$

where $Z_0 = 50\,\Omega$, $Z_L = 12.5\,\Omega$ and $l = 0.5\,\text{mm}$. Figure 4.11 (a) shows the simulation and measurement results of the 4:1 TLT measured with the 50 Ω system when the taper is not de-embedded. Since the geometrical taper does not have a significant effect on the output impedance, the taper can be deembeded by simply adding a 12.5 Ω port to the data in a circuit simulator. Figure 4.11 (b) shows the measured and simulated de-embedded results for this transformer.

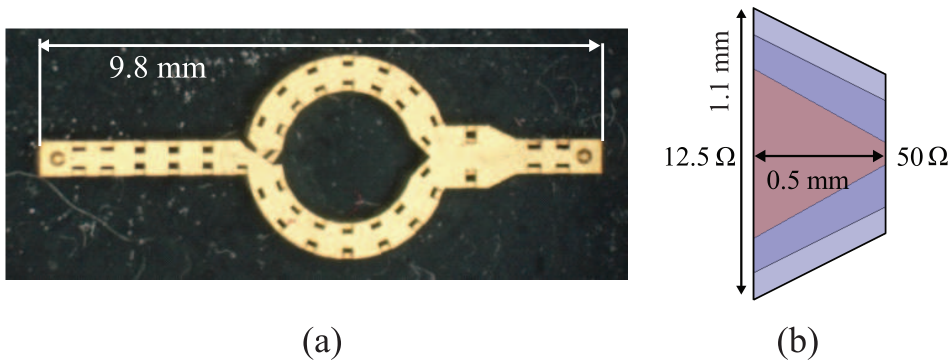


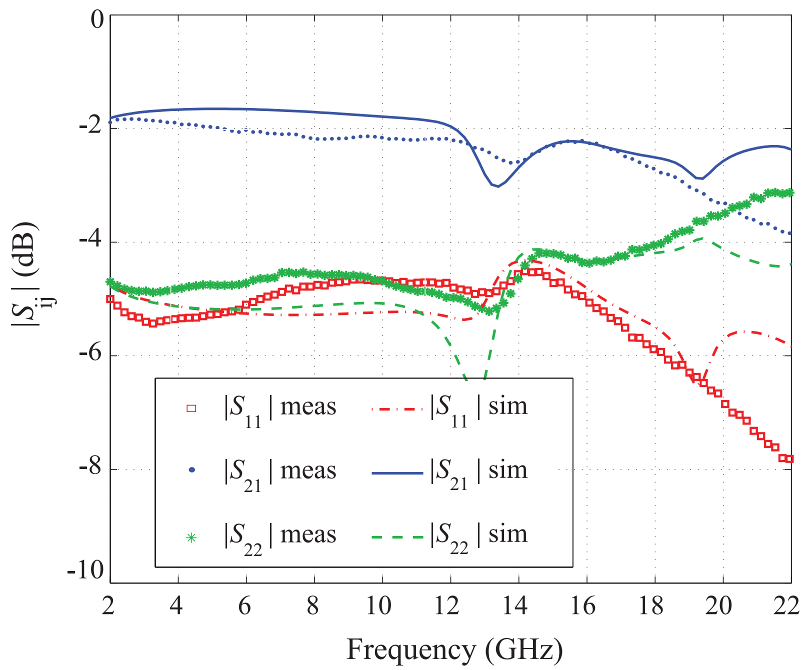
Figure 4.10: (a) Photograph of the single transformer on silicon with geometrical taper. (b) Detail of the geometrical taper connecting the 12.5 Ω line to 50 Ω line.

Micro-coaxial Transformer on Silicon and Ground

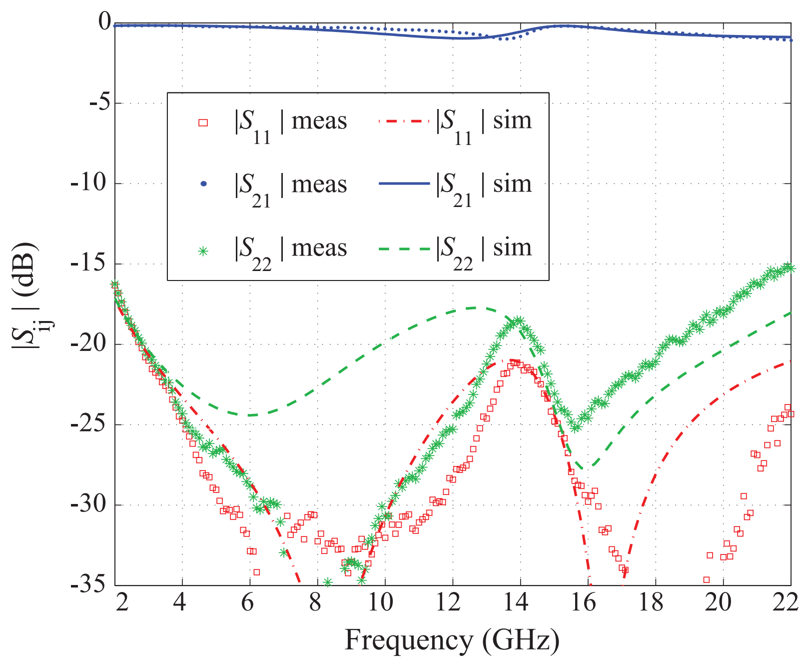
When the transformer is placed on Silicon above a ground plane, as shown in Figure 4.12 (a), sharp resonances appear in the s-parameter performance of the transformer.

Figure 4.12 (b) shows the measured results for the following cases

- Transformer on silicon on ground plane (probe station chuck)
- Transformer on silicon, on absorber 1 (ECCOSORB QR-13/SS-3), and on ground
- Transformer on silicon, on absorber 2 (ECCOSORB LS-26/SS-3), and on ground

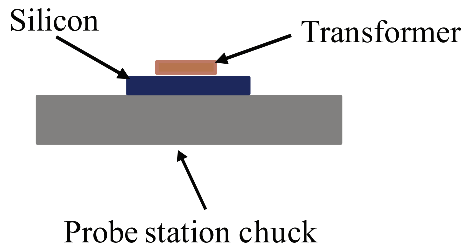


(a)

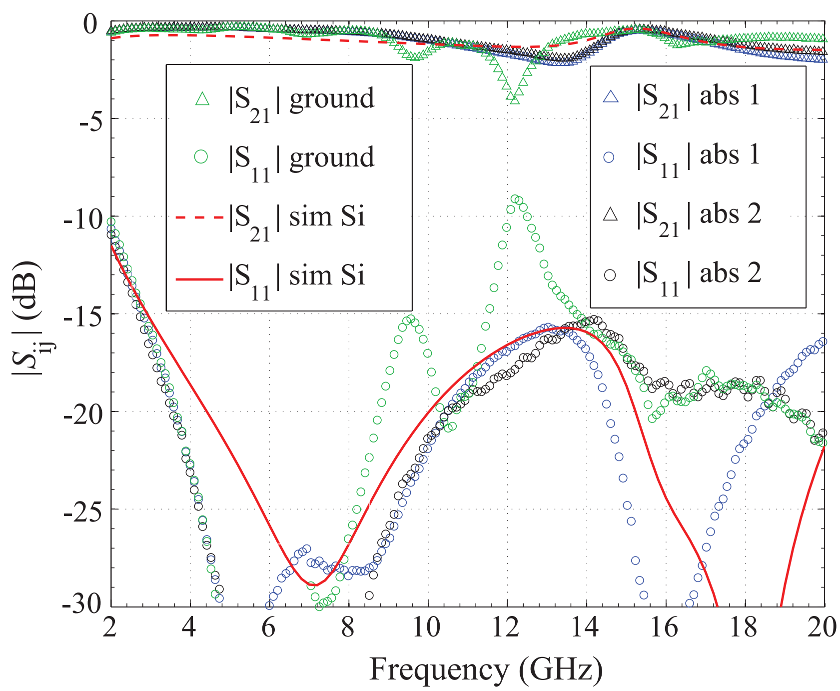


(b)

Figure 4.11: (a) Simulated and measured results of a 4:1 transformer with geometrical taper on silicon. The geometrical taper is included in both simulation and measurement. (b) Simulated and measured results of a 4:1 transformer on silicon. The geometrical taper is de-embedded from both simulation and measured results. The measurements are done in a $50\,\Omega$ system.



(a)



(b)

Figure 4.12: (a) Stack up showing transformer above silicon and ground plane. (b) Measured s-parameter results for the 4:1 transformer placed above silicon and ground plane (probe station chuck), above silicon and ground plane and two different absorbers. Simulation results are for the case with no ground plane.

- Transformer on silicon, on absorber 2 (ECCOSORB LS-26/SS-3), and on ground

The simulation results are performed for the case of the transformer on silicon. Depending on the type of the absorber between the ground plane and silicon the resonances effect due to ground plane can be eliminated. These resonances can also be eliminated by using a thicker silicon substrate like 2 mm substrate.

Due to this reason we believe the silicon and the ground plane together acts like a grounded dielectric slab.

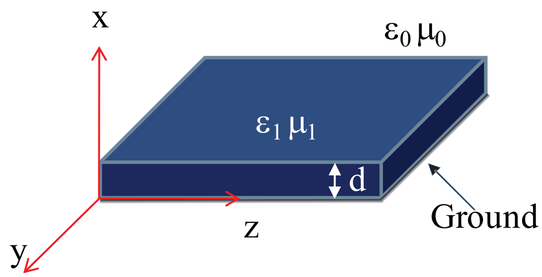


Figure 4.13: Infinite grounded dielectric slab.

Figure 4.13 shows a grounded dielectric slab. The TM modes in such a slab can be found in a standard way by solving the wave equation with appropriate boundary conditions, as in, e.g., [52, pages 149–169]:

$$\left(\frac{\partial^2}{\partial x^2} + \omega^2\mu\epsilon + \gamma^2\right) H_y = 0 \tag{4.2}$$

or

$$\left(\frac{\partial^2}{\partial x^2} + {h_1}^2\right) H_y = 0, \quad 0 < x < d \tag{4.3}$$

$$\left(\frac{\partial^2}{\partial x^2} - {p_0}^2\right) H_y = 0, \quad x > d \tag{4.4}$$

where

$${h_1}^2 = \omega^2\mu\varepsilon_1 - \beta^2 = {k_1}^2 - \beta^2 \tag{4.5}$$

and

$${p_0}^2 = \beta^2 - \omega^2\mu\varepsilon_0 = \beta^2 - {k_0}^2. \tag{4.6}$$

The solutions to Equations 4.3 and 4.4 are

$$H_y = B\sin(h_1 x) + C\cos(h_1 x), \quad 0 < x < d \tag{4.7}$$

$$H_y = Ae^{-p_0 x}, \quad x > d \tag{4.8}$$

By applying the following boundary conditions to the solutions,

$$E_z = 0, \quad x = 0 \tag{4.9}$$

$$H_y|_{x=d^-} = H_y|_{x=d^+} \tag{4.10}$$

$$\frac{1}{\varepsilon_1}\frac{dH_y}{dx}|_{x=d^-} = \frac{1}{\varepsilon_0}\frac{dH_y}{dx}|_{x=d^+} \tag{4.11}$$

we can find the eigenvalue equation for TM modes:

$$\tan(h_1 d) = \frac{p_0\varepsilon_1}{h_1\varepsilon_0}. \tag{4.12}$$

.

A grounded dielectric slab has only even TM modes and odd TE modes [52], which can be solved with the same method shown above.

Defining a normalized frequency V as

$$V = \sqrt{{k_1}^2 - {k_0}^2}d = \sqrt{(p_0 d)^2 + (h_1 d)^2}, \tag{4.13}$$

following can be obtained from 4.12 and 4.13

$$p_0 d = \sqrt{V^2 - (h_1 d)^2} \tag{4.14}$$

$$p_0 d = \frac{\varepsilon_0}{\varepsilon_1} h_1 d \tan(h_1 d). \tag{4.15}$$

Figure 4.14 shows the geometrical solution of TM modes for lossless grounded dielectric slabs. As shown, the fundamental mode TM_0 has zero cutoff frequency. However, there are some regions in which there is no solution. By placing the transformer on top of grounded silicon, it is possible to excite the TM_0 mode through the $50\,\Omega$ junction of the transformer. For a different thickness of the silicon substrate, there might be no solution to the eigenvalue equation. This phenomena was proven through HFSS simulations. A lossy grounded dielectric slab has similar but more complicated solutions for eigenvalues (the solutions are out of the scope of this thesis).

4.4 2.25:1 Impedance Transformer

The only realizable transformation ratios of equal delay transmission line transformers are ratios that have a rational square root quantity, a proof of which can be found in [53]. An exact 2:1 impedance transformation is therefore not possible. However, an impedance transformation of 2.25:1, can be achieved by connecting only three equal delay transmission lines as shown in Figure 4.15 (a).

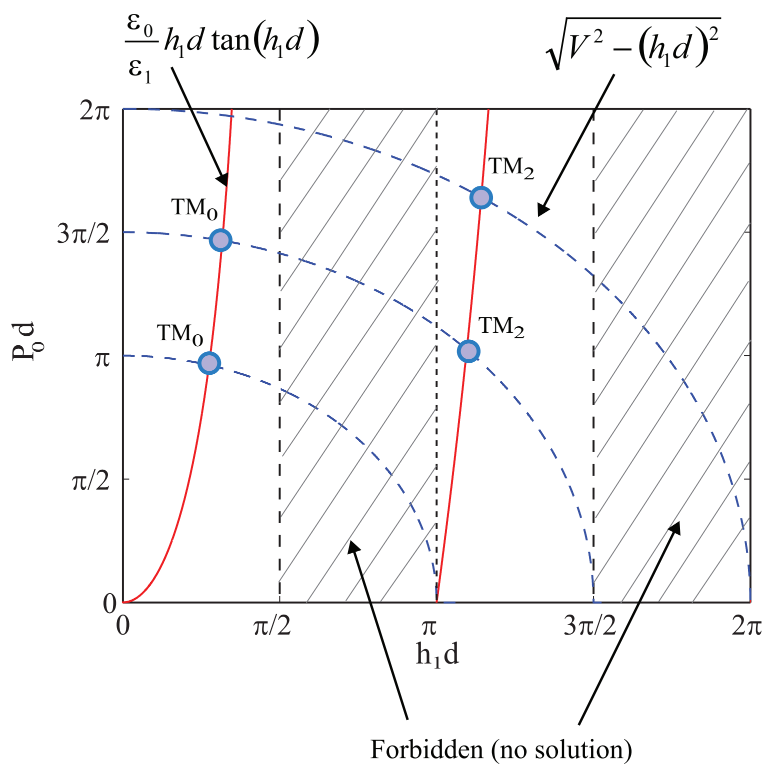
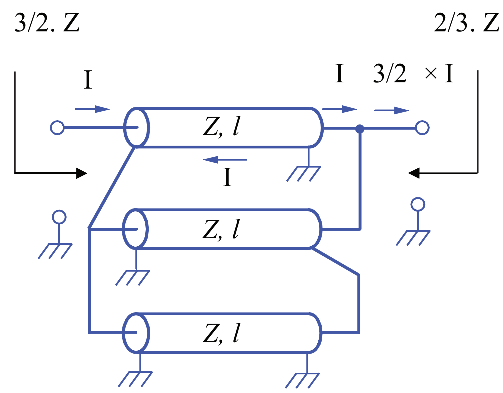


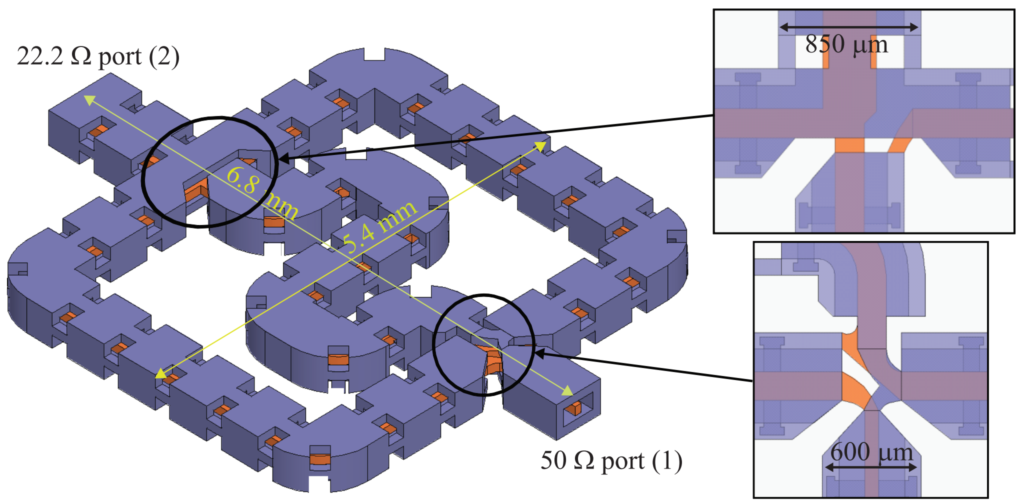
Figure 4.14: Graphical representation of TM mode eigenvalue solutions of an infinite grounded dielectric slab.

4.4.1 Design and Implementation

HFSS is used to implement the transmission line model of the 2.25:1 impedance transformers in the PolyStrata environment. Since there are additional transmission lines and intra-transformer connections, this design is more challenging than the 4:1 impedance transformer. Figure 4.15 (b) shows the HFSS model of this transformer. In this design, the lengths of the transmission lines are kept constant, and the intra-transformer connections, as shown on the right side of the figure, are optimized for the lowest possible parasitics given the PolyStrata design rules. Figure 4.16 shows the simulated s-parameter comparison between the 2.25:1 impedance transformer shown in Figure 4.15 (b), and an un-optimized device with parallel straight transmission lines. The resonances that appear in



(a)



(b)

Figure 4.15: (a) Transmission line model of a 2.25:1 impedance transformer. (b) HFSS model of the 2.25:1 impedance transformer; this transformer transforms 50 Ω to 22.22 Ω. The zoomed areas shows the interconnection at the 50 Ω (bottom) junction and 22.2 Ω (top) junction.

the un-optimized transformer are mainly due to the close proximity of the three transmission lines, and differences in their lengths. In order to prevent these effects and to isolate the transmission lines from each other as much as possible, the lines are meandered as shown in Figure 4.15 (b).

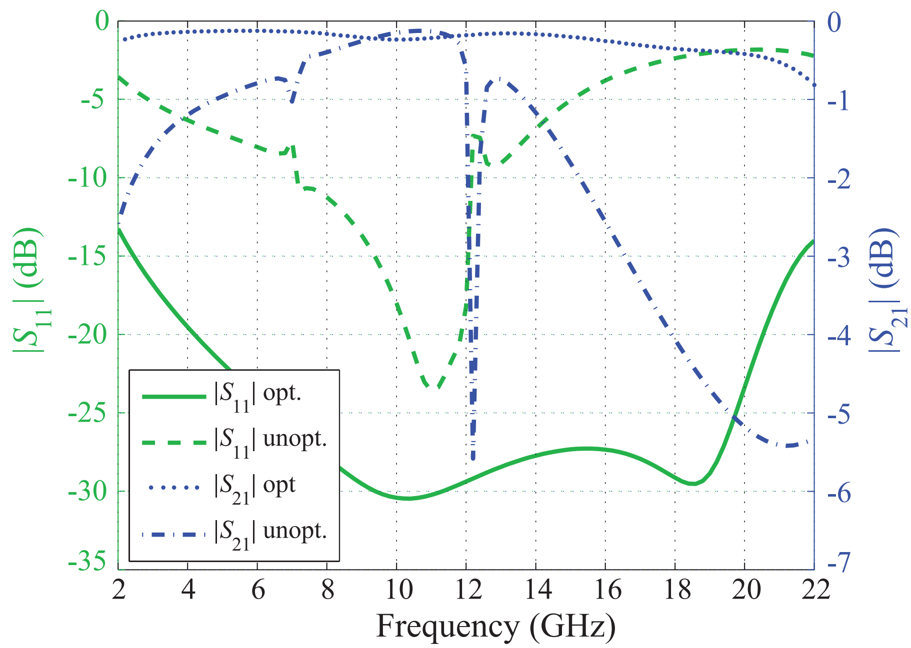


Figure 4.16: Simulated s-parameter results comparison for a 2.25:1 impedance transformer with optimized interconnections and isolated transmission lines to a 2.25:1 impedance transformer with un-optimized interconnection and side-by-side transmission lines.

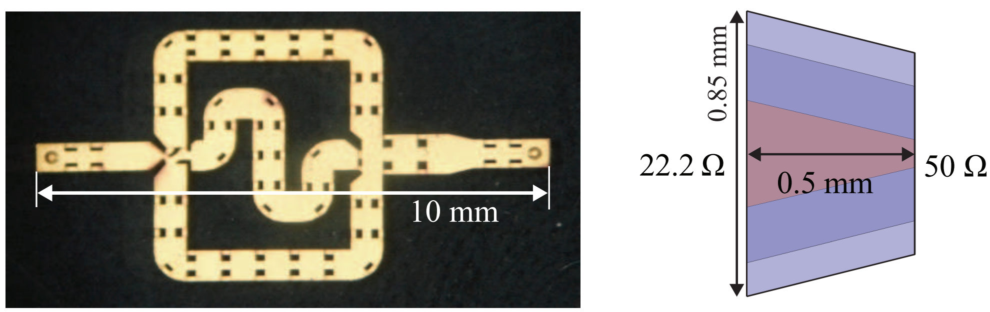
4.4.2 Prototype Performance

For measurement, the fabricated transformer was removed from the silicon and placed on foam. Figure 4.17 (a) shows the fabricated transformer with the geometrical taper, and (b) shows the sketch of the geometrical taper connecting $22.22\,\Omega$ to $50\,\Omega$ port. The taper like the one discussed in Section 4.2 does not change the $22.2\,\Omega$ port impedance significantly due to its short length:

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} = 22.5 + j5.05\,\Omega, \tag{4.16}$$

where $Z_0 = 50\,\Omega$, $Z_L = 22.2\,\Omega$ and $l = 0.5\,\text{mm}$. The measurement was performed with the same setup and calibration standards as discussed in Section 4.3. Figure 4.18 shows the measured and simulated s-parameter results. Agilent's Advanced Design System (ADS) software was used to deembed the geometrical taper from the measured results. For the simulation, the geometrical taper was included and then de-embedded with the same method that was applied to the measured results for fair comparison.

The slight shift in the upper frequency limit is due to a small fabrication defect on this particular wafer that has been subsequently fixed; the layer height of the micro-coaxial line varied more than 10 % resulting in characteristic impedance variations greater than expected.



(a) (b)

Figure 4.17: (a) Photograph of the 2.25:1 transformer on si with geometrical taper. (b) Sketch of the geometrical taper connecting the 22.2 Ω line to 50 Ω line.

4.5 Discussion and Summary

The main application of the impedance transformers is broadband matching, so it is important to compare their performance to commonly used broadband matching networks such as linear and Klopfenstein tapers. For 15 dB return loss at frequencies above 2 GHz, a Klopfenstein and linear taper that match 50 Ω to 12.5 Ω implemented in the micro-coaxial environment are 6 cm and 10 cm long,

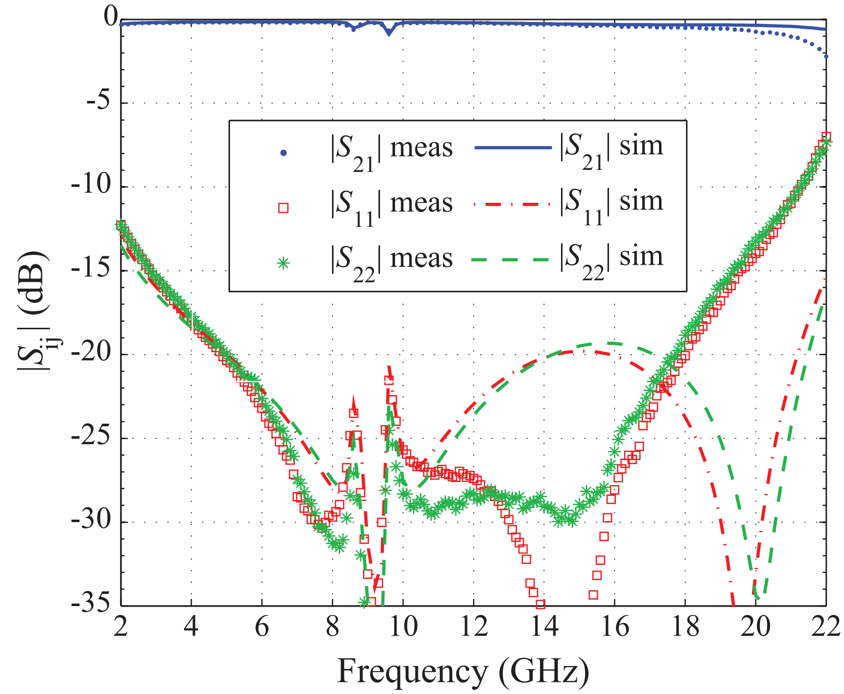


Figure 4.18: Simulated and measured results of a 2.25:1 transformer on foam. The measurement is performed in a 50 Ω system, and the geometrical taper is de-embedded from both simulation and measured results.

respectively. These tapers are more than an order of magnitude longer than the 4:1 impedance transformer presented in this chapter, and would therefore be more lossy. Figure 4.19 compares the group delay of a Klopfenstein taper and 4:1 transformer designed in micro-coaxial environment and simulated in HFSS. The group delay for both the transformer and the Klopfenstein taper varies about 10 ps between 2–5 GHz, however the transformer group delay is approximately constant above 5 GHz, making it more suitable for pulsed applications.

To summarize, in this chapter two types of impedance transformers (4:1 and 2.25:1) implemented in wafer-scale fabricated micro-coaxial lines were explored. The 4:1 impedance transformer has 12:1 bandwidth with an upper frequency limit as high as 24 GHz. The effects of different environments around the 4:1 transformer, such as air, cavity, and silicon, were investigated. The cavity backing the transformer

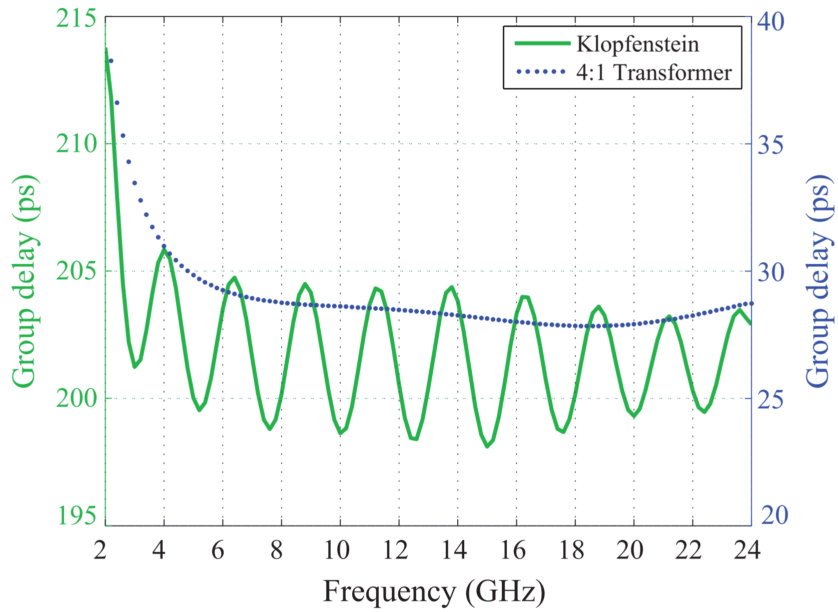


Figure 4.19: Group delay for both a 6 cm Klopfenstein taper implemented in the micro-coaxial environment with 15 dB return loss, and the 4:1 transformer.

increases mechanical stability but does not affect the performance, while when placed on silicon, the transformer bandwidth increases at the cost of greater loss. The design method was extended to a 2.25:1 meander-shaped transformer with a 11:1 bandwidth. The measured insertion loss for both transformers in air is less than 1 dB across the bandwidth [54]. These transformers are attractive for use as matching networks for broadband amplifiers. PolyStrata technology allows for design of other impedance transformation ratios, such as 8:1, with similar bandwidth capabilities. The Guanella impedance transformer design can be implemented as both a balun and simultaneously as a matching network for push-pull designs.

Chapter 5

Frequency-Scanning Antenna Arrays

Seek the wisdom that will untie your knot

Seek the path that demands your whole being

Leave that which is not, but appears to be

Seek that which is, but is not apparent

—Mawlana Jalal ad-Din Muhammad Balkhi (Rumi)

Contents

5.1 Introduction

This chapter presents an extension of the PolyStrata-based designs to millimeter-wave antenna arrays with frequency scanning. An example application is NASA radar for planetary landing systems, which imposes constraints on both size and weight, implying operation at frequencies above existing Ka-band systems. For two-dimensional antenna arrays, a two-fold increase in frequency results in a reduction of area by a factor of four. Since the cost per kilogram of satellite hardware is very high, it is cost efficient to put the effort on designing and fabricating components that operate in W-band ($f_0 = 95\,\mathrm{GHz}$) or G-band ($f_0 = 180\,\mathrm{GHz}$). Another motivation is the fact that the spatial resolution of a radar increases as wavelength decreases. Additionally, millimeter waves propagate through dust clouds and propellant plumes that arise during spacecraft landing.

Previous chapters presented rf front-end broadband components that operate below 25 GHz, but due to the nature of the fabrication process all of those components can be scaled to millimeter-wave frequencies. As mentioned in Chapter 1, one of the main components of an rf front-end system is the antenna or antenna array. This chapter presents an overview of scanned arrays and requirements on feed networks and antenna elements, followed by specific designs in PolyStrata technology for 1D 10–20 element slotted waveguide arrays at both W-band and G-band. Since the PolyStrata micro-coax can also be used for frequency scanned arrays this chapter first presents a discussion of losses in both micro-coax and waveguide.

5.1.1 Loss comparison between waveguide and micro-coaxial lines at W-band and G-band

The dominant loss mechanism in PolyStrata micro-coaxial lines is the loss in the metal due to the skin effect since the dielectric straps occupy less than 1% of the total volume. The attenuation coefficient for a waveguide with a rectangular cross section shown in Figure 5.1 and used in W-band and G-band slot array designs, is given in [55] as

$$\alpha_c = \frac{\Delta Z_0}{\sigma \mu v {\delta_s}^2 Z_0}, \tag{5.1}$$

where σ and μ are the conductivity and the permeability of the metal, and ΔZ_0 is the change in the impedance when the conductor walls are receded by half the skin depth in the conductor ($\delta_s/2$), following the Wheeler incremental inductance rule. This results in $\alpha_c = 0.21\,\text{dB/cm}$ at $100\,\text{GHz}$, and $\alpha_c = 0.26\,\text{dB/cm}$ at $150\,\text{GHz}$. Since fabrication introduces both lateral and transverse surface roughness components, a modified formula for the loss is given in references [13, 55] as

$${\alpha_c}' = \alpha_c \left[1 + \frac{2}{\pi} \arctan \left(1.4 \left(\frac{\Delta}{\delta_s} \right)^2 \right) \right], \tag{5.2}$$

where Δ is the rms surface roughness of the conductor. This formula is derived from the Wheeler incremental inductance rule as described in [42, page 86] and

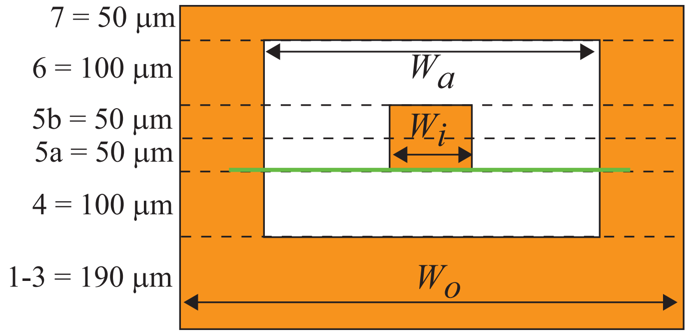


Figure 5.1: Cross-section of the micro-coaxial line used to feed the slot array. At 100 GHz, $W_i = 180\,\mu\text{m}$ and $W_a = 3.08\,\text{mm}$. At 150 GHz, $W_i = 180\,\mu\text{m}$ and $W_a = 1.9\,\text{mm}$.

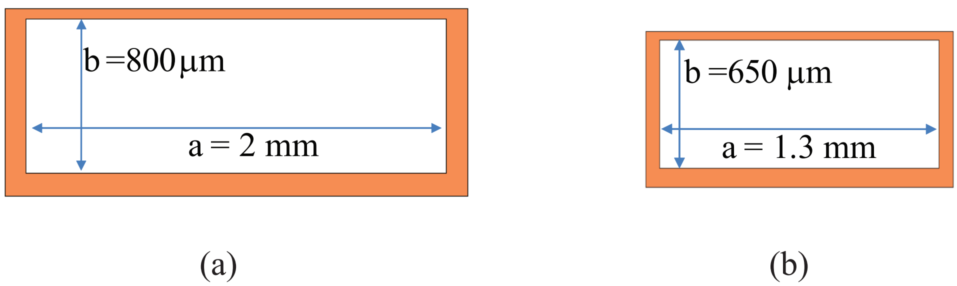


Figure 5.2: (a) W-band and (b) G-band rectangular waveguide cross-sections.

does not specify the type of roughness, so it is only used as a guideline here in the absence of other a formal treatment.

For the PolyStrata process, a reasonable value for the rms surface roughness is $0.13\,\mu\text{m}$, resulting in an increased attenuation of $1.316\alpha_c$ at W-band, and $1.437\alpha_c$ at G-band.

Figure 5.2 shows cross-sections of W-band and G-band dominant-mode rectangular waveguides that can be fabricated using the same process as for the micro-coaxial line shown in Figure 5.1.

The loss for the fundamental mode is given by, e.g., Marcuvitz [56, page 61] as

$$\alpha_c^{TE_{10}} = \frac{R_s}{b\eta\sqrt{1-\left(\frac{f_c}{f}\right)^2}}\left[1+\frac{2b}{a}\left(\frac{f_c}{f}\right)^2\right] \tag{5.3}$$

where R_s is the surface resistance, $\eta = 377\,\Omega$, and f_c is the cutoff frequency. Therefore at 100 GHz and at 150 GHz, the attenuation is 0.052 dB/cm and 0.091 dB/cm, respectively.

Table 5.1: Micro-coaxial line and waveguide loss at W- and G-band

Transmission media			Micro-coaxial line		Waveguide	
Frequency [GHz]			150	100	150	100
Attenuation [dB/cm]	$\Delta = 0$		0.253	0.207	0.0902	0.052
	$\Delta = 0.13\,\mu\text{m}$	Vertical walls	0.285	0.226	0.110	0.060
		All walls	0.404	0.305	0.1443	0.077
Roughness loss [%]	$\Delta = 0.13\mu\text{m}$	Vertical walls	0.36	0.22	0.23	0.1
		All walls	1.71	1.12	1.21	0.29

A summary of predicted loss in the micro-coaxial line from Figure 5.1 and the waveguide from Figure 5.2 is shown in Table 5.1. These losses are simulated with HFSS when the rms surface roughness was applied to (1) vertical walls and (2) all of the walls of the micro-coaxial line and the waveguide. These simulation results show that waveguides have significantly lower loss compared to micro-coaxial lines at G-band and W-band. However, the rms surface roughness has a larger effect on the loss of waveguides compared to micro-coaxial lines.

5.2 Frequency-Scanned Antenna Arrays

In a frequency scanning antenna array, the beam scans as the operating frequency of the array varies. The scanning is due to the variable phase shift in the feed lines of the individual elements, as shown conceptually in Figure 5.3. When the feed is dispersive, the phase velocity and thus the relative phase between elements changes with frequency and as a result the beam steers. The wave travels down the feed line and loses power at each element to radiation; this power loss is accounted for when the element excitations are determined. Thus, elements near the feed must couple weakly to the feed line, while elements near the load must couple strongly.

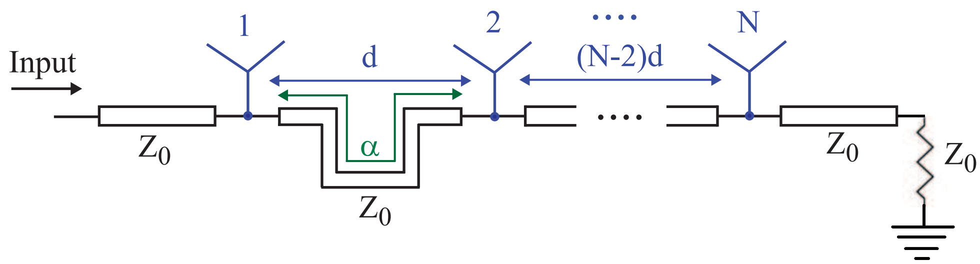


Figure 5.3: A conceptual sketch of an N-element frequency scanned antenna array fed by a dispersive line.

The phase of each element is determined by the length of the feed line section between the elements, as well as the mutual coupling [57, page 133]. When the inter-element path length in a dispersive feed line increases, a small frequency change will result in a larger phase change between elements and so greater scanning can be achieved compared to a line with low dispersion. In Figure 5.3 the antenna array is fed by a line of physical length α between elements and propagation constant β, with element spacing of d in air. For a scan angle θ_m the following can be written:

$$\beta_0 d \sin\theta_m = \beta\alpha - 2m\pi, \tag{5.4}$$

where m is an integer.

The phase equation can be written as

$$\sin\theta_m = \frac{\alpha\lambda_0}{d\lambda_g} - \frac{m\lambda_0}{d}, \tag{5.5}$$

where λ_0 is the free-space wavelength and λ_g is the guided wavelength in the feed. It is clear from these equations that a larger length of the feed line section (α/λ_g) gives a greater beam scan with frequency [58, pages 181–182].

Examples of frequency scanning antennas are traveling wave patch arrays (series fed arrays of patches) [59] and slotted waveguide arrays, which will be discussed in more detail in the next parts of this chapter.

Based on existing system specifications [60, 61] for the planetary landing radar, the array examined in this study should have a beam steering range of $\pm 16°$. The FWHM beamwidth should be around 0.5°. At 160 GHz, the beamwidth specification requires an approximately 20 cm × 20 cm aperture. Two approaches were investigated to meet these requirements: slotted waveguides and slotted micro-coaxial lines. This chapter focuses primarily on the lower loss waveguide approach, and compares these results to the performance of one possible micro-coaxial approach.

5.3 Slotted Waveguide Frequency Scanned Antenna Array Analysis

A slotted waveguide array antenna consists of a number of slots cut into the broad or narrow walls of a rectangular waveguide. Such arrays can have high radiation efficiencies and are mechanically robust and reliable. There are two types of slotted waveguide arrays: resonant and traveling wave. The former is achieved by terminating the waveguide with a short, and the latter by terminating the waveguide with a matched load. A resonant array is narrowband, since a standing wave is setup in the waveguide feed. However, in traveling wave arrays, the reflections from the slots tend to cancel each other out and so the array remains matched over a much broader frequency range [62]. Since waveguides are dispersive and the group velocity or delay between slots varies with frequency, the beam radiated by a slot array scans along the longitudinal axis of the waveguide as the input frequency is varied [63, pages 9-1–9-34].

Elliot [64, 65, 66] discussed the theory of slotted waveguide arrays, including when mutual coupling between the slots is taken into account. Based on a set of iterative methods, the total admittance and voltage across each slot is calculated as a function of the slot length and offset from the center of the waveguide. Several X-band arrays have been designed, built, and measured using this method [67]. MoM and FEM have been also used for designing such arrays [68]. An iterative analysis was presented combining Elliot's method with three-port generalized scattering parameters to take into account the input transitions from the feed network, with the slotted waveguide being excited either at one end or at the center [69].

Figure 5.4 shows a 3D model of a W-band slotted waveguide array. The equivalent circuit model of such array is shown in Figure 5.5.

The slots can be modeled as shunt complex admittances. The normalized conductance (real part of admittance) of a longitudinal slot cut in a waveguide operating in TE_{10} mode at resonance is [70]:

$$g = \frac{2.09a\lambda_g}{b\lambda_0} \cos^2\left(\frac{\lambda_0 \pi}{2\lambda_g}\right) \sin^2\left(\frac{x\pi}{a}\right), \tag{5.6}$$

where λ_0 is the free space wavelength, λ_g is the guided wavelength, x is the displacement from the waveguide centerline, and a and b are the width and height

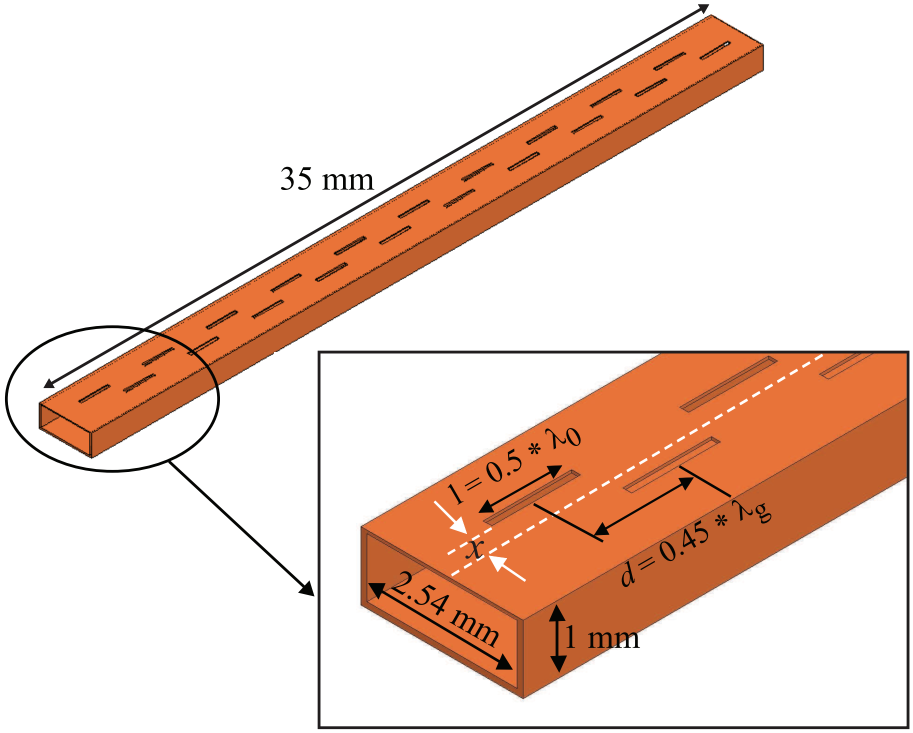


Figure 5.4: W-band broadside slotted waveguide array with 20 slots.

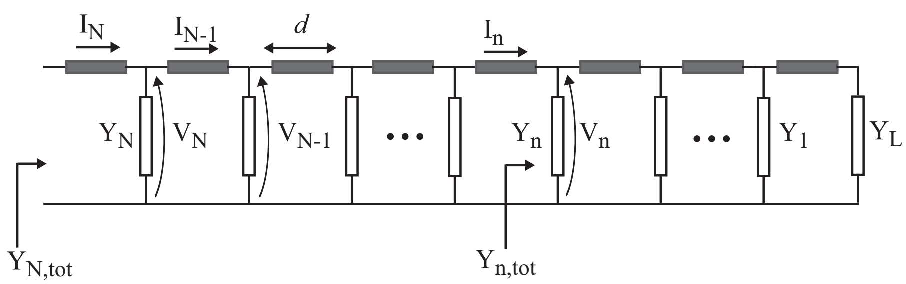


Figure 5.5: Equivalent circuit model of a slotted waveguide antenna array. The slots are modeled as normalized shunt admittances along the terminated feedline. Y_L in the case of traveling wave antenna is equal to 1.

of the waveguide, respectively.

The admittance of a slot excited by the TE_{10} mode of a rectangular waveguide is commonly measured or calculated from [68]

$$\frac{Y}{Y_0} = \frac{-2\Gamma}{1+\Gamma}, \tag{5.7}$$

where Y_0 is the characteristic admittance of the TE_{10} mode in the waveguide, Y is the admittance of the slot, and Γ is the reflection coefficient. The normalized admittance (Y/Y_0) is usually referred to as self-admittance (Y_{self}), which is a function of frequency, slot length, and offset from the waveguide centerline.

Now consider a waveguide with N slots terminated by a matched load, Y_L, as shown in Figure 5.5. The total normalized input admittance and voltage based on transmission line theory is calculated by

$$Y_n^{tot} = Y_n + \frac{Y_{n-1}^{tot}\cos\phi + j\sin\phi}{\cos\phi + jY_{n-1}^{tot}\sin\phi}, \tag{5.8}$$

where

$$V_n = V_{n-1}\left(\cos\phi + jY_{n-1}^{tot}\sin\phi\right), \tag{5.9}$$

$$\phi = \beta_{10}d, \tag{5.10}$$

and

$$Y_1^{tot} = Y_1 + Y_L. \tag{5.11}$$

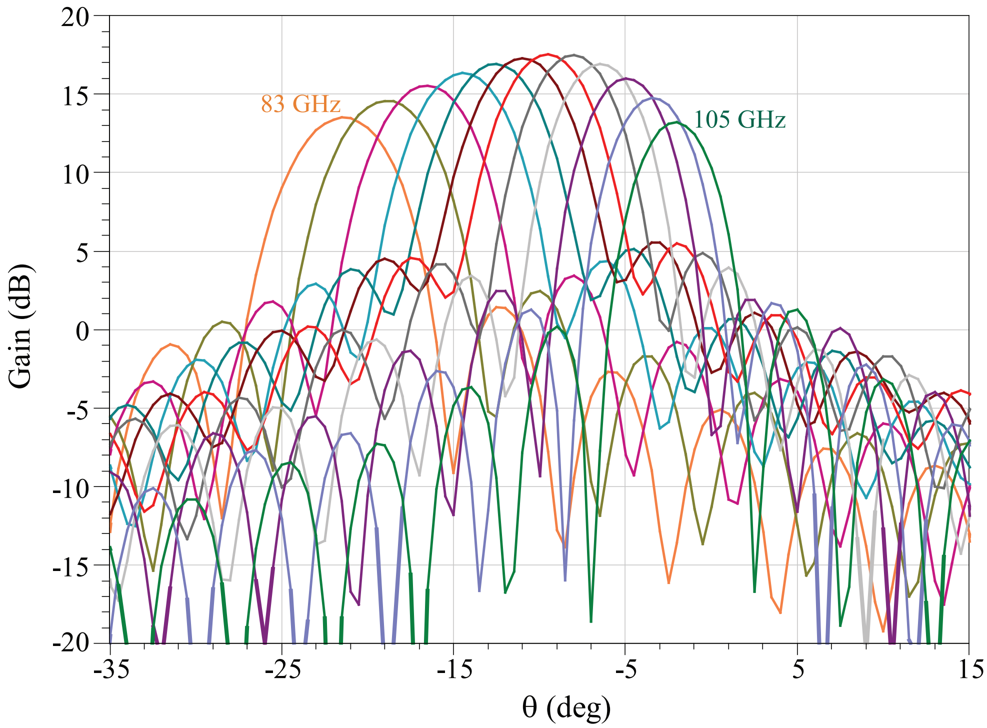
Elliot, in ref. [66], calculated the admittance Y_n and the mode voltages V_n. By assuming a slot length and array of N narrow slots, the coupling from the mode voltages V_n to the slot voltages V_n^s can be found. Because the slots are coupled mutually, the problem reduces to a matrix equation with a coupling described by an $N \times M$ matrix of coupling coefficients g_{mn}. This allows an iterative algorithm for solving the slot voltages (V_n^s) from which the radiation pattern can be obtained.

For the design of the W-band and G-band antenna arrays that are discussed in the following sections of this chapter, instead of this analytical method, a full-wave simulator (HFSS) is used. However, one can compare the results of these analytical methods with the HFSS results [69]. Also, in a 2D array when the slotted waveguides are placed side by side a similar analytical method could be used to take into account the couplings, since the design will be too large for full-wave simulations.

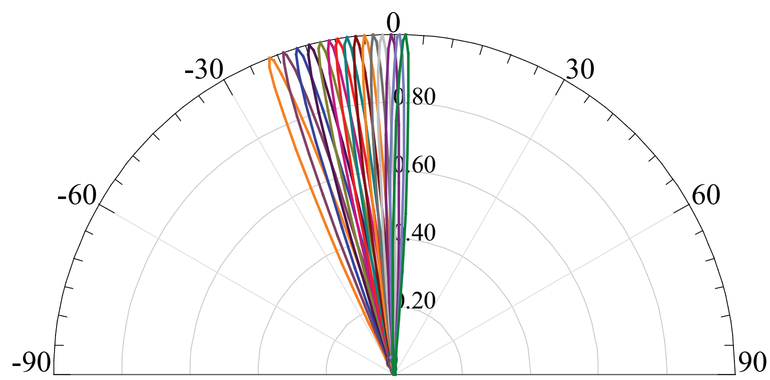
5.4 PolyStrata W-band and G-band Arrays

A 20-slot W-band broadside frequency-scanned array was designed with Ansoft HFSS. Figure 5.4 shows the 3D model of this array, where the dimensions are chosen to be compatible with a 10-layer PolyStrata process. Since this array is a traveling-wave array, the output must be matched. For this case wave ports are used at both ends of the waveguide to ensure a match at both ends of the array feed.

In order to achieve the greatest possible scan angle and the lowest gain variation over the scanning frequencies, several parameters, such as the length and width of the slots, the distance between each slot, and the lateral position of the slots from the center of the waveguide d were optimized. Figure 5.6 (a) shows the simulated realized gain at $\phi = 0$ for the frequency range of 83–105 GHz. For 3 dB gain variation the scan range is $\approx 16°$; if we allow 4 dB gain variation, the scanning increases to $> 20°$. Figure 5.6 (b) shows the normalized radiation pattern of the same antenna over the frequency range of interest.



(a)



(b)

Figure 5.6: (a)Simulated gain vs. θ at $\phi = 0$, for frequencies 83–105 GHz (from left to right with 2 GHz increments). (b) Normalized radiation pattern from 83–107 GHz (from left to right with 2 GHz increments)

To increase the scanning to $> 30°$ the width of the waveguide was reduced to 2 mm. This increases the cutoff frequency from 59 GHz for WR–10 to 76 GHz resulting in higher dispersion and more scanning. Figure 5.7 shows the simulated

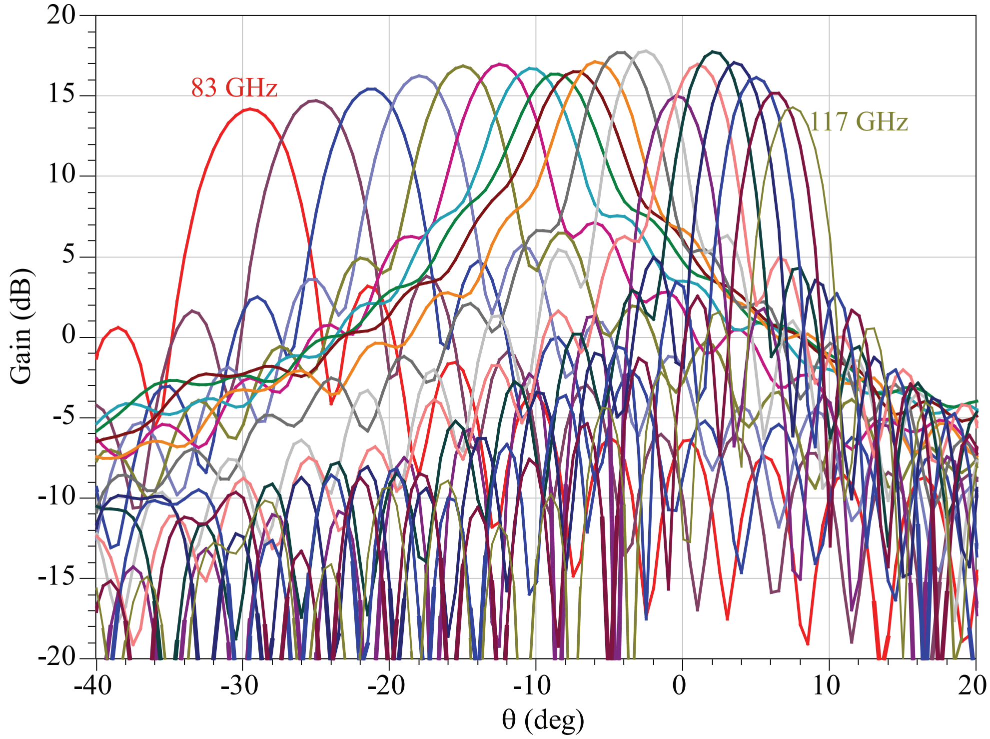


Figure 5.7: Simulated gain vs. θ at $\phi = 0$, for frequencies 83-117 GHz (from left to right with 2 GHz increments) for the reduced-width waveguide.

gain of a 20-element array at $\phi = 0$ for the frequency range of 83–117 GHz. Allowing for variations in gain of 3 dB, the scan range is approximately 32°. Although this method increases the achievable scanning range, it broadens the main beam between 91–99 GHz, and makes the beam non-uniform.

At broadside, the slots are spaced by even or odd multiples of $\lambda_g/2$. The input admittance for these slots is the sum of the slot's individual admittance and the characteristic admittance of the waveguide TE_{10} mode. Since the sum of the individual slot admittances cannot be zero, the input admittance is not equal to the characteristic admittance of the waveguide. Therefore the system is not matched, and the gain drops at broadside [71].

Following the above approach, a G-band broadside slot waveguide antenna array with 10 radiating elements was also designed. The size of standard G-band waveguide is 1.3 mm ×0.65 mm with f_c = 115 GHz. To increase the dispersion at the lower end of the waveguide band, the width of the waveguide is reduced to 1.19 mm, giving a cutoff frequency of 126 GHz. As mentioned in the previous sections, higher dispersion increases the phase shift and as a result the array will have a greater scanning range. Figure 5.8 shows the 3D model of this G-band antenna. The resultant simulated gain of this array is shown in Figure 5.9. The scanning range from 135 GHz to 180 GHz for 3 dB gain variation is about 34°. The gain drops at broadside for the same reason explained in the previous section. The pattern broadens around 150–155 GHz; this is due to non-uniform excitation of the slots at these frequencies. Figure 5.10 shows the electric field distribution at the top wall of the waveguide at 135, 150, and 180 GHz. At 150 GHz most of the power couples through the first few slots, causing main beam broadening. However, at 135 and 180 GHz, where the patterns are uniform as shown in Figure 5.9, the coupled power is uniformly distributed between all of the slots.

5.5 Possible Feeding Mechanism

To excite the TE_{10} mode in a W-band waveguide using micro-coaxial lines, a transition was designed utilizing an E-field probe by Oliver and colleagues [72]. Figure 5.11 (a) shows the 3D HFSS model of this transition. The probe is simply an extension of the micro-coaxial line's inner conductor into the back short W-band waveguide. The release holes do not have any significant effect on the performance of the transition due to their small size. Figure 5.11 (b) shows the s-parameter simulation results for this transition. This design can be easily modified for non-

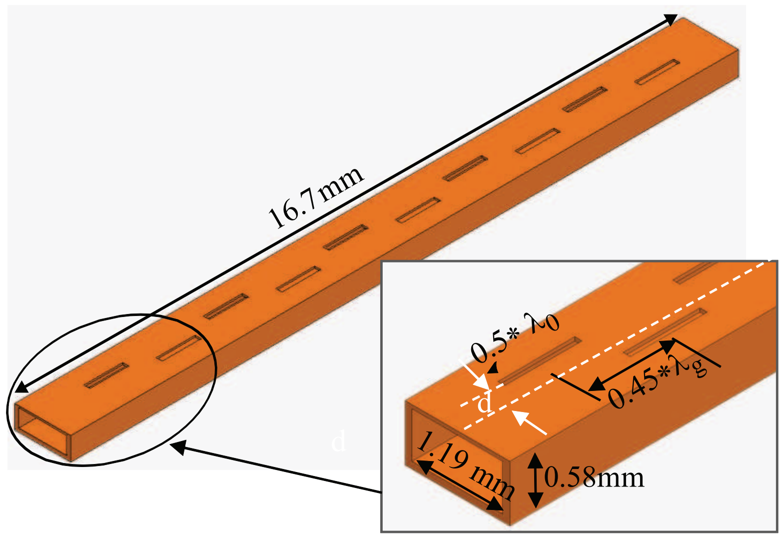


Figure 5.8: G-band broadside slotted waveguide array with 10 slots and an absorber at the end.

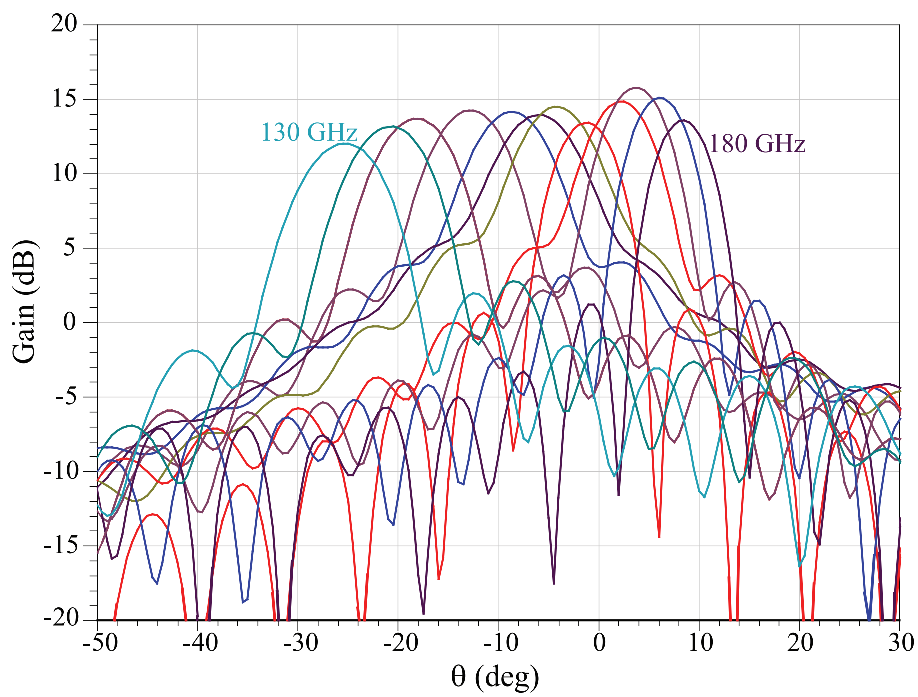


Figure 5.9: Simulated gain vs. θ at $\phi = 0$, for frequencies 130–180 GHz (from right to left in 5 GHz increments).

standard size waveguides, such as those discussed in this chapter.

Aperture coupling is a common approach to feed slotted waveguide arrays. This

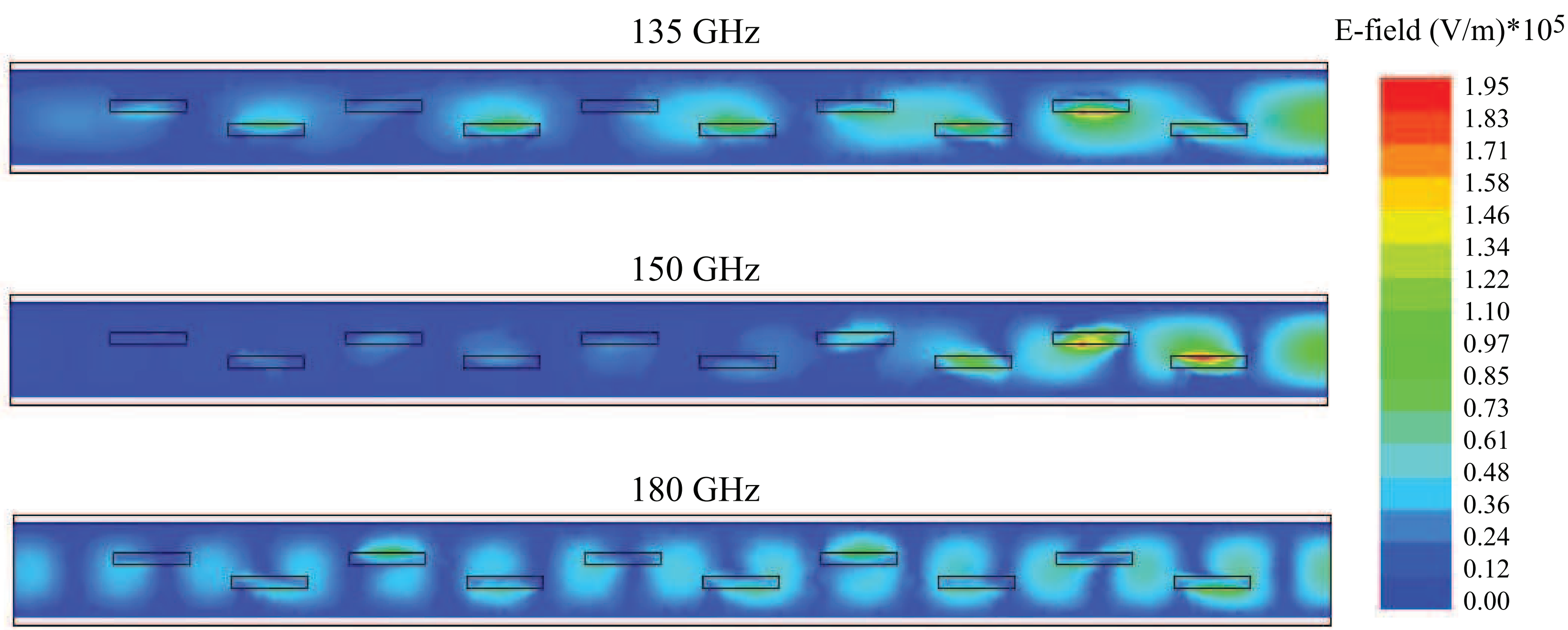
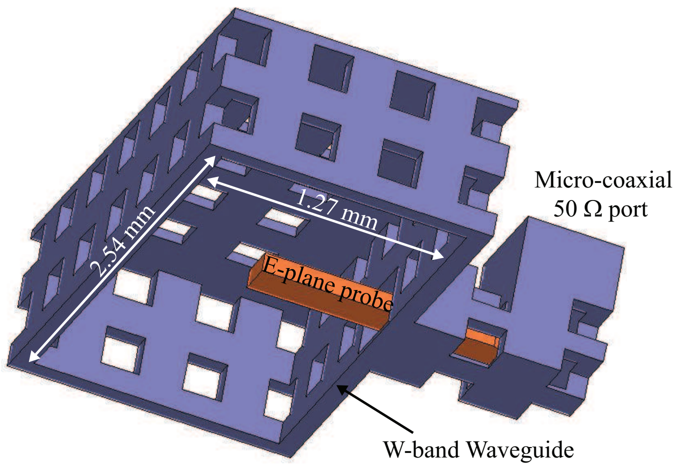
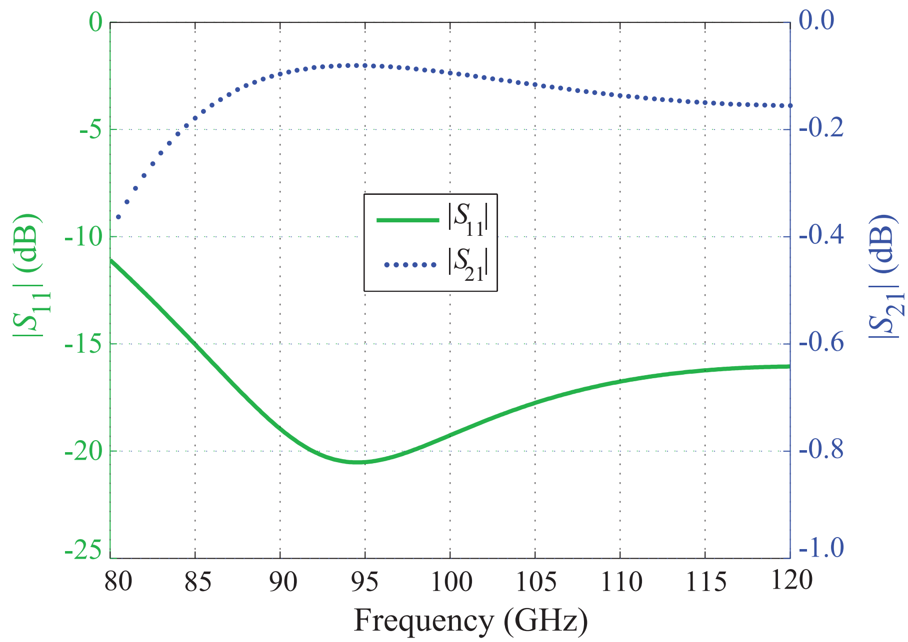


Figure 5.10: Electric field distribution on the top wall of the slotted waveguide at 135, 150, and 180 GHz. These plots explain why the main beam broadens at 150 GHz.



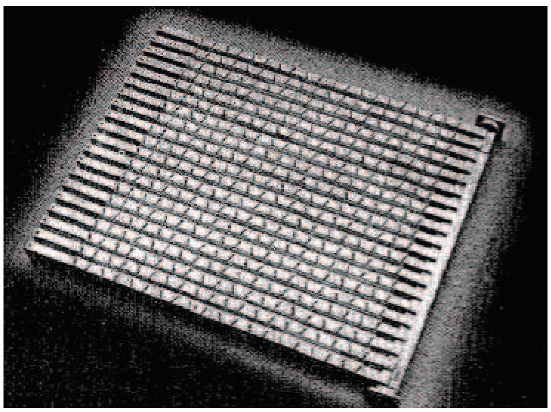
(a)

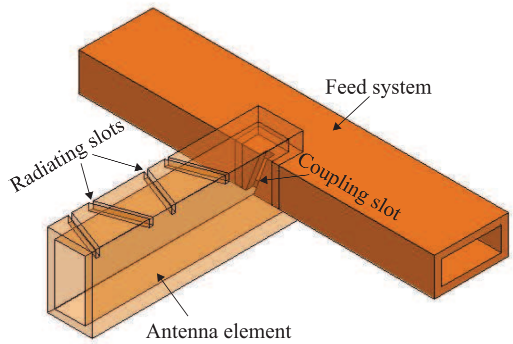


(b)

Figure 5.11: (a) Waveguide to micro-coaxial transition. $TE_1 0$ mode is excited through the extension of the inner conductor of the micro-coaxial line (E-probe). (b)Simulated s-parameter results of the waveguide to micro-coaxial transition.

method usually is a simpler and more compact design than the waveguide end-feed system given the same antenna designs. Large resonant planar arrays are typically fed using corporate or series-fed waveguide networks [63, pages9-10–9-11]. This method can be used for traveling-wave slotted waveguide arrays. In the design of a two-dimensional array, the aperture distribution for a given sidelobe level can be generated in the feed system, which excites each waveguide antenna element. The coupling is achieved by slots rotated to an angle that couples the correct amount of power into each sub-array. Figure 5.12 (a) shows a 400 element edge-slot waveguide array designed for 9 GHz, fed with an edge-slot waveguide (b). This array scans about 15° between 8.5–9.5 GHz [73].





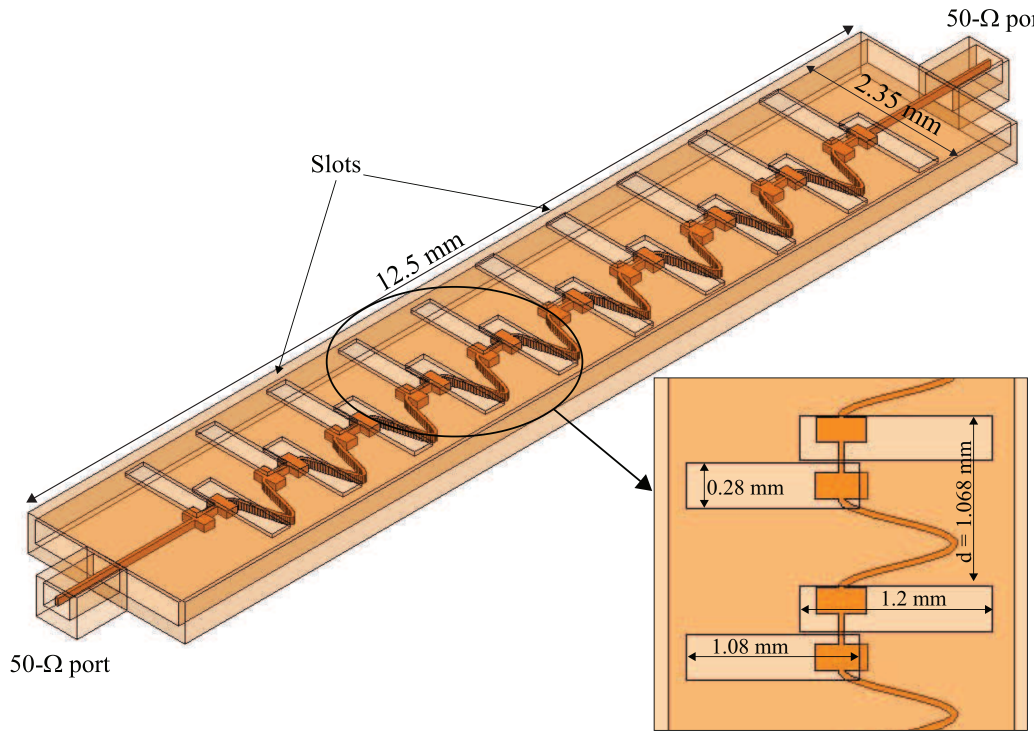
(a) (b)

Figure 5.12: (a) 400-element X-band planar edge-slot waveguide array fed by a linear edge-slot waveguide [73], (b) feed system employed for excitation of antenna elements.

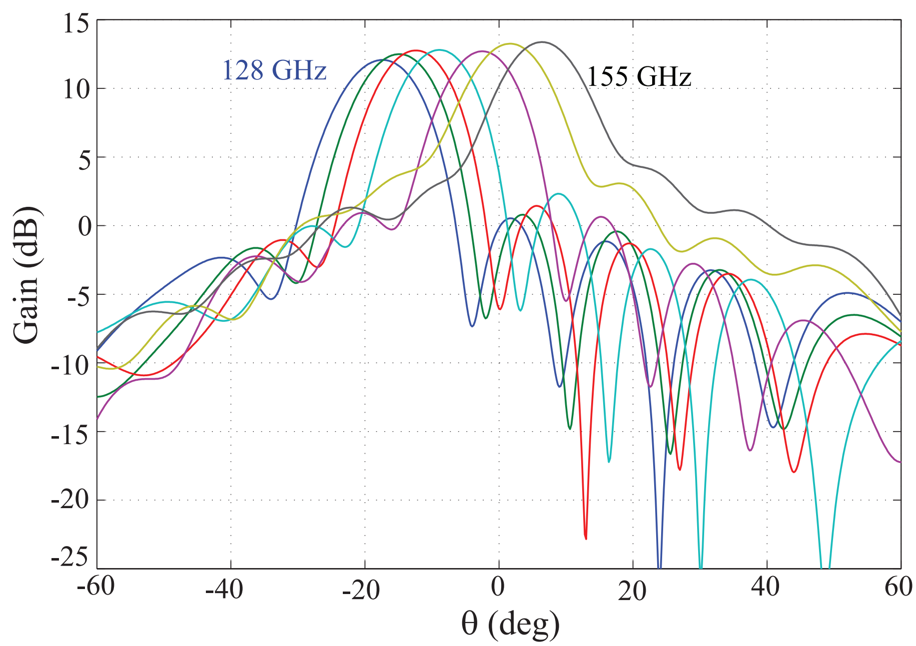
5.6 A Micro-coaxial Antenna Array

Micro-coaxial lines can be also used to feed an array of slots. Figure 5.13 (a) shows a micro-coaxial slotted array with 10 double slots. This work was performed by Dr. Leonardo Ranzani at CU and it is included in this chapter for comparison with the waveguide approach.

Since the micro-coaxial line that feeds the slots has very low dispersion, achieving



(a)



(b)

Figure 5.13: (a) Double slotted micro-coaxial antenna array. (b) Realized gain vs. θ at $\phi = 0$, for frequencies 128–155 GHz.

the desired frequency scanning with this method requires more design complexity. Several methods of increasing the scanning and increasing the bandwidth of the design have been investigated. Capacitive loading of the transmission line between the slots, meandering the transmission line between the radiating elements to provide two paths, increasing the size of inner conductor under the slots, changing the width of the slots, and using double slots are some of the methods that have been investigated. The best scanning is achieved when the inner conductor is meandered between double radiating slots (with a slight length difference), as well as using a wider inner conductor below the two slots as shown in Figure 5.13 (a). Figure 5.13 (b) shows the resultant beam steering of this array at $\phi = 0°$. The scanning is 30° from 128–155 GHz, and the gain is approximately constant for all scan angles. However, the pattern broadens and become non-uniform at higher frequencies. This is due to the non-uniform excitation of the slots at these frequencies.

The drawbacks of this method are the higher loss of micro-coaxial lines at higher frequencies compared to the waveguide, and the additional design complexity. However, the feeding mechanism for the slotted micro-coaxial array is simpler and measurements can be performed more directly compared to the slotted waveguide array.

5.7 Summary

In summary, this chapter presented initial designs of W-band and G-band frequency-scanned slotted-waveguide antenna arrays for implementation in the PolyStrata process. At W-band, a 20-element slot array is shown to steer 32° when excited between 80 GHz and 110 GHz. The design is extended to G-band where 32°

steering is obtained between 135 GHz and 170 GHz. A possible feeding mechanism is proposed. The performance of the G-band waveguide array is compared to a G-band micro-coaxial slotted array. Both arrays achieve the scanning goal, however the micro-coaxial slotted array is considerably more lossy at G-band compared to the waveguide approach.

Chapter 6

Discussion and Conclusion

With them the seed of wisdom did I sow, and with my own hand labour'd it to grow and this was all the harvest that I reap'd-: "I came like water, and like wind I go"

—Omar Khayyam

Perfection is achieved, not when there is nothing more to add, but when there is nothing left to take away.

—Antoine de Saint-Exupéry

Contents

This chapter summarizes the contributions of the thesis and presents some suggestions for future work. In particular, preliminary PolyStrata broadband power amplifier results are analyzed and possible improvements are suggested. Additional broadband components that can be envisioned in the PolyStrata technology are also discussed. Finally, extensions to the work on the W-band and G-band frequency-scanned arrays are presented.

6.1 Summary

This thesis presents a number of contributions in the areas of broadband microwave component design in a new technology. In many cases the results from this thesis exceed the performance of the state-of-the-art components found in the literature to date. The contributions can be summarized as follows:

In Chapter 2 the limits on characteristic impedance of micro-coaxial lines are considered in detail and confirmed for the first time with several experimental test structures. In order to obtain agreement with full-wave simulations, a careful study of on-wafer calibration standards was required and it is another practically important contribution discussed in this chapter. In addition, power handling limitations of PolyStrata micro-coaxial lines are analyzed both from the thermal perspective and the electric field breakdown perspective. These findings have been published in [4, 36, 74].

Chapter 3 is a comprehensive discussion of micro-coaxial broadband Wilkinson divider/combiners, including full-wave design and analysis, characterization methods and measurement results. The demonstrated bandwidth of 11:1 (2–22 GHz) is the highest reported in the literature and accompanied by low insertion loss 0.2–0.8 dB across the band. The associated amplitude and phase balance and isolation exceed specifications for most published and commercially available broadband dividers. The theoretical and experimental results on both 5-layer and 11-layer Wilkinsons with hybridly-integrated surface-mount resistors and miniaturized footprints are reported in [75].

In Chapter 4, an extension of UHF Guanella-type transmission line impedance transformers to the frequency range of 2–24 GHz is presented for the first time. This high frequency of operation and 12:1 bandwidth is enabled by the micro-coaxial lines and the PolyStrata process, which allows excellent control of the parasitics. Comprehensive full-wave analysis was applied to design of the inter connections within the transformer, mechanical support structures, substrate effects, and tolerance to geometrical and electrical imperfections. Theoretical and experimental results for 50–12 ohm and 50–22 ohm transformers are detailed in a recently submitted paper [54].

Chapter 5 presents initial designs of W-band and G-band frequency-scanned slotted waveguide antenna arrays for implementation in the PolyStrata process. At W-band, a 20-element slot array is shown to steer 32° when excited between 80 and 110 GHz (32 % bandwidth). The design is extended to G-band where 32° steering is obtained between 135 and 170 GHz. Most reported slotted waveguide arrays have been demonstrated at X-band and Ka-band, and one result was found around 76 GHz [76]. Therefore the designs presented in this chapter, when fabricated in PolyStrata, will be the highest frequency traveling-wave slotted waveguide frequency-scanning arrays.

This work is continuing at the University of Colorado in collaboration with Nuvotronics as a JPL planetary landing radar project and publications with the results from this chapter are anticipated after fabrication is completed.

6.2 Hybrid Broadband PolyStrata Amplifier Result

Components designed in Chapters 2, 3, and 4 were integrated in an implementation of a 20 W amplifier operating from 4–18 GHz, which can be used in the transmit section of a typical rf front-end. Figure 6.1 (a) shows the mask layout of the full final stage amplifier. This amplifier combines the power of four distributed MMIC GaN PHEMT power amplifiers. Each of the two dies combines on chip two PAs at their outputs, resulting in three-port GaN MMICs. Two of these MMICs are then combined in PolyStrata. The input and output impedances of the GaN devices are approximately 10 Ω from 4–18 GHz. The maximum available power for each MMIC is 20 W. The GaN devices are biased through hybridly-integrated broadband bias tees, designed by Cullens *et al.* [78] in a 12.5 Ω micro-coaxial environment. The bias tees consist of PolyStrata inductors and assembly structures for surface-mount chip capacitors similar to the resistor structures in Chapter 3. Similar assembly structures referred to as "active sockets" have been designed for the GaN MMICs that are wire-bonded to the input and output micro-coaxial lines. The matching networks immediately adjacent to the active sockets are the 4:1 impedance transformers described in Chapter 4, and the combining networks are the broadband Wilkinson devices described in Chapter 3. Figure 6.1 (b) shows a photograph of the portion of the total amplifier outlined with a green dashed line in Figure 6.1 (a). The full amplifier was fabricated on a silicon substrate and placed on a metal fixture for heatsinking purposes during power testing.

Figure 6.2 shows the preliminary measured output power result of the combined

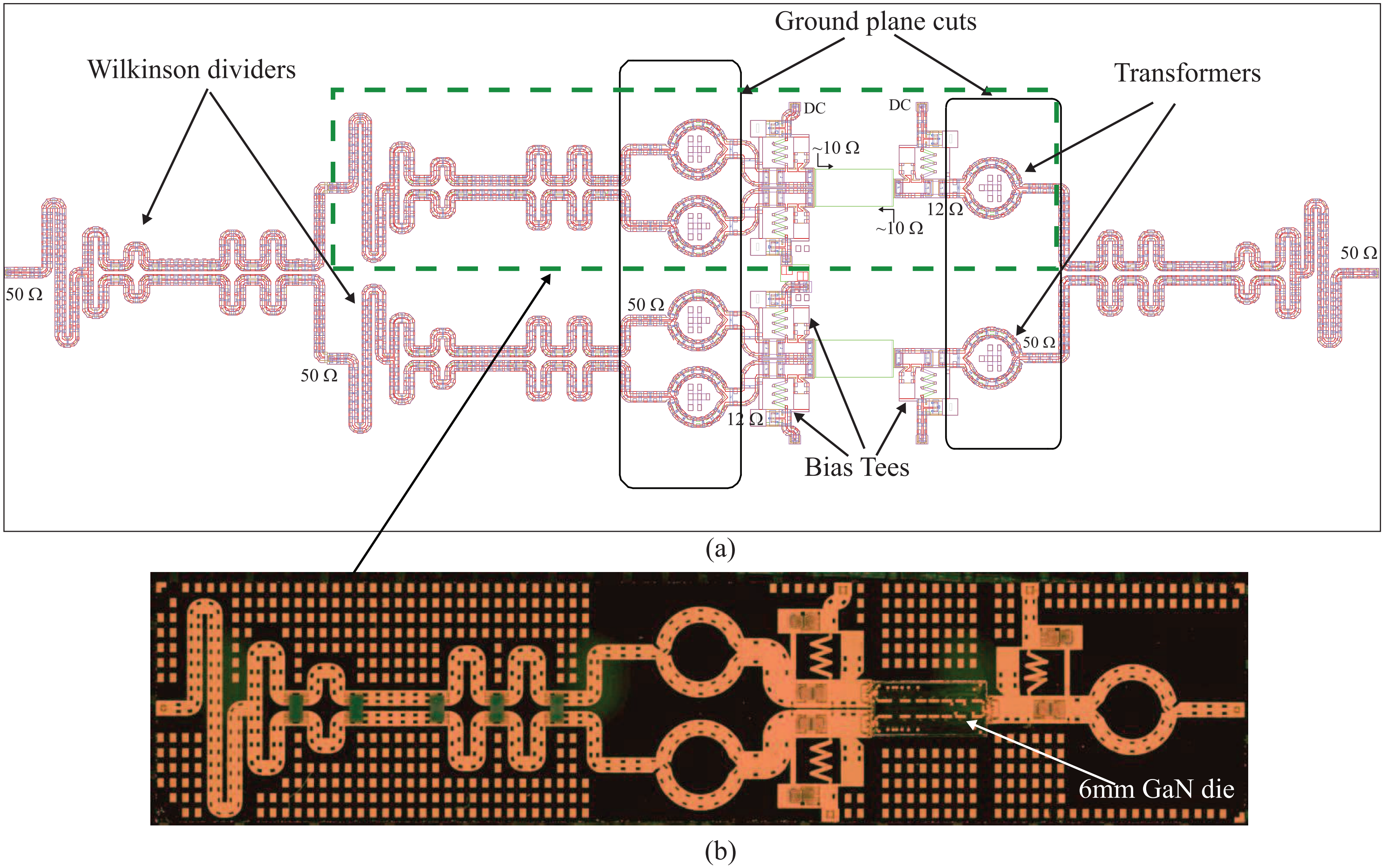


Figure 6.1: (a) Layout of a 20 W PolyStrata based 4–18 GHz power amplifier. The blank rectangles are spaces left for bonding GaN broadband MMICs fabricated by BAE Systems [77]. (b) Photograph of the top branch of the power combined PA.

amplifier in saturation, ranging 13–29 W over the band. There are several causes for the greater-than 3 dB output power variation over the operating frequency range, as discussed in the next section.

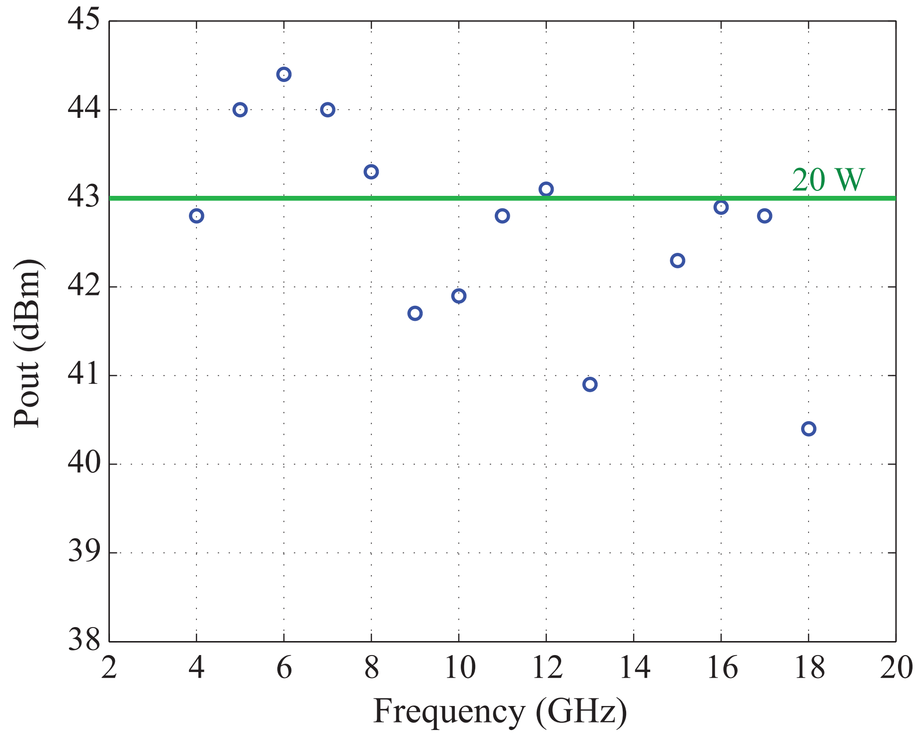


Figure 6.2: Power measurement result for the system shown in Figure 6.1.

6.2.1 Preliminary Power Measurement Discussion

The amplifier from Figure 6.1 was fabricated on silicon and placed on a metallic heat sink. As discussed in Chapter 4, when a TLT is placed on a high-ϵ_r substrate above a ground plane, sharp resonances appear in its s-parameter performance. To prevent this effect, holes were milled in the ground plane beneath each transformer. The locations of the holes are outlined in Figure 6.1 (a). These holes should have been filled with absorber to prevent the resonances, but at the time of measurements they were not. Thus it is possible that a contribution to the lower measured output power level at 13 GHz as shown in Figure 6.2 is due to substrate mode loss.

Another reason for the reduced output power is the bias tee performance. The bias tees were designed for 12.5 Ω lines, and due to the geometry of the 12.5 Ω line and mismatch to the non 12 Ω input and output MMIC impedances, the return loss was relatively poor; this is discussed in more detail in [78].

However, the main cause of the output power reduction is due to the inductance of the bond wires connecting the GaN die to the Polystrata environment. An inductive termination impedance can significantly affect the performance of the bias tees, 4:1 impedance transformers, and the Wilkinson dividers. To examine the effect of series reactance on the performance of the transformer in a circuit simulator, an inductor was added to the 12.5 Ω side of the transformer as shown in Figure 6.3. Figure 6.4 shows the simulated $|S_{11}|$ for the circuit in Figure 6.3. As shown, inductance as low as 0.1 nH reduces the input return loss from 28 dB to 8 dB.

Similarly, two inductors are added to the outputs of the Wilkinson divider as shown in Figure 6.5. This circuit has both imaginary and real mismatch, but as discussed in Chapter 3, real mismatch (up to 20 %) does not have any significant effect on the performance of the Wilkinson divider. The simulated $|S_{11}|$ of this circuit for different inductance values is shown in Figure 6.6.

Although the wire bonds were not directly attached to the Wilkinson dividers or the transformers in the combined amplifier, their effect on the bias tees can introduce imaginary mismatches, causing reflection and significant power drops. For example, for a 0.2 nH bond wire inductance between a 12 Ω bias tee and a 10 Ω MMIC input, the reflection coefficient on the bias tee side is around 0.7, implying

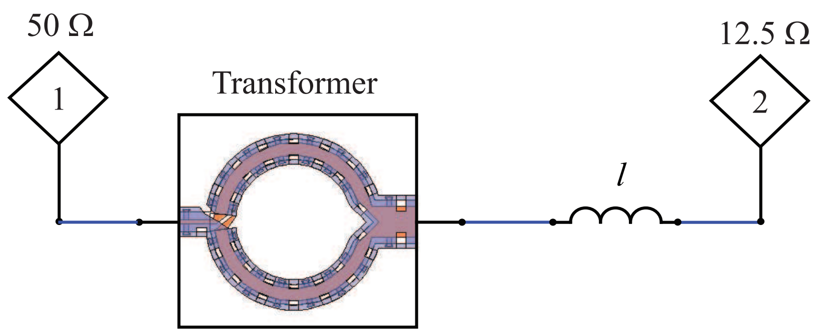


Figure 6.3: 4:1 impedance transformer with a series inductor connected to the $12.5\,\Omega$ port.

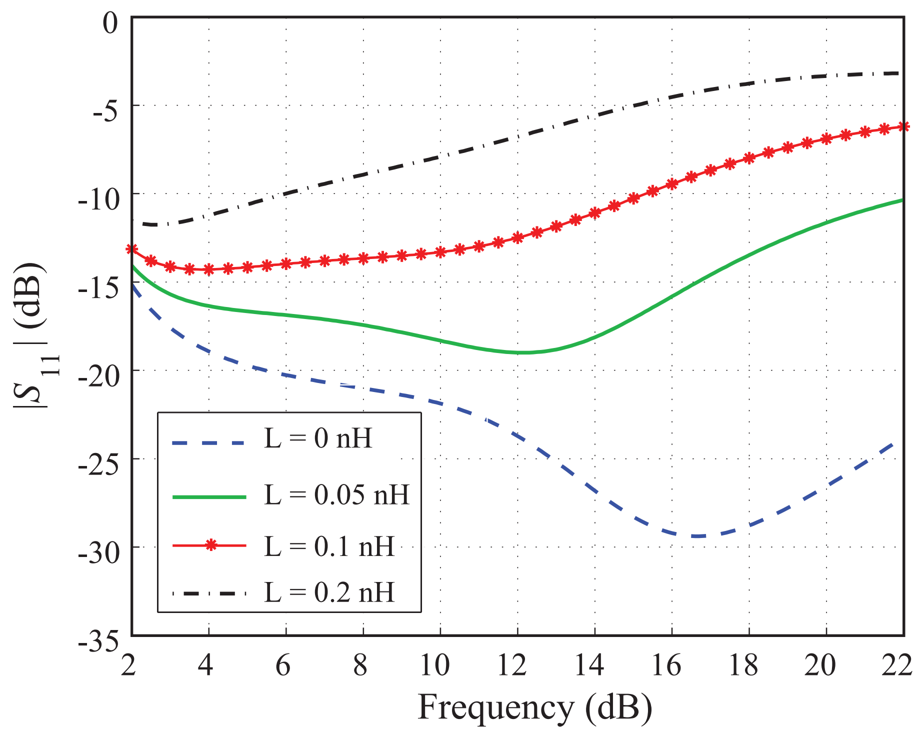


Figure 6.4: Simulated $|S_{11}|$ for the circuit shown in Figure 6.3. The inductors vary between 0–0.2 nH

that 50 % of the power is reflected.

The performance of the combined amplifier can be improved in several ways:

First, the silicon under the transformers can be back-etched to eliminate substrate mode loss. The second significant improvement would be to eliminate bond wires via flip-chip assembly. Prematching implemented in PolyStrata can also be

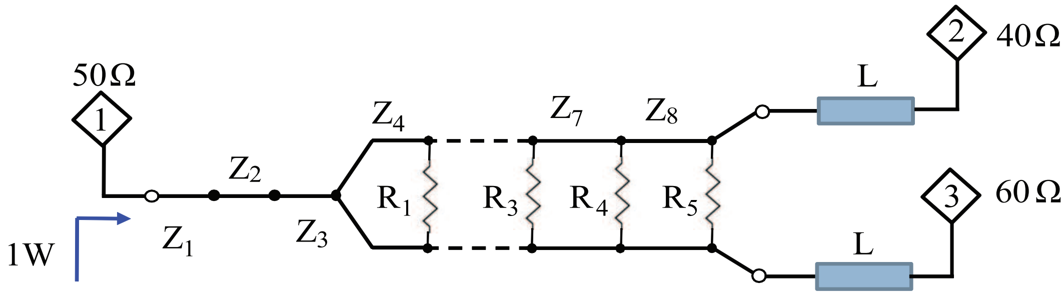


Figure 6.5: Broadband Wilkinson divider with series inductors connected to the two output ports.

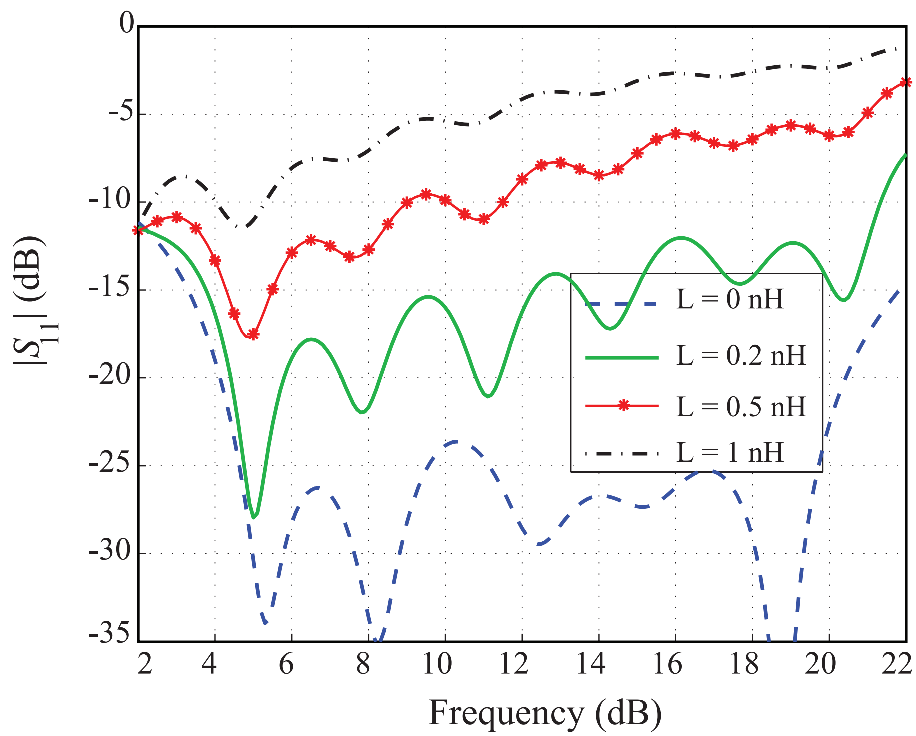


Figure 6.6: Simulated $|S_{11}|$ for the Wilkinson divider with inductors connected to the two output ports. The inductors vary between 0–1 nH

implemented to compensate for the bond wire reactance over a broad frequency range, at the expense of increased size and loss. Finally, an improved package with improved interconnects to the driver amplifier and output load would significantly flatten the power response over the bandwidth.

6.3 Suggestion for Future Work

This section presents some preliminary designs which are extensions to the work described in Chapters 3, 4, and 5. Although fully designed, these components have not been fabricated and measured, but based on excellent simulation/measurement agreement of related structures, it is expected that these components will perform as designed.

The implemented divider networks from Chapter 3 were all designed for $50\,\Omega$ ports. The intended application for this component is a miniaturized power-combining broadband amplifier. Since active devices have low input and output impedances, it is advantageous to have the Wilkinson divider also perform partial impedance matching to the active device. Therefore, a broadband Wilkinson divider was designed in the eleven-layer PolyStrata configuration, with an input port impedance of $50\,\Omega$ and two $32\,\Omega$ output ports. The circuit schematic is the same as that of the eleven-layer divider in Section IV B and shown in Figure 3.14. The characteristic impedances and lumped resistor values for this type of design are given in Table 6.1.

Table 6.1: Eleven-layer $50\,\Omega$ to $32\,\Omega$ Wilkinson parameters

Section	0	1	2	3	4	5	6
$Z\,[\Omega]$	50	44.7	37.3	59.3	48	42	37
$l\,[\mathrm{mm}]$	1	6	6	5	3.8	5.3	5.2
$R\,[\Omega]$	—	50	200	200	200	—	—

Another divider with low input and output impedances was designed for $12.5\,\Omega$ ports, in the eleven-layer PolyStrata process. The characteristic impedances selected for this divider are based on an optimization process and range from $12.5\,\Omega$ to $22\,\Omega$, and the resistor values are $25\,\Omega$, $50\,\Omega$, $100\,\Omega$, and $100\,\Omega$. The input port consists of one section that is 12.5 Ω, unlike the other dividers in Chapter 3. Since the characteristic impedances necessary for this divider are relatively low, the inner conductor height shown in Figure 3.15 (a) is increased to 700 µm (layers 3 to 9). This can cause problems in the design of the passive sockets, since the electric field distribution is highly concentrated in the top (layer 10) and bottom (layer 2) gaps between the inner and outer conductors. In order to reduce the exposure of the electric field to the open areas of the passive sockets, the inner conductor is designed to be on layers 3 to 8 (i.e., vertically offset from the center), leaving a gap of 150 µm on the top between the inner and outer conductor. This causes the electric field distribution to be concentrated in layer 2, and less concentrated between layers 9 and 10, making the structure suitable for implementing the sockets. Figure 6.7 shows the electric field distribution for the two 12.5 Ω lines implemented in the eleven-layer configuration. This divider exhibits 2–22 GHz bandwidth, and its overall length after miniaturization is 14.5 mm. Figure 6.8 shows a 3D rendering of the 12.5 Ω to 12.5 Ω divider without release holes and dielectric straps. Figure 6.9 shows the simulated s-parameter results of this divider.

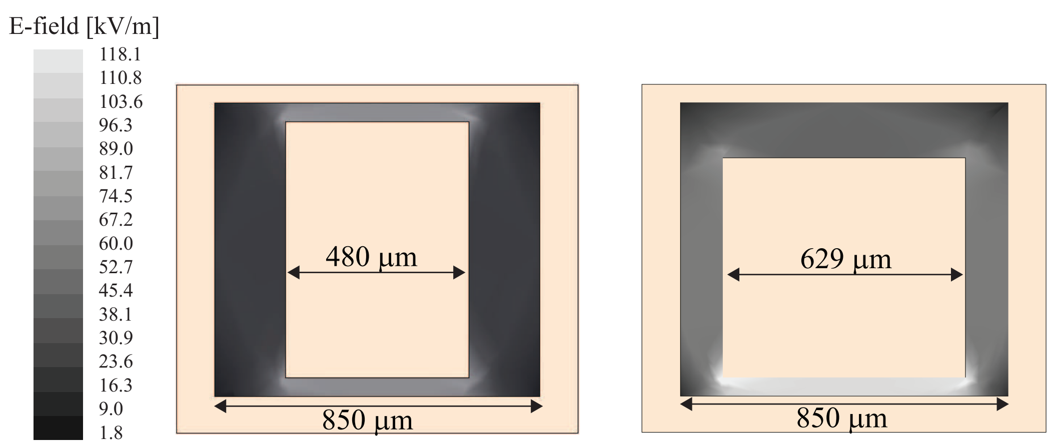


Figure 6.7: Electric field distribution in 12.5 Ω lines in eleven-layer configuration for inner conductor height of (left) 700 µm and (right) 600 µm.

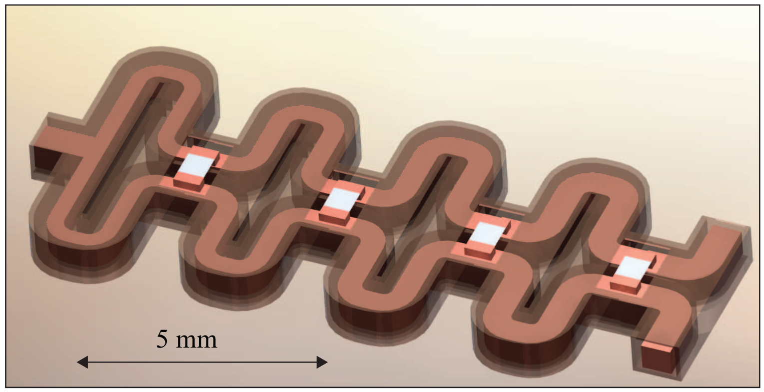


Figure 6.8: Rendering of the miniaturized 12 Ω to 12 Ω Wilkinson divider implemented for the eleven-layer fabrication process. Release holes and straps are not shown in this figure. The outer conductor is rendered with 50 % transparency to show the inside of the divider.

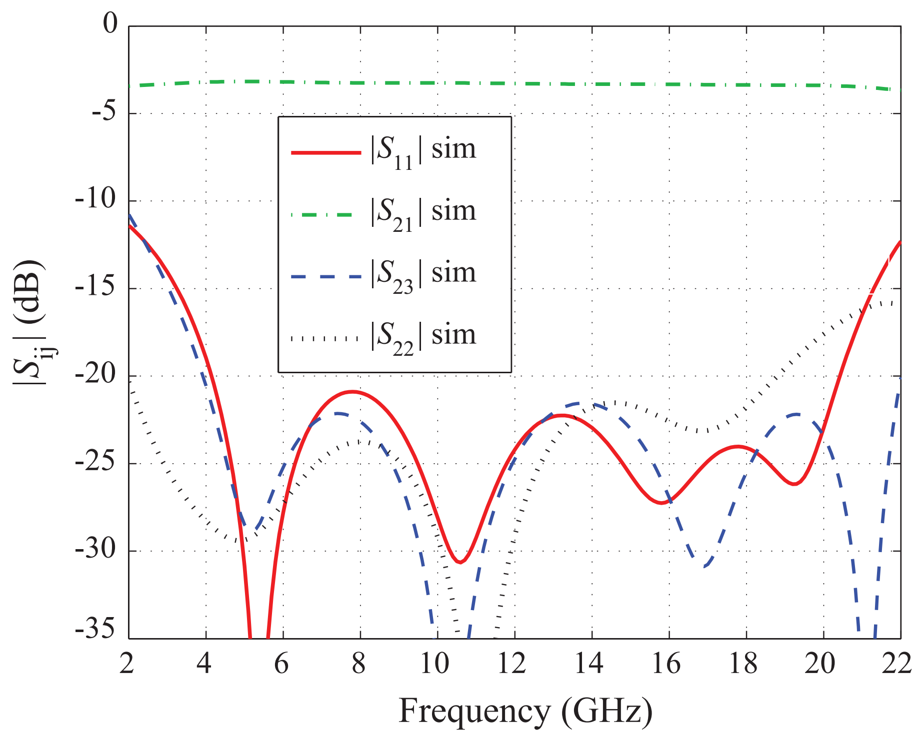


Figure 6.9: HFSS s-parameter simulation results for the 12 Ω to 12 Ω Wilkinson divider.

The 4:1 impedance transformer configuration can be used to implement other transformation ratios that are close to 4:1, such as 3:1, by simply changing the characteristic impedance of the transmission lines and/or the input and output port impedances. This resulting transformer is no longer frequency independent and so the performance is not as good as a 4:1 transformer. Figure 6.10 shows a transformer that transforms $5\,\Omega$ to $16\,\Omega$ designed for the 11-layer process; the characteristic impedance of the transmission lines is $9.5\,\Omega$. The s-parameter simulation results are shown in Figure 6.11; compared to an ideal linear taper that matches $5\,\Omega$ to $16\,\Omega$ with 14 dB return loss above 2 GHz, this transformer is an order of magnitude shorter and will have more uniform group delay.

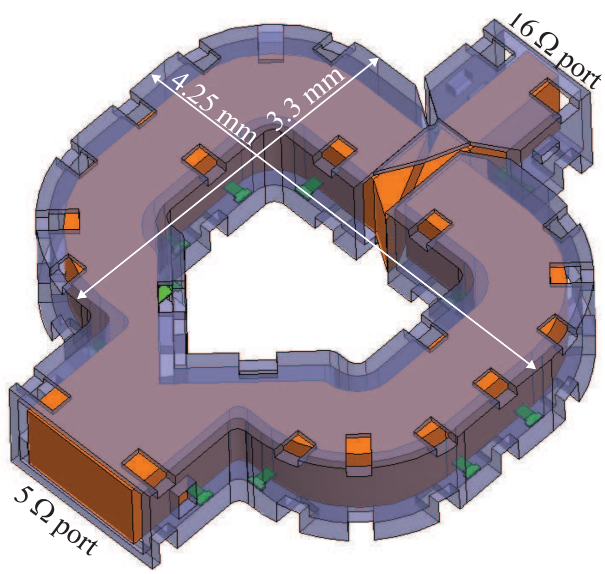


Figure 6.10: 5 to $16\,\Omega$ impedance transformer with $9.5\,\Omega$ impedance branches.

In Chapter 5 only broadside frequency-scanned array designs were discussed. However, edge-slot frequency scanned arrays are possible and have excellent scanning capabilities. To design an edge slot array, the broadside width of the array needs to be reduced to be manufacturable with PolyStrata technology. To this end, ridge-type waveguides can be designed with a broadside wall width of less than 50 % of the standard waveguide width. The theory and experimental results of broad-wall slotted ridge waveguide arrays have been studied [79, 80, 81]. These designs can be extended to edge-wall slotted ridge waveguides. Figure 6.12 (a)

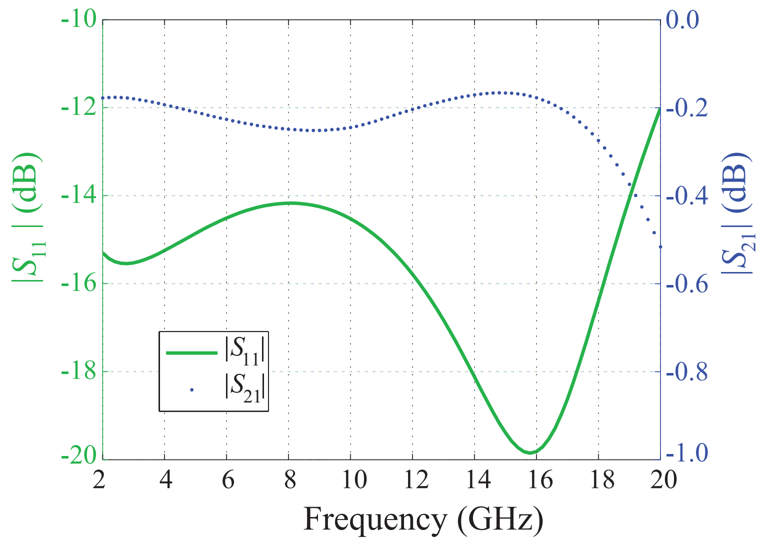
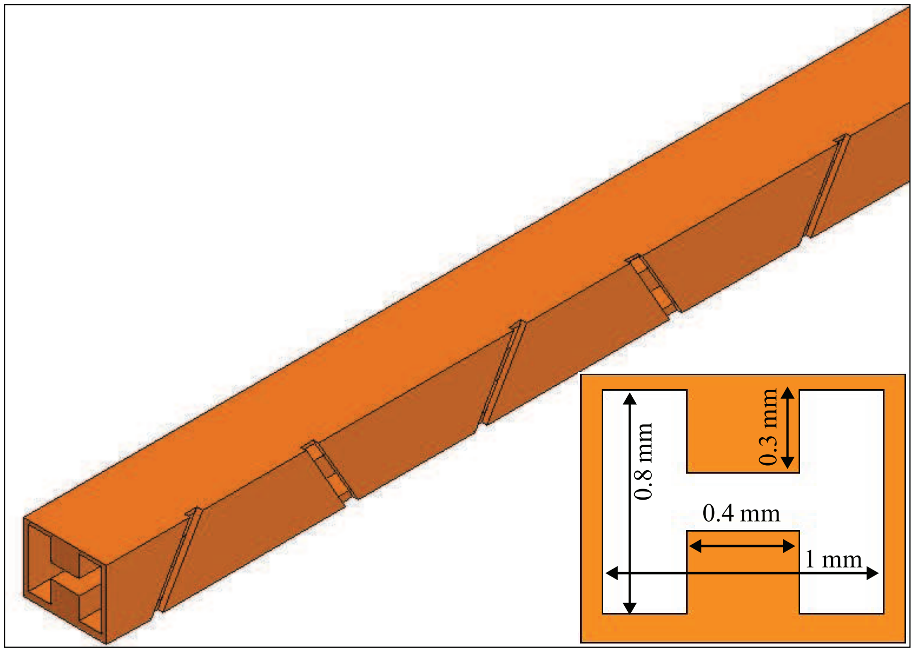


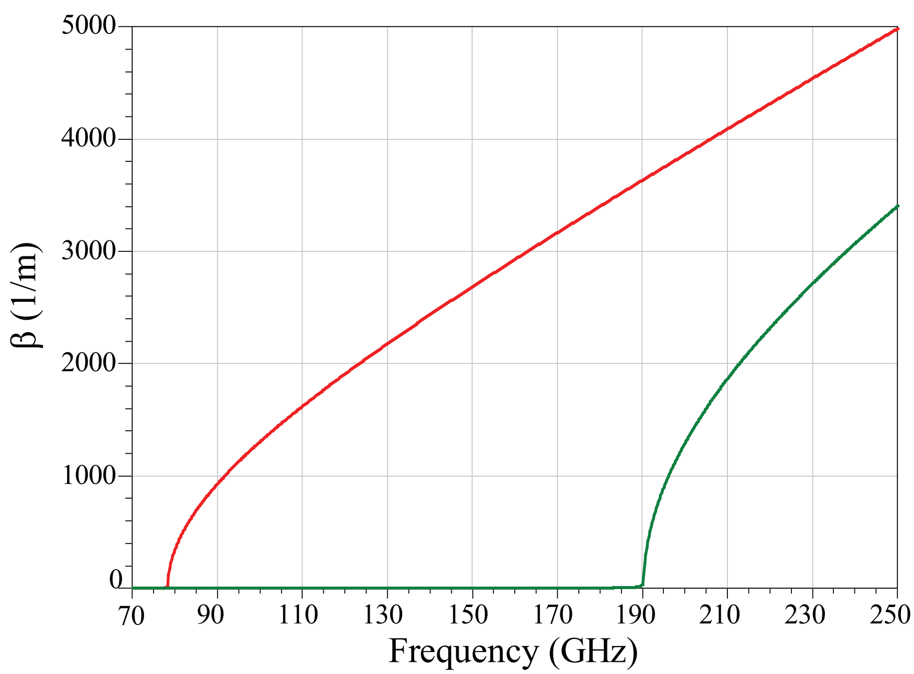
Figure 6.11: Simulated s-parameters for the transformer from Figure 6.10.

shows an example of a W-band ridge waveguide that can be used for an edge-slot antenna array. Figure 6.12 (b) shows the simulated β diagram (imaginary part of γ) of this waveguide; the cutoff frequency of the fundamental mode in this waveguide is 79 GHz.

In summary, this thesis presents new designs of a number of broadband microwave and millimeter-wave passive components at frequencies from 2 to 170 GHz. The performance of the components is comparable to or exceeds the state-of-the-art results found in the literature as a result of their implementation in the microfabricated coaxial and waveguide PolyStrata process. In the research collaboration that led to this thesis, the components were all fabricated in the Nuvotronics LLC process, while the designs, optimization and characterization were performed at the University of Colorado. The thesis results are reported in a number of journal and conference publications, and pave a path to new or improved microwave and millimeter-wave components and sub-systems.



(a)



(b)

Figure 6.12: (a) HFSS model of a W-band slotted ridge-waveguide; (b) β-diagram showing the first two propagating modes in the waveguide. The cutoff frequency of the fundamental mode is 79 GHz.

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