X-Band Outphasing GaN MMIC PA with Power Recycling

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***Abstract*—We demonstrate an outphasing GaN MMIC PA with power recycling operating at 10.35 GHz. The MMIC includes high-efficiency PAs, a miniaturized rat-race combiner, and a high-efficiency, self-synchronous transistor rectifier. A peak total efficiency of 65.2 % is achieved with 6 W of output power. Up to 2.24 W of rectified power improves total efficiency by up to 6.5 points at -3.5 dB normalized output power, matching presented theory.**

***Index Terms*—outphasing, LINC, rectifier, power amplifier.**

I. Introduction

Outphasing power amplifiers offer a solution to the trade-off between linearity and efficiency when amplifying signals with complex modulation schemes [1]. Amplitude modulation is converted into differential phase modulation, enabling each of the two PAs to operate in saturation without contributing distortion to the system. The combiner performs a vector addition of the signals, reconstructing the envelope. The choice between isolated and non-isolated combining is a trade-off between linearity and efficiency, respectively [2]. The isolated combiner suffers a sharp roll-off in efficiency due to power dissipated in the isolated port.

At frequencies below 2 GHz, [3]–[5] improved the efficiency in an isolated outphasing PA by rectifying the RF power wasted in the isolated port. Further research on diode based rectifiers has been performed in [6], [7]. At X-band frequencies, however, diodes cannot efficiently rectify watt-level power. Thus, the time-reversal duality of high-efficiency PAs from [8] is employed to create a high-efficiency transistor rectifier. In this work, we present an outphasing GaN MMIC PA with power recycling, operating at 10.3 GHz, the highest frequency reported in the literature for outphasing PAs, to the best of our knowledge. The GaN integrated design utilizes a high-efficiency, self-synchronous transistor rectifier.

II. Theoretical Principle

Considering the isolated outphasing PA shown in Fig. 1, expected efficiency improvement can be found with the assumptions that (1) the internal PAs are identical, matched, and isolated, (2) the rectifier is matched and operates at constant efficiency, and (3) the combiner is lossless.

From the constant envelope signals in [9], the power at the sum and difference ports are found as:

$$P_{\sum} = 2P_{out,PA}\cos^2(\theta) \tag{1}$$

$$P_{\Delta} = 2P_{out,PA}\sin^2(\theta) \tag{2}$$

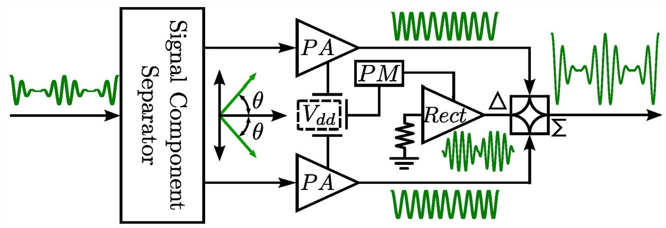

Fig. 1. Block diagram of an outphasing PA with power recycling. This work utilizes a high-efficiency transistor rectifier on the isolated combiner port to recover over 2 watts of power at 10.3 GHz.

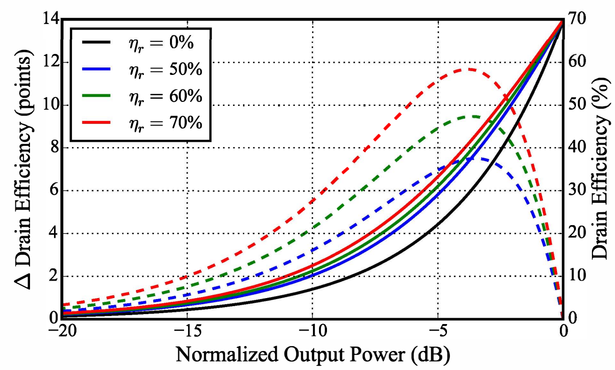

Fig. 2. Theoretical improvement in system drain efficiency with rectification of power on the isolated port. $\eta_{d,PA}$ = 70 %, and η_r is set to 50 %, 60 %, and 70 %.

where θ is the outphasing angle. The total DC power consumption can be related to the drain efficiency of the internal PAs, $\eta_{d,PA}$, as:

$$P_{DC,tot} = 2\frac{P_{out,PA}}{\eta_{d,PA}} \tag{3}$$

The system drain efficiency without rectification is simply:

$$\eta_d = \frac{P_{\sum}}{P_{DC,tot}} = \eta_{d,PA}\cos^2(\theta) \tag{4}$$

Considering the rectified power, the system drain efficiency becomes:

$$\eta_{d,r} = \frac{P_{\sum}}{P_{DC,tot} - \eta_r P_{\Delta}} = \frac{\eta_{d,PA}\cos^2(\theta)}{1-(\eta_{d,PA})(\eta_r)\sin^2(\theta)} \tag{5}$$

where η_r is the rectification efficiency. The efficiency improvement with rectification is:

$$\Delta\eta_d = \eta_{d,r} - \eta_d = \frac{(\eta_{d,PA}^2)(\eta_r)\cos^2(\theta)\sin^2(\theta)}{1-(\eta_{d,PA})(\eta_r)\sin^2(\theta)} \tag{6}$$

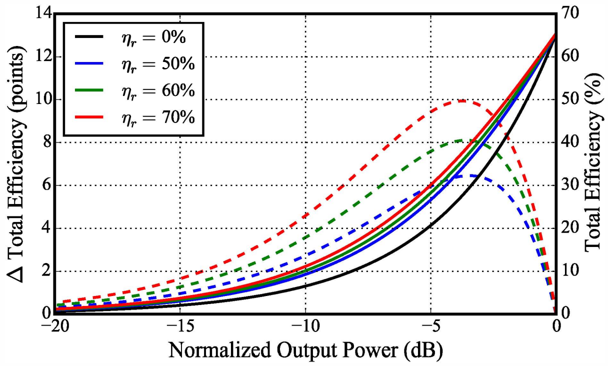

Fig. 3. Theoretical improvement in system total efficiency with rectification of power on the isolated port. $\eta_{d,PA}$ = 70 %, and η_r is set to 50 %, 60 %, and 70 %.

Fig. 2 illustrates the theoretical improvement in system drain efficiency given by the rectifier. $\eta_{d,PA}$ is set to 70 % with η_r set to 50 %, 60 %, and 70 %, leading to peak $\Delta\eta_d$ values of 7.5, 9.5, and 11.7 points, respectively, which all occur at -3.5 dB normalized output power ($P_{out,n}$).

In outphasing, the efficiency definition should include input power, since it is constant and significant. We consider the total efficiency, because the PAE unintuitively drops below zero when $P_{out} > P_{in}$. The available input power is defined as:

$$P_{av} = \frac{2P_{out,PA}}{G} \tag{7}$$

where G is the available power gain of the internal PAs. The system total efficiency is:

$$\eta_{tot} = \frac{P_{\sum}}{P_{DC,tot} + P_{av}} = \frac{(G)(\eta_{d,PA})\cos^2(\theta)}{G + \eta_{d,PA}} \tag{8}$$

Considering the rectified power, the system total efficiency becomes:

$$\begin{aligned} \eta_{tot,r} &= \frac{P_{\sum}}{P_{DC,tot} + P_{av} - \eta_r P_{\Delta}} \\ &= \frac{(G)(\eta_{d,PA})\cos^2(\theta)}{G + \eta_{d,PA} - (G)(\eta_{d,PA})(\eta_r)\sin^2(\theta)} \end{aligned} \tag{9}$$

The efficiency improvement with rectification is:

$$\begin{aligned} \Delta\eta_{tot} &= \eta_{tot,r} - \eta_{tot} \\ &= \frac{(G^2)(\eta_{d,PA}^2)(\eta_r)\cos^2(\theta)\sin^2(\theta)}{[G + \eta_{d,PA}][G + \eta_{d,PA} - (G)(\eta_{d,PA})(\eta_r)\sin^2(\theta)]} \end{aligned} \tag{10}$$

Fig. 3 illustrates the theoretical improvement in system total efficiency given by the rectifier. $\eta_{d,PA}$ is set to 70 % with η_r set to 50 %, 60 %, and 70 %, leading to peak $\Delta\eta_{tot}$ values of 6.5, 8.1, and 9.9 points, respectively, which all occur at -3.5 dB normalized output power ($P_{out,n}$).

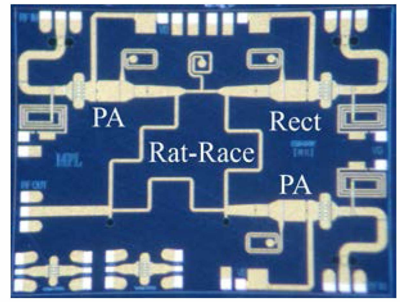

Fig. 4. Photograph of outphasing GaN MMIC PA with integrated rectifier. PAs and rectifier utilize 10x100 μm pHEMTs. 180° rat-race provides isolation and combining.

III. MMIC Design

The MMIC is fabricated in TriQuint's 0.15 μm GaN process. The internal PAs utilize a single 10x100 μm pHEMT, are optimized for efficiency, and biased at pinch-off. Simulation shows a peak PAE of 60 % with an output power of 34.6 dBm.

The rectifier is an exact duplicate of the internal PAs. As demonstrated in [8], [10], high-efficiency rectifiers are the dual of high-efficiency PAs. Since the periphery of the rectifier is half of the total PA periphery, the rectifier will reach peak efficiency at half the envelope magnitude and maintain it as the envelope decreases.

A 180° rat-race combiner achieves 46 dB isolation and 31 dB return loss. Due to size constraints, the 270° TL is approximated by a C_s-L_p-C_s high-pass T-network, and the 90° TLs are approximated by C_p-L_s-C_p low-pass Pi-networks, given in [11] but with a TL replacing L_s as in [12]. The input impedance of the rectifier will vary with input power [10] and may de-tune the combiner, effectively reducing isolated port power at low envelope magnitudes. However, simulation shows that under large loading mismatch ($Z_L = 10\,\Omega$, $300\,\Omega$), performance will not be affected significantly since the rectifier still receives enough input power to maintain peak efficiency.

IV. Measurement Setup and Method

In the measurement setup in Fig. 5, a phase shifter sweeps the differential phase, φ, which is twice the outphasing angle, θ. The variable attenuation of the phase shifter is overcome by adjusting the source amplitude on that branch. Constant available power is maintained to within 0.1 dB after calibration, whereby offsets are calculated for each phase shifter control voltage. The available power of the second source is calibrated to match that of the first, in order to maintain balance (<0.1 dB) between the two inputs. The RF inputs and output are filtered and measured with a power meter.

As discussed in [10] and shown in Fig. 5, the rectifier has three parameters: R_D, $V_{GG,r}$, and Z_{gate}, which are the DC load, the bias voltage, and the RF load, respectively. Note that we did not implement a circuit handle the rectified power, which is dissipated in the DC load. Additionally, several PA parameters must be determined: frequency, available power, and PA bias. Due to the large number of unknown parameters, a method is developed to find optimal operation.

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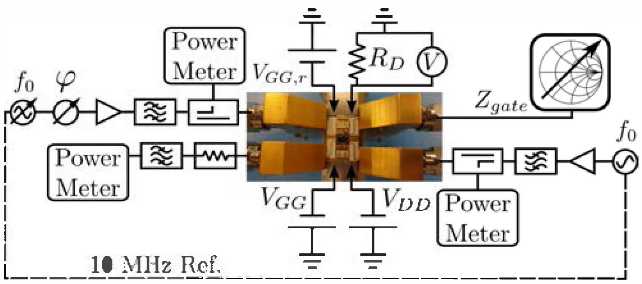

Fig. 5. Measurement setup sweeps differential phase while maintaining balanced available power (<0.1 dB). The rectifier parameters (R_D, $V_{GG,r}$, and Z_{gate}), and PA parameters (Freq, P_{avail}, V_{GG}, V_{DD}) are tunable.

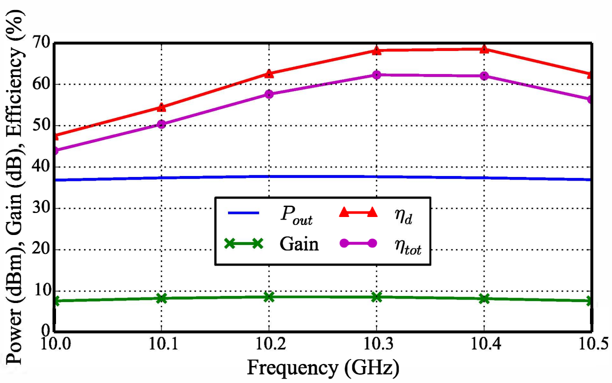

Fig. 6. Power, gain and efficiency across frequency with in-phase drive. $\eta_{tot} > 50\,\%$ and $P_{out} > 5\,\text{W}$ achieved over at least 400 MHz bandwidth.

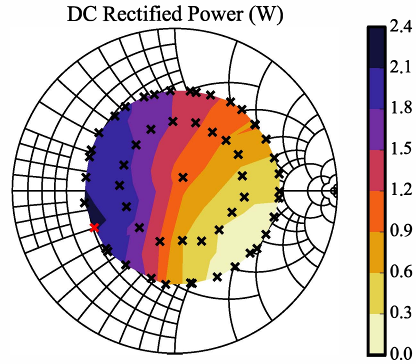

Fig. 7. Rectifier load-pull (Z_{gate}) for DC rectified power reaches a sensitive peak of 2.24 W. Because $|\Gamma|$ is limited to 0.6, optimal rectified power and efficiency cannot be achieved. Smith Chart is normalized to 50 Ω.

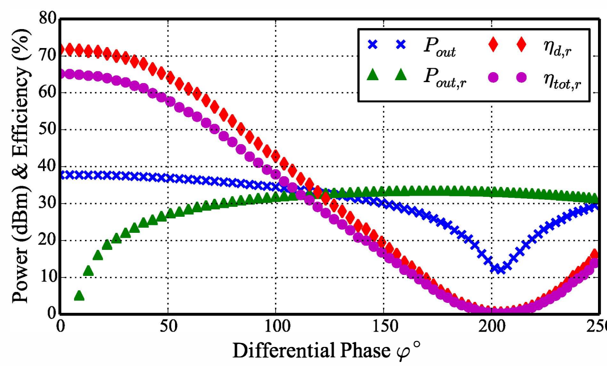

Fig. 8. RF output power, DC rectified power, $\eta_{d,r}$, and $\eta_{tot,r}$ with optimal PA and rectifier parameters. A peak η_{tot} of 62.5 % is achieved with 6 W of RF output power at 10.35 GHz.

First, the optimal PA operation is determined with frequency, power, and bias swept measurements. Because performance at peak output power is evaluated here, the rectifier parameters are set to conservative values. Typically, transistor rectifiers are biased at pinch-off [10]. R_D was set to an estimated value of 100 Ω, and Z_{gate} is set at 50 Ω. Fig. 6 illustrates performance at peak power across frequency for the optimally found available power of 26.2 dBm and bias of -4.0 V. The MMIC achieves $\eta_{tot} > 50\,\%$ and $P_{out} > 5\,\text{W}$ over at least 400 MHz bandwidth. A finer sweep revealed the optimal operating frequency to be 10.35 GHz.

Next, the rectifier parameters are swept with those of the PA fixed at optimal values. Rectified power is measured while load-pull is performed on the gate of the rectifier over various bias conditions and DC loads. The differential phase is set to produce the minimum RF output power prior to the load-pull, to ensure that the rectifier is being driven hardest. Fig. 7 shows an optimal rectifier load-pull measurement for $R_D = 50\,\Omega$ and $V_{GG,r} = -4.0\,\text{V}$, with 2.24 W of rectified power. Although Z_{gate} is the most sensitive parameter for rectified power, it is insensitive to variation of R_D and $V_{GG,r}$. Losses between the MMIC and tuner at X-band limit the $|\Gamma| \leq 0.6$. Improved performance is expected with a higher reflection coefficient, achieved in active load-pull as in [10] or on-chip termination.

V. Outphasing Results

With all of the optimal PA and rectifier parameters set, the system performance is measured in Fig. 8. $\eta_{d,r}$ and $\eta_{tot,r}$ include rectified power, and reach peaks of 71.80 % and 65.2 %, respectively, at a peak output power of 37.78 dBm or 6 W at 10.35 GHz. As expected the output power and efficiency peak when driven in-phase, and decrease with differential phase, opposite of the rectified power.

The efficiency improvement achieved through the addition of the rectifier is demonstrated in Figs. 9 and 10, with up to 2.24 W of rectified power. η_d and η_{tot} do not include the rectified power, while $\eta_{d,r}$ and $\eta_{tot,r}$ do. The differences, labeled $\Delta\eta_d$ and $\Delta\eta_{tot}$, reach peak values of 8.1 and 6.5 points at -3.5 dB normalized output power, respectively. The efficiency improvement is confined to the middle region of $P_{out,n}$, because little power is available for rectification at peak output power, and rectified power becomes insignificant at very low output power.

The agreement between measurement and theory shows that the idealized assumptions are realistic. An internal PA drain efficiency of 71.8 % and gain of 8.5 dB are extracted from measurement and used in theoretical calculations. Although

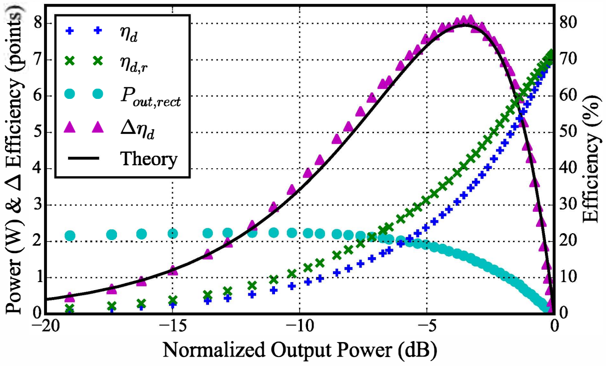

Fig. 9. Measured η_d, $\eta_{d,r}$, DC rectified power, $\Delta\eta_{d,r}$, and theoretical $\Delta\eta_{d,r}$ demonstrating efficiency improvement through power recycling as envelope amplitude is decreased. Up to 2.24 W of rectified power improves the system drain efficiency by up to 8.1 points at -3.5 dB $P_{out,n}$, matching theory.

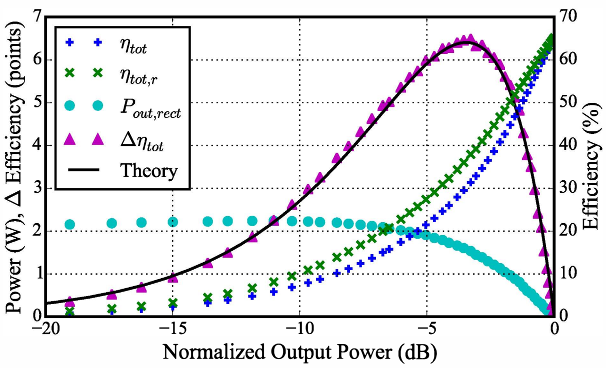

Fig. 10. Measured η_{tot}, $\eta_{tot,r}$, DC rectified power, $\Delta\eta_{tot,r}$, and theoretical $\Delta\eta_{tot,r}$ demonstrating efficiency improvement through power recycling as envelope amplitude is decreased. Up to 2.24 W of rectified power improves the system total efficiency by up to 6.5 points at -3.5 dB $P_{out,n}$, matching theory.

it cannot be measured, a rectification efficiency of 51 % is found to match theory to measurement. Based on our experience from [10], this rectification efficiency is valid given the reduced range of $|\Gamma|$ in this measurement. We expect that the rectification efficiency would improve to that of the internal PA drain efficiency ($> 70\,\%$) by increasing $|\Gamma|$ through active load-pull, or on-chip termination (Z_{gate}). In that case, the peak improvement in system drain and total efficiencies would be 12.9 % and 10.2 %, respectively.

VI. Conclusion

A GaN MMIC outphasing PA with effective power recycling has been demonstrated to operate at 10.35 GHz with a peak $\eta_{d,r}$ of 71.8 % and peak $\eta_{tot,r}$ of 65.2 % at an output power of 6 W. At -3.5 dB normalized output power, the system drain and total efficiencies are improved by 8.1 and 6.5 points, respectively. This design is one of three outphasing PAs with power recycling, and operates at the highest frequency, 10.35 GHz, among its peers through the use of a high-efficiency, self-synchronous transistor rectifier and GaN integration.

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