Multi-Level Chireix Outphasing GaN MMIC PA

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***Abstract*—This paper presents the design and performance of a 9.7 GHz GaN MMIC Chireix outphasing PA with discrete supply modulation. This architecture is referred to as Multi-Level Chireix Outphasing (ML-CO). The internal PAs include class-F harmonic terminations, while the Chireix combiner provides the fundamental frequency load modulation. A peak output power of 37 dBm (5 W) is achieved, while a peak η_{tot} of 60.2 % is reached at 35.7 dBm. The average total efficiency calculated for a 6 dB PAR QPSK signal is 48.1 %, a 15.5 point improvement over the constant supply case.**

***Index Terms*—outphasing, power amplifier, Chireix, MMIC.**

I. Introduction

Modern modulation schemes utilize signals with high peak-to-average power ratios (PAPR) to achieve spectral confinement and high data rates, challenging power amplifiers (PAs) to operate efficiently over a large output power range. The Multi-Level Chireix Outphasing (ML-CO) PA, shown in Fig. 1, offers a solution. As in Chireix outphasing [1], amplitude modulation is converted into additional differential phase modulation, enabling the two internal PAs in each branch to operate in saturation at peak efficiency. However, in ML-CO, the discrete supply modulator varies the amplitude of the internal PA vector outputs, A, which reduces the range of outphasing angle, θ, required for envelope reconstruction by the non-isolated (lossless) combiner. The internal PAs benefit from reduced DC power consumption with supply reduction.

The second peak efficiency improvement at low output power of lossless combining has not been realized in outphasing PAs at 5 GHz [2] or 10.1 GHz [3]. Nonetheless, lossless combining shows improvement over lossy combining [3]. At higher frequencies, the internal PAs are hindered by parasitics which rapidly degrade efficiency under reactive loading. This effect is mitigated in ML-CO, because the reduced outphasing angle range decreases the load modulation range, and thus the reactive loading.

In outphasing literature, discrete supply modulation has only been shown to improve the poor efficiency roll-off in LINC PAs (isolated combining). In Multi-Level LINC (ML-LINC), the supplies are varied symmetrically, which reduces power wasted in the isolated combiner [4]. In Asymmetric Multi-level Outphasing (AMO), the supplies are varied independently to achieve further efficiency improvement [5].

Multi-Level Chireix Outphasing, shown in Fig. 1, further improves the efficiency performance of Chireix outphasing with discrete supply modulation. At 9.7 GHz, a GaN MMIC prototype is shown to achieve a peak output power of 37 dBm with 51.6 % total efficiency, and an average total efficiency of 48.1 % for a 6 dB PAR QPSK signal.

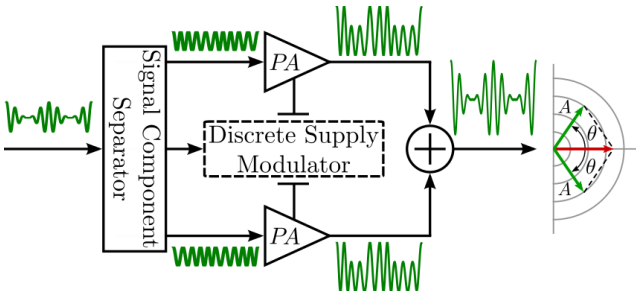

Fig. 1. Block diagram of Multi-Level Chireix Outphasing, showing the signal component separation, which must control the additional phase modulation (θ) as well as amplitude control via the discrete supply modulator. The combiner is a lossless, three-port network, often incorporating Chireix compensation.

II. MMIC Design

The MMIC is fabricated in Qorvo's 0.15 μm GaN process. From the layout in Fig. 2, the MMIC is 3.8 mm × 3.2 mm and utilizes a $10 \times 100\,\mu$m HEMT for each internal PA, while integrating the Chireix combiner.

A. Internal PAs

The internal PAs are designed to operate in Class-F with second (short) and third (open) harmonic terminations. To realize the fundamental and harmonic impedances at the intrinsic drain, the transistor parasitics must be de-embedded. In absence of a package, these parasitics are well approximated by the output capacitance, which is extracted from the nonlinear model at 10 MHz, using the method in [6]:

$$C_{gd} = -\frac{\mathrm{Im}(\mathrm{Y}_{12})}{2\pi f} \tag{1}$$

$$C_{ds} = \frac{\mathrm{Im}(\mathrm{Y}_{22})}{2\pi f} - C_{gd} \tag{2}$$

$$C_{gs} = \frac{|Y_{11} + Y_{12}|^2}{2\pi f \times \mathrm{Im}(\mathrm{Y}_{11} + \mathrm{Y}_{12})} \tag{3}$$

$$C_{out} = C_{ds} + C_{gd}||C_{gs} \tag{4}$$

At pinch-off ($I_{dq} = 3$ mA), the estimated output capacitance is 0.332 pF, which is absorbed into the output matching network to shift the design reference plane to the intrinsic drain. The third harmonic open is realized with a shunt resonant (at $3f_0$) stub, as shown in Fig. 2. Care must be taken to achieve the deepest resonance possible ($|S_{21}| = -33.8$ dB), while minimizing loss at the fundamental ($|S_{21}| = -0.24$ dB), which restricts realizable loads. The electrical length between the

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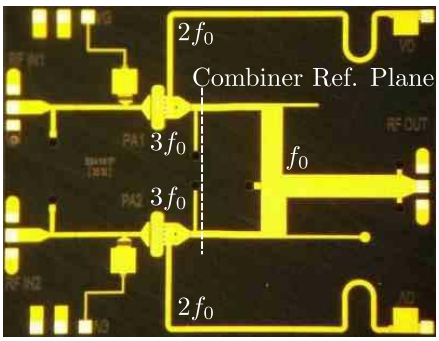

Fig. 2. Photograph of ML-CO GaN MMIC PA, showing harmonic terminations and combiner design reference plane. The internal PAs operate in Class-F, with the combiner providing all fundamental frequency matching. Overall size is 3.8 mm × 3.2 mm.

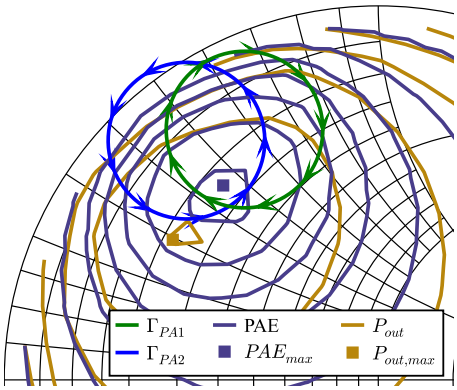

Fig. 3. Load modulation of each PA, Γ_{PA1} and Γ_{PA2}, overlaid on PAE and P_{out} load-pull contours, at combiner reference plane.

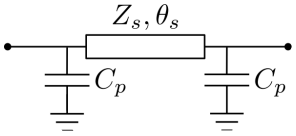

Fig. 4. Ideal TL-π equivalent network.

transistor and resonant stub must be carefully tuned to achieve the desired phase of the high $|\Gamma|$, $3f_0$ load at the intrinsic drain. The phase is sensitive due to the output capacitance, and highly dependent upon its estimation.

The second harmonic short is realized by the bias line in Fig. 2, where the shunt bypass capacitor provides RF-DC isolation by shorting the RF. In this design, the quarter-wavelength bias line transforms the capacitor short circuit to open, short, and open circuits at f_0, $2f_0$, and $3f_o$, respectively. Thus, it provides a low impedance at $2f_0$ (1.3Ω) without interfering with fundamental matching or the $3f_0$ termination. Typically, the highest harmonic termination is closest to the transistor, but the $2f_0$ short has the proper phase at the end of the bias line, so it is connected closest to the transistor.

Together, the harmonic terminations account for 0.075 dB of network power loss at the fundamental frequency, with loss defined as:

$$\text{Network Power Loss (dB)} = 10\log\left(\frac{|\mathrm{S}_{21}|^2}{1-|\mathrm{S}_{11}|^2}\right) \tag{5}$$

B. Combiner

To minimize loss, the combiner performs all fundamental matching directly, without matching to an intermediate impedance. Therefore, the internal PAs are characterized by load-pull simulation immediately after the harmonic terminations, labeled the combiner reference plane in Fig. 2. In Fig. 3, the desired f_0 load modulation, labeled Γ_{PA1} and Γ_{PA2}, is overlaid on the PAE and P_{out} load-pull contours. The load modulation intersects at an outphasing angle near the peak PAE impedance, then moves toward the edge of the Smith Chart while maintaining internal PA P_{out} balance along the inner trajectory. With the combiner, the total dissipative loss in the output matching network at f_0 increases to 0.32 dB. For this calculation, the PA ports are connected as a single port and the loss definition above is used.

An implementation issue arises from Chireix outphasing thoery, which assumes a differential load [1] that is not easily implemented at GHz frequencies in microstrip [7]. In [8], quarter-wave transformers are used to convert each voltage source (internal PA) to a current source, so that the two outputs can be summed using a common grounded load [7]. However, two quarter-wave transmission lines (TLs) are difficult to fit into the restricted area of a MMIC. To save space, TL equivalent circuits can be used. Unfortunately, these equivalences are only available for the 90°, 180°, and 270° TLs common to passive combining structures [9]. In [8], the TL transformers are 90° because the combiner is referenced to the intrinsic drain, but in our design the reference plane has shifted and the TLs are no longer 90°. Therefore, an equivalent circuit, shown in Fig. 4, is derived for a variable length TL. In this MMIC process, it is favorable to use a TL rather than an inductor in the π network to reduce loss.

First, the ABCD matrix of the TL-π network must be found by cascading the ABCD matrices of its three elements (C_p-TL-C_p) as follows:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \begin{bmatrix} \cos\theta_s & jZ_s\sin\theta_s \\ jY_s\sin\theta_s & \cos\theta_s \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C_p & 1 \end{bmatrix} \tag{6}$$

Leading to the follow ABCD parameters:

$$\begin{aligned} A &= \cos\theta_s - \omega Z_s C_p \sin\theta_s \\ B &= jZ_s \sin\theta_s \\ C &= j\left[2\omega C_p \cos\theta_s + \sin\theta_s\left(\frac{1}{Z_s} - \omega^2 C_p^2 Z_s\right)\right] \\ D &= \cos\theta_s - \omega Z_s C_p \sin\theta_s \end{aligned} \tag{7}$$

Equating Eqn. (7) to the ABCD matrix of a TL [10], two of the three unknown variables (C_p, θ_s, Z_s) can be found. In this case, θ_s is chosen at the onset, and the others are solved by:

$$C_p = \frac{1}{Z_0}\frac{\cos\theta_s - \cos\theta}{\omega\sin\theta} \tag{8}$$

$$Z_s = Z_0\frac{\sin\theta}{\sin\theta_s} \tag{9}$$

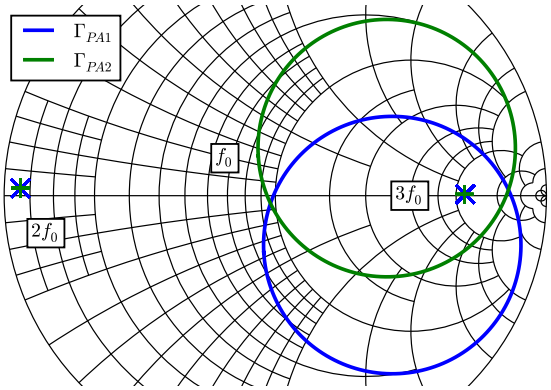

Fig. 5. Simulated load modulation at the intrinsic drain of each PA during outphasing. The high Q of the resonators used in the harmonic terminations keeps their impedances from changing even as the fundamental load modulates. The effectiveness of the $3f_0$ termination reduces as the fundamental load becomes larger than it with increasing outphasing angle.

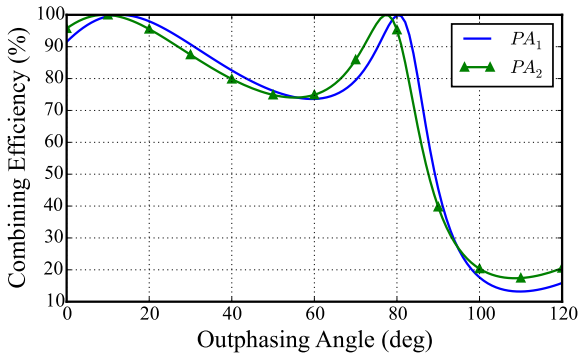

Fig. 6. Simulated combining efficiency of the microstrip combiner (referenced to the intrinsic drain) is maintained above 70 % over 85° of outphasing range.

Rather than using two TL transformers at the PA outputs, one can be used after the combining node. Using the TL-π equivalent circuit, the long TL is shrunk to fit on the MMIC. The shunt capacitors are visible in Fig. 2, and the one near the RF pads is split into two parallel capacitors for symmetry.

Fig. 5 shows the simulated load modulation at the intrinsic drain of each PA during outphasing, performed in NI/AWR MWO with a nonlinear model by Modelithics. The fidelity of the harmonic terminations is demonstrated in their immobility. Their effectiveness, though, is always relative to the fundamental impedance. As the f_0 impedance increases with outphasing angle, the effect of the $3f_0$ termination is decreased. The $2f_0$ terminations is always much lower than the f_0 loading, and thus provides a good short circuit.

Using the fundamental load modulation at the intrinsic drain, the combining efficiency or power factor can be calculated and is shown in Fig. 6. The system efficiency is the product of the combining and internal PA efficiencies. A second peak is created by the Chireix compensation at $\theta = 80°$. The difference between combining efficiencies for each internal PA is small, confirming that the designed load modulation in Fig. 3 maintains balanced output power.

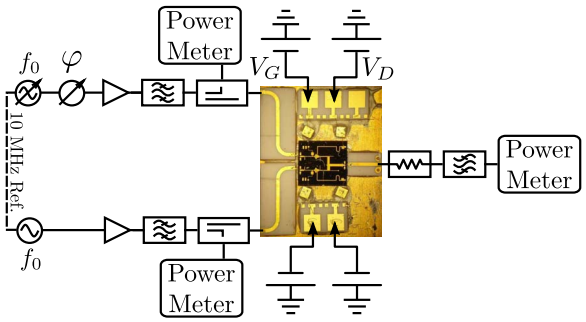

Fig. 7. ML-CO measurement setup. Separate sources drive each PA branch, while a phase shifter sweeps the differential phase. The source driving the phase shifter adjusts its amplitude to maintain constant available input power to within 0.1 dB.

III. Measurements

Each die is mounted on a 40 mil thick CuMo carrier plate, as seen in Fig. 7. The PA input and output RF pads are bonded, with two short bond wires, to 10 mil thick alumina lines, on which connectorized launchers are landed for testing. The calibration procedure de-embeds the launchers and alumina lines up to the bond wire/alumina interface. The DC pads are connected with a bondwire to off-chip AC de-coupling capacitors.

A. Setup

In the measurement setup in Fig. 7, a phase shifter sweeps the differential phase, φ, which is twice the outphasing angle, θ. The source amplitude on that branch is adjusted to compensate for the variable attenuation of the phase shifter. Constant available input power is maintained within 25.1 dBm $\pm$ 0.1 dB after calibration, whereby offsets are calculated for each phase shifter control voltage. The available input power of the second source is then calibrated to match that of the first, in order to maintain balance within $\pm$ 0.1 dB between the two inputs. The RF inputs and output are filtered and measured with a power meter. For each desired supply level, V_D, a CW differential phase sweep is performed. Note that the supply levels are varied statically, and the implementation of a discrete supply modulator is left for future work.

B. Results

Fig. 8 shows a compilation of phase sweeps for swept supply levels from 6 V to 20 V in 2 V increments at 9.7 GHz. We find the total efficiency η_{tot} definition applicable to outphasing PAs, since it takes the constant input power into account, but does not drop below zero when $P_{out} > P_{avail}$ as does the power-added efficiency (PAE).

$$\eta_{tot} = \frac{P_{out}}{P_{dc} + P_{avail}} \tag{10}$$

A peak output power of 37 dBm (5 W) is achieved, while a peak η_{tot} of 60.2 % is reached at 35.7 dBm. The optimal trajectory, which is chosen to maximize η_{tot}, remains within 10 points of its peak η_{tot} for 5.45 dB of output power range. Although only a CW characterization was performed on this

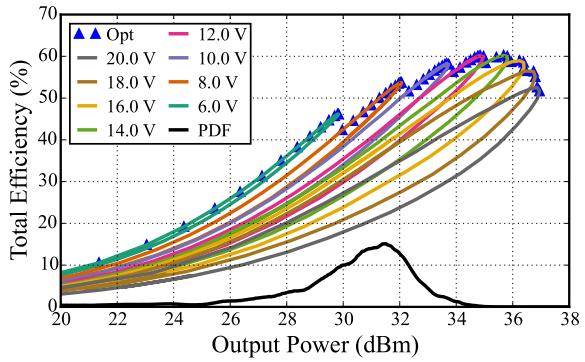

Fig. 8. Compilation of measured phase sweeps for swept supply levels from 6 V to 20 V in 2 V increments at 9.7 GHz. The optimal trajectory is selected to maximize η_{tot}. In black is the PDF of a 6 dB PAPR QPSK signal used to calculate average total efficiency.

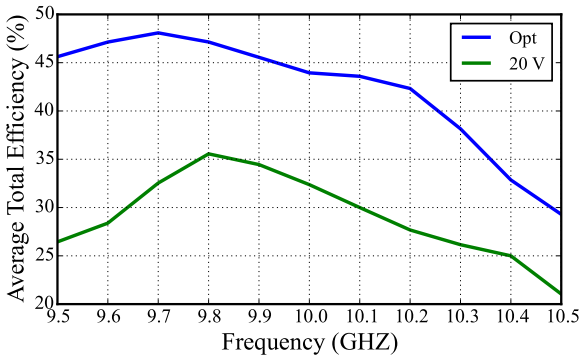

Fig. 9. Comparison of average total efficiency across frequency between the optimal trajectory and 20 V supply, showing improvements between 8 and 19 points. Optimal operation achieves 400 MHz of bandwdith with $\eta_{tot,avg} > 45\,\%$.

ML-CO MMIC PA, the average total efficiency ($\eta_{tot,avg}$) for a real signal is calculated in post-processing to provides valuable performance insight. The probability density function (PDF) of a QPSK signal with a 6 dB PAPR is shown in Fig. 8 and used as a weighting function to yield the average efficiency using the optimal trajectory. At 9.7 GHz, an average total efficiency of 48.1 % is achieved, which is 15.6 points higher than the average total efficiency for 20 V supply.

The average total efficiency for the defined QPSK signal is calculated across frequency, where the optimal trajectory is determined as described above for the same range of supply voltages. Fig. 9 compares $\eta_{tot,avg}$ for the optimal trajectory at each frequency as well as for only the 20 V supply. In the optimal case, $\eta_{tot,avg}$ is greater than 45 % for at least 400 MHz of bandwidth, from 9.5 GHz to 9.9 GHz. The improvement in efficiency of supply modulation over constant supply ranges from 8 to 19 points across the measured frequency range.

Finally, the average total efficiency at 9.7 GHz is calculated for restricted number of supply levels and shown in Table I. The 20 V level must be included in all cases to maintain the same peak power. For each number of supply levels, the optimal subset of the measured supplies is found for the QPSK signal used in this work. Even the addition of one supply level shows a significant improvement in average total efficiency, from 32.54 % to 44.3 %. The improvements diminish beyond the addition of a second supply level.

TABLE I
AVERAGE TOTAL EFFICIENCY WITH RESTRICTED SUPPLY LEVELS

# Levels	Supply Levels (V)	$\eta_{tot,avg}$ (%)
1	20	32.54
2	10, 20	44.3
3	8, 12, 20	45.88
4	8, 10, 12, 20	47.23
5	6, 8, 10, 12, 20	47.96
6	6, 8, 10, 12, 14, 20	48.07
7	6, 8, 10, 12, 14, 16, 20	48.09
8	6, 8, 10, 12, 14, 16, 18, 20	48.09

IV. Conclusion

For the first time in literature, a Multi-Level Chireix Outphasing PA is demonstrated. The X-band MMIC is shown to achieve state-of-the-art performance in terms of average total efficiency, 48.1 %, for high-PAR signals, 6 dB. The intricacies of the class-F PA and Chireix combiner designs are discussed. A comparison of performance variation with supply level restriction reveals the significant improvement with the addition of a second supply level, and the diminishing returns with further additions.

Acknowledgements

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