X-Band GaN Multi-Level Chireix Outphasing PA with a Discrete Supply Modulator MMIC

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***Abstract*—This paper presents the characterization of a multi-level Chireix outphasing PA with a GaN discrete supply modulator MMIC at 9.7 GHz. The internal PAs include class-F harmonic terminations, while the Chireix combiner determines the fundamental frequency load modulation. A power-DAC architecture provides 8 supply levels with 3 half-bridges, maintaining more than 85% efficiency. The combination of the two achieves a peak output power of 4.8 W, and average total efficiencies for a 6 dB PAR QPSK signal of 44.1% and 48.1% with and without considering the supply modulator consumption, respectively, demonstrating the feasibility of this PA architecture with a real discrete supply modulator.**

***Index Terms*—outphasing, discrete supply modulation, power amplifier, Chireix, MMIC.**

I. Introduction

Spectral mask requirements for both communication and radar systems has led to the development of signals with high peak-to-average power ratios (PAPR). Traditional and high efficiency power amplifier (PA) classes cannot operate efficiently over a wide output power range, significantly degrading the transmitter efficiency for such signals. Outphasing is a PA architecture developed for efficiently amplifying high PAPR signals [1]. In Chireix outphasing, a non-isolated combiner enables and dictates load modulation, maintaining high efficiency operation. In LINC outphasing, an isolated combiner preserves linear amplification at the cost of poor efficiency roll-off with output power.

Discrete supply modulation can improve the back-off efficiency of LINC PAs. In multi-level LINC (ML-LINC), the supplies are varied symmetrically, which reduces power wasted in the isolated combiner [2]. In asymmetric multilevel outphasing (AMO), the supplies are varied independently to achieve further efficiency improvement [3].

Chireix outphasing also benefits from discrete supply modulation, as demonstrated by the multi-level Chireix outphasing (ML-CO) architecture [4], shown in Fig. 1. In Chireix outphasing the amplitude modulation of the input signal is converted to additional differential phase modulation, which controls the load modulation at the output, thereby controlling the output amplitude. The combiner is designed to modulate the load in a high efficiency region, to maintain efficiency at low output powers. Discrete supply modulation provides an added benefit of reduced DC power consumption by the internal PAs. The addition of discrete supply modulation has been proven indispensible for high frequency outphasing PAs [5], where the peak in back-off efficiency has not been realized at 5 GHz [6] or 10.1 GHz [5].

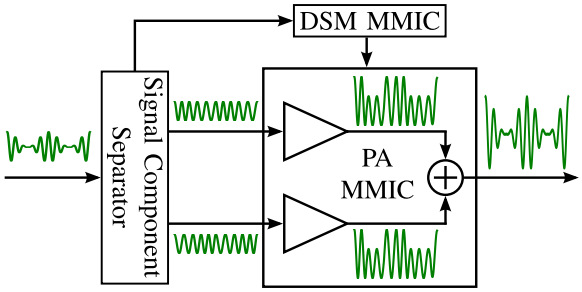

Fig. 1: Block diagram of multi-level Chireix outphasing and discrete supply modulator GaN MMICs. The signal component separator controls the additional phase and discrete supply modulation.

This work expands on the previous introduction of the ML-CO PA architecture, through the inclusion of a GaN discrete supply modulator (DSM) MMIC in measurement. At 9.7 GHz, the combination of the two achieves a peak output power of 4.8 W, and average total efficiencies for a 6 dB PAR QPSK signal of 44.1% and 48.1% with and without considering the supply modulator consumption, respectively. The practicality of this topology is substantiated by a reasonable efficiency degradation of 4 points with a MMIC supply modulator. This is the only case of supply modulated outphasing (ML-LINC, AMO, ML-CO) making use of a discrete supply modulator that is not a simple switch network.

II. PA and DSM MMICs

Both the PA and DSM are fabricated in Qorvo's 0.15 µm GaN process. The MMIC PA is from [4] and reviewed here for completeness. The chip is $3.8\times3.2\,\text{mm}^2$, as shown in Fig. 2. The internal PAs are designed to operate in class-F with second (short) and third (open) harmonic terminations. At the combiner reference plane, the internal PAs are characterized by load-pull simulation. The Chireix combiner performs all fundamental matching, and designates the desired load modulation for outphasing operation.

An implementation of a discrete supply modulator, referred to as a power-DAC in [7], is implemented in Qorvo's 0.15 µm GaN-on-SiC process. The power-DAC is based on a direct digital-to-analog conversion architecture, where the digital bits, b_i and $\overline{b_i}$, control the three half-bridges of the circuit, as shown in Fig. 3a. The three half-bridges are supplied with $N = 3$ isolated voltages, whose values are chosen to be binary scaled: $V_D/2$, $V_D/4$, and $V_D/8$. Since the voltage is modulated

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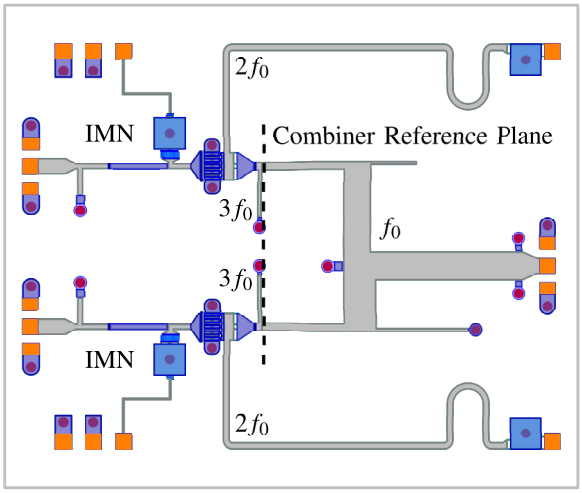


Fig. 2: Layout of ML-CO GaN MMIC PA, showing harmonic terminations and combiner design reference plane. The internal PAs operate in Class-F, with the combiner providing all fundamental frequency matching. Overall size is $3.8\times3.2\,\text{mm}^2$.

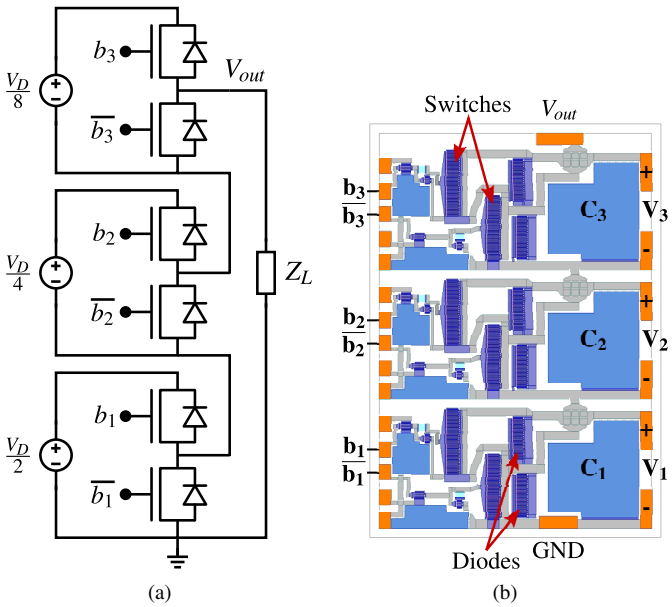


Fig. 3: (a) Circuit diagram of the power-DAC architecture. (b) Layout of the $3.8\times5.4\,\text{mm}^2$ GaN power-DAC MMIC.

from 5.5 V to 19.6 V in measurement, a voltage offset of 5.5 V is added in series. The power-DAC output voltage applied to the load is obtained by:

$$V_{out} = \sum_{i=1}^{3} b_i \frac{V_D}{2^i} + V_{offset} \tag{1}$$

thus behaving like a DAC circuit, where the output can deliver power to the load. In actuality, the load Z_L in the circuit diagram is the power amplifier.

The MMIC layout is shown in Fig. 3b, where the high-side and the low-side switches of each half-bridge employ large periphery pHEMT devices ($64\times150\,\mu\text{m}$) to reduce the conduction resistance, R_{on}. In parallel to these power switches, high-side and low-side diodes ($40\times125\,\mu\text{m}$) are used to maintain a current path when both switches are turned off (blanking time). The conduction resistance of the power switches has been accurately measured in DC regime to be $0.33\,\Omega$. In every control bit configuration, three switches are connected in series, so the total conduction resistance of the power-DAC is just below $1\,\Omega$. The isolated supply voltages of each half-bridge are bypassed with an on-chip MIM (Metal-Insulator-Metal) capacitor of 330 pF. In order to control each half-bridge of the power-DAC, The digital control signals, b_i and $\overline{b_i}$, are isolated, level-shifted and amplified by external isolators. Fig. 4 demonstrates the power-DAC MMIC output voltage approximating a 1 MHz sinusoid across a fixed, $33\,\Omega$ resistive load at a measured efficiency of 96.4%. The GaN-on-Si hybrid implementation in [7] demonstrated linearized tracking of vary fast signals, e.g. 10 MHz LTE.

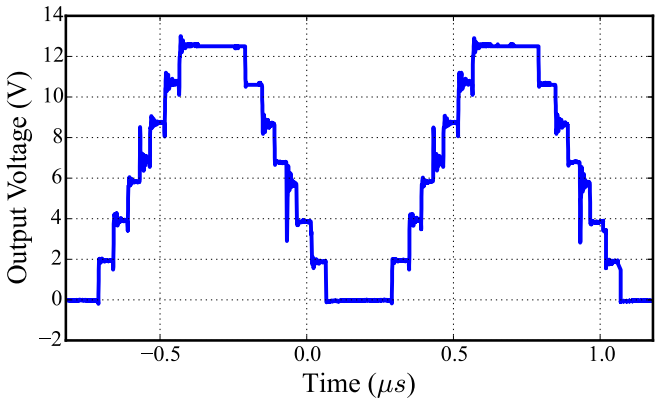


Fig. 4: GaN power-DAC MMIC output voltage approximate of 1 MHz sinusoid across a fixed resistive load.

III. Measurements

The ML-CO MMIC PA is mounted on a 40 mil thick CuMo carrier plate. The PA input and output RF pads are bonded, with two short bond wires, to 10 mil thick alumina lines, on which connectorized launchers are landed for testing. The calibration procedure de-embeds the launchers and alumina lines up to the bond wire/alumina interface. The DC pads are connected with a bondwire to off-chip AC de-coupling capacitors. The QFN packaged power-DAC MMIC is mounted on a test board to interface with the digital control signals and isolated supply voltages.

A. Setup

In the measurement setup in Fig. 5, a phase shifter sweeps the differential phase, φ, which is twice the outphasing angle, θ. The source amplitude on that branch is adjusted to compensate for the variable attenuation of the phase shifter. Constant available input power is maintained within 25.1 dBm $\pm$ 0.1 dB after calibration, whereby offsets are calculated for each phase shifter control voltage. The available input power of the second

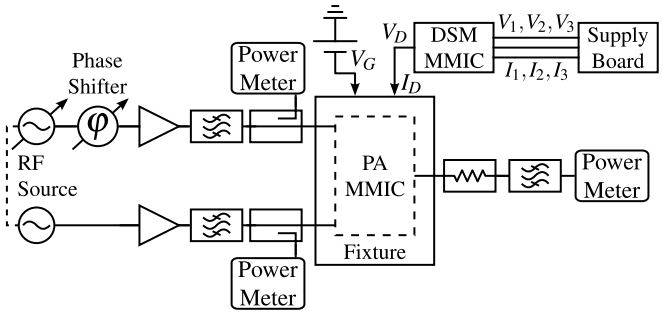


Fig. 5: ML-CO measurement setup. Separate sources drive each PA branch, while a phase shifter sweeps the differential phase. The source driving the phase shifter adjusts its amplitude to maintain constant available input power to within 0.1 dB.

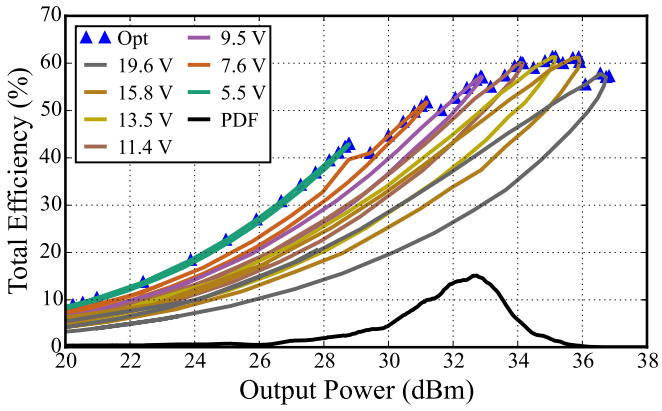
source is then calibrated to match that of the first, in order to maintain balance within $\pm$ 0.1 dB between the two inputs. The RF inputs and output are filtered and measured with a power meter. For each desired supply level, V_D, a CW differential phase sweep is performed. Since modulated measurements are not performed, the average total efficiency ($\eta_{tot,avg}$) for a modulated signal is calculated in post-processing to provide valuable performance insight. The probability density function (PDF) of a QPSK signal with a 6 dB PAR is shown in Fig. 6 and used as a weighting function to yield the average efficiency using the optimal trajectory.

The total DC input power for the power-DAC is measured at the three outputs of the supply board with an oscilloscope via current (I_1, I_2, I_3) and voltage (V_1, V_2, V_3) probes. The DC output power of the power-DAC is measured in a likewise manner along the wires interfaced to the MMIC PA. When a measurement accounts for the power-DAC consumption, the power-DAC input power is used as the DC power in the efficiency calculation, otherwise, the power-DAC output power is used as the DC power.

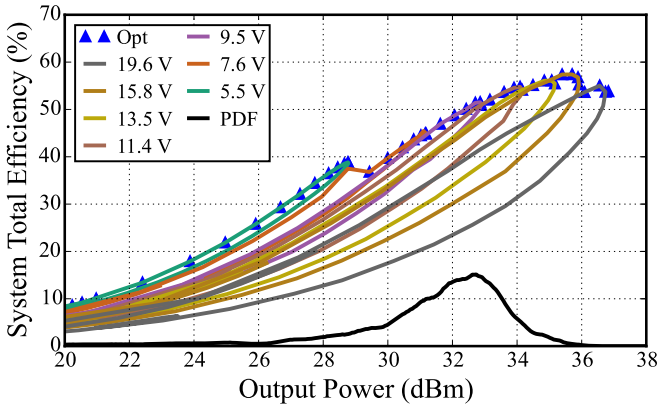
B. Results

Fig. 6 shows a compilation of phase sweeps for seven supply levels from the voltage offset in (1), 5.5 V, to 19.6 V at 9.7 GHz, with and without considering the power-DAC efficiency. At 19.6 V, a peak output power of 36.8 dBm or 4.8 W is achieved in both cases. When taking the consumption of the power-DAC into account, the peak total efficiency drops from 61.3% to 57.4%, and the average total efficiency for a 6 dB PAPR QPSK signal drops from 48.1% to 44.1%. Due to a small resistance in the power-DAC transistors, the supply voltage varies during the phase sweep, since the DC current is varying. The variation ranges from 0.48 V for the 5.5 V level to 1.3 V for the 19.6 V level, showing the variation increases with the supplied current. The supplies are labeled in Fig. 6 by the average voltage across the phase sweep.

The decrease in efficiency is evident in the comparison of the optimal trajectories in Fig. 7. The system efficiency decreases more at higher supply voltages, because the efficiency of the power-DAC holds more weight at the system level, since it is supplying significantly higher currents. At



(a)



(b)

Fig. 6: Compilation of measured phase sweeps for swept supply levels from 5.5 V to 19.6 V at 9.7 GHz (a) without and (b) with considering power-DAC dissipation. The optimal trajectory is selected to maximize η_{tot}. In black is the PDF of a 6 dB PAPR QPSK signal used to calculate average total efficiency.

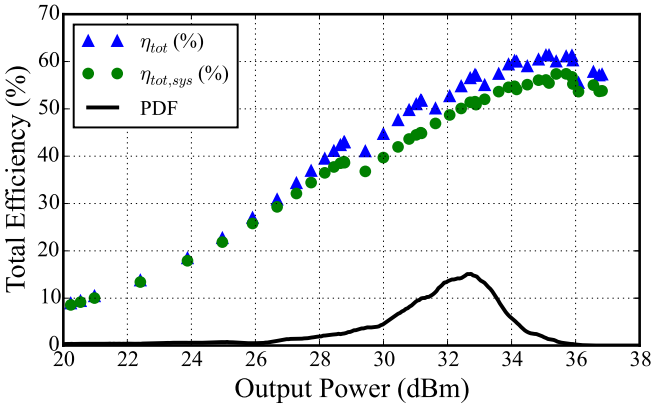


Fig. 7: Comparison of optimal trajectories with (η_{tot}) and without ($\eta_{tot,sys}$) accounting for power-DAC consumption.

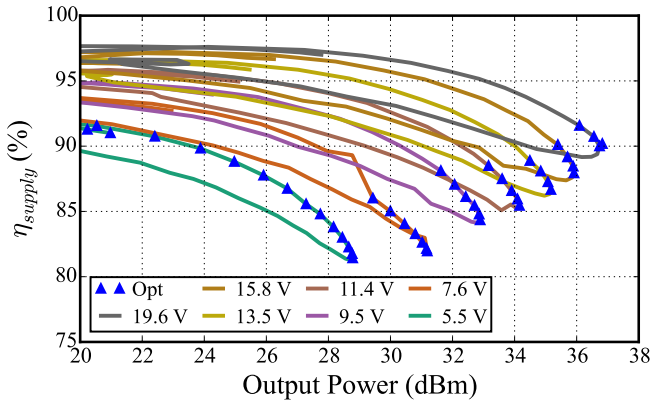


Fig. 8: Efficiency of the power-DAC, showing the operating points of the optimal trajectory.

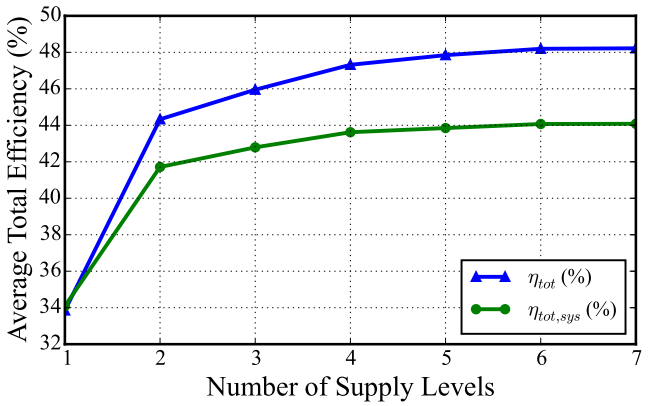


Fig. 9: Comparison of the average total efficiency for a 6 dB PAR QPSK signal with restricted supply levels, with (η_{tot}) and without ($\eta_{tot,sys}$) considering the power-DAC efficiency.

5.5 V, the power-DAC is supplying a maximum of 218 mA, while at 19.6 V, it is supplying 419 mA, corresponding to DC powers of 1.2 W and 8.2 W respectively. However, even when considering the consumption of the power-DAC, the average total efficiency for the 6 dB PAR signal only drops 4 points.

The efficiency of the power-DAC is shown in Fig. 8 for each supply level, and differential phase sweep, which varies the power-DAC load along with the PA output power. The operating points of the optimal trajectory are marked. The power-DAC operates more efficiently for higher voltage output, and less current (power). The curve for each level exhibits hysteresis caused by the load modulation in the ML-CO PA. Along the more efficient load trajectory, the internal PAs draw less current, thereby improving the power-DAC efficiency. As the output power decreases, the power-DAC current decreases, causing the voltage drop across its 1 Ω internal resistance to decrease, increasing the output voltage. Thus, at low output power, the power-DAC supplies the highest voltage for a given supply level and the lowest current, which allows it to operate most efficiently. Along the optimal trajectory the power-DAC operates between 81.5% and 91.5% efficiency.

The average total efficiency is calculated for restricted number of supply levels, as shown in Fig. 9, with and without consideration for the power-DAC consumption. The 19.6 V level is included in all cases to maintain the same peak output power. For each number of supply levels, the optimal subset of the measured supplies is found for the QPSK signal used in this work. In both cases, the diminishing returns are clearly visible, with the system efficiency (considering power-DAC dissipation) approaching 44.1%, 4 points lower than the previous measurements ignoring the efficiency of the discrete supply modulator.

Although these measurements do not prove the dynamic capabilities of amplifying a modulated signal with a ML-CO PA, they provide a more realistic, static characterization of expected performance. In order to amplify with acceptable linearity, nonlinearities caused by both the outphasing dynamics at RF as well as the transient response of the discrete supply modulator will need to be taken into account.

IV. Conclusion

A multi-level Chireix outphasing PA with a GaN discrete supply modulator MMIC is measured to demonstrate 44.1% average total efficiency for a 6 dB PAPR signal at 9.7 GHz with 4.8 W of peak output power. The feasibility of the ML-CO PA architecture is further substantiated by static measurements with a GaN power-DAC DSM.

Acknowledgements

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