Dynamic Dual-Gate Bias Modulation for Linearization of a High-Efficiency Multistage PA

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***Abstract*— This paper investigates the linearization of high-efficiency multistage PAs through gate bias modulation derived from the envelope of the RF input signal. We show that separate control of the driver- and power-stage gate bias voltages allows for independent linearization of gain and phase. An iterative algorithm determines signal-dependent gate voltage functions that minimize amplitude-to-amplitude (AM/AM) and amplitude-to-phase (AM/PM) distortion, and is demonstrated on a 10-W high-efficiency X-band GaN monolithic microwave integrated circuit (MMIC) PA with a custom-designed hybrid dual-gate bias modulator. The noise power ratio (NPR) of a 5-MHz-wide signal is improved by as much as 9.4 dB compared to the PA with a static bias, without degradation in power-added efficiency (PAE) and gain. The measured average PAE improves from 19.9 % at 9.8-dB backoff by 0.8 points, with a saturated gain increase of 0.2 dB at 9.7 GHz. A long-term evolution (LTE) signal with different envelope statistics and a 10.6-dB peak-to-average power ratio (PAPR) is amplified with an adjacent channel power ratio (ACPR) improvement of up to 7.9 dB.**

***Index Terms*— Broadband communication, efficiency, monolithic microwave integrated circuit (MMIC), nonlinear distortion, power amplifiers, predistortion.**

I. Introduction

THE challenge of achieving high efficiency and linearity of a PA for high-PAPR signals is usually addressed through load or supply modulation with additional digital predistortion (DPD) [1]. For increasingly high instantaneous bandwidth signals, and in cases where baseband (BB) knowledge is missing such as in the case of repeaters, DPD can become impractical. An alternative is analog predistortion [2], which requires additional control and RF hardware. Instead, the PA gate (or base) bias voltage can be used to alter the output amplitude and phase and can be used to improve the efficiency and linearity with minimal additional circuitry.

Dynamic gate biasing was initially proposed in [3] for linearization of a MESFET amplifier, and in [4] to improve the PAE. More recently, this concept was successfully demonstrated in [5]–[9] for single-stage PA linearization, and for two-stage PAs driven with identical gate voltages [10]. Dynamic gate bias was shown to improve supply-modulated amplifiers [11]–[14], and partially to mitigate load modulation effects [14]. For load-modulated PAs, dynamic gate bias can improve backoff efficiency in outphasing [15], and independent gate control was shown to improve the linearity and efficiency of a Doherty PA [16].

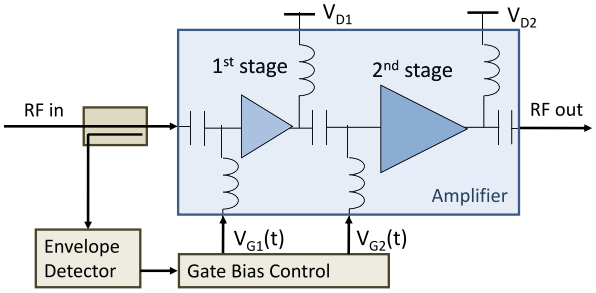

Fig. 1. Block diagram of two-stage dynamic gate bias derived from the envelope of the RF input signal for improving the linearity of a power amplifier. V_{G1} and V_{G2} are controlled independently for gain amplitude and phase linearization with minimal additional hardware.

In this paper, we use two independent time-varying gate bias functions to linearize a two-stage amplifier with minimal additional hardware. Since the dc gate currents are very small, fast (five to ten times the signal IQ bandwidth) dynamic bias modulators can consume low power, in contrast to supply modulators in envelope tracking (ET) PAs. The concept is not limited to two-stage amplifiers, but we show that two dynamic gate biases are sufficient for linearization. As depicted in Fig. 1, the envelope of a modulated input signal is used to derive gate voltages for the first (V_{G1}) and second stages (V_{G2}) of a multistage PA, resulting in two degrees of freedom which can simultaneously linearize amplitude and phase if memory effects are neglected [17], [18]. Memory effects [19], especially present in III–V semiconductor PAs [20]–[22], complicate linearization since the gate functions cannot be found from characterizing the PA at different gate voltages. This is true for both static continuous-wave (CW) and dynamic signal measurements, because the dynamic gate voltage trajectory itself causes memory and alters PA behavior. To determine the gate functions, we, therefore, iterate between PA measurements and gate function adaptation until AM/AM and AM/PM modulation is sufficiently reduced.

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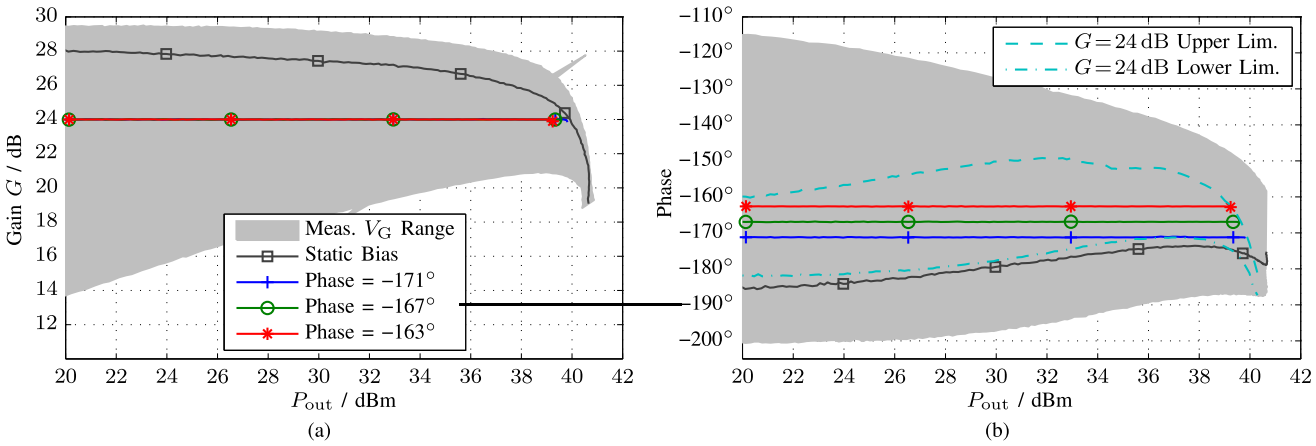


Fig. 2. (a) Static gain and (b) transfer phase characterization of a two-stage GaN MMIC PA. The gray area shows the obtainable gain (a) and phase (b) range when the gates are swept according to Table I. The dark solid line corresponds to the conventional static bias and the colored lines show the resulting gain and phase for three dynamic bias cases with 24 dB of gain. For the PAE of this PA measured for a similar gate range, see [17, Fig. 4].

In Section II, static characterization of the X-band 10-W GaN MMIC PA is presented to show the feasibility of amplitude and phase linearization and point to output power limitations. Dynamic measurements with a custom gate drive circuit, including calibration and equalization of the setup, are discussed in Section III. The gate function finding algorithm (GFFA) for the dynamic case is presented in Section IV and applied to find 25 different gate function pairs, corresponding to different target gain and output power levels. The corresponding linearity and efficiency are evaluated in Section V for two types of test signals, both with nominal bandwidths of 5 MHz: an NPR multicarrier signal and an LTE signal. The latter is used to evaluate improvements in normalized mean square error (NMSE) and ACPR.

II. Static Characterization

A two-stage X-band 10-W MMIC PA manufactured in Qorvo's GaN-on-SiC 150-nm process is used for all measurements presented in this paper. Peak efficiencies range between 47% and 55% [17], [23] at 9.7 GHz, depending on the chip. The die is mounted on a CuMo carrier and bonded to 50-Ω microstrip alumina lines. The drain pads are bonded to external pads through single-layer capacitors. The gate pads are directly bonded to external dc pads and connected to a dual gate drive printed circuit board (PCB). The reported efficiency numbers are referenced to the ends of the alumina lines. Due to strong memory effects, the required gate functions are found from dynamic measurements (Section IV), but initial static characterization shows trends important for linearization [17], [18]. The static bias parameters are given in Table I and the measured data at 9.8 GHz plotted in Fig. 2. The "Static Bias" trace shows the behavior of the PA for nominal, static bias. The initial gain at $P_{out} = 20$ dBm is 28.0 dB, and gradually drops to 23.7 dB as the PA is driven into compression at $P_{out} = 40$ dBm. In the same range, the transfer phase of the PA has an S shape, starting at −186°, peaking at $P_{out} = 37.8$ dBm with −174° and finally reaching −177° at 10-W output, with a total span of 10°.

TABLE I
Bias Parameters at $V_D = 20$ V

Values	V_{G1}, V	V_{G2}, V	I_{D1}, mA	I_{D2}, mA
min	-3	-3.05	1.1	2.3
max	-2.4	-2.45	101	454.9
nom	-2.64	-2.67	60	250

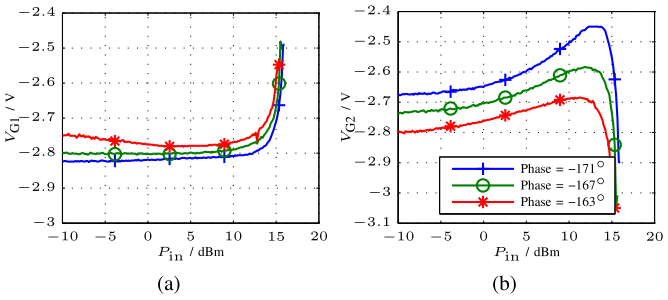


Fig. 3. (a) Gate 1 and (b) gate 2 tracking functions for the three flat amplitude and phase trajectories providing 24 dB of gain and the indicated phase value.

The gray-shaded area corresponds to the observed range in terms of PA transfer gain and phase, when independently varying the gate voltages. We see that at an output power of 20 dBm, the gain of the PA varies between 13.6 to 29.4 dB, and the phase can be varied in an 85° range. At $P_{out} = 40$ dBm, a gain range of 20.5–25.2 dB is available, and the phase range drops to 35°. However, not all combinations of gain and phase settings are possible. To illustrate this, the bounds of the phase range corresponding to gate settings producing 24 dB of gain are plotted as dashed lines in Fig. 2(b). The phase range that allows for flat gain and phase over the full measured amplitude range is examined for three cases shown by colored traces in Fig. 2(a) and (b), with nominal phases of −163°, −167°, and −171°. The required gate tracking functions for these cases are plotted in Fig. 3. From this example, we observe the following.

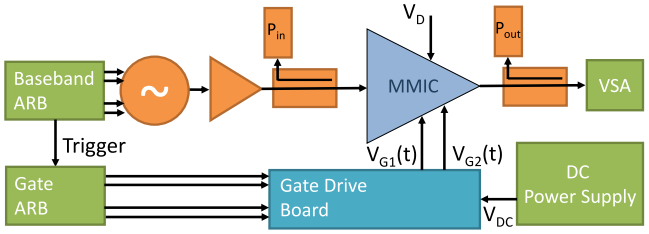


Fig. 4. Simplified block diagram of two-stage PA measurement setup with gate bias control for driver stage (V_{G1}) and final stage (V_{G2}).

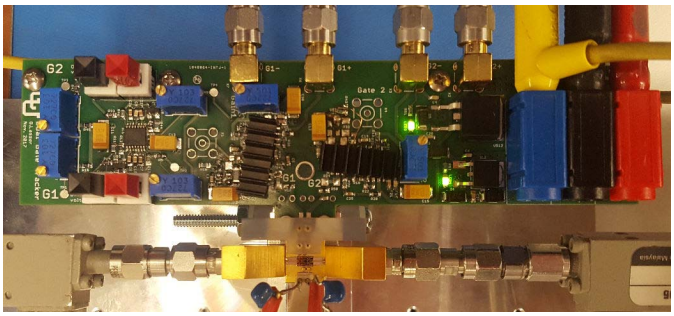


Fig. 5. MMIC amplifier in fixture (bottom center) with dual gate drive board above, drain connections at the bottom.

1) Two independently controllable gate voltages provide two degrees of freedom and enable linearization of amplitude and phase.
2) The output power range for complete linearization is limited.
3) For the same gain, different phase settings result in slightly different output power ranges and efficiencies.

To explain the last point, inspecting Fig. 3(b) shows that for different phase settings, similar but shifted gate 2 functions are required. This is true for gate 1 [Fig. 3(a)], but to a lesser degree. Since stage 2 uses larger transistors (3.6 mm for stage 2 versus 0.8 mm in stage 1), and the gate voltage difference is larger, the voltage shift in the gate 2 tracking functions dominates the total current consumption and thus efficiency. The −163° case, therefore, provides the best efficiency of the three investigated 24-dB cases, but a slightly smaller peak output power.

III. Dynamic Measurement Setup

The concept of dynamic gate tracking as shown in Fig. 1, in principle, does not require digital BB knowledge; however, a digitally controlled measurement system is beneficial for determining the gate tracking functions. A block diagram of the measurement setup is shown in Fig. 4, and a photograph of the gate drive board and the MMIC amplifier in its fixture is shown in Fig. 5. Two synchronized arbitrary waveform generators (ARBs) create the differential BB and drive signals, respectively. The BB is upconverted to X-band with a vector signal generator (VSG) and amplified, whereas the drive signals are inputs to a custom gate driver that generates time-varying gate bias voltages for the PA and in the current implementation consumes 2.7 W. Directional couplers are

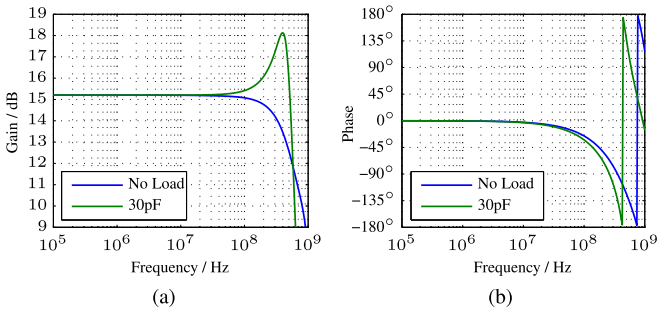


Fig. 6. (a) Simulated voltage gain and (b) phase of the gate drive board with and without an external 30-pF load.

used to measure the average input and output power to the MMIC PA, and the vector signal analyzer (VSA) measures spectrum and time-domain I/Q-data. The VSA is connected to the MMIC input through a coupler and switch (not shown in Fig. 4) to monitor the linearity of the drive signals.

The dynamic dual-gate bias circuit is implemented on a PCB with two amplifiers designed with TI THS3202 current feedback double op-amps, with the differential-to-single-ended conversion of the input signal with low susceptibility to common-mode distortions. The differential input signals are independently terminated in 50-Ω resistors, amplified by the first-stage THS3202 pair, and then level-shifted with an adjustable negative offset voltage. The second op-amp is not used in the output stage THS3202. A 5-Ω series stability resistor connects the output to the MMIC gate pads through an interconnect that consists of spring-loaded contacts and bond wires. The resistor also reduces the Q factor of the resonant circuit formed by the bond wire and on-chip bypass capacitor (approximately 30 pF). The simulated frequency response of the gate tracker is shown in Fig. 6. Up to 40 MHz, the frequency response is unaffected by the capacitive loading of the on-chip gate bypass capacitors. However, the phase response starts to deviate from 0° already at 10 MHz. To ensure a flat frequency response within the tracking bandwidth, the tracking signal is digitally equalized, as described in the following.

A. Measurement Calibration

Several levels of calibration and equalization are performed, and described in the following order: 1) RF amplitude calibration; 2) time alignment; and 3) gate drive amplitude calibration and interconnect equalization.

The RF signal path is calibrated with a CW signal by replacing the MMIC by the P_{out} power sensor. The input and output directional couplers are then directly connected with P_{out} power sensor at its normal location. By comparing the power levels in these two cases, the amplitude offsets for the power meters are found. The I/Q-data recorded by the VSA are calibrated in a postprocessing step. Its average power is normalized to the average power measured with the calibrated P_{out} power sensor. The gain calibration of the I/Q-data is essential for AM/AM linearization in the on-the-fly GFFA.

Time alignment ensures that the RF input signal and the bias signals align at the RF PA [1], [24]. In ET, it is done by

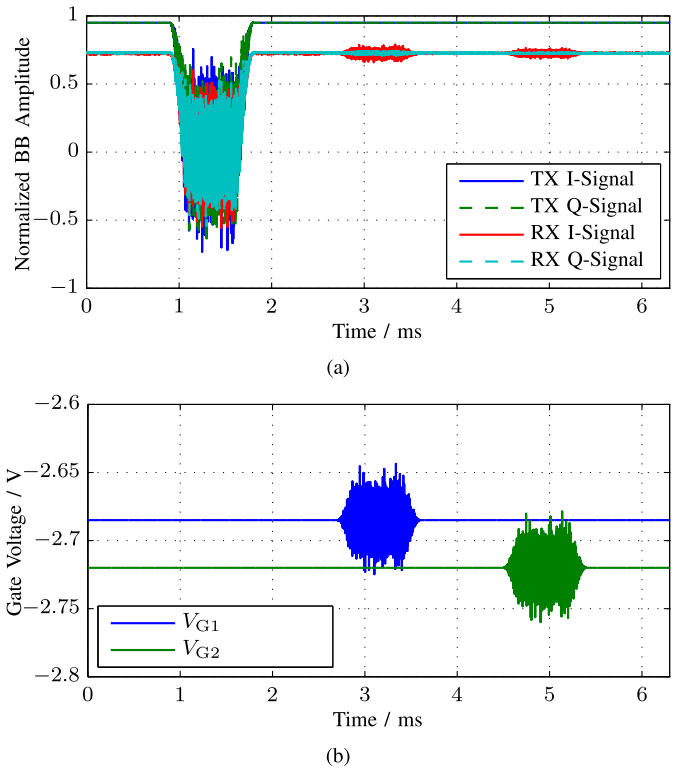


Fig. 7. Signals used for time alignment and gate equalization. (a) Transmitted (TX) and received (RX) BB I/Q-signals. (b) Transmitted gate signals.

optimizing linearity or efficiency [25]–[27], but this assumes a known tracking function, which is not the case in gate tracking. In addition, the two gate signals have different path delays, so the alignment of three signals is required. Instead, we observe the effect of a perturbation on the gate voltage as an amplitude modulation in the PA RF output signal and compare its temporal occurrence with a reference signal on the RF carrier. The signal bandwidths are chosen to fit within the 140-MHz bandwidth of the VSA. Therefore, the gate signal bandwidths may not exceed 70 MHz, since they will appear with twice the bandwidth at the RF signal. The temporally shifted pseudorandom test noise signals are shown in Fig. 7.

The 6.3-ms-long RF signal consists of an unmodulated carrier, augmented with a 900-μs-long noise signal created by applying a Tukey window [28, see (6.9)] with parameter $p = 0.5$ to a concatenated signal consisting of three copies of a 300-μs noise signal. The windowing creates smooth amplitude tapers at the beginning and end of the signal, reducing the bandwidth. The repetition allows cutting out a 300-μs portion of the composite signal in postprocessing, resulting in a circularly shifted version of the original signal. This is beneficial for time alignment and frequency-domain processing, as explained below. To obtain smooth transitions between the CW and noise signal parts of the test signal, Fig. 7(a) from 0.9 to 1.8 ms, the CW signal is windowed by 1 minus the Tukey window, and the two signals are added.

The gate signals shown in Fig. 7(b) consist of identical copies of a 65-MHz-wide noise signal, created in the same way as the RF signal, and unmodulated dc voltages chosen to create standard biasing conditions of the PA. For this bias setting of approximately 75 mA/mm, the transconductance of the transistors rises with increased gate voltages. The modulation on the gate signals is separated by 900 μs and both signals are shifted by the same amount from the RF modulation pulse. The gate modulation amplitude is kept small to maintain approximately linear bias dependence of the PA transconductance, creating an amplitude modulation of the unmodulated carrier sections of the RF output signals, as seen in the received (RX) I-signal in Fig. 7(a). The received signals are time- and phase-aligned to the RF modulation pulse using cross correlation in postprocessing. The modulation from V_{G1} in the in-phase component of the received signal at around 3 ms is larger in amplitude than the modulation from V_{G2} seen around 5 ms due to the gain of the second stage of the PA. The time delay introduced by the different paths is found by cross correlating the received in-phase signal with the corresponding gate signal so that the two paths are synchronized up to a single clock cycle of the ARBs (800 ps).

Finally, the last calibration step addresses the gate drive amplitude, enabling direct mapping between the gate ARB settings and the gate voltages applied to the PA. The gate ARBs are consecutively loaded with two static signals: the first one corresponding to the maximum, the second one to the minimum ARB output. The corresponding gate voltages are measured and used to compute the offset and slope of the linear relation between the ARB setting and the gate voltage.

The gain and phase response of the gate drive boards are well behaved up to 10 MHz; however, the theoretical bandwidth of the gate tracking signal, as derived from the RF signal envelope, is infinite. In addition, the interconnect between the gate drive PCB and the MMIC PA affects the frequency response of the tracking signal. To mitigate this, we apply a zero-forcing equalizer [29, p. 220] to the gate signal prior to loading it to the ARB. The equalizer is found from the same measurement used for time alignment. The original 300-μs-long centerpiece of the noise signal is cut out of the in-phase received signal, and processed in the frequency domain. Since the signal was transmitted repeatedly, applying the cyclic Fourier transform does not introduce any extra distortions, and the equalizer is directly found in the frequency domain by comparing to the original noise signal applied on the gate. This results in flat frequency response at the PA transistor gate from dc to 65 MHz.

IV. Gate Function Finding Algorithm

The gate function performs the mapping from an RF input amplitude to a gate voltage. To allow arbitrary shapes with smooth transitions and no overshoots, the gate signal is created by piecewise cubic Hermite interpolation [30] between $N = 12$ nodes, linearly spaced in amplitude. The GFFA finds the two sets of 12 gate voltages of both gates, for a given average RF input power $\overline{P_{\text{in}}}$ and a given target gain G_{T}. The static parameters of the GFFA are summarized in Table II. Throughout this paper, N refers to the number of amplitude nodes, M to the number of trendline amplitude bins, and n and m are the corresponding indices. The mapping between amplitude node and trendline bin indices is $m = n(k+1)-k$, which results in k extra trendline bins for every center node

TABLE II
STATIC PARAMETERS OF THE GFFA

Parameter	Symbol	Value
Amplitude nodes	N	12
Extra trendline bins/node	k	2
Trendline amplitdue bins	M	34
Initial Phase Gate range		0.85
V_{G1} variations	I	7
V_{G2} variations	J	7
Treshold Gain Dev.	ΔG_T	0.5 dB
Transition node range	r	3
APO max step number	S_{max}	30
APO abort value	C_a	1×10^{-4}

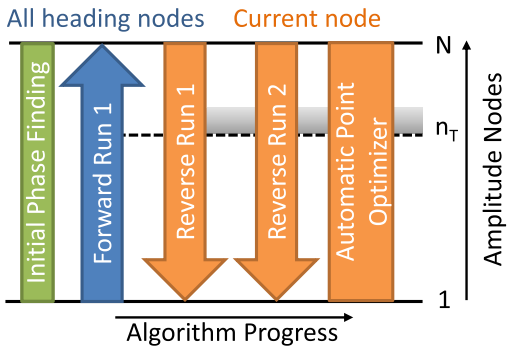


Fig. 8. Graphic representation of dynamic GFFA. Blue runs operate on all trailing nodes, orange runs operate only on the currently select node. The gray shaded area corresponds to the soft-switching range where the algorithm switches between pure phase trend optimization, and compromise phase and amplitude optimization below the threshold amplitude step n_T.

$(2 \leq n \leq N-1)$. The node which is currently optimized is called n_c and the corresponding amplitude trendline bin m_c. The gates 1 and 2 variation counts are called I and J, respectively, the corresponding indices are i and j.

Fig. 8 shows a graphic representation of the GFFA. As the algorithm progresses, it operates on the full input amplitude range to find the N coefficients for each gate function. It is structured in an initial phase finding section, a forward progressing optimizer (F1), two reverse progressing optimizers (R1 and R2), and a final automatic point optimizer (APO). Although the F1 optimizer will affect the complete remaining set of nodes that lie ahead of current node n_c in every step, the R1, R2, and APO optimizers only operate on the current node. This GaN PA shows strong memory effects, and changing any node of a gate function will have an effect on the whole amplitude and phase response. For this reason, several linear runs that step from node to node are required before the APO is used to fine-tune the gate functions.

All phases of the GFFA use the same training signal, repeated several times to form individual test segments, while slightly different gate functions are used for each segment. Under this excitation, the output signal of the PA is captured with the VSA in the time domain, the received signal is split into individual test segments and is used to create AM/AM and AM/PM trendlines using $M = N(k+1) - k$ amplitude bins. The trendlines are compared to the target gain and the target phase at the current optimization step, and the gates 1 and 2 voltage nodes corresponding to the test segment with the best match in gain and phase is selected. The algorithm-dependent parameters used in this implementation are found in Table III.

TABLE III
ALGORITHM-DEPENDENT GFFA PARAMETERS

Parameter	F1	R1	R2	APO
V_{G1} Search Window	0.2 V	0.2 V	0.1 V	dyn.
V_{G2} Search Window	0.25 V	0.25 V	0.15 V	dyn
$V_{G1,2}$ max	−2.5 V	−2.4 V	−2.4 V	−2.4 V
$V_{G1,2}$ min	−3.2 V	−3.25 V	−3.25 V	−3.25 V
Gain/phase weighting α_1	5	10	10	10
Gain/phase comp. w. α_2	1×10^3	1×10^3	1×10^4	1×10^5

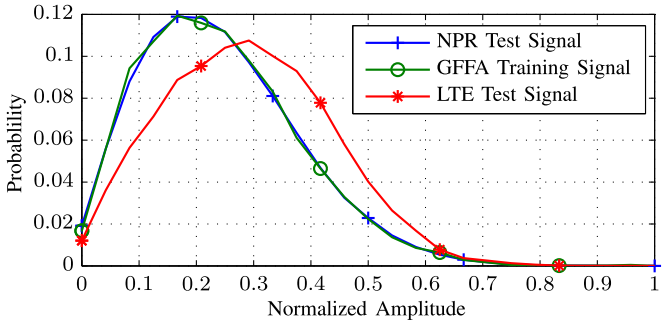


Fig. 9. Estimated pdfs of the training signal used in the GFFA and for the linearity testing signals reported in Section V.

A. Training Signal

The training signal used throughout the GFFA needs to be short enough so that several repetitions can be captured in the VSA memory, but also needs to have a comparable PAPR and amplitude statistics to the signals of interest. Although our NPR test signal used for the measurements in Section V-A consists of 30 001 carriers, we now only use 601 carriers spaced across the same 5-MHz bandwidth. Like the NPR test signal, it is constructed in the frequency domain by creating carriers with equal amplitudes, but unlike the NPR test signal, we limit the phase range of the uniformly distributed, random phases, which influences the PAPR of the signal. Since a signal with a low carrier number does not necessarily have the right amplitude statistics [31], we randomly create 7000 training signals, varying the phase range between 1.7π and 2π, and then pick the signal for which the estimated amplitude power density function (pdf) and the NPR test signal pdf are closest in a root-mean-square (rms) sense. The estimated pdfs for those test signals and the LTE signal used in Section V-B are shown in Fig. 9.

B. Initial Phase Finding

The static measurements presented in Section II already show the importance of the target phase, which affects the total linearization range and efficiency. For each selected target gain and average input power, the GFFA, therefore, starts with a short routine to find a good target phase. The PA is excited with the training signal, and the gate voltages are independently set to seven different variations spanning 85% of the F1 voltage range for V_{G1} and V_{G2} indicated in Table III, resulting in a total of 49 data sets retrieved in a single

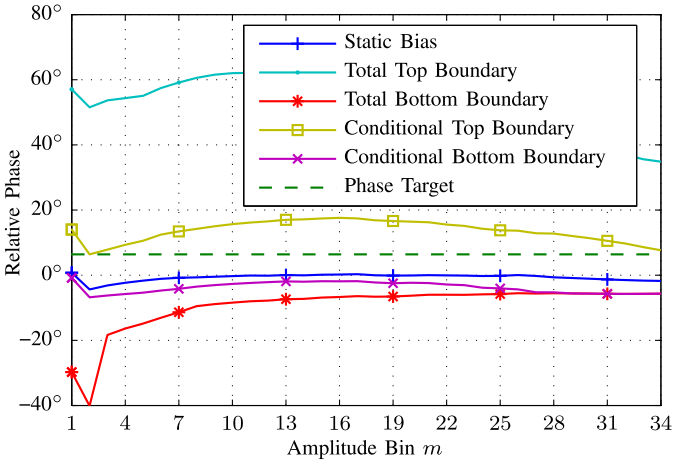


Fig. 10. Initial phase finding results for a target gain of $G_T = 24$ dB at $P_{in} = 6$ dB. The labeled amplitude bins correspond to the $N = 12$ nodes of the gate functions.

measurement. The output of the PA is captured as I/Q-data using the VSA and postprocessed to align the signal with a reference section with nominal bias, detailed in the next section. Results of this measurement are split up according to the $IJ = 49$ gate settings and corresponding phase responses corresponding to $M = 34$ amplitude bins are found. Fig. 10 shows the results after classification, including the static bias reference case. The available total phase range is indicated by its top and bottom boundaries. Finally, the phases that allow for a target gain of $G_T = 24\,\text{dB} \pm 1\,\text{dB}$ are indicated by two lines bounding this conditional phase range. The phase target is picked as the highest value within this range that can be kept constant through all amplitude bins, as this corresponds to the maximum efficiency setting for this PA as found in Section II.

C. Linear Runs

The single forward (F1) and the two reverse runs (R1 and R2) form the core of the GFFA. No assumptions on the shapes of the gate functions are made, and F1 starts with a flat gate function set to the gate voltages most closely fitting the gain and phase target values at minimum input amplitude, as found in Section IV-B.

1) F1: Starting at $n = 2$, the F1 optimizer will step through all amplitude nodes and on-the-fly create the first gate-tracking functions by finding a gate voltage for each node. In this work, the GFFA was set to evaluate $I = J = 7$ gate settings for both gates at each step (see Table II), corresponding to 49 test segments. For illustration purposes, the F1 test signals used at node $n_c = 4$ are shown in Fig. 11 for only three gate variations, resulting in a total of nine test segments, labeled 1–9. While Fig. 11 (top) shows the used RF signal envelope, which is composed of identical repetitions of the same training signal as described in Section IV-A, the gate signals shown in Fig. 11 (bottom) are different, following the gate functions shown in Fig. 12. The gate functions up to amplitude node $n = 3$ are identical, and then branch out to span the search windows as given in Table III. The search range for V_{G2} is chosen to be larger, since its impact on gain is smaller. The gate variation numbers I, J should be odd, so that the middle trace corresponds to an unaltered tracking function. While creating the gate test signal, the maximum and minimum gate voltage limits indicated in Table III are observed; the search range is moved up or down to prevent the gate drive to exceed the limits given for each GFFA section.

The total test signal shown in Fig. 11 contains extra sections required for synchronization. First, the signal starts with a ramp-up (RU) section, where the gate voltage is kept at the nominal bias and the training signal is slowly ramped-up to nominal amplitude using a raised cosine function. Similarly, the signal ends with a ramp-down (RD) section using the flipped raised cosine amplitude taper. This amplitude tapering allows synchronization of the signal obtained from the VSA. For phase synchronization, the "S" section with the nominal static bias is used; since this signal is preceded with two sections of static bias (the previous "RD" and the "RU"), it serves well as a phase reference, as it is relatively independent of long-term memory effects in the PA due to gate drive and average output power. To avoid false readings in section 1 due to memory from the previous, differently biased static section, a dummy section "D" with dynamic bias is inserted before section 1, which is discarded in postprocessing. The gate function used here is the unaltered gate function without applying any variations, corresponding to the middle gate functions shown in Fig. 12.

The results for F1 at step $n_c = 5$ using 49 gate variations and an average input power of 10 dBm is shown in Fig. 13. The data are processed in $M = 34$ amplitude bins, and the average value for each bin is shown. The vertical dashed line at $m_c = 13$ corresponds to node $n_c = 5$. To find the best gate voltage for that node, all dynamic traces are analyzed at $m_c = 13$ and one extra neighboring amplitude bin, since $k = 2$ (see Table II). This is done by minimizing the following cost function

$$C_{i,j}(m_c) = \left(\frac{1}{k+1} \sum_{m=m_c-\frac{k}{2}}^{m_c+\frac{k}{2}} \left| \frac{G_{i,j}(m)}{G_T} - 1 \right| \right)^2 + \alpha(m_c) \left(\frac{1}{k+1} \sum_{m=m_c-\frac{k}{2}}^{m_c+\frac{k}{2}} \left| \frac{\varphi_{i,j}(m) - \varphi_T}{\pi} \right| \right)^2 \quad (1)$$

where $G_{i,j}$ and $\varphi_{i,j}$ are the gain and phase traces for the gate function indices i, j; and G_T and φ_T are the target gain and target phase values. In the F1 run, the initial weighting parameter $\alpha = \alpha_1 = 5$, putting a relatively strong emphasis on gain. As seen in Table III, this parameter is later increased to 10, as long as no compression is detected, i.e., $n_c < n_T$. The indices i, j corresponding to the smallest cost function are picked, indicated by the "Compromise traces" in Fig. 13. It is clear that the cost function finds a compromise between amplitude and phase, since the "best trace" is different in the two plots. Note that the trendline traces for amplitude bins $1 \leq m \leq 10$ are close to the target value, but do not match perfectly. This is due to the altered PA memory state, illustrating the need for several runs before the GFFA converges.

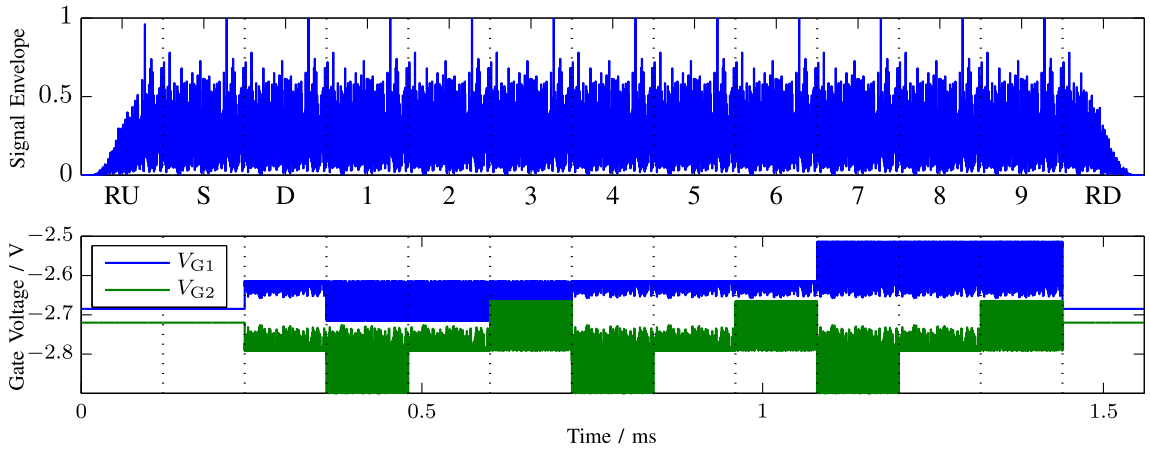


Fig. 11. Signal envelope and gate voltages for a dynamic optimization step. Three levels are tested at both gates, resulting in nine test segments (1–9). In addition, RU and RD phases, a static phase (S, used for phase synchronization), and a dummy phase (D, data is discarded, allows for thermal equalization) are transmitted in each step.

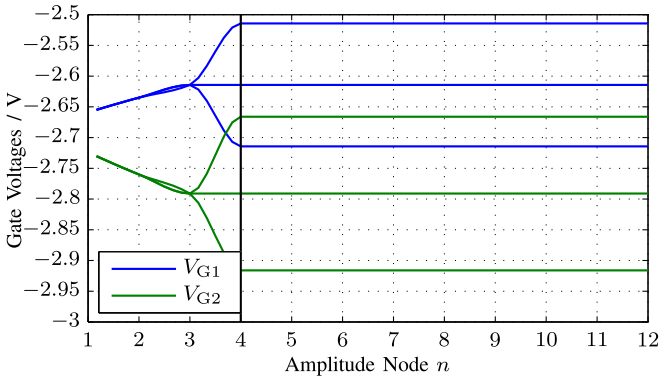


Fig. 12. Gate trajectory corresponding to the optimization signals plotted in Fig. 11 for a F1 at step $n_c = 4$ testing three levels at both gates.

2) Weighting Threshold Handling: When the PA is driven hard into compression, the effect of the gate voltages on the gain diminishes. This effect is even more pronounced for dynamic signals and is not accurately predicted by the measurements reported in Section II. In a high-amplitude regime where the total linearization fails, we, therefore, change the weighting parameter α to α_2, to put most emphasis in (1) on the phase. The node number n_T where this happens is found in the F1 algorithm. For every node, the F1 algorithm checks if for any combination i, j

$$\frac{G_T}{G_{i,j}(m_c)} < \Delta G_T. \tag{2}$$

In case there is no trace that reaches the target gain minus the allowed deviation ΔG_T, the current node is declared as threshold node n_T and subsequent iterations of F1 will pick α_2 as weighting parameter. However, if in a later step n_c a combination of i, j fulfills 2, the threshold node n_T is moved to this step.

3) Reverse Runs: The algorithm for the reverse runs R1 and R2 is identical, and only the gain/phase weighting in compression (α_2) is changed. They start at the end node $n = 12$ corresponding to the highest input amplitude, and work backward to $n = 1$, using the same cost function (1) as the F1 optimizer. The weighting function is picked as follows:

$$\alpha = \begin{cases} \alpha_1, & \text{for } n_c \le n_T \\ \alpha_2, & \text{for } n_c > n_T + r \\ \frac{n_c(\alpha_2-\alpha_1)}{r+1} + d, & \text{else. } d = \alpha_1 - \frac{n_T(\alpha_2-\alpha_1)}{r+1} \end{cases} \tag{3}$$

which allows a smooth transition from the two weights within the transition range r.

Since the reverse runs traverse all the way to $n = 1$, the amplitude bin $m = 1$ is evaluated. However, the measurement data in this lowest amplitude bin is highly affected by noise, and so this bin is omitted. For $n_c = 1$, the sums in (1), therefore, degenerates to picking bin $m = 2$ only.

D. Automatic Point Optimizer

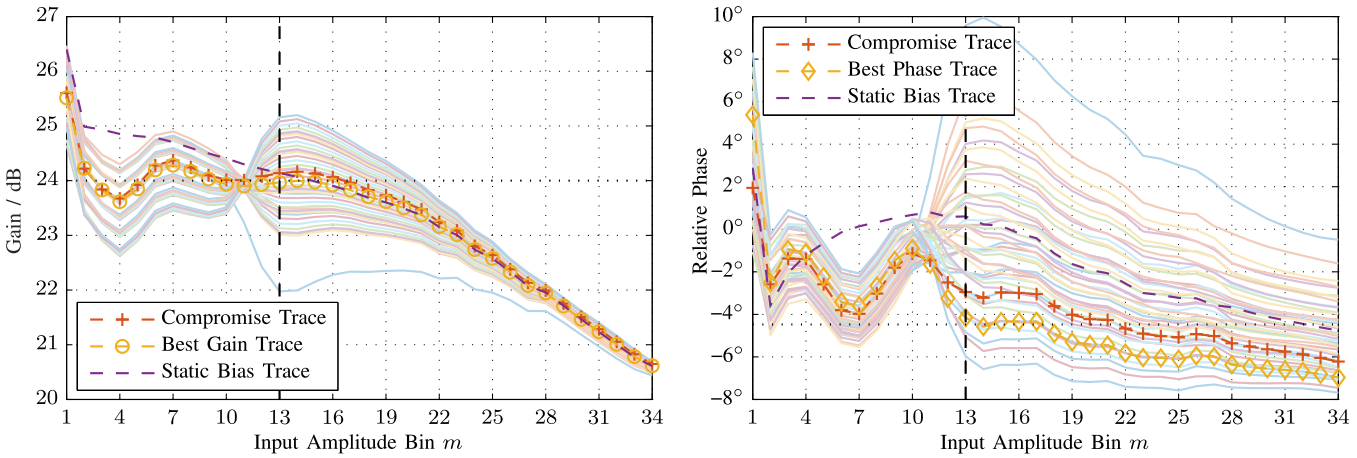
The last step of the GFFA starts at $n = 1$, using the same cost function (1) and the same weighting function (3) as the reverse optimizers. However, after the compromise gate function indices i and j are found, the next node for optimization is selected by calculating the APO cost function for all m

$$C_{APOi,j}(m) = \beta(m) \left| \frac{G_{i,j}(m)}{G_T} - 1 \right|^2 + \alpha_1 \left| \frac{\varphi_{i,j}(m) - \varphi_T}{\pi} \right|^2 \tag{4}$$

where the parameter β is selected as

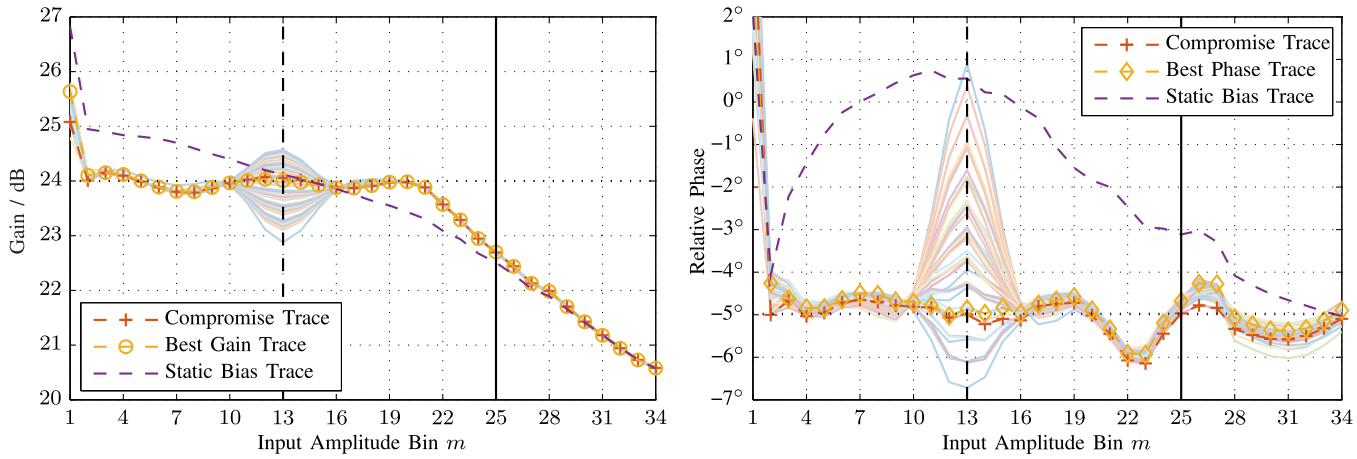
$$\beta = \begin{cases} 1, & \text{for } m_c < m_T \\ 0, & \text{for } m_c \ge m_T \end{cases} \tag{5}$$

and the node n corresponding to the m found to give the largest C_{APO} is picked. The value of $\max(C_{APO})$ is stored for later use. The APO then checks if the new node is identical to the old one, and when this is the case if the tested gate swing was large enough to bring at least one trace above and one trace below the target gain and phase value. (The test for gain is omitted for $n_c \ge n_T$.) If any of those criterions is not met, the APO assumes that the gate swing was too small and increases the V_{G1} search range to 35% and the V_{G2} search range to 50% of the maximum allowed range. If in the next iteration the step size is still insufficient, the gate swing is increased to 44% and 63% for gates 1 and 2, respectively.



(a) (b)

Fig. 13. (a) Gain and (b) relative phase trend plots for F1 of the GFFA at $\overline{P_{\text{in}}} = 10$ dB and node $n_{\text{c}} = 5$ corresponding to amplitude bin $m_{\text{c}} = 13$, as indicated by the vertical dashed line. The target gain is $G_{\text{T}} = 24$ dB, the relative target phase is φ_{T}=-4.5°, both targets indicated with a horizontal pointed line.



(a) (b)

Fig. 14. (a) Gain and (b) relative phase trend plots for APO of the GFFA at $\overline{P_{\text{in}}} = 6$ dBm and node $n_{\text{c}} = 5$ corresponding to amplitude bin 13, as indicated by the vertical, dashed line. The threshold node for gain/phase and pure phase optimization lays at $n_{\text{T}} = 9 \Leftrightarrow m_{\text{T}} = 25$, indicated by a solid, black, vertical line. The target gain is $G_{\text{T}} = 24$ dB, the relative target phase is $\varphi_{\text{T}} = -5°$, both targets indicated with a horizontal pointed line.

Similarly, if the same point is repeated, but gain and phase traces can be found on above and below the target value, the APO assumes that the search range was too coarse, and it is reduced. If a node is repeated more than 5 times, it is added to a blacklist and not considered for future optimization.

This procedure continues until either abort criterion $\max(C_{\text{APO}i,j}) < C_{\text{a}}$ is met or the maximum step number $S_{\max} = 30$ is reached. The first case means that the gain and phase trendlines are sufficiently close to the target values and no further optimization is required. In the second case, the stored vector of $\max(C_{\text{APO}})$ is investigated for the smallest value, corresponding to the best overall performance during the APO. The gate functions corresponding to this step are then restored.

Gate and phase trend plots for an intermittent step of the APO are shown in Fig. 14. When compared to the previous trend plots shown in Fig. 13 which are for the exact same input drive conditions, we see that the gain is now mostly flat up to amplitude bin 24, exceeding the gain of the static case from bin 17 to 26. The past trends shown in Fig. 14(b) also lie very close to the target phase, except for some deviation around bin 22, which is probably tackled next by the APO. At the current optimization node $n_{\text{c}} = 5 \Leftrightarrow m_{\text{c}} = 13$ both gain and phase traces fall below and above the target, so in case of an immediate repetition, the gate search range would not be increased.

V. Measurement Results

The GFFA is applied using target gains G_{T} ranging from 21 to 26 dB, and average, target output powers of $\overline{P_{\text{out,T}}} = \{26, 28, 30, 32, 34\}$dBm. The input powers for the GFFA are set according to $\overline{P_{\text{in}}} = \overline{P_{\text{out,T}}} - G_{\text{T}}$. This range is chosen since the PA has a nominal peak output power of 40 dBm and the test signals have a PAPR of approximately 10 dB. The low target output powers should allow for total linearity (gain and phase), while the higher output powers demonstrate

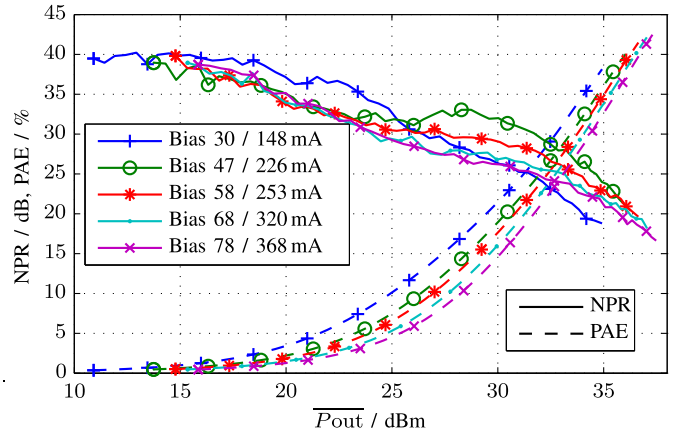


Fig. 15. PA characterization for different static quiescent currents using the NPR test signal. first number is the stage 1 quiescent current, the second number the second stage. The "58/253mA" trace corresponds to nominal bias and is used for comparison with dynamic gate bias cases.

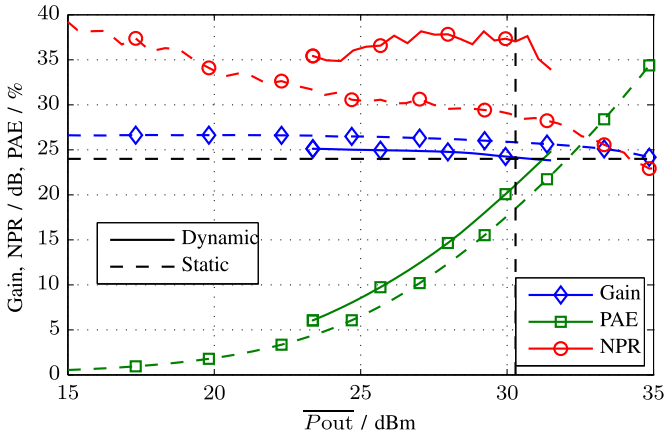


Fig. 16. Measured NPR, Gain, and PAE for static, nominal bias, and dynamic gate bias according to the tracking function shown in Fig. 17(a). GFFA settings were $G_{\mathrm{T}} = 24$ dB and $\overline{P_{\mathrm{out,T}}} = 30$ dBm, also indicated by the dashed horizontal and vertical lines.

the effect of the adaptive weighting of the cost function (1), and the threshold handling as described in Section IV-C2, providing higher efficiencies. The linearized PA is tested with two signals: an NPR test signal and an LTE uplink signal, both with a nominal bandwidth of 5 MHz. The gate tracking functions found by the GFFA remain constant for both modes; we expect better performance with the NPR test signal since the training signal was optimized to fit the NPR signal's amplitude pdf (see Fig. 9).

A. NPR Test Signal

The test signal is a 30 001 carrier, 5-MHz-wide pseudonoise signal with a 1% notch at the center, and a PAPR of 10.6 dB. For comparison, the PA is first characterized with fixed bias (see Fig. 15). We note that the lower bias settings show some improvement in NPR and PAE, at the cost of gain, which at backoff is {22.9, 25.7, 26.6, 27.2, 27.7} dB (not shown for clarity of plot). In the region of interest around $\overline{P_{\mathrm{out}}} = 30$ dBm, the "47 / 226 mA" bias case performs up to 3.5 dB better than the nominal quiescent "58/253 mA" case. All dynamic gate bias cases will be compared with the nominal bias case.

To illustrate the improvement in linearity, we pick the GFFA settings of $G_{\mathrm{T}} = 24$ dB and $\overline{P_{\mathrm{out,T}}} = 30$ dBm, and show a comparison in NPR, gain and PAE in Fig. 16. The dynamic gate bias case is measured for an input power range from $\overline{P_{\mathrm{in}}} = -2$ dBm to $\overline{P_{\mathrm{in}}} = \overline{P_{\mathrm{in,T}}} + 1.5$ dB. The output power corresponding to $\overline{P_{\mathrm{out}}} = \overline{P_{\mathrm{in}}} + G$ is indicated by the vertical dashed line in Fig. 16 and slightly exceeds 30 dBm since the gain at this point is slightly higher than the target gain G_{T}, indicated by the horizontal dashed line. For all measured power levels, the NPR and PAE of the dynamically gate-biased PA are improved over any static bias case. The peak NPR improvement versus the nominal bias is $\Delta NPR_{\max} = 9.1$ dB, at an average output power of $\overline{P_{\mathrm{out,N}}} = 30.7$ dBm, reaching an NPR of $NPR_{\max} = 37.6$ dB at this point. These data are also found in Table IV. Two values of PAE improvement are given; the direct improvement for the same output power is denoted as ΔPAE, which is 2.6 percentage points in this case.

TABLE IV
NPR MEASUREMENT RESULTS

$\overline{P_{\mathrm{out,T}}}$	$NPR_{\max}$	$\Delta NPR_{\max}$	$\overline{P_{\mathrm{out,N}}}$	ΔPAE	$\Delta PAE_{\mathrm{NPR}}$
		$G_{\mathrm{T}} = 26$ dB			
26 dBm	36.5 dB	6.1 dB	26.8 dBm	0.8 pp	9.5 pp
28 dBm	38.0 dB	8.5 dB	29.0 dBm	1.2 pp	15.3 pp
30 dBm	**37.9 dB**	9.4 dB	30.7 dBm	0.8 pp	19.7 pp
32 dBm	32.5 dB	6.1 dB	32.7 dBm	–0.5 pp	22.7 pp
34 dBm	30.8 dB	4.9 dB	33.1 dBm	–1.0 pp	20.7 pp
		$G_{\mathrm{T}} = 25$ dB			
26 dBm	**38.5 dB**	8.1 dB	25.9 dBm	2.0 pp	9.4 pp
28 dBm	38.2 dB	8.6 dB	27.9 dBm	2.1 pp	13.6 pp
30 dBm	37.0 dB	8.5 dB	30.5 dBm	2.0 pp	20.0 pp
32 dBm	**35.5 dB**	8.9 dB	32.5 dBm	–1.1 pp	22.8 pp
34 dBm	29.2 dB	5.2 dB	34.2 dBm	–1.9 pp	12.5 pp
		$G_{\mathrm{T}} = 24$ dB			
26 dBm	37.6 dB	7.5 dB	26.2 dBm	2.5 pp	10.3 pp
28 dBm	**38.4 dB**	8.8 dB	28.8 dBm	2.9 pp	16.7 pp
30 dBm	37.6 dB	9.1 dB	30.7 dBm	2.6 pp	21.5 pp
32 dBm	33.8 dB	7.3 dB	32.6 dBm	–0.2 pp	23.7 pp
34 dBm	28.7 dB	5.0 dB	34.3 dBm	–1.6 pp	11.8 pp
		$G_{\mathrm{T}} = 23$ dB			
26 dBm	37.9 dB	7.8 dB	26.4 dBm	3.3 pp	11.4 pp
28 dBm	37.8 dB	8.2 dB	28.8 dBm	3.3 pp	16.8 pp
30 dBm	36.2 dB	7.7 dB	30.5 dBm	3.0 pp	20.9 pp
32 dBm	34.1 dB	6.7 dB	32.2 dBm	–1.0 pp	21.6 pp
34 dBm	**33.4 dB**	8.2 dB	33.6 dBm	–1.0 pp	25.9 pp
		$G_{\mathrm{T}} = 21$ dB			
26 dBm	37.2 dB	7.0 dB	26.2 dBm	**4.2 pp**	11.9 pp
28 dBm	36.6 dB	7.0 dB	28.5 dBm	**4.2 pp**	16.7 pp
30 dBm	35.6 dB	7.1 dB	30.5 dBm	**3.2 pp**	20.8 pp
32 dBm	32.4 dB	6.2 dB	33.0 dBm	–1.1 pp	22.5 pp
34 dBm	32.8 dB	7.7 dB	33.7 dBm	–0.6 pp	26.5 pp

The second value, PAE_{NPR}, corresponds to the improvement in PAE when the same NPR value is considered. This corresponds to tracing back the output power level in Fig. 16 for the static bias case to a value that corresponds to an NPR of 37.6 dB or more, and results in a PAE degradation of the static bias case of 21.5 points.

For the same case ($G_{\mathrm{T}} = 24$ dB and $\overline{P_{\mathrm{out,T}}} = 30$ dBm), Fig. 17(a) shows the gate functions, AM/AM (b), and AM/PM (c) plots. Note that the gate-tracking functions are now plotted

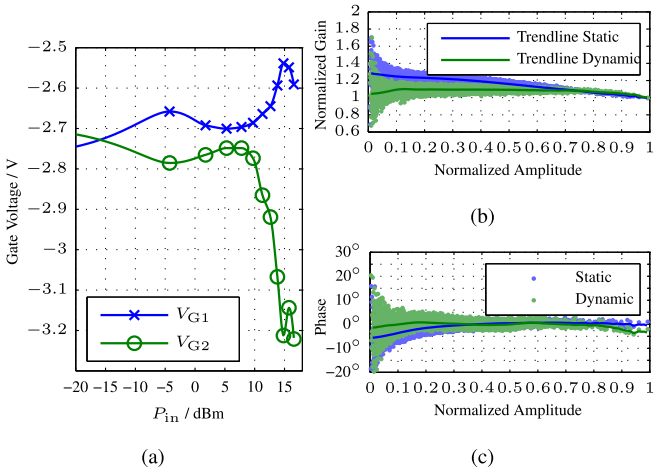


Fig. 17. Gate tracking functions (a), AM/AM (b), and AM/PM (c) measurements for $G_{\text{T}} = 24$ dB and $\overline{P_{\text{out}}} = \overline{P_{\text{out,T}}} = 30$ dBm. The markers in (a) are plotted at the positions of the voltage nodes that define the gate functions, node 1 is at $P_{\text{in}} = -\infty$dBm and not visible.

for the input power in dBm, compressing the equally linear spaced nodes toward the highest input power level, indicated by the markers. The improvement in linearity is also visible in the AM/AM and AM/PM characteristics, especially in the dynamic AM/AM trendline [Fig. 17(b)].

The analysis of NPR and PAE improvements for all measured cases is summarized in Table IV. The linearity improvement ΔNPR_{max} is the peak improvement found within a 1-dB window around the target output power. The NPR value NPR_{max} and the output power $\overline{P_{\text{out,N}}}$ at this point are also reported. The largest NPR value for each target output power is printed in boldface. We note that a target gain $G_{\text{T}} = 25$ dB corresponding to a 1.6-dB reduction in backoff-gain to the conventionally biased amplifier shows excellent performance in terms of NPR improvement (see Fig. 18). Only for the highest tested target output power $\overline{P_{\text{out,T}}} = 34$ dBm, the performance at $G_{\text{T}} = 25$ dB is not optimal and a lower target gain of 23 dB offers a clear advantage. Target gains below 23 dB do not further improve NPR, but provide a higher improvement in PAE when compared to the conventionally biased amplifier, as shown in Table IV.

B. LTE Test Signal

The test signal is an LTE uplink reference channel signal following the A5-4 option [32, annex A] [25 resource blocks, 64-quadratic-amplitude modulation (QAM) modulation, code rate $R = 5/6$], with a payload of purely "1" bits. The nominal bandwidth is 5 MHz, but due to the guard bands, the actual bandwidth of the signal is 4.5 MHz. It is created using the MATLAB LTE toolbox and results in a PAPR of 9.7 dB. Although the PAPR is similar to the NPR and training signals, its amplitude statistic is different, as shown in Fig. 9. We perform tests with this signal to show the robustness of the gate tracking functions found in the GFFA; for best linearization results, the GFFA should be rerun using a different training signal optimized to match this signal in amplitude statistics.

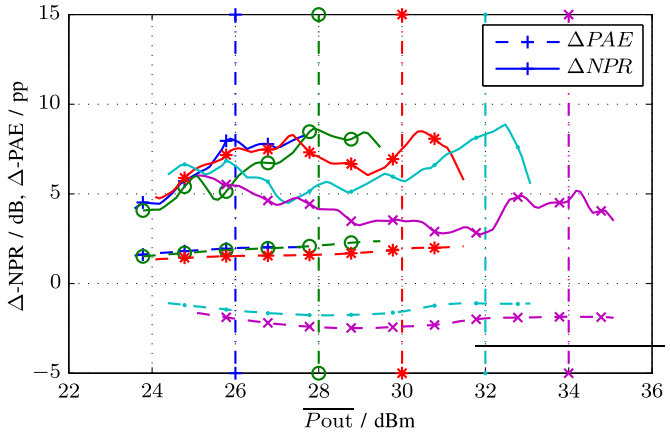


Fig. 18. Improvement in NPR and PAE for dynamic gate bias compared to the nominal bias, for $G_{\text{T}} = 25$ dB and five different target output powers as indicated by the vertical chain dotted lines.

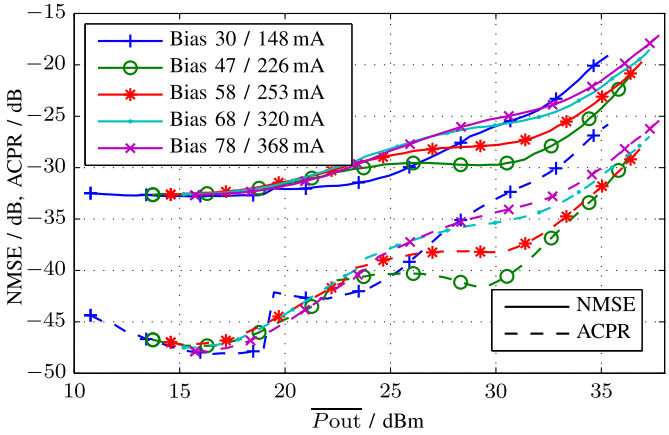


Fig. 19. PA characterization for different static quiescent currents using the LTE test signal. The "58/253mA" trace corresponds to nominal bias and is used for comparison with dynamic gate bias cases. The plotted ACPR is the worst case (maximum) between the left and right channel ACPR.

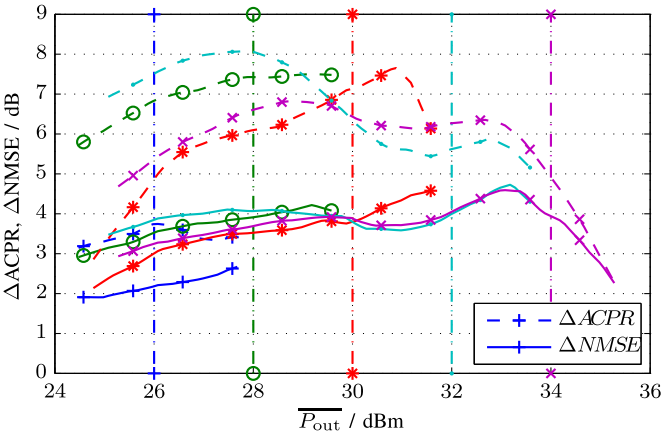


Fig. 20. Improvement in NMSE and ACPR for dynamic gate bias compared to the nominal bias, for $G_{\text{T}} = 26$ dB and five different target output powers as indicated by the vertical chain dotted lines.

The results of a characterization of the PA in terms of NMSE and ACPR using five static bias settings are shown in Fig. 19. To compute the NMSE, the received signal and the

TABLE V
LTE MEASUREMENT RESULTS FOR $G_T = 26$ dB

$\overline{P_{out,T}}$	$\Delta NMSE_{max}$	$\overline{P_{out,L}}$	ΔPAE	ΔPAE_{NMSE}	$\Delta ACPR_{max}$
26 dBm	2.7 dB	27.7 dBm	0.7 pp	9.2 pp	3.7 dB
28 dBm	4.2 dB	29.2 dBm	0.9 pp	14.5 pp	7.5 dB
30 dBm	4.6 dB	31.6 dBm	0.5 pp	20.8 pp	7.7 dB
32 dBm	4.7 dB	33.2 dBm	−0.8 pp	23.5 pp	6.2 dB
34 dBm	4.6 dB	33.1 dBm	−1.2 pp	22.8 pp	6.4 dB

initial transmit signals are first normalized to their average power, before computing the mean square error and normalizing it to the input power of the received signal. The ACPR reported here is the worst case value between the ACPRs of the lower and upper channels. Similar to the NPR results, the nominal bias is the second most linear case at $\overline{P_{out}} = 30$ dBm, only outperformed by the "47/226 mA" case.

The dynamic gate bias is evaluated for the same GFFA settings (and corresponding gate functions), and the improvements in NMSE are analyzed similar to the NPR data, and the case of $G_T = 26$ dB is given in Table V. The peak improvement in NMSE is represented in the second column, where we now allow for a ± 2 dB window around the target output power in the search. Columns 3 and 4 show the output power $\overline{P_{out,L}}$ and PAE improvement ΔPAE, corresponding to the point of maximum NMSE improvement $\Delta NMSE_{max}$. Analogous to the NPR case, the improvement in PAE when compared to the backoff amplifier achieving the same NMSE is reported by ΔPAE_{NMSE}. Finally, the maximum achieved ACPR improvement, again in a ± 2 dB window, is reported in the last column, $\Delta ACPR_{max}$. The improvements in NMSE and ACPR are plotted in Fig. 20 for a target gain of 26 dB. The ACPR curve corresponding to a target output power of $\overline{P_{out,T}} = 34$ dBm shows a local maxima at 32.7 dBm of 6.4 dB, which is the value reported in Table V. The global maximum at 28.9 dBm is ignored because it lays outside the ± 2 dB window around 34 dBm. Also, note that the global peak in NMSE improvement is close to the local peak found for ACPR and the lower output powers do not improve the NMSE.

In conclusion, the linearity improvement gained by gate-tracking functions found for a signal with similar PAPR but different amplitude statistics gracefully degrades for the LTE signal. The power of peak improvement in linearity parameters shifts from the target output power and the obtained improvements in NMSE and ACPR are not very large but still in many cases exceed the ones obtainable for static bias cases (Fig. 19).

VI. CONCLUSION

Dual-stage power amplifiers have two gate bias voltages that, when driven independently, separately allow for gain and phase alterations of the amplified output signal. The two gate controls differently affect amplitude and phase and thereby, for the memory-free case, allow for perfect linearization of a PA, up to some output power limit. The required gate functions can easily be found from static measurements. For PAs with memory effects, such as the investigated GaN X-band MMIC, a direct application of the gate functions found from those measurements fails with modulated signals, since memory effects alter the dynamic AM/AM and AM/PM characteristics of the PA. Furthermore, the dynamic gate signals itself causes memory states that affect the PA behavior compared to dynamic measurements with static gate bias. An on-the-fly GFFA is shown to be an efficient iterative method to achieve flat AM/AM and AM/PM trendlines, thereby linearizing the PA.

Although this method cannot linearize for memory-related nonlinearities (AM/AM and AM/PM spreading), it allows for flattening of the AM/AM and AM/PM curves on average. NPR improvements of up to 9.4 dB are obtained without gain reduction and a slight improvement of PAE. For the same output power, a reduction in target gain yields relatively constant NPR improvements, but a greater increase in PAE. Compared to static bias, an effective PAE improvement of up to 26.5% points for the same NPR value was observed. Using the same gate functions, the PA is also tested with an LTE signal with different amplitude statistics. Although not optimized for this case, NMSE improvements of up to 4.7 dB and ACPR reductions of up to 7.9 dB were observed with almost no change in efficiency.

The presented analog linearization is well suited for applications lacking digital BB knowledge, e.g., in repeaters. Compared to DPD, this approach does not require digital to analog converters since the linearization is based only on the instantaneous input envelope. In addition, for dynamic gate supply designs with sufficient bandwidth, and PAs with wideband gate bias circuits, there is no fundamental limit in the achievable signal bandwidth and the practical limit depends only on the circuit technology. The implementation of the dynamic bias control presented in this paper is based on laboratory equipment, so a fair comparison to a conventional DPD in terms of power consumption is not possible at this stage of the research. Since dynamic dual-gate bias demands driving the gate capacitances of the PA field effect transistors, larger devices and higher bandwidths would require higher drive currents and would, therefore, result in higher overall power consumption of the gate driving circuitry. A quantitative analysis of the power consumption of dynamic dual-gate biasing with respect to the signal bandwidth remains an open question that should be addressed in the future.

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