Gate Control of a Two-Stage GaN MMIC Amplifier for Amplitude and Phase Linearization

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***Abstract*—In this paper we study static and dynamic gate biasing of a two-stage X-band MMIC GaN PA. The PA is first characterized under different bias conditions using large-signal static measurements, and the determined conditions are then applied to dynamic measurements with a 20 MHz noise power ratio (NPR) test signal. Biasing the gates of the two stages independently allows simultaneous reduction of amplitude and phase distortion. AM/AM, AM/PM and PAE measurements are obtained for three different static scenarios. Consistent results from static and dynamic tests are obtained showing NPR values exceeding 31 dB. Adding predistortion alters the efficiency of the investigated static biases by more than 4 % points.**

***Index Terms*—Power amplifiers, MMICs, efficiency, nonlinear distortion, broadband communication, predistortion.**

I. Introduction

The ultimate goal in RF amplifier design is to combine linearity with efficiency for high-bandwidth high peak-to-average power ratio (PAPR) signals. As already discussed in [1], [2], modulating the drain and gate bias can improve both linearity and efficiency. In [3], gate bias is used to linearize a S-band class-B 10 W GaN single-stage amplifier by dynamically increasing the bias for low input powers. While the direct influence of the gate bias on efficiency is rather small, the amplitude and phase responses are greatly affected [4], [5].

When dynamically varying the gate bias (or drain supply), the dependence of V_{G} (or V_{D}) on input/output power is referred to as a trajectory. Modulating the gate bias of a single stage as in [2]–[6], or using two stages but driving them in parallel as in [1] allows for a trajectory design creating a tradeoff between phase and amplitude stability. In this work, we investigate independent gate biasing for a two-stage GaN X-band MMIC, as illustrated in Fig. 1. The MMIC is designed in the Qorvo 150 nm GaN-on-SiC process specifically for supply modulation [7]. We show that the two degrees of freedom, i.e., the two dynamic gate voltages of the driver and final stage amplifier, allow linearization both for amplitude and phase distortions.

The paper is organized as follows. First, static large-signal characterization measurements of the MMIC are presented. The results of these measurements are then used to obtain both static and dynamic gate settings designed for different linearity constraints. Finally, we show efficiency and linearity using the previously found static settings for a 20 MHz pseudo-noise test signal, with and without predistortion.

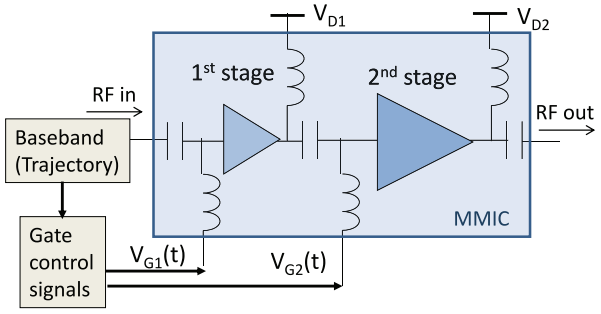

Fig. 1. Block diagram of two-stage PA with gate bias control for driver stage (V_{G1}) and final stage (V_{G2}).

II. Static Characterization Measurements

To characterize the PA in terms of gain, PAE and absolute phase variation, a measurement setup based on a vector network analyzer (VNA) is used. The VNA (E8364C) is equipped with an external large-signal test set, comprised of a benchtop high-power amplifier and a bi-directional coupler. This allows for large-signal measurements calibrated at the DUT reference plane. A full 2-port calibration is applied and a source calibration performed with a USB power sensor. This ensures absolute phase and magnitude results for a calibrated input drive level. The input power is swept between 0 dBm and 22 dBm, and both gates are independently swept in a 0.5 V range around their design values of −2.6 V and −2.65 V. This leads to a quiescent current swing between 12 mA to 110 mA at the first stage, and between 53 mA to 494 mA at the second stage.

The obtained data is shown in Fig. 2, Fig. 3 and Fig. 4 indicated in grey lines, showing gain and phase responses and power added efficiency (PAE). We observe the compressed gain for outputs larger than 10 W that are relatively independent of the quiescent current (Fig. 2). For operation in back-off, the gain variation becomes very large and ranges from 18.3 dB to 27.5 dB at 30 dBm output power. The phase response (Fig. 3) similarly varies over a large range (51° at 30 dBm), but the variation does not degrade as much at compression as for the gain. The variation of the PAE is less pronounced, which allows choosing the gate voltages for improved linearity without automatically sacrificing efficiency.

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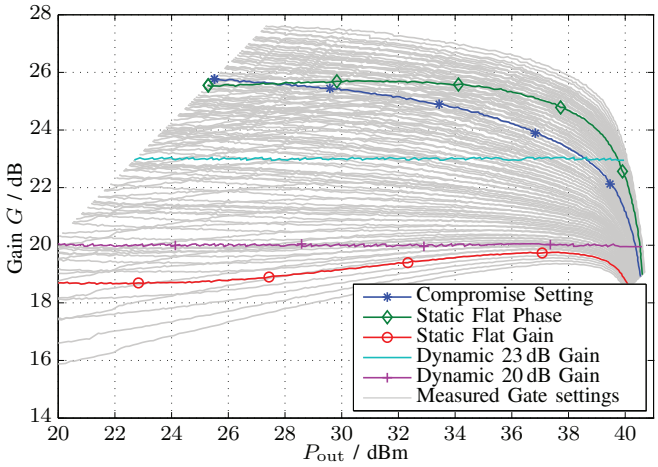

Fig. 2. Static gain characterization for a range of V_{G1} and V_{G2} shown in grey lines, and gain for chosen bias conditions shown in colored lines. The two drain supply voltages are kept at $V_{\mathrm{D1}} = V_{\mathrm{D2}} = 20\,\mathrm{V}$.

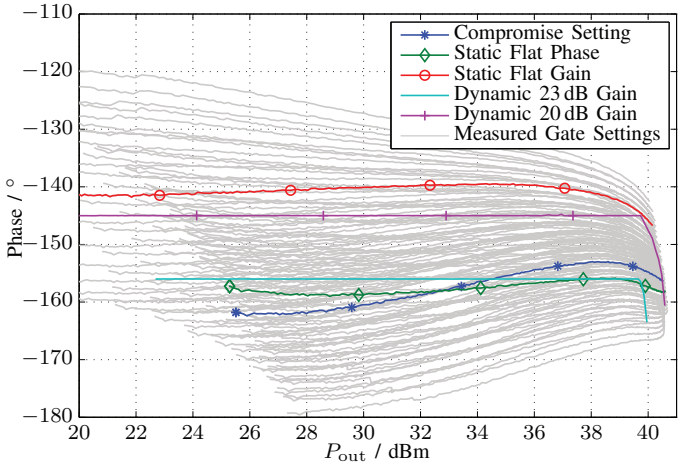

Fig. 3. Static phase characterization for a range of V_{G1} and V_{G2} shown in grey lines, and phase for chosen bias conditions shown in colored lines. The two drain supply voltages are kept at $V_{\mathrm{D1}} = V_{\mathrm{D2}} = 20\,\mathrm{V}$.

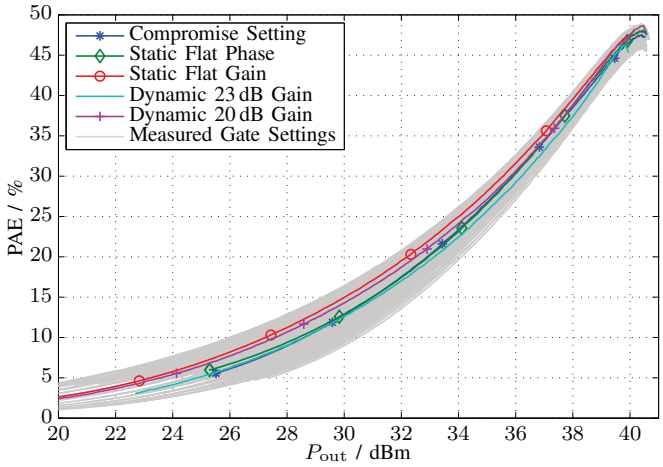

Fig. 4. Static efficiency (PAE) characterization for a range of V_{G1} and V_{G2} shown in grey lines, and PAE for chosen bias conditions shown in colored lines. The two drain supply voltages are kept at $V_{\mathrm{D1}} = V_{\mathrm{D2}} = 20\,\mathrm{V}$.

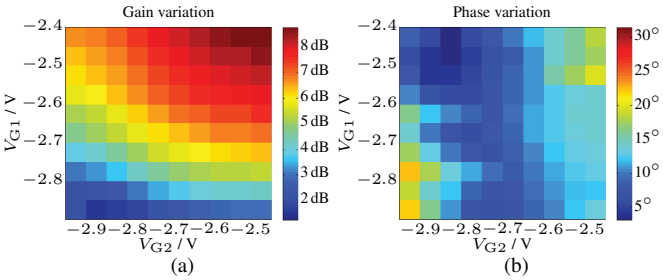

Fig. 5. Gain amplitude (a) and phase (b) variation evaluated over the entire input power range (0 dBm to 22 dBm) for measured static biasing conditions.

TABLE I
EVALUATED STATIC BIASING CONDITIONS

Drive	V_{G1}	V_{G2}	I_{D1}	I_{D2}
Compromise	−2.6 V	−2.65 V	60 mA	250 mA
Flat Phase	−2.45 V	−2.8 V	95 mA	235 mA
Flat Gain	−2.9 V	−2.75 V	14 mA	236 mA

III. Gate Bias Trajectory Selection

A. Static Gate Biasing

The obtained measurement data allows optimization of the MMIC biasing for minimum distortion within the measured V_{G1} and V_{G2} range. Fig. 5a shows the gain variation for different biasing conditions, i.e. the difference between the maximum and minimum gain in the measured 22 dB input power range. For high quiescent currents of both stages (top right corner in Fig. 5a), the gain for different input drive levels varies by more than 8 dB, since the high gain available at lower input drives drops at compression. Note that the gain variation is more sensitive to the driver stage bias, V_{G1}, than the output stage bias, V_{G2}. We find a biasing condition designed for flat gain, as noted in Table I, and the gain to vary between 18.7 dB and 19.8 dB, see Fig. 2.

In a similar fashion a static biasing for minimum phase variation is found. The corresponding plot showing the difference between the largest and smallest value of the unwrapped phases is Fig. 5b. Note that the phase variation, in contrast to the gain, is more sensitive to V_{G2}, the bias of the final stage.

Comparing the two optimized biasing schemes two a compromise bias in Fig. 2, Fig. 3 and Fig. 4 shows that the flat phase biasing is similar to the compromise setting, but shows a lower phase variation in the static measurements. The flat gain biasing operates both stages in deep class-AB so the gain is considerably lower to the other two settings, but the PAE is highest.

B. Dynamic Gate Trajectory

Since we investigate the behavior of gate drive for a two-stage MMIC we have two degrees of freedom for linearization. Using both gate biases, a trajectory is found that maintains the amplitude gain and phase as flat as possible, using a three-step approach. We start by choosing a desired gain and an allowed maximum gain deviation. For each input power level, we select all gate settings that result in a gain that lays in the

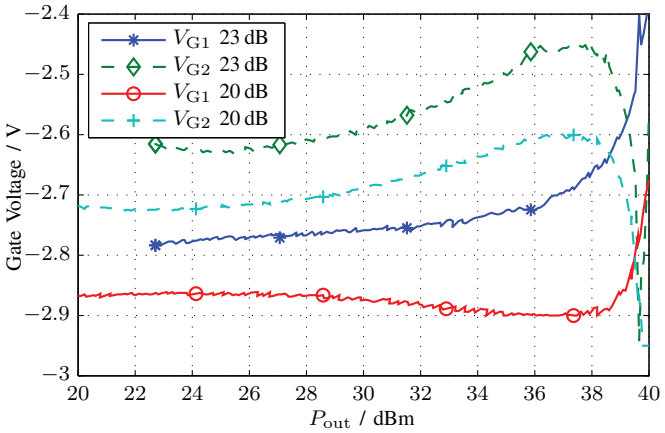

Fig. 6. Gate bias trajectories for dynamic flat gain and phase tracking. Two cases (23 dB and 20 dB gain) are plotted.

gain corridor. The phase responses using these gate settings are then evaluated in the second step, and a target phase which allows for the smallest phase variation over the power range is selected. In the third step, for each power level, the gate settings which allow for minimum deviation from the target phase are chosen from the availible settings found in step one.

Here, we first interpolate the measured data in the gate voltage domain and then set the gain margin to ± 0.05 dB and find the trajectories for constant gains of 23 dB and 20 dB. The corresponding amplitude and phase behavior is found in Fig. 2 and Fig. 3. We see that by design definition the amplitudes are flat, but do not reach the same peak power. The 23 dB gain trajectory only reaches an output power of 40.0 dBm, while the 20 dB trajectory peaks at 40.6 dBm. Inspecting the phase response (Fig. 3) we note that the 20 dB trajectory suffers from more phase distortion at peak power levels. The target phase cannot be set lower $-145°$, since otherwise the desired gain could not be reached with the available gate voltage swing, especially at V_{G1}, which was only measured to -2.9 V. The corresponding drive signals for both trajectories are plotted in Fig. 6. Both gain trajectories show similar but shifted behaviour in terms of the gate trajectories. At high output powers, the amplification is shifted from the second stage to the first stage, to maintain flat gain and phase.

While the 23 dB gain trajectory offers more amplification, it shows slightly less efficiency when compared to the 20 dB trajectory, see Fig. 4. The efficiency at peak power is even better than for the static constant gain trajectory. This shows that the dynamic gate drive allows a tradeoff between efficiency and gain while ideally maintaining linearity. Lower gains result in higher compression and therefore higher efficiencies, while higher design gains result in more quiescent current, i.e. lower efficiencies and a slightly reduced output power range.

IV. NPR Measurements

The static bias settings found in Section III-A and summarized in Table I are evaluated for their dynamic performance

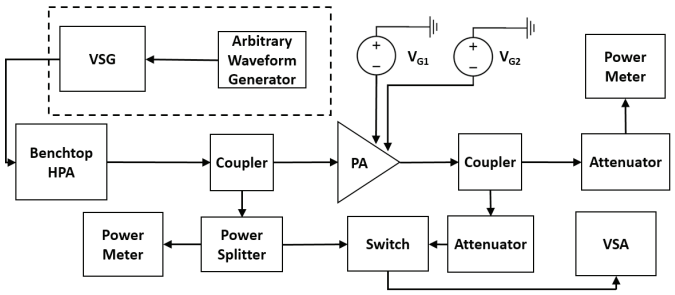

Fig. 7. Bench setup for NPR measurements.The 20-MHz test signal with a PAPR=10.8 dB is upconverted to the 9.8 GHz carrier. The drain supplies are set at 20 V, while the gate bias voltages of the 1st and 2nd stage of the MMIC PA are adjusted based on the values determined through static measurements.

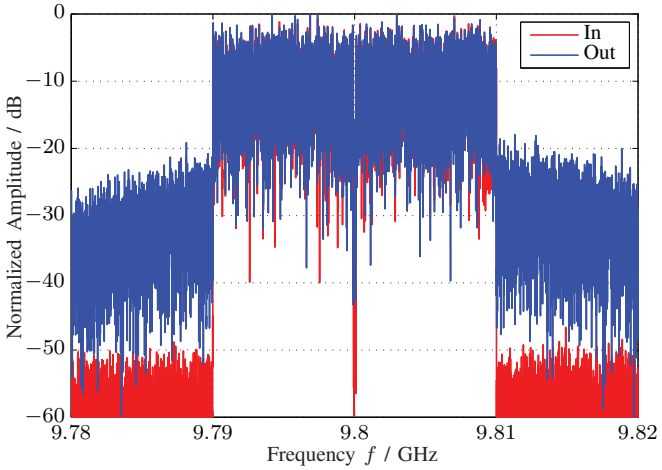

Fig. 8. Measured spectrum of 20 MHz NPR test signal for the static flat gain setting.

using noise power ratio (NPR) measurements and digitally generated noise [8]. These measurements are performed on the bench shown in Fig. 7 using a pseudo-noise signal with 20 MHz bandwidth that is created using 30 000 carriers and has a peak to average power ratio of PAPR=10.8 dB and a notch of 1 %. The signal is loaded into an arbitrary waveform generator and upconverted using a vector signal generator (VSG). IQ and spectrum data were gathered using a vector signal analyzer (VSA). Measurements are taken both at the input and output of the PA to account for any distortion the benchtop high power amplifier (HPA) may have added.

A. Direct Measurements

The spectrum of the flat gain setting is shown in Fig. 8. The data is analyzed in terms of AM/AM (Fig. 9) and AM/PM (Fig. 10) distortion, as well as NPR and average PAE as summarized in Table II. The input power is adjusted to drive the amplifier to the same peak output power of 40.1 dBm. Comparing the AM/AM, AM/PM plots we see very similar behavior of the compromise bias and flat phase bias settings, which also corresponds to similar NPR and PAE values, trading of average gain and NPR.

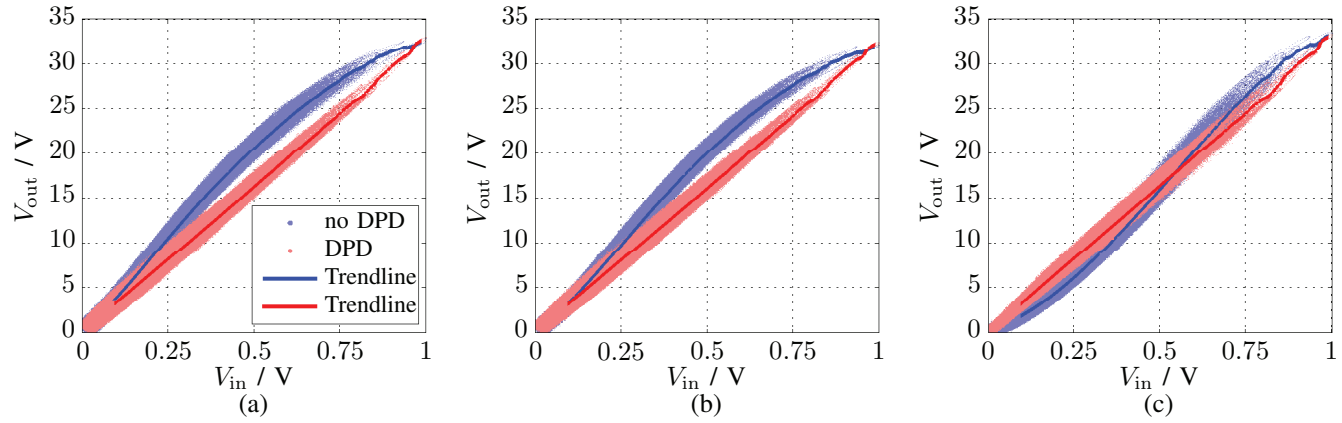

Fig. 9. Measured AM/AM response: (a) Compromise setting bias, (b) flat phase, (c) flat gain, both for direct measuremnts (blue), and predistorted PA operation (red). A trend line (local average) is shown for both cases as a darker line.

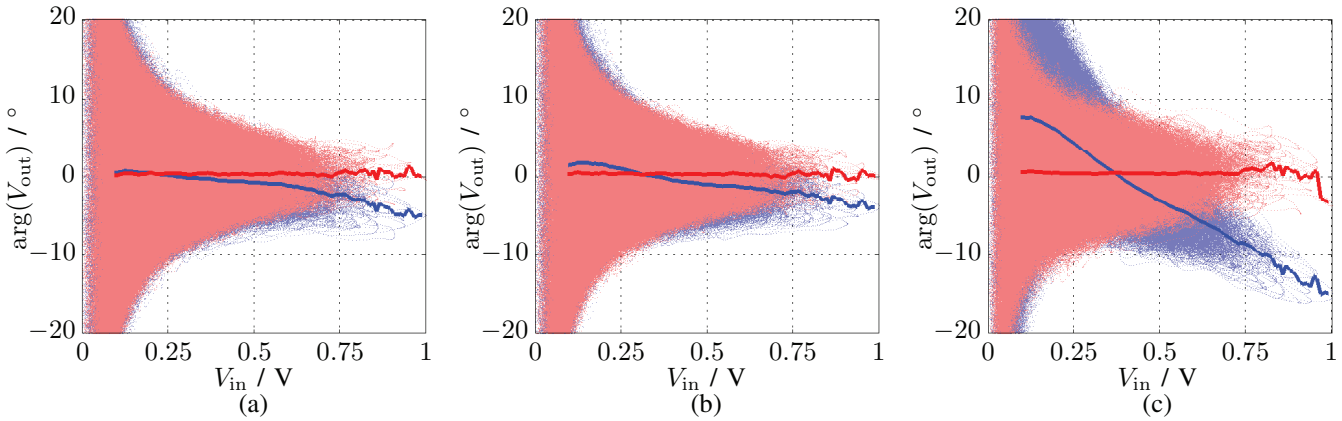

Fig. 10. Measured AM/PM response: (a) Compromise setting bias, (b) flat phase, (c) flat gain, both for direct measuremnts (blue), and predistorted PA operation (red). A trend line (local average) is shown for both cases as a darker line.

TABLE II
NPR RESULTS WITH STATIC BIASING, $\widehat{P}_{\text{out}} = 40.1\,\text{dBm}$.

Drive	NPR	$\overline{G}$	$\overline{P_{\text{out}}}$	$\overline{\text{PAE}}$	Δ-Phase
Compromise	31.3 dB	23.0 dB	31.0 dBm	19.0 %	5.7°
Flat Phase	30.7 dB	24.6 dB	31.1 dBm	17.8 %	6.0°
Flat Gain	18.7 dB	16.6 dB	27.4 dBm	14.2 %	18.8°

TABLE III
NPR RESULTS WITH STATIC BIASING AND DPD, $\widehat{P}_{\text{out}} = 40.1\,\text{dBm}$.

Drive	NPR	$\overline{G}$	$\overline{P_{\text{out}}}$	$\overline{\text{PAE}}$	Δ-Phase
Compromise	32.4 dB	22.3 dB	29.3 dBm	14.9 %	1.2°
Flat Phase	31.6 dB	23.3 dB	29.2 dBm	13.2 %	1.0°
Flat Gain	29.1 dB	17.3 dB	29.5 dBm	16.9 %	2.8°

The flat gain setting indeed shows the least bending in the AM/AM curves for higher drive levels. However, since we investigated only a 20 dB swing in the static measurements, and the MMIC is biased in deep class AB it is not surprising that the gain drops for low input power levels. Note the low measured average gain of 16.6 dB. The largest source of distortion is the AM/PM, which is the worst for all three investigated cases, and does not correspond well to the statically measured phase response. This leads to a relatively low NPR of 18.7 dB. The lowest PAE value seen in this setting, which seems to contradict the highest PAE curve in Fig. 4, is explained by the lowest amplitude compression of this bias setting. The flat phase and compromise settings which employ higher gain compression show about 3.6 dB higher average output power, so the PAE is better.

B. Predistorted Measurements

In a second measurement run, we used a memory polynomial based digital predistortion (DPD) algorithm [9] of order 18 and memory order 6 (corresponding to 4.8 ns delay) to enhance the linearity of the PA and investigate the influence on efficiency. The desired gain was set to the individual compressed gain at the peak output, so that all three cases again deliver a peak output power of $\widehat{P}_{\text{out}} = 40.1\,\text{dBm}$. The resulting AM/AM and AM/PM characteristics using DPD are plotted as red curves in Fig. 9 and Fig. 10, respectively. Observing the trend lines, it is obvious that the DPD algorithm manages to flatten the amplitude and phase response. Flattening the amplitude response of course changes the amplitude

statistics of the input signal and therefore affects the efficiency. Table III lists the results for the three cases using DPD. The predistortion slightly improves the NPR for the compromise and flat phase cases, and raises the NPR of the flat gain case to a comparable level. The average output power of all three cases now is almost identical at approximately $\overline{P_{\mathrm{out}}} = 29.3\,\mathrm{dBm}$. But most importantly, now the PAE of the compromise and flat phase cases drop to 14.9 % and 13.2 %, respectively. The efficiency of the flat phase gain setting is increased as expected, since the amplitude of the input signal is increased for small input amplitudes to compensate for the lower gain at low input powers. It is now the highest of the three cases, with almost 17 %, which agrees well with the highest PAE curve in Fig. 4.

V. Conclusion

This paper studies the gate biasing of an X-band GaN PA MMIC. Gate biasing settings are found from static amplitude/phase measurements under full power drive conditions. A flat gain setting which biases the MMIC in deep AB, and a flat phase setting which uses a slightly higher first stage current are compared to a compromise setting. Further, two dynamic gate drive signals are found which allow for flat gains of 20 dB and 23 dB, respectively, and low phase variations. NPR measurements using the static biases show good agreement of the AM/AM curves to the static measurement data. The flat gain setting is found to have the highest phase distortion and therefore the lowest NPR. The flat phase setting performs similar to the compromise setting but offers 1.6 dB more average gain as was predicted from the previous static measurements. Applying DPD the efficiencies of these three static biases are affected in different ways: the flat gain case becomes the most efficient one, as predicted by the static characterization.

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References

[1] J. Staudinger, R. Sherman, and T. Quach, "Gate and drain power tracking methods enhance efficiency in reverse link cdma amplifiers," *Applied Microwave and Wireless*, vol. 13, no. 3, pp. 28–39, 2001.

[2] B. Sahu and G. A. Rincon-Mora, "A high-efficiency linear RF power amplifier with a power-tracking dynamically adaptive buck-boost supply," *IEEE transactions on microwave theory and techniques*, vol. 52, no. 1, pp. 112–120, 2004.

[3] P. Medrel, A. Ramadan, J.-M. Nebus, P. Bouysse, L. Lapierre, and J.-F. Villemazet, "High efficiency class B GaN power amplifier with dynamic gate biasing for improved linearity," *Electronics letters*, vol. 48, no. 18, pp. 1136–1137, 2012.

[4] D. Gecan, M. Olavsbråten, and K. M. Gjertsen, "Measured linearity improvement of 10 w GaN HEMT PA with dynamic gate biasing technique for flat transfer phase," in *Microwave Symposium (IMS), 2016 IEEE MTT-S International*. IEEE, 2016, pp. 1–4.

[5] ——, "Investiogation of linearity improvement with dynamic gate bias technique for flat gain or phase of an 10 w GaN HEMT power amplifier," in *Wireless Information Technology and Systems (ICWITS) and Applied Computational Electromagnetics (ACES), 2016 IEEE/ACES International Conference on*. IEEE, 2016, pp. 1–2.

[6] A. Conway, Y. Zhao, P. Asbeck, M. Micovic, and J. Moon, "Dynamic gate bias technique for improved linearity of GaN HFET power amplifiers," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 2005, p. 4.

[7] A. Zai, D. Li, S. Schafer, and Z. Popovic, "High-efficiency X-band MMIC GaN power amplifiers with supply modulation," in *Microwave Symposium (IMS), 2014 IEEE MTT-S International*. IEEE, 2014, pp. 1–4.

[8] T. Reveyrand, D. Barataud, J. Lajoinie, M. Campovecchio, J.-M. Nebus, E. Ngoya, J. Sombrin, and D. Roques, "A novel experimental noise power ratio characterization method for multicarrier microwave power amplifiers," in *ARFTG Conference Digest-Spring, 55th*, vol. 37. IEEE, 2000, pp. 1–5.

[9] L. Ding, G. T. Zhou, D. R. Morgan, Z. Ma, J. S. Kenney, J. Kim, and C. R. Giardina, "A robust digital baseband predistorter constructed using memory polynomials," *IEEE Trans. Commun.*, vol. 52, no. 1, pp. 159–165, 2004.