Efficient and Linear Microwave Transmitters for High Peak-to-Average Ratio Signals

by

John Hoversten

B.S., Embry-Riddle Aeronautical University, 2005

M.S., University of Colorado, 2008

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical and Computer Engineering

May 2010

This thesis entitled:

Efficient and Linear Microwave Transmitters

for High Peak-to-Average Ratio Signals

written by John Hoversten

has been approved for the Department of Electrical and Computer Engineering

Zoya Popović

Dragan Maksimović

Date April 12, 2010

The final copy of this thesis has been examined by the signatories, and we find that both the content and the form meet acceptable presentation standards of scholarly work in the above mentioned discipline.

Hoversten, John (Ph.D., Electrical Engineering)

Efficient and Linear Microwave Transmitters

for High Peak-to-Average Ratio Signals

Thesis directed by Professor Zoya Popović

Current wireless communication systems use spectrally efficient modulation of microwave-frequency carriers (e.g. W-CDMA, OFDM). The base-station downlink signal is characterized by high peak-to-average power ratio (PAR) and a Rayleigh amplitude distribution and requires highly linear microwave transmitters. Traditional power amplifiers (PAs) can have high efficiency near peak output power and, as a result, have low average efficiencies for high-PAR signals. This thesis addresses the challenge of maintaining linearity and high efficiency over a broad output power range in high-power microwave communication transmitters.

PA efficiency is addressed with an improved load pull characterization method for high-power transistors in the 2-GHz range, in which fundamental frequency load pull is extended to include harmonic impedance termination and full-wave electromagnetic discontinuity analysis. The method is validated for harmonic-tuned and switched-mode high-efficiency PA topologies reaching 81% efficiency at 2.14GHz with 36 W peak output power and 14.5 dB gain from a class-F^{-1} prototype.

The high-efficiency operation is extended to reduced output power levels using an envelope tracking (ET) transmitter architecture implementing both drain and drive modulation. Drain modulation is achieved using an analog dynamic supply designed in close collaboration with colleagues in analog and power electronics. A variety of signal processing techniques (e.g. digital pre-distortion) addressing specific distortion mechanisms are used to fully restore transmitter linearity. A methodology for system design and integration is developed which relies on a new measurement-based ET system

simulation tool. The simulation merges aspects of digital baseband, signal processing, digital-to-analog conversion, up-conversion, envelope-bandwidth analog circuits, and RF components.

The integrated ET demonstration transmitter measures 50.6% total system PAE with over 7 dB adjacent channel power linearity margin for a 40-W peak power 7 dB PAR W-CDMA downlink signal at 2.14 GHz. The ET transmitter dissipates 61% less total heat than the standard drive-modulated solution, operating more than 74% longer from an equivalent fixed energy supply, while exceeding W-CDMA 3GPP linearity specifications.

Dedication

To Kate.

Personal Acknowledgments

It has been my great pleasure to share the graduate school experience with the present and past members of the research group. For their invaluable technical expertise and comradery I extend my sincere thanks to Dr. Patrick Bell, Dr. Jason Breitbarth, Evan Cullens, Erez Falkenstein, Dan Kuester, Dr. Hung Loui, Dr. Qianli Mu, John O'Brien, Dr. Mabel Ramírez, Dr. Leonardo Ranzani, Dr. Sébastien Rondineau, Rob Scheeler, Jason Shin, Thomas Thalmann, Dr. Kenneth Vanhille, Christi Walsh, and Dr. Narisi Wang. I am especially grateful to Dr. Alan Brannon for dispensing sage advice about graduate student life; to Jonathon Chisum for time spent discussing so many topics unrelated to microwave microscopy; to Dr. Charles Dietlein for an introduction to beautifully type-set documents and for eagerness to share his knowledge of nearly everything; to Dr. Negar Ehsan for solidarity in studying for the qualifying exam; to Dr. Mike Elsbury, Dr. Luke Sankey, and Dr. Aaron Scher for *esprit de corps* as we spent our first years at CU; to Nicola Kinzie for proof-reading this entire thesis; to Dr. Néstor López for his patience while working with a new graduate student; to the Pepsi Cola Corporation for faithfully distributing a light, crisp, and refreshing beverage; and to Michael Roberg for being a great collaborator and friend. I am also grateful to Phil Bonzell, Rev. Daniel Burhop, Prof. Milton Cone, Dr. Kyle Lampe, Lisa Lampe, Chan La-o-vorakiat, Joseph McCalley, and Dr. Karl Siebold for their friendship, support, and encouragement. I could not have asked for better colleagues, teachers, or friends.

I would like also to thank my family for their prayers, love, and support throughout

my life. I am grateful to my parents for providing opportunities and encouragement to pursue this goal. I learned the value of hard work and dedication by their example. Finally, thank you Kate for your unwavering love, patience, and reassurance. You put life into perspective, and help me to focus on the things that really matter.

Soli Deo Gloria

Professional Acknowledgments

I am sincerely grateful to Prof. Zoya Popović for serving as my advisor. She has worked tirelessly to provide exciting research projects, technical direction, funding, an impressively-equipped lab, and an outstanding group of colleagues. My graduate school experience has been punctuated by numerous collaborations, internships, and travel experiences that she made possible. I am honored to have studied with her.

I very much appreciate the efforts of my thesis committee: Prof. Zoya Popović, Prof. Ken Baker, Prof. Tim Brown, Prof. Dejan Filipović, Prof. José Angel García, Dr. Cole Howard, and Prof. Dragan Maksimović who took time to discuss, read, evaluate, and make valuable suggestions.

Several others have contributed critical pieces to my graduate education and to the work presented in this thesis, and must be acknowledged:

- Researchers in the group who did excellent work in the field of power amplifiers, and so freely share their time, knowledge, and experience - especially my predecessor Dr. Néstor López, and successor Michael Roberg.

- Jarka Hladisova, Adam Sadoff, and Wayne Gardener for handling many of the administrative aspects of graduate research with professionalism and efficiency.

- Prof. Dragan Maksimović and Mark Norris of the Colorado Power Electronics Center for collaboration throughout most of my graduate work, but especially in the envelope tracking research.

- Rob Woolf at National Semiconductor for research funding, internship and employment opportunities, words of advice and wisdom, and for being a good friend.

- Steve Berg, Dr. Sandeep Dhar, Mark Kagey, Yushan Li, Kevin Vannorsdel, Prof. Vahid Yousefzadeh, and Art Zirger at the National Semiconductor Longmont Design Center, for contributing further analog and power electronics expertise. Envelope tracking transmitter research without their input, collaboration, and prototype circuitry would have been impossible.

- The U.S. Department of Education, for funding Prof. Popović's Graduate Assistance In Areas of National Need (GAANN) fellowship proposal, which funded my first year of graduate research.

- Dan Hornung of Roydan Enterprises, Mark Klatt of Motorola, and Mark Bloom formerly of Freescale Semiconductor for internship experiences early in my collegiate education which provided a valuable real-world perspective.

- Bill McCalpin, Bob Crispell, Dr. Joe Hagerty, Dr. Srdjan Pajić, and several others at TriQuint Semiconductor for collaboration, discussion, and use of equipment.

- Tim Driver with RF Micro Devices, Dr. David Choi formerly with RF Micro Devices, Randy Cochran with Nitronex, and Dr. Todd Nichols formerly with Nitronex for collaboration, practical advice, and providing sample transistors.

- Dr. Cole Howard at Science Applications International Corporation for funding research, and for the opportunity to spend a summer in Washington D.C. exploring digital predistortion techniques.

- Dr. Michael Forman at Sandia National Labs for funding research, the opportunity to speak at Sandia, and also the opportunity to gain experience using harmonic load pull tuners.

- Prof. José Angel García at the University of Santander for the invitation to give a course with Prof. Popović, the opportunity to travel to Spain, for providing comprehensive feedback on this thesis, and for traveling to the Colorado to attend my defense.

Contents

List of Tables

List of Figures

List of Abbreviations

2DEG 2D electron gas 81

3GPP 3rd Generation Partnership Project 19

ACLR adjacent channel leakage ratio 21

ACP adjacent channel power 19

AuSn gold tin 82

AWG arbitrary waveform generator 142

BJT bipolar junction transistor 5

CAD computer aided design 82

CCDF complementary cumulative distribution function 17

CF crest factor 19

CFR crest factor reduction 10

CuMo copper molybdenum 87

CW continuous wave 66

DDR dynamic deviation reduction 155

DPD digital pre-distortion 10

DSP digital signal processing 179

DUT device under test 59

EDGE Enhanced Data rates for GSM Evolution 8

EER envelope elimination and restoration 12

EM envelope modulator 13

EVM error vector magnitude 19

FEM finite element method 6

FET field effect transistor 4

FIR finite impulse response 159

GaN gallium nitride 24

GMSK Gaussian multiple shift keying 105

GSM Global System for Mobile Communications 3

HBT heterojunction bipolar transistor 52

HEMT high electron mobility transistor 29

HFSS High Frequency Surface Simulator 6

HVHBT high-voltage heterojunction bipolar transistor 11

IPD integrated passive device 177

LDMOS laterally-diffused metal oxide semiconductor 9

LINC linear amplification using nonlinear components 11

LUT look-up table 138

MESFET metal semiconductor field effect transistor 71

MIMO multiple input multiple output 178

MMIC monolithic microwave integrated circuit 179

MOS metal oxide semiconductor 30

MOSFET metal oxide semiconductor field effect transistor 81

MP memory polynomial . . . 155

OFDM orthogonal frequency division multiplexing . . . 16

OBW occupied bandwidth . . . 17

OPB output power back-off . . . 8

PA power amplifier . . . 1

PAE power added efficiency . . . 4

PAR peak-to-average power ratio . . . 1

PCDE peak code domain error . . . 22

PDF probability density function . . . 17

PEP peak envelope power . . . 7

PSD power spectral density . . . 17

RS Rohde and Schwarz . . . 142

RF radio frequency . . . 1

RMS root mean squared . . . 19

RRC root raised cosine . . . 19

RSPC repeated scaled peak cancelation . . . 22

SC-FDMA single-carrier frequency division multiple access . . . 178

Si silicon . . . 30

SiC silicon carbide . . . 70

SMPS switched-mode power supply . . . 109

SNR signal to noise ratio . . . 143

SPDT single pole double throw . . . 67

TM test and measurement . . . 142

TRL thru reflect line 63

UAV unmanned arial vehicle 178

UHF ultra high frequency 23

VNA vector network analyzer 57

VSA vector signal analyzer 141

VSWR voltage standing wave ratio 68

W-CDMA Wideband Code Division Multiple Access 1

ZVS zero voltage switching 50

Chapter 1

Introduction

Contents

This thesis addresses the problem of efficient amplification of RF[1] signals with high PAR[2]. Such signals have come into widespread use as communication links demand more data throughput with limited spectrum. The single-channel W-CDMA[3] downlink signal is used throughout this work as a representative high-PAR signal, though concepts presented here apply to a wide variety of similar signals.

The first portion of this chapter discusses general RF transmitters, PA[4] efficiency enhancement, and high-PAR transmitter efficiency enhancement techniques. Next a brief overview of W-CDMA modulation and linearity requirements is presented, followed by an outline of the thesis.

[1] radio frequency

[2] peak-to-average power ratio

[3] Wideband Code Division Multiple Access

[4] power amplifier

1.1 Microwave Transmitters

A general RF transmitter block diagram is shown in Fig. 1.1. The PA (also called the power stage) is the dominant source of power dissipation and nonlinearity in the transmitter, so this work focuses on that key component. Therefore, in this work "transmitter" performance will reflect the contribution of only the PA, assuming other transmitter components are ideal. Center frequency, output power, gain, and modulation type are the main parameters that impact PA design.

This thesis focuses on design of transmitters producing peak output power levels from 5 W to 250 W at frequencies ranging from 300 MHz to 2.5 GHz and with gain from 10 dB to 18 dB. Modulation types can be divided into two classes: constant envelope and varying envelope.

The following general definitions will be used throughout this work, referring to Fig. 1.1:

Fundamental and Harmonic Frequencies – f_o is the fundamental, or carrier frequency, of the transmitter. f_n is used to denote frequencies which are an integer multiple of the fundamental. A frequency $f_2 = 2f_o$ is referred to as the second harmonic.

RF Input and Output Power – P_{in} and P_{out} are average input and output RF

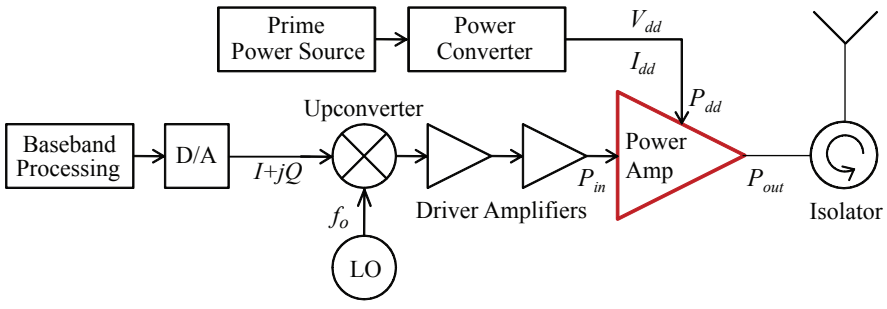


Figure 1.1: Block diagram of a general RF transmitter. The PA is the primary contributor to transmitter power dissipation and nonlinearity, and is the focus of this work.

power, always referenced to a 50Ω termination, and expressed in units of watts unless otherwise noted. The decibel-milliwatt (dBm) scale is also used with the following conversion:

$$P_{dBm} = 10\log\left(P_W * 1000\right) \tag{1.1}$$

Conversion between RF power and the peak value of the RF voltage (also called envelope voltage or modulation amplitude) is achieved using the following:

$$P = \frac{|V_{rms}|^2}{R} = \frac{\left(\frac{|V_{pk}|}{\sqrt{2}}\right)^2}{R} = \frac{|V_{pk}|^2}{2R} \tag{1.2}$$

In this work these quantities will be used with reference to the power stage PA only. Only power at f_o is included in this definition, as harmonic power delivered to the load is not useful.

Drive and Drain Modulation – Traditionally PA output power is controlled by variation of RF input power (drive modulation). Techniques discussed in this work will also include variation of drain supply voltage V_{dd} as a means of output power control (drain modulation).

Gain – G is the ratio of output power to input power for a stage or series of stages. Gain of RF components in this work is always with reference to the power stage PA, and always expressed in decibels:

$$G = 10\log\left(\frac{P_{out}}{P_{in}}\right) \tag{1.3}$$

1.1.1 Power Amplifier Efficiency

Constant envelope waveforms, such as those used in the GSM[5] communications standard and most radar applications, have constant output power; they do not rely on precise amplitude variation to convey information. As a result these signals can make use of a PA operating in a highly non-linear, gain compression region. As a result of the

[5]Global System for Mobile Communications

gain compressed operation, the PA operates with improved efficiency. Even so, a 50%-efficient PA producing 100 W requires 200 W input power, generating 100 W waste heat. Active thermal management is frequently required to ensure high reliability, adding to energy requirements. In mobile applications, PA efficiency has a direct impact on battery life.

The following additional definitions will be used throughout this work:

Amplifiers and Transmitters – An amplifier is distinct from a transmitter in that both its input and output are RF signals. Modern *transmitters* have digital inputs and may incorporate many *amplifiers*.

Drain Efficiency – η_d is the ratio of output RF power to drain supply power:

$$\eta_d = \frac{P_{out}}{P_{dd}} \tag{1.4}$$

Note that no consideration is given to the amount of RF input power consumed. When gain is low (and input power is an appreciable fraction of output power) it becomes important to state both drain efficiency and gain or use a different efficiency metric. Measurement of drain efficiency is very straightforward because it involves measurement of only two quantities.

Power Added Efficiency – PAE[6] takes into account the required input power:

$$PAE = \frac{P_{out} - P_{in}}{P_{dd}} = \frac{P_{out}(1 - \frac{1}{G})}{P_{dd}} = \eta_d \left(1 - \frac{1}{G}\right) \tag{1.5}$$

PAE is always less than η_d, but as gain rises η_d and PAE begin to converge to the same value.

Fig. 1.2 is a general block diagram of a PA using a FET[7]. Input power, output power, and drain supply voltage and current are the same quantities defined for the power stage in Fig. 1.1. Additional terminology includes the following:

[6] power added efficiency

[7] field effect transistor

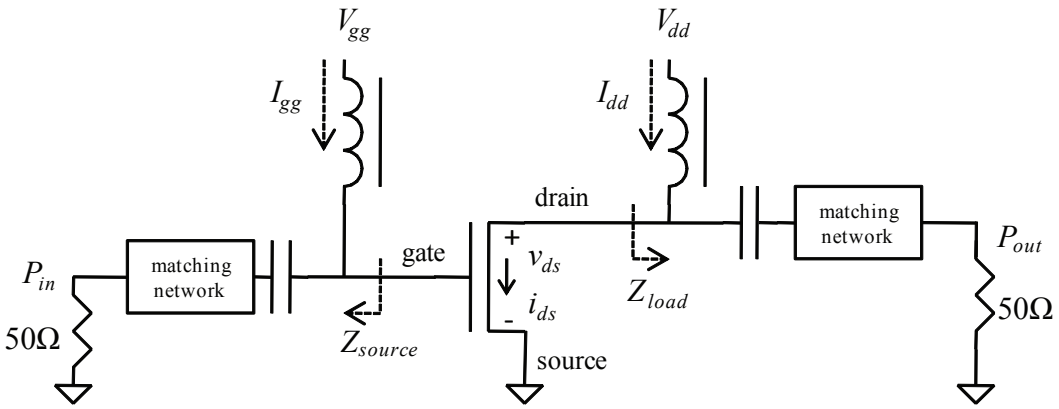


Figure 1.2: Block diagram of a general PA.

Gate, Drain, and Source – FETs are used throughout this work, with corresponding gate, drain, and source nomenclature. A BJT[8] transistor has equivalent terminal names: base, collector, and emitter, respectively.

Source and Load Impedance – Z_{source} and Z_{load} are the impedances seen by the transistor. Note that these impedances are defined at not only the fundamental, but all frequencies.

Gate Supply Voltage and Current – V_{gg} is the DC value of the gate bias voltage. Some types of transistors draw a small amount of gate current I_{gg} under saturated operation.

Drain Supply Voltage and Current V_{dd} and I_{dd} are isolated from the FET drain by an RF choke, and are thus constant for a constant value of P_{out}.

Drain Voltage and Current v_{ds} and i_{ds} are the instantaneous voltage across and current through the transistor drain and source terminals. Simultaneously non-zero drain voltage and current create power dissipation in the transistor. This is the dominant cause of dissipation in traditional PAs. Note that v_{ds} is not equal to the voltage across the 50Ω PA output terminal due to the presence of a matching

[8] bipolar junction transistor

network.

High-efficiency harmonic-tuned and switched-mode PA operation can dramatically reduce PA power dissipation as compared to traditional classes of operation (A, AB, B, C) [1]. Both methods increase PA efficiency by shaping v_{ds} and i_{ds} to reduce overlap, avoiding loss in the transistor. This wave shaping is achieved by, for example, summing odd-harmonic voltage components to produce a square v_{ds} waveform rather than the class AB sinusoidal shape. High-efficiency modes of operation are more complex to design, demand higher-performance transistors than traditional PA designs, and require design of specific fundamental and harmonic load impedances.

High-power transistor packages are often an obstacle to high-efficiency design [2]. Though designed for adequate electrical performance at the fundamental frequency, commercial packaging frequently presents a high-Q network at harmonic frequencies, making harmonic impedance control difficult. Ansoft HFSS[9] is used in this work for FEM[10] simulation of the package transformation. In cases where packaging makes high-efficiency design impractical, alternative packaging methods are pursued, including modification of the package and use of un-packaged (chip) devices. In this method the die is wire-bonded directly to the microstrip PA circuit, reducing parasitic effects but adding significant time and complication in prototype assembly.

Traditional amplifier design methods using S-parameters are not useful for inherently nonlinear high-efficiency design. Furthermore, existing non-linear models have been found inadequate for high-power high-efficiency designs [3] in which the well-modeled transistor active region is largely avoided. Instead, empirical design methods supplement approximate analytical designs. In a load pull system mechanical tuners are used to present varying source and load impedance to the transistor via pre-matching circuitry, resulting in mapping of device performance over a range of impedances [4]. A

[9] High Frequency Surface Simulator

[10] finite element method

specialized load-pull method is described in this work which includes the impact of harmonic impedance control in the measurement [5].

A 110-W class E PA [6] at 360 MHz achieving 83% drain efficiency with 16 dB gain and a 36-W class F^{-1} PA [2] at 2.14 GHz achieving 81% drain efficiency with 14.5 dB gain are presented to illustrate the high-efficiency design methods described in this work.

1.1.2 High-PAR Transmitter Efficiency

The following definitions related to modulated signals will be used throughout this work (consistent with [7]):

Envelope, or Amplitude – Amplitude modulation results in slow variations of the peak RF voltage of the carrier. This level is referred to as the envelope, or amplitude, of the modulated signal.

Baseband Representation – Vector modulation of an RF carrier can be expressed in terms of amplitude and phase or as the sum of orthogonal in-phase and quadrature carrier components:

$$v(t) = A(t)\cos(\omega t + \phi(t)) = (I(t)\cos\omega t - Q(t)\sin\omega t) = \Re\left(\tilde{v}(t)e^{j\omega t}\right) \tag{1.6}$$

When analyzing signals in the modulation domain it is useful to eliminate the time-harmonic variation of the RF carrier, leaving a baseband representation using either "IQ" ($I(t)$ and $Q(t)$) or "Aϕ" ($A(t)$ and $\phi(t)$) forms. Both forms are equivalent and useful in different contexts. Throughout this work complex baseband modulation signals are indicated by lower-case variables beneath a tilde (e.g. $\tilde{v}$).

Peak Envelope Power – PEP[11] is the maximum instantaneous value of the RF output power. Envelope voltage magnitude and PEP are related by the power-voltage relationship of Eqn. 1.2.

[11] peak envelope power

Average Power – P_{avg} is the time-averaged RF output power.

Modulated, or Average, Efficiency – Because efficiency varies with output power level it becomes critical to distinguish between efficiency with constant output power and with modulated output power. Average efficiency is not equal to the average of the time-varying efficiency but is instead defined as:

$$\eta_{avg} = P_{out,avg}/P_{dd,avg} \tag{1.7}$$

Average efficiency is assumed when discussing efficiency of modulated signals.

Output Power Backoff – OPB[12] is the amount by which maximum transmitter power is reduced to avoid gain compression non-linearity.

Driven by demand for increased spectral efficiency, waveforms with varying amplitude and phase such as EDGE[13] and W-CDMA have time-average power significantly lower than the PEP. The PAR of these waveforms ranges from 3 dB to more than 10 dB. The efficiency of the high-efficiency modes of operation described previously degrades quickly with reduced output power, resulting in a low time-average efficiency.

Amplitude modulated signals require input-output power linearity and can withstand only limited distortion due to gain compression. Such distortion is traditionally limited by avoiding very high output power levels at which PA gain is compressed. OPB causes the PA to operate in the linear region, further reducing the average output power and average efficiency.

Notional curves representing typical PA efficiency and gain behavior with decreasing output power are shown in Fig. 1.3 along with the amplitude probability density function for a high-PAR signal. Note that the highest-probability output power levels are produced with low efficiency, and that output power back-off exaggerates the problem.

[12] output power back-off

[13] Enhanced Data rates for GSM Evolution

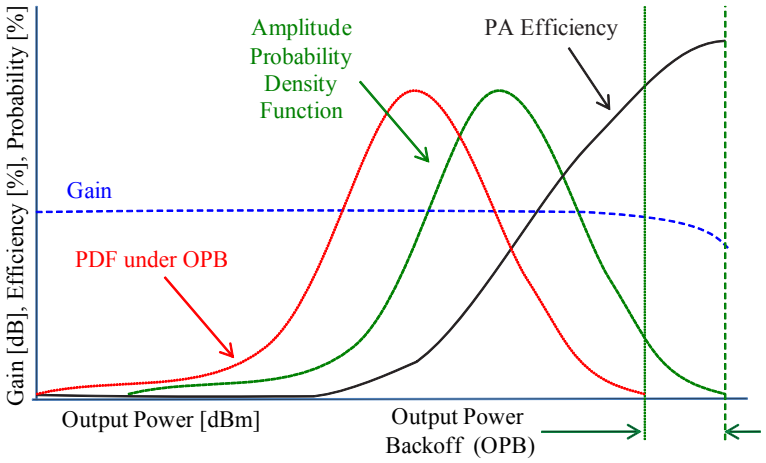


Figure 1.3: Typical PA efficiency and gain behavior over output power. Probability density functions for a high-PAR signal at two average output power levels are overlaid.

The impact of high-PAR signals is apparent when examining power consumption of high-power cellular base stations in the 2.14 GHz downlink band, in which power stage PA efficiency is typically on the order of 9% for an LDMOS[14] class AB transmitter power stage [8]. Average output power of 50 W therefore requires more than 550 W DC power, resulting in 505 W heat dissipation. Dissipation due to air conditioning systems and DC power converter systems result in a further penalty of 1.41 W per watt dissipated [9]. Table 1.1 illustrates this impact for three PA power stage efficiencies.

Improving PA efficiency from 9% to 50% reduces PA input power requirements from 555 W to only 100 W. Total power required including peripheral equipment drops from

Table 1.1: Impact of PA efficiency on total transmitter power consumption.

PA Efficiency	9%	30%	50%
PA Output Power	50 W	50 W	50 W
PA Input Power	555 W	167 W	100 W
PA Dissipated Power	505 W	117 W	50 W
Peripheral Losses (e.g. Cooling, Power Distribution)	712 W	165 W	71 W
Total Power Dissipation	1217 W	282 W	121 W
Transmitter Efficiency Including Peripheral Losses	4.0%	15.1%	29.2%

[14] laterally-diffused metal oxide semiconductor

1,267 W to only 171 W - an 86.5% reduction in power stage energy consumption. This type of improvement has a large impact on systems operating from a limited energy supply, such as mobile applications. The impact is also significant in terms of energy cost.

Transmitter efficiency for high-PAR signals has been previously addressed with a number of methods [10]. DPD[15] techniques [11] account for the non-linearity gain compression in high-efficiency class AB operation by modifying the digital baseband input signal. The ability to operate closer to maximum PEP with reduced OPB allows increased average output power and higher average efficiency.

The baseband signal can be pre-processed using CFR[16] techniques to reduce PAR [12]. Infrequently-occurring high-power peaks are clipped to a lower power level. PAR can be significantly reduced with acceptable increase in distortion, resulting in increased PA efficiency.

Invented many decades ago [13], Doherty power amplifiers make use of a main amplifier biased class AB and a peaking amplifier biased class C and connected via a special impedance transformation network. At low output power levels the main amplifier operates linearly and the peaking amplifier is inactive, dissipating no power. As power increases the main amplifier becomes compressed and operates efficiently as the peaking amplifier turns on. Operation of the peaking amplifier changes the load impedance seen by the main amplifier, which is adjusted with output power level to achieve improved efficiency at low input power and improved output power at high input power. A variety of permutations have evolved from this basic concept [14] varying the size and number of peaking amplifiers. These techniques improve efficiency at reduced output power levels and, therefore, average efficiency of high-PAR modulated signals.

[15] digital pre-distortion

[16] crest factor reduction

In [15] an LDMOS-based Doherty PA designed for W-CDMA downlink modulation with 9.8 dB PAR at 2.14 GHz achieved 41% PAE average efficiency at 46 dBm average power. This performance is an increase of 15% over class AB operation with the same device. A similar design using cutting-edge HVHBT[17] device technology from Triquint [16] resulted in 57% average collector efficiency for a W-CDMA downlink signal with 6.5 dB PAR at 47 dBm average output power, an increase of 25% efficiency over class AB operation. This record result comes largely from the application of cutting-edge device technology, shown by the fact that the main PA exhibited an impressive 72% collector efficiency at PEP.

Though very significant in terms of efficiency enhancement, the Doherty solution is not without disadvantages. Linearity is necessarily degraded as compared to class AB operation and requires the use of DPD linearization. Though not always active, both amplifiers are always driven with RF input power, reducing gain by at least 3 dB. Furthermore, the output transformation network has bandwidth typically less than 10%.

Chiriex, outphasing, and LINC[18] architectures (discussed in detail in [17] and [18]) also utilize two high-efficiency PAs to maintain high efficiency over a range of output power levels. The input to both PAs is a constant envelope signal, maintaining high-efficiency compressed operation continuously. Peak power is achieved by feeding both PAs with an identical signal. A phase offset of equal magnitude and opposite sign can be applied to the input signal of each PA resulting in out-of-phase output power combining, and consequently reduced output amplitude.

Supply modulation techniques all involve variation of the PA drain supply voltage with desired output power. Reduced drain supply voltage changes the PA operating point and consequently reduces output power capability. Gain compression, and thus efficient operation, occurs at reduced output power. This fundamental idea has been

[17] high-voltage heterojunction bipolar transistor

[18] linear amplification using nonlinear components

implemented in the literature in many ways and with varying terminology.

EER[19] was originally conceived in 1952 by Kahn [19]. An amplitude detector is used to determine the RF input modulation amplitude, and a drain supply modulator applies a linearly related PA drain supply voltage. A limiter at the PA input eliminates envelope variation, applying a constant input power level to the PA. Gain changes with drain supply variation and imposes amplitude modulation on the PA output signal.

The constant input power to a Kahn EER PA must be large enough to produce high efficiency and output power, resulting in excessive gain compression at average output power leading to reduced PAE especially in the case of high-PAR signals. Power coupling from PA input to PA output, even in the absence of drain supply voltage, is also a problem for signals which must instantaneously reach zero output power. Authors have since realized the advantage of drive modulation [20] in EER systems to produce required output power with high efficiency and the minimum required drive power. Cripps describes such systems as "Polar" or "Envelope Restoration" systems lacking the input RF limiter [21].

Digital implementations of EER are also frequently described in literature as polar transmitters [22] [23]. A variety of terms have appeared to describe drain- and drive-modulated transmitter power stages, including Hybrid EER [24] [25], Wideband EER [26], Hybrid Quadrature Polar Modulated [27], and Wideband Envelope Tracking [28]. These methods vary among each other in the type of PA used (switched mode or linear), in the degree of gain compression created in the PA, and in implementation.

The family of supply modulation techniques most closely related to the work in this thesis are encompassed by "Envelope Tracking". This term most frequently refers to a digitally controlled system driving a class AB biased PA into heavy saturation. A number of ET implementations have been described addressing the W-CDMA downlink application with a power level and center frequency similar to systems in this work [29]

[19] envelope elimination and restoration

[30] [31]. The primary distinctions between these references and this thesis lie in the PA design (discussed in Chapters 2 and 3), ET system simulation (Chapter 4), and specific signal processing techniques used for linearization (Chapter 5).

1.1.3 Envelope Tracking Transmitter

An ET system block diagram is shown in Fig. 1.4. The ET architecture makes use of analog circuitry to vary the PA drain supply voltage with respect to the instantaneous output power. In this work the drain supply modulation circuitry is called an EM[20]. Supply variation results in gain compressed, high-efficiency PA operation for both peak and average output power levels. Efficiencies must be re-defined when discussing ET transmitters:

System, or Transmitter, Efficiency – PAE and drain efficiency of envelope tracking systems must consider losses in the EM:

$$\eta_d = \frac{P_{out}}{P_{DC}} \tag{1.8}$$

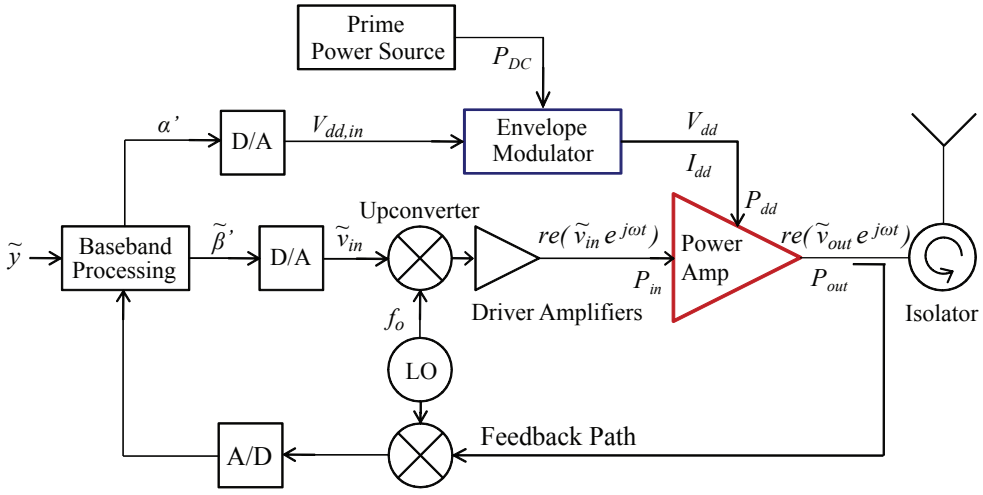


Figure 1.4: Block diagram of an envelope tracking transmitter. Note the addition of a supply modulation circuit and a down-conversion feedback path from the PA output used to correct transmitter linearity.

[20] envelope modulator

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{1.9}$$

Component Efficiency – Individual EM and PA efficiencies are also defined:

$$\eta_{d,PA} = \frac{P_{out}}{P_{dd}} \tag{1.10}$$

$$PAE_{PA} = \frac{P_{out} - P_{in}}{P_{dd}} \tag{1.11}$$

$$\eta_{EM} = \frac{P_{dd}}{P_{DC}} \tag{1.12}$$

Unlike the PA, the EM has a high-impedance input which consumes no input power. Therefore power-added efficiency of an EM is undefined.

The baseband representation of complex PA input and output signals are labeled with $\tilde{v}_{in}$ and $\tilde{v}_{out}$, while transmitter input (a digital baseband signal) is labeled $\tilde{y}$.

Complex PA and Transmitter Gain – Magnitude and phase of the complex gain are also called "insertion gain" and "insertion phase." Complex gain can be defined at the PA and transmitter reference planes:

$$\tilde{g}_{PA} = \tilde{v}_{out}/\tilde{v}_{in} \tag{1.13}$$

$$\tilde{g} = \tilde{v}_{out}/\tilde{y} \tag{1.14}$$

The complex PA gain $\tilde{g}_{PA}$ varies with drain supply voltage, and the complex transmitter gain $\tilde{g}$ defines transmitter linearity.

Many signal processing techniques are used in the baseband processing block to achieve transmitter linearity: (1) the modulated input signal $\tilde{v}_{in}$ must be adjusted for the time-varying complex PA gain $\tilde{g}$ using a look-up table filled with gain and phase correction factors, (2) EM frequency response is corrected through the use of a linear equalizer, (3) a delay adjustment algorithm ensures that drain supply variation and PA input modulation occur in synchrony, and (4) dynamic distortion in the PA is

accounted for through the use of a polynomial-based digital pre-distortion algorithm. These techniques are discussed in detail in Chapters 4 and 5.

ET system efficiency is the product of the efficiencies of PA and EM components. Placing certain demands on the EM to achieve PA efficiency can dramatically reduce EM efficiency, leading to reduced overall system efficiency. This tradeoff is made by carefully shaping the drain supply as a function of the instantaneous desired output power, dictating the waveform that the EM must reproduce. The relationship between drain supply voltage and instantaneous desired output power also impacts PA efficiency. Thus the EM waveform can be made easier to reproduce, increasing EM efficiency at the expense of PA efficiency.

An ET system proof-of-concept test bed has been designed and implemented to enable this research. Well suited to a wide variety of high-PAR signals, the ET demonstration is cast as a W-CDMA downlink transmitter. Test and measurement equipment and extensive MATLAB computer control are used to generate modulated RF and analog signals, down-convert and capture waveforms, and realize the signal processing algorithms described above. A number of previously unforseen challenges in PA, EM, and system design are only uncovered after integration on the test bench.

This work presents measured results from many pieces of the ET proof-of-concept system. ET system PAE above 50% is demonstrated at 8.5 W average power for a 7 dB PAR W-CDMA signal with excellent linearity. This represents more than 20% efficiency improvement over the traditional drive-modulated final PA stage, and a reduction in dissipated power of 12.1 W, or 38.9%. Dissipated power in the RF transistor is reduced from 19.8 W to only 2.7 W, a reduction of 86.4%. The high level of system complexity of the ET system is offset by significant performance improvements.

1.2 High-PAR Signals

Throughout this work the W-CDMA downlink modulation signal is used as a representative high-PAR signal. Large amplitude peaks and a Rayleigh amplitude distribution result from the summation of many statistically independent signals. In fact, most all spectrally efficient modulation types, such as OFDM[21], exhibit similar characteristics. The concepts and results shown in this work can thus be generalized to other modulation schemes sharing certain important features.

1.2.1 Signal Characteristics

The complex IQ trajectory for a 10-msec segment of a downlink W-CDMA signal is shown in Fig. 1.5. Note that the amplitude reaches a very high peak value only once during the segment.

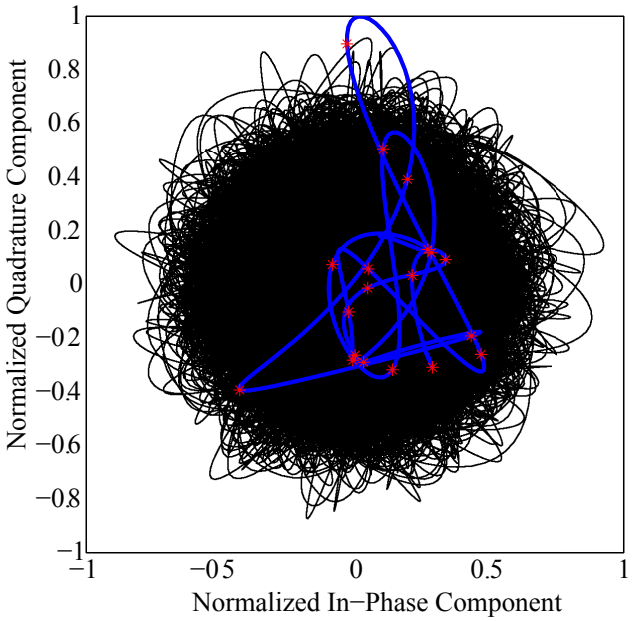


Figure 1.5: Complex IQ trajectory for a 10-msec segment of a downlink W-CDMA signal shown in black. The blue portion is a 5-μsec segment used in the plots of Fig. 1.6, and connects the chipping instances which are shown by red stars.

[21] orthogonal frequency division multiplexing

The 5-μsec blue segment of Fig. 1.5 is shown projected into amplitude/phase (Fig. 1.6(a)) and in-phase/quadrature (Fig. 1.6(b)) components. Note from Fig. 1.6(a) that the amplitude, and thus the output power, of the signal value changes (slews) from minimum to maximum in only 250 nsec. This feature, coupled with sharp amplitude nulls such as the one occurring at 2.5 μsec, are of great importance in an ET system. Ideally the EM would track this wide-bandwidth amplitude profile exactly.

The salient features of any modulated signal can be described using the following metrics and plots:

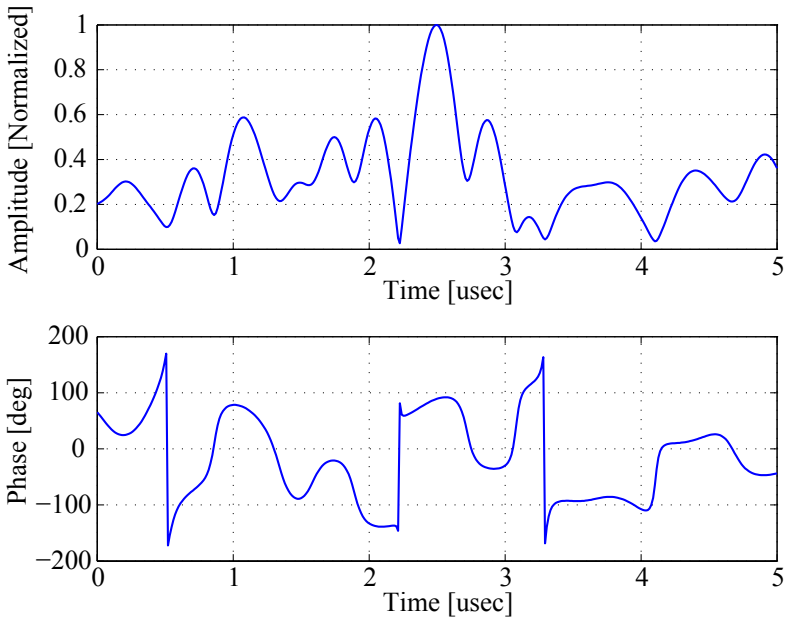
Power Spectral Density – The PSD[22] for an ideal W-CDMA downlink signal is shown in Fig. 1.7(a). Note that the signal under analysis is the baseband representation – the carrier has been removed. The ideal modulated RF signal can be instead shown by shifting the PSD x-axis from DC to the carrier frequency.

Output Power Back-off – OBW[23] is the bandwidth required to encompass 99% of the power in the signal. In the case of the case of the signal shown in Fig. 1.7(a) the OBW is 4.165 MHz.

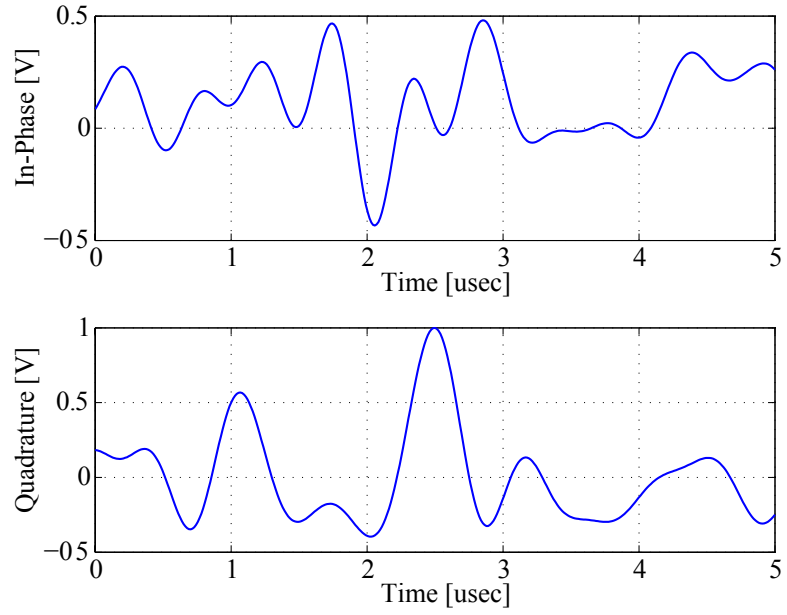
Probability Density Function – The PDF[24] for an ideal W-CDMA downlink signal is shown in Fig. 1.7(b), and indicates the likelihood of a given instantaneous modulated output power level. Technically the amplitude distribution of a quantized variable is called a probability mass function, but PDF is used in this work for consistency with literature.

Complementary Cumulative Distribution Function – The CCDF[25] for an ideal W-CDMA downlink signal is shown in Fig. 1.7(b), and indicates the likelihood that the instantaneous modulated output power will be higher than a given value.

[22] power spectral density
[23] occupied bandwidth
[24] probability density function
[25] complementary cumulative distribution function



(a)



(b)

Figure 1.6: Amplitude and phase (a), and in-phase and quadrature (b) components of a 5-μsec segment of a W-CDMA downlink signal.

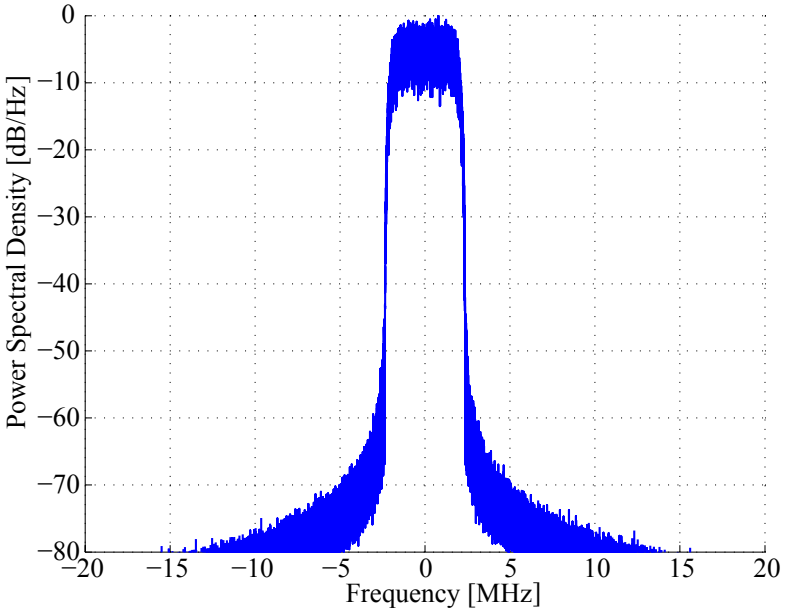
Peak-to-Average Ratio and Crest Factor – PAR was previously described based on the ratio of a single peak power value to the average power. In reality this value occurs very infrequently and can be difficult to measure with high precision. Instead PAR is defined henceforth as the ratio of power occurring at 0.01% CCDF to average power. CF[26] will retain the previous definition of PAR: absolute peak power to average power. Both metrics find distinct and important application in this work, but are elsewhere used interchangeably.

1.2.2 Linearity Metrics

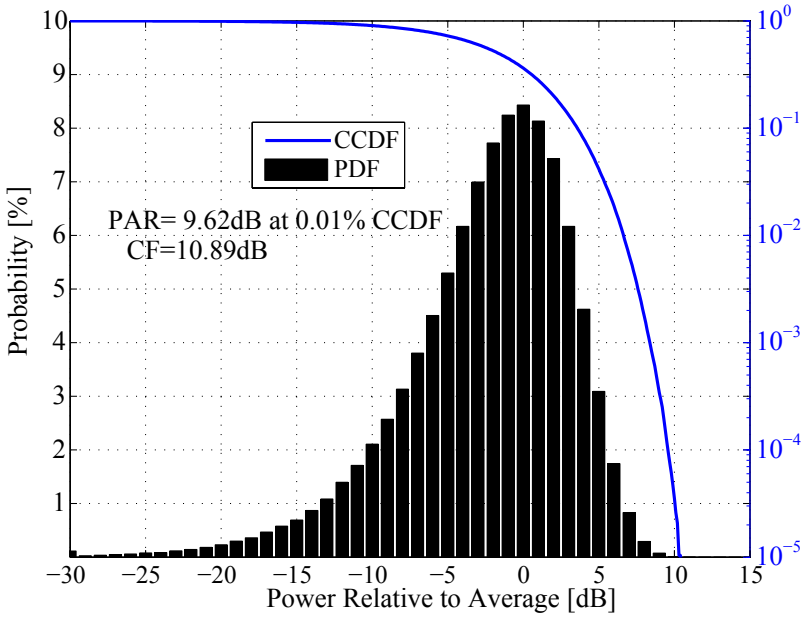
Performance specifications for W-CDMA base station transmitters are outlined by the 3GPP[27] standards organization in [32]. EVM[28] and ACP[29] are two linearity specifications which especially concern the power stage of a transmitter. These metrics define transmitter in-band and out-of-band linearity. Testing and limits for these metrics are precisely defined in [33], and [34] is an excellent high-level reference.

Error Vector Magnitude – EVM is a measure of the difference between the desired and transmitted IQ trajectory at each symbol time (red stars shown in Fig. 1.5). Before comparison, the transmitted waveform is first passed through a 3.84 MHz RRC[30] receive filter and processed using the same means available to a receiver: frequency, absolute phase, absolute amplitude, and chip clock timing adjustments to minimize EVM. Final EVM calculation consists of the ratio of RMS[31] error magnitude at each chipping instant to the RMS modulation amplitude. Limits in [32] set maximum EVM for W-CDMA base station transmitters at 17.5%.

[26] crest factor
[27] 3rd Generation Partnership Project
[28] error vector magnitude
[29] adjacent channel power
[30] root raised cosine
[31] root mean squared



(a)



(b)

Figure 1.7: PSD (a) and PDF (b) of an ideal W-CDMA downlink signal. Note the distinction between CF (10.9 dB) and PAR at 0.01% CCDF (9.6 dB).

Adjacent Channel Power – ACP, also sometimes referred to as ACLR[32], is the ratio of RRC filtered power centered on an adjacent channel relative to that in the desired channel. Power in adjacent channels can interfere with operation of other RF systems. Two adjacent channels are typically measured at offsets 5 MHz and 10 MHz above and below the desired carrier with a specified resolution bandwidth. Absolute maximum levels for the W-CDMA bases station application are set by [32] at 45 dBc and 50 dBc for a 5 MHz and 10 MHz offsets, respectively. The 5-MHz band can be called ACP1, or the adjacent channel, and the 10-MHz band can be called ACP2, or the alternate channel. Fig. 1.8 shows these channels overlaid on a W-CDMA PSD. The PSD is computed without spectral averaging to prevent main channel energy from bleeding into the adjacent channel.

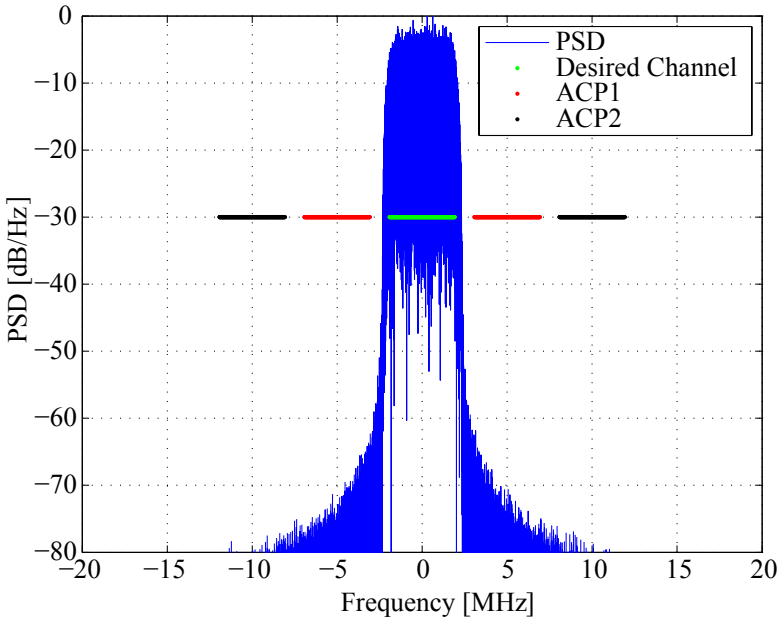


Figure 1.8: PSD computed with very little spectral averaging, providing the best estimate of ACP. Desired, adjacent (ACP1), and alternate (ACP2) channel bands are shown with green, red, and black bars.

[32] adjacent channel leakage ratio

Other transmitter-level linearity metrics, such as PCDE[33], are not relevant to performance of the power stage, or are easily met when the power stage achieves ACP requirements [35]. The reference also shows that, if the power stage meets ACP requirements it will also meet EVM requirements assuming typical PA distortion mechanisms (e.g. gain compression).

1.2.3 Test Signals

The W-CDMA downlink is highly reconfigurable, allowing transmission at varying data-rates to varying numbers of users. To standardize test conditions a set of six test models are defined in [33], each to be used for different base station conformance tests. Test Model 1 specifies spreading codes, relative power levels, and timing offsets for 64 user channels, representing a typical base station operating condition. This test model was used to generate the plots of Section 1.2.1 and will be used throughout this work.

Recall that average PA efficiency is a strong function of modulation PAR. As a result, significant work has been devoted to reducing the PAR of modulated signals while maintaining acceptable linearity. CFR algorithms add band-limited distortion to the original signal to reduce peak amplitude levels, and thus PAR, while maintaining acceptable linearity. Some degradation of linearity is expected, typically most evident in increased EVM.

The CFR algorithm used in this work is called RSPC[34] [36]. This algorithm was chosen for its relatively simple implementation and ability to be extended to multi-carrier modulation. PAR for the single-carrier W-CDMA Test Model 1 signal is reduced using RSPC from 9.8 dB PAR to 7.0 dB PAR with no increase in ACP and less than 5% increase in EVM. This increase in EVM is an acceptable degradation, as the decrease in PAR will allow increased average power and efficiency. In some cases a 2-3 dB reduction

[33] peak code domain error

[34] repeated scaled peak cancelation

of PAR can lead to reduced DC power consumption of 50% [10].

Because EVM at a certain PAR varies depending upon the CFR algorithm in use and its implementation, the impact of CFR on EVM measurements will be removed from transmitter linearity performance. Additive EVM is thus defined as the difference between EVM measured at the transmitter output and EVM of the desired signal. Throughout this work additive EVM will be assumed.

1.3 Thesis Organization and Contributions

The remainder of the thesis is divided into the following chapters. Original publications, workshop segments, courses, and disclosures concerning the material in each chapter are noted. A topical summary of contributions is presented in Chapter 6, along with a thesis summary and directions for future work.

Chapter 2: High-efficiency PA theory in this chapter provides a foundation for discussions of method and results in Chapters 3 and 4. Load line theory and reduce conduction angle operation are reviewed, providing context for two distinctly different high-efficiency PA techniques: (1) harmonic-tuned operation, in which harmonic energy is used to shape drain waveforms, and (2) switched-mode operation, a time-domain technique based on the approximation of the RF transistor as an ideal switch. Theory of operation, idealized performance, and practical pitfalls of each technique are discussed.

Chapter 3: Design methods for harmonic-tuned and switched-mode PA prototypes are discussed and developed with measured results. The non-ideality of high-power devices and lack of accurate nonlinear models forces the use of empirically-driven design to realize prototypes based on the theory of Chapter 2. Harmonic load pull is used to demonstrate a switched-mode class E 110-W LDMOS PA design at UHF[35] with 83% drain efficiency. A method involving analysis of package and device parasitic effects

[35] ultra high frequency

is presented to determine feasibility of high-efficiency operation at higher frequencies. Demonstration of the method results in a harmonic-tuned class F^{-1} 36-W GaN[36] PA design at S-band with 81% drain efficiency. Original contributions in the area of high-efficiency PA design techniques include the following:

- [37] An invited short course describing high-efficiency PA theory and load pull techniques. Results were also presented for a 6-W class E GaN HEMT PA prototype at 2.14 GHz achieving over 79% PAE.

- [38] [39] An invited workshop segment describing high-efficiency class E PA design and linearization techniques, and presenting a variety of prototypes from UHF to X-band.

- [40] A conference paper discussing characterization of a 65-W class E GaN HEMT transistor and measurements from a PA prototype at 370 MHz achieving 82% PAE.

- [6] A conference presentation discussing design of a 110 W class E LDMOS PA prototype at 360 MHz with 83% drain efficiency and 16 dB gain. A power combining strategy is presented for greater than 5 kW total power.

- [41] A conference presentation discussing class E PA design for a 449 MHz wind profiler radar system.

- [5] A conference paper and presentation discussing a oad-pull-based design method for UHF class E PAs utilizing a power-efficiency optimization metric. Results are presented for four different prototypes of varying device technology.

- [2] A conference paper and presentation discussing a new methodology for high-efficiency design at S-band using fundamental-frequency tuners and including analysis of high-efficiency feasibility for a given transistor and microwave package. A

[36] gallium nitride

example 36-W GaN HEMT class F^{-1} design is presented with 81% drain efficiency and 14.5 dB gain at 2.14 GHz.

Chapter 4: PA drain supply modulation is introduced as a method of achieving high-efficiency performance for high-PAR signals. General requirements are outlined for the PA and drain supply circuit components. An ET architecture is presented which allows a tradeoff between system efficiency and linearity using the "signal split". Finally, a measurement-based system analysis method is developed which clearly shows the impact of the signal split, and also component non-idealities, on system performance. Original contributions in the area of general supply modulation include the following:

- [42] A conference paper and presentation describing a measurement-based ET system analysis method used to illustrate the usefulness of the signal split to trade system efficiency vs. linearity, and also to determine EM fidelity requirements.
- [23] A conference paper and poster concerning the tradeoff between efficiency and linearity of an X-band digital polar transmitter under load pull conditions.
- [43] An intellectual property disclosure concerning a low-parasitic PA-EM interconnect.
- [44] An intellectual property disclosure describing measurement methods for PA characterization data used to predict ET system performance.

Chapter 5: An automated testbed is developed to demonstrate proof of concepts in Chapter 4. Commercial test and measurement equipment is employed for signal generation and capture, and custom MATLAB scripting is used to implement signal processing. Linearization algorithms are investigated and applied, targeting specific distortion mechanisms. The final system exhibits over 50% system PAE with a 40-W PEP 7 dB PAR W-CDMA test signal with excellent linearity. Original contributions in the area of envelope tracking and system integration include:

- [45] A conference presentation discussing integration of a signal split to optimize PA efficiency with a polynomial-based digital pre-distortion algorithm.

- [46] An intellectual property disclosure concerning methods of V_{dd}-$\tilde{v}_{in}$ time alignment.

- [47] A conference presentation discussing the benefits of ET architecture in radar applications.

- An invited follow-on article for a special issue of *Microwave Theory and Techniques* elaborating on the high-efficiency S-band PA design techniques and results presented in [2], and also including integration of the prototype into the ET system.

- [48] A four-part invited course spanning the areas of active devices, PA theory, high-efficiency PA design techniques, load pull methods, digital pre-distortion, general supply modulation, and the envelope tracking architecture developed in this thesis, including concepts, methods, and results.

Chapter 6: Performance of the ET system is compared to that of traditional drive modulation, clearly demonstrating the benefits of the ET architecture described in Chapter 5. The contributions of this thesis are summarized, followed by discussion of future work and applications.

Chapter 2

High-Efficiency PA Theory

Contents

This chapter provides background and theoretical basis for the design of power amplifiers, and in particular the high-efficiency PA designs presented in Chapter 3. The chapter begins with a brief discussion of high-power microwave transistors and basic PA operation followed by three approaches for achieving high PA efficiency: reduced conduction angle, harmonic-tuned, and switched-mode operation. The relevant classes of operation in each theory are discussed along with the benefits and pitfalls of each.

The following is intended to provide theoretical context for Chapters 3-6. The interested reader is referred to the following comprehensive treatments for more information:

- Bahl [49], for a complete overview of theory, implementation, and practical issues

involved in many types of amplifier design running the gamut of frequency, power, and technology.

- Krauss [1], for a long-standing and concise description of PA fundamental concepts.
- Schwierz [50], for an understanding of device technology, advantages, and limitations, including more recent advances in technology.
- Cripps [21], for an insightful, more advanced discussion of theory and design issues for all types of PAs.

The complexities of high-power microwave transistors in high-efficiency operation are not adequately reproduced by many nonlinear models or rigorous theoretical treatments, leading to measurement-driven PA design methods described in Chapter 3. A deep understanding of the theory and underlying transistor behavior is necessary to develop and make appropriate use of such methods.

2.1 High-Power Microwave Transistors

Design of high-efficiency PAs begins with consideration of the active device, a simplified model of which is shown in Fig. 2.1. FETs are more common than BJTs in high-power RF applications and are the only type of device considered throughout this work. Furthermore, microwave devices are almost exclusively used in common-source configuration.

The impedance presented to the current source at plane P1 in the model of Fig. 2.1 is denoted $Z_{ds,1}$. This is the impedance critical in PA design and analysis. Reference planes P2 and P3 are also defined because their impedances can be more easily measured. The parameters in this model can be extracted from small-signal S-parameters [51], provided that S-parameters are measured inside the package reference plane. The total output

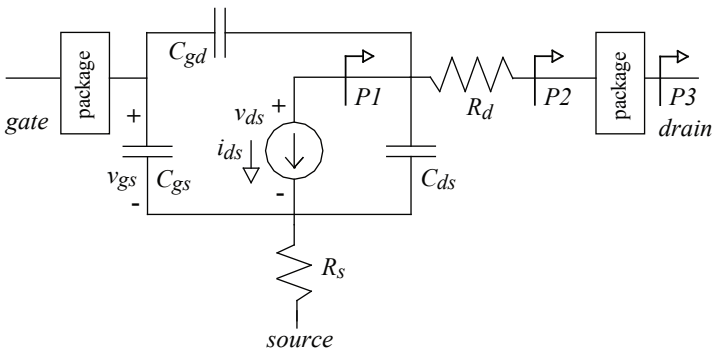


Figure 2.1: First order model of a FET. Important output-side reference planes are denoted P1, P2, and P3.

capacitance is calculated as:

$$C_{out} = C_{ds} + C_{gd}||C_{gs} \tag{2.1}$$

The FET is most simply described as a voltage-controlled current source. In the case of enhancement-mode devices, such as the LDMOS transistor, a positive gate voltage v_{gs} is required to enhance the channel below the gate, allowing current to flow from the drain terminal to source terminal. Depletion-mode devices, for example HEMTs[1], require negative voltage to deplete the channel thus preventing current flow. N-type devices are dominant in microwave power amplifier applications. A cross-section for a high-power LDMOS microwave transistor is shown in Fig. 2.2.

LDMOS devices for high-power microwave applications are slightly modified from

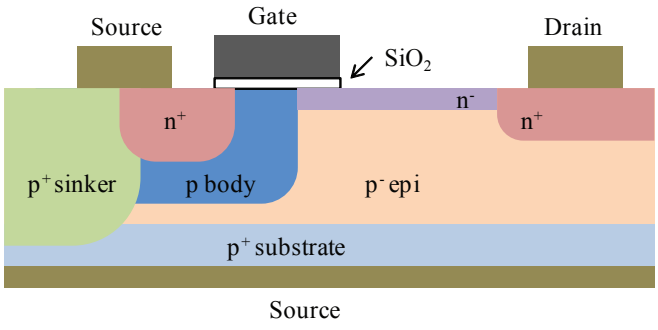


Figure 2.2: Cross section of a high-power LDMOS microwave transistor.

[1] high electron mobility transistors

traditional MOS[2] structures. A lightly doped drain region n^- separates the drain terminal from gate and source terminals, increasing breakdown voltage [50]. The channel is formed by a p-type region directly beneath the gate, and is considerably shorter than the gate length. High-power LDMOS device technology is currently viable for class AB applications up to 2.5 GHz and with power exceeding 100 W from a single transistor. LDMOS technology is mature, inexpensive, and dominates the cell-phone base station market as well as many other infrastructure applications in that frequency range [52].

It will be shown in this chapter and the next that LDMOS lacks the performance necessary for high-efficiency operation at S-band, requiring the use of alternate technology. HEMTs built on wide-bandgap semiconductor materials will be discussed in the next chapter along with high-efficiency design examples using Si[3] LDMOS at UHF and GaN HEMT at S-band.

2.2 Load Line and Bias

A general PA block diagram is shown in Fig. 2.3. Input and output terminals are always 50 Ω. DC bias is supplied to the gate and drain via bias tees, represented in the figure by a DC blocking capacitor and an RF choke. Chokes are assumed to be ideal such that currents I_{gg} and I_{dd} do not vary at the RF frequency. The same reference planes are noted as in Fig. 2.1, but a simpler equivalent circuit represents the active device. In most PA analysis R_{on} is neglected and C_{ds}, C_{gs}, and C_{gd} are combined into C_{out} using Eqn. 2.1.

Fig. 2.4 shows the DC operation of a FET, commonly referred to as IV curves. A DC bias (V_{dd} and I_{dq}, set by V_{gg}) is applied to the device, referred to as the quiescent bias point. Increasing v_{gs} beyond a minimum value V_{pinch} causes linearly increased i_{ds}. Above some maximum value of v_{gs} the channel is saturated and i_{ds} cannot increase any

[2] metal oxide semiconductor

[3] silicon

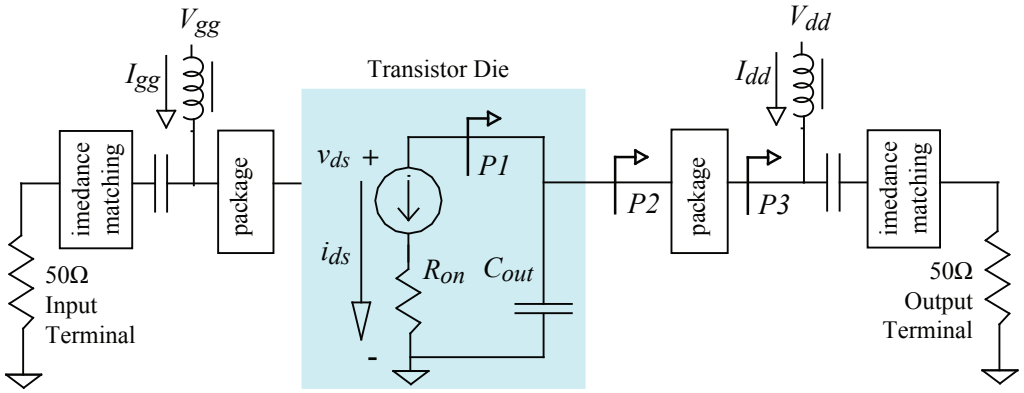


Figure 2.3: PA block diagram showing bias, matching, and important reference planes.

further, converging to a value I_{max}. v_{ds} exceeding V_{break} causes drain-source breakdown. V_k is called the knee voltage, below which maximum current I_{max} cannot be achieved.

The quiescent bias point is set by the voltages V_{dd} and V_{gg}, resulting in some quiescent current I_{dq}. The RF input signal varies v_{gs} around its DC value of V_{gg}, resulting in subsequent variation in i_{ds}. Assuming a purely real load impedance at P1, called R_L, the current variation will result in linearly related drain-source voltage and current. The i_{ds} vs. v_{ds} trajectory, or load line, has slope equal to the inverse of R_L.

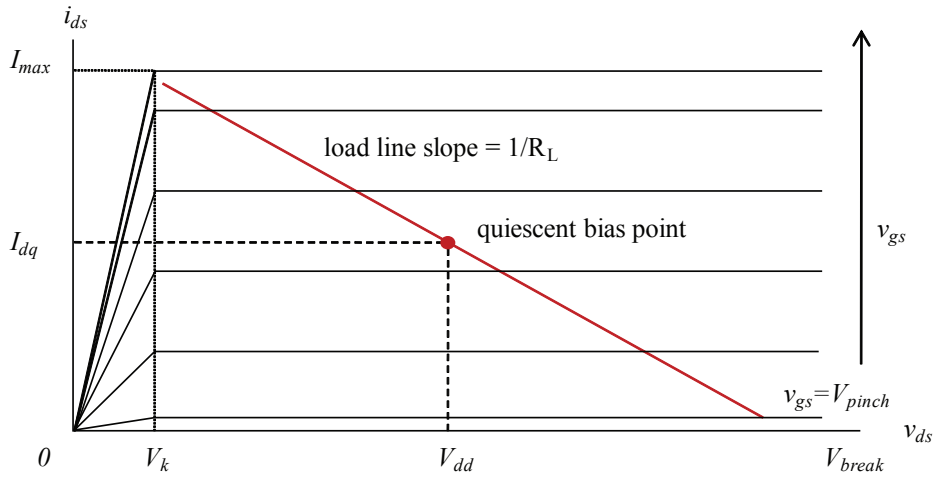


Figure 2.4: Idealized IV curves for a FET transistor showing a class A bias point and load line.

Amplifier design using a small-signal conjugate match aims to extract maximum gain from a device. In large-signal PA design the goal is to extract maximum power at the expense of gain. The load impedance is designed to achieve maximum voltage and current excursion on the same load line, resulting in maximum output power.

Class A bias requires that I_{dq} is set to 50% I_{max}. Given a recommended value of V_{dd} (typically about $V_{break}/2.5$ [50]), the load required to achieve I_{max} can be calculated:

$$R_L = \frac{(V_{dd} - V_k) \cdot 2}{I_{max}} \tag{2.2}$$

It is important to recall that this load resistance must be presented to the transconductance at P1, also called the virtual drain. All PA analysis and theory is based at this reference plane. Simultaneous voltage across (v_{ds}) and current through (i_{ds}) the virtual drain is the primary source of power dissipation in a PA. High-power devices are constructed by placing many unit cell transistors in parallel. Based on Fig. 2.1 we conclude that a higher-power version of the same transistor will have increased C_{out}, increased I_{max}, and thus reduced R_L.

Drain efficiency of a theoretical PA can be calculated based on drain waveforms shown in Fig. 2.5:

$$\eta = \frac{P_{out,f_o}}{P_{dd}} = \frac{v_{ds,f_o} \cdot i_{ds,f_o}}{V_{ds,DC} \cdot I_{ds,DC}} \tag{2.3}$$

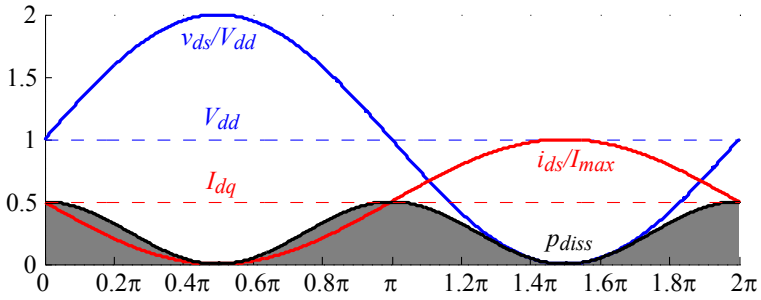


Figure 2.5: Class A drain voltage and current waveforms.

For the case of the class A bias point, the consumed power is constant ($V_{dd} \cdot I_{dq}$) over the whole range of output power, and the maximum output power is $V_{dd}/\sqrt{2} \cdot I_{dq}/\sqrt{2}$, resulting in 50% efficiency at maximum output power. Efficiency degrades linearly with reduced output power, to only 10% when output power is 7 dB less than maximum.

Another way to evaluate efficiency is by observing the amount of overlap in drain voltage and current waveforms. Simultaneous voltage across and current through a current source results in power generation or dissipation, depending upon the sign. Note that in Fig. 2.5 the $i_{ds} \cdot v_{ds}$ product is always non-zero except for the instants when voltage or current itself is zero. Instantaneous power dissipated is indicated by the black line in Fig. 2.5.

The class A PA is linear to the degree that the transconductance is linear - that is, a reduction in input power leads to a linearly proportional reduction in output power. High-efficiency modes of operation use the transistor in saturation and cutoff, sacrificing gain linearity for increased efficiency.

2.3 Reduced Conduction Angle PAs

High efficiency operation has traditionally been achieved through the use of reduced conduction angle PAs. These modes of operation reduce quiescent current to less than the class A 50% I_{max}, preventing conduction through the current source for some fraction of the RF period. When the transistor does not conduct it is said to be in "cutoff". The length of time (in radians) when the transistor is conducting current during each RF cycle is called the conduction angle α.

2.3.1 Class AB, B, and C Operation

Allowing the transistor to enter cutoff leads to non-sinusoidal drain waveforms with frequency content at harmonics of the fundamental frequency. Traditional reduced-

conduction angle classes of operation (AB, B, C) require that a short circuit is presented to the current source at harmonic impedances [1]. A harmonic short circuit causes harmonic voltage to be zero (leading to fundamental-frequency sinusoidal drain voltage waveforms) while allowing the drain current waveform to contain harmonic energy.

The conduction angle (α) is defined as the portion of the RF cycle during which current i_{ds} is allowed to flow, achieved by reducing the value of I_{dq} relative to I_{max}. Class AB bias requires α between 2π and π, class B bias requires α equal to π, and class C bias requires α less than π. Class AB, B, and C drain waveforms are shown in Fig. 2.6.

Note (visually) that in all cases the amount of drain voltage-current overlap is significantly reduced from the class A waveforms of Fig. 2.5, leading to reduced dissipation in the transistor current source. Input power requirements and resulting fundamental frequency output power are also different in each case.

Efficiency of ideal reduced conduction angle modes can be calculated using Eqn. 2.3, approximating the half-rectified sine wave drain current as a function of α. The DC component of i_{ds} can be reduced to:

$$i_{ds,DC} = \frac{1}{2\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot d\theta \tag{2.4}$$

$$i_{ds,DC} = \frac{I_{max}}{2\pi} \cdot \frac{2 \cdot \sin(\alpha/2) - \alpha \cdot \cos(\alpha/2)}{1 - \cos(\alpha/2)} \tag{2.5}$$

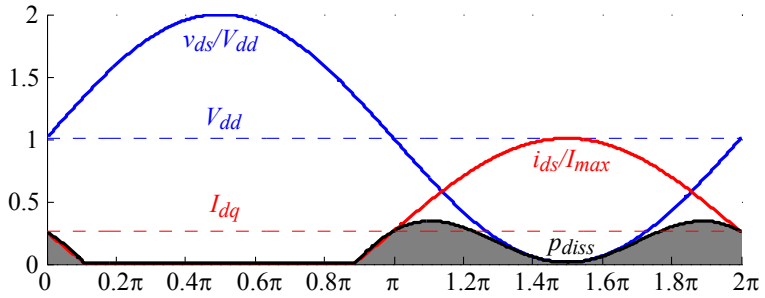
The harmonic components of i_{ds} can be expressed as:

$$i_{ds,f_n} = \frac{1}{\pi} \cdot \int_{-\alpha/2}^{\alpha/2} \frac{I_{max}}{1 - \cos(\alpha/2)} \cdot (\cos\theta - \cos(\alpha/2)) \cdot \cos n\theta d\theta \tag{2.6}$$

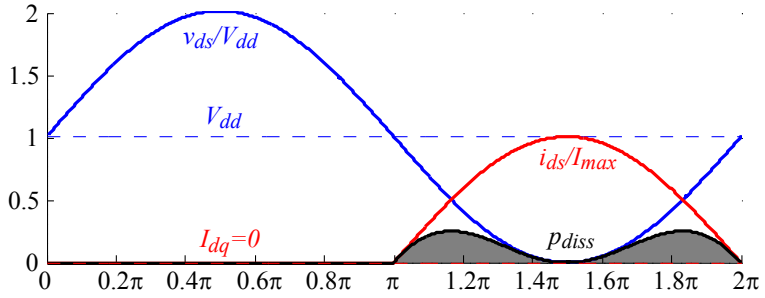
Of primary importance for power and efficiency calculations is the fundamental frequency component of i_{ds}, which can be simplified to:

$$i_{ds,f_0} = \frac{I_{max}}{2\pi} \cdot \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)} \tag{2.7}$$

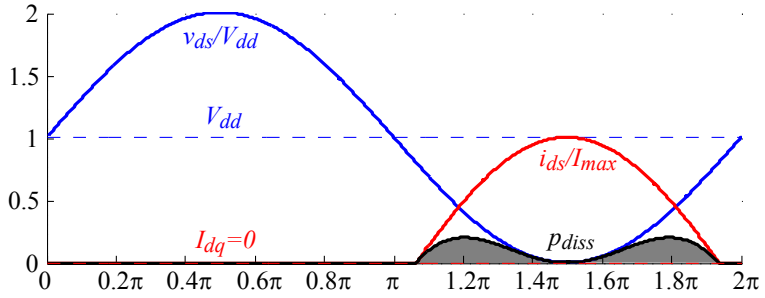
In the case of class B operation the DC component of i_{ds} is I_{max}/π while the fundamental frequency component of i_{ds} is $I_{max}/2$. Output power is thus equal to the class



(a)



(b)



(c)

Figure 2.6: Class AB with $\alpha = 1.2\pi$ (a), class B with $\alpha = \pi$ (b), and class C with $\alpha = 0.8\pi$ (c) drain voltage and current waveforms. Instantaneous dissipated power is shown in black on all plots.

A case while DC power is reduced by a factor of $\pi/2$, resulting in an ideal class B efficiency of $\pi/4$, or 78.5%. This increase in efficiency, however, is not without cost. Twice the gate voltage swing, an increase of in 6 dB input power, is required as compared to class A, though the same maximum output power is achieved. Therefore ideal class B operation has 6 dB less gain than class A at peak output power.

Fig. 2.7 shows efficiency and relative output power for changing conduction angle.

Notice that class C approaches 100% efficiency only as output power drops to zero.

The reduced conduction angle modes of operation lack linearity that was intrinsic to the class A mode. Even so, the class AB PA is the most dominant design for high-power communications applications today [49].

2.3.2 Overdriven PAs

Previous analysis assumes v_{gs} is sufficient to achieve i_{ds} equal to I_{max}, but no more. Input "overdrive" causes the transistor to operate in current saturation, the region above which increased v_{gs} no longer produces increased i_{ds}. Increased input drive results in increased output power, but dissipated power remains nearly constant (i_{ds}-v_{ds} overlap does not increase notably). Overdriven class B drain waveforms are shown in Fig. 2.8.

Even more significant harmonic content is introduced, and gain is reduced (input power rises faster than output power). An analysis of overdriven class B is presented in [53], demonstrating theoretical efficiency well above that of the unsaturated class B PA. Cripps [21] describes an analysis similar to the result of Fig. 2.7 detailing the efficiency

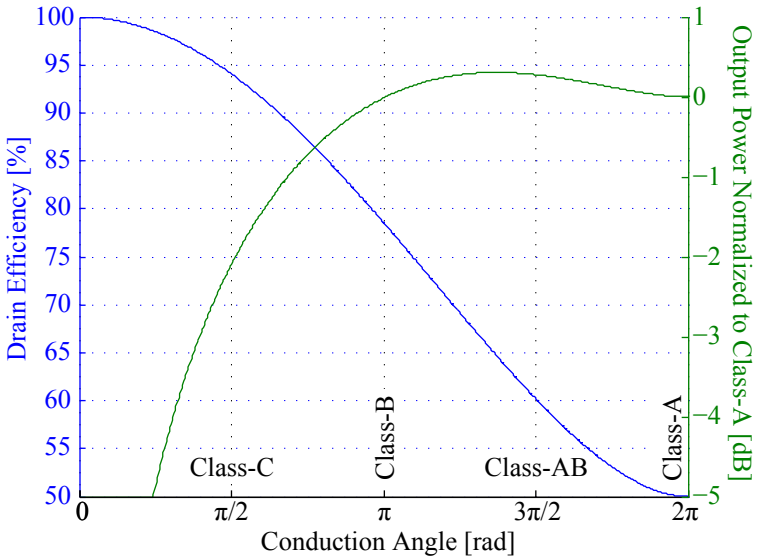


Figure 2.7: Theoretical efficiency and output power for reduced conduction angle modes of operation.

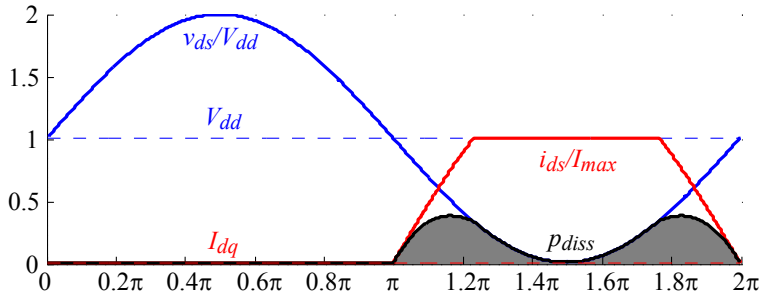


Figure 2.8: Overdriven class B drain voltage and current waveforms.

and power trends for reduced conduction PAs at varying levels of overdrive.

Many practical PA designs make use of overdrive. Performance is often specified at the P1dB and P3dB operating points, indicating that the PA is overdriven to compress gain by 1 dB or 3 dB as compared to gain in linear operation. Compression and saturation are frequently used interchangeably, but have very different meanings. Gain compression describes power gain of the PA at a given input power level, while current saturation refers to a condition in which the transistor cannot source more current. Gain compression can be caused by many factors, one of which is current saturation.

2.3.3 Practical Issues

Theoretical analysis is a very useful tool in understanding and synthesizing PA behavior. Throughout literature many complexities of high-power transistors and PA implementation are neglected or approximated to make such analysis analytically tractable. Design of actual hardware, however, involves many non-ideal effects that are difficult to account for in theory.

The requirement for harmonic impedance terminations is seldom enforced in modern-day PA design [21]. Short circuit harmonic impedance terminations make analysis simple by forcing fundamental frequency sinusoidal drain voltage waveforms, but are difficult to realize depending upon device parameters, frequency of operation, and parasitic package effects (discussed in detail in Chapter 3). The next section will discuss

methods of increasing PA efficiency by presenting alternate impedances at harmonic frequencies with the intention of shaping drain voltage and current waveforms to avoid power dissipation.

The efficiency analysis supposes that the knee voltage V_k is very small compared to the drain supply voltage. In reality, many high power transistors have significant knee voltage on the order of 4 V to 7 V compared to drain supply voltage of 28 V or 32 V. Implementation of the PA described by theory requires an increase in drain supply voltage to keep the load line above the knee voltage. An increase in DC supply voltage reduces efficiency of the class AB PA to the following:

$$\eta_{knee} = \frac{V_{dd} - V_k}{V_{dd}} \tag{2.8}$$

In this case the drain current waveform is no longer a rectified sine shape due to reduced current when drain voltage is below V_k. The resulting "bifurcated" shape is more difficult to analyze, as shown in Fig. 2.9. Reduced fundamental-frequency current reduces output power.

Current waveform bifurcation due to the knee voltage can be an advantage in terms of the harmonic-tuned PAs discussed in the next section. An approximate analysis of load lines below knee voltage is presented in the literature (e.g. [49]).

An alternative way to look at loss due to knee region is in terms of R_{on}, the total resistance encountered by i_{ds}. R_{on} includes drain and source resistance and also the

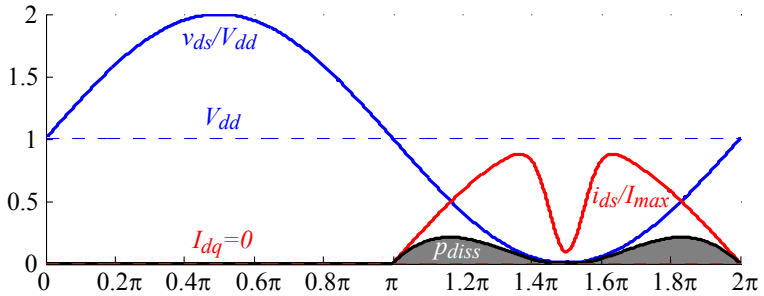


Figure 2.9: Class B drain voltage and current waveforms assuming realistic knee behavior.

effective resistance of the transconductance saturation effect [1]. This resistance leads to a voltage drop with high current, and largely defines the slope of the IV curves below V_{knee}. The impact of this loss on efficiency can be calculated as follows:

$$\eta_{R_{on}} = \frac{1}{1 + \psi \frac{R_{on}}{R_L}} \tag{2.9}$$

Different classes of amplifiers use varying values of ψ to account for different theoretical i_{ds} waveform shapes. For class B operation $\psi = 2$, while in class E operation (discussed later in this chapter) $\psi = 1.365$. Also note that the efficiency reduction is made worse when R_L is small, as is the case with high-power transistors. [54] suggests that $\psi = 1.365^2$ can be considered a practical upper-bound on PA efficiency given finite on-resistance. Maximum possible efficiency due to on-resistance is a useful figure of merit in comparing transistors for high-efficiency applications, independent of operating mode.

Drive power requirements can become a significant factor in high-efficiency designs. An additional 6 dB input power required for class B may result in unacceptably low gain, despite the resulting efficiency enhancement. Output power reduction carries the same concern: despite drain efficiency over 90% a class C PA may be unacceptable due to a 5 dB output power reduction as compared to class A output power.

High power transistors are formed by the parallel combination of many unit cells and therefore typically have small R_L and large C_{out}. Recall from Fig. 2.1 that the ideal load line R_L must be presented at P1. Thus the impedance match at P2 must be designed to include the effect of the output capacitance. Large values of C_{out} lead to high-Q matching requirements and further reduced impedance at P2. Sub-ohm output matching is not uncommon for a 100-W LDMOS transistors, resulting in very high impedance transformation ratio and significant matching network losses. [49] includes an analysis for distributed and lumped matching network losses given the quality factor of the matching components.

Many transistors are packaged with internal matching components to achieve matching with lower loss and broader bandwidth [18], as shown in Fig. 2.10.

Matching networks can be easily formed by series bond wire inductance and shunt chip capacitance. Internal input and output matching networks raise the impedance at P2 over a desired bandwidth but limit the packaged transistor's usefulness outside of the intended band. Such internal networks also limit the PA designer's ability to control harmonic impedances required for high-efficiency modes of operation, discussed in the next section.

Stability is difficult to analyze and predict in high-power large-signal operation. As mentioned previously, small-signal S-parameter techniques cannot be used due to the nonlinear operating point. In practice, stability is dealt with by (1) mismatching the source to reduce gain, (2) adding a resistive input or output termination at the frequency of oscillation, or (3) improving bias network design. Inadequate low-frequency termination of bias networks is perhaps the most prevalent source of instability for high-power UHF to S-band PA designs.

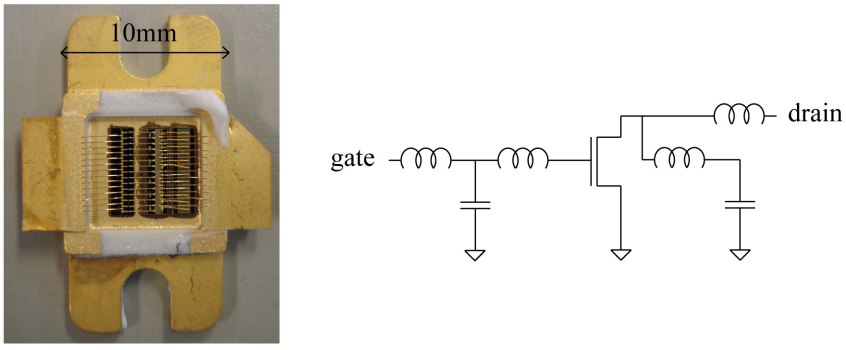


Figure 2.10: A packaged 45-W LDMOS transistor with internal prematching. Active device is the center die. Bond wire inductance is used with a shunt capacitor die on either side of the active device to form internal input and output matching networks.

2.4 Harmonic-Tuned PAs

Recall that a short at P1 for all harmonic frequencies is required for ideal classes A, AB, B, and C. This constraint forces v_{ds} to remain sinusoidal (no harmonic voltage can be produced across a short) but allows harmonic components to exist in i_{ds}, changing the shape of the drain current waveform to a half rectified sine wave. Power dissipation in the current source is reduced and even eliminated by shaping v_{ds} and i_{ds} to avoid overlap in time (e.g. class C) at the expense of fundamental frequency output power and gain. In this section other drain voltage and current waveform shapes are discussed which reduce power dissipation without the downfalls of class C.

2.4.1 Wave Shaping

The time harmonic nature of PA operation limits the designer's ability to arbitrarily change the shape of drain waveforms. The only means available is the addition of harmonic energy to the fundamental voltage and current waveforms. We assume for now that harmonic voltage and current energy is available, and can be either added or eliminated by presenting appropriate harmonic impedance at the virtual drain.

Ability to shape current and voltage drain waveforms creates many possibilities for high-efficiency operation. Harmonic impedances can be used to generate specific combinations of voltage and current wave shapes which avoid overlap but still result in high output power at the fundamental frequency. Many well-known configurations [1] are analyzed in literature, along with theoretical exploration [55] of other possible configurations, many of which are used less frequently for practical reasons. The harmonic terminations in these cases are limited to "open" or "short". If this condition is met there cannot be both harmonic voltage and current at the load, effectively suppressing harmonic output power.

Cripps [21] suggests that many supposed class AB designs actually have capacitive

harmonic terminations, in which the transistor's own output capacitance approximates nearly a short circuit. Theory for a new mode of operation is developed based on such harmonic terminations and a reactive load impedance. The class J mode of operation [56] has been used to achieve high efficiency (12 W with over 81% at 2.1 GHz) over a broad bandwidth. Harmonic-tuned amplifier design in this work is limited to the more traditional classes F and F^{-1} (class F-inverse).

2.4.2 Class-F and -F^{-1}

The class F mode of operation was invented by Tyler [57]. An open circuit is presented at odd harmonics while a short circuit is presented at even harmonics. The presence of only odd-harmonic voltage is used to synthesize a square wave, and the even-harmonic current causes current peaking as shown in Fig 2.11. Theory [58] and measurement [59] have shown increased efficiency and output power under compressed operation for a broad range of applications up to S-band [60].

In reality the ideal waveforms of Fig. 2.11 cannot be realized, as infinite harmonic content and control would be required. An approximation of the square wave can be achieved using only 3rd harmonic voltage content, where the resulting shape depends upon the relative magnitude of the 3rd harmonic component, as shown in Fig. 2.12.

A maximally flat voltage waveform (e.g. $v_{ds,3f_o}/v_{ds,f_o} = 1/9$ for only 2nd and 3rd harmonic terminations) results in class F operation by definition. An analysis in

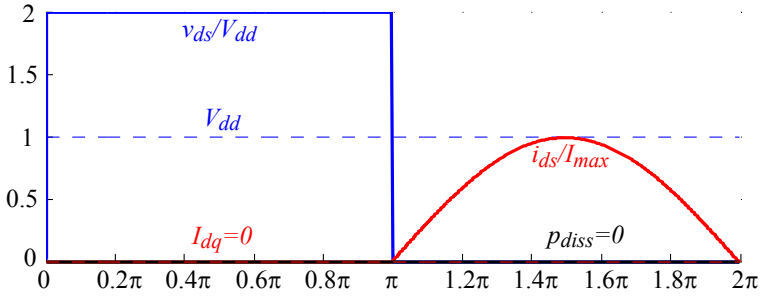


Figure 2.11: Ideal class F drain voltage and current waveforms.

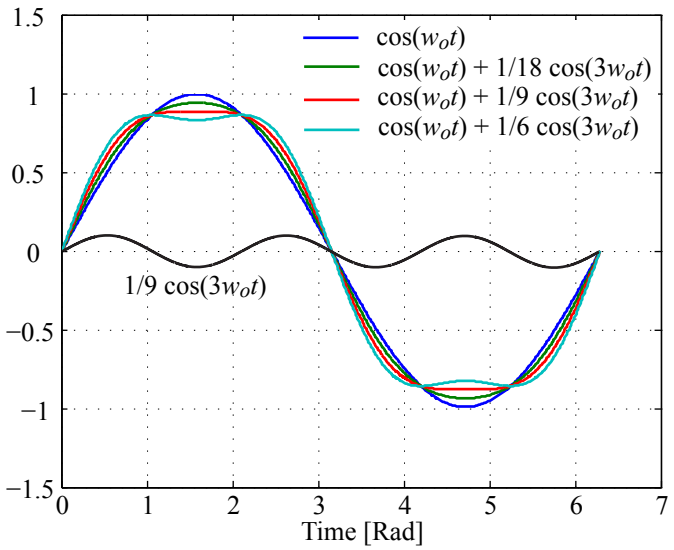


Figure 2.12: Sine wave with addition of a 3rd harmonic component of various relative amplitudes.

[61] explores the range of waveform shapes possible with varying relative harmonic amplitudes, and provides expressions for resulting power and efficiency gains. As a result of imperfect squaring, the optimum efficiency for the 3rd harmonic case is 88.4%, with a 0.5 dB increase in output power as compared to class B. Class F waveforms considering only 2nd and 3rd harmonic content are shown in Fig. 2.13.

As additional harmonics are considered (5th, 7th, etc) further theoretical efficiency and power gains are observed [62]. Consideration of the 5th harmonic yields 94.8% efficiency and a 0.82 dB increase in output power compared to class B.

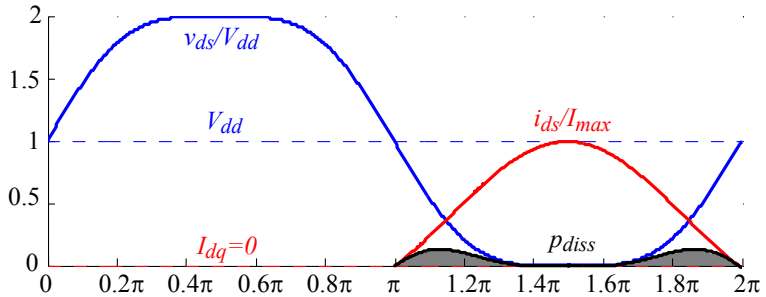


Figure 2.13: Class F drain voltage and current waveforms assuming only 2nd and 3rd harmonic termination.

Class F^{-1} [63] reverses the even and odd harmonic terminations to achieve current squaring and voltage peaking. As compared to class F, higher v_{ds} peaks and lower i_{ds} peaks are expected (relative to V_{dd} and I_{dd}). Higher peak voltage is undesirable, requiring careful attention to drain-source breakdown. However, lower current peaks cause reduced degradation in efficiency with increasing R_{on} [64], and theoretical fundamental load impedance is also higher. Expressions for fundamental load impedance of class F and class F^{-1} and a comparison of efficiency degradation with R_{on} can be found in [59]. Higher fundamental load impedance results in lower transformation ratios and reduced matching circuit losses. Further practical reasons making class F^{-1} desirable will be discussed in the next section.

2.4.3 Practical Issues

Addition of even harmonics creates a result with larger amplitude than the original fundamental waveform. In-phase addition of even voltage harmonic components can result in larger-than-intended peak v_{ds}, nearing V_{break}. With short circuit harmonic termination (as required for class AB), the peak v_{ds} should be no greater than $2V_{dd}$, but practical class AB amplifiers do not often enforce 2nd and 4th harmonic short circuit terminations. As a result, drain supply voltage is commonly limited to $V_{break}/2.5$ [50]. The problem of voltage breakdown is even more pronounced for classes of high-efficiency operation requiring open circuit terminations at even harmonics. A reduction of V_{dd} prevents breakdown but also reduces output power, a common tradeoff in high-efficiency design.

Matching circuits become impractical, sensitive, and lossy as the number of harmonics under consideration rises. Control of higher harmonic impedances is further complicated by the nature of high-power microwave transistors. Large package parasitic effects and output capacitance must be absorbed into the matching network to present the correct impedance at the intrinsic drain (plane P1).

The active device must be capable of producing harmonic content. Low gain at harmonics and high output capacitance limit the harmonic content available to be shaped by harmonic impedance. For example, a high-performance 100-W LDMOS microwave device performs well in class AB mode at 2 GHz but has inadequate performance at 4 GHz and 6 GHz for harmonic-tuned operation.

The efficiency enhancement benefit of harmonic tuning is only realized when the PA operates in compression. Until the device operates in saturation or cutoff there can be no harmonic energy generated. Furthermore, the amplitude of harmonic content relative to that of the fundamental content is very difficult to predict and accurately control. Variation of I_{dq}, drive level, and fundamental load impedance will produce a wide range of harmonic content.

The knee voltage effect is a source of significant harmonic content. Consider a fundamental load and drive level which forces v_{ds} below the knee voltage in each RF cycle. The typical half-sinusoid i_{ds} current waveform will be "bifurcated", naturally generating large amounts of 3rd harmonic drain current as shown in Fig. 2.9. This behavior proves even more beneficial for current-squaring class F^{-1}, where a large 3rd harmonic component can be difficult to achieve at high fundamental frequencies.

It is more difficult to present an open at plane P1 than it is to present a short. A short at plane P2 is in parallel with the output capacitance and results in a short at plane P1 regardless of the value of C_{out}. An open at plane P2 presents an open in parallel with C_{out} (a capacitive termination) at plane P1. Presenting an open at P1 requires that C_{out} be accurately estimated and resonated with an inductance at plane P2, resulting in an open termination at P1. This becomes a challenge as C_{out} becomes larger resulting in a more sensitive high-Q resonance.

In the same vein, higher frequency harmonic open circuits are more difficult to realize than lower frequency harmonic terminations. The same value of C_{out} incurs a larger reactance with increasing frequency, dominating the impedance at plane P1 to an

ever larger degree and approximating a short. When terminating only two harmonics, Class F^{-1} is more practically realizable than class F because it requires an open circuit termination at the 2nd harmonic rather than the 3rd harmonic.

Throughout this section, and literature also, harmonics are said to be terminated in an "open" or "short". In reality a perfect open or short is impossible to achieve, leading to the question: how low or high must an impedance be to produce the desired waveform shaping effect? [62] addresses this question by analyzing 2nd and 3rd harmonic termination impedances as a continuum, and with respect to the fundamental load impedance. Reactances of $0.3R_L$ and $3R_L$ are stated as approximate transitions between short, resistive, and open terminations for harmonic-tuned classes. [21] also notes that, when considering 2nd and 3rd harmonic class F with a realistic knee voltage model, the resistance of the 3rd harmonic short needs only to be "reasonably smaller" than the fundamental load. In this work the criteria has been adopted that open and short terminations have $R_{f_n} > 3R_L$ and $R_{f_n} < 0.3R_L$.

2.5 Switched-Mode PAs

Switched modes of amplification are fundamentally different from those based on load line theory and the harmonic-tuned modes described in the previous section. Instead of a current source with linear transconductance the transistor is modeled as an ideal switch, eliminating all notion of load lines and DC bias. Instead of the frequency-domain wave shaping used in harmonic-tuned PAs, switched-mode theory shapes waves by directly controlling time-domain voltage and current transients after a change in switch state.

The ideal switch is always in one of two states: completely on - a perfect short circuit, or completely off - a perfect open, and can move between the two states instantaneously. Switched-mode circuits are very popular in DC-DC conversion applications [65], but at microwave frequencies it is difficult to identify transistors that can be approximated as

a switch. A number of criteria must be satisfied for the switched-mode assumption:

- The transistor must be biased at cutoff (class B) to prevent current from flowing when the switch is off.
- Input drive level must be large to transition from cutoff to saturation (just as a switch transitions from completely off to completely on) very quickly.
- The transistor must have gain at many harmonics of the fundamental to allow for fast transitions between off and on states.

The simplest switching amplifier consists of an ideal switch connected to a load by an ideal DC blocking capacitor and is fed with constant current through a DC choke and driven at a 50% duty cycle. Such an amplifier is shown in Fig. 2.14 and produces drain waveforms shown in Fig. 2.15.

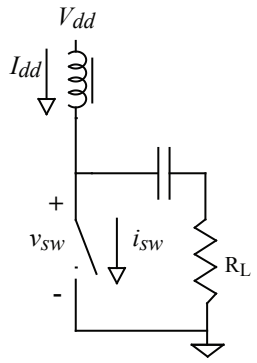


Figure 2.14: Schematic representation of a simple switching amplifier.

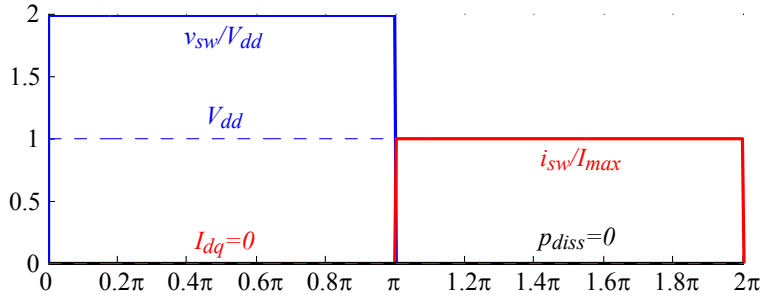


Figure 2.15: Drain voltage and current waveforms for a simple switching amplifier.

The ideal simple switching amplifier avoids power dissipation in the switch, making the DC-RF conversion 100% efficient. However, almost 20% of the RF energy delivered to the load is at harmonic frequencies. The maximum drain efficiency (defined in Chapter 1 to include only power at the fundamental frequency) is just over 80%. This example illustrates the need for a harmonic tuning network between the output of a switched-mode amplifier and the load.

Other problems with the concept illustrated in 2.14 include the output capacitance inherent in semiconductor devices. A realizable switching amplifier must include the output capacitance shunting the switch. Other classes of switching amplifiers include D, E, and S. Class D is frequently used in analog applications at much lower frequencies, and requires two transistors driven in a complementary fashion [1]. Square voltage and current switch waveforms result in ideally 100% efficiency and an output network removes harmonics to restore sinusoidal load voltage and current. Common-source configuration is preferred at UHF and higher RF frequencies to enhance stability, so class D has found limited application in this frequency range.

Class S makes use of pulse width modulation to control the load voltage amplitude [1]. As in class D, complementary transistor configuration is required along with switching frequencies many times higher than the fundamental frequency. These factors make class S impractical for the carrier frequencies used in this work.

2.5.1 Class E

Like other switched modes, class E was invented for very low frequency applications [66]. Ideal class E performs 100% efficient conversion of DC to fundamental-frequency RF energy, in exchange for reduced output power, gain, and high-frequency performance. Mader et. al. [67] pioneered the use of the class E method at GHz frequencies. A block diagram of the ideal class E PA is shown in Fig 2.16.

As compared to the simple switching PA of Fig. 2.14 the class E amplifier incor-

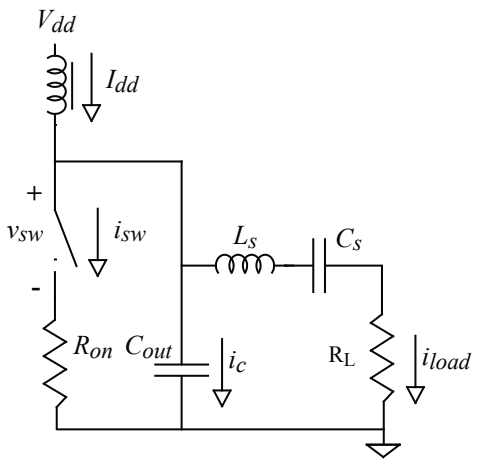


Figure 2.16: Schematic representation of an ideal class E amplifier.

porates a harmonic open circuit termination at the output capacitance. In Fig. 2.16 a high-Q resonance formed by C_s and L_s presents an open to all harmonic frequencies but is resonant at the switching frequency f_s (also referred to in this section as the angular switching rate ω_s). In contrast to other harmonic termination requirements discussed previously, the class E harmonic open circuit must be placed at the load side of the output capacitance, corresponding to plane P2 of Fig. 2.3.

Class E operation specifies a transient response that should occur between each RF cycle. This response is synthesized by the matching network and output capacitance C_{out}. The following assumptions must be satisfied to achieve class E operation:

(1) The choke which feeds drain current from the supply is ideal, and current I_{dd} does not vary during the RF cycle,

(2) All harmonics are terminated in an open circuit, resulting in sinusoidal load current, and

(3) The switch is ideal and operates with 50% duty cycle, which results in highest output power [68].

This problem has been rigorously solved in many ways in the literature ([3] [4] [69]

[66]), and such analysis will not be repeated here. However, class E operation can be qualitatively understood using the following:

- Beginning with condition 1, require that a constant current I_{dd} flows into the circuit from the DC supply. Current must go into the load, into the capacitor, or through the switch.

- Next, condition 2 requires sinusoidal load current, so the load resistor can be replaced by an AC current source of unknown phase and amplitude ($i_{load} = I_{dd} + a \cdot cos(\omega t + \theta)$).

- Since currents from the DC supply and from the load are known we see that the switch-capacitor combination must source or absorb the difference such that $I_{sw} + I_c = I_{dd} - I_{load}$.

- When the switch is closed, v_{sw} is zero by condition 3, and the current flows entirely through the switch ($I_{sw} = I_{dd} - I_{load}$, $I_c = 0$).

- When the switch is open, the same current flows entirely into (and out of) the capacitor ($I_c = I_{dd} - I_{load}$, $I_{sw} = 0$), and v_{sw} is the voltage developed across the capacitor.

The following three boundary conditions are also required to eliminate power dissipation in the switch-capacitor combination:

(1) $v_{cap} = v_{sw} = 0$ while the switch is closed,

(2) $v_{sw} = 0$ when the switch closes to avoid dissipating energy remaining in the capacitor, and

(3) $dv_{sw}/dt = 0$ when the switch closes to facilitate "soft switching" (the capacitor is fully discharged). This requirement corresponds to ZVS[4] in high-efficiency DC-DC

[4] zero voltage switching

converters [65].

Based on these boundary conditions the unknown amplitude and phase of the AC current source can be uniquely determined to be $a = 1.862$ and $\theta = -32.48°$. The AC current source can then be converted back to the form of a fundamental load impedance:

$$Z_E = \frac{0.28}{C_{out} \cdot \omega_s} e^{j49°} \tag{2.10}$$

Expressions for switch voltage and current can now be written in piecewise fashion:

$$(0 \leq w_s t \leq \pi) : v_{sw}(t) = \frac{I_{dd}}{w_s t}(w_s t + a(\cos(w_s t + \theta) - \cos\theta)) \tag{2.11}$$

$$(\pi \leq w_s t \leq 2\pi) : v_{sw}(t) = 0 \tag{2.12}$$

$$(0 \leq w_s t \leq \pi) : i_{sw}(t) = 0 \tag{2.13}$$

$$(\pi \leq w_s t \leq 2\pi) : i_{sw}(t) = I_{dd}(1 - a\sin(w_s t + \theta)) \tag{2.14}$$

These equations describe the ideal class E waveforms shown in Fig. 2.17.

Though these waveforms are highly nonlinear and rich in harmonic content, the high-Q filter network maintains purely fundamental output power at the load. Fundamental output power delivered to the load is about 78% (-1.07 dB) of that which would be delivered by the same device operating in class B [1].

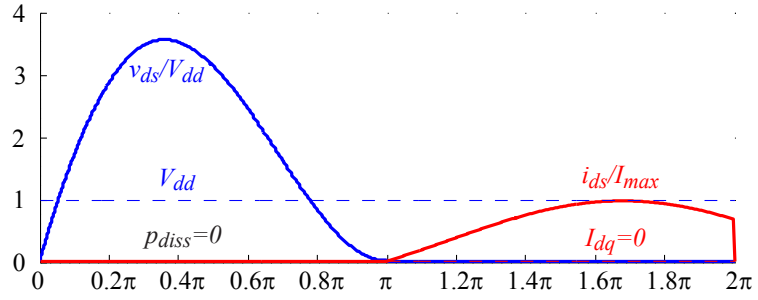


Figure 2.17: Drain waveforms for an ideal class E amplifier.

2.5.2 Practical Issues

Stress on the microwave transistor is extreme for switched modes. In class E operation the switch current peaks at $2.86 \times I_{dd}$, and the maximum switch voltage is $3.56 \times V_{dd}$. A device must be carefully selected to withstand this stress, and drain supply voltage may need to be reduced to avoid drain-source voltage breakdown. Furthermore, microwave devices commonly exhibit nonlinear output capacitance variation with drain voltage. [3] determined that a certain nonlinear characteristic describing an HBT[5] device would increase peak switch voltage by 28%,

Recall that drain supply voltage for class AB is conservatively set to $V_{dd} = V_{break}/2.5$. Ideal class E instead requires that $V_{dd} = V_{break}/3.6$, resulting in significant reduction of output power capability for a given transistor. Practical designs do not experience such high peaks due to a finite number of harmonic terminations, but some reduction in drain voltage from class AB levels is typically required for reliable operation.

The ideal switch transitions between open and closed states instantaneously. A microwave transistor can only emulate a short transition time from cutoff to saturation with a high level of overdrive (compare Fig. 2.6(b) with Fig. 2.8). Class E amplifiers thus operate in heavy gain compression and have high input drive power requirements. Additionally, the amplifier is completely nonlinear in the sense that reduced input power does not linearly reduce output power. As input drive is reduced, the switch approximation begins to fail, and the amplifier no longer exhibits class E characteristics.

Output amplitude control of class E amplifiers has been performed through the use of drain supply modulation (e.g. [20], [23]). Class E has a desirably linear relationship between peak RF load voltage and drain supply voltage (as shown in [70]):

$$v_{load} = \pm V_{dd}(26 \cdot f_s C_{out} \sqrt{R_E \cdot 50}) \tag{2.15}$$

where R_E is the real part of Z_E as defined in Eqn. 2.10. This method and similar drain

[5] heterojunction bipolar transistor

supply modulation methods are discussed in greater detail in Chapter 4.

A transistor must have a very small output capacitance relative to the fundamental frequency to satisfy the switch approximation. A maximum class E frequency can be defined based on I_{max}, C_{out}, and V_{dd} [3]:

$$f_{E,max} \simeq \frac{I_{max}}{56.5 C_{out} V_{dd}} \tag{2.16}$$

Above this frequency the capacitor of size C_{out} cannot completely discharge in one RF period, and ideal class E operation is impossible. In these cases sub-optimal class E has still been shown to provide significant efficiency enhancement [67]. Even so, this relationship requires the use of transistor technology that is advanced, and typically very expensive relative to the center frequency [5].

At UHF and microwave frequencies, lumped elements L_s and C_s of Fig. 2.16 are not available. Instead transmission line networks are used to emulate the resonator's harmonic open circuit impedance (e.g. [71], [40]). As with harmonic-tuned PAs, these networks can become lossy, sensitive, and large when controlling an increasing number of harmonics. The effect class E loss mechanisms including finite harmonic termination Q-factor and finite switch on- and off-resistance are considered in [72]. Termination of a finite number of harmonics is analyzed in [62]. As with all practical PA topologies, matching and bias circuitry also make a significant contribution to loss especially with large impedance transformation ratios.

2.6 Summary

Following the general discussion of transistors and load line theory, three categories of high-efficiency operation were discussed in this chapter: reduced conduction angle, harmonic-tuned, and switched mode. Though the philosophies are different, each method has the goal of increasing efficiency by reducing power dissipation in the virtual

drain while preserving fundamental-frequency output power. Varying tradeoffs exist among the methods:

- Reduced conduction angle modes are very commonly used, relatively easy to implement, and provide moderate efficiency. Linearity, gain, and output power can be traded for efficiency by variation of the conduction angle.

- Harmonic-tuned modes require a better understanding of device packaging and output capacitance, and precise control of harmonic impedances. The transistor must have gain at harmonics and withstand high drain voltage and current peaks. Dramatic increase in efficiency is possible for compressed operation, along with a theoretical increase in output power over class B operation. Broadband harmonic terminations are difficult to implement, typically resulting in a more narrowband operational bandwidth than reduced conduction angle modes.

- Switched modes (specifically class E) operate fundamentally differently than the previous two, and require a very high-performance device relative to that required for class AB operation. The transistor must satisfy switch approximations, with very high frequency performance and high voltage breakdown limits. Gain is reduced due to high levels of compression, and theoretical output power is 1.1 dB lower. Bandwidth is limited, as in the harmonic-tuned classes. The class E mode of operation does, however, offer 100% theoretical efficiency.

In the next chapter transistor characterization and high-efficiency PA design methods are presented to deal with non-idealities of real-world active devices. Class E and class F^{-1} designs with 110 W at UHF and 40 W at S-band with excellent results validate the approach.

Chapter 3

High-Efficiency PA Design

Contents

Chapter 2 provided theoretical basis of PA operation, templates for PA design, and a framework for understanding behavior. The theory is highly idealized to allow for mathematical tractability and intuitive understanding, and fails to account for many complex non-idealities of high-power transistors, especially when operated in high-efficiency modes. Nonlinear models are widely used for many types of PA design, but most are unreliable in the compressed regime required for high-efficiency operation. Relatively new transistor technologies often lack nonlinear models. Load-pull transistor characterization [73] is used to map transistor performance under different impedance, bias, and drive conditions. In this chapter, load-pull-based high-efficiency PA design methods are discussed and example PA designs are demonstrated.

Load-pull is an empirically-based PA design method guided by theory and sup-

plemented by models. This chapter contributes extensions to standard load-pull to facilitate measurements for harmonic-tuned and switched-mode operation. The method is applied to high-efficiency characterization of high-performance transistors, and the resulting data is used for numerous high-efficiency UHF PA designs (e.g. [5] [40] [38] [39]). As a representative example, an LDMOS device is characterized to illustrate the techniques for class E design at UHF, resulting in a demonstrated PA with 110 W output power at 360 MHz with 83% drain efficiency and 16.0 dB gain [6].

High-performance GaN HEMT transistors developed over the last decade have enabled high-power, high-efficiency PA operation at S-band [74]. As fundamental frequency rises, package and transistor parasitic effects have increasing impact, adding to the difficulty of harmonic impedance control. Transistor and FEM package analysis are used to evaluate devices and packaging technology for high-efficiency operation. New methods are developed in this chapter to determine feasibility and realize design of harmonic-tuned PAs. A swept harmonic load-pull technique was developed using fundamental-frequency tuners to allow verification of transistor and package approximations. Feasibility analysis of two GaN transistors shows that only one is suitable for harmonic-tuned operation at S-band, and also shows the benefit of reducing package parasitics. Load-pull contours are presented illustrating the dramatic impact of varying 2nd harmonic termination. A 3rd harmonic termination is added to satisfy conditions for class F^{-1} load-pull, resulting in an 8% efficiency improvement over the best-case 2nd harmonic termination. Load-pull measurements are verified by design and measurement of a 36-W class F^{-1} PA prototype at 2.14 GHz with 81% drain efficiency and 14.5 dB gain (78% PAE) in pulsed operation [2], among the best reported results with this frequency, power level, and device technology.

3.1 Load Pull Characterization

Load-pull is a highly customizable measurement method for nonlinear devices requiring a great deal of experience in both calibration and measurement to perform correctly. This section describes highlights of the methods used in this work, but is by no means a comprehensive discussion of the procedure and does not cover all intermediate steps required to obtain the presented results. Focus Microwaves hosts a library [75] of useful application notes, and [4] treats some underlying concepts.

The impedance and gain of active devices in small signal operation is commonly measured using a VNA[1] with 50Ω ports. Linearity allows mathematical post-processing to predict the device's behavior with non-50Ω ports. Large signal transistor behavior, by contrast, changes nonlinearly with port impedance, requiring that measurements be made with the appropriate port impedance. Load-pull involves measurement of active devices under varying load impedances. Note that "source-pull" denotes variation of the input impedance, and not variation of the impedance at the transistor's source terminal. Similarly, "source impedance" refers to input impedance.

Many types of active devices, ranging from low-noise-terahertz to high-power-megahertz, can make use of load-pull techniques. Load-pull equipment is therefore far less standard than a VNA and is often highly specialized in terms of frequency, power level, and parameter of interest (e.g. noise, power, efficiency). Fig. 3.1 shows photographs of load-pull measurement benches at UHF and S-band along with a block diagram of a general power transistor load-pull setup.

In the block diagram, a synthesizer drives a highly linear pre-amplifier whose output power is measured using a coupler. The circulator ensures that pre-amplifier performance and the coupler's coupling factor do not change with input impedance. Circulators are inherently narrow-band, so an attenuator of perhaps 3 dB is used to prevent

[1] vector network analyzer

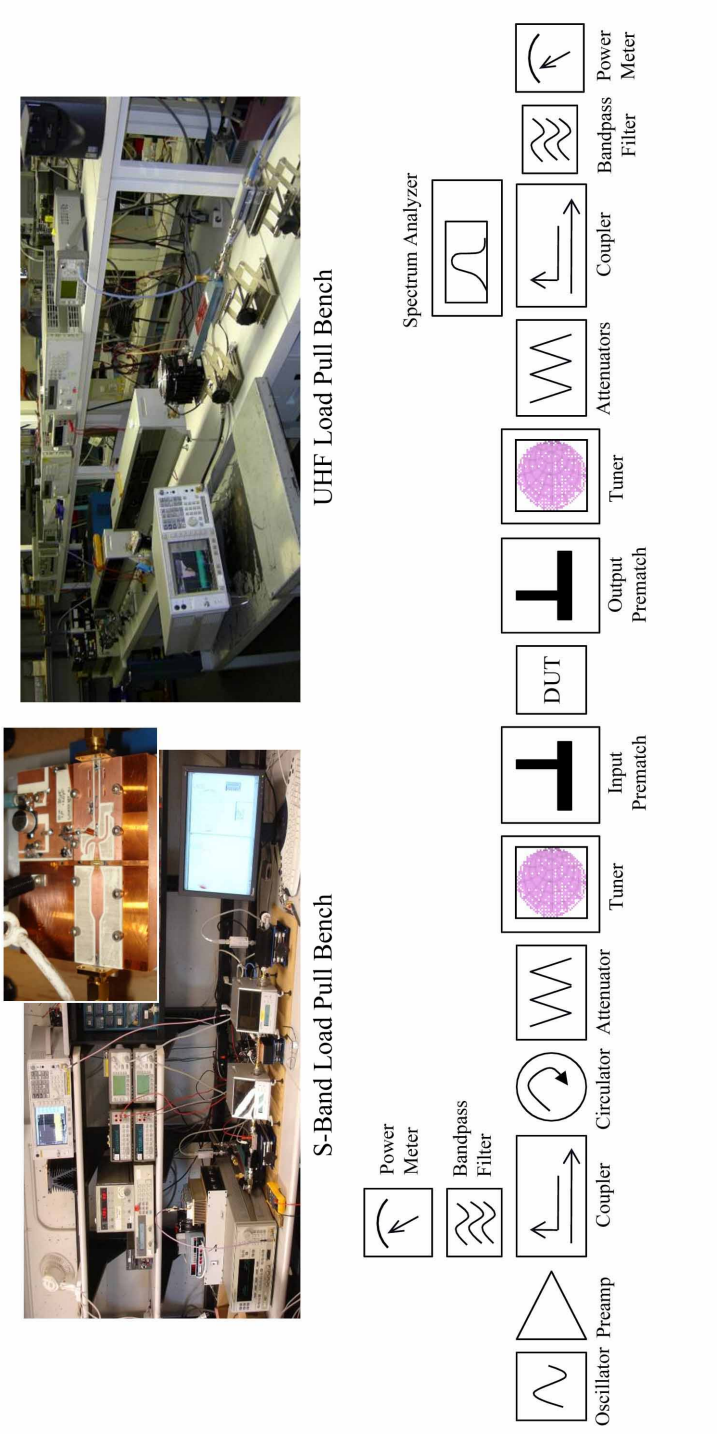


Figure 3.1: Photographs (top) of two load-pull benches and an end-to-end block diagram (bottom) for a power transistor load-pull configuration. Inset photograph is an enlargement of the input prematch, output prematch, and device under test.

highly reflective out-of-band input impedance. In this case the input reflection coefficient will be at least 6 dB even if the circulator presents a short out-of-band. These components make up the "input block".

Mechanical tuners and prematch circuits achieve impedance transformation between system impedance and desired DUT[2] impedances. Both will be described in more detail in the next section.

Output attenuators must be selected to avoid variation due to temperature under high load. Instead of one 30-dB attenuator capable of 100 W input power, a cascade of three attenuators might be preferable: a 150 W 6 dB attenuator, a 50 W 6 dB attenuator, and a 25 W 20 dB attenuator. A spectrum analyzer is critical in detecting instability, and output power is measured using a bandpass filter to eliminate harmonic energy from the measurement. These components make up the "output block".

3.1.1 Mechanical Tuners and Prematching Circuits

Mechanical tuners are commercially available from Focus Microwaves and Maury Microwave and exist to transform the 50Ω system impedance to a new input (or output) impedance presented to the DUT. A schematic representation of a single-slug tuner is shown in Fig. 3.2.

The tuners consist of a 50Ω coaxial air line and a metallic slug which can be repeatably moved along two axes: closer to or farther from the DUT (X) and closer to

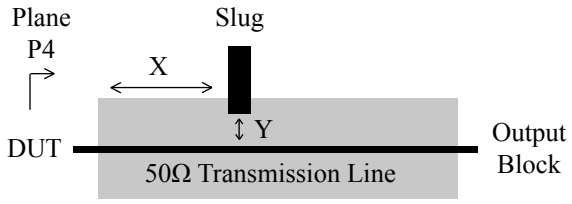


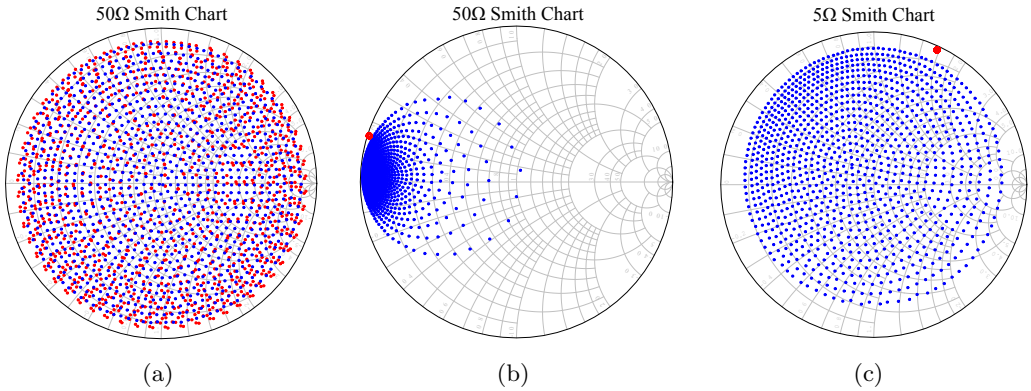
Figure 3.2: Single-slug mechanical load-pull tuner schematic.

[2]device under test

or farther away from the center conductor (Y). As Y becomes small the slug becomes increasingly capacitively coupled to the center conductor, transforming the impedance as would a single-stub matching network. A small gap Y transforms the 50Ω system impedance to a high reflection coefficient of variable phase. The phase is adjusted by slug movement in the X direction. A predefined set of impedances which the tuner can present is called a constellation. Note in the typical tuner constellation shown in Fig. 3.3(a) that the constellation has a maximum reflection coefficient magnitude, which defines minimum and maximum impedances.

In this work, load-pull is performed at UHF (360 MHz) and S-band (2.14 GHz) at power levels up to 120 W. Recall from Chapter 2 that high-power transistors have small load and source impedance values. Impedances on the order of 5Ω are poorly represented on the tuner constellation of Fig. 3.3(a), and near the edge of the constellation where power calibration uncertainty is large. A prematch circuit is used to implement a fundamental impedance transformation from 50Ω to 5Ω, translating each impedance in the constellation by the same ratio and resulting in the constellation of Fig. 3.3(b). Fig. 3.3(c) shows the constellation at planes P2 on a Smith chart normalized 5Ω.

Traditional load-pull tuners described earlier precisely control fundamental frequency



(a) (b) (c)

Figure 3.3: Fundamental (blue) and 2nd harmonic (red) impedance constellations at plane P4 (a), P3 (b), and P2 (c). The constellation at P2 is plotted on a Smith chart normalized to 5Ω.

impedances while harmonic impedances are allowed to vary arbitrarily as evidenced by the 2nd harmonic constellation of Fig. 3.3(a). Elaborate active [76] and passive [77] harmonic load-pull techniques are available but are less common and significantly more expensive. Later in this work it is shown that varying harmonic impedance has a dramatic impact on performance of some transistors, making it important to fix harmonic impedance conditions for repeatable results. In this chapter, harmonic quarter-wave transmission-line stubs are added to prematch circuits, placing a short at a fixed distance from the DUT reference plane. The output prematch circuit at the right side of Fig. 3.4 implements harmonic termination in this way, and the circuit at the left is used to measure the impedance of the output prematch.

Any harmonic tuner impedance will combine in parallel with the prematch short, resulting in a constant high-gamma harmonic impedance for the whole fundamental frequency impedance constellation. The distance of the short from the DUT determines the phase of the high reflection coefficient termination at the harmonic frequency. The prematch implemented to achieve the constellations of Fig. 3.3(c) terminates the 2nd harmonic (red) in a constant inductive high reflection coefficient impedance for all fundamental frequency impedances.

Figure 3.4: Break-apart TRL impedance verification standard (left) and output prematch circuit (right) which incorporates a fundamental impedance transformation to 5Ω, 2nd and 3rd harmonic termination stubs, and a bias tee. The bias tee choke is implemented by a quarter-wave transmission line terminated at the DC end by a capacitor resonant at the center frequency. Additional shunt bias tee capacitance for low-frequency termination is not shown on this prematch.

Available gain increases as frequency decreases, requiring careful bias network design. Bias networks should present a low-impedance termination at low frequencies (10s to 100s of MHz). This is most commonly achieved by placing the bias network close to the DUT and placing a bank of shunt bypass capacitors on the DC side of the RF choke. In this work the DC bias is supplied as close to the device as possible, through the prematch circuit.

3.1.2 Calibration

Before load-pull measurement can take place a VNA is used to measure two-port S-parameters of the input block, output block, and prematch circuits. The S-parameters of the tuners are also measured over a constellation of XY positions. The S-parameters at each XY point are cascaded with input and output block and prematch circuit S-parameters resulting in a constellation of input and output impedances and corresponding input and output power calibration factors (procedure detailed in appendix of [4]). The calibration factors take into account both resistive and reflection loss from the DUT measurement plane to the input or output power meter. It is important to understand that the uncertainty of this factor rises with increasing mismatch. Near the outside edge of the calibrated constellation (high reflection coefficients) power measurements have larger uncertainty [78].

When dealing with non-50Ω port impedances (e.g. output prematch circuits) it is important to distinguish between types of loss. In a 50Ω system it can be said that loss (in dB) is simply $10\log|S_{21}|^2$. If, for example, the device is mismatched at the input port to 40Ω instead of the desired 50Ω, the reflection loss will be included in that calculation. However, if the device is *designed* to have a 40Ω input impedance we do not wish to penalize the device for input mismatch loss. This is the case for load-pull and PA matching networks, where the input prematch is designed to operate with a 5Ω input port and a 50Ω output port. After 50Ω S-parameters are measured, insertion loss

effectively re-normalizes the data such that port 1 is conjugately matched:

$$IL = 10\log\left(\frac{|S_{21}|^2}{1-|S_{11}|^2}\right) \tag{3.1}$$

Output prematch S-parameters are measured from the DUT reference plane P3 to the coaxial reference plane P4. This measurement is performed using standard coaxial VNA calibration and a microstrip verification standard. The photograph of Fig. 3.4 shows such a standard placed to the left of the prematch circuit. The standard's S-parameters are determined from three measurements using the TRL[3] procedure described in [79]. Two verification standards are constructed along with an insertable line of well-known impedance, as shown in Fig. 3.5.

The TRL standards and prematch circuits are soldered to modular copper blocks and can be very repeatably connected to each other. The TRL procedure outlined in [80] solves the S-parameters of TRL blocks A and C using S-parameter measurements of A+C, A+B+C, a 1-port measurement of A alone, and a 1-port measurement of B alone. After S-parameters of block A are known it can be connected to an output prematch as shown in 3.4. The cascade of A with the output prematch is measured, and then the known S-parameters of A are de-embedded. Only the S-parameters of the prematch remain and are referred to planes P3 and P4 as desired.

Guidelines for design of TRL standards can be found in [80]. Fields across the

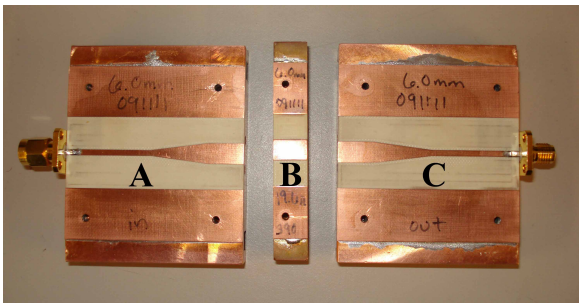


Figure 3.5: Input, line, and output line standards for a break-apart microstrip TRL calibration kit.

[3] thru reflect line

junction between blocks should be as continuous as possible (same substrate, same line width, no discontinuities near the junction). In the case of harmonic prematch circuits it is critical that the verification blocks be well-characterized over a bandwidth including the highest harmonic frequency of interest.

Some load-pull methods use the input and output prematch as the verification standards as well. Prematch circuits with harmonic terminations have deep resonance at the harmonic frequencies, resulting in a singularity in the TRL solution. Therefore separate verification standards are required which do not have such resonances and can be solved over the whole frequency range using the TRL method.

Small errors in S-parameter measurements of any load-pull component have two impacts on load-pull accuracy. The first is obvious: a slightly different input or output impedance will be presented to the DUT than is expected from calibration data. Secondly, an error in S-parameters impacts calculation of reflection loss, and thus the calibration factor added to the output power measurement. At each impedance point in the constellation the error will be different, resulting in a gradient of power measurement error over impedance. Best performance contours are skewed toward regions of increasingly optimistic power measurement error and give a false impression of device performance. A number of verification measurements can be performed to determine calibration accuracy for each branch of the system. For example, Fig. 3.6 shows a measurement of gain contours when no DUT is present, and the source is tuned very near 50Ω. If the load-pull system is well-calibrated, a conjugate load impedance should result in 0 dB gain, and gain should decrease uniformly with increasing reflection coefficient magnitude due to mismatch loss:

$$ML = 10\log(1 - |\Gamma|^2) \tag{3.2}$$

The maximum gain and gain contours of Fig. 3.6 therefore indicate good calibration.

More time is often devoted to calibration of a load-pull system than to actual DUT

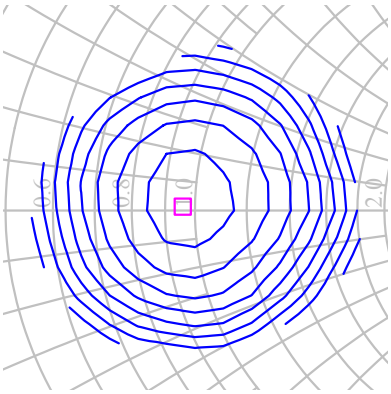


Figure 3.6: Gain contours spaced by 0.05 dB for a load-pull of a source tuner set to Z_{source}=48.0-j0.2Ω. Maximum gain is -0.02 dB at Z_{load}=47.9+j0.2Ω, and gain decreases uniformly in all directions with increasing reflection coefficient magnitude, verifying that the load-pull system is well-calibrated.

measurements. Extreme attention to detail is critical when high output power and efficiency are expected, as very slight power, voltage, and current measurement errors have a large impact. Some degree of constant error in efficiency or output power is acceptable for load-pull measurements, because transistor performance at one impedance relative to another is correctly shown. Errors which vary significantly over the impedance constellation are not tolerable, as they indicate false trends. Drain efficiency and gain measurements are used separately in this work to limit error sources and more clearly expose error trends caused by incorrect S-parameter calibration data. Though PAE provides a more comprehensive picture of performance, it combines input, output, and bias power into one metric along with errors from each. Fig. 3.7 shows the impact on calculated drain efficiency for an output power or current measurement error.

For example, 45.5 dBm output power with 36 V and 1.26 A supply voltage and current results in 78.2% drain efficiency, but a supply current measurement error of only 20 mA changes efficiency by as much as 1.2%. Similarly, a power measurement error of only 0.05 dB changes drain efficiency by as much as 0.9%. Sensitivity to these errors increases as output power and efficiency rise, making clear the importance of high-precision calibration.

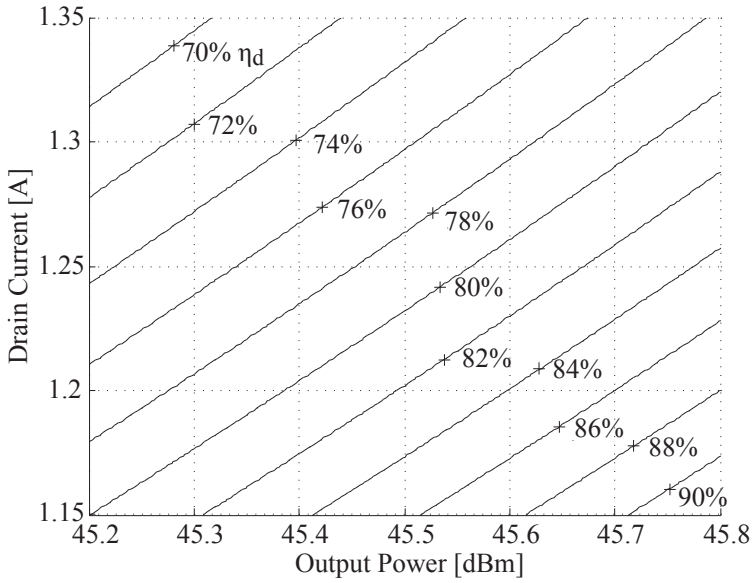


Figure 3.7: Drain efficiency for varying I_{dd} and P_{out} with constant V_{dd}.

3.1.3 Power Measurement

In modulated or pulsed power applications high-power PA performance is often better than in CW[4] applications due to transistor self-heating effects. Pulsed-RF (or simply "pulsed") load-pull measurements are used in some of this work to emulate the pulsed power application. The synthesizer is set to produce pulses of a certain duty cycle and period and sends a trigger to start measurements at the beginning of each pulse. RF power, RMS drain current, and RMS drain voltage are measured over the middle 80% of the pulse to avoid startup transients and timing-related errors.

Measurement of drain current is complicated by the drain bias tee capacitance required for stable operation of high-power transistors. The drain bias circuit for pulsed-RF measurement is shown in Fig. 3.8. I_{dd} would ideally be measured directly using an oscilloscope, but the addition of a current probe (and its parasitic inductance) would impact RF performance. Therefore the current measurement is made immediately before the PA bias network. Recall that low-frequency bias network termination is impor-

[4]continuous wave

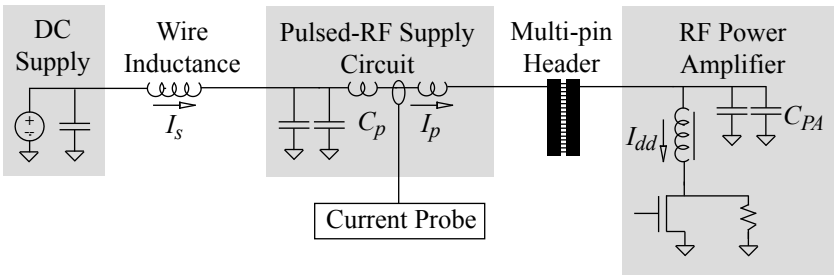


Figure 3.8: Drain bias circuit schematic for a pulsed-RF measurement.

tant for stable operation of high-power transistors, and is implemented by the capacitor bank C_{PA}. When the RF pulse starts and current is drawn into the RF transistor some current will initially come from this capacitance C_{PA}, thus the measured current I_p does not equal I_{dd}. This error is transient, and quickly becomes small provided the capacitance C_{PA} is sufficiently low. The portion of the pulse being measured should not begin until this error is small. A multi-pin header is used to connect the pulsed-RF supply circuit to the PA to minimize parasitic reactance between the two components. On the DC supply side of the current measurement the DC supply and wire inductance respond very slowly to a step change in current I_p. Therefore, to keep the voltage at the PA from dipping, a large value of capacitance C_p is required, implemented as a bank of capacitors of varying size to provide very low impedance over a broad frequency range. The values and components used to implement C_{PA} and C_p depend on PA stability requirements, pulse width, and I_{dd} during the pulse.

Pulsed RF power is measured with a spectrum analyzer set to zero span. The instrument is connected to either the input or output power measurement ports by means of an RF SPDT[5] switch. The spectrum analyzer is not an acceptable instrument for absolute power measurement, so the high degree of accuracy inherent in a CW power sensor is transferred to the spectrum analyzer by means of a power offset calibration factor. A zero-span spectrum analyzer measures CW power and pulsed power with the

[5]single pole double throw

same relative accuracy.

Mechanical tuner power limits range from 10's to 1000's of watts and can be defined at both peak and average power levels. High average power causes heating and expansion of the center conductor leading to loss of precise calibration and protrusion of the center pin in external connectors. Provided the pulse duration is smaller than the thermal time constant of the center conductor, the average power of the waveform should be used to ensure compliance with the the average power limitation. Duty cycle can be varied to set average power as desired:

$$P_{avg,dBm} = P_{peak,dBm} + 10 \log DC \tag{3.3}$$

For example, 50 dBm peak power with a 5% duty cycle pulse results in 37 dBm average power.

The manufacturer suggests a maximum average power of 30 W, limited by the tuner's APC-7 coaxial connectors, but does not provide any guidance about maximum peak power [75]. We wish to use the tuners to characterize transistors up to 250 W peak, so an analysis was performed to approximate the safe peak power level for a given tuner. High peak power causes air breakdown between the center conductor and the slug in the tuner, leading to damage of the slug and center conductor. The critical field between the two surfaces is not well known due to variation in air humidity and a dielectric coating on the slug. The minimum spacing between the two surfaces is 5 mil in the Focus CCMT-1816 tuners used in this work [81]. Peak voltage along a transmission line can be derived from basic transmission line expressions [82] as a function of mismatch and peak power:

$$V_{peak} = \sqrt{\frac{2Z_o P}{1 - |\Gamma|^2}}(1 + |\Gamma|) \tag{3.4}$$

Thus the peak power limit of the tuner is dependant upon the VSWR[6] produced by the tuner. Fig. 3.9 was produced using the relationship between peak power, tuner

[6] voltage standing wave ratio

VSWR, and critical field. Based on discussions with the manufacturer [81], it is reasonable to expect that the critical field should be higher than 35 kV/cm, so peak power of 100 W can be safely used provided tuner reflection coefficient magnitude is less than 0.9. Fig. 3.9 therefore provides a conservative estimate of the peak power which can be applied to a tuner given a maximum reflection coefficient magnitude. This analysis proves to be a useful tool for high-power load-pull.

3.1.4 General Measurement Procedure

After calibration, the transistor is slowly brought to the quiescent bias point, watching for potential oscillation. In some cases the load or source impedance must be adjusted, or the bias network low-frequency termination improved, to avoid instabilities.

Realistic transistors are bilateral, so source and load-pull must be performed in an

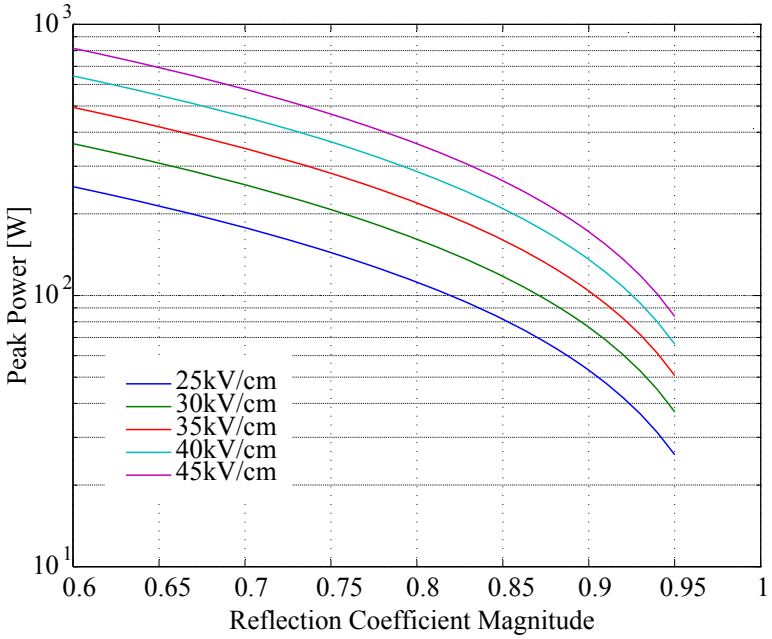


Figure 3.9: Peak power limit analysis for Focus CCMT-1816 load-pull tuners. The plot shows power and impedance mismatch required to achieve the specified maximum electric field strength on a transmission line. This plot is used to determine the maximum safe peak power level in the load-pull tuners. For the tuners used in this work the maximum allowable field is assumed to be 35 kV/cm.

iterative fashion. First source-pull is performed using a small input signal to determine input impedance for high gain. Load impedance during this source-pull should be set to a reasonable value, typically the theoretical load line impedance.

High gain is a key ingredient in large-signal oscillation. During initial load-pulls it is sometimes helpful to intentionally mismatch the input impedance away from maximum gain. Gain will be reduced because power is reflected, or not effectively delivered, to the transistor gate. Roughly the same output power and efficiency will be achieved by supplying more incident power to make up for the power which was reflected. The tradeoff between reduced gain and stability must be made when selecting final prototype impedances as well. Fortunately, in many cases the input impedance has very little impact on large signal output power and efficiency provided the same level of gain compression is achieved.

Transistor performance measurements are be performed at each impedance in the a constellation under one of many input power conditions including constant input power, swept input power, and constant gain compression. In this work the constant gain compression method is implemented for GaN HEMT devices by increasing input power until a consistent value of gate current I_{gg} is measured, indicating an approximately constant level of device compression.

3.2 UHF Class E Load Pull and PA Design

An example of class E load-pull and subsequent PA prototype design procedure is presented in this section. The DUT is an LDMOS transistor (TriQuint PLD365F) intended to produce about 100 W at 2 GHz and does not make use of internal input or output matching networks. The same procedure was also used to characterize a collection of lower-powered devices as well, including GaN on Si HEMT, GaN on SiC[7] HEMT, SiC

[7] silicon carbide

MESFET[8], and LDMOS [5] [83] [40]. The load-pull system was configured, calibrated, and verified; and transistor load-pull data was collected over a four-day period using a UHF load-pull system (shown in Fig. 3.1 at the top-right) located at dBm Engineering, now TriQuint Semiconductor, in Boulder, CO.

3.2.1 Class E Load Pull

Output capacitance of the large LDMOS transistor is estimated to be 45 pF, leading to a theoretical class E fundamental load impedance of 1.8+j2.1 at 360 MHz (Eqn. 2.10). The device is specified for class AB operation at V_{dd}=28 V, so breakdown voltage is estimated to be about 70 V. This class E implementation will make use of only 2nd harmonic termination, avoiding the ideal class E $3.6 \cdot V_{dd}$ peak drain-source voltage [62]. Still, the drain supply voltage is de-rated for class E operation to 24 V, assuming $V_{ds,max} \leq 3V_{dd}$ for the one-harmonic case. I_{max} is not specified by the manufacturer for this device, but load-line approximations and IV curve simulation of similar devices indicate I_{max} >21 A. Maximum frequency for ideal class E operation ($F_{E,max}$ from Eqn. 2.16) can be calculated for a 24 V drain voltage as 340 MHz, below the target frequency of 360 MHz. Ideal class E performance is not expected in this case, but instead a sub-optimal class E mode.

General prematch circuits were constructed to center the fundamental constellation at 10Ω and fix the second harmonic at an open. The impact of device packaging and bond wires is small and was assumed negligible at harmonic frequencies - that is, a harmonic open at the prematch plane (P3) edge is assumed to represent an open at the output capacitance (P2). Reference planes are shown in Fig. 2.3. The input and output prematch circuits were fastened to break-apart aluminum blocks with nylon screws and measured using TRL verification standards. A photograph of the load-pull fixture is shown in Fig. 3.10. This characterization was performed with a CW input

[8] metal semiconductor field effect transistor

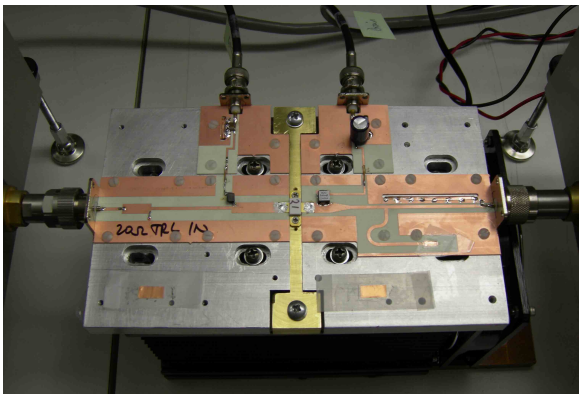


Figure 3.10: Photograph of a break-apart load-pull fixture used for characterization of the 100-W LDMOS device in class E mode.

signal, consistent with the target application. A very large heat sink was used during the load-pull procedure because some load impedance regions produce highly inefficient operation, resulting in a large amount of dissipated heat.

Small-signal source-pull measurement was performed with the output impedance set near the ideal class E impedance, and results are shown in Fig. 3.11. Note that contours do not close because the well-calibrated source constellation did not extend to a high-enough reflection coefficient magnitude to achieve decreasing gain. We can, however, reasonably predict that the 20 dB contour is the largest that would occur. The

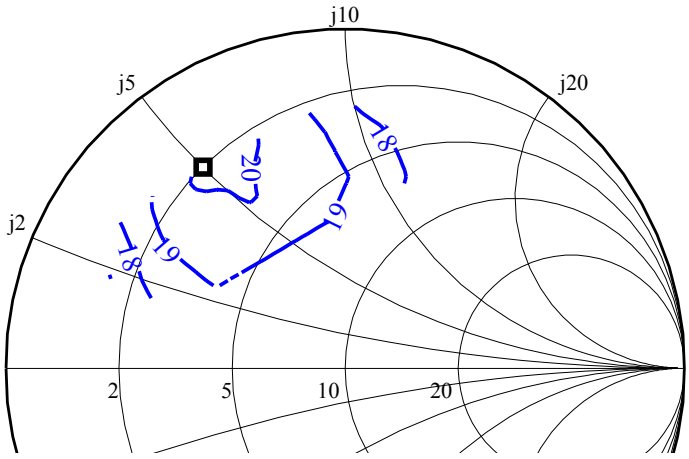


Figure 3.11: Source-pull gain contours for an LDMOS transistor, black square at 2+j5Ω is source impedance selected for final prototype design. Smith chart is normalized to 10Ω.

black square in Fig. 3.11 shows the input impedance (2+j5Ω) used in the final prototype design. This impedance has a high ratio of reactance to resistance - a relatively high-Q impedance. Low-loss matching networks insensitive to manufacturing errors are difficult to design with very high-Q impedances.

Load-pull measurement was carried out with constant input power levels. Low input power was applied for the first load-pull to map regions of high heat dissipation or oscillation. Those regions were noted and avoided in subsequent load-pulls. A final load-pull measurement is shown in Fig. 3.12. Note that output power (red) is shown in watts. The green circle indicates the theoretical class E impedance, and the black square shows the impedance used in the final prototype design. Again, contours do not close due to limitations of the prematch circuit fundamental transformation. A transformation centered at 5Ω would have provided a constellation that more completely encompassed the region of interest, but a transformation centered at 2Ω would have put the high-reactance optimal source impedance at the edge of the constellation.

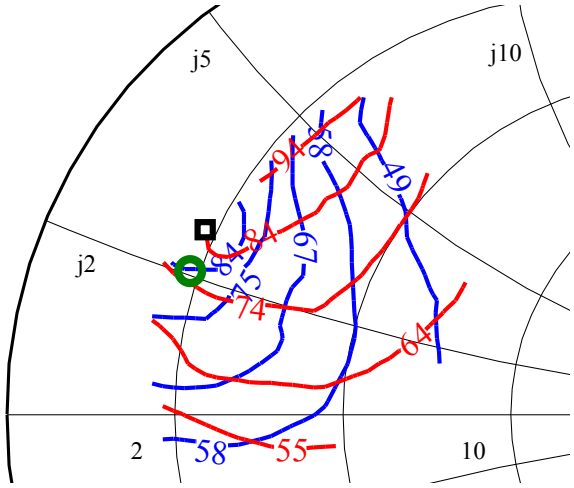


Figure 3.12: Load-pull power (red, in watts), and drain efficiency contours (blue) for the LDMOS device in class E configuration. Theoretical class E impedance of 1.8+j2.1Ω is shown with a green circle, prototype impedance of 1.8+j2.9Ω shown with a black square. Smith chart is normalized to 10Ω.

3.2.2 Prototype Design

Low-impedance matching networks can incur significant loss and also frequently have very narrow bandwidth [49]. Losses at the input have the effect of reducing PA gain, and thus PAE, while output loss reduces ultimate output power and drain efficiency, as shown in Fig. 3.13. For example, a 0.3 dB output matching loss (typical for these applications) results in a 7% reduction in efficiency. If the transistor was originally 80% efficient the PA efficiency should be 74.4% (80% reduced by 7%). The impact of loss clearly becomes less when initial efficiency is not as high. Thus, a large part of high-efficiency PA design focuses on low-loss matching network design.

A broad-band low-loss coaxial unbalanced-unbalanced transformer (un-un) can achieve matching from 50Ω PA terminals to 12.5Ω by connecting transmission lines in parallel at the low-impedance end and in series at the high-impedance end [84], [85]. The same structure can be used to achieve transformation from an unbalanced 50Ω port to two

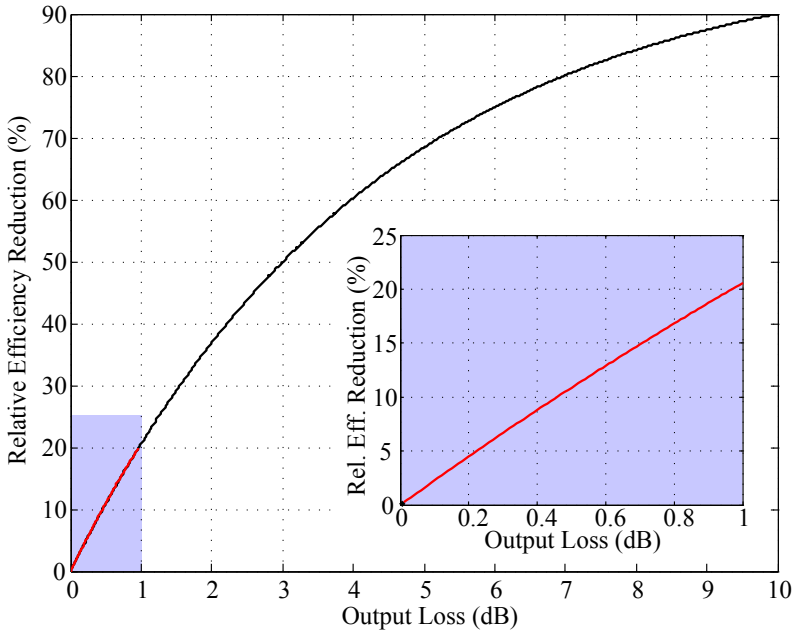


Figure 3.13: Fractional drain efficiency reduction due to output loss. Y-axis indicates the percentage by which the drain efficiency is reduced from the original value given loss in an output matching network.

balanced 6.25Ω ports (called a bal-un, or balun). The constructed un-un transformer and a schematic representation is shown in the photograph of Fig. 3.14.

Low-loss matching from the 12.5Ω output of the coaxial transformer to the desired input and output impedances obtained using load-pull was achieved using both distributed and lumped elements. Another segment of coaxial line is used to implement a quarter-wave open-circuit stub at the 2nd harmonic, placing a short on the transmission line at some electrical distance away from the DUT. This method of harmonic termination is used throughout this work with increasing complexity as additional harmonics are controlled and is described in [86]. One advantage of the coaxial stub is the ability to move the position of the harmonic short nearer and further from the DUT, making slight adjustments to the phase of the 2nd harmonic termination at the DUT. The complete prototype output matching circuit is shown in Fig. 3.14 with a block diagram.

Adjustment to the physical position of lumped elements and the 2nd harmonic stub was required. The final output impedance trajectory is shown in Fig. 3.15 with the black box indicating the impedance at the fundamental, the red circle showing the 2nd harmonic termination, and the green circle showing ideal class E fundamental impedance.

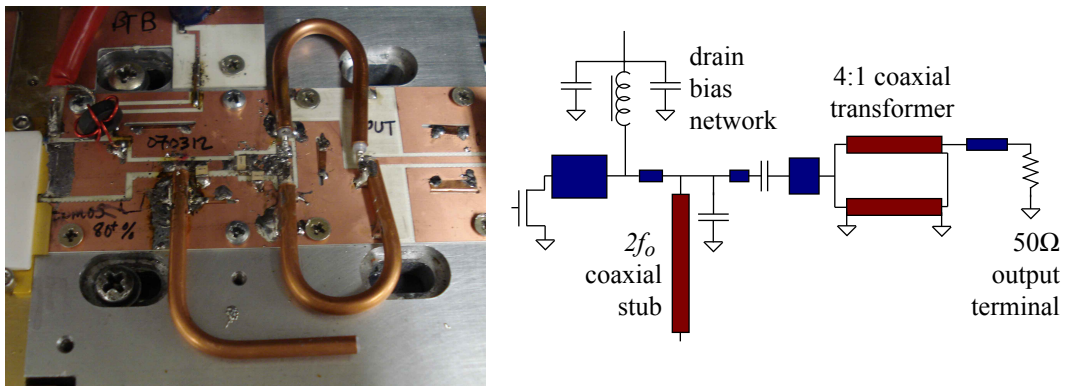


Figure 3.14: Low-loss output matching and bias network for the UHF class E LDMOS PA prototype. Final fundamental impedance at plane P3 is 2.5+j3.2Ω with a 2nd harmonic open-circuit. A block diagram of the circuit (right) shows microstrip transmission lines in blue and semi-rigid coax in red.

The matching circuit impedance trajectory was measured using the same procedure used to measure load-pull prematch circuits.

3.2.3 Prototype Performance

Fig. 3.16 shows a photograph of the complete class E UHF PA prototype. Note that the transistor package houses two identical devices, but this PA prototype makes use of only one.

Input and output terminal connections are made with N-connectors. Both input and output matching circuits use semi-rigid coaxial 4:1 impedance transformers to transform the 50Ω terminal impedance to 12.5Ω. A combination of lumped and distributed matching techniques are used to achieve transformation from 12.5Ω to the desired DUT input and output impedances. All capacitors are from the Advanced Technical Ceramics ATC100B series, selected for high breakdown voltage and relatively low loss. The substrate is 30-mil-thick 2-oz copper-clad Rogers RO4350B, with ϵ_r=3.5, selected primarily for low loss, high power handling capability, and ease of manufacturing. The dielectric constant and thickness allow microstrip lines over a reasonable range of Z_o, important

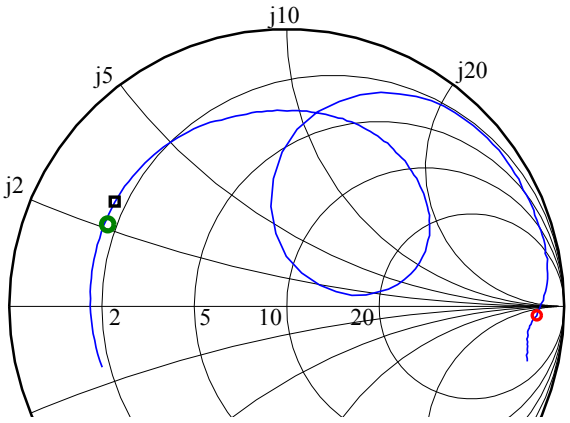


Figure 3.15: Fundamental (black square) and 2nd harmonic (red circle) measured impedance of the 110 W class E UHF prototype. Theoretical class E fundamental impedance is 1.8+j2.1Ω for C_{out} = 45 pF at 360 MHz, is shown in green. The Smith chart is normalized to 10Ω.

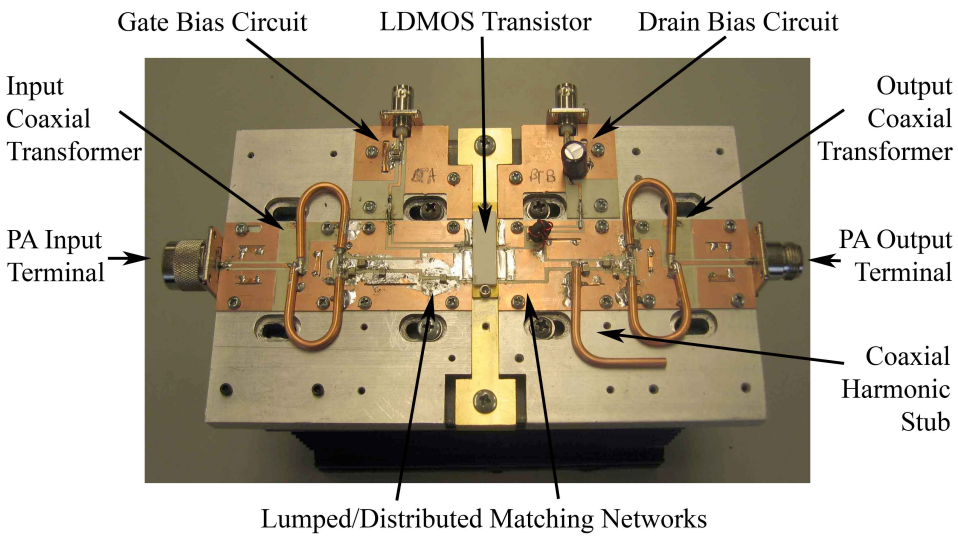


Figure 3.16: Photograph of the 110 W class E UHF PA prototype.

for low-impedance matching. Gate bias is supplied through a 100Ω resistive choke, and drain bias is supplied through a custom inductor wound around a torroidal ferrite. The 2nd harmonic termination is implemented by an open-ended stub made of semi-rigid coax which is $\lambda/4$ at the 2nd harmonic frequency. The prototype is mounted on the same fixture blocks used for load-pull characterization, though in class E mode very little heat is dissipated (less than 23 W at 110 W output power), making the large heat sink unnecessary.

Final measurement results of the UHF class E PA prototype under CW operation are presented in [6]. The prototype is biased at 24 V drain and with less than 50 mA quiescent current. In ideal class E operation the transistor should be in complete cutoff when the "switch" is not on. A more practical design allows some quiescent current to allow the transistor to turn on and reach saturation more quickly. In the end, selection of quiescent current is a tradeoff between power dissipation in the switch's off-state and power dissipation due to slow turn-on.

Standard power and frequency sweep measurements are shown in Fig. 3.17 and Fig. 3.18. The class E UHF prototype measures 110 W output power with 16 dB gain

and 83% drain efficiency at 360 MHz. 80% drain efficiency is achieved over an 8% bandwidth. This result compares well with other high-efficiency work at this frequency and approximate power level, even when more expensive and exotic device technology is used (e.g. [5] [87] [83]). Note from the power sweep that gain is quite nonlinear with input power due to the low quiescent current. For low modulation bandwidth signals, techniques have been used for many decades to restore linearity to non-linear power amplifiers such as class E [19]. A similar supply modulation technique is discussed, simulated, and implemented in Chapters 4 and 5.

3.3 S-Band Transistors and Packaging

The previous section described a method of load-pull characterization and class E PA design in the UHF range, where transistors which meet the criteria for high-efficiency operation are readily available, and packaging parasitics have little effect. In this section, S-band transistors and packaging are considered. The target application is a harmonic-tuned PA with more than 30 W peak power and over 70% PAE in the 2.14 GHz downlink W-CDMA cell phone band. Only recently has device technology advanced to make this possible [74]. Packaging is found to be a critical consideration at this frequency.

3.3.1 GaN HEMT Transistor Technology

The Si LDMOS transistor technology described in Chapter 2, and used earlier in this chapter for the UHF class E PA, lacks high-frequency performance required for harmonic-tuned or switched-mode operation at S-band. Output capacitance for a 50 W LDMOS device is on the order of 25 pF, and very closely approximates a short at harmonics of a 2.14 GHz fundamental frequency. The approximate short relieves the designer of explicitly enforcing harmonic terminations for high-power class AB PA designs when output capacitance is high relative to the fundamental frequency.

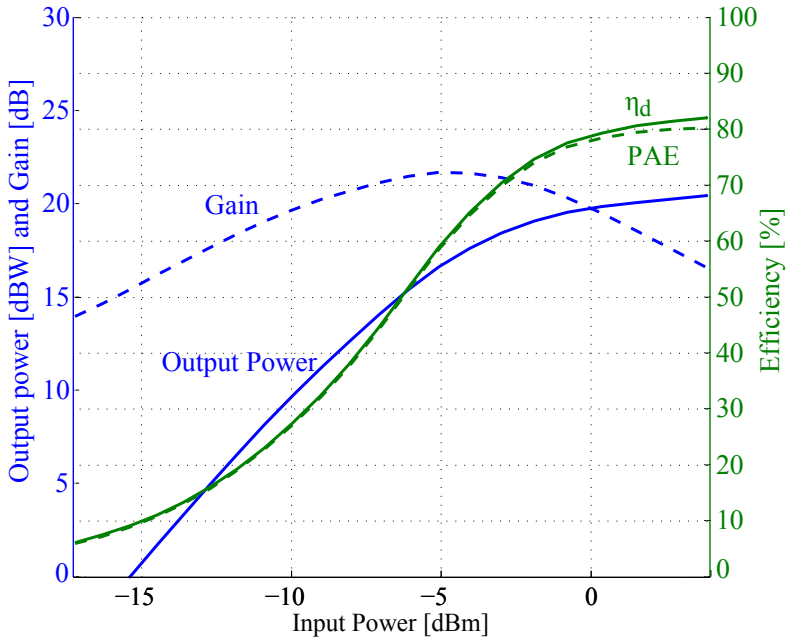


Figure 3.17: Measured gain, output power, and efficiency over input power for the final 110 W class E UHF PA prototype using an LDMOS transistor.

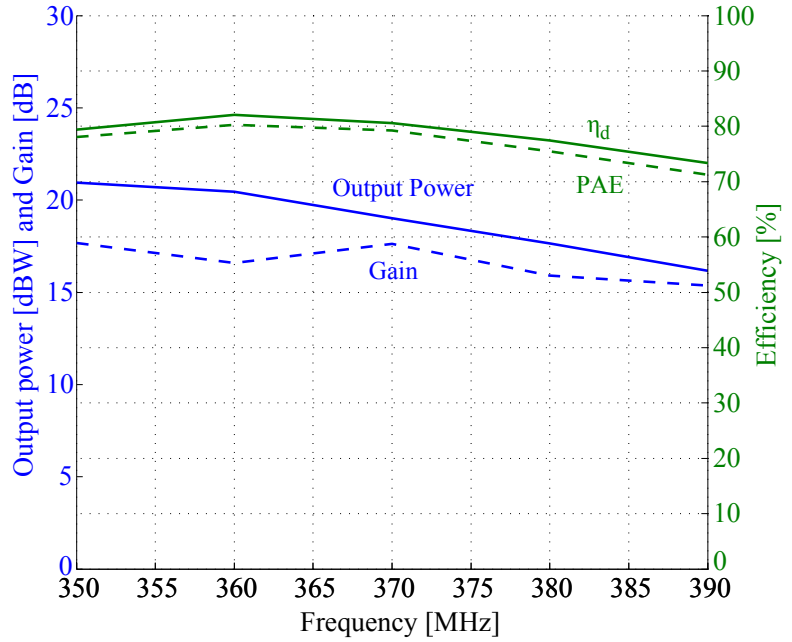


Figure 3.18: Measured gain, output power, and efficiency over frequency for the final 110 W class E UHF PA prototype using an LDMOS transistor.

GaN HEMT transistor technology has been made commercial in the last decade with unprecedented power density per unit cell and holding the possibility of excellent high-frequency performance [50]. A summary of Si and GaN semiconductor materials is given by Table 3.1.

GaN outshines Si in every category except thermal conductivity. However, to date GaN for HEMTs is grown on other substrates such as Si or SiC, meaning only a thin layer of GaN is used and limits the impact of its thermal conductivity. Instead thermal performance of GaN-based devices depends on the thermal conductivity of the substrate. SiC has a thermal conductivity of 120 W/mK - a great potential advantage over devices built using Si substrates - but is much more expensive.

PA design benefits from these enhancements in a number of tangible ways [88], including the following:

- Output capacitance reduced as much as an order of magnitude compared with LDMOS,
- Increased input and output impedance allowing lower-loss and broader-band matching circuits,
- Increased reliability under high temperature operation,
- Maximum operating frequency increased by more than a factor of 8 compared with LDMOS, and
- Increased drain voltage breakdown limits.

Table 3.1: Material properties of Si and GaN.

Metric	Si	GaN
Bandgap Energy	1.12 eV	3.40 eV
Breakdown Field	5.7e5 V/cm	38e5 V/cm
Electron Low-Field Mobility	710 cm^2/Vs	1200 cm^2/Vs
Electron Peak Velocity	1e7 cm/s	2.46e7 cm/s
Thermal Conductivity	1.3 W/mK	1.2 W/mK

HEMT operation [50] is fundamentally different than that of MOSFETs[9] described in Chapter 2. The conduction channel is made a junction between two materials having different band gaps (called a heterojunction). In this way current is not slowed by traveling through a channel doped with impurities (as in a MOSFET), but instead travels using high-mobility electrons generated at the heterojunction in a thin layer called the 2DEG[10]. Instead of the MOSFET gate oxide, the HEMT has a Shottky gate which allows forward current conduction under saturation. Also unlike MOSFETs, microwave HEMTs are almost exclusively depletion mode meaning that a negative voltage is required to turn off the channel.

GaN HEMTs are not without downsides. The relatively immature technology carries with it a large price tag, optimistically 4 times the cost per watt of comparable LDMOS; as demand and volume increase the cost is expected to decrease. Reliability, performance drift, and manufacturing issues are gradually being addressed [89], and a number of GaN devices are commercially available from manufacturers such as TriQuint, Nitronex, Cree, Sumitomo, and RF Micro Devices.

A type of memory effect behavior usually attributed to charge trapping [90] is particular to III-IV semiconductor devices. The behavior can be qualitatively described as a reduction in quiescent current immediately following a high-power pulse. The quiescent current recovers gradually to its original value with a time constant ranging from microseconds to minutes depending upon device design. This leads to time-varying quiescent current which depends on the history of the output power, and thus time-varying PA gain.

[9] metal oxide semiconductor field effect transistors

[10] 2D electron gas

3.3.2 Traditional High-Power Transistor Packaging

A traditional high-power microwave package available from Zentrix and other well-known package manufacturers, and traditionally used for LDMOS PA designs, was simulated using HFSS. A photograph and the CAD[11] drawing used for simulation are shown in Fig. 3.19. The goal of the simulation was to determine the fundamental and harmonic impedance transformation from the microstrip circuit edge to the die "drain manifold," where bond wires contact the active device. Note that planes P3 and P2 in the figure are located at the microstrip prematch edge and at the die drain manifold, respectively, and include 16 gold bond wires of 1.25 mil diameter. The simulation results are de-embedded to these reference planes. The microstrip transmission line connects to the package lead, which is supported vertically by a dielectric "windowframe". In many cases this material is alumina (Al_2O_3), with a relative dielectric constant of about 8.8. The transistor sits on the flange, built of a material providing a good thermal match to the transistor's substrate. The transistor is attached to the flange with eutectic AuSn[12] or similar solder.

The HFSS analysis shows that package parasitics between planes P3 and P2 are quite significant at the 2nd harmonic of the intended 2.14 GHz center frequency. The

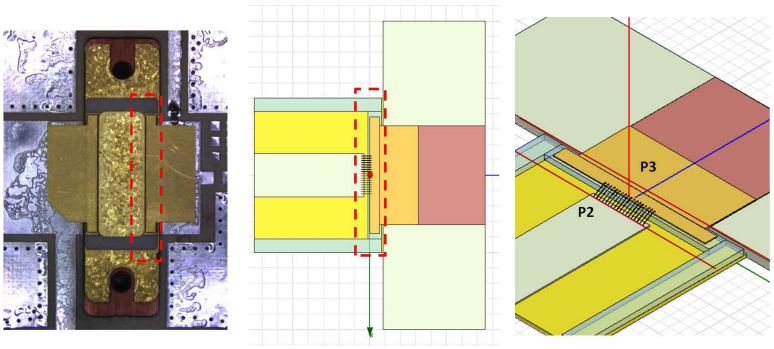


Figure 3.19: Photograph and HFSS simulation of the transformation between a transistor and microstrip circuit edge through bond wires and the RF705 package.

[11] computer aided design

[12] gold tin

transformation can be roughly approximated below 4.7 GHz as a shunt capacitance of 1.8 pF at plane P2 and a shunt capacitance of 3.5 pF connected by an inductance of 320 pH. A resonance occurs at 4.7 GHz, indicating the difficulty of 3rd harmonic impedance control through the transformation. This package is unsuitable for harmonic-tuned applications at 2.14 GHz.

In the case of this package a much simpler analysis, based only on the width of a required microstrip transmission line used to interface between the PA output circuit and the transistor, yields the same result. Gupta et. al. [91] discusses a number of issues which impact the maximum useful frequency for microstrip lines. The cutoff frequency of the first higher-order mode can be approximated as the following:

$$f_c = \frac{300}{\sqrt{\epsilon_r}(2W + 0.8h)} \tag{3.5}$$

where W and h are specified in millimeters and f_c is in GHz. Higher order radiating modes can also be excited at transmission line discontinuities. Significance of radiating modes can be determined using the radiating Q-factor of a $\lambda/2$ resonator, approximated by the following:

$$Q_{rad} = \frac{3\epsilon_r}{8h^2}\left(\frac{\lambda_o}{2}\right)^2 \frac{Z_o}{120\pi} \tag{3.6}$$

Radiation loss is of concern for transmission lines with a low radiating Q-factor of, perhaps, less than 50. Radiating Q and cutoff frequency for a typical substrate (30-mil Rogers 4350B) are shown in Fig. 3.20 for various microstrip line widths. Low values of Q_{rad} imply that energy is easily transferred to the radiating mode. For example, the 10Ω line on this substrate will radiate 10 times more effectively at 6 GHz compared to 2 GHz.

Though this package is widely used for LDMOS 2 GHz class AB applications, it exhibits a very low value of radiating Q and cutoff frequency at 6 GHz for the 13.5 mm microstrip line. This simple analysis indicates that this package likely is not suitable for harmonic-tuned applications at 2.14 GHz. Special attention must be paid to packaging

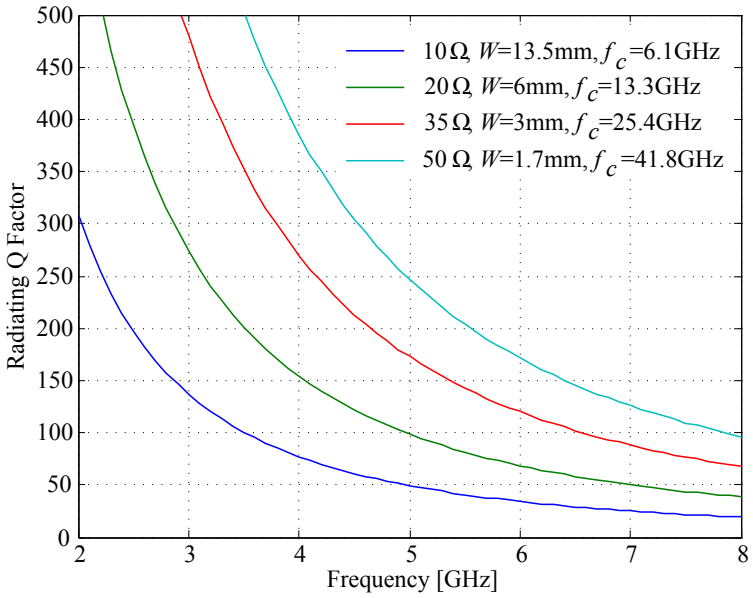


Figure 3.20: Radiating Q-factor for microstrip transmission lines constructed on 30-mil-thick Rogers RO4350B substrate. Transmission line width W, characteristic impedance Z_o, and cutoff frequency f_c for the next higher-order mode are shown in the legend.

when considering harmonic termination of high-power devices. Methods for quantifying and mitigating package limitations are presented next.

3.4 S-Band Class F^{-1} Load Pull and PA Design

In this section a simple, low cost method for control and systematic variation of harmonic impedances based on the block diagram of Fig. 3.21 is described. The source side of the load-pull setup is identical to that described earlier, and only the load side is considered here.

By convention, fundamental frequency impedance is referenced to plane P3 (as in previous sections of this chapter) and harmonic frequency impedances are referenced to plane P1 (as in Chapter 2). Fig. 3.22 shows the position of reference planes P2 and P3 from Fig. 3.21 for two packaging configurations.

Full-wave electromagnetic analysis of these configurations, presented in the next

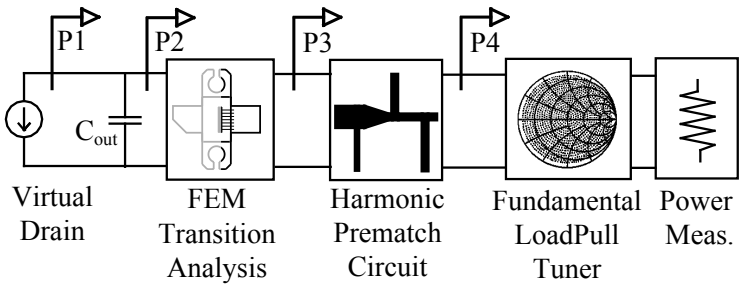


Figure 3.21: Block diagram of the load-pull system including device and package parasitic effects. Transistor virtual drain (P1) is a critical reference plane for high-efficiency operation. The package reference plane (P3) is most frequently used for load-pull and PA design. FEM transition analysis is used to model only the output half of the transistor.

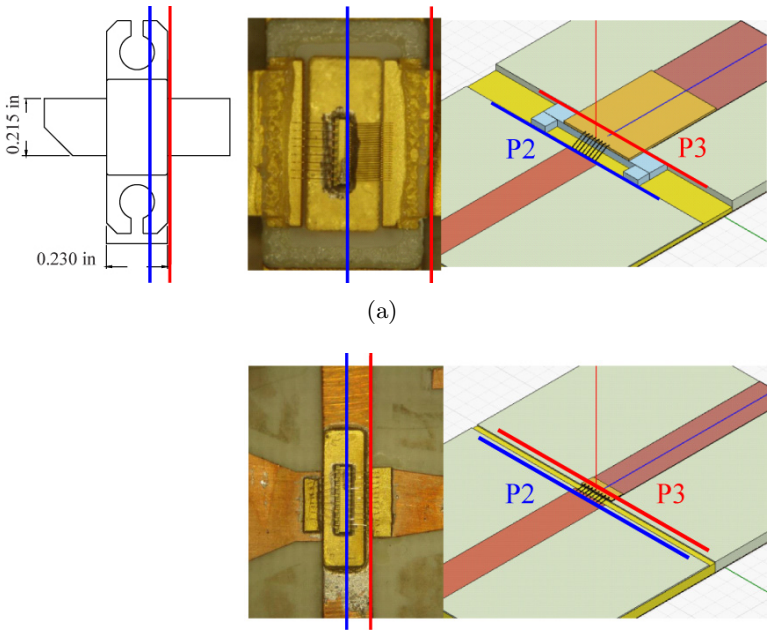


Figure 3.22: Photograph and FEM model for the transformation incurred for a microwave power transistor package (Zentrix RF701) (a), and chip/wire construction for a typical 50 W GaN transistor (b). Both models include eight gold bond wires of 1.25-mil diameter.

section, is used to calculate the impedance at the unmeasurable plane P1 based on the measured impedance at P3. A swept harmonic load-pull method and accuracy verification are described, followed by results from load-pull under varying harmonic conditions.

3.4.1 Feasibility of Harmonic Termination

The ability to terminate harmonics at the virtual drain is determined by device and package characteristics. In this section two 50 W GaN HEMTs are compared. Properties of both GaN HEMTs are summarized in Table 3.2.

Most of the data in Table 3.2 is available from the manufacturer. $R_{L,classAB}$ is the load line resistance at P1 for an ideal class AB design (as in Eqn. 2.2). $Z_{L,classAB}$ is the impedance which must be presented at P2 to realize $R_{L,classAB}$ at P1. $\eta_{R_{on}}$ is the upper-bound on possible efficiency due to on-resistance, as described in Chapter 2 (Eqn. 2.9). Where appropriate, the data in the table is based on a fundamental frequency of 2.14 GHz.

Recall that an open-circuit harmonic termination at P1 requires an inductive harmonic termination at P2 to resonate C_{out}, resulting in a high impedance. In Chapter 2 it was also determined that $3 \cdot R_{L,f_o}$ is the minimum resistance which can be considered an "open" termination. Therefore we can define the impedance with minimum resistance at plane P2 required to present an "open" at P1 for the n-th harmonic frequency:

$$Z_{nf_o,P2} = \frac{1/(j2\pi n f_o C_{out}) \cdot 3 \cdot R_{L,f_o}}{1/(j2\pi n f_o C_{out}) - 3 \cdot R_{L,f_o}} \tag{3.7}$$

Table 3.2: Characteristics of two GaN HEMT transistors.

Metric	DUT1 [92]	DUT2 [93]
Max. Application Freq.	18 GHz	4 GHz
Gate Periphery	10 mm	16 mm
$P_{out,AB}$	50 W	50 W
C_{out}	2.7 pF	7.4 pF
V_k	5 V	7 V
I_{max}	9 A	9.8 A
$V_{dd,AB}$	35 V	32 V
$R_{L,AB}$ at P1	6.7Ω	5.1Ω
$Z_{L,AB}$ at P2	6.6+j0.8Ω	4.8+j1.2Ω
R_{on}	0.10Ω	0.23Ω
$\eta_{R_{on}}$	97%	92%
$Q_{2f_o,open}$	1.2	2.5
$Q_{3f_o,open}$	1.8	3.8

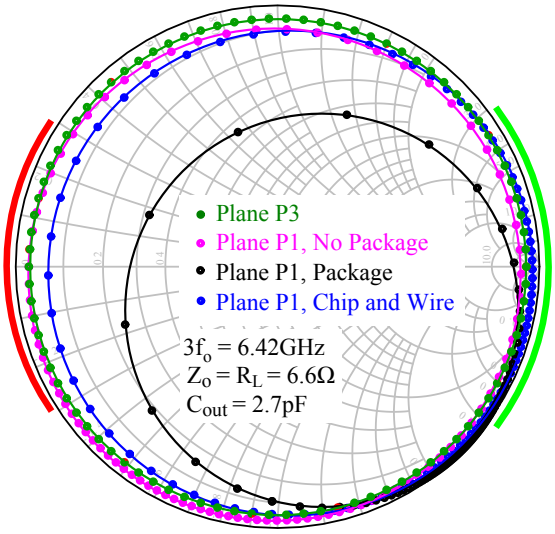
The difficulty of presenting an open harmonic termination at P1 can be quantified by the Q-factor of this impedance, $Q_{nf_o,open}$. Note that larger output capacitance increases the harmonic open-circuit Q-factor, and that $Q_{3f_o,open} > Q_{2f_o,open}$, indicating that a 3rd harmonic open-circuit is more difficult to realize than a 2nd harmonic open-circuit. Conversely, a harmonic short at P2 appears in shunt with the output capacitance. From this perspective, it is easier to accurately present a short termination than an open termination, especially at higher harmonics and when the output capacitance estimate is poor.

DUT1 and DUT2 are characterized in the two package configurations shown in Fig. 3.22. The first is a standard package used for medium-power (50 W) S-band applications [94] (shown in Fig. 3.22(a)). The second is a chip/wire construction in which the die is eutectic-attached to a 15-mil-thick gold-plated CuMo[13] pedestal, which is soldered to an underlying copper block. The die is directly connected to the input and output matching circuits (built with 30-mil Rogers 4350B) by eight 1.25-mil-diameter gold wire bonds. Both configurations are simulated using Ansoft's HFSS FEM software. The ports are de-embedded to planes P1 and P3 of Fig. 3.21. The goal of the analysis is to determine what impedance must be presented by the prematch circuit at P2 to achieve a harmonic short or open at the virtual drain (P1).

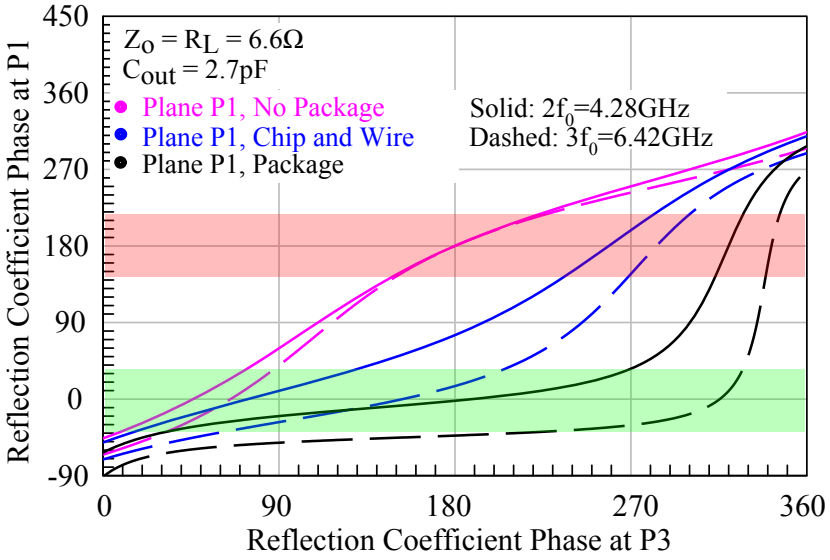
A comparison between two devices in both packaged and chip/wire configurations is shown in Fig. 3.23 and Fig. 3.24. The following conclusions can be drawn from these plots:

- It is important to normalize harmonic impedances to the load line impedance. When presenting an approximate open termination, a reactance of j5Ω is unimportant compared to a 50Ω load line, but unacceptably large compared to a 5Ω load line. Plots are therefore normalized to the load line impedance.

[13] copper molybdenum

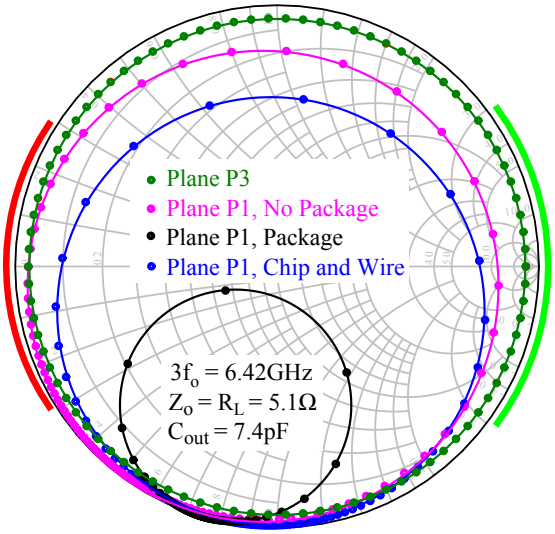


(a)

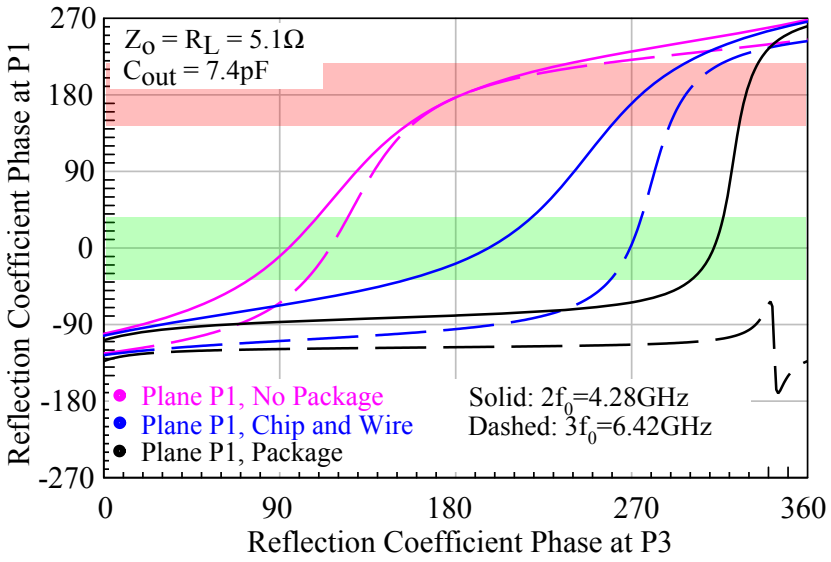


(b)

Figure 3.23: Impedance transformation from P3 to P1 for DUT1 for different package configurations represented by different colors. The Smith chart (a) shows transformation of a constellation of high-reflection-coefficient 3rd harmonic impedances through three package configurations. The rectangular plot (b) is a clear indicator of reflection coefficient phase sensitivity at P1 relative to phase at P3 in each configuration. Sensitivity increases with C_{out} and package parasitics making harmonic termination at P1 difficult. Red and green arcs and bands indicate regions of approximately short and open harmonic termination as defined in Chapter 2. Plots are normalized to the theoretical device load line impedance of 6.6Ω.



(a)



(b)

Figure 3.24: Analysis of Fig. 3.23, repeated for DUT2. Plots are normalized to the theoretical device load line impedance of 5.1Ω.

- Considering only the transformation of C_{out} (magenta), both devices have a reasonable range of phase angle at P3 which result in an approximate short or open at P1 (indicated by red and green bands of the rectangular representations).

- Addition of the chip/wire transformation to C_{out} (blue) has a large impact for DUT2 angle sensitivity at the 3rd harmonic. This corresponds to the significantly

smaller and more irregularly spaced constellation of Fig. 3.24(a). Also, the slope of the dashed blue line in Fig. 3.24(b) is quite steep, indicating a narrower range of angles at P3 which result in an approximate short or open at P1.

- The standard package with C_{out} (black) makes an approximate short or open termination impossible at the 3rd, and difficult at the 2nd harmonic for DUT2.

Conclusions of the analysis have clear implications for load-pull methodology. Package parasitics and C_{out} can clearly restrict the ability to enforce harmonic terminations at the virtual drain. The harmonic terminations of DUT2 in the standard package are nearly fixed under traditional load-pull (fundamental frequency only) due to large parasitic reactances at harmonic frequencies. In chip/wire configuration harmonic impedance of DUT1 can be easily controlled at a 2.14 GHz fundamental frequency.

3.4.2 Swept Harmonic Load Pull Method

High-power fundamental-frequency load-pull is carried out with the addition of pulsed power measurement and harmonic impedance tuning; the measurement setup is shown in Fig. 3.25, corresponding to the block diagram of Fig. 3.21. The pulse duty cycle is 5% and the period is 1 msec.

In the block diagram of Fig. 3.21 the harmonic prematch circuit [5] performs the following functions:

- Transforms the 50Ω fundamental constellation to 5Ω,
- Supplies DC bias near the device drain to avoid large signal oscillation,
- Constrains 2nd harmonic impedance to a single high reflection coefficient value for the whole fundamental impedance constellation, and
- Increases the angle of the 2nd harmonic termination by decreasing the length of a tuning stub, labeled "I" in Fig. 3.25, with only a small impact on the fundamental

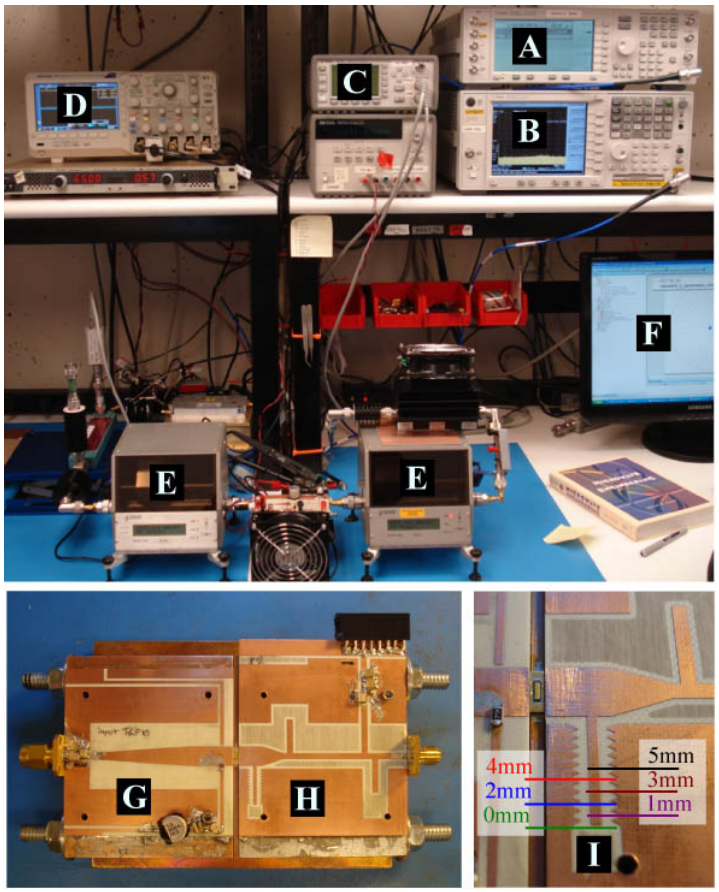
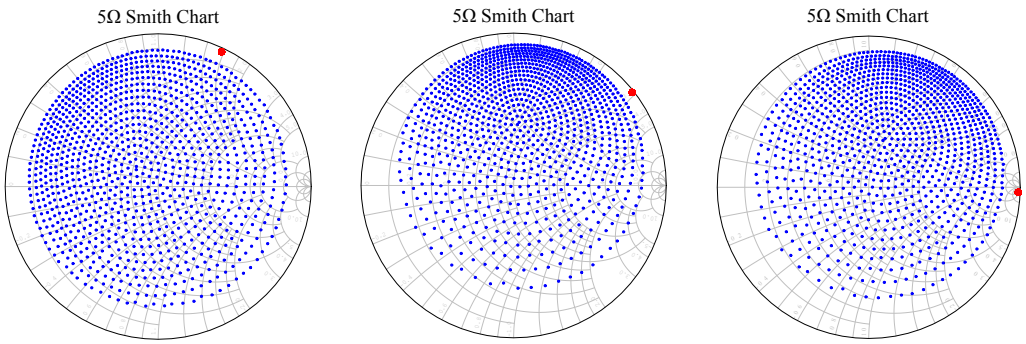


Figure 3.25: Photograph of the load-pull equipment (top) corresponding to the block diagram of Fig. 3.21: A-Agilent ESG4438C Synthesizer, B-Agilent PSA4440A VSA, C-Agilent 4419B Power Meter, D-Tektronix DSO2023 Oscilloscope, E- Focus CCMT-1816 Mechanical Tuners, F-Custom Matlab instrument and tuner control software. Photograph of the load-pull fixture and detail of the harmonic tuning stub (bottom): G-Input prematch transformer to 5 Ω and bias network, H-Output prematch transformer to 5 Ω with bias network, I-Detail of 2nd harmonic tuning stub.

frequency impedance transformation. Note that the tuning stub exists to load the transmission line connecting the device to the resonant stub (shown at the right of the photograph), and reducing tuning stub length makes the electrical distance between the two shorter.

The fundamental and 2nd harmonic constellations at reference planes P3, P2, and P1 are shown in Fig. 3.26. Note the great importance of considering even the low-parasitic chip/wire transformation from P3 to P2.



(a) (b) (c)

Figure 3.26: Load-pull impedance constellation at reference planes P3 (a), P2 (b), and P1 (c) for the fundamental (blue) and 2nd harmonic (red) frequencies.

Two-port S-parameters of the output prematch, mechanical tuner, and output attenuators are separately measured to allow de-embedding of resistive and reflection loss at each fundamental impedance in the load-pull constellation. The input and output prematch blocks are built as break-apart fixtures [5], allowing S-parameter measurement using a microstrip TRL calibration kit.

Two identical prematch circuits are constructed, one for S-parameter measurement (A) and one to remain permanently wire bonded to the device (B) thus eliminating parasitic variations and limiting potential for damage to the device. Both circuits' 2nd harmonic stubs are tuned identically so that S-parameters from A can be de-embedded from the load-pull measurements made using B. The accuracy of this method is verified after tuning the 2nd harmonic termination by measuring small-signal gain contours as shown in Fig. 3.27.

Varying harmonic termination should change large-signal transistor performance, but small-signal gain at a given fundamental frequency impedance should remain constant. Five of the contours are tightly grouped, indicating that the measured S-parameters of A match the S-parameters of B, and power measurement error is acceptably small. The dashed-red curve shows an instance where the calibration check failed, indicating that A measurements did not match that of B, and must be repeated.

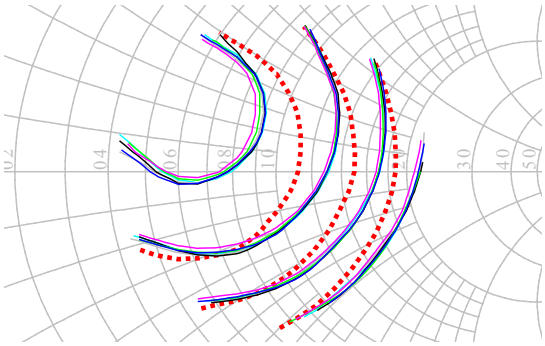


Figure 3.27: Small-signal gain contours for six prematch harmonic terminations are used for validating load-pull calibration. Disagreement of dashed red contour indicates a calibration error. The Smith chart is normalized to 5Ω.

3.4.3 Load Pull and PA Prototype Results

Swept-harmonic load-pull procedure was performed for the GaN HEMTs (DUT1 and DUT2) described earlier in this section. Consistent with the feasibility analysis, harmonic tuning did not have a notable impact on efficiency as compared to standard class AB operation for DUT2 using standard microwave packaging. From this we can surmise that the harmonic termination at P1 is dominated by the package and output capacitance and could not be adequately varied by harmonic impedance variation at P3. Some variation in drain efficiency with harmonic termination at P2 was noted for DUT2 in chip/wire configuration; maximum efficiency did not exceed the maximum efficiency achieved using standard microwave packaging. As predicted by the analysis, DUT2 was found to be unsuitable for harmonic-tuned operation at 2.14 GHz. The remainder of this section presents details of the swept-harmonic load-pull and results for DUT1.

DUT1 was biased at 28 V drain supply with a class AB bias of 300 mA. High v_{ds} peaks are possible in harmonic-tuned operation, as noted in the class E analysis of Chapter 2. Drain voltage is reduced from the suggested class AB bias point by 20% for the initial harmonic sweep to prevent such peaks from exceeding V_{break}. Source-pull was first performed to optimize small-signal gain, followed by large-signal load-pull measurements at the six 2nd harmonic reflection coefficient angles shown by colored dots

in Fig. 3.28, referenced to the virtual drain at P1. At each impedance point input power was increased until gate current measured 20 mA, corresponding to an approximately consistent level of gain compression. Fig. 3.28 shows power and drain efficiency achieved at each harmonic termination. The figure also illustrates the required modification to the prematch circuit to achieve each harmonic termination. The highest efficiency region (77%) is achieved with 2nd harmonic nearest an open circuit (blue). In this case the 3rd harmonic was not explicitly controlled, but was nearly fixed at a capacitive impedance.

Next we investigate the impact of 3rd harmonic control. Another output prematch circuit was designed to terminate 2nd and 3rd harmonics in an open and short at P1, respectively (the class F^{-1} condition). Fig. 3.29 compares results from this measurement to the 2nd-harmonic-only measurement of Fig. 3.28. Intentional termination of the 3rd harmonic with a short at P1 increases transistor drain efficiency by 8% without reducing output power.

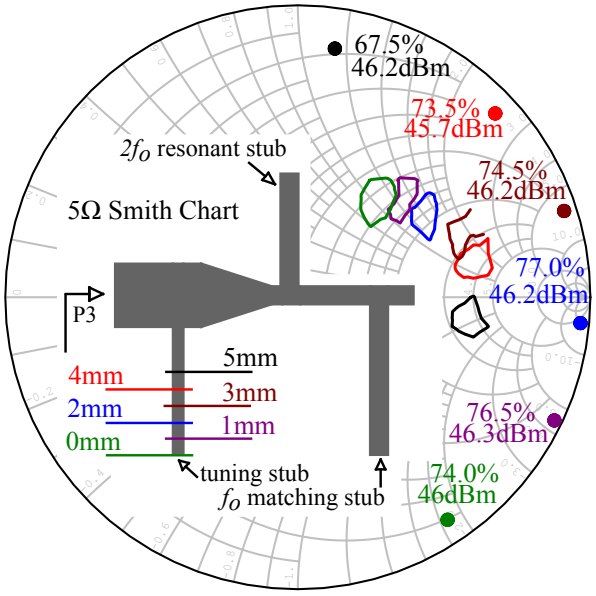


Figure 3.28: Fundamental frequency constant drain efficiency contours (referenced to P3) shown in colors that correspond to six 2nd harmonic terminations (dots, referenced to P1). Efficiency and maximum power of each contour is indicated next the corresponding harmonic termination dot of the same color. The Smith chart is normalized to 5Ω.

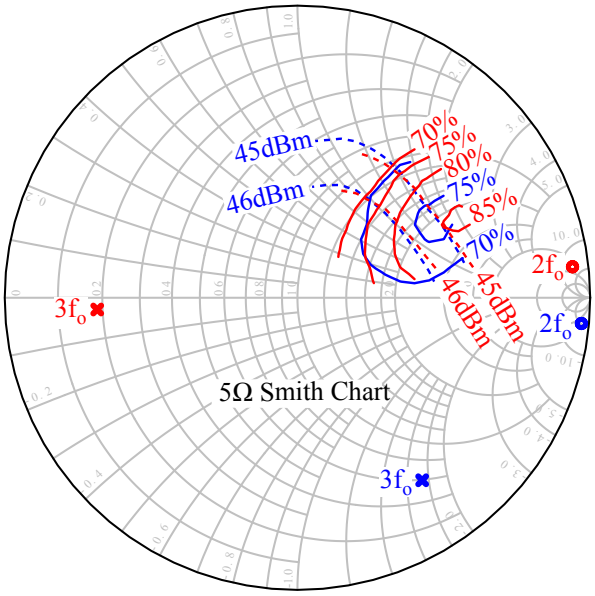


Figure 3.29: Power (dashed) and drain efficiency (solid) load-pull contours with two different harmonic environments (red and blue, referenced to P3). Both sets of 2nd (o) and 3rd (x) harmonic terminations are shown referenced to plane P1. The Smith chart is normalized to 5Ω.

A prototype PA was designed using results of the measurements in Fig. 3.29. A fundamental load impedance of $10.2 + j6.2\Omega$ was presented at plane P3 with 0.27 dB insertion loss in the output matching circuit. 2nd and 3rd harmonic impedances approximate an open and short at plane P1 similar to those shown Fig. 3.29. Fig. 3.30 shows the measured and simulated output impedance of the final PA prototype.

A load-pull method is presented to systematically sweep harmonic termination and is verified by the prototype PA performance, resulting in a high-efficiency class F^{-1} PA prototype. A photograph of the prototype is shown in Fig. 3.31. The die is mounted on a CuMo gold-plated pedestal using AuSn eutectic solder. The pedestal is soldered to the copper block below, providing a low-resistance thermal path. SMA connectors are used at the 50Ω PA input and output terminals. The matching circuit is made from 30-mil 1-oz copper-clad Rogers RO4350B substrate with ϵ_r=3.5. The circuit is soldered to the copper block below with a reflow process, ensuring ground plane continuity between the SMA connectors, matching circuits, and die. Impedance matching at the input and

output is achieved with a combination of lumped and distributed techniques. Capacitors are from the American Technical Ceramics (ATC) 600S or 100B series, depending upon desired loss, resonance, and form factor characteristics. Harmonic terminations are realized by transmission line stubs.

Input and output bias networks use a quarter-wave transmission line choke, where one end is terminated in a narrow-band short formed by a resonant ATC 100B capacitor. The gate bias tee connects to the DC supply using banana jacks, and the choke includes a 10Ω resistor. In saturated operation this resistor passes gate current, developing a voltage and varying V_{gg} at the transistor. Both bias networks include bypass capacitance on the DC supply side of the RF choke. The PA drain supply is connected via a 100-mil double-row Molex header to a pulse-power measurement board, containing a current measurement loop and large bypass capacitors to prevent drain voltage sag during the pulse. The 100-mil header interface is also required for work in Chapter 5, where this

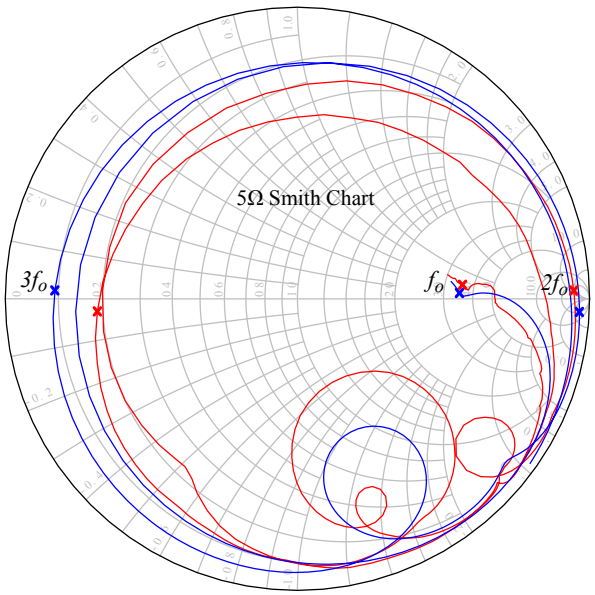


Figure 3.30: Simulated (blue) and measured (red) output impedance for the 36-W class F^{-1} S-band prototype at plane P1. Simulated and measured fundamental load impedances were 17.4+j1.0 Ω and 17.8+j2.4Ω, respectively. The Smith chart is normalized to 5Ω.

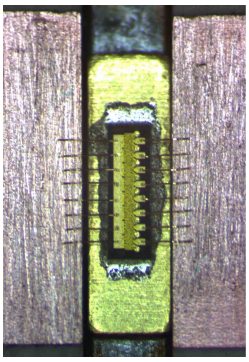
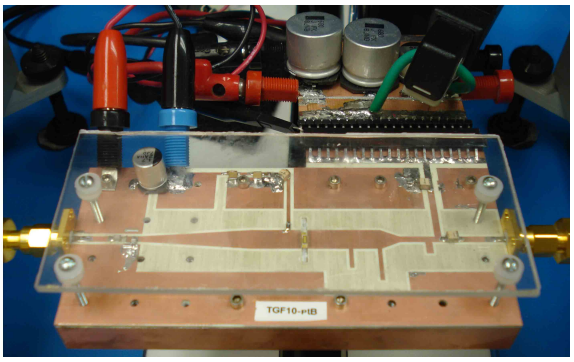



Figure 3.31: Photograph of the TGF2023-10 die (left, detail blurred). The complete fabricated PA prototype is shown at the right.

PA is integrated with an envelope modulator in an envelope tracking system.

Output power of 36 W was measured with 14.5 dB gain and 81% drain efficiency, or 78% PAE at 2.14 GHz, consistent with load-pull characterization results. Further details of PA performance are presented in Chapter 5, where this PA is used in an envelope tracking system.

3.5 Conclusion

Important features of general load-pull configuration, calibration, and measurement were discussed followed by two examples with varying output power, frequency, mode of operation, device technology, and input stimulus. New load-pull techniques were introduced in both cases to enable and enhance measurement for high-efficiency operation. Contributions described in this chapter include the following:

- Development of a harmonic load-pull characterization methodology used with variety of transistors at UHF [38] [39] [48]. The methodology is verified by design of many high-efficiency class E UHF power amplifiers with up to 100 W and efficiencies up to 90% [40] [5] [41], and illustrated in this work using a class E LDMOS PA at 360 MHz, resulting in greater than 83% drain efficiency, 110 W output power, and 16.0 dB gain [6].

- Extension of the load-pull method including full-wave electromagnetic analysis of microwave packages parasitics and alternative construction methods to determine and enhance feasibility of effective harmonic terminations. These techniques are illustrated in this work using a class F^{-1} PA at 2.14 GHz resulting in greater than 81% drain efficiency, 36 W output power, and 14.5 dB gain [2].

Chapter 4

Envelope Tracking Components and Simulation

Contents

Chapters 2 and 3 focused on improving efficiency of the PA in compressed operation at peak output power. This chapter applies supply modulation to achieve high-efficiency compressed operation over a wide range of output power levels. A general ET transmitter is developed (shown in Fig. 4.1) which utilizes both drive and drain modulation, followed by a discussion of PA and envelope modulator hardware requirements and limitations. A block called the signal split is introduced to control the ratio of drain modulation to drive modulation, and is used to trade PA efficiency and EM requirements. A simulation method is developed for modeling the impact of component

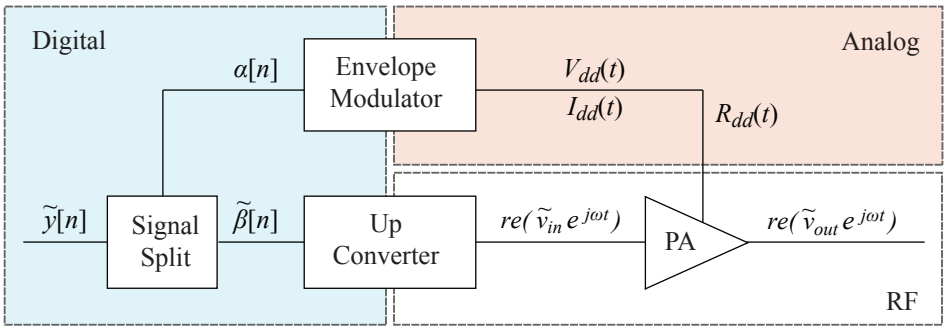


Figure 4.1: Simplified block diagram of the ET transmitter system. The PA is driven with an input signal $\tilde{v}_{in}$ modulated with both amplitude and phase, and the envelope modulator (EM) varies drain voltage V_{dd}. At low output power levels drain voltage is reduced, causing PA gain compression and thus improving PA efficiency. Digital algorithms pre-correct the PA input signal to account for variations in PA gain and insertion phase, achieving system linearity from input $\tilde{y}$ to output $\tilde{v}_{out}$.

non-idealities on system performance, starting from hardware measurement data. An example analysis evaluates tradeoffs between ET system linearity, PA efficiency, and EM requirements for a W-CDMA downlink transmitter.

4.1 Supply Modulation

High-efficiency PA theory and designs described in Chapters 2 and 3 provide significant improvement in PA efficiency in compressed operation. Efficiency still drops quickly as output power is reduced and the PA operates in an ever-more linear regime. Amplitude-modulated signals such as W-CDMA have probability distributions weighted far away from maximum output power, resulting in inefficient operation at the average power level. Fig. 4.2 shows PA performance over instantaneous output power along with the PDF for a typical 8 dB PAR W-CDMA test signal. For example, the blue line with square markers of Fig. 4.2 shows PAE for a class AB 120-W PA based on a GaN HEMT transistor at 2.14 GHz. The PA has over 60% PAE near the maximum output power, but efficiency falls quickly as power level decreases. The average power of the 8 dB PAR W-CDMA signal is produced with less than 25% PAE.

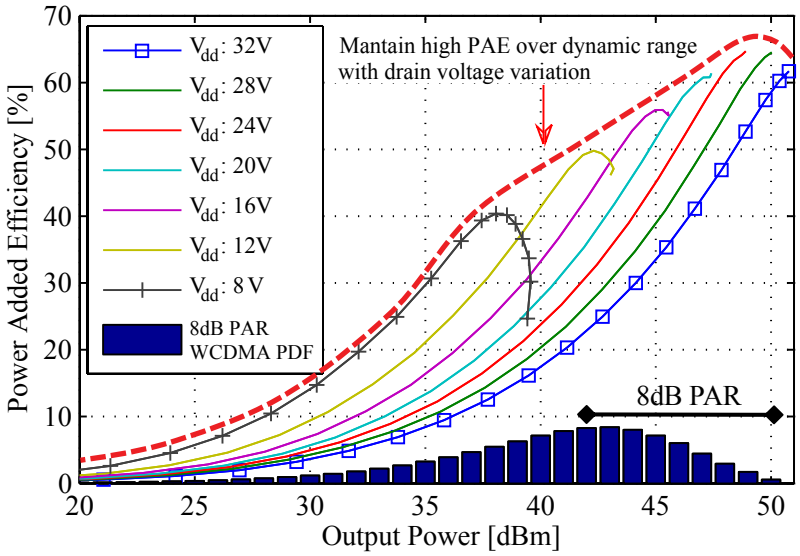


Figure 4.2: Measured efficiency vs. output power for varying drain voltage for a 2.14 GHz class AB PA prototype. The PDF of an 8 dB PAR W-CDMA signal is shown in the PDF bar plot.

The solid lines of Fig. 4.2 show PA performance at varying drain supply voltage levels, indicating that the average power level of 42 dBm could be produced with 50% PAE if voltage were reduced to only 12 V. Supply modulation techniques aim to continuously vary drain supply voltage, maintaining efficient saturated PA operation over a wide range of output power levels as shown by the dashed red line in Fig. 4.2.

The first application of supply modulation was introduced by Kahn [19] in 1952 in the form of EER, described earlier in this thesis. Kahn, along with many other authors (e.g. [1] [95]), viewed supply modulation as a method for restoring amplitude linearity to efficient, nonlinear PAs. By contrast, the ET technique used in this work begins with a fundamentally linear PA. Supply modulation is applied to achieve efficient PA operation at the expense of linearity. Digital techniques are developed and applied to restore system linearity. Classical EER supply modulation also does not make use of input power level modulation. The heavy drive required to achieve saturation at peak output power causes distortion and wasted input power at low output power levels. For high-PAR signals, and also when the signal is required to instantaneously achieve near

zero output power, some level of drive modulation is desirable [20].

Nomenclature in the literature is somewhat inconsistent and many authors choose new names for similar concepts. The definition of envelope tracking used here is based on several excellent and leading references ([96] [21] [28] [10] [97]): Drain voltage of a fundamentally linear PA is varied to maintain saturation and to improve modulated PA efficiency.

A great deal of work has been done in this area with varying modulation types, output power levels, center frequencies, and device technologies. Each application poses unique challenges to different parts of the system. For example, a low-power application at X-band with narrowband modulation [23] will naturally involve smaller EM voltage and current swings, easing that aspect of the EM design task. However, high-frequency efficient PA design and integration into the system is a larger challenge than at lower frequencies.

In this work the target application is a W-CDMA downlink transmitter with 10-200 W peak output power at 2.14 GHz. The combination of power level, modulation signal, frequency, and stringent linearity requirements create major challenges in all three aspects of the ET system:

RF – High power relative to the center frequency requires new high-efficiency techniques described in Chapters 2 and 3,

Analog and Power Electronics – High-PAR signal and high peak drain voltage and current requirements demand new EM architectures and careful attention to the EM-PA interface, and

Signal Processing – Linearity requirements force the use of new and more complex correction algorithms and high signal bandwidth requires a high degree of timing precision.

Transmitters with similar requirements have been investigated in the literature [29]

[30] [31] with excellent results. This thesis work takes a system-level approach to the problem, contributing an ET framework and system simulation tool used to analyze the impact of component performance on system performance. The signal split concept proves useful for trading PA performance with EM linearity requirements, resulting in new transmitter architectures.

Fig. 4.1 is a highly simplified block diagram of the system implemented in this work. As in Chapter 1, variables beneath a tilde (e.g. $\tilde{y}[n]$) indicate complex vectors. Variables such as $\alpha[n]$ indicate discrete digital signals while $v(t)$ indicates continuous analog signals. A desired signal $\tilde{y}[n]$ is used to create digital drain voltage $\alpha[n]$ and complex baseband $\tilde{\beta}[n]$ components. Many combinations of $\alpha[n]$ and $|\tilde{\beta}[n]|$ exist which would produce the required output magnitude, each with a different impact on insertion phase and PA efficiency. The signal split defines the combinations of $\alpha[n]$ and $|\tilde{\beta}[n]|$ which should be used to obtain a desired output power and can be designed to maximize PA efficiency or EM efficiency. The PA insertion phase for each output power level is known, and the signal split pre-corrects $\tilde{\beta}[n]$ to maintain constant PA insertion phase.

A wide range of dynamic distortion mechanisms accompany the static distortion (insertion gain and phase variation) incurred by varying the PA drain voltage. Digital techniques will be introduced in Chapter 5 to identify and deal with dynamic issues.

4.2 Envelope Modulator

While design of the EM hardware is outside the scope of this work, some level of understanding is crucial for system integration. At the system level it is easy to optimize for high PA efficiency without regard for the impact on EM efficiency or linearity requirements. As in PA design, linearity and efficiency are continually opposed in EM design. It is clear from the simple block diagram of Fig. 4.1 that distortion in the EM will impact system linearity to some degree. The simulation tool described in this chapter

is used to determine the level of EM distortion which can be tolerated in exchange for EM efficiency. The ability to account for EM operation and design tradeoffs is critical in achieving a high-performance ET system.

Design of the many EM prototypes used throughout this work was performed by collaborators in the field of analog and power electronics - primarily Mr. Mark Norris, a Ph.D. candidate at the time studying under Prof. Dragan Maksimović at the Colorado Power Electronics Center (CoPEC). If there is only one point made in this chapter, it should be that design of ET components cannot be done in isolation. Analog, RF, and system engineers must effectively communicate the challenges, limitations, and tradeoffs in their design tasks to achieve a high-performance system.

4.2.1 EM Requirements for Linearity

The EM is generally responsible for amplifying a voltage waveform, but more specifically:

- with a certain minimum and maximum output voltage level,
- with flat gain and insertion phase over a specified bandwidth,
- with given maximum short- and long-term slew rates, and
- while driving a time-varying load.

The first and second requirements are opposed due to the same problem facing high-frequency high-power RF devices: realizable high-power devices incur large capacitance, limiting maximum speed. High-speed processes and off-the-shelf parts are limited in voltage and power handling capability. For example, many components offer to 36 V maximum supply rails and require several volts of headroom to maintain linearity, incurring a 30 V output dynamic range voltage. Architecture may allow a DC offset to be applied to the output voltage range to allow higher peak voltages at the expense of higher minimum voltage. The maximum and minimum drain voltages available to the PA impact PA efficiency (shown later in this chapter).

Many analog applications intentionally make use of gain peaking to extend bandwidth, but in this case a flat EM gain is desired to maintain V_{dd} linearity (and thus system linearity). In Chapter 5 flat EM gain and group delay are achieved using a linear equalizer, allowing the hardware to retain the extended bandwidth associated with gain peaking.

Bandwidth and frequency response are small-signal measurements, only valid for purely linear operation. For example, inadequate bandwidth can be observed by increasing the frequency of a very low-amplitude input sine wave and watching the output waveform decrease in amplitude as gain rolls off. Slew rate, conversely, is a measurement of large-signal phenomena. As an example, a fast voltage ramp into a low-impedance load may deplete the charge stored in EM decoupling capacitors, causing the EM supply voltage rail to dip. The resulting output signal distortion is the result of inadequate slew rate capability. A wide variety of complex transistor, component, and circuit problems can be responsible for this type of behavior.

Bandwidth and dynamic performance requirements for an EM *cannot* be estimated based on the bandwidth of the complex modulation. Some references generalize that EM bandwidth should be 3x-5x the modulation bandwidth. Instead, the required EM bandwidth is related to the bandwidth of the *amplitude* of the complex modulation. GMSK[1] modulation with 4 MHz double-sided complex modulation bandwidth has a constant amplitude, with 0 KHz modulation bandwidth. In this case the EM must have bandwidth equal to "0x" the complex modulation bandwidth (no EM is required), showing the 3x-5x rule to be faulty. Conversely, consider the spectrum of the four-tone signal shown in Fig. 4.3.

Though the in-phase and quadrature components are nicely band-limited to 4 MHz (double-sided, just as the GMSK signal) note that the amplitude component has frequency components extending far beyond that bandwidth, so the degree of amplitude

[1] Gaussian multiple shift keying

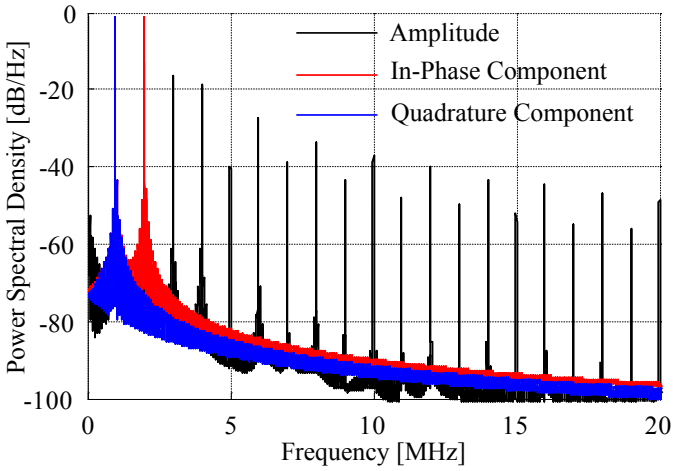


Figure 4.3: PSD of the in-phase, quadrature, and amplitude components of a four-tone signal.

bandwidth expansion depends upon the structure of the modulation. Complex modulation signals with amplitude passing through zero will have sharp amplitude nulls in the time-domain; amplitude quickly descends to zero before instantly changing direction and increasing toward a peak. This feature can be observed in the time-domain plot of W-CDMA amplitude shown in Fig. 1.6. The PSD of the in-phase, quadrature, and amplitude components is shown in Fig. 4.4. More than 85% of the spectral power of the W-CDMA amplitude signal is concentrated below 300 kHz, and the higher-frequency portion of the signal has significant content beyond the in-phase or quadrature component bandwidth.

The signal split applies a nonlinear transformation to this waveform (described in more detail later in this chapter), changing its time-domain characteristics and further complicating the issue. The waveform bandwidth may be either expanded or condensed depending upon the design of the signal split. Therefore, the required EM bandwidth and dynamic performance is not straightforward to predict, since the input signal depends on both system configuration and modulation signal characteristics.

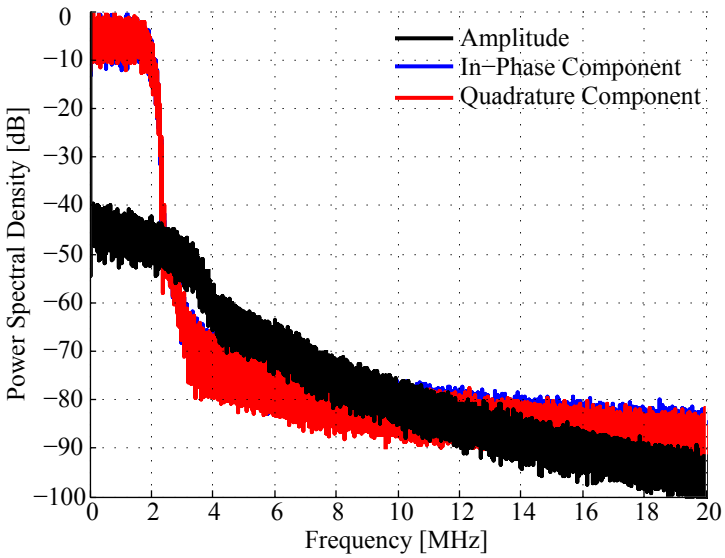


Figure 4.4: PSD of the in-phase, quadrature, and amplitude components of a W-CDMA downlink signal.

The load driven by the EM ($R_{dd} = V_{dd}/I_{dd}$) at the PA drain supply terminals is referred to as the drain resistance, shown in Fig. 4.1. Carefully note that this is not directly related to the PA load line or any RF impedance and is constant over the RF cycle by virtue of the RF choke. R_{dd} varies with PA output power and efficiency as follows:

$$R_{dd} = \frac{V_{dd}}{I_{dd}} = \frac{V_{dd}^2 \eta_d}{P_{out}} \tag{4.1}$$

Later in this chapter it will be shown that the variation is dependent upon design of the signal split.

Consider an op-amp driving a load which steps from 3Ω to 100Ω with a constant voltage. A small EM output impedance of 1Ω will cause an insignificant voltage division with a 100Ω load, but will cause a significant voltage error with the 3Ω load. Negative feedback will effectively lower the output impedance, but is subject to frequency response. Output impedance control is found to have a large impact for high-power applications where R_{dd} can easily swing between 3Ω and 100Ω for a reasonably efficient 100 W PA. Therefore output impedance of the EM is kept low over a wide frequency

range to limit V_{dd} error at the PA drain due to voltage division between EM output impedance and PA load impedance.

The gain and delay of the EM are impacted by more complex mechanisms than can be discussed in this work. Practical designs optimized for efficiency exhibit changing behavior with frequency, slew rate, varying DC signal amplitude, varying AC signal amplitude, DC load, and load variation. Variation in small-signal frequency response (100 mV peak-peak) at 10 V DC is shown in Fig. 4.5 for three different DC loads. High gain peaking at 40-50 MHz is used to extend the useful bandwidth and will be flattened with a digital equalizer in Chapter 5. The equalizer can attenuate the frequency response (to flatten the gain peaking which occurs between 20 MHz to 65 MHz) but has limited capability for amplifying high-frequency components (as would be necessary above 65 MHz). After equalization the EM characterized in Fig. 4.5 has about 65 MHz bandwidth where gain is 31 dBV. The variation with load means that the same linear equalizer will not provide a good correction under all load conditions.

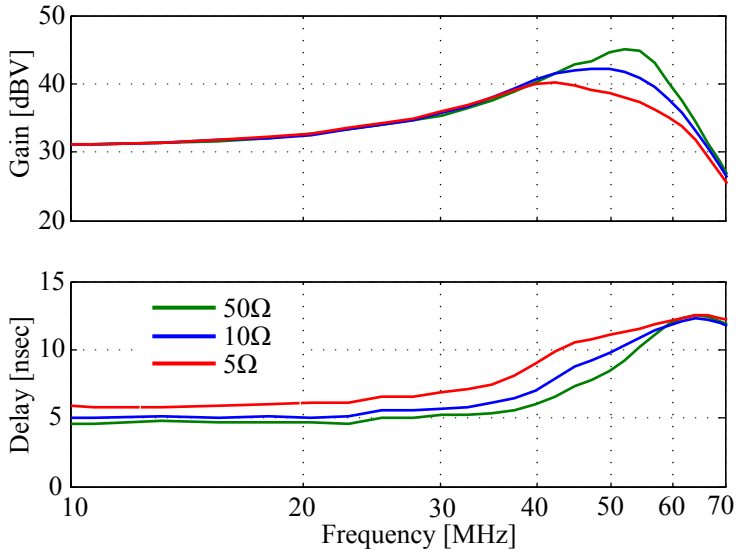


Figure 4.5: Measured small-signal frequency response for an EM prototype under varying DC loads. Excitation signal is a frequency chirp of 100 mV with a 10 V DC component.

The problem of frequency response variation with load is only one example of the difficulty of completely specifying EM fidelity requirements. Some level of frequency response variation under light load will likely provide an acceptably linear ET system. However, the quantitative amount of acceptable variation is system- and signal-dependent, and also depends on the other non-idealities simultaneously involved.

EM bandwidth, slew rate, and output impedance required to reproduce the V_{dd} signal "accurately enough" to achieve system linearity is a function of the input signal, the PA behavior, and the signal split. Reduced EM dynamic requirements lead to improved EM efficiency, but also force a signal split resulting in lower PA efficiency. The system simulation method presented in this chapter quantifies these relationships.

4.2.2 EM Architecture for Efficiency

ET system efficiency is the ratio of all power consumed to average output power delivered. Therefore EM efficiency must be high to minimize the impact on system efficiency. Purely linear amplifiers are inherently inefficient and unsuitable for the EM design. The SMPS[2] class of DC-DC converters [65] share much of the same theory as the switching amplifiers described in Chapter 2 and have high efficiency but low bandwidth and linearity. For example, [22] used an EM comprised of an SMPS with 4.33 MHz switching frequency and a 1.3 MHz output filter. The transmitter met spectral requirements of the 270.8 kHz-bandwidth EDGE downlink signal. Similar bandwidth-frequency ratios for the W-CDMA system in this work would call for SMPS switching frequencies higher than are practically realizable. The class S EM architecture suggested by Raab et. al. [95] can be thought of as a pulse-width modulated amplifier with a very high switching frequency. This technique showed excellent performance in an EER system for using two-tone modulation signals of up to 150 kHz bandwidth. The W-CDMA signal has RF bandwidth more than 30 times larger, making the class S design similarly unsuitable

[2] switched-mode power supply

for use in this work.

Many EM designs in literature utilize a combination of linear and SMPS blocks to produce high- and low-frequency components. Band separation [98] divides the desired signal into the two components in the digital realm, while other techniques utilize analog control of either the SMPS or linear blocks based on performance of the other component. A simplified circuit diagram of the EM used in this work is shown in Fig. 4.6, and is based on the configuration described in [28].

The linear amplifier provides current to the load through a small sense resistance. The SMPS controller opens and closes the switch Q_1, ramping inductor current up and down in an effort to minimize current which must be supplied by the linear amplifier. The SMPS responds slowly with bandwidth on the order of 300 kHz, and the linear amplifier has very high bandwidth up to perhaps 80 MHz. The simulated waveforms shown in Fig. 4.7 illustrate the SMPS and linear amplifier current contribution when driving the W-CDMA envelope voltage into a constant resistive load. The SMPS produces the contents of the signal within its useful bandwidth (shown in red) very ef-

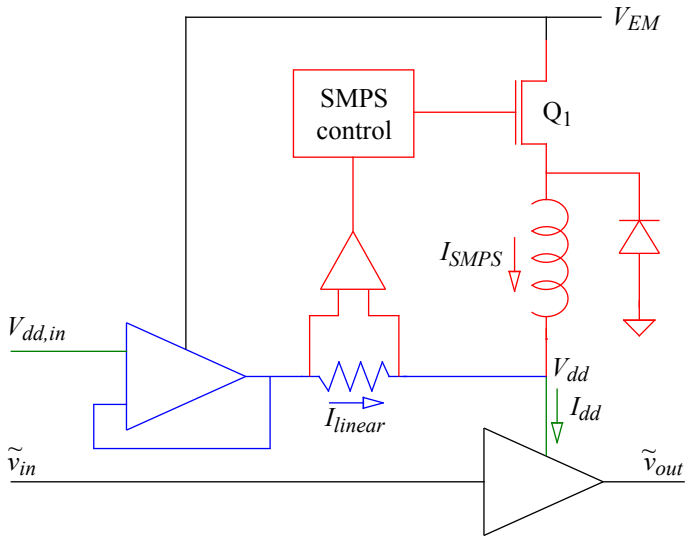
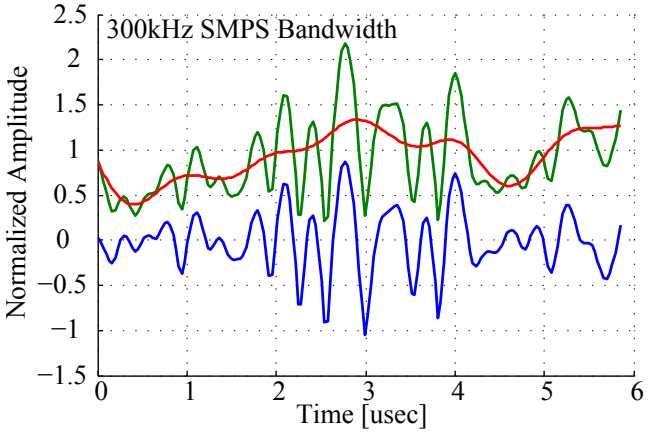
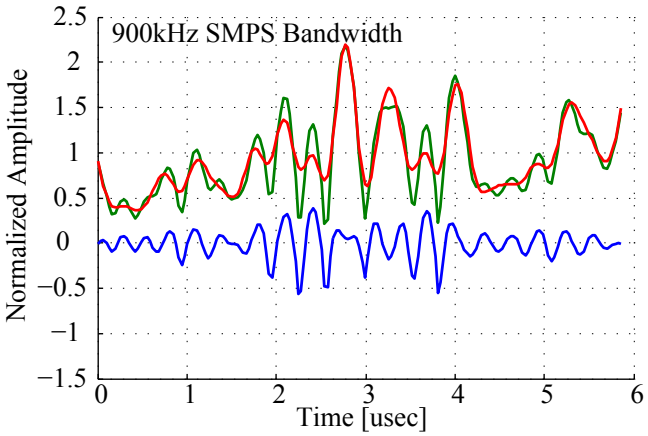


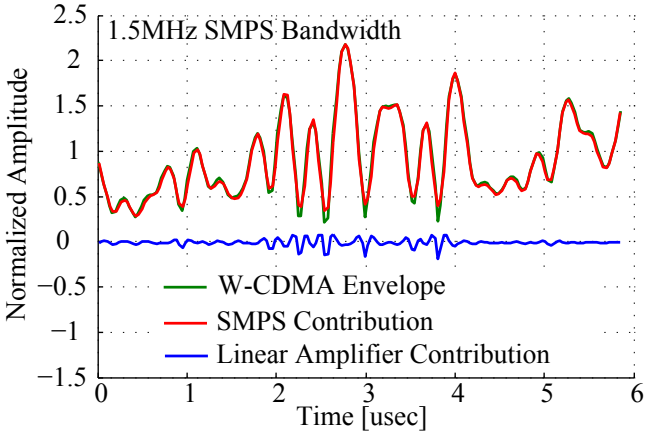
Figure 4.6: Block diagram of an EM architecture using a SMPS supplemented by a linear amplifier.



(a)



(b)



(c)

Figure 4.7: Ideal W-CDMA envelope and simulation of SMPS and linear amplifier components considering three different SMPS bandwidths. Vertical scale is normalized to the RMS value of the ideal W-CDMA envelope.

ficiently, while the linear amplifier contribution (shown in blue) provides the difference between the SMPS output and the desired output. As the SMPS bandwidth increases less low-efficiency linear amplifier correction (blue) is required to achieve the desired output waveform. However, high-bandwith SMPS design also results in reduced SMPS efficiency; optimal design of a SMPS-linear EM requires careful investigation of these tradeoffs in order.

Depending upon implementation, SMPS efficient may be more than 90% while the linear amplifier is only 30% efficient. Thus, high-frequency content is produced much less efficiently than is low-frequency content. Fortunately, about 85% of the W-CDMA envelope energy is concentrated below 300 kHz as shown in Fig. 4.4, and can be reproduced by the efficient SMPS.

If the SMPS sources less of the required dynamic current peak linear amplifier current requirements are increased. Higher peak current requires a more capable linear amplifier design. The larger linear amplifier will dissipate more quiescent current, degrading EM efficiency. In the same way, increased EM linearity can be gained at the expense of a more powerful, inefficient, linear amplifier design. These decisions are made at design time, and cannot be easily scaled or modified during operation. The goal of ET system simulation tool is to determine at design time what type and amount of EM nonlinearity can be allowed at the system level in exchange for additional EM efficiency.

4.2.3 EM-PA Interface

Impedance between the EM output and PA drain cause distortion in the output voltage waveform with varying current, similar to the effect of non-zero op-amp output impedance. In early experiments the EM and PA were connected with a BNC cable, which was later found to be the source of significant V_{dd} distortion. Resistance and inductance of a cable connecting the two incurs a significant system linearity penalty, so a double-row 100-mil-pitch header is used to connect the PA and EM [43] to minimize

interconnect impedance. The pulsed-power measurement circuit board is connected to the PA using such a connector in Fig. 3.31. Additionally, the EM feedback loop sense point was placed on the PA side of the interconnect so that the closed loop gain of the linear amplifier rejects some V_{dd} distortion caused by the interconnect impedance.

A traditional PA bias tee includes significant bypass capacitance which provides a low-frequency termination, enhancing PA stability. The EM cannot be made to efficiently drive a large capacitance at a high speed, so the bias tee capacitance must be eliminated. Fortunately, the EM provides a low output impedance over a range of low frequencies, emulating the low-impedance low-frequency termination of a traditional PA bias network. PA bias networks for ET application is discussed further in the next section.

In the linearized system, even insertion of a current probe to measure instantaneous current results in a decrease of ACP1 from -52 dBc to -43 dBc, indicating a significant change in instantaneous drain voltage, though average RF output power remains constant. Inability to measure drain current without impacting system linearity makes it difficult to gauge EM efficiency under real ET conditions and emphasizes the importance of a low-impedance interconnect.

4.3 Power Amplifiers for Envelope Tracking

Chapters 2 and 3 described theory and design of PAs for CW and pulsed applications. Like most PA designs, these applications have fixed drain supply voltage, constant quiescent current, and some static thermal load. ET operation changes many of these assumptions and requires a new PA design method for optimal ET efficiency. It is impossible to predict how an RF transistor will perform in an ET system based upon characterization in standard conditions. An RF transistor datasheet performance and suggested application circuit is optimized for a specific modulation or pulsed mode of

operation, almost certainly not the ET mode of operation.

The next chapter will compare a standard drive-modulated PA to the same PA operated in ET mode, showing that power dissipated in the transistor drops from 19.8 W to only 2.7 W. The transistor thermal load is only 13.6% of that which the transistor was designed for, leading to improved RF performance. Reduced thermal load requirements also opens possibilities for the design of ET-application-specific microwave transistors, which could be optimized for higher power, efficiency, or breakdown voltage in the absence of a heavy class AB-type thermal load.

4.3.1 ET PA Theory and Design

Drain supply modulation modifies the load line of a class AB PA as shown in Fig. 4.8. When V_{dd} is maximum at 32 V the transistor operates in cutoff for a significant fraction of the RF period, providing the class AB boost in peak efficiency. As V_{dd} is reduced the output power is reduced, along with the required drive level. Recall that the theoretical load line depends upon V_{dd}, and thus can only be optimized at one point in the V_{dd} range. Some efficiency at the infrequent high-V_{dd} levels may be sacrificed for an efficiency

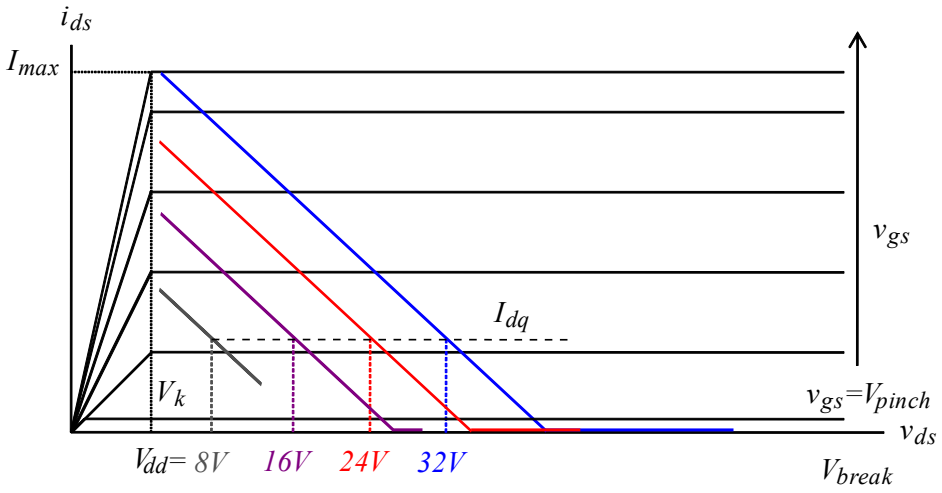


Figure 4.8: Load lines notionally corresponding to varying drain voltage and input drive levels of Fig. 4.2.

enhancement at the more frequent low-V_{dd} levels. As an approximation, [29] suggests that the PA be designed for maximum efficiency at the RMS voltage of the expected V_{dd} waveform. More generally, the design should achieve the efficiency vs. drain voltage profile which most reduces PA power dissipation given signal statistics.

The knee voltage of many high-power devices is significant compared to nominal drain supply voltage as shown in Table 3.2 and becomes a major factor in ET mode. As V_{dd} is reduced very little output power can be produced without running into the knee voltage region, corresponding to low gain or even attenuation at low drain voltage. From a PAE standpoint it does not, therefore, make sense to use V_{dd} values lower than, or even near to the knee voltage to produce low output power.

Full control of the amplitude through drain voltage is used in the EER technique, but does not provide any benefit for signals with high linearity requirements and significant low-power output power distribution. Instead, amplification of small signals is done with the minimum, or "troughing," drain supply voltage. The PA must be designed with a load line that preserves a significant small-signal gain at low V_{dd}.

The issue is more complex when considering harmonic-tuned and switched-mode PA design. Output capacitance is of critical importance in correct harmonic termination and varies with drain supply voltage [54]. Fortunately for the class E case, Z_E remains constant over drain voltage, though class E operation is only realized while the device is saturated (operating like a switch). Switched-mode class E lacks the small-signal gain required for this application and is not considered in this ET application.

As in Chapter 3, load-pull characterization was used to facilitate PA design. The Nitronex NPT25100 transistor is a GaN on Si HEMT transistor designed to produce 125 W at 3 dB gain compression between 2.1 GHz and 2.7 GHz. The device has internal input prematching only, output capacitance of about 17 pF, and is designed for operation up to 32 V drain supply in class AB operation. The harmonic termination feasibility analysis described in Chapter 3 was performed to determine that the packaged device is

not a good candidate for harmonic-tuned PA design. The part was evaluated for class AB operation at many drain voltages under pulsed conditions, resulting in the load-pull contours of Fig. 4.9.

In ET configuration only one load impedance must be selected which is a good compromise of performance over all drain voltage levels. The gain at the troughing drain voltage is important, so a 12 V gain contour is shown in green. Between minimum and maximum V_{dd}, compressed drain efficiency determines PA efficiency because the ET drive power will be controlled at each point to achieve compressed operation. Drain efficiency was measured with input power sufficient to achieve a consistent level of gain compression (as described in Chapter 3), resulting in blue, magenta, maroon, and red contours at 12 V, 24 V, 32 V, and 40 V, respectively. Finally, output power at the maximum output voltage will determine the ET system peak envelope power capability, and is shown in black contours.

Based on this data, a matching circuit was designed to achieve a fundamental load impedance of $1.7+j1.5$, resulting in near-maximum output power at 40 V, peak efficiency

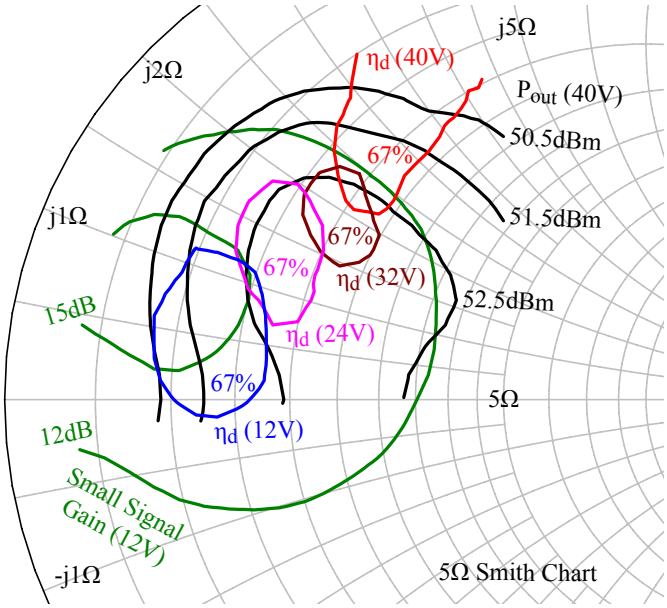


Figure 4.9: Summary of measured load-pull data for designing a PA for ET operation, shown for the Nitronex NPT25100 GaN HEMT at plane P3.

near 24 V, and greater than 13 dB small-signal gain at 12 V. This design varies from the traditional PA designed for peak power, peak efficiency, or maximum gain at a single drain voltage. The resulting class AB prototype in Fig. 4.10 was constructed and measured under pulsed conditions resulting in the PAE vs. output power plot of Fig. 4.2.

4.3.2 ET PA Bias Network

PA designs for ET application require non-standard bias network design [43]. Many PA bias tees implement the RF choke as a large-valued inductor, providing a high impedance over a relatively broad bandwidth. However, such an inductor has significant impedance at the envelope bandwidth, adding a voltage drop proportional to current slope. PAs for ET application therefore must use a narrowband RF choke. Such a choke is implemented in this work as a quarter-wave transmission line shorted at the drain supply side by a capacitor resonant at the fundamental frequency (as shown in Fig. 4.10). At the transistor drain the quarter-wave transmission line appears to be an

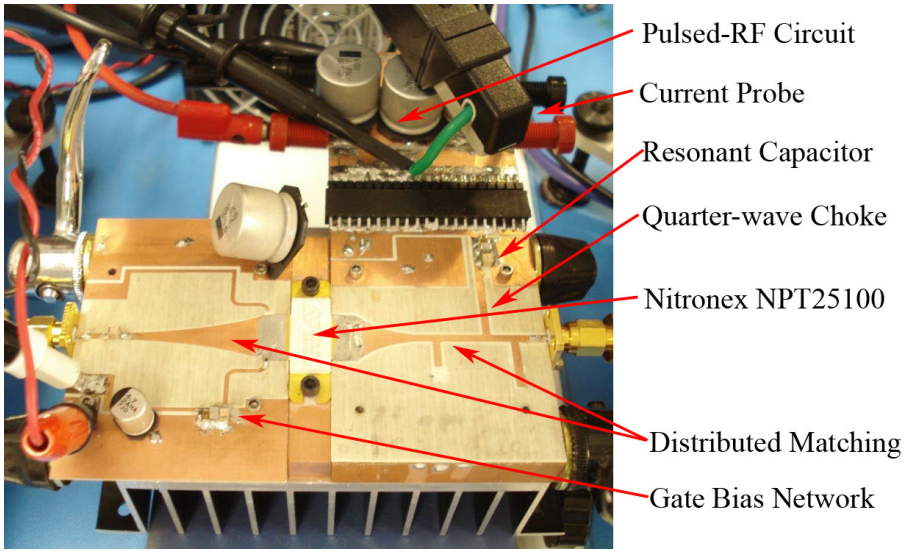


Figure 4.10: Photograph of the 100 W class AB PA prototype designed for ET applications using the Nitronex NPT25100 GaN HEMT, shown here connected to the pulse-power measurement board in place of an EM.

open at the fundamental frequency and odd harmonics thereof, but presents negligible impedance at the envelope bandwidth.

A traditional bias tee also makes use of a bank of large shunt capacitors on the drain supply side to present low impedance at the envelope bandwidth, enhancing low-frequency stability. In an ET application the EM would be forced to drive the bias tee capacitance in parallel with the RF transistor, leading to high capacitor power losses, low EM efficiency, and dramatically reduced EM bandwidth. In the ET application the capacitance is removed. Recall that the EM output impedance is ideally low over a bandwidth much larger than the envelope bandwidth, and thus presents a low impedance to the RF transistor at low frequencies just as the bank of capacitors had previously. The stabilizing effect has been observed when a PA for ET applications (lacking bias network bypass capacitance) exhibits low-frequency oscillation when connected to a standard DC drain supply, but is stable when connected to an EM drain supply.

The PA of Fig. 4.10 is designed for ET operation but being measured in pulsed RF power mode using a constant DC supply. Note the quarter-wave line and fundamental-frequency-resonant capacitor at the drain supply side of the line. Without the EM present, additional shunt capacitance is used for stability and to keep the drain voltage from sagging or ringing when a current pulse is drawn. In ET mode the pulsed-RF measurement circuit is replaced with an EM prototype, and all capacitors are removed from the drain bias network except for the fundamental-frequency-resonant capacitor.

4.3.3 ET PA Characterization

In an ET transmitter the PA acts as a nonlinear combiner of $\tilde{v}_{in}$ and V_{dd}, and the output signal $\tilde{v}_{out}$ is a strong function of both inputs. The gain, insertion phase, and drain current of the PA must be characterized over V_{dd} and $|\tilde{v}_{in}|$ rather than just the traditional constant-V_{dd} input power sweeps. Some methods of characterization are discussed in literature (e.g. [99], [45]), resulting in plots such as the ones shown in

Fig. 4.11 and Fig. 4.12. PA behavior is completely described for every combination of $|\tilde{v}_{in}|$ and V_{dd}. For example, if an an instant in time the $|\tilde{v}_{in}|$ and V_{dd} are 15 V and 25 V respectively the PA insertion gain and phase will be 14 dB and 110 degrees while PA efficiency and drain current will be 58% and 4.2 A.

The impact of a $\tilde{v}_{in}$ or V_{dd} error on $\tilde{v}_{out}$ can now be determined. In ET simulations this data set will be used as a static 2-d look-up table (LUT) model for PA behavior.

This static measurement method reflects PA behavior under pulsed operating conditions faster than the thermal time constant of the device. As the pulse becomes longer heat builds up in the device, raising junction temperature and reducing output power, gain, and efficiency. In this measurement the pulse was set to be short enough that no degradation in transistor performance could be observed over the pulse duration. Therefore dynamics due to thermal loading, charge storage, and other PA memory effects [100] are isolated from static behavior, leading to a memoryless PA model. In this way ET system dynamics can be analyzed separately from PA dynamics. Chapter 5 will address sources and mitigation of dynamic distortion.

As noted in the introduction to this section, the measurement conditions are critical to correctly evaluate PA performance. The thermal conditions for pulsed-RF (constant-V_{dd}) operation are meant to approximate conditions of ET operation. However, in ET operation quiescent current is continually varying with drain supply voltage, resulting in a different (likely lower) thermal load. This characterization data will, therefore, not predict absolute PA performance in ET mode, but will prove a useful tool in determining trends and evaluating sensitivity to distortion in the V_{dd} and $\tilde{v}_{in}$ paths.

A second characterization method was also employed to pulse both the RF input power and the DC drain supply voltage. By reducing V_{dd} between RF pulses (called pulsed-RF/DC measurement) the measurement conditions are brought closer to those of a real ET system. This method requires equipment capable of providing large voltage and current pulses; an EM is the ideal drain supply pulse generator. Output impedance

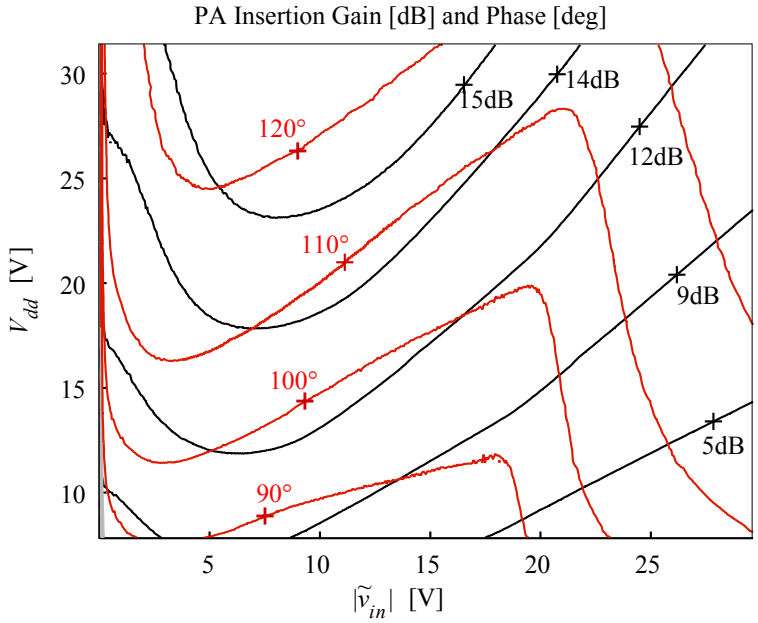


Figure 4.11: Gain and insertion phase for the NPT25100-based PA prototype measured over a matrix of input and drain voltage measured in pulsed-RF mode biased with 600 mA quiescent current.

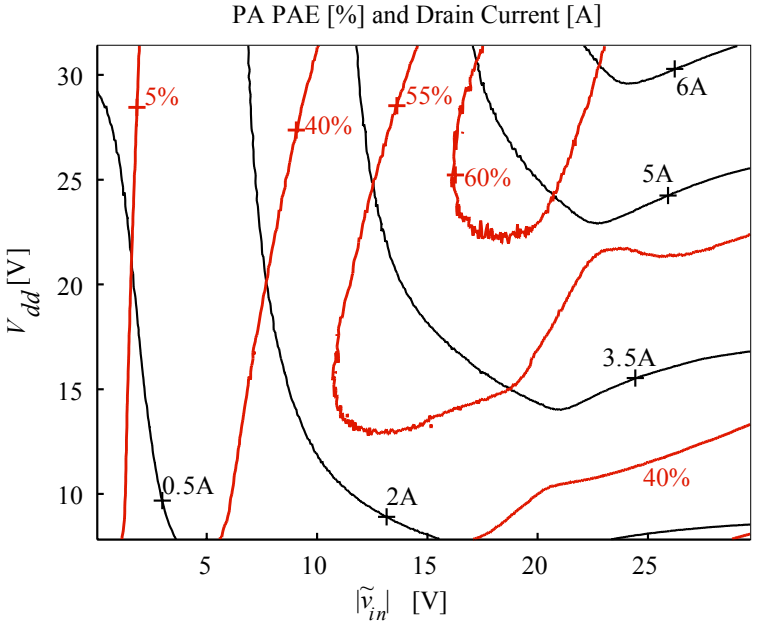


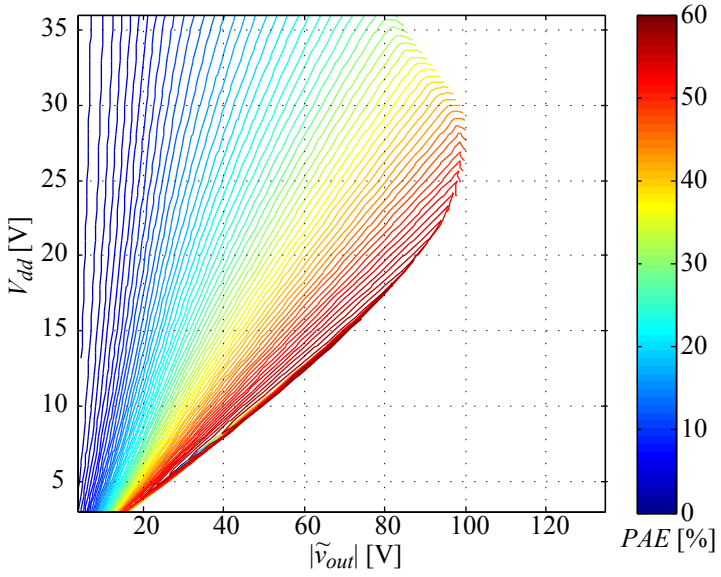
Figure 4.12: Drain current and PAE for the NPT25100-based PA prototype measured over a matrix of input and drain voltage measured in pulsed-RF mode biased with 600 mA quiescent current.

of the EM must be very low to maintain output voltage in the presence of large drain current when the RF pulse begins (slightly after the V_{dd} pulse begins). Measurements of this type were collected for the prototype presented in Chapter 5, used in simulations, and are compared to system efficiency measurements in that chapter as well.

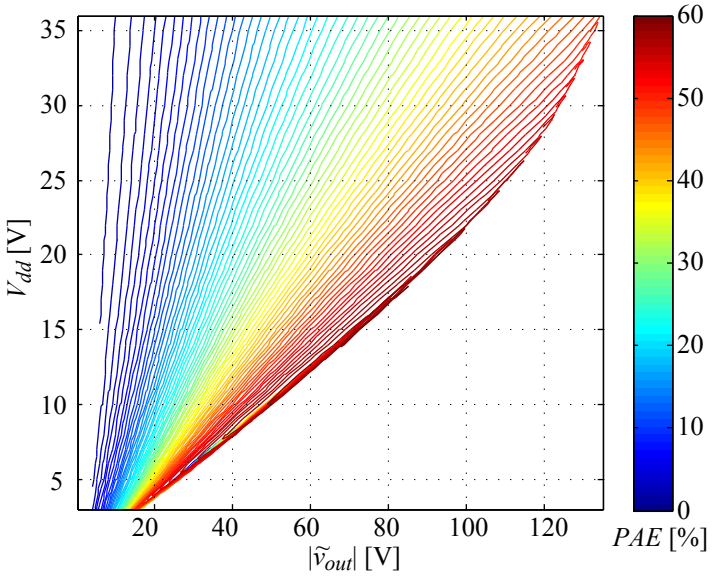
Fig. 4.13 shows simulated contours of transistor PAE over a range of output power levels for varying drain voltages. Simulation was performed using the Angelov large-signal nonlinear model available from Nitronex for the NPT25100 GaN HEMT. The top plot includes self-heating effects and the bottom plot ignores heating effects.

In this model self-heating applies a thermal load as though the device were in steady state (CW) operation. When self-heating is turned off the nonlinear model operates as though the device is at room temperature. Pulsed-RF operation is close to zero self heating performance, but still incurs the thermal load of quiescent bias current. Pulsed-RF/DC is even closer to the zero self heating case, as the quiescent current is eliminated between pulses. Pulses close together will still cause a temperature rise, but not so significant as the pulsed-RF or CW operation modes. The ET mode of operation falls between pulsed-RF and pulsed-RF/DC operation, as some reduced quiescent current (due to reduced drain voltage) is present even when output power is low.

Note the significant performance change in simulation due to thermal effects. When self-heating is considered the device is output-power-limited at 100 W, but in the absence of the thermal load an additional 2.6 dB, or 180%, more output power is possible from the same device, along with an appreciable increase in low-voltage gain and efficiency. Clearly, the mode of operation (CW, pulsed, or ET) will have a dramatic impact on PA performance. Very different performance should be expected from the same transistor operated in class AB CW, drive modulated, Doherty, and ET configurations.



(a)



(b)

Figure 4.13: Comparison of simulated output power and efficiency over drain voltage with (a) and without (b) self-heating effects for a PA using the NPT25100 GaN HEMT transistor.

4.4 Signal Split

The ET transmitter can be optimized for PA efficiency using the signal split to vary V_{dd} to operate the transistor along the dashed line in Fig. 4.2 with 50% efficiency at the average output power level. However, the PA is not the only component in an

ET transmitter, and highest PA efficiency does not necessarily translate to highest transmitter efficiency. It is clear from previous discussions of EM architecture that increased EM dynamic requirements translate to lower EM efficiency. It will be shown that the improving PA efficiency leads to increased EM dynamic requirements. Thus a tradeoff exists between EM efficiency and PA efficiency.

Classical EER systems sets V_{dd} equal to the signal envelope amplitude, sacrificing system linearity, EM efficiency, and PA gain at the lower envelope power levels. In Fig. 4.14 the colored gradient shows measured PA efficiency for all $|\tilde{v}_{out}|$ levels at every possible V_{dd} for the 100-W class AB PA prototype of Fig. 4.10. Note that as $|\tilde{v}_{out}|$ increases a minimum level of V_{dd} is required, below which $|\tilde{v}_{out}|$ cannot be achieved.

Three V_{dd} trajectories, denoted T1, T2, and T3, achieve different modulated PA efficiencies as summarized in Table 4.1. These trajectories describe the V_{dd} value that should be applied when the desired output signal $\tilde{v}_{out}$ has a given magnitude. The

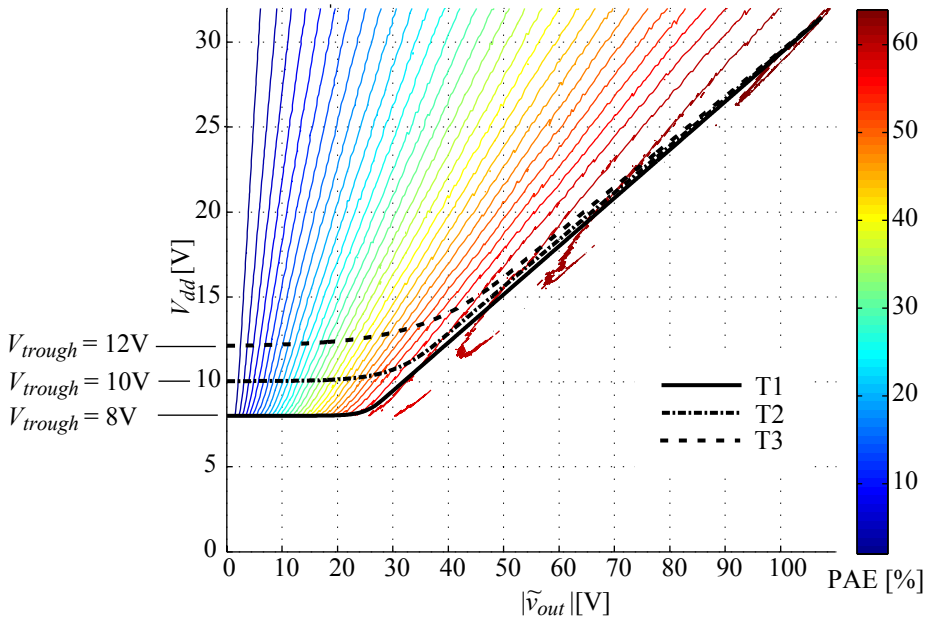


Figure 4.14: Measured PAE for the 120-W class AB PA prototype shown in colored contours over a range of output voltage levels for a range of drain voltage levels. Three possible V_{dd} trajectories are shown.

Table 4.1: Expected average PA efficiency for three signal split trajectories.

Signal Split	PA PAE
T1	50.6 %
T2	47.5 %
T3	43.4 %

minimum, or "troughing," voltage for a trajectory is called V_{trough}. Each trajectory presents a different tradeoff between PA efficiency and EM dynamic requirements. For example, T1 has a lower troughing voltage and a sharper inflection point, presenting a challenge to the EM which must produce higher bandwidth voltage waveforms over a wider voltage dynamic range. In exchange for the more difficult EM requirement the PA operates in a high-efficiency region over a larger dynamic range, increasing average PA efficiency. By contrast, T3 requires less EM dynamic capability (a more efficient EM design is possible) at the expense of high-efficiency PA operation at reduced output power levels.

Fig. 4.15 shows estimated PA insertion gain and phase variation for each trajectory based on measured PA characterization data. These curves are digitally implemented by the signal split as a transfer function $\tilde{y} \rightarrow \tilde{\beta}$ to produce a pre-corrected $\tilde{v}_{in}$ which restores system linearity. This transformation is analogous to the memoryless pre-distortion used in [29]. Fig. 4.15 also shows the change in PA drain resistance (EM load resistance) for each trajectory. T1 is associated with the largest first derivative of the drain resistance, and thus the most difficult dynamic load regulation challenge to the EM. Stated another way, T1 requires low EM output impedance over the broadest bandwidth.

Each trajectory defines a different time domain V_{dd} and $\tilde{v}_{in}$ waveform for a given W-CDMA signal, placing new requirements on the RF up-conversion chain and EM. Changing bandwidth, slew rate, voltage range, and average load requirements will have

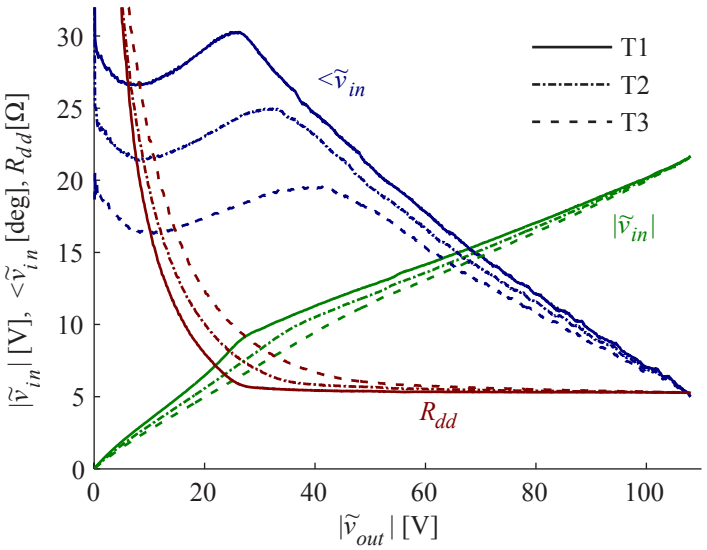
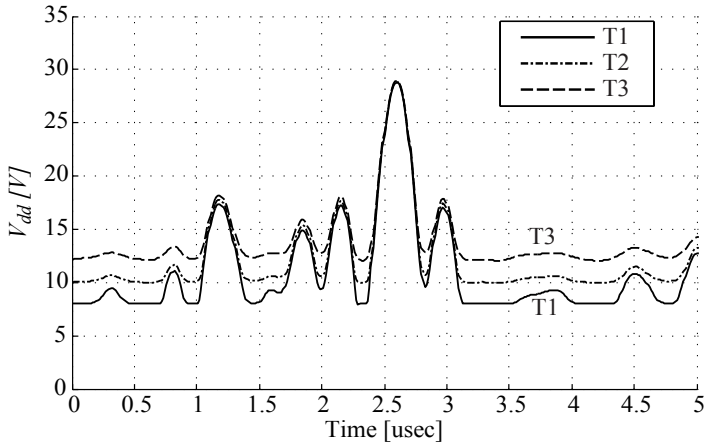


Figure 4.15: Projected $\tilde{v}_{in}$ and R_{dd} trajectories based on measured PA data for three signal split V_{dd} trajectories.

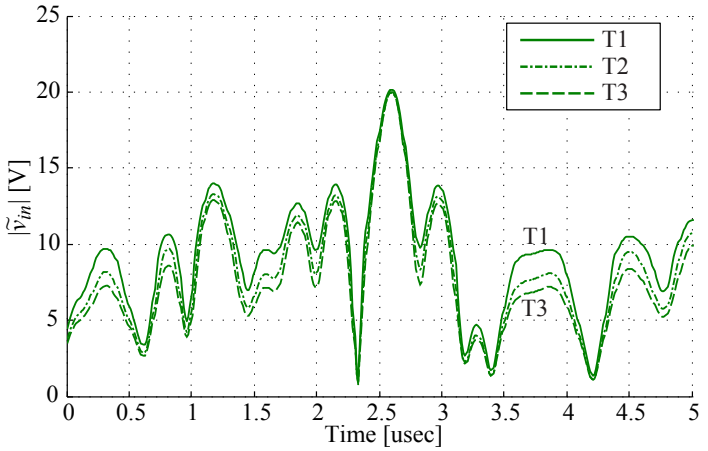
an impact on maximum possible EM design efficiency, which may entirely negate the increase in PA efficiency. Based on the relationships of Fig. 4.15, V_{dd}, $|\tilde{v}_{in}|$, and R_{dd} waveforms can be projected given an ideal W-CDMA signal. The resulting time-domain waveforms are shown in Fig. 4.16. Note how quickly the load changes from only 5Ω to 45Ω in Fig. 4.16(c) and how variation in the signal split can change the shape of V_{dd}, $|\tilde{v}_{in}|$, and R_{dd} waveforms, impacting frequency content and amplitude distribution of each.

Error in the EM output waveform V_{dd} will cause variation in the PA output $\tilde{v}_{out}$ which has not been pre-compensated by the signal split, resulting in ET system distortion. The plot of Fig. 4.17 shows contours for the ratio of $\%\triangle|\tilde{v}_{out}|$: $\%\triangle V_{dd}$, or $V_{dd} \rightarrow \tilde{v}_{out}$ sensitivity. The red region indicates that a 1% V_{dd} error corresponds to a 1% $|\tilde{v}_{out}|$ error.

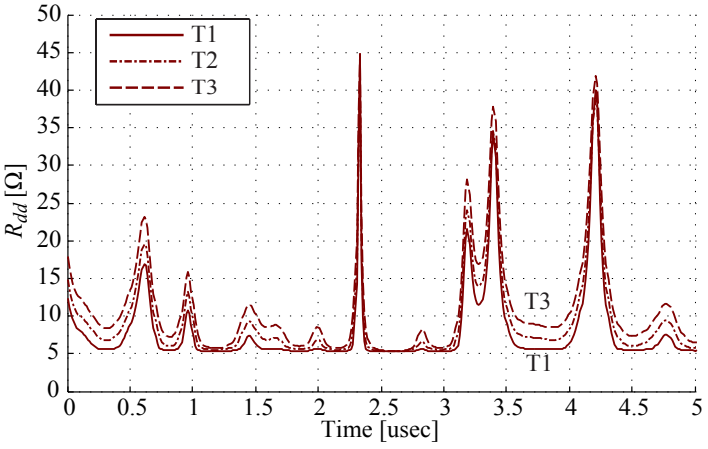
An interesting observation can be made from the sensitivity plot of Fig. 4.17 with regard to bias line memory effects in traditional PAs [100]. A common cause of memory effects in traditional drive-modulated power amplifiers is inadequate drain supply



(a)



(b)



(c)

Figure 4.16: Projected V_{dd}, $|\tilde{v}_{in}|$, and R_{dd} time domain waveforms resulting from the three signal split trajectories of Fig. 4.14 based on measured PA data.

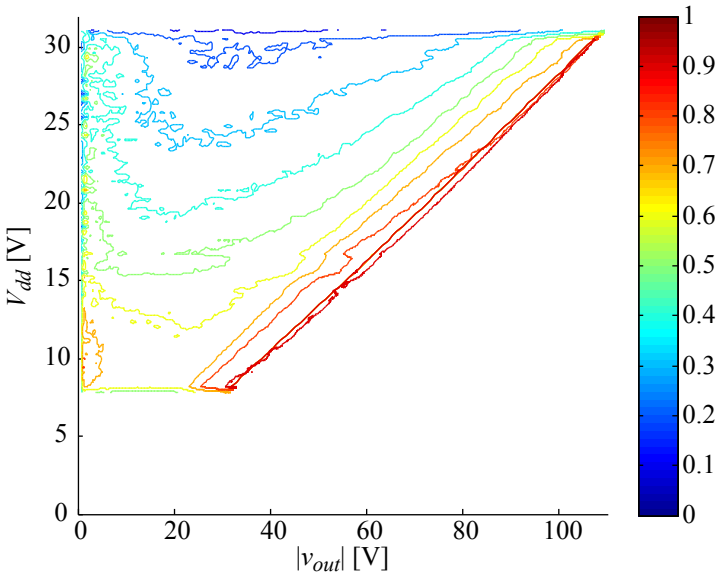


Figure 4.17: Contours calculated from PA characterization data indicating sensitivity of $\tilde{v}_{out}$ to V_{dd} error. Sensitivity metric is the ratio $\%\triangle|\tilde{v}_{out}|$: $\%\triangle V_{dd}$.

capacitance, resulting in a drain voltage sag when a current spike is demanded by the PA. Fig. 4.17 demonstrates that, especially at high output power levels, deviation from nominal drain voltage will bring a significant deviation in the output signal. Variation of output waveform due to supply voltage variation is a problem known to analog electronics as poor supply rejection ratio.

The signal split (and PA behavior) determine EM design requirements including small-signal bandwidth, large-signal slew rate, voltage range, load regulation, and efficiency. These requirements impact the following:

- ET system efficiency is defined as $\eta_{ET} = \eta_{EM} \times \eta_{PA}$, demanding high EM efficiency;
- High η_{PA} requires large voltage and current swings, reducing η_{EM};
- Inadequate bandwidth, slew rate, or load regulation will translate through the PA into $\tilde{v}_{out}$ distortion and degrade system linearity.

Increasing bandwidth and slew rate requirements forces the high-bandwidth linear am-

plifier to produce a larger portion of the output power, reducing EM efficiency. EM efficiency/linearity compromises cannot be easily quantified, as a change in architecture or technology is often required rather than the adjustment of a load line or quiescent current. The system analysis tool thus proves very useful in optimizing a simulated EM design to achieve maximum efficiency while not significantly degrading transmitter linearity.

4.5 System Analysis Tool

A method has been developed to quantify the impact of component non-idealities and inter-dependency on the overall ET transmitter linearity ($\tilde{y} \rightarrow \tilde{z}$) and efficiency ($\eta_{ET} = \eta_{EM} \times \eta_{PA}$). The method is also useful for design, simulation, and optimization of algorithms by emulating ideal or non-ideal hardware. The method is applied to evaluation of PA efficiency vs. EM requirements for an ET transmitter.

Each of the components in the previous section has been implemented in a MATLAB simulation environment using the simplified block diagram of Fig. 4.1. A standard W-CDMA downlink signal is generated at a 20x oversampling rate, and de-crested to 8 dB PAR ($\tilde{y}[n]$), followed by the signal split which produces $\alpha[n]$ and $\tilde{\beta}[n]$ according to one of the trajectories shown in Fig. 4.4. EM and up-converter models translate $\alpha[n]$ and $\tilde{\beta}[n]$ into $V_{dd}(t)$, and $\tilde{v}_{in}(t)$. The PA is modeled using the 2-d LUT formed by the data of Fig. 4.11 and Fig. 4.12. A variety of non-idealities are synthesized to distort $V_{dd}(t)$ and $\tilde{v}_{in}(t)$. A few examples include DAC quantization, up-converter phase imbalance, EM group delay, and ADC path frequency response. The impact of component non-ideality on system efficiency, linearity, and the performance of other components can thus be easily observed.

A generic EM was modeled using the cascade of a low-pass filter and a slew-rate limiter (two key limitations in EM design directly opposing ET efficiency). Fig. 4.18

shows the impact of a 6-MHz Bessel low pass response on an ideal V_{dd} waveform.

The ideal V_{dd} waveform of Fig. 4.19 has been processed with a 100 V/μsec slew rate limiting algorithm followed by a 12-MHz Bessel response. Applying the slew rate before a band limiting filter removes non-physical high-frequency artifacts of the mathematical slew-limiting process. The ideal and impaired slew rate is shown in the bottom of Fig. 4.19.

The filters used in the two previous examples have significant group delay (as does real EM hardware), but impaired waveforms have been shifted in time to match with the original waveform with smallest RMS error.

The ideal $V_{dd}(t)$ signal component was distorted by this EM model for a variety of different EM bandwidth and EM slew rate impairments and then recombined with the $\tilde{v}_{in}(t)$ signal using the PA model. The $\tilde{v}_{out}(t)$ signal linearity was then evaluated using EVM and ACP. As expected from [35] ACP was found to be the limiting metric. Fig. 4.20 shows degradation in ET system linearity due exclusively to two specific cases of EM impairment.

As mentioned in the previous section, increased PA efficiency can be achieved with an aggressive signal split at the expense of increased EM requirements. The method described above was used to quantify the EM bandwidth and slew rate performance required to achieve ET system linearity of -45 dBc ACP and -65 dBc ACP (at which point the EM has a nearly negligible system linearity impact) with the three signal split trajectories shown in Fig. 4.14. The simulation noise floor for these simulations due to quantization, interpolation, and numerical accuracy was less than -69 dBc ACP.

Fig. 4.21 summarizes the resulting EM requirements for each signal split trajectory, drawing a clear connection between EM component behavior and ET system performance. From a system design perspective we see that signal splits weighted toward high PA efficiency clearly require higher EM bandwidth, slew rate, and voltage dynamic range (all of which lead to reduced EM efficiency). Summarized in Table 4.2,

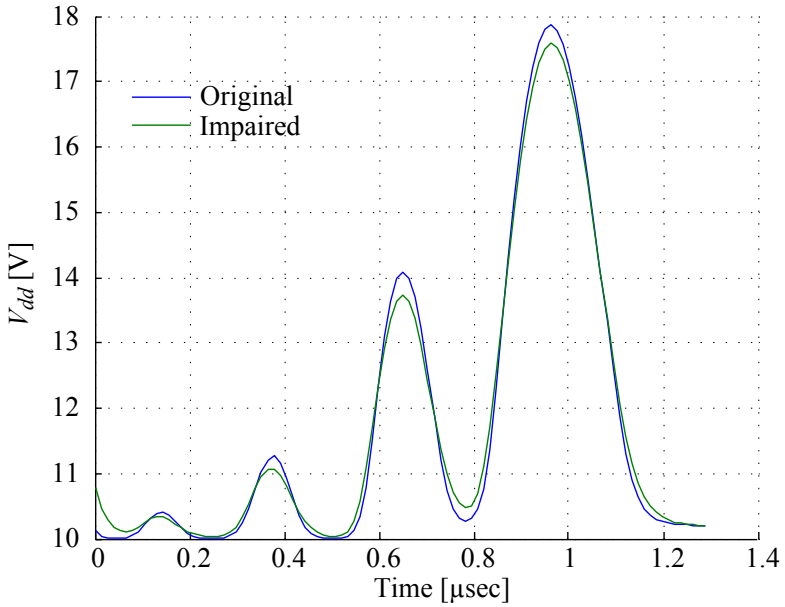


Figure 4.18: Ideal and EM-impaired drain voltage waveform for a W-CDMA signal using signal split trajectory T2 assuming a 6-MHz EM bandwidth limit impairment.

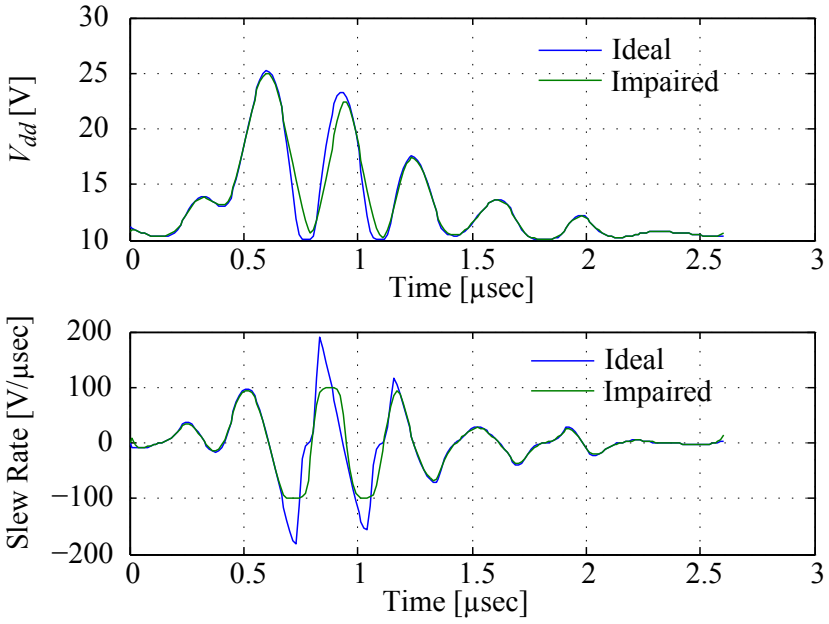


Figure 4.19: Ideal and EM-impaired drain voltage waveform for a W-CDMA signal using signal split trajectory T2 assuming a 100-V/μsec slew limit impairment.

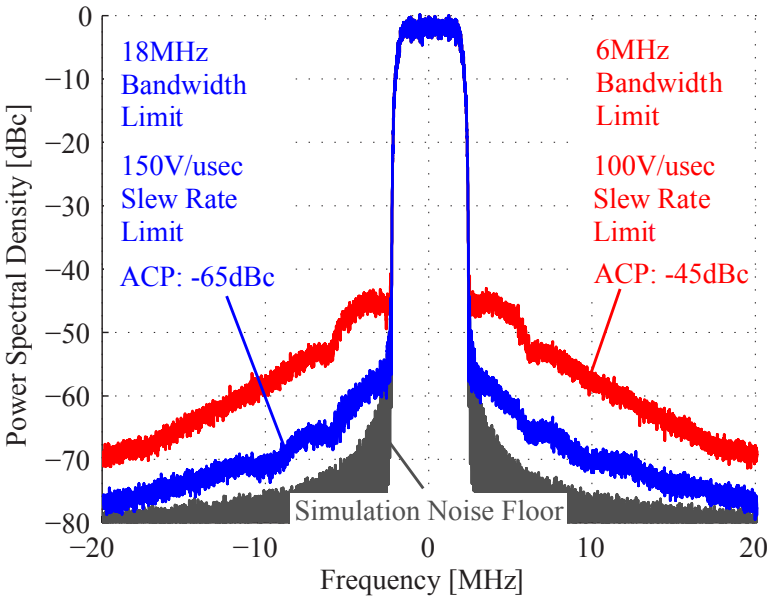


Figure 4.20: Simulated ET system output PSD for a W-CDMA waveform using trajectory T2 from Fig. 4.14 given two non-ideal EM models. Degradation in ACP is due only to EM non-ideality. The simulation noise floor shown in gray.

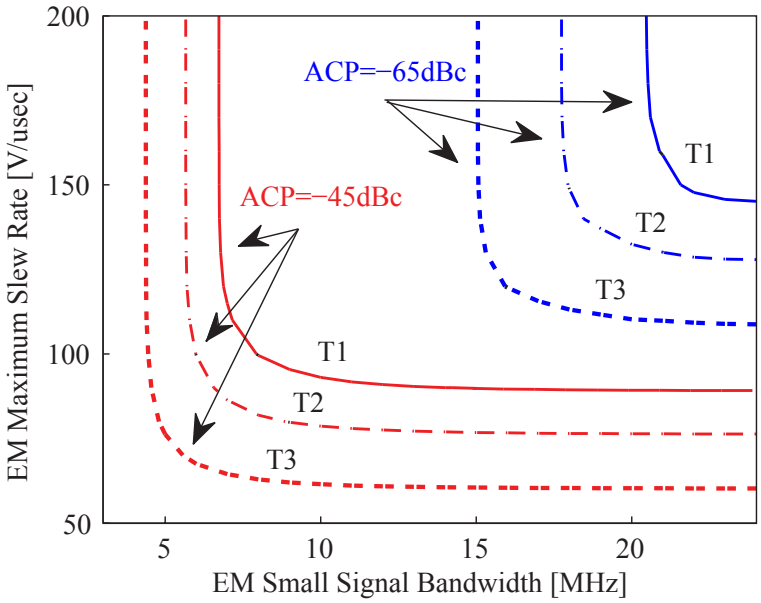


Figure 4.21: EM bandwidth and slew rate required to meet -45dBc (3GPP minimum spec) and -65dBc adjacent channel power considering only distortion from the V_{dd} path for each of the signal split trajectories shown in Fig. 4.4 are shown.

these results give the EM and system designers a starting point for designs and insight into system-level tradeoffs.

Another useful analysis includes the effects of resistance and inductance in the path between the EM and PA, which result in current-dependent distortion of the V_{dd} signal. Fig. 4.22 and Fig. 4.23 shows the impact of series DC resistance and inductance on ET system linearity. These simulations were performed using a lower oversampling ratio and different interpolation technique, resulting in a -54 dBm ACP1 simulation noise floor.

EM prototypes with frequency-dependent output impedance can be modeled in the same way. After finite bandwidth and slew rate, output impedance was found in this work to be the next most dominant source of EM-path distortion. Defining EM linearity requirements is a much more difficult task than for other analog circuit designs. It becomes apparent that some types of distortion at some output voltage levels are more tolerable than others. The ET system analysis method is useful for translating actual component behavior into system performance.

4.6 Conclusion

General supply modulation was discussed with an emphasis on ET techniques, in which a fundamentally linear amplifier is used. Requirements, architecture, and typical non-idealities of EM hardware were discussed to provide context for ET system discussion. New PA design goals were outlined, emphasizing the importance of gain, efficiency, and

Table 4.2: Simulated ET system PA performance and EM requirements.

Signal Split	PA PAE	Min./Mean/Max. V_{dd}	Min. EM Bandwidth	Min. EM Slew Rate
T1	50.6 %	8.0 V / 11.0 V / 31.5 V	20 MHz	150 V/usec
T2	47.5 %	10.0 V / 12.3 V / 31.5 V	18 MHz	130 V/usec
T3	43.4 %	12.0 V / 14.0 V / 31.5 V	15 MHz	110 V/usec

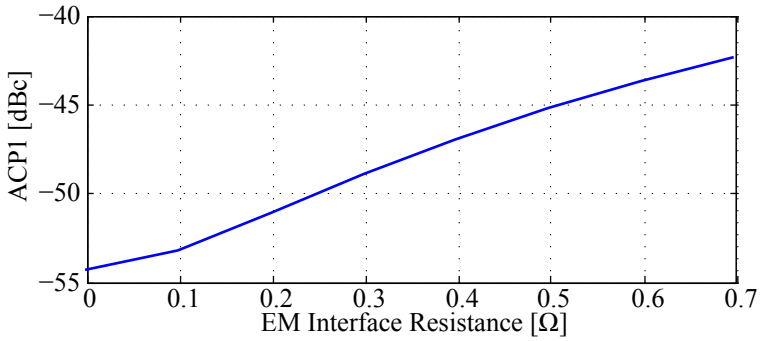


Figure 4.22: Degradation in ET system ACP1 due to EM-PA interface resistance.

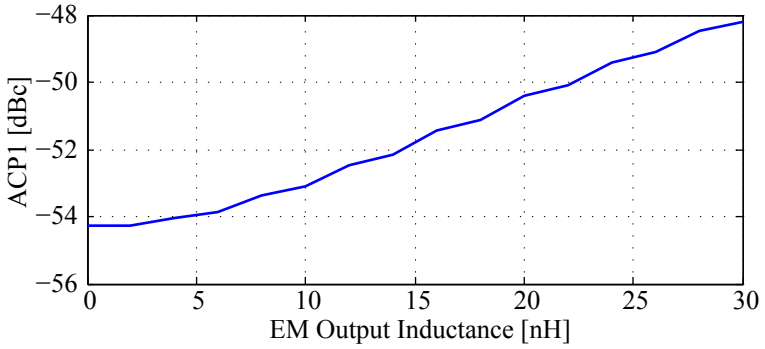


Figure 4.23: Degradation in ET system ACP1 due to EM-PA interface inductance.

output power at different points in the V_{dd} range. Other changes to conventional PA design include bias network design and special attention to the interface between the PA and drain supply. The signal split was introduced as a method of trading PA efficiency and EM requirements and illustrated using an ET system simulation method.

Many other types of analysis are possible using the presented simulation technique. The bandwidth, slew rate, and output impedance EM models can be replaced with a more complex mathematical model, a circuit simulation, or even EM prototype measurements. This simulation method has been used extensively by EM design collaborators with circuit-level Cadence models to validate linearity.

Another use for the simulation method is diagnosis of system distortion in hardware. Once assembled all components of the ET system contribute unique distortion mecha-

nisms that are mixed together, making it difficult to determine which component is at fault. The simulation can be driven by measured data from the ET test bench to determine the impact of EM distortion with a perfect PA. The ability to observe the impact of only one type of distortion (EM, PA, up-converter, driver, etc.) provides insight into system-level problems. Similarly, a suspected EM distortion mechanism can be added to the simulation and correlation drawn between the simulated and measured results. The simulation method has been used as a diagnostic tool in achieving the measured ET system results in Chapter 5.

Contributions described in this chapter include the following:

- A systematic framework for drive/drain modulated ET transmitters making use of a "signal split" to trade component performance, resulting in optimal system efficiency given linearity constraints [45].

- Identification of important design issues and requirements for EM prototypes including bandwidth, slew rate, output impedance, and PA-EM interconnect design [43].

- Adaptation of traditional PA design techniques discussed in Chapter 3 to PA design for ET applications. The load-pull procedure is modified to help select a load impedance achieving gain, efficiency, and power at appropriate points in the drain voltage range, and the drain bias network is modified to allow fast variation of drain supply voltage and current [48].

- Pulsed-RF and pulsed-RF/DC characterization methods to emulate PA performance in ET mode over the range of input power and drain voltage, resulting in data ultimately used for system simulation and signal split configuration [44].

- ET system simulation using custom-designed MATLAB software to observe the impact of component non-idealities on system performance [42]. This method is

used by our collaborators in EM prototype design, in hardware integration as a diagnostic tool, and in the next chapter to design and evaluate signal processing algorithms.

Chapter 5

Envelope Tracking System Integration

Contents

This chapter describes the integration of the EM and PA hardware into an ET testbed. In addition to the idealized static interaction of an EM and PA described in Chapter 4, realization of an ET system in hardware requires attention to the following details:

- calibration of EM output DC voltage level,
- equalization of EM frequency response,
- delay adjustment of $\tilde{v}_{in}$ with respect to V_{dd} at the PA to ensure time alignment,
- adaptation of PA static nonlinear transfer function $\tilde{x} \rightarrow \tilde{\beta}$, implemented as a

complex gain LUT[1], and

- correction of PA and system dynamic nonlinear characteristics using polynomial-based digital pre-distortion.

These issues were identified and solutions formulated over the course of a 2-year integration effort in parallel with EM and PA prototype design. Initial, intermediate, and final results are presented at the end of this chapter after discussing several key integration and testbed issues. Signal processing techniques are discussed with illustrative examples taken from various stages of system development. The final proof-of-concept ET system PAE was 50.6% with greater than 7 dB ACP margin with a W-CDMA 7 dB PAR test signal at 40 W PEP, and incorporated an optimized PA, and an EM designed using the static simulation method of Chapter 4.

5.1 System Block Diagram

The ET proof-of-concept system was assembled from commercial test and measurement equipment and integrated with custom MATLAB-based software. This state-of-the-art testbed was designed to be flexible enough to accommodate a wide range of ET research, far exceeding the requirements for an implemented ET system. A great deal of time was dedicated to designing the testbed, which subsequently allowed PA and EM prototype integration, linearization algorithm development, research to identify distortion mechanisms, and the final proof-of-concept demonstration.

Fig. 5.1 shows a block diagram of the ET proof-of-concept system including signal (top) and hardware (bottom) block diagrams. Signal processing algorithms are developed and implemented using MATLAB. The hardware in the bottom of the block diagram emulates ideal transmitter up- and down-conversion, A/D, and D/A functionality. Each piece of equipment was selected specifically for this application, incorporating special-

[1] look-up table

ized features required for desired ET testbed functionality (e.g. high-precision waveform generator time alignment, wide-bandwidth IQ demoduator/digitizer). All testbed hardware functionality is automated using MATLAB-based instrument control. The complex nature of this powerful system makes manual operation difficult, highly error- prone, and easily leads to damaged equipment or hardware prototypes. The system operates in batch mode (not real time): a single frame of data is run as a continuous loop until the capture can be completed, data is analyzed, system parameters are updated, and a new frame of data is loaded.

5.1.1 Signal Flow

Signal flow through the block diagram proceeds as follows:

- Standard W-CDMA test signals are generated, circularly filtered, de-crested, and scaled to the desired output power level, resulting in the complex sampled baseband signal $\tilde{y}$. If the system were perfect, $\tilde{y}$ would be equal to transmitter output $\tilde{v}_{out}$.

- A polynomial-based DPD algorithm is used to pre-correct dynamic transmitter distortion (e.g. PA memory effects), resulting in the new, pre-corrected, input signal $\tilde{x}$. The expansion function weighting vector $\tilde{k}$ describes the DPD behavior and is adapted to signal type and transmitter distortion signature.

- Desired drain voltage V_{dd} is represented in the digital domain by α. α is a nonlinear function of either the original signal $\tilde{y}$ (configuration B) or the pre-distorted signal $\tilde{x}$ (configuration A). The transfer function is set by the signal split V_{dd} trajectory as described in Chapter 4.

- Gain, offset, and linear frequency response corrections account for non-idealities in the V_{dd} path. These are applied to α, resulting in the corrected signal α' required to obtain calibrated EM output voltage, such that $V_{dd} = \alpha$.

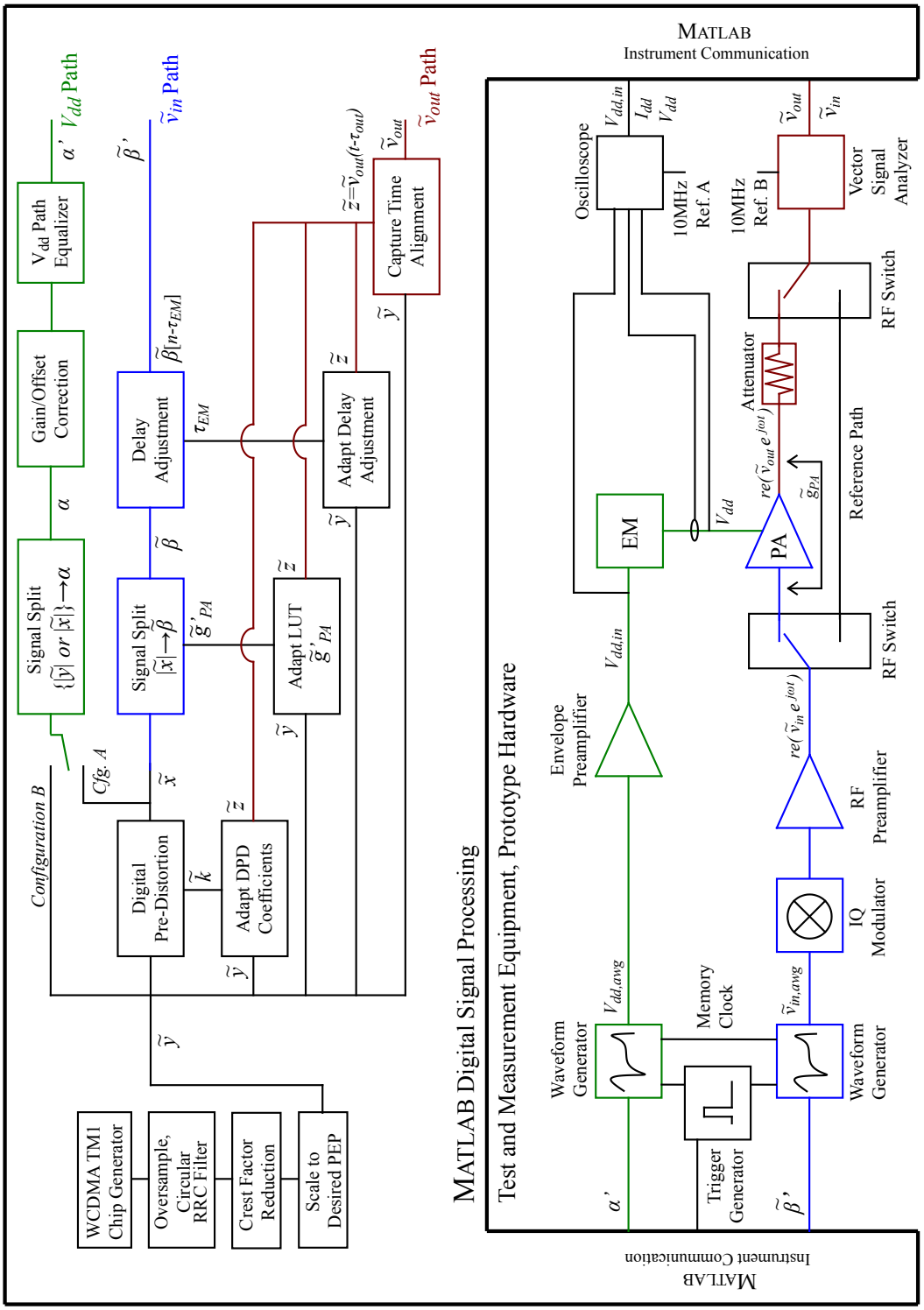


Figure 5.1: Block diagram of the ET transmitter system.

- The signal split in the $\tilde{v}_{in}$ path transforms $\tilde{x}$ into $\tilde{\beta}$, accounting for variations in the complex PA gain $\tilde{g}_{PA}$, which varies as a function of V_{dd} and $\tilde{v}_{in}$. $\tilde{\beta}$ is calculated as $\tilde{x}/\tilde{g}_{PA}$.

- Delay is added to $\tilde{\beta}$ to account for group delay mismatch between the V_{dd} and $\tilde{v}_{in}$ paths, resulting in $\tilde{\beta}'$. The optimal value of delay τ_{EM} is determined by iteration and has sub-sample precision.

- Closely synchronized waveform generators are fed α' and $\tilde{\beta}'$, producing analog voltages $V_{dd,awg}$ and $\tilde{v}_{in,awg}$. An up-converter modulates $\tilde{v}_{in,awg}$ onto an RF carrier. Preamplifiers in both V_{dd} and $\tilde{v}_{in}$ paths bring signals to the expected voltage and power levels.

- Signal components V_{dd} and $\Re(\tilde{v}_{in}e^{j\omega t})$ are recombined in the PA to produce the modulated RF output $\Re(\tilde{v}_{out}e^{j\omega t})$.

- A digitizing oscilloscope captures $V_{dd,in}$ and V_{dd}. I_{dd} can be captured to evaluate performance of EM and PA components individually, but requires use of a current sense loop which degrades system linearity due to V_{dd} distortion.

- A VSA[2] is used to demodulate and digitize either PA input ($\tilde{v}_{in}$) or output ($\tilde{v}_{out}$) signals, selectable using mechanical RF switches.

- All captured signals are sub-sample time aligned to a digital reference signal using correlation techniques. $\tilde{z}$ is the digital capture of $\tilde{v}_{out}$ and used in adaptation of DPD, signal split, and delay adjustment algorithms. Captured V_{dd} and $V_{dd,in}$ waveforms are used in calibrating the V_{dd} path gain, offset, and equalizer.

[2] vector signal analyzer

5.1.2 Peripheral Hardware

In the testbed system commercial TM[3] equipment is used to emulate typical transmitter functionality. Power required for these components is not considered when stating system efficiency (consistent with literature). High-performance TM equipment is employed to control non-ideal effects like quantization, finite sample rate, IQ imbalance, and distortion, thus limiting the possible sources of distortion. Especially in early stages of development, there is enough non-ideality inherent in the system without these additional concerns. Non-ideal system effects can be added artificially in the testbed to evaluate absolute component performance requirements for an embedded implementation.

Signal Generation

In the final testbed system two RS[4] AFQ 100B AWGs[5] were selected for V_{dd} and $\tilde{v}_{in}$ path signal generation at up to 300 MSps. The maximum rate far exceeds the typical sample rates (between 30.72 MSps and 69.12 MSps) used for the single-carrier W-CDMA work. A specialized synchronization feature was employed to lock the memory clocks and achieve very precise triggering between the two generators. An RS SMBV100A signal generator was selected to upconvert the IQ modulation to RF. A highly linear RF preamplifier with more than 50 W PEP and gain around 55 dB was used in the $\tilde{v}_{in}$ path. Clearly not the choice for an embedded system, these components were selected to avoid non-ET-related distortion mechanisms. A variable-gain three-stage EM preamplifier was designed using the LM6703 operational amplifier with more than 1.2 GHz gain-bandwidth product preserve bandwidth. The EM preamplifier also achieves level shifting to accommodate EM prototypes requiring a bipolar input signal.

[3] test and measurement

[4] Rohde and Schwarz

[5] arbitrary waveform generators

In addition to the typical transmitter D/A and upconversion paths, ET architecture requires an additional D/A channel for the V_{dd} path. Synchronization between the two paths must be very repeatable; requirements depend on the signal bandwidth. In the next section the linearity impact of uncompensated delay between the V_{dd} and $\tilde{v}_{in}$ paths is shown to be dramatic. This analysis shows that for single-carrier W-CDMA, time alignment between the two paths should be adjusted with resolution on the order of 500 psec. Thus the drift or jitter in time alignment between the two paths must be some fraction of that resolution, near 250 psec.

The $\tilde{v}_{in}$ path incorporates two mechanical RF switches, allowing $\tilde{v}_{in}$ to be routed to either the PA input or to the VSA. The "reference path" is useful for evaluating $\tilde{v}_{in}$ path linearity and for input power measurement. Care must be taken to avoid biasing the PA when the switches are in the "reference path" position, as some PA prototypes are unstable without 50Ω terminations at input and output terminals. The power attenuator network following the PA has attenuation approximately equal to the peak PA gain, such that PEP is the same at the VSA for the the PA and reference paths. Excessive attenuation leads to reduced SNR[6] in VSA waveform measurements.

Signal Capture

The RS FSQ was selected with an option for 120 MHz digitizing bandwidth and 14 bits dynamic range, again exceeding the typical sample rates used for single-carrier work. SNR was improved by applying frame averaging, in which one long consecutive capture consists of many repeated loops of the same signal. Digitally captured samples of each loop will be perfectly time aligned with respect to each other provided one full loop is comprised of an integer number of samples, allowing for highly precise averaging not possible with multiple triggered capture events. A deep capture memory and fast data transfer is therefore an essential VSA feature.

[6] signal to noise ratio

Especially in early system iterations (before linearization correction) the bandwidth of $\tilde{v}_{out}$ is much larger than that of $\tilde{v}_{in}$, resulting in high Nyquist sampling rates. However, $\tilde{v}_{out}$ data acquisition sample rate can be varied depending upon where it is to be used. Signal split adaptation can be performed with undersampled data, and some DPD algorithms also allow adaptation using $\tilde{v}_{out}$ captured at the Nyquist rate for the $\tilde{v}_{in}$ signal rather than the $\tilde{v}_{out}$ signal [101]. Reduced sample rate allows capture of data over a longer time span, and therefore additional averaging, and is also makes an embedded system more tractable. A digitizing oscilloscope was used to capture signals associated with the EM. Frame averaging was used in this case as well, and was even more important given the 8-bit resolution of almost all digitizing oscilloscopes.

Time Reference

A 10-MHz reference signal is commonly used to frequency lock multiple pieces of TM equipment, forcing all to agree on a common definition of time. In the testbed it is critical that equipment generating and capturing a signal share this definition. Otherwise, the generator may stretch a 10 msec signal over 10.01 msec though the VSA captures for only 10.00 msec, missing a portion of the signal. The digitizing oscilloscopes used here have the ability to supply a 10-MHz reference but cannot lock to an external reference. The oscilloscope reference is distributed to generators, upconverter, and VSA while the oscilloscope is used to capture waveforms. The VSA's more stable 10-MHz reference is substituted when the VSA is used to capture waveforms.

5.2 System Linearization

This section discusses distortion mechanisms in each part of the transmitter. Signal processing techniques are selected and adapted to linearize each in the most direct way and in the correct sequence.

5.2.1 Distortion Mechanism Investigation

System distortion is investigated using two methods: (1) experiments on the testbed making use of test signals designed to emphasize specific distortion sources; and (2) experiments in the controlled environment of the ET system simulation tool described in Chapter 4.

For example, the following experiment was used in early work to identify a time alignment problem: a triangle-shaped amplitude waveform was filtered to remove high-bandwidth peaks and used in the V_{dd} and $\tilde{v}_{in}$ paths. When the two waveforms are misaligned, the V_{dd} waveform will either lead or lag the $\tilde{v}_{in}$ waveform, leading to a different combination of V_{dd} and $|\tilde{v}_{in}|$ for rising and falling edges of the waveform, and thus different PA gain. Fig. 5.2 shows this effect for a segment of a W-CDMA waveform rather than a triangle, but the result is the same.

The use of a filtered triangle waveform reduced the impact of high-bandwidth EM distortion of a W-CDMA signal that was present due to the EM prototype in use at the time of this experiment. However, when a signal split is applied with a troughing voltage, V_{dd} is constant for a portion of the triangle. The varying gain effect of time misalignment cannot be observed for that portion of the waveform, making the

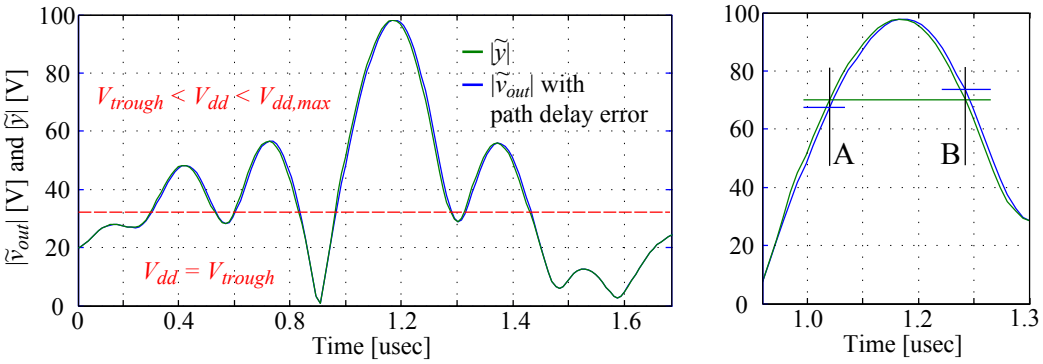


Figure 5.2: Simulated $|\tilde{y}|$ and $|\tilde{v}_{out}|$ with a small V_{dd}-path delay error (left), and close-up showing how error can be positive or negative for the same expected amplitude in the presence of V_{dd} path delay error (right).

time alignment algorithm described in [24], and later in this section, unsuitable for ET applications with large troughing voltage. The diagnostic waveform led to a deeper understanding of the time delay distortion and also sheds light on a possible solution. The fact that PA gain varies for rising and falling edges at high amplitude levels (above V_{trough}) can be used to determine if path time alignment should be advanced or delayed.

In another case the ET system simulation tool was used to determine the source of system distortion on the testbed. Both the V_{dd} and $\tilde{v}_{in}$ paths exhibited some level of distortion. The testbed and ET simulation tool were configured to operate identically, and the V_{dd} waveform was captured from the testbed. After applying the measured V_{dd} waveform in the simulation (assuming an ideal $\tilde{v}_{in}$ waveform) similar degradation in the simulated linearity was noted, pointing to the EM distortion as the dominant source of the problem. Further ET simulations with bandwidth-limited EM models showed that simulated and measured V_{dd} matched, indicating that the measured waveform distortion was primarily caused by limited EM bandwidth. In this case the ET system analysis tool proved quite useful in attributing system-level distortion to a component-level problem.

The above examples illustrate only two specific cases of distortion mechanism investigation. Many such experiments were performed in gaining the insight needed to develop the linearization methods described in the rest of this section.

5.2.2 EM Gain, Offset, and Equalization

The V_{dd} path includes several analog components, each requiring some level of DC gain and offset calibration. Correction for the whole path is determined by measuring a very slow ramp from minimum to maximum drain voltage without V_{dd} gain and offset correction. The relationship between measured V_{dd} and α is linearly fit resulting in gain and offset calibration factors. These values are not expected to change dramatically over time, temperature, or operating condition. In the lab environment this calibration is performed only once for each new EM prototype.

Measurement of the frequency response is achieved by driving the V_{dd} path with a logarithmic chirp ranging from 1 MHz to 110 MHz. Non-ideal response of the path causes variation in gain and delay of the EM output signal, as captured by the oscilloscope. The captured data is first multiplied by the original chirp signal and then multiplied by the original chirp shifted by 90 degrees and low-pass filtered, yielding an in-phase and quadrature component of gain at each instant in time.

In this measurement the chirp signal is actually "modulated" by the frequency response of the V_{dd} path. The modulated chirp signal is down-converted by a "mixer," implemented with multiplication by in-phase and quadrature versions of the original chirp (the carrier signal) followed by a low-pass filter. Frequency variation in time is combined with amplitude and phase variation in time to yield the frequency response. The measured response of the V_{dd} path for a $100\,\mathrm{mV}_{pp}$ chirp at $10\,\mathrm{V}_{dc}$ is shown in Fig. 5.3.

Frequency response in the V_{dd} path is measured and corrected using an FIR filter with the inverse response. In some testbed revisions the filter was implemented as a

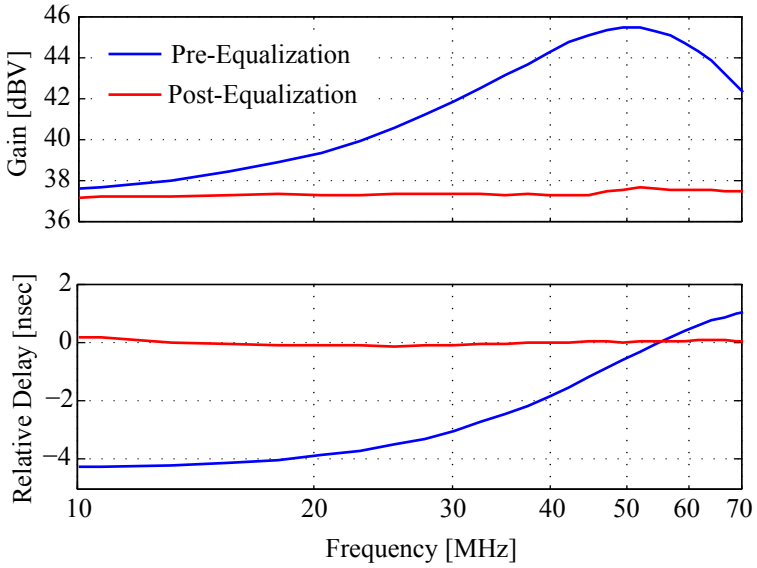


Figure 5.3: V_{dd} path frequency response before and after equalization. The linear frequency equalizer makes up a portion of the transfer function $\alpha \rightarrow \alpha'$.

feature of the commercial TM signal generator. The corrected response is shown in Fig. 5.3. The issue of EM frequency response variation with load, power level, and voltage was mentioned in Chapter 4; this method is used to evaluate EM prototype hardware at the component level under small- and large-signal excitation, over a range of DC signal levels and under varying load conditions.

This measurement and correction is only valid for linear frequency response. The addition of nonlinear distortion results in an invalid measurement and errors in correction frequency response. Note also that the frequency response of the oscilloscope will cause errors in the correction, but the error is assumed to be insignificant in this application.

Gain and offset correction are the first step in ET system calibration, followed by V_{dd} path linear frequency equalization. As noted in the introduction to this section, V_{dd} path error will be corrected to some degree (although with larger computational complexity) by the system DPD algorithm. Therefore we wish to make the V_{dd} path as linear as possible before applying other linearization techniques.

5.2.3 Signal Split

V_{dd} Signal Path

The V_{dd} path signal split is selected as a system design parameter, as discussed in Chapter 4, and is not adapted. Configurations A and B shown in the block diagram of Fig. 5.1 allow the V_{dd} signal to be derived from the desired signal $\tilde{y}$ or the post-DPD signal $\tilde{x}$. The post-DPD signal $\tilde{x}$ contains broadband anti-distortion components, requiring additional EM bandwidth, while in configuration B the V_{dd} path input signal properties remain constant throughout system linearization. Configuration B was preferred for the final proof-of-concept system. Note that $\tilde{v}_{in}$ path signal split adaptation is performed before DPD adaptation, so for the remainder of this discussion, $\tilde{x} = \tilde{y}$.

$\tilde{v}_{in}$ Signal Path

Variation of V_{dd} causes a change in PA gain and insertion phase ($\tilde{v}_{in} \rightarrow \tilde{v}_{out}$, also called complex gain $\tilde{g}_{PA}$). To achieve linear transmitter gain $\tilde{g}$ ($\tilde{y} \rightarrow \tilde{v}_{out}$) an adjustment must therefore be made to each sample of $\tilde{v}_{in}$ to account for $\tilde{g}_{PA}$. $\tilde{y}$ is scaled to the desired output power level, so the ideal PA input signal accounting for V_{dd} variation is calculated by $\tilde{\beta} = \tilde{y}/\tilde{g}_{PA}$. The signal split implements $\tilde{\beta} = \tilde{y}/\tilde{g}'_{PA}$ where $\tilde{g}'_{PA}$ is the current estimate of $\tilde{g}_{PA}$. Unfortunately $\tilde{g}_{PA}$ is a nonlinear function of the input signal statistics, which are determined by $\tilde{g}'_{PA}$. Therefore $\tilde{g}'_{PA}$ must be determined iteratively. When the solution is accurate, the transmitter gain $\tilde{g}$ becomes unity: $\tilde{v}_{out} = \tilde{y} \div \tilde{g}'_{PA} \times g_{PA} = \tilde{y} \times \tilde{g}$.

In a perfectly static (non-time-variant) system, $\tilde{g}_{PA}$ should always be the same for a given level $|\tilde{y}|$. Therefore the same value of $\tilde{g}_{PA}$ can be applied to all values of $|\tilde{y}|$. This procedure can be thought of as LUT implementation of static (or memoryless) predistortion [29]. However, dynamic effects do still exist in the system, as shown by the plot of complex transmitter gain in Fig. 5.4. Note from the plot that gain drops with reduced output power level due to the application of reduced V_{dd}.

The objective of the $\tilde{v}_{in}$ path signal split adaptation is therefore to correct for the *average* complex gain at each level $\tilde{y}$. After adaptation the black transfer function of Fig. 5.4 will still be thick (indicating dynamics have not been corrected), but the average value of gain and insertion phase at each level $\tilde{y}$ should be unity and zero, respectively. Dynamic effects will be corrected using other techniques (time alignment, DPD) in subsequent steps.

Initially the LUT implements a single value of linear gain $\tilde{g}$ for all values of $\tilde{y}$ and no variation of insertion phase ($\tilde{g}'_{PA} = 1\angle 0^\circ$ for all values of $|\tilde{x}|$). Thus, for this first iteration the PA gain $\tilde{g}_{PA}$ is equal to the measured transmitter gain $\tilde{g}$ as shown in Fig. 5.4. Signal split adaptation takes place by linear adjustment of the PA gain estimate: $\tilde{g}'_{PA,next} = \tilde{g}'_{PA,prev}/\tilde{g}$. If the PA had a linear gain characteristic over the

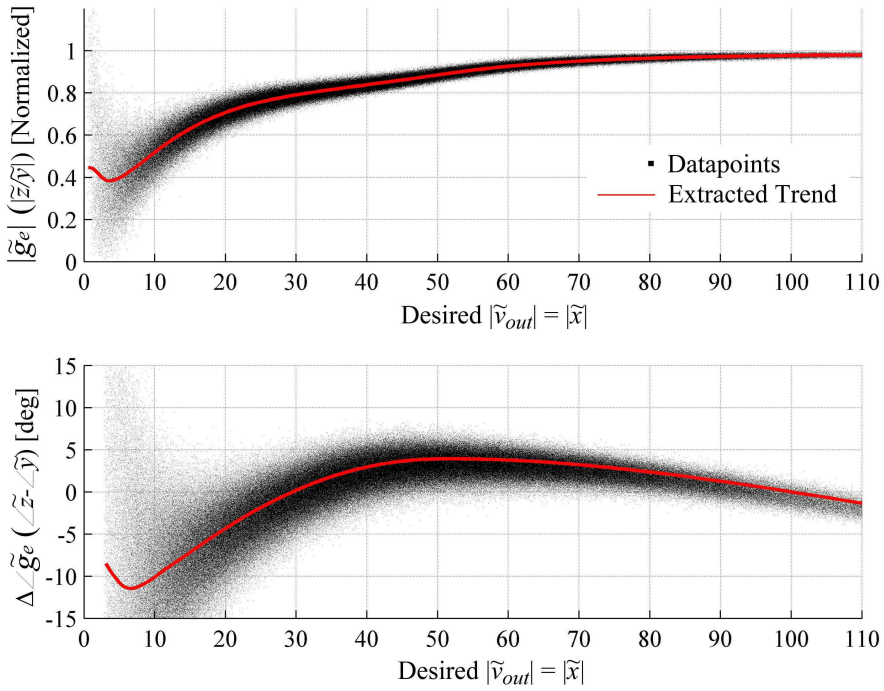


Figure 5.4: Measured instantaneous transmitter gain and insertion phase ($\tilde{g}$) after the first iteration, and the extracted trend used to adapt the estimate of PA gain ($\tilde{g}'_{PA}$) used in the second iteration.

whole V_{dd} and $\tilde{v}_{in}$ range only one adaptation would be necessary to set $\tilde{g}'_{PA}$ equal to $\tilde{g}_{PA}$. However, the PA compression characteristic indicates that as input power rises gain decreases, making the increase still inadequate to achieve desired output power. Additionally, PA insertion phase also changes with $|\tilde{v}_{in}|$, requiring further adaptation to achieve flat insertion phase.

PA gain is highest at PEP and decreases with reduced V_{dd}, so the initial gain is set equal to PEP gain. PA gain at low power (and low V_{dd}) will be inadequate for initial iterations, resulting in insufficient output power at those levels, but this practice avoids applying of too much power resulting in excessive output power or excessive compression.

Fig. 5.5 shows the adaptation history of the transfer function $|\tilde{y}| \rightarrow \tilde{\beta}$, defined by the inverse of the complex gain estimate $\tilde{g}'_{PA}$. Note that the last two iterations come to approximately the same solution, indicating acceptable convergence. The signal split

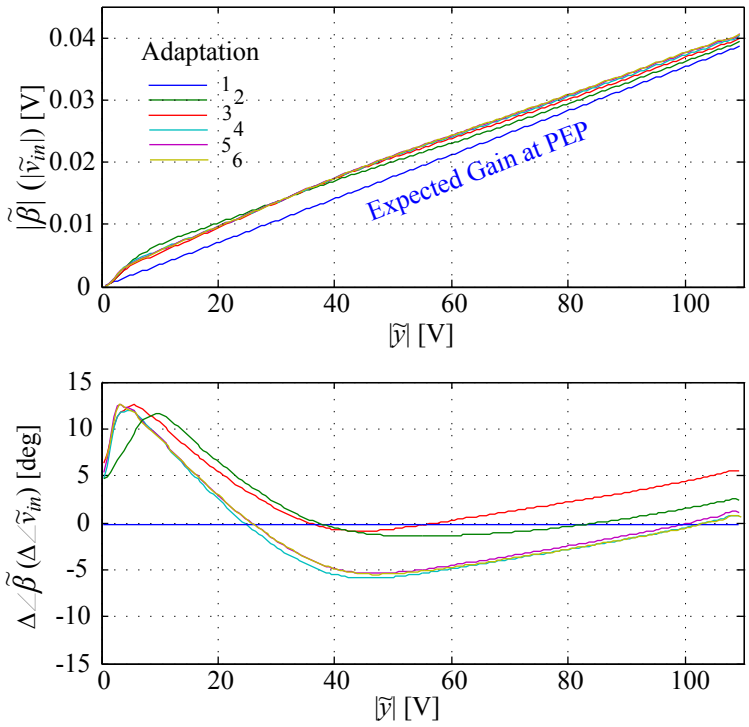


Figure 5.5: Adapted $|\tilde{y}| \rightarrow \tilde{\beta}$ transfer function after each of six signal split iterations.

aims to eliminate the average PA static nonlinear characteristics. This is a challenge in the presence of strong dynamic distortion (shown by the thickness of the transfer function of Fig. 5.4). The dominant source of such dynamic distortion is path time misalignment between the V_{dd} and $\tilde{v}_{in}$ paths. On the testbed signal split adaptations are performed until no further improvement can be made due to interference from dynamic effects. Delay adjustment (described next) is performed next to eliminate the highest-order source of dynamic distortion, followed by further iterations of signal split adaptation.

5.2.4 Delay Adjustment

The importance of correct time alignment between V_{dd} and $\tilde{v}_{in}$ paths has been discussed earlier in this chapter. Delay in the V_{dd} path is contributed primarily by the EM, and is between 5 nsec and 15 nsec for the EM prototype hardware used in this work. Some

small group delay is also naturally present in the $\tilde{v}_{in}$ path, but an adjustment is always required to synchronize V_{dd} and $\tilde{v}_{in}$ signals at the PA. The absolute amount of differential delay between a modulated RF and an analog signal cannot be directly measured, so the correct value is inferred by observing system performance metrics while delay is varied.

The problem is illustrated in Fig. 5.2 by output from an ET simulation, in which both PA and EM are ideal and the only source of distortion is a small time alignment error (V_{dd} path is slightly advanced with respect to the $\tilde{v}_{in}$ path). Recall that $V_{dd} = V_{trough}$ for low values of $|\tilde{v}_{out}|$, in this case 34 V. Since V_{dd} does not vary in the low range, delay mismatch has no effect, but above this value the time-advanced V_{dd} creates an advance in $|\tilde{v}_{out}|$. In the close-up (right) note the impact on PA gain error ($\tilde{v}_{out}/\tilde{y}$) at points A and B. At both points $|\tilde{y}|$=70 V, but, due to the path alignment error, $|\tilde{v}_{out}|$ is lower or higher than expected, resulting in gain error which changes in time. This type of gain error is also called dynamic distortion, and contributes directly to the thickness of the PA transfer function of Fig. 5.4.

Various metrics and methods have been proposed to directly compute the correct value of delay which must be added to the $\tilde{v}_{in}$ path [24]. The method assumes that the magnitude of $\tilde{v}_{out}$ is dominated by the V_{dd} path and the phase of $\tilde{v}_{out}$ is dominated by the $\tilde{v}_{in}$ path. Correlation of $|\tilde{v}_{out}|$ with $|\tilde{y}|$ yields an optimal magnitude-component delay, and correlation of $\angle\tilde{v}_{out}$ with $\angle\tilde{y}$ yields an optimal phase-component delay. The difference between the two delays indicates the error in path time alignment. This method proves inadequate for the ET system presented in this work, resulting in delay estimates which degrade final system linearity compared to blind optimization of delay values. In this ET system it cannot be assumed that the magnitude of $\tilde{v}_{out}$ is dominated by the V_{dd} path, due to the V_{dd} troughing region. Therefore the delay value obtained from correlation of $|\tilde{v}_{out}|$ with $|\tilde{y}|$ reflects the best compromise between low- and high-valued $\tilde{v}_{out}$ delay.

A delay adjustment method was discussed earlier in this section which is based on PA gain variation for rising and falling edges. That method is still under investigation, so a less elegant, brute force method is used to obtain the results presented in this work. Dominant distortion mechanisms mask the impact of corrections to less dramatic distortion mechanisms. Static nonlinear distortion typically dominates initially, so signal split adaptations are first performed to achieve coarse system linearity. Path delay adjustment is then swept through a reasonable range, searching for a minimum in ACP, as shown in Fig. 5.6.

The delay sweep must be performed after sufficient signal split adaptation, otherwise the ACP minimum will be very shallow and difficult to identify due to more-dominant nonlinear distortion. The trend can be fit to a spline and the minimum-delay value estimated using measurements at only 3-4 delay points, reducing algorithm run-time. Finally, it is critical that delay adjustment be performed before DPD correction. If path delay error is present DPD algorithms can provide some correction, though with significantly more computational overhead.

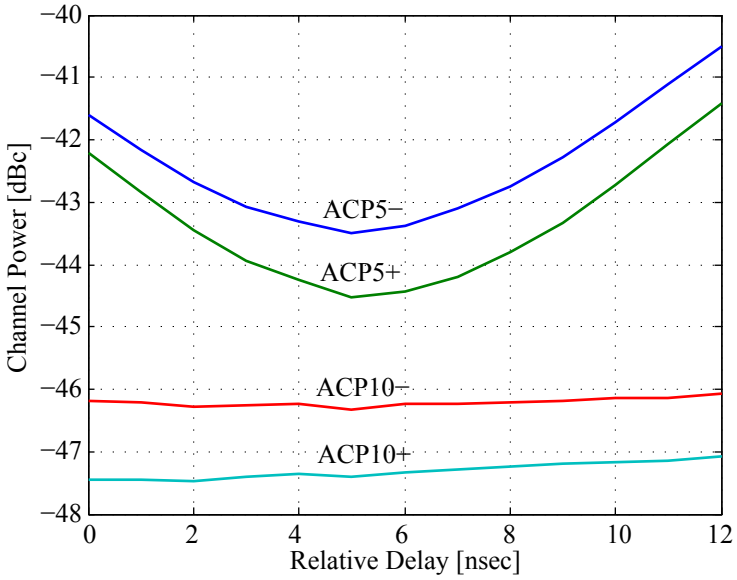


Figure 5.6: ET system ACP given varying τ_{EM} value.

5.2.5 Digital Pre-Distortion

The area of digital pre-distortion encompasses a wide variety of techniques [11], all with the same goal: to create a digital "inverse" of the PA distortion such that the cascade of DPD and PA is linear. Fig. 5.7 illustrates this concept by cascading an expanding-gain DPD with a compressing-gain PA resulting in a linear overall system.

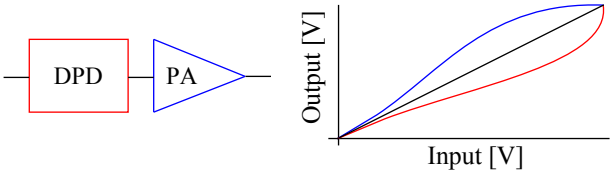


Figure 5.7: Digital pre-distortion conceptual block diagram and transfer functions.

It turns out that an adaptive static DPD has already been implemented earlier in this section to account for PA gain variation with V_{dd}. However, the LUT-based adaptation and correction used in the $\tilde{v}_{in}$ path signal split is limited to correction of static nonlinearity. The linear equalizer used in the V_{dd} path is another type of pre-distortion, in that case limited to linear time invariant distortion. In this work DPD refers to polynomial-based techniques which can correct dynamic linear and nonlinear distortion.

Polynomial-based predistorters use a set of weighted expansion functions to synthesize the inverse of the PA transfer function as shown in Fig. 5.8. Expansion functions are computed based on the desired signal $\tilde{y}$, weighted, and summed to produce DPD output $\tilde{x}$. Some representative expansion functions are shown in the figure which account for static nonlinearity ($y^p[n]$), linear frequency response ($y[n-m]$), and dynamic nonlinearity. The complete set of these expansion functions is called the Volterra series [102], and it can describe a general nonlinear time-variant system. Due to complexity, Volterra series are practical for modeling only weakly nonlinear systems with memory. Transmitter DPD requires careful down-selection of expansion functions to limit

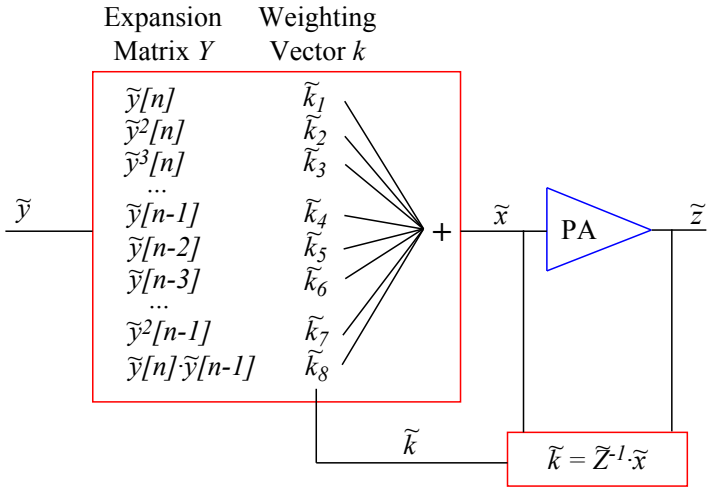


Figure 5.8: General polynomial predistorter with indirect learning.

computational complexity.

PA modeling is concerned with determination of the PA transformation $\tilde{x} \rightarrow \tilde{z}$. The DPD transfer function would ideally invert the PA response: $\tilde{y} \rightarrow \tilde{x} = \tilde{z} \rightarrow \tilde{x}$. The indirect learning method [103] is used in this work and shown in the block diagram of Fig. 5.8. In this method the expansion matrix $\tilde{Z}$ is formed from the PA input and a weighting vector $\tilde{k}$ calculated to satisfy the relationship $\tilde{Z}\tilde{k} = \tilde{x}$. This combination of expansion functions and weights is now set to emulate the inverse PA transfer function $\tilde{z} \rightarrow \tilde{x}$, and is next implemented in the forward path, applying the same transformation on $\tilde{y}$ resulting in $\tilde{x}$, the predistorted input signal.

A primary challenge in design and application of DPD algorithms is selection of an appropriate expansion function set. A small set will be unable to reproduce complex PA behavior, and a large set becomes computationally intractable. Addition of expansion functions which do not correctly represent the distortion also dilutes DPD correction power. The MP[7] [104] and DDR[8] [105] are two expansion sets used in literature. Both were investigated in this work, but the final proof-of-concept made use of the DDR

[7] memory polynomial

[8] dynamic deviation reduction

predistorter. The real-valued form of the DDR is shown below.

$$x[n] = \sum_{p=1}^{P} k_{p,0}(0,...,0)y^p[n] + \sum_{p=1}^{P}\left(\sum_{r=1}^{p}\left[y^{p-r}[n]\sum_{i_1=1}^{M}\cdots\sum_{i_r=i_{r-1}}^{M}k_{p,r}(0,...,0,i_1,...,i_r)\prod_{j=1}^{r}y[n-i_j]\right]\right) \quad (5.1)$$

The DDR leaves three degrees of flexibility: P, M, and R. Nonlinear order P determines the maximum nonlinear order for expansion functions; only odd orders are included. Memory depth M limits the number of historical expansion functions included in the model. Long-term memory effects (or dynamic distortion) require high values of M. This parameter is also dependent upon the selected capture and signal generator sample rates. High dynamic order R adds terms to bring the polynomial closer to the original Volterra series, while $R = 0$ is full reduction to a memoryless power series polynomial. In this work the useful range for P, M, and R was 3-7, 2-5, and 1-2. Increase in value of any parameter causes an increase in computational complexity. If model parameters are set for higher nonlinear order, memory depth, or dynamic order than is present in the system, the DPD can become overfit. Rather than describing system behavior it begins to describe the particular dataset.

Expansion functions are defined by the following expression for a first-order dynamic ($R = 1$) DDR predistorter, shown in the low-pass equivalent:

$$\tilde{x}[n] = \sum_{h=0}^{\frac{P-1}{2}}\sum_{i=0}^{M}\tilde{k}_{2h+1,1}(i)|\tilde{y}[n]|^{2h}\tilde{y}[n-i] + \sum_{h=1}^{\frac{P-1}{2}}\sum_{i=1}^{M}\tilde{k}_{2h+1,2}(i)|\tilde{y}[n]|^{2(h-1)}\tilde{y}^2[n]\tilde{y}^*[n-i] \quad (5.2)$$

The decomposed piecewise Volterra series [106] is an extension to the DDR theory that is especially useful to ET applications. In this work the PA is operated in two fundamentally different modes - linear or saturated - depending upon if the drain voltage is at or above V_{trough}. These modes exhibit different types of dynamic distortion. Rather than fitting one pre-distorter to both regions this method applies threshold vector de-

composition, splitting the original signal into two components as shown in Fig. 5.9.

A predistorter can be designed for each region with its own expansion functions and weighting vector. The components are then re-combined to form the full predistorted signal. Baseband signals are complex, and special attention is required to maintain phase continuity during signal decomposition and recombination. This method was applied in the final proof-of-concept system.

DPD is adapted and applied only after all other linearizing corrections have been made. Using the system simulation tool of Chapter 4 it was determined that an MP DPD is capable of compensating for a significant delay adjustment error, but requires additional expansion functions and thus increases computational complexity. As a result DPD should be disabled before adapting delay adjustment or signal split, and then re-adapted afterward.

Commercially available DPD implements feedback to continually adapt the weighting vector, responding to changing transmitter operating conditions. Such a DPD solution could integrate the $\tilde{v}_{in}$ signal split LUT capability along with the polynomial-based dynamic correction.

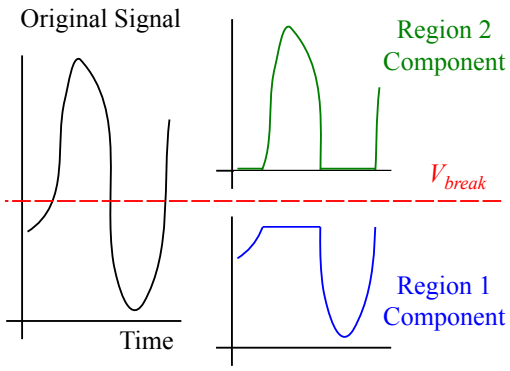


Figure 5.9: Threshold decomposition of an amplitude-only signal into two components.

5.2.6 Circular Signal Generation and Time Alignment

A single frame (10 msec) of W-CDMA chips are generated, oversampled, and filtered with a root-raised-cosine filter. In the batch-mode system the same frame is continually repeated, and the capture will likely not begin precisely at the first sample. Therefore circular convolution is used when filtering so there is no discontinuity between the amplitude and phase of the last and first samples. A CFR algorithm is applied to reduce waveform PAR to the desired level (7 dB throughout this chapter) as described in Chapter 1. In industry and literature PAR is commonly reduced to values ranging from 6.5 dB to 8 dB depending upon the acceptable level of CFR-induced distortion and the capability of the CFR algorithm in use. The resulting waveform is the complex baseband vector $\tilde{y}$, representing the desired system output.

Note that waveforms captured from the hardware ($\tilde{v}_{out}, \tilde{v}_{in}, V_{dd}, I_{dd}$, and V_{in}) are time aligned with a digital waveform before analysis or use in adaptation. The alignment must have sub-sample precision, which is achieved using Whittaker-Shannon interpolation. This process requires that waveforms be circular, band limited, and Nyquist sampled and is implemented by circularly convolving the waveform with a shifted sinc function. In practice, measured waveforms can contain aliasing due to sub-Nyquist sampling. This method continues to provide good results in these cases as well, provided that the aliased energy is not significant compared to the in-band energy.

5.2.7 Order of Adaptions

Gain, offset, linear equalization, delay adjustment, LUT adaptation, and DPD are all used to linearize different aspects of the ET system. Each block is carefully placed in the signal flow and performed in a specific sequence to correct a specific distortion mechanism. Some techniques can correct multiple mechanisms, linearizing them in an inefficient way or transforming distortion into a more complex problem.

For example, DPD adaptation must be performed last because it has the ability to correct the simple problem of path time misalignment in a very complex way. The DPD effectively implements an FIR[9] filter to shift the $\tilde{v}_{in}$ signal with respect to the V_{dd} signal. Several weights for each tap of the filter must be adaptively determined, and several expansion functions must be calculated for each sample. This use of DPD increases complexity and reduces its effectiveness for other types of distortion. Instead, adjustment of a single number - the path time delay adjustment - can be used to fix this distortion, allowing the DPD to be simplified and to better adapt to the remaining distortion it was intended to correct.

As another illustration consider a non-ideal, but linear frequency response in the V_{dd} path. Normal V_{dd} variation causes variation in PA gain and insertion phase which are pre-corrected by the signal split. Frequency-dependent amplitude distortion of V_{dd} will cause un-corrected variation in PA gain and insertion phase. Recall from Fig. 4.17 of Chapter 4 that V_{dd} distortion causes a different amount of $\tilde{v}_{out}$ distortion depending upon $|\tilde{v}_{in}|$ (or rather, depending on the level of gain compression). Therefore, a simple linear frequency response in the EM path causes $\tilde{v}_{out}$ distortion which varies with both V_{dd} frequency content and $\tilde{v}_{in}$ amplitude. This nonlinear, frequency dependent (dynamic) distortion can be corrected with a relatively simple linear equalizer (a FIR filter) in the V_{dd} path or with a significantly more complex DPD algorithm. Therefore it is important to make simple corrections in the V_{dd} path before applying more global techniques with increased complexity and corrective power.

5.3 Final Proof of Concept ET System

The testbed described above has been used to investigate many EM and PA prototypes as well as linearization techniques over the course of this work. Results spanning output

[9] finite impulse response

power level, PAR, linearity, PA technology, and signal type have been measured and used in development. The measurements presented in this section make use of the latest design iterations, and represent state-of-the-art ET performance for a 7 dB PAR W-CDMA signal with 40 W PEP at 2.14 GHz. Final system efficiency is greater than 50% with at least 7 dB ACP linearity margin.

5.3.1 PA and EM Prototype Hardware

The class F^{-1} PA of Chapter 3 was designed with ET operation in mind. The load impedance was selected for peak efficiency at 28 V, around 15 dB small signal gain near the troughing voltage, and 50 W PEP at 36 V using the load-pull contours shown in Fig. 5.10.

The latest EM prototype available at the time of this testing was designed to operate between 8 V and 33 V, so maximum system voltage was limited to 32 V and maximum output power limited to 40 W. Additionally, the EM prototype was designed to provide 400 W peak power to the PA though a maximum around only 50 W was required for this

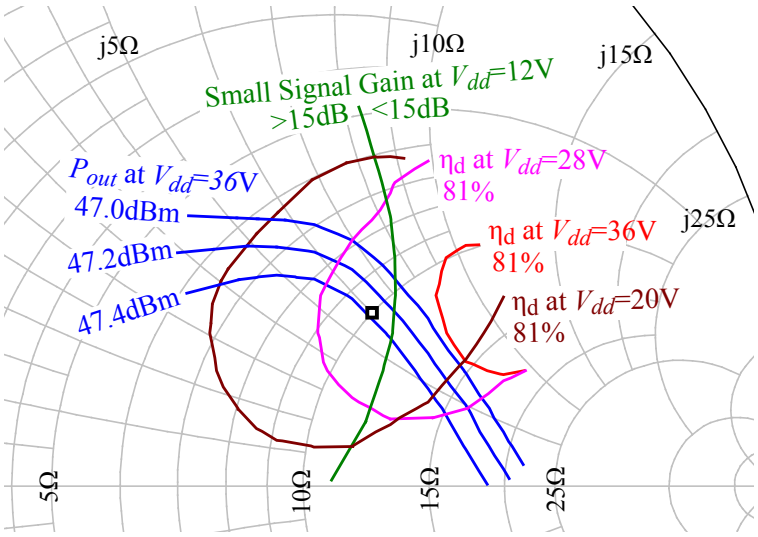


Figure 5.10: Measured load-pull contours for the TGF2023-10 GaN HEMT with class F^{-1} harmonic terminations. Efficiency is shown at 20 V, 28 V, and 36 V, small signal gain is shown at 12 V, and output power is shown at 36 V to facilitate PA design for an ET application. The black square indicates the load design impedance of 10+j6Ω.

test. Design of an EM optimized for the lower power level would reduce EM quiescent currents and improve EM efficiency. The photograph of Fig. 5.11 shows the final PA and proprietary EM prototype hardware.

5.3.2 Linearization

The EM prototype gain, phase, and frequency response were first calibrated as discussed earlier in this chapter. Next the PA was characterized under pulsed-RF/DC conditions using the measurement technique described in Chapter 3. Three V_{dd} signal split trajectories were selected for system measurement. PA efficiency and the signal split trajectories are shown in Fig. 5.12. Trajectories T1, T2, and T3 result in theoretical PAE_{PA} of 75.4%, 71.1%, and 67.1%, respectively for the W-CDMA test signal with 40 W PEP and 7 dB PAR.

Initial adaptation of the $\tilde{v}_{in}$ path signal split was successful for trajectories T2 and T3, but failed for trajectory T1. Notice how T1 comes very close to the edge in Fig. 5.12, requiring the absolute maximum amount of output power possible at each drain voltage level. Each successive adaptation of the signal split demanded higher levels of input power as shown in Fig. 5.5, but the demand was not decreased with each iteration. The

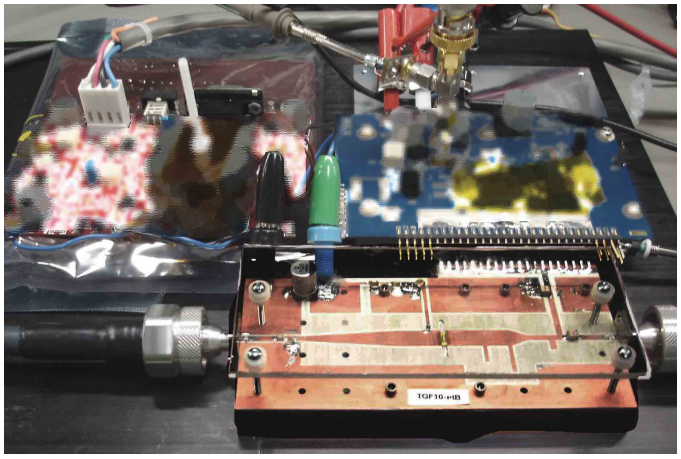


Figure 5.11: Photograph of the final PA prototype connected to the proprietary EM hardware designed by colleagues in analog and power electronics.

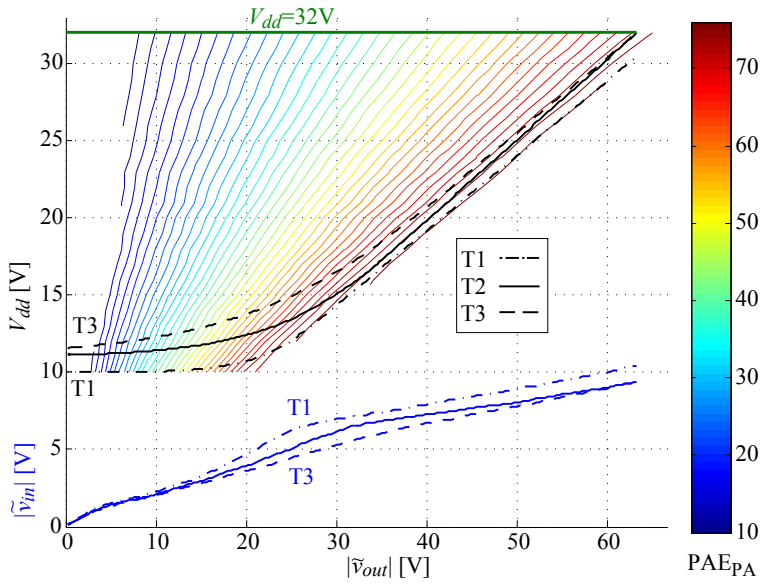


Figure 5.12: Three V_{dd} trajectories (black) and $\tilde{v}_{in}$ trajectories (blue) expected based on PA characterization data. PAE$_{PA}$ (colored contours) is measured under the pulsed-RF/DC condition.

maximum safe input power limit was reached before the $\tilde{v}_{in}$ signal split converged. No system results are available for this test case, but it serves to illustrate the problem of an overly-aggressive V_{dd} signal split trajectory.

Delay adjustment was performed, followed by additional signal split adaptations to minimize static nonlinearity. The DDR predistortion method with threshold decomposition was then used to correct dynamic nonlinearity. Region 1 was defined from 0 V $\leq |\tilde{v}_{in}| <$ 14 V and used a predistorter with parameters P, M, and R set to 5, 4, and 2, respectively. Region 2 was defined from 14 V $\leq |\tilde{v}_{in}| <$ 65 V and used a predistorter with parameters P, M, and R set to 7, 3, and 1, respectively. The threshold and DPD parameters were set by manual optimization, but in a real system these parameters will not change with operating condition or test signal.

Fig. 5.13 shows ET system output PSD at the various stages of linearization with trajectory T2. Linearized adjacent and alternate channel power levels were lower than -55 dBc and -57 dBc. Comparison with the -45 dBc and -50 dBc specifications shows a

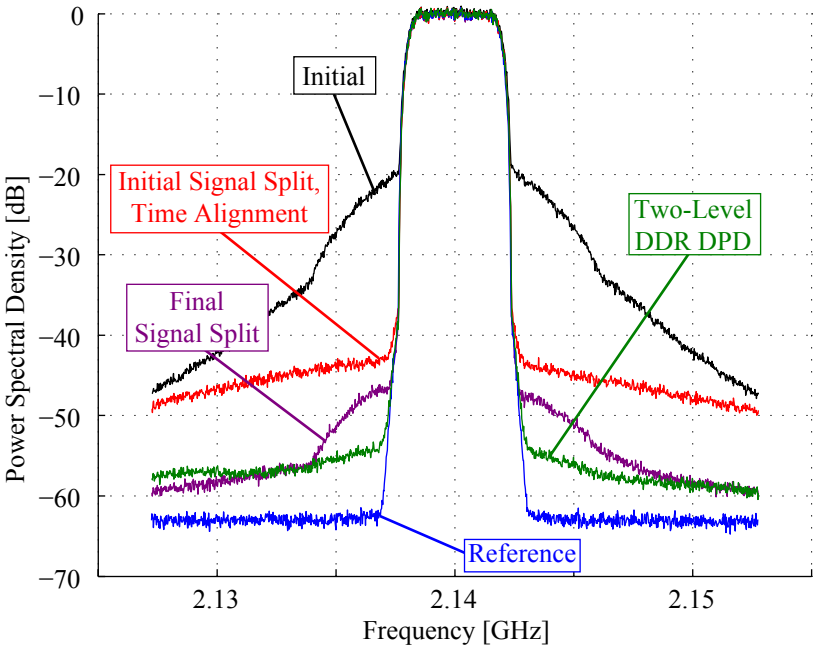


Figure 5.13: ET system output PSD at various stages of linearity correction.

linearity margin of 10 dB for ACP1 and 7 dB for ACP2. Additive EVM was less than 1%. Final linearity performance was not notably different for trajectory T3.

5.3.3 Power and Efficiency Measurements

It was noted in Chapter 3 that high efficiency is difficult to measure precisely due to uncertainty in RF power and current measurements. The problem is exacerbated here by output power modulation and the difficulty of measuring I_{dd}. The most precise, complete, and trustworthy measurements are those of average power at the system level (including loss in both the PA and EM). For these measurements a wideband RF power meter was used to measure RF input and output average power, and RMS voltage and current meters measured power into the EM. Measured average gain was 13.7 dB with 8.47 W output power. System η_d was 52.8%, resulting in a system PAE of 50.6%.

Separate EM and PA efficiency calculation requires measurement of power flowing between the two components. A heavy-gauge current loop was added between the

EM and PA, and the I_{dd} waveform was measured with a 120 MHz-bandwidth current probe. Making no other changes, the adjacent channel power rose from -55.7 dBc to -48.3 dBc, indicating a significant degradation in system linearity performance. Under this condition $\eta_{d,PA}$ was 75.9% and PAE_{PA} was 72.3%, and η_{EM} was 69.1%. Based on these component efficiency measurements system η_d (calculated $\eta_{EM} \times \eta_{PA}$) should be 52.4%, and system PAE (calculated $\eta_{EM} \times \text{PAE}_{PA}$) should be 50.0%. Given the extremely close agreement between system efficiency directly measured and calculated from component efficiency we assume that the component efficiency measurements are usefully accurate, despite the degradation in system linearity.

As a final comparison the PA was operated with a constant drain voltage supply set to 32 V. This was the maximum voltage used in the ET case and is near the minimum required to obtain 40 W PEP. DPD was applied to achieve comparable linearity to the previously described ET result with the same W-CDMA test signal. While average gain was higher (nearly 18 dB), PA drain efficiency fell from 72.3% to 30.0%.

A comparison of simulated and measured efficiency for three ET test cases and the constant-V_{dd} case is shown in Table 5.1. Note that PA efficiency is consistently higher in ET mode than was projected by simulation, even though the simulation is based on measured data. This is due to the change in operating conditions from the pulsed-RF/DC measurement to ET operation. Reduced quiescent current and dramatically reduced heating produces a change in operating conditions and total efficiency. Simulated efficiency under constant-V_{dd} operation is higher than measurement because

Table 5.1: Simulated and measured $\eta_{d,PA}$ for ET and constant-V_{dd} operation.

Trajectory	Simulated $\eta_{d,PA}$	Measured $\eta_{d,PA}$
T1	75.4 %	–
T2	71.1 %	75.9 %
T3	67.1 %	71.3 %
V_{dd}=32V	37.2 %	30.0 %

thermal loading is dramatically higher in constant-V_{dd} operation than in pulsed-RF/DC operation.

5.4 Conclusion

A state-of-the-art testbed has been designed for ET research capable of synthesizing the signal processing, generation, and capture portions of an ET transmitter. The testbed far exceeds the requirements of an implemented transmitter, limiting possible sources of distortion to the ET components and providing flexibility in the research direction. System distortion mechanisms were identified and a system of of linearization techniques were applied targeting each mechanism, along with a method to most efficiently adapt the corrections.

The testbed and linearization algorithms were developed in parallel with PA and EM prototypes over the course of approximately two years. Many useful discoveries were only possible by integration of hardware, making the early EM and PA prototypes valuable learning tools despite their inefficiency. Hardware and system configurations can be grouped into one of four configurations:

Initial Proof-of-Concept A 45-W PEP LDMOS class AB PA operated primarily in the linear region was driven by an EM prototype comprised only of a linear stage. Neither EM or PA was optimized for efficiency, but the combination was used to facilitate system level investigation and understand design requirements for future prototypes. Useful results include a signal processing method to divide V_{dd} and $\tilde{v}_{in}$ signals [45] and identification of component integration issues [43]. The system was operated in block diagram configuration A.

PA/EM Revision The higher-power 120-W PEP GaN HEMT overdriven class AB PA described in Chapter 4 was driven by an EM prototype incorporating a SMPS for improved efficiency. Further improvements at the system level include path time

alignment methods [46] and PA characterization methods [44] enabling the system analysis method of Chapter 3 [42].

System/EM Revision The same 120-W PEP GaN HEMT PA was driven by a new EM prototype with significantly more dynamic capability. A signal split algorithm to adapt the $|\tilde{x}| \rightarrow \tilde{\beta}$ transfer function was also incorporated [42].

Final Proof-of-Concept The 40-W PEP GaN HEMT class F^{-1} PA described in Chapter 3 provided a significant increase in PA efficiency. An advanced EM prototype was designed by collaborators with design guidance from the static ET simulation tool presented in Chapter 4 [42]. A DDR DPD algorithm with amplitude decomposition was used in place of the previous memory polynomial method, and block diagram configuration B was found to provide more system-level linearity correction.

Table 5.2 summarizes results obtained at each stage of development, spaced by roughly six months. The final proof-of-concept configuration achieves excellent efficiency and significant system and PA efficiency improvement. A comparison between drive modulation and this ET configuration is presented in the next chapter.

The primary contributions of this chapter are the following:

- A state-of-the-art automated ET testbed was developed using specialized commercial test and measurement equipment. Signal processing and hardware control is achieved through the use of custom MATLAB-based software. The testbed exceeds requirements for an implemented ET system, an essential feature for ET research which also provides a great deal of flexibility.

- ET system distortion mechanisms are identified and quantified with hardware experiments using diagnostic waveforms. Linearization methods are developed targeting each distortion mechanism including V_{dd} DC calibration and path equaliza-

tion, signal split adaptation, path delay adjustment, and polynomial-based DPD. A procedure is also outlined to achieve system linearization in the most computationally efficient manner.

- Several iterations of PA and EM design and integration produce prototypes and linearization techniques incorporated into a final proof-of-concept demonstration. The ET proof-of-concept transmitter meets 3GPP W-CDMA linearity specifications with more than 7 dB ACP margin and 50.6% system PAE at 2.14 GHz with 7 dB PAR W-CDMA modulation at 40 W PEP.

Table 5.2: Summary of four milestone ET transmitter measurement results.

Parameter	Initial PoC	PA/EM Revision	System/EM Revision	Final PoC
System Performance				
Test Signal PAR	10.0 dB PAR	8.0 dB PAR	7.0 dB PAR	7.0 dB PAR
$P_{out,avg}$	2.0 W	17.0 W	26.5 W	8.5 W
$P_{out,peak}$	20.6 W	121.9 W	151.2 W	40.0 W
Gain	10.2 dB	13.4 dB	12.9 dB	13.7 dB
Additive EVM	<1 %	<1 %	<1 %	<1 %
ACP5	-52.0 dB	-46.7 dB	-50.5 dB	-55.7 dB
ACP10	-56.0 dB	-55.7 dB	-59.5 dB	-57.8 dB
System η_d	9.9 %	33.2 %	33.3 %	52.8 %
System PAE	8.9 %	31.6 %	31.6 %	50.6 %
EM Performance				
Design Type	Linear Amp	Lin+SMPS rev1	Lin+SMPS rev2	EM rev3
Component η_d	34.6 %	61.2 %	60.8 %	69.1 %
PA Performance				
Design Type	Backed-off Class AB	Overdriven Class AB	Overdriven Class AB	Class F^{-1}
Transistor	AGR21045 LDMOS	NPT25100 GaN	NPT25100 GaN	TGF2023-10 GaN
Component η_d	28.6 %	54.5 %	55.3 %	75.9 %
Component PAE	25.7 %	52.0 %	52.6 %	72.3 %

Chapter 6

Conclusion

Contents

6.1 Thesis Summary

The goal throughout this work has been to reduce power dissipation in high-power microwave transmitters for high-PAR signals while maintaining a high degree of linearity. Chapter 1 described statistics of a representative high-PAR signal (single-carrier W-CDMA downlink), in which the average power level is 6 dB to 10 dB higher than the infrequently-occurring peak power level. PA efficiency naturally degrades with reduced output power level, resulting in low average PA efficiency for high-PAR signals.

This research combines three different approaches in different frequency and signal regimes to achieve high efficiency and linearity for high-PAR signals: (1) high-efficiency PAs at the RF carrier frequency; (2) supply modulation at the envelope bandwidth frequency; and (3) linearization and signal processing in the digital domain.

1) High-Efficiency PA Design - In a high-efficiency PA transistor dissipation is reduced by shaping drain voltage and current waveforms using harmonic energy. This RF design technique dramatically increases PA efficiency in compressed operation, but efficiency still degrades with output power back-off. Theory of high-efficiency design was discussed in Chapter 2. Chapter 3 developed practical design techniques demonstrated with example prototypes at UHF and S-band.

2) Supply Modulation - Analog electronics are required to precisely vary the PA drain supply voltage for compressed operation at reduced output power levels. The ET system presented here maintains a specific relationship between drain voltage and input power to achieve high PA efficiency over a wide range of output power levels. Chapter 4 described requirements and interaction of the two components and introduced a measurement-based system simulation method for system analysis, design validation, and diagnostics.

3) Linearization - Adaptive signal processing techniques at baseband include linear equalization, static look-up-table predistortion, path delay adjustment, and polynomial-based dynamic predistortion. Design, choice of technique for specific distortion mechanisms, and adaptation algorithms for each signal processing block is discussed in this chapter.

Fig. 6.1 illustrates these concepts with projections of traditional and ET operation based on measured data from the class F^{-1} design used in the final proof-of-concept demonstration described in Chapter 5.

PA drain efficiency over 70% is shown over an 8 dB output power range, provided drain supply voltage is varied between 12 V and 32 V. This combination of high-power, high-frequency, high-efficiency performance is made possible by using the theory and techniques described in Chapters 2 and 3. In conventional operation drain voltage remains fixed with output power level and efficiency quickly degrades, as shown by the blue "32 V Drive Modulation" curve. The signal PDF in the middle plot reveals that the

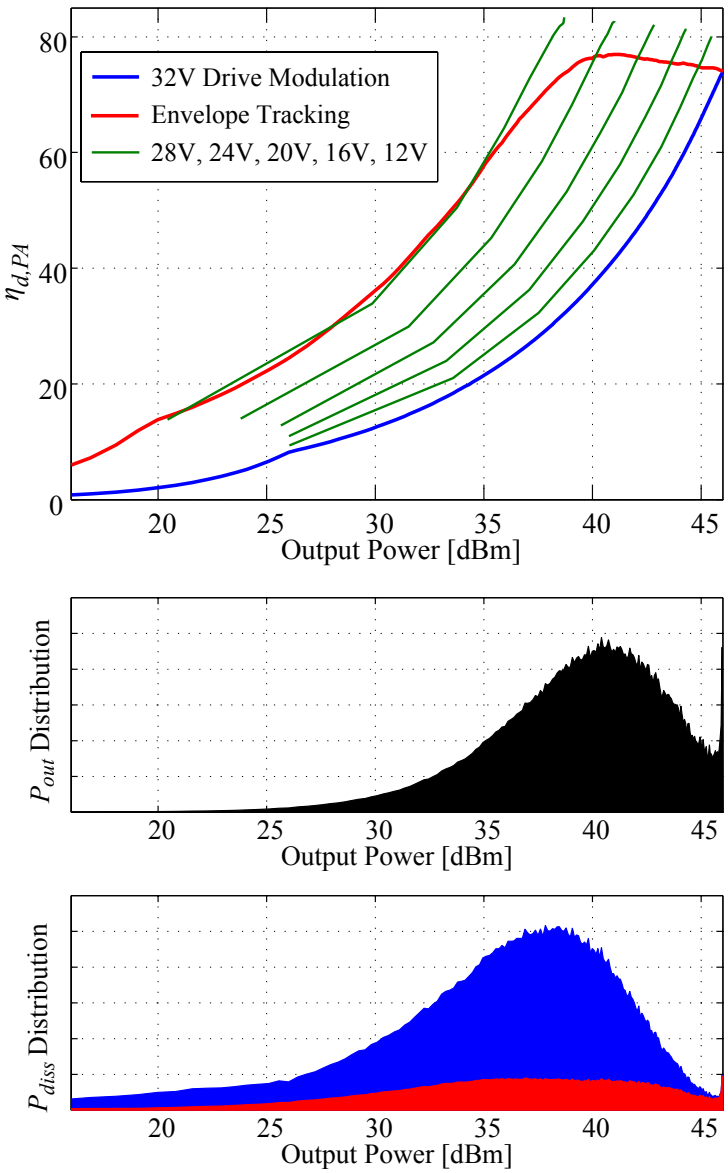


Figure 6.1: Measured drain efficiency vs. output power for the class F^{-1} GaN HEMT PA at 2.14 GHz described in Chapter 5. Measurements are made with varying drain supply voltages under pulsed-DC/RF condition (top). Projected efficiency in ET mode is shown by the red efficiency vs. output power curve. Output power distribution for the 40 W PEP, 7 dB PAR W-CDMA test signal (middle). Distribution of PA power dissipated in the RF transistor for 32-V drive modulated and ET modes (bottom).

bulk of the output distribution is produced with low efficiency, leading to high power dissipation as shown by the blue area in the bottom plot. ET operation maintains high efficiency over a much larger output power range, dramatically reducing the power

dissipated in the RF transistor.

Table 6.1 compares power measurements for the class F^{-1} PA prototype under drive modulation and ET configurations with 7 dB PAR W-CDMA modulation, both exceeding W-CDMA linearity requirements with significant margin. Envelope tracking results offer a significant improvement over equivalent drive modulated PA performance, bringing transmitter drain efficiency from 30.0% to 52.6%. System power consumption drops from 28.3 W to only 16.2 W. Operating from a fixed power supply, the ET solution provides 74.7% longer operation than the drive modulated solution. The ET solution consumes 42.8% less power than the drive modulated solution, cutting energy cost and emissions.

Fig. 6.2 compares power dissipation in ET and drive modulation conditions. Cooling requirements are greatly reduced in the ET transmitter. In addition to dissipating less total power, the ET transmitter divides power dissipation into two blocks. The EM dissipates 5.0 W and the PA dissipates 2.7 W in ET mode, as compared to the single-point thermal load of 19.8 W at the RF transistor in drive-modulated mode.

PA efficiency is dramatically increased in ET mode as well, bringing $\eta_{d,PA}$ from only 30.0 % to 75.9 %. Power dissipated in the RF transistor thus falls from 19.8 W to only

Table 6.1: Transmitter power budget in traditional and ET configurations using a high-efficiency class-F^{-1} PA.

	Drive Modulation	Envelope Tracking
Average RF Output Power	8.5 W	8.5 W
Peak RF Output Power	40.0 W	40.0 W
Transmitter Drain Efficiency	30.0%	52.5%
Transmitter Supply Power	28.3 W	16.2 W
Transmitter Dissipated Power	19.8 W	7.7 W
EM Efficiency	–	69.1%
EM Input Power	–	16.2 W
EM Dissipated Power	–	5.0 W
PA Drain Efficiency	30.0%	75.9%
PA Drain Supply Power	28.3 W	11.2 W
PA Dissipated Power	19.8 W	2.7 W

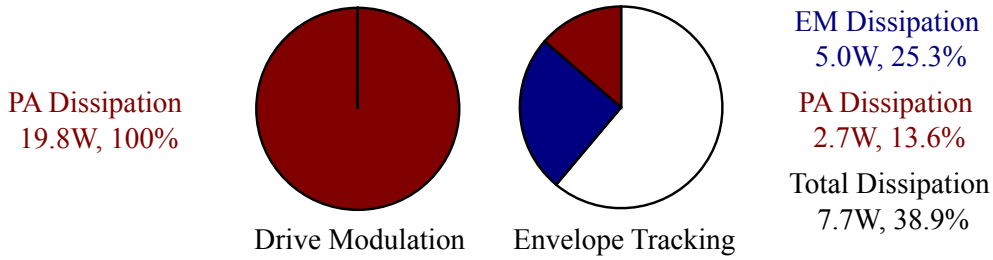


Figure 6.2: Transmitter power dissipation in drive modulated and ET configurations using the final proof-of-concept class F^{-1} PA prototype with 7 dB PAR W-CDMA modulation.

2.7 W in ET mode, dramatically reducing thermal loading. Reduced die temperature leads to higher RF performance and improved reliability. Lifting the requirement that an RF transistor operate under a high thermal load allows new degrees of flexibility in device design, potentially leading to higher performance transistors in the future.

6.2 Contributions

All the theory and techniques described in this thesis target high-efficiency linear transmitter design and can be grouped into three areas of contribution: (1) high-efficiency PA design techniques and prototypes; (2) ET architecture and system simulation; and (3) ET system integration and proof-of-concept hardware demonstration. A list of publications, presentations, courses, and disclosures is presented in Chapter 1. Contributions are listed at the end of Chapters 3, 4, and 5, and also summarized here:

1) High-Efficiency PA Design Techniques and Prototypes

- High-efficiency PA design relies heavily upon empirical design techniques due to complex and non-ideal behavior of high-power microwave devices as described in Chapter 2. A new load-pull technique is developed which makes use of harmonic pre-match circuits to enforce harmonic impedance terminations necessary for high-efficiency operation. This innovation allows harmonic impedance control without

the use of expensive and not commonly available mechanical harmonic tuners. The method is demonstrated for the case of a switched-mode class E LDMOS design at 360 MHz producing 110 W with 83% drain efficiency and 16.0 dB gain.

- Package and device parasitic effects play an increasing role as power and frequency of operation rise. A method is developed to determine feasibility of different modes of high-efficiency operation given these impediments, requiring full-wave analysis of packaging technology and extraction of device parasitics. A demonstration of the method results in a 36-W GaN HEMT class F^{-1} design example at 2.14 GHz achieving 81% drain efficiency with 14.5 dB gain, a literature-leading result to the best of the author's knowledge.

2) ET Architecture and System Simulation

- High PA efficiency can be maintained over a range of output power levels using supply modulation. An ET architecture is presented making use of both drain and drive amplitude modulation in a ratio defined by a "signal split". The signal split is designed at the system level to emphasize EM linearity or PA efficiency in an effort to optimize overall transmitter efficiency and linearity.

- New methods for PA design considering ET applications are described. A collection of load-pull contours are measured at varying drain voltage, at different levels of compression, and showing different performance metrics. Load impedance must be a compromise of performance in several categories: low-drain-voltage small-signal gain; high efficiency at a specific drain voltage (typically the RMS value of the V_{dd} waveform); and peak power at maximum EM voltage. The drain bias network is also re-designed to allow modulation supply voltage and current at the envelope bandwidth.

- A method of PA characterization is developed and used to build an ET system

simulation. A number of simulation analyses are used to: 1) demonstrate how the signal split connects EM dynamic performance, PA efficiency, and system linearity; 2) show the impact of EM output impedance on system linearity; and 3) investigate the power of DPD to correct path delay adjustment and V_{dd} path distortion. In the process of system integration the simulation also proved useful as a diagnostic tool for identifying causes of system distortion.

3) ET System Integration and Proof-of-Concept

- A flexible ET testbed is constructed using commercial TM equipment and MATLAB signal processing. The successful final implementation was the result of four increasingly better EM prototypes and PA prototypes and their integration. The EM prototypes were designed by analog and power electronics colleagues based on knowledge gained through the work described in Chapters 4 and 5. The ET system simulation tool was instrumental in providing specifications and validating EM performance in the ET system. It should be noted that one of the biggest challenges in this work is successful integration of analog, digital, and RF components. For example, integration of the PA and the EM requires design of a new type of bias network in which the EM provides the low-frequency low-impedance termination, replacing the bypass capacitance traditionally required for PA stability. Additionally, the inductance of the RF choke and interconnect must be minimized, in contrast to the usually desired large inductance of an ideal RF choke. This leads to new insights into PA stability in an ET system.

- ET distortion mechanisms were identified through the use of the ET simulation tool and in hardware through the use of diagnostic experiments using test waveforms designed to isolate specific behaviors. For example, the problem of EM output impedance peaking was only identified through the use of the ET simulation tool, leading to new EM design guidelines. The various distortion mecha-

nisms that were identified and corrected for with signal processing include linear EM frequency response, path time delay, static PA nonlinearity due to V_{dd} and $|\tilde{v}_{in}|$ operating conditions, and PA dynamic distortion including self-heating and charge trapping effects. This investigation led to a new understanding of how ET distortion mechanisms are distributed among different ET components, as well as in the time, frequency, and amplitude domains. This, in turn, led to targeted linearization approaches which result in a simpler, more computationally efficient, and better final performance system.

- A 40-W class F^{-1} PA is designed for ET application at 2.14 GHz using the harmonic load-pull techniques described earlier and paired with an advanced EM prototype developed by collaborators. System linearization techniques provide greater than 7 dB ACP linearity margin with a 7 dB PAR W-CDMA test signal at 40 W PEP (8.5 W average power), and system PAE over 50%. This performance is among the highest reported in literature at this power level, frequency, and modulation type.

6.3 Future Directions

The broad scope of this work leaves open questions in the areas of high-efficiency PA design, analog and power electronics, signal processing techniques, and system integration. Additionally, the concepts presented in this work can be used in applications besides the W-CDMA base station, bringing new requirements and challenges. The flexibility of the ET simulation method and hardware testbed will allow us in the future to investigate applications well outside the scope of the high-power S-band W-CDMA downlink base-station transmitter. Several of the most interesting avenues for future investigation are described below.

Harmonic-Terminated Module Design - Chapter 3 described chip/wire con-

struction used to eliminate package parasitics, allowing the microstrip harmonic termination network to be placed closer to the transistor. Alternately, the harmonic resonators could be implemented inside a microwave package in the form of an IPD[1], or with chip capacitors and bond-wire inductors. The result is a packaged module with internal harmonic termination networks, simplifying external matching network design. Module-level terminations can be placed electrically closer to to the transistor, potentially lowering the Q-factor of the harmonic match. Modules can also be built with tight dimensional tolerance, allowing precise repeatability for sensitive high-Q terminations. This work would begin with investigation of the types of resonant structures which can practically be constructed in a module, e.g. coaxial resonators, MOS capacitors, followed by full-wave EM simulations verified by component measurements. This requires industrial-type resources and to the best of the author's knowledge some transistor manufacturers (e.g. Freescale, Sumitomo) have started pursuing this path.

RF Transistors Optimized for ET Operation - Chapter 6 noted dramatically reduced power dissipation in the RF transistor when operating in ET mode (from 19.8 W under drive modulation to only 2.7 W). In Chapter 5 it was noted that transistor performance was improved in ET mode, even as compared to low-duty-cycle pulsed operation. It is clear that operation in ET mode is quite different from other traditional modes, and it follows that some requirements of traditional modes no longer apply (e.g. no need to withstand a large thermal load). Potential exists for microwave devices to be optimized for the ET mode of operation, giving up the ability to operate in CW or pulsed modes for further increased ET mode efficiency.

Integrated DPD Solution for ET - Due to the highly proprietary nature of DPD chipsets, it is not known whether or not a given commercially-implemented DPD solution would be suitable for ET applications. Ideally, an integrated DPD solution would implement both an adaptive static LUT (signal split adaptation), an adaptive

[1] integrated passive device

polynomial-based memory correction, and path delay adjustment. An ET-specific DPD should also compute the drain voltage signal based on the desired V_{dd} path signal split trajectory and apply V_{dd} path equalization.

Combination Doherty-ET Architecture - Doherty operation was discussed in Chapter 1 as an alternative method for efficient amplification of high-PAR signals. Benefit could be realized from merging the two concepts. Consider a typical Doherty design with an EM controlling drain voltage of the carrier amplifier. In the simplest case the carrier PA is supplied maximum drain voltage while the peaking PA is operating, and ET operation takes over when the peaking amplifier turns off. The carrier amplifier would continue to operate in compression until the minimum drain voltage was reached, extending the high-efficiency output power range below the 6 dB range typical of Doherty operation. This basic idea is already under investigation [107], and a wide variety of more complex control schemes can also be considered.

Mobile Applications - Mobile high-power high-PAR transmitters, such as those in UAVs[2], operate from a fixed power supply and are sensitive to mass and size. ET offers the possibility of reducing battery size or extending battery life. Additionally, less heat dissipation spread over a larger area can lead to smaller and lighter thermal management solutions. New cellular standards make use of OFDM and SC-FDMA[3] modulation [108], as well as MIMO[4] transmit diversity to improve performance of the uplink. These improvements increase signal PAR, making the ET architecture described in this thesis an attractive alternative to traditional drive modulation. The low power and small form factor of the handset application adds a number of ET implementation challenges not yet addressed in this thesis, such as: 1) miniaturization of the EM switching components, requiring a higher switching frequency to reduce the size of magnetics; 2) simplification

[2] unmanned arial vehicles

[3] single-carrier frequency division multiple access

[4] multiple input multiple output

of the signal processing algorithms to keep DSP[5] power consumption low; and 3) design of harmonic-tuned low-power MMIC[6] PAs for ET applications.

Radar Transmitters - The most common radar transmit modulation is the constant-amplitude, phase-modulated pulse. The high power levels required demanded pulsed operation and an efficient class C amplifier strictly from a heat management perspective. Because the class C amplifier is so inherently nonlinear, and to keep efficiency high, no amplitude modulation is incorporated. Unfortunately, these constant-amplitude waveforms often produce large spectral skirts, interfering with frequency-adjacent applications. Availability of a highly-efficient transmitter for high-PAR waveforms opens a new degree of freedom for radar waveform designers: amplitude modulation. Recent work [47] has shown that radar performance and spectral benefits can be realized even using the simplest amplitude-modulated radar waveforms. Furthermore, the amplitude modulation of these waveforms is likely to have far less dynamic content than the communications applications considered here, easing the EM design challenge and improving system efficiency.

[5] digital signal processing

[6] monolithic microwave integrated circuit

Bibliography

[1] H. L. Krauss, C. W. Bostian, and F. H. Raab, *Solid State Radio Engineering*. John Wiley & Sons, first ed., Mar. 1980. 6, 28, 34, 39, 41, 48, 51, 101

[2] J. Hoversten, M. Roberg, and Z. Popovic, "Harmonic load pull of high-power microwave devices using fundamental-only load pull tuners," in *ARFTG Microwave Measurement Symposium Digest, 2010. ARFTG 2010.*, (Anaheim, CA), May 2010. 6, 7, 24, 26, 56, 98

[3] T. Mader, *Quasi-Optical Class-E Power Amplifiers*. PhD thesis, Department of Electrical and Computer Engineering, University of Colorado at Boulder, Boulder, CO, 1995. 6, 49, 52, 53

[4] S. Pajic, *Robust Design Methodology for Class-E Amplifiers for Microwave Communications*. PhD thesis, Department of Electrical and Computer Engineering, University of Colorado at Boulder, Boulder, CO, 2005. 6, 49, 57, 62

[5] N. Lopez, J. Hoversten, and Z. Popovic, "Design method for UHF class-E power amplifiers," in *Compound Semiconductor Integrated Circuit Symposium, 2009. CISC 2009. Annual IEEE*, pp. 1–4, 2009. 7, 24, 53, 56, 71, 78, 90, 92, 97

[6] J. Hoversten, M. Roberg, and Z. Popovic, "Ultra-high-efficiency LDMOS UHF PAs for radar applications." to be presented at the 2010 CNC/USNC/URSI Radio Science Meeting, July 2010. 7, 24, 56, 77, 97

[7] J. Proakis and M. Salehi, *Digital Communications*. McGraw-Hill, 5th ed., Nov. 2007. 7

[8] K. Li, "Mobile communications 2008: green thinking beyond TCO consideration," Whitepaper IN0804307WHT, InStat, May 2008. 9

[9] D. Zimring and A. Fedosseev, "Energy efficiency, dematerialization, and the role of the broadband forum," Marketing Report MR-204, Broadband Forum, Sept. 2009. 9

[10] L. Larson, D. Kimball, and P. Asbeck, "Linearity and efficiency enhancement strategies for 4G wireless power amplifier designs," in *Custom Integrated Circuits Conference, 2008. CICC 2008. IEEE*, pp. 741–748, 2008. 10, 23, 102

[11] L. Larson, D. Kimball, P. Asbeck, P. Draxler, J. Deng, and M. Li, "Digital predistortion techniques for linearized power amplifiers," in *Microwave Conference, 2006. APMC 2006. Asia-Pacific*, pp. 1048–1051, 2006. 10, 154

[12] R. Sperlich, Y. Park, G. Copeland, and J. Kenney, "Power amplifier linearization with digital pre-distortion and crest factor reduction," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, vol. 2, pp. 669–672, 2004. 10

[13] W. Doherty, "A new high efficiency power amplifier for modulated waves," *Proceedings of the IRE*, vol. 24, no. 9, pp. 1163–1182, 1936. 10

[14] B. Kim, J. Kim, I. Kim, and J. Cha, "The Doherty power amplifier," *Microwave Magazine, IEEE*, vol. 7, no. 5, pp. 42–50, 2006. 10

[15] R. Sweeney, "Practical magic," *Microwave Magazine, IEEE*, vol. 9, no. 2, pp. 73–82, 2008. (Doherty design techniques). 11

[16] C. Steinbeiser, T. Landon, and C. Suckling, "250W HVHBT Doherty with 57% WCDMA efficiency linearized to -55dBc for 2c11 6.5dB PAR," in *Compound Semiconductor Integrated Circuit Symposium, 2007. CSIC 2007. IEEE*, pp. 1–4, 2007. 11

[17] X. Zhang, L. E. Larson, and P. Asbeck, *Design of Linear RF Outphasing Power Amplifiers*. Artech House Publishers, Mar. 2003. 11

[18] S. Cripps, *Advanced Techniques in RF Power Amplifier Design*. Artech House Publishers, 2002. 11, 40

[19] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," *Proceedings of the IRE*, vol. 40, no. 7, pp. 803–806, 1952. 12, 78, 101

[20] F. Raab, "Drive modulation in Kahn-technique transmitters," in *Microwave Symposium Digest, 1999 IEEE MTT-S International*, vol. 2, pp. 811–814 vol.2, 1999. 12, 52, 102

[21] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*. Artech House Publishers, 2 ed., May 2006. 12, 28, 36, 37, 41, 46, 102

[22] N. Lopez, X. Jiang, D. Maksimovic, and Z. Popovic, "A high-efficiency linear polar transmitter for EDGE," in *Radio and Wireless Symposium, 2008 IEEE*, pp. 199–202, 2008. 12, 109

[23] N. Wang, N. Lopez, V. Yousefzadeh, J. Hoversten, D. Maksimovic, and Z. Popovic, "Linearity of X-band Class-E power amplifiers in a digital polar transmitter," in *Microwave Symposium, 2007. IEEE/MTT-S International*, pp. 1083–1086, 2007. 12, 25, 52, 102

[24] F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, and L. Larson, "An improved power-added efficiency 19-dBm hybrid envelope elimination and restoration power amplifier for 802.11g WLAN applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 12, pp. 4086–4099, 2006. 12, 146, 152

[25] I. Kim, Y. Y. Woo, J. Kim, J. Moon, J. Kim, and B. Kim, "High-efficiency hybrid EER transmitter using optimized power amplifier," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, no. 11, pp. 2582–2593, 2008. 12

[26] F. Wang, D. Kimball, J. Popp, A. Yang, D. Lie, P. Asbeck, and L. Larson, "Wideband envelope elimination and restoration power amplifier with high efficiency wideband envelope amplifier for WLAN 802.11g applications," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 2005. 4 pp. 12

[27] C. Li, C. Chen, T. Horng, J. Jau, and J. Li, "High average-efficiency multimode RF transmitter using a hybrid quadrature polar modulator," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 55, no. 3, pp. 249–253, 2008. 12

[28] F. Wang, A. Yang, D. Kimball, L. Larson, and P. Asbeck, "Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, no. 4, pp. 1244–1255, 2005. 12, 102, 110

[29] P. Draxler, S. Lanfranco, D. Kimball, C. Hsia, J. Jeong, J. van de Sluis, and P. Asbeck, "High efficiency envelope tracking LDMOS power amplifier for W-CDMA," in *Microwave Symposium Digest, 2006. IEEE MTT-S International*, pp. 1534–1537, 2006. 12, 102, 115, 124, 149

[30] D. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, and P. Asbeck, "High-efficiency envelope-tracking W-CDMA base-station amplifier using GaN HFETs," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 11, pp. 3848–3856, 2006. 13, 103

[31] D. Kimball, M. Kwak, P. Draxler, J. Jeong, C. Hsia, C. Steinbeiser, T. Landon, O. Krutko, L. Larson, and P. Asbeck, "High efficiency WCDMA envelope tracking Base-Station amplifier implemented with GaAs HVHBTs," in *Compound Semiconductor Integrated Circuits Symposium, 2008. CSIC '08. IEEE*, pp. 1–4, 2008. 13, 103

[32] 3rd Generation Partnership Project, "3GPP technical specification 25.104 v3.7.0 (2001-06), UTRA (BS) FDD; radio transmission and reception (rel. 1999)." 19, 21

[33] 3rd Generation Partnership Project, "3GPP technical specification 25.141 v3.6.0 (2001-06); base station conformance testing (rel. 1999)." 19, 22

[34] M. Rumney, *LTE and the Evolution to 4G Wireless*. Agilent Technologies, 2009. 19

[35] C. Potter, "System analysis of a W-CDMA base-station PA employing adaptive

digital predistortion," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2002 IEEE*, pp. 275–278, 2002. 22, 129

[36] W. Kim, K. Cho, S. Stapleton, and J. Kim, "An efficient crest factor reduction technique for wideband applications," *Analog Integrated Circuits and Signal Processing*, vol. 51, pp. 19–26, Apr. 2007. 22

[37] J. Hoversten and Z. Popovic, "High efficiency power amplifier design." short course presented at Sandia National Laboratory, Livermore, CA, May 2008. hosted by Dr. Michael Forman. 24

[38] Z. Popovic, J. Hoversten, and N. Lopez, "Design and linearization techniques for high-efficiency UHF through X-band class-E power amplifiers." Invited workshop segment presented at the 2008 IEEE International Microwave Symposium, June 2008. 24, 56, 97

[39] Z. Popovic, J. Hoversten, and N. Lopez, "UHF to X-Band Class-E amplifier: Design and linearization." Invited workshop segment presented at the 2008 IEEE Radio and Wireless Sympoisum, Jan. 2008. 24, 56, 97

[40] N. Lopez, J. Hoversten, M. Poulton, and Z. Popovic, "A 65-W high-efficiency UHF GaN power amplifier," in *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pp. 65–68, June 2008. 24, 53, 56, 71, 97

[41] B. Lindseth, W. Brown, S. Cohn, J. Jordan, D. Law, T. Hock, N. Lopez, J. Hoversten, and Z. Popovic, "High power amplifier design for a new 449MHz wind profiler radar." presented at the 2009 CNC/USNC/URSI Radio Science Meeting, Jan. 2010. 24, 97

[42] J. Hoversten and Z. Popovic, "Envelope tracking system analysis method," in *IEEE Radio and Wireless Symposium, 2010. RWS 2010.*, (New Orleans, LA), Jan. 2010. 25, 134, 166

[43] J. Hoversten, Z. Popovic, M. Norris, and D. Maksimovic, "Power amplifier to envelope modulator interconnect for envelope tracking transmitters." Intellectual property disclosure at the University of Colorado at Boulder, Boulder, CO, Apr. 2009. 25, 112, 117, 134, 165

[44] J. Hoversten and Z. Popovic, "RFPA characterization method for use in envelope tracking transmitter design." Intellectual property disclosure at the University of Colorado at Boulder, Boulder, CO, Apr. 2009. 25, 134, 166

[45] J. Hoversten, M. Norris, Z. Popovic, and D. Maksimovic, "Optimal-PAE polar split for efficient and linear drain modulated power amplifiers." presented at the 2009 IEEE Topical Symposium on Power Amplifiers, Jan. 2009. 26, 118, 134, 165

[46] J. Hoversten and Z. Popovic, "Methods of alignment between signal paths in an envelope tracking transmitter." Intellectual property disclosure at the University of Colorado at Boulder, Boulder, CO, Apr. 2009. 26, 166

[47] J. Hoversten, M. Roberg, and Z. Popovic, "Linear and efficient envelope tracking PA for High-PAR waveforms." presented at the 2010 CNC/USNC/URSI Radio Science Meeting, Jun. 2010. 26, 179

[48] Z. Popovic and J. Hoversten, "Linear and efficient power amplifiers." four-part course presented at the University of Cantabria, Santander, Cantabria, Spain, Oct. 2009. hosted by Professor Jose Angel Garcia. 26, 97, 134

[49] I. Bahl, *Fundamentals of RF and Microwave Transistor Amplifiers*. Wiley-Interscience, June 2009. 27, 36, 38, 39, 74

[50] F. Schwierz and J. Liou, *Modern Microwave Transistors: Theory, Design, and Performance*. Wiley-Interscience, Dec. 2002. 28, 30, 32, 44, 80, 81

[51] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 36, pp. 1151–1159, Aug. 2002. 28

[52] N. Dye and H. Granberg, *Radio Frequency Transistors - Principals and Practical Applications*. Newnes, 2nd ed., 2001. 30

[53] D. Snider, "A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifier," *Electron Devices, IEEE Transactions on*, vol. 14, pp. 851–857, Dec 1967. 36

[54] J. Jeong, D. Kimball, M. Kwak, C. Hsia, P. Draxler, and P. Asbeck, "Modeling and design of RF amplifiers for envelope tracking WCDMA base-station applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, pp. 2148–2159, Sept. 2009. 39, 115

[55] S. D. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, "The class-E/F family of ZVS switching amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 6, pp. 1677–1690, 2003. 41

[56] P. Wright, A. Sheikh, C. Roff, P. Tasker, and J. Benedikt, "Highly efficient operation modes in GaN power transistors delivering upwards of 81% efficiency and 12W output power," in *Microwave Symposium Digest, 2008 IEEE MTT-S International*, pp. 1147–1150, 2008. 42

[57] V. Tyler, "A new high-efficiency high power amplifier," *Marconi Review*, vol. 21, pp. 96–109, Fall 1958. 42

[58] F. Raab, "Maximum efficiency and output of class-F power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 6, 2001. 42

[59] Y. Y. Woo, Y. Yang, and B. Kim, "Analysis and experiments for high-efficiency class-F and inverse class-F power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, pp. 1969 – 1974, May 2006. 42, 44

[60] D. Schmelzer and S. Long, "A GaN HEMT class F amplifier at 2 GHz with greater than 80% PAE," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 2130–2136, Oct. 2007. 42

[61] F. Raab, "Class-F power amplifiers with maximally flat waveforms," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 45, no. 11, pp. 2007–2012, 1997. 43

[62] F. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, pp. 1462 –1468, Aug 2001. 43, 46, 53, 71

[63] F. Lepine, A. Adahl, and H. Zirath, "L-band LDMOS power amplifiers based on an inverse class-F architecture," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 2007–2012, June 2005. 44

[64] C. Wei, P. DiCarlo, Y. Tkachenko, R. McMorrow, and D. Bartle, "Analysis and experimental waveform study on inverse class class-F mode of microwave power FETs," in *Microwave Symposium Digest., 2000 IEEE MTT-S International*, vol. 1, pp. 525–528, 2000. 44

[65] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2nd ed., 2001. 46, 51, 109

[66] N. O. Sokal and A. D. Sokal, "Class E - A new class of high-efficiency tuned single-ended switching power amplifiers," *Solid-State Circuits, IEEE Journal of*, vol. 10, pp. 168–176, June 1975. 48, 50

[67] T. Mader, E. W. Bryerton, M. Markovic, M. Forman, and Z. Popovic, "Switched-mode high-efficiency microwave power amplifiers in a free-space power-combiner array," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, pp. 1391–1398, Aug. 2002. 48, 53

[68] M. Albulet and R. Zulinski, "Effect of switch duty ratio on the performance of class E circuits," in *Circuits and Systems, 1997. Proceedings of the 40th Midwest Symposium on*, vol. 1, pp. 99–105, Aug 1997. 49

[69] F. Raab, "Idealized operation of the class E tuned power amplifier," *Circuits and Systems, IEEE Transactions on*, vol. 24, no. 12, pp. 725–735, 1977. 49

[70] S. Pajic, N. Wang, P. Watson, T. Quach, and Z. Popovic, "X-band two-stage high-efficiency switched-mode power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 2899–2907, Sept. 2005. 52

[71] P. Aflaki, H. Bae, R. Negra, and F. Ghannouchi, "Novel compact transmission-line output network topology for class-E power amplifiers," in *Microwave Conference, 2008. EuMC 2008. 38th European*, pp. 238–241, Oct. 2008. 53

[72] F. Raab and N. Sokal, "Transistor power losses in the class E tuned power amplifier," *Solid-State Circuits, IEEE Journal of*, vol. 13, pp. 912–914, Dec 1978. 53

[73] V.Camarchia, V. Teppati, S. Corbellini, and M. Pirola, "Microwave measurements part II non-linear measurements," *Instrumentation Measurement Magazine, IEEE*, vol. 10, pp. 34–39, June 2007. 55

[74] J. Milligan, S. Sheppard, W. Pribble, Y.-F. Wu, S. Muller, and J. Palmour, "SiC and GaN wide bandgap device technology overview," in *Radar Conference, 2007 IEEE*, pp. 960–964, apr 2007. 56, 78

[75] F. Microwaves, "Application note database." online: http://focus-microwaves.com/, Jan 2006. 57, 68

[76] J. Benedikt, R. Gaddi, P. Tasker, and M. Goss, "High-power time-domain measurement system with active harmonic load-pull for high-efficiency base-station amplifier design," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, pp. 2617 –2624, Dec 2000. 61

[77] C. Tsironis, A. Jurenas, and C. Liu, "Highly accurate harmonic tuners for load pull testing," in *Microwave Conference, 2001. APMC 2001. 2001 Asia-Pacific*, vol. 3, pp. 1311–1314, 2001. 61

[78] Focus Microwaves, "Error in power measurements as a function of tuner VSWR and tuner accuracy." online: http://focus-microwaves.com/template.php?unique=183, 01 2006. 62

[79] G. Engen and C. Hoer, "Thru-reflect-line: An improved technique for calibrating the dual six-port automatic network analyzer," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 27, pp. 987–993, Dec. 1979. 63

[80] Staff, "In-fixture microstrip device measurement using TRL* calibration," Application Note 8720-2, Agilent Technologies, June 2000. 63

[81] N. Misljenovic, "Private communication." Focus Microwaves, Sept 2009. 68, 69

[82] D. Pozar, *Microwave Engineering*. Wiley, 3rd ed., February 2004. 68

[83] N. Lopez, *High Efficiency Power Amplifiers for Linear Transmitters*. PhD thesis, Department of Electrical and Computer Engineering, University of Colorado at Boulder, Boulder, CO, 2008. 71, 78

[84] J. Walker, D. Myer, F. Raab, and C. Trask, *Classic Works in RF Engineering: Combiners, Couplers, Transformers, and Magnetic Materials*. Artech House Publishers, Jan 2006. 74

[85] J. Sevick, *Understanding, Building, and Using Baluns and UnUns*. CQ Communications, Inc., 2003. 74

[86] R. Negra, F. M. Ghannouchi, and W. Bachtold, "Study and design optimization of multiharmonic transmission-line load networks for class-E and class-F K-band MMIC power amplifiers," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, pp. 1390–1397, June 2007. 75

[87] J. Martinetti, A. Katz, and M. Franco, "A highly efficient UHF power amplifier using GaAs FETs for space applications," in *Microwave Symposium, 2007. IEEE/MTT-S International*, pp. 3 –6, june 2007. 78

[88] R. Trew, "Wide bandgap semiconductor transistors for microwave power amplifiers," *Microwave Magazine, IEEE*, vol. 1, no. 1, pp. 46–54, 2000. 80

[89] U. K. Mishra, S. Likun, T. E. Kazior, and Y. Wu, "GaN-based RF power devices and amplifiers," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 287–305, 2008. 81

[90] S. De Meyer, C. Charbonniaud, R. Quere, A. Campovecchio, R. Lossy, and J. Wurfl, "Mechanism of power density degradation due to trapping effects in AlGaN/GaN HEMTs," in *Microwave Symposium Digest, 2003 IEEE MTT-S International*, vol. 1, pp. 455–458, 2003. 81

[91] K. Gupta, R. Garg, I. Bahl, and P. Bhartia, *Microstrip lines and slotlines*. Artech House Publishers, 2nd ed., 1996. 83

[92] TriQuint Semiconductor, "TGF2023-10 Datasheet." online, accessed 2/15/10, Nov 2009. http://www.triquint.com/prodserv /more_info/proddisp.aspx?prod_id=TGF2023-10. 86

[93] Nitronex Corporation, "NPTB00050 Datasheet." online, accessed 2/15/10, May 2009. http://nitronex.com/pdfs/NDS-007%20Rev86

[94] Zentrix, "RF701 datasheet." online, accessed 2/15/10. http://www.zentrix.com/FileLibrary /index.cfm/RF701.pdf?action=GetFile&FileID=61. 87

[95] F. Raab, B. Sigmon, R. Myers, and R. Jackson, "L-band transmitter using Kahn EER technique," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 46, no. 12, pp. 2220–2225, 1998. 101, 109

[96] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal, "Power amplifiers and transmitters for RF and microwave," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, pp. 814 –826, Mar 2002. 102

[97] T. Haynes, "The power to talk," *Power Engineer*, vol. 21, no. 5, pp. 46–47, 2007. 102

[98] V. Yousefazadeh, *Digitally Controlled Power Converters for RF Power Amplifiers*. PhD thesis, University of Colorado at Boulder Department of Electrical and Computer Engineering, Boulder, CO, 2006. 110

[99] H. Nemati, C., Fager, U. Gustavsson, R. Jos, and H. Zirath, "Characterization of switched mode LDMOS and GaN power amplifiers for optimal use in polar transmitter architectures," in *2008 IEEE MTT-s Dig.*, pp. 1505–1508, June 2008. 118

[100] J. Vuolevi and T. Rahkonen, *Distortion in RF Power Amplifiers*. Artech House Publishers, Feb. 2003. 119, 125

[101] D. Wisel and P. Handel, "Implementation considerations on the use of Zhu's

general sampling theorem for characterization of power amplifiers," in *Instrumentation and Measurement Technology Conference Proceedings, 2007. IMTC 2007. IEEE*, pp. 1–4, may 2007. 144

[102] M. Schetzen, *The Volterra and Wiener Theories of Nonlinear Systems*. Krieger Publishing Company, revised ed., Apr. 2006. 154

[103] L. Ding, G. Zhou, D. Morgan, Z. Ma, J. Kenney, J. Kim, and C. Giardina, "A robust digital baseband predistorter constructed using memory polynomials," *Communications, IEEE Transactions on*, vol. 52, pp. 159–165, jan 2004. 155

[104] D. Morgan, Z. Ma, J. Kim, M. Zierdt, and J. Pastalan, "A generalized memory polynomial model for digital predistortion of RF power amplifiers," *Signal Processing, IEEE Transactions on*, vol. 54, pp. 3852–3860, Oct 2006. 155

[105] A. Zhu, P. Draxler, J. Yan, T. Brazil, D. Kimball, and P. Asbeck, "Open-loop digital predistorter for RF power amplifiers using dynamic deviation reduction-based Volterra series," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, pp. 1524–1534, July 2008. 155

[106] A. Zhu, P. Draxler, C. Hsia, T. Brazil, D. Kimball, and P. Asbeck, "Digital predistortion for envelope-tracking power amplifiers using decomposed piecewise Volterra series," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, pp. 2237–2247, Oct 2008. 156

[107] J. Choi, D. Kang, D. Kim, and B. Kim, "Optimized envelope tracking operation of Doherty power amplifier for high efficiency over an extended dynamic range," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 57, pp. 1508–1515, June 2009. 178

[108] H. Myung, J. Lim, and D. Goodman, "Single carrier FDMA for uplink wireless transmission," *Vehicular Technology Magazine, IEEE*, vol. 1, pp. 30 –38, sept 2006. 178