Independent Dynamic Gate Bias for a Two-Stage Amplifier for Amplitude and Phase Linearization

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***Abstract*—This work describes an analog linearization technique for two-stage power amplifiers using gate bias modulation. Independently driving the gates of the first and second stage with a signal dependent voltage allows for theoretically perfectly flat AM/AM, AM/PM while sacrificing average gain. Using a GaN 10 W MMIC driving and a custom built gate tracker, and a target NPR of 24 dB, dynamic gate tracking improves the average output power by 1.25 dB and raises the PAE more than 4 % points for a 5 MHz white noise signal.**

I. Introduction

Modern communication systems demand increased bandwidths for high peak to average power ratios (PAPR) signals. This poses an ongoing challenge for efficient but linear power amplifier concepts. One way to address the linearity issue is to use a dynamic gate bias, i.e. the gate voltage is a function of the RF amplitude of the signal [1]–[4].

This work is based on the method presented in [5] (Fig. 1), where the two gates of a two-stage power amplifier are used independently to linearize the amplitude-to-amplitude (AM/AM) and amplitude-to-phase modulation (AM/PM) simultaneously. Based on new measurement data, here we extend to a systematic way of creating gate tracking functions optimized to achieve the largest possible peak output power without distortion. In the second part of the paper, we present dynamic measurement results obtained using a custom-built gate tracker independently driving the gates of a GaN X-band MMIC [6] using a 5 MHz wide noise power ratio (NPR) test signal.

II. Static Characterization

The PA is first characterized using a vector network analyzer (VNA), operated in powersweep mode at a single frequency (9.8 GHz). An external test set and a laboratory power amplifier provide an input power of up to 22 dBm. For every power step, the VNA triggers two current meters which record the drain currents of the first and second stage of the PA. A conventional VNA power and S-parameter calibration allows to measure the complex gain and PAE in a single measurement sweep, covering −10 dBm to 22 dBm in 201 steps. Additionally, both gates are independently set to a DC voltage ranging between −3.05 V to −2.4 V before each power sweep.

Fig. 2 shows the resulting phase response of the PA at 9.8 GHz. For static design bias conditions the phase varies between −185° at low power, raises to −173° at $P_{\text{out}} = 37.6\,\text{dBm}$ and finally settles at −179° for the peak power of 40.7 dBm

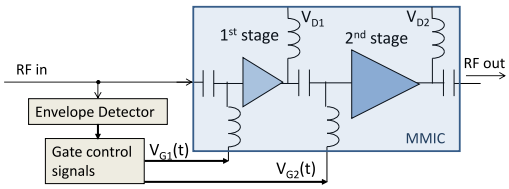

Fig. 1. Block diagram of two-stage PA with independent gate bias modulation.

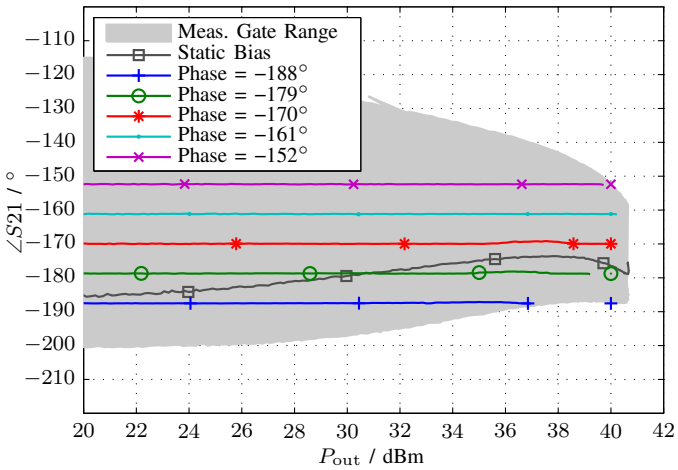

Fig. 2. Static transfer phase ($\angle S21$) characterization of a 2-stage GaN MMIC PA. The grey area shows the obtainable phase range when the gates are swept from $V_{G1} = -3$ V to −2.4 V and $V_{G2} = -3.05$ V to −2.45 V. The dark solid line corresponds to the conventional static bias, the colored lines show the resulting phase for 5 dynamic bias cases.

reachable in this bias configuration. Using different static gate voltages, very different transfer phases are obtained. The total range spanned by the different gate voltages is plotted as the grey area in Fig. 2.

A. Gate Bias Function Selection

Inspecting Fig. 2 it is evident that the two gate voltages allow for a large variation in phase, however the decreases as the power approaches the peak. To systematically investigate the best choice of a dynamic gate bias function, we select the largest (−152°) and smallest (−188°) obtainable phase at $P_{\text{out}} = 40\,\text{dBm}$, and equally divide the phase range to get five phase values, corresponding to the markers at 40 dBm in Fig. 2. Using the measured data set of the amplifier, interpolated to 400 gate voltage settings, a search is performed for all gate voltage combinations that will result in our selected

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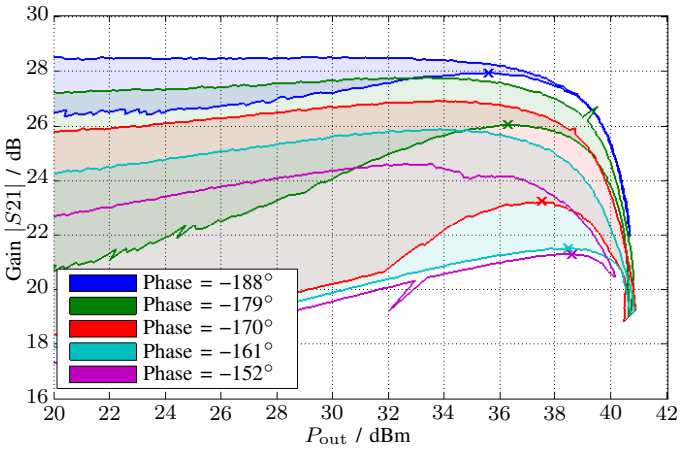


Fig. 3. Obtainable gain ranges for the 5 fixed phases selected in Fig. 2.

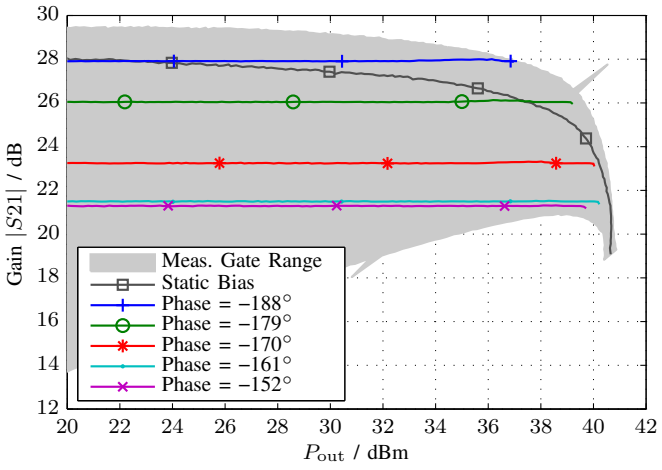


Fig. 4. Static gain ($|S21|$) characterization of a 2-stage GaN MMIC PA. The grey area shows the obtainable ain range when the gates are swept from $V_{\mathrm{G1}} = -3\,\mathrm{V}$ to $-2.4\,\mathrm{V}$ and $V_{\mathrm{G2}} = -3.05\,\mathrm{V}$ to $-2.45\,\mathrm{V}$. The dark solid line corresponds to the conventional static bias, the colored lines show the resulting gain for 5 dynamic bias cases.

five phases, allowing for a deviation of 1°. Those gate settings correspond to the gain areas shown in Fig. 3. The largest constant gain and phase range can be obtained if the target gain for each selected phase is set to the maximum gain of the lower gain boundary, as idicated by the "x" markers. We have now found a target gain for each target phase, which results in the highest possible peak output power and a perfectly flat gain and phase response. The resulting gain and phase performance is shown as the colored lines in Fig. 2 and Fig. 4, and the corresponding tracking functions for the first and second gate biases are plotted in Fig. 5.

B. Calculated Dynamic Performance and Discussion

By dividing the available phase range at $P_{\mathrm{out}} = 40\,\mathrm{dBm}$ we obtain five constant phase and constant gain trajectories with different characteristics. Using a 5 MHz wide NPR test signal constructed from 30 001 carriers with a PAPR of 10.6 dB and a 1 % notch, we estimate the performance for both the static biasing and dynamic biasing cases, using the interpolated static

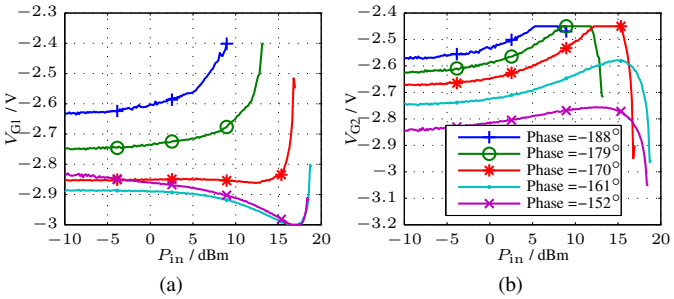


Fig. 5. Gate 1 (a) and gate 2 (b) tracking functions for the five investigated flat amplitude and phase trajectories.

data obtained with the VNA bench. This method of course does not take thermal, trapping or any other memory effects of the PA into account, but allows a qualitative comparison of the different bias cases. The results are summarized in Table I. For the static bias, we see the typical soft compression characteristics of GaN: Reducing the average input power by 9 dB causes the average output power to drop by 7.1 dB, but the peak power only reduces by 2.4 dB. The NPR and PAE are severely affected. Driving the amplifier hard will drop the peak gain below 20 dB (see Fig. 4) and thus move larger portions of the NPR signal towards more efficient operation.

The dynamic bias cases result in PAEs between 5.8 % and 15.5 %, when the input signal is scaled so that the peak hits the peak output of the theoretic perfectly flat amplitude and gain operation. The −188° and −179° bias cases show relatively low PAE because they correspond to the highest gain settings and provide a relatively low peak output power, especially the −188° case. It is evident from Fig. 4 that this case has a higher gain than the static bias even for low output powers of $P_{\mathrm{out}} = 24\,\mathrm{dBm}$, therefore systematically requiring higher bias currents. The other cases with lower gains show higher PAEs, also because they reach higher average output powers, and therefore higher efficiency regions. The NPR values given for the dynamic bias cases reflect numerical effects of the tracking function selection, and are given for completeness.

It is also interesting to note how the different gate tracking functions affect the bandwidth required for the gate tracker, which we define as the frequency range where the DC-free gate tracking spectrum is 30 dB below the peak or larger. Note the very large bandwidth required to track gate 1 for the −170° case, which can be explained by the almost step-like gate 1 tracking function as seen in Fig. 5a.

III. Dynamic Measurements

A dynamic measurement bench is used to validate analog linearization using dual dynamic gate bias. It consists of two synchronized arbitrary waveform generators (ARBs), a vector signal generator, a vector signal analyzer, power meters, DC supplies, and a custom made dual-gate driver designed around THS3202 current feedback op-amps. While one ARB generates the baseband, which is the same 5 MHz NPR signal used in Section II-B, the second ARB generates the tracking signals for the two gates that are amplified and level shifted by the custom dual-gate driver. A direct application of the

TABLE I
CALCULATED PERFORMANCE COMPARISON BASED ON STATIC MEASUREMENT DATA FOR A 5 MHZ NPR TEST SIGNAL

Mode	Gain	Peak Pow.	Avg. Pow.	PAE	NPR	Tracking BW G1	Tracking BW G2
Static Bias, no backoff	25.4 dB	40.7 dBm	36.4 dB	32.3 %	18.2 dB	–	–
Static Bias, 6 dB backoff	26.9 dB	39.8 dBm	31.9 dB	17.6 %	24.7 dB	–	–
Static Bias, 9 dB backoff	27.3 dB	38.3 dBm	29.3 dB	11.4 %	26.5 dB	–	–
Dyn. Bias, Phase = −188°	27.9 dB	37.0 dBm	26.4 dB	5.8 %	58.3 dB	8.3 MHz	11.0 MHz
Dyn. Bias, Phase = −179°	26.0 dB	39.2 dBm	28.7 dB	10.3 %	54.8 dB	9.3 MHz	8.0 MHz
Dyn. Bias, Phase = −170°	23.2 dB	40.0 dBm	29.6 dB	13.2 %	53.4 dB	69.8 MHz	8.0 MHz
Dyn. Bias, Phase = −161°	21.5 dB	40.2 dBm	29.8 dB	15.1 %	71.8 dB	7.1 MHz	9.0 MHz
Dyn. Bias, Phase = −152°	21.3 dB	39.7 dBm	29.3 dB	15.5 %	71.4 dB	11.5 MHz	13.3 MHz

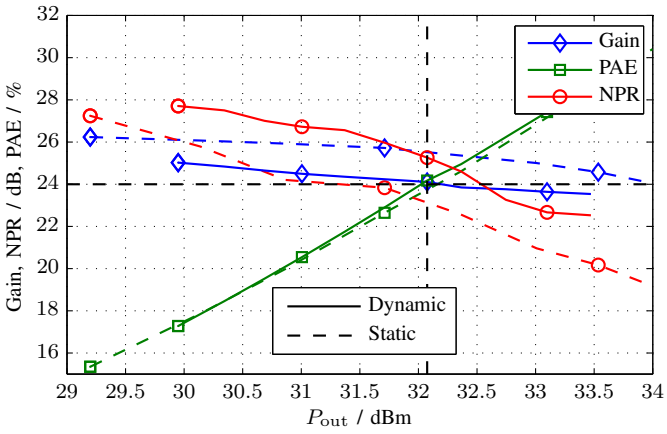
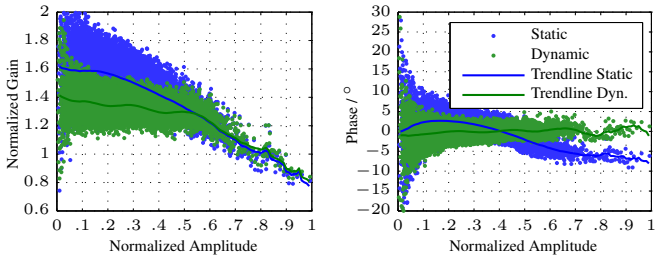


Fig. 6. Measured NPR, PAE and average Gain of 5 MHz test signal for dynamic gate bias optimized for 8 dBm input power and 24 dB of gain, as indicated by the dashed black lines.

tracking functions found from the static measurements did not prove to be fruitful, since the dynamic behavior of the amplifier diverges too much from the static measurements. However, using an optimization algorithm on the measured AM/AM and AM/PM data for different gain trajectories was successful. Fig. 6 shows results for a power sweep; the gate functions are optimized for a target gain of 24 dB and an average input power of 8 dBm, as indicated by the dashed black lines in the figure. At the design output power, the target gain is achieved but varies slightly with P_{out}, due to thermal and other memory effects. When compared to static bias, the NPR for this setting improves by 2.3 dB, the PAE slighly improves by 0.25 % points. Varying the drive level from the design setting degrades the NPR improvement, since the gate signals are not optimized for this average power level. AM/AM and AM/PM plots obtained for the design input power are shown in Fig. 7. For the given drive level, target gain, and allowed gate swing, the output amplitude could only be linearized up to some power, but the phase is linearized for the full amplitude range. Since the gate drive linearization is memoryless, the broadening of the AM/AM and AM/PM curves is not corrected.

IV. CONCLUSION

This work investigates linearization of a two stage amplifier using independent gate biases that are a function of the input



(a) (b)

Fig. 7. Measured AM/AM (a) and AM/PM (b) response: for static conventional gate biasing and dynamic bias.

signal amplitude. We first characterize the PA in a large-signal VNA setup for different gate bias settings and find five different dynamic gate tracking functions that ensure constant phases and constant gains. Choosing the setting with the smallest gain (21.3 dB) in calculations leads to perfectly linear operation with a PAE of 15.5 % when compared to 17.6 % PAE and 24.7 dB NPR for static biasing at 6 dB backoff, which provides similar peak output power. This principle is then applied in dynamic measurements with a high-PAPR, 5 MHz NPR test signal, where the NPR is improved by 2.3 dB with slightly improved PAE when compared to static biasing.

ACKNOWLEDGMENT

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