Supply Modulation of a Linear Doherty Power Amplifier

Dan Fishler[#1], Tommaso Cappello[#2], William Hallberg[*3], Taylor W. Barton[#4], Zoya Popovic[#5]
[#]University of Colorado Boulder, USA
[*]Chalmers University of Technology, Sweden
{[1]Dan.Fishler, [2]Tommaso.Cappello, [4]Taylor.W.Barton, [5]Zoya}@colorado.edu, [3]wilhal@chalmers.se

***Abstract*— This paper presents a study of supply modulation of a Doherty power amplifier (DPA) designed for linear operation. The symmetrical DPA is designed with Wolfspeed 6-W packaged devices for operation at 3.5 GHz with a peak output power of 42 dBm and a peak power-added efficiency (PAE) of 55%. Supply modulation is characterized statically when the main and auxiliary amplifier supply voltages are modulated separately, as well as simultaneously. The DPA is then characterized with 60-MHz LTE-like signals with 6 dB and 10 dB peak-to-average power ratios (PAPR). After digital pre-distortion using an iterative learning control algorithm, the composite PAE for a 10-dB PAPR signal is 38.7%, with mean-square error (NMSE) and ACLR values of 0.3% and -47 dBc.**

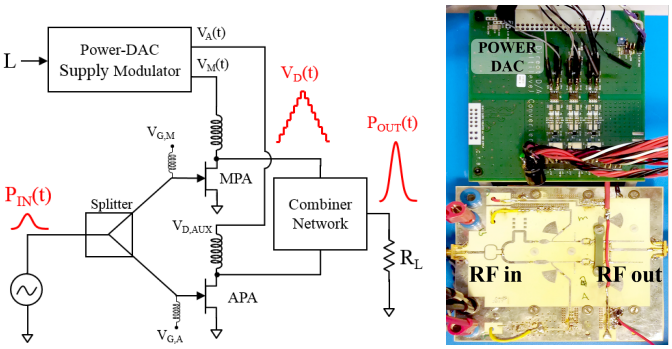
***Keywords*— Doherty amplifier, envelope tracking, power amplifiers, supply modulation, power-dac, predistortion**

I. Introduction

As peak to average power ratios (PAPRs) in commercial cellular systems trend higher, efficient power amplification increasingly requires a combination of multiple efficiency enhancement techniques in order to increase power amplifier (PA) efficiency at deep back-off. In particular, by adding supply modulation to existing architectures the range of efficient operation may be extended. The Doherty PA (DPA) is an interesting candidate architecture for supply modulation because its multiple bias and supply voltages enable a range of control parameters.

Previously, the benefits of combining the DPA architecture with supply and bias modulation techniques was explored in various combinations: varying the main PA (MPA) supply [1], [2], auxiliary PA (APA) supply [3], APA bias [4], and APA and MPA bias [5]. One goal of this work is a comprehensive study comparing the effects of each supply voltage modulation on the overall performance of the PA. Fig. 1(a) shows a generalized block diagram of the experimental approach, in which the supply of both the main and auxiliary PAs can be independently controlled.

With the goal of simultaneous efficiency and linearity for high-PAPR signals, the DPA has been designed for a linear response rather than for the characteristic DPA efficiency back-off curve. Then, efficiency is increased over a range of back-off values using discrete-level supply modulation. We show that simultaneously modulating the main and auxiliary supply voltages leads to significant efficiency improvement, while linearity is maintained through simple digital pre-distortion (DPD).



(a) (b)

Fig. 1. (a) Block diagram of the supply-modulated Doherty PA (SM-DPA). (b) Detail of the measured DPA with Power-DAC discrete modulator connected to both the drain of the auxiliary (APA) and main power amplifier (MPA).

II. Doherty PA Design

The symmetric linear Doherty PA was designed in two steps: starting with a design method resulting in linear CW performance and later fine-tuning design parameters for a desired 2-tone response. Wolfspeed CGH40006 devices and a Rogers RO4350 substrate are used. The initial CW design method follows the steps in [6], where biases, harmonic terminations, the ratio of the maximum power from the main and auxiliary transistors, and load impedances presented to the main and auxiliary transistors at maximum output power and at a desired backed-off power level are swept for a suitable trade-off between efficiency and linearity. The solution yields equations for a combiner network that is synthesized using the method in [7]. The resulting linear CW behavior of the DPA serves as an excellent starting point for fine tuning the design parameters for a linear 2-tone behavior. For this design, the performance goal was to maximize PAE with IMD3 not exceeding -30 dBc. The design parameters used for fine tuning are the biases, supply voltages, second harmonic terminations, and the components of the combiner network, where the latter effectively changes the impedances presented to the transistors. The layout of the DPA is shown in Fig. 1(b). The impedances presented to the transistors during the two steps are summarized in Table 1 for equal 26-V supplies (after full-wave electromagnetic simulations of the layout).

The DPA is connected to a discrete-level GaN-on-Si supply modulator similar to the one described in [8] and capable of delivering 8 discrete supply voltages ranging from 8 V to

Table 1. Impedances presented to the transistors in the linear DPA at the fundamental frequency.The 2nd harmonic extrinsic load termination is $-0.41 + j0.88\,\Omega$ in both branches.

	$Z_{MAIN,MAX}$	$Z_{MAIN,BO}$	$Z_{AUX,MAX}$	$Z_{AUX,BO}$
Ideal, extrinsic	14.8+j17.54	16.7+ j27.7	9.9 + j14.8	0.58 -j30.4
Post, EM, extrinsic	17.7 + j14.1	12.2 + j19.6	12.8 + j18.7	0.11 - j29.2
Post, EM, intrinsic	60.4 +j9.35	92.8 + j30.8	87 + j22.75	open

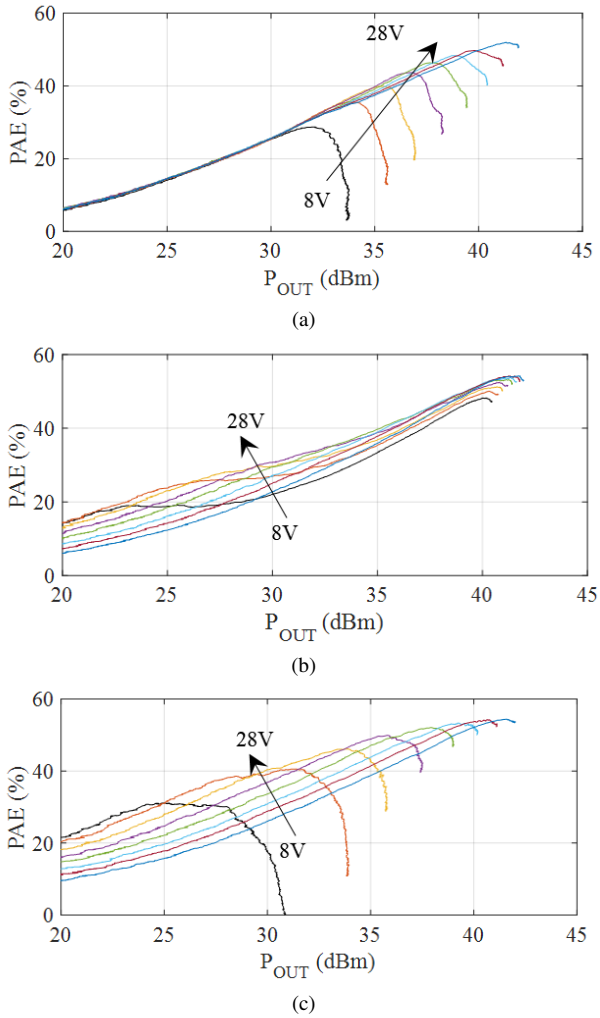


Fig. 2. Pulsed measurements of the PAE for different supply modulation approaches: (a) supply modulation of the APA with the MPA supply fixed at 28 V; (b) supply modulation of the MPA with the APA supply fixed at 28 V; and (c) supply modulation of the MPA and APA supplies together.The 8 levels are (8, 11.2, 13.6, 16.8, 19.2, 22.4, 24.8, 28) V.

28 V. The supply modulator is connected to the DPA with a short connection loop to minimize the parasitic inductance. A photograph of the connection is shown in Fig. 1(b).

III. Static Supply-Modulation Characterization

The DPA is characterized statically with a pulsed measurement system based on a 200-MHz National Instruments Vector Signal Transceiver (VST) following

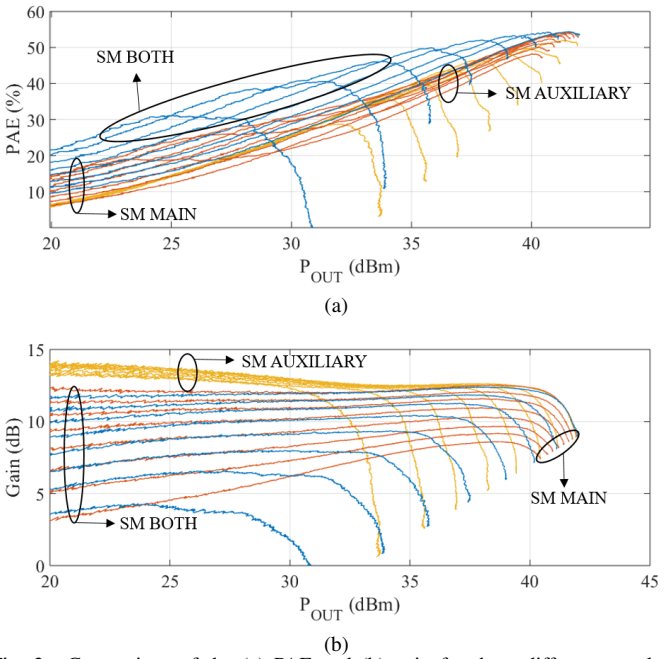


Fig. 3. Comparison of the (a) PAE and (b) gain for three different supply configurations: MPA supply (SM) modulated (red); APA modulated (yellow) and both modulated (blue).

the technique described in [9]. Stepped supply voltages from 8 V to 28 V are applied to MPA supply only, to the APA supply only, and to both supplies together (Fig. 2).

The measurements show that the DPA sees little efficiency improvement when only the APA supply is modulated. As expected, the APA supply modulation only affects the DPA performance over the upper 6-8 dB of output power, as also reported in [3], and in this range provides only a few percentage points efficiency improvement. When only the MPA supply is modulated (see Fig. 2(b)), there is significant efficiency improvement below approximately 10 dB back-off, at the expense of gain, and approximately 11 percentage point improvement in PAE. When both supplies are modulated simultaneously, a substantial improvement is seen, with a PAE>50% at 6-dB back-off compared to 41% for fixed supplies. We note that none of the PAE curves have the classic DPA characteristic; this is due to the gate biasing and design choices that prioritize linear performance over efficiency.

The measured PAE and gain of all three modes are shown in Fig. 3. The efficiency enhancement observed when the supplies are modulated together comes at the expense of gain variation. Nonetheless, it is possible to select a flat gain trajectory if the lowest three voltage levels are omitted, without sacrificing efficiency in the 6-8 dB back-off region of interest.

In Fig. 4, PAE for the simultaneous supply modulation case is compared to that when the PA is biased in a more efficient mode. Note that the supply modulation performance curve shows the peak PAE curves only, based on the measurements in Fig. 2(c). The APA bias is adjusted to deep class-C to provide improved efficiency and a more conventional efficiency back-off curve. Although the comparison is not

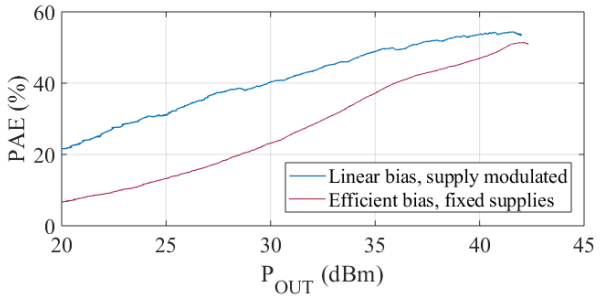


Fig. 4. PAE comparison between efficient-mode bias $V_{G,M} = -2.6\,\text{V}$, $V_{G,A} = -4.5\,\text{V}$ with simultaneous supply modulation of the MPA and APA, and linear-mode bias $V_{G,M} = -2.6\,\text{V}$, $V_{G,A} = -3.7\,\text{V}$ with fixed supplies.

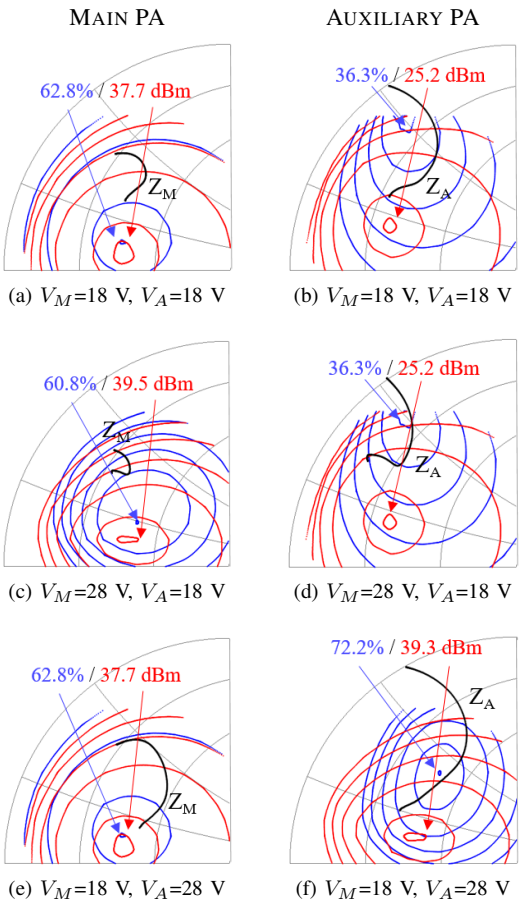
ideal, as the PA was not designed for this bias condition, the linear bias with supply modulation does provide improved efficiency over a wide range of output power levels.

IV. Simulations of Load Modulation

The measured characterization clearly indicates that modulation of both supplies together provides the greatest efficiency improvement for this DPA. To validate this conclusion, the load impedance trajectories at the outputs of the main and auxiliary PA transistor extrinsic drains are simulated. Each pair of plots in Fig. 5 shows the loading trajectory under different supply combinations for the MPA (Fig. 5(a), (c), and (e)) and APA devices (Fig. 5(b), (d), and (f)). For example, in Fig. 5(a) and (b), the MPA and APA load trajectories are shown in black as output power is swept and when both supplies are set at 18 V. Also shown are the simulated load pull contours at the extrinsic drains of the transistors in the MPA and APA under the same supply conditions. Fig. 5(c)–(f) compare load trajectories to load pull contours for supply modulation of only the MPA or only the APA. For each pair of simulations, an appropriate input power is selected based on the expected output power for that supply modulation configuration. Comparing the load trajectories to the load pull contours, it can be seen that asymmetric supply modulation tends to degrade the load trajectory design in the PA. This conclusion supports that of the measured characterization.

V. SM-DPA with Modulated Signals

The DPA performance is evaluated with 6-dB and 10-dB PAPR LTE-like signals with 60 MHz bandwidth. For each signal we compare fixed-bias and supply modulated operation. The results of these measurements are shown in the time and frequency domains in Figs. 6 and 7, respectively. Here we consider the composite PAE (CPAE) which includes the Power-DAC supply modulator efficiency. For the fixed bias case, the CPAE corresponds to the average PAE of the DPA. The resulting efficiencies and power levels of the SM-DPA are summarized in Table 2. When supply modulation is employed, CPAE improves 9 points for the 6 dB PAPR signal and 15 percentage points for the 10 dB PAPR case.



(a) V_M=18 V, V_A=18 V (b) V_M=18 V, V_A=18 V

(c) V_M=28 V, V_A=18 V (d) V_M=28 V, V_A=18 V

(e) V_M=18 V, V_A=28 V (f) V_M=18 V, V_A=28 V

Fig. 5. Simulated load modulation Z_L at the extrinsic drains of the transistors in the main (left column) and auxiliary (right column) PAs under different combinations of drain supply conditions. The figure also shows simulated load pull contours of PAE (blue) and P_{out} (red).

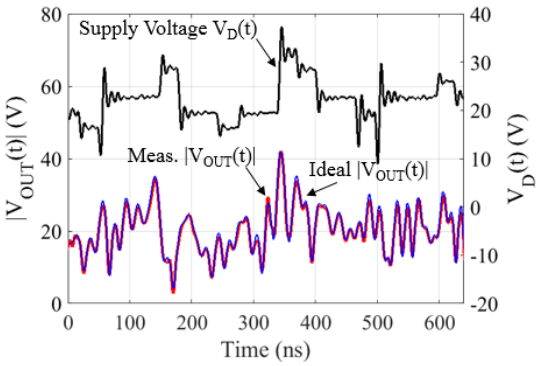
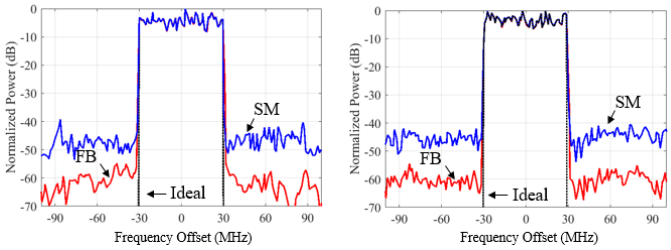


Fig. 6. Measured time-domain waveforms of the ET-DPA including dynamic supply voltage (black) with digital predistortion when a 6-dB PAPR, 60-MHz bandwidth, LTE-like signal is amplified. The output voltage envelope of the DPA (red) is compared to the ideal envelope (blue) showing the effectiveness of the ILC DPD.

Table 2. Modulated performance for 6-dB and 10-dB PAPR, 60-MHz bandwidth LTE-like signals. CPAE includes the Power-DAC supply modulator efficiency.

Signal	PAPR	Drain Control	NMSE	ACLR	$P_{DC,TOT}$	$P_{IN,AVG}$	$P_{OUT,AVG}$	$CPAE_{AVG}$
LTE-like 60-MHz	6 dB	Fixed Bias	0.1%	-52.1 dB	11.3 W	0.24 W	4.10 W	34.2%
LTE-like 60-MHz	6 dB	Supply Mod.	0.2%	-42.3 dB	8.52 W	0.32 W	3.71 W	43.2%
LTE-like 60-MHz	10 dB	Fixed Bias	0.3%	-57.1 dB	8.24 W	0.10 W	2.04 W	23.6%
LTE-like 60-MHz	10 dB	Supply Mod.	0.3%	-47.0 dB	3.90 W	0.20 W	1.71 W	38.7%



(a) (b)

Fig. 7. Output spectra of the SM-DPA architecture with supply modulation and fixed bias operation. Spectrum of the 6-dB (a) and 10-dB (b) PAPR signals.

Table 3. DPA comparison with different gate and supply control strategies.

Ref.	DPA Control Strategy	Freq. (GHz)	P_{OUT} (dBm)	PAE (%) (0 - 6-dB BO)
[1]	SM MAIN	2.14	43	51 - 30*
[2]	SM MAIN	1.88*	24	39 - 23*
[5]	GM MAIN + AUX	2.14	34	41 - 26*
[3]	SM AUX	2.40	44*	76*+ - 63*+
[4]	GM AUX	2.14	44	47* - 30*
This work	SM MAIN + AUX	3.50	42	55 - 49

* value read from graph; + drain efficiency.

An iterative learning control (ILC) algorithm [10] is implemented to pre-distort the input signal of the SM-DPA and recover linearity. In this approach, the non-linear behavior with memory of the DPA under supply-modulation is compensated by comparing the ideal signal with the actual output of the PA on a sample-by-sample basis. A gain-based learning approach [10] is employed to correct the output nonlinearities of the SM-DPA. The ILC algorithm is initialized with a predistorted sequence obtained with a pre-pulsing characterization of the SM-DPA as discussed in [9]. With this initialization, the algorithm converges very rapidly and with only two iterations it achieves the desired linearity (NMSE and ACLR, Table 2).

It is worth observing that this approach is also effective in compensating the distortion during the commutations of the discrete voltage levels as can be appreciated from Fig. 6. Severe ringing is measured because of the voltage probe, whereas no discontinuities or ringing are noticeable in the output linearized envelope. Good linearity performance can also be observed in the spectra (Fig. 7), as reported by the ACLR metric in Table 2. Operation at a greater signal bandwidth is limited due the non-optimized interconnect between the DPA and the Power-DAC PCB (see Fig. 1(b)). The impedance of the interconnect introduces self-modulation effects on the drain supply line at increasing bandwidths that cannot be recovered with the ILC predistortion.

VI. Conclusion

The DPA presented in this work is designed for linearity, while efficiency enhancement is provided through discrete-level supply modulation. A comparison to prior works investigating gate and supply control strategies of DPAs is shown in Table 3. After pulsed characterization at multiple supply voltage combinations, we conclude that for this PA the best performance is achieved when both supply voltages are modulated simultaneously. Dynamic performance of the presented SM-DPA architecture is evaluated with 60-MHz LTE-like signals with 6 and 10 dB PAPR. When digital pre-distortion is employed, the SM-DPA architecture presents efficiency improvements between 9 and 15 percentage points with NMSE below 1% and ACLR under -42 dBc.

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