Optimal Definition of Class F for Realistic Transistor Models

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***Abstract*— An optimal three-harmonic definition of class F at the intrinsic level is presented for realistic transistor models exhibiting IV characteristics with a nonzero knee voltage. This updated class-F definition is needed for use with the recently reported *embedding device model*, which predicts in a single harmonic balance simulation the voltage and current waveforms required at the package reference planes to sustain an intrinsic mode of operation. Optimal class-F operation is obtained by setting to infinite the third-harmonic output impedance of the transistor IV characteristics instead of using an open load for the third-harmonic termination. This is achieved by fine tuning the class-F quasi-rectangular drain voltage waveform. The required third-harmonic component of the drain voltage in the optimal class F is then found to be generated by the lossless inductive termination of the third-harmonic component of the drain displacement current arising from the nonlinear drain-to-source capacitance. The proposed class-F definition is verified for a gallium nitride (GaN) high electron mobility transistor using third-harmonic load–pull simulations with a realistic GaN transistor model. The optimal third-harmonic load termination predicted using the class-F definition is found to be in full agreement with the one obtained from the drain efficiency contour plots. A close agreement is also obtained for the predicted and measured optimal third-harmonic load termination, bringing experimental support for the proposed class-F definition.**

***Index Terms*— Amplifier classes, class F, embedding device model, load pull, power amplifiers (PAs).**

I. Introduction

DESIGNERS of microwave power amplifiers (PAs) have become interested in accessing the current and voltage waveforms at the transistor current-source reference planes to monitor the intrinsic mode of operation of the transistor(s) in their PA designs [1]–[3]. Indeed by optimizing the intrinsic mode of operation of the transistors, a higher power efficiency can be obtained at the device terminal levels.

A novel approach for designing microwave PAs based on the characterization of the intrinsic electron-device load line using nonlinear embedding was proposed and demonstrated in [4]. With the *embedding device model* introduced in [5], it became possible for PA designers to directly control, within the confine of the simulation environment, the intrinsic operation mode of the device at the current-source reference planes while the required multiharmonic load and source impedance terminations at the package reference planes (device terminals) were simultaneously determined [6], [7]. Time-consuming source- and load–pull simulations are no longer needed since the optimal multiharmonic source and load impedance terminations are obtained in a single simulation. Note that the embedding device model has the further advantage of being less prone to convergence issues compared with the device model. The design of amplifiers of various classes and architectures such as Doherty, Chireix, or broadband class-J PAs designed using an *embedding device model* has been demonstrated in [8]– [10].

Within the various modes of operation, class F remains of great interest, as among other things, it permits the realization of Doherty and Chireix PAs that exhibit a high efficiency at both peak and backoff. Since its initial proposal in the late 1910s [11], [12], and its detailed description in [13], class F (named as such by Raab [14]) has been the object of many theoretical investigations [15]–[20], practical implementations, and experimental investigations [21]–[23] to quote a few recent examples. The initial class-F theoretical investigations [15]–[17] relied on a zero-knee voltage model for the transistor and established the theoretical performance for an ideal device, while more realistic IV models were used in [18] and [20]. The importance of clipping was highlighted using load–pull measurements in a recent study of continuous class-F PAs [23]. Finally, it is to be noted that it was proposed in [20] that the second harmonic could be optimized in class-F PAs with the help of the nonlinear drain capacitance.

Given that the design of class-F PAs can now be greatly facilitated with the use of the *embedding device model*, it is beneficial to revisit the class-F definition for ideal devices in order to introduce an optimized version for the case of realistic IV characteristics. In a classic paper on class F [17], it is stated that "*class F is probably the oldest technique for improving the efficiency of an RF PA, but is perhaps also the least well understood.*" Cripps [24] refers to the "*great class-F puzzle*." In this section, we shall elaborate on the motivation for these comments.

The required waveforms for class-F operation are well established for the ideal FET device that features a constant transductance with an abrupt threshold and zero knee voltage ($V_{ON} = 0$) [17]. Ideally, the class-F waveforms

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consist of a rectangular drain voltage waveform (with $\min[v_{\rm DS}] = V_{\rm ON}$) and an ideal half-rectified drain current sinewave such that the current–voltage product remains null at all times. In the case of vanishing on-voltage, this yields theoretically 100% efficiency. In practice, only three harmonics (higher harmonics shorted) are usually considered. For an ideal device with zero knee voltage and $V_{\rm DS,1}$ approaching $V_{\rm DD}$, this yields a maximum theoretical efficiency of 90.7% for three harmonics [24].

In the case of an ideal FET with abrupt thresholds and constant transconductance, the ideal half-rectified current sinewave yields only even harmonics (see [17]), and the power dissipation for the odd harmonics is zero. However, when the class-F drain voltage waveforms are applied to realistic FET devices with nonzero on-voltage and a nonlinear subthreshold region, odd-harmonic drain-current components are generated and the transistor current source can either dissipate (active load) or generate power (passive load) at each of the odd harmonics. In this paper, we will demonstrate that to sustain class-F operation with zero power dissipation at the third harmonic, we can simply tune the class-F waveform so that the power generation by the transistor at the third harmonic is null.

Let us now address the issue of the impedance loading required to sustain the class-F drain voltage waveform. The well-known loading conditions for class-F operation at the current-source level are the following for each harmonic n [13], [16]:

$$Z_{L,n} = \begin{cases} \dfrac{4}{\pi}\dfrac{V_{D,\max} - V_{\rm ON}}{I_{D,\max}}, & \text{for } n = 1 \\ 0, & \text{for even } n > 0 \\ \infty, & \text{for odd } n > 1\ . \end{cases} \tag{1}$$

The short termination at the even harmonics is required so that no even harmonic voltages appear between the drain and source terminals. The open load at the odd harmonics is justified since in the ideal linear device, there are no odd-harmonic drain-current components supported by the ideal half-rectified current sinewave even though odd harmonic voltages are applied. The question arises in both ideal and real devices on how the open load terminations at the odd harmonics can support the formation of the required odd-harmonic voltages. Indeed, as PA designers commonly experience, the loading conditions defined in (1) do not usually provide the desired drain class-F waveform for real transistors.

Let us discuss in more detail the case of devices with realistic IV characteristics featuring a smooth knee region (nonzero on-voltage). As is explained in [24], "*the action of the device knee region is to clip the peaks of the current waves, thus generating substantial amount of third harmonics.*" It is then suggested that the generated third-harmonic drain current can be used to sustain the third-harmonic drain voltage using third-harmonic resistive loading. Examples are given in [24], and the following resistive loading equation is provided in [18] and [25]:

$$\frac{Z_{L,3}^{(IV)}}{Z_{L,1}^{(IV)}} = \frac{R_3}{R_1} = -\frac{1}{6}\frac{I_{D,1}}{I_{D,3}}.$$

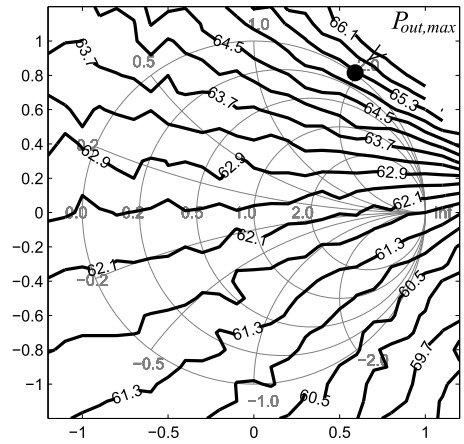

Fig. 1. Drain efficiency contour plot (in %) from an on-wafer third-harmonic load pull on a GaN HEMT. The optimal third-harmonic load W (black circle) yielding maximum drain efficiency is located on the Smith chart edge and is thus lossless (from [26]).

These designs have the advantage of presenting a practical scenario for class-F implementation. The power dissipated by the resistive termination R_3 is usually very small compared with the dc power. However, it is well known by practioners of multiharmonic load pull and source pull that the highest power efficiency is attained for lossless passive loads as shown in Fig. 1. It is not surprising that lossless harmonic terminations are desirable since we do not want to transfer any of the dc supply power into RF power dissipated in the harmonic terminations. Thus, an alternative mechanism for generating the third-harmonic drain voltage is required. We will demonstrate in Section II that such a lossless mechanism is provided by the lossless third-harmonic termination of the drain-current third-harmonic component generated by the *nonlinear* drain-to-source capacitance.

At this point, it should be noted that the nonlinear embedding performed by the *embedding device model* [5] provides us with the means to automatically implement the normal and optimal class-F waveform definition. Indeed, the *embedding device model* provides the PA designer the exact multiharmonic source and load impedance terminations required to sustain the class-F operation established at the current-source reference planes.

Before proceeding with the outlined plan, it should be noted that in practical amplifiers, it will be difficult to fully achieve the ideal class-F operation. The reason is that when the *embedding device model* is used to exactly implement the desired intrinsic class-F mode, harmonic loads that are slightly active are usually required. In other words, the harmonic load reflection coefficients are usually located slightly outside the Smith chart. Thus, class F cannot be exactly implemented in practical PAs using passive loads; rather it requires active loads (small harmonic power injection) to be observed in order to compensate for the lossy device parasitics. This limitation can be easily addressed in practice by renormalizing the harmonics reflection coefficients to the edge of the Smith chart in order to obtain the closest class F like solution available. Embedding may also require the injection of small harmonics components at the gate terminals, which is not

always practical. As expected, these realizability issues lead to a reduction of a few percent in the expected efficiency. But as we shall verify in both simulation and measurements, these effects are relatively small and the embedding model greatly accelerates the design.

This paper will present the theory and simulation verifications of the new optimal class-F definition for realistic transistor models in Section II. The optimal class-F design targeted for the measurement verification will be introduced in Section III, and the measurement testbed used to experimentally verify it will be described in Section IV. Experimental results will then be presented in Section V and compared with simulation results. Finally, in Section VI, the key results will be discussed and summarized.

II. Class-F Theory, Limitations, and Extension

In Section I, we reviewed the traditional definitions of class F based on: 1) the waveform and 2) the harmonic termination definitions. We argued that each had their own advantages and weaknesses. For the waveform class-F definition, voltage sources at the fundamental and harmonic frequencies are connected in series between the drain and source terminals to apply the ideal class-F waveforms. They do not, however, automatically enforce the optimal requirement for zero odd-harmonic drain-current components, since in realistic devices, the drain current is not a perfect half-rectified sinewave. The resulting odd-harmonic drain-current components flowing in the transistor current source (IV) are then associated with unwanted generation or dissipation (external injection) of harmonic power by the transistor.

In the impedance-termination class-F definition, an open load is used for the odd harmonics, and we cannot guaranty that the desired third-harmonic voltages ($V_{DS,n}$) will be sustained as prescribed by the class-F waveform definition. We thus need a combination of both conditions, which is impossible to satisfy using just the load network side, since we cannot simultaneously rely on the drain waveform and load impedance terminations to define passively or actively the class-F loading. As we shall see below, one possible resolution of these conflicting requirements is obtained by initially relying on voltage sources (at the drain terminals) to set the desired class-F drain voltage waveform while independently suppressing the third harmonic of the drain current at the transistor level by tuning the drain voltage waveform.

In the case where only three harmonics (higher harmonics shorted) are considered, the class-F waveforms are given by

$$\begin{aligned} v_{GS} &= V_{GS} - V_{GS,1}\cos(\omega t) \\ v_{DS} &= V_{DD} + V_{DS,1}\cos(\omega t) + V_{DS,3}\cos(3\omega t) \end{aligned} \tag{2}$$

with V_{GS} the dc gate bias, $V_{GS,1}$ the fundamental gate voltage (taken as positive real), V_{DD} the dc drain bias, $V_{DS,1}$ the fundamental drain voltage (taken as positive real), and $V_{DS,3}$ the third-harmonic drain voltage (taken as real).

The gate V_{GS} and drain V_{DD} dc biases and the gate $V_{GS,1}$ and drain $V_{GS,1}$ fundamental voltages define the large signal operating point (LSOP) for the transistor, while $V_{DS,3}$ the third-harmonic drain voltage is the perturbation defining the class-F operation.

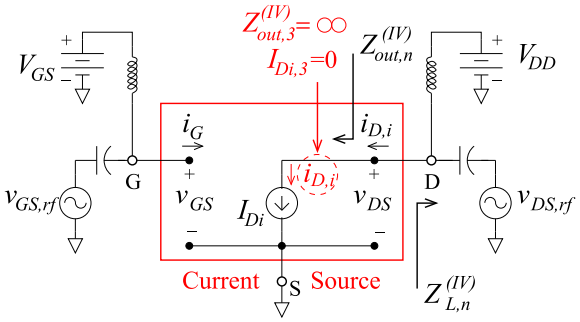

Fig. 2. Load $Z^{(\text{int})}_{L,n}$ and output $Z^{(IV)}_{\text{out},n}$ impedances at the current-source reference planes. Optimal class F requires $Z^{(IV)}_{\text{out},n} = \infty$ for n odd.

It has been determined for the ideal device (no knee voltage) that the optimal third-harmonic drain voltage $V_{DS,3} = -\alpha_3\ V_{DS,1}$ giving maximum efficiency [24] and maximum voltage gain [25] requires a third-to-first harmonic ratio of $\alpha_3 = 1/6$. This result motivated the use of $\alpha_3 = 1/6$ for our experimental verification and the determination of its associated LSOP. However, as we shall verify later on, different optimal α_3 may be required for different LSOPs.

The drain efficiency for a transistor operating in class F is defined as: $\eta = P_{RF,1}/P_{dc}$ with $P_{dc} = V_{DD}I_D$ and $P_{RF,1} = \text{Re}[V_{DS,1}I^*_{DS,1}]/2$ the RF output power generated by the transistor and delivered to the load at the fundamental frequency. The output RF power $P_{RF,1}$ generated by the transistor can be rewritten as

$$P_{RF,1} = P_{dc} - P_{diss} - P_{RF,3} \tag{3}$$

with $P_{RF,3} = \text{Re}[V_{DS,3}I^*_{DS,3}]/2$ the output RF power generated by the transistor at the third harmonic and P_{diss} the power dissipated in the transistor defined as

$$P_{diss} = \frac{1}{T}\int_0^T v_{DS}(t)i_D(t)dt. \tag{4}$$

It is assumed in (3) that all the even harmonics are shorted and the odd harmonics of order larger than three have a negligible power contribution. It results that the drain efficiency can be written as

$$\eta = 1 - \frac{P_{diss}}{P_{dc}} - \frac{P_{RF,3}}{P_{dc}}. \tag{5}$$

To maximize η, the class-F waveform should be selected to minimize both the power ratios P_{diss}/P_{dc} and $P_{RF,3}/P_{dc}$ while delivering sufficient output RF power $P_{RF,1}$. The fractional dissipated power P_{diss}/P_{dc} is minimized when the transistor class-F voltage v_{DS} and current i_D waveforms in (4) approach orthogonality. The fractional third-harmonic output power $P_{RF,3}/P_{dc}$ is minimized by setting $I_{DS,3} = 0$ in $P_{RF,3} = \text{Re}[V_{DS,3}I^*_{DS,3}]/2$. The latter requirement can be achieved by fine tuning either the bias V_{DD}, the fundamental amplitude $V_{DS,1}$, or the third-harmonic amplitude $V_{DS,3}$ of the class-F drain voltage waveform applied to achieve infinite third-harmonic output impedance $Z^{(IV)}_{\text{out},3} = \infty$ as shown in Fig. 2.

As an example, let us consider the gallium nitride (GaN) high electron mobility transistor (HEMT) Angelov model [27]

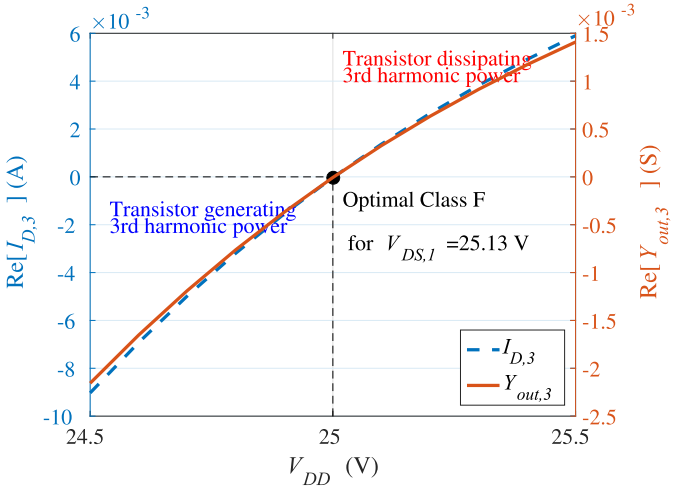

Fig. 3. Variation of $I_{D,3}$ and Re[$Y_{\text{out},3}$] versus the drain supply voltage V_{DD} for a GaN HEMT excited by a fundamental drain voltage of $V_{\text{DS},1} = 25.13$ V.

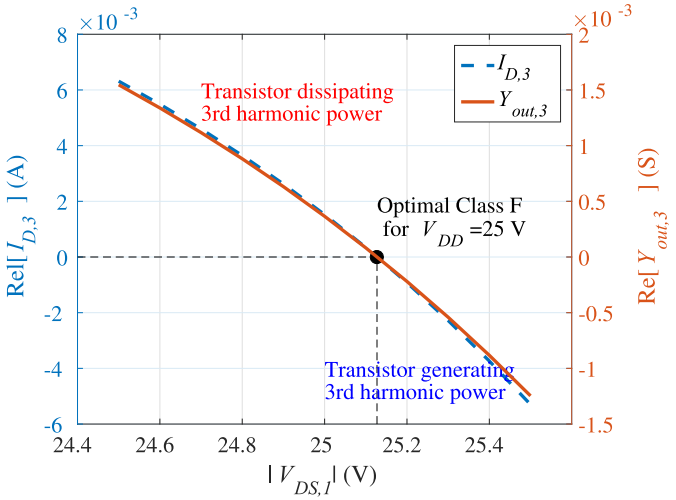

Fig. 4. Variation of $I_{D,3}$ and Re[$Y_{\text{out},3}$] versus the fundamental drain voltage $|V_{\text{DS},1}|$ for a GaN HEMT biased with a drain supply voltage of $V_{\text{DD}} = 25$ V.

extracted for the CREE CGH27015F transistor [5]. The device is biased with $V_{\text{DD}} = 25$ V to generate about 10 W output power. In Figs. 3 and 4, the pure-real third-harmonic component $I_{D,3}$ of the drain current and the pure-real third-harmonic output admittance $Y_{\text{out},3}^{(IV)} = 1/Z_{\text{out},3}^{(IV)}$ are plotted as a function of the drain dc bias V_{DD} and the pure-real fundamental RF component $V_{\text{DS},1}$ of the applied drain-to-source voltage, respectively. As can be seen in Figs. 3 and 4, respectively, as the dc drain voltage V_{DD} decreases or the fundamental drain voltage $V_{\text{DS},1}$ increases, the third-harmonic drain current $I_{D,3}$ and $Y_{\text{out},3}^{(IV)}$ switches from positive to negative. This is due to the fact that when the minima values of the drain voltage enter the knee region of the IV, the transistor usually switches from third-harmonic power dissipation to third-harmonic power generation. It is this feature that makes it possible to support class F without using resistive harmonic loads. Indeed, at the transition between these two modes of operation, the third-harmonic component of the drain current reverses sign and thus vanishes, and no third-harmonic power dissipation is taking place in either the transistor or the

TABLE I

SIMULATED EFFICIENCIES AS A FUNCTION OF α_3 FOR $V_{\text{DD}} = 25$ V AND $V_{\text{DS},1} = 25.13$ V

α_3	P_{DC} (W)	$\frac{P_{RF,3}}{P_{DC}}$ (%)	$\frac{P_{diss}}{P_{DC}}$ (%)	η (%)	$\eta^{(P)}$ (%)	$\lvert\Gamma_{L,3}\rvert$
0.13666	13.74	0.24	22.33	77.43	74.09	0.56
0.16666	13.94	0.00	22.17	77.83	74.44	1.00
0.26666	14.01	-0.24	22.14	78.10	74.67	1.33

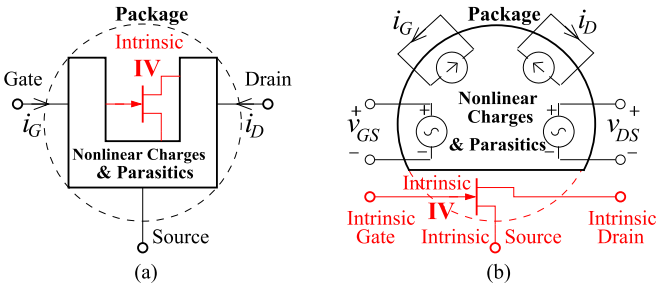

Fig. 5. Conventional (a) FET model and (b) embedding device model.

external load. Then there is no need to apply an open output load at the third harmonic as specified in the conventional class-F harmonic impedance-termination definition, since the third harmonic current $I_{D,3}$ is already zero. Thus, instead of requiring an open load for the third harmonic load $Z_{L,3}^{(\text{int})}$, it is the third-harmonic output impedance $Z_{\text{out},3}^{(IV)}$ of the transistor that must be set to infinite.

In the above examples, α_3 equal to 1/6 (optimal value for the ideal device) was used and the LSOP was tuned via V_{DD} or $V_{\text{DS},1}$ to achieve $Z_{\text{out},3}^{(IV)} = \infty$. Alternately given an optimal LSOP, we can tune the perturbative third-harmonic voltage $V_{\text{DS},3}$ or equivalently α_3 to achieve $Z_{\text{out},3}^{(IV)} = \infty$. As is demonstrated in Table I for the previous LSOP example with $V_{\text{DD}} = 25$ V and $V_{\text{DD}} = 25.13$ V, the fractional dissipated power $P_{\text{diss}}/P_{\text{dc}}$ switches for positive to negative when α_3 becomes larger than $1/6 \simeq 0.16666$ and $|\Gamma_{L,3}|$ becomes larger than one. The efficiencies η and $\eta^{(P)}$ at the current-source and package reference planes, respectively, are both seen to increase as α_3 increases.

The drain voltage waveforms or drain loads that must be applied at the package reference planes to sustain the required third harmonic drain voltage $V_{D,3}$ at the intrinsic terminals can then be determined using the *embedding device model*. Two equivalent approaches are possible. The first approach relies simply on applying the desired class-F waveform of (2) while the second approach examines the physical process sustaining the class-F waveform by determining the required third-harmonic impedance terminations at the intrinsic reference planes. Both methods are equivalent and yield the same results but require different embedding device models as we shall see. The first method is straightforward given we have already determined the optimal drain voltage (dc, fundamental, and third harmonic) sustaining the new optimized class F intrinsically. The conventional embedding device model shown in Fig. 5 will then determine the required multiharmonic impedance terminations at the package or connector levels to achieve this optimized intrinsic class-F mode. The second approach, to be described next, has the advantage of revealing

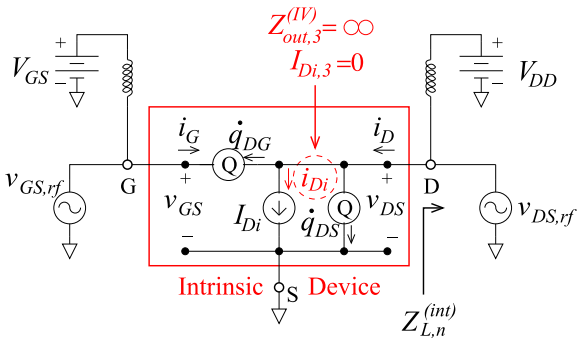

Fig. 6. Intrinsic device model with optimized class-F conditions.

the physical process required for class F to be self-sustained with a lossless passive third-harmonic impedance termination at the intrinsic reference planes.

As is shown in (2), the fundamental frequency component $V_{\mathrm{GS},1}$ of the gate-to-source voltage v_{GS} is in opposition of phase (180° phase shift) with the fundamental frequency component $V_{\mathrm{DS},1}$, and in phase (0° phase shift) with the third-harmonic component $V_{\mathrm{DS},3} = -\alpha_3\ V_{\mathrm{DS},1}$ of the drain-to-source voltage v_{DS}. This explains why the generation of the third-harmonic drain voltage $V_{\mathrm{DS},3}$ was naturally hypothesized to be generated by a positive load resistor $Z^{(\mathrm{int})}_{L,3} = R_3$ when driving the drain voltage such that its minima be in the knee region. In the derivation to follow, we shall demonstrate that the third-harmonic drain voltage can be alternatively sustained by terminating with a lossless load, the third-harmonic displacement current originating from the nonlinear gate-to-drain capacitance.

To describe the mechanism where class F is self-sustained with a lossless third-harmonic termination, let us consider the intrinsic device model in Fig. 6 where the drain-to-source q_{DS} and drain-to-gate q_{DG} nonlinear charges are considered together with the intrinsic IV I_{Di}. Note that for simplicity, the charges q_{DS} and q_{DG} considered are quasi-static, and no charging time constant or charging resistances are considered. The total displacement drain current sustained by these charges is then given by

$$\begin{aligned} i_{D,\mathrm{displ}} &= \frac{dq_{\mathrm{DG}}(v_{\mathrm{DG}})}{dt} + \frac{dq_{\mathrm{DS}}(v_{\mathrm{DS}})}{dt} \\ &= C_{\mathrm{DS}}\frac{dv_{\mathrm{DS}}}{dt} + C_{\mathrm{DG}}\frac{dv_{\mathrm{GS}}}{dt} \end{aligned}$$

with

$$\begin{aligned} C_{\mathrm{DS}} &= \frac{\partial q_{\mathrm{DS}}(v_{\mathrm{DS}})}{\partial v_{\mathrm{DS}}} + \frac{\partial q_{\mathrm{DG}}(v_{\mathrm{DG}})}{\partial v_{\mathrm{DG}}} \\ C_{\mathrm{DG}} &= -\frac{\partial q_{\mathrm{DG}}(v_{\mathrm{DG}})}{\partial v_{\mathrm{DG}}}. \end{aligned}$$

Let us expand the current and charge in a Fourier series

$$\begin{aligned} i_{D,\mathrm{displ}} &= \mathcal{R}e\left\{\sum_{n=1}^{n_H} I_{D,\mathrm{displ},n}e^{jn\omega t}\right\} \\ q_{\mathrm{DG}} &= \mathcal{R}e\left\{\sum_{n=1}^{n_H} Q_{\mathrm{DG},n}e^{jn\omega t}\right\} \\ q_{\mathrm{DS}} &= \mathcal{R}e\left\{\sum_{n=1}^{n_H} Q_{\mathrm{DS},n}e^{jn\omega t}\right\}. \end{aligned} \tag{6}$$

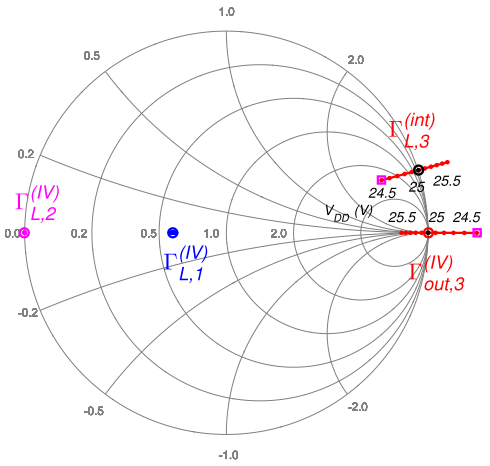

Fig. 7. Trajectory of $\Gamma^{(\mathrm{int})}_{L,3}$ with V_{DD} at 2 GHz. Also shown are the reflection coefficients $\Gamma^{(IV)}_{L,1}$, $\Gamma^{(IV)}_{L,2}$, and $\Gamma^{(IV)}_{\mathrm{out},3}$ at the optimized class-F operating point.

We can then readily write the identity

$$I_{D,\mathrm{displ},n} = jn\omega\ (Q_{\mathrm{DG},n} + Q_{\mathrm{DS},n})$$

where the $Q_{\mathrm{DG},n}$ and $Q_{\mathrm{DS},n}$ are pure real coefficients, since the class-F waveforms drain $V_{\mathrm{DS},n}$ and gate $V_{\mathrm{GS,n}}$ voltages applied in (2) are all cosine waves. Thus, the displacement current components $I_{D,\mathrm{displ},n}$ are all 90° out of phase (sinewave) relative to the drain-to-source voltage.

The odd-harmonic impedances are then given by

$$Z^{(\mathrm{int})}_{L,n} = \frac{V_{\mathrm{DS},n}}{-I_{D,n}} = \frac{V_{\mathrm{DS},n}}{-I_{D,\mathrm{displ},n}} = \frac{jV_{\mathrm{DS},n}}{n\omega\ (Q_{\mathrm{DS},n} + Q_{\mathrm{DG},n})}$$

where we assume that we have set the odd harmonic of the dc IV equal to zero ($I_{\mathrm{Di},n} = 0$ for odd $n > 1$). Given that $V_{\mathrm{DS},n}$, $Q_{\mathrm{DG},n}$, and $Q_{\mathrm{DS},n}$ are all pure real coefficients and nonzero for the odd harmonics, the class-F operation can be sustained by a *lossless* impedance termination. Typically, $(Q_{\mathrm{DS},3} + Q_{\mathrm{DG},3})/V_{\mathrm{DS},3}$ is real and positive for the third harmonic, and an inductor is required for $\Gamma^{(\mathrm{int})}_{L,3}$ as is shown in Fig. 7 (black circles on Smith chart edge). The trajectories (red dotted lines) of $\Gamma^{(IV)}_{\mathrm{out},3}$ and $\Gamma^{(\mathrm{int})}_{L,3}$ as V_{DD} varies are also shown in Fig. 7. The variation of the fundamental load $\Gamma^{(IV)}_{L,1}$ (blue dots) with the drain bias is itself nearly not distinguishable. The class-F design used for these simulations is described in more detail in the next section. To confirm the validity of the load $\Gamma^{(\mathrm{int})}_{L,3}$ predicted by the simulation of the circuit in Fig. 6, an efficiency contour plot obtained for a third-harmonic load–pull simulation is shown in Fig. 8. This confirms that the load $\Gamma^{(\mathrm{int})}_{L,3}$ obtained for the proposed optimized class-F design is indeed the optimal solution for the device at the intrinsic reference planes. Instead of using the class-F drain voltage waveform, we can now use an inductor for the third-harmonic load termination as shown in Fig. 9.

The calculation of the voltage and current waveforms at the package reference planes starting from the augmented intrinsic circuits in Figs. 6 and 9 now requires the modified embedding device model shown in Fig. 10, since two of the nonlinear capacitances were included in the intrinsic device model in Figs. 6 and 9.

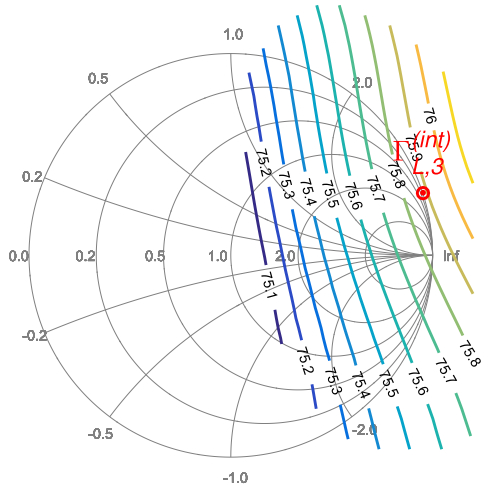

Fig. 8. Efficiency (%) contour plot for the third-harmonic load–pull simulation at 2 GHz for the intrinsic device model of Fig. 6 confirming the validity of the optimal load $\Gamma_{L,3}^{(\mathrm{int})}$ predicted by the proposed optimal class-F theory with a single simulation of the circuit of Fig. 6.

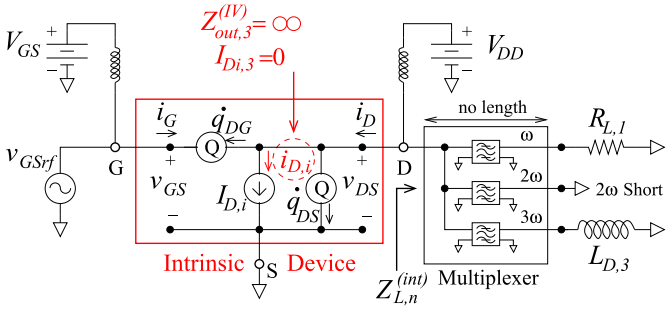

Fig. 9. Multiharmonic loading requirements at the intrinsic reference planes for optimized class-F operation.

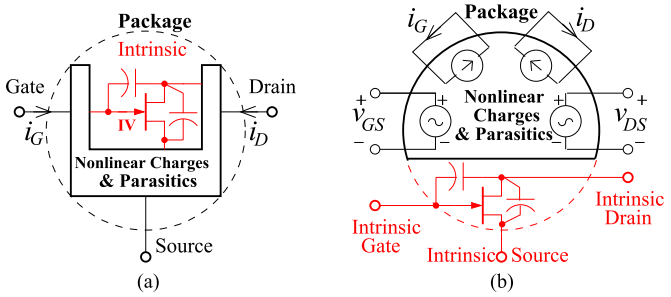

Fig. 10. Modified (a) FET model and (b) embedding device model when the optimized class-F operation is defined by multiharmonic impedance terminations at the intrinsic reference planes.

III. Class-F PA Design

To validate the updated definition of class F at the intrinsic level, an optimized class-F PA was designed using a realistic transistor model. The embedding device model for the Angelov model was implemented in Keysight Technologies Advanced Design System (ADS) using symbolically defined devices (SDDs) [5]. These SDDs are multiport devices that allow us to create equation-based user-defined nonlinear components. They are defined by relationships that relate the port voltages, currents, and their derivatives, as well as the currents from other devices. The procedure to obtain the package parasitics and model coefficients is presented in [5]. Harmonic balance within ADS was used to calculate the voltages (v_{GS} and v_{DS}) and current I_D at the intrinsic level for the fundamental, second, and third harmonic (ω, 2ω, and 3ω). The design approach was based on [17] and [24] for a maximally flat voltage response and the optimal V_{DS} taking into account the first three harmonics. The impedance terminations are based on (2).

TABLE II

Simulated Results for $V_{\mathrm{DS},n}$ and $I_{\mathrm{Di},n}$ at the Intrinsic Reference Planes for a Class-F PA

n	Frequency (GHz)	$V_{DS,n}$ (V)	$I_{Di,n}$ (A)
1	2	$25.13\angle 180°$	$0.863\angle -0.572°$
2	4	0	$0.349\angle 0.78°$
3	6	$4.19\angle 0°$	$0.013\angle 89.9°$
4	8	0	$0.044\angle 171°$
5	10	0	$0.035\angle 3.85°$

The drain was biased at $V_{\mathrm{DD}} = 25$ V and the gate at -2.9 V to yield a quiescent drain current of 95 mA. The input voltage source was set to a fundamental frequency of 2 GHz and a magnitude of 2.37 V. At the output, two voltage sources were connected in series. The magnitude of the drain-to-source voltage that corresponds to the fundamental frequency was 25.13 V with a 180° phase shift with respect to the input gate voltage source. On the other hand, the magnitude of the voltage source for the third harmonic (3ω) was 4.19 V and in phase (0° phase shift) with respect to the input gate voltage source. The harmonic balance simulation was performed using the first 15 harmonics to obtain the voltages and currents at the intrinsic reference planes. The simulated results for $v_{\mathrm{DS},i}$ and i_{Di} corresponding to the first five harmonics are presented in Table II.

The designed intrinsic load line and waveforms calculated from simulation are shown in Fig. 11(a) and (b), respectively. Also, the intrinsic dc–IV curves obtained from the transistor model are displayed in Fig. 11(a) as a reference. One can observe that the load line is reaching the IV knee at low drain voltages and the waveforms correspond to the rectangular drain voltage waveform and the half-rectified sinewave current as intended for class-F mode operation.

From Table II, one can obtain the intrinsic load impedances for the fundamental and the second and third harmonics from the circuit in Fig. 6 using the following equation:

$$Z_{L,n}^{(\mathrm{int})} = -\frac{V_{\mathrm{DS},n}}{I_{D,n}}.$$

The calculated load impedances were $Z_{L,1}^{(\mathrm{int})} = 29.1\ \Omega$, $Z_{L,2}^{(\mathrm{int})} = 0\ \Omega$, and $Z_{L,3}^{(\mathrm{int})} = j\ 311.9\ \Omega$. These values are in good agreement with the fundamental and second-harmonic load impedances described by (1). However, for the third harmonic, the load impedance is not infinite (open circuit), but its value corresponds to an inductive reactance. The 180° out-of-phase third harmonic is generated by terminating the 90° out-of-phase current $-I_{D,3}$ and inductor $L_{D,3}$ such that

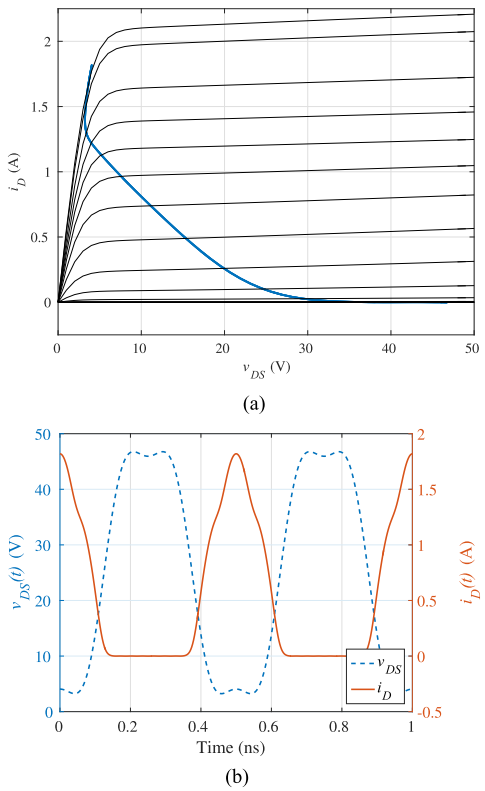

Fig. 11. Simulated intrinsic (a) load line and (b) waveforms.

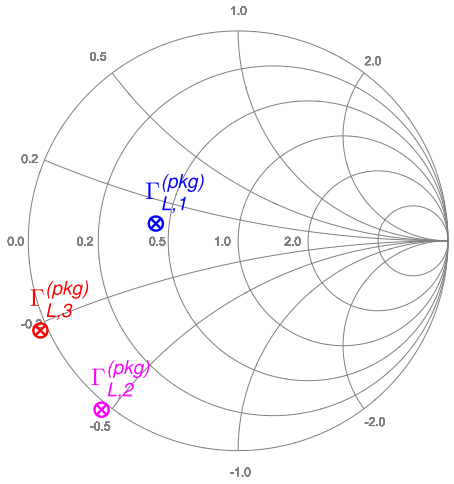

Fig. 12. Multiharmonic loads at the packaged reference planes predicted by the *embedding device model* at ω, 2ω, and 3ω sustaining class-F operation at 2 GHz for the demo GaN HEMT.

we have $Z_{L,3}^{(\text{int})} = j3\omega L_{D,3}$. To determine the required input excitation or load for each harmonic at the packaged reference planes, an external projection of the internal operation to the package reference planes is accomplished in a single simulation using the embedding device model. The resulting fundamental and harmonic loads obtained from the projection through the linear extrinsic and package parasitics are shown in Fig. 12.

Note that the harmonic loads at the packaged reference planes are rotated and slightly outside of the Smith chart. This effect can be explained due to the reactive and lossy elements that form both the extrinsic and package parasitics. Therefore, to obtain the desired class-F operation at the intrinsic reference plane, the fundamental and harmonic impedance terminations at the packaged reference planes are given by $Z_{L,1}^{(\text{pkg})}$, $Z_{L,2}^{(\text{pkg})}$ and $Z_{L,3}^{(\text{pkg})}$. Thus, the harmonic loads should be slightly active to synthesize the optimal mode of operation at the device intrinsic reference planes. In practical PA implementations, the closest passive load will be used. However, since the intention of this paper is to approach the optimal class-F operation, slightly active loads were synthesized using harmonic injection in the load–pull measurements.

TABLE III

SIMULATED EFFICIENCIES AS A FUNCTION OF α_3 FOR $V_{\text{DD}} = 23.2$ V AND $V_{\text{DS},1} = 25.13$ V

α_3	P_{DC} (W)	$\frac{P_{RF,3}}{P_{DC}}$ (%)	$\frac{P_{diss}}{P_{DC}}$ (%)	η (%)	$\eta^{(P)}$ (%)	$\lvert\Gamma_{L,3}\rvert$
0.1875	10.79	0.38	17.78	81.84	78.65	0.69
0.1975	10.85	0.00	17.74	82.26	79.04	1.00
0.2075	10.88	-0.40	17.76	82.64	79.39	1.38

The new optimized class-F design procedure was presented here for a GaN HEMT example. It was also verified that similar results could be obtained with an SOI-MOSFET using a previously reported ANN model [28]. An infinite third-harmonic output impedance ($Y_{\text{out},3}^{(IV)} = 0$) was obtained at the current-source reference planes by tuning the drain bias voltage while using $\alpha_3 = 1/6$. The resulting voltage and current waveforms were quite similar to the GaN HEMT even though the drain voltage was limited to 2.5 V. An efficiency of 67% and 60% was obtained at the current-source and package reference planes, respectively, while using $\alpha_3 = 1/6$. These results demonstrate that it is possible to use to our advantages the nonlinearities of the IV characteristics in other technologies besides GaN technologies.

In the demonstration example presented in this section, the LSOP (primarily V_{DD} and $V_{\text{DS},1}$) is selected such that the third-harmonic drain voltage verifies $V_{\text{DS},3} = -V_{\text{DS},1}/6$. This was motivated by the fact that $\alpha_3 = 1/6$ is the optimal value yielding the best drain efficiency for ideal devices [24]. However, a different LSOP (V_{DD} and $V_{\text{DS},1}$) could be first selected to further reduce $P_{\text{diss}}/P_{\text{dc}}$ and obtain a higher drain efficiency. The amplitude of the third-harmonic voltage $V_{\text{DS},3} = -\alpha_3\ V_{\text{DS},1}$ or equivalently α_3 can then be tuned to minimize $P_{\text{RF},3}$ and obtain the optimal class-F operation. The goal is to obtain a device dynamic load line that follows the edge of the IV characteristics in the triode region more closely, by accounting for the reduction of the IV knee voltage at lower instantaneous gate voltages. As shown in Table III, an intrinsic efficiency above 80 % can then be achieved that way at the current-source reference planes for the GaN HEMT considered with an optimized LSOP maintaining about the same output power. Similar intrinsic efficiencies around 80 % were also obtained for the SOI-MOSFET by jointly optimizing the LSOP and α_3.

IV. MEASUREMENTS AND MEASUREMENT SETUP

In order to validate the simulated results obtained in Section III, experiments were carried out to demonstrate the good agreement between simulated and measured results.

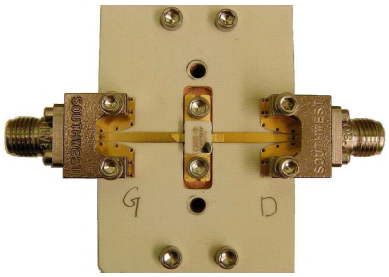

Fig. 13. Photograph of the testbed for measuring the GaN transistor (CGH27015F).

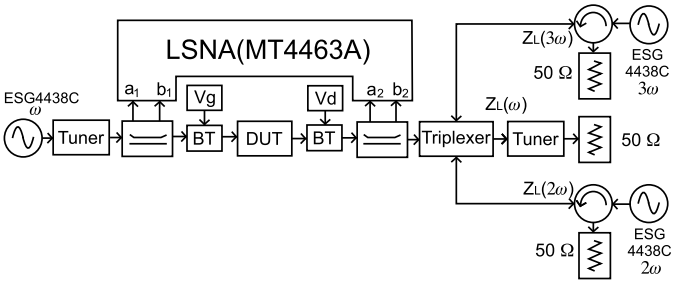

Fig. 14. Harmonic load–pull measurement setup with an LSNA.

An active harmonic load–pull measurement setup with a large-signal network analyzer (LSNA) was used to characterize a commercially available GaN transistor CGH27015F from CREE Semiconductors. This HEMT was originally designed for high efficiency, high gain, and wide bandwidth capabilities. The 15-W peak power device provides in the 440166 package a 2 W average power with 28 V drain voltage. The TRL testbed shown in Fig. 13 was used to mount the transistor. A plastic pressure bar (not shown in Fig. 13) was used to electrically connect the gate and drain terminal contacts to the microstrip lines of the testbed. On the other hand, underneath the transistor, a copper bar that acts as a heat sink is used to connect the source terminal, which sat on a temperature-controlled thermal chuck. The measurements were performed at a chuck temperature of 10 °C.

With the help of the LSNA (MT4463A), the multiharmonic incident (a_1 and a_2) and the reflected (b_1 and b_2) waves at each port of the device under test (DUT) were measured using two directional couplers (RT0812H). These power waves along with the characteristic impedance of the system allow one to calculate the magnitudes and phases of the voltages and currents at the testbed reference planes. The testbed or DUT is then placed on the active harmonic load–pull setup as shown in Fig. 14. The fundamental frequency (ω) of the input signal source (Agilent ESG4438C) is set to 2 GHz. An automatic mechanical tuner connected between the input signal source and the testbed's input is used to obtain the input matching network at the fundamental. On the other hand, at the output stage, an active harmonic injection for the second and third harmonics (2ω and 3ω) is accomplished with the help of two RF signal sources (Agilent ESG4438C) and a triplexer (Maury Microwave, 9677G). The triplexer is used to connect the DUT's output to the fundamental load as well as the second- and third-harmonic loads. These harmonic loads at the reference planes of the DUT's output can be obtained by wave injection using the above-mentioned RF signal sources.

To protect the RF sources, circulators are used between each of the signal sources and the triplexer to inject the incident wave a_2 and a_3 into the DUT's output while redirecting the reflected power wave b_2 and b_3 to a matched load. Two bias tees are used to provide the required biasing of the transistor. A dc current meter is used to measure the drain current.

A. Experimental Conditions

Before excitations are applied to the DUT, it is important to note that another projection of the fundamental and harmonic loads at the packaged reference planes (obtained with the help of a linear embedding model) is required to take into account the transmission lines and the connectors of the testbed. The TRL calibration method was used to characterize the error boxes of the testbed fixture.

Initially, the transistor was biased as follows: $V_{\mathrm{DD}} = 25$ V, $V_{\mathrm{GS}} = -2.65$ V, and $I_D = 95$ mA. The input power source was set to an amplitude $|a_1(\omega)|$ of 27 dBm with a fundamental frequency of 2 GHz. With the help of a passive tuner, the fundamental load impedance was obtained at the connector reference plane. Two RF power sources were used at the DUT's output to implement harmonic injections at 2ω and 3ω. By controlling the corresponding harmonic magnitude and phase of each power source, one can obtain the required harmonic load impedances at the connector reference planes. A 10-MHz reference signal was used to phase-lock the LSNA with the three RF sources. By sweeping V_{DD} in a 24–27-V range, the best drain efficiency was obtained at 26 V. This drain bias tuning is required to compensate for the difference in knee voltages between the real device and the device model used. This bias voltage was then used in the rest of the measurements. In order to experimentally determine the dependence of the drain efficiency on the third-harmonic impedance termination, an active load–pull was implemented by changing the magnitude and phase of the power source that injects the signal at 3ω.

V. Measured Results and Discussion

The resulting efficiency contour plot obtained from the third-harmonic load pull is shown in Fig. 15. The power waves a_1, b_1, a_2, and b_2 measured with the LSNA at the connector reference planes were de-embedded to the package reference planes. The third-harmonic load reflection coefficient $\Gamma_{L,3}^{(\mathrm{pkg})}$ predicted by the embedding device model for the proposed optimized class-F operation is also plotted (red crosses and circles) for comparison and shown to be in good agreement with the load–pull measurements. This experimentally demonstrates the accuracy of the third-harmonic impedance prediction, as well as reveals the great time savings achieved by this methodology. Indeed the embedding process (a single simulation) together with the proposed class-F definition directly predicts the optimal third-harmonic impedance termination without the need for third-harmonic load–pulls.

The measured power waves allow us to obtain the voltages and currents at the connector level. However, with the help of the deembedding transfer network, one can predict the actual harmonic drain voltage and drain current at the intrinsic ref-

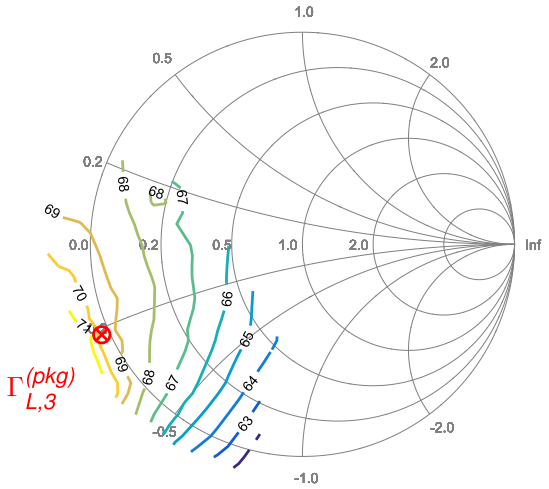

Fig. 15. Experimental drain efficiency contour plot obtained from the measured third-harmonic load–pull after deembedding from the connector to the package reference planes. The third-harmonic load reflection coefficient $\Gamma_{L,3}^{(pkg)}$ predicted by the embedding device model from the proposed optimized class-F theory and plotted using a red cross and circle is properly positioned at the location yielding maximum efficiency in the measured efficient contour plot.

TABLE IV

DE-EMBEDDED MEASURED V_{DS} AND I_D AT THE INTRINSIC REFERENCE PLANES

n	Frequency (GHz)	$V_{DS,n}$ (V)	$I_{Di,n}$ (A)
1	2	$27.38\angle -8.28°$	$0.939\angle 171.8°$
2	4	$0.114\angle 124.5°$	$0.199\angle -23.3°$
3	6	$5.90\angle 166.4°$	$0.025\angle 64.9°$
4	8	$1.03\angle 122.4°$	$0.125\angle 15.9°$
5	10	$1.17\angle 152.8°$	$0.105\angle 43.14°$

TABLE V

SIMULATED AND MEASURED DRAIN EFFICIENCIES

Reference Planes	Simulated Drain Efficiency	Measured Drain Efficiency
Intrinsic	75.88 %	72.64 %
Package	72.63 %	69.78 %

erence planes [5]. The de-embedded measurement magnitude and phases for ω, 2ω, and 3ω are presented in Table IV.

From Table IV, one can observe a 180° phase shift between $V_{\mathrm{DS},i}(\omega)$ and $I_{\mathrm{Di}}(\omega)$, as well as between $V_{\mathrm{DS},i}(\omega)$ and $V_{\mathrm{DS},i}(3\omega)$. Also, the magnitudes of $V_{\mathrm{DS},i}(2\omega)$ and $I_{\mathrm{Di}}(3\omega)$ are very small, as expected. The de-embedded measured intrinsic load line and waveforms are shown in Fig. 16(a) and (b), respectively. The intrinsic dc IV characteristics obtained from the transistor model are also displayed as a reference. Table V summarizes the efficiency predicted and measured at the intrinsic and package reference planes. About 3% percent difference is observed. It should be noted that in this paper the harmonics were not terminated at the gate reference planes with the impedance predicted by the embedding device model, which could explain the residual efficiency loss observed. Also the device model extracted is of limited accuracy. However, the optimal load for the third harmonic predicted by the embedding device model is in close agreement with the prediction of the embedding device model for the proposed optimal class-F mode of operation.

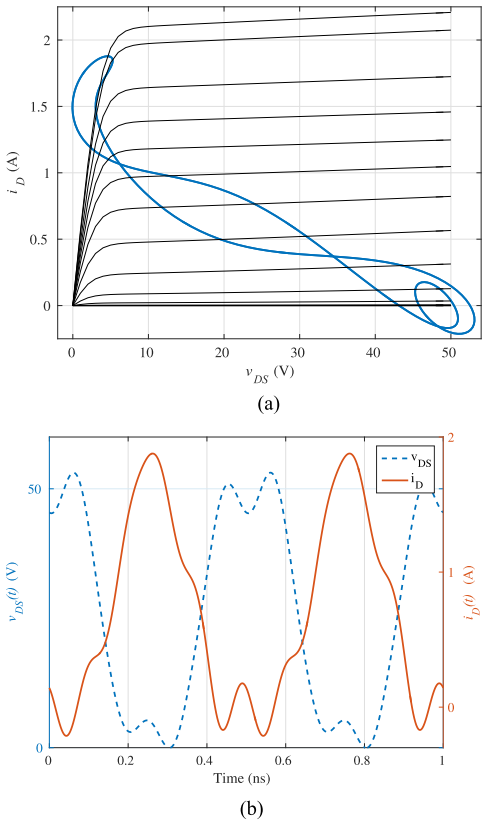

Fig. 16. De-embedded measured intrinsic (a) load line and (b) waveforms using the five measured harmonics.

VI. CONCLUSION

In this paper, an updated definition of class F at the intrinsic level was presented for realistic transistor models exhibiting a nonzero IV knee voltage. This was motivated by the fact that the conventional definitions of class F based on voltage waveforms or harmonic impedance terminations are found not to be optimal when applied to realistic device models because they cannot simultaneously sustain: 1) zero harmonic power dissipation and 2) the desired quasi-rectangular waveform. On the other hand, the proposed optimized class-F definition is able to simultaneously yield: 1) zero odd-harmonic power dissipation and 2) the desired quasi-rectangular waveform. This is achieved by setting to infinite the odd-harmonic device output impedance instead of the odd-harmonic load impedance. It was shown that for the third harmonic this can be achieved by fine tuning the RF fundamental amplitude or/and the drain bias so as to place the drain voltage minima at the required sweet point in the IV knee. This tuning can be readily performed after the PA has been built to optimize the PA performance. It was verified that these third-harmonic tunings have themselves a negligible effect on the fundamental and second-harmonic impedance terminations.

Further in this paper, it was demonstrated that the third-harmonic voltage does not need to be supported by lossy harmonic impedance terminations. Instead, it can be sustained using a proper (typically inductive) lossless impedance termination at the intrinsic reference planes for the third harmonic of the drain displacement current generated by the nonlinear gate-to-drain capacitance. The displacement current

being already 90° out of phase with the drain-to-source voltage, the inductive load termination brings about another 90° phase shift such that the third-harmonic drain voltage is 180° out of phase with the fundamental drain voltage as required to form the optimal quasi-rectangular waveform. The inductance value $L_{D,3}$ is itself used to set the desired amplitude for the third-harmonic drain voltage.

It was verified in simulation that the third-harmonic load $\Gamma_{L,3}^{(\mathrm{int})}$ predicted by the proposed optimized class-F definition at the intrinsic reference planes was indeed the optimal load when compared with the drain efficiency contour plot obtained from third-harmonic load–pull simulations. These simulations confirmed that the proposed class-F design methodology yields the optimized class-F three-harmonic solution for the device.

The experimental verification of the optimized class F for realistic transistors was conducted on a GaN HEMT by comparing the measured and simulated load–pull results for the drain efficiency at the package reference planes. A close agreement was obtained for the predicted and measured optimal third-harmonic load termination bringing experimental support to the optimized class-F definition.

The extension of this paper to higher harmonics, e.g., fifth order, is conceivable, but this may require the injection of harmonics at the gate to simultaneously set the output conductances $Y_{\mathrm{out},3}^{(IV)}$ and $Y_{\mathrm{out},5}^{(IV)}$ of the transistor equal to zero.

It was shown in this paper how the optimized class-F definition presented here could readily be used in combination with the embedding device model to predict in a single-harmonic balance simulation the voltage and current waveforms required at the package reference planes to sustain the optimal intrinsic class-F mode. However, given the fact that the knee voltage in GaN HEMTs is known to change with temperature and trapping, a fine tuning of the RF fundamental amplitude or/and the drain bias will usually be required in practice to achieve and maintain the optimized class-F operation described in this paper.

To conclude, it should be pointed out that in the design of a class-F amplifier, care should be taken to optimize the LSOP in addition to the third-harmonic component of the drain voltage. The selection of the LSOP involves a tradeoff in which the fractional dissipated power is reduced at the cost of an acceptable decrease in RF output power. Once the LSOP is determined, the optimal class-F operation as defined in this paper (infinite third-harmonic output impedance) should then be obtained by tuning only the third-harmonic component of the drain voltage. Note that the tuning of the third harmonic drain voltage is done automatically in harmonic-balance simulations when the load presented to the IV characteristics (see Fig. 2) at the third harmonic is an open circuit. The final multiharmonic impedance terminations at the package reference planes are then obtained using the *embedding device model*.

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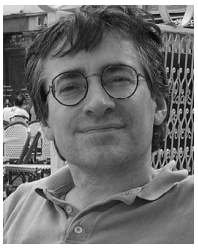

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