Metal-Embedded Chip Assembly Processing for Enhanced RF Circuit Performance

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***Abstract*— This paper presents the radio frequency (RF) benefits of a heterogeneous integration technique for multi-chip modules. Passive components, such as lumped metal–insulator–semiconductor (MIS) and ceramic capacitors, as well as coupler circuits implemented on alumina substrates, are integrated in a metal-embedded chip assembly (MECA) process together with GaN monolithic microwave-integrated circuits (MMICs) in a way that provides a common RF and thermal ground. Simulations show that photolithographically defined interconnects can outperform wire bonds from 10 to 100 GHz. The interconnect layer of the MECA process forms bridge transmission lines with lower loss and comparable dispersion to microstrip lines, and with 35% higher characteristic impedances, validated by measurements up to 25 GHz. Microstrip Lange and branch-line couplers are designed partially on alumina and completed with MECA interconnects during the integration process, resulting in good performance in agreement with simulations. Finally, measurements of a GaN power amplifier (PA) MMIC integrated into the MECA process show gain and power-added efficiency (PAE) improvements of up to 3 dB and 3.2 percentage points, respectively.**

***Index Terms*— Couplers, GaN, heterogeneous integration, interconnects, multi-chip modules, power amplifiers (PAs), transmission lines.**

I. Introduction

HETEROGENEOUS integration is gaining increased interest for miniaturized radio frequency (RF) front ends [1], [2]. The goal is to enable the integration of RF compound semiconductor (GaAs, GaN, and InP) monolithic microwave integrated circuits (MMIC) with digital and analog CMOS circuits and low-cost high-performance passives implemented in alumina, aluminum nitride, silicon, or glass with good thermal performance. An example discussed in this paper is shown in Fig. 1, which shows a variety of chips embedded in a common thick copper ground. Previous demonstrations of heterogeneous integration include a double heterojunction bipolar transistor (DHBT) InP 300-GHz amplifier that is heterogeneously integrated with a 130-nm RF CMOS chip without performance degradation [3]. In another integration process, InP heterojunction bipolar transistor (HBT) chiplets were interconnected to Si CMOS chips in [4] in a differential amplifier with a slew rate of 2.56×10^4 V/μs and an output swing of 3.42 V. Integration of InP HBTs grown next to Si CMOS transistors on a Si substrate is demonstrated in [5]. The integration allows tight device placement with a separation between the HBTs and CMOS transistors as small as 2.5 μm. Another example of InP integration with GaN and CMOS is shown in [6], with a Q-band InP HBT voltage-controlled oscillator (VCO) and a GaN high-electron mobility transistor (HEMT) amplifier on a common 65-nm CMOS substrate.

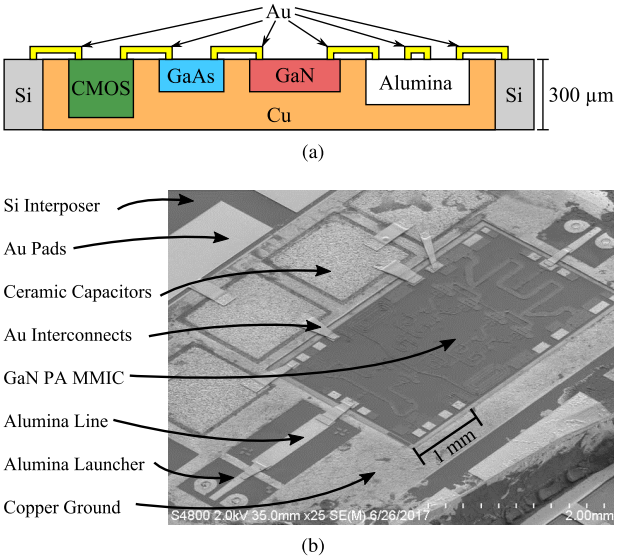

Fig. 1. (a) MECA process cross-sectional example showing different technologies integrated into a single thermal and RF ground within a Si interposer wafer (not to scale). (b) Photograph of a GaN MMIC PA integrated with alumina launchers, an alumina transmission line, and ceramic off-chip capacitors.

Several "quasi-MMIC" circuits have been demonstrated, where GaN power amplifiers (PAs) are integrated with partial matching networks implemented in a different material. For example, [7] demonstrates a 0.25-μm GaN MMIC with pre-matching performed on chip and wire bonded to a partial matching circuit on a Rogers 4350B substrate. The results using limited GaN-on-SiC area show a power-added efficiency (PAE) of 71% with a saturated gain of 12 dB and output power of 3 W (power density of 4.5 W/mm) at 9.8 GHz in

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continuous wave (CW) operation. GaN HEMTs wire bonded to GaAs' passive matching circuits and mounted on a common carrier metal plate form a quasi-MMIC Doherty PA operating from $1.7 to 2.7$ GHz with a 37% back-off efficiency [8]. A similar Doherty quasi-MMIC at 5.5–6.5 GHz is demonstrated in [9]. In [10], GaN HEMTs are interconnected heterogeneously with Si matching networks, resulting in 170-W output power and PAE $>$ 40% using a copper interconnect structure. A single-stage copper-embedded X-band PA quasi-MMIC with improved efficiency is also demonstrated in [11] using a GaN transistor, Si matching networks, and an interconnect layer.

HRL's metal embedded chip assembly (MECA), formerly integrated thermal array plate (ITAP) [12], [13], is a technique for heterogeneous integration that provides an excellent thermal and RF ground. Fig. 1 shows an example MECA cross section and a photograph of a portion of an implemented module. The approach integrates chips into a copper heat spreader block within the thickness of a silicon interposer wafer. An intimate contact between the backside of the chips and the heat spreader, with no thermal interface materials (TIMs), improves the thermal management compared to traditional technologies. A lithography-based interconnect layer replaces wire bonds and the minimum demonstrated distance between the chips is 70 μm, with a possibility of reduction to 30 μm through further process optimization.

The MECA process is shown in Figs. 2 and 3. Fig. 2 describes the pre-processing steps required for copper plating that enable a good thermal and electrical ground. Various chips and passive circuits are mounted face-down on a temporary carrier wafer. Fig. 2(b) shows several temporary bonded circuits (alumina, GaN MMICs, and ceramic capacitors), as well as some alignment marks used for chip placement. In parallel, a silicon interposer wafer is etched [Fig. 2(c)] allowing for a number of different heterogeneous modules to be fabricated simultaneously. The interposer (body) wafer is then bonded to the temporary carrier wafer, as shown in Fig. 2(d). At this point in the process, the cavities and ground planes of the individual circuits are prepared for copper plating, which will provide the common thermal and electrical ground. The copper heat spreader is then electroformed into the cavities, as shown in Fig. 3(a), and the MECA wafer released from the temporary carrier wafer [see Fig. 3(b)] and flipped. Finally, single-layer air-bridge gold MECA interconnects for chip-to-chip, chip-to-interposer, and intra-chip electrical connections are fabricated [see Fig. 3(c)].

In this paper, which is an extension of the investigation presented in [14], we demonstrate the improved performance of several passive networks, as well as a GaN MMIC PA, to showcase the use of the MECA interconnects as an additional design tool for microwave circuits, combined with alumina microstrip structures that can be manufactured in a simple and economical way. Section II extends the work in [14] to a study of the basic interconnect and transmission line elements available in the MECA process with supporting measurements. Section III shows results for passive circuits implemented in alumina, specifically broadband branch-line and Lange couplers, which use the interconnect layer as a part

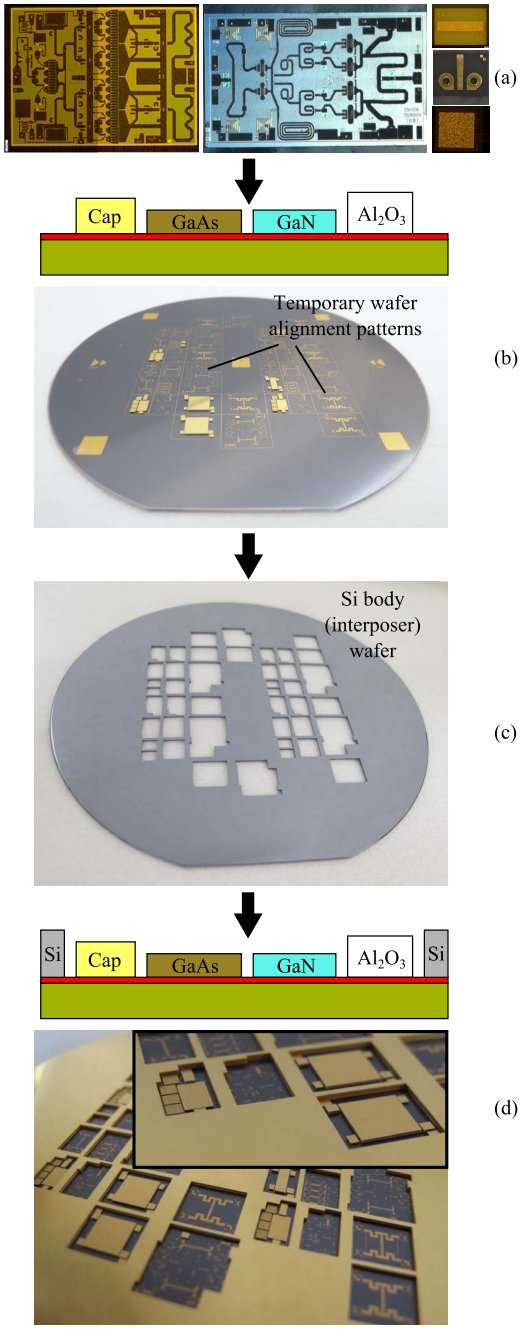


Fig. 2. High-level illustration of the MECA process flow. (a) Chips and passives of diverse technologies. (b) Face-down placement and bonding of chips on a temporary carrier wafer. (c) Metalized interposer Si wafer with etched cavities. (d) Assembled chips and temporary wafer with the interposer wafer.

of the circuit. Section IV further extends the research presented in [14] with a demonstration of an MECA-integrated GaN MMIC PA with improved thermal performance, as well as associated integration of surface mount capacitors for biasing.

II. Interconnects

In this section, detail on the MECA high-frequency interconnects is provided, as well as a comparison to wire bonds.

A. Photolithographically Defined MECA Interconnects

The most common interconnect between chips and packages is wire bonds. Gold wire bonds are used at high frequencies for

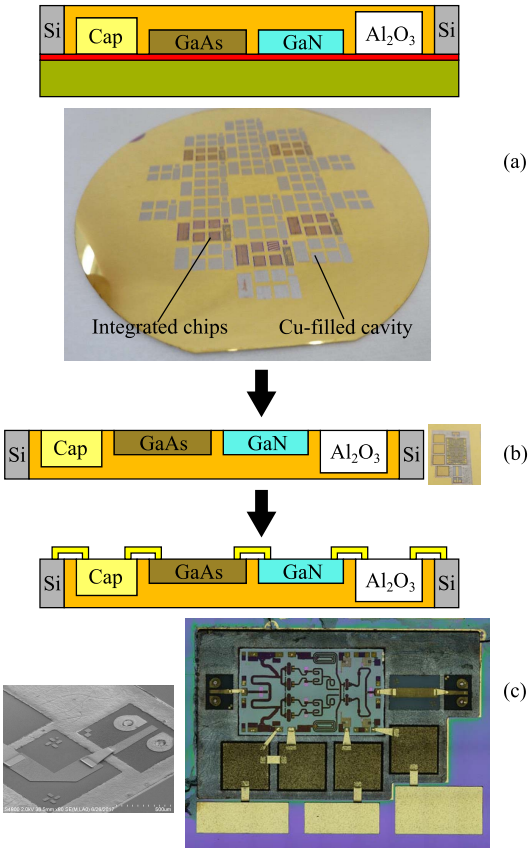


Fig. 3. Continuing from Fig. 2(d). (a) Copper heat spreader is electroformed into the cavities. (b) MECA wafer released from the temporary carrier wafer and flipped. (c) Finally, single-layer air-bridge Au MECA interconnects for chip-to-chip, chip-to-body, and intra-chip electrical connections are fabricated.

interconnecting microwave transistors and MMICs to passive circuits, with typical diameters of 0.75, 1, and 2 mils (19, 25.4, and 50.8 μm), depending on frequency and current density.

The impedance due to the self-inductance and mutual inductance of multiple wire bonds needs to be taken into account in circuit design [15], [16] and limits the performance at high frequencies [17]. Due to the 3-D nature and limited tolerances of bonding machines, it is difficult to predict the behavior at high frequencies. MECA interconnects allow for the placement of precisely controlled bridge interconnects that can be designed to maximize the matching between the two components and this comes at no added cost. Fig. 4 shows the geometry of the interconnects. Those interconnects are fabricated using conventional photolithography to deposit a stackup of benzocyclobutene (BCB), air, and gold, as shown in Fig. 4.

Fig. 5 shows simulation model geometries used to compare several MECA interconnects and wire bonds. Simulations were performed using Ansys HFSS (full-wave 3-D electromagnetic simulation with the finite-element method). Fig. 6 shows the simulated performance, where it can be seen that the MECA interconnects outperform wire bonds, with dimensions given in Fig. 5, for all the frequency ranges. MECA interconnects can also be designed to resonate in a particular bandwidth with improved performance. In Fig. 6, it can be seen that for interconnect widths of 20, 30, 40, and 50 μm, the return losses are remarkably good for a 360-μm bridge at 97, 76, 48, and 23 GHz and around those frequencies, respectively. Fig. 7 shows the S-parameters of the interconnects as a function of width for different frequencies. It can be seen that there is an optimum width for matching

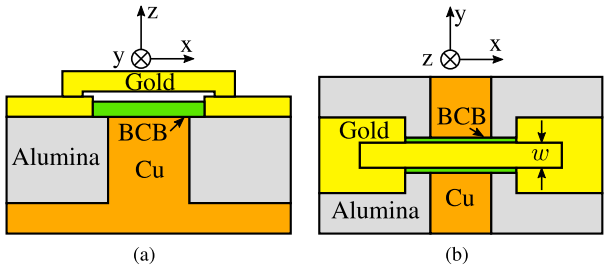


Fig. 4. (a) Side and (b) top views of the interconnect geometry showing the different materials (not to scale). For this paper, we use a 254-μm alumina substrate, 3-μm-thick BCB layer, 5-μm air gap, and 5-μm gold thickness for both microstrip lines and bridges.

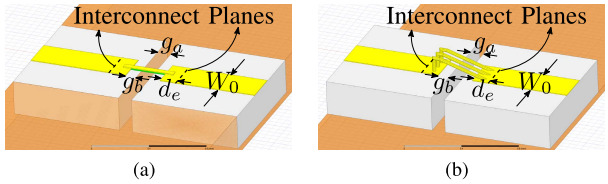


Fig. 5. Interconnect geometries used in simulations. The ports are deembedded to the interconnect plane which is $d_e = 130$ μm away from the strip edge. The widths (W_0) of the microstrip lines are 254 μm (50-Ω lines). The width of the MECA interconnect is w and the wire bond has standard dimensions: 25.4-μm diameter, 100-μm height, and 360-μm bridged distance. (a) MECA interconnect. (b) Wire bond.

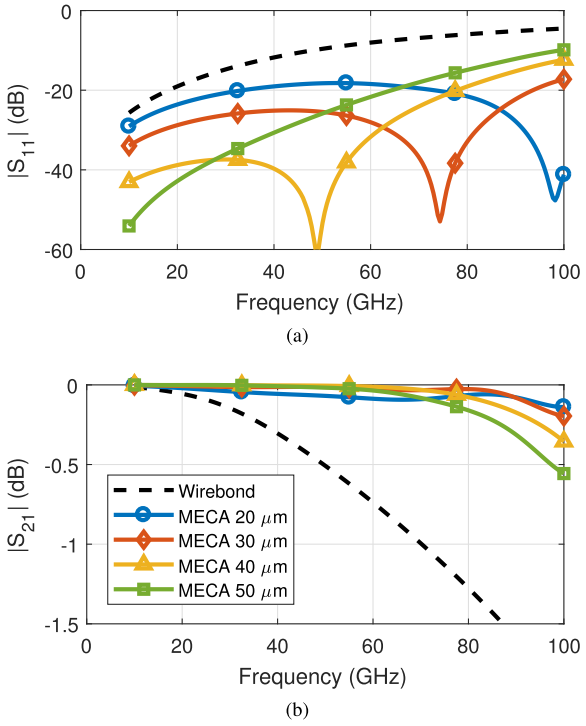


Fig. 6. Simulated frequency response for (a) $|S_{11}|$ and (b) $|S_{21}|$ of the MECA interconnects for different interconnect widths with a standard wire bond shown for comparison, as shown in Fig. 5.

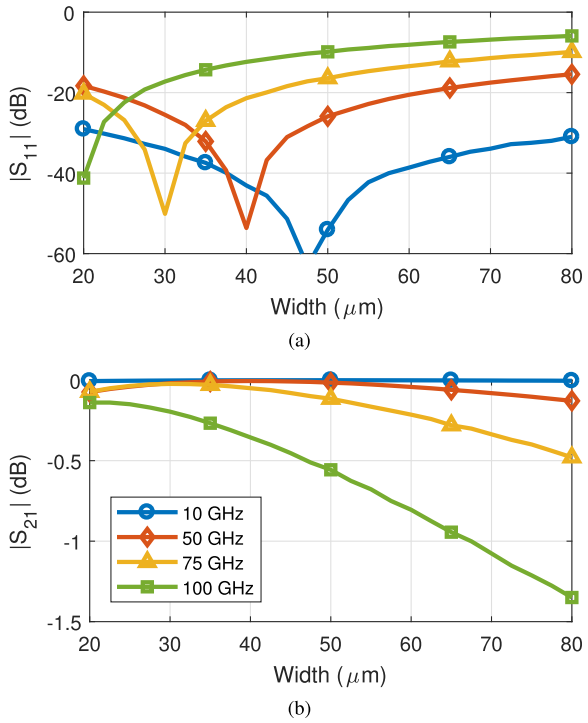


Fig. 7. Plots of (a) $|S_{11}|$ and (b) $|S_{21}|$ for the MECA interconnects versus width simulated at different frequencies, where the interconnect length is kept at 360 μm.

in a particular frequency band and for a particular length. Since the ground of the interconnect is very close to the bridge, the optimum width is small compared to the traces on the substrates. Interconnects can also be tapered to improve matching over large bandwidths at high frequencies.

MECA interconnects can handle larger power levels than gold wire bonds. In both the cases, the maximum current density is about 1 mA/μm^2 which accounts for the joule heating, electromigration, and slow diffusion effects. Direct current (dc) interconnects can be designed to have the same cross section as a wire bond by using an equivalent width of

$$w = \frac{\pi d^2}{4h_{\text{gold}}} \tag{1}$$

where d is the wire-bond diameter and h_{gold} is the gold height of the MECA interconnect. For a 25.4-μm-diameter wire bond, the equivalent MECA width is $w = 101$ μm. At higher frequencies, skin depth becomes smaller than 1 μm (e.g., the skin depth for gold at the X-band is smaller than 0.9 μm) and the cross-sectional perimeter becomes more relevant. The line width that provides the same perimeter as a wire bond is

$$w = \frac{\pi d}{2} - h_{\text{gold}} \tag{2}$$

and for 25.4-μm wire bonds, this width is $w = 35$ μm. Therefore, a 40-μm-wide MECA interconnect can handle the same current as a 25.4-μm-diameter wire bond.

Breakdown in MECA interconnects is dominated by the air gap, which has a 100 times smaller dielectric strength than BCB, as well as a lower relative permittivity. Assuming a homogeneous field distribution across the micro-scale (5 μm) air gap and using a breakdown field strength

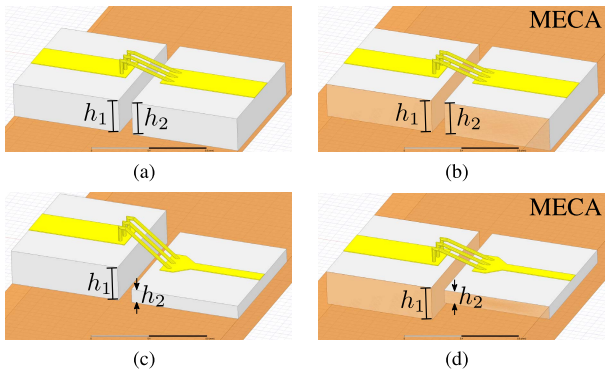


Fig. 8. Four wire-bond geometries with substrate heights of 254 and 100 μm. Wire bonds between two chips of (a) same height ($h_1 = h_2$), (b) embedded in copper and of the same height, (c) different heights ($h_1 > h_2$) and (d) different heights and embedded in copper. The spacing between the two substrates is 360 μm.

of 20 MV/m [18, see Fig. 3], we estimate the breakdown voltage to be 100 V. Full-wave field simulations show that for a 50-Ω interconnect, the error introduced by assuming a homogeneous field distribution is within 6% and therefore, negligible. The breakdown voltage is more than three times larger than the typical 20–30 V used for biasing GaN transistors. Those 100 V correspond to 100 W in a 50-Ω interconnect, assuming low-frequency excitation. For higher frequencies, the power handling in terms of breakdown will exceed this value given the higher breakdown voltage for RF [19]. For higher power designs, the interconnect process may be modified to increase current handling and breakdown voltage even further.

B. Wire Bonds in the MECA Process

Some off-the-shelf MMICs are designed for wire-bond interconnects and these can also be included in a heterogeneously integrated module. Therefore, we next consider the case where MECA and wire bonds coexist and we examine the quality of the wire bonds. MECA processing improves the matching of wire-bond interconnects due to increased proximity of the ground plane to the wire, which, in turn, increases the wire-to-ground capacitance and decreases the interconnect characteristic impedance. When chips of different heights are embedded in metal, their top surfaces are flush against the plated copper surface and require shorter wire bonds with lower inductance. Fig. 8 shows four different cases used for comparing the behavior of wire-bond interconnects in chips that are embedded in metal with those that are traditionally mounted on a heat sink.

The S-parameters of the interconnects shown in Fig. 8 are shown in Fig. 9. It can be seen that wire bonds are better matched when used to interconnect metal-embedded chips. The simulated frequency at which the insertion loss becomes larger than 0.5 dB for a standard wire bond increases from 51 to 87 GHz.

III. Bridge-Line Microstrip

The same processing steps used to form the chip-to-chip interconnects (Section II-A) can be used to form

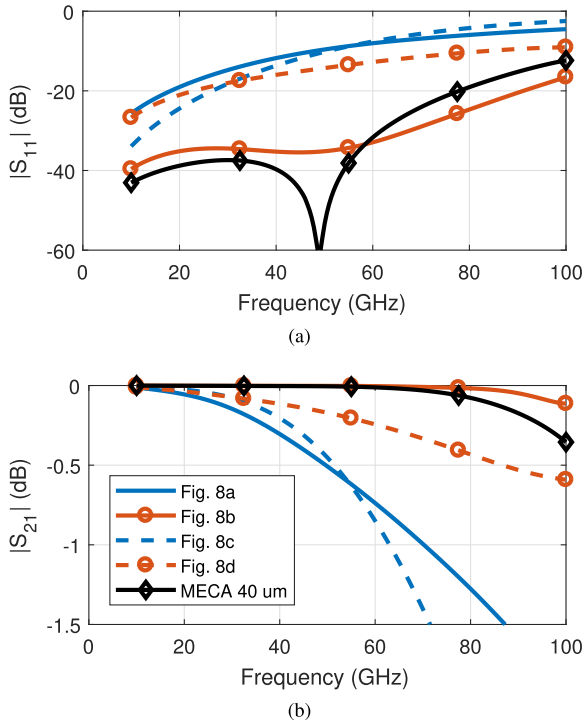


Fig. 9. Plots of the wire-bond (a) $|S_{11}|$ and (b) $|S_{21}|$ for the different configurations shown in Fig. 8 and a 40-μm-wide MECA interconnect for comparison.

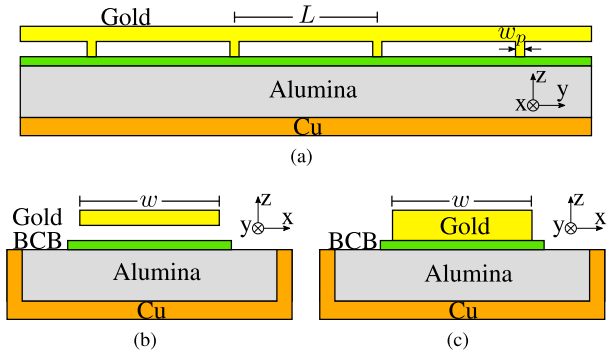


Fig. 10. Bridge-line microstrip geometry after [14]. (a) Side cross section. (b) Strip cross section. (c) Post cross section. w is the strip width and L is the length of one section measured between the centers of two adjacent posts. In this paper, we use 254-μm alumina, 3-μm BCB, 5-μm air, 5-μm gold thickness, $w_p = 20$ μm, and $L = 220$ μm. A section of transmission line L is defined from the center of a bridge to the center of the next one.

inhomogeneous transmission lines on top of existing chips which we refer to as a "bridge line," with cross sections illustrated in Fig. 10. Fabricated bridge lines formed on alumina substrates are shown in Fig. 11.

The available characteristic impedances as a function of line width w for a given spacing between support posts $L = 220$ μm and strip thickness of 5 μm are shown in Fig. 12 for a bridge line with and without the BCB layer and compared to conventional microstrip on 254-μm-thick alumina. Note that higher impedances can be accomplished with the bridge lines due to a decrease in capacitance per unit length [20], which will prove to be useful for the design of MECA passives. The range of realizable impedances for a bridge line and a microstrip is given in Table I. Bridge-line microstrip can thus

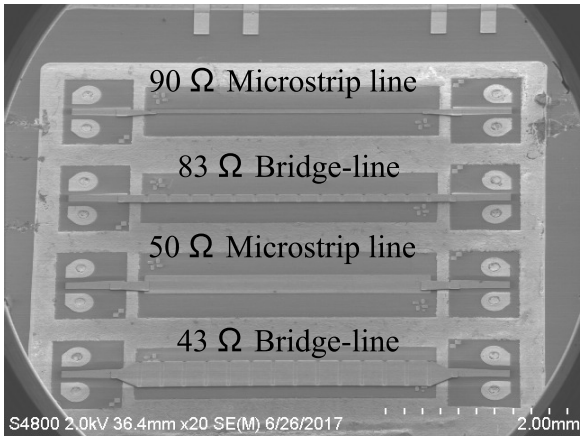


Fig. 11. Photograph of the fabricated test transmission lines after [14]. The second and fourth lines are bridge-line microstrip, and the posts can be seen in this photograph. The launchers are alumina ProbePoint 0503.

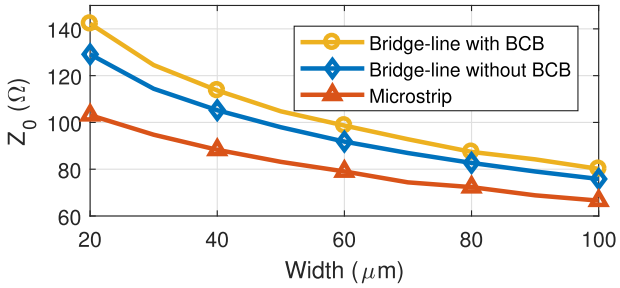


Fig. 12. Characteristic impedance at 10 GHz as a function of line width for different microstrip geometries based on full-wave electromagnetic simulations.

TABLE I

REALIZABLE IMPEDANCES WITH DIFFERENT MICROSTRIP WIDTHS BASED ON FULL-WAVE ELECTROMAGNETIC SIMULATIONS AND FIG. 10

Line type	$w = 400\,\mu$m	$w = 20\,\mu$m
Microstrip	38 Ω	108 Ω
Bridge-Line Microstrip	43 Ω	147 Ω

be used to increase the maximum realizable impedance from 108 to 147 Ω (a 35% increase) for the same line width.

The phase velocity is given by

$$v_p = \lambda_g f = \frac{L}{\tau} \tag{3}$$

where λ_g is the guided wavelength, f is the frequency, and τ is the group delay of the section. The frequencies where the length of this section is $P\%$ of the wavelength are given by

$$f = \frac{\left(\frac{P\lambda_g}{100}\right)}{\lambda_g \tau} = \frac{P}{100\tau}. \tag{4}$$

Full-wave electromagnetic simulations (using Ansys HFSS) show that the group delay for one section of line is around $\tau = 2$ ps, resulting in $P = f_{\mathrm{GHz}}/5$. From here, it can be seen that frequencies under 25 GHz have a section length that is smaller than 5% of the guided wavelength; therefore, the bridge line behaves as a distributed transmission line.

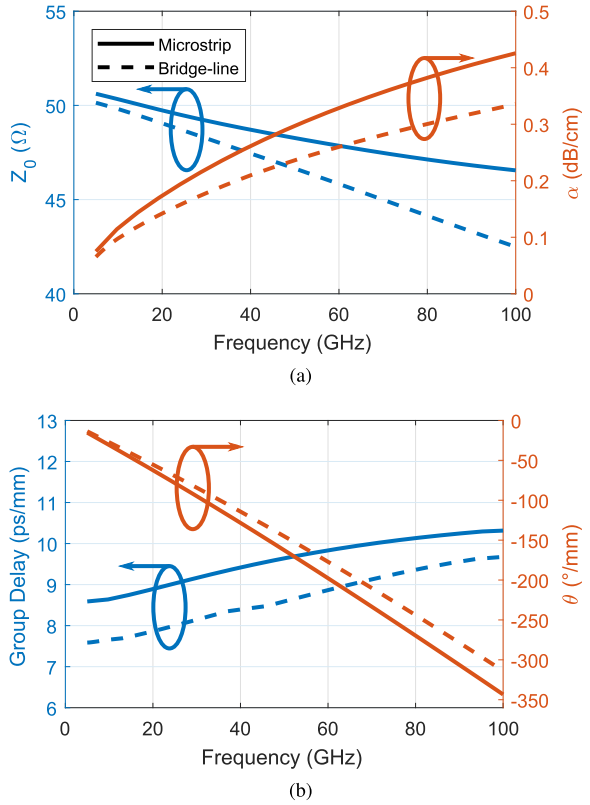


Fig. 13. Plots of the line parameters for one section of a bridge line versus frequency and compared to a conventional microstrip. (a) Characteristic impedance and attenuation constant. (b) Group delay and phase angle.

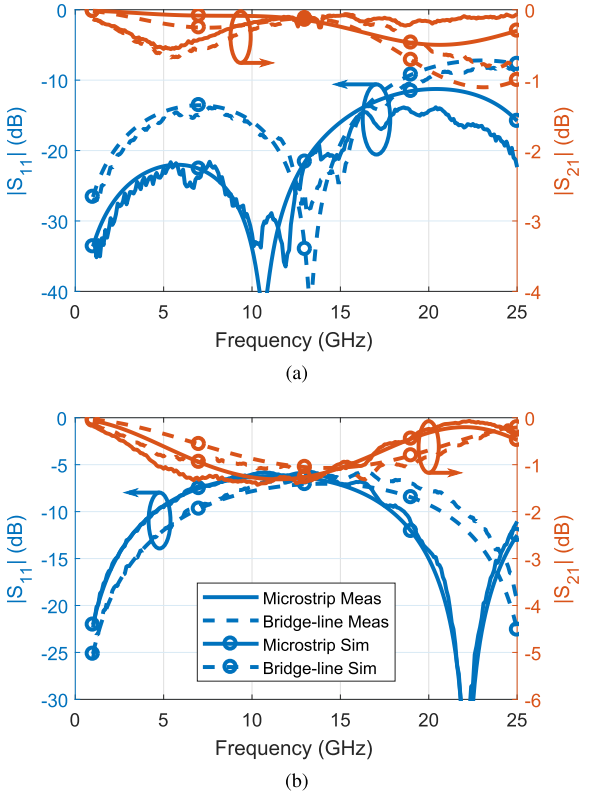


Fig. 14. S-parameter magnitudes of (a) 43-Ω line with $W = 240$ μm for the microstrip and $W = 330$ μm for the bridge line and (b) 83-Ω line with $W = 46$ μm for the microstrip and $W = 96$ μm for the bridge line. The rest of the parameters are the same as in Fig. 10. The measurements are calibrated with a Cascade Microtech 101−190 C impedance standard substrate and the launchers and interconnects are deembedded.

Simulations also show that higher order and transverse modes limit the maximum operating frequency and appear at about 140 GHz, which is comparable to the cutoff frequency of a microstrip line on the same substrate [21].

The periodic posts that provide structural stability also increase the capacitance per unit length of the line, thereby decreasing the characteristic impedance. For high characteristic impedances, these posts should be made as small and far apart as possible. For example, the simulated characteristic impedance of a bridge line with 254-μm-thick alumina, 3-μm BCB, 5-μm air, 5-μm gold, and line width of 330 μm decreases from 45 to 43 Ω when the posts (20-μm post length and $L = 220$ μm) are included.

The characteristic impedance, attenuation, and group delay of the bridge line as a function of frequency are plotted in Fig. 13, along with plots for microstrip lines for comparison. Dispersion is similar in both bridge lines and microstrip while the bridge lines have lower loss. The bridge-line group delay is slightly smaller because of the smaller effective permittivity.

Lines with 50- and 90-Ω characteristic impedances were designed to have respective widths of 350 and 116 μm. Due to the experimental nature of the MECA process, in this particular fabrication run, the BCB layer was omitted, resulting in a reduction of bridge height from 8 to 5 μm. As a result, the line impedances dropped from $Z_0 = 50$ to 43 Ω and from $Z_0 = 90$ to 83 Ω. These bridge lines have 12 sections with posts that are 5-μm tall. The removal of the BCB layer should not substantially affect the performance of the lines. Commercial alumina launchers (ProbePoint 0503) are included and interconnected to the bride-lines by a tapered MECA interconnect and Fig. 14 shows a comparison of the measurement and simulation results. For these simulations, the interconnects to the lines are also modeled and no BCB layer is used.

IV. Hybrid Couplers in MECA

In this section, two types of broadband quadrature hybrids are discussed showcasing the usefulness of the MECA interconnects and bridge lines for enhancing performance of microwave components and providing extra design flexibility. Lange couplers are limited in frequency by the gap between coupled lines and the air bridge between coupled-line sections. Multi-section broadband branch-line couplers can be designed for higher frequencies, but are limited by the highest characteristic impedance [22]. Here, bridge lines fabricated in the interconnect step of MECA are used as an additional degree of freedom in the design of broadband couplers on alumina. Two X-band multi-section branch-line couplers are designed following the design procedure in [22]: one using high-impedance bridge lines and the other employing entirely conventional microstrip lines on alumina for comparison purposes. The fabricated coupler can be seen in Fig. 15, along with the measured and simulated results in Fig. 16, where the

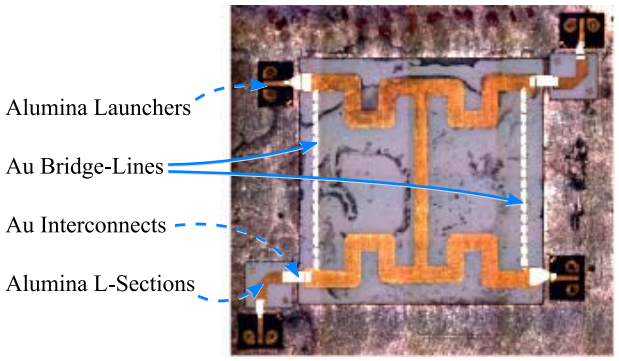
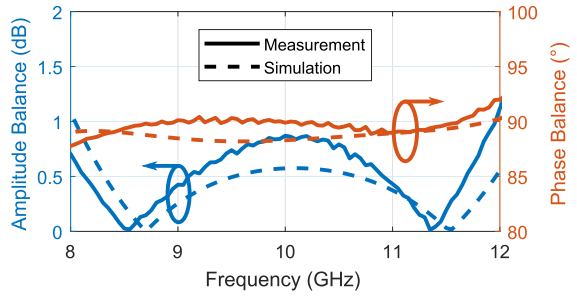
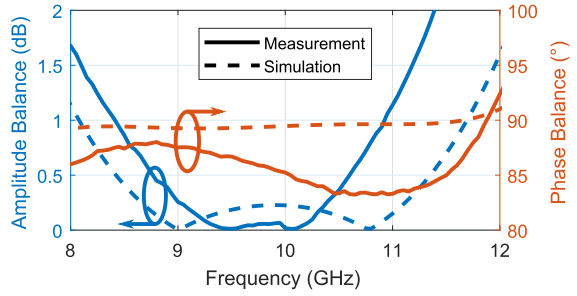


Fig. 15. Photograph of a multi-section branch-line coupler with the high impedance lines implemented using bridge lines. The total length of the coupler is 5 mm. The launchers are alumina ProbePoint 0503. Alumina L-sections were used to enable 4-port on wafer probing of the coupler, and these are deembedded in all the shown measurements.



(a)



(b)

Fig. 16. Multi-section branch-line coupler measurements for (a) coupler fully implemented in microstrip and (b) coupler with high-impedance lines implemented as bridge lines.

TABLE II

MEASURED BANDWIDTH, RETURN LOSS (RL), INSERTION LOSS (IL), AND ISOLATION (I) OF THE BRANCH-GUIDE COUPLERS. THE BANDWIDTH IS THE RANGE IN WHICH THE AMPLITUDE BALANCE IS LESS THAN 1 dB

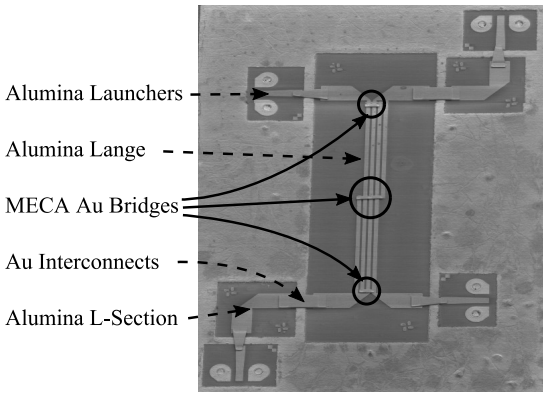
Coupler	f_L (GHz)	f_H (GHz)	RL (dB)	IL (dB)	I (dB)
Regular	7.8	12.0	18	0.2	18.8
Bridge-Line	8.4	10.9	15	1.4	17.4

amplitude and phase balances are calculated as

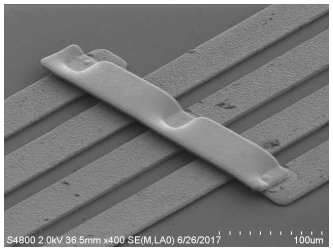
$$|\Delta|S|| = ||S_{31}| - |S_{21}|| \tag{5}$$

$$\Delta\phi = \angle S_{31} - \angle S_{21}. \tag{6}$$

Table II summarizes their characteristics.



(a)



(b)

Fig. 17. (a) Photograph of the fabricated Lange coupler after [14] (total length 5 mm). (b) Zoomed-in view of bridge. The launchers are alumina ProbePoint 0503. Alumina L-sections were used to enable 4-port on wafer probing of the coupler, and these are deembedded in all the shown measurements.

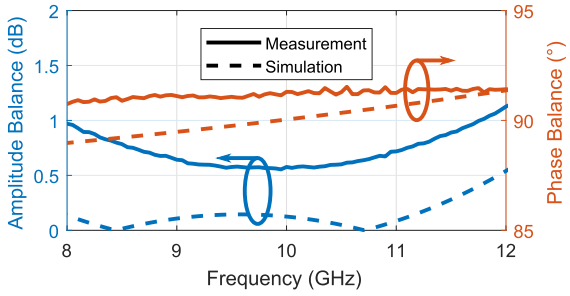
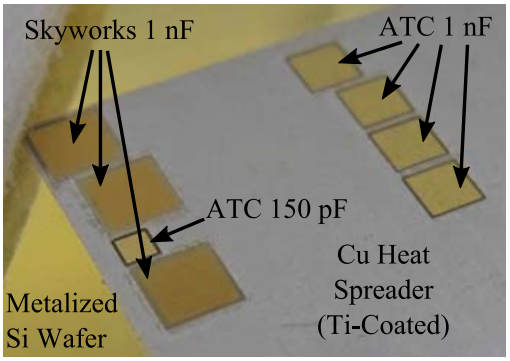


Fig. 18. Lange coupler measurement results after [14]. RL = 22.5 dB, IL = 0.5 dB, and I = 24.6 dB.

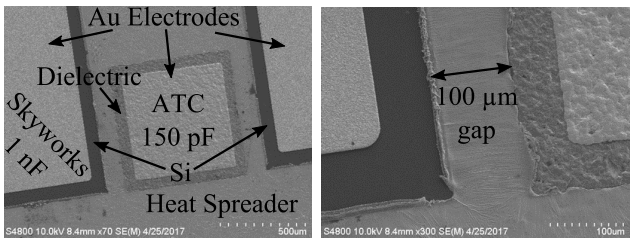
Another straightforward way to take advantage of the interconnect layer in the heterogeneous integration process is to use it for bridges in Lange couplers. The fabricated Lange coupler can be seen in Fig. 17 with measured results shown in Fig. 18. The coupler has a frequency range from 7.9 to 11.8 GHz over which the amplitude balance is less than 1 dB and the phase balance is within 90.7° and 91.5°. The insertion loss is 0.5 dB, and return loss and isolation are both greater than 22.5 and 24.6 dB, respectively.

V. MMIC PA INTEGRATION

Off-chip capacitors are required in many circuits, e.g., in stabilization networks and bias lines of PAs. High dielectric constant capacitors can be integrated as off-chip capacitors using MECA. The top capacitor electrode is recessed from the edge while the bottom electrode is directly in contact with



(a)



(b) (c)

Fig. 19. (a) Photograph showing the Skyworks 1-nF MIS capacitors (SC99906068), ATC ceramic 150-pF capacitor (118FGA151M100TT), and ATC ceramic 1-nF capacitor (118JL102M100TT) integrated in the MECA process. (b) Zoomed-in view of the ATC 150-pF capacitor showing the recessed electrodes and the dielectric. (c) Zoomed-in view of the gap between the capacitors.

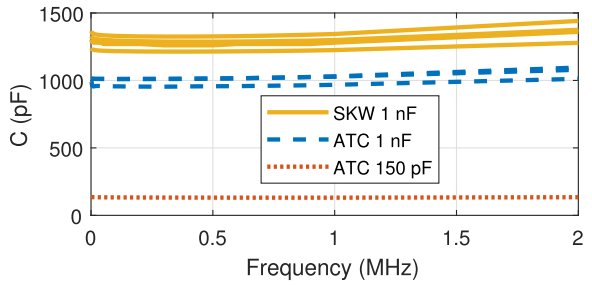
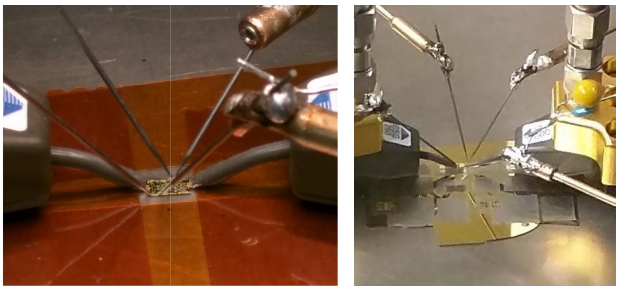


Fig. 20. Low-frequency measurements for the capacitors shown in Fig. 19(a).

the heat spreader. Skyworks 1-nF low profile silicon metal–insulator–semiconductor (MIS) capacitors and ATC ceramic 150- and 1000-pF capacitors were integrated, as shown in Fig. 19. The MECA integrated capacitors were characterized at low frequency using an LCR meter (1–2000 kHz). For measurements, the capacitors were probed from the top and through the heat spreader. All three capacitor designs perform as expected and the results can be seen in Fig. 20, confirming that the MECA process is compatible with high dielectric constant ceramic and silicon-based MIS capacitors.

A two-stage GaN PA MMIC [23] designed in Qorvo's 150-nm GaN on SiC process is used to test the MECA processing. This chip operates at the X-band (10 GHz) and has a gain of 25 dB and peak PAE of 45%. The chip was characterized prior to going through the MECA process to determine the effects of processing and improved thermal operating conditions on MMIC performance. Fig. 21 shows the photographs of the setup used to measure the MMIC before and after heterogeneous integration. In both the cases,



(a) (b)

Fig. 21. Photographs of the MMIC measurement setups. (a) Before MECA. (b) After MECA.

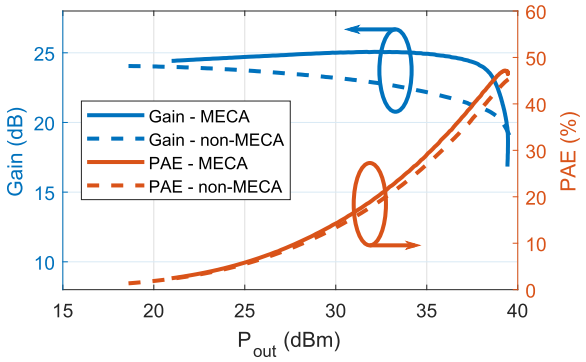


Fig. 22. Gain and PAE comparison for a GaN PA MMIC before and after heterogeneous integration.

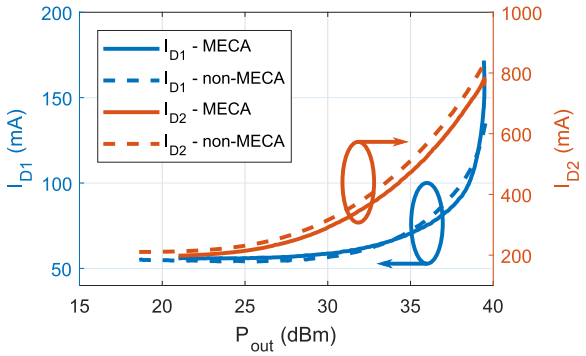


Fig. 23. Driven drain currents for both stages of the GaN PA MMIC before and after heterogeneous integration.

the thermal contact to the ground of the die is made using vacuum on a Cascade Microtech Summit 9000TM probe station. A PNA E8364C microwave network analyzer was used with an automated high power measurement setup based on [24], example B. The MMICs are probed using Cascade Microtech ACP50 probes with 250-μm pitch and tungsten dc probes for biasing. Off-chip capacitors are also added to the setup to provide low-frequency stability for the amplifiers. Additionally, a bare-die MMIC was measured alongside the MECA die to validate the measurement setup repeatability.

Fig. 22 shows the gain and PAE comparison for the MMIC before and after being metal embedded. Improvement in gain as well as in efficiency can be seen due to the improved thermal environment. Gain and PAE are improved by up to 3 dB and 3.2 percentage points, respectively. Fig. 23 shows

the driven drain currents for both stages of the MMIC PA, showing a reduction in dc power consumption, which leads to the increased efficiency.

VI. Conclusion

In this paper, we demonstrate the benefits of the MECA heterogeneous integration technique for multi-chip modules. Specifically, we show measurements on integrated alumina passives, surface mount capacitors, and GaN MMICs connected with a unique interconnect network fabricated as the last step of the MECA process. The interconnect layer is shown to provide additional degrees of freedom for the design of microwave components.

Since MECA interconnects are photolithographically defined, their shape can be precisely controlled to provide enhanced return loss and transmission. The flexibility of interconnect shape enables integration of MMICs that are designed to be wire bonded, such as the ones demonstrated in this paper. Full-wave simulations show that they can be easily designed to outperform wire bonds over a broad frequency range (10 to 100 GHz). MECA interconnects are additionally useful as bridges within a single circuit such as a Lange coupler, demonstrated here on alumina at the X-band.

The interconnect layer can also be used to implement transmission lines, referred to as bridge lines, with reduced loss and higher possible characteristic impedances compared to microstrip. A multi-section branch-line coupler incorporating bridge lines of the interconnect layer combined with microstrip on alumina is implemented and characterized to demonstrate the additional design capabilities. A similar approach can be applied to a wide range of microwave components, such as filters, couplers, hybrids, matching networks, and so on.

The benefits of the MECA interconnects come at no added cost for heterogeneously integrated RF front end modules using the MECA process. In this paper, we show integration of PAs, couplers, capacitors, and launchers in the metal embedded process. The improvement of thermal performance of PAs is shown by increased gain and efficiency for an X-band GaN MMIC. For MMICs designed with wire-bond interconnects, we show that these can also be integrated in the MECA process with improved wire-bond performance allowing higher frequency operation. The current process is well suited for III–V chip integration with CMOS control chips with a 10-μm-wide 10-μm spaced interconnect process. For digital applications, a more advanced multi-layer and higher resolution interconnect process is required.

In summary, the interconnect layer of the MECA process gives additional design parameters that can improve performance and footprint of passive components necessary in RF front ends while the intimate thermal contact of MECA improves the performance of the active circuitry. The components designed and measured in this paper can directly be used to implement a more complex circuit, e.g., an X-band balanced amplifier.

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