Broadband Microwave Integrated Circuits for Voltage Standard Applications

by

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Broadband Microwave Integrated Circuits for Voltage Standard Applications

Thesis directed by Professor Zoya Popović

Abstract

This thesis addresses integrated circuit component, packaging, and microwave design for both AC and DC Josephson voltage standard (JVS) systems. The components developed in this work combine techniques from both the distributed and lumped-element microwave design in the frequency range 0–40 GHz. The National Institute of Standards and Technology (NIST) JVS systems rely on 10 000 to 300 000 micro-fabricated Josephson junctions (JJs) in superconducting niobium on a silicon substrate at 4 K. This work focuses on both monolithically integrating specialized microwave devices with this JJ fabrication technology as well as enhancing the microwave performance of other system components.

Improved microwave packages for JVS circuits developed in this work have increased operating margins, reliability, and longevity of both AC and DC JVS systems. Monolithically-integrated, broadband, lumped-element dividers with bandwidth exceeding 15–22 GHz were designed and fabricated to uniformly distribute power to arrays of Josephson junctions, an enabling technology for the NIST 10 V programmable JVS system. Monolithic-microwave-integrated-circuit (MMIC) bias-tees, corners, JJ arrays, and terminations have all been redesigned in this work to improve JVS system operations. To deliver the microwave excitation to the JJs a broadband, MMIC, distributed amplifier was designed and tested with 3–18 GHz bandwidth. These increases in the bandwidth and microwave power on-chip have paved the way for enhanced current and future NIST JVS systems.

Dedication

To people, places, and things to come.

Personal

Acknowledgments

I would like to thank my family for instilling in me a sense of adventure, and the confidence that anything can be accomplished.

To the current and former students in the microwave research group, a sincere thanks for all the advice, technical help, camping trips, and nights away from school: Dr. Patrick Bell, Dr. Alan Brannon, Dr. Jason Breitbarth, Dr. Michael Buck, Jonathan Chisum, Evan Cullens, Dr. Charles Dietlein, Dr. Negar Ehsan, Erez Falkenstein, Dr. John Hoversten, Dr. Miloš Janković, Nicola Kinzie, Dr. Néstor López, Dr. Hung Loui, Dr. Milan Lukić, Joseph Mruk, Dr. Qianli Mu, John O'Brien, Dr. Mabel Ramírez, Michael Roberg , Dr. Sébastien Rondineau, Luke Sankey, Robert Scheeler, Dr. Aaron Scher, Jason Shin, Dr. Kenneth Vanhille, Christi Walsh, and Dr. Narisi Wang.

Professional

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Dr. Paul Dresselhaus and Dr. Samuel Benz have been instrumental in not only motivating and overseeing this work, but also in providing an environment where gaining knowledge through experimentation reigns supreme. Dr. Paul Dresselhaus, Norm Bergren and Dr. David Olaya have enabled this work by spending countless hours in the NIST Quantum Device Fabrication facility building the many test chips this thesis relies upon. The other members of the NIST Quantum Electrical Metrology team have also played key roles in completing this thesis, among them: Dr. Burm Baek, Charlie Burroughs, Mary Filla, Dr. Clark Hamilton, Dr. Oliver Kieler, Alessio Pollarolo, Dr. Dave Rudman, Dr. Alain Rüfenacht, Maureen Teichman, and Steve Waltman. To them, and all my other NIST colleagues over the years, I extend my deepest gratitudes.

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of electrical engineering. I would not be here today without outstanding professors like yourselves willing to pass knowledge on to the next generation.

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Chapter 1

Introduction

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1.1 Scope of This Thesis

This thesis discusses the design, implementation, and characterization of broadband 0–40 GHz components utilized in National Institute of Standards and Technology (NIST) Josephson voltage standard (JVS) systems. Fundamentally, a JVS uses a Josephson junction (JJ) to convert quantized photon energies into quantized voltages through the Josephson constant, $K_{J-90} = 483.5979\,\mathrm{GHz/mV}$ [1]. These micro-fabricated superconducting JJs necessitate cryogenic operation, primarily at 4 K, the temperature of liquid helium. This superconducting cryogenic integrated circuit environment presents the designer with both unique challenges and unique opportunities.

System, package, and circuit level designs for the improvement of JVS systems will be explored in this work. First, Chapter 1 presents an overview of Josephson junction and JVS technology, along with a brief outline of this thesis. In Chapter 2 a significantly improved packaging solution for NIST JVS chips is presented. Chapters 3, 4, and 5 present microwave circuit solutions to JVS challenges. Among these are broadband, low-loss, lumped-element power-dividers; a broadband, lumped-element directional-coupler; a lumped-element diplexer; and a selection of process and device characterization circuits. In Chapter 6 a broadband monolithic microwave integrated circuit (MMIC) GaAs distributed amplifier is designed, fabricated, and tested for use in the microwave excitation of JVS systems. Chapter 7 discusses initial experiments and challenging future work in implementing the next generation of JVS systems. Finally, this work will close with the latest results from the NIST prototype 10 V programmable JVS (PJVS) system, enabled by the work described in this thesis, and a summary of the contributions of this work in Chapter 8.

This introductory chapter will start with a brief overview of superconducting physics and the governing principles of Josephson junction. Next, a quick outline of Josephson junction technologies, and the NIST Quantum Voltage JJ integrated circuit fabrication process will be presented. Finally, past and present JVS systems will be described to motivate the remainder of this thesis.

1.2 Introduction to Superconductors

The superconducting phenomenon was discovered in 1911 when Heike Kamerlingh Onnes found that the resistance of mercury goes to zero when cooled to 4.2 K in his concurrent innovation, liquefied helium [2], together winning him a 1913 Nobel Prize in Physics. This discovery opened a new field in low temperature superconductors (LTS). It was subsequently experimentally verified that as the temperature approaches absolute zero the resistance goes to zero for many metals, at a material dependent critical temperature T_C [3, 4]. This experimentally determined T_C varies between 0.1 K and 10 K for most elemental superconductors. Mercury (Hg), lead (Pb), tin (Sn), and niobium (Nb) are commonly used LTS elements. High temperature superconductors (HTS), typically exotic compound ceramics, have been discovered more recently with critical temperatures between 60 K and 125 K (in the 77 K liquid nitrogen range). One of the more common Yttrium based ceramics exhibiting the HTS phenomenon is $YBa_2Cu_3O_7$ (YBCO) with $T_C = 93\,\mathrm{K}$ [4]. While HTS devices are more difficult to fabricate than LTS devices, the abundance and low cost of liquid nitrogen makes HTS a more attractive technology for large scale production, e.g. in cell phone base station applications [5].

Many models of the superconducting phenomena have arisen over the years. Among the most useful are the Ginzburg-Landau model [6], with a macroscopic phenomenological approach, and the Barden, Cooper and Schrieffer (BCS) theory [7], which examines the microscopic viewpoint. The Ginzburg-Landau model is a two fluid model, modeling superconducting properties over temperature and magnetic field utilizing two interacting fluids of superconducting and normal electrons respectively. The BCS theory, winning a 1972 Nobel Prize in Physics, is built upon the formation of Cooper pairs of electrons. At extremely low temperatures where the thermal vibration of the atomic lattice (phonon energy in quantum mechanics) is very low, the attractive force of a negatively charged free electron is sufficient to slightly deform the surrounding positive lattice. This lattice deformation makes a potential well which traps a second electron in close proximity to the first.

The superconducting superfluid, comprised of Cooper pairs of interacting electrons, has a lower potential energy than either the normal fluid of free unpaired electrons or the phonon vibration energy of the lattice. This gives the Cooper-pair superfluid a free path through the lattice, leading to the zero DC resistance property of superconductors [4]. Tests of DC currents impressed in superconducting rings have been run for many years with no decay in the current magnitude. Strictly, a superconducting line is lossless only at DC, but they are very low loss in the microwave regime exhibiting $10^{-}4$ lower resistivity than coper at 10 GHz [8]. As such, a superconducting line is typical modeled in this work as a perfect electric conductor (PEC).

1.3 Introduction to Josephson Junctions

In 1962, Brian Josephson, then a graduate student at Cambridge, postulated the existence of a superconducting-normal material-superconducting junction through which a DC current could flow in the absence of an electric field [9]. This DC Josephson effect produces a DC current proportional to the difference between the Cooper-pair superfluid wave function phases, θ_2 and θ_1, across the junction. This current, I, can be expressed through the DC Josephson relation:

$$I = I_C \sin(\theta_2 - \theta_1) \tag{1.1}$$

where I_C is the critical current [3]. The JJ parameter I_C is the maximum current at which the voltage across the JJ remains 0 V with no external excitation. This discovery won Josephson the Nobel Prize in Physics in 1973.

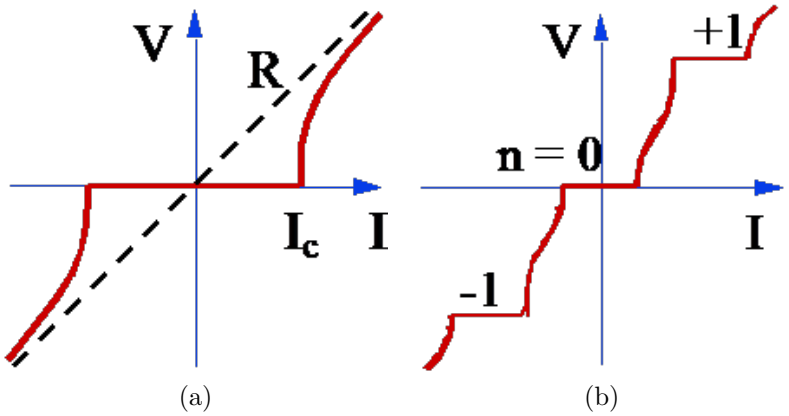
Further, Josephson predicted that if a DC bias voltage was applied while the Josephson current passed through the junction it would be generate a microwave current through the JJ. By applying a DC voltage, V, across the junction, a potential energy difference between the superfluid wave functions arises across the JJ causing a linear increase in phase with respect to time. This change in phase causes the junction current to oscillate in accordance with the AC Josephson equation [4]:

$$\frac{\partial \phi}{\partial t} = \frac{2e^{-}}{h} V \tag{1.2}$$

where $\phi = \theta_2 - \theta_1$. Likewise, the inverse is true, a junction under microwave current excitation at given frequency, f, will have a quantized DC voltage across the barrier through the relation $f = \frac{2e^-}{h}V$ from Equation 1.2. This direct relation between frequency and voltage based on only fundamental constants is termed the AC Josephson relation, where $K_J = \frac{2e^-}{h}$ is the Josephson constant. Evaluated, this expression gives the relation between the microwave current oscillation and the DC voltage as K_{J-90} =483.5979 GHz/mV by international convention in 1990 on the values of the fundamental constants e^- and h based on historically averaged measured values [1]. This AC Josephson effect is the basis of many of the useful applications of Josephson junctions, including the JVS systems supported by this thesis.

From basic physics [3], the energy transfered by a microwave current over time is quantized into photons with energy $E = hf$. Fundamentally, it is the coupling of this hf quantized photon energy packet with the $2e^-$ cooper pair to form a flux quantum, $\Phi_0 = h/2e^-$, that yields the quantized potential increase V. From a circuit design stand point, the JJ can be interpreted as a typical nonlinear element and characterized in a similar manner. By varying the thickness and composition of the JJ barrier a range of characteristics can be designed, from weakly superconducting, to fully insulating. In the NIST QV IC process, discussed in detail in Section 1.4.1, the barrier is adjusted to produce superconductor—normal-metal—superconductor (SNS) JJs with a small normal-metal resistance shunting the JJ.

Figure 1.1 a is a sketch of the voltage across a typical NIST QV SNS JJ as a function of the DC current through the junction without microwave excitation. When biased past the critical current I_C, the IV characteristic asymptotically approaches the normal state resistance R_n. The junction properties I_C and R_n can be designed with appropriate choices of JJ geometry (area) and materials (barrier and electrodes). The product of these values (scaled by K_J) is called the JJ characteristic frequency $f_c = I_C \cdot R_n \cdot K_J$; the JJ is most responsive to microwave excitations near f_c. In Fig 1.1 b a microwave current excitation near f_c is applied to the junction showing the flat voltage steps in the IV characteristic known as Shapiro steps. The n^{th} Shapiro step refers to the number flux quanta per cycle of the microwave excitation, i.e. the number of hf



(a) (b)

Figure 1.1: (a) JJ IV curve with DC bias only, governed by Equation 1.1. (b) JJ IV curve with DC bias and external excitation near the JJ characteristic frequency f_c, governed by Equation 1.2.

photon energies to reach the quantized voltage of the step. Figure 1.1 b shows the -1, 0 and $+1$ Shapiro steps, where a negative Shapiro step is achieved by reversing the DC bias current direction and hence the polarity of the potential difference across the junction.

1.4 JJ Applications and Fabrication

Since its first realization in 1963 by Shapiro [10], the JJ has become the primary active device in superconducting electronics. The JJ has many applications in a broad range of fields. JJ parasitic nonlinear inductances have been used to tune high-Q superconducting filters [11]. The AC Josephson effect has been harnessed in everything from high precision microwave oscillators [12] and millimeter wave detectors [13], to precise superconducting quantum interference device (SQUID) magnetometers and amplifiers [14, 15] and voltage references [1]. There are also several logic families incorporating Josephson junctions able to achieve computing clock rates of up to 750GHz [4]. In the last few years JJ fabrication technologies have matured, enabling the production of very large scale JJ integrated circuits, for example a direct digitizing receiver at L-band with sample rates in excess of 30 GHz was recently demonstrated [16].

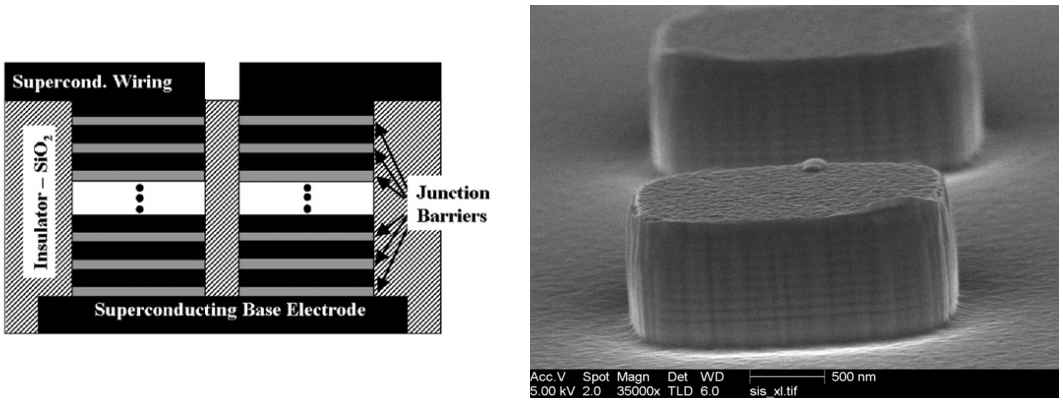
Modern Josephson junction fabrication technology is a specialized spin off of standard silicon integrated circuit fabrication. Tools and methods from planar silicon processing have been adapted to JJ circuits. Most LTS applications, including single photon detectors, SQUIDs,

superconducting logic, microwave oscillators, variable inductors, and voltage metrology, utilize a deposition technology where the base electrode, barrier, and top electrode (e.g. superconductor—insulator—superconductor (SIS): 170nm Nb - 10nm AlO_x - 170nm Nb) are all deposited and then patterned simultaneously. This creates a self-aligned junction with contact layers above and below. Applications like JVSs that require large numbers of JJs generally utilize a stacked multilayer topology with several junctions stacked vertically and simultaneously patterned. The JJ technology, SIS or SNS, and performance parameters, I_C, R_n, etc, are typically adjusted based on the specific junction application [1, 11, 12, 13, 14, 15, 16].

1.4.1 JJ Fabrication Technology at NIST Boulder

In this work a NIST SNS JJ integrated circuit (IC) process optimized for JVS applications at the Boulder quantum device fabrication facility is used [17]. The Quantum Voltage (QV) group at NIST uses a Nb_xSi_{1-x} JJ barrier that can be adjusted during deposition from insulating performance to normal-metallic performance by adjusting the ratio of niobium to silicon [18]. This allows for an additional degree of freedom in junction design over traditional fixed-barrier-composition JJ processes in which only the thickness of the barrier and area of the JJ can be varied to achieve the desired performance. For JVS applications x is set to achieve normal-metal JJ characteristics. A cross sectional diagram of a NIST SNS Josephson junction stack is shown in Fig. 1.2 a, and a SEM image of two stacks of 10 JJs is shown in Fig. 1.2 b.

In order to interconnect JJs and build useful microwave structures, the NIST IC process also includes two superconducting niobium wiring layers, an interlayer SiO_2 dielectric, and a resistor layer. The NIST QV IC fabrication process layer stack is shown in Table 1.1. This process begins with a 380 µm bare silicon wafer with approximately 150 nm of native SiO_2 oxide. At 4 K essentially all of the carriers in the silicon freeze out, and it becomes a cheap, flat, high-dielectric-constant, low-loss substrate [19]. For large JVS junction arrays, trenches are etched in the native oxide to improve JJ heat-sinking to the silicon chip by thermally anchoring the Nb1 base electrode. Niobium is sputter deposited 300 nm thick for the Nb1 base electrode



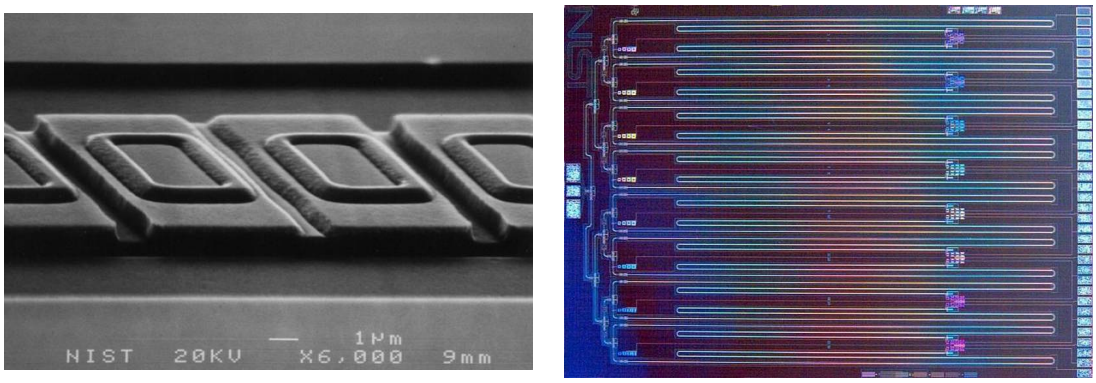
(a) (b)

Figure 1.2: (a) A cross-section diagram of two JJ stacks wired in series for JVS applications [1]. (b) A NIST SEM image of two stacks of 10 JJ each before the deposition of insulating oxide and superconducting wiring layers.

Table 1.1: NIST Quantum Voltage IC fabrication process layer stack.

Layer name	**Material**	**h [µm]**	**Properties**
Passivation	SiO_2	0.30	$\epsilon_r = 4.5$
Resistor	AuPd	0.12	$\sigma = 4\,\mathrm{E}^6\,\mho/\mathrm{m}$
Nb2 Wiring	Nb	0.60	∼PEC
MIM oxide	SiO_2	0.35	$\epsilon_r = 4.5$
JJ counter electrode	Nb	0.06	JJ tri-layer:
JJ barrier	Nb_xSi_{1-x}	0.03	adjusted
JJ middle electrode	Nb	0.06	to define
JJ barrier	Nb_xSi_{1-x}	0.03	performance
Nb1 base electrode	niobium	0.30	∼PEC
Native Oxide	SiO_2	0.15	$\epsilon_r = 4.5$
Substrate	Si	380	$\epsilon_r = 11.5$

layer. Next, the JJ multi-layer is sputtered in situ with the junction barrier deposition adjusted for the desired thickness and composition. The entire multi-layer is patterned and dry-etched in a single step with the Nb1 base electrode serving as a stop point to define the JJ stacks. The Nb1 base electrode interconnect is then patterned with a positive photo resist and dry-etched. 350 nm of SiO_2 is sputtered to insulate the JJs and form an interlayer dielectric with vias etched in this dielectric to contact the JJs and the base electrode. The Nb2 wiring layer, 600 nm, is then



(a) (b)

Figure 1.3: (a) A close-up SEM image of of two JJ stacks wired in series in the center conductor of a CPW transmission in a JVS array, a cross section of which is illustrated in Fig. 1.2 a. (b) A micrograph of a state-of-the-art 12 mm × 17 mm PJVS chip with on-chip 16-way power division, Chapter 3, to 16 arrays of 15 600 JJs each.

sputter deposited over the top, filling the via holes and providing a large suppercurrent carrying capacity for interconnects. For pad bonding surfaces and on-chip resistors, 120 nm thick AuPd is patterned by first applying the mask, deposition of AuPd, and then lifting off the undesired areas with acetone. Finally, another thin layer of SiO_2 is sputtered to serve as passivation to protect the IC. Figure 1.3 a is a SEM image of a section of the center conductor of a co-planar waveguide (CPW) transmission line loaded with JJs, while Fig. 1.3 b is a micrograph of a 10 V JVS chip with 16 arrays and 268 800 JJs.

Minimum line widths and spacings are 1 μm for all layers. The NIST QV IC process generates resistors of $\sim 2\,\Omega/\square$, metal-insulator-metal (MIM) capacitors of $\sim 0.1\,\mathrm{fF}/\mu\mathrm{m}^2$, and under-passed spiral inductors in the range of 100–7000 pH. These high Q elements offer the circuit designer many advantages over distributed circuit topologies in the same technology. Lumped $\lambda/4$ Π sections with L_s and C_p integrated into 50 Ω CPW with a center conductor width of 16 μm and gap of 8 μm can be realized in a 130 μm length of CPW with very little penalty in loss, as compared to 1600 μm for a distributed $\lambda/4$ transmission line at 20 GHz. These unique advantages, largely due to cryogenic operation, will be further explored in Chapters 3, 4, and 5.

1.5 Josephson Voltage Metrology

The international system of units (SI) volt is defined in relation to current and power: "The volt is that electromotive force between two points on a conductor carrying a constant current of 1 ampere when the power dissipated between the two points is 1 watt," [20]. Unfortunately this physical relation is very difficult to experimentally realize with an uncertainty of less than about 1 part in 10^6; this level of reproducibility is insufficient for the demands of modern electronic systems. As discussed in Section 1.3, the inverse AC Josephson effect offers an intrinsic relation between voltage and frequency: K_{J-90} =483.5979 GHz/mV depending only on the fundamental constants e^- and h. Frequency standards with stability on the order of 1 part in 10^{12} or 10^{13} are commercially available, while the NIST-F1 atomic clock is stable to 1 part in 10^{15}. Because it depends only on fundamental constants, rather than physical artifacts, the Josephson volt is said to be an *intrinsic standard*. For JVSs the AC Josephson Equation 1.2 is applied in the form of $V = Nnf/K_{J-90}$, where N is the number of JJs, n is the Shapiro step number, and f is the microwave excitation frequency.

The Josephson voltage standard is a device used to realize the SI volt (uncertainty 0.4 in 10^6) through K_{J-90} at a precise, repeatable, agreed-upon value by international convention in 1990 [21]. The Josephson voltage standards presently in use by national standards organizations around the world agree to 1 in 10^9, compared to a uniformity of about 1 in 10^6 possible with the previous technology, stabilized and calibrated Weston cells (a specialized type of chemical batteries) [1]. Figure 1.4 shows a historical progression of voltage standards, note the huge decrease in uncertainty with the invention of the JVS in the early 1970s, and again in the 1980s with the advent of arrays of JJs.

The earliest systems designed to harness the Josephson effect were initially intended to improve the measurement of the fundamental constants e^- and h [22, 23]. It quickly became obvious that the uncertainty of the SI volt and the stability of Weston cells were insufficient for this task, but that the system could be reversed and be used to vastly improve the stability of the realization of the volt [24, 25]. Early JVSs utilized a single junction or a handful of

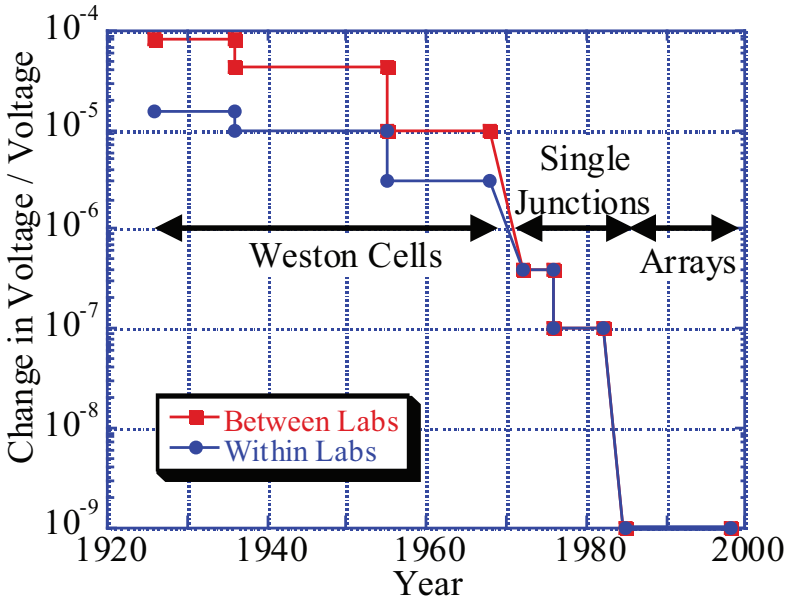


Figure 1.4: A plot of the historical level of agreement between volt standards at various national standards laboratories [1].

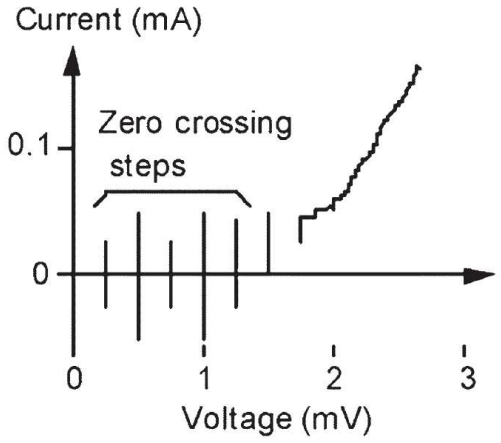
independently current biased junctions in series because early fabrication technology could not produce junctions with tight enough parameter targeting to have overlapping IV characteristics. These systems were only capable of generating very small voltages on the order of a few millivolts, but nonetheless revolutionized the measurement of the volt [26].

Advances in JJ technology in the 1980s brought about the Conventional Josephson Voltage Standard (CJVS) utilizing arrays of hysteric JJs to generate output voltages of 1–10 V [27]. In the 1990s, breakthroughs in superconducting integrated circuit processing, utilizing technology developed in the semiconductor industry and in the quest for a Josephson computer, finally allowed modern large arrays of non-hysteretic JJs to be built with sufficient uniformity to be globally current biased. In modern non-hysteretic junctions, there is functional relation of the voltage across the junction for every bias current value, hence the IV characteristic is said to be single valued. These fabrication advances paved the way for the modern Programmable Josephson Voltage Standard (PJVS) [28] and the arbitrary waveform generating AC Josephson Voltage Standard (acJVS) [29].

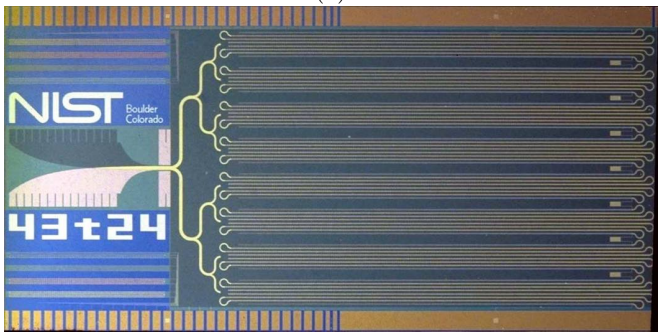
1.5.1 Conventional Josephson Voltage Standards

The CJVS was the first JVS with practical output voltages on the order of volts. The enabling technology for the conventional JVS was the 1977 Levinsen discovery of hysteretic JJs [30] with stable operating points only on quantized voltage steps, as shown in the IV curve in Fig 1.5 a. These zero-current-crossing voltage-steps allowed the junction uniformity problem to be circumvented by biasing the array at, or near, zero DC current. The drawback of this solution is that while the output voltage of a CJVS is precisely quantized, it is impossible to set the output voltage to a desired value. Further, in CJVS systems a given combination of DC current bias and microwave excitation does not uniquely determine the output voltage so system noise can cause spontaneous transitions in the step number n and hence the output voltage. Nonetheless, by the end of the 1980s 10 V CJVS systems were developed and deployed to over 50 standards laboratories around the world [31, 32, 33]. The CJVS was the first large scale superconducting integrated circuit to be widely adopted [1].

CJVS systems typically operate in lower W-band, 70–96 GHz. While this affords advantages in requiring fewer JJs to achieve a given voltage, it also places severe constraints on the system due to the availability, cost, and complexity of millimeter-wave components. Figure 1.5 b shows a CJVS chip, and Fig. 1.5 c is a block diagram of a typical CJVS system. A 75 GHz Gunn-diode oscillator provides microwave excitation to the CJVS chip through ∼1 m of over-moded circular waveguide in a cryoprobe to reach 4 K at the bottom of a liquid helium dewar. The bias voltage and current are computer controlled through a four-wire measurement system, and an additional pair of wires are brought out of the cryoprobe for the output voltage once the bias procedure is complete. Because the array only operates very near zero-current, only very high-impedance loads are acceptable on the CJVS voltage output. The biasing and measurement procedure with a CJVS, while effective, is slow and painstaking, requiring the skills of a trained metrologist. Readers interested in the detailed operation of CJVS systems are referred to the JVS technology review article by Benz [1]. These CJVS systems are still the dominant primary voltage standard



(a)



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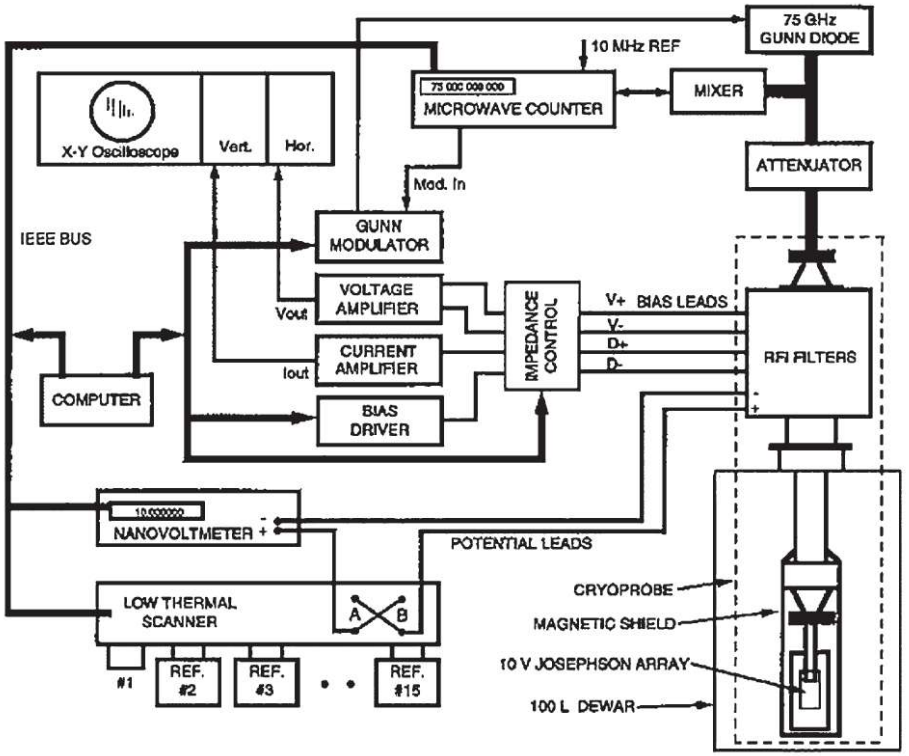
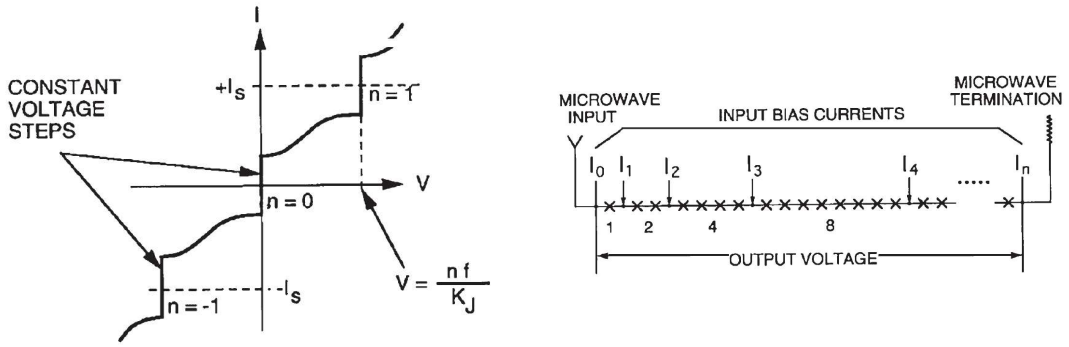


(c)

Figure 1.5: (a) A sketch of a typical CJVS JJ hysteretic IV characteristic [1] (b) A micrograph of a NIST 20 208 JJ 10 V CJVS chip circa 1992. (c) A block diagram of the CJVS measurement system [1].



(a) (b)

Figure 1.6: (a) A diagram showing a PJVS non-hysteretic junction IV characteristic [1]. (b) A simplified schematic of the PJVS binary array structure [1].

used around the world to calibrate secondary standards, e.g. Zener references, and precision digital voltmeters.

1.5.2 Programmable Josephson Voltage Standards

The shortcomings of the CJVS systems highlight the need for a JVS more adaptable to quickly setting a desired output voltage, and with a higher output drive current. These requirements lead to the development of modern PJVS systems capable of quickly and easily calibrating modern precision digital volt meters (DVMs), digital-to-analog converters (DACs), and analog-to-digital converters (ADCs) [28]. PJVS systems use lithographically uniform non-hysteretic JJs with single valued IV curves so that many junctions can be collectively current biased and all have a stable operating point on the same constant voltage Shapiro step, usually +1, 0, or -1 as shown in Fig 1.6 a. The junctions are arranged in arrays with binary, or trinary, numbers of junctions in each sub-array with separate current biases, as shown in Fig 1.6 b. This allows the total PJVS voltage to be programmed by switching the current bias point of each sub-array to the desired constant voltage step and taking the series combined sum of the sub-array voltages.

The enabling technologies for PJVS systems are modern lithography and fabrication techniques. In JVS system the voltage summation of many single JJ IV curves yields the array IV performance. To implement a PJVS system, large arrays of several thousand junctions have to have parameters

that only vary by a few percent across the silicon wafer, as well as a similarly uniform microwave excitation [34, 35, 36, 37]. The barrier thickness and area of many thousands of JJs can be very tightly controlled using planar IC techniques such that the constant voltage steps, shown in Fig. 1.6, of all the junctions are aligned over a large range of bias current, typically greater than 1 mA, when the JJs are collectively current biased and excited with microwaves. When evaluated across the entire array, the $n = 0$ step suppression below I_C indicates the maximum single JJ microwave excitation, and $n = |1|$ step current height indicates microwave excitation uniformity across all the JJs in the array. This large bias current range for quantized voltage operation, referred to as bias margin, allows PJVS systems to drive much larger loads and significantly improves the tolerance for noise as compared to CJVS systems.

This lithographic JJ uniformity allows PJVS systems to integrate more junctions on chip than CJVS systems, and thus PJVS systems often operate with lower microwave excitation frequencies, around 20 GHz. The lower excitation frequency provides significant advantages in cost and complexity of microwave components, but at the same time places new area constraints on the on-chip component designs. On-chip power dividers, bias structures, and other components all need to be designed for minimal area and maximum microwave power delivered to the very large junction arrays comprising a total of 268 800 JJs in the latest NIST 10 V prototype PJVS chip shown in Fig. 1.3 b [38].

Figure 1.7 shows a block diagram of a typical PJVS system. Efforts in recent years have concentrated on increasing the reliability, usability, and output voltage of PJVS systems. Components of this system optimized in this thesis are highlighted and will be discussed in depth in the chapters to come. The end goal of current NIST PJVS research efforts, with major contributions from this thesis, is to produce a NIST "turn-key" 10 V PJVS system. The completed system will be able to set and verify all of its various bias and excitation parameters such that a user untrained in cryogenics and JVS technology can obtain any desired output voltage or stepwise approximation at the push of a button.

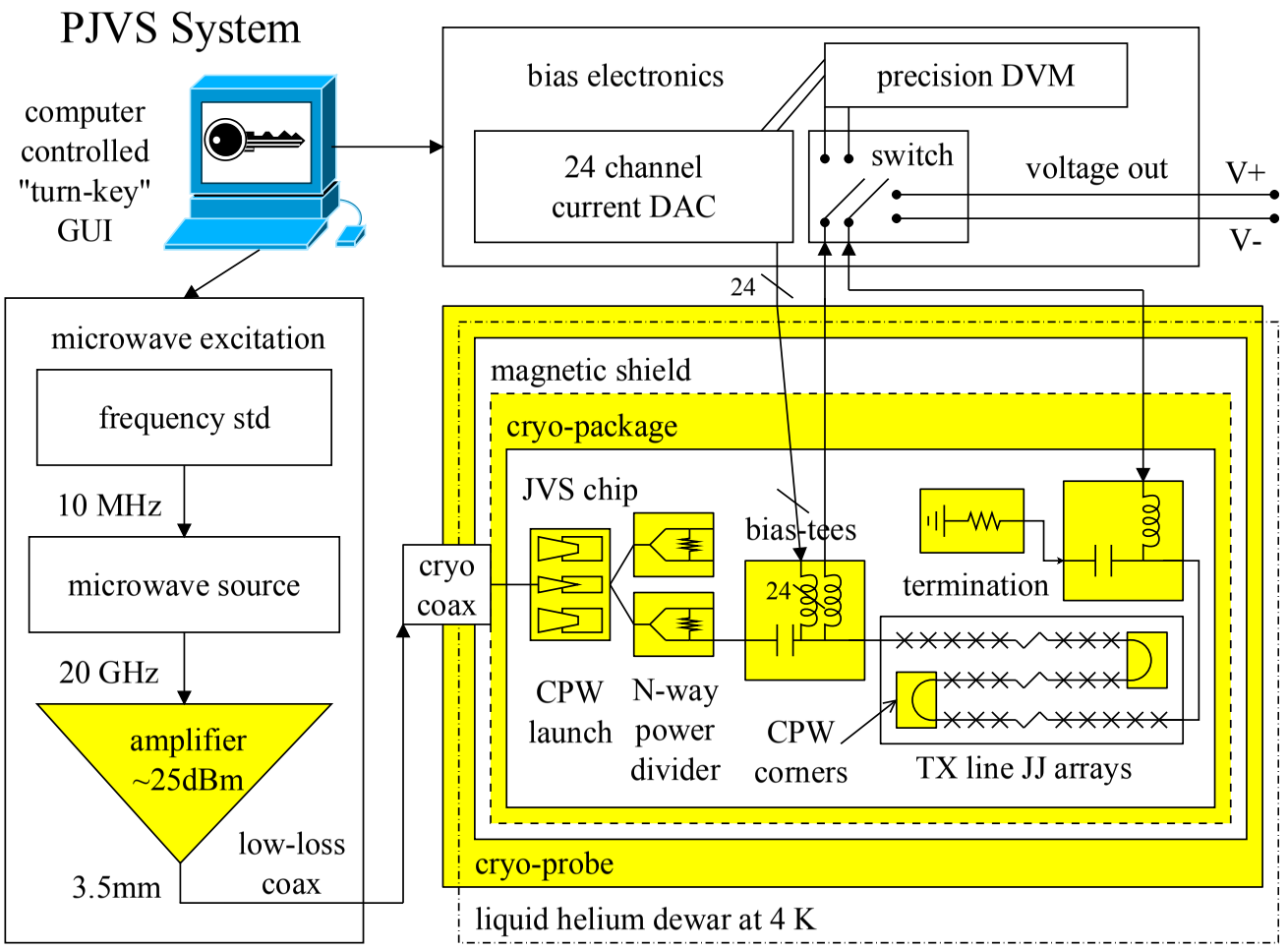


Figure 1.7: A simplified block diagram of the "turn-key" 10 V PJVS system under development at NIST. A frequency standard with stability better than 1 part in 10^9 is required for PJVS operation; many commercial microwave sources are sufficiently stable, or for precision measurements a GPS time receiver or cesium standard can be used. The blocks highlighted in yellow will be treated in detail in this thesis.

The character of the JJ as a fundamental frequency to voltage converter presents many challenging microwave design tasks. While the PJVS system operates under CW microwave excitation, a broad tuning range of the CW signal is desired to allow sub-least-significant-bit (LSB) frequency tuning of the output voltage, as well as have a large degree of flexibility so the system can adapt to a variety of JJ characteristics without having to revisit the microwave design. For the PJVS component designs presented in Chapters 3, 4, and 5 a bandwidth of 15–22 GHz is considered the band of interest. Every component in the microwave excitation chain needs to operate consistently over this band with minimal reflection and loss to provide maximum flexibility to the JJ array designer.

PJVS systems with ±2.5 V output are in the field at standards laboratories around the world [39], and 10 V PJVS systems are on the cusp of the transition from research to field use [40, 41, 42, 43, 44]. The functional dependence of output voltage on bias current allows simple control schemes and fast settling times on the order of tens of nanoseconds in PJVS systems [45]. Stepwise approximated arbitrary waveforms can be generated with PJVS systems, but the voltage and timing uncertainty in the transition regions between the quantized steps presently limits their metrogolical utility to signals at 1 kHz and below [45, 46, 47].

1.5.3 AC Josephson Voltage Standards

In order to synthesize waveforms with quantum accuracy at higher speeds, a different approach is needed. CJVS and PJVS systems program the output voltage by changing n, the Shapiro step number, and N, the number of junctions, respectively, but a third option in $V = Nnf/K_{J-90}$ exists: changing the frequency. This can be a useful technique in CW excited PJVS system to achieve sub-LSB tuning; unfortunately, as the CW excitation frequency gets much lower or much higher than the JJ characteristic frequency, f_c, the bias current margins degrade rapidly [48]. Instead, the acJVS system is excited by a train of high speed current pulses such that each non-zero bit of the excitation code produces one flux quantum per junction. The time domain voltage across the pulse excited junction has a quantized area in volt-seconds, or alternatively an integer

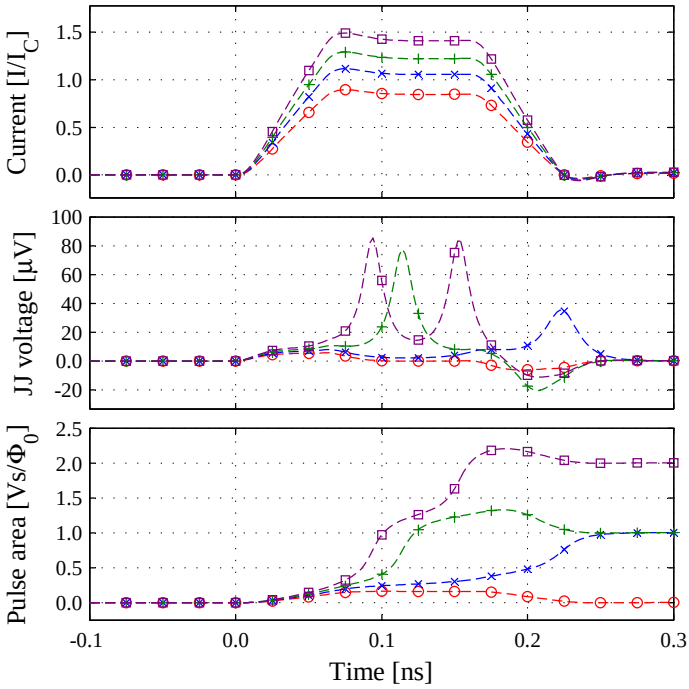
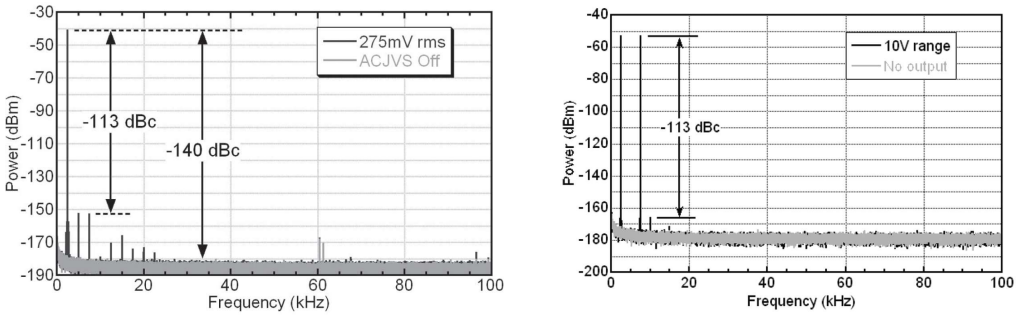


Figure 1.8: Simulated current pulse excitation of a typical JVS junction ($I_C = 10\,\text{mA}$, $R_n = 3\,\text{m}\Omega$) showing voltage pulse quantization. (top) Applied time domain current pulse excitation. (center) Output voltage across the JJ. (bottom) Integrated voltage pulse area. The $0.9\,I_C$ pulse in red is insufficient to yield a net voltage pulse. The $1.1\,I_C$ pulse in blue results in a minimum voltage pulse. The $1.3\,I_C$ current pulse in green results in a large voltage pulse with significant overshoot and recovery. The $1.5\,I_C$ current pulse in purple results in two voltage pulses, i.e. two flux quanta tunneling across the barrier. The JJ quantizes the analog current pulses to an $n\Phi_0$ voltage pulse area where the number of flux quanta is an integer n: -1, 0, 1, 2, etc.

number of flux quanta tunneling across the JJ barrier from Equation 1.2. This pulse quantization is simulated in Fig. 1.8 for various current pulse excitation amplitudes [49]. These quantized fluxes can then be integrated in time with a low-pass filter to achieve quantum-accurate-voltage arbitrary-waveform synthesis. Further, because the shape and duration of each individual pulse determines the quantized output, the repetition rate of single pulses can be arbitrarily varied without loss of bias current margins [48]. A tri-state $\Delta\Sigma$ code can be used to produce both positive and negative quantized pulses [50].

In practice the acJVS system operates as a massively oversampled $\Delta\Sigma$ pulse-density modulator with a 10 Gbps bit-stream being used to generate signals in the audio frequency range. In order to produce trinary pulses with a commercial two-level bit-stream-generator, the $\Delta\Sigma$ bit-stream



(a) (b)

Figure 1.9: (a) A measurement of a single quantum pure 275mV$_{\text{rms}}$ tone from the NIST acJVS system [51]. (b) A demonstration of acJVS arbitrary waveform generating capability, a −113 dBc two tone measurement [52].

is combined with an amplitude and phase matched CW microwave source at 15 GHz, 3/2 the ΔΣ clock frequency. The quantum voltage accuracy and an oversampling rate on the order of a million allows the acJVS system to produce arbitrary waveforms of unmatched purity [53]. Figure 1.9 a shows a recent acJVS measurement of a 275mV$_{\text{rms}}$ sine wave at 2.5 kHz with -113 dBc spectral purity [51], while Fig. 1.9 b shows a two-tone 70mV$_{\text{rms}}$synthesized waveform at 2.5 kHz and 7.5 kHz also with better than -113 dBc linearity [52]. The very stringent performance specifications of this system, shown schematically in Fig. 1.10 and in use in Fig. 1.11 a, present unique challenges to the circuit designer. All the components in the microwave ΔΣ-bit-stream excitation chain need to be very broadband and low-dispersion from a few megahertz to 30 GHz, while simultaneously keeping all the components in the analog output chain distortion-free to -113 dBc. An advanced cryogenic packaging solution that enabled permanent acJVS chip mounting, as well as microwave circuits for future acJVS applications will be discussed in the coming chapters.

1.5.4 JVS Packaging

The PJVS and acJVS chips have a very harsh packaging environment. The JVS chip is only cryogenically cooled when a secondary standard is calibrated so the package must withstand

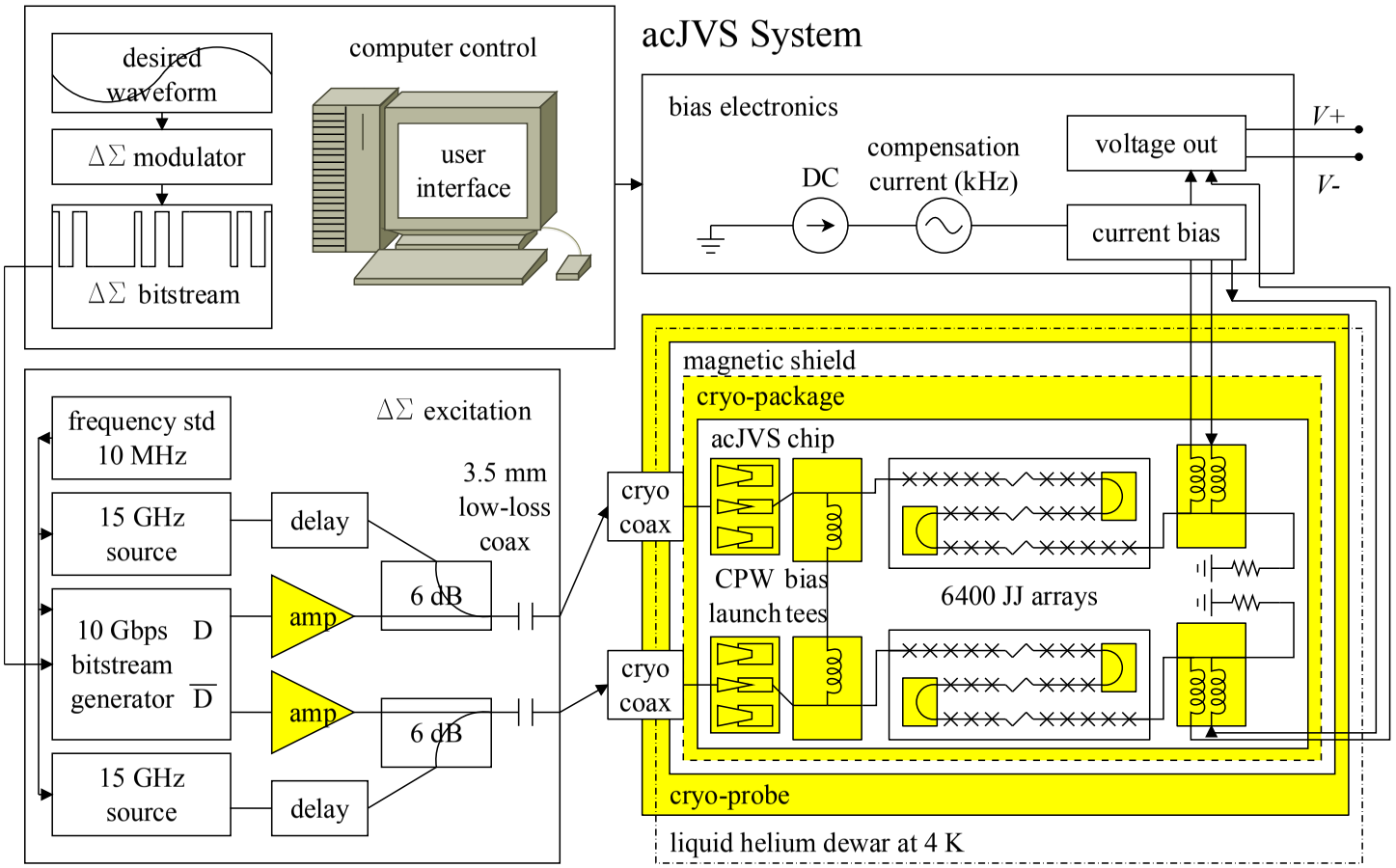
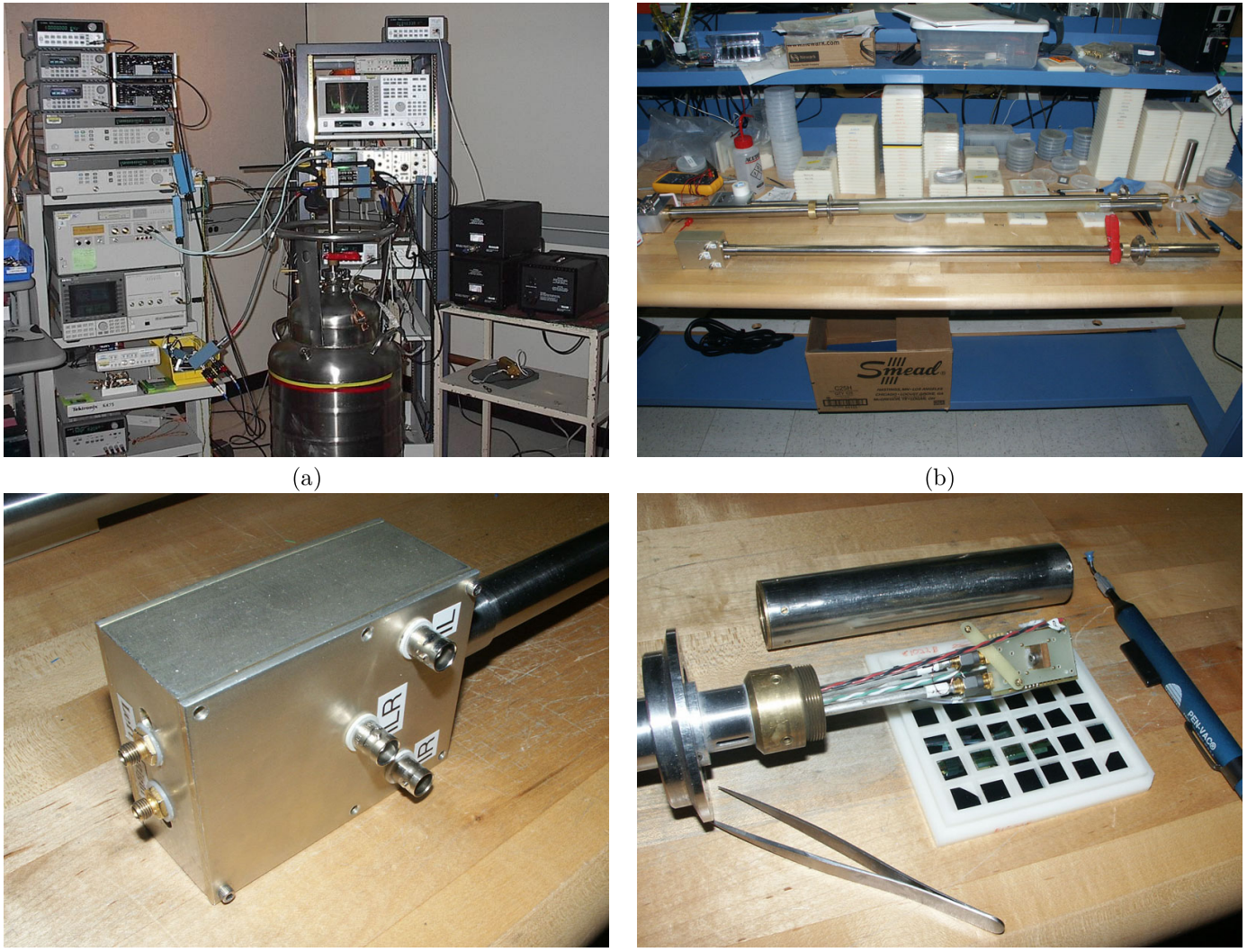


Figure 1.10: A simplified block diagram of the state-of-the-art 275 $\mathrm{mV_{rms}}$ acJVS system. A frequency standard with stability better than 1 part in 10^9 is required for acJVS operation, many commercial microwave sources are sufficiently stable provided all of the components are synchronized to a single source.



(a) (b)

(c) (d)

Figure 1.11: (a) The NIST acJVS system, Fig. 1.10, with cryoprobe at 4 K in a He dewar, (b) NIST acJVS cryoprobe, (c) A close-up photo of the probe head with microwave and analog input/output ports, and (d) a close-up photo of the cold-stage and a spring-finger JVS package.

many 4–300 K cycles, as well as be magnetically shielded, have multiple DC I/O connections, and have broadband 30 GHz microwave excitation ports.

The present solution to these packaging issues is a cryoprobe, as shown schematically in Figs. 1.7 and 1.10. This 1 m stainless steel tube encases two Astroflex Cobraflex cryogenic coaxial cables and multiple DC wires for immersion in liquid helium in a storage dewar. The cryogenic cables are specifically designed with a crimp corrugated outer conductor to captivate the dielectric and maintain mechanical alignment of the shield, dielectric, and conductor over many thermal cycles. Precision 3.5 mm connectors are used at the room-temperature end for electrical repeatability, and SMA connectors are used at the 4 K end for mechanical stability. The DC and analog frequency connections are made with fine gauge twisted pair wires for low thermal losses.

For permanent mounting in JVS systems, the chip is flip-chip bonded to a flexible polytetrafluoroethylene (PTFE) substrate to help alleviate thermal stresses from the package, as discussed in Chapter 2. This flexible substrate is then mounted with 26 GHz precision SMA connectors and soldered to fine twisted-pair DC wires for the output voltage and DC bias currents. The connecting wires and microwave coax are inserted in a magnetic shield at the end of the cryoprobe [54]. Chapter 2 will be an in-depth treatment of microwave improvements to the flip-chip package. Figure 1.11 is a pictorial tour of the the complete NIST acJVS cryogenic system with the JVS chip at 4 K in the liquid He dewar, Fig. 1.11 a, the cryoprobe, Fig. 1.11 b, and the room temperature probe head, Fig. 1.11 c. For short-term test connections, a CuBe spring-finger on FR4 chip package is used. In this package the the chip is held against the spring-loaded contacts with a pressure screw, shown in Fig. 1.11 d.

1.6 Contributions

This chapter has given an introduction to JVS applications, fabrication, and packaging. The NIST JVS systems have been described with their various challenges. In the following chapters many of these challenges will be addressed and solutions presented, improving the performance of

the overall system. The contributions of this thesis to microwave engineering and JVS technology can be summarized as follows:

- Improved JVS packaging technology bandwidth [55], Chapter 2.
  - Enabled 300 $\mathrm{mV_{rms}}$ acJVS permanent mounting [56].
  - Enabled 20GHz 10V PJVS prototype excitation [38].
- Designed and implemented a broadband lumped-element Wilkinson divider, using both superconducting and commercial processes [57], Chapter 3.
  - Applied balanced topology to N-way dividers.
  - Devised divider/attenuator/combiner test configuration for N-way dividers.
  - Implemented 16-way and 32-way division in a working 10V PJVS system [40][1] .
- Designed and implemented broadband lumped-element symmetric-hybrid with a phase inverter [58][2] , Chapter 4.
- Performed initial experiments toward a next generation JVS systems, Chapter 7.
- Improved JJ array microwave performance for the 10V PJVS prototype [59], Chapter 8.

While not exhaustive, this list will also serve as a rough outline of the remainder of this thesis. Many of these developments are already in the field at the NIST calibration laboratory, as well as building a solid groundwork for future applications with even more stringent microwave requirements.

[1] 2009 National Conference of Standards Laboratories International (NCSLI) Best Technical Paper Award.
[2] 2009 International Microwave Symposium Best Interactive Forum Paper Award.

Chapter 2

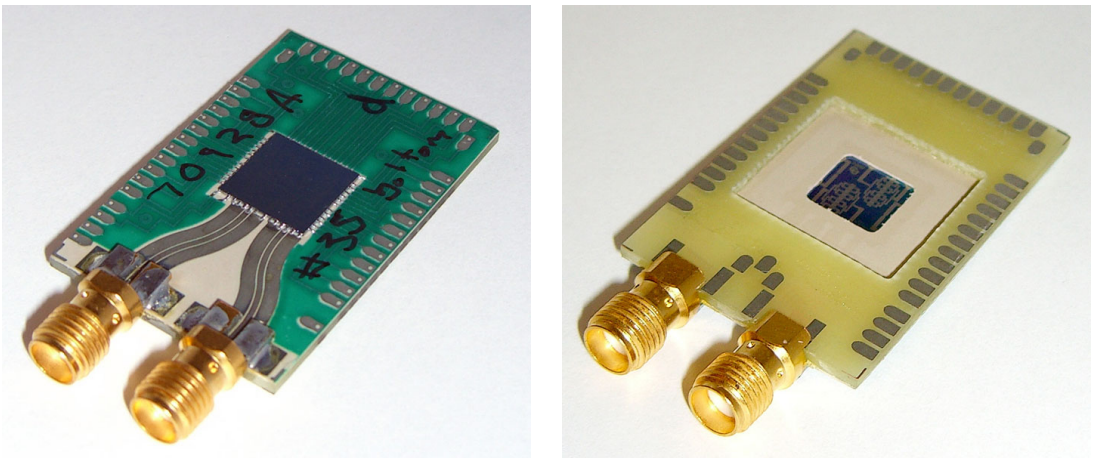
Microwave Packaging for Josephson Voltage Standards

Contents

Improved packages for Josephson Voltage Standard circuits have increased operating margins, reliability, and longevity of JVS systems [60]. By using the "flip-chip-on-flex" technique, reliable chip and cryoprobe mounting have been demonstrated. The microwave structures on these packages have been improved such that more power can be delivered to the JVS chip over a wider frequency range: DC to over 30 GHz [55]. Detailed finite-element simulations were performed to optimize the chip-to-flex launches as well as the on-flex transmission lines. It was found that coplanar waveguide transmission line designs had improved insertion and return losses compared to those of the microstrip transmission line designs, in large part due to the large discontinuities associated with through-substrate vias for microstrip ground connections. The improved coplanar-waveguide package/probe yielded insertion loss dominated by the ∼0.25 dB/GHz cable loss and VSWR better than 2:1 for the entire 0–30 GHz band. Substantially larger JVS system operating margins were measured using the coplanar-waveguide package; for a 5120 junction array a quantized voltage step with greater than 1 mA in bias current range is shown for a 10–30 GHz band.

2.1 Introduction

This chapter addresses the refinement of microwave packaging technology for a superconductive Josephson voltage standard (JVS) chip directly soldered to a flexible carrier [60]. The primary design considerations for these cryo-packages are long service life, improved microwave performance, and stable, reliable chip-to-carrier contacts. For the past 10 years [1], NIST has been designing and fabricating a variety of circuits based upon superconductor—normal-metal—superconductor Josephson junction technology including chips for programmable Josephson voltage standards, discussed in Section 1.5.2 [61, 62, 63, 38], and pulse-driven AC Josephson voltage standards, discussed in Section 1.5.3 [53, 56]. Recent efforts have been focused on increasing the bias-current operating margins and long-term reliability of these devices so that they may be used for many years in their respective applications.



(a) (b)

Figure 2.1: Photographs of the optimized flip-chip-on-flex microwave package with a microwave test structure chip mounted: (a) flex side, showing CPW microwave launches and DC bias/output lines and (b) chip side, showing chip (center), flip-chip bonded to flex (surround), and FR4 mechanical stiffener (outer).

To resolve long-term chip-contact reliability issues in previous-generation CuBe spring-finger based JVS packages, as shown in Fig. 1.11 d, a "flip-chip-on-flex" method of permanently bonding JVS chips to a flexible cryo-package was developed and discussed thoroughly in [60]. This technology utilizes InSn solder to directly attach the bond pads on the 1 cm × 1 cm JVS chip to traces on a flexible microwave substrate, hereafter referred to as "flex". This robust and repeatable structure is capable of absorbing the thermal expansion and contraction of the silicon chip when it is cycled many times between room temperature and 4 K. Building upon the previous work in [60], this work presents a redesign of the microwave aspects of the package. By use of improved components and CPW geometry optimized using full-wave simulations, the usable bandwidth of the microwave package has successfully been extended from DC to 30 GHz. An example of a JVS chip bonded to microwave-optimized flex is shown in Fig. 2.1.

The improved microwave bandwidth of this package has been an enabling technology for a 20 % improvement in the output voltage of the broadband-pulse-waveform-driven acJVS system to 275 $\mathrm{mV_{rms}}$ [53, 56]. For the PJVS systems, the extension of the operational bandwidth of the package has allowed the prototype 10 V PJVS system to operate at 20 GHz rather than 16 GHz, thus reducing the junction count by 20 % [64].

2.2 Microwave Package Design

The microwave package can be broken down into several functional blocks relating to design choices. First, there is the connector itself; low cost, broad bandwidth to greater than 20 GHz, and mechanical robustness are critical features. Next, the choice of microwave substrate determines transmission-line geometry, affects loss, and must allow enough flexibility to absorb the differential thermal expansion of the Si chip. The flex-to-chip interface must maintain mechanical stability and electrical repeatability without sacrificing microwave performance. Finally, the on-chip pad geometry must be large enough to bond repeatably, small enough to keep the I/O count high, and backwards-compatible with legacy designs at a reduced level of performance for testing purposes. All of these factors of the package must be optimized to achieve a broadband, well-matched microwave-feed to the chip.

The previous flip-chip-on-flex package used a low-cost, off-the-shelf, edge-mount SMA connector and a 50 µm-thick Cu microstrip (MS) transmission line on 250 µm-thick, Rogers RO3003$^{\text{TM}}$ [65] substrate. These standard edge-mount connectors, while providing good mechanical stability, degraded in microwave performance quickly above 16 GHz. The choice of microstrip (MS) transmission lines required the use of through-substrate vias to make the ground connections at the chip and connector. The inductance of these vias introduced several strong resonant bands at which the feed exhibited large reflections, and consequently very little microwave power was delivered to the JVS chip. The increased dispersion of microstrip transmission lines as compared to a CPW realization is also likely to be detrimental to the acJVS operating margins under 20 Gbps pulsed excitation [66]. Full-wave CPW simulations show approximately half the change in group delay between DC and 20 GHz when compared with MS simulations.

In the optimized design, CPW transmission lines were selected to eliminate the need for through-substrate vias and reduce package dispersion. The Johnson 142-0761-891 [65] precision SMA connector, optimized for fine-dimension CPW to 26.5 GHz, was identified as a good compromise between the additional expense and mounting complexity of a 3.5 mm connector and the unacceptable performance of a standard edge-mount SMA connector. To better match

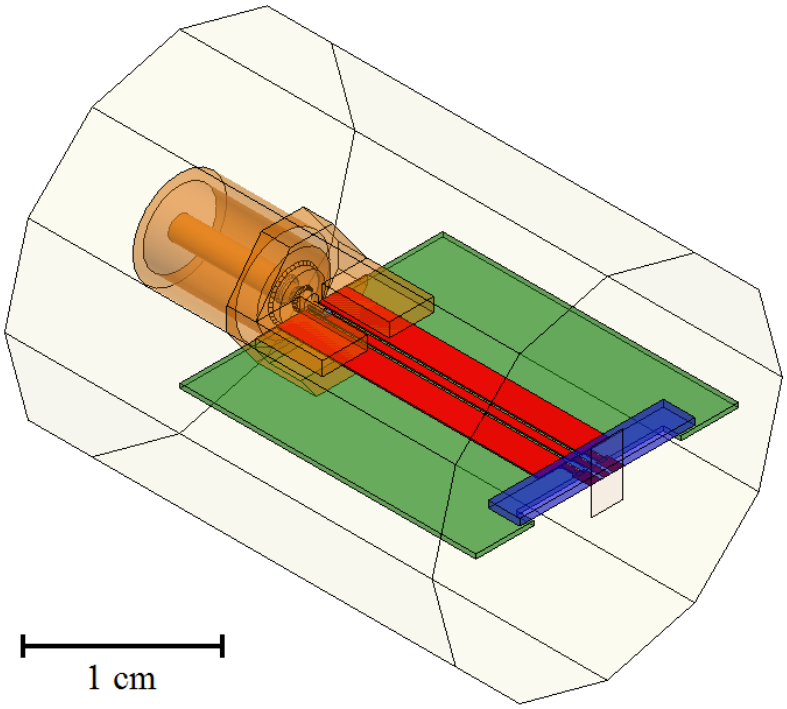


Figure 2.2: Broadband flip-chip-on-flex interface model in HFSS. From left to right, the wire-frame is the FEM domain boundary, orange is the Cu connector, white is PTFE, green is the RO3006^{TM}, red is copper traces, yellow is InSn solder, blue is the Si chip, and maroon is the Nb traces on-chip.

the flex CPW to the chip pads and the connector geometry, a higher-dielectric substrate was desired. Rogers RO3006^{TM} [65] in 250 µm thickness was chosen, trading slightly less stability of the dielectric constant over temperature for better manufacturability of 50 Ω CPW dimensions.

Initial layout geometries were obtained using canonical, closed-form CPW models, then simulated and refined as single transmission line elements of uniform-cross-section using Ansoft's HFSS [65] 3-D finite-element-method (FEM) simulator. The single-segment HFSS results were integrated in a complete HFSS simulation for final adjustments. Figure 2.2 shows the three-dimensional geometry of the flip-chip-on-flex package. Solder bump reflow was modeled to first order as a trapezoidal connection from flex-pad edge to chip-pad edge. The HFSS simulation results from the model shown in Fig. 2.2 were cascaded in a circuit simulator with ideal lossy transmission lines calculated from the HFSS port impedances to represent the 1.2 m PFTE

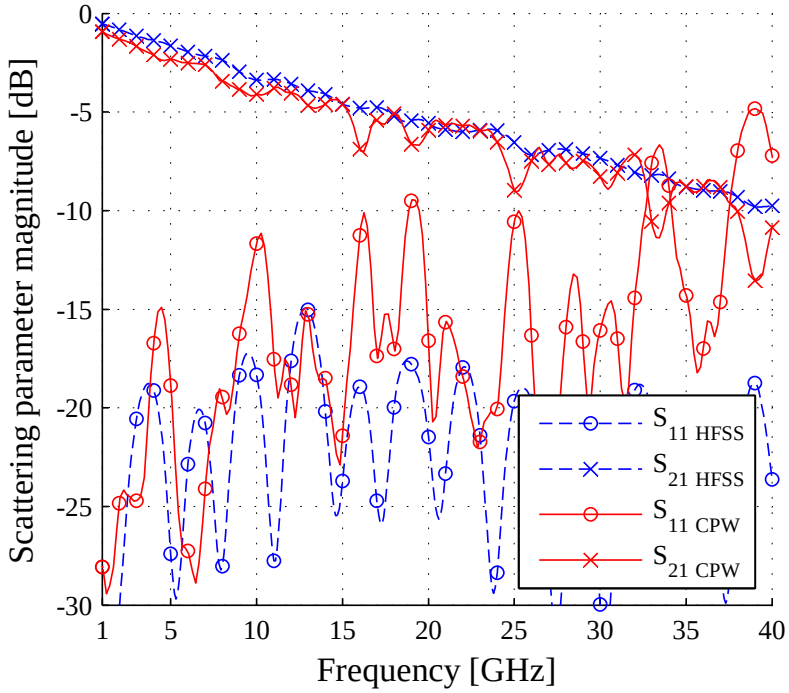


Figure 2.3: Simulated scattering (S) parameter performance of optimized CPW flex-to-chip launch, in blue dashed lines, compared to measured cryoprobe with CPW flex through line results from Section 2.3, in red solid lines.

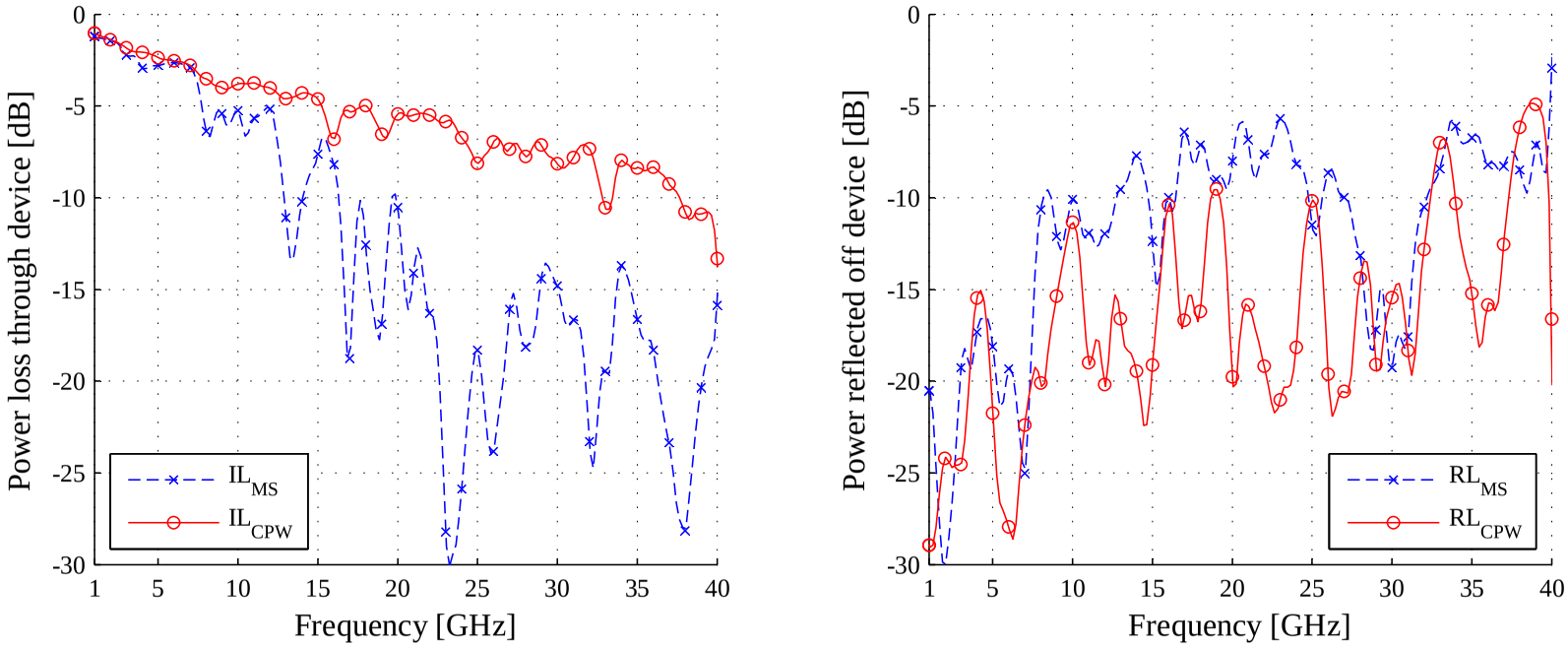
coaxial cable and the 6.4 mm on-chip transmission lines. Figure 2.3 shows the results of the circuit simulation compared with measured results discussed in Section 2.3.

2.3 Testing

In order to test the optimized package structure, 1 cm × 1 cm chips were fabricated on a Si wafer with a through-connected, 50 Ω, 6.4 mm long, superconducting Nb CPW transmission line between two optimized microwave launches. These were flip-chip-bonded to the optimized flex carrier using the process described in [60]. For comparison, identical through-line chips were packaged using the legacy MS flex design. These packaged chips were installed in a 1.2 m cryoprobe utilizing 3.58 mm semi-rigid coaxial cable with solid PTFE dielectric, copper conductors, and SMA connectors to reach the bottom of a liquid helium dewar at 4 K.

Measurements were performed with an Agilent 8722ES [65] vector network analyzer (VNA). The calibration reference plane was set at the room-temperature end of the cryoprobe using an Agilent 85052C [65] Short—Open—Load—Through (SOLT) calibration kit. Figures 2.4 a and b show a comparison by package of the measured cryoprobe insertion loss, IL, (power lost through the device) and return loss, RL, (power reflected off of the device), respectively. The optimized CPW flex has all but eliminated the power dropouts that plagued the MS flex design at 13, 17, 19, and 21 GHz, and above 22 GHz. These lossy bands prevented the acJVS system from working in the MS package with 5000 or more JJs. The dominant slope of the through IL versus frequency measurement corresponds to the measured frequency-dependent loss of the PTFE cables. Neglecting this slope, the CPW flex has no dropouts larger than -3 dB from DC to 30 GHz. The entire CPW cryoprobe system is matched to better than 2:1 VSWR over the entire 0–30 GHz bandwidth. In time domain reflectometry (TDR) measurements of these test structures the dominant source of reflections is the solder joint between the connector center pin and the package. In later work the connector to connector repeatability of this joint has been improved by using metered solder paste reflow to form this joint as opposed to hand soldering, as well as further optimization from full wave simulations.

A figure of merit for the power and uniformity of the microwave excitation of the Josephson junction array is the range of DC bias current for which the JJ Shapiro DC voltage steps are quantized. This DC bias range, or current margin, is measured with a DC IV sweep under microwave excitation, as shown in Fig. 1.1. The suppression of the zero-voltage step below I_C (11.5 mA for these chips) is an indication of the microwave current through any one junction. A quantized $n = |1|$ step over a larger bias current range is an indication of better microwave current uniformity through the entire array. A larger bias current range on a step makes the JVS system more immune to noise and allows it to source or sink more current in a measurement while remaining quantized, defining the operating margins of the system. For acJVS systems the JJ array needs to respond in a uniform manner over the broad bandwidth of the 10 Gb/s pulsed $\Delta\Sigma$ excitation waveform [56].



(a) (b)

Figure 2.4: (a) Measured cryoprobe IL, using room-temperature SOLT calibration, of MS legacy flex package in blue dashed lines, and CPW optimized flex package in red solid lines. (b) Measured cryoprobe RL, using room-temperature SOLT calibration, of MS legacy flex package in blue dashed lines, and CPW-optimized flex package in red solid lines.

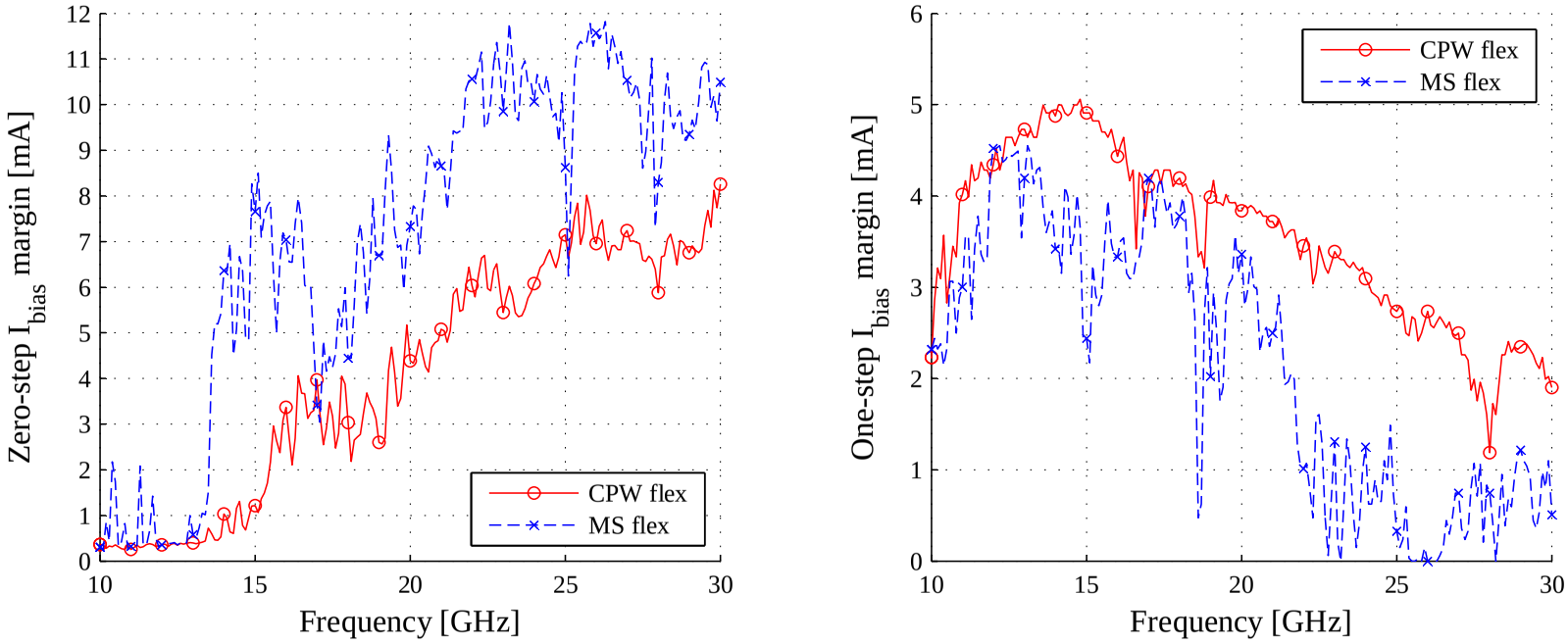
Table 2.1: Piecewise linear power sweep functions. Source output power is the command waveform in the leveled synthesizer range. Approximate on-chip power is calculated by applying measured system gain to the sweeper output power function.

Frequency	**10 GHz**	**15 GHz**	**20 GHz**	**25 GHz**	**30 GHz**
Source Output Power	–13.0 dBm	–10.0 dBm	–10.0 dBm	–10.0 dBm	–8.0 dBm
Approximate On-chip Power	10.0 dBm	12.5 dBm	11.0 dBm	10.5 dBm	9.0 dBm

In order to evaluate real array performance, two pre-screened, identical 5120-JJ array acJVS chips were mounted using the CPW and MS flex mounts, then evaluated for current margin versus frequency. The microwave excitation power was monotonically ramped over frequency to maximize the one-step on the CPW flex chip mount, compensating for amplifier gain, cable loss, and junction response. The piecewise-linear power ramp frequency corner points are shown in Table 2.1. The MS flex chip data sets are taken using the same power ramp for a direct comparison with the improved CPW flex. Figures 2.5 a and b show the resultant zero-step and one-step current margins, respectively. Consistently improved bias current margins over the entire band are shown with the CPW flex mounted chip. The 19 GHz and 28 GHz resonant dropouts in the one-step and zero-step using both packages are the second and third resonance of the array length on chip. The 90 MHz standing wave apparent in this finer sweep is due to resonant length of the 1.2 m cryoprobe coax. When tested in the acJVS system under pulsed excitation, the MS packaged chip exhibited 1.4 mA of bias current margin while the CPW packaged chip had more than double the bias current margin with a 3.0 mA range of quantized output voltage for a 5120-JJ array.

2.4 Summary

The CPW flex is a considerable enhancement to the legacy MS flex design, especially above 16 GHz, where insertion and return losses are improved by nearly an order of magnitude, providing substantially more microwave power on-chip. Access to 0–30 GHz bandwidth of the CPW flex has enabled permanent flex-mounting of acJVS chips. The limited bandwidth, large reflections,



(a) (b)

Figure 2.5: (a) Measured zero-step current bias magnitude of 5120-JJ arrays on two identical acJVS chips mounted in different "flip-chip-on-flex" packages. Zero-step suppression below I_C of 11.5 mA is an indication of absolute microwave power reaching any one junction in the array. (b) Measured one-step current bias magnitude of 5120-JJ arrays on two identical acJVS chips mounted in different "flip-chip-on-flex" packages. A larger one-step magnitude is an indication of better microwave power uniformity across all the junctions in the array. The improved CPW package data set is shown in red solid lines marked with ∘; the legacy MS package data set is shown in blue dashed lines marked with ×.

and lossy dropouts of the legacy MS package did not provide adequate pulse-waveform power levels on chip to operate the 5120-JJ array acJVS system.

Very broadband, mechanically robust microwave packaging technology for JVS applications has been demonstrated. This packaging technology using precision SMA microwave connectors, CPW transmission lines on a low-loss microwave substrate, and flip-chip-on-flex bonding technology exhibits improved microwave performance from DC to above 30 GHz. The reliability and performance gains of these packages over legacy designs are an enabling technology for NIST acJVS and 10 V PJVS systems. Future improvements may be realized by tackling the reliability, standing-wave, and loss challenges in the cryoprobe. A cryoprobe design incorporating precision 3.5 mm connectors, Cobraflex [65] captivated dielectric cables, and a spring finger package designed with lessons learned in this investigation is under construction for the next generation of JVS systems at NIST.

Chapter 3

Lumped-Element N-way Wilkinson Power Dividers for Voltage Standards

Contents

This chapter presents a monolithically-integrated, broadband, lumped-element, Wilkinson power divider centered at 20 GHz which was designed and fabricated to uniformly distribute power to arrays of Josephson junctions for superconducting voltage standards. The goal of this work is to utilize a monolithically integrated sixteen-way power divider to excite ∼250 000 junctions at 20 GHz for a 10 V programmable Josephson voltage standard [40]. This solution achieves a 4-fold decrease in chip area, and a 2-fold increase in bandwidth when compared to the previous narrow-band, distributed circuit. A single Wilkinson divider demonstrates 0.4 dB maximum insertion loss, a 10 dB match bandwidth of 10–24.5 GHz, and a 10 dB isolation bandwidth of 13–30 GHz. A 16-way, 4-level, binary, Wilkinson power divider network is characterized in a divider/attenuator/combiner back-to-back measurement configuration with a 10 dB match bandwidth from 10–25 GHz. In the 15–22 GHz band of interest, the maximum insertion loss for the sixteen-way divider network is 0.5 dB, with an average of 0.2 dB. The amplitude balance of the divider at 15, 19, and 22 GHz is measured to be ±1.0 dB utilizing 16 arrays of 15 600 Josephson junctions as on-chip power detectors [57].

3.1 Introduction

The superconducting niobium used for the junctions gives the IC designer the advantage of creating complex low-loss circuits using integrated superconducting CPW transmission lines, high-quality inductors, and very low series resistance capacitors [67]. This enables broadband, lumped-element, Wilkinson power dividers with very low loss, compact size, and broad bandwidth compared to commercial and published dividers in CMOS, stripline, and other technologies [68, 69, 70, 71, 72, 73].

This chapter begins with the design of a lumped-element Wilkinson divider unit cell, followed by a discussion of layout and fabrication, and then cryogenic measurement results are shown from 10–30 GHz. Next, a 4-level, binary, balanced divider utilizing these unit cells was designed to meet the challenge of increasing the number of junction arrays under parallel microwave excitation on a JVS chip. Cryogenic measurements are performed on the sixteen-way Wilkinson

divider in a back-to-back divider/10 dB-attenuator/combiner configuration. This configuration preserves the desired matched-load, N-way divider in a 2-port through test circuit suitable for insertion loss measurements. A prototype 10 V programmable Josephson voltage standard is also built and utilized as an on-chip power detector to evaluate the amplitude balance of the divider. Finally, the unit cell is successfully implemented in TriQuint's commercial TQPED [65] process at room temperature with a modest penalty in area and loss.

3.2 Broadband Lumped Element CPW Wilkinson

A Wilkinson power divider is a three-port microwave circuit optimized for power division [74]. Three-port circuits are fundamentally limited in that they can not be simultaneously lossless, matched, and reciprocal [75]. The Wilkinson divider is a reciprocal, matched device that adds loss in such a way that the three-port is only lossy in the reverse direction, as an out-of-phase combiner. The divider is not lossy provided no current flows through the 100 Ω Wilkinson isolation resistor between the two output ports, shown in a broadband Cohn divider configuration [76] in Fig. 3.1 a. Hence if the circuit is excited at port 1 as a divider, or as a in-phase combiner with phase and amplitude matched signals at ports 2 and 3, it behaves as if it were lossless, matched, and reciprocal.

A lumped-element Wilkinson power divider can be synthesized by replacing the typical physical $\lambda/4$ sections of transmission line with lumped-element equivalent Π networks [77]. This lumped-element topology allows a 10-fold reduction in physical length for this application. The availability of superconducting planar spiral inductors allows multiple lumped-element $\lambda/4$ equivalent sections in a broadband Butterworth configuration [68, 76, 78, 75, 79]. The two-section Wilkinson power divider, shown in Fig. 3.1 c, incurs a negligible penalty in loss and a very modest 30 % increase in area for approximately double the bandwidth compared to that of a single-section lumped-element Wilkinson divider.

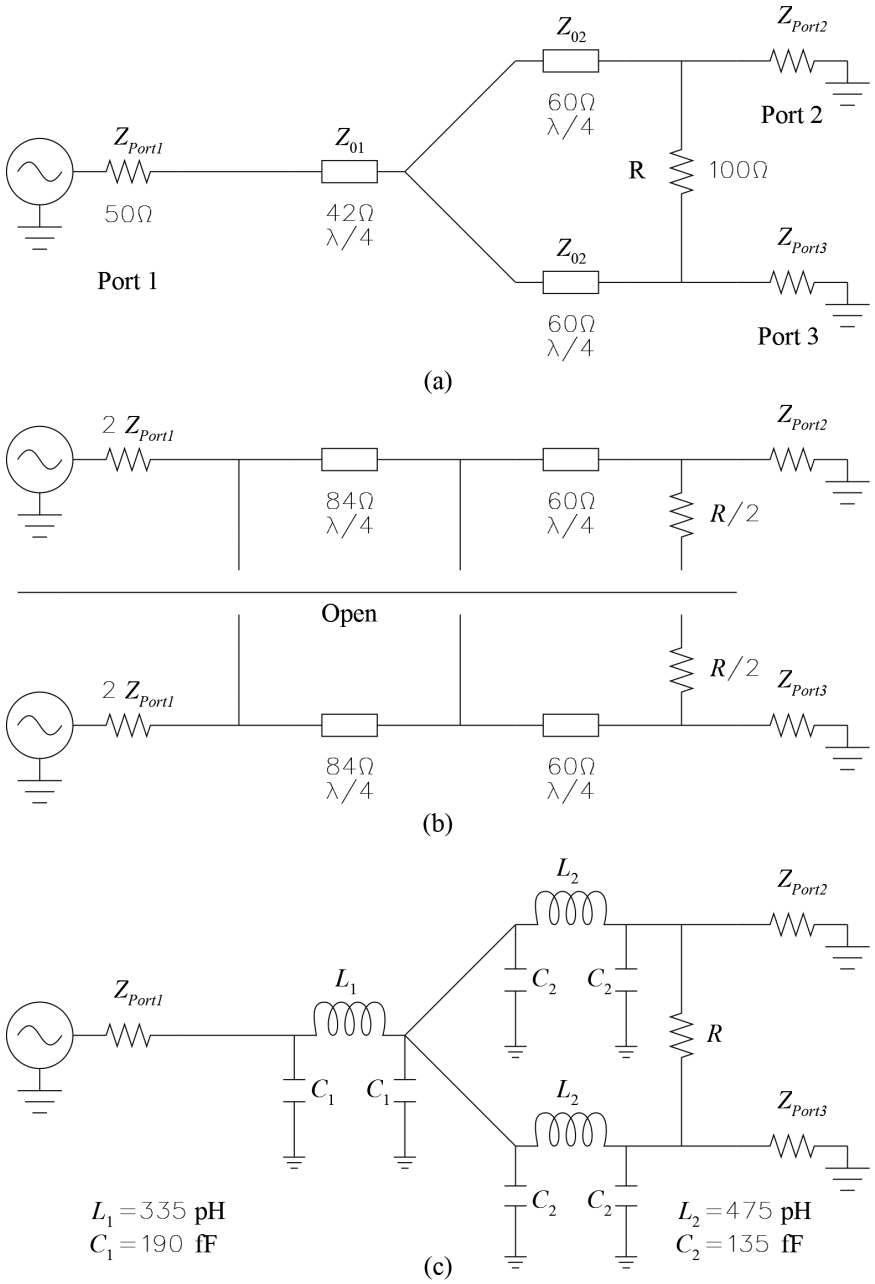


Figure 3.1: 20 GHz broadband Wilkinson power divider circuit schematics: (a) Distributed 50 Ω input and output impedance broadband Cohn divider, (b) forward, even-mode divider half-circuit Butterworth transformers, (c) divider with $\lambda/4$ transmission line elements replaced by Π section lumped-element equivalents.

3.2.1 Design

The values for a canonical low-pass Π network with series inductance, L_s, and shunt capacitance, C_p, of electrical length θ in radians, frequency f_0 in hertz, and characteristic impedance Z_0 in ohms are given by [77]:

$$L_s = \frac{\theta \cdot Z_0}{\pi^2 \cdot f_0} \text{ , and } C_p = \frac{\theta}{\pi^2 \cdot f_0 \cdot Z_0} \text{ .} \tag{3.1}$$

While used most often to realize $\lambda/4$ transmission-line segments, these expressions can be used to generate arbitrary length and impedance transmission line equivalents. This allows pseudo-distributed circuit design in lumped elements, examples of which are shown in Table 3.1.

A broadband Wilkinson power divider can be synthesized by replacing the single $\lambda/4$ matching section from $100\,\Omega$ to $50\,\Omega$ in the forward, even-mode Wilkinson analysis circuit with multiple $\lambda/4$ sections designed for a Butterworth/binomial response. A published study of several possible distributed, broadband Wilkinson designs shows that two series (low-pass) $\lambda/4$ sections have a broader bandwidth than one series (low-pass) and one shunt (high-pass) $\lambda/4$ section, trading bandwidth for out-of-band isolation [78]. A reduced component count and smaller area can be achieved by placing the additional series $\lambda/4$ section before, rather than after, the split between the two legs of the Wilkinson, as in Fig. 3.1 a, with negligible effect on divider performance.

Analysis of the even-mode half circuit, shown in Fig. 3.1 b, yields design equations for the characteristic impedance of each section, Z_{01} and Z_{02}, in terms of the desired input and output port impedances, Z_{Port1} and Z_{Port2}, respectively:

$$2 \cdot Z_{01} = 2 \cdot Z_{Port1} \cdot e^{\left[2^{-2} \cdot K_0^2 \cdot \ln\left(\frac{Z_{Port2}}{2 \cdot Z_{Port1}}\right)\right]} \text{ ,} \tag{3.2}$$

$$Z_{02} = 2 \cdot Z_{01} \cdot e^{\left[2^{-2} \cdot K_1^2 \cdot \ln\left(\frac{Z_{Port2}}{2 \cdot Z_{Port1}}\right)\right]} \text{ .} \tag{3.3}$$

These expressions are derived from the general binomial transformer equations [75]:

$$Z_{m+1} = Z_m \cdot e^{\left[2^{-M} \cdot K_n^M \cdot \ln\left(\frac{Z_{out}}{Z_{in}}\right)\right]} \text{ ,} \tag{3.4}$$

Table 3.1: L_s and C_p values for $\lambda/4$ Π equivalent sections of various useful impedances at 20 GHz.

Z_0	L_s	C_p	Application
35 Ω	280 pH	230 fF	Branch line coupler Z_{BL}
42 Ω	335 pH	190 fF	Broadband Wilkinson Z_{01}
50 Ω	400 pH	160 fF	Balanced divider Z_0
60 Ω	475 pH	135 fF	Broadband Wilkinson Z_{02}
70 Ω	560 pH	110 fF	Standard Wilkinson Z_{Wilk}

$$K_m^M = \frac{M!}{(M-m)! \cdot m!} \ . \tag{3.5}$$

where Z_{in} is the input impedance, Z_{out} is the output impedance, M is the total number of binomial transformer sections, and m is the current section.

These distributed sections can then be converted to LC Π $\lambda/4$ sections using equation 3.1, as shown in Fig. 3.1 c. For a two-stage broadband Wilkinson centered at 20 GHz, the desired $\lambda/4$ section impedances and corresponding L and C values are shown in Table 3.1. These values are well within the range of impedance values realizable in the NIST IC process discussed in Section 1.4.1.

The lumped-element Wilkinson models derived from the closed-form expressions were optimized in Agilent's ADS circuit simulator to obtain the desired trade-off between bandwidth and reflections. Initial layout geometries were obtained based on an ideal parallel plate capacitor model and Stanford Spiralcalc [80] planar spiral inductor models, then simulated and tuned as single L and C elements embedded in a CPW transmission line using Ansoft's HFSS v10 [65] 3-D FEM simulator. Superconducting niobium traces are modeled with 3-D perfect electric conductors (PEC) in HFSS. The solid blue lines in the ground planes of the divider layout in Fig. 3.2 indicate the HFSS L and C cell boundaries.

The HFSS results were exported as S-parameter blocks into ADS for further tuning of the entire circuit via this hybrid simulation. This final design was then verified using a complete HFSS simulation. For comparison: the single L or C element HFSS simulations required less than first-order 50 000 tetrahedra, a few hundred megabytes of memory, and less then 20 minutes of

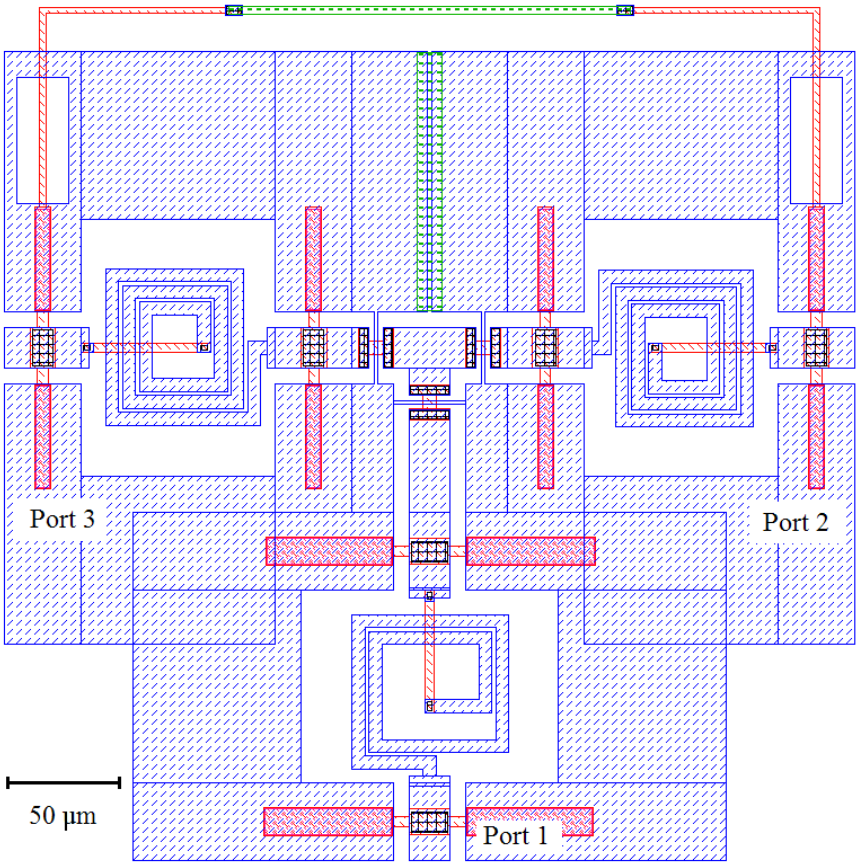


Figure 3.2: A layout of the broadband lumped-element 20 GHz Wilkinson from Fig. 3.1 c. Red ⧅ hatch is Nb1, black ⊞ hatch is Nb1-2 via, blue ⧄ hatch is Nb2 and green ⧈ hatch is AuPd. Solid blue lines in the CPW ground planes show the HFSS L and C simulation cell boundaries. Approximate divider dimensions are 400 µm (0.07 λ) × 300 µm (0.05 λ) with minimum trace width and spacing of 1.5 µm (0.0002 λ).

processor time per element simulation; the hybrid simulations in ADS utilized a few megabytes of memory and less than a minute; the full divider simulations in HFSS required first-order 141 000 tetrahedra, over 4 GB of memory space, and 7 hours of real time to solve on a 32-bit Pentium D 3.4 GHz processor with 3 GB RAM [65].

3.2.2 Layout

Figure 3.2 shows a typical layout of a 20 GHz center-frequency broadband, lumped-element Wilkinson power divider with 50 Ω input and output impedances. Approximate dimensions of this lumped-element Wilkinson are 400 µm (0.07 λ) × 300 µm (0.05 λ), as compared with a

standard distributed Wilkinson at 20 GHz, which would be approximately 1600 µm (0.25 λ) × 400 µm (0.07 λ) in this technology.

The layout of a MMIC circuit is often critical to the design as seemingly minor nuances can have detrimental effects in circuit performance due to unwanted electromagnetic coupling. For example, the circuit shown in Fig. 3.2 exhibits sub-optimal amplitude and phase balance. The orientation of the spiral inductor winding induces a mirror current in the CPW ground plane on the side facing the outermost coil, hence this layout shows a slight amplitude imbalance due to opposing output inductor senses. Figure 3.3 shows a comparison of surface currents on the original design, and the final improved design with matched inductor sense, and better CPW ground balancing. To show this level of surface current detail, each of the HFSS simulations of the entire Wilkinson required 250 000 first-order tetrahedra, and 8 hours of processor time to solve.

Several test circuits were considered to facilitate testing, shown in Fig. 3.4. In the test circuit 1, Fig. 3.4 a, no on-chip termination is required, but the port 2 and port 3 S-parameter responses are not directly measurable. In addition, power reflections between the two dividers can cause deviations in the measurement from the desired matched load case. Circuit 2, Fig. 3.4 b, allows port 2 characterization, but introduces another unknown in the on-chip termination. Circuit 3, Fig. 3.4 c, uses an on-chip resistive termination at port 1. This allows isolation characterization of port 2 to port 3 with the caveat of a separate physical device and possible process variations across the wafer. Only circuits 2 and 3 were realized for Wilkinson unit-cell testing. All superconducting circuits reported here were fabricated in the NIST Boulder Quantum Device Fabrication facility.

3.2.3 Testing

Measurements were performed with an Agilent 8722ES [65] vector network analyzer (VNA). Calibration was accomplished using on-chip Through-Reflect (short)-Line (1.5 mm) (TRL) standards custom-fabricated with a band of 8–35 GHz at 4 K immersed in a liquid helium ($\epsilon_r = 1.005$) dewar. The repeatability of the measurements is limited by several factors in the test setup.

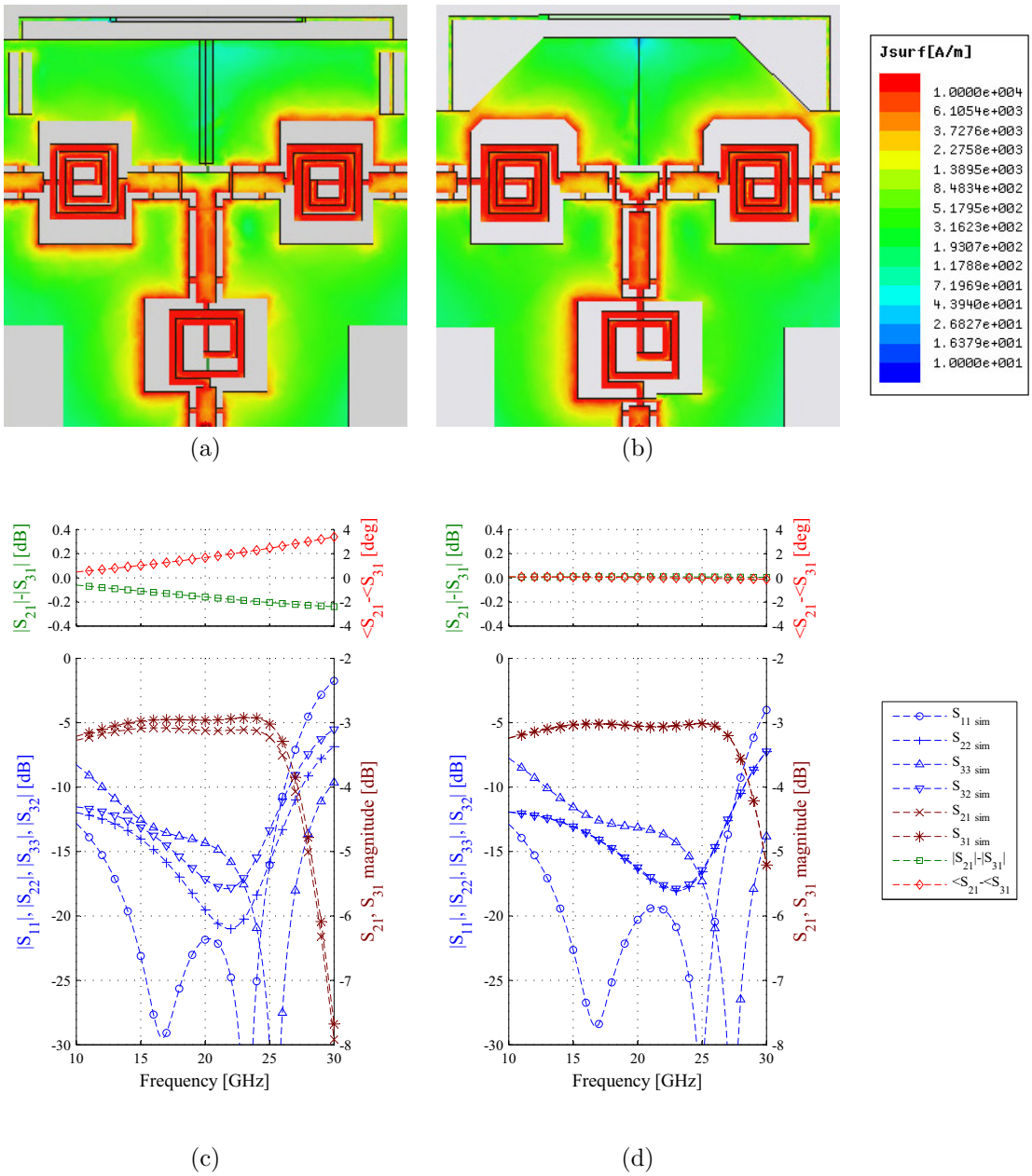


Figure 3.3: HFSS surface current simulation comparison of: (a) Wilkinson with counter oriented inductors, (b) Wilkinson with matched orientation inductors, (c) Simulated amplitude balance of counter oriented inductors, (d) Simulated amplitude balance matched orientation inductors.

The calibration procedure requires three thermal cycles from room temperature to 4 K, boiling ∼1 liter of helium. This changes the thermal gradient along the 1.2 m cryoprobe coaxial cable, hence its electrical length and loss, with each successive measurement. The chip contact is made via a pressure screw that engages a set of copper-beryllium (Cu-Be) spring fingers with the gold-palladium (Au-Pd) coated pads on the chip, with only moderate repeatability. Finally, the

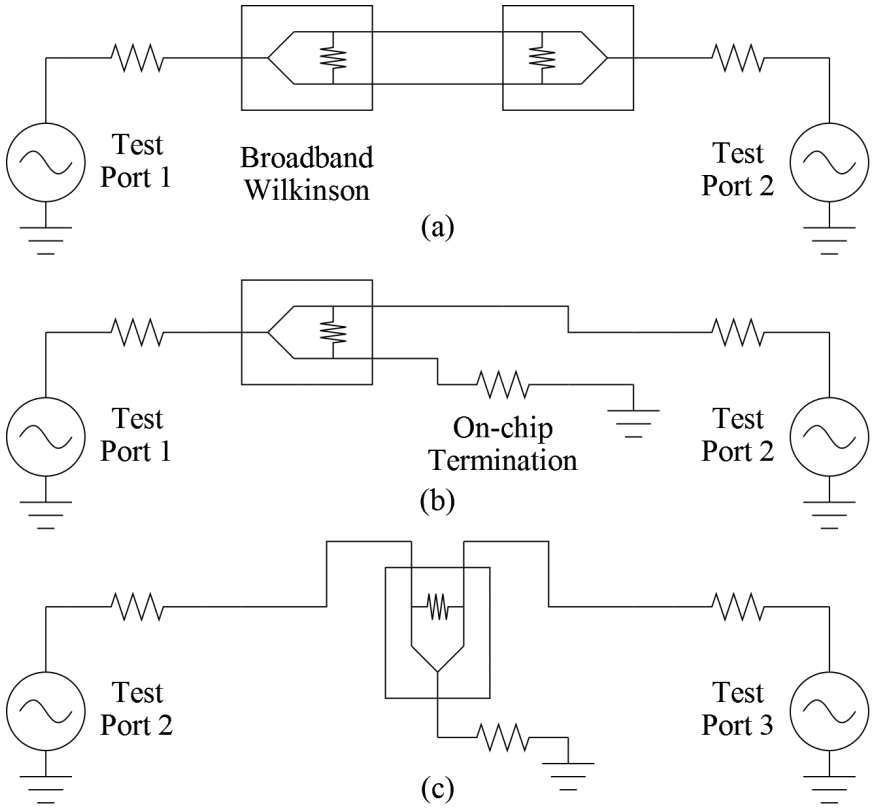


Figure 3.4: Three-port Wilkinson divider to two-port network analysis conversion circuits: (a) Circuit 1: back-to-back dividers. (b) Circuit 2: port 3 terminated on-chip. (c) Circuit 3: port 1 terminated on-chip.

economical SMA connectors used have resonances in the upper end of the measurement band. A flip-chip bonded permanent mounting solution has been developed in Chapter 2 to address these issues in the final programmable Josephson voltage standard system [55] but is not practical for use with the many test circuits and VNA calibration standards needed here.

Figure 3.5 a shows a comparison of HFSS simulations and measurements for test circuit 2 from Fig. 3.4 b. HFSS simulation and measurement results for test circuit 3 from Fig. 3.4 c are shown in Fig. 3.5 b. The greater than 10 GHz bandwidth around 20 GHz and the low insertion and return losses of this circuit makes it well suited to integration into the N-way binary divider, Section 3.3, for the 10 V PJVS system. Table 3.2 shows a summary of Wilkinson divider test circuit measurement results comparing the superconducting work discussed here with the commercial TQPED process version of this design, discussed in Section 3.4. The 15–22 GHz band is considered the band of interest for this design, allowing for ample tuning around the

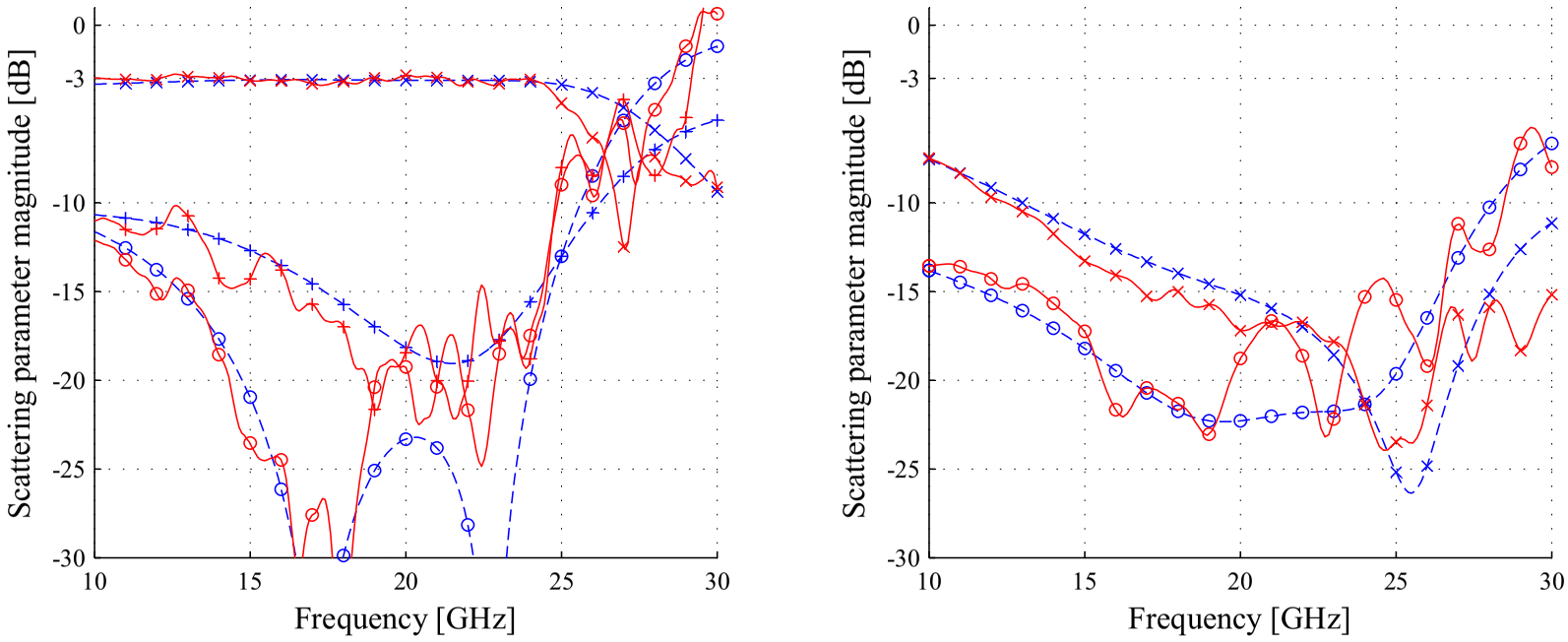


Figure 3.5: (a) Broadband lumped-element Wilkinson, Fig. 3.2, HFSS simulated data (blue dashed lines) and measurement results (red solid lines) from test circuit 2, Fig. 3.4 b, using a 4 K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$. (b) Broadband lumped-element Wilkinson, Fig. 3.2, HFSS simulated data (blue dashed lines) and measurement results (red solid lines) from test circuit 3, Fig. 3.4 c, using 4 K TRL calibration on-chip. S_{23} is marked with $\times$, S_{33} is marked with $\circ$.

Table 3.2: Broadband divider measurement summary comparing the NIST superconducting IC process, Section 3.2, and the TriQuint commercial TQPED process, Section 3.4. Summary data is calculated from the results shown in Fig. 3.5 a, Fig. 3.5 b, and Fig. 3.10.

Process	**Parameter**	$\boldsymbol{BW}\vert_{\mathbf{-10\,dB}}$	$\mathbf{Ave}\vert_{\mathbf{15\,GHz}}^{\mathbf{22\,GHz}}$	$\mathbf{Max}\vert_{\mathbf{15\,GHz}}^{\mathbf{22\,GHz}}$
NIST	S_{11}	10–25 GHz	–21.7 dB	–17.4 dB
NIST	S_{22}	10–25 GHz	–16.6 dB	–12.9 dB
NIST	S_{23}	13–30 GHz	–15.6 dB	–13.3 dB
NIST	S_{33}	10–28 GHz	–19.9 dB	–16.6 dB
NIST	IL	–	0.1 dB	0.4 dB
TQPED	S_{11}	10–25 GHz	–23.0 dB	–19.2 dB
TQPED	S_{22}	10–24 GHz	–23.3 dB	–18.0 dB
TQPED	IL	–	0.6 dB	0.9 dB

20 GHz junction array design point. Average in-band values in Table 3.2 are computed as the base-10 logarithm of mean power:

$$\text{Ave}|S_{ij}| = 10 \cdot \log_{10}\left[\text{Mean}|_{15\,\text{GHz}}^{22\,\text{GHz}}(|S_{ij}|)^2\right] \ . \tag{3.6}$$

Insertion loss, IL, for this work is defined as

$$IL = -10 \cdot \log_{10} \frac{\sum_{i=2}^{N}(|S_{i1}|^2)}{1-|S_{11}|^2} \ . \tag{3.7}$$

By circuit symmetry and from simulation results shown in Fig. 3.3 d, S_{31} is assumed to be approximately equal to S_{21} for measured insertion loss calculations in Table 3.2.

3.3 Balanced Sixteen-Way Power Divider

The concept of a balanced divider/combiner, widely used in broadband amplifier design [75], can be applied here to achieve a many-way power division to many identical arrays of junctions. A balanced divider relies upon the fact that each array has a nearly identical return loss. By inserting an additional $\lambda/4$ transmission line between port 2 of the Wilkinson and the junction array, the round trip reflection path is 180° longer than the corresponding round trip reflection

path from the junction array connected to port 3 of the Wilkinson. These two reflections are out of phase at port 1 and cancel, leading to a well matched and very broadband system. Many-way power division can be achieved as shown in Fig. 3.6. This solution addresses the fundamental issue with 360°, round-trip, in-phase reflection combining in N-way, even-$\lambda/4$-section, binary, power dividers reported in [69]. Here the total interconnect layout length between dividers is unconstrained, only the $\lambda/4$ delta between branches (implemented in lumped-elements) is required.

3.3.1 Design

The prototype 10 V PJVS chip at 20 GHz reported in [40] requires 268 800 JJs. A sixteen-way on-chip power division allows this massive JJ count to be divided across sixteen smaller junction arrays of 15 600 junctions [59] to improve microwave power distribution from end-to-end of each array. The chip area required for a sixteen-way divider on-chip is reduced by a factor of 4 using the lumped-element Wilkinson dividers and $\lambda/4$ 50 Ω LC Π sections, from Table 3.1, compared to the previously used single $\lambda/4$ distributed matching sections. The entire sixteen-way divider network is simulated in ADS using the hybrid simulation methodology discussed in Section 3.2.1.

In order to appropriately characterize a many-way divider, a test circuit is needed that preserves both the desired loading at the output, as well as the ability to measure insertion loss through the device. The back-to-back circuit shown in Fig. 3.4 a has a fundamental flaw of terminating a divider circuit with its own complex output impedance, rather than the desired real 50 Ω load needed to obtain valid S-parameters. To solve this problem 10 dB attenuators are monolithically integrated between the divider circuit under test, and the combiner output circuit. A schematic of this balanced divider/attenuator/combiner configuration is shown in Fig. 3.6.

Identical length 50 Ω CPW superconducting transmission lines were used to interconnect the divider, the attenuators, and the combiner; the $\lambda/4$ sections were arranged such that the net phase delays along any given division and recombination path are equal. A 1.2 pF coupling capacitor was inserted between the third and fourth levels of power division and recombination

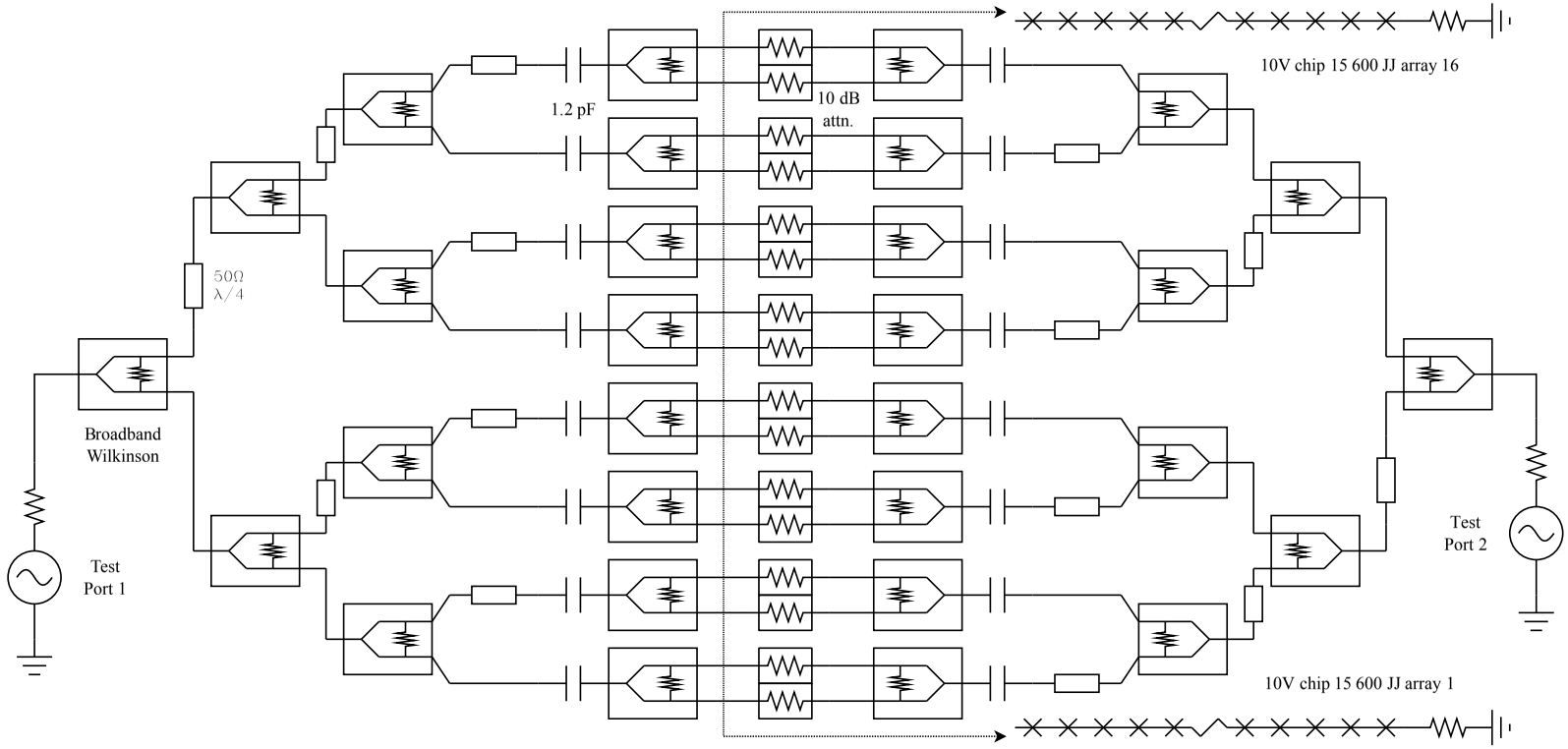


Figure 3.6: A simplified schematic of the balanced divider/attenuator/combiner configuration test circuit, showing broadband lumped-element Wilkinson power dividers, $\lambda/4$ lumped Π sections for reflection cancellation, 10 dB isolation attenuators, and 1.2 pF coupling capacitors between the third and fourth levels of division and combination. Simulated transmission line interconnects and bends are not shown. The dotted cut plane indicates the position of the junction arrays in the 10 V programmable Josephson voltage standard.

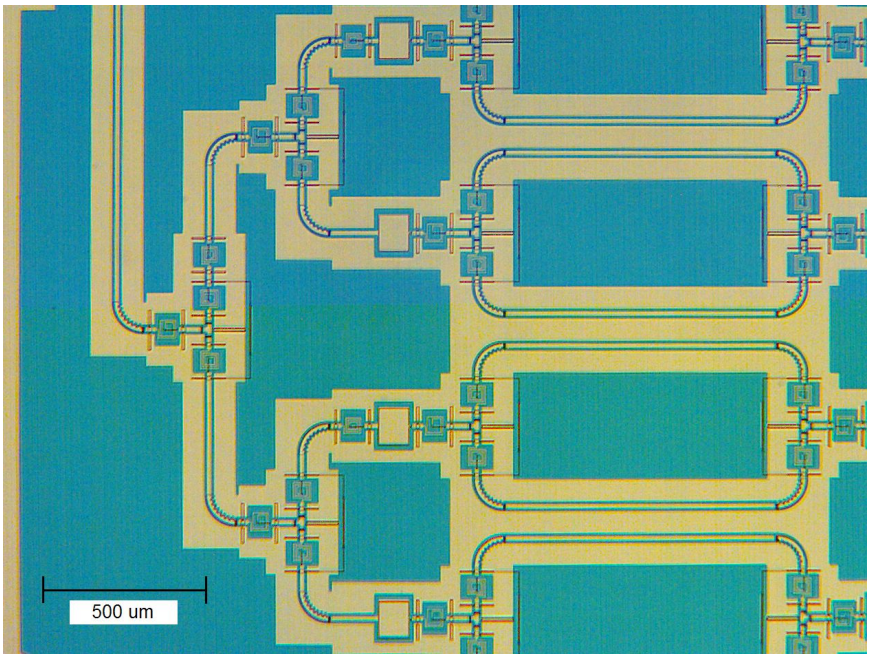


Figure 3.7: A micrograph of a portion of the broadband, balanced, sixteen-way divider/combiner configuration. Three binary levels of power division utilizing the 20 GHz lumped-element Wilkinson divider are shown. The light colored yellow material is Nb, the darker blue material is the silicon substrate.

to AC-couple each pair of junction arrays and enable connecting all of the arrays in series at DC to achieve 10 V. A lithographically identical 10 dB attenuator was fabricated on the same test chip as the divider/attenuator/combiner to allow deembedding of the divider performance.

3.3.2 Testing

The sixteen-way divider/attenuator/combiner (D/A/C) configuration test chip was evaluated in the same manner as the Wilkinson divider chips, discussed in Section 3.2.3. A sixteen-way divider/combiner (D/C) test circuit without attenuators, shown in Fig. 3.7, was also fabricated and tested to demonstrate the utility of the added attenuators. Figures 3.8 a and 3.8 b compare measured and simulated results from the sixteen-way balanced divider/combiner and divider/attenuator/combiner configurations, respectively. Table 3.3 summarizes the measurement data from both test configurations and the 10 dB reference attenuator (10 dB attn.). The measured insertion loss and return loss of the back-to-back test configuration both improve markedly with the incorporation of the 10 dB attenuators. This divider/attenuator/combiner configuration,

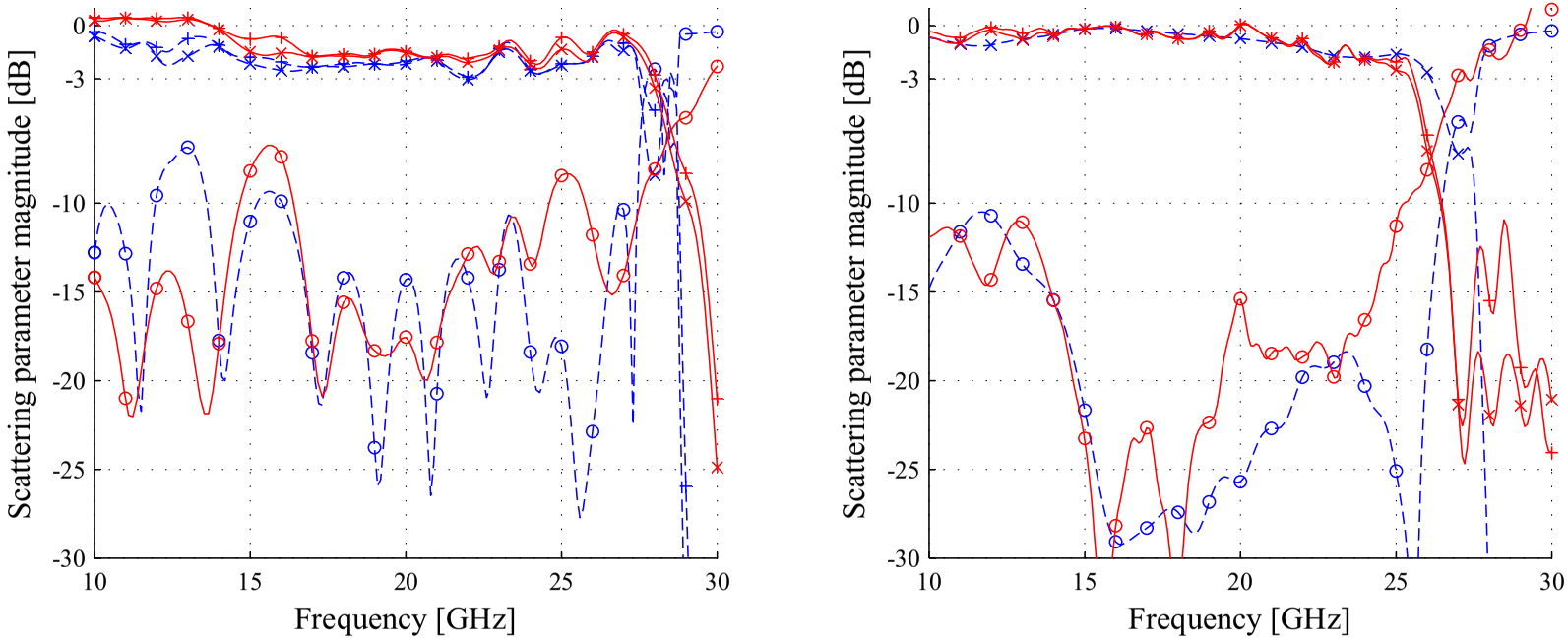


Figure 3.8: (a) Divider/combiner (D/C) configuration measured versus simulated results for sixteen-way balanced broadband Wilkinson divider, Fig. 3.7. Hybrid HFSS 3-D FEM and ADS circuit simulated data (blue dashed lines), and measurements using 4 K TRL calibration on-chip (red solid lines). Note the standing waves between the divider and the combiner apparent in the S_{11} measurement. (b) Divider/attenuator/combiner (D/A/C) configuration sixteen-way balanced Wilkinson divider measured versus simulated, Fig. 3.6, results. S_{21} and IL are calculated by deembedding the 10 dB attenuator data from the D/A/C test configuration data. Hybrid HFSS 3-D FEM and ADS circuit simulated data (blue dashed lines), and measurements (red solid lines) using 4 K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and insertion loss is marked with $+$.

Table 3.3: Sixteen-way balanced divider summary. Values are calculated from the measurements of D/C configuration (Fig. 3.8 a), the on-chip 10 dB attenuator, and D/A/C configuration (Fig. 3.8 b).

Test Circuit	**Parameter**	$\boldsymbol{BW}\vert_{\mathbf{-10\,dB}}$	$\mathbf{Ave}\vert^{\mathbf{22\,GHz}}_{\mathbf{15\,GHz}}$	$\mathbf{Max}\vert^{\mathbf{22\,GHz}}_{\mathbf{15\,GHz}}$
D/C	S_{11}	16.5–24.5 GHz	–11.6 dB	–6.7 dB
D/C	IL_{total}	–	1.4 dB	2.2 dB
D/C	IL_{divider}	–	0.7 dB	1.1 dB
D/A/C	S_{11}	10–25 GHz	–20.5 dB	–15.1 dB
D/A/C	IL_{total}	–	10.0 dB	10.5 dB
10 dB attn.	S_{11}	10–30 GHz	–25.7 dB	–21.4 dB
10 dB attn.	IL	–	9.5 dB	9.9 dB
D/A/C	IL_{divider}	–	0.2 dB	0.5 dB

introduced here, is a useful measurement technique for characterization of many-port integrated dividers.

Assuming the loss in the division is the same as the loss in the recombination, the average and maximum insertion loss through a single sixteen-way divider network, IL_{divider}, can be computed as half of the total for the divider/combiner, IL_{total}. The divider/attenuator/combiner measured data in Fig. 3.8 b and Table 3.3 has been calculated by deembedding the measured insertion loss of a matched, lithographically-identical, 10 dB attenuator on the same chip. The 0.5 dB maximum sixteen-way power divider loss is very small compared to the 3 dB cable loss incurred in the 1.2 m cryoprobe, or to any commercially available broadband divider solution in the 15–22 GHz band. While not measured, the simulated isolation of the sixteen-way divider is similar for adjacent branches, and improved for non-adjacent branches, when compared to the single Wilkinson divider.

The bulk of the insertion loss is due to the balanced out-of-phase divider reflections producing a voltage drop across the Wilkinson isolation resistor before they cancel. This assertion is supported by simulations as well as the noted drop in IL with the addition of the attenuators, suppressing the reflections from the combiner. A tradeoff in a balanced divider, versus a standard corporate divider without the $\lambda/4$ reflection canceling sections, is that the uniformity of division

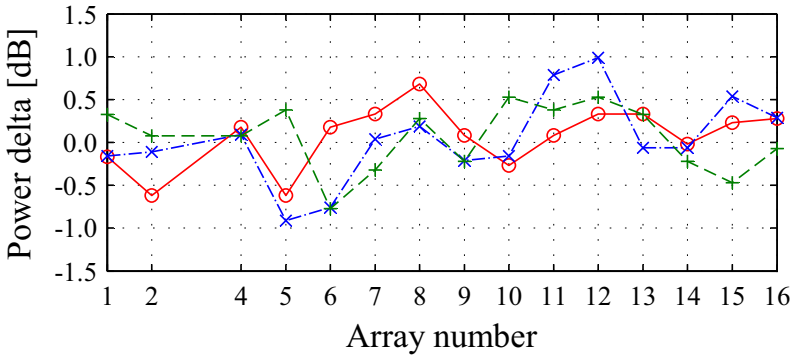


Figure 3.9: Measured power division uniformity results from broadband Wilkinson in sixteen-way balanced divider feeding a prototype 10V chip with 16 arrays of 15 600 junctions at 15 GHz (red solid line, marked ∘), 19 GHz (blue dash-dot line, marked ×), and 22 GHz (green dashed line, marked +). The x-axis indicates array number, coinciding with Fig. 3.6 with one at the bottom and sixteen at the top. The y-axis is the change from nominal source input power at which each array exhibits an equal I_{bias}/I_C ratio (an indicator of equal microwave power delivered to that array).

in simulations suffers slightly away from the center frequency of the $\lambda/4$ section. By inspection, a balanced divider will have a 90° phase progression between outputs rather than phase balance.

A prototype 10 V programmable Josephson voltage standard was fabricated using the sixteen-way, balanced divider to split a single microwave feed from a room-temperature power amplifier into sixteen arrays of 15 600 junctions each [40]. The DC bias current range over which the Shapiro zero-voltage step is quantized in the junction DC IV curve is a strong indicator of microwave current through the junction [64], as discussed in Section 2.3. This property allows the arrays themselves to be used as an on-chip relative power meter to evaluate the amplitude balance of the divider. Figure 3.9 shows the amplitude balance of the divider at 15, 19, and 22 GHz across the sixteen output arrays. This data is derived from a measurement of I_{bias}/I_C for the top of the zero-voltage Shapiro step over a sweep of power from approximately 2 mW to 200 mW on-chip for all sixteen arrays. The normalization by I_C helps account for junction variation across the wafer, where I_C is the junction critical current [1]. With the exception of array 3, all of the arrays cross an arbitrarily selected constant I_{bias}/I_C within a ±1 dB range of input power, indicating a good microwave power division amplitude balance. Array 3 displayed an isolated junction fabrication defect and is omitted.

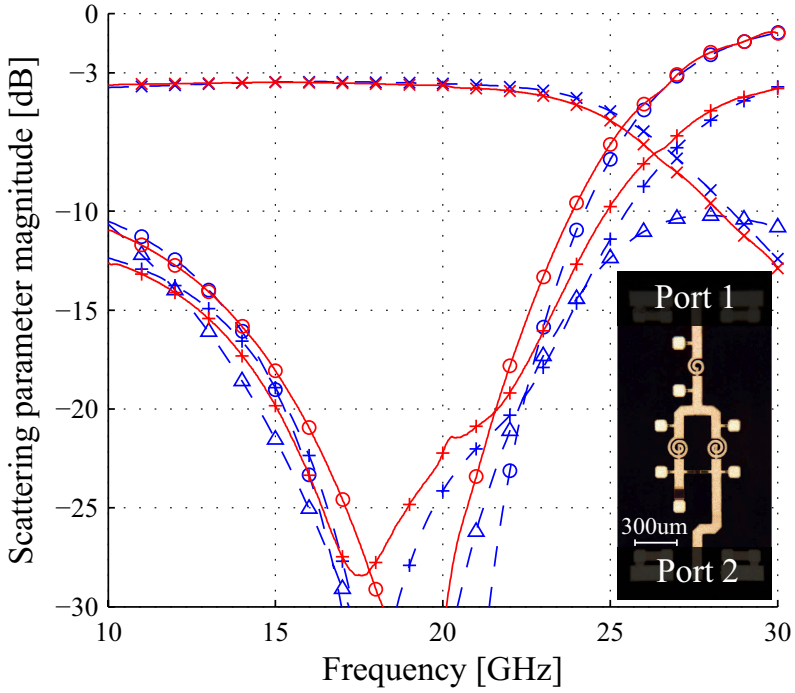


Figure 3.10: Broadband lumped-element TQPED Wilkinson simulated data (blue dashed lines) and measurement results (red solid lines), using room-temperature TRL calibration on-chip. S_{11} is marked with ∘, S_{21} is marked with ×, S_{32} is marked with △, and S_{22} is marked with +. This device was fabricated using the commercial TriQuint TQPED GaAs MMIC process and tested at room-temperature. Port 3 is terminated with an on-chip resistor. The inset is a micrograph of the fabricated device.

3.4 GaAs Wilkinson MMIC

The lumped-element Wilkinson divider shown in Fig. 3.1 c was also implemented in the TriQuint commercial TQPED [65] GaAs MMIC process in 4 µm thick gold microstrip on a 100 µm substrate. A summary of the TQPED process is given in Section 6.3. The port 1 and port 2 through test configuration shown in Fig. 3.4 b was designed and fabricated requiring an area of approximately 1200 µm × 1500 µm. Simulations were performed using the FMCIND2 circular planar spiral inductor model and the TQPED_HP_CAPA parallel plate capacitor model in AWR MWO [81].

This normal metal design at room temperature exhibited a measured average IL of 0.6 dB compared to the measured superconducting device average IL of 0.1 dB in the 15–22 GHz band of interest, shown in Table 3.2. The measured and simulated S-parameters of this device are compared in Fig. 3.10 using wafer probe measurements with on-chip TRL calibration. Even

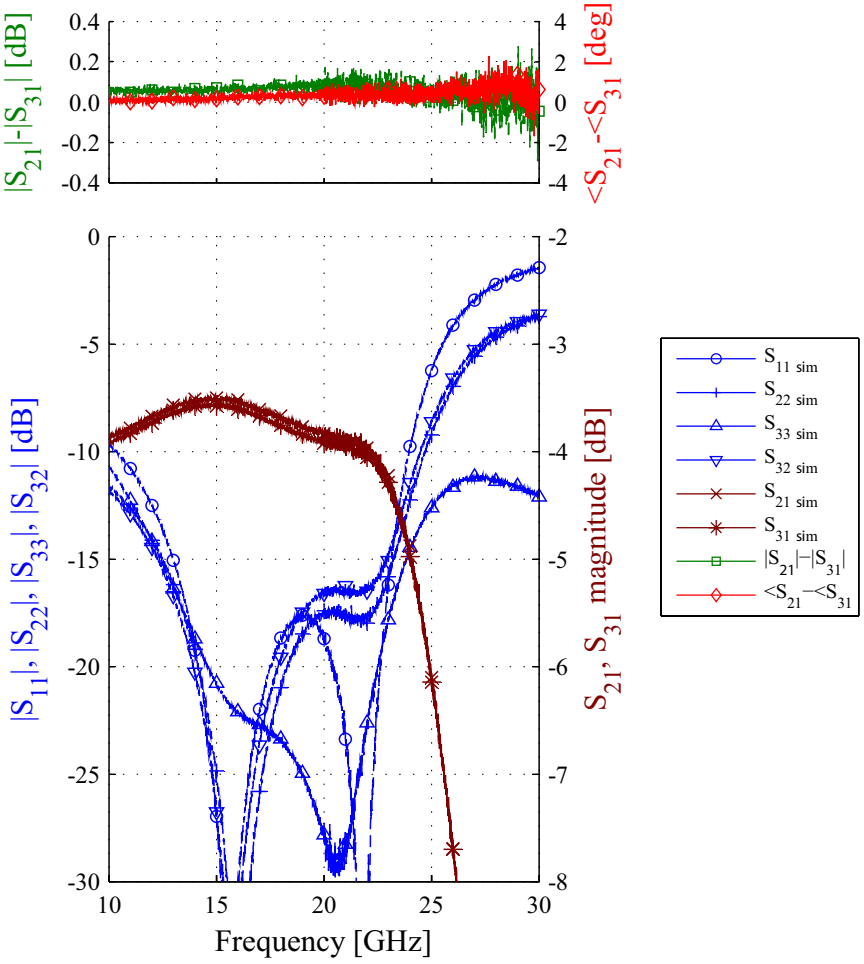


Figure 3.11: Broadband three-port lumped-element TQPED Wilkinson measured scattering parameters, amplitude balance, and phase balance.

without the advantage of superconducting inductors this implementation compares favorably to other published and commercial dividers as shown Table 3.4. This validates the broadband lumped-element design methodology presented here for room temperature IC design with a modest penalty in loss and area.

Porting the lumped-element Wilkinson design to a room-temperature IC process also affords advantages in testability. In addition to better calibration, the availability of a three-port wafer probe station and VNA allowed the full three-port device to be fabricated and evaluated.

Figure 3.11 shows the relevant measured 3-port S-parameters, as well as the amplitude and phase balance of a representative device. Amplitude balance is better than 0.15 dB, and there is less than 1 degree of phase imbalance across the 15–22 GHz band. As would be expected for a commercial process, the device to device repeatability is also very good.

3.5 Summary

Table 3.4 shows a comparison of this work to other published and commercially available N-way power dividers. Comparisons can be made upon the basis of number of divider outputs, N; bandwidth (defined by the match and isolation specification in the S_{11} column), BW; maximum insertion loss in band, IL; and size. Table 3.4 is sorted first by N, then by IL/BW to aid in this comparison. The availability of superconducting, low-loss inductors enables very large and complex circuits including many $\lambda/4$ lumped Π sections to emulate distributed microwave circuit designs in a small fraction of the area with very little penalty in loss. This work, published in [57], exhibits the best bandwidth and insertion loss for its size scale, normalized across N, when compared to published work and commercially available devices.

Table 3.4: Comparison of **this work** and other published and commercially available power dividers sorted by N, then IL/BW.

N	f_-[GHz]	f_+[GHz]	BW[%]	IL[dB]	S_{11}[dB]	Topology	Size[mm × mm × mm]	Reference
16	**15.0**	**22.0**	**37.8**	**0.5**	**-15.0**	**LC Nb on Si, Fig. 3.6**	**4.9 x 1.5 x 0.4**	**Fig. 3.8 b, 15–22 GHz**
16	**13.0**	**25.0**	**63.2**	**1.1**	**-10.0**	**LC Nb on Si, Fig. 3.6**	**4.9 x 1.5 x 0.4**	**Fig. 3.8 b, Full band**
16	10.0	10.8	6.7	0.3	-15.5	Radial cavity to SMA	∼500 x ∼500 x ∼20	Ciao 100107-1601 [65]
16	10.2	12.0	16.2	2.5	-15.0	Substrate integrated WG	200 x 120 x 0.5	Z.C. Hao [70]
8	**15.0**	**22.0**	**37.8**	**1.0**	**-17.9**	**LC Nb on Si, Fig. 4.4 b**	**4.0 x 1.7 x 0.4**	**Fig. 4.4 a, 15–22 GHz**
8	**10.8**	**22.0**	**68.3**	**1.0**	**-15.0**	**LC Nb on Si, Fig. 4.4 b**	**4.0 x 1.7 x 0.4**	**Fig. 4.4 a, Full band**
8	4.0	18.0	127.3	1.2	-11.7	Stripline to SMA	63 x 108 x 10	Empower 0400-0151 [65]
8	8.0	18.0	76.9	2.0	-12.7	Stripline to SMA	61 x 101 x 10	ATM P816H [65]
8	2.5	8.5	109.1	∼2.5	-12.7	Microstrip to SMA	64 x 16 x 0.3	J. Zhou [69]
8	0.5	18.0	188.2	6.5	-11.7	Stripline to SMA	161 x 152 x 13	Narda 4426-8 [65]
4	6.0	18.0	∼100.0	0.8	-12.0	MS on alumina	40 x 20 x 16	A.R. Barnes [71]
4	22.0	26.0	16.7	2.4	-15.5	Lumped 0.13 um CMOS	0.33 x 0.33 x .3	J.G. Kim [72]
2	**13.0**	**24.0**	**61.3**	**0.4**	**-10.0**	**LC Nb on Si, Fig. 3.2**	**0.3 x 0.4 x 0.4**	**Fig. 3.5, Full band**
2	4.0	12.0	100.0	∼0.6	∼-10.0	180° Parisi Hybrid Nb on Si	1.4 x 0.5 x 0.4	A.R. Kerr [68]
2	**15.0**	**22.0**	**37.8**	**0.5**	**-15.4**	**LC Nb on Si, Fig. 4.2 b**	**1.2 x 1.5 x 0.1**	**Fig. 4.2 a, 15–22 GHz**
2	**12.5**	**23.5**	**61.1**	**0.5**	**-10.0**	**LC Nb on Si, Fig. 4.2 b**	**1.2 x 1.5 x 0.1**	**Fig. 4.2 a, Full Band**
2	**15.0**	**22.0**	**37.8**	**0.9**	**-18.0**	**LC Au on GaAs, Fig. 3.1**	**1.2 x 1.5 x 0.1**	**Fig. 3.10, 15–22 GHz**
2	**10.0**	**24.0**	**82.4**	**1.4**	**-10.0**	**LC Au on GaAs, Fig. 3.1**	**1.2 x 1.5 x 0.1**	**Fig. 3.10, Full Band**
2	17.5	22.5	25.0	0.6	-15.0	Ti/Au on micromachined Si	0.3 x 0.4 x 0.3	L.H. Lu [73]
2	22.0	26.0	16.7	1.4	-8.9	Lumped 0.13 um CMOS	0.12 x 0.29 x 0.3	J.G. Kim [72]

Chapter 4

Lumped-Element Symmetrical-Hybrid N-way Power Dividers

Contents

The two-$\lambda/4$ section Wilkinson divider topology presented in Chapter 3 has the drawback of a 180° phase delay through each Wilkinson divider requiring a balanced N-way topology with reduced amplitude and phase balance. In this chapter, a symmetrical-hybrid (s-hybrid) based divider is investigated to circumvent these issues at the cost of larger area and a short-circuit DC path. When compared to a canonical distributed 180°-hybrid, this solution achieves a ten-fold decrease in chip area, and a two-fold increase in bandwidth by utilizing broadband LC Π sections and a coplanar-waveguide phase inverter instead of distributed transmission lines.

To open this chapter, the design of a lumped-element s-hybrid divider unit cell is presented, including cryogenic measurement results from 10–30 GHz. Next, a three-level, binary divider utilizing these unit-cells is designed to meet the challenge of increasing the number of junction arrays under parallel microwave excitation on a chip. Cryogenic measurements are performed on the eight-way divider in a back-to-back divider/10 dB-attenuator/combiner configuration as discussed in Section 3.3. This configuration preserves the desired matched-load, N-way divider in a two-port through test circuit suitable for insertion loss measurements.

4.1 Parisi S-Hybrid with Phase Inverter

The s-hybrid topology of Fig. 4.1 a, introduced in [82], improves the phase and amplitude balance of the canonical 180° hybrid [75] by creating a five-port circuit with a central line of symmetry for power divider applications. A lumped-element Parisi s-hybrid, shown in Fig. 4.1 b, can be synthesized by replacing the typical physical $\lambda/4$ sections of transmission line in a with lumped-element equivalent Π networks of $\pm\lambda/4$ electrical length [79]. This lumped-element topology allows a 10-fold reduction in physical length in the NIST QV IC technology. The availability of superconducting planar spiral inductors enables multiple lumped-element Π sections in a $\lambda/4$ equivalent broadband configuration [68, 79]. The bandwidth of the circuit can be further improved by implementing the 180° transmission-line section using a broadband CPW phase inverter. The broadband lumped-element s-hybrid power divider topology, shown in Fig. 4.1 c,

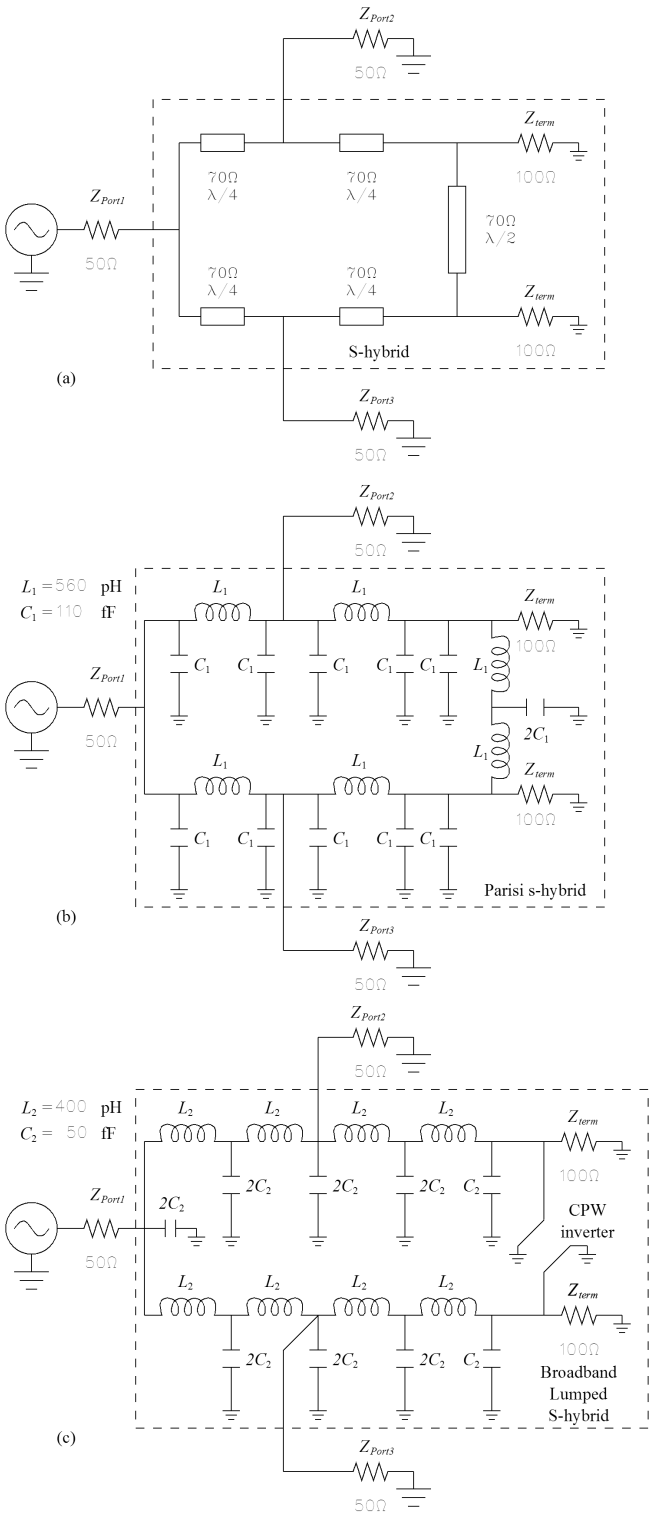


Figure 4.1: Symmetrical-hybrid power divider circuit schematics: (a) Distributed 50 Ω input and output impedance divider, (b) Parisi s-hybrid with $\lambda/4$ transmission line elements replaced by Π section lumped-element equivalents with values given for a 20 GHz center frequency. (c) Broadband lumped-element s-hybrid with 180° CPW phase inverter for further improved bandwidth.

exhibits approximately double the bandwidth compared to that of a distributed 180° s-hybrid, shown in Fig. 4.1 a, in one-tenth the area.

4.1.1 Design

The values for a canonical low-pass $\lambda/4$ Π network with series inductance, L_1, and shunt capacitance, C_1, are given by [79]:

$$L_1 = \frac{Z_0}{2 \cdot \pi \cdot f_0} \text{ , and } C_1 = \frac{1}{2 \cdot \pi \cdot f_0 \cdot Z_0} \text{ ,} \tag{4.1}$$

where frequency f_0 is in hertz and characteristic impedance Z_0 is in ohms. To realize a broader bandwidth $\lambda/4$ equivalent segment, expressions for multiple LC Π sections in a $\lambda/4$ line can be derived by solving the lumped-element equivalent circuit for the desired phase shift response as in [79]. For a two LC Π section $\lambda/4$ equivalent line, the L_2 and C_2 values are given by:

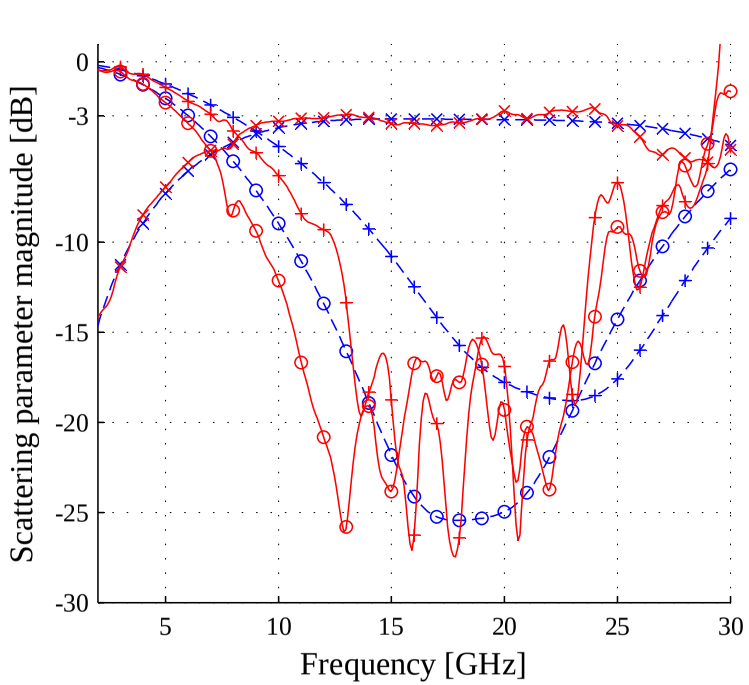
$$L_2 = \frac{Z_0}{\sqrt{2} \cdot 2 \cdot \pi \cdot f_0} \text{ , and } C_2 = \frac{\sqrt{2} - 1}{2 \cdot \pi \cdot f_0 \cdot Z_0} \text{ .} \tag{4.2}$$

L and C values for 70 Ω $\lambda/4$ sections centered at 20 GHz are given in Figs. 4.1 b and c. These values are well within the range of impedance values realizable in the NIST QV IC process.

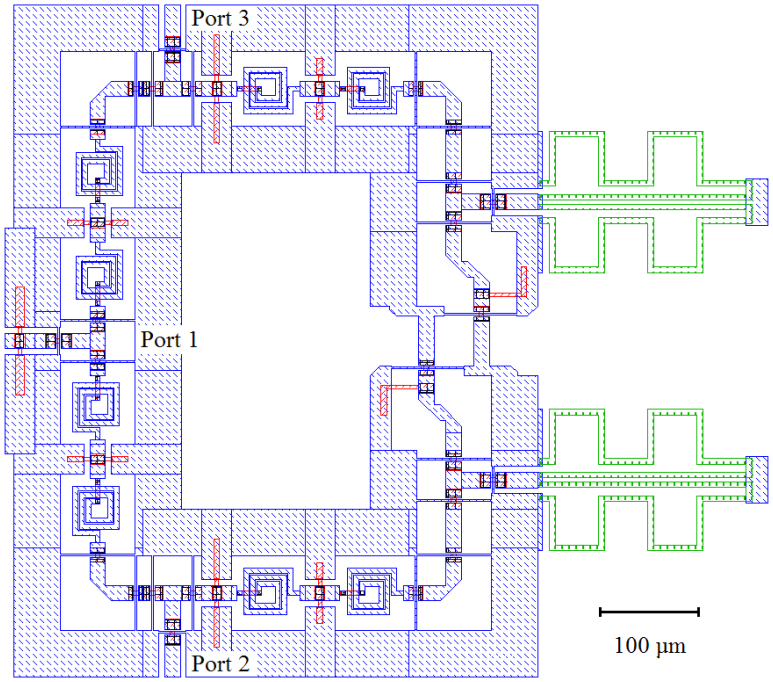
The closed-form circuit models in Fig. 4.1 c were optimized in Ansoft's Designer v3.5 [65] circuit simulator using 3-D FEM L and C circuit element models from Ansoft's HFSS v11 [83] to correct for layout parasitics. Each superconducting niobium trace is modeled with a 3-D perfect electric conductor (PEC) in HFSS. The solid blue lines in the ground planes of the divider layout in Fig. 4.2 b indicate the HFSS L and C cell boundaries. The final layout was then verified with a complete HFSS simulation.

4.1.2 Layout and Fabrication

The superconducting NIST QV IC fabrication process used to realize this s-hybrid divider is described in detail in Section 1.4.1. Figure 4.2 b shows a typical layout of a 20 GHz design-frequency broadband, lumped-element s-hybrid power divider with 50 Ω input and output impedances. Approximate dimensions of this lumped-element s-hybrid are 800 µm (0.13 λ) × 700 µm (0.11 λ),

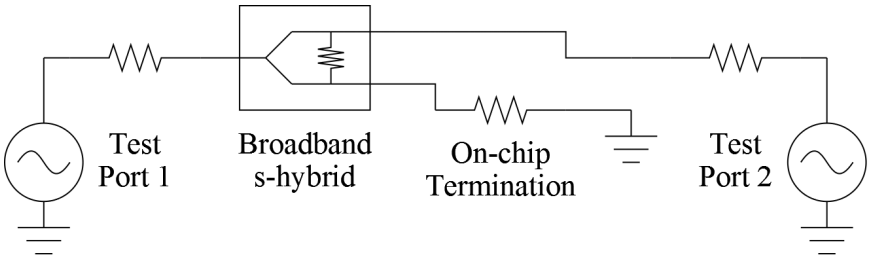


(a)

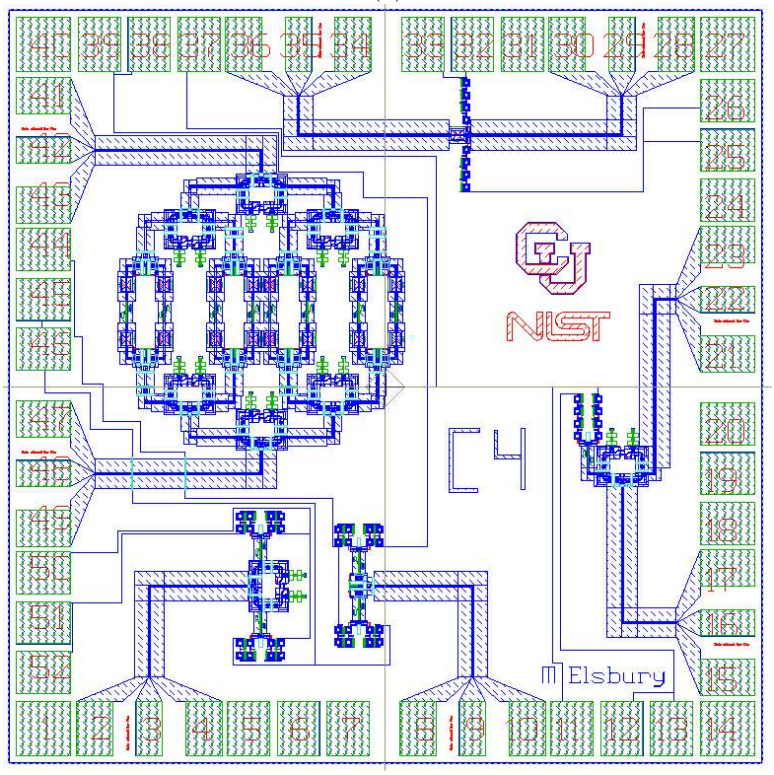


(b)

Figure 4.2: (a) Broadband lumped-element s-hybrid HFSS simulated data (blue dashed lines) and measurement results (red solid lines) from test circuit shown in Fig. 4.3 a using a 4 K TRL calibration on chip. (b) A layout of the broadband lumped-element 20 GHz s-hybrid from Fig. 4.1 c. Red ▨ hatch is Nb1, black ⊞ hatch is Nb1-2 via, blue ▧ hatch is Nb2 and green ▣ hatch is AuPd. Solid blue lines in the CPW ground planes show the HFSS L and C simulation cell boundaries. Approximate divider dimensions are 800 µm (0.13 λ) × 700 µm (0.11 λ) with minimum trace width and spacing of 1.5 µm (0.0002 λ).



(a)



(b)

Figure 4.3: Three-port divider to two-port network analysis conversion circuit with port 3 terminated on-chip. (b) The 10 mm × 10 mm test chip layout including the a) 2-port s-hybrid test circuit (right), 1-port s-hybrid and Wilkinson test circuits with Section 5.3.3 on-chip powder detectors, discussed in Section 5.3.3 (bottom), 8-way divider/attenuator/combiner test structure (left), and a Section 5.1 PJVS bias-tee test circuit (top).

as compared with a standard distributed 180°-hybrid at 20 GHz, which would be approximately 3000 µm in diameter. The two-port test circuit, shown in Fig. 4.3 a with port 3 terminated on-chip, was fabricated for unit-cell testing on the test chip shown in Fig. 4.3 b, as well as the 8-way divider/attenuator/combiner discussed in Section 4.2.

Table 4.1: S-hybrid divider unit-cell and eight-way divider measurement data calculated from the results shown in Figs. 4.2 a and 4.4 a.

Test Circuit	**Parameter**	$\boldsymbol{BW}\vert_{\mathbf{-15\,dB}}$	$\mathbf{Ave}\vert^{\mathbf{22\,GHz}}_{\mathbf{15\,GHz}}$	$\mathbf{Max}\vert^{\mathbf{22\,GHz}}_{\mathbf{15\,GHz}}$
Unit-cell	S_{11}	13–23 GHz	–18.4 dB	–15.4 dB
Unit-cell	S_{22}	10–25 GHz	–19.2 dB	–15.2 dB
Unit-cell	IL	–	0.2 dB	0.5 dB
D/A/C	S_{11}	11–22 GHz	–22.3 dB	–17.9 dB
D/A/C	IL_{total}	–	10.4 dB	11.2 dB
10 dB attn.	S_{11}	10–30 GHz	–25.7 dB	–21.4 dB
10 dB attn.	IL	–	9.5 dB	9.9 dB
D/A/C	IL_{divider}	–	0.5 dB	1.0 dB

4.1.3 Testing

Measurements were performed with an Agilent 8722ES [65] VNA. Calibration was accomplished using on-chip Through-Reflect (short)-Line (1.5 mm) standards with a band of 8–35 GHz at 4 K immersed in a liquid helium ($\epsilon_r = 1.005$) dewar. Table 4.1 shows a summary of divider test circuit measurement results. Figure 4.2 a shows a comparison of HFSS simulations and measurements for the test circuit in Fig. 4.3 a. The 15–22 GHz band is considered the band of interest for this design, allowing for ample tuning around the 20 GHz junction array design point. Average in-band values in Table 4.1 are computed as the base-10 logarithm of mean power using Equation 3.6. Insertion loss, IL, for this work is defined using Equation 3.7. By circuit symmetry and from simulation results, S_{31} is assumed to be approximately equal to S_{21} for insertion loss calculations for the s-hybrid unit-cell.

4.2 Eight-Way Power Divider

Many-way power division can be achieved in a corporate divider topology by creating a binary division tree of two-way dividers. Due to chip area constraints only an eight-way division is implemented here with broadband lumped-element Wilkinson dividers from Chapter 3 for the final level of division. The number of divisions scales easily in simulation; the 16-way or 32-way division required for the 10 V PJVS prototype could be implemented in a larger chip area.

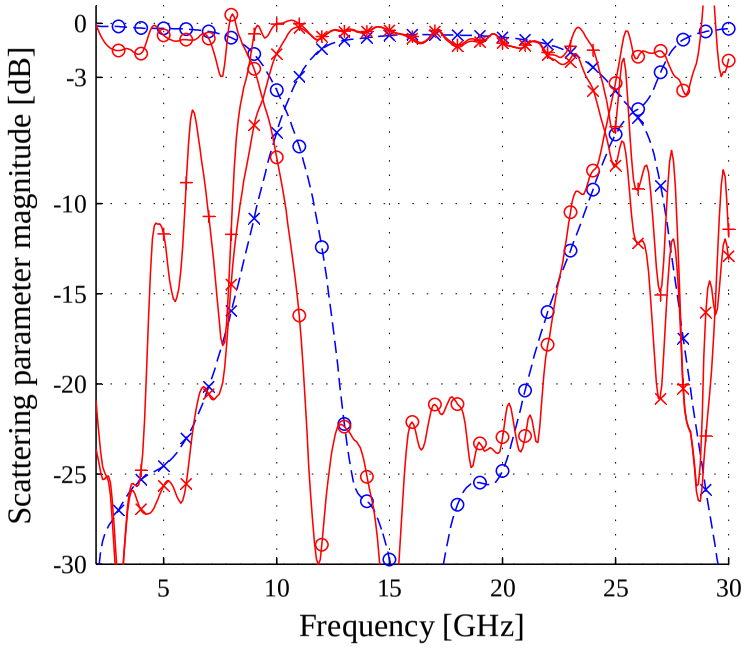
In order to appropriately characterize a many-way divider, a test circuit is needed that preserves both the desired loading at the output, as well as the ability to measure insertion loss through the device. A simple back-to-back divider/combiner circuit has a fundamental flaw of terminating a divider circuit with its own complex output impedance, rather than the desired real 50 Ω load needed to obtain valid S-parameters, as discussed in Section 3.3. To solve this problem 10 dB attenuators are monolithically integrated between the divider circuit under test and the combiner output circuit. The entire eight-way divider/attenuator/combiner network is simulated in Designer using the hybrid simulation methodology discussed in Section 3.2.1. A lithographically identical 10 dB attenuator was fabricated on the same wafer as the divider/attenuator/combiner to allow deembedding of the divider performance.

The eight-way divider/attenuator/combiner configuration circuit, shown in Fig. 4.4 b, was evaluated in the same manner as the unit-cell divider, discussed in Section 4.1.3. Figure 4.4 a compares measured and simulated results from the eight-way divider/attenuator/combiner configuration. Table 4.1 summarizes the measurement data from the divider/attenuator/combiner (D/A/C), and the 10 dB attenuator (10 dB attn).

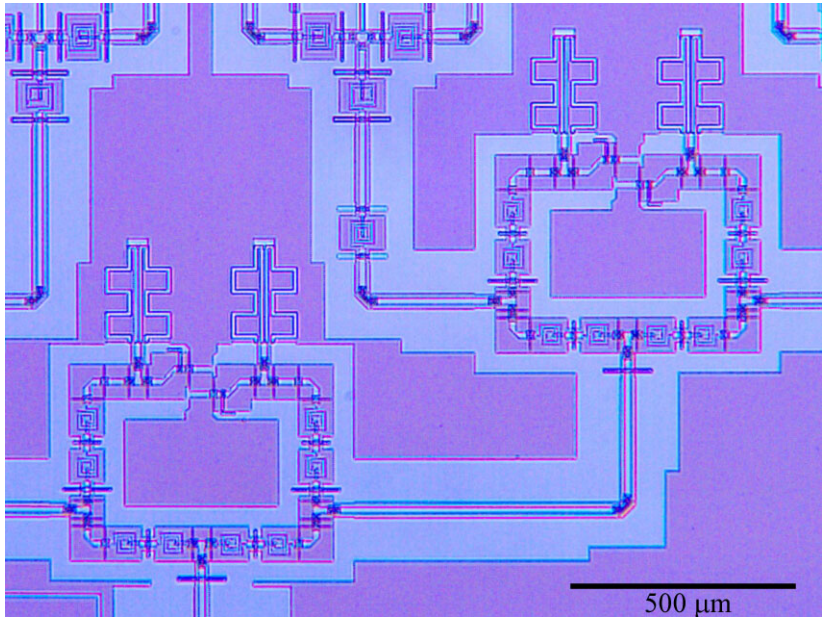
Assuming the loss in the division is the same as the loss in the recombination, the average and maximum insertion loss through a single eight-way divider network, IL_{divider}, can be computed as half of the total for the divider/combiner, IL_{total}, after subtracting the measured insertion loss of a matched, lithographically-identical, 10 dB attenuator on the same chip. The divider/attenuator/combiner measured data set shown in Fig. 4.4 b and Table 4.1 has been calculated in this manner. The 1 dB maximum eight-way power divider loss is very small compared to the 3 dB cable loss incurred in the 1.2 m cryoprobe or to any commercially available broadband divider solution in the 15–22 GHz band, compared in Table 3.4.

4.3 Summary

The lumped-element s-hybrid with a CPW phase inverter demonstrated in this chapter has double the bandwidth in one-tenth the area and improved amplitude and phase balance, when compared



(a)



(b)

Figure 4.4: (a) Divider/attenuator/combiner (D/A/C) configuration eight-way s-hybrid divider measured versus simulated results. S_{21} and IL are calculated by subtracting 10 dB attenuator data from D/A/C test configuration data. Hybrid Designer circuit and HFSS 3-D FEM simulated data (blue dashed lines), and measurements (red solid lines) using a 4 K TRL calibration on chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$. (b) A micrograph of a portion of the broadband, eight-way divider/attenuator/combiner configuration. Two binary levels of power division utilizing the 20 GHz lumped-element s-hybrid divider are shown. The light colored blue material is Nb, the darker purple material is the silicon substrate.

to a canonical distributed 180° hybrid. This topology can be optimized for improved power handling and heat dissipation with two shunt resistors to ground, when compared to a Wilkinson based divider topology with one signal-to-signal resistor [82]. A single divider demonstrates 0.5 dB maximum insertion loss, and a 1.5:1 VSWR bandwidth of 13–23 GHz. An eight-way, three-level, binary, power divider network is characterized in a divider/attenuator/combiner back-to-back measurement configuration with a 20 dB match bandwidth from 11.5–21.5 GHz. In the 15–22 GHz band of interest, the maximum insertion loss for the sixteen-way divider network is 1.0 dB, with an average of 0.5 dB reported in [58].

The 180° s-hybrid match and bandwidth are superior to the Wilkinson divider demonstrated in Chapter 3 and other commercial and published works shown in Table 3.4. The Wilkinson divider, on the other hand, has a smaller area and a through path at DC. For the 10 V PJVS prototype, a DC divider path simplifies DC biasing and yield screening significantly, so the Wilkinson divider was chosen to implement the 10 V PJVS system [40], Fig. 1.7, on these grounds.

Chapter 5

Integrated Circuit Components for JVS applications

Contents

A JVS, as described in Section 1.5, requires a multitude of components all designed to rigorous specifications. Previous chapters have addressed some of the more complicated components in detail; this chapter presents a collection of monolithically-integrated circuit elements for JVSs with improved microwave performance to aid future designers of similar systems. Design goals for this collection are minimal loss and a match better than -20 dB over a band of 15–22 GHz for PJVS applications, or DC–25 GHz for acJVS applications.

As in previous chapters, these components were designed in HFSS at the sub-circuit level, then combined in a circuit simulator, and finally verified in their entirety with a full-wave 3D simulation. These simulation results will be presented, along with experimental verification of preliminary test structures. Elements that have been redesigned to enable the next generation of NIST JVS systems include: bias-tee networks, CPW corners, CPW ground-plane ties, and termination resistors.

The packaging constraints of working at 4 K, as discussed in Chapter 2, make superconducting MMIC characterization difficult. To address this challenge, often circuits must be designed not only to serve a purpose in the end design, but also to provide a characterization vehicle for other circuits and the IC process. Several circuits were designed and fabricated as process monitoring and characterization devices: attenuators, power-detecting terminations, distributed 90° hybrids, stepped-impedance filters, and a lumped-element 20 dB directional coupler. This collection of circuits was invaluable for initial process and device characterization, as well as contributing to the performance of JVS systems.

5.1 Bias-tee Networks

Cryogenic Josephson junctions, like standard transistors and diodes, are non-linear devices that convert DC bias into microwave energy, or visa-versa. A broadband bias network is needed to current bias the multiple arrays of many JJs. These bias-tees are used to current bias individual sub-arrays, as well as to sum the quantized voltage across the chip and observe the output, shown in Fig. 1.7. To meet this need, a low-microwave-leakage 10-25 GHz bandwidth bias-tee with a

superconducting DC path is required for the 10 V programmable Josephson voltage standard, Section 1.5.2 [40].

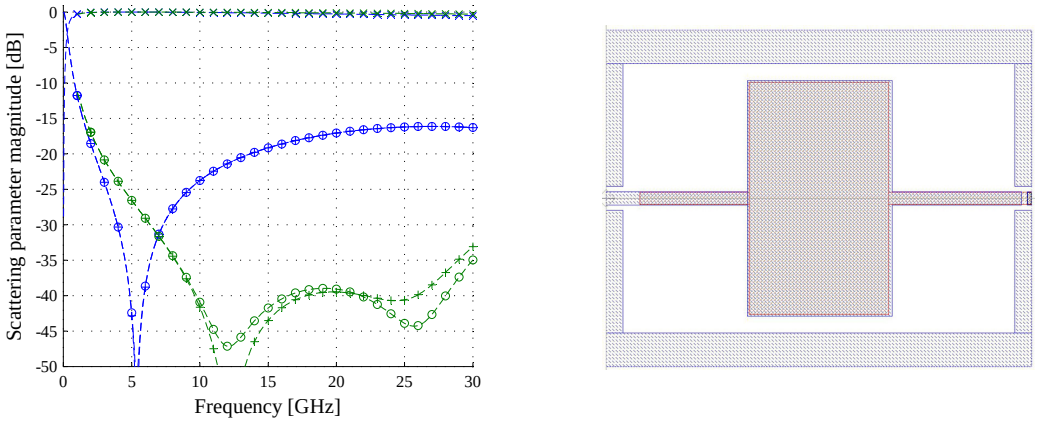
A JVS bias-tee requires a large valued capacitor to serve as a DC-block down to a few megahertz, but the capacitor needs to remain electrically small to maintain lumped performance up to 25 GHz. Likewise, the bias inductor needs to be a RF-choke at megahertz frequencies, but remain below its self resonant frequency (SRF) to 25 GHz. To achieve this challenging bandwidth, several specialized circuit elements were designed. This section presents a broadband integrated bias-tee in superconducting niobium on silicon with a 3 dB passband from 2 GHz to more than 25 GHz, with >30 dB of DC port isolation from 2–25 GHz, measured including the cryoprobe structure discussed in Chapter 2. Larger coupling capacitors have been designed and fabricated with 3dB points as low as 180 MHz and can be incorporated into the bias-tee, at the cost of higher radiation loss.

A broadband "bow-tie" capacitor is discussed first and compared to a standard rectangular form factor metal-insulator-metal (MIM) integrated capacitor. After showing measurement and simulation results, the capacitor is combined with a broadband, planar-spiral inductor circuit to create the desired broadband, lumped-element, integrated bias-tee for JVS applications.

5.1.1 Broadband On-chip DC-blocking Capacitors

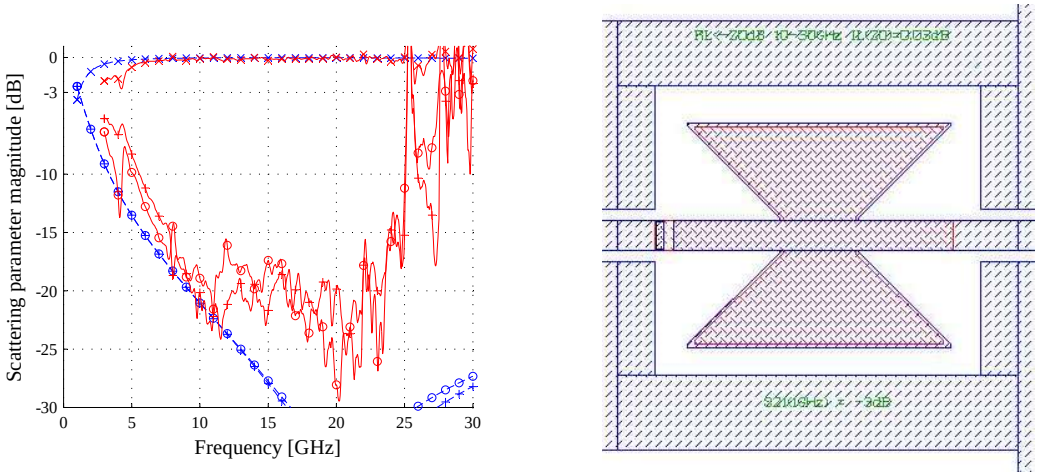
The challenge of realizing a broadband microwave blocking capacitor lies in balancing the lumped and distributed nature of the element. As any dimension of the inter-plate dielectric medium approaches $\lambda_g/8$, the distributed nature of the device becomes as important a design consideration as the lumped capacitance. Hence, to achieve a very broad bandwidth both must be taken into account, requiring a large lumped capacitance at lower frequencies which acts as an intelligent distributed circuit at higher frequencies.

A design in the NIST two layer IC process, Section 1.4.1 is needed that presents a large lumped capacitance at long wavelengths, but maintains a desirable distributed response as guided wavelength decreases. To this end, a "bow-tie" parallel plate capacitor structure is devised. In a



(a) (b)

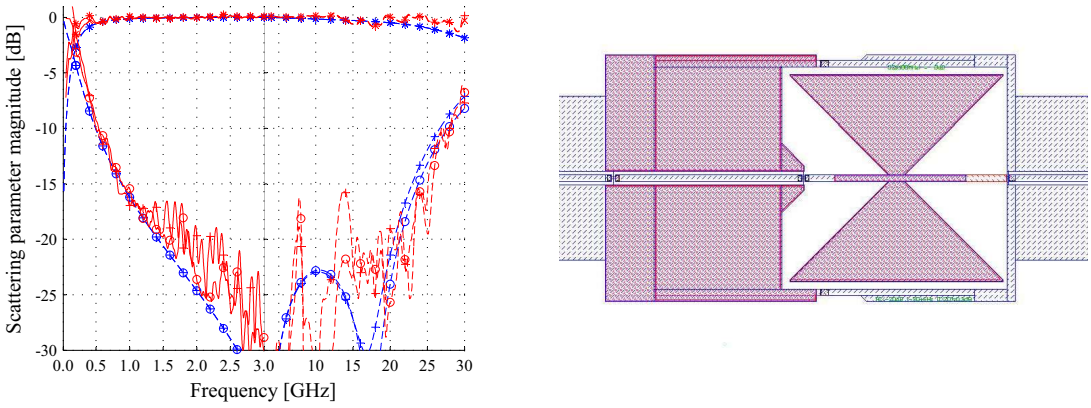
Figure 5.1: (a) A comparison of HFSS 3-D FEM simulated scattering parameters from the 300 µm × 400 µm bow-tie capacitor (green dashed lines), similar to Fig. 5.2 b, and a square capacitor (blue dashed lines) of the same area shown in b). S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. (b) A layout of the standard square 300 µm × 200 µm capacitor simulated in a).



(a) (b)

Figure 5.2: (a) 140 µm × 120 µm bow-tie capacitor, b), HFSS simulated S-parameters (blue dashed lines) and measurement results (red solid lines). S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. (b) A layout of the 140 µm × 120 µm bow-tie blocking capacitor structure used for DC blocking in the 10 V PJVS system, measured and simulated in a).

bow-tie capacitor the initial overlap of the plates starts small at their intersection point, and grows radially to present a larger overlap to waves at lower frequencies. Figure 5.1 a presents a comparison of simulated S-parameters of the 300 µm × 400 µm bow-tie capacitor and a standard rectangular 300 µm × 200 µm parallel plate capacitor of the same plate area shown in Fig. 5.1 b.



(a) (b)

Figure 5.3: (a) A comparison of measured and simulated scattering parameters from the 500 µm × 500 µm bow-tie capacitor. Bow-tie capacitor HFSS 3-D FEM simulated data (blue dashed lines), and measured data (red solid lines) using 4 K TRL calibration on chip. S_{11} is marked with ∘, S_{21} is marked with ×, S_{21} is marked with ∗, and S_{22} is marked with +. (b) A layout of the GSG 500 µm × 500 µm blocking capacitor structure targeted for DC-blocking in the acJVS system.

Figure 5.2 a compares measured and simulated s-parameters of a smaller 140 µm × 120 µm bow-tie capacitor for PJVS applications shown in Figure 5.2 b. This PJVS DC-block has a low frequency 3 dB cutoff of 2 GHz and an average measured IL over the 15–22 GHz band of 0.1 dB. For all the layouts in this chapter red ⧅ hatch is Nb1, black ⊞ hatch is Nb1-2 via, blue ⧄ hatch is Nb2 and green ⧈ hatch is AuPd.

A significant effort was dedicated to searching for a physically intuitive circuit model for this device. The literature [84, 85, 86] offers several lumped-element and distributed circuit models for high frequency capacitors, but none provided adequate performance modeling without the addition of many parametrically fit elements that are difficult to link to the geometry. In the end, it was decided that without a clear contribution to the understanding of the device a circuit model is no more helpful to the designer than the S-parameter results of a 3D HFSS simulation.

For the acJVS systems the digital ΔΣ bit-stream requires a much lower 3 dB cutoff frequency than for PJVS systems. For this application, several larger bow-tie capacitor structures with ground-signal-ground (GSG) DC-blocking were designed. The largest, shown in Figure 5.3 b with a 500 µm × 500 µm extent, has a 3 dB cutoff frequency of 180 MHz. While it has a much

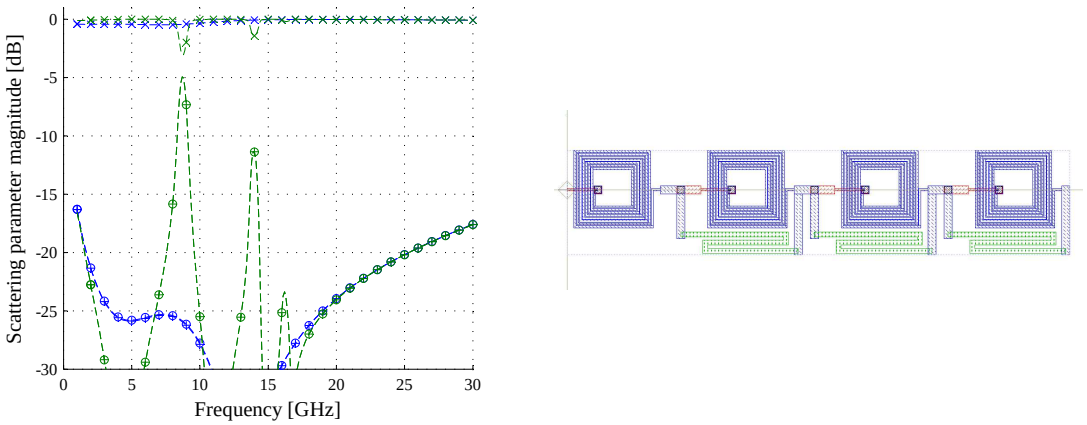
larger pass band than the PJVS capacitor in Fig. 5.2, this structure suffers from significant radiation loss, 0.6 dB at 20 GHz, due to the large distance between the center conductor current, and its ground plane return current. Figure 5.3 a shows a comparison of the measurement and simulation results for this device. At the low end of the band, measurement artifacts due to the resonant length of the cryoprobe are evident, as mentioned in Chapter 2. These capacitors were eventually integrated with acJVS arrays for further testing, as discussed in Section 7.2.

5.1.2 Broadband Bias Inductors

In general, high quality factor inductors with large inductance values and high SRF are very difficult to design and fabricate. As discussed previously, superconducting niobium affords the IC designer serious advantages in this realm as compared to conventional CMOS and even specialized GaAs processes. The NIST QV IC process, discussed in Section 1.4.1, can achieve very fine coil pitches while maintaining nearly lossless performance. Despite the gains afforded by superconductivity, geometric limitations still bring the self resonant frequency (SRF) of large (>10nH) inductors down into the 0–30 GHz band of interest.

Within the constraints of the NIST QV IC process, typical planar spiral inductors in the RF path have 5 μm wide conductors (to avoid saturating the supercurrent at typical on-chip power levels) and 1.5 μm spacing between turns as a compromise between area and inter-turn capacitance. In the bias inductors, 3 μm conductors with 1 μm spacing are used to achieve 7 nH inductors in a 100 μm × 100 μm area with a SRF above 40 GHz. Unfortunately, an inductance on the order of 50–100 nH is required to achieve low frequency bias-tee isolation into the megahertz frequency range.

In order to decrease the low frequency limit of the bias-tee, multiple inductors in series are required. Unfortunately, as high Q inductors are placed in series, the higher-order resonances due to the capacitive parasitics creep into the band of interest. In order to combat this effect, a standard de-Q-ing technique was employed by adding 100 Ω resistors in parallel with all but the first inductor, as shown in Fig. 5.4 b. This solution preserves the broad high frequency bandwidth,



(a) (b)

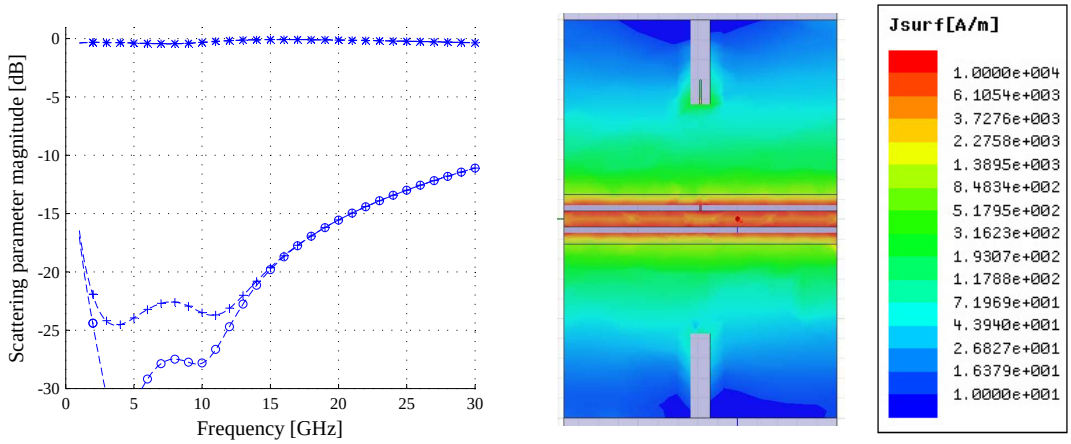
Figure 5.4: (a) A comparison of simulated scattering parameters for the bias-tee inductor circuit shunting a 50 Ω transmission line. Hybrid simulated data without the de-Q-ing resistors is shown in green dashed lines, while the blue dashed lines show the simulation results from the circuit in b). S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. (b) A layout of the bias inductor circuit with de-Q-ing resistors.

the superconducting path at DC, and is low loss in the 10-40 GHz band, but suffers ∼0.25 dB of loss in the de-Q-ing resistors below 10 GHz. Figure 5.4 a shows a comparison of inductor circuit simulations with and without the de-Q-ing resistors. The additional low frequency loss is considered a reasonable trade-off for the improved bandwidth.

5.1.3 CPW Bias-tee Interconnects

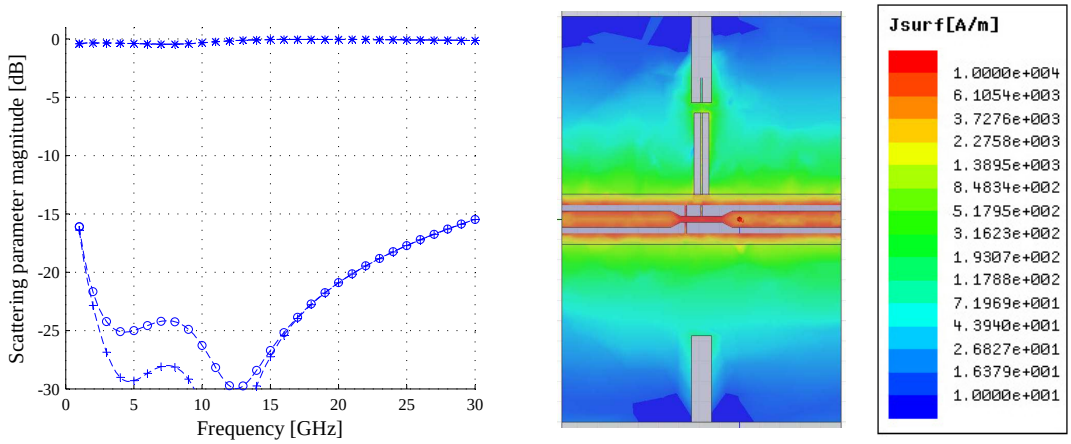
Yet another challenge faced when implementing a bias-tee in CPW is connecting to the center conductor confined within the ground planes. The NIST two conductor process allows for crossover interconnects, but the single 350 nm dielectric layer presents a significant capacitive discontinuity when the 3 µm bias line runs under the 100 µm wide ground plane, about 30 fF to ground. Canonically, as verified by HFSS simulations of these interconnects, the ground currents in a CPW line are strongly concentrated on the inner and outer edges of the ground plane.

The parasitic capacitance of the bias-tee interconnect can be reduced ten-fold by simply removing 90% of the ground plane over the interconnect, leaving narrow stips at the ground-plane edges to carry the current in the areas of natural concentration. To compensate for the remaining parasitic capicatance a small inductance was added by narrowing the center



(a) (b)

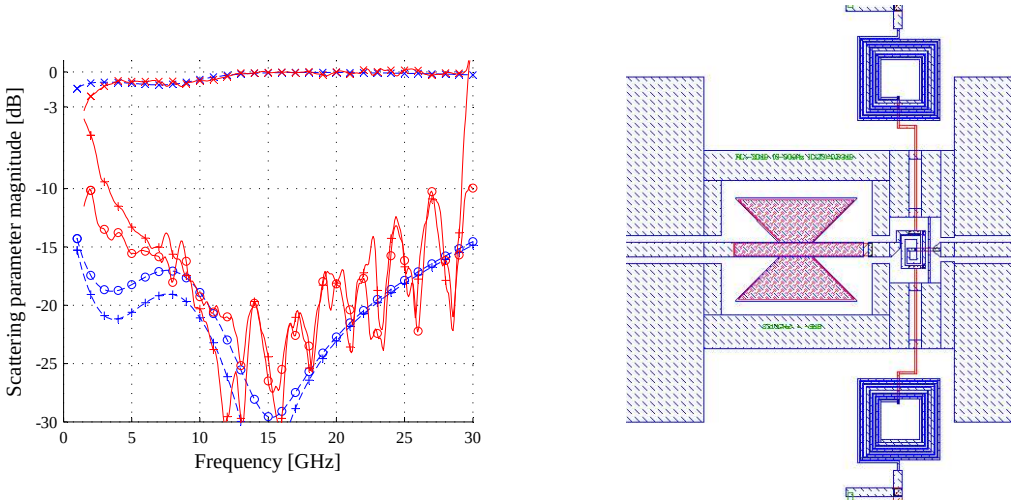
Figure 5.5: (a) Hybrid simulated S-parameters of standard bias-tee interconnect where S_{11} is marked with $\circ$, S_{21} is marked with $\times$, S_{12} is marked with $*$, and S_{22} is marked with $+$. (b) HFSS simulated surface currents for standard bias-tee interconnect.



(a) (b)

Figure 5.6: (a) Hybrid simulated S-parameters of bias-tee improved interconnect where S_{11} is marked with $\circ$, S_{21} is marked with $\times$, S_{12} is marked with $*$, and S_{22} is marked with $+$. (b) HFSS simulated surface currents for improved ground plane cutout bias-tee interconnect.

conductor at the attachment point, forming a LC transmission line of the appropiate impedance. Figures 5.5 and 5.6 show before and after 3D surface current simulations of this structure in a $50\,\Omega$ transmission line and hybrid simulation results from the two cases. These hybrid simulations load the DC port with the inductor structure discussed in Section 5.1.2. Similar methods were used to design bias-tees interconnects spanning an impedance range of 10–$85\,\Omega$.



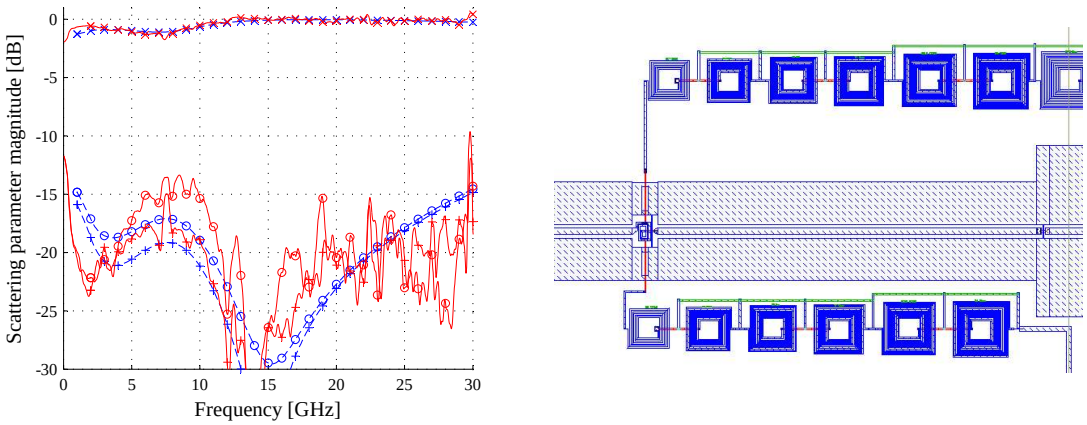
(a) (b)

Figure 5.7: (a) A comparison of simulated and measured scattering parameters from the PJVS bias-tee. Hybrid simulated data (blue dashed lines), and measured data (red solid lines) using 4 K TRL calibration on chip. S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. (b) A layout of the PJVS bias-tee using the 140 µm × 120 µm bow-tie capacitor and four 7 nH inductors, where the upper three are shunted with 100 Ω resistors as shown in Fig. 5.4 b.

5.1.4 Broadband Bias-tee Implementation

A broadband bias-tee using these components has been built and tested, and is in use in various forms in the NIST PJVS and acJVS systems. Two typical implementations were broken out for sub-circuit testing: one for PJVS applications with the 140 µm × 120 µm bow-tie capacitor and two sets of four series 7 nH inductors, and one for acJVS applications with an off-chip connectorized commercial blocking capacitor and two larger bias-inductor circuits for greater low-frequency isolation. These dual bias inductor configurations facilitate a four-wire measurement with the DC bias current applied to one bias-line and the output voltage measured on the other bias-line.

Figure 5.7 a shows a comparison of the hybrid simulation and measured device results for the 250 µm × 600 µm PJVS bias-tee shown in Fig. 5.7 b. This device exhibits a -3 dB passband from 2–30 GHz, with less than 0.5 dB of loss from 3-12 GHz, less than 0.2 dB of loss from 12–30 GHz, and better than -15 dB match from 10–22 GHz. The measured and simulated results for the 1 mm × 2 mm acJVS low-frequency bias-tee, shown in Fig. 5.8 b, are compared in Fig. 5.8 a.



(a) (b)

Figure 5.8: (a) A comparison of simulated and measured scattering parameters from the acJVS bias-tee. Hybrid simulated data (blue dashed lines), and measured data (red solid lines) using 4 K TRL calibration on chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$. (b) A layout of the 1 mm $\times$ 2 mm acJVS bias-tee using the the six 7–10 nH inductors in the voltage tap and ten 7–40 nH inductors in the current tap, where all the inductors but the smallest are shunted with 100 Ω resistors.

These on-chip bis-tee structures are now in use in the field in NIST PJVS and acJVS systems. For comparison, the measured s-parameters of a commercial CPW surface mount bias-tee are shown in Figure 5.9. This implementation, with an ATC 545L [87] broadband blocking capacitor and a Coilcraft BCL-802 [88] conical inductor, is used in Section 6.7. In the 15–22 GHz band-of-interest the on-chip PJVS bias-tee significantly out-performs the commercial solution. The low frequency corner of the commercial bias-tee is below the 50 MHz cutoff frequency of the VNA, but is measured using an analog gain-phase meter to be 500 kHz when integrated with the Avago AMMP-5024 amplifier, Fig. 6.8. This device has a 5 mm $\times$ 11 mm board footprint.

5.2 CPW Corners and CPW Ground-plane Ties

Printed circuit corners require special attention to minimize reflections due to parasitic effects and higher order mode excitation [89, 90]. Minimum bend radii, compensated corners, and chamfered corners can all be used to ensure that transmission line corners do not degrade the microwave performance of the circuit. In non-grounded CPW, the mainstay of the NIST QV IC process, it is also critical to ensure that the ground currents remain balanced by providing ground

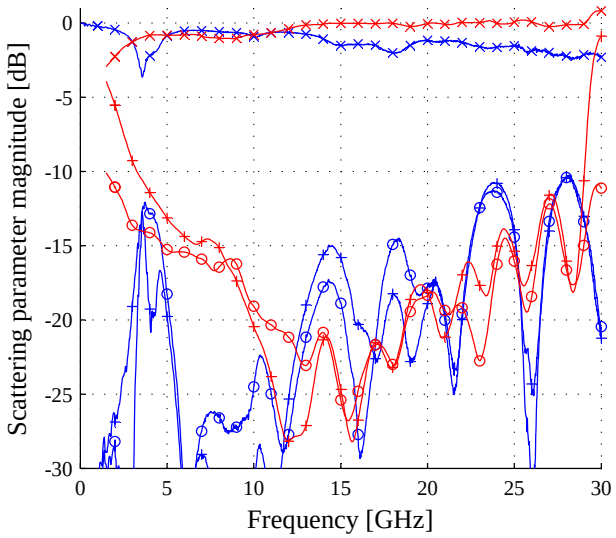
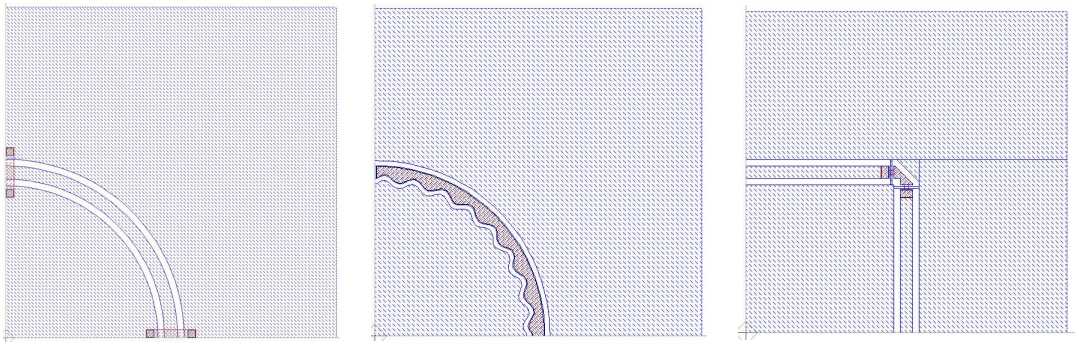


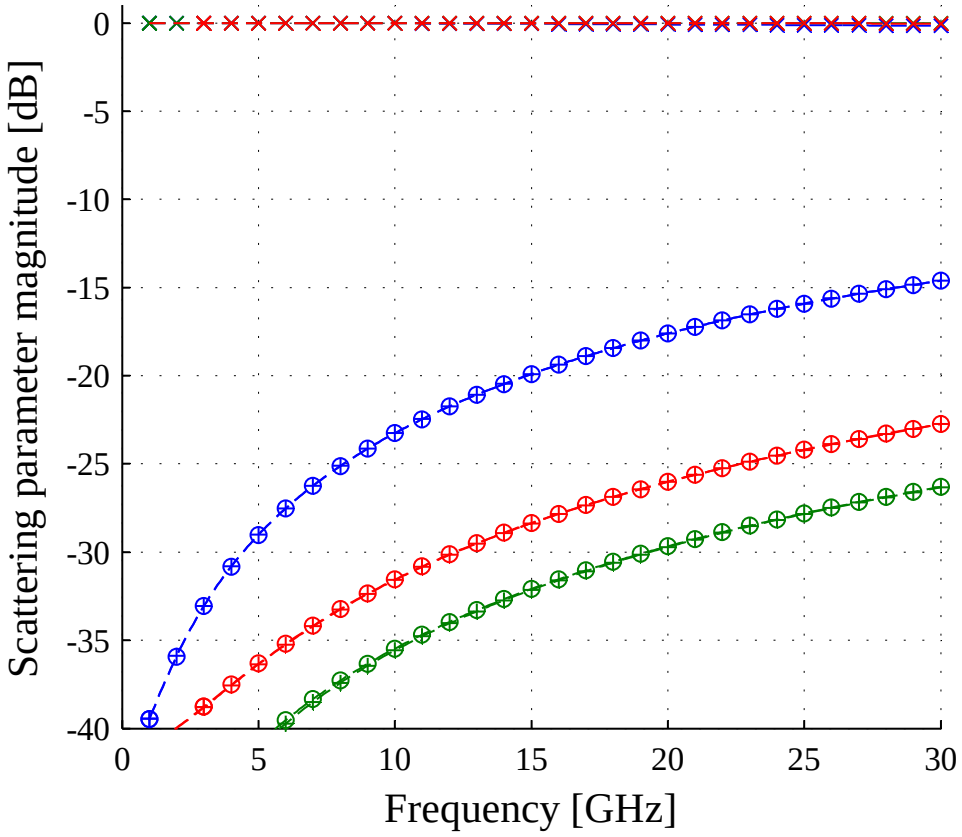
Figure 5.9: A comparison of measured scattering parameters from the PJVS bias-tee shown in Fig. 5.7 b (red solid lines), and measurements of an ATC 545L and Coilcraft BCL-802 on RO4350 CPW (blue solid lines). S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and insertion loss is marked with $+$.

ties on each side of a discontinuity, e.g. a corner or a lumped-element, and a minimum of $\lambda/4$ at the maximum desired frequency of operation to avoid $\lambda/2$ resonant slot-line modes. It should be noted that HFSS simulations can be misleading with respect to slot-line mode problems; all wave-port edges in the simulation domain are numerically forced to a global ground potential, very effectively damping slot-line modes unless specific measures are taken to observe them.

Several different corner approaches have been tried over the years in NIST JVS IC designs. Early designs had simple circular swept bends at the ground plane radius, shown in Fig. 5.10 a, which were were easy to design, but marginal in performance and marginal in IC mask generation time. These were replaced by swept bends with a sinusoidally modulated inner slot, shown in Fig. 5.10 b, to compensate for the differential path length in the inner and outer slots. These corners, while improved in performance, are very "expensive" in terms of IC mask generation time due to their highly non-manhattan geometry. Recently, a chamfered CPW corner [89], shown in Fig. 5.10 c, has been designed to achieve the performance of the sinusoidally modulated bend in a manhattan and 45° geometry. Manhattan geometry requires significantly less IC



(a) (b) (c)



(d)

Figure 5.10: (a) A screen capture of the layout of a simple swept bend. (b) A screen capture of the layout of a sinusoidally modulated bend. (c) A screen capture of the layout of a chamfered CPW bend with improved ground ties. These bends all have a 200 µm bend radius. (d) A comparison of HFSS simulated scattering parameters of: a) a swept corner (blue dashed lines), b) a sinusoidally modulated corner (red dashed lines), and c) a chamfered corner (green dashed lines). S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$.

mask generation time, reducing fabrication costs. Figure 5.10 d compares the HFSS simulated performance of the three corners.

As with the CPW bias-tee interconnects, Section 5.1.3, the major problem with ground-plane ties in the NIST QV IC process is the rather large capacitance to ground where the ground tie overlaps the center conductor. Again, the effects of this discontinuity can be minimized by minimizing the overlap area: tapering both the center conductor and the ground tie under it. This structure, utilized in the chamfered corner in Fig. 5.10 c, effectively trades the CPW slot capacitance for the overlap capacitance of the ground tie yielding a ground tie structure with negligible power reflection.

5.3 Lossy Termination Circuits

The 2 Ω/□ AuPd resistor layer in the NIST IC process allows complex on-chip lossy structures to be realized. These are used in various ways; the termination resistors at the end of JJ arrays [64], Wilkinson divider isolation resistors (Section 3.2.1), multi-port circuit characterization attenuators (Section 3.3), and power-detecting terminations.

5.3.1 Array Termination Resistors

The primary design consideration with the array termination resistors is maintaining adequate size for power handling while remaining electrically small. In PJVS array termination applications it is also desirable to integrate a large DC-blocking capacitor with the termination resistor to combine the DC output voltages of many arrays. Maximum current densities in the 150 nm thick AuPd traces are ∼10 mA/μm as measured by DC fusing current tests. From this result, a 50 Ω termination with a single resistor trace requires a minimum width of 6 μm to handle the maximum on-chip RF power of ∼200 mW. In array terminations, 10 μm wide resistor traces provide a comfortable design margin. By splitting the termination into a pair of 100 Ω resistors, one to each ground plane, and folding them into the center conductor and ground plane of the CPW total termination size can be kept under $\lambda/20$ at 20 GHz with 10 μm resistor widths.

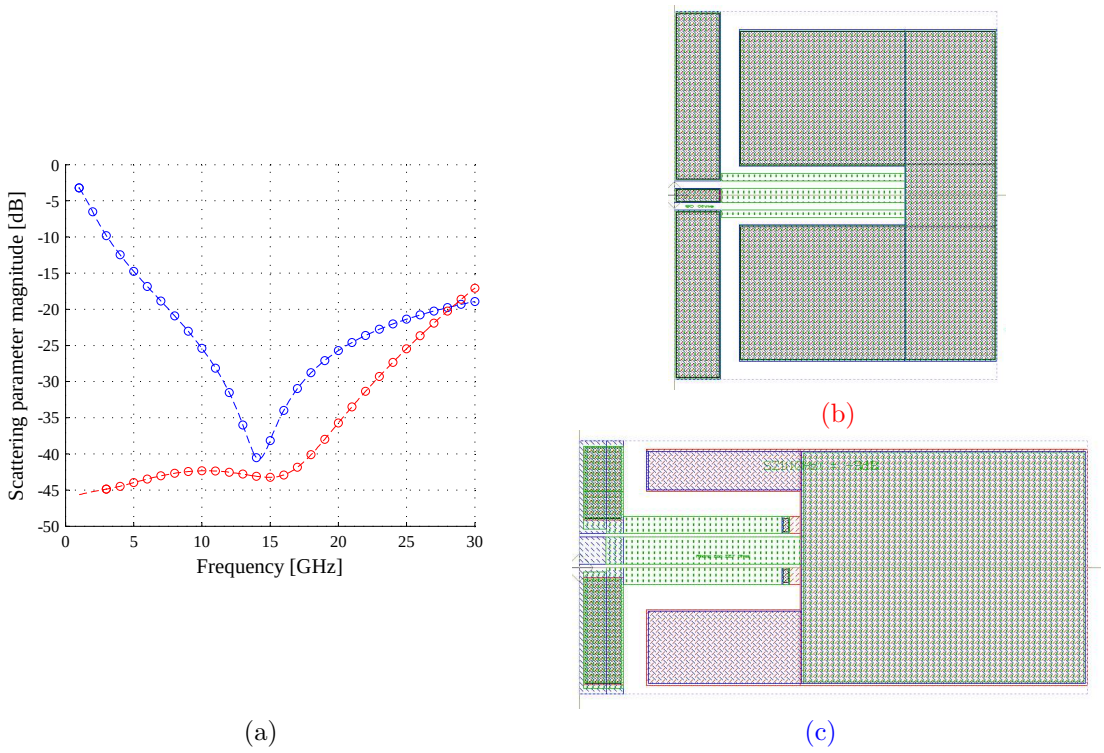


Figure 5.11: (a) HFSS simulated S_{11} of the 50 Ω termination, in red, and the 22 Ω AC coupled termination, in blue. (b) A screen capture of the 200 µm × 200 µm layout of a 50 Ω termination. (c) A screen capture of the 85 µm × 200 µm layout of a 20 Ω AC coupled termination.

In order to ensure the resistor stays as close as possible to the 4 K helium bath temperature, array termination resistors are anchored thermally to the silicon chip by etching away the SiO_2 native oxide under large Nb pads tied to the ends of the resistors. Figure 5.11 b shows a large 50 Ω termination resistor for an acJVS test array, while Fig. 5.11 c shows a 22 Ω AC coupled termination for PJVS array applications. Simulated S-parameters of these two structures, scaled to the desired impedance, are shown in Figure 5.11 a.

5.3.2 Attenuators

In microwave design a broadband, well-matched element is invaluable, even with a penalty in loss. In characterization circuits the use of an attenuator can provide a matched termination, while still allowing measurable amounts of power to be transmitted, e.g. Section 3.3.2. To this end canonical lumped T-network attenuators were designed and fabricated with -3 dB, -5 dB, and -10 dB values in a 50 Ω system. These devices proved to be not only useful in characterization circuits, but

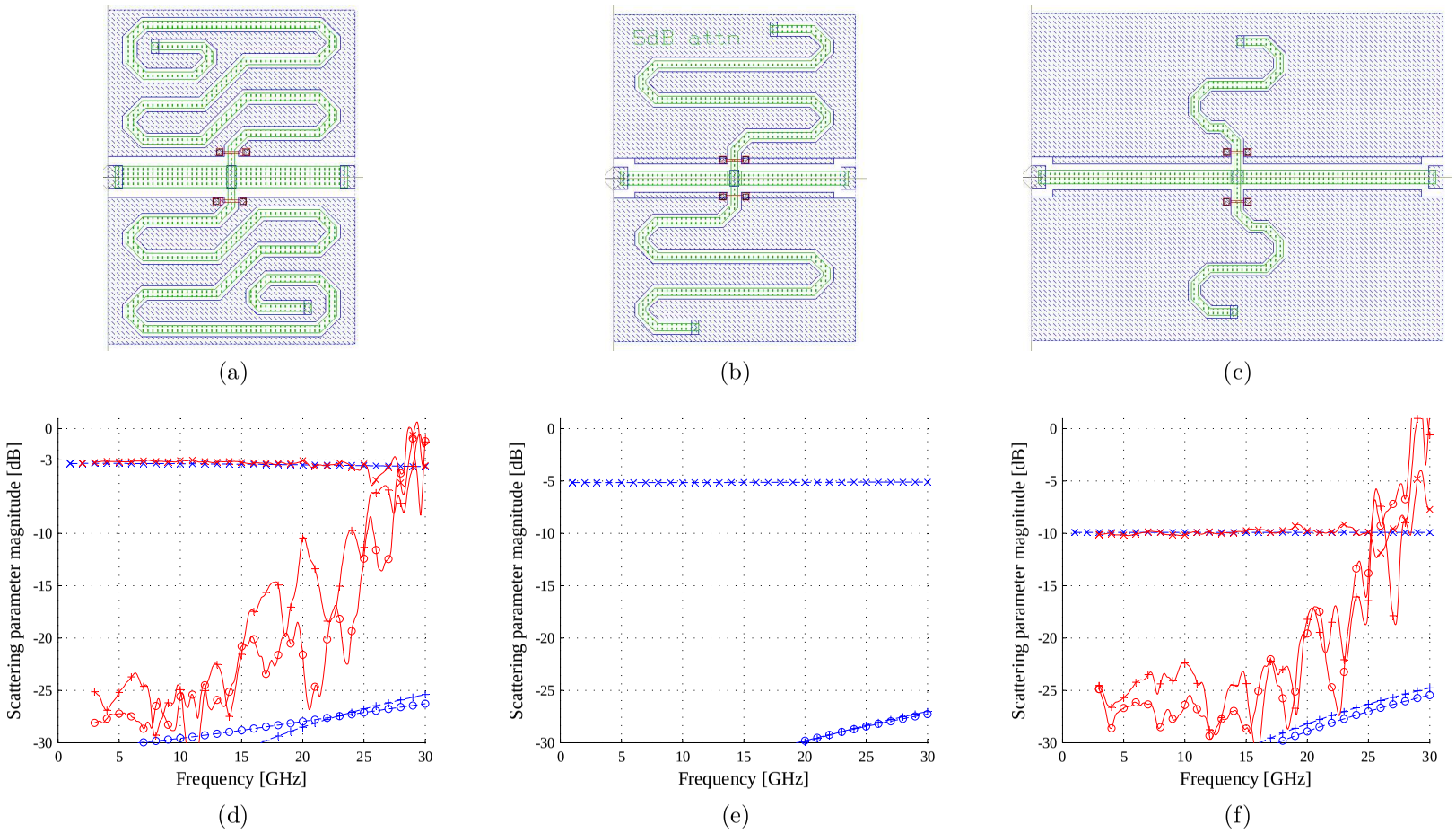


Figure 5.12: (a) A layout of a 3 dB attenuator. (b) A layout of a 5 dB attenuator. (c) A layout of a 10 dB attenuator. These attenuators are integrated into a CPW transmission line 230 µm wide from ground-plane-edge-to-ground-plane-edge. (d) 3 dB attenuator HFSS simulated S-parameters, in blue dashed lines, and measurement results, in red solid lines. (e) 5 dB attenuator HFSS simulated S-parameters in blue dashed lines. (f) 10 dB attenuator HFSS simulated S-parameters, in blue dashed lines, and measurement results, in red solid lines. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} loss is marked with $+$.

also invaluable as on-chip calibration verification structures. The appropriate T-network resistor values, series and shunt respectively, can be calculated using the following equations: [91, 92]

$$Z^{\mathrm{T}}_{\mathrm{series}} = Z_0 \cdot \tanh\frac{a}{2} \text{ and } Z^{\mathrm{T}}_{\mathrm{shunt}} = \frac{Z_0}{\sinh a} \ . \tag{5.1}$$

While not used here, due to increased component count in a CPW implementation, the Π-network equations for the shunt and series resistors, respectively, are:

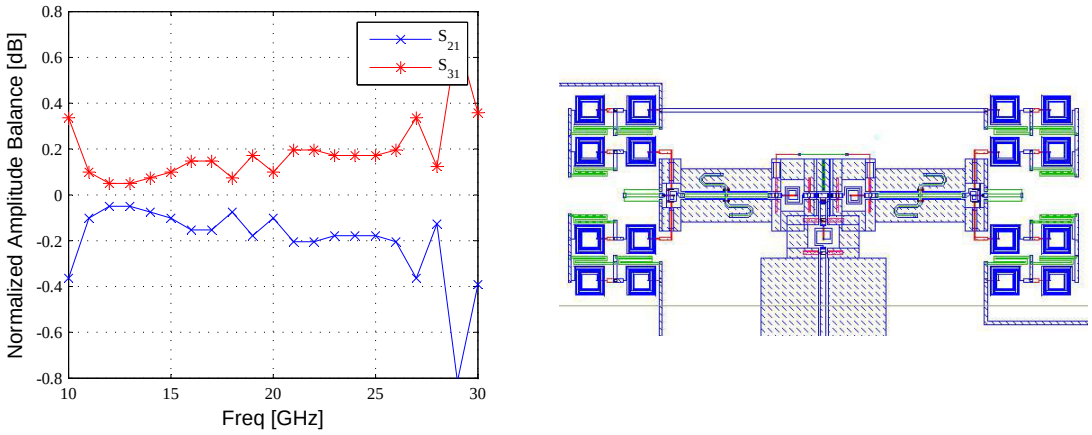
$$Z^{\Pi}_{\mathrm{shunt}} = \frac{Z_0}{\tanh\frac{a}{2}} \text{ and } Z^{\Pi}_{\mathrm{series}} = Z_0 \cdot \sinh a \ . \tag{5.2}$$

Figure 5.12 summarizes the results of this work: Fig. 5.12 a is a layout of a 3 dB attenuator, Fig. 5.12 b shows a 5 dB attenuator, and Fig. 5.12 c is a 10 dB attenuator. Figures 5.12 d-f show S-parameters from the respective HFSS simulations versus the measured results from fabricated devices.

5.3.3 Power Detecting Terminations

While the on-chip 50 Ω termination, discussed in Section 5.3.1, is critical to building and measuring devices in the MMIC environment, it can still be improved for specific applications. The JJ microwave-dependent IV curve relationships, discussed in detail in Section 2.3, can be used as an on-chip scalar-power-detector. This useful JJ feature inspired the development of an on-chip power sensing termination, shown in Fig. 5.13 b. This device utilizes the 10 dB attenuator (Section 5.3.2) to maintain input match, then a modified bias-tee interconnect cell (Section 5.1.3) that integrates two DC taps with two JJ stacks in between them, and a final 50 Ω termination resistor similar to those described in Section 5.3.1. While these JJ power detectors are difficult to calibrate absolutely, it is easy to obtain a relative calibration by simply including an auxiliary input port on the test chip terminated in the power detector.

The precision of the power measurements taken with this device is limited by JJ barrier thickness variations across the wafer and amplitude variations of the microwave source, power amplifier, and cryoprobe over the several hours of testing required to obtain all the DC IV Shapiro-



(a) (b)

Figure 5.13: (a) Measured power division balance on chip for the Wilkinson divider with counter-wound inductors simulated in Fig. 3.3 a. This measurement corresponds closely to the simulation results shown in Fig. 3.3 b. (b) The layout of the test circuit with the on-chip power detecting terminations and the 300 µm × 400 µm Wilkinson divider DUT.

step-corner sweeps with respect to power, over frequency. Figure 5.13 a shows a power division balance measurement of the Wilkinson power divider with counter wound output inductors from Fig. 3.3 a. This plot is obtained by assuming that the $0.5I/I_C$ step height point corresponds to equal power-on-chip as calculated from JJ IV power sweeps at each frequency point. Fig. 5.13 b is a layout of the test circuit with the power detecting terminations on the left and right, and the Wilkinson divider DUT in the center.

5.4 NIST QV IC Process Characterization Circuits

Another challenge of MMIC design is measuring the low-level model parameters of a process. Before the development of the more complex circuits described here it was essential to characterize the IC medium and ensure that transmission line impedance, loss, capacitance, etc. were being modeled adequately. To this end, a collection of process characterization circuits were devised to convert difficult-to-measure geometric and material properties into easy-to-measure electrical quantities.

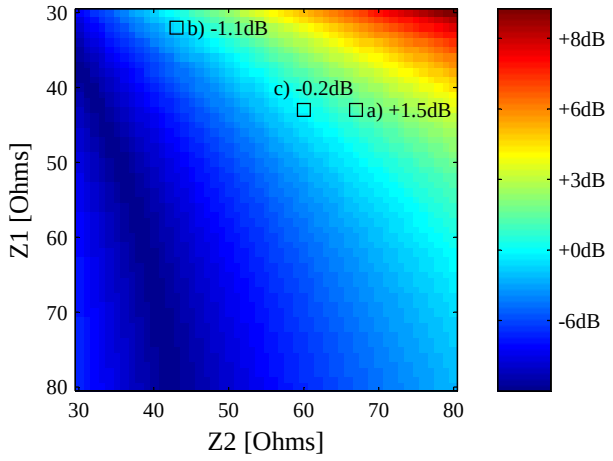


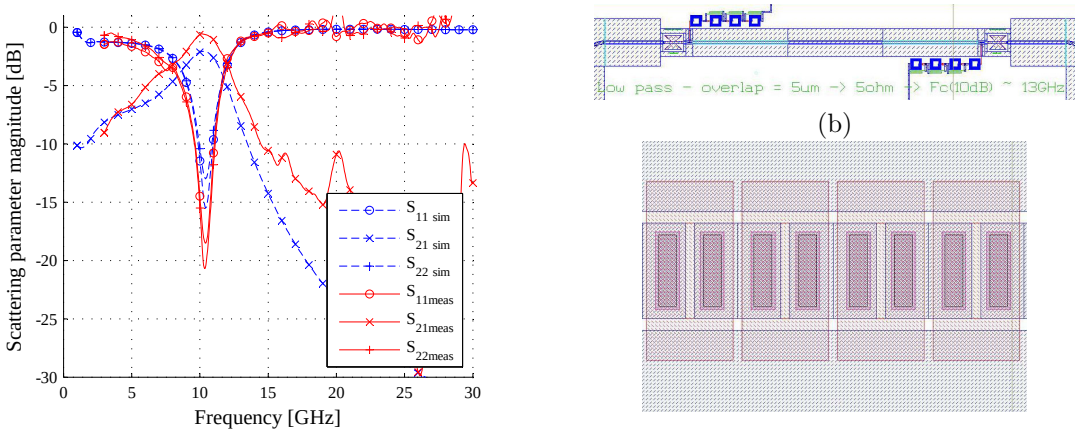
Figure 5.14: A contour plot of branch-line $|S_{21}|/|S_{31}|$ as the transmission-line impedances Z_1 and Z_2 are varied with measured points marked. The center conductor width of the CPW is fixed at 16 µm, and the series and shunt transmission line gaps, respectively, are varied as follows: a) 6 µm and 30 µm, b) 2 µm and 6 µm, and c) 6 µm and 20 µm.

5.4.1 Branchline Hybrid Coupler

The division ratio of a 90° branch-line hybrid coupler [93] at resonance is strongly dependent on the impedance ratio of the through and coupled branch-lines, with characteristic impedances Z_1 and Z_2 respectively. While this ratiometric measurement does not give an absolute measure of transmission line impedance, by fabricating a selection of CPW geometric ratios the the geometric ratios can be fitted to the correct section of the impedance ratio curve. In the simplified matched case where $Y_1^2 - Y_2^2 = Y_0^2$, the division ratio is governed by the following equations [74]:

$$S_{21} = -j\frac{Y_0}{Y_1} \text{ and } S_{31} = -\frac{Y_2}{Y_1} \ . \tag{5.3}$$

Figure 5.14 shows a contour plot of the branch-line amplitude imbalance $|S_{21}|/|S_{31}|$ in terms of the Z_1 and Z_2 transmission line impedances. The marked points are fabricated and measured devices. This branch-line hybrid technique is useful for characterizing transmission line impedances relatively near Z_0 =50 Ω, approximately 30–80 Ω.



(a) (b) (c)

Figure 5.15: (a) A comparison of ideal transmission-line simulation, in blue dashed lines, and measured, in red solid lines, scattering parameters of the 5–50 Ω stepped impedance filter used to verify the 5 Ω transmission line geometry. (b) A layout of the 5–50 Ω stepped impedance filter with 800 µm transmission-line sections. (c) The 5 Ω JJ loaded modified CPW transmission line geometry with 5 µm of Nb1 (red) center conductor underneath the Nb2 (blue) ground plane.

5.4.2 Stepped Impedance Filters

Another impedance sensitive circuit that is useful for characterizing a wider range of impedances is a stepped-impedance filter. For short line lengths, $\leq \lambda_g/8$, a high-impedance transmission-line segment can be approximated as a series inductive reactance, X, and a low-impedance segment as a shunt capacitive susceptance, B: [75]

$$X \approx Z_0 \cdot \beta l \text{ and } B \approx Y_0 \cdot \beta l \tag{5.4}$$

By inspection, if the electrical length, βl, is fixed, and one line is fixed at a known impedance, 50 Ω, then the impedance of the other transmission line segment can be calculated by measuring the LC cutoff frequency of the filter. This technique was used to characterize the low-impedance end of the tapered JJ arrays, down to Z_0 =5 Ω [64]. Figure 5.15 a shows an ideal transmission line simulation, versus measured results for a 5–50 Ω stepped impedance filter with 800 µm sections, $\lambda_g/8$ for a 20 GHz maximum operation frequency. This test structure, shown in Fig. 5.15 b, was used to validate both the transmission line geometry for a given impedance, as well as the layer-by-layer-planarized HFSS modeling technique that was used throughout this thesis.

5.4.3 Transmission-line Loss

In order to measure the loss of typical transmission line topologies in the NIST superconducting IC process, a very long 8 cm on-chip 50 Ω meander line was constructed. A linear fit to the measured IL data yields a measured loss of 0.08 dB/cm at 20 GHz. In a typical PJVS 10 V chip design, there is approximately 8 mm of transmission line in the on-chip power division tree to feed each array, or a maximum IL of 0.07 dB. This substrate loss is very small when compared to resistive element losses and mismatch-loss for the physical size of circuits designed in this thesis, so this substrate and conductor loss is typically neglected.

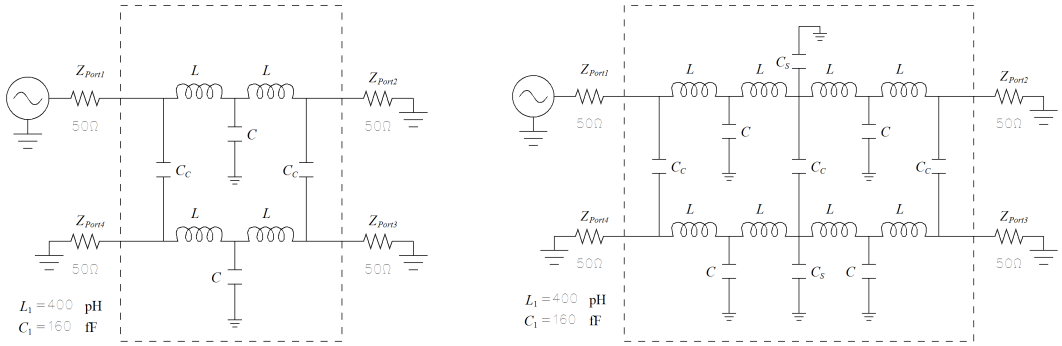
5.5 Lumped-element 20 dB Directional Coupler

Thus far, several hybrid coupler designs have been discussed for use as power dividers and process characterization vehicles. Another useful coupler application is a low coupling-ratio hybrid to tap-off a small portion of a signal for measurement purposes without detrimentally affecting the system. A 20 dB lumped element hybrid coupler is ideal for this task; the coupling is high enough to yield measurable coupled output powers, but low enough to only redirect 1% of the power in the system under test. While this could be done with distributed elements, as described in Section 5.4.1, such an implementation tends to be very large and narrow-band. Instead, as in Chapters 3 and 4, a lumped-element topology was choosen as a more efficent use of MMIC real estate. The basic loosely coupled lumped-element hybrid is shown in Fig. 5.16 a. The equations for calculating the 20 dB hybrid circuit elements, are as follows [94]:

$$L = \frac{Z_0}{2\pi \cdot f} \ , \ C = \frac{1}{2\pi \cdot f \cdot Z_0} \ , \text{ and } C_C = \frac{10^{CF/20}}{2\pi \cdot f \cdot Z_0} \ . \tag{5.5}$$

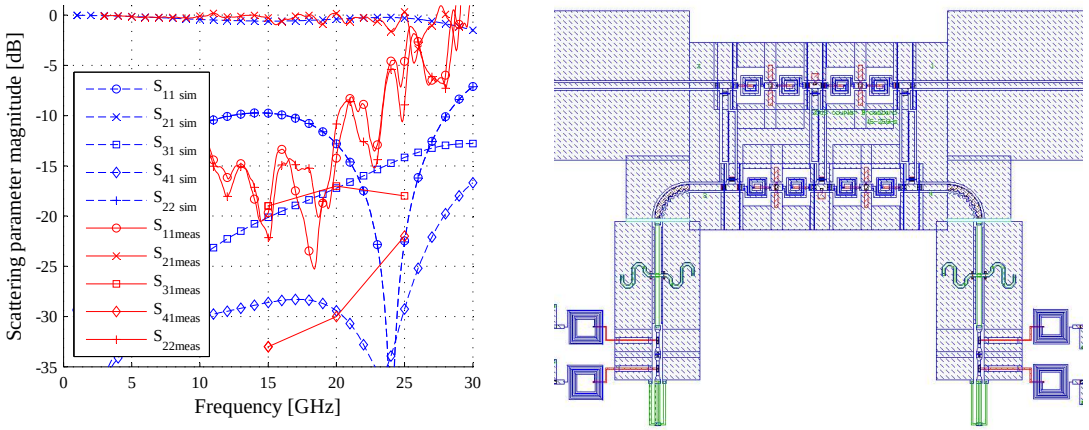
where the coupling factor, $CF = -20$ in units of decibels.

To achieve a broader bandwidth and better isolation, a second identical hybrid is added in in series with the first, along with the additional tuning element C_S, which was used to optimize for bandwidth in simulation. A schematic of this broadband lumped-element 20 dB coupler topology is shown in Fig. 5.16 b. In order to realize the very small $C_C = 16$ fF with sufficient precision, a



(a) (b)

Figure 5.16: (a) A schematic representation of a canonical 20 dB lumped-element hybrid coupler. (b) The schematic of the improved bandwidth cascade 20 dB lumped-element hybrid coupler.

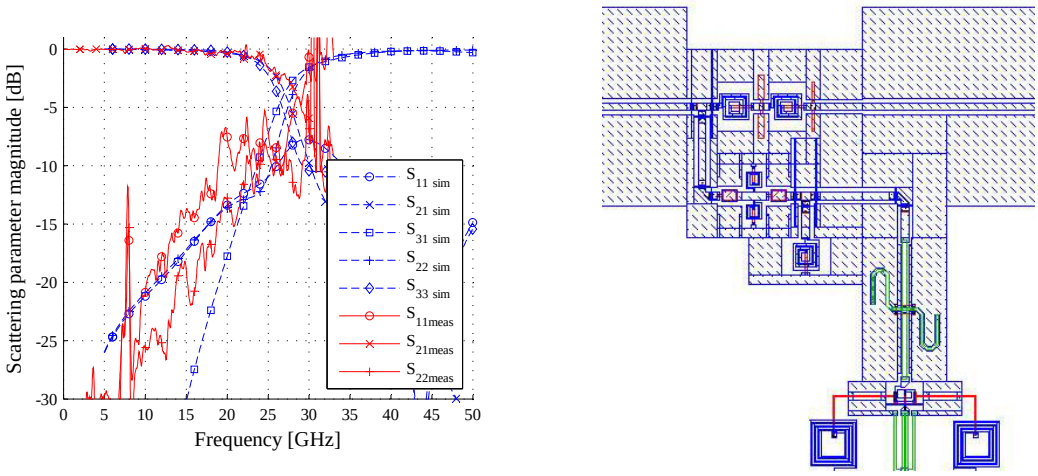


(a) (b)

Figure 5.17: (a) A comparison of simulated (blue dashed lines) and measured (red solid lines) scattering parameters of the 20 dB lumped-element hybrid in b). S_{31} and S_{41} were measured at 15, 20, and 25 GHz using the on-chip power detectors from Section 5.3.3. (b) A Layout 600 µm × 800 µm of the 20 dB lumped-element directional coupler in Fig. 5.16 b).

200 µm coupled line capacitor was used instead of a very small parallel plate capacitor to help mitigate process tolerance effects.

The broadband 20 dB hybrid in Fig. 5.17 b was fabricated with VNA test points on ports 1 and 2, while ports 3 and 4 were terminated with the power detecting termination from Section 5.3.3. Figure 5.17 a compares HFSS simulated and measured S-parameters for this 20 dB hybrid. The on-chip power detectors from Section 5.3.3 were used to measure the magnitude of S_{31} and S_{41} at 15, 20, and 25 GHz. This coupler exhibits very good bandwidth on the through port, and



(a) (b)

Figure 5.18: (a) 25 GHz diplexer HFSS simulated S-parameters, in blue dashed lines, and measurement results, in red solid lines. (b) A layout of the 400 µm × 400 µm lumped-element diplexer.

the coupled port is -18 ± 1 dB at the 15, 20, and 25 GHz measurement points. The isolation is marginal at only -30 dB at the 15 and 20 GHz, degrading to -22 dB at 25 GHz. While this device is usable as a scalar power sensor, it is not sufficiently directional to make useful forward and reverse wave measurements.

5.6 Lumped-element Diplexer

Often a frequency selective circuit is desired to split an input into multiple bands for different purposes, or conversely to combine multiple inputs in different bands on a single output or antenna. The simplest device in this category is a high-low diplexer. A high-low diplexer consists of a high-pass filter and a low-pass filter with cut-off frequencies such that the input is matched across the entire band. If one of the outputs of this device is terminated in a matched load it then becomes an absorptive filter, a useful device when dealing with the very broadband digital $\Delta\Sigma$ signals of the acJVS systems. More complicated duplexers and multi-band channelizers can be constructed by combining multiple bandpass filters with aligned corner frequencies.

As a proof of concept, a first-order, lumped-element, high-low diplexer at 25 GHz was designed and fabricated with the hybrid simulation methodologies discussed previously. The high-pass

section of this device could be combined with the broadband Wilkinson divider from Chapter 3 to divide the acJVS $\Delta\Sigma$ bitstream into two parallel arrays of JJs without reflecting the high frequency components that could interfere with the 10 Gbps bitstream generator operation. Figure 5.18 b shows a layout of the fabricated 25 GHz diplexer with the high frequency output terminated in the power sensing termination from Section 5.3.3. In Fig. 5.18 a the measured S-parameters are compared with the HFSS simulated results.

5.7 Summary

This chapter describes a number of useful circuits that were designed to contribute to NIST JVS systems development. MMIC design elements often ignored in the literature, e.g. bias-tees and DC-blocking capacitors, are critical to system performance and deserve requisite care in their implementation. In addition, canonical transmission line circuits can be used to simplify process characterization. This collection of circuits has been invaluable in the development of NIST JVS systems.

Chapter 6

An Investigation of MMIC Distributed Amplifier Design

Contents

This chapter presents an investigation of microwave distributed amplifier design as a gain stage in the microwave excitation chain of a JVS system. In this study a 4-stage, 20 GHz, distributed GaAs pHEMT MMIC amplifier with identical gate and drain transmission line topologies is evaluated [95]. The measured power gain of the fabricated amplifier is greater than 10 dB over a 1–20 GHz bandwidth. The measured saturated output power across this band is ∼10 dBm. To achieve the more rigorous bandwidth required by acJVS applications a custom implementation of the commercial Avago AMMP-5024 distributed amplifier was evaluated.

6.1 Introduction

One of the most common broadband microwave amplifier topologies is a distributed amplifier. In a distributed amplifier the transistor gate and drain capacitances are each incorporated into a LC equivalent transmission line. When properly matched to the external circuit, and phase matched to each other, this amplifier topology provides a flat broadband gain characteristic up to the low-pass LC cutoff frequency of the artificial transmission line. This extreme bandwidth comes at the cost of area, transistor count, and efficiency [75].

This chapter focuses on the design, layout, and testing of a distributed amplifier in TriQuint's TQPED MMIC 0.5 µm pHEMT process [96]. Using a 4-finger, 0.5 µm long by 15 µm wide, enhancement-mode transistor, a distributed amplifier is designed with the goal of operating to 20 GHz, power gain greater than 10 dB, and reasonable input/output matching. The final design utilizes four stages in a 1-2-2-3 topology (a 1-transistor first stage, 2-transistor second and third stages, and a 3-transistor output stage) to meet these specifications.

6.2 Amplifier Design

A typical design procedure for a distributed amplifier calls for creating LC-equivalent phase-matched transmission lines using the parasitic transistor capacitances C_{gs} and C_{ds} and either lumped or distributed transmission line elements as inductors [75]. This procedure can be

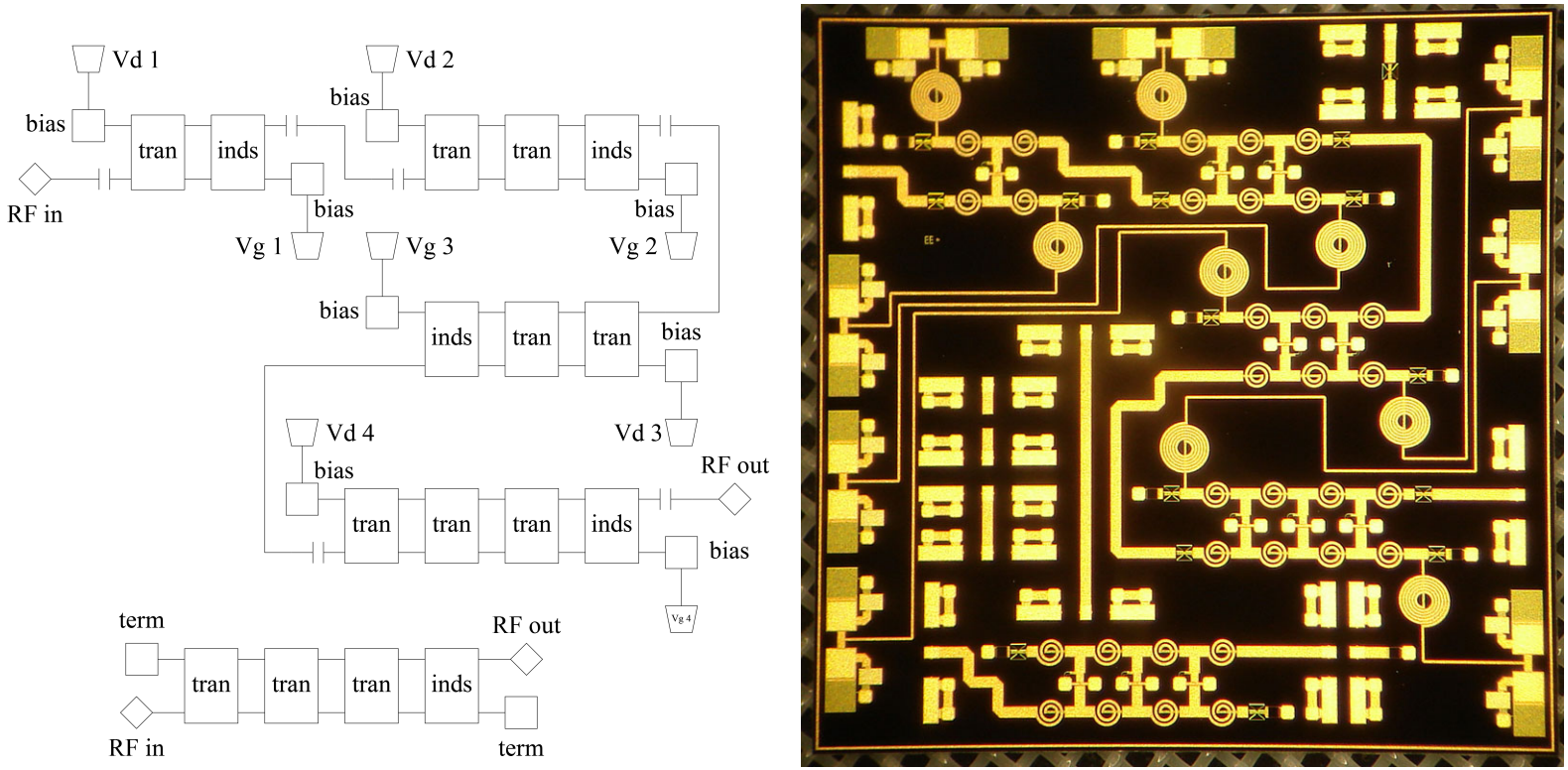
significantly simplified by adding external capacitors, C_{ext} to the transistor drain such that:

$$C_{gs} = C_{ds} + C_{ext} \ . \tag{6.1}$$

In this case the same transmission line topology and inductive cells can be used in both gate and drain transmission lines, simplifying the design and improving the chance of first pass success. This simplification significantly reduces the impact of transistor model inaccuracies since the passive, well defined C_{ext} typically dominates the parasitic device capacitance C_{ds} which may or may not be modeled accurately. In this topology the gate and drain transmission line phase matching is inherent to the circuit, rather than an additional constraint upon the system.

An additional advantage of this topology is that gate and drain lines are inherently broadband matched to each other. As such, interconnecting drain and gate transmission lines realizes a multistage distributed amplifier, without the need for interstage matching. Figure 6.1 b shows the distributed amplifier chip fabricated by TriQuint. The upper half of the die is dedicated to the four stage 1-2-2-3 transistor distributed amplifier. The lower LC transmission line is the gate line, and the upper LC transmission line is the drain line in each stage; the non-feed ends of both lines are terminated on-chip with a large coupling capacitor and a 50 Ω resistor to ground. The lower half of the chip includes an on-chip TRL cal kit and breaks out the single three transistor output amplifier for troubleshooting.

In order to characterize the 4x15 μm TriQuint E-mode pHEMT used in this design, the TOM3 device model from TriQuint was inserted into an AWR microwave office (MWO) testbed with ideal bias-tees and S-parameter ports. Evaluations of this testbed were used to choose the desired transistor sizing, bias point, and then extract C_{gs} and C_{ds} from the S-parameter response. This method neglects any changes in C_{gs} or C_{ds} due to amplifier saturation. This amplifier will be operated in the linear region, or lightly compressed, so this approximation was deemed acceptable. The extracted parameters for a 4x15 μm transistor at V_{gs}=0.8 V and V_{ds}=3.5 V are C_{gs}=210 fF and C_{ds}= 90 fF.



(a) (b)

Figure 6.1: (a) A hierarchal schematic of the distributed amplifier test chip, using cells shown in Fig. 6.2. (b) A micrograph of final 5 mm × 5 mm die fabricated by TriQuint. The upper half of the die is a four stage 1-2-2-3 transistor distributed amplifier. The lower half contains an on-chip TRL cal kit, and the distributed amplifier 3-transistor output stage.

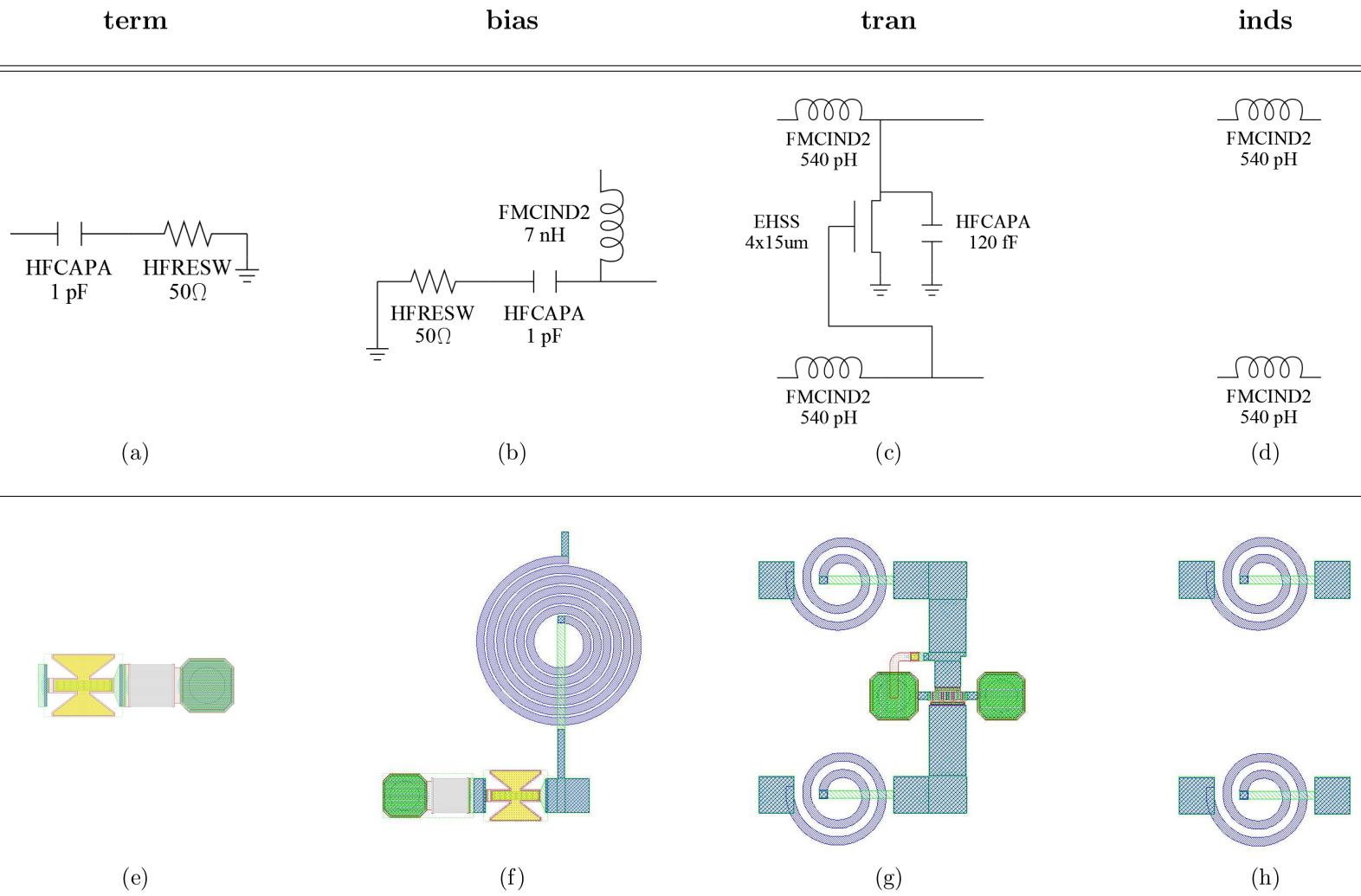


Figure 6.2: (a) Schematic of AC coupled termination. (b) Schematic of on-chip bias-tee cell with FMCIND2 model. (c) Schematic LC transistor cell with FMCIND2 model. (d) Schematic of final L cell with FMCIND2 model. (e) Layout of AC coupled termination. (f) Layout of on-chip bias-tee cell with FMCIND2 model. (g) Layout of LC transistor cell with FMCIND2 model. (h) Layout of final L cell with FMCIND2 model.

Utilizing these extracted parameters, an ideal LC transmission line can be constructed using planar spiral inductors. This design is constrained by:

$$Z_0 = \sqrt{\frac{L}{C}} \ , \tag{6.2}$$

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \ , \tag{6.3}$$

and equation 6.1, setting the characteristic impedance and cutoff frequency of the transmission line. Solving these equations with the extracted transistor parameters give L=540 pH and C_{ext}=120 fF for a 50 Ω line with a cutoff frequency approaching 20 GHz.

These ideal lumped elements were then converted into MMIC planar spiral inductors specifications using Spiralcalc [80] and an ideal parallel plate capacitor model integrated into the AWR TriQuint design kit. These MMIC lumped elements were integrated into a hierarchal design utilizing one transistor amplifier unit-cells with gate and drain transmission lines utilizing the TQPED_EHSS transistor, TQPED_HP_CAPA capacitor, and FMCIND2 inductor cells and associated AWR Microwave Office (MWO) [81] models. The overall topology and the interconnect were controlled at the higher level to define the design. This allowed for improved tuning and ensured that all stages remained identical through the design process. Figure 6.2 shows the schematic and layout of cells used in the hierarchal schematic, Fig. 6.1 a: the on-chip bias-tee, the transistor LC transmission line cell, the inductor cell, and the termination cell. The final fabricated chip is shown in Fig. 6.1 b.

6.3 Layout and Fabrication

AWR MWO's integrated of design, simulation, and layout tools were used to layout and design rule check (DRC) the designs. The final hierarchal design schematic is shown in Fig. 6.1 a and Fig. 6.1 b is a micrograph of the fabricated chip. The integration of simulation and layout in the MWO tool set allows a 1:1 correspondence between simulation cells and layout cells. This design flow integration helps avoid transcription errors between schematic components and layout components. The layout of a unit cell is shown in Fig. 6.2 g. The drain and gate transmission

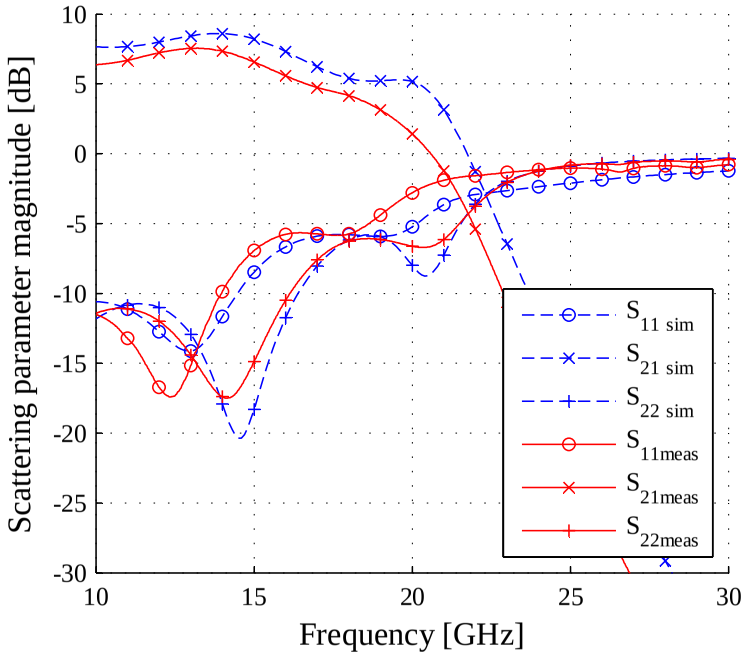
lines, top and bottom respectively, are composed of identical circular planar spiral inductors and the transistor parasitic capacitors augmented with C_{ext}. The 0.5 µm by 15 µm transistor, center, is dwarfed by its two source vias to ground. All of the hierarchal cells are specifically dimensioned to have input and output ports that align with the adjacent cells.

The MMIC shown in Fig. 6.1 b was fabricated using TriQuint's TQPED MMIC 0.5 µm gate pHEMT process [97]. This process uses a 100 µm thick GaAs microstrip substrate with through-hole vias and a backside gold ground plane. Active TQPED devices are enhancement and depletion mode 0.5 µm gate pHEMT transistors with f_t near 30 GHz. Passive devices can be realized with three gold wiring layers, up to 6 µm thick when stacked, 50 Ω/□ thin film NiCr resistors, and 630 pF/mm^2 parallel plate capacitors. As discussed in Section 3.4 this process can be used to make low-loss passive circuits, as well as the active circuits discussed here.

6.4 Probed Measurements

The devices on the chip shown in Fig. 6.1 b were measured using an Agilent E8346B PNA and a custom on-chip TRL calibration from 10-35 GHz. Figure 6.3 shows good agreement between measured and simulated S-parameters for the 3-transistor distributed amplifier output stage. A maximum gain of 7.5 dB was measured, with better than 5 dB gain from 10-17 GHz, and better than -5 dB return loss from 10-19 GHz.

The fabricated amplifier exhibited significantly different performance with respect to bias point than simulations indicated. Optimal gain flatness was achieved in simulation at $V_g = 0.8$ V and $V_d = 3.5$ V, whereas in the real device the optimal bias point was $V_g = 1.0$ V and $V_d = 2.0$ V. These bias points are used in Fig. 6.3 for comparing the measured and simulated results, respectively. It should be noted that while the TriQuint TOM3 model available for the 0.5 µm × 15 µm TQPED E-mode pHEMPT device gave a fair estimation of input and output capacitances (i.e. match, and bandwidth), it significantly overestimated the gain and was not indicative of optimal gain bias.



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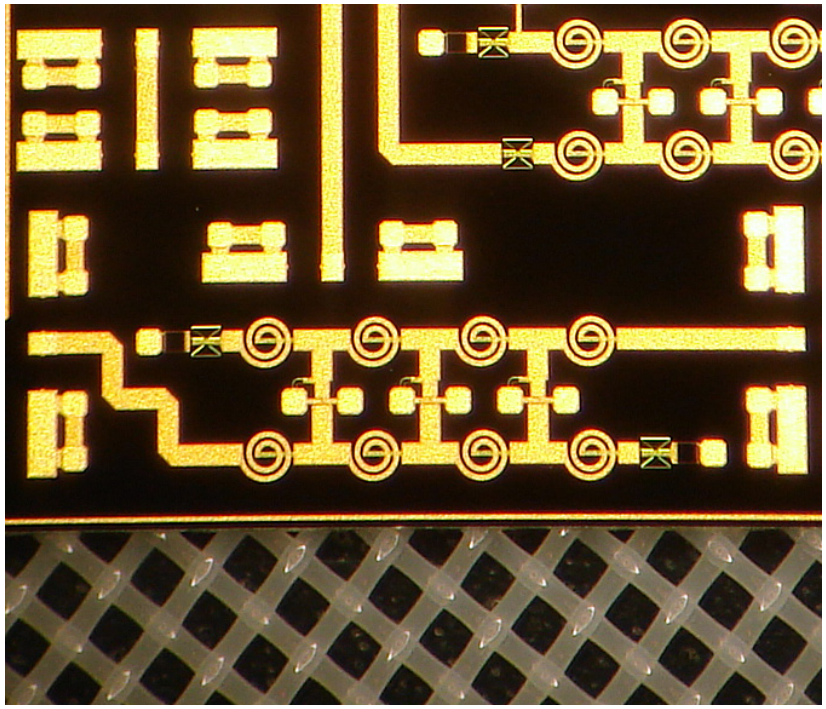
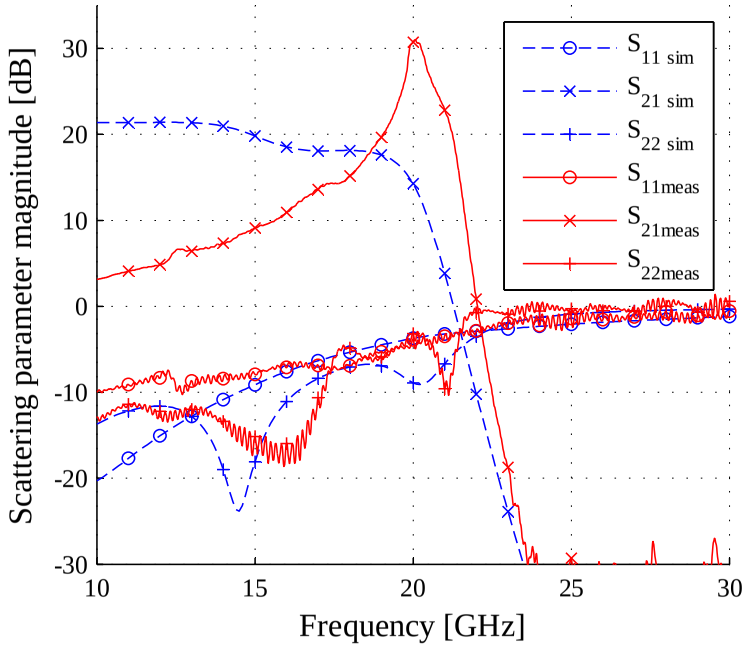


(b)

Figure 6.3: (a) Distributed amplifier 3-transistor output stage measured, red solid lines, versus simulated, blue dashed lines, S-parameters. These measurements utilize a 10-30 GHz on-chip TRL calibration with the amplifier biased using external commercial bias tees at $V_g = 1.0\,\mathrm{V}$ and $V_d = 2.0\,\mathrm{V}$. (b) A micrograph of the measured output stage test circuit.



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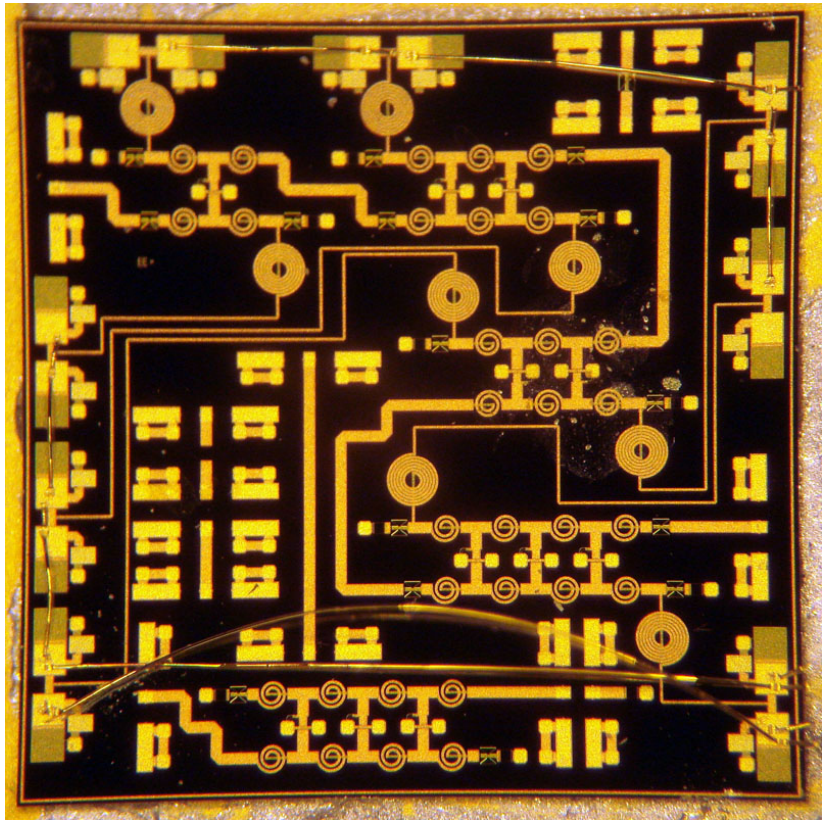


(b)

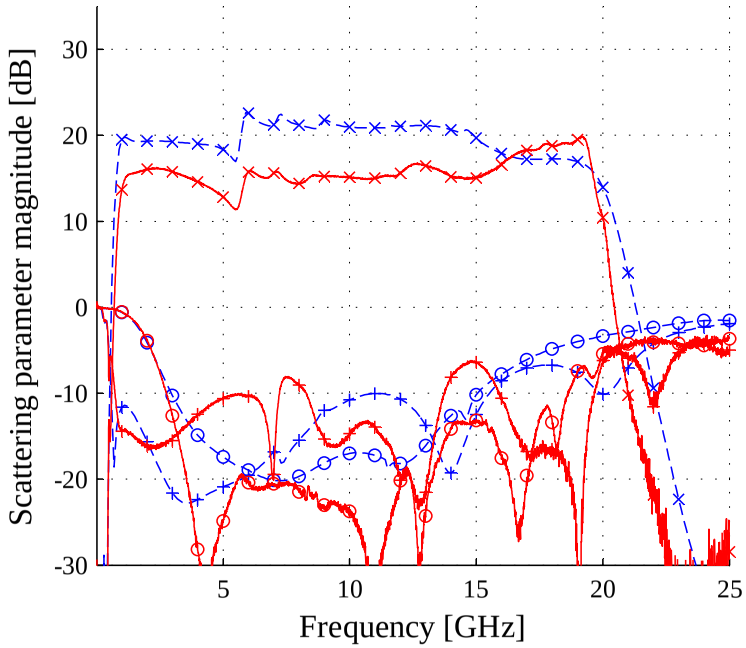
Figure 6.4: (a) Distributed amplifier S-parameters with bond wire biasing measurement in red solid lines, versus simulation in blue dashed lines. These measurements utilize a 10-30 GHz on-chip TRL calibration with the amplifier biased using on-chip bias-tees at $V_g = 1.0\,\mathrm{V}$ and $V_d = 2.0\,\mathrm{V}$. Note the 20 GHz resonance due to 5 mm pre-characterization wire bond. (b) A micrograph of the pre-characterization circuit with long wire bonds to allow for initial measurements using only two DC probes.

6.5 Packaging

In order appropriately characterize the fabricated 4-stage MMIC amplifier a permanent packaging solution was required. To allow for better bias isolation with discrete components, each gate and drain bias inductor was pinned out individually to 8 DC pads, too many for probed measurement. A pre-characterization was attempted utilizing very long wire-bonds to interconnect the DC bias pads, shown in Fig. 6.4 b. Figure 6.4 a displays the measured results from this first pass test. The result is sufficient to verify that the biasing network is intact, but the 5 mm gate pad wire bond has a large 20 GHz resonance that precludes serious characterization of the amplifier.

The packaged solution requires bandwidth to 20 GHz, minimal loss, connectorized operation, mechanical stability, and thermal capability to radiate the $\sim$1/2 W dissipated by the amplifier. For low cost and ease of manufacturing a 25 mm $\times$ 25 mm area of 500 µm Rogers 4350 substrate was chosen. DC and microwave connections to the chip were made using minimal length wire bonds, about 200 µm long. Through plated via holes allow the MMIC ground plane to be soldered to the top trace of the package with a thermal connection to the backside ground-plane/heat-sink. Precision 26 GHz SMA connectors were used at the package edge of the grounded co-planar waveguide input and output transmission lines.

Using a microwave substrate for the package afforded sufficient area to improve several parameters of the amplifier design that were not fully realized for lack of area on the MMIC. First, the MMIC bias-tees, constrained by chip area, were augmented off-chip with surface mount LC components to improve bias isolation and suppress the resonance seen in the on-chip measurements. The available range of surface mount component values also allowed for a high pass filter to be added at the low end of the band to flatten the gain curve from 1-3 GHz, at the cost of reduced input match in this band. Figure 6.5 b shows a photograph of the packaged, connectorized amplifier with bias leads.



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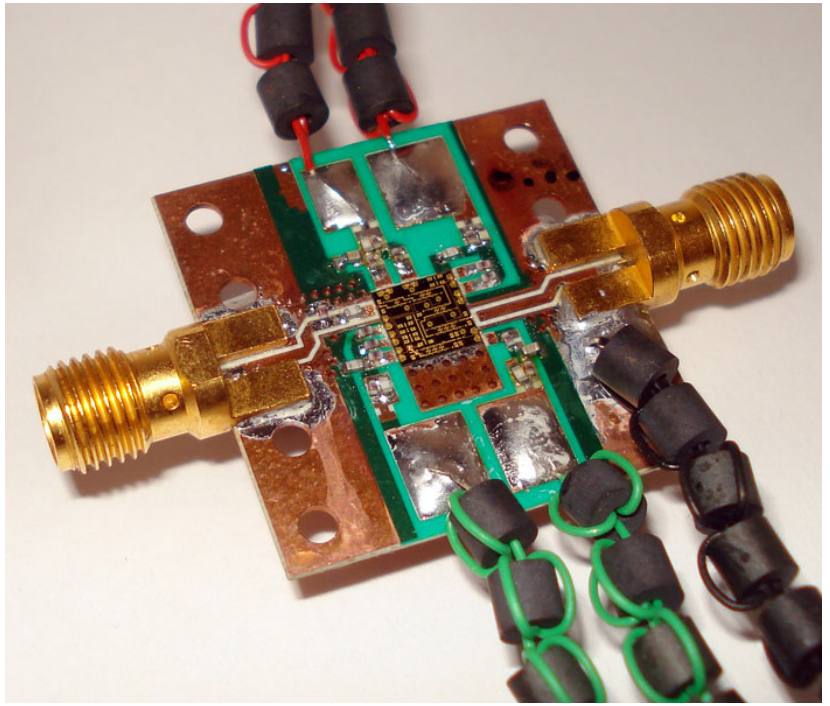
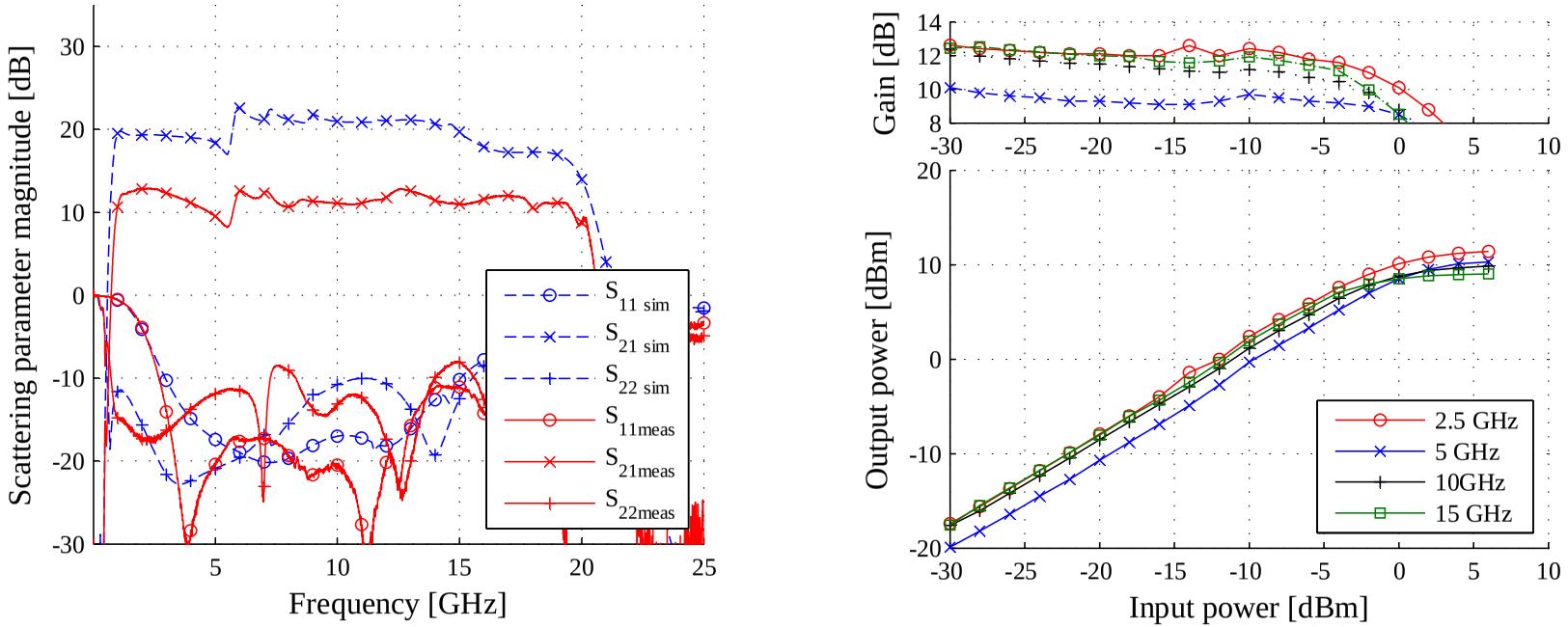


(b)

Figure 6.5: (a) Measured (red solid lines) versus simulated (blue dashed lines) S-parameters for the packaged 4 stage distributed amplifier at the maximum gain bias point of V_g=1.0 V and V_d=1.0 V. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$. (b) A photo of the packaged and connectorized distributed amplifier circuit.



(a) (b)

Figure 6.6: (a) Measured (red solid lines) versus simulated (blue dashed lines) S-parameters for the packaged 4-stage distributed amplifier at the optimal flatness bias point of V_g=1.0 V and V_d=2.0 V. S_{11} is marked with ∘, S_{21} is marked with ×, and S_{22} is marked with +. (b) Measured amplifier gain saturation at V_g=1.0 V and V_d=2.0 V.

6.6 Packaged Measurements

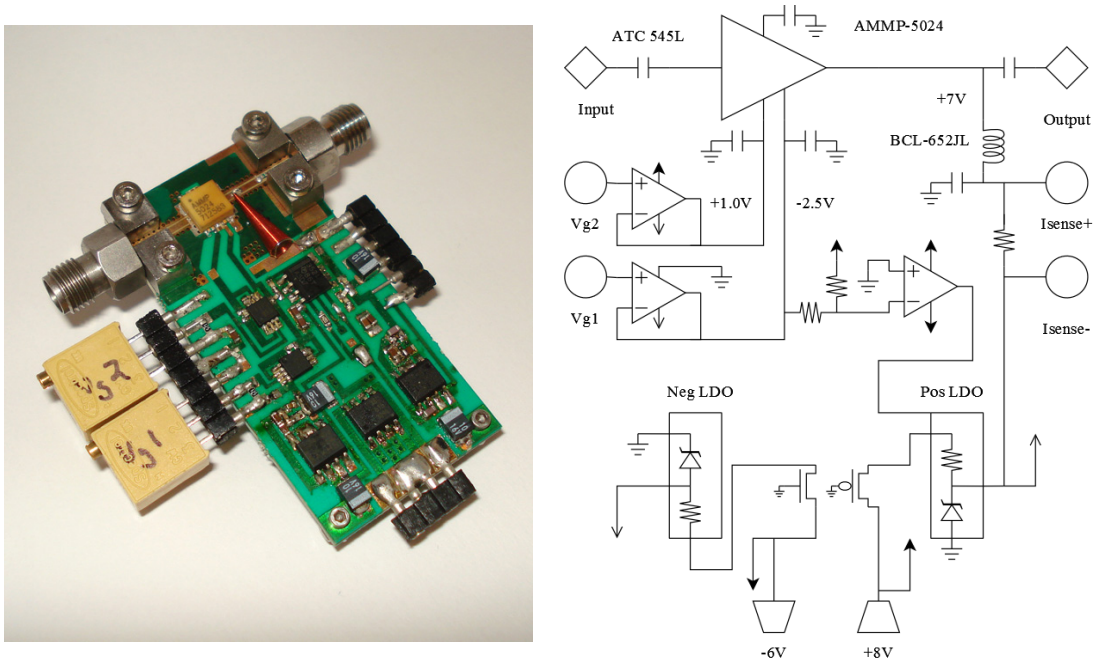
The packaged device, Fig. 6.5 b, was measured using an Agilent E8346B PNA and a 3.5 mm e-cal calibration over a 10 MHz–25 GHz band. The maximum gain bias point, $V_g = 1.0\,\mathrm{V}$ and $V_d = 1.0\,\mathrm{V}$ in Fig. 6.5 a, and the optimal gain flatness bias point $V_g = 1.0\,\mathrm{V}$ and $V_d = 2.0\,\mathrm{V}$, in Fig 6.6 a both show good frequency response agreement between measured (at the package connector) and simulated S-parameters for the 4-stage distributed amplifier. Unfortunately as previously mentioned, the gain is significantly overestimated by the TOM3 model. The optimal gain flatness bias point for the packaged amplifier was again $V_g = 1.0\,\mathrm{V}$ and $V_d = 2.0\,\mathrm{V}$, a far cry from the optimal simulated bias point $V_g = 0.8\,\mathrm{V}$ and $V_d = 3.5\,\mathrm{V}$. A gain of $\sim$12 dB was measured across a 1–20 GHz band. The amplifier exhibits better than $\pm$1 dB gain flatness in this band, with the exception of an undamped resonance at 5 GHz attributed to the bias line wire bonds. The packaged amplifier exhibits better than -8 dB return loss from 3-18 GHz.

Figure 6.5 d shows measured input power versus output power, at the package edge, for the amplifier. At the $V_g = 1.0\,\mathrm{V}$ and $V_d = 2.0\,\mathrm{V}$ bias point the amplifier has $\sim$10 dBm of saturated output power. Increasing the drain bias to its maximum $V_d = 4.0\,\mathrm{V}$, at the cost of gain and flatness, would likely increase the saturated output power by 3-5 dB.

6.7 Commercial Solution

In acJVS testing, discussed in Chapter 7, it was found that optimal acJVS operating margins occur with a low frequency -3 dB corner in the 10 MHz range, much lower than the custom MMIC distributed amplifier operates stably. To address this issue a commercially available surface mount distributed amplifier, the Avago AMMP-5024, was chosen for evaluation [98]. It is specified to have 16 dB of gain from 100 kHz to 40 GHz and 22.5 dBm output power, with the low frequency corner depending on the off-chip bias-tee implementation.

It was desired to create an evaluation module for this amplifier that could also serve as a low-cost, easy-to-use, broadband, general-purpose laboratory amplifier. As such, the final



(a) (b)

Figure 6.7: (a) A photo of the final prototype Avago AMMP-5024 amplifier and bias circuitry. (b) A simplified schematic of the analog protection circuitry.

implementation needs to be connectorized to 40 GHz (2.92 mm or 2.4 mm connectors), support turnkey operation (internal power supply regulation and phasing), and have sufficient microwave and thermal performance to support long term operation with 20 Gbps acJVS $\Delta\Sigma$-waveforms.

A 0.5 mm Rogers 4350 substrate was chosen for the design as a good trade off between low-cost commercial manufacturability and low-loss microwave performance. Commercial board manufacturers will produce a full sheet of two side patterned and solder masked RO4350 for about $1000. Figure 6.7 a is the final prototype amplifier board showing the microwave design and bias electronics. The 0.5 mm board gives very good mechanical rigidity, at the cost of a slight dimensional mismatch at the AMMP-5024 microwave ports with negligible effect on performance.

The gate and drain microwave bias circuits were designed for the lowest cutoff frequency with commercially available components. ATC 545L DC-blocking capacitors, and a Coilcraft 652L inductor are chosen to yield a low frequency 3 dB corner on the order of 1 MHz. To function as a user friendly laboratory amplifier, analog drive electronics were implemented to protect from

reverse voltage polarity and ensure appropriate depletion mode gate biasing before the drain voltage is applied. A schematic representation of the lab amplifier circuit is shown in Fig. 6.7 b.

The completed device, shown in Fig. 6.7, was measured over a 10 kHz–50 GHz band. The measured performance of this device is very close to the Avago specification with 14 dB of gain from 250 kHz–40 GHz. The analog control circuit allows for either mechanical or electrical control of the gain over a 30 dB range via the cascade V_{g2} input to the amplifier. Figure 6.8 a shows a log frequency measurement of the small signal scattering parameters of the amplifier at maximum gain. The S-parameter plot in Fig. 6.8 b shows the power gain, $|S_{21}|$ of the amplifier over various V_{g2} control voltages; 20 dB of output dynamic range is easily attainable with relatively flat gain to 30 GHz and a smooth roll-off to 40 GHz.

6.8 Summary

In this chapter distributed amplifier design, layout, and testing has been completed using AWR MWO targeted as a pathfinder on the TriQuint TQPED process. There are many design trade offs and a wide range of possible solutions to problems relating to matching, gain, layout tradeoffs, biasing, etc. For a given application there are several possible topologies all with different strengths and weaknesses to weigh before deciding on a final design. This design was optimized for simplicity in both design, and layout, at the likely cost of a margin of performance. While not the highest performance amplifier, first pass success in a previously untried MMIC process is a significant accomplishment. For the final JVS system, the commercially available solution proved better value for performance than the custom MMIC.

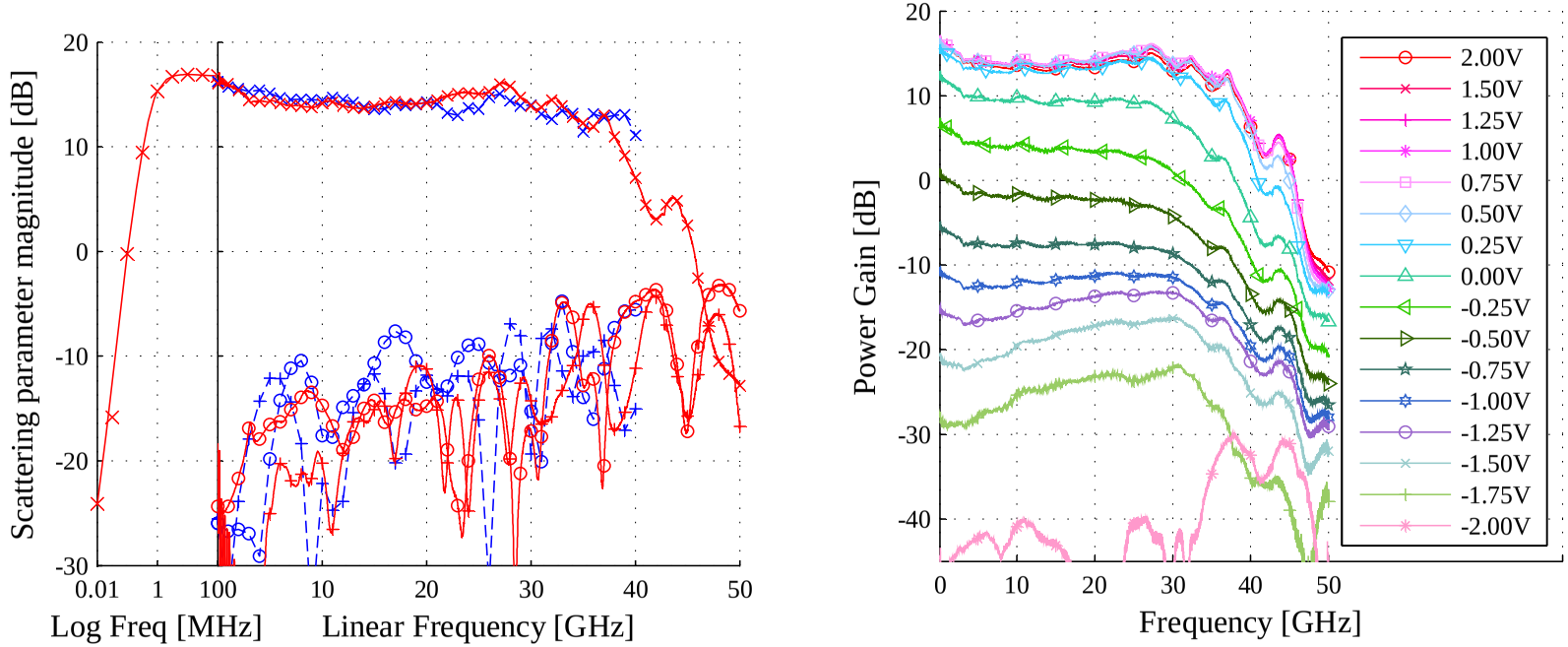


Figure 6.8: (a) Measured (red solid lines) versus published (blue dashed lines) for the packaged 4-stage distributed amplifier on a log frequency scale. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, and S_{22} is marked with $+$. (b) Measured power gain, S_{21}, at various V_{g2} bias levels.

Chapter 7

Challenges and Future Directions in JVS Systems

Contents

This chapter summarizes the design challenges of next-generation JVS systems. The first challenge explored is microwave efficiency in PJVS systems. Even with recent advances in cryocooler technology, 4 K thermal loads are limited to a few hundred milliwatts. To use the microwave excitation power more efficiently, resonant arrays for PJVS systems are interesting. Several circuits were designed and fabricated to test these resonant PJVS arrays. The measured results from these test structures are discussed to direct future work in this area.

Increasing the output voltage of acJVS systems is another major challenge. The state-of-the-art NIST acJVS system is capable of producing 300 $\mathrm{mV_{rms}}$ up to a few kilohertz with part-per-million precision. A 1 $\mathrm{V_{rms}}$ acJVS output would significantly increase the utility of this system. Experimental devices for on-chip power division of the $\Delta\Sigma$ excitation waveform using the Wilkinson powder dividers from Chapter 3 were designed and fabricated. Measurement results from these devices were promising, but highlight another challenge to develop JVS system simulation technology.

The final challenge this chapter presents is a Microwave Josephson Voltage Synthesizer (MJVS) system. This system, an extension to the acJVS concept, would be excited by a band-pass $\Delta\Sigma$ code designed to synthesize multi-tone microwave waveforms with very good spectral purity. Such an arbitrary microwave waveform synthesis capability would be very useful for testing high-linearity devices. The challenges and preliminary investigation results presented in this chapter highlight areas for future research in specialized microwave circuits for JVS systems.

7.1 Efficient Microwave Arrays for JVS systems

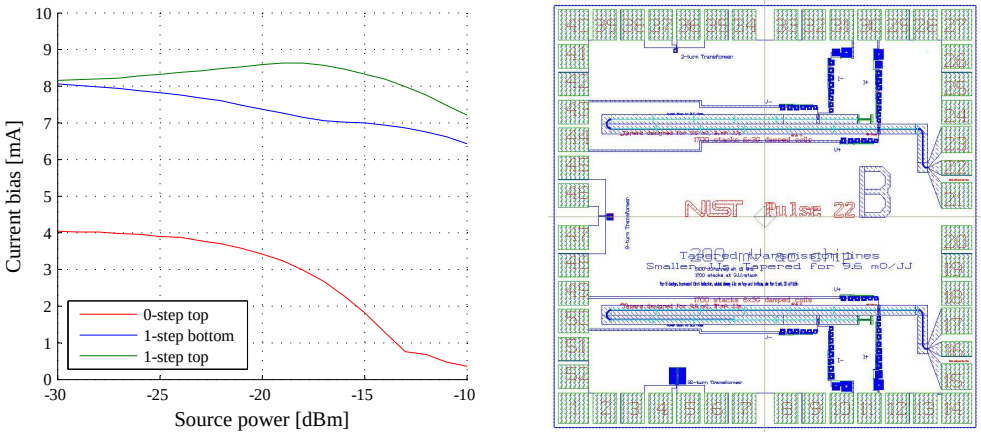
This section explores improvements to JVS microwave efficiency. The 1 V PJVS system, discussed in Section 1.5.2, utilized relatively short 4 000 JJ arrays with a resistive termination that dissipates a significant portion of the microwave excitation power. The 10 V PJVS prototype system, discussed thoroughly in Section 8.1, uses transmission lines with an 85 Ω to 22 Ω impedance taper to reduce the resistive dissipation [59]. In order to eliminate on-chip resistive dissipation entirely, a resonant array topology is a possible component of future JVS systems.

A hybrid lumped/distributed JJ loaded resonator is designed, fabricated, and tested as a proof-of-concept. A short-circuited resonator topology an odd number of quarter wavelengths long utilizing lumped $\lambda/4$ LC Π sections in the nulls of the microwave current standing wave is proposed. This resonant circuit allows for a significant reduction in microwave bias power while still enabling the microwave excitation of many JJs in a minimum area.

7.1.1 Resonator Requirements

A JJ loaded resonator needs to be optimized to contain the maximum number of JJs at the highest reasonable frequency. A target operating frequency of 20 GHz is chosen as an optimal trade off between higher Josephson voltage per junction, and the convenience of being able to use low-cost coaxial and precision SMA components in the microwave feed. To avoid standing waves in the microwave current through the JJs in a lumped resonator, the maximum physical size of the resonator is constrained to approximately $\lambda/8$, or $\sim$800 µm at 20 GHz in coplanar waveguide (CPW) on silicon. With the three JJ stack height of the present NIST QV IC process, this limits the total number of junctions to approximately 300, providing a JVS output voltage of only 1 mV [63, 99].

To integrate more junctions a physically larger resonant circuit is required, necessitating a distributed transmission line resonator which supports standing waves. Unfortunately, the JJs at standing wave nulls experience a reduced microwave current excitation, reducing the size of the desired quantized voltage steps. Figure 7.1 a plots the JJ bias current values for the quantized voltage step corners, shown in Fig. 1.1, as microwave excitation power is varied. Fig. 1.1 a corresponds to the −30 dBm point and Fig. 1.1 b corresponds to the −17 dBm point in Fig 7.1 a. In [12] the current-null limitation is circumvented by only placing JJs in small sections of the resonant circuit near the current standing-wave maximums. This topology requires large amounts of chip area for relatively few JJs. In the experimental JJ arrays presented here, lumped-element LC Π transmission line sections are inserted at the standing-wave current nulls. Such a hybrid lumped/distributed resonator can be designed with a significantly reduced size.



(a) (b)

Figure 7.1: (a) JJ quantized Shapiro step height in applied bias current as a function of uniform microwave excitation power in a resistively terminated array; for reference, Fig. 1.1 a corresponds to the −30 dBm point and Fig. 1.1 b corresponds to the −17 dBm point. (b) A layout screen capture of the JJ array measured in a), a typical 6400 JJ resistively-terminated-array 10 mm × 10 mm chip for acJVS applications.

7.1.2 Design

As shown in Figure 7.1 a, the one-step voltage of a non-resonant JJ array, Fig. 7.1 b, exhibits 1 mA or better of bias current margin over a ∼6 dB range of microwave power. The current over a $\lambda/4$ cut centered at the maximum of a standing wave varies from 70–100 % of maximum, corresponding to 3 dB range of microwave power in a non-resonant case. Conversely, the current over the $\lambda/4$ cut centered at the minimum has a 0–70 % variation. If the JJs measured in Fig. 7.1 a were excited at -15 dBm and integrated into a resonant array, the Shapiro voltage step in the maximum $\lambda/4$ sections would be the summation of the Shapiro steps between -18 dBm and -15 dBm, and the the Shapiro voltage step in the minimum $\lambda/4$ sections would be the summation of the Shapiro steps between -30 dBm and -18 dBm. If only the maximum $\lambda/4$ sections of a resonant array are loaded with JJs, quantized voltage steps with the required 1 mA of bias current margin can be achieved.

As discussed in Chapter 3, a transmission line of a given electrical length, frequency, and characteristic impedance can be decomposed into an LC equivalent Π or T network [77]. The values for a low pass network with series L_s and shunt C_p of electrical length l in radians,

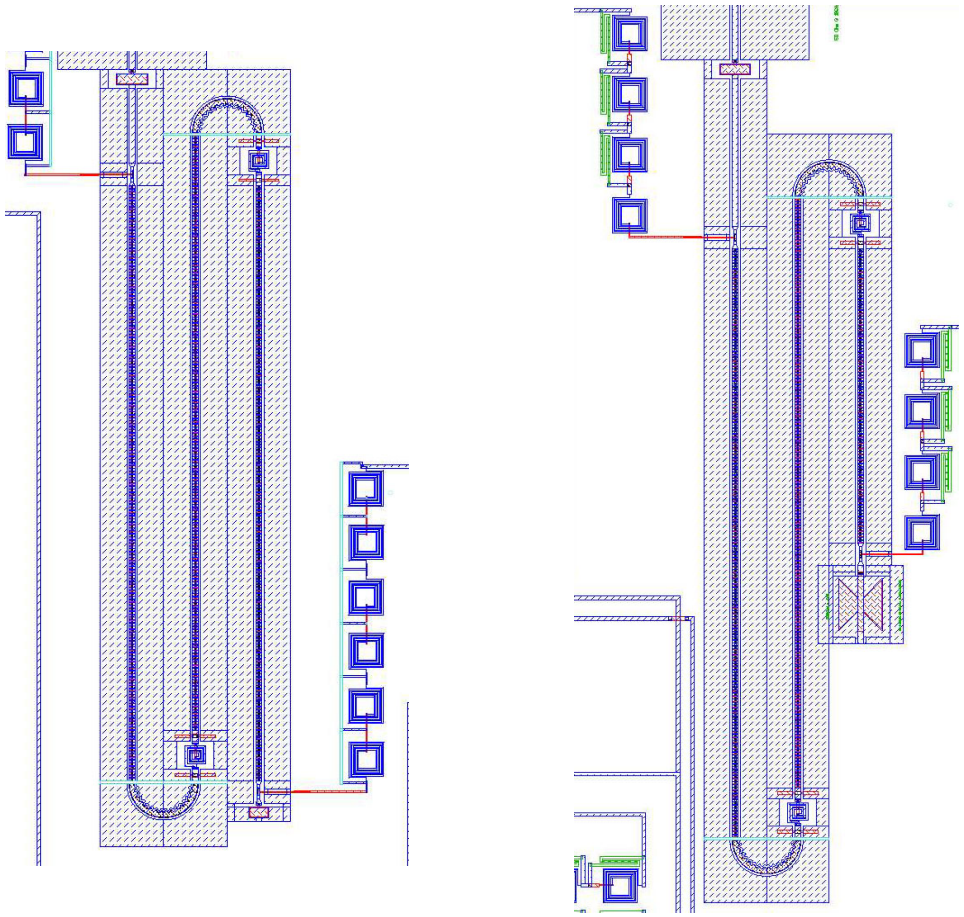
frequency f_0 in hertz, and characteristic impedance Z_0 in ohms are given by Equation 3.1. These JJ loaded resonators at 20 GHz utilize 50 Ω $\lambda/4$ Π sections at the current minimums with L_s of 400 pH and C_p of 160 fF. Integrated into a CPW transmission line, this 135 μm long LC $\lambda/4$ section is equivalent to a 1600 μm distributed transmission-line section.

A short-circuit terminated transmission line resonator topology is chosen to maintain a current maximum near the end of the line. Because the JJs require a DC bias current the array termination must be capacitively coupled to ground, possibly shifting the current maximum away from the termination by some capacitive phase shift. Two design topologies were implemented, one in which this capacitive phase shift was used to introduce a $\lambda/8$ negative phase shift at the termination allowing all the JJ arrays to be $\lambda/4$ long, and one in which the final array was shortened to $\lambda/8$ and a large DC-blocking capacitor was used, introducing negligible phase shift at the termination.

Each $\lambda/4$ JJ loaded section of the resonator contained 200 stacks of 3 JJs with I_C=3.5 mA and R_n=5 mΩ. This configuration exhibits 1.5 Ω series resistance for each quarter wave JJ loaded segment, setting the unloaded quality factor of the resonator at about 10, and the loaded Q to 5 with three JJ loaded segments in a $5\lambda/4$ electrical-length resonator. This low Q resonance allows for a few percent adjustment of the desired JVS output voltage by fine tuning the microwave frequency.

7.1.3 Fabrication

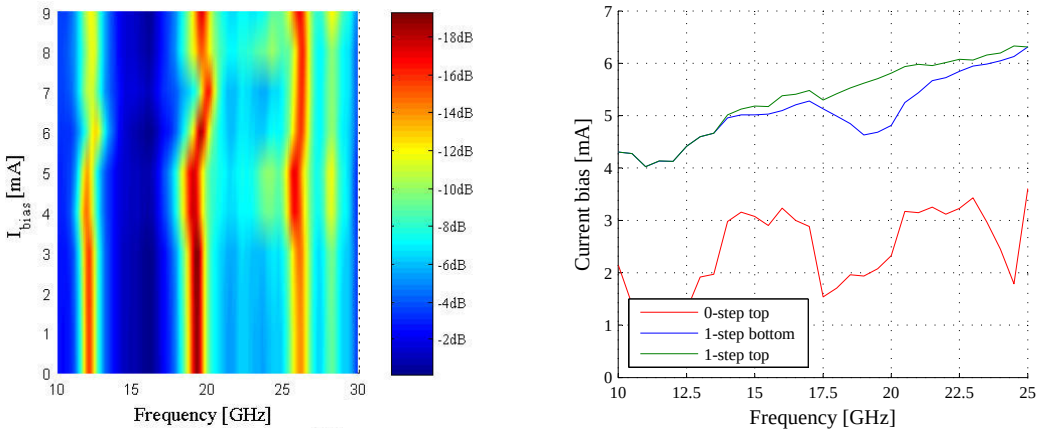
The NIST QV IC technology, described in Section 1.4.1, is used to fabricate these resonant JVS arrays. In the first test circuit, a negative phase shift capacitive termination was attempted, with multiple bias-tees to allow the ratios of microwave current in three subsegments of each $\lambda/4$ line to be measured. While the microwave power leakage out of these electrically closely spaced bias lines was significant, this increased experimental resolution allowed the negative phase shift capacitor to be adjusted to optimize the second pass fabrication, shown in Fig. 7.2 a. In the other test circuit, Fig. 7.2 b, an arbitrarily large DC-blocking capacitor was used as a



(a) (b)

Figure 7.2: (a) A layout of the capacitive phase-shift terminated resonant JVS array circuit. (b) A layout of the short-circuit terminated resonant JVS array circuit. Each meandered JJ loaded CPW array section is 1600 µm long, $\lambda/4$ at the 20 GHz design frequency. The output voltage is measured and the current bias is applied to these resonant arrays using the bias-tee structures, from Section 5.1, at either end.

short-circuit termination, avoiding the problem of precise modeling and/or design iteration to tune the microwave current standing wave peaks to lie in the JJ loaded sections. This circuit, while sacrificing 300 total junctions, is more desirable from a design perspective as it is less susceptible to process and modeling variations than the $-\lambda/8$ capacitive phase shift topology. These test chips were fabricated in the NIST Boulder quantum device fabrication facility by Paul Dresselhaus and Norm Bergren.



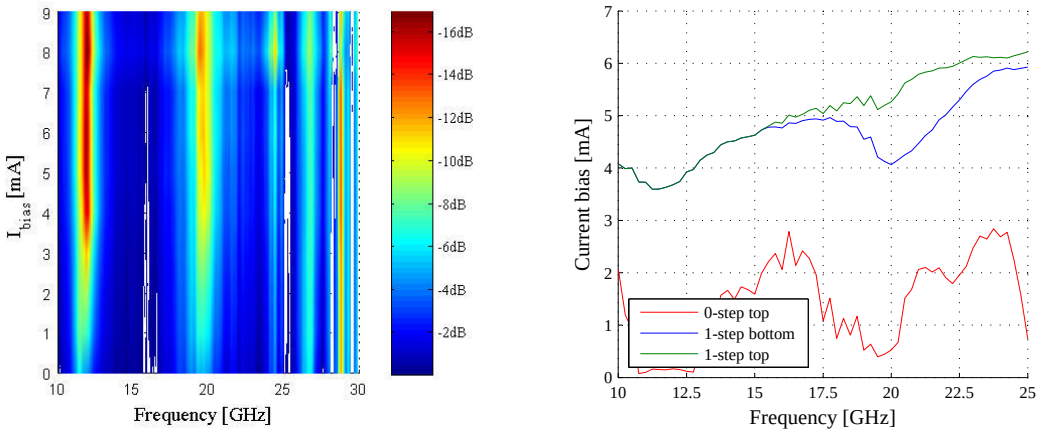
(a) (b)

Figure 7.3: (a) A three-dimensional plot of measured capacitively-terminated JJ resonator, Fig. 7.2 a, characteristics. Color indicates input reflection coefficient, plotted over a range of frequency and bias current. (b) The measured Shapiro step heights of the capacitively-terminated resonator sweeping the microwave excitation through the resonance.

7.1.4 Testing

Measurements, shown in Fig. 7.3 a and Fig. 7.4 a, were performed with an Agilent 8722ES VNA using the same methods described in Section 3.2.3 The reflection coefficient of the -$\lambda/8$ phase shift capacitive termination resonator is shown in Fig. 7.3 a with color indicating match. The change in the match and resonant frequency with DC bias is due to the nonlinear inductance of the JJ. The matched area at 19 GHz and near $I_C = 5$ mA is the desired operating point. Figure 7.3 b, shows the DC bias current margins on the voltage-step versus microwave frequency for the phase-shift terminated resonator circuits. Note the maximized one-step near the 20 GHz design frequency.

The reflection coefficient of the short-circuit resonator with a large DC-blocking capacitor is shown in Fig. 7.4 a. Fig. 7.4 b shows DC bias current margins on the voltage steps versus microwave frequency. With the short-circuit termination a larger margin of bias current on the quantized voltage step was demonstrated with a more robust and manufacturable design. This circuit exhibits better than -10 dB match with 10% bandwidth around its 20GHz design point and exceeds the 1 mA bias margin on the one-step design goal of these arrays.



(a) (b)

Figure 7.4: (a) A three-dimensional plot of measured short-circuit JJ resonator, Fig. 7.2 b, characteristics. Color indicates input reflection coefficient, plotted over a range of frequency and bias current. (b) The measured Shapiro step heights of the short-circuit resonator sweeping the microwave excitation through the resonance.

7.2 Increasing acJVS Output Voltage

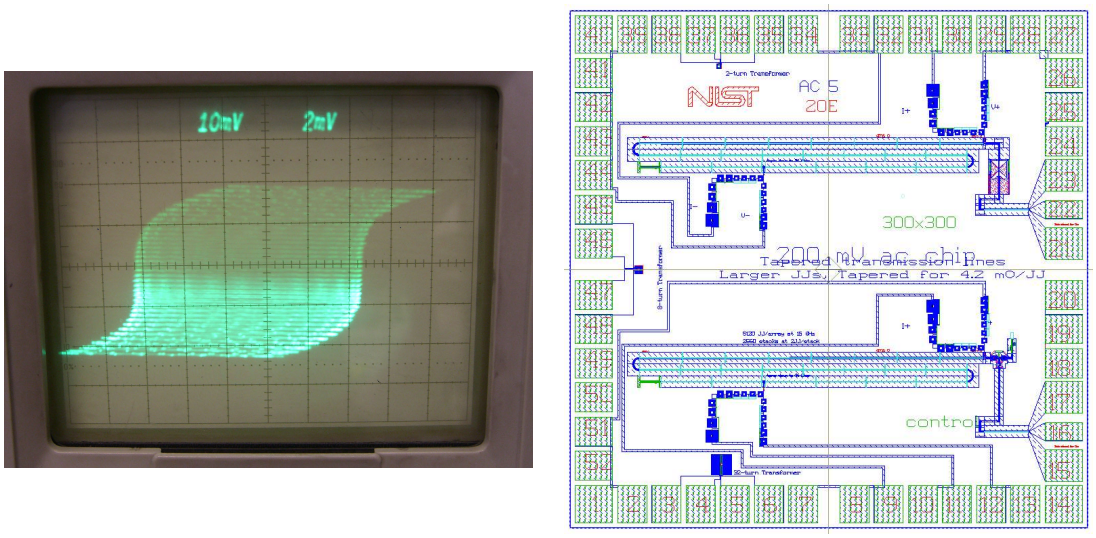
This section covers experiments on improving NIST acJVS systems. The two basic long term challenges in acJVS systems are increasing the output voltage and increasing the synthesis frequency. This section will first start with feasibility experiments in applying the on-chip power division technology discussed in Chapter 3 to the broadband low-pass-$\Delta\Sigma$-modulated excitations of acJVS systems. Next, several on-chip DC-blocking capacitor designs with low cut-off frequencies are presented. This collection of experiments highlights the need for a simulation technology to order to provide a vehicle for studying and specifying $\Delta\Sigma$ excitation chain microwave component requirements for future acJVS-based systems.

From Section 1.5.3, the acJVS system is excited by a train of high speed current pulses such that each non-zero bit of the excitation code produces one flux quantum per junction. This pulse quantization allows acJVS systems to achieve quantum-accurate-voltage arbitrary-waveform synthesis. In practice the acJVS system operates as a massively oversampled $\Delta\Sigma$ pulse density modulator with a 10 Gbps bit-stream being used to generate signals in the audio frequency range. The acJVS system is shown schematically in Fig. 1.10.

7.2.1 acJVS Arrays with On-chip Power Division

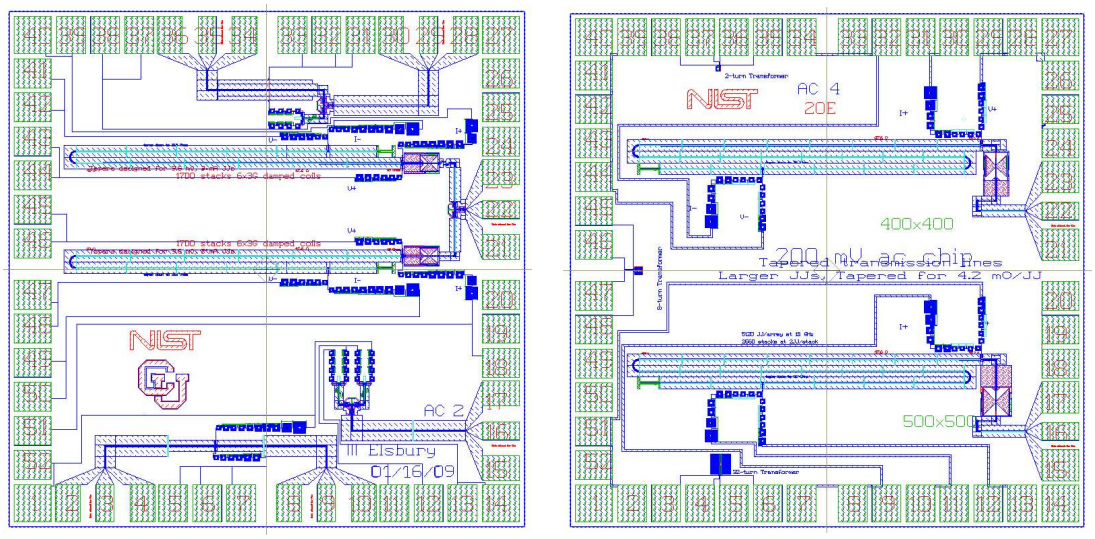
A test circuit was designed with the broadband Wilkinson power divider from Chapter 3 feeding a standard acJVS 5120 JJ array (2560 stacks 2 JJs high). The other output port of the Wilkinson was terminated in a resistive termination from Chapter 5 to reduce the IC mask complexity of the circuit and save pattern generation time. This chip, shown in Fig. 7.5 b was evaluated in the acJVS system with a $\Delta\Sigma$ code that generates a small $4\,\mathrm{mV_{rms}}$ (5% of full scale) amplitude tone at 2.5 kHz. Small output-amplitude $\Delta\Sigma$ codes reduce the dependence on the low frequency current compensation and make initial testing easier. The bias current margins of an acJVS array can be measured using an analog oscilloscope in XY mode using a custom built NIST JVS sweeper box to sweep the array bias current. Flat voltage steps bounding the oscillating acJVS voltage waveform are an indication the array is exhibiting proper pulse-quantization operation, Section 1.5.3. Figure 7.5 a is a ± 2 mA sweep of bias current (vertical axis) showing a $\sim$1.0 mA of bias current range where the voltage step bounding the oscillating output that appears flat. This measurement applies a small, phase-matched 2.5 kHz bias current compensation to achieve a quantized output voltage. This viable current margin with a Wilkinson divided $\Delta\Sigma$ excitation is a successful proof-of-concept result.

In order to fully implement $\Delta\Sigma$ excitation division on-chip in acJVS systems, the $\Delta\Sigma$ code for one array needs to be inverted such that the array voltages can be added in series. The 180° CPW phase inverter from Chapter 4 should be sufficiently broadband to perform this data inversion. In addition, the signal and ground of the arrays need to be DC blocked to avoid a ground loop shorting out the summation. The broadband bow-tie capacitors from Section 5.1.1 were enlarged to have cutoff frequencies of a few hundred megahertz and used to DC block the $\Delta\Sigma$ excitation. Unfortunately, array mask defects in the fabrication process prevented testing this full prototype, shown in the top right of Fig. 7.6 a. Rather than repeating this complex test device, it was decided to begin by verifying each of the components in the $\Delta\Sigma$ excitation chain individually to better determine system requirements.



(a) (b)

Figure 7.5: (a) A photograph of the XY analog oscilloscope trace showing a ±2 mA of bias current sweep at 0.1 mA/mV (vertical axis) for a 5120 JJ array with on-chip power division of a ΔΣ excitation producing a 4 mV 2.5 kHz output waveform. The ∼1.0 mA bias current range for which the output voltage (horizontal axis) has a quantized boundary is an indication of quantized operation. (b) The layout of a 10 mm × 10 mm acJVS proof-of-concept test chip. The top 5120 JJ array is excited through a 300 µm extent DC-blocking capacitor, Section 5.1.1, while the the lower array is excited through the Wilkinson divider designed in Chapter 3.



(a) (b)

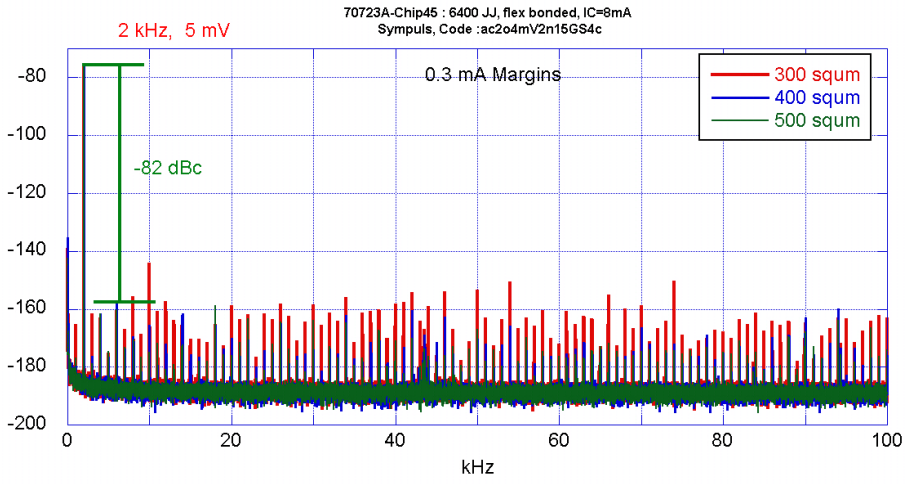
Figure 7.6: (a) The layout of the acJVS 10 mm × 10 mm ΔΣ division test chip. Two DC-blocked acJVS 5120 JJ arrays, one with a phase inverter, are excited from pads 21–23 through the Wilkinson divider from Chapter 3. Various other test structures are also on this chip including the acJVS bias-tee (bottom) from Section 5.1, and a port-1 to port-2 Wilkinson divider test circuit (top). (b) The layout of the 10 mm × 10 mm acJVS DC-blocking capacitor test chip with two acJVS 5120 JJ arrays excited through DC-blocking capacitors with cut-off frequencies of 300 MHz (top) and 500 MHz (bottom).

7.2.2 acJVS Arrays with On-chip DC-blocking Capacitors

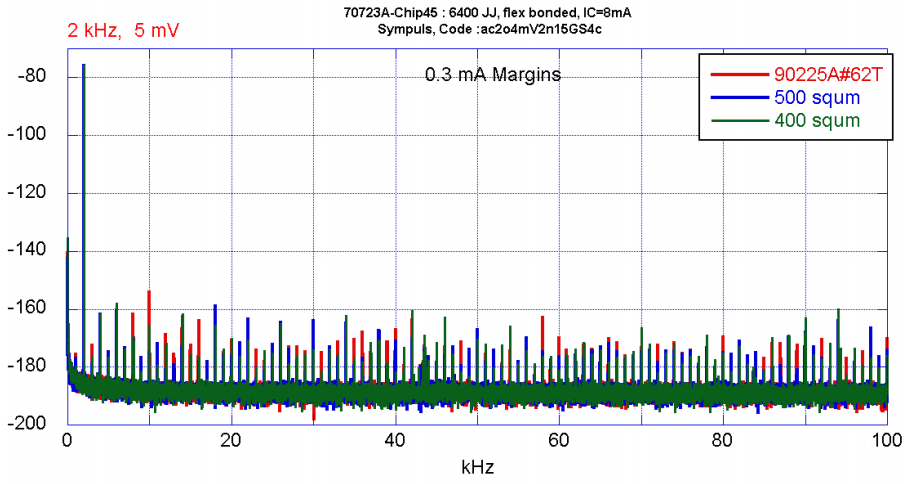
In the acJVS system, shown in Fig. 1.10 the DC-blocking capacitor in the $\Delta\Sigma$ excitation block serves as a low pass filter to remove the in-band portions of the $\Delta\Sigma$ code. This filter needs to attenuate the noise floor of the bit stream generator and the synthesized signal by more than 60 dB. The JJ array then quantizes the remaining $\Delta\Sigma$ out-of-band quantization noise spectrum such that every bit once again results in a quantized volt-second pulse area. This pulse quantization recovers the original $\Delta\Sigma$ modulation desired signal with part-per-million voltage precision and better than -100 dB spectral purity, provided the low pass filter both attenuates the in-band noise/signal sufficiently and passes the out-of-band $\Delta\Sigma$ quantization noise. In order to characterize this filtering requirement a selection of large on-chip DC-blocking capacitors were fabricated with maximum extents of 500 µm, 400 µm, and 300 µm, yielding 3 dB cutoff frequencies of 180 MHz, 300 MHz and 400 MHz respectively. The measurement results of the largest device are shown in Fig. 5.3 a with a screen capture of the layout in Fig. 5.3 b.

Initial measurements were performed using discrete capacitor chips combined into a multi-chip-module with a permanently mounted 6400 JJ acJVS array chip. In this test setup two JVS packages from Chapter 2, one for each chip, were inserted into a single cryoprobe and interconnected with a short coaxial cable at 4 K. This allowed a quick proof-of-concept measurement of on-chip acJVS low-pass filtering, but with the additional parasitic effects of two packages. Figure 7.7 a shows the output spectral measurements overlaid using each of the three capacitors with an identical 2 kHz, 5 mV tone. Figure 7.7 b is the same data but for only the two larger capacitors and a through-line reference chip. These multi-chip-module test cases had only 0.3 mA of bias current margin, as compared to 2 mA of margin with only the acJVS chip in the probe. While multi-chip-module approach significantly degrades the spectral purity of the output signal, as compared to the 113 dBc of Fig. 1.9, it is clear that the 300 µm capacitor degradation is more pronounced when compared to the larger capacitors and the through line reference.

To further test this concept, a set of test chips was fabricated with 5120 JJ acJVS arrays, and large DC-blocking capacitors on the same chip, shown in Figs. 7.5 b and 7.6 b. These arrays



(a)



(b)

Figure 7.7: (a) Measured 2 kHz, 5 mV acJVS output spectra of the 300 µm, 400 µm, and 500 µm capacitor multi-chip-modules. (b) Measured 2 kHz, 5 mV acJVS output spectra of the 400 µm, and 500 µm capacitor and through-line multi-chip-modules. Note the marked increase in distortion with the 300 µm capacitor multi-chip-module. For comparison, acJVS measurement results with commercial DC blocks and better than 110 dBc spectral purity are shown in Fig. 1.9.

were evaluated with the same 2.5 kHz 4 mV output $\Delta\Sigma$ excitation code as the Wilkinson divider. The same code as the multi-chip-module testing could not be used since these devices utilize a different test array due to yield issues on the 6400 JJ arrays. Unfortunately, the on-chip capacitively coupled arrays did not exhibit sufficient bias current margins to be considered useful. Figure 7.8 a shows the DC IV sweep with $\Delta\Sigma$ excitation of the 500 µm capacitor feeding the acJVS array with performance nearly but not quite exhibiting a quantized voltage step. This test circuit is the bottom array in Fig. 7.6 b. This discouraging result could be a sign of any

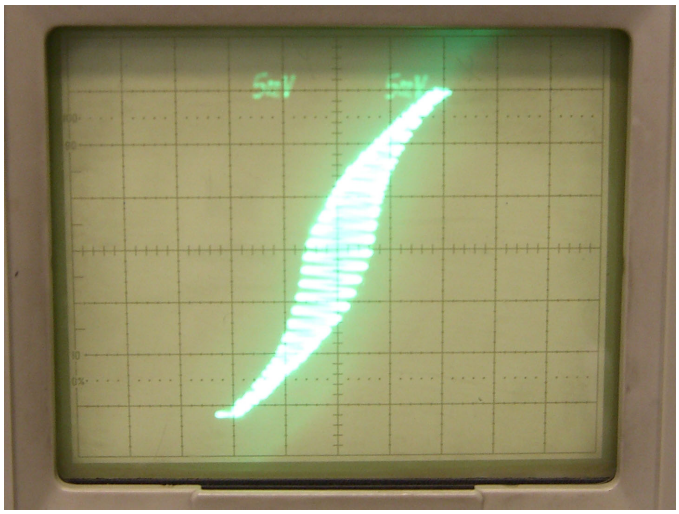


Figure 7.8: A photograph of the analog oscilloscope trace showing the edges of a flat step in bias current at 0.1 mA/mV (vertical axis) for which the output voltage (horizontal axis) does not quite have a quantized boundary from a 5120 JJ array with a 500 µm extent on-chip DC-blocking capacitor.

number of issues in the arrays, the capacitors, the $\Delta\Sigma$ excitation, or the bias electronic set points. In order to better understand and isolate the effects of microwave filtering on the $\Delta\Sigma$ code, a simulation technology is needed.

7.3 Simulation of acJVS Filtering Requirements

To meet the challenge of better understanding what spectral components of the $\Delta\Sigma$ code are required, a zero-order JJ quantization simulation was devised using MATLAB [100]. From Section 1.5.3, the JJ array in the acJVS system is functioning as a pulse area quantizer in volt-seconds. To emulate this behavior in MATLAB, the original 4 Mb $\Delta\Sigma$ modulated code, discrete in both time and amplitude, is fed through a Simulink time-domain lumped-element representation of the analog low-pass filter, with a floating point double amplitude output in 10 Gbps discrete time. After the low-pass filter, the output amplitude is discretized to the nearest integer, simulating the JJ array pulse area, volts $\times$ seconds, quantization shown in Fig. 1.8. A block diagram of this simulation methodology is shown in Fig. 7.9.

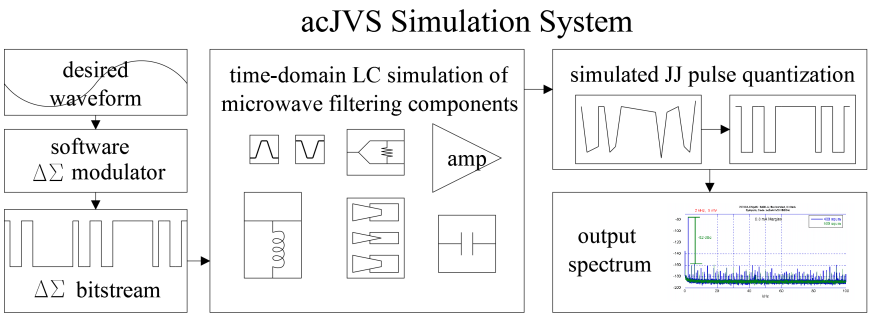


Figure 7.9: acJVS simulator conceptual block diagram to explore the relation of microwave component specifications to next-generation JVS outputs.

Initial simulations were performed in MATLAB to explore the acJVS parameter space. These simulated investigations suggest, as the performance envelope of acJVS systems is expanded, that all of the major system components shown in Fig. 1.10 will need to be simultaneously optimized: software $\Delta\Sigma$ modulator topologies, microwave $\Delta\Sigma$ excitation generators, microwave filtering components, bias electronics, and JJ arrays. The first step toward next-generation acJVS performance is to validate and expand this simulation methodology using simple hardware test cases like those discussed in Section 7.2. Once the challenges of designing and validating such a simulation system are met, it will be invaluable in the design of next-generation JVS systems.

7.4 A Feasibility Study for Microwave JVS Systems

The final challenge explored in this chapter lies in increasing the output frequency of acJVS systems. A far-reaching goal is the design of a microwave Josephson voltage synthesizer (MJVS) capable of generating arbitrary waveforms at microwave frequencies with the spectral purity advantages afforded by JJ pulse quantization. Such a system could employ a band-pass $\Delta\Sigma$ modulator algorithm to synthesize complex multi-tone microwave signals. This system would be fundamentally similar to the present acJVS system, illustrated in Fig. 1.10, with more stringent specifications on the microwave filtering components, and a high speed coaxial microwave output. A block diagram of a proposed MJVS system is shown in Fig. 7.10. A high-performance microwave notch filter is one of the vital components to realize such a system.

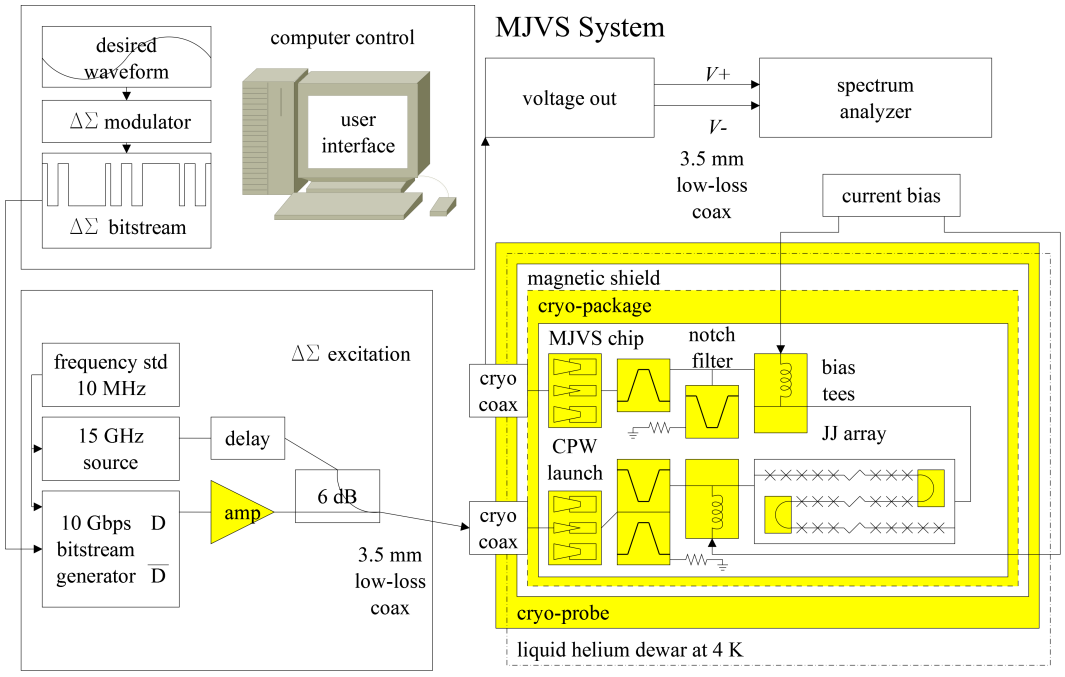
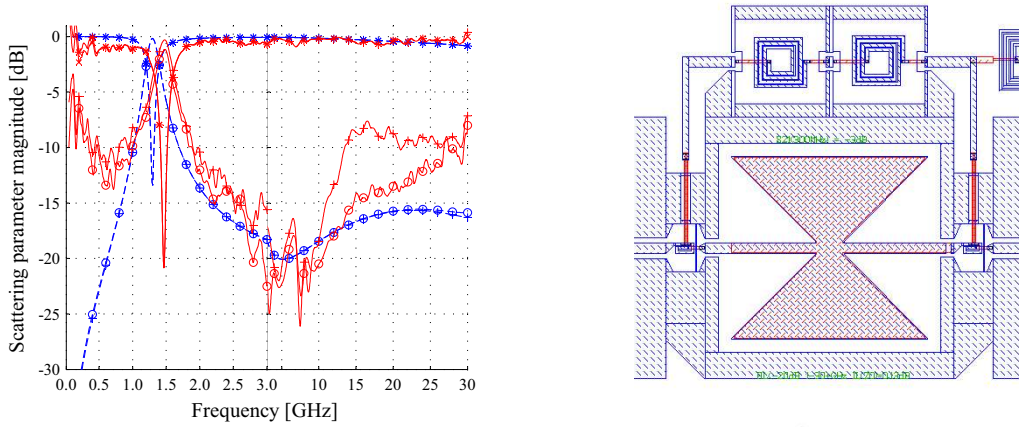


Figure 7.10: A block diagram of the band-pass ΔΣ modulated MJVS concept system for generating arbitrary waveforms at microwave frequencies.

7.4.1 MJVS Filter Feasibility Experiments

One of the components of this concept system that is most challenging to implement is the microwave filter. For proof-of-concept experiments, a MJVS synthesis frequency near 1 GHz was chosen as a viable trade off in component value requirements and synthesis frequency. The MJVS system, like the acJVS, will require a significant attenuation of the in-band signal and noise, at least 30 dB, and a broad pass-band from DC to the edge of the synthesis frequency and from the synthesis frequency to a high frequency set by the ΔΣ bit-stream-generator rise time, near 30 GHz. Further, because the pulse JJ quantization is a time domain mechanism, it is likely that an absorptive low-dispersion filter design will be required to implement the final system [101, 102].

As a proof-of-concept, first-order band-pass and band-stop filters were designed in the NIST QV IC technology to determine if such stringent specifications were achievable. Figure 7.11 a shows the measured and simulated S-parameters of the band-stop lumped-element filter layout shown in Fig 7.11 b. As these results show, achieving the very large upper pass band to pass the



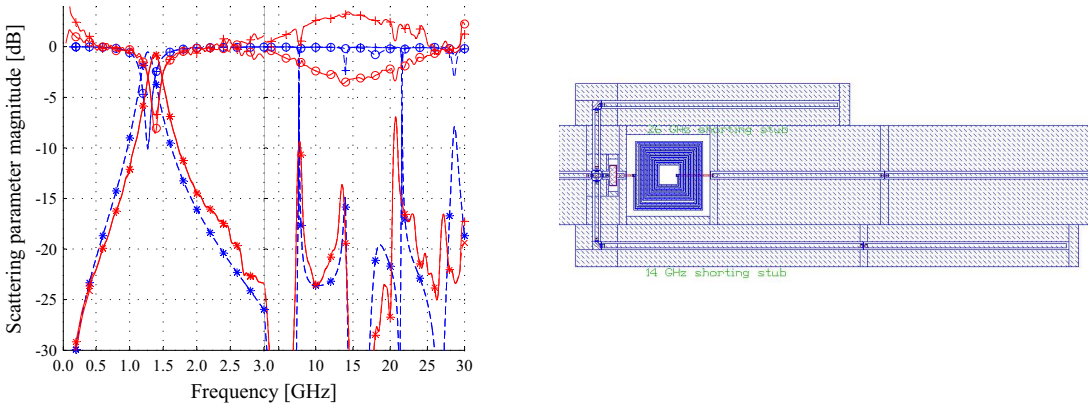
(a) (b)

Figure 7.11: MJVS 1.2 GHz band-stop filter prototype (a) measured and simulated S-parameter performance and (b) layout screen capture. HFSS simulated data is shown in blue dashed lines and measurement results are in red solid lines using a 4 K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, S_{21} is marked with $*$, and S_{22} is marked with $+$.

$\Delta\Sigma$ quantization noise without resonant drop-outs is a significant challenge. Further, designing a band-pass filter with a matched band to implement an absorptive filter is beyond the reach of the present modeling, design, and fabrication parameter targeting processes used in this thesis. Figure 7.12 c shows the measured and simulated S-parameters of the band-pass lumped-element filter layout shown in Fig 7.12 d.

7.5 Summary of Challenges to Future Investigators

In Section 7.1, hybrid lumped/distributed JJ loaded resonant arrays were demonstrated as a vehicle to improve microwave efficiency in JVS systems. These circuits successfully proved the resonant JJ array is a viable course of investigation for future JVS applications. The present state of the JJ technology is, unfortunately, insufficient to achieve useful voltage output levels. Bias current margins degrade rapidly for junction stack heights of more than three due to temperature gradients through the JJ stack [63]. For the hybrid resonant array topology to be applied in JVS systems, stack heights of 10–50 will be required. This resonant array technology has the potential to become useful with further advances in JJ stack technology.



(a) (b)

Figure 7.12: MJVS 1.4 GHz band-pass filter prototype (a) measured and simulated S-parameter performance and (b) layout screen capture. HFSS simulated data is shown in blue dashed lines and measurement results are in red solid lines using a 4 K TRL calibration on-chip. S_{11} is marked with $\circ$, S_{21} is marked with $\times$, S_{21} is marked with $*$, and S_{22} is marked with $+$. Note: a fabrication defect in the custom TRL short-circuit calibration standard for this measurement caused a offset in the measured S_{11} and S_{22} amplitudes at high frequencies.

Achieving higher output voltages and higher frequencies is the future of acJVS systems. The challenge of meeting these goals lies not only in improved microwave and JJ components, but in furthering the understanding of how each component affects the system. In order to establish causal links between component specifications and output waveform effects, an acJVS system simulation methodology needs to be designed, implemented, and validated against hardware.

Such a simulation technology will be vital in exploring the parameter space of a MJVS system. It is likely that the software $\Delta\Sigma$ modulator topology, the hardware band-pass filter, and the JJ array design will have to be simultaneously optimized to achieve a viable MJVS system. Results from the first-pass filter experiments, while encouraging with respect to feasibility, are a clear indication that these circuits will require a more precisely targeted modeling, design, and fabrication system. Even with improvements in the design flow, it is likely that a complex, multi-pole, low-dispersion-elliptical filter topology will require the ability to do post production tuning. This filter tuning will require the development of improved circuit elements and topologies, either electrically tunable elements, or mechanically laser-trimmed elements. MJVS systems are an exciting extension of this thesis for future investigation.

Chapter 8

10 V PJVS Prototype and Summary of Accomplishments

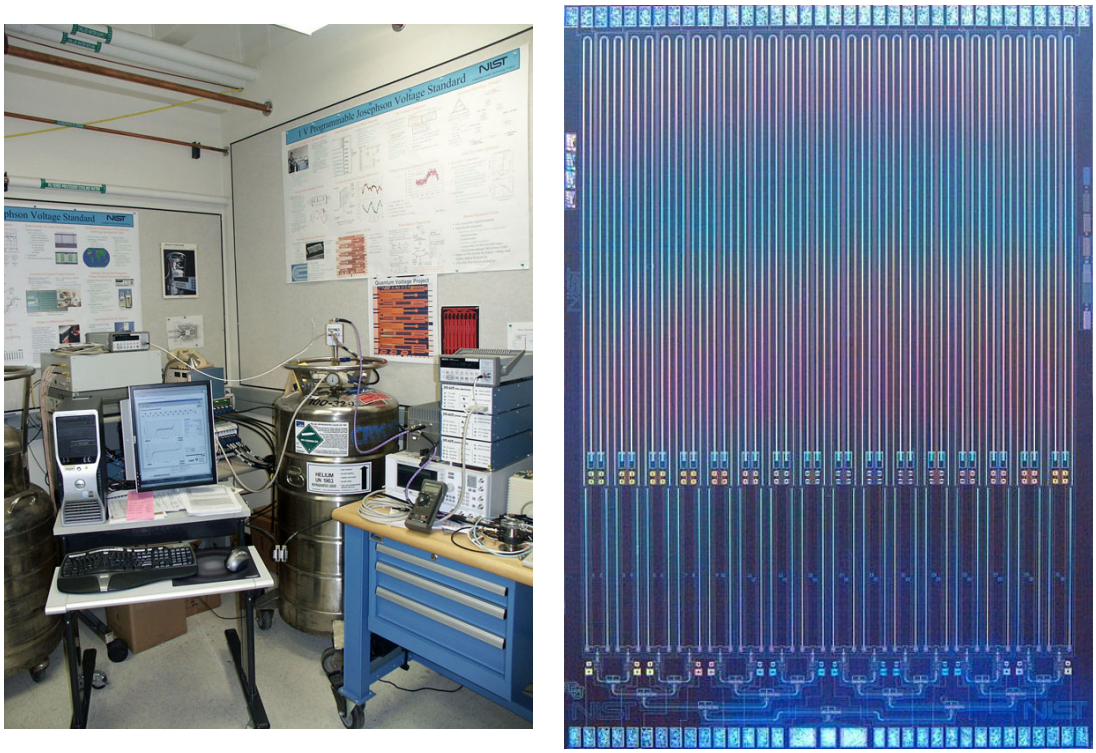
Contents

In the preceding chapters, a variety of microwave solutions have been presented to increase the performance of JVS systems. All of the highlighted components in Figs. 1.7 and 1.10 have now been discussed in detail, with significant improvements in performance demonstrated. In this chapter the measured results from the state-of-the-art NIST 10 V PJVS prototype will be presented in detail, highlighting the enabling microwave technologies. The 10 V PJVS is in the final stages of development, with only fabrication yield and final integration remaining to implement a production version.

The final sections of this thesis summarize the contributions of this work to JVS systems, and to the microwave community at large. This will include both work that is complete, as well as opportunities for future improvements.

8.1 A "Turn-key" 10 V PJVS System

As discussed in Chapter 1, JVS technology has revolutionized the measurement of the volt over the last few decades. One of the major hurdles in going from a staple of standards laboratories to a viable tool for a broader user base is the level of system integration. The dominant 10 V CJVS systems still require a metrologist trained in JVS technology and cryogenics to operate and periodically adjust the system for optimum operation. To overcome this challenge and be a viable tool for day-to-day measurements, the next generation 10 V PJVS needs to have front-to-back "turn-key" integration. Ideally, an untrained user should be able to turn the system on and, at the push of a button, automatically set all the required bias and excitation conditions, verify quantized operation, and output the desired voltage or stepwise approximated waveform. To achieve this goal, not only do the technical challenges discussed in this thesis need to be met, but the entire system needs to achieve a high level of integration. This will likely entail a closed cycle cryocooler and automatic control software with the capability to start, operate, and adjust the system without user intervention [40].



(a) (b)

Figure 8.1: (a) A photograph showing the NIST automated PJVS system of Fig. 1.7. Major components left-to-right include the control computer with a custom software package, the bias electronics, the helium dewar, the cryoprobe and package improved in Chapter 2, and the microwave excitation source. (b) A micrograph of the a 10 V PJVS prototype 12 mm × 17 mm chip with the 32-way Wilkinson divider technology developed in Chapter 3 (bottom) and 32 JJ arrays utilizing components developed in Chapter 5 (top).

8.1.1 System Components

The first steps toward this goal are quickly coming together due to the ongoing efforts of the NIST Quantum Voltage team. The fielded NIST 2.5 V PJVS systems in use around the world are capable of automatically adjusting bias parameters and verifying quantized operation. There are still areas that need further work to enable a turn-key 10 V PJVS: improved ability of the automated system to self-diagnose error conditions, cryocooler integration to shield the details of cryogenic operations from the user, and final tweaking of the microwave and junction technologies to achieve the 10 V benchmark with sufficient performance and yield to begin distributing systems. Figure 8.1 a shows a photograph of the NIST PJVS system.

This thesis has been primarily concerned with the microwave technology required to realize the system. The 10 V PJVS prototype chip, shown in Fig. 8.1 b, would not operate without the microwave components highlighted in Fig. 1.7. The improved bandwidth of the cryoprobe package discussed in Chapter 2 has enabled the microwave frequency to increase from 15 GHz to 18–20 GHz, yielding a 25% increase in output voltage. The high-performance, compact, divider technologies discussed in Chapters 3 and 4 were critical in both improving bandwith and squeezing the required 268 800 JJs onto the 12 mm × 17 mm chip, the maximum pattern area of the NIST quantum device fabrication facility.

The improved microwave structures discussed in Chapter 5 were vital to optimizing the performance of the large, impedance-tapered junction arrays, shown in Fig. 8.3 b, required to achieve 10 V [59]. Figures 8.2 and 8.3a compare the bias current boundaries of the quantized Shapiro voltage steps, shown in Fig. 1.1, over the 15–22 GHz frequency band of interest. When evaluated across an entire array, the $n = 0$ step suppression below I_C indicates the maximum single JJ microwave excitation, and $n = 1$ step current height indicates microwave excitation uniformity across all the JJs in the array. Figures 8.2 a and b show these step boundaries for legacy arrays with microwave issues, and Fig. 8.3 a shows the broadband step boundaries for the optimized 10 V PJVS prototype arrays incorporating the contributions of this thesis. For reference, Fig. 7.1 shows how Shapiro step height varies with uniform microwave power at a fixed 20 GHz frequency. This work has all but eliminated PJVS array performance dropouts in the microwave spectrum as shown in Fig. 8.3 a.

In the 10 V PJVS system, a custom software package is used to control both the microwave excitation channel and the DC bias electronics. The bias electronics package is a custom configuration of computer-controlled commercial components. The present system uses a 24-channel commercial DAC driving a custom amplifier board that converts the DAC outputs to appropriate array bias currents. This system is capable of driving 23 arrays, but is expandable for future higher resolution circuits. It is highly desirable to design the system with tight enough component tolerances that the desired level of bias point precision is achievable without calibration

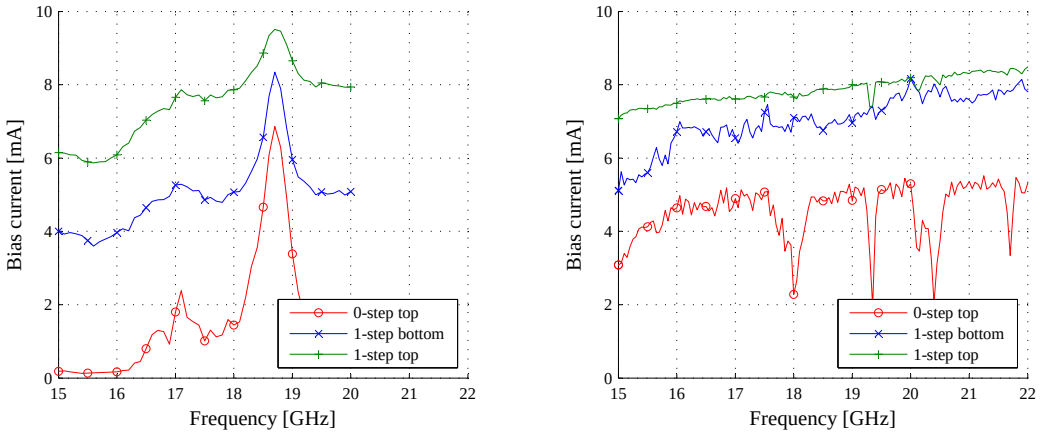


Figure 8.2: (a) A legacy PJVS array frequency sweep showing Shapiro step heights and a large reflection where very little microwave power is delivered to the chip at 18.7 GHz increasing the zero-step height and decreasing the one-step height. (b) A legacy PJVS array frequency sweep showing Shapiro step heights with several microwave resonances inside the array where some junctions are receiving too large a microwave power at 18.0, 19.5, 20.2 and 21.7 GHz decreasing the zero-step height and the one-step height.

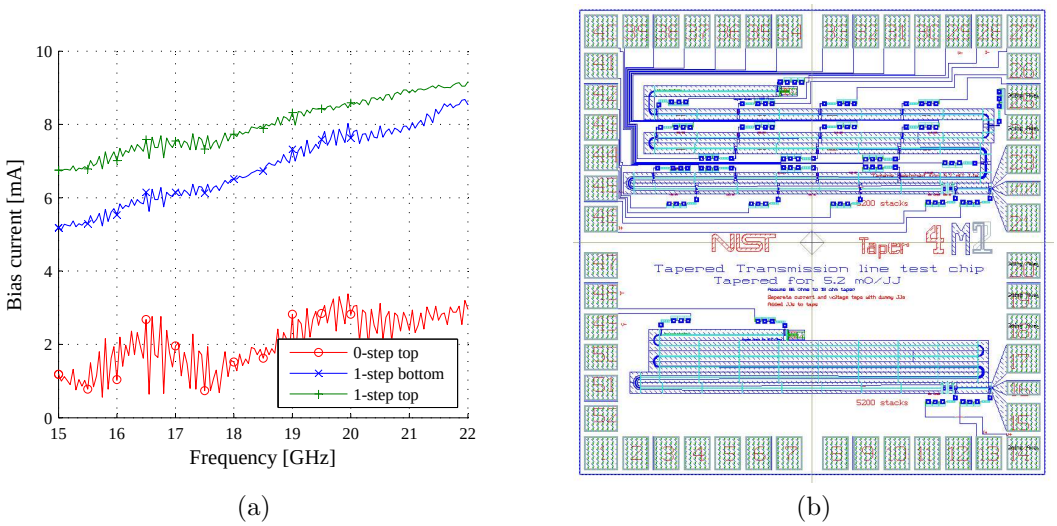


Figure 8.3: (a) A frequency sweep showing the broadband Shapiro step heights of a modern PJVS array after the optimizations detailed in this work. This device is packaged using technology developed in Chapter 2. For reference, Fig. 7.1 shows how Shapiro step height varies with uniform microwave power at a fixed 20 GHz frequency. (b) A layout of the most recent 10 mm × 10 mm PJVS array test chip with a full 15 600 JJ array (bottom) and 20 sub-arrays for microwave uniformity testing (top). These 85 Ω to 22 Ω impedance tapered arrays utilize the bias-tee, ground-tie, and termination structures developed in Chapter 5.

Table 8.1: 10 V PJVS Bias Electronics Design [40]

Design parameter	**Requirement**	**Current set point deviation**
DAC resolution	16 bits	0.004 mA/LSB
Output resistor	±0.05 %	±0.01 mA
Cryoprobe wire resistance	±0.05 Ω	±0.01 mA
Output stage gain uniformity	±0.02 %	±0.02 mA
Output stage DC offset	±0.05 mV (max)	±0.005 mA

of the DC bias electronics. For system self-verification purposes, ten distinct set-points in the 1 mA current range of the quantized voltage step are desired, setting the system specification at ±0.05 mA total accuracy. Table 8.1 breaks this acceptable tolerance down into various component requirements.

8.1.2 Measurements

The 10 V PJVS prototype chips, Figs. 1.6 b and 8.1 b, are nearly ready for integration into production systems. Figure 8.4 shows the measured current bias margins for which the entire chip has a quantized voltage step near 10 V scaled by the 18–20 GHz test frequency. It is this entire chip 268 800 JJ bias current margin that is important for system operation. This device exhibits a quantized voltage over a range of current greater than 0.55 mA for all frequencies between 18.2 GHz and 19.8 GHz. This voltage-step current height is obtained by subtracting the one-step bottom-corner bias-current value from the one-step top-corner bias-current value, e.g. the green line minus the blue line in Fig 8.3 a. The 10 V PJVS prototype bias current margins are somewhat smaller than the 2 mA current margins of fielded 1 V NIST PJVS devices [40]. These reduced bias current margins are partly by design due to the 10 V PJVS circuits using JJs with a smaller critical current, approximately 6 mA as compared with 10 mA for the 1 V PJVS, to decrease the IV power dissipated on the chip and ensure cryocooler compatibility of the final 10 V PJVS. The 10 V PJVS arrays are also a much larger and more difficult integration task at 15 600 JJs as compared to 4000 JJs per array on the 1 V PJVS. An improved prototype is

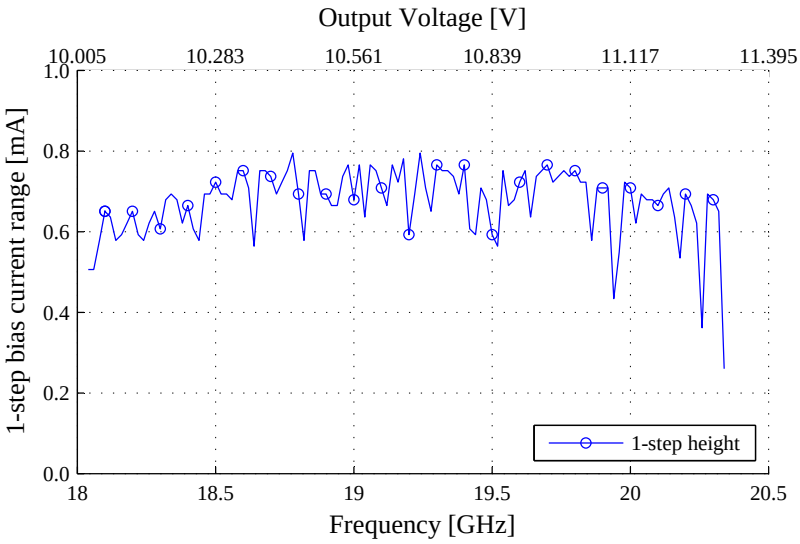


Figure 8.4: Measured 10 V PJVS prototype system bias current range for a quantized voltage step near 10 V, as scaled by the test frequency, with all arrays biased on the 1-step [40]. This step current height is obtained by subtracting the one-step bottom-corner bias-current value from the one-step top-corner bias-current value, e.g. the green line minus the blue line in Fig 8.2.

currently in work with incremental improvements to the microwave structures and JJ arrays in hopes of meeting the 1 mA current margin benchmark desired for the final system.

This 10 V PJVS achievement would not be possible without the hard work of the entire quantum voltage group, under Samuel Benz [1]. The system level integration, and the measurements shown in Fig. 8.4 were performed by Charles Burroughs [40], while the software integration effort was headed by Alain Rüfenacht [103]. Paul Dresselhaus headed the JJ array optimization effort [64] using JJ technology developed with the help of David Olaya, Nicola Hadacek, and Burm Baek [17, 18, 104].

8.2 Contributions of This Work

The contributions of this thesis to microwave engineering, and JVS technology, covered in detail in the preceding chapters, are summarized here. Portions of this work are enabling technologies for the next generation of JVS systems. The work summarized in this thesis has lead

to the publication of a first-author journal paper [57], two peer-reviewed first-author conference papers [55, 58], and several co-authored papers [38, 40, 59, 105, 106].

8.2.1 Improved JVS Packaging Technology Bandwidth

Contributions to the microwave design of cryogenic packages for NIST JVS devices were covered in detail in Chapter 2 [55]. This packaging technology has been critical to performance enhancements in both PJVS and acJVS systems. Wider package bandwidths have enabled permanent mounting of the state-of-the-art 300 $\mathrm{mV_{rms}}$ acJVS [56], as well as increasing the target excitation band of the 10V PJVS prototype to 18–20 GHz [38].

8.2.2 Broadband Lumped-element Wilkinson Dividers

To the best of the author's knowledge, Chapter 3 is the first demonstration of a broadband, multi-section, lumped-element Wilkinson power divider. The implementation of this device topology in both superconducting and commercial processes further validates its utility to a range of applications beyond the PJVS systems for which it was developed [57]. This concept was extended to a balanced topology for N-way dividers. Further, the divider/attenuator/combiner test configuration for N-way dividers significantly improves the testability of these devices. Sixteen-way and 32-way division using these circuits is a critical component in the working 10V PJVS system [40][1] .

8.2.3 Broadband Lumped-element Symmetric-hybrid Dividers

In Chapter 4 a broadband lumped-element symmetric-hybrid with a phase inverter was designed and implemented [58][2] . This topology presented is a combination of Parisi hybrid lumped-element sections [79], the symmetric-hybrid topology with its power division symmetry [82], and a 180° CPW phase inverter. This combination provides approximately double the bandwidth, and

[1] 2009 National Conference of Standards Laboratories International (NCSLI) Best Technical Paper Award.
[2] 2009 International Microwave Symposium Best Interactive Forum Paper Award.

significantly better amplitude and phase balance in 1/10 the area when compared to a canonical distributed 180° hybrid.

8.2.4 On-chip Microwave Devices to Improve JJ Array Performance

Chapter 5 is a collection of microwave circuits that were critical in achieving the JJ array microwave performance needed for the 10V PJVS prototype [59]. The collective contribution of these improved microwave devices has enabled modern PJVS arrays to operate resonance-free over the the entire 15–22 GHz PJVS band-of-interest, Fig. 8.2.

8.2.5 Progress Toward Next-generation JVS Systems

Initial experiments toward resonant JVS arrays, and larger-voltage, higher-frequency acJVS systems were performed in Chapter 7. These experiments have helped to eliminate several less fruitful paths of inquiry, and taken initial steps in directions that may prove promising for the next generation of JVS systems.

8.3 Conclusions

While this thesis has made significant progress, the microwave optimization of NIST JVS systems is by no means complete. Further improvements to both PJVS and acJVS systems remain as significant challenges posed to future investigators. Further microwave optimizations, as well as the system level challenges described in Chapter 7 and Section 8.1, promise to advance JVS technology from its current critical role in calibration and precision experiments, to a more broadly accepted and user-friendly measurement system for research and industry alike.

The 10 V PJVS is in final array optimization, while all of the quantitative microwave performance tests to date indicate microwave performance is vastly improved, the qualitative measurements of microwave performance through array bias current margins are still undergoing final parameter optimization. Isolating these issues and progress in the realm of both JJ effects

and microwave effects has occupied many months of research with much success. Future work promises to resolve these issues and achieve the desired 1 mA of bias current margins for a field-ready system.

The next big challenge in the JVS world, following the successful turn-key integration of 10 V PJVS systems, is to achieve 1 V_{rms} output voltages from an acJVS system, and to extend its frequency range. Initial experiments toward these goals have been covered in detail in Chapter 7. These future systems will have stringent microwave performance specifications. Key areas that need to be addressed to enable next-generation systems are: tunable linear circuits for high performance filters, higher density JJ arrays, improved process targeting and control, multilayer capacitor technologies to achieve large coupling capacitors, 4 K probed calibration and measurements of precision microwave components at NIST, microwave circuit topologies with stringent dispersion specifications, and improved understanding and optimization of the interactions of the entire $\Delta\Sigma$ excitation chain from the software modulator through the bit-stream-generator and microwave circuits to the JJ array.

This thesis is not the final word on microwave optimization for JVS systems, but merely a starting point on a lengthy and exciting path. Many challenges to future investigators in this realm remain, but the contributions of this thesis are intended to provide a solid foundation, a starting point for achievements to come. This work has provided a invaluable learning experience, as well as an opportunity to significantly contribute to critical systems, both presently in use and in development. It has been a pleasure to be involved in the many advances cataloged here, and it is hoped that this work will contribute to many more.

Bibliography

[1] S. P. Benz and C. A. Hamilton, "Application of the Josephson Effect to Voltage Metrology," *Proceedings of the IEEE*, pp. 1617–1629, October 2004. 2, 5, 6, 7, 8, 10, 11, 12, 13, 14, 25, 52, 130

[2] H. K. Onnes *Adad. Van Werschnappen*, vol. 1, p. 113, 1911. 3

[3] C. Kittel, *Introduction to Solid State Physics*. Upper Saddle River, NJ: Prentice Hall., 1999. 3, 4, 5

[4] T. V. Duzer and C. W. Turner, *Superconductive Devices and Circuits*. Upper Saddle River, NJ: Prentice Hall., 1998. 3, 4, 6

[5] B. A. Willemsen, "Practical Cryogenic Receiver Front Ends for Commercial Wireless Applications," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1457–1460, June 2009. 3

[6] V. L. Ginzburg and L. D. Landau *Zh. Eksp. Teor. Fiz.*, vol. 20, p. 1064, 1950. 3

[7] J. Barden, L. N. Cooper, and J. R. Schrieffer *Physics Review*, vol. 106, p. 162, 1957. 3

[8] R. Kautz, "Miniaturization of Normal-State and Superconducting Striplines," *Journal or Research of the National Bureau of Standards*, vol. 84, pp. 247–259, May-June 1979. 4

[9] B. Josephson, "Possible new effects in superconducting tunneling," *Physics Review Letters*, vol. 1, pp. 251–253, 1962. 4

[10] S. Shapiro, "Josephson Currents in superconducting tunneling, the effect of microwaves and other observations," *Physics Letters*, vol. 1, pp. 80–82, 1963. 6

[11] V. Kaplunenko and G. M. Fischer, "Josephson junction arrays as a variable inductor in RF circuits and tunable filters," *Institute of Physics Publishing: Superconductor Science and Technology*, pp. S145–S149, February 2004. 6, 7

[12] B. Bi, S. Han, J. E. Lukens, and K. Wan, "Distributed Josephson Junction Arrays as Local Oscillators," *IEEE Transactions on Applied Superconductivity*, vol. 3, pp. 2303–2306, March 1993. 6, 7, 109

[13] S. V. Shitov, "Recent Advancement in SIS Mixers for ALMA Project." Presentation to University of Colorado Active Antennas Group, September 2006. 6, 7

[14] S. K. Range, "Gravity Probe B: Exploring Einstein's Universe with Gyroscopes." NASA [Online document] [cited 2009 Dec 02], Available online: http://einstein.stanford.edu/content/education/GP-B_T-Guide4-2008.pdf (PDF), 2004. 6, 7

[15] L. Spietz, K. Irwin, and J. Aumentado, "Superconducting quantum interference device amplifiers with over 27 GHz of gain-bandwidth product operated in the 4–8 GHz frequency range," *Applied Physics Letters*, vol. 95, pp. 092505–1–3, 2009. 6, 7

[16] D. E. Kirichenko and T. V. Filippov and D. Gupta, "Microwave receivers with direct digitization," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1449–1452, June 2009. 6, 7

[17] P. D. Dresselhaus, Y. Chong, N. Hadacek, B. Baek, M. Watanabe, C. J. Burroughs, and S. P. Benz, "Silicide Barrier SNS Junctions for AC Josephson Voltage Standards," *Proceedings of the 10th International Superconductive Electronics Conference, ISEC'05*, pp. O–J04, September 5–9 2005. 7, 130

[18] B. Baek, P. D. Dresselhaus, and S. P. Benz, "Co-Sputtered Amorphous Nb_xSi_{1-x} Barriers for Josephson-Junction Circuits," *IEEE Transactions on Applied Superconductivity*, vol. 16, pp. 1966–1970, December 2006. 7, 130

[19] J. W. Lamb, "Miscellaneous Data on Materials for Milimetre and Submilimetre Optics," *International Journal of Infrared and Millimeter Waves*, vol. 17, pp. 1997–2034, December 1996. 7

[20] B. D. Taylor and Ed., "The International System of Units (SI)." Washington, DC: U.S. General Printing Office, NBS Special Publication, 1991. 10

[21] T. J. Quinn, "News from the BIPM," *Metrologia*, vol. 26, pp. 69–74, 1989. 10

[22] W. H. Parker, D. N. Langenberg, A. Denenstein, and B. N. Taylor, "Determination of e/h using macroscopic phase coherence in superconductors," *Physics Review*, vol. 177, p. 639, 1969. 10

[23] T. F. Finnegan, A. Denenstein, and D. N. Langenberg, "ac-Josephson-Effect Determination of e/h: A standard of electrochemical potential based on macroscopic quantum phase coherence in super conductors," *Physics Review B, Condensed Matter*, vol. 4, p. 1487, 1971. 10

[24] B. N. Taylor, W. H. Parker, D. N. Langenberg, and A. Denenstein, "On the use of the AC Josephson effect to maintain standards of electromotive force," *Metrologia*, vol. 3, p. 89, 1967. 10

[25] B. F. Field, T. F. Finnegan, and J. Toots, "Volt maintenance at NBS via 2e/h: A new definition of the NBS volt," *Metrologia*, vol. 9, pp. 155–166, 1973. 10

[26] T. Endo, M. Koyanagi, and A. Nakamura, "High-accuracy Josephson potentiometer," *IEEE Transactions on Instrumentation and Measurement*, vol. IM-32, pp. 267–271, March 1983. 11

[27] J. Niemeyer, J. H. Hinken, and R. L. Kautz, "Microwave-induced constant-voltage steps at one volt from a series array of Josephson junctions," *Applied Physics Letters*, vol. 45, pp. 478–480, 1984. 11

[28] C. A. Hamilton, C. J. Burroughs, and R. L. Kautz, "Josephson D/A converter with fundamental accuracy," *IEEE Transactions on Instrumentation and Measurement*, vol. 44, pp. 223–225, April 1995. 11, 14

[29] S. P. Benz and C. A. Hamilton, "A pulse-driven programmable Josephson voltage standard," *Applied Physics Letters*, vol. 68, pp. 3171–3173, May 1996. 11

[30] M. T. Levinsen, R. Y. Chiao, M. J. Feldman, and B. A. Tucker, "An inverse ac Josephson effect voltage standard," *Applied Physics Letters*, vol. 31, p. 776, 1977. 12

[31] C. A. Hamilton, R. L. Kautz, R. L. Steiner, and F. L. Lloyd, "A practical Josephson voltage standard at 1 volt," *IEEE Electron Device Letters*, vol. EDL-6, p. 623, December 1985. 12

[32] J. Niemeyer, L. Grimm, W. Meier, J. H. Hinken, and E. Vollmer, "Stable Josephson reference voltages between 0.1 and 1.3 V for high-precision voltage standards," *Applied Physics Letters*, vol. 47, p. 1222, 1985. 12

[33] F. L. Lloyd, C. A. Hamilton, J. A. Beall, D. Go, R. H. Ono, and R. E. Harris, "A Josephson array voltage standard at 10 V," *IEEE Electron Device Letters*, vol. 8, pp. 449–450, October 1987. 12

[34] S. P. Benz, "Superconductor-normal-superconductor junctions for programmable voltage standards," *Applied Physics Letters*, vol. 67, pp. 2714–2716, October 1995. 15

[35] H. Sachse, R. Pöpel, T. Weimann, F. Müller, G. Hein, and J. Niemeyer, "Properties of PdAu barriers of SNS junctions for programmable voltage standards," in *Applied Superconductivity 1997: Proc. EUCAS 1997, 3rd Eur. Conf. Applied Superconductivity, Inst. Phys. Conf. Series*, vol. 158, pp. 555–558, 1997. 15

[36] H. Schulze, R. Behr, F. Müller, and J. Niemeyer, "Nb/Al/AlOx/AlOx/Al/Nb Josephson junctions for programmable voltage standards," *Applied Physics Letters*, vol. 73, pp. 996–998, August 1998. 15

[37] H. Yamamori, M. Itoh, H. Sasaki, A. Shoji, S. P. Benz, and P. D. Dresselhaus, "All-NbN digital-to-analog converters for a programmable voltage standard," *Superconductor Science Technology*, vol. 14, pp. 1048–1051, November 2001. 15

[38] P. D. Dresselhaus, M. M. Elsbury, C. J. Burroughs, D. Olaya, S. P. Benz, N. F. Bergren, R. Schwall, and Z. Popović, "Design of a Turn-key 10 V Programable Josephson Voltage Standard System," *Conference on Precision Electromagnetic Measurements Digest*, pp. 102–103, June 2008. 15, 23, 25, 131

[39] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable 1 volt programmable voltage standard," *Applied Physics Letters*, vol. 71, pp. 1866–1868, September 1997. 17

[40] C. J. Burroughs, A. Rüfenacht, P. D. Dresselhaus, S. P. Benz, and M. M. Elsbury, "A 10 Volt "Turnkey" Programmable Josephson Voltage Standard for DC and Stepwise-Approximated Waveforms," *NCSLI Measure*, vol. 4, pp. 70–75, September 2009. 17, 23, 36, 47, 52, 66, 70, 125, 129, 130, 131

[41] P. Medawar, "Is the scientific paper a fraud?," *The Listener*, vol. 70, pp. 377–378, September 1963. 17

[42] T. Yamada, C. Urano, H. Nishinaka, Y. Murayama, A. Iwasa, H. Yamamori, H. Sasaki, A. Shoji, and Y. Nakamura, "Single-Chip 10-V Programmable Josephson Voltage Standard System Based on a Refrigerator and Its Precision Evaluation," *IEEE Transactions on Applied Superconductivity*, vol. 20, pp. 21–25, February 2010. 17

[43] J. P. A. Ioannidis, "Why most published research findings are false," *PLoS Med*, vol. 2, p. e124, August 2005. 17

[44] F. Mueller, R. Behr, T. Weimann, L. Palafox, D. Olaya, P. Dresselhaus, and S. Benz, "1 V and 10 V SNS programmable voltage standards for 70 GHz," *IEEE Transactions on Applied Superconductivity*, vol. 19, pp. 981–986, June 2009. 17

[45] C. Burroughs, A. Rüfenacht, S. Benz, and P. Dresselhaus, "Systematic Error Analysis of Stepwise-Approximated AC Waveforms Generated by Programmable Josephson Voltage Standards," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, pp. 761 –767, April 2009. 17

[46] P. Helistö, J. Nissilä, K. Ojasalo, J. S. Penttilä, and H. Seppä, "AC voltage standard based on a programmable SIS array," *IEEE Transactions on Instrumentation and Measurement*, vol. 52, pp. 533–537, April 2003. 17

[47] P. Kleinschmidt, P. D. Patel, J. M. Williams, and T. J. B. M. Janssen, "Investigation of binary Josephson arrays for arbitrary waveform synthesis," *IEE Proceedings - Science, Measurement and Technology*, vol. 149, pp. 313–319, November 2002. 17

[48] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, L. A. Christian, and J. X. Przybysz, "Pulse-driven Josephson digital/analog converter," *IEEE Transactions on Applied Superconductivity*, vol. 8, pp. 42–47, June 1998. 17, 18

[49] J. M. Williams, T. J. B. M. Janssen, L. Palafox, D. A. Humphreys, R. Behr, J. Kohlmann, and F. Muller, "The simulation and measurement of the response of Josephson Junctions to optoelectrically generated short pulses," *Superconductor Science and Technology*, vol. 17, pp. 815–818, 2004. 18

[50] S. P. Benz, C. A. Hamilton, C. J. Burroughs, and T. E. Harvey, "AC and DC bipolar voltage source using quantized pulses," *IEEE Transactions on Instrumentation and Measurement*, vol. 48, pp. 266–269, April 1999. 18

[51] S. Benz, P. Dresselhaus, A. Rüfenacht, N. Bergren, J. Kinard, and R. Landim, "Progress Toward a 1 V Pulse-Driven AC Josephson Voltage Standard," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, pp. 838–843, April 2009. 19

[52] S. Benz, P. Dresselhaus, C. Burroughs, and N. Bergren, "Precision Measurements Using a 300 mV Josephson Arbitrary Waveform Synthesizer," *Applied Superconductivity, IEEE Transactions on*, vol. 17, pp. 864 –869, June 2007. 19

[53] S. P. Benz, P. D. Dresselhaus, N. F. Bergren, and R. P. Landim, "Progress toward a 1 V Pulse-Driven AC Josephson Voltage Standard," *Conference on Precision Electromagnetic Measurements Digest*, pp. 48–49, June 2008. 19, 25, 26

[54] C. J. Burroughs, "Flexible Cryo-Packages for Josephson Devices," *IEEE Transactions on Applied Superconductivity*, vol. 15, pp. 465–468, June 2005. 22

[55] M. M. Elsbury, C. J. Burroughs, P. D. Dresselhaus, S. P. Benz, and Z. Popović, "Microwave Packaging for Voltage Standard Applications," *IEEE Transactions on Applied Superconductivity*, vol. 19, pp. 1012–1015, June 2009. 23, 25, 44, 131

[56] S. P. Benz, P. D. Dresselhaus, C. Burroughs, and N. Bergren, "Precision Measurements Using a 300 mV Josephson Arbitrary Waveform Synthesizer," *IEEE Transactions on Applied Superconductivity*, vol. 17, pp. 864–869, June 2007. 23, 25, 26, 30, 131

[57] M. M. Elsbury, P. D. Dresselhaus, N. F. Bergren, C. J. Burroughs, S. P. Benz, and Z. Popović, "Broadband Lumped-Element Integrated N-Way Power Dividers for Voltage Standards," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, pp. 2055–2063, August 2009. 23, 36, 55, 131

[58] M. M. Elsbury, P. D. Dresselhaus, S. P. Benz, and Z. Popović, "Integrated Broadband Lumped-Element Symmetrical-Hybrid N-way Power Dividers," *IEEE MTT-S International Microwave Symposium Digest*, pp. 997–1000, June 2009. 23, 66, 131

[59] P. D. Dresselhaus, M. M. Elsbury, and S. P. Benz, "Tapered Transmission Lines With Dissipative Junctions," *IEEE Transactions on Applied Superconductivity*, vol. 19, pp. 1012–1015, June 2009. 23, 47, 108, 127, 131, 132

[60] C. J. Burroughs, "Flexible Cryo-Packages for Josephson Devices," *IEEE Transactions on Applied Superconductivity*, vol. 15, pp. 465–468, June 2005. 25, 26, 29

[61] S. P. Benz, C. A. Hamilton, C. J. Burroughs, T. E. Harvey, and L. A. Christian, "Stable 1-volt programmable voltage standard," *Applied Physics Letters*, vol. 71, pp. 1866–1868, September 1997. 25

[62] C. J. Burroughs, S. P. Benz, T. E. Harvey, , and C. A. Hamilton, "1 volt dc programmable voltage standard system," *IEEE Transactions on Applied Superconductivity*, vol. 9, pp. 4145–4149, June 1999. 25

[63] Y. Chong, C. J. Burroughs, P. D. Dresselhaus, N. Hadacek, H. Yamamori, and S. P. Benz, "Practical high-resolution programmable Josephson voltage standards using double- and triple-stacked MoSi -barrier junctions," *IEEE Transactions on Applied Superconductivity*, vol. 15, pp. 465–468, June 2005. 25, 109, 122

[64] P. D. Dresselhaus, S. P. Benz, C. J. Burroughs, N. F. Bergren, and Y. Chong, "Design of SNS Josephson Arrays for High Voltage Application," *IEEE Transactions on Applied Superconductivity*, vol. 17, pp. 173–176, June 2007. 26, 52, 80, 86, 130

[65] This commercial tool is identified in this paper only in order to adequately specify the experimental procedure. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the equipment identified are necessarily the best available for the purpose. 27, 28, 30, 34, 37, 40, 41, 42, 53, 56, 60, 63

[66] C. J. Hsu, "Coplanar-Waveguide Dispersion Characteristics Including Anisotropic Substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 362–368, February 2001. 27

[67] R. R. Mansour, "Microwave Packaging for Voltage Standard Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, pp. 750–759, March 2002. 36

[68] A. R. Kerr, A. W. Lichtenberger, C. M. Lyons, E. F. Lauria, L. M. Ziurys, and M. R. Lambeth, "A Superconducting 180° IF Hybrid for Balanced SIS Mixers," *17th International Symposium on Space and Terahertz Technology*, May 2006. 36, 37, 56, 58

[69] J. Zhou, K. A. Morris, and M. J. Lancaster, "General Design of Multiway Multisection Power Dividers by Interconnecting Two-Way Dividers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, pp. 2208–2215, October 2007. 36, 47, 56

[70] Z. C. Hao, W. Hong, H. Li, H. Zhang, and K. Wu, "Multiway Broadband Substrate Integrated Waveguide (SIW) Power Divider," *Antennas and Propagation Society International Symposium, 2005 IEEE*, vol. 1A, pp. 639–642, July 2005. 36, 56

[71] A. R. Barnes, M. T. Moore, M. B. Allenson, and R. G. Davis, "A Compact 6–18 GHz Power Amplifier Module with 10 W Output Power," *IEEE MTT-S International Microwave Symposium Digest*, pp. 959–962, June 1999. 36, 56

[72] J. G. Kim and G. M. Rebeiz, "Miniature Four-Way and Two-Way 24 GHz Wilkinson Power Dividers in 0.13 µm CMOS," *IEEE Microwave and Wireless Components Letters*, vol. 17, pp. 658–660, September 2007. 36, 56

[73] L. H. Lu, P. Bhattacharya, L. P. B. Katehi, and G. E. Ponchak, "X-Band and K-Band Lumped Wilkinson Power Dividers with a Micromachined Technology," *IEEE MTT-S International Microwave Symposium Digest*, pp. 287–290, May–June 1979. 36, 56

[74] R. E. Collin, *Foundations for Microwave Engineering*, pp. 432–434. New York, NY: McGraw Hill, Inc., 1980. 37, 85

[75] D. M. Pozar, *Microwave Circuits, 2nd Ed*, pp. 278–282 470–473 632–640. New York, NY: John Wiley & Sons, Inc., 1998. 37, 39, 46, 58, 86, 92

[76] S. B. Cohn, "A Class of Broadband Three-Port TEM-Mode Hybrids," *IEEE Transactions on Microwave Theory and Techniques*, vol. 16, pp. 110–116, February 1968. 37

[77] F. Noriega and P. J. González, "Designing LC Wilkinson power splitters." [Online document] [cited March 13, 2007], Available online: http://rfdesign.com/images/archive/0802Noriega18.pdf, August 2002. RFdesign.com. 37, 39, 110

[78] G. S. Makineni and W. T. Joines, "Comparison of Broadband Performance of Two-Way Power Dividers and Combiners," *Microwave and Optical Technology Letters*, vol. 17, pp. 29–37, January 1998. 37, 39

[79] S. J. Parisi, "180° Lumped Element Hybrid," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1243–1246, June 1989. 37, 58, 60, 131

[80] S. S. Mohan, M. Hershenson, S. P. Boyd, and T. H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE Journal of Solid-State Circuits*, pp. 1419–1424, October 1999. 40, 96

[81] Applied Wave Research, USA, *Microwave Office*. 53, 96

[82] J. Hughes and K. Wilson, "High Power Multiple Impatt Amplifiers," *European Microwave Conference*, vol. 4, pp. 118–122, October 1974. 58, 66, 131

[83] Ansoft, USA, *HFSS*. 60

[84] A. Mellberg and J. Stenarson, "An Evaluation of Three Simple Scalable MIM Capacitor Models," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, January 2006. 72

[85] K. Y. Lee, S. Mohammadi, P. Bhattacharya, and L. P. B. Katehi, "Compact Models Based on Transmission-Line Concept for Integrated Capacitors and Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, December 2006. 72

[86] R. Shimon, D. Scherrer, D. Caruth, J. Middleton, H. Hsia, and M. Feng, "Accurate Passive Component Models in Coplanar Waveguide for 50 GHz MMICs," *IEEE MTT-S International Microwave Symposium Digest*, June 1997. 72

[87] American Technical Ceramics, *ATC 545L Series UBC™Capacitors: Data Sheet*, 2009. [Online document] [cited: February 27, 2009] Available online: http://www.atceramics.com/pdf/545l_series.pdf. 77

[88] Coilcraft, *Document 334L-1: Broadband Conical Inductors*, 2010. [Online document] [cited: December 12, 2009] Available online: http://www.coilcraft.com/pdfs/showpdf.cfm?file=bcl.pdf. 77

[89] P. M. Watson and K. C. Gupta, "EM-ANN Modeling and Optimal Chamfering of 90° CPW Bends with Air-bridges," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1603–1606, June 1997. 77, 78

[90] A. A. Omar, Y. L. Chow, L. Roy, and M. Stubbs, "Effects of Air-Bridges and Mitering on CPW 90 Degrees Bends: Theory and Experiment," *IEEE MTT-S International Microwave Symposium Digest*, pp. 823–826, 1993. 77

[91] U. Siart, "Matched resistive lumped element two-port attenuators." [Online document] [cited: Feb 22, 2010], Available online: http://www.siart.de/lhre/attenuator.pdf, 2009. 83

[92] H. W. Schubler, *Netzwerke, Signale, und Systeme*. Springer, 2009. 83

[93] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*. Dedham, MA: Artech House Books., 1980. 85

[94] rfic.co.uk, "RF, RFIC, & Microwave Theory, Design: Hybrids." [Online document] [cited: June 2, 2008] Available online: http://www.odyseus.nildram.co.uk/RFMicrowave_Circuits_Files/Hybrid.pdf, 2007. 87

[95] B. Manz, "UC Boulder Students Design Real-World MMICs," *Microwave Product Digest*, pp. 70–75, June 2009. [cited 2010 Jan 21], Available online: http://www.mpdigest.com/issue/Articles/2009/june/barry/Default.asp. 92

[96] TriQuint Semiconductor, Hillsboro, OR, USA, *TQPED Design Manual V1.9*, 2007. 92

[97] TriQuint Semiconductor, Hillsboro, OR, USA, *Production Process TQPED 0.5 um E/D pHEMT Foundry Service*, 2007. [Online document] [cited March 23, 2008] Available online: http://www.triquint.com/prodserv/foundry/docs/TQPEDv2_2.pdf . 97

[98] Avago Technologies, *AMMP-5024: 30kHz–40 GHz Traveling Wave Amplifier: Data Sheet*, 2008. [Online document] [cited: October 13, 2010] Available online: http://www.avagotech.com/docs/AV02-0465EN.pdf. 103

[99] N. Hadacek, P. D. Dresselhaus, and S. P. Benz, "Lumped 50-Ω Arrays of SNS Josephson Junctions," *IEEE Transactions on Applied Superconductivity*, vol. 16, December 2006. 109

[100] The MathWorks, Inc., USA, *MATLAB Version R2009b*. 119

[101] J. R. Andrews, "Application Note AN-3a: Pulse Measurements in the Picosecond Domain." [Online document] [cited: November 29, 2009] Available online: http://www.picosecond.com/objects/AN-03a.pdf, 1988. 121

[102] J. Breitbarth and D. Schmelzer, "Absorptive Near-Gaussian Low Pass Filter Design with Applications in the Time and Frequency Domain," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1303–1306, June 2004. 121

[103] A. Rüfenacht, C. J. Burroughs, and S. P. Benz, "Precision sampling measurements using ac programmable Josephson voltage standards," *Review of Scientific Instruments*, vol. 79, pp. 044704–1–044704, 2008. 130

[104] D. Olaya, P. D. Dresselhaus, S. P. Benz, J. Bjarnason, and E. N. Grossman, "Amorphous Nb-Si Barrier Junctions for Voltage Standard and Digital Applications," *IEEE Transactions on Applied Superconductivity*, vol. 19, June 2009. 130

[105] C. J. Burroughs, P. D. Dresselhaus, A. Rüfenacht, M. M. Elsbury, and S. P. Benz, "Design of the NIST 10 V Programmable Josephson Voltage Standard System," *Conference on Precision Electromagnetic Measurements Digest*, 2010. in press. 131

[106] P. D. Dresselhaus, M. M. Elsbury, C. J. Burroughs, and S. P. Benz, "Microwave Optimization of 10 V PJVS Circuits," *Conference on Precision Electromagnetic Measurements Digest*, 2010. in press. 131