A 10.8-GHz GaN MMIC Load-Modulated Amplifier

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***Abstract*— This work presents a 10.8-GHz load-modulated MMIC power amplifier designed in the 0.25 μm GaN-on-SiC Cree Wolfspeed process. The carrier amplifier has a single stage and is biased in class-AB, while the peaking path is designed as a two-stage amplifier. The output power at saturation is 35.5 dBm with 7.6 dB of gain and PAE of 38%. At 7-dB output power backoff, the PAE remains above 26%. The combiner network is synthesised with a black-box method constrained to exhibit Doherty amplifier behaviour. The disagreement between measurements and simulations is explained in part through an analysis of the interstage matching network using scattering parameters renormalised to complex terminations.**

***Keywords*— Gallium Nitride, power amplifier, Monolithic Microwave Integrated Circuit (MMIC), Doherty, load modulation**

I. Introduction

The Doherty amplifier topology, an industry workhorse for decades, has been demonstrated in previous generations of communications bands below X-band as well as at Ka-band with capabilities for MIMO array integration [1], [2], [3]. While Doherty examples operating in X-band have been documented [4], [5], for radar and remote sensing applications, recent redistribution and division of commercial spectrum and expansion merits greater investigation into frequency scalable designs.

Various modifications of the Doherty topology at millimetre-wave frequencies include the incorporation of bondwires in a quasi-MMIC Doherty structure [6], variation of load modulation range for maximum backoff performance [7], and reduction in size [8]. The work presented in this paper follows a black-box design method that enables a network to be synthesised from current and voltage behavioural bounds set by the expectations of load-modulated Doherty-type operation. A load-modulated amplifier at 11 GHz, shown in Fig.1 is designed in the 0.25 μm Cree Wolfspeed GaN process with 6x100 μm slot vias. It is tested with a continuous wave signal and reaches a maximum output power of 35.5 dBm with 7.6 dB of gain and 38% PAE, and at 7 dB output power back off has 7.4 dB of gain, 32% drain efficiency, and 26% PAE.

II. MMIC Design and Analysis

The topology of the load-modulated amplifier is chosen to enable an unequal split at the input by adding gain to the peaking path and enabling control of the back-off level through controlling the bias and therefore the gain of the driver. The driver stage in the peaking path is designed around a $2\times100\,\mu$m device biased at -5 V (class-C with low gain) and a power stage with a $6\times100\,\mu$m device biased in class C at -3.2 V. The power stage transistor of the peaking branch is biased to be completely off during back-off operation. The single-stage main carrier branch with a $6\times100\,\mu$m device is biased in class AB at -2.8 V (18 mA). All transistors are supplied with a nominal 28 V drain voltage. Simulated load-pull data at 11 GHz is presented in Table 1. The design targets PAE at saturation and at 6-dB output back-off.

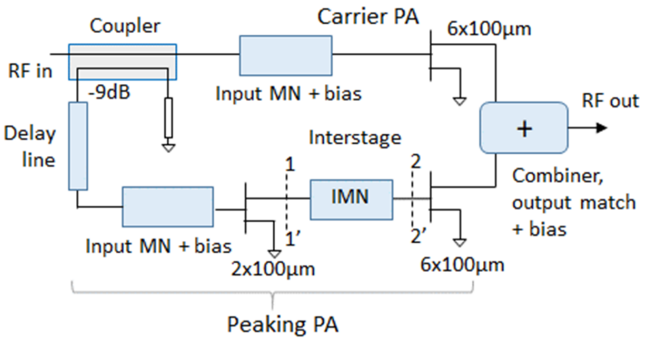


Fig. 1. A block diagram of the Doherty-type load-modulated PA. The RF input is divided between the carrier and peaking paths through a 9-dB coupler. The peaking amplifier path is a two-stage design with a delay line that compensates for the phase shift of the coupler, combiner network and peaking driver.

Table 1. Simulated load-pull data at 11 GHz for the stabilised and input-matched carrier and peaking branches.

	$Z_L(\Omega)$	P_{out}(dBm)	P_{in}(dBm)	PAE(%)
Carrier, P_{max}	26+j54	34.2	26	53
Carrier, P_{bo}	14+j63	30.8	21	48
Peaking, P_{max}	28+j60	32.2	22	40

The design is performed using a "black-box method" presented in [9], [10] using the manufacturer-provided nonlinear device models. Fig. 2 shows the load-pull contours of the carrier path for delivered power and PAE, the contours of delivered output power at the first gain stage of the peaking path, and the PAE of the second stage of the peaking path when cascaded with the first stage. The load-pull data for the two branches is extracted with EM-simulated input matching, interstage matching, stabilisation networks, and bias networks included (i.e. everything but the combiner and input splitter). The off-state impedance of the peaking amplifier branch is $4-j71\,\Omega$. From the load-pull data, 72% of the input power should be split into the carrier path with the input un-even divider. At X-band, the mutual loading of the two paths is significant

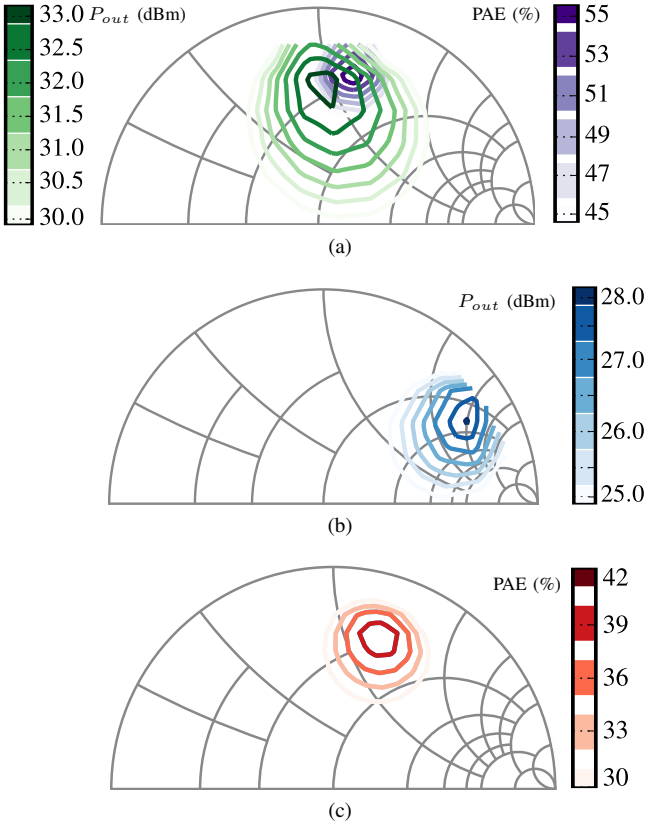


Fig. 2. Load-pull contours for (a) output power and PAE at the main carrier stage transistor drain, and (b) output power at the first peaking stage transistor drain. (c) Load-pull PAE contours at the second peaking stage transistor drain when driven by the first peaking stage.

and the initial estimate is adjusted to 86% after tuning for best efficiency. The 9-dB input divider is implemented with a coupled line, and the combiner is synthesised assuming a topology with two high-pass Π-networks, following the method in [9]. A delay line in the peaking path compensates for the phase shift of the coupler, combiner network and driver.

III. Measurements

A photograph of the fabricated MMIC is shown in Fig. 3. The inputs and outputs are wire-bonded to 50-Ω microstrip lines on alumina. Each MMIC measures 3.9 mm by 2.4 mm, and is mounted onto copper tungsten plates measuring 13.64 mm by 20.24 mm. Fig. 4 shows the input match of the amplifier circuit at low drive power. The measured match of the three fabricated chips at low drive power (approximately 5 dBm) is best around 9.5 GHz; as the drive power increases to 31 dBm, the match improves to cover the 10.5-11.3 GHz range. The simulated input match is around 11 GHz. In Fig. 5, the simulated small-signal gain reaches a maximum of 10.9 dB at 9.6 GHz, with an approximate fractional bandwidth of 16 %.

The measured scattering parameters of the MMICs show a similar trend as simulated between 10 and 11 GHz. The gain is in general lower than simulated, except around 9.6 GHz where the input match is unpredictably good. These two plots suggest that the transistor models may not predict small-signal conditions. The model validation obtained

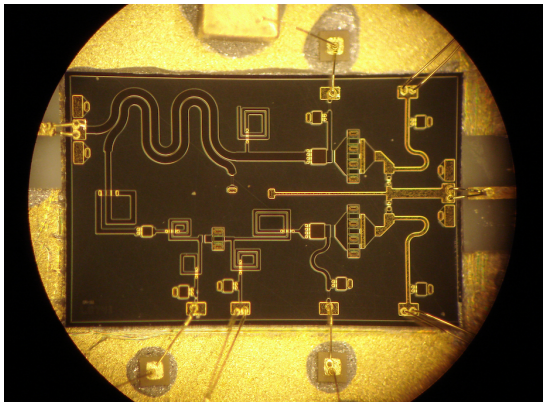


Fig. 3. A photograph of one of three measured die. The inputs and outputs are wire-bonded to 50-Ω alumina microstrip lines. The MMIC measures 3.9 mm by 2.4 mm, and is mounted onto copper tungsten plates measuring 13.64 mm by 20.24 mm.

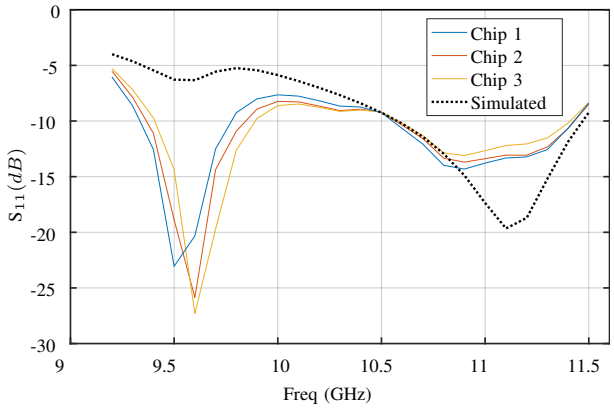


Fig. 4. $|S_{11}|$ of the three MMICs: measured (solid lines) and simulated (dotted line). The measured scattering parameters of the MMICs show a trend similar to simulation between 10 and 11 GHz.

from the manufacturer is performed over a broad range of parameters, making it difficult to accurately predict the highly pinched-off class-C peaking amplifier in a load-modulated environment.

The amplifier is driven with a continuous-wave signal at 10.8 GHz. Fig. 6 shows the gain and output power as

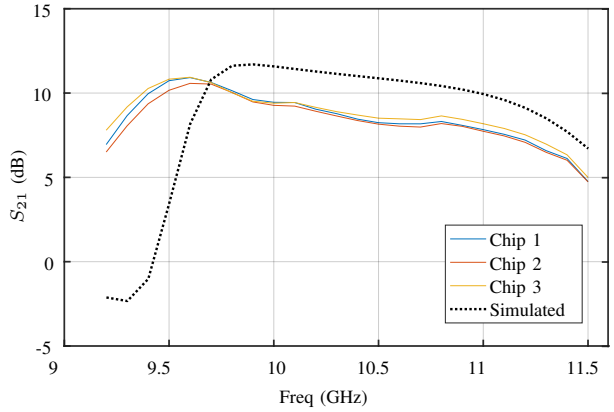


Fig. 5. The measured (solid line) small-signal gain compared to simulated (dotted line). The gain is in general lower than simulated, except around 9.6 GHz where the input match is unpredictably good.

Table 2. A comparison of X-Band Doherty MMICs in literature

Author, Year	Freq	V_{DD}	Output Power (dBm)	Gain	Peak PAE	PAE at 6-dB OPBO	Technology
[4], 2015	10	20	36.2	9.2	47	40	0.15 μm GaN on SiC pHEMT
[5], 2017	14.6	-	36	7	39	27	0.25 μm GaN on SiC HEMT
[6], 2017	7	30	42	18	36	31	0.25 μm GaN HEMT
[7], 2017	15	4	26.5	17	41	29	0.15 μm GaAs pHEMT
This work	**10.8**	**28**	**35.6**	**7.4**	**38**	**28**	**0.25 μm GaN HEMT**

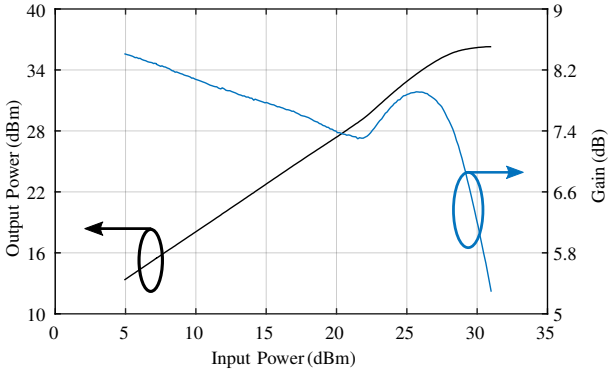


Fig. 6. Measured output power and gain versus input power at 11 GHz. The maximum output power is 35.5 dBm at an input drive of 27.9 dBm.

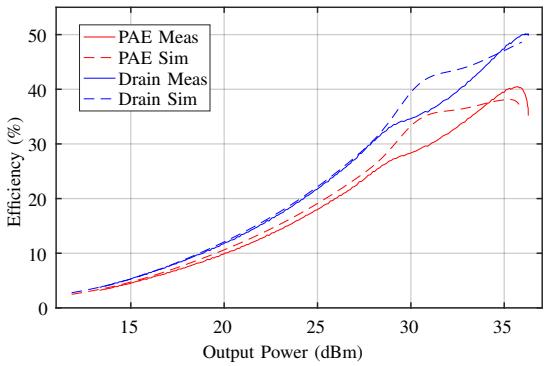


Fig. 7. Measured (10.8 GHz) and simulated (11 GHz) efficiency match at saturated output power as well as at 7 dB back-off.

functions of input power. Fig. 7 shows the power-added and drain efficiencies from both simulation (11 GHz) and measurement(10.8 GHz. The load-modulating prototype reaches a maximum output power of 35.5 dBm, with 7.6 dB of saturated gain, 48% drain efficiency, and PAE = 38%. At 7 dB output power back off, the gain is 7.4 dB with 32% drain efficiency and PAE 26 %. These values are summarised in Table 2 alongside other documented Doherty MMIC designs at similar frequencies.

IV. Interstage Analysis

The measured gain of the PA is lower than expected, indicating an additional source of loss. If the peaking PA interstage network loss is high, the overall gain of this path will be reduced. The dissipative loss of the network is further investigated using the equation

$$DL = 10\ log_{10}\frac{|S_{21}|^2}{1-|S_{11}|^2}, \tag{1}$$

which accounts for input mismatch loss assuming a terminated output port. This analysis requires us to renormalise the network from a 50 Ω port termination to one of complex terminations. To do this, we use the following equations [11]:

$$S_{21}(\gamma_1,\gamma_2) = \frac{\Lambda_1^*\Lambda_2^* S_{21}}{(1-\gamma_2 S_{22})(1-\gamma_1 S_{11}) - (\gamma_1\gamma_2 S_{12}S_{21})} \tag{2}$$

$$S_{11}(\gamma_1,\gamma_2) = \eta_1\frac{(1-\gamma_2 S_{22})(S_{11}-\gamma_1^*) + \gamma_2 S_{12}S_{21}}{(1-\gamma_2 S_{22})(1-\gamma_1 S_{11}) - (\gamma_1\gamma_2 S_{12}S_{21})}, \tag{3}$$

$$S_{22}(\gamma_1,\gamma_2) = \eta_2\frac{(1-\gamma_1 S_{11})(S_{22}-\gamma_2^*) + \gamma_1 S_{12}S_{21}}{(1-\gamma_2 S_{22})(1-\gamma_1 S_{11}) - (\gamma_1\gamma_2 S_{12}S_{21})}, \tag{4}$$

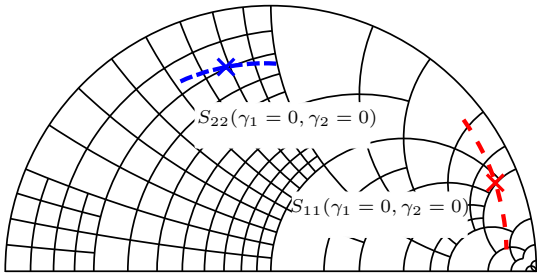
where the γ parameters describe the deviation of the complex port impedances from 50Ω:

$$\gamma_n = \frac{Z_n - R_{0n}}{Z_n + R_{0n}}\ , \qquad \eta_n = \Lambda_n^*/\Lambda_n$$

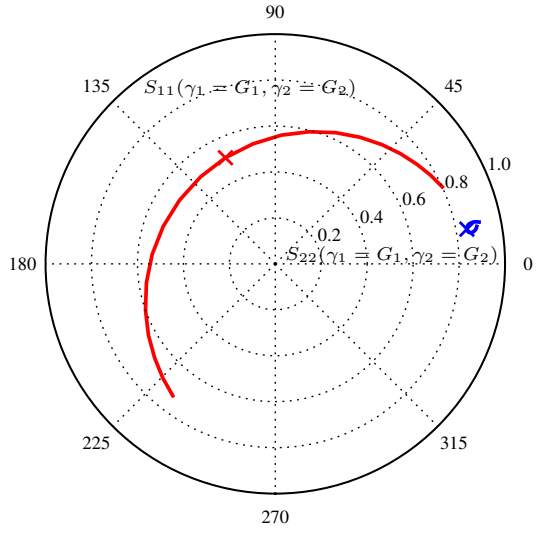
$$\Lambda_n = (1-\gamma_n^*)\sqrt{\frac{1-\gamma_n\gamma_n^*}{(1-\gamma_n)(1-\gamma_n^*)}}, \qquad n = 1,2$$

In this case, $S_{ij}(\gamma_1 = 0, \gamma_2 = 0)$ indicates standard scattering parameters with real terminations $R_{01} = R_{02} = 50\,\Omega$. Fig. 8a shows the input and output matches of the network when the circuit analysis is normalised in this way. The port impedance at plane 11' in Fig. 1 is $Z_1 = 72.9 - j160.4\,\Omega$, i.e. the small-signal output impedance of the driver transistor under class-B bias, so as to represent the transistor in an "on" state while driven. The port impedance at plane 22' is $Z_2 = 3.57 - j7.3\,\Omega$, as it is the input impedance of the second stage transistor, also biased in class-B. $S_{ij}(\gamma_1 = 0.7 - j0.4, \gamma_2 = -0.83 - j0.25)$ is the renormalisation of the scattering parameters to these complex terminations. The reflection coefficient magnitudes after renormalisation to complex port impedances are shown in Fig. 8b, indicating that the match to Z_1 and Z_2 could still be improved by adjusting the interstage matching network design.

Fig. 8c shows $|S_{11}|$ and $|S_{22}|$ for both cases, as well as the dissipative loss of the network using the complex-normalised definitions. At the design frequency, there is approximately 6.5 dB of loss due to a combined effect of conduction loss, coupling of lines, bias tee design, and the series resistor which is necessary for stability.



(a)



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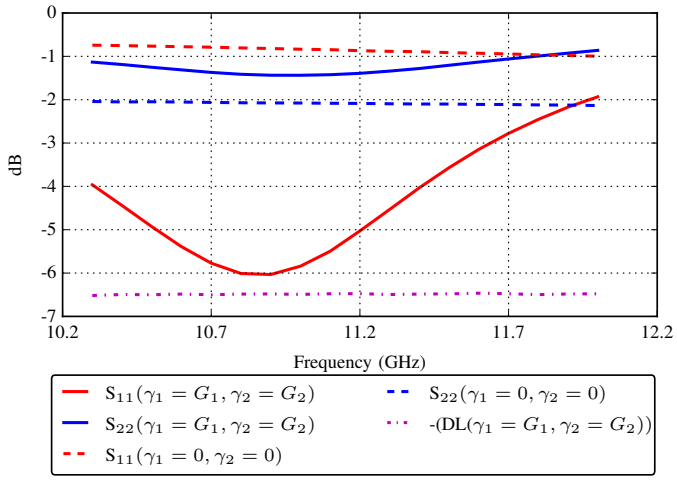

(c)

Fig. 8. The S_{11} and S_{22} of the interstage matching network when normalised to (a) $50\,\Omega$ and (b) $Z_1 = 72.9 - j160.4\,\Omega$ and $Z_2 = 3.57 - j7.3\,\Omega$, which corresponds to $G_1 = 0.7 - j0.4$ and $G_2 = -0.83 - j0.25$. (c) A comparison of the two sets of $|S_{11}|$ as well as the dissipative loss plotted across frequency. At the design frequency, indicated by an "×" in (a) and (b), there is approximately 6.5 dB of loss.

V. Conclusion

The load-modulated Doherty-type PA designed in this work employs an uneven split and additional gain in the peaking path in order to address potential gain limitations at X-band. Although agreement between measurement and simulation is limited near 2–7 dB output back-off, the PA demonstrates comparable efficiency and output power to the best reported works in this band. We investigate interstage loss using renormalised scattering parameters to evaluate potential causes for the measured behaviour. The discrepancy from simulation is in part attributed to limitations in the device models, which are often fitted to a broad range of frequency and power, providing versatility but offering limited accuracy for specific arbitrary use cases. Nonetheless, the load-modulated Doherty-type MMIC amplifier designed with a black-box method demonstrates satisfactory first-pass performance.

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