A Three-Stage 18.5–24-GHz GaN-on-SiC 4 W 40% Efficient MMIC PA

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***Abstract*— This paper presents the design and measured continuous-wave (CW) performance of a three-stage *K*-band monolithic microwave integrated circuit (MMIC) power amplifier (PA) implemented in a 150-nm GaN-on-SiC process. The transistor peripheries are staged at a ratio of 1:2:8, and the output stage consists of two reactively combined 8 × 100 μm HEMTs with individual source vias. The measured peak output power is greater than 4 W with peak power added efficiency (PAE) of greater than 40%. The output power exceeds 3.2 W over the frequency range of 18–24 GHz with less than 1.5-dB variation. The three-stage architecture enables greater than 20 dB of saturated gain from 18.5 to 24 GHz. The bandwidth, output power, and efficiency performance are investigated as a function of output stage drain voltage. A statistical analysis for 230 die fabricated on five wafers is presented, and eight MMICs are mounted and characterized over power and frequency.**

***Index Terms*— Broadband, efficiency, GaN, monolithic microwave integrated circuit (MMIC), power amplifiers (PAs).**

I. Introduction

ONE of the standard frequency ranges for satellite communications is in the *K*-band, from approximately 18–27 GHz [1]. For increased spectral efficiency, multi-carrier signals with over 1-GHz instantaneous bandwidths and high peak-to-average power ratios (PAPR) are desired. Gallium nitride (GaN) solid-state power amplifiers (PAs) are considered for these satellite applications as an alternative to TWTs, and are therefore required to operate very efficiently. GaN-based Doherty PAs [2] and linear amplifiers [3] have been explored to this end. Published *K*-band GaN PAs include a single-frequency [4] and broadband two-stage designs [2], [5] in a commercial GaN-on-SiC process. Other three-stage [3], [6], two-stage [7], [8], and single-stage [9] PAs have been demonstrated in research GaN processes, as summarized in Table I.

Here, we demonstrate a three-stage reactively matched *K*-band GaN monolithic microwave integrated circuit (MMIC) amplifier, shown in Fig. 1, fabricated in the Qorvo 150-nm, 28-V process. The design maximizes efficiency, with power added efficiency (PAE) exceeding 40% while reaching a target peak output power of 4 W and peak saturated gain of 25 dB. The output power exceeds 3.2 W with over 20-dB gain for the 18.5–24-GHz frequency range. Performance and design criteria are evaluated for a drain supply voltage range of 10–28 V, with a nominal bias point of 100 mA/mm for a drain voltage of 20 V.

The paper presents the design flow, starting with transistor sizing and network design, and statistical analysis of 230 on-wafer probed amplifier chips. Section II overviews process considerations focusing on the performance of the final stage transistor over supply voltage and frequency. Section III discusses matching network synthesis for a non-isolated reactive combiner and details the design approach for the amplifier, including stabilization. Section IV presents probed performance of the amplifier and shows a statistical analysis of

TABLE I
Comparison of *K*-Band GaN Amplifiers

Freq. (GHz)	Frac. BW (%)	P_{out} (dBm)	PAE (%)	Gain (dB)	Year Ref.
26	-	33.5	42	8	2017 [4]
17-20	16	29.7	36	4	2017 [9]
21-23	9.1	37	48	16.7	2012 [2]
18-20	10.5	31	22	16	2014 [6]
18-19	5.4	40	30	20	2016 [7]
20.8-22.4	7.4	39.5	35	22	2016 [3]
17.2-20.2	16	40	38	18	2017 [5]
18-19	5.7	40	30	14	2017 [7]
18.5-24	**26**	**36.5**	**40**	**25**	**This work**

Peak values at saturation are shown for all table entries.

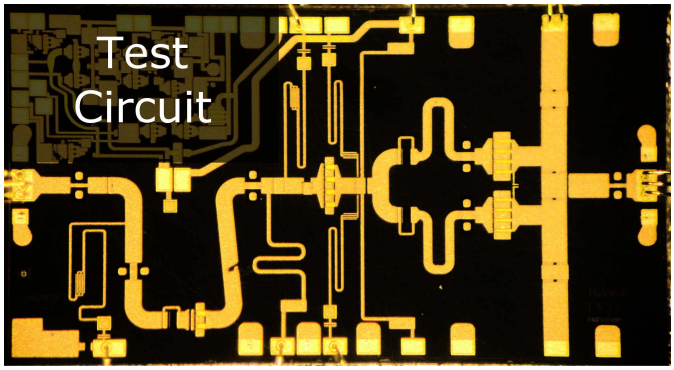

Fig. 1. Photograph of the three-stage *K*-band MMIC, 4 mm × 2 mm in size, fabricated in the Qorvo 150-nm GaN-on-SiC process. The top left part of the die is a test circuit which is not a part of the PA. The output stage devices are 8 × 100 μm with a nominal drain voltage of 20 V at 100 mA/mm. Three bondwires connect the amplifier RF bond pads to the alumina input and output lines. A single bondwire is used for all dc bias lines excluding the final stage where dc current draw is the highest.

Manuscript received January 21, 2019; revised May 15, 2019; accepted June 12, 2019. Date of publication July 11, 2019; date of current version August 23, 2019. This work was supported by Lockheed Martin under Award #S16-025. This paper was approved by Guest Editor Shahriar Shahramian. *(Corresponding author: Maxwell Robert Duffy.)*

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Digital Object Identifier 10.1109/JSSC.2019.2924087

measured large signal data over five wafers. Finally, Section V shows connectorized measured PA performance.

II. Power Stage Transistor Analysis

The amplifier presented in this work is designed in a Qorvo 150-nm GaN on 100-μm SiC process with slot vias. An 8 × 100 μm transistor, with pairs of 15-μm spaced gates with internal source vias within the 52-μm spacing between pairs, is chosen for the output network. A nonlinear model (EEHEMT in NI/AWR Microwave Office), validated up to 18 GHz for a 25 °C backside temperature, is extrapolated through K-band.

Load–pull is simulated at 21 GHz, which is the center frequency of the design band (18–24 GHz). The output stage transistor is simulated for drain voltages from 10 to 28 V (28 V being the highest recommended bias point for the process) with a 100-mA/mm quiescent current. For each load–pull point, the optimum source impedance is also found, in order to ensure a good input match. This is done to evaluate the output stage transistor performance for possible supply modulation operation.

The load–pull data are gathered for a range of bias voltages and assessed for two cases: a maximum PAE match and a maximum P_{out} match. For each of these cases, at each voltage level, the output reflection coefficient, Γ_{L}, is converted into an equivalent parallel RC network that models the output impedance at the drain. A similar process is performed to model the gate as an equivalent series RC circuit [10]. From the results shown in Fig. 2(a), there is a less than 0.5-dB variation in P_{out} when using either an optimized PAE or P_{out} match for the range of voltages. Fig. 2(b) shows that this is accompanied by a 1–5 percentage point (pp) variation in PAE. Some of the ripple in PAE is likely due to the settings of the load–pull sweep and the drain voltage extrapolation of the model.

Using the RC models of the transistor drains, the achievable bandwidth of a matching network can be estimated using the Bode–Fano criterion [11]. It can be shown that the bandwidth, ΔB, is related to the return loss of the reflection coefficient, RL(|Γ|), by

$$\Delta B \leq \frac{10}{\text{RC} \cdot \ln(10) \cdot \text{RL}(|\Gamma|)}. \tag{1}$$

Using a 20-dB return loss as the match criterion, a plot as a function of drain voltage is obtained in Fig. 2(c). As the transistor is biased at a higher voltage, the optimal reflection coefficient for P_{out} and PAE moves toward the edge of the Smith chart. This increases the Q factor of the RC network and reduces the achievable bandwidth of a matching network.

Based on this analysis, a transistor load impedance, Z_{T}, corresponding to the maximum PAE point at 20 V is chosen for the design. The corresponding PAE and P_{out} performance is shown in Fig. 2(a) and (b).

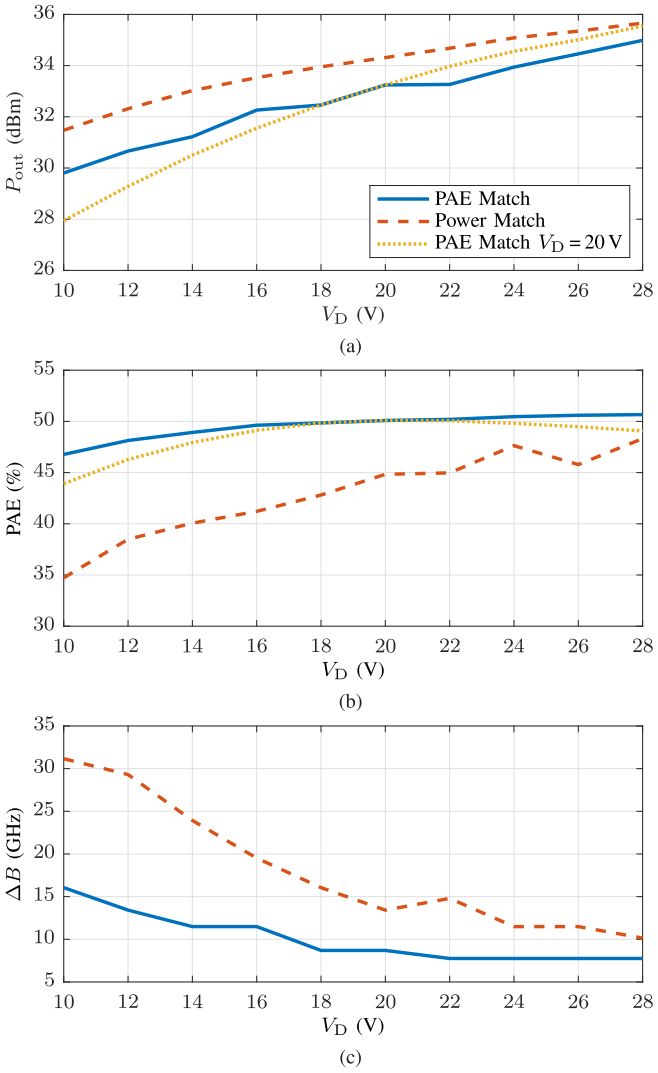


Fig. 2. Simulated (a) P_{out} and (b) PAE performance of the 8 × 100 μm transistor at 21 GHz over drain voltage. (c) Drain bandwidth assessed using the Bode–Fano criterion.

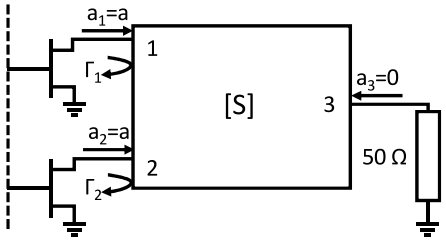


Fig. 3. Circuit diagram of three-port non-isolated power combiner with output-stage devices at ports 1 and 2 replaced by their equivalent RC network impedances.

III. Amplifier Design

A. Matching Network Synthesis

Based on the load–pull data for the transistors and the target output power of 4 W, two 8 × 100 μm transistors are selected for the final stage of the amplifier. The transistors are combined through a reactive three-port network as shown in Fig. 3. The S-parameters are defined for $Z_1 = Z_2 = Z_T$ at ports 1 and 2 and with $Z_3 = 50\ \Omega$, using complex port parameters [12]. Referring to Fig. 3, the S-parameter representation of this network is

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} a \\ a \\ 0 \end{bmatrix} \tag{2}$$

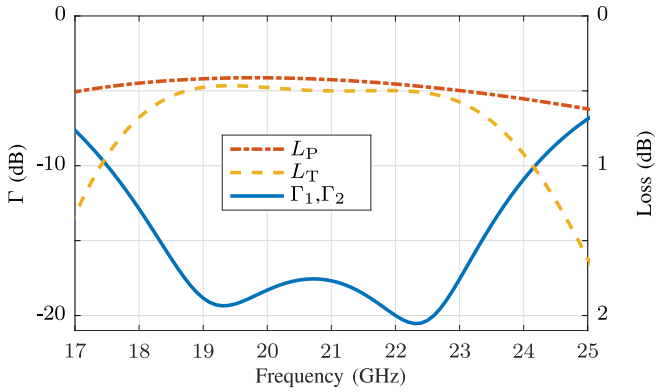


Fig. 4. Simulated power loss, transducer loss, and reflection coefficients for the power combiner network in the final stage of the PA.

and the reflection coefficient at port 1 becomes

$$\Gamma_1 = \frac{b_1}{a} = S_{11} + S_{12}. \tag{3}$$

In (3), the reflection seen at port 1 is not simply S_{11} but includes the coupling from port 2, S_{12}, therefore taking into account the non-isolated combiner effects.

A common loss definition [13] used in amplifier design is the power loss of the circuit, L_P, which removes the effects of the mismatch. This will be defined in terms of the power delivered to the load, P_{LD}, and the power delivered to the combiner, P_{CD}

$$L_P = \frac{P_{LD}}{P_{CD}}. \tag{4}$$

Using the assumptions made in (2), the power delivered to the load becomes

$$\begin{aligned} P_{LD} &= (|b_3|^2 - |a_3|^2) = |b_3|^2 \\ &= |S_{31} + S_{32}|^2 \cdot |a|^2. \end{aligned} \tag{5}$$

The power delivered to the combiner is then found to be

$$\begin{aligned} P_{CD} &= P_{CD,1} + P_{CD,2} \\ &= (|a_1|^2 - |b_1|^2) + (|a_2|^2 - |b_2|^2) \\ &= (|a_1|^2 - |S_{11} + S_{12}|^2 \cdot |a_1|^2) \\ &\quad + (|a_2|^2 - |S_{21} + S_{22}|^2 \cdot |a_2|^2) \\ &= ((1 - |S_{11} + S_{12}|^2) + (1 - |S_{21} + S_{22}|^2)) \cdot |a|^2. \end{aligned} \tag{6}$$

Combining the above, the power loss can be expressed as

$$L_P = \frac{|S_{31} + S_{32}|^2}{(1 - |S_{11} + S_{12}|^2) + (1 - |S_{21} + S_{22}|^2)}. \tag{7}$$

Simulation results for this loss metric for the output combiner (Fig. 1) is shown in Fig. 4. This metric gives a conservative estimate of loss as the match of the network degrades. For the efficiency of the final stage of an amplifier, it is important to maximize the match of the network to the optimal transistor load and a different loss metric, transducer loss L_T, which is more appropriate for the design of the output matching network. This is defined in terms of the power delivered to the load, P_{LD}, and the power available to the combiner, P_A

$$L_T = \frac{P_{LD}}{P_A}. \tag{8}$$

The power available at the input ports of the combiner is

$$P_A = (|a_1|^2 + |a_2|^2) = 2 \cdot |a|^2 \tag{9}$$

and combined with (5) and (8) results in the transducer loss

$$L_T = \frac{|S_{31} + S_{32}|^2}{2}. \tag{10}$$

This loss metric more accurately reflects the frequency response of the combiner without masking the effects of deviation from the large signal impedance match at the transistor ports or coupling between transistors.

The loss metrics along with the derived Γ for the output matching network are illustrated in Fig. 4. Since the design is symmetric ($S_{11} = S_{22}$), the two transistors see the same reflection coefficient. The same method is valid for the input network of this stage.

B. Amplifier Design and Stability Analysis

To achieve 30 dB of small-signal gain, a three-stage design is selected. The chosen staging ratio for the transistor peripheries is 1:2:8. This ensures that the current draw of the two driver stages has a minimum impact on the total efficiency of the amplifier. The first and second driver stages use 4×50 μm and 8×50 μm transistors, respectively. The transistor models are validated for 18–35-GHz operation.

Once the topology is determined, small- and large-signal models are used for a final optimization of the matching networks. Concurrent small- and large-signal optimizations were performed to ensure maximum large-signal performance while maintaining stability, gain flatness (small-signal gain >30 dB with ±1.5-dB flatness), and match ($|S_{11}|$ and $|S_{22}| < -10$ dB). It should be noted that all bypass capacitors at the gates and drains are minimized to allow supply modulation in the future while maintaining low-frequency stability. The gate bypass capacitances are 1, 2, and 2 pF, while the drain bypass capacitances are 3, 6, and 8 pF for the first, second, and third stage, respectively. The smaller capacitor values do not negatively affect RF performance.

The final layout of the circuit can be seen in Fig. 5. The 4×50 μm transistor used for the first stage has the highest Q factor gate equivalent circuit, shown in Fig. 6, requiring a higher order matching network. Two capacitors to ground create an easily tunable low-loss matching network. A small series capacitor along with a RLC and R network are used to decrease the out-of-band gain and eliminate in-band oscillations. The first interstage network uses a simple LCL matching network; the microstrip lines act as inductors, combined with a RC stability circuit to suppress low-frequency gain. The second interstage match follows the same topology as the first but a RLC stability network is used. This network suppresses higher and lower frequency gain while allowing the in-band gain to be shaped by appropriate choice of the resonant frequency. The output matching network makes use of low-impedance lines to minimize loss. Bias circuits are absorbed into the matching networks, and all gate bias lines have resistors that dampen any resonances. Both input and output matching networks account for 10-mil alumina

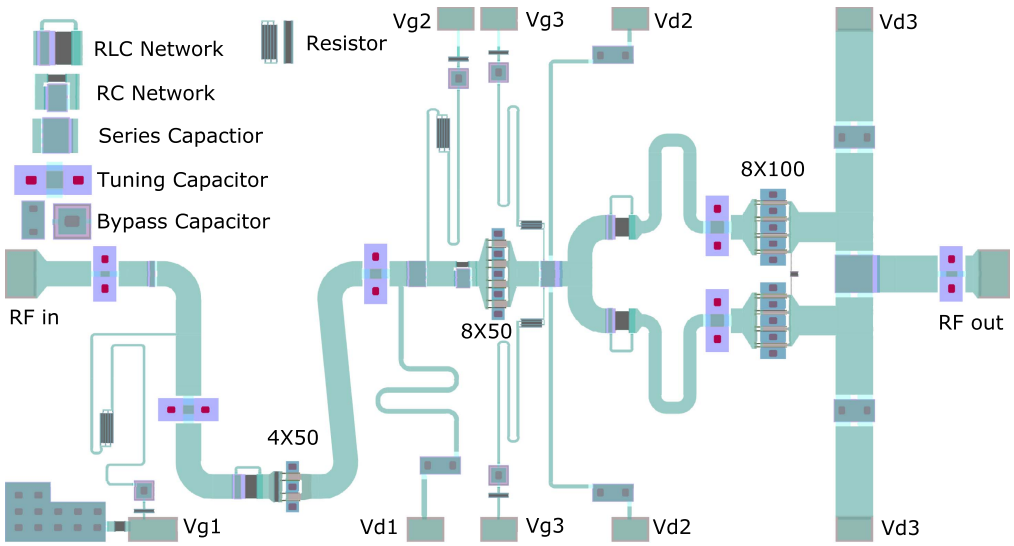


Fig. 5. Final MMIC layout in a 4 mm × 2 mm footprint. A legend for sub-circuits discussed in the text of the paper is included in the top left. The drain bias lines of the second and third stage and the gate bias lines of the second stage are designed with vertical symmetry to ensure equal impedances are presented to the output-stage devices.

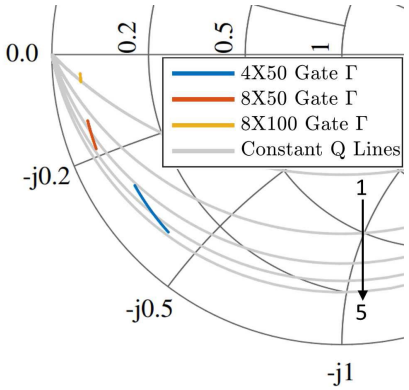


Fig. 6. Impedances of the transistor gates modeled as series RC circuits from 16 to 25 GHz, with constant Q-factor arcs shown for Q = 1–5. Smaller transistors are modeled by higher Q resonators, making broadband matching more difficult.

to 100-μm SiC bondwire transition modeled in a full-wave electromagnetic simulator (HFSS).

K factor is not sufficient for stability analysis of multi-stage power-combining amplifiers [14]; therefore, a Nyquist loop-gain analysis is performed [15] under large- and small-signal operation at various bias points. Odd mode stability is evaluated for the final stage and a resistor is added [16].

IV. Probed Amplifier Performance

A. Small-Signal Performance

The amplifier was fabricated as part of a shared wafer run, and 230 chips were made on five wafers, $W = \{1, 2, 3, 4, 5\}$ in seven positions along the axis normal to the gate fingers, $Y = \{10, 15, 20, 25, 30, 35, 40\}$, and nine positions parallel to the gate fingers, $X = \{5, 7, 9, 11, 13, 15, 17, 19, 21\}$. Pulsed large- and small-signal measurements were performed on the chips at nine frequency points, $f = \{19.5, 20, 20.5, 21, 21.5, 22, 22.5, 23, 23.5\}$ GHz. Large signal on-wafer pulsing was performed with a 100-μs pulse using a 10% duty cycle at three drive levels $P_{\text{in}} = \{8, 10, 12\}$ dBm.

The probed data performance is expected to differ from the mounted amplifier performance, as the amplifier was designed to have a transition to alumina on the input and output, but can still be used to see trends in the performance of the amplifier across the wafer and X/Y position.

Probed small-signal performance of the amplifier chips is shown in Fig. 7. A small percentage of chips, deemed outliers, are excluded from these plots in order to improve readability but are included in the final analysis of performance. Boxplots are used to show the quartiles and means of the data set because they make no assumptions about the distribution of the amplifiers dependent variable.

Return loss, $|S_{11}|$, varies from -7 to -20 dB across the frequency band. The lower frequency performance ($\leq$21 GHz) shows a greater variation than the higher frequency data. The $|S_{22}|$ similarly varies from -4 to -22 dB across the frequency band. The mid band of the performance (20–22.5 GHz) shows the best match with a $|S_{22}| \leq -10$ dB. $|S_{21}|$ shows an approximately 4-dB variation at each frequency point. The mean gain varies from 39 dB at the lowest frequency to 32 dB at the highest frequency. The higher than expected gain variation across the band is likely due to the lack of bondwire interconnect and is not observed for mounted chip measurements. It should be noted that, based on the frequency dependence of the gain, we expect that measurements would show high-gain performance below 19.5 GHz. Note also that the transmission phase response, Fig. 7(d), varies linearly over frequency, as expected.

B. Large-Signal Performance

Large-signal performance at $P_{\text{in}} = 12$ dBm is shown in Fig. 8. Data from 28 of the 230 measured chips are considered outliers and removed for readability. Average PAE stays around 40% excluding the 23.5-GHz point. The mean of P_{out} varies in the range of 37 dBm $\pm$ 0.5 dB excluding the 23.5-GHz point which drops down to below 36 dBm.

A statistical analysis is performed in which the PAE data at a 12-dBm drive level is the dependent variable. The analysis

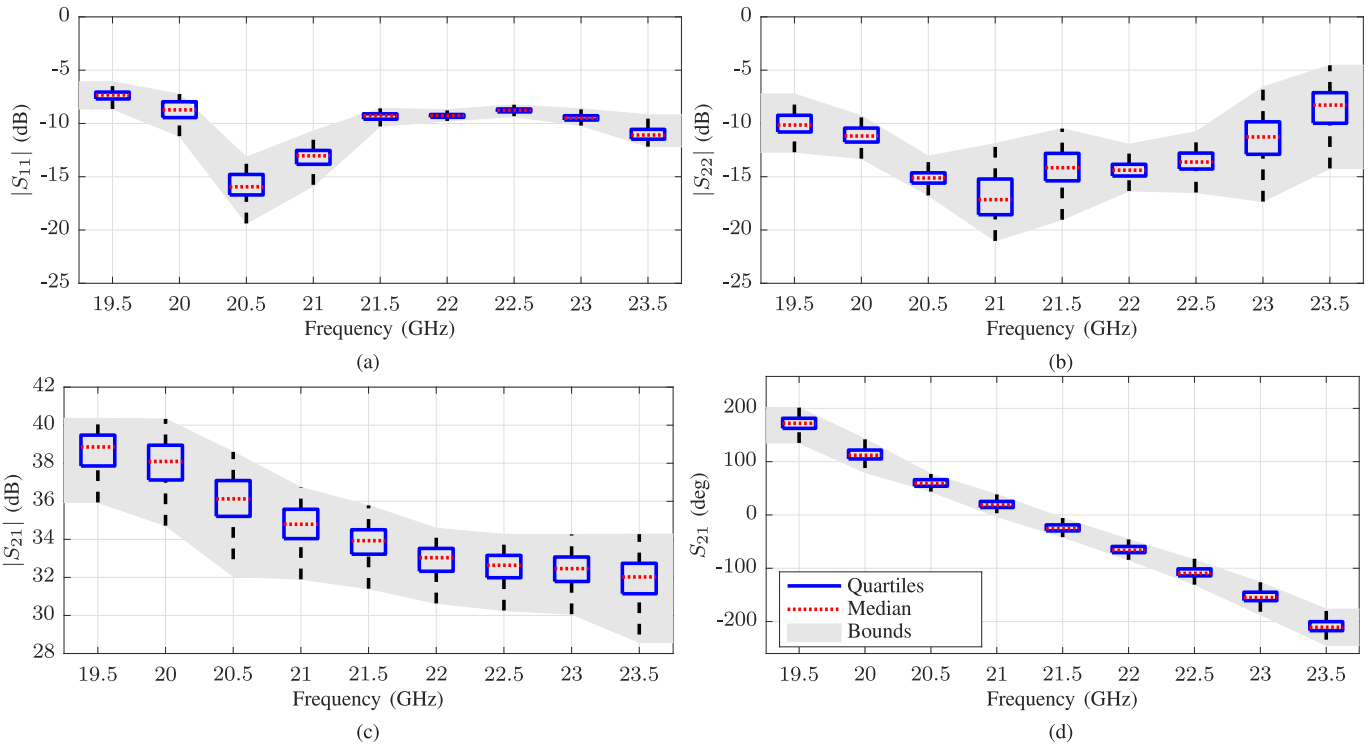


Fig. 7. Small-signal (a) $|S_{11}|$, (b) $|S_{22}|$, (c) $|S_{21}|$, and (d) $\angle S_{21}$ measured across five wafers. The graph shows the performance of 202 of 230 measured chips. Two hundred and thirty chips were probed of which 28 of the chips performed as outliers and are not shown. An outlier is defined as performing below $Q_1 - 1.5 \times$ IQR or above $Q_3 + 1.5 \times$ IQR, where IQR is the interquartile range and Q_1 and Q_3 are the lower and upper quartiles, respectively. The boxes include 50% of the measured chips, and the range shows the performance of all 202 die.

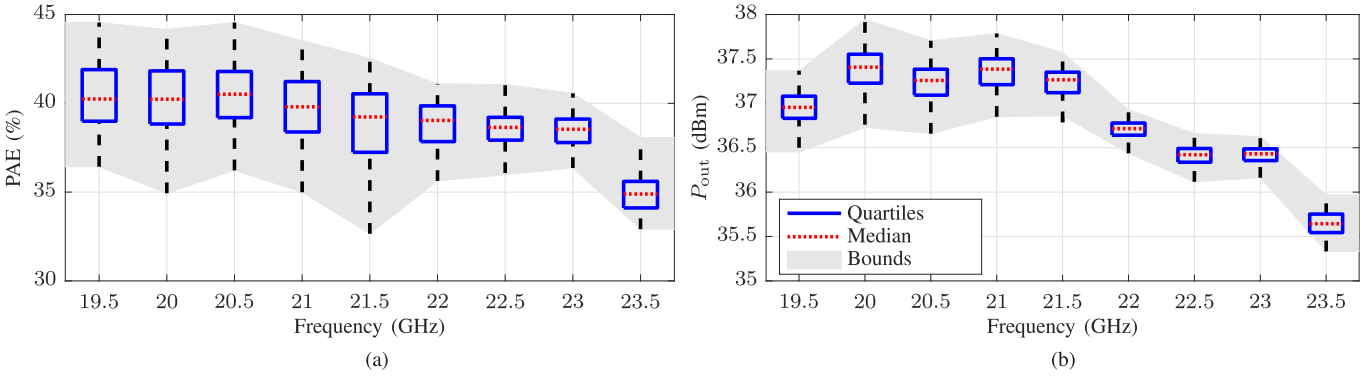


Fig. 8. Measured (a) PAE and (b) output power for wafer-probed amplifier die at 11-dBm input drive. The graph shows the performance of 202 of 230 measured chips. Two hundred and thirty chips were probed of which 28 of the chips performed as outliers and are not shown. An outlier is defined as performing below $Q_1 - 1.5 \times$ IQR or above $Q_3 + 1.5 \times$ IQR, where IQR is the interquartile range and Q_1 and Q_3 are the lower and upper quartiles, respectively. The boxes include 50% of the measured chips, and the range shows the performance of all 202 die.

aims to see how W, X, Y, and f affect the efficiency of the chips. From this, we can derive the main manufacturing factors that affect the variation in the amplifiers performance. All statistical analysis is performed using SPSS [17]. An analysis of variance (ANOVA), which allows multiple group means to be compared for statistical significance, is performed. Outlying chips were not manually remeasured, so any error in the probing cannot be thoroughly ruled out while examining the performance of the chips.

A four-way ANOVA analysis is performed on the main effects and all possible two-way interactions of W, X, Y, and f. The analysis results are shown in Table II with an additional column added for the "importance", ω_i^2, of each parameter calculated as

$$\omega_i^2 = \frac{SS_i + (df_i)MS_{\text{residual}}}{SS_{\text{total}} + MS_i} \tag{11}$$

where SS is the sum of squares, MS is the mean square, df is the degrees of freedom, and i is the grouping of variables. A type-III SS is used due to unequal variances between the groups [18]. The results for f are not shown due to a lack of statistical significance.

The ANOVA is able to explain 81.8% of the variation in the means. The dominant causes of the variation are related to the wafer-to-wafer performance and the Y position on the wafer which account for 68.5% of the variations in means. Boxplots

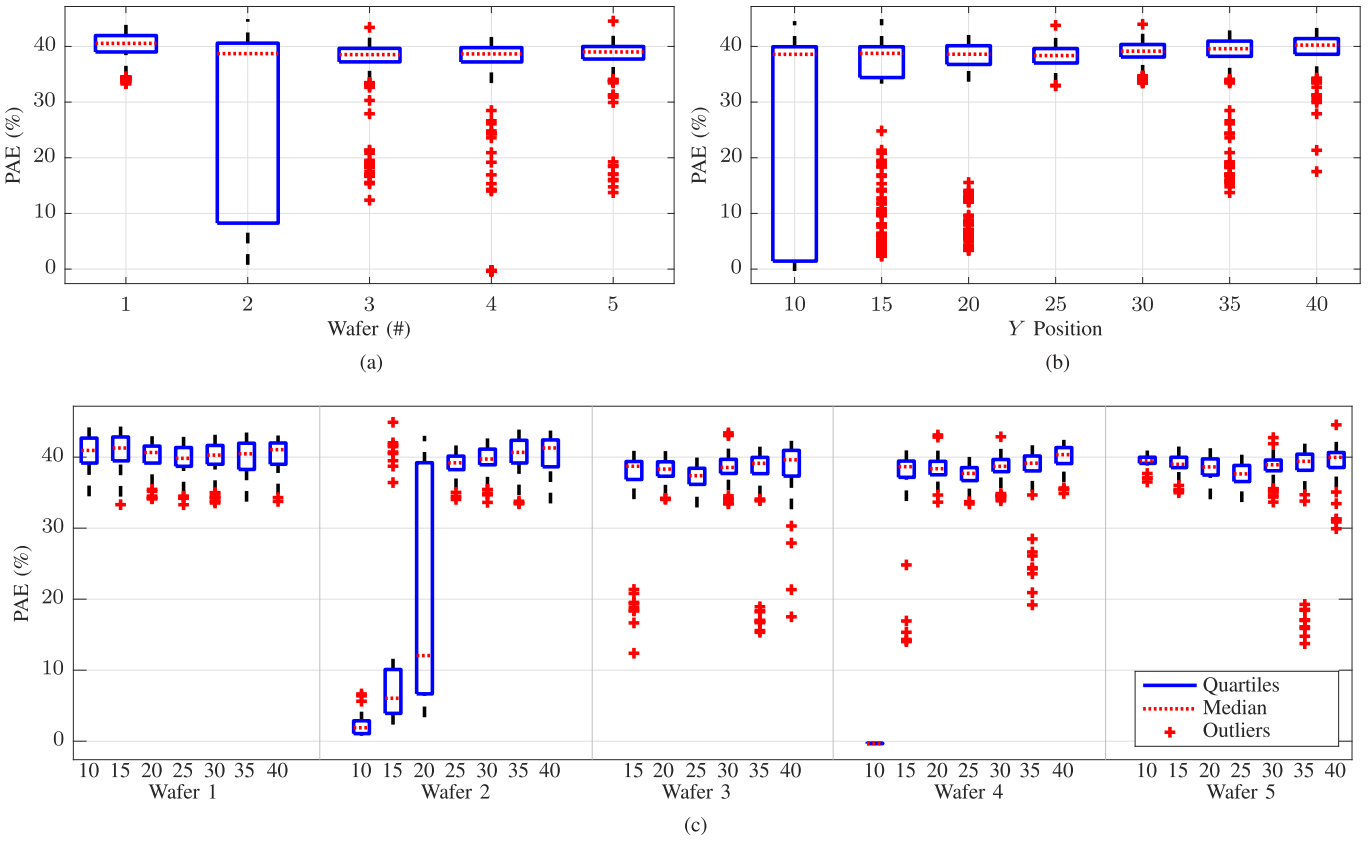


Fig. 9. PAE statistics as a function of (a) wafer number W, (b) position Y, and (c) number versus position W:Y for 230 probed die.

TABLE II
ANOVA OF MEANS

Source	df	SS	MS	ω^2 (%)
X	8	3202.7	400.3	1.7
Y	6	35942.3	5990.4	18.3
W	4	27089.3	6772.3	13.8
X:Y	33	11312.6	342.8	6
X:W	32	10659.1	333.1	5.6
Y:W	23	71246.3	3097.7	36.4
Error	1811	24953.4	12.7	
Total	2069	196511.4		81.8

analyzing these variations are shown in Fig. 9. It can be seen that wafer $W = 2$ has the worst performance while the $Y = 10$ position performs the worst of the Y positions.

A Games–Howell test [19] is used for the *post-hoc* analysis of the ANOVA results. The results of this analysis are discussed for the three independent variables, W, X, and Y, without interactions and the following conclusions can be made.

1) PAE performance is the lowest for $W = 2$, with the mean performance being 8 pp lower than for $W = 4$, the second lower performing wafer.
2) Amplifiers with higher Y values perform better with a 17 pp variation from $Y = 10$ to $Y = 40$.
3) There is no clear performance trend in the X values, but PAE varies by over 5 pp depending on X (from 34% to 39%).

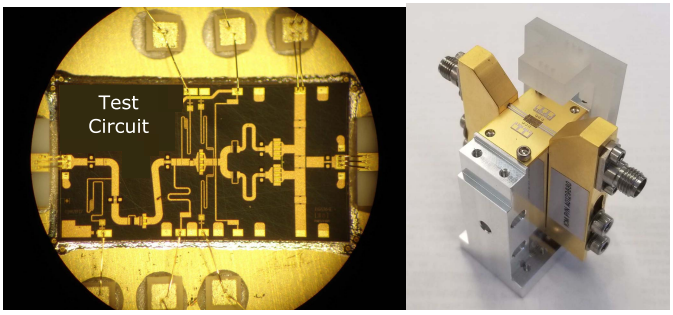
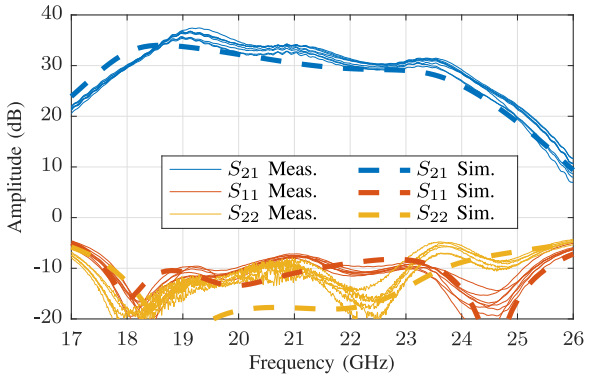


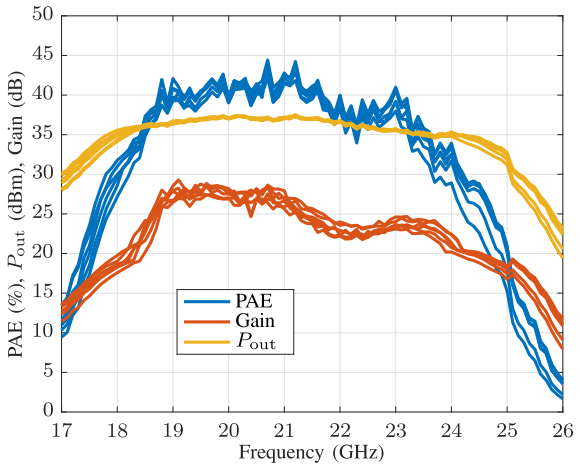
Fig. 10. (a) Photograph of the three-stage K-band MMIC mounted on a CuMo carrier and bonded to 10-mil alumina microstrip lines at input and output. Bypass capacitors of 100 pf are bonded to the six bias pads. Three bondwires connect the amplifier RF bond pads to the alumina input and output lines. A single bondwire is used for all dc bias lines excluding the final stage where dc current draw is the highest. (b) Photograph of an MMIC in a fixture. The CuMo carrier is attached to an aluminum heat sink. The 3-D printed plastic mount and spring-loaded pins supply dc bias to the amplifier. 100-pf off-chip bypass capacitors are bonded to the six bias pads.

V. PACKAGED IC PERFORMANCE

Ten MMICs are evaluated in the fixture shown in Fig. 10(b). The MMIC is mounted on a CuMo carrier and wire bonded to 50-Ω microstrip lines on 10-mil thick alumina. The carrier is attached to a custom aluminum fixture and connected to 2.9-mm coaxial connectors via a microstrip-to-coaxial transition. Spring loaded pins are used to connect the bias voltages to pads on the chip through 100-pF off-chip bypass capacitors mounted on the CuMo carrier, seen in Fig. 10(a).



(a)



(b)

Fig. 11. (a) Simulated (dashed) and measured (solid) small-signal S-parameters and (b) measured large signal performance for eight mounted chips from 17 to 26 GHz.

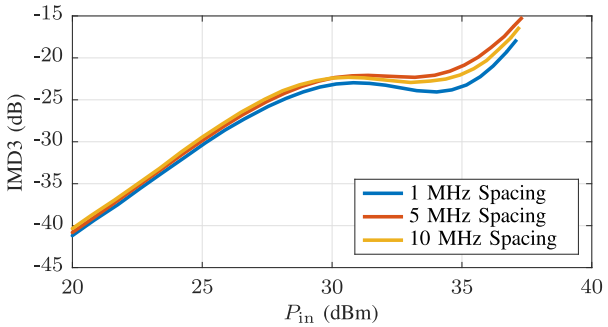


Fig. 12. Measured third-order intermodulation product relative to the carrier power of one of the MMIC amplifiers at 20 GHz for three tone spacings: 1, 5, and 10 MHz.

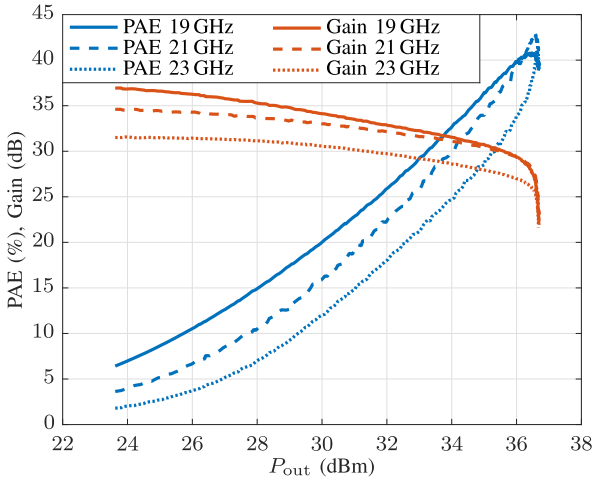


Fig. 13. Measured large signal amplifier gain and efficiency saturation curves for three frequencies within the band of interest.

Off-chip bypass capacitors are present for testing but are not necessary for amplifier stability.

Testing is done with a 20-V drain bias at 100-mA/mm quiescent current. A small signal gain of 33 dB with a ±3-dB gain variation from 18 to 24 GHz is shown in Fig. 11(a). The input return loss is better than 10 dB from 17.5 to 25 GHz, with good agreement between simulated and measured results for the mounted packaged amplifier.

The large-signal performance over frequency for the chips is shown in Fig. 11(b). The measurements show a large-signal gain of 25 dB with a variation of ±2.5 dB from 18.5 to 23.5 GHz. Large-signal performance drops off at 18.5 GHz on the low end and 23.5 GHz on the high end with >35% PAE for that band. Saturated output power for this band peaks above 36 dBm. This GaN process has been shown to have minimal power droop under high-power operation [20].

The third-order inter-modulation distortion (IMD3) relative to the power at the 20-GHz carrier frequency can be seen in Fig. 12 for three tone spacings. The C/I ratio degrades as a function of tone spacing peaking just over −20 dB when the amplifier is saturated. In Fig. 13, gain and PAE curves are shown for three discrete frequencies across the band. The PA saturates at the same output power point at the three frequencies and is compressed by 3–5 dB at the point of maximum PAE.

VI. Conclusion and Discussion

The performance and design methodology of a three-stage K-band MMIC are presented. The operational bandwidth of the amplifier extends from 18.5 to 24 GHz, a greater than 25% fractional bandwidth. The MMIC shows greater than 4-W peak output, a peak efficiency exceeding 40%, and a saturated gain greater than 22 dB. The MMIC PA is designed with consideration to the supply-voltage dependence of the PAE, P_{out}, and bandwidth for intended supply modulation to further increase the efficiency.

Fig. 14 shows the measured large-signal gain, output power, and efficiency as the supply voltages of all three stages are varied simultaneously. These measurements indicate that the PA is a good candidate for supply modulation with potentially high bandwidth since it is designed to be stable with minimal capacitance in the drain circuit. In addition, the gain does not vary substantially over a wide range of supply voltages, implying that relatively simple linearization can be used under dynamic supply operation.

The analysis shown in Fig. 2 at 21 GHz predicts the PAE response over drain voltage measured in Fig. 14(c). The 19–23 GHz range shows an area of optimal supply modulation performance, where peak PAE will be higher (or equal) for lower drain voltages. As the frequency changes to values greater than 23 GHz, the PAE for lower voltages degrades. Similarly, below 19 GHz, supply modulation would not be

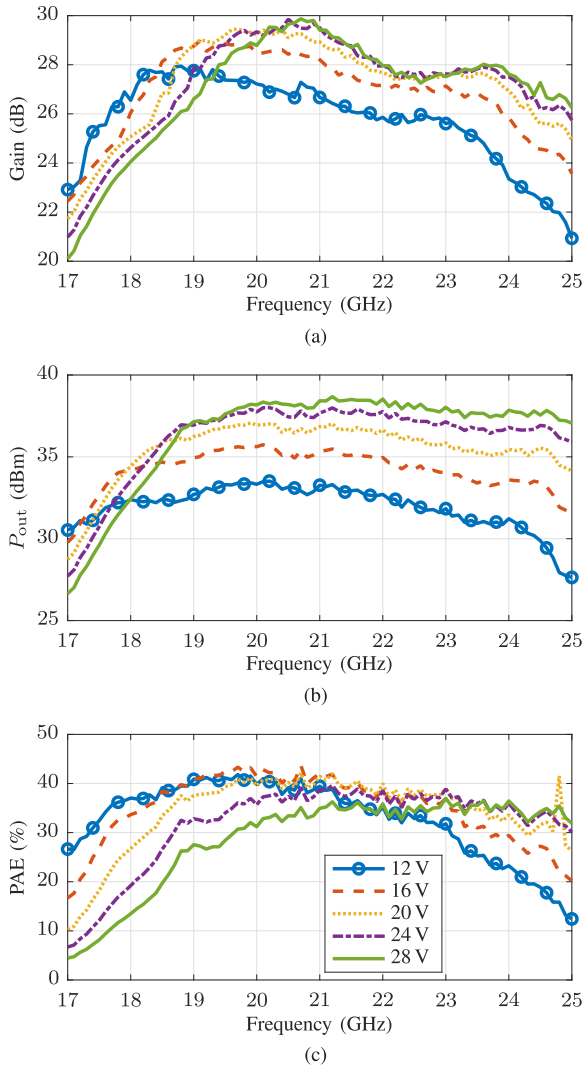


Fig. 14. (a) Measured gain, (b) output power, and (c) PAE for a MMIC mounted in a fixture over 12–28-V variation of supply voltage for all three stages simultaneously, shown at peak efficiency.

practical due to the drop-off in P_{out} for higher drain voltages, which can be seen by the overlapping lines in Fig. 14(b). The bandwidth where supply modulation is practical lines up well with the areas of peak PAE seen in Fig. 11(b).

In summary, this paper presents the design flow, starting with transistor sizing and network design and includes matching network synthesis for a non-isolated reactive combiner, as well as stabilization. Measured PA performance over five wafers is statistically analyzed for both small- and large-signal data on 230 on-wafer probed MMICs. Large-signal measurements are performed on 10 fixture-mounted die, including PAE, P_{out}, and saturated gain over frequency and power, and two-tone linearity is characterized.

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