Dual Gate and Drain Supply Modulation of an X-Band PA

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***Abstract*— This paper addresses an analog method for mitigating the nonlinearities introduced by discrete supply modulation of a high-efficiency power amplifier. A 10-W two-stage X-band GaN MMIC PA, with a peak power-added efficiency (PAE) of 55%, is tested with drain supply modulation from 10 to 20 V. Drain supply modulation increases the efficiency, but substantially degrades the amplifier linearity. In this work, we demonstrate that gate modulation can improve back-off gain and linearity, specifically when gate biases of the two stages of a PA are independently modulated. Simultaneous gate and drain modulation results in 15 percentage point improvement in efficiency over a static supply, and a 10 dB improvement in noise power ratio (NPR) over drain supply modulation only, for a 10 MHz noise-like signal.**

***Keywords*— Power amplifiers, efficiency, GaN, broadband.**

I. Introduction

Modern satellite communication systems require broadband transmitters capable of simultaneous linear and efficient operation. Drain supply modulation has been shown as an effective method for improving efficiency, but efficient continuous supply modulators are faced with bandwidth limitations, as discussed e.g. in [1], [2]. Discrete supply modulators can be used for reduced slew-rate modulation, and show promise for efficiency improvement when broadband signals are amplified, but the discontinuous supply voltage of the tracker introduces distortion [3], [4]. Gate modulation was shown to improve the linearity of amplifiers under static drain bias conditions in [5], [6], while simultaneous gate and drain modulation was applied to improve supply modulator efficiency in [7].

In this work, a method to improve linearity and gain of a drain supply-modulated PA is shown. A two-stage GaN X-band PA [8] is tested at 9.7 GHz under drain supply modulation, with the two drain voltages varied together. Simultaneously, the gate biases of the transistors in the two stages are varied independently, as shown in Fig. 1. An efficient discrete supply modulator [9] is used to generate the drain supply voltage, while two high-speed instrumentation amplifiers are used to drive the gates of the amplifier. Performing gate and drain bias modulation provides the efficiency improvement of drain supply modulation with improved linearity performance. This method can be implemented entirely in the analog domain, without the knowledge of digital baseband signals, useful for, e.g. repeaters.

II. Constant Quiescent Current Mode

To maintain efficiency, the drain voltage, V_{D}, of the amplifier can be reduced for lower input RF voltages, V_{RF},

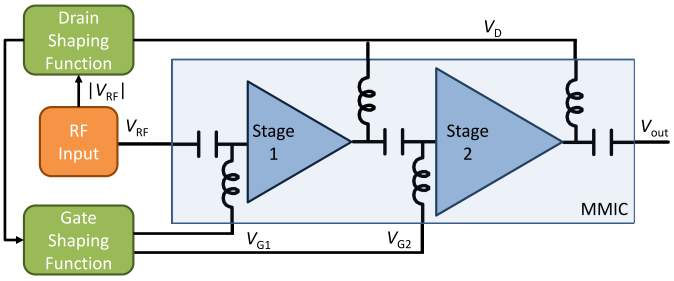


Fig. 1. Block diagram of a transmitter in which a two-stage PA is supply-modulated with a single dynamic drain voltage V_D and two independently-controled gate bias voltages, V_{G1} and V_{G2}.

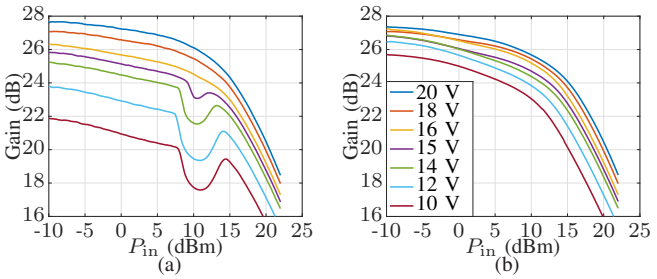


Fig. 2. Measured gain at 9.7 GHz of the two-stage MMIC PA as a function of input power P_{in} for (a) constant and different V_{G1} and V_{G2} and (b) constant quiescent current, when the single drain supply V_D is varied from 10 to 20 V.

and increased for higher V_{RF} levels. The quiescent current of an ideal amplifier would remain the same over a range of V_{D}, provided the transistors are biased in saturation. In a practical amplifier, the quiescent current can vary greatly over V_{D}. In drain supply-modulated amplifiers, this effect can lead to an increase in gain variation and a resulting degradation of linearity. Fig. 2 shows measured results for the amplifier tested in this work for constant gate voltages, V_{G1} and V_{G2}, and a constant quiescent current, while varying statically the common drain voltage.

For the constant V_{G} case of Fig. 2a, the measured gain varies over 6 dB from 10-20 V. Additionally, there are gain dips around P_{in}=10 dBm that are indicative of parametric oscillations, which practically limit the amplifier drain modulation range to 16-20 V for linearity. Efficiency measurements show that this limitation in supply voltage range results in a >10 percentage point (pp) impact on efficiency relative to the full range. If the quiescent current of the amplifier is held constant over drain bias by adjusting the gate bias accordingly, seen in Fig. 2b, the gain variation are reduced to <2 dB and

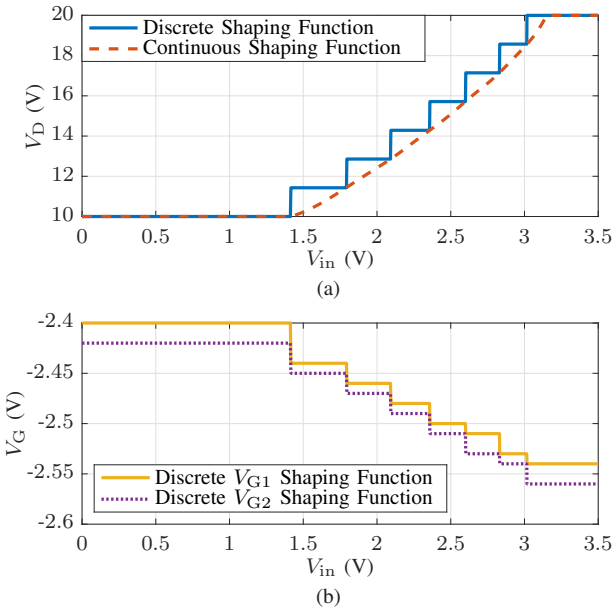


Fig. 3. (a) Drain shaping function maps the input envelope to the dynamic drain supply voltage, and (b) gate shaping functions for the two stages. V_{in} is calculated from the input power assuming a 50-Ω impedance.

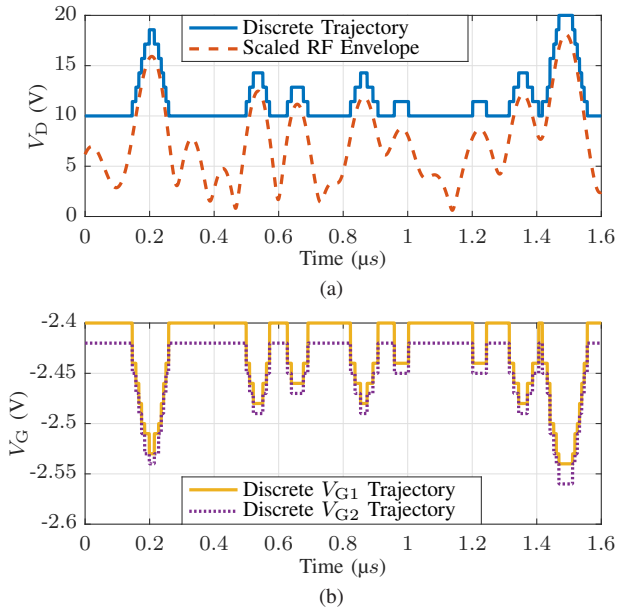


Fig. 4. Time domain voltage waveforms for a 10 MHz noise-like signal at P_{in}=14 dBm, for (a) the drain voltage and continuous envelope (b) gates 1 and 2.

the parametric oscillations are eliminated.

A static amplifier characterization was performed to define the dependence of drain voltage on input voltage. This drain shaping function is seen in Fig. 3a and is designed to maintain a flat gain over drive power. The shaping function is discretized assuming 8 discrete voltage levels are available [10]. To compensate for the drain current variation due to the discrete nature of the drain voltage, the gate shaping functions are also discontinuous and shown in Fig. 3b. They are designed from static measurements by selecting gate voltages that keep the quiescent current constant. Because the gates of the transistors draw virtually no current, this can be done without reducing efficiency.

The application of the shaping functions from Fig. 3 to a 10 MHz noise-like signal in the time domain can be seen in Fig. 4. As the supply voltage reduces on the drain, the gate supply provides a more positive voltage, compensating for the quiescent current drop seen for a static supply. The two gate voltages vary synchronously, but to different values due to the different bias voltages needed to maintain a constant quiescent current for the two stages.

III. Measurement Method and Results

The PA with dynamic drain and gate biasing is characterized with a test setup illustrated in Fig. 5. A low phase noise synthesizer is used to generate a 2.5 GHz clock signal fed into a bit pattern generator (BPG) which in turn provides the control signals for the switches on the 8-level tracker. The BPG also outputs auxiliary clock signals which are fed to two N8241A arbitrary waveform generators (AWGs) along with a trigger. The AWGs operate in slave mode of the BPG, allowing signal alignment within 800 ps. One AWG feeds differential

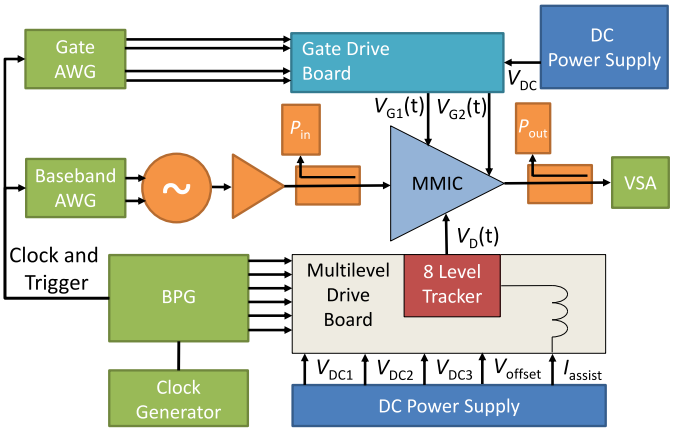


Fig. 5. Block diagram of test setup. Gates 1 and 2 are varied independently of one another. The dynamic drain voltage is provided by a 8-level tracker controlled by a bit pattern generator (BPG) that commutates three external voltages, $V_{DC1}, V_{DC2}, V_{DC3}$, while the dynamic gate signals are provided synchronously by the AWG.

outputs into a gate drive board, while the other feeds a vector signal generator (VSG). A vector signal analyzer (VSA) is used to receive the signal and provides the 10 MHz reference used throughout the setup. Power measurements are done using average USB power sensors that are calibrated up to the plane of reference of the DUT on both the input and output.

A custom 8-level tracker is used to provide the dynamic drain supply, and is based on three stacked half bridges which allow 2^3 combinations of the supply voltages (V_{DC1},V_{DC2},V_{DC3}) [4]. An offset voltage (V_{offset}) is used so that even when all the supplies are off the voltage is still set to 10 V [11]. Additionally, a current assist (I_{assist}) circuit is used that injects dc current at the output of the 8-level tracker.

This circuit reduces the current flowing through the tracker circuit, thereby reducing power-stage losses. The tracker is connected to the two drains through spring loaded pins. The switching speed is limited to 150 MHz by digital isolators in the drive circuit.

The gate drive circuit is based on the THS3202 dual current feedback op-amp. Two of these are connected in an instrumentation amplifier configuration [12]. The board takes the differential output of the AWG and converts it to a single ended signal and shifts the level to a required negative offset. A 5 Ω series resistor is connected in the output path of the output op-amp which then connects to the DUT through spring loaded pins.

The RF path is aligned with the gate and drain path in a two-step process. First, a CW carrier that is modulated for a fixed fraction of a periodically-repeated input signal is applied to the amplifier. During the unmodulated part of the signal transmission period, the drain supply of the amplifier is modulated with another signal; this modulation appears in the RF output of the amplifier as amplitude modulation. The time shifts of these two modulated signals are then found in post processing and the offset delay is determined. Second, the same RF signal is transmitted through the amplifier with a static drain bias while the two gate biases of the amplifier are modulated during the CW transmission period. The RF output is again used to time align the V_{G1} and V_{G2} signal paths with respect to the RF path and relative to each other, as they can have different time delays. The amplitude modulation appearing on the RF output from the gate modulation is also used to generate an equalization function for the AWG gate signals, in order to compensate for the linear effects of the op-amps, interconnects, and gate bypass capacitors.

The amplifier is tested for linearity using noise power ratio (NPR). The test signal is generated by creating 30,000 carriers

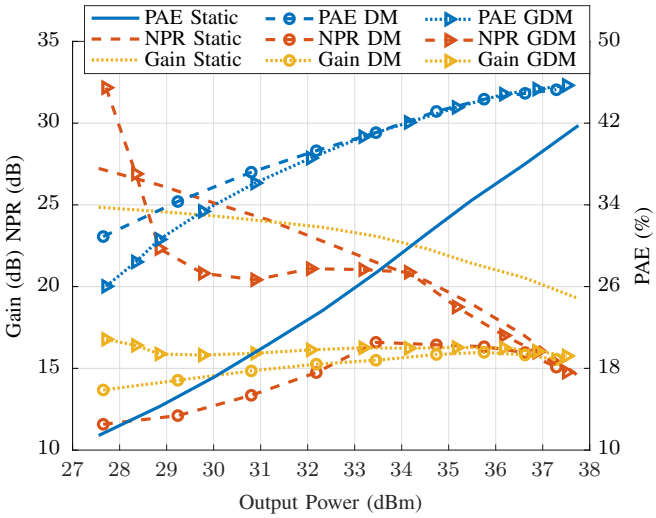
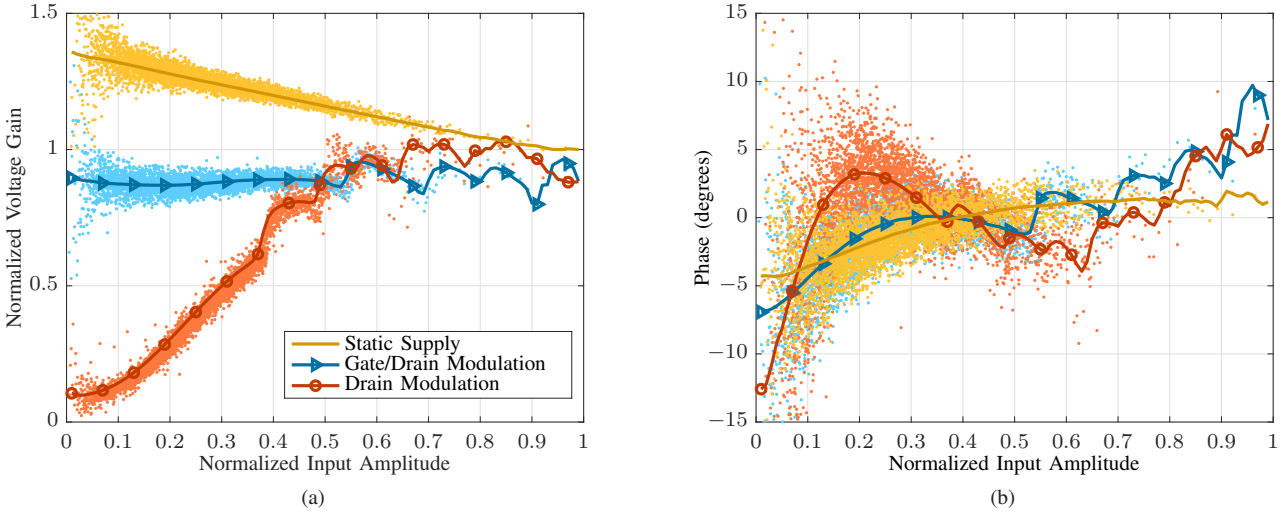


Fig. 6. Measured results for the transmitter under static bias, with drain modulation (DM), and with both gate and drain modulation (GDM). PAE values include power stage losses of the supply modulator.

in the frequency domain and ascribing them a random, uniformly distributed phase from 0 to 2π. At the center frequency of the signal 1 % of the carriers are removed. In the time domain, this signal generation results in in-phase/quadrature signals with uncorrelated Gaussian amplitude distributions and a composite signal with a Rayleigh distributed amplitude. The PAPR of the signal is greater than 10 dB [13]. The amplified signal is captured in the frequency and time domains. For time domain data, the signal is received by the VSA, upsampled from the received sampling rate to the generation sampling rate, and then time and phase aligned to the original signal.

Fig. 6 shows results for a power sweep for three cases: static supply, drain modulation (DM), and gate and drain modulation (GDM). While GM and GDM show similar PAE



(a) (b)

Fig. 7. Measured results at 9.7 GHz and 28 dBm output power showing (a) AM/AM and (b) AM/PM for a 10-MHz NPR signal with a PAPR=10 dB. Blue shows performance for just a static supply, red shows gate and drain modulation, and green shows drain modulation. The discrete points are faded and a darker trend line is superimposed for clarity.

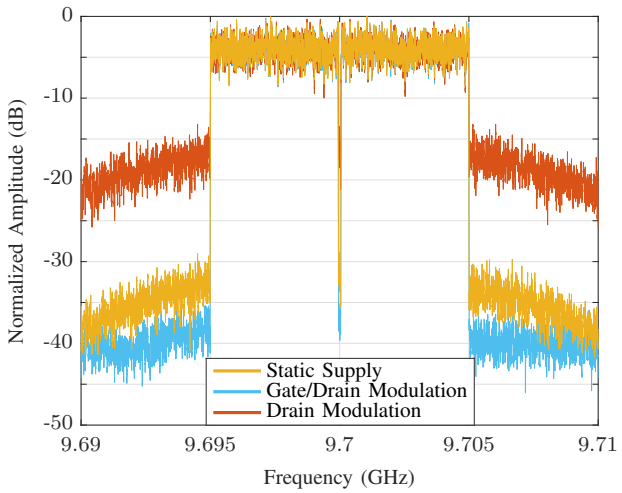


Fig. 8. Measured spectrum of a 10 MHz noise-like signal at 28 dBm output power for static supply (yellow), gate and drain modulation (blue) and drain modulation (red).

improvements over the static supply case, the NPR penalty is very different. The GDM consistently outperforms DM in NPR by over 20 dB at P_{out}=28 dBm and over 10 dB up to P_{out}=34 dBm. For output powers exceeding 34 dBm, GDM is equal to or outperforms the static supply in terms of NPR, while improving PAE between 5 pp and 12 pp. Using GDM reduces efficiency in back-off by <5 pp compared to DM, as a higher gate voltage will increase current draw at lower power levels, however the efficiency degradation disappears at higher drive levels.

AM/AM and AM/PM data for the three cases of the static supply, DM, and GDM can be seen in Fig. 7. The steep drop in gain at lower drive levels is a known phenomenon in GaN [14], and it is seen that GDM prevents this gain decrease which is pronounced with DM. Additionally, there is a tighter spread on the AM/PM at lower input amplitudes for the GDM case compared to DM. Compared to the static supply case, the GDM AM/AM is more linear. Measured spectra for the static supply, DM, and GDM cases are given in Fig. 8. At P_{out}=28 dBm GDM provides the best linearity, even exceeding that of the static supply case, with a substantial, 20 dB, improvement over DM alone.

IV. Conclusion

A two-stage X-band GaN MMIC amplifier is characterized under both drain and gate modulation, with demonstrated improvement in efficiency and linearity. While drain modulation improves efficiency, as expected for supply modulated PAs, the linearity characterized by NPR is degraded. If an NPR >16dB is desired, the distortion for drain modulation only renders the PA practically useless, since backing-off the power degrades performance further. Adding gate modulation improves the NPR to levels of over 20 dB for output power levels up to 34 dB with a marginal PAE penalty. This is enabled by modulating the gate biases of the driver and output stage of the PA independently. In this case, the PAE is improved by 15 percentage points from 18 to 33% at P_{out}=30 dBm and by 5 percentage points as peak power is approached, while maintaining linearity.

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