# Two-Stage High-Efficiency X-Band GaN MMIC PA / Rectifier

Mike Coffey, Scott Schafer, Zoya Popović
Electrical Computer and Energy Engineering
University of Colorado at Boulder
Boulder, Colorado 80309
Email: zoya@colorado.edu

***Abstract*—This paper details the performance of an X-Band MMIC fabricated in a 0.15 µm GaN on SiC process that operates as both a high-efficiency power amplifier (PA) and a high-efficiency rectifier. The MMIC characterized as a PA biased in class AB, achieves over 10 W of output power, >20 dB of gain and a PAE of 50% at 9.9 GHz. As a rectifier, the MMIC, achieves over 52% RF-DC conversion efficiency at a power level of >8 W. To the best of the authors' knowledge, this is the first demonstration of a two-stage power combined high-efficiency GaN X-band MMIC power rectifier. The applications are in bi-directional high power wireless energy transfer.**

***Index Terms*—high-efficiency power amplifiers (PAs), load-pull, microwave rectifiers, MMIC**

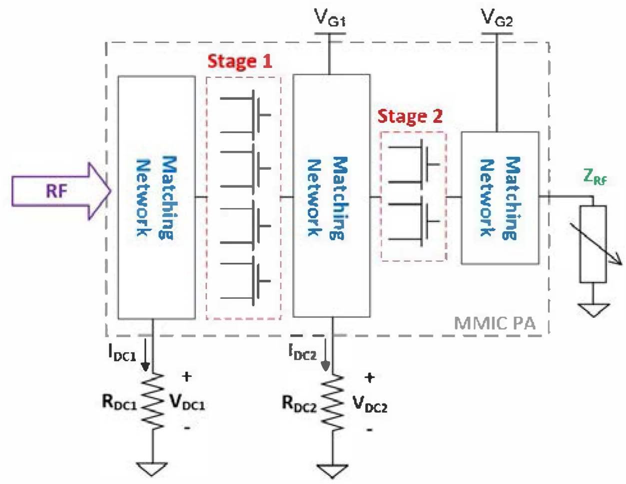
## I. Introduction

RF rectifiers operating in the microwave region have applications in wireless powering, energy recycling and as key parts of wireless sensor networks [1], [2]. The use of diodes for RF and microwave rectification has an established well documented history [3], [4], [5]. Multi-watt level wireless power transmission and rectification has been demonstrated with solid state power amplifiers and diodes fabricated in wide-bandgap semiconductors [6] and silicon by means of power division at the rectifier/rectenna [7]. More recently, it was shown theoretically in [8] with the time reversal duality principle that high efficiency power amplifiers can operate as RF rectifiers. Time reversal duality, [9], was demonstrated experimentally in [10] and [11]. High efficiency self synchronous rectifiers are obtained by applying RF power to the drain and terminating the gate in a optimal load. In [10] and [11] class C and $F^{-1}$ single stage PAs were demonstrated to rectify watt-level powers in the 2 GHz range with over 80% conversion efficiency. The approach was extended to an X-band single stage GaN MMIC with 60% conversion efficiency in [12].

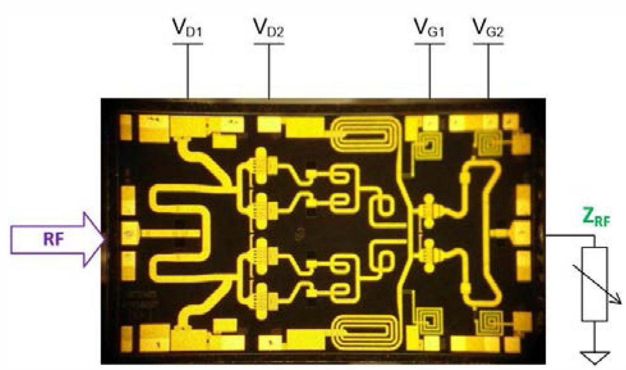
In this work we investigate the performance of a two stage class AB power amplifier as a rectifier, shown in Fig 1a. The PA utilizes two 8x50 µm devices for the driver stage and four power-combined 10x90 µm devices for the output stage. Since the amplifier RF output becomes the RF input of the rectifier, the output stage is referred to as Stage 1 and the driver stage as Stage 2. DC loads are connected at the drain bias lines of each stage and an RF load terminates the PA input on the gate of the driver stage.

## II. PA and Rectifier Measurements

The MMIC is characterized as an amplifier and operates from right to left in the orientation of Fig. 1. The measured PA output power, gain and PAE are shown in Fig. 2. Peak power and efficiency is achieved at an input power of 20 dBm with a resulting output power of 40 dBm, and a PAE of 50% representing state of the art results in X-band. Following the time reversal duality, a RF rectifier using this amplifier should be able to rectify 10 W of RF power with an approximate 50% conversion efficiency, close to the peak PAE.




(a)




(b)

Fig. 1: (a) Block diagram of the MMIC PA configured for operation as a rectifier. DC generated from rectification is collected at the drain of each stage. (b) Photograph of two stage MMIC PA used for rectification. From left to right, four 10x90 µm transistors with two 8x50 µm.

For the RF rectifier measurements, a test bench similar to Fig. 1a is setup to perform RF measurements, with $Z_{RF}$ implemented with a Focus impedance tuner. When utilizing

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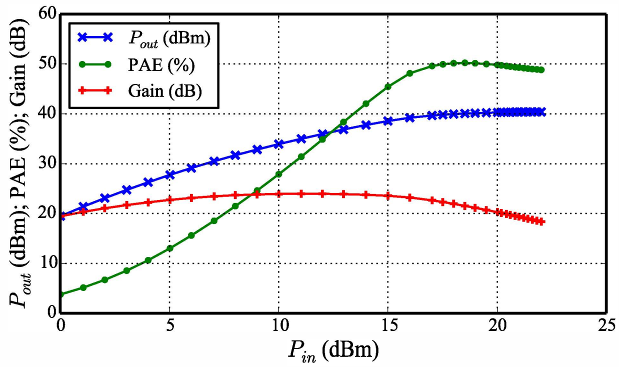


Fig. 2: Measured performance of the MMIC PA as an amplifier at 9.9 GHz with $V_{G1}$=-2.4 V and $V_{G2}$=-3.0 V. Following the time-duality principle, the rectifier should achieve similar efficiency at the corresponding output power of 40 dBm.

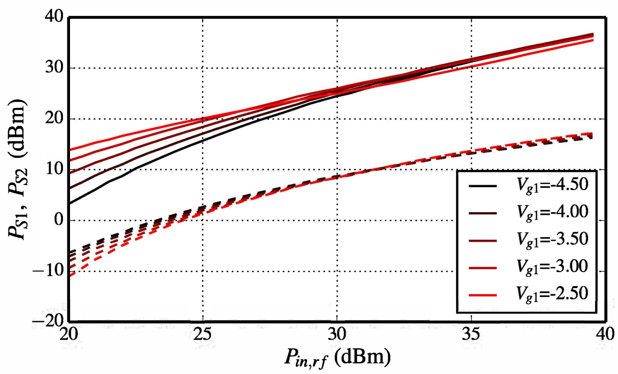


Fig. 3: Stage 1 and Stage 2 rectified power as a function RF input power at various Stage 1 gate bias voltages ($V_{G1}$). The optimal bias point depends on input power. For high input power, a lower gate bias for Stage 1 and a higher gate bias for Stage 2 gives maximum output power for each stage respectively. The measurement is performed at 9.9 GHz with $R_{DC1} = R_{DC2} = 30\,\Omega$.

a two stage amplifier as a rectifier there are several control variables that can be studied and optimized. Since the gate of the output stage is loaded by the combination of the RF load and the Stage 2 equivalent impedance, the gate bias on the input stage, as well as the $Z_{RF}$, set the operating point of the Stage 1 rectifier. Previous work on RF rectifiers that involved class C and $F^{-1}$ amplifiers biased the device in cutoff. In this work, the PA was designed as a class AB amplifier, so it is important to also look at the gate bias of the output stage as an additional optimization variable. To investigate and determine the optimal mode of operation, the DC power of each stage is measured separately and the corresponding gate voltages, $V_{G1}$ and $V_{G2}$, and $Z_{RF}$ are varied.

For Stage 1, the gate voltage was varied from -4.5 V to -2.5 V, with the optimal $V_{G1}$ = -3.5V. The devices in this process are pHEMTs and are effectively cutoff at -4 V. Measured rectified power for both stages is shown in Fig. 3. The optimal gate bias for Stage 2 was -3.0 V, used for the remainder of this

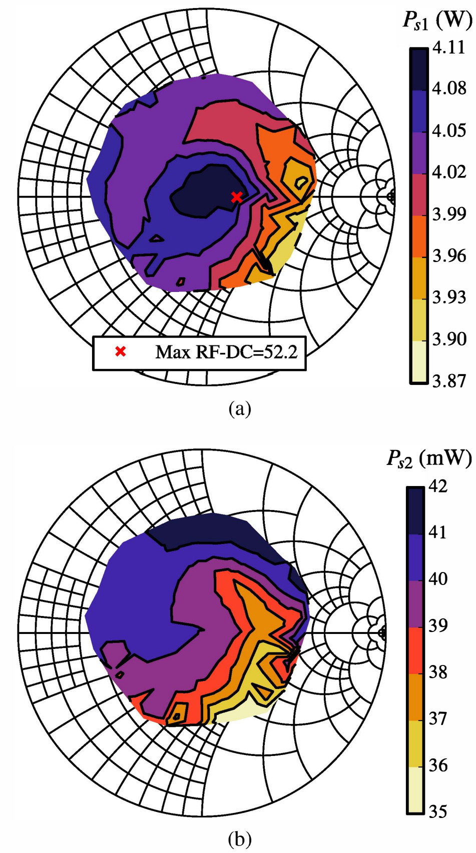


Fig. 4: (a) Stage 1 and (b) Stage 2 DC rectified power contours as a function of the RF load impedance at 8 W RF input power, $V_{g2}$=-3.0 V. The maximum system conversion efficiency point is shown at 69-0.4j Ω. The measurements are performed at 9.9 GHz with $R_{DC1} = R_{DC2} = 30\,\Omega$.

paper. After the optimal Stage 1 gate bias was determined, $Z_{RF}$ is varied using the tuner. The rectified power for each stage from the loadpull is shown in Fig. 4a. At 8 W RF input power, the maximum RF efficiency is observed at 69-0.4j Ω within the peak DC power contour of 4.11 W. The measured rectified power of Stage 2 as a function of $Z_{RF}$ is shown in Fig. 4b. It is seen that the optimal RF load for Stage 2 differs significantly from the one that maximizes efficiency of Stage 1, and the power contribution from Stage 1 accounts for 98% of the total rectified power. The role of Stage 2 in the rectifier configuration is to terminate the primary power handling stage (Stage 1) correctly and therefore optimize overall rectifier efficiency.

The Stage 1 rectified power and voltage are measured as a function of the Stage 1 DC load, $R_{DC1}$. An optimal DC load of approximately 30 Ω is found as shown in Fig. 5. This DC load is also used for Stage 2, and a method of combining the DC loads and therefore DC power is currently under investigation. The overall RF efficiency depends primarily on the Stage 1 gate bias voltage and is summarized in Fig. 6. The overall conversion efficiency as a function of the RF load is shown in Fig. 7 with a maximum measured value of 52.2% at 8 W input power.

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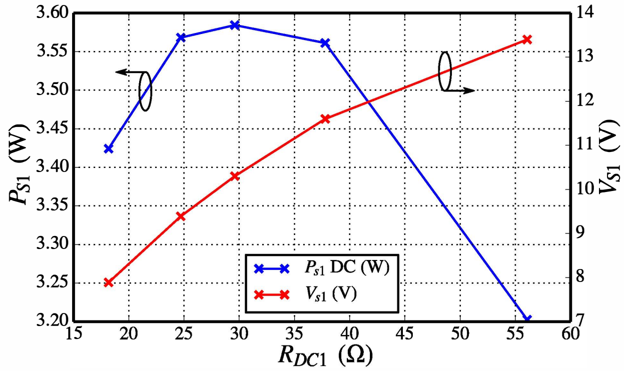


Fig. 5: Stage 1 DC rectified power and voltage versus DC load with 8 W RF input power. The optimum DC load resistance is approximately 30 Ω.

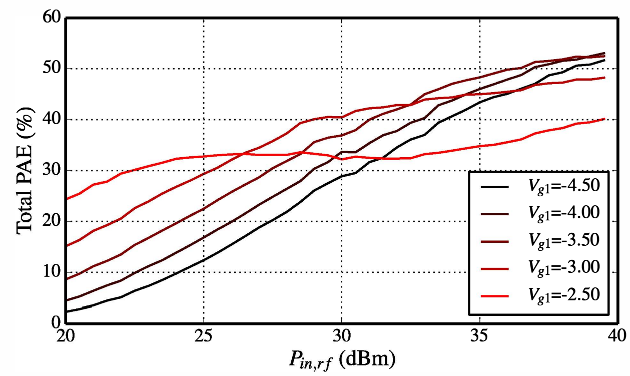


Fig. 6: Total RF-DC conversion efficiency as a function of stage 1 gate bias voltage. RF-DC efficiency at optimal gate bias voltage and RF load impedance matches the peak PAE results from the amplifier section.

## III. Conclusion

This paper has demonstrated that high efficiency and high power RF rectifiers can be realized with MMICs designed as two-stage power combined PAs. As a PA the MMIC achieved 10 W of output power and >20 dB of gain with a PAE of 50%. For 8 W of input power in the rectifier configuration the MMIC achieved a peak RF-DC efficiency of 52.2% at a peak DC power of 4.11 W. In previous work, [11], a maximum rectification efficiency of 85% was achieved at 10 W RF input power, exceeding the PA maximum output power by close to 3 dB. Therefore it is anticipated that higher efficiencies can be achieved with more RF input power, which is the current limitation of our setup.

The envisioned applications of this rectifier is in wireless power transfer when high power levels are required. In fact, the same MMIC can be used as both a transmitter and receiver/rectifier as illustrated in Fig. 8 with the blue (dashed) lines representing the rectification mode and the red (solid) lines representing the PA mode. This work demonstrates that high power multistage MMIC amplifier/rectifier pairs, designed using traditional PA techniques, can be applied to bi-directional high efficiency wireless power transfer systems. Additionally, power combining, as demonstrated in both the PA and rectifier modes in this work, is scalable on either transmitter or receiver side with additional MMIC modules. The power that can be wirelessly transferred is largely limited to the efficiency and feasibility of combining multiple MMIC modules on the transmitter side as further increases in RF input power above 8W showed no improvement in rectifier efficiency.

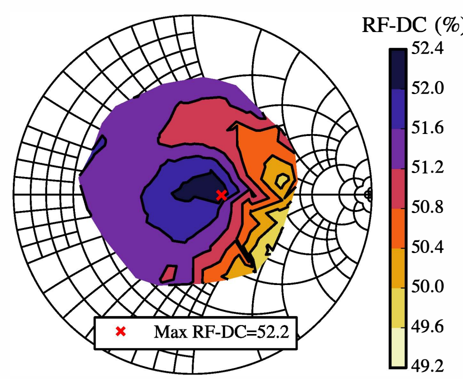


Fig. 7: Total RF-DC contours showing how the RF load affects system efficiency. A maximum PAE of 52.2% is achieved at $Z_{rf}$=69-0.4j Ω.

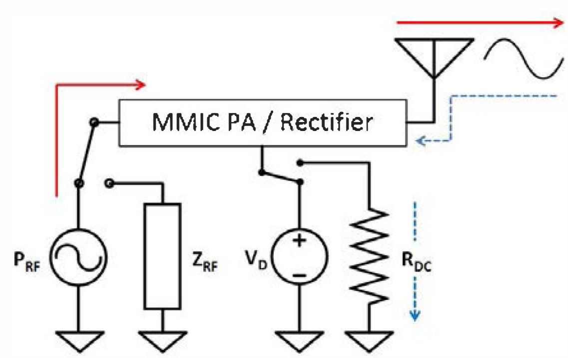


Fig. 8: Block diagram of a bi-directional transmitter/rectifier for wireless power transfer. By switching RF loads and excitation sources, a single MMIC can be utilized for both roles.


## Acknowledgment

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