A 4.2-W 10-GHz GaN MMIC Doherty Power Amplifier

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***Abstract*—This paper describes the design and performance of an X-band GaN monolithic microwave integrated circuit (MMIC) Doherty power amplifier (DPA) in a 0.15 μm gate length GaN on SiC process. The measured output power is greater than 36 dBm at peak PAE of 47% at 10 GHz. Gain flatness of $\pm$0.1 dB around 9.2 dB is obtained at up to 25 dBm input power. The PAE at 6 and 10 dB backoff is 41% and 31% respectively. For a 10-Mbps OQPSK signal, the ACPR at 10 MHz is $>$30 dBc at maximum output power and $>$33 dBc at 10 dB backoff. This combination of linearity and efficiency at backoff represents state of the art for an X-band DPA. Limitations of supply modulation in DPAs to further extend output power back-off are highlighted in the discussion.**

***Index Terms*—Monolithic microwave integrated circuit (MMIC), Gallium Nitride (GaN), peak to average power ratio (PAPR)**

I. Introduction

Modern spectrally-efficient signals consist of multiple sub-carriers resulting in high peak-to-average power ratios (PAPR) and large channel bandwidths. When N unity-amplitude sinusoidal waveforms are added, the peak amplitude can be as high as N, while the average is in general much lower due to destructive addition. The majority of the research performed in investigating how to amplify these spectrally-efficient signals is performed in the low or sub-GHz range for the mobile handset and base station market.

Several GaN MMICs have been reported at X-Band frequencies; under pulsed input in [1], PAE=51% with P_{out}=40.6 dBm and a saturated gain G_{sat}=10 dB is reported at 10 GHz. Under CW operation, 58% PAE with 9.7 dB gain at 37 dBm saturated output power was shown in [2]. Four different two-stage GaN MMIC designs are reported with up to 41 dBm output power, 65% PAE and 20 dB gain in [3]. These results were all obtained with PAs at various levels of saturation and the PA efficiency degrades at backed off power levels. In order for the PA to efficiently amplify high PAPR signals, several methods such as Doherty [4], envelope tracking [5], harmonic injection [6], and outphasing (LINC) [7] have been suggested.

At X-band, a GaN MMIC PA combined with a supply modulator demonstrated PAE=34.8%, G_{sat}=6.4 dB, and peak power of 36.5 dBm under 18 MHz OFDM, 11 dB PAPR signal [8]. An X-Band GaN envelope-tracking PA is reported with 35.3% PAE, and average output power of 1.096 W with a 60 MHz LTE-A, 6.6 dB PAPR modulated signal in [9]. Using GaAs technology, an X-band Doherty PA is presented which has 53% drain efficiency with 6.5 dB gain and 30 dBm output power with 6 dB power back-off [10].

In this paper an X-band Doherty power amplifier is realized using the Qorvo 0.15 μm GaN on SiC process which efficiently and linearly amplifies signals with more than 6 dB PAPR. A K-Band Doherty PA is demonstrated in the same process with 25% PAE at 8 dB back-off [11]. A summary of previous results and the current work is given below.

TABLE I
Summary of X-band PA Performance

Topology	Max PAE (%)	P_{out} (dBm)	Gain (dB)	Ref
-	39.5	45.5	13.5	[1]
Supply-Modulated	59.9	41.14	20	[3]
Supply-Modulated	69	36	8.5	[8]
Envelope Tracking	35.3	38.5	7.6	[9]
Doherty	53 (η_{drain})	30	6.5	[10]
Doherty	47	36	9.2	This paper

The paper is organized as follows: design of the MMIC DPA along with its layout is detailed in section II; section III presents the measurement results; an attempt to investigate the performance of this Doherty with discrete voltage supply modulation is presented in section IV.

II. X-Band MMIC Doherty PA

The conventional Doherty amplifier consists of two amplifiers in parallel as shown in Fig. 1(a). The carrier amplifier (top), is biased such that it is always on and in Class AB or Class B mode. The peaking amplifier (bottom), is biased in Class C. The goal of the Doherty design is to select biases and a device periphery ratio such that the peaking amplifier is turned on when the carrier amplifier is saturating [12]. Load modulation between the carrier and peaking amplifiers assures that at higher power levels, the load of the carrier amplifier decreases, while that of the peaking amplifier increases, thus maintaining high efficiency over a large range of output power levels.

A. Design

The circuit in Fig. 1(b) is implemented as a MMIC and differs from the conventional Doherty architecture in Fig. 1(a). The input divider is implemented without the typical coupler as detailed in [13]. The input divider network is an unequal power divider that changes the ratio of power delivered to

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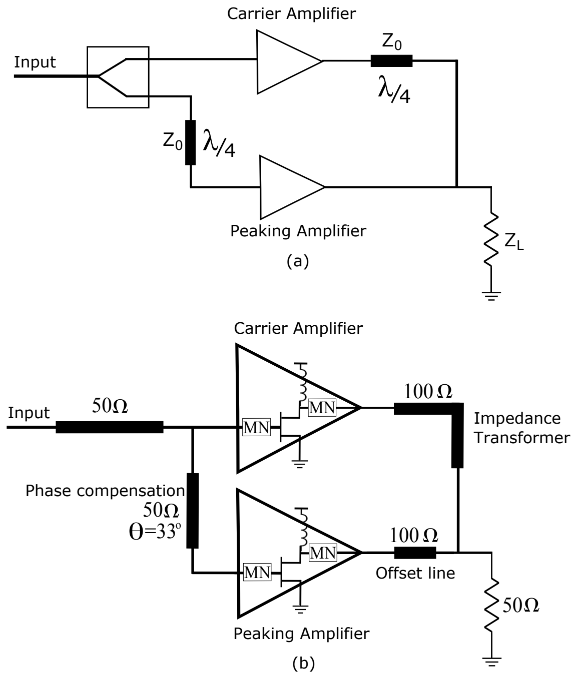

Fig. 1. (a) Conventional topology of the Doherty power amplifier. (b) The Doherty architecture used in this paper. The $\lambda/4$ transformer is replaced with a combined matching network and impedance transformer. The input is an unequal-power reactive divider that compensates the output phase offset.

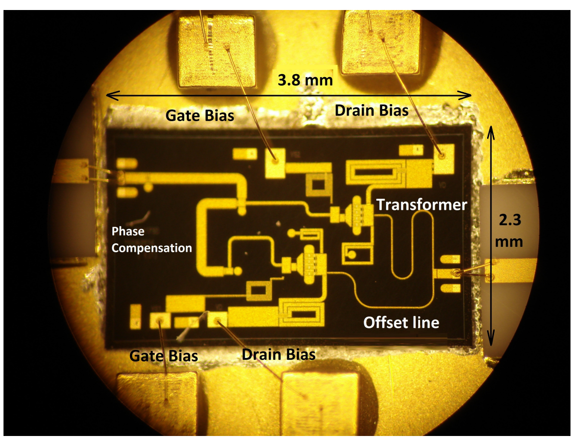

Fig. 2. The MMIC DPA on a CuMo carrier with alumina microstrip interconnects as tested. 100 pF bypass capacitors are shown connected to drain and gate DC pads. The die size is 3.8mm x 2.3 mm.

each device as input power increases. This is due to the fact that the carrier and peaking amplifiers have drastically different changes in input capacitance (C_{in}) over input drive. The carrier amplifier C_{in} typically experiences a 10% increase while the peaking amplifier C_{in} experiences a 200% increase [13]. The increased C_{in} of the peaking amplifier reduces the load impedance presented to the input divider network at the peaking amplifier port and therefore as input power increases, more power is directed to the peaking amplifier. This effect is desirable as the carrier amplifier is not overly saturated and kept in a high efficiency region when input power is

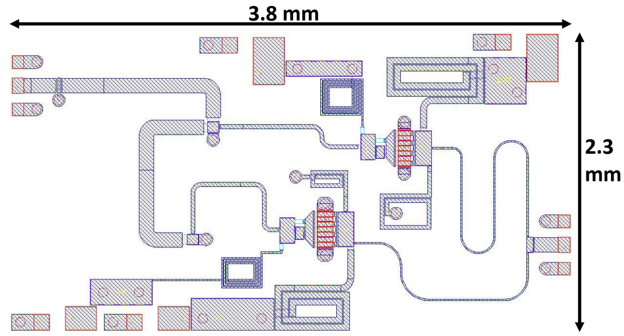

Fig. 3. Layout of X-Band MMIC Doherty PA. Vias are visible in the capacitor-over-via bypass capacitors and in the ground pads for RF and DC probes.

further increased. The output network does not employ a $\lambda/4$ impedance transformer but a matching circuit that transforms the dynamic load impedance seen by the carrier amplifier and simultaneously achieves optimal output power. The output transformer electrical length is compensated in the peaking amplifier input path by additional $50\,\Omega$ microstrip line. An image of the fabricated MMIC is shown in Fig. 2 and layout in Fig. 3

B. Layout

The layout is performed using the process development kit (PDK) with related design rules and an Angelov nonlinear model and HB simulations. The process offers three metal interconnects (3MI), allowing air-bridges and plated lines that can handle 16 mA/μm current density. There are three different types of MIM capacitors, 240, 300 and 1200 pF/mm^2 as well as TaN and ohmic metal resistors. As shown in Fig. 3, each bypass capacitor is constructed in a capacitor-over-via way. Substrate via dimensions are predefined for the specific substrate thickness and are circular with a 40 μm diameter. The input line is 92 μm wide, $50\,\Omega$ microstrip connected to 50 μm pitch GSG CPW probe footprints at the input. This input line splits to the carrier and peaking amplifier and forms the unequal input divider. For the carrier amplifier path, the line is 25 μm wide and corresponds to $85\,\Omega$.

The carrier amplifier is designed to operate in moderate class AB mode and is biased at -2.7 V with a 20 V drain supply. The pinch-off voltage for these pHEMT devices is near -4.0 V. After the expected output power and optimal load impedance was determined from nonlinear load-pull simulations, the output transformer and integrated supply and bias line network were designed. The drain supply is connected to the carrier amplifier with a 40 μm wide line as a planar inductor with a 23 pF capacitor-over-via bypass capacitor. The carrier amplifier device periphery is 8x80 μm. The carrier amplifier is connected to the amplifier output via a $100\,\Omega$ impedance transformer. Since this line needs to be such a high impedance, a 10 μm line width was implemented with multiple metal layers retaining the current handling capability of 160 mA. The DC drain current is never present on the output impedance transformer line as all drain current passes through the much wider 40 μm lines previously mentioned. Referring to Fig. 1(b), the phase offset of the output impedance transformer requires a phase compensation line on the input unequal power divider that is seen in the additional 50Ω line after the input power divider split. Source inductance was added with planar inductors between the source and ground vias for each device. This was done to reduce the reactance of each device and pre-match the devices to the transmission line transformers. A parallel RC was added to each gate to ensure stability. In this design, the devices were made unconditionally stable prior to input and output network synthesis.

The carrier to peaking amplifier device periphery ratio is what controls the power back-off range and is therefore critical to successful Doherty operation. In this design, the ratio was chosen close to unity to optimize efficiency and maximum output power. Initially, synthesis of the input and output networks was performed using linear transmission line, capacitor, and resistor models available from the PDK. Using the AWR Axiem method of moments simulator, these linear simulated layout blocks were then validated by EM simulation. Full simulation of the Doherty is then repeated iteratively to ensure efficiency and output power targets were met. The finalized layout of X-Band MMIC Doherty is shown in Fig. 3.

III. CHARACTERIZATION

The die is mounted on a CuMo carrier and the pads are bonded to 50 Ω alumina lines. Probe station measurements are made with a drain supply of 20 V, a carrier gate bias of -2.7 V, and peaking gate bias of -5 V. The measured PAE of the Doherty is shown in Fig. 4. More than 41% PAE is obtained over 6 dB output power back-off. More than 30% PAE is obtained at 10 dB back-off at 10 GHz. Fig. 5 shows the measured output power and gain. The DPA provides a peak power of >36 dBm, peak PAE of 47% and peak gain of 9.2 dB.

At the low-power region, the linearity of the amplifier is entirely determined by the carrier amplifier. Therefore, the carrier amplifier should be highly linear. The measured PAE vs. P_{out} characteristic in Fig. 4 does not exhibit the textbook Doherty behavior illustrated by the dashed line, where the carrier PA is fully saturated before the peaking amplifier turns on. In the design presented here, the saturation onset is soft which improves the linearity because of reduced clipping. Additional possible linearity improvement can be attributed to the harmonic cancellation from the two amplifiers using appropriate gate biases [4]. In Fig. 6, the power spectral density of the DPA is shown for a 10 Mbps OQPSK signal at different output power levels. The Adjacent Channel Power Ratio (ACPR) of the DPA with this 3.3-dB PAR signal is measured to be better than 30 dBc at an output power of 35 dBm and more than 33 dBc for 25 dBm of output power 10 MHz away from the carrier.

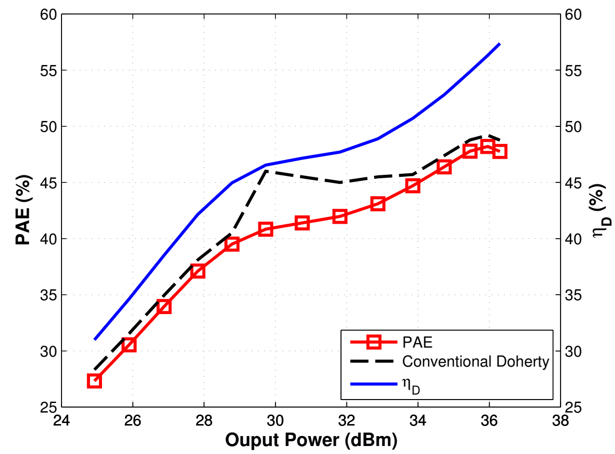

Fig. 4. Measured drain efficiency (blue) and PAE (red) of the DPA versus output power at 10 GHz. The dashed line shows idealized Doherty PAE for a comparison.

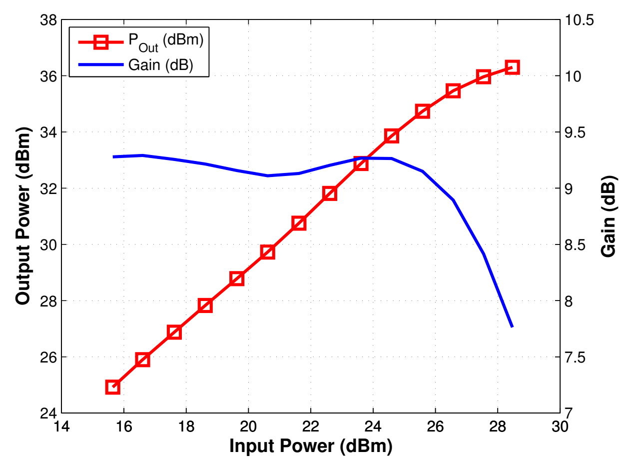

Fig. 5. Measured output power (red) and gain (blue) of the DPA versus input power at 10 GHz. The output power peaks at 36 dBm.

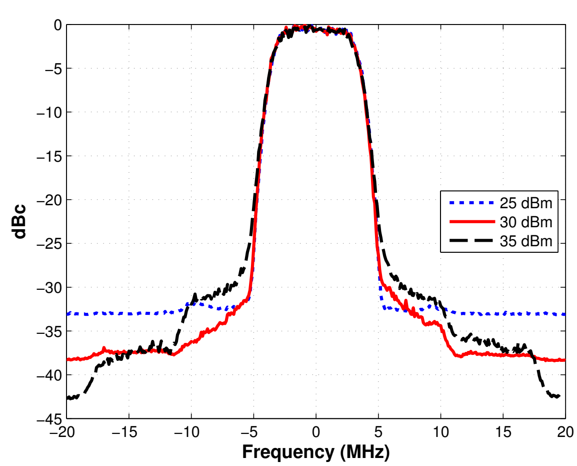

Fig. 6. Measured output frequency spectrum around 10 GHz of DPA for a 10 Mbps OQPSK signal for different output powers.

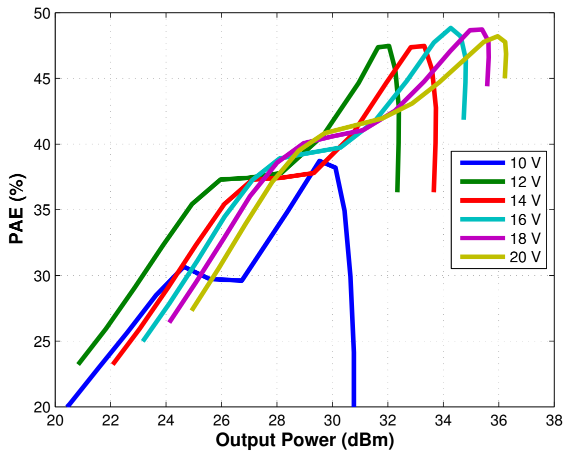

Fig. 7. PAE and output power in a supply modulation experiment where both carrier and peaking PA were simultaneously modulated.

IV. Discussion and Conclusion

Fig. 4 demonstrates the Doherty operation of this MMIC PA with 6 dB output power back-off. Part of the design motivation for this PA was to determine if the output power back-off of a Doherty could be extended even further than conventional and state of the art designs. One application is a potential mixed output power mode operation, using maximum output power in emergencies and largely backed-off and linear power modes nominally, for a phased array unit cell [14]. To achieve further output power back-off, a stepped drain supply modulation experiment was performed [8]. The results of this experiment are shown in Fig. 7. Moderate gains in PAE can be achieved by following the 20 – 12 V range trajectory. However, as the drain voltage drops below 10 V, the 20 -V, fixed-supply Doherty PA maintains more efficient operation. The moderate gains of the 20 – 12 V range are also likely to be offset by the additional complexity and efficiency degradation due to a multi-level switched dynamic supply.

In summary, this paper presents a highly linear and efficient 4.2-W MMIC Doherty Power Amplifier at 10 GHz. A peak PAE of 47% is obtained in CW operation. The measured PAE is greater than 40% at 6 dB back-off. More than 30 dBc ACPR is achieved at a maximum output power of 35 dBm with a 10 Mbps OQPSK input signal. The results demonstrate that high efficiency in back-off can be achieved with good linearity in an X-band Doherty GaN MMIC.

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