Single-DC-Input Multi-Level Envelope Tracking of a High-Efficiency X-band Power Amplifier

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***Abstract* — This paper addresses the efficiency enhancement of microwave power amplifiers (PAs) with discrete-level supply-modulation. We demonstrate an efficient modulator architecture that generates three levels of drain supply voltages from a single dc voltage. Each level is stored in a "flying" capacitor that acts as a temporary voltage supply and is dynamically regulated by feedback through reversal of the PA drain current. A hybrid modulator based on GaN-on-Si technology is tested with a single-stage 2-W X-band MMIC PA with a drain efficiency of 55% at the peak output power. The overall average drain efficiency (PA and modulator) of up to 43% is measured with Gaussian-like pulses for radar and a 5-MHz 6-dB PAPR OFDM signal, and is improved up to 14 percentage points over a constant supply case, with normalized root mean square error below 1.5% when pre-distortion is used.**

***Keywords* — bootstrap capacitor, envelope tracking (ET), flying capacitor, power amplifier, rf system, supply modulation**

I. Introduction

Envelope tracking is applied to communications and radar transmitters to improve back-off efficiency when waveforms with high peak-to-average power ratios (PAPRs) are amplified [1], [2] [3]. In communications, continuous [1] or discrete [2] supply modulation has shown to significantly increase the back-off efficiency. In pulsed radars, the RF power amplifier (PA) can be operated with a variable drain supply to reduce dissipation in the case of amplitude modulated pulses, used to reduce time sidelobes and simultaneously improve spectral confinement [4], [5].

Ideally, continuous envelope tracking maximizes PA efficiency for every output power level. However, this requires either a linear voltage regulator, usually aided by a switching circuit for efficiency, or multiple voltage sources multiplexed at the PA drain. Applying multiple discrete voltage levels has the advantage of efficiency when implemented with power switches, at the expense of hardware complexity that requires additional voltage supplies for high-resolution voltage discretization [2]. The losses of the external voltage supplies should be accounted for a realistic assessment of the total power budget of a supply-modulated PA.

In this work, we address supply modulation of a PA together with the additional voltage level generation starting from a single-dc-input supply [6]. In an approach similar to that of [7], [8], a flying capacitor is used to store the intermediate voltage level, but rather than using a filter on the output to smooth the drain voltage, digital pre-distortion (DPD) is used to recover linearity of the PA. This approach is amenable to monolithic integration, and has the potential of wider bandwidth operation. In this paper, this method is demonstrated with three discrete voltage levels, but the topology is scalable to *N* levels by using *N-2* flying capacitors.

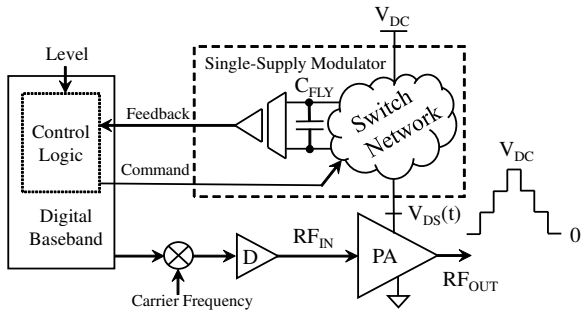
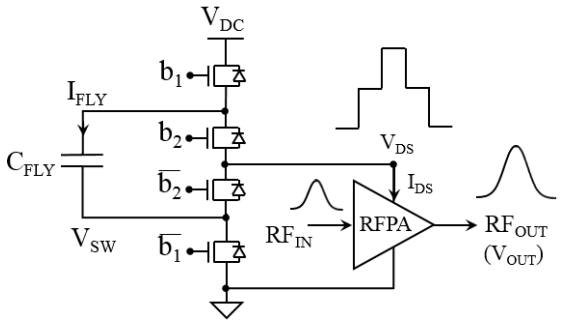


Fig. 1. Conceptual block diagram of the control technique enabling single-supply discrete envelope tracking of RF power amplifiers (PAs). In place of multiple external supplies, a flying capacitor C_{FLY} is used to store the voltage level and a control logic keeps the voltage regulated to a set-point.

II. Flying-Capacitor Multi-Cell Modulator

In the supply-modulated transmitter shown in Fig. 1, a switch network is fed by a single dc supply V_{DC} and generates an intermediate voltage level for back-off efficiency enhancement. In our approach, this lower voltage is directly derived from V_{DC} through the commutations of the switch network, by storing energy in a "flying" capacitor. The voltage across the capacitor is sensed with a comparator that generates a pulse-width modulation (PWM) signal representative of the capacitor state-of-charge. The PWM signal is fed back to the control logic, which selects a suitable switch configuration to both generate the required level V_{DS} and regulate the voltage across the capacitor. Because the I_{DS} current is always entering the PA drain (fast transient apart), it is necessary to design a switch network capable of reversing the I_{DS} direction through the flying capacitor. This can be accomplished with several topologies [9] and is demonstrated here with the *multi-cell converter* of Fig. 2(a), which uses a single flying-capacitor C_{FLY} with a switch network controlled by the bits b_1, b_2, and their complements.

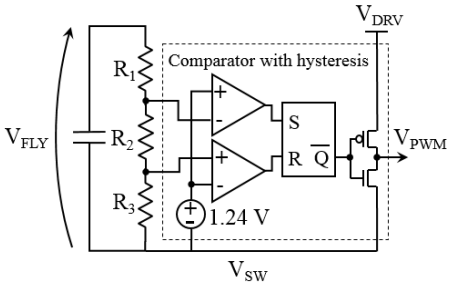
The circuit operation is summarized in Fig. 2(b): when the output voltage is 0 or V_{DC}, no regulation of the flying capacitor is possible. When an intermediate level is selected, V_{FLY} can be regulated upward or downward through I_{FLY} ($\{b_1, b_2\} = \{1, 0\}$) or its reversal ($\{b_1, b_2\} = \{0, 1\}$). This



(a)

b_1 b_2	I_{FLY}	V_{FLY}	V_{DS}
0 0	-	-	0
0 1	$-I_{DS}$	↘	V_{FLY}
1 0	I_{DS}	↗	V_{DC} - V_{FLY}
1 1	-	-	V_{DC}

(b)



(c)

Fig. 2. (a) Flying-capacitor multi-cell supply modulator used to demonstrate the feedback regulation with a dynamically varying load (RFPA). This circuit generates three voltage levels 0, $V_{DC}/2$, and V_{DC} with a single external supply V_{DC}. The control bits are selected to keep the flying-capacitor voltage V_{FLY} regulated to the set-point $V_{DC}/2$. (b) Circuit operation. (c) Flying-capacitor sensing circuit realized with a high-impedance voltage divider and comparator with hysteresis. The output is a PWM waveform V_{PWM} representative of the state-of-charge of C_{FLY}.

control is implemented in the finite-state machine (FSM) of Fig. 3. Assuming that V_{FLY} has already reached the set-point $\langle V_{FLY} \rangle = V_{DC}/2$, the three outputs are 0, $V_{DC}/2$, and V_{DC}. In our demonstration, V_{FLY} is sensed with the circuit of Fig. 2(c) in which a high-impedance voltage divider and comparator generates the PWM signal representative of the state-of-charge of C_{FLY}. For $V_{DC} = 20\,\text{V}$ and a ripple of 100 mV, the resistor values are $R_1 = 261\,k\Omega$, $R_2 = 384\,\Omega$, and $R_3 = 38.4\,k\Omega$.

The multi-cell modulator, sensing circuit and FSM are simulated in Powersim PSIM with ideal components and resistive load, as reported in Fig. 4. A three-level control signal consisting of a 1-MHz discretized sinusoid is applied at the input of the FSM. The voltage V_{FLY} is sensed by the comparator, which generates a PWM signal. This is fed back to the FSM to select the bit configuration b_1, b_2 based on the drain voltage V_{DS} and the state-of-charge of the flying capacitor. Once the set-point is reached, the simulation in Fig. 4 shows stable regulation of the flying capacitors within 100-mV ripple voltage.

III. Experimental Results

A prototype of multi-cell modulator is realized with a 4-layer FR4 board, Fig. 5. GaN-on-Si normally-off transistors (EPC 2014C) and GaN-specific gate drivers (TI LM5114) are selected. The external low-power driver supply $V_{DRV} = 6\,\text{V}$ is distributed in the circuit with a diode-capacitor bootstrap technique [10]. The flying capacitor is a 20-μF ceramic component and is placed on the bottom side of the board for low loop parasitics. The voltage across C_{FLY} is sensed with a low power consumption comparator (Microchip 841) which generates the PWM feedback signal. The control of the power switches is performed with four high-speed digital isolators: the top two are monodirectional (Si Labs 8610), while the other two are bidirectional (Si Labs 8622) to allow the PWM feedback signal.

The supply modulator is connected to a single-stage MMIC PA designed in the Qorvo 0.15-μm GaN-on-SiC process for efficient operation at X-band. At a nominal supply voltage of 20 V and a quiescent drain current of 60 mA, a peak output power of 34 dBm is measured with a drain efficiency

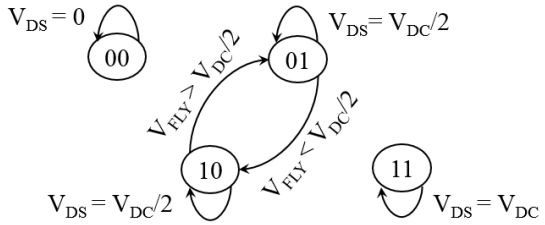


Fig. 3. Regulation network represented as a finite-state machine. Two redundant states ("01" and "10") are used to keep V_{FLY} regulated at $V_{DC}/2$.

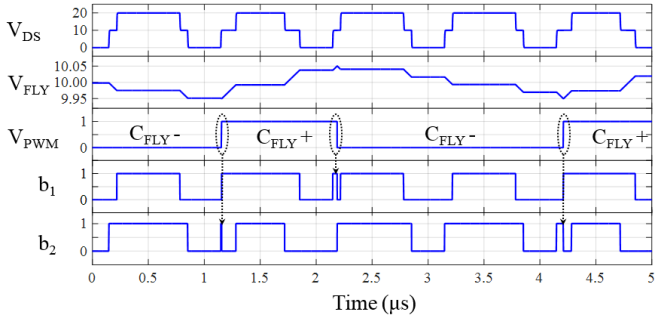


Fig. 4. Simulation with ideal components showing the operation of the circuit. A 3-level sinusoid is generated at the output. The waveform V_{FLY} shows the ripple voltage around the set-point (10 V) which is regulated by the FSM.

of 55 % at 10.2 GHz. At the peak input power of 27 dBm, I_{DS} peaks to 210 mA. The small-signal gain is 10.7 dB. The MMIC PA is mounted on a Rogers TMM10i substrate which provides gate supply bypassing and connection to the modulator. The PA characterization at 20 V and $V_{DC}/2 = 10\,\text{V}$ is shown in Fig. 6, with an improvement of more than 22 percentage points obtained from six to ten dB of backed-off power. The dependence of gain on supply voltage, characteristic of GaN, needs to be corrected with DPD.

The operation of the circuit is verified by supply modulating the PA. An 80-MHz bandwidth vector signal transceiver (NI VST 5645R) with X-band frequency extension [5] is used to test the system. The FSM is mapped in the FPGA within the VST for real-time control of the voltage feedback. We note that the closed-loop system is stable as long as the sum of delays in the feedback loop is a small part of the *RC*

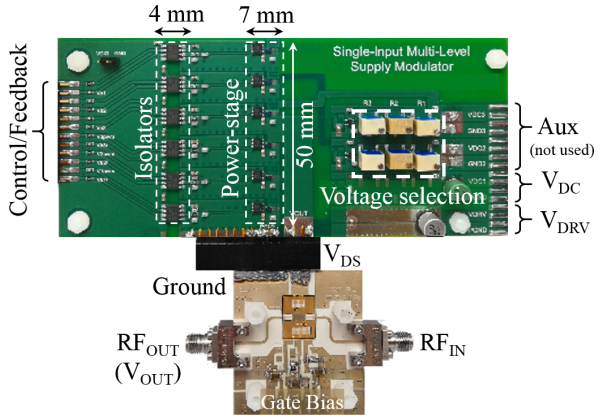


Fig. 5. Photograph of the supply-modulated PA with flying capacitor. The active area of the circuit is 11 mm × 50 mm. In this paper, only part of the circuit is used (four switches instead of six).

time constant, where $R = V_{DS}/I_{DS}$. This condition can be easily satisfied with typical load values because C_{FLY} can be arbitrarily increased at the expense of a slower start-up time.

As in other dc/dc converters, the start-up time is required to charge C_{FLY} and the switch driver capacitors before normal operation. This happens as follows: the FPGA generates the bit sequence (i.e., voltage staircase) and this activates a soft-startup of the drivers, comparator, and isolators as shown in Fig. 7 ($t = 0 \rightarrow 25$ ms). After the driver start-up ($t = 0 \rightarrow 2.5$ ms), the switch network regulates V_{FLY} to $V_{DC}/2$. Note that this start-up time is only required at the turn-on of the supply-modulated PA and is not necessary once the circuit is operating. Additionally, no RF signal amplification is required during the start-up phase as only the PA quiescent current charges the flying capacitor. Hence, the start-up duration is dependent on the *RC* time constant.

Fig. 8 shows the significant measured waveforms of the system once it reaches stable regulation: V_{OUT} is the PA RF output with Gaussian envelope and with drain modulation as 0-10-20-10-0 V and DPD enabled [11] (7 dB of linearized gain). The intermediate voltage level shows stable behavior around 10.35 V, kept within a 100 mV ripple by the PWM feedback (about 500 Hz commutation rate).

Radar pulses and an OFDM signal are used to test the supply-modulated PA. Given the *a-priori* knowledge of waveforms in radar transmitters, an iterative linearization technique [11] is utilized to compensate for PA non-idealities and provide a best-case performance estimation with DPD. Rectangular pulses and other Gaussian-like shapes are considered for this comparison. The duration of the pulses is varied to obtain the same average RF output power $P_{OUT,AVG}$ with the period kept fixed to 100 μs. Average drain efficiency $\eta_{D,AVG} = P_{OUT,AVG}/P_{DC}$ is used to evaluate the performance of the PA including also the supply modulator losses.

Table I reports a compilation of measurements performed with different windowing functions for radar applications [12]. A comparison is made between a typical rectangular drain voltage pulse (i.e., "Rect. + DPD" case) and supply modulation (i.e., "SM + DPD" case) with regard to linearity

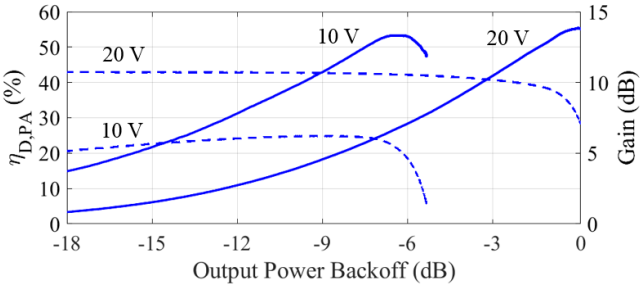


Fig. 6. Measured pulsed drain efficiency (continuous) and gain (dashed) of the PA at 10.2 GHz for 10 and 20 V supplies. More than 22 percentage point improvement is observed between 6 to 10 dB back-off (the PA is optimized for drain voltages between 10 and 20 V).

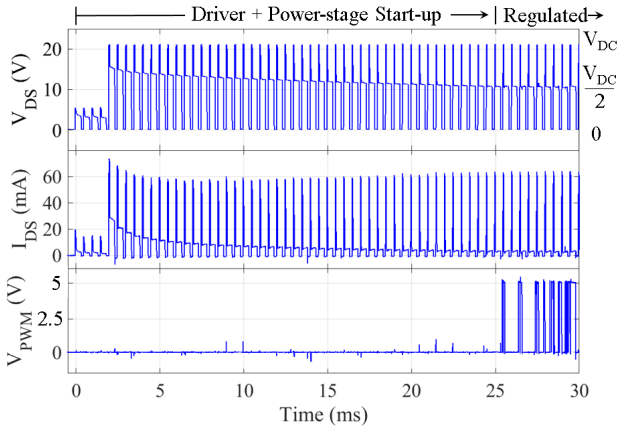


Fig. 7. Measured waveforms for the start-up of the supply-modulated PA. At $t = 0$ ms, the driver capacitors and C_{FLY} are discharged. The FSM generates commands to charge the capacitors to $V_{DC}/2$ through the bias current at V_{DS} of the PA. During the start-up, no RF signal is amplified by the PA (only quiescent current present).

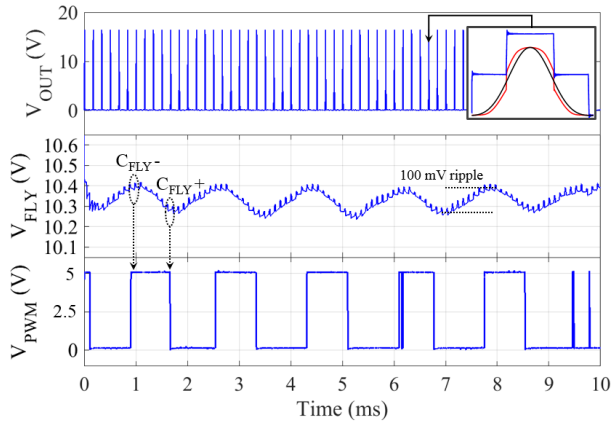


Fig. 8. Measured waveforms after the FSM has started to regulate V_{FLY}. At $t = 0$ ms, both the driver's capacitors and C_{FLY} are discharged. The FSM generates the digital commands that initiate the charge of these capacitors to the selected set-point ($V_{DC}/2$) through the bias current at V_{DS} of the PA.

and efficiency. Figs. 9-11 report the time and frequency domain output of the amplifier for a rectangular, Blackman, and OFDM sequence with 5-MHz bandwidth and 6-dB PAPR. Up to 11 percentage points of improvement are observed for the radar waveforms with normalized root mean square error (NRMSE) linearity recovered with DPD. The 5-MHz 6-dB PAPR OFDM signal achieves improvement of about 14 percentage points as compared to the fixed V_{DC} case. These

Table 1. Result summary for different radar waveforms with fixed average output power and 100-μs repetition period.

Waveform			Supply-Modulated PA		Linearity		Efficiency
Window	Supply	Duration	$P_{OUT,AVG}$	P_{DC}	NRMSE	1st spectral sidelobe	$\eta_{D,AVG}$
Rectangular	Rectangular	10 µs	240 mW	460 mW	1.2%	-13 dB	52%
Raised Cosine	Rect. + DPD	27 µs	235 mW	734 mW	0.9%	-32 dB	32%
Raised Cosine	SM + DPD	27 µs	236 mW	548 mW	1.1%	-32 dB	43%
Triangular	Rect. + DPD	30 µs	237 mW	846 mW	0.8%	-28 dB	28%
Triangular	SM + DPD	30 µs	240 mW	615 mW	1.3%	-28 dB	39%
Blackman	Rect. + DPD	33 µs	232 mW	859 mW	1.0%	-56 dB (-58 dB ideal)	27%
Blackman	SM + DPD	33 µs	235 mW	652 mW	1.5%	-55 dB (-58 dB ideal)	36%

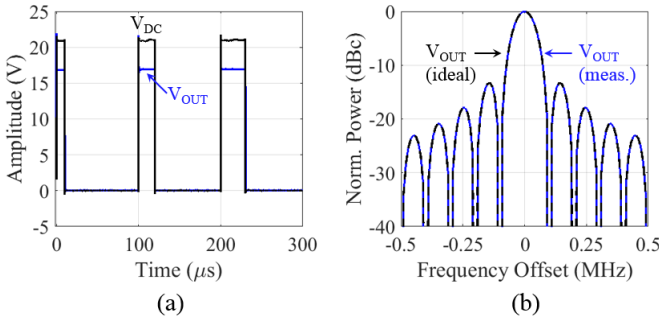


Fig. 9. (a) Time domain rectangular pulses with variable duty cycle (10%, 20%, and 30%) and 100-μs repetition period. (b) Ideal and measured spectra for the only 10% pulse and 100-μs repetition period.

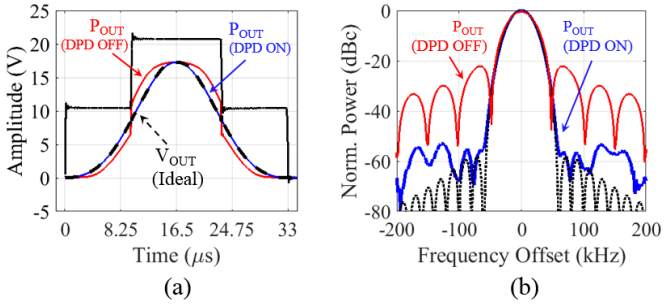


Fig. 10. (a) Time domain Blackman pulse with 100-μs repetition period (not visible). (b) Ideal and measured spectra for the only 10% pulse and 100-μs repetition period.

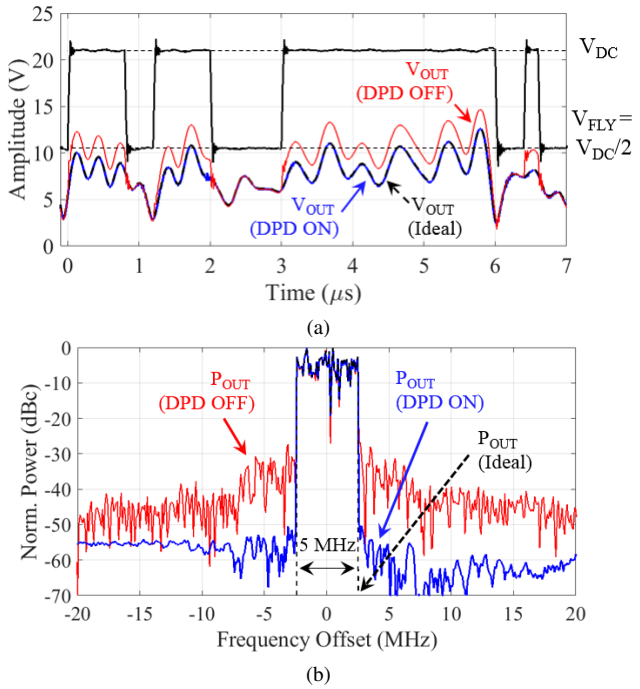


Fig. 11. (a) Time- and (b) frequency-domain representation of a 10-μs long OFDM signal with 6-dB PAPR and 5-MHz bandwidth. Even for highly variable signals, the FSM is capable to regulate V_{FLY} to $V_{DC}/2$. Low distortion is achieved by iterative learning DPD.

results also includes the modulator efficiency as well as the synthesis of the intermediate voltage $V_{DC}/2$.

In summary, we have shown significant efficiency enhancement of an X-band MMIC PA with a single-dc-input three-level supply modulator. The approach is scalable to more levels, which is the topic of ongoing research.

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