0.01–22-GHz Feedback-Stabilized Single-Supply GaAs Cascode Distributed Amplifiers

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***Abstract*— This letter presents the design of five-cell cascode distributed amplifiers (DAs) in the WIN Semiconductor PIH1-10 enhancement-mode GaAs pHEMT process. Single- and two-stage DA monolithic microwave integrated circuits (MMICs) are demonstrated, with die areas not exceeding 2.5 × 1.5 mm^2 and same-polarity supply and bias voltages. The cascode cells are stabilized using an *RC* drain-gate feedback network at the common-gate transistor of each cell, and a stability analysis is presented. All transistors have a gate width of 2 μm × 75-μm, with 750-μm total common-source gate periphery per single-stage design. The measured small-signal gain is 11.5 dB with 2.6 dB flatness and 23.2 dB with 3.2 dB flatness for the one- and two-stage amplifiers, respectively, from 10 MHz to 22 GHz. The amplifiers produce over 20-dBm output power at 3-dB gain saturation across the band.**

***Index Terms*— Distributed amplifier (DA), HEMT, monolithic microwave integrated circuit (MMIC), stability.**

I. Introduction

MONOLITHIC microwave integrated circuit (MMIC) distributed amplifiers (DAs) are often the architecture of choice for multioctave and multidecade bandwidth applications [1]–[3]. In this type of circuit, the input and output capacitances of the transistors or gain cells together with series inductors form artificial transmission lines at the input (gate-side) and output (drain-side), respectively. This approach is used for broadband small-signal gain stages and low-noise amplifiers [4], and nonuniform DAs (NDPAs) in GaN are shown to produce 10 W of output power over a 2–20 GHz decade [5].

A cascode amplifier as a gain cell improves the DA's gain-bandwidth product. The cascode DA topology has inherently wider bandwidth due to reduction of the Miller effect [6], and higher output voltage swing for increased output power [7]. The common-gate (CG) transistor's input impedance at its gate node is a concern for possible instabilities, and a gate-degeneration resistor is most commonly used, as in some earlier cascode-based DAs [7]–[9]. Another stabilization method for a cascode cell in a DA is an *RC*-network between the drain and the gate of the CG transistor [10], which we, for the first time, validate experimentally in this work for a DA.

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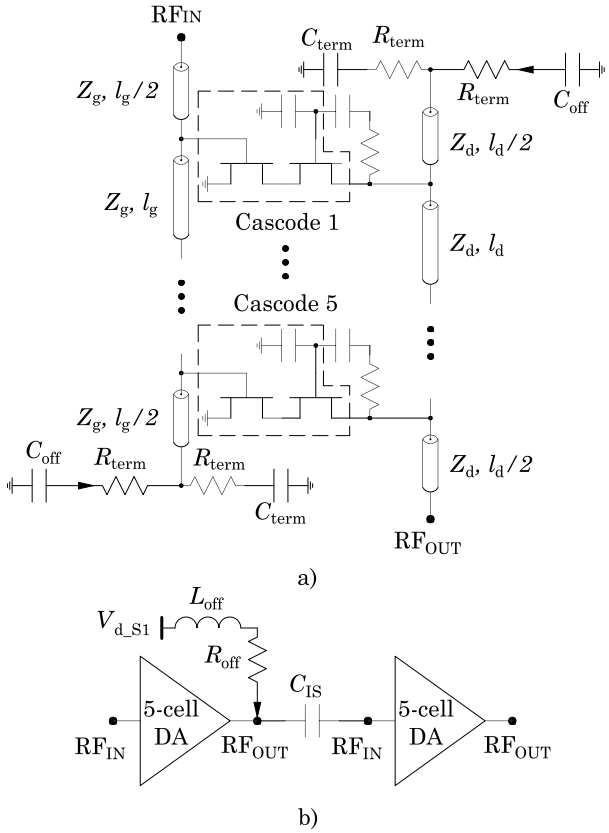

Fig. 1. (a) Simplified circuit diagram of a single-stage five-cell DA with *RC*-feedback stabilization in the CG transistor. External bias tees are connected to the RF input and output. Each transistor in the cascode cells is of 2 μm × 75-μm gate periphery. (b) Block diagram of the two-stage DA. The arrows indicate wire bonds.

In [11], [12], the network had different configuration and purpose.

The single-stage DA circuit is shown in Fig. 1(a). Five cells provide at least 10 dB of small-signal gain in a reasonable footprint. Fig. 1(b) shows a block diagram of the two-stage DA consisting of two single-stage, five-cell amplifiers connected via an on-chip interstage capacitor $C_{IS} = 3$ pF. The conical inductor $L_{OFF} = 1.65$ μH provides the first-stage supply voltage V_{d_S1} and resistor $R_{OFF} = 50$ Ω damps bias-line resonances.

In this letter, we present one- and two-stage cascode DA MMICs fabricated in an enhancement (E)-mode GaAs pHEMT process. To the best of our knowledge, this is the first demonstration of a single-polarity supply and bias, full E-mode HEMT DA. Earlier similar works include a combined E-/D-mode DA [13] and an E-mode triple cascode low-noise

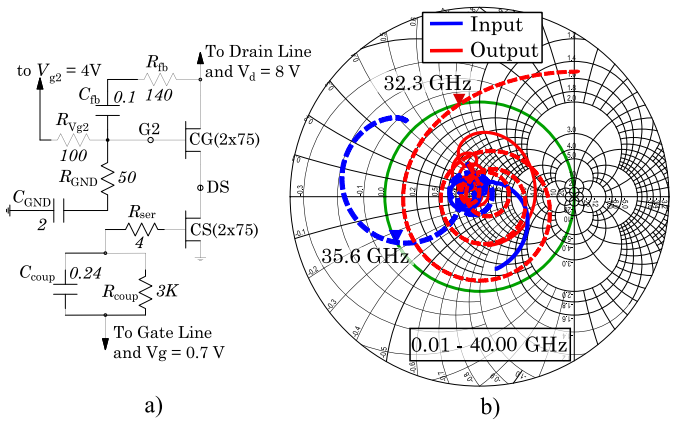

Fig. 2. (a) Schematic of stabilized DA cascode cell. Resistances and capacitances values are in ohms and picofarad, respectively. Gatewidths are in micrometer. The loop gain is evaluated at the "DS" and "G2" nodes in Fig. 3. (b) Input and output reflection coefficients of one-stage DA with (solid) and without (dashed) feedback stabilization circuitry. The Smith chart radius is 2, and markers indicate frequencies where input and output impedances cross the $\Gamma = 1$ circle (green).

amplifier [11]. We present the design and RC-network stabilization of the single-stage DA evaluating the loop gain at different cells [14], followed by measurements of the single- and two-stage MMIC DAs.

II. Five-Cell DA Design

The amplifiers are implemented in the PIH1-10 WIN Semiconductors E-mode pHEMT process on a 100-μm GaAs substrate [15]. A 150-μm gate periphery for both common-source (CS) and CG devices [Fig. 2(a)] is chosen as a compromise between small input–output capacitance and sufficient peak dc $g_m \approx 110$ mS. Each CS transistor is biased with a quiescent current of $I_{dq} = 45$ mA with supply and bias voltages as in Fig. 2(a). Each stage is supplied and biased off-chip at "RF In" and "RF Out" (Fig. 1).

Although series gate resistors are used initially for both CS and CG transistors (Fig. 2, R_{ser} and R_{GND}, respectively) the electromagnetic (EM) simulations of the single-stage DA show potential instabilities. Input and output reflection coefficients with magnitudes > 1 are observed in the small-signal regime at frequencies above the operating range [dashed lines in Fig. 2(b)]. A series RC-network (R_{fb} and C_{fb}) is therefore added between the drain and the gate of the CG transistor in each cell [10]. The network limits the cascode cell gain at high frequencies with no considerable degradation in the operating frequency range. Upon adding the RC-network to each cell of the amplifier, unconditional low- and high-frequency stability [solid lines in Fig. 2(b)] is achieved. The small-signal loop-gain stability criterion is evaluated at two nodes ("G2" and "DS" in Fig. 2) for each cascode cell and results for odd-number cells with and without feedback stabilization are shown in Fig. 3. Note that the stability criterion applied to different identical cascode cells within the DA gives different results, necessitating analysis of each cell.

A lossless gate artificial transmission line consists of the total shunt input capacitance C_{in} of the cascode cells and the series inductors L_g. Simulated small-signal equivalent-circuit parameters for a 150-μm CS device are $C_{gs} = 240$ fF, $C_{gd} \approx C_{ds} = 40$ fF. Compared to feedback and output capacitances, the gate–source capacitance C_{gs} of an FET is dominant [1], limiting the gate-line cutoff frequency and the overall gain-bandwidth product, as well as making it difficult to design gate and drain lines with the same characteristic impedance. A series capacitor C_{coup} at the input of each cell reduces the capacitive loading of the gate line (Fig. 2), providing $C_{in} = C_{gs}/2$ for $C_{coup} = C_{gs}$ [16]. A several kΩ shunt resistor R_{coup} provides the gate bias for each CS transistor.

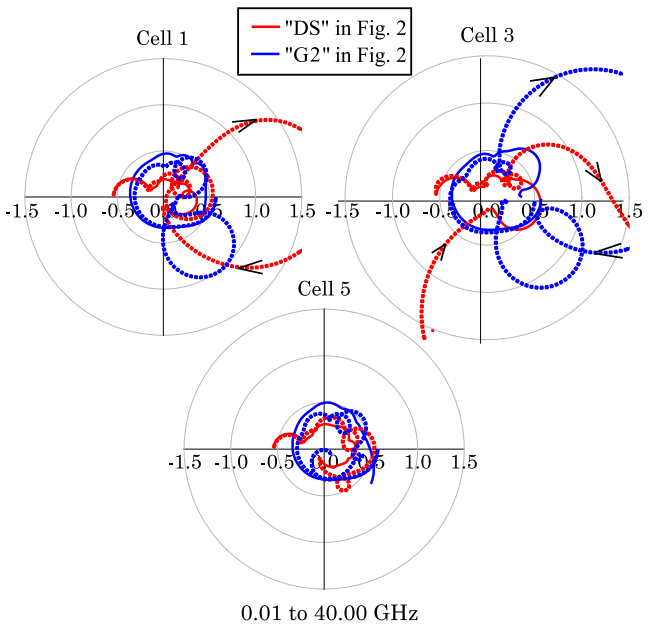

Fig. 3. Loop gain plots for the first, third, and fifth cells of the single-stage, five-cell DA EM-simulated without (dashed) and with (solid) the RC-feedback network. Before stabilization, only the fifth cell is stable.

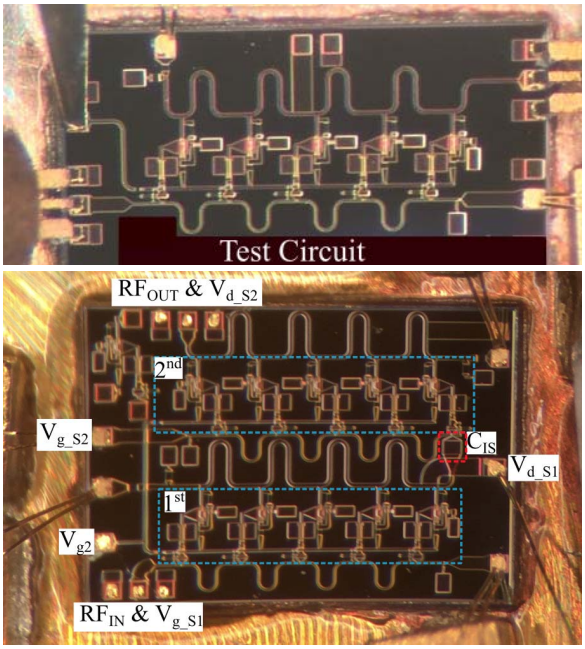

Fig. 4. Photograph of the 2.5 × 1 mm^2 single-stage (top) and 2.5 × 1.5 mm^2 two-stage (bottom) DA MMICs. Subscript "1" ("2") refers to the bonding pads of the first (second) stage. The V_{g2} voltage is shared on-chip between the two stages and is probed directly as in the top photograph. All dc pads except V_{g2} and V_{d_S1} are wire-bonded to 6.8-nF capacitors (C_{OFF} in Fig. 1). The V_{d_S1} pad is bonded to a 1.65-μH conical inductor via a 50-Ω series resistor.

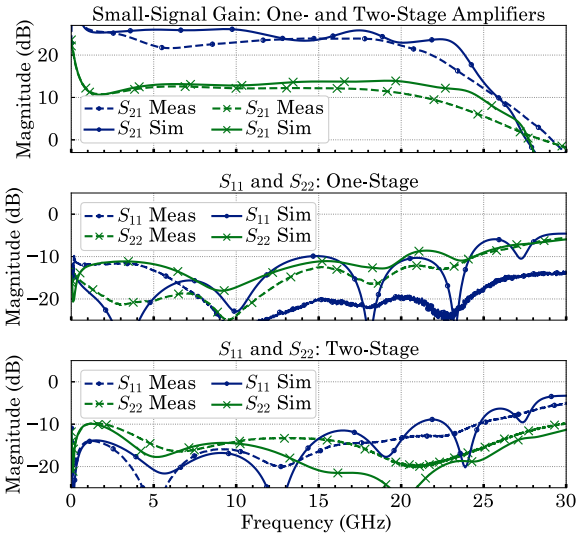

Fig. 5. Simulated (solid) and measured (dashed) small-signal response of one- and two-stage DAs. The S_{21} dip around 5 GHz for the two-stage design is due to the damped resonances in the off-chip first-stage supply network ("V_{d_S1}" in Fig. 4). The isolation is better than 32 and 60 dB for one- and two-stage designs, respectively. The bias point is $V_g \approx 0.7$ V and $I_{dq} \approx 190$ mA for one-stage design and for both stages of the two-stage circuit, with $V_d = 8$ V.

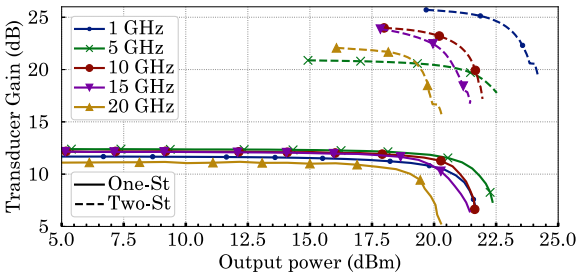

Fig. 6. Measured gain compression of one-(solid) and two-stage (dashed) DAs. The bias conditions are as in Fig. 5.

The output capacitance of the plain cascode cell is much smaller than $C_{gs}/2$ [17], also complicating the phase and impedance matching between the gate and drain lines. The RC-feedback stability network reduces the output impedance of each cascode cell, e.g., from $(114 - j601\ \Omega)$ to $(81 - j215\ \Omega)$ at 3 GHz, making gate and drain lines of the same characteristic impedance possible within fabrication process limitations. The equal gate and drain-line phase velocity condition gives initial estimates for inductances of $L_g = 500$ pH and $L_d = 650$ pH. The inductors are implemented as $Z_g = 94\ \Omega$ and $Z_d = 83\ \Omega$ high-impedance microstrip lines [Fig. 1(a)].

III. Measured Performance

Photographs of the measured one- and two-stage cascode DAs are shown in Fig. 4. The two-stage design consists of two identical five-cell DAs with an interstage capacitor C_{IS}. The chips are mounted on oxygen-free copper heatsinks.

The simulated and measured small-signal performance of the one- and two-stage DAs shown in Fig. 5 are in reasonable agreement. The bias conditions are given in the caption.

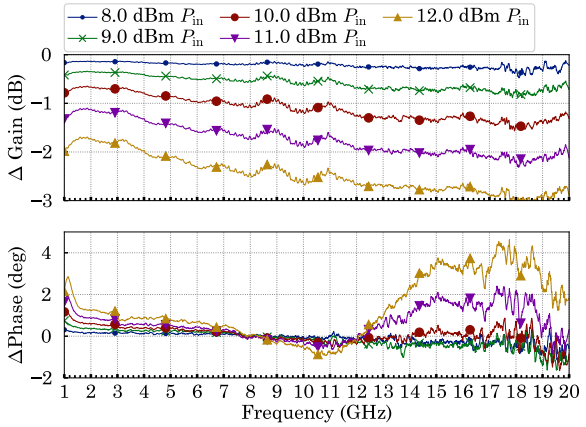

Fig. 7. Relative gain magnitude (top) and phase (bottom) measurements of the one-stage DA referenced to the response for $P_{in} = 7$ dBm. The bias conditions are as in Fig. 5.

TABLE I

Comparison of Multidecade GaAs Amplifiers. Power and Gain Are Averaged Across Frequency. Underlined Metrics Are the Best Among the Compared

Ref. [#]	Topology -	Mode E, D, E/D	BW (GHz)	$\overline{P_{max}}$ (dBm)	$\overline{\lvert S_{21}\rvert}$ (dB)	GBW (GHz)
[7]	NDPA	D	0-22	33.5	12	88
[8]	Cascode DA	D	0-40	19	13	179
[13]	Cascode DA	E/D	0-33	9	10	104
[11]	Triple Cascode	E	0.1-52	10	20	520
[12]	Cascode DA	D	0.1-40	23	17	283
This Work	**Two-Stage Cascode DA**	**E**	**0-22**	**21**	**23**	**311**

Large-signal characterization of the amplifiers is performed using a vector network analyzer, with its source and receivers power-calibrated to the on-wafer reference plane from 1 to 20 GHz. The available input power is swept from 0 to 15 dBm and from −5 to 5 dBm for the single- and two-stage circuits, respectively. The measured gain compression curves are shown in Fig. 6. The compressed gain and phase over frequency versus input power are presented in Fig. 7. We compare this work to previous results in Table I.

IV. Conclusion

In summary, we present one- and two-stage five-cell cascode DAs operating at 0.01–22 GHz. The E-mode GaAs process allows a single-polarity dc biasing network. A simple RC-feedback network in the CG transistor of the cascode pair provides stability in both simulations and measurements. The over-a-decade bandwidth MMIC DAs produce at least 20 dBm (≈30 mW/mm^2) of output power across the operating frequency range.

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