Broadband Supply Modulated PAs for Efficient and Linear Transmit Arrays

by

Connor Nogales

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Committee Members:

Gregor Lasser, Chair

Zoya Popović

Dragan Maksimović

Taylor Barton

Joshua Hawke

Christian Fager

Nogales, Connor (Ph.D., Electrical Engineering)

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Thesis directed by Prof. Gregor Lasser

Next-generation transmitters require large RF bandwidths, high effective isotropic radiated power (EIRP), broadband signals with a time-varying amplitude, and high power amplifier (PA) efficiency. Broadband architectures at the PA, antenna, and beamforming network achieve large RF bandwidths. Implementing PAs with high output power and high-gain antennas can achieve a high EIRP. However, signals with a time-varying envelope statistically operate most of the time at power levels backed-off from the peak. This substantially reduces PA efficiency, particularly for signals with a high peak-to-average power ratio (PAPR). By dynamically changing the drain supply of the PA, the efficiency can be improved, an approach known as supply modulation.

This thesis addresses the efficiency and linearity enhancement of PAs through dynamic discrete supply modulation. The hardware design and characterization of dynamic supply modulators and PAs suitable for an array of many active elements are investigated. The PAs in this thesis are designed to operate across a 6 GHz to 12 GHz bandwidth and amplify signals with an instantaneous bandwidth ranging from 10 MHz to 67.5 MHz. First, an overview of broadband supply modulation is presented. This thesis begins with the design of a 10 W GaN-on-SiC MMIC PA designed for high efficiency with a dynamic drain supply. The trade-offs between continuous and discrete supply modulation are discussed, and the modulated performance of this PA is examined through simulation.

One challenge identified is the PA's gain magnitude and phase dependence on supply voltage, which can degrade the linearity of supply-modulated PAs. Through load/source pull simulation and measurement of a fabricated 5 W GaN-on-SiC MMIC PA, it is shown that by deviating from conventional PA match for efficiency or output power and instead matching for low gain variation,

the PA's supply-modulated performance can be improved.

Additionally, a high-power discrete supply modulator is designed to generate a drain waveform suitable for many PA elements with a shared drain supply. Through careful selection of the switching transistors, this modulator achieves a peak output power of 800 W and a switching frequency of 10 MHz. Parasitics in the output trace interconnect and switching devices create significant ringing upon voltage level transition. The ringing is reduced by pulsing the gates of the transistors briefly before turning them on. This puts the transistors in a lossy state and dampens the ringing with a small cost to efficiency ($\sim$ 1% point).

Integrating a dynamic supply modulator with an active array is an additional challenge. For instance, the drain bias interconnect must have low inductance and capacitance to avoid low-pass filtering the dynamic drain signal. Additionally, broadband antennas are not always perfectly matched to 50 Ω and, therefore, can degrade the PA performance. These challenges are investigated through the dynamic supply measurements of a 4×1 antenna array with four commercially available GaN MMIC PAs supplied by an MMIC GaN supply modulator with a switching speed of 100 MHz. This thesis concludes with a summary of contributions and an overview of future work.

Dedication

To my parents and Sierra.

Acknowledgements

First of all, my advisors, Gregor Lasser, and Zoya Popović, deserve very special thanks for all the long hours they worked with me to get to this point. Thank you, Gregor, for all the time you spent pouring over my designs, data, and papers, along with always being available to meet and guide me through this Ph.D. journey. Without your guidance and support, I certainly would not be where I am today. Thank you, Zoya, for adopting me into your already large group of students, making sure I had funding through my whole Ph.D., helping me with my writing, and keeping the lab full of equipment to do interesting experiments, along with all the other incredible things she does for me and my colleagues.

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Introduction

1.1 Background and Motivation

From electronic warfare [4–6], to 5G multiple input multiple output (MIMO) arrays [1, 7], weather monitoring [8,9], automotive radar [10,11], satellite communication [12,13] and even gesture recognition [14] high-performing RF front-ends have a large and varied demand. They often operate in transmit and receive modes with a shared antenna element. A generalized block diagram of an RF front-end is shown in Fig. 1.1. On the transmit side, the baseband signal is generated digitally with a digital-to-analog converter (DAC) and up-converted through a mixer and local oscillator (LO). In the receiver, the modulated RF carrier is down-converted and sampled with an analog-to-digital converter (ADC). Filters are added to reject interference sources and image frequencies that result from the mixing operation. The modulated RF signal is amplified through a power amplifier (PA) in the transmitter and a low noise amplifier (LNA) on the receiver. Both the transmit and

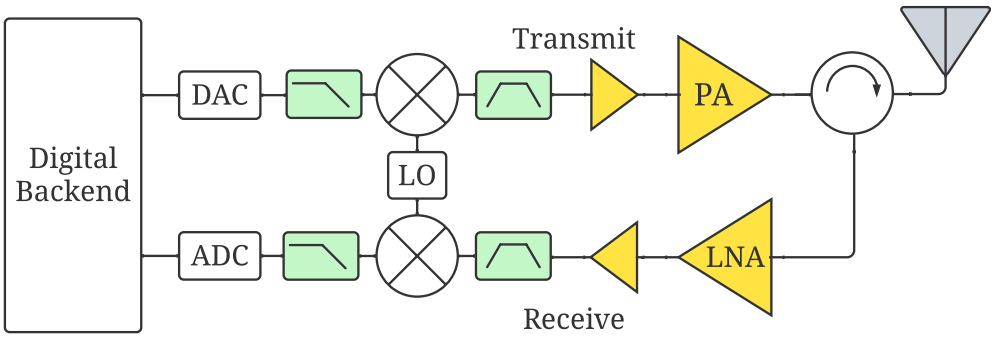

Figure 1.1: Generalized Transmit/Receive RF front-end module with a circulator to isolate the receive chain from the transmit chain.

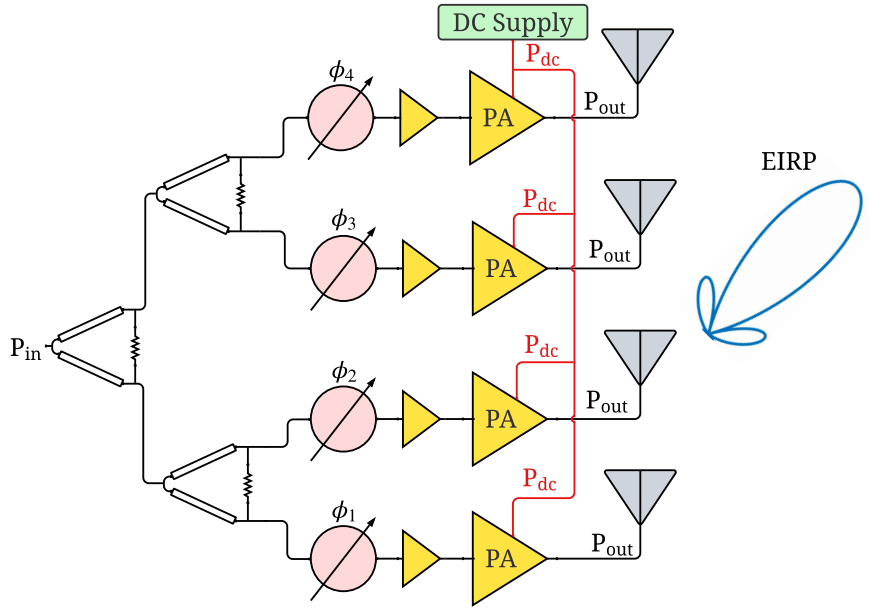

Figure 1.2: A 4x1 element active transmit array. The input signal is split four ways through symmetric Wilkinson dividers. The phase of each path is controlled with multiple phase shifters. Drivers are used to overcome losses in the beamforming network and saturate the PA elements.

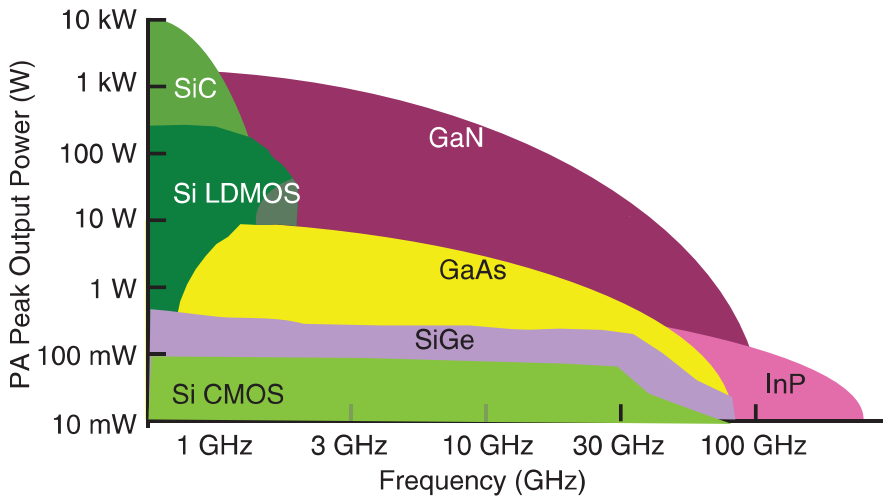

Figure 1.3: An overview of semiconductor device power handling vs. frequency. Figure adapted from [1, Figure 1, pg. 101]

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receive signals are present at the antenna but are isolated from each other using a circulator [15,16], switch, or combination of analog and digital isolation [17]. Additionally, the transmit and receive chains can be isolated by allocating different frequency bands, and using a diplexer filter [18].

RF front-ends are often connected to an array of antennas. The primary advantage of arrays

is increased gain and beam steering capabilities enabled by adding a progressive phase shift to the RF signal applied to each antenna element [19, 20]. Phased arrays are an important aspect of 5G communication systems. Digital beamforming enables multiple beams and spatial multiplexing, which can increase data rates in dense urban environments [21]. Additionally, in MIMO arrays, each element transmits and receives an independent stream of information [22]. This reduces the impact of fading and multi-path and can increase throughput [23]. The high effective isotropic radiated power (EIRP) also enables transmitters to overcome path losses, especially at mm-wave frequencies [1]. A block diagram of a four-element transmit array is shown in Fig. 1.2. The RF input signal is split through Wilkinson dividers and a phase shift is applied through phase shifters at the input of the PAs. The output power (P_{out}) from each PA element is combined spatially over the air through the antenna elements.

To meet the demands of high power, III-V semiconductors such as gallium-nitride (GaN) transistors are used due to their high band-gap and power handling properties [24, 25]. The advantage of III-V semiconductors can be seen in Fig. 1.3 adapted from [1, Figure 1, pg. 101], which shows the maximum power handling vs. frequency of different semiconductor technologies. For powers exceeding 1 W per element and frequencies between 2 and 100 GHz, GaN and GaAs semiconductors dominate. At higher powers and frequencies, thermal management becomes exceedingly challenging [1, 26]. In compact high-frequency arrays with many high-power PA elements for electronic warfare and satellite communication applications, the problem is exacerbated by reduced surface area, and temperatures can exceed 200°C [27, 28]. GaN-on-SiC technology can survive these high temperatures, however, insufficient thermal management can force transmitters to operate with reduced duty cycles to avoid device failure. Additionally, memory effects such as trapping are prevalent in GaN HEMTs and are affected by temperature. Trapping occurs when parasitic charge attaches to imperfections in the semiconductor lattice and affects the channel conduction [29]. The capture and release time of these traps is dependent on temperature [30]. Using DPD to linearize trapping effects in PAs is challenging when the temperature is dynamically changing. Thermal management techniques include forced airflow and liquid cooling pipes [27]. Additionally, analog

temperature sensing and bias compensation can be used to cancel out the gain and phase distortion due to changing temperatures [28].

In high-power transmitters, the dominant source of power dissipation is the final stage PA, quantified by efficiency, and the thermal issue can be addressed at its source by improving the PA efficiency. There are three commonly used definitions of PA efficiency: drain efficiency (η_{d}); total efficiency (η_{total}); and power added efficiency (PAE); defined as follows:

$$\eta_{\mathrm{d}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}}} \tag{1.1}$$

$$\eta_{\mathrm{total}} = \frac{P_{\mathrm{out}}}{P_{\mathrm{dc}} + P_{\mathrm{in}}} \tag{1.2}$$

$$PAE = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} \tag{1.3}$$

where $P_{\mathrm{out}} = GP_{\mathrm{in}}$ is the output power, P_{in} is the input power, G is the gain, and P_{dc} is the dc power applied to the PA. Each of these definitions includes the gain in different ways. The definition of drain efficiency does not include gain and is, therefore, the least conservative. The total efficiency includes the input power and gain; however, if the dc power is much larger than the input power, the total efficiency is dominated by the dc power consumption. The gain has a strong impact on the PAE which makes PAE a popular definition. For instance, if the gain is zero, the PAE is zero, which is not the case for the other definitions. As the gain of the PA increases, each of these definitions converges to the drain efficiency. Therefore, when analyzing the power dissipation in a PA, the drain efficiency definition will be used, and the PA is assumed to have a high gain. The power dissipation (heat generation) in a PA as a function of drain efficiency is shown below:

$$P_{\mathrm{diss}} = P_{\mathrm{out}} \left(\frac{1}{\eta_{\mathrm{d}}} - 1 \right) \tag{1.4}$$

The relationship between P_{diss} and drain efficiency is non-linear and plotted in Fig. 1.4a, in this example, $P_{\mathrm{out}} = 1\,\mathrm{W}$. At efficiencies greater than 40%, the power dissipation is not strongly affected

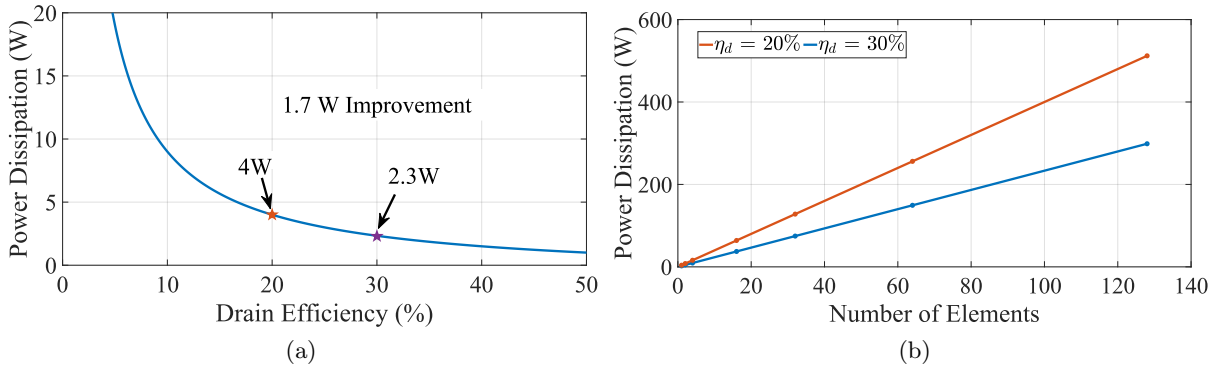


Figure 1.4: (a) Power dissipation vs. drain efficiency (η_{d}) for 1 W of output power. (b) Power dissipation vs. number of PA elements in a transmit array with a drain efficiency of 20% and 30%. The output power of each element is 1 W.

by improvements in efficiency. However, at low efficiencies, the power dissipation is a strong function of efficiency. For instance, improving the drain efficiency from 20% to 30% reduces P_{diss} from 4 W to 2.3 W, which is a 43% reduction. This improvement becomes even more apparent when scaling to multiple PAs in an array. Fig. 1.4b shows the power dissipation of an array as a function of the number of 1 W transmit elements with a drain efficiency of 20% and 30%. The power dissipation scales linearly with the number of elements, and as the number of elements exceeds 32, the difference in power dissipation resulting from the efficiency improvement becomes dramatic. These efficiencies and power levels are chosen to demonstrate how seemingly small efficiency improvements can have a dramatic impact on power dissipation.

When PAs amplify signals with a time-varying envelope, the overall average efficiency is lower than the peak efficiency. This is a fundamental issue in PAs and will be examined in more detail in section 1.2. There are several efficiency enhancement approaches to overcome this problem which will be discussed in section 1.3. The approach taken in this thesis is a technique known as supply modulation, also referred to as envelope tracking. A block diagram of a supply-modulated PA is shown in Fig. 1.5a. Here the dynamically changing drain voltage is generated with a supply modulator and applied to the drain bias of the PA. The drain voltage must be aligned with the input envelope signal so that when the input envelope drops, the drain voltage follows to continuously

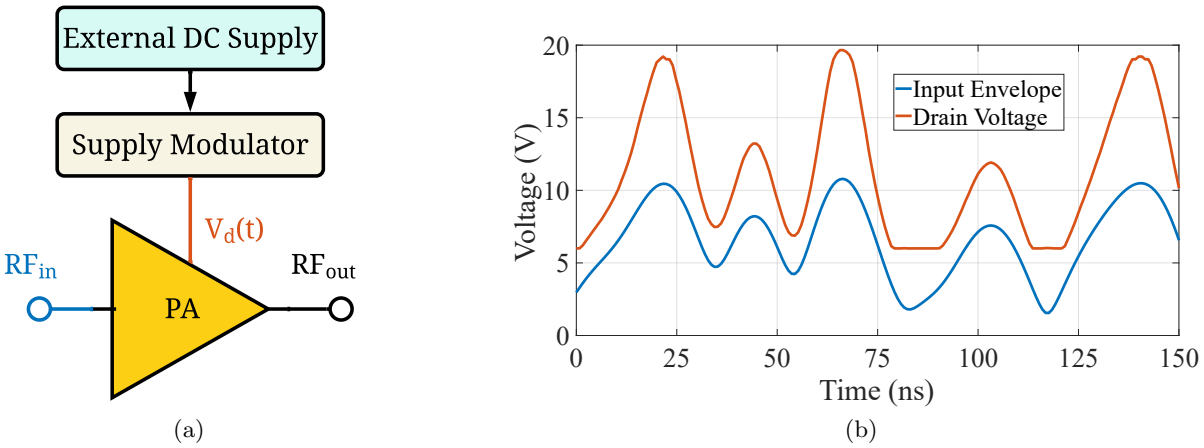


Figure 1.5: (a) Simplified block diagram of a supply modulated PA. (b) Time domain input and output signal envelope of a GaN on SiC MMIC PA amplyfing a 64-QAM 67.5 MHz signal with dynamic drain voltage.

saturate the PA. An example of the input envelope signals and the drain voltage is shown in the time domain in Fig. 1.5b with a 67.5 MHz 64-QAM signal. The drain voltage is generated for the 10 W GaN on SiC MMIC PA presented in chapter 2. The voltage range of the supply modulator is limited to operate between 6 V and 20 V.

1.2 Power Amplifier Overview

The objective of every PA is to amplify a signal to a higher power level. For communication, radar, and electronic warfare, high power is necessary to overcome free space losses [6]. However, PAs have applications in industrial heating [31], wireless power transfer [32], and many more. Some common challenges of PA design are high efficiency, high gain, high output power, and linear amplification. It is impossible to design a PA with optimal performance in each of these categories, so designers must make tradeoffs depending on the system requirements and the application [33]. The fundamental core of a microwave high-power PA is a transistor, which is typically in a common-source configuration with the source terminal connected to ground. The work presented in this thesis uses GaN high electron mobility transistors (HEMT) on a silicon carbide (SiC) substrate. The primary benefit of GaN-on-SiC transistors is the increased power capabilities enabled by the wide bandgap properties of GaN and the high thermal conductivity of SiC [24]. Some of the

disadvantages of GaN are soft compression and trapping effects which degrade linearity [34, 35]. A block diagram of a generalized single-stage PA is shown in Fig. 1.6a. The gate-source voltage modulates the conduction of the channel between the drain and source terminals. The gate and drain terminals are biased by a dc voltage. The input RF signal is applied to the gate, and the amplified signal is generated at the drain terminal. The transistor impedances at the gate and drain terminals must be matched to optimize the gain, efficiency, and output power. The output matching network (OMN) transforms the PA load impedance (typically $50\,\Omega$) to the desired impedance at the virtual drain/current source of the transistor. This typically means resonating out the drain-source capacitance and presenting a resistive load which maximizes efficiency or output power. This resistive load ensures that at the peak output power, the voltage waveform swings between the knee voltage (V_k) and twice the dc bias voltage (V_d) while the current swings from zero to the maximum current (I_max) which maximizes output power. Each of these parameters is shown in Fig. 1.6b along with the IV curves of a GaN HEMT and optimal load lines for different PA classes. At the gate, the complex input impedance of the transistor is conjugate-matched through the input matching network (IMN) to maximize the gain and minimize reflections. There are many different classes of power amplifiers, which are defined by the biasing of the transistor and the voltage/current waveforms at the drain terminal. Class-A is biased with a quiescent current (I_q) equal to $I_\mathrm{max}/2$. Class-B is biased with the gate voltage equal to the threshold voltage (I_q of zero). Class-C is biased with the gate voltage below the threshold voltage, and class-AB is biased with a quiescent current (I_q) in between class-A and class-B. Note that class-C and class-AB are defined across a range of bias points, while class-A and class-B are only defined for a single bias point. An in-depth discussion of all the classes of PAs is beyond the scope of this thesis, however, a class-B PA will be examined to illustrate typical PA behavior.

1.2.1 Class-B PA

Class-B PAs are biased with a positive drain-source voltage and the gate-source voltage equal to the threshold voltage of the transistor. The sinusoidal RF input voltage generates a half-wave

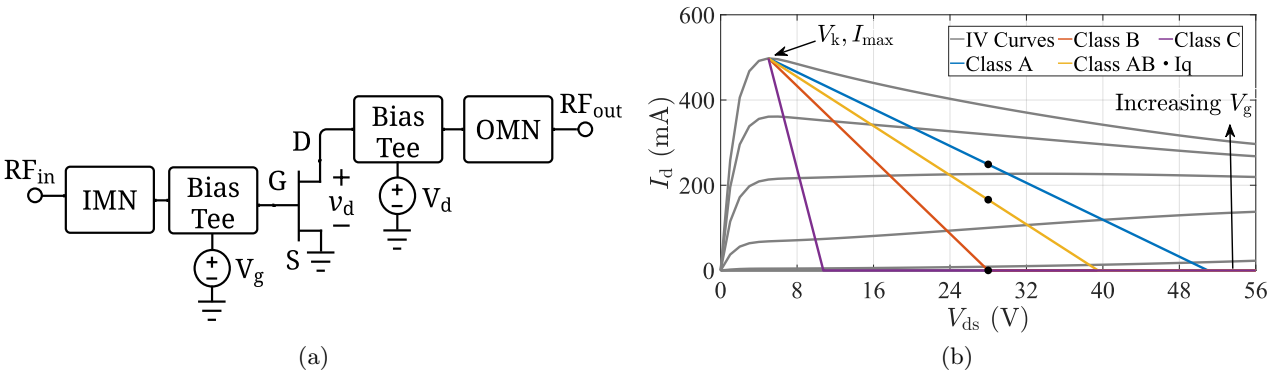


Figure 1.6: (a) basic PA schematic, (b) IV curves of a GaN transistor with load lines in class-A, B, AB, and C operation with $V_\mathrm{k} = 5\,\mathrm{V}$.

rectified current waveform and sinusoidal voltage waveform at the drain of the transistor, as shown in Fig. 1.7. For this analysis, a fixed dc drain bias (V_d) of 28 V is used, and the transistor maximum current (I_max) is set to 1.43 A. These values are chosen to produce 10 W of maximum output power. The maximum output power and optimal load resistance of a class-B PA are:

$$P_\mathrm{max} = \frac{V_\mathrm{d} I_\mathrm{max}}{4}, \tag{1.5}$$

$$R_\mathrm{opt} = \frac{2V_\mathrm{d}}{I_\mathrm{max}}, \tag{1.6}$$

where P_max is the maximum RF output power, V_d is the dc drain bias voltage, I_max is the maximum current a device can supply, and R_opt is the optimal load resistance presented to the transistor [33].

The voltage is centered at V_d and swings from zero to $2V_\mathrm{d}$ while the current peaks at I_max. The power dissipated at the drain can be found by multiplying the voltage and current, power dissipated at the drain is converted to heat and reduces the PA efficiency. These waveforms are only valid when the input voltage and gain produce drain waveforms that are less than or equal to $2V_\mathrm{d}$ and I_max. Increasing the input voltage beyond that clips the waveforms and generates harmonics, which can improve efficiency but will produce non-linearities. This analysis also assumes the transistor knee voltage is equal to zero and the impedance at all harmonics a short.

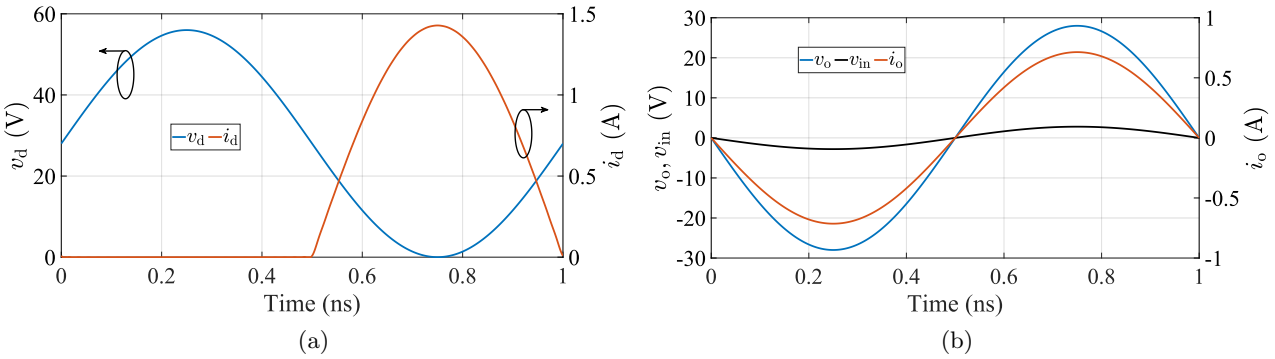


Figure 1.7: Instantaneous (a) drain and (b) input/output voltage and current waveforms for an ideal class-B PA at 1 GHz with a dc drain bias of 28 V and I_{max} of 1.43 A.

The RF output power is determined by multiplying the fundamental components of the drain voltage and current waveform, shown in Fig. 1.7b along with the input voltage. The dc power consumption is calculated by multiplying the average current and voltage on the drain. When the drain voltage and current swing across their full range, the drain efficiency is equal to 78.5%, which is the maximum efficiency from a class-B PA, assuming the waveforms are not clipping. Reducing the input power lowers the efficiency since the drain waveforms are not swinging across the full range. For this example, $V_d = 28\,V$, $I_{max} = 1.43$ A, $R_L = 39.2\,\Omega$, and $P_{max} = 10\,W$. The fundamental component of the output current is equal to the product of the input voltage and the transconductance ($I_{out} = g_m V_{in}$). The output voltage is the product of the output current and load resistance ($V_{out} = I_{out} R_L$). Therefore, the voltage gain is $G_v = g_m R_L$. For this example, g_m is set to 0.255 S and produces a voltage gain of 20 dB.

1.2.2 Communication and Test Signals

Most wireless applications such as communication [36], radar [37], and electronic warfare [38] require baseband modulation schemes. Although each application is important, this section will focus on communication signal modulation. Baseband signals have an instantaneous bandwidth (e.g., 67.5 MHz) and modulate RF carriers. The RF carrier can be anywhere inside the operational bandwidth of the PA (e.g., 6 GHz to 12 GHz). There are three fundamental methods of encoding

information in a baseband signal: frequency, phase, and amplitude [39]. Frequency and phase modulation schemes have constant envelopes, which allow the PA to operate at its peak efficiency point continuously. However, to increase the data transfer rate, these modulation schemes require more spectrum. Since spectrum allocation is expensive, most modulation schemes focus on maximizing information transfer while minimizing the signal bandwidth. The theory for maximum information transfer and minimizing errors through a channel with additive white noise was developed in the late 1940s by Claude E. Shannon [40, 41] resulting in the famous equation:

$$C = B \log_2 \left[\frac{S}{N} + 1 \right], \tag{1.7}$$

where C is the channel capacity, S is the power of the signal, N is the power of the noise, and B is the signal bandwidth. This equation shows that information transfer through a channel is dictated by the bandwidth and signal-to-noise ratio. As the signal power drops, the information becomes indistinguishable from white noise.

For digital baseband signals, each bit is encoded onto a complex signal at a fixed rate. The instantaneous amplitude and phase of the signal which corresponds to a sequence of bits, is referred to as a symbol. The number of bits per symbol increases with higher modulation orders. The frequency at which symbols are transmitted/received is called the symbol rate (baud rate) The bandwidth of the signal is proportional to the symbol rate. The instantaneous amplitude and phase of the complex signal can be visualized on a polar plot referred to as a constellation. For comparison, phase shift keying (PSK) and quadrature amplitude modulation (QAM) schemes are shown in Fig. 1.8.

PSK encodes information by modulating the phase of an RF carrier. The example shown in Fig. 1.8a has four constellation points, so it is called quadrature phase shift keying (QPSK) and transmits 2 bits per symbol. QAM signals consist of two amplitude-modulated components that are 90° out of phase and orthogonal when they are summed. These baseband signals are complex, with the in-phase (I) component consisting of the real part of the signal and the quadrature (Q)

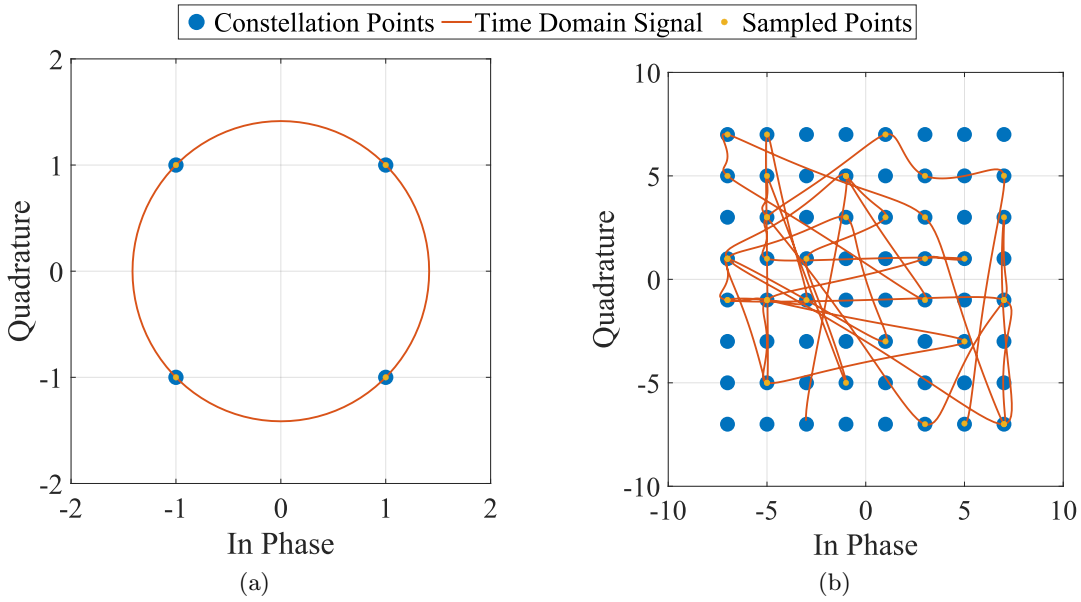


Figure 1.8: Comparison of (a) QPSK and (b) 64-QAM constellations. The constellation points are shown in blue. A small section of the baseband signal is shown in orange. Note that the magnitude of the baseband signal is constant for the QPSK signal and changes dynamically with the 64-QAM signal. The symbols in this segment of the signal are shown in yellow, and the time between each symbol is 20 ns, corresponding to a symbol rate of 50 MHz.

component being the imaginary part. The QAM signal shown in Fig. 1.8b has 64 constellation points, so it is referred to as 64-QAM and transmits 6 bits per symbol.

The QPSK modulation has a constant envelope, however, to achieve the same bit rate as the 64-QAM signal, the symbol rate of the QPSK signal would have to be three times greater which expands the bandwidth by a factor of three. However, the envelope of the 64-QAM signal is changing and has a peak-to-average power ratio (PAPR) greater than zero. Since the input power of PAs is typically scaled such that the peak output power of the PA corresponds to the peak input power of the signal, the PA must operate at reduced power levels and efficiency at all levels except the peak.

This effect is shown in Fig. 1.9 where the drain efficiency of an ideal class-B PA is plotted vs. output power with the PDF of a 64-QAM signal. Here the PA operates the majority of the time at backed-off power levels. The average power level is 7 dB backed off from the peak power, where drain efficiency is 35%, which is substantially lower than at the peak power level where drain

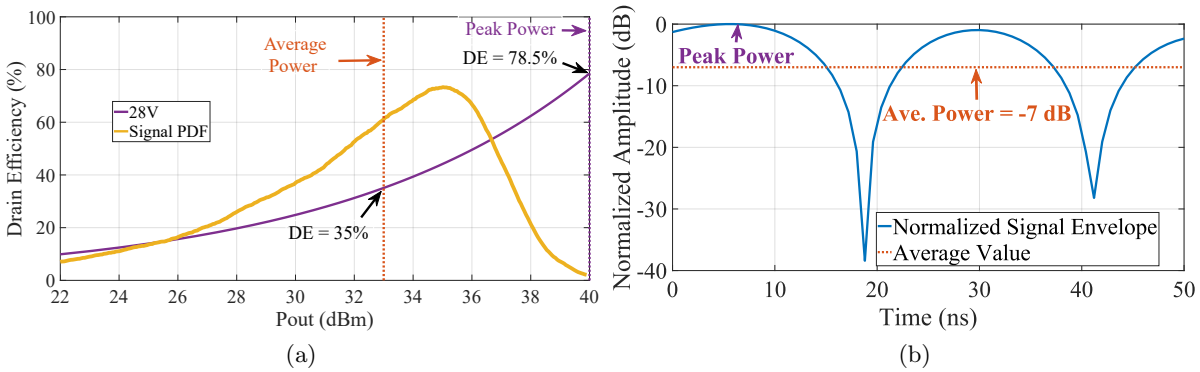


Figure 1.9: (a) Ideal class-B PA drain efficiency plotted vs. output power with a 64-QAM signal PDF. (b) normalized 64-QAM signal envelope.

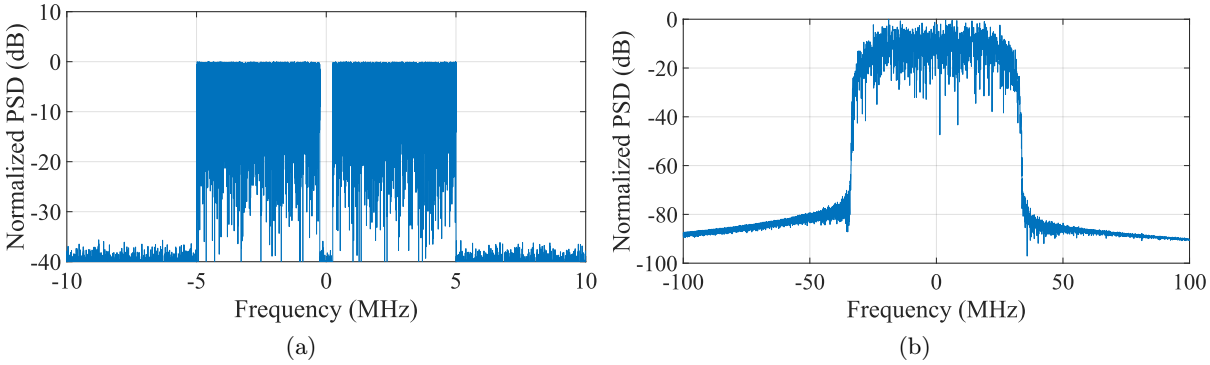


Figure 1.10: (a) 10 MHz NPR signals spectrum (b) 67.5 MHz 64-QAM signal with a baud rate of 50 Mega-symbols/s and roll-off factor of 0.35.

efficiency is 78.5%. The envelope of this signal is normalized and plotted in the time domain in Fig. 1.9b. For this example, the symbol rate is 50 Mega-symbols per second with a roll-off of 0.35 and bandwidth of 67.5 MHz. In some instances, the signal envelope drops to below 40 dB backed-off from the peak, at these points the drain efficiency is nearly zero. Higher modulation orders could be used with phase shift keying, however, the constellation points become so close together that they become susceptible to bit errors created by white thermal noise [40].

Two signal types are used in this thesis. The normalized power spectral density (PSD) is shown for both of these signals in Fig. 1.10. The first is a noise-like signal that consists of 30,001 random phase tones with equal amplitude placed inside a defined bandwidth, e.g., 10 MHz. A notch with 5% of the total bandwidth is placed in the center of the band, where the amplitudes of the

tones are set to zero. The non-linearities in the PA generate intermodulation products and produce spectral regrowth inside the notch. The ratio of the in-band power to the power in the notch is a measurement called noise-power ratio (NPR). This type of signal is also referred to as a noise-power-ratio (NPR) signal. The advantage of using an NPR signal is the amplitude statistics are similar to an orthogonal frequency division multiplexing (OFDM) scheme used in communication standards, but NPR signals are more general and do not require choosing a specific standard.

The second signal used is a 64-QAM signal. Each bit of a QAM signal must be encoded onto the amplitude of an in-phase and quadrature component. The simplest method of encoding this data is through multiple time domain pulses with different amplitudes. However, the frequency spectrum of a pulse is large. To reduce spectral content, time domain pulse shaping is adopted. An ideal time-domain sinc function would produce the minimum spectral content with zero inter-symbol interference (ISI). However, practical implementations produce expanded bandwidths due to the truncation of the sinc function, and in-accurate sampling timing will increase ISI due to the sharp edges of the sinc ripples. Therefore, a raised cosine filter is adopted to manage the spectral content while suppressing the time domain ripples [42]. It is often desirable to implement a matched digital filter on the transmitter and receiver, so root-raised cosine filters are a popular choice that, when cascaded together, give a raised cosine response [42, 43]. These digital filters are defined by a roll-off factor also called α. High roll-off factors suppress ripples but expand the bandwidth. Alternatively, low roll-off factors lower the bandwidth but can increase ISI due to the increased ripples. The bandwidth of a QAM signal B_{QAM} is defined by the Baud (symbol) rate and roll-off factor (α) defined as:

$$B_{\mathrm{QAM}} = Baud(1 + \alpha) \tag{1.8}$$

the roll-off factor ranges from zero to one. A roll-off factor of one corresponds to twice the signal bandwidth, and a roll-off factor of zero corresponds to a pulse shape of a sinc function in the time domain with a bandwidth equal to the baud rate.

The linearity of a QAM signal is quantified through two metrics; adjacent channel power ratio

(ACPR) and error vector magnitude (EVM). The ACPR metric is the ratio of the in-band power to the neighboring channel power. This is calculated mathematically by integrating the in-band and adjacent channel PSD. A guard band often separates the in-band channel and adjacent channel in the frequency domain to reduce interference. The frequency bounds of integration for the channel's PSD and the guard bands can be determined from a specific communication standard or through the roll-off factor of the QAM signal. In this thesis, the roll-off factor is used to determine the bounds of integration. The spectrum and adjacent channels of a 67.5 MHz QAM signal are shown in Fig. 1.11. Here the channel bandwidths are defined by the baud rate. The signal in Fig. 1.11 has a baud rate of 50 Mega-symbols/s, so the in-band channel bandwidth is 50 MHz. The roll-off factor of 0.35 expands the bandwidth to 67.5 MHz as expressed in (1.8). The guard band on the upper and lower channels is defined by this expanded bandwidth and is equal to 8.75 MHz.

The EVM quantifies how much error there is in de-modulated symbols of the baseband signal. If the EVM is too high, bit errors will occur, and the information will be corrupted. Mathematically, the EVM is the root-mean-square error of the in-phase and quadrature symbol components, normalized to the average power:

$$EVM = 100 * \frac{\sqrt{\frac{\sum_{i=1}^{N} (I_{\text{tx}}(i) - I_{\text{rx}}(i))^2 + (Q_{\text{tx}}(i) - Q_{\text{rx}}(i))^2}{N}}}{P_{\text{ave,tx}}}, \tag{1.9}$$

where I_{tx} and Q_{tx} are the in-phase and quadrature components of the transmitted (ideal) signal and I_{rx} and Q_{rx} are the components of the received signal, and $P_{\text{ave,tx}}$ is the average power of the transmitted signal. In practice, the phase and amplitude of the transmitted and received signals must be linearly scaled and aligned so that EVM calculation only accounts for non-linear distortion. For the EVM calculations in this thesis, the phase and amplitude are linearly scaled in software until the EVM is minimized. Additionally, the instruments used to generate the IQ signal, such as an arbitrary waveform generator or vector signal generator, can introduce phase and amplitude imbalance in the IQ signals. This imbalance is calibrated out by taking an initial measurement of the generated IQ signal, point by point computing the difference between the ideal and measured

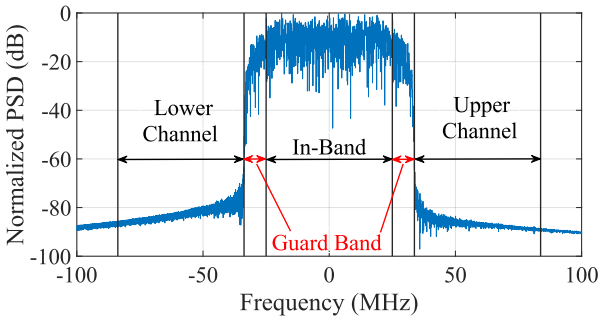


Figure 1.11: 67.5 MHz 64-QAM signal with a baud rate of 50 Mega-symbols/s and roll-off factor of 0.35. The channel bandwidths are 50 MHz wide, and the guard bands are 8.75 MHz wide.

signal, and subtracting this difference from the original signal and re-uploading the new signal. This is essentially a point-by-point digital pre-distortion used to linearize the instruments.

1.3 PA Efficiency Enhancement Techniques

When the input signal to a PA has a time-varying instantaneous power, the PA efficiency is reduced. This is observed in Fig. 1.9 and results from the drain voltage and current waveforms not swinging across their maximum range. There are several techniques to improve PA efficiency at reduced power levels, however, the most popular are load modulation and supply modulation (envelope tracking). Load modulation presents a dynamically changing impedance to the transistor, which ensures that the current and voltage waveforms swing across their maximum range at different input powers. The dynamic load lines of a load-modulated PA are shown in Fig. 1.12a. Ideally, load-modulated PAs have a fixed bias point but dynamically change the slope of the load line, increasing the impedance at lower power levels [44]. Load modulation architectures include the Doherty power amplifier (DPA), Chireix (Outphasing) amplifier, and load-modulated balanced amplifier (LMBA). Supply modulation dynamically changes the bias point of the transistor to improve efficiency. The dynamic load lines of a drain-modulated PA are shown in Fig. 1.12b. Ideally, drain-modulated PAs have a fixed load impedance but dynamically change the position of the load lines moving to lower drain voltages as the input power is reduced. The majority of published work on supply modulation focuses on modulating the drain bias for efficiency enhancement [45], however, there are examples

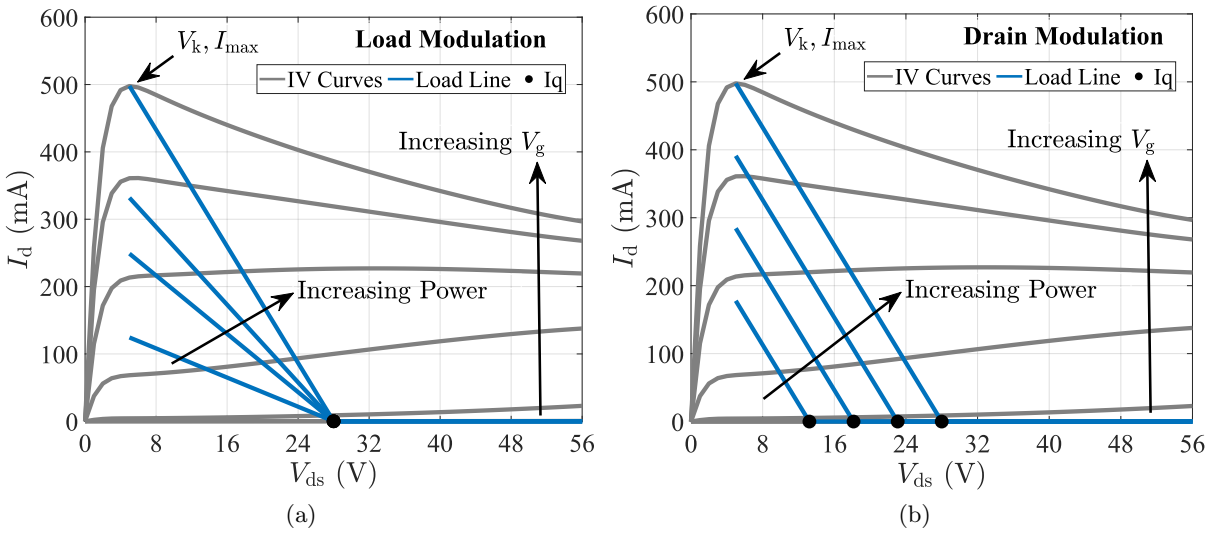


Figure 1.12: Example IV curves and load lines of a class-B PA with (a) load modulation and (b) drain supply modulation.

of gate bias modulation which primarily focus on linearity improvement [46, 47].

1.3.1 Doherty PA

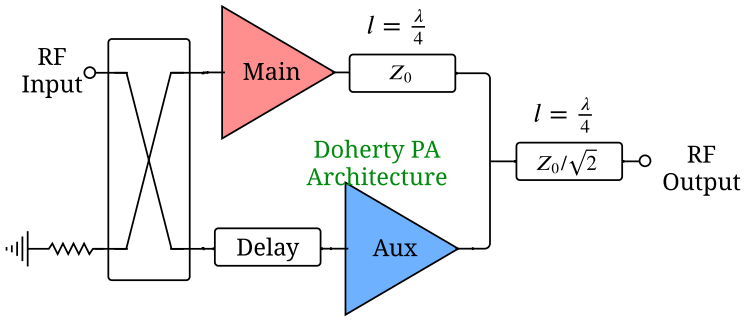


Figure 1.13: Block diagram of a Doherty PA

The block diagram of a Doherty amplifier is shown in Fig. 1.13, which consists of a main amplifier typically biased in class-B or AB and an auxiliary amplifier biased in class-C. The input RF signal is split between the main and auxiliary PAs. At low power levels, the main PA amplifies the signal, and the auxiliary PA is off. As the input power is increased, the auxiliary PA begins amplifying the signal, and load modulates the main PA, presenting a changing optimal resistance with drive power. A delay line is added at the input of the auxiliary PA to ensure that the

two amplifiers combine in phase at the output [48]. The drain efficiency of an ideal Doherty PA peaks at 6 dB backoff power, however, through asymmetric sizing of the main and auxiliary PA the peak backoff point can be moved to lower powers. For instance, sizing the auxiliary device to be four times larger than the main (1:4 DPA) causes the amplifier efficiency to peak at 12 dB backed off from the maximum power [49]. Furthermore, with multiple auxiliary PAs, the backoff efficiency can be improved such that multiple peaks in the efficiency occur referred to as a multi-stage DPA. The efficiency of a standard Doherty as well as a 3-stage and 4:1 Doherty PAs is shown in Fig. 1.14 (figure adapted from [2, Figure 3, pg. 561]) along with the PDF of an LTE and 802.11b signal. The primary limitations of the Doherty PA are the bandwidth and linearity. The bandwidth is limited due to the impedance inverter on the output, which is typically implemented as a quarter wave transformer [50]. Practical implementations have significant AM-AM and AM-PM distortion [51, 52], which is often corrected through digital pre-distortion (DPD).

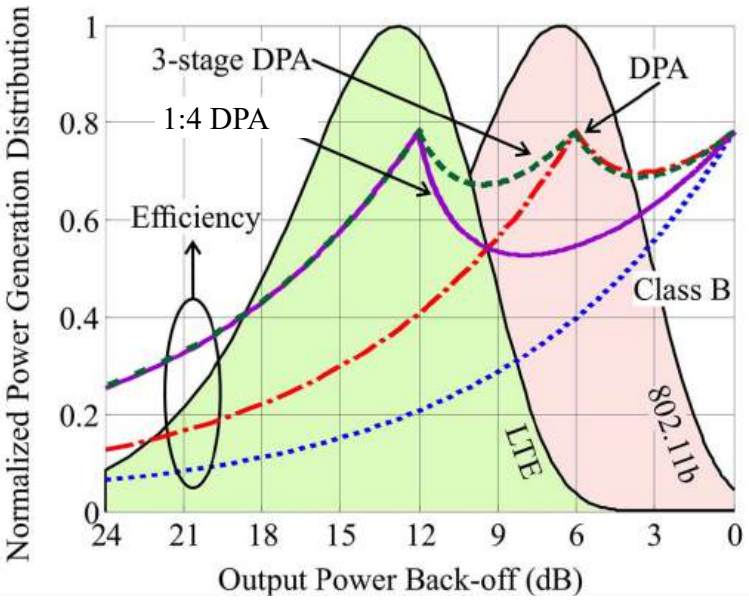


Figure 1.14: Efficiency of two-stage, three-stage, and 4-way Doherty PAs with the PDF of LTE and 802.11b signals vs. output power. Figure adapted from [2, Figure 3, pg. 561]

1.3.2 Outphasing PA

The block diagram of an outphasing PA is shown in Fig. 1.15 and consists of two saturated PAs with a modulated input phase and combined through a power combiner. If the power combiner is isolated, this PA has a linear amplification using non-linear components (LINC) architecture. If the power combiner is non-isolated, allowing for load modulation, the architecture is Chireix. In outphasing PAs, the output power is controlled by changing the relative phase between the amplifiers. If a Chireix architecture is adopted, the two PAs load modulate each other through the output combiner [53]. Outphasing PAs can achieve large RF bandwidths with a high backoff efficiency [54]. One challenge with outphasing PAs is maintaining high efficiency deep in back off, particularly when the signal amplitudes go to zero. In such cases, a mixed-mode operation can be adopted where both the amplitude and phases are modulated. When the input signal power drops, the RF amplitude applied to each outphasing PA is reduced to minimize the dc power dissipation. An additional challenge of outphasing PAs is the bandwidth expansion resulting from the non-linear operation of converting amplitude information into outphasing angles of the two branches [53]. This obstacle can be overcome through an inphasing network that operates in the analog domain and uses non-linear elements to convert amplitude information into an outphasing angle [55].

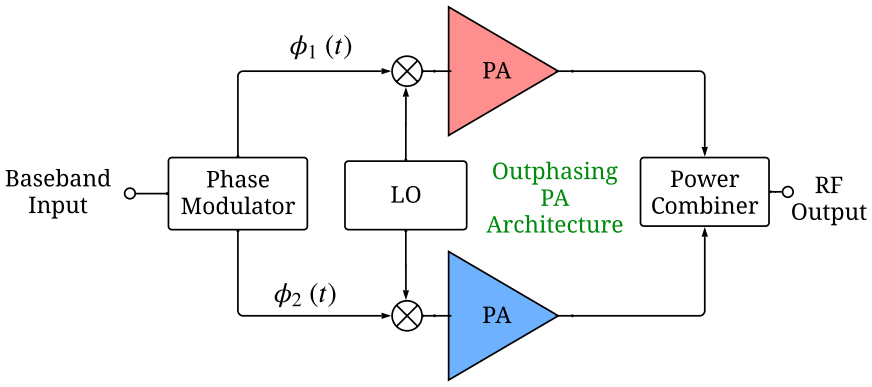


Figure 1.15: Block diagram of an outphasing PA. Here the power combiner can be isolated (LINC) or non-isolated (Chireix).

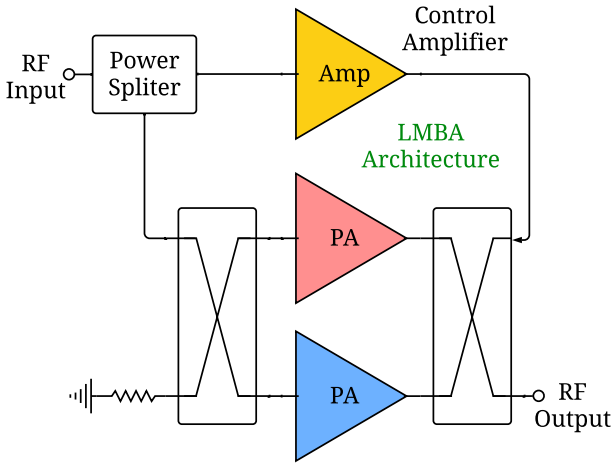


Figure 1.16: Block diagram of a LMBA

1.3.3 Load Modulated Balanced Amplifier

The block diagram of an LMBA is shown in Fig. 1.16 and consists of two PAs in a balanced configuration with a third amplifier injecting a control signal into the isolated port of the output coupler. The control amplifier load modulates the balanced amplifiers to maintain efficient operation as the signal power changes. The LMBA has many advantages over the Doherty PA; it supports larger bandwidths, eliminates the delay lines, and has a higher degree of reconfigurability [56]. Broadband examples of LMBAs have been demonstrated [57,58], which split the input RF signal to the control and balanced amplifiers, thus eliminating the need to independently operate the control amplifier.

1.3.4 Supply Modulation

An alternative to load modulation techniques is supply modulation, where the drain or gate bias of the PA is dynamically changed to follow the signal envelope and improve efficiency or linearity. The work in this thesis focuses on drain modulation, so the terms drain modulation and supply modulation will be used interchangeably. A block diagram of a supply-modulated PA is shown in Fig. 1.17. The working principle of supply modulation can be seen in Fig. 1.18 which shows the drain efficiency of a class-B PA at drain voltages from 14 to 28 V along with the PDF

of a 64-QAM signal with a PAPR of 7 dB. With a static supply of 28 V, the efficiency drops to 35% at 7 dB of back off (OBO). However, by reducing the drain voltage to 14 V, the efficiency can be improved to 70%. By dynamically changing the drain voltage to follow the instantaneous input power, the overall efficiency of PAs can be improved [46, 59–65]. The modulated input RF signal is split between the input of the PA and an envelope detector. The signal envelope is applied to a controller, which determines the instantaneous output voltage (V_{d}) of the supply modulator. The drain voltage and RF input signal are aligned using a delay at the input of the PA. The drain voltage to input power relationship is referred to as a shaping function and can be used to maximize efficiency, linearity, or a compromise between them [59, 66]. The shaping function will be explained in more detail in the following chapter. An advantage of supply modulation is that it is carrier frequency agnostic, meaning the RF operating frequency and bandwidth of the PA have no impact on the supply modulator. Additionally, if existing front-end transmitters need improved efficiency, they can be retrofitted with supply modulation, assuming the drain bias lines have low inductance and capacitance. Furthermore, if the modulator and PA are thermally de-coupled, even a low-efficiency modulator can improve the heat dissipation of the PAs. The baseband bandwidth is typically limited by the supply modulator. Many publications focus on improving the bandwidth of supply modulators [67–70] or reducing the bandwidth of the envelope signal [59, 71, 72]. One technique to track higher signal bandwidth is to discretize the continuous drain signal into a fixed number of voltage levels [61–63, 73]. The discrete drain signal low-pass filters the envelope, so relatively low bandwidth supply modulators can track high bandwidth signals.

Supply Modulation Diagram

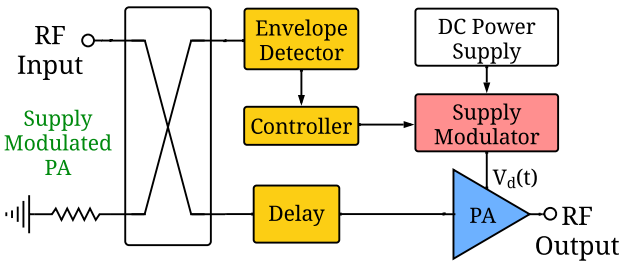


Figure 1.17: Block diagram of a supply modulated PA

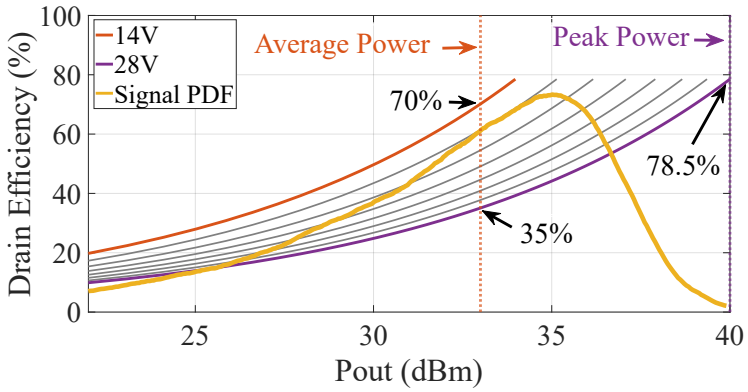


Figure 1.18: Drain efficiency (η_d) of a class-B PA at multiple drain voltages with the PDF of the envelope of a 64-QAM signal.

Additionally, combined supply modulation and load modulation have been demonstrated for the Doherty PA [74–77], outphasing PA [78], and LMBA [79].

Ongoing research in supply modulation has many subjects, but three will be addressed in this thesis. The first is system linearization through PA design methods in chapter 3 [80–82]. The second is the design of supply modulators for improved bandwidth, output power, linearity, and efficiency in chapters 4 and 5 [70,73,83–87]. The third subject is scaling a supply modulated system to multiple PAs in an array demonstrated in chapter 6 [88–92].

1.4 Thesis Organization

Supply modulation has been the topic of research dating back to the 1950s [93], but there are few studies on supply modulation in the context of a transmit array with multiple PA elements. This thesis investigates the design and characterization of the PA and supply modulator in a broadband supply modulated transmit array operating from 6 GHz to 12 GHz.

One challenge at the PA level is that GaN PAs exhibit an expansive gain magnitude and phase with increasing drain voltage. This can degrade linearity when the drain bias is dynamically changed [80–82, 94–96]. A study of the gain magnitude and phase dependence on drain voltage is performed across different source/load impedances and applied to a GaN MMIC PA design in chapter 3. By reducing the gain dependence on drain voltage, the distortion created by ringing and bandwidth limitations in the high power supply modulator can be reduced.

Supply modulating each PA in an array with an individual modulator adds substantial complexity to a system, especially with a large number of PA elements. An alternative is to feed the entire array or sub-array with a single high-power modulator [83, 88–90, 92]. The design of a discrete four-level supply modulator with a peak output power of 800 W is presented in chapter 5. A major challenge of high-power supply modulators is the tradeoff between switching speed and power handling. This is investigated through a survey of different commercially available transistor technologies and manufacturers to find the optimal device selection for this application. The fabricated high-power supply modulator has four discrete voltage levels and utilizes GaN transistor switches. This discrete supply modulator exhibited significant ringing upon voltage level transition, which can degrade PA linearity and efficiency [3]. The ringing is accurately predicted by modeling the parasitics of the output trace interconnect using RLC elements in chapter 4. Additionally, an active technique to reduce the ringing is introduced and investigated in chapter 5.

When the PA and supply modulator are integrated into an array, there are additional challenges. For instance, the drain bias interconnect feeding each PA must be as short as possible to minimize inductance and capacitance, which filter the dynamic drain voltage. Furthermore, antenna arrays can present a mismatch to the PAs that depends on the element location and scanning. Element variation can be exacerbated by a non-uniform delay in the drain signal and beam steering. Chapter 6 investigates these challenges through the efficiency and linearity measurements of a 4×1 ridge horn array fed by four GaN PAs with a dynamic drain voltage.

By investigating these topics and adding to the literature, this thesis aspires to illuminate new paths forward to achieving an efficient and linear RF transmitter. This thesis is organized as follows:

- Chapter 1 introduces the fundamental concepts of this thesis, including PA design, baseband signals, and power amplifier efficiency enhancement techniques.
- Chapter 2 gives an overview of a broadband supply modulated system, presenting the design of a 10 W MMIC PA operating from 6 GHz to 12 GHz, discussing the trade-offs

between continuous and discrete supply modulation, and giving an example of how the instantaneous drain voltage and RF input power are related.

- Chapter 3 investigates how the gain magnitude and phase variation across the drain voltage of PAs impact the efficiency and linearity with a dynamically changing supply. A technique to minimize the gain variation is presented, which mismatches the source/load impedance and is experimentally validated through the design and characterization of a 5 W MMIC PA operating from 6 GHz to 12 GHz.

- Chapter 4 presents the design and characterization of a high-power four-level supply modulator designed for a peak output power of 1 kw at 20 V and a maximum switching speed of 10 MHz.

- Chapter 5 introduces a new technique to reduce transient ringing in discrete supply modulators by pulsing the gate of the transistor switches.

- Chapter 6 presents the design and measurements of a 4×1 active array with a shared dynamic drain voltage applied to the four 2 W GaN PAs. The efficiency and linearity of this transmitter are presented when the PAs are loaded with the antenna array and with 50 Ω terminations. These results are compared to measurements of a single supply modulated PA.

Chapter 2

Broadband Supply Modulated PA System Aspects

2.1 Introduction

The previous chapter introduced a fundamental challenge consistent throughout this thesis: the average efficiency is reduced when PAs amplify signals with a time-varying amplitude. The proposed solution is a technique known as supply modulation, which was introduced in chapter 1. Supply-modulated systems consist of a PA, which amplifies a modulated carrier in the RF domain, and a supply modulator, which follows the signal envelope in the baseband domain. One advantage of supply modulation is that the supply modulator does not impose limitations on the system's RF bandwidth. Thus, supply modulation can be applied to a broadband RF PA with the modulated RF carrier operating anywhere inside the PA's RF bandwidth. This makes supply modulation an attractive solution for the efficiency enhancement of broadband frequency agile transmitters. In the baseband domain, the upper limit on signal bandwidth is determined by the transient speed/bandwidth of the supply modulator. Therefore, it is desirable for supply-modulated systems to have a high RF and baseband bandwidth to support broadband signals and operate over a large portion of the RF spectrum. Additionally, the efficiency of the PA and supply modulator drops as the bandwidth increases, so this tradeoff must be considered in the design process. This chapter examines a broadband supply modulation system. First, a broadband PA design is introduced. Second, two supply modulator architectures are examined in terms of efficiency and bandwidth. Third, it is demonstrated that the relationship between instantaneous input power and drain voltage can be tailored to improve system efficiency, linearity, or a compromise of the two.

2.2 Broadband PA Design and Non-linearities

This section investigates a broadband PA design specifically targeting high efficiency in a supply-modulated system. The beginning of the section discusses an approach to high-efficiency PA design in which the drain voltage and current are shaped to minimize power dissipation in the PA. Next, the design and characterization of a high-efficiency GaN-on-SiC MMIC PA is presented.

2.2.1 Waveform Engineering

The efficiency of an RF transmitter is dominated by the final stage PA. Therefore, designing high-efficiency PAs is critical. The ideal class-B PA presented in chapter 1 has a maximum drain efficiency of 78.5%. This efficiency is achieved when the current and voltage waveforms peak at the maximum current and twice the dc drain voltage. The efficiency can be improved by increasing the drive power and overdriving the PA. In this mode of operation, the voltage/current waveforms clip, and the PA begins to saturate. This generates harmonic content, which can improve efficiency through proper impedance termination, known as waveform engineering [97]. A classic example of this is the class-F PA. The drain current and voltage waveforms of an ideal class-F PA are shown in Fig. 2.1a. For this example, the dc drain voltage is 28 V, and the maximum drain current ($I_{\max}$) is 1.43 A. These values are chosen to be consistent with the class-B example in section 1.2.1. class-F PAs are typically biased with a reduced conduction angle similar to that of class-B or AB. The virtual drain of the device is terminated with a short circuit at the even harmonic frequencies, and at the odd harmonic frequencies terminated with an open circuit [33]. This results in a square-shaped voltage waveform and a half-wave rectified current waveform. With an infinite number of harmonics, there is no overlap between the voltage and current waveforms at the drain of the PA, and no power is delivered to the harmonics since the impedance is either a short or an open circuit. Therefore, efficiencies up to 100% are possible in the ideal case [98].

In practice, transistors do not have gain up to infinite harmonics. The output capacitance of the device presents a short circuit at higher frequencies, so only a limited number of harmonics

can be used. For instance, if up to the 3rd harmonic is terminated for maximally flat waveforms and the rest are a short circuit, the current and voltage waveforms overlap as shown in Fig. 2.1b. The drain efficiency derived from these waveforms is 75% [98]. Note that this is lower than the ideal class-B PA. However, the current waveform in an ideal class-B PA includes infinite harmonics in the current waveform. This analysis ignores the knee voltage, which will reduce efficiency and generate additional harmonics [33].

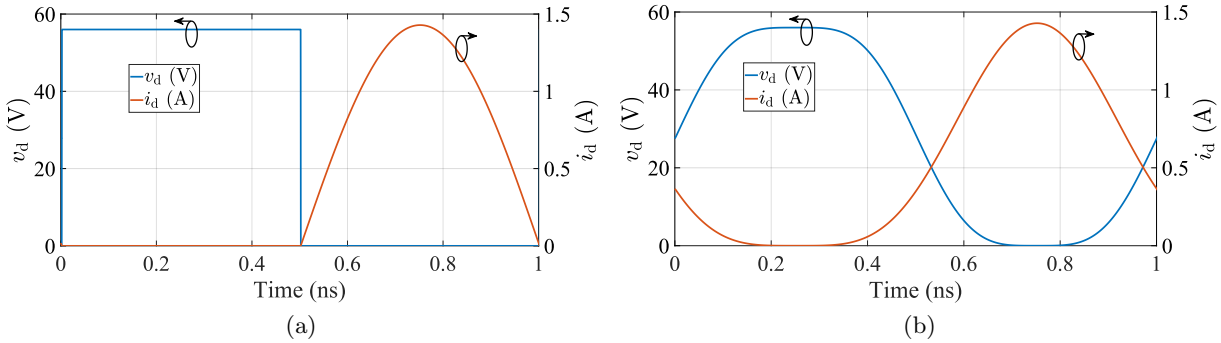


Figure 2.1: Drain voltage and current waveforms of a class-F PA with (a) an infinite number of harmonics optimally terminated and (b) up to the third harmonic terminated for maximally flat waveforms. For this example the dc drain voltage is 28 V and the transistor maximum current is 1.43 A.

In broadband PAs, ideal class-F waveforms are impossible to achieve due to the overlap between fundamental and harmonic terminations. For example, if a PA has an octave of bandwidth, operating from 1 GHz to 2 GHz. At a fundamental frequency of 1 GHz, the second harmonic is 2 GHz. However, the PA is also designed to be operated at a fundamental of 2 GHz. Here, the fundamental frequency match must be prioritized over the harmonic termination. Therefore, the PA will not operate with ideal class-F waveforms at 1 GHz. An analysis of PA performance across a range of harmonic impedances is shown in [99]. In practice, the operating class of broadband PAs is somewhere between a class-F and an overdriven class-A PA. Therefore, an overdriven class-A PA will be examined next.

2.2.2 Overdriven class-A PA

class-A PAs are biased with a quiescent current equal to half the maximum current ($I_{\max}$). The drain current and voltage waveforms are shown in Fig. 2.2. The voltage waveform is centered at the dc drain voltage (V_{d}), and the current waveform is centered at the quiescent current. When the drain waveforms swing across their maximum values without clipping, the drain efficiency is 50%, and the waveforms are shown in Fig. 2.2a. If the input power is increased, the PA saturates, and the waveforms clip. This increases the efficiency but reduces the gain, a phenomenon known as

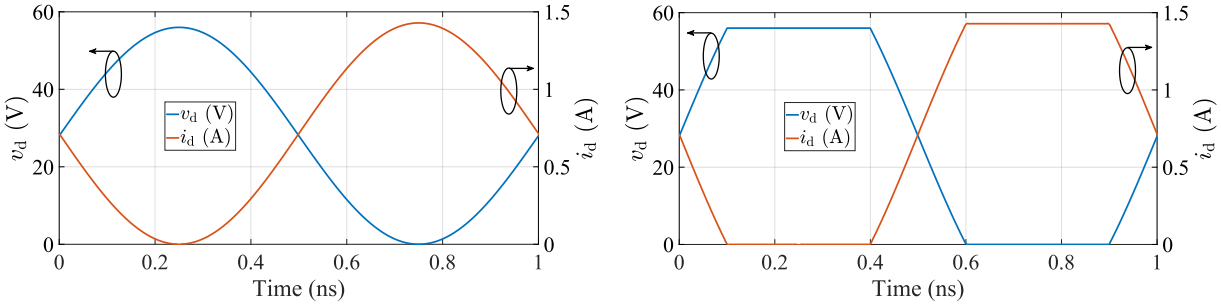


Figure 2.2: Overdriven ideal class-A PA drain waveforms operating at 1 GHz. (a) Waveforms when the PA is driven to its maximum without clipping. (b) Waveforms when the PA is driven 3 dB into compression.

gain compression. The drain waveforms at the 3 dB gain compression point are shown in Fig. 2.2b. By operating the PA 3 dB into compression, the PAE is improved to 70% from 50%. The peak drain efficiency of an overdriven class-A PAs is 81%, which is lower than a class-F PA with infinite harmonics because power is being delivered to the harmonics [33]. This analysis is performed similarly to the class-B analysis in section 1.2.1 with the drain waveforms decomposed into a Fourier series to determine the dc power dissipated and RF power delivered to the load [33]. The difference occurs when the PA is overdriven. Here ideal clipping is applied to the voltage waveform so it does not exceed $2V_{\mathrm{d}}$ or drop below zero following the analysis in [33]. This analysis omits transistor effects such as the knee-voltage, gate diode forward biasing in GaN HEMT's, and the non-linear transconductance. The current waveform is reconstructed from the voltage

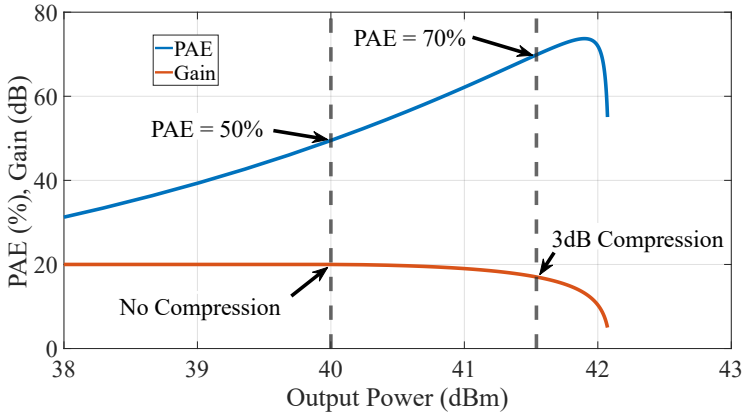


Figure 2.3: PAE and gain of an overdriven class-A PA plotted vs. output power.

assuming the impedance is terminated with an R_{L} of $39.2\,\Omega$ at the fundamental frequency and all harmonics. For this analysis, the drain voltage is $28\,\mathrm{V}$, and the quiescent current is $0.71\,\mathrm{A}$. The PAE, gain, and output power are calculated from the waveforms and plotted in Fig. 2.3. The peak efficiency point occurs when the PA gain is in compression. This is common to most PAs and can produce high efficiencies; however, the output signal is no longer linearly related to the input signal, generating non-linear distortion. When amplifying a communication signal, this distortion degrades error vector magnitude (EVM) and generates intermodulation products which increase ACPR [33]. Furthermore, this analysis neglects the phase distortion caused by the non-linear input/output capacitance and non-linear transconductance, which are dependent on input power and create additional distortion in the baseband signal. This could be included in the model by adding a power-dependent complex component to the transconductance [100]. The distortion can be compensated by pre-distorting the input signal to cancel out the non-linearities of the PA. This can be done in the analog [101,102] or digital domains [103,104]. The tradeoff between PA linearity and efficiency is a subject that will be discussed throughout this thesis but is addressed directly in chapter 3.

2.2.3 Broadband MMIC PA Design and Characterization

The waveform engineering discussed previously is challenging to apply across a large RF bandwidth. For instance, non-ideal transistors have parasitic inductance, capacitance, and resistance, which the output-matching network must match to present the appropriate impedance at the intrinsic transistor drain. However, there are limits on the bandwidth over which a reactive impedance can be matched, known as the Bode-Fano limit [105, 106]. Furthermore, the frequency-dependent reactance is challenging to match accurately over a large bandwidth. Therefore, the load impedance presented to transistors through the OMN often deviates from the optimum case at the fundamental and harmonic frequencies. Additionally, the transistor parasitics make it difficult to de-embed to the plane of the intrinsic gate and drain. Therefore, designers adopt a load/source pull approach. In a load pull analysis, the performance of the PA is measured or simulated with different drain-side load impedances. Load pull is typically performed for the fundamental load impedance and the harmonics. In source pull, the gate-side source impedance is swept. This is typically performed only at the fundamental frequency. If the device is bilateral, meaning there is feedback from the gate to drain, this process is interactive, performing multiple load/source pull sweeps. Designers can choose impedances that optimize PAE, output power, gain, or a tradeoff between them.

The design and measurement of a broadband high-efficiency MMIC PA will now be described to illustrate techniques used throughout this thesis. The PA is designed in the WIN Semiconductors NP15 150 nm GaN on SiC process. The target RF bandwidth is 6 GHz to 12 GHz with an output power of 10 W at a drain voltage of 20 V and the highest possible efficiency across multiple drain voltages.

For supply-modulated PAs, load pull is performed at multiple drain voltages. The PAE contours of a $20\times100\,\mu$m transistor at 9 GHz in the WIN Semiconductors NP15 process are shown in Fig. 2.4 at drain voltages of 6 V, 15 V, and 20 V. The simulations are performed using the foundry nonlinear model, which was under development when this PA was designed. The maximum PAE

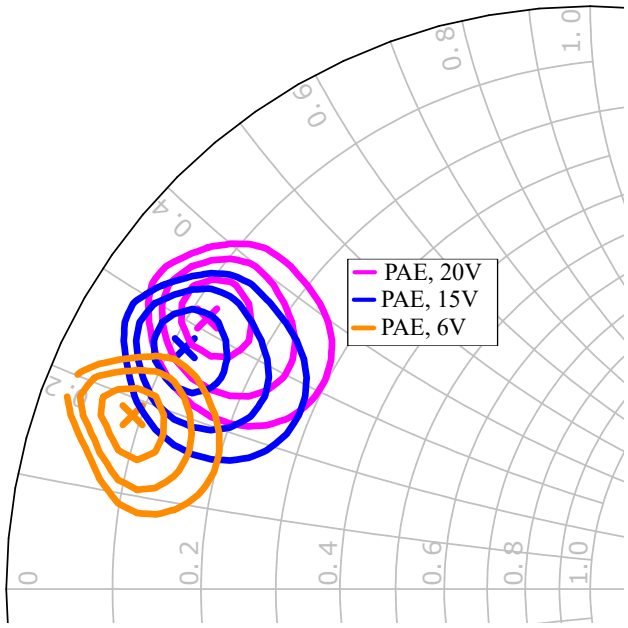


Figure 2.4: Load pull of $20\times100\,\mu$m device at drain voltages of 6, 15, and 20 V and 9 GHz each with a maximum PAE of 69.8%, 70.0%, and 69.3%, respectively. The contours are in 5% steps referenced to the maximum PAE at the center of each contour.

impedance changes at different drain voltages. The primary cause of this is the changing optimal resistance according to Eq. 1.6 and the non-linear output capacitance, which is a function of drain voltage. As the drain voltage is changed, the load impedance presented to the transistor is fixed. The drain voltage of supply-modulated PAs follows the instantaneous input power. Typically this results in the PA operating at the highest drain voltage at the peak input power, the lowest drain voltage deep in back-off, and at medium drain voltages in between. Statistically, most signals have a higher probability of operating at medium or low power levels than at high power levels. Therefore, the PA will be operating at medium or low drain voltages the majority of the time. This PA was originally designed to operate with a drain voltage from 10 V to 20 V, so to maximize the efficiency, it was matched at a drain voltage of 15 V where it will be operating the most.

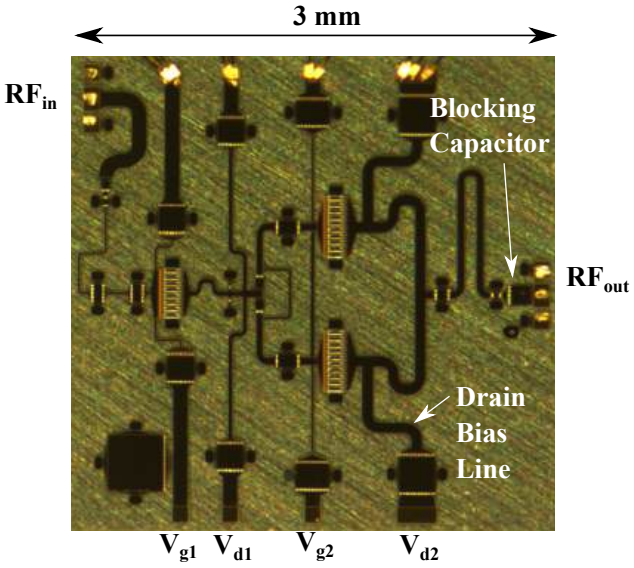
This design uses lumped element inductors and capacitors to match the PA reactively. The input impedance is modeled as a series RC circuit, which is conjugate-matched. The chosen load impedance is conjugated and converted to an equivalent parallel RC circuit, which models the transistor's optimum load resistance and output capacitance [107]. The input and output RC

circuits are initially matched using ideal series inductors and shunt capacitors. A shunt inductor and series capacitor are also inserted into the network, to form a bias tee and are used as additional matching elements. The realized second stage drain bias line and blocking capacitor are labeled in the MMIC photo shown in Fig. 2.5a. A schematic of the PA matching networks is shown in Fig. 2.5b. For a supply-modulated PA, the bypass capacitance on the drain bias line must be minimized to avoid filtering the dynamic drain signal, however large enough to ensure stability. Inductors are implemented in the MMIC as meandered transmission lines with a high impedance, and the capacitors are implemented as metal-insulator-metal capacitors. This process is repeated for the input matching network (IMN), inter-stage matching network (ISMN), and output matching network (OMN).

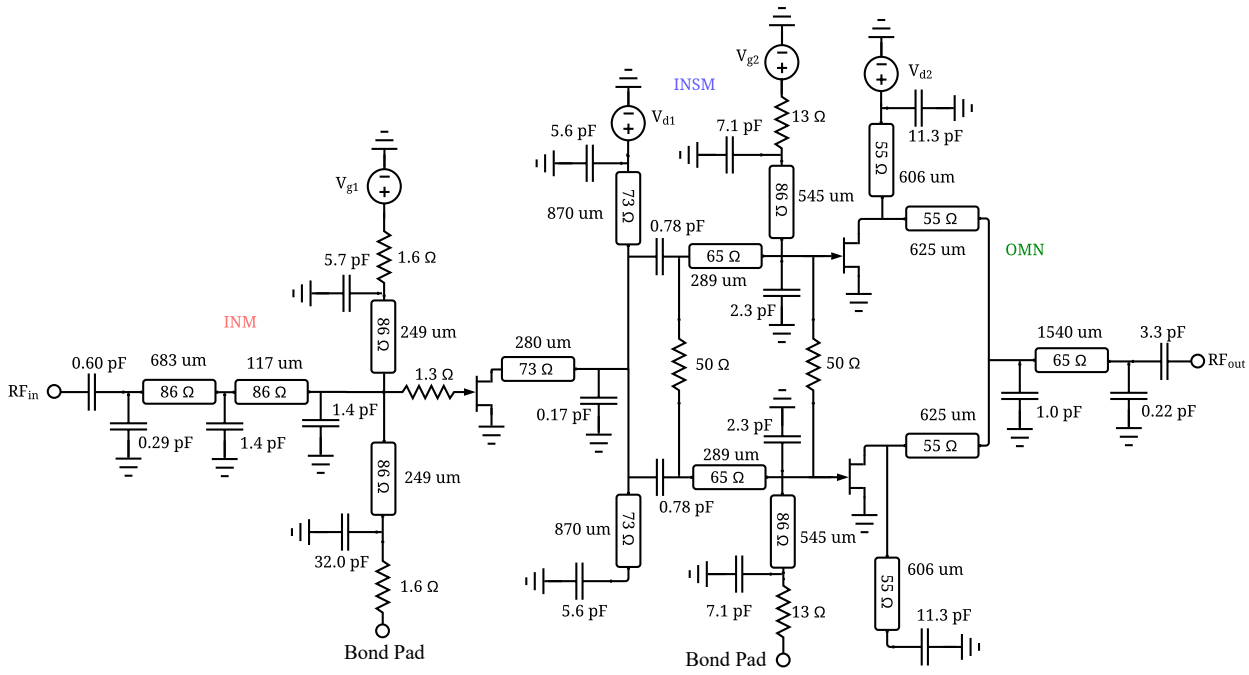
The harmonic impedance can have a substantial impact on efficiency. Fig. 2.6 shows the simulated PA efficiency at 6 GHz as the second harmonic reflection coefficient angle is swept with a magnitude of 0.95 when the third harmonic is terminated with an open and short circuit impedance and the fundamental impedance is matched for maximum PAE. The high magnitude of the reflection coefficient is chosen to shape the time domain waveforms at the drain plane for high efficiency and reflects the behavior of matching networks, which tend towards reactive impedances at harmonic frequencies. Additionally, resistive harmonics reduce efficiency since power is delivered to the harmonics.

For both cases, the PAE drops by 30% when the second harmonic is terminated near a short circuit; however, when the third harmonic is terminated in an open circuit, the range of angles where the PAE drops is relatively narrow. This region is described as a "keep-out" region for the second and third harmonics. It is mathematically defined as the range of angles where the efficiency drops 1% below the average PAE across the full phase sweep.

A photograph of the realized MMIC PA is shown in Fig. 2.5a. The first stage consists of a single $16\times100\,\mu$m device, and the second stage has two $20\times100\,\mu$m devices (staging ratio of 1:2.5). Each device is biased at 125 mA/mm at a nominal drain voltage of 20 V. The small input impedance of the large devices makes it challenging to achieve a broadband impedance match at the input and



(a)



(b)

Figure 2.5: (a) Photograph of the 10 W MMIC operating from 6 GHz to 12 GHz. (b) Schematic of MMIC matching network and bias tee.

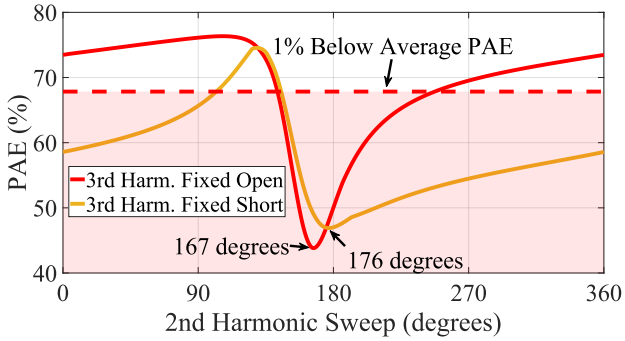


Figure 2.6: Sweep of the 2nd harmonic phase when the 3rd harmonic is fixed with an open and short at an f_0 of 6 GHz.

inter-stage. For instance, the input impedance of the 16×100 μm driving device at 9 GHz is Z_{in}= 0.33 - j2.2 Ω when loaded by the inter-stage matching network and final stage. In order to make the input impedance more manageable, a series 1.3 Ω resistance is added to the gate of the first stage using a thin film resistor available in the process. This improves the return loss and stability at the expense of gain and PAE. Stability resistors of 1.6 Ω and 13 Ω are added in series with the first and second stage gate bias lines close to the bypass capacitors. These resistors are shown in Fig. 2.5b. Additionally, 50 Ω resistors are placed across two branches in the inter-stage matching network to suppress odd-mode instabilities. The stability of the PA is evaluated using the Nyquist criterion from 1 MHz to 36 GHz at drain voltages from 10 to 20 V in 1 V steps.

The PAE-optimized load-pull impedances of the 20×100 μm device are shown in Fig. 2.7 from 6 to 12 GHz when the input is conjugate-matched at 9 GHz and the PA is driven at 26 dBm of input power. These ideal impedances are compared to the OMN impedance presented to one of the 20×100 μm devices from 6 to 36 GHz along with the "keep-out" regions for the 2nd and 3rd harmonics at 6 and 12 GHz. For each load pull simulation, the harmonics not being swept are set to a fixed open circuit with a magnitude of 0.95. The magnitude of the 2nd harmonic "keep-out" region is slightly reduced for visual clarity. The "keep-out" regions are mostly avoided, except at the 2nd harmonic of 6 GHz, which falls into the octave bandwidth, and the fundamental match at 12 GHz is prioritized.

To perform CW measurements of the PA, the MMIC is mounted on a copper-molybdenum

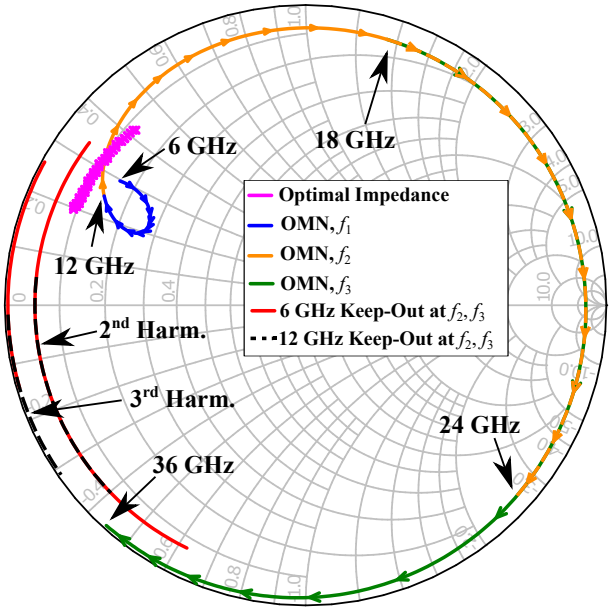


Figure 2.7: Efficiency-optimal fundamental load-pull impedance for the final stage device at 15 V, compared to the implemented fundamental, 2nd, and 3rd harmonic impedances and corresponding keep out regions at the band edges as defined in Fig. 2.6.

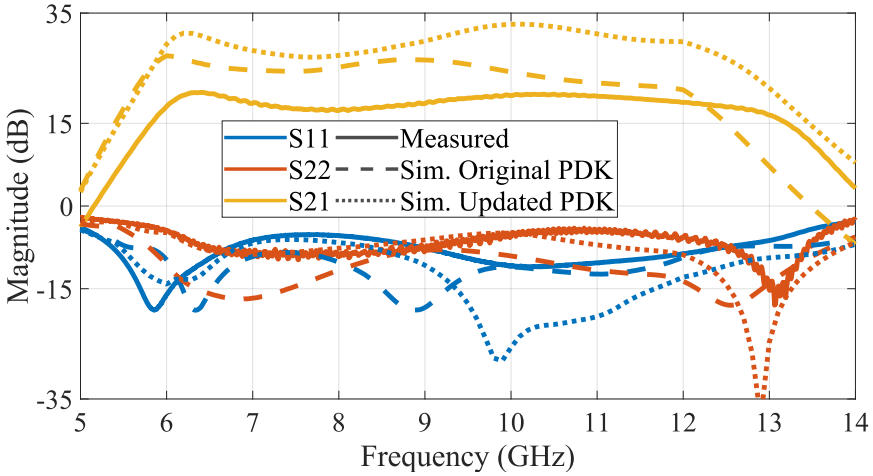


Figure 2.8: Measured magnitude of scattering parameters of the PA compared to simulated results using two different PDKs at a drain voltage of 20 V.

slab along with 100 pF and 1000 pF off-chip bypass capacitors placed in parallel with each of the gate and drain bias lines. The off-chip drain capacitance helps ensure stability during on-wafer probing and is omitted when the PA is supply-modulated. The PA is measured on-wafer using a probe station with 150 um probes. large-signal vector measurements are performed on a Keysight network analyzer (part number: E8364C). A diagram of the setup is shown in Fig. 2.9. The driver is necessary to compress the device under test (DUT). Each of the voltage waves a_1, b_1, a_2, and b_2 are calibrated to the plane of the DUT and measured as complex values. The input wave (a_1) is used for power leveling during large-signal power sweeps and is calibrated by placing an external power meter at the input plane of the DUT and measuring the relative power between the a_1 and the power meter. The remainder of the system is calibrated using a standard short open load thru (SOLT) calibration.

The measured and simulated S-parameters of the PA are shown in Fig. 2.8 at a drain voltage of 20 V. In measurements, the small and large-signal characteristics are slightly shifted towards higher frequencies, covering 6.3 to 12.6 GHz. The simulations use the PDK model the MMIC was designed in and an updated model that was provided after tape-out. The measured $|S_{21}|$ of the PA is lower than simulated and varies from 17.3 to 20.5 dB while the return loss is better than 5 dB across the band. The updated PDK model more accurately predicts $|S_{11}|$ and $|S_{22}|$ as well as the shifted frequency performance, however, $|S_{21}|$ is significantly larger across the band in simulations.

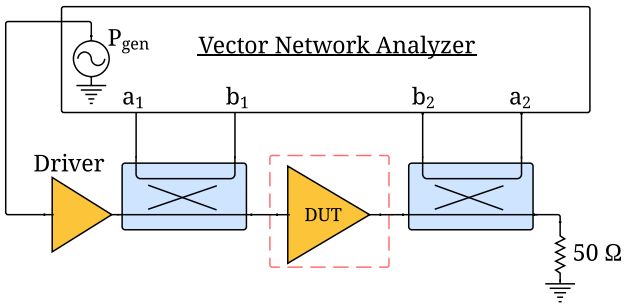


Figure 2.9: Large-signal vector measurement setup using external dual-directional couplers to measure the "a" and "b" waves of the PA.

The CW large-signal PAE and gain are shown in Fig. 2.10a – c as a function of output power

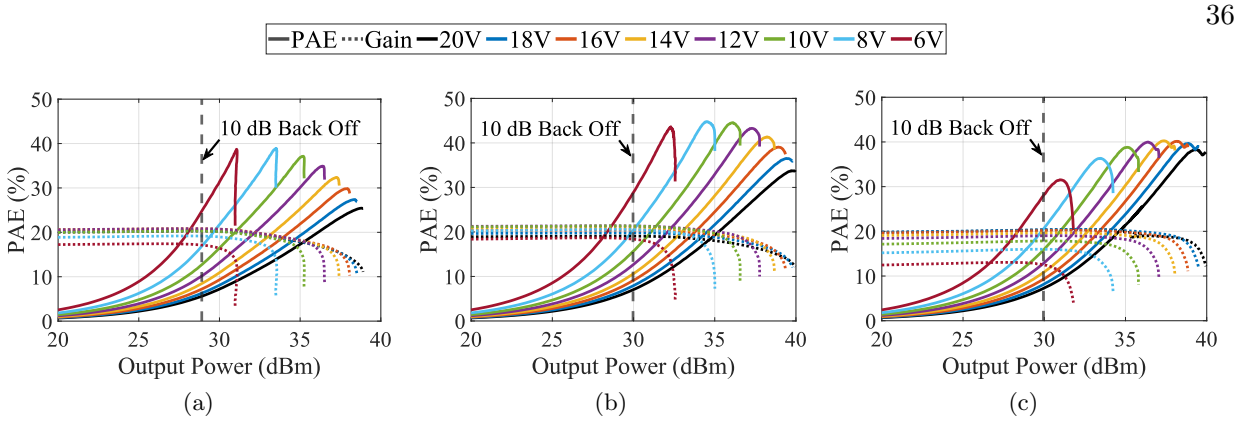


Figure 2.10: Measured PAE and gain vs. output power for drain voltages ranging from 6 V to 20 V at frequencies of (a) 6.3 GHz, (b) 9 GHz, (c) 12 GHz.

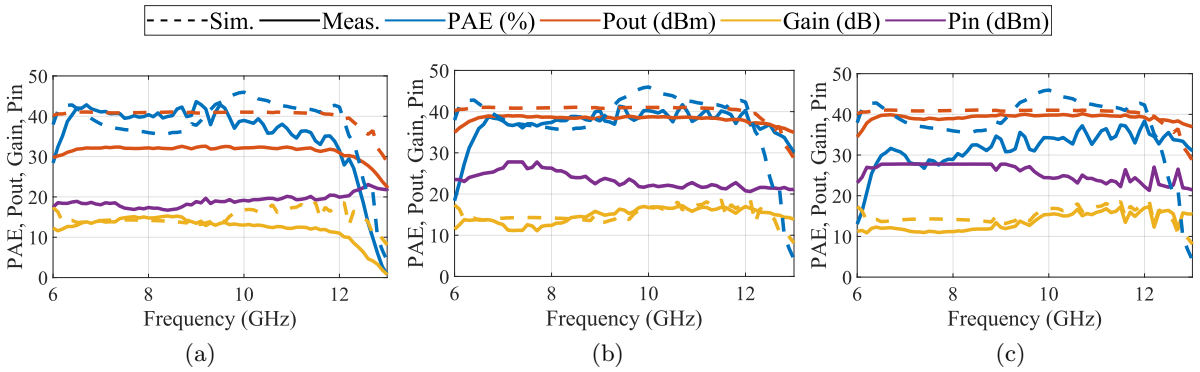


Figure 2.11: PAE, output power, and gain with the drive power at each frequency optimized for PAE at drain voltages of (a) 6 V, (b) 15 V, and (c) 20 V.

for drain voltages from 6 to 20 V with 2 V spacing, at 6.3 GHz, 9 GHz, and 12 GHz. The first and second-stage drain voltages are equal for each measurement. Across a 10 dB back-off range utilizing drain voltages from 6 to 20 V, the PAE is greater than 24.9%, 28.8%, and 28.2% at 6.3 GHz, 9 GHz, and 12 GHz.

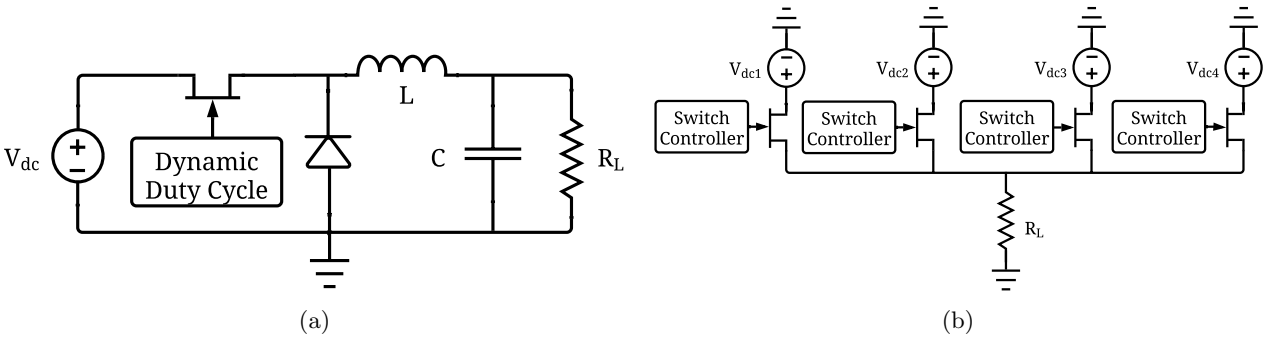
In addition, we observe a backed-off gain variation of 3.4 dB, 2.7 dB, and 7.3 dB, respectively, at these same frequencies. The lower gain variation found at low and medium frequencies reduces the linearity degradation of the PA when it is supply-modulated and will be discussed further in chapter 3. The large-signal frequency dependence of the PAE, gain, input power, and output power is shown in Fig. 2.11. The drive power is chosen for maximum PAE at the corresponding drain voltage for each frequency point. The dashed lines show the simulated results using the

original PDK model and the same input powers. When the input power is adjusted for PAE a very flat output power response is observed for all drain voltages. At 20 V the output power exceeds 39.5 dBm from 8.4 to 11.6 GHz, and the power exceeds 38.1 dBm across the full 6.3 to 12.6 GHz bandwidth.

2.3 Supply Modulator Architectures

Another key aspect of supply modulation is the dynamic power supply called a supply modulator. The requirements of these converters are high bandwidth (switching speed/slew rate), high efficiency, and large dynamic voltage range. Additionally, the supply modulator must meet the output power demands of the PA. The drain waveform generated by the supply modulator can be a continuous waveform or a discretized approximation. Examples of continuous supply modulators are buck converters [67, 69, 87] and dynamic linear regulators [108]. Examples of discrete supply modulators are the various multi-level converter topologies [73,83,109], and power digital to analog converter (DAC) [65, 110]. Additionally, hybrid approaches are capable of improving the efficiency and bandwidth of a supply-modulated system [111]. These hybrid converters consist of different combinations of buck converters, multi-level converters, and linear regulators in series and parallel configurations.

The schematic of a buck converter is shown in Fig 2.12a. This converter uses a transistor and diode (or two transistors) to switch between ground and a dc voltage supply. This switching waveform is filtered through an LC low-pass filter and applied to a resistive load. The instantaneous output voltage is controlled by the duty cycle of the transistor switch and is always less than or equal to the dc voltage supply. By dynamically changing the duty cycle, the output voltage can be changed to track the envelope of a signal. The primary drawback of the buck converter for supply modulation applications is the limited bandwidth. The switching frequency of the buck converter must be 5 to 10 times greater than the envelope of the signal it is tracking [112]. The losses increase with higher switching frequency, so the buck converter can be inefficient when tracking high signal bandwidths. This limitation is exacerbated since supply modulators follow the signal envelope,



(a) (b)

Figure 2.12: Power converter schematic for (a) buck converter (b) multi-level converter

which has a larger bandwidth than the signal. This bandwidth expansion is due to the non-linear operation of taking the magnitude of an IQ signal. The envelope voltage of a QAM signal is:

$$v_{env} = \sqrt{v_I^2 + v_Q^2} \tag{2.1}$$

where v_{I} is the in-phase voltage component and v_{Q} is the quadrature voltage component. Due to the increased losses with higher switching speeds, buck converter implementations of continuous supply modulation (CSM) are typically limited to tracking signal bandwidths below 20 MHz.

A discrete supply modulation (DSM) approach approximates continuous supply modulation with a limited number of voltage levels. The schematic of a four-level multi-level converter is shown in Fig.2.12b. This converter uses transistor switches to apply several discrete voltage levels synchronously. The primary advantage of discrete supply modulation is that it can efficiently track higher bandwidth signals than its continuous counterpart. This is because the discrete supply modulation architectures reduce the number of switching instances by an order of magnitude compared to continuous supply modulation architectures. The disadvantage of discrete supply modulation is reduced PA linearity performance, which results from the discretized drain waveform deviating from the ideal continuous case. Additionally, upon each voltage level transition, there is ringing in the output voltage. This ringing adds to the PA non-linearities and is the topic of chapter 5. A summary of state-of-the-art continuous and discrete supply modulators is shown in Table 4.1 in chapter 4.

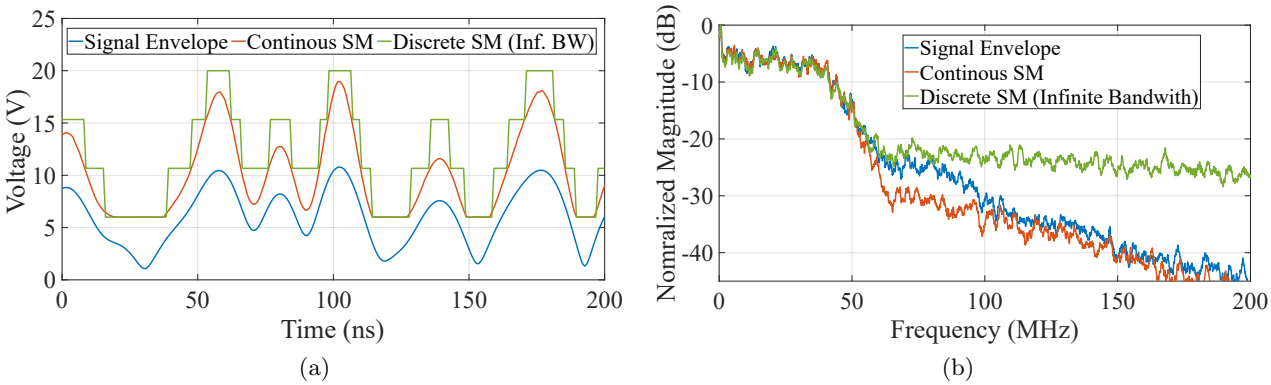


Figure 2.13: Example of continuous and discrete drain waveforms along with a 64-QAM 67.5 MHz signal envelope in the (a) time domain and (b) frequency domain. There are no bandwidth limitations imposed on the discrete waveform.

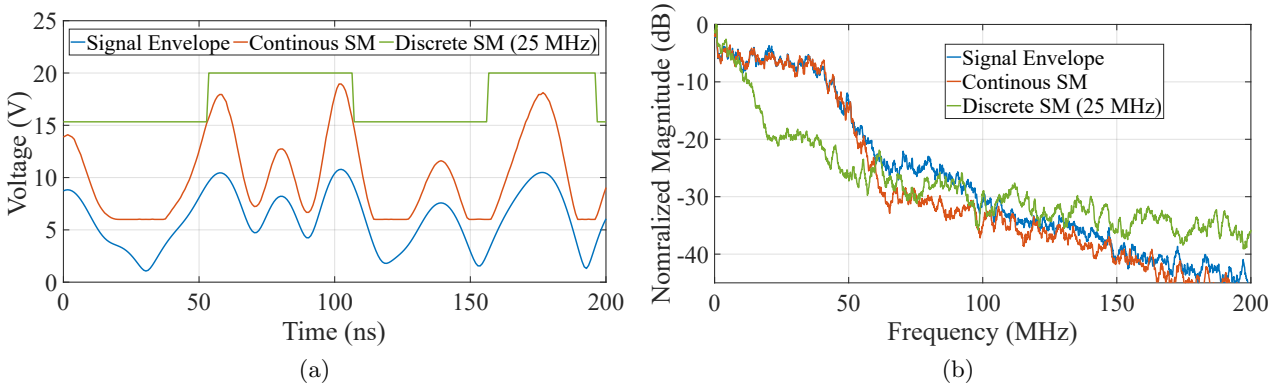


Figure 2.14: Example of continuous and discrete drain waveforms along with a 64-QAM 67.5 MHz signal envelope in the (a) time domain and (b) frequency domain. The maximum switching frequency of the discrete waveform is limited to 25 MHz.

All supply modulators have an upper limit on their tracking bandwidth. This is due to the parasitic inductance, capacitance, and resistance, in the transistor, passive output trace interconnect, and gate drivers. These parasitic elements low pass filter the output voltage and add distortion to the signal. To circumvent this issue, continuous supply modulators can track a reduced bandwidth version of the original envelope signal [72, 113], which avoids distortion due to filtering at the output of the modulator. In discrete supply modulators, the maximum switching frequency is lowered, reducing the discrete signal's bandwidth. To illustrate this point, the time domain and frequency spectrum of continuous and discrete drain voltages tracking a 67.5 MHz

64-QAM signal is shown with an unbounded switching frequency in Fig. 2.13 and a maximum switching frequency of 25 MHz in Fig. 2.14. Note that the continuous drain voltage and signal envelope are identical in each figure, and only the discrete waveform is changed. For these figures, the drain voltage is tailored to maximize the efficiency of the 10 W PA presented in section 2.2.3. The drain voltage range is 6 V to 20 V, which is consistent with the drain supply voltages measured in section 2.2.3. By limiting the switching frequency of the discrete waveform, the bandwidth is significantly reduced. However, the voltage waveform deviates further from the ideal continuous case. The reduced switching frequency has a small impact on efficiency; however, it can degrade PA linearity [80]. This effect will be discussed further in chapter 3.

The maximum switching frequency is defined by the minimum pulse width as:

$$f_{\mathrm{sw,max}} = \frac{1}{PW_{\mathrm{min}}}, \tag{2.2}$$

where PW_{min} is the minimum allowed pulse width in the discrete drain supply. This definition is adopted since rising and falling edges in the supply modulator are both switching instances. Therefore, the period is equal to the time between rising and falling edges. This definition differs from a conventional definition of a square wave, where one period is the time between two rising or falling edges.

2.4 Drain Voltage to Input Power Relationship

In a supply-modulated system, the drain voltage waveform can deviate from the signal envelope. This is one of the factors that distinguishes supply modulation from envelope tracking and enables an extra degree of freedom to improve system performance. For instance, the dynamic drain signal can maximize efficiency, linearize the PA, or a compromise between the two [59, 66]. This is achieved by tailoring the relationship between instantaneous drain voltage and the input power incident on the PA, which is referred to as a shaping function. Fig. 2.15 shows a block diagram of a supply-modulated PA. The arbitrary waveform generator (AWG) and supply modulator controller

are programmed digitally and aligned at the PA. The shaping function is implemented through a look-up table (LUT) and determined from the CW PAE and gain of the PA as a function of input power and drain voltage. The CW PAE and gain are plotted in Figs. 2.16 and 2.17 at 6.5 GHz and 11.5 GHz along with the continuous PAE and gain trajectory which results from dynamically changing the drain voltage. Here, trajectory refers to the PA CW performance, which results from the changing drain voltage.

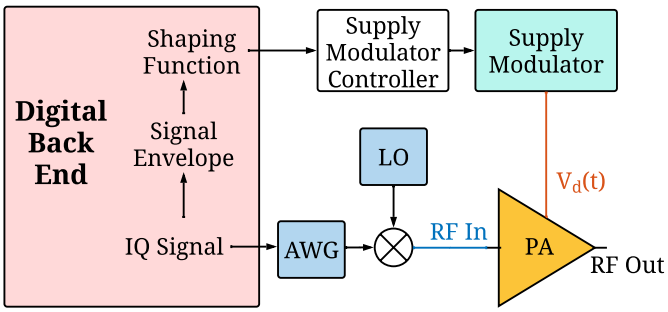


Figure 2.15: Block Diagram of a supply modulated PA. The digital back-end programs the arbitrary waveform generator and supply modulator controller to create the IQ signal and drain voltage. The shaping function LUT is implemented digitally and used to relate the input envelope to the desired drain voltage waveform.

Here three shaping functions are used at each frequency. The first is a flat-gain shaping function, which linearizes the AM-AM (gain magnitude) response of the PA. The second is a compressed flat-gain shaping function, which allows the gain to compress by a limited amount to achieve a higher efficiency than the flat-gain case. The third is a maximum efficiency shaping function, which yields the highest efficiency but typically degrades linearity. For the flat-gain and compressed flat-gain shaping functions, the target gain selected is the small signal gain at the lowest drain voltage of 6 V. In the compressed flat-gain shaping function, the range of deviation from the target gain is 1 dB. Typically, flat-gain shaping functions produce a constant gain across output power but reduced PAE, as is the case in Fig. 2.16a. However, at 11.5 GHz, the PAE trajectory shown in Fig. 2.17 is nearly the same for the flat-gain, compressed flat-gain, and maximum efficiency shaping functions.

To generate the shaping functions and trajectories, the CW measurements/simulations are

two-dimensionally interpolated onto a fine input power and drain voltage grid. Across the full range of output powers, all the combinations of drain voltage and input power that yield a given output power are binned together. From these combinations, a single drain voltage and input power combination is selected for each output power bin. For a maximum PAE shaping function, the combinations that yield the highest PAE are chosen. For a flat-gain shaping function, the combination which yields the target gain is chosen. With a compressed flat gain shaping function, the combination that yields the highest efficiency inside the allowed range of gain values is chosen.

The shaping functions are generated without consideration of the phase. However, the power and drain voltage dependent phase variation (AM-PM) can have a substantial impact on linearity. The output phase is plotted vs output power at multiple drain voltages for each of the three shaping functions in Figs. 2.18 and 2.19 at 6.5 GHz and 11.5 GHz respectively. Here, the phase variation across each shaping function is 55.8° at 6.5 GHz and 64.6° at 11.5 GHz. For this PA, the phase variation across power is relatively small compared to the phase variation across drain voltage. Overall, the phase variation across power and drain voltage significantly degrades the linearity and is discussed in the following section.

2.4.1 Continuous Shaping Function

To evaluate the performance of these shaping functions under dynamic supply modulation conditions, a behavioral model of the PAs is created in MATLAB using measured interpolated CW PAE, gain magnitude, and phase as a function of input power and drain voltage. The inputs of this model are the instantaneous power of the baseband signal envelope and the drain voltage of the PA. These inputs are the operating point of the PA. At each instant, the PA is considered to be operating in a CW state. Therefore, the modulated output power, PAE, gain magnitude, and phase can be determined from CW measurements/simulations of the PA. Repeating the process point by point across one period of the signal envelope accurately predicts the PA performance with a modulated signal. This can be repeated with any drain voltage waveform bounded by the range of measured drain voltages. From this simulation, the PAE, gain, and linearity are predicted. The

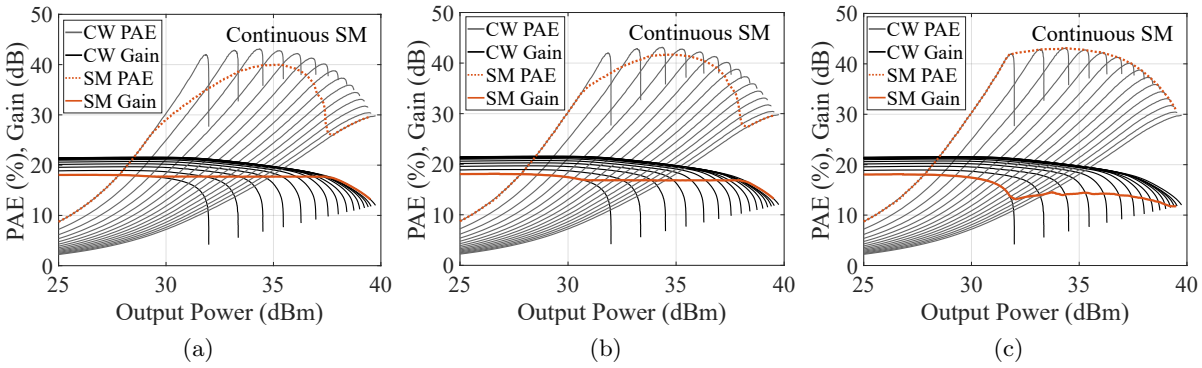


Figure 2.16: Continuous supply modulation trajectories of the MMIC PA at 6.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

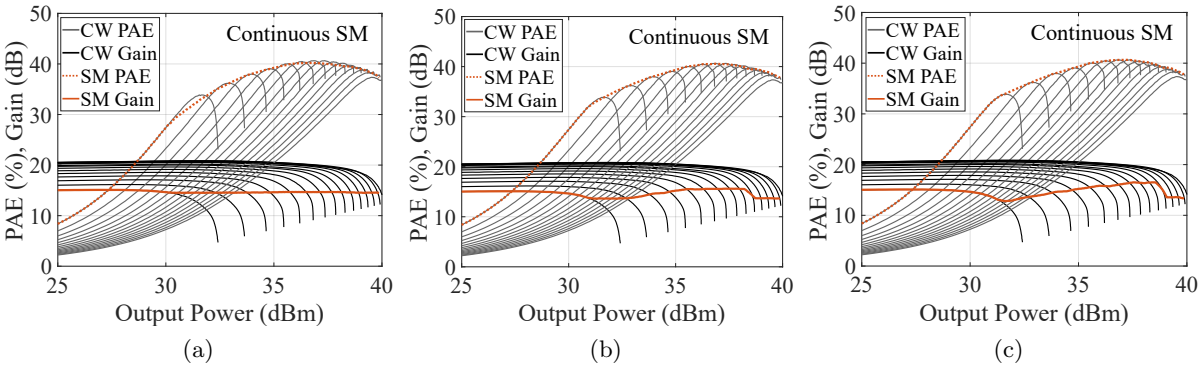


Figure 2.17: Continuous supply modulation trajectories of the MMIC PA at 11.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

envelope simulator does not include memory effects such as trapping, thermal dependence, and bias line effects. However, the AM-AM and AM-PM distortion is the dominant non-linearity in GaN HEMT PAs. Therefore, this behavioral model works as a first-order approximation of the non-linearities, including the complex gain variations due to the changing drain voltage [47], [114]. This approach is also used in chapter 3, where the simulator results are validated with measurements.

In order to evaluate the effect of phase variation on the linearity, the average error vector magnitude (EVM), PAE, and gain are predicted using the envelope simulator with the continuous shaping functions shown in Fig. 2.20 and the 64-QAM 67.5 MHz signal. The results are shown omitting phase variation in Fig. 2.21 and with the phase included in Fig. 2.22 at 6.5 GHz and 11.5 GHz. At both frequencies, the EVM is the lowest with the flat-gain shaping function and the

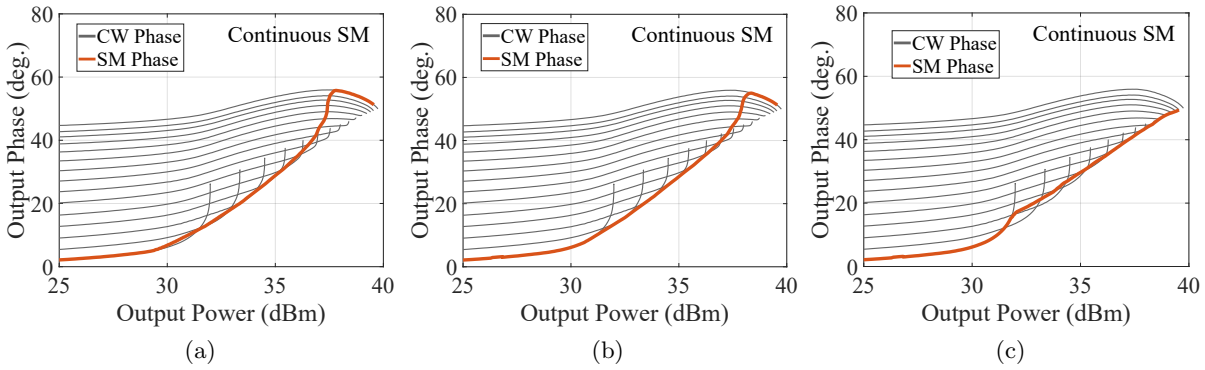


Figure 2.18: Continuous supply modulation phase of the 10 W MMIC PA at 6.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

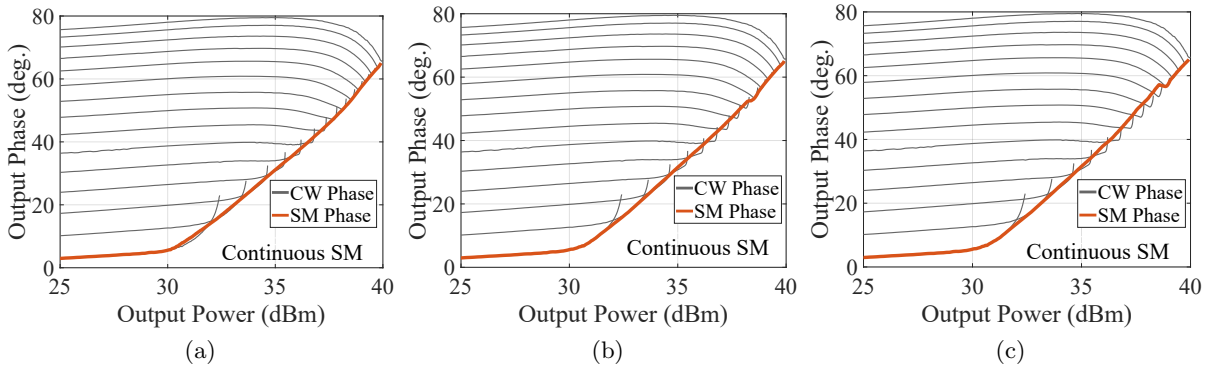
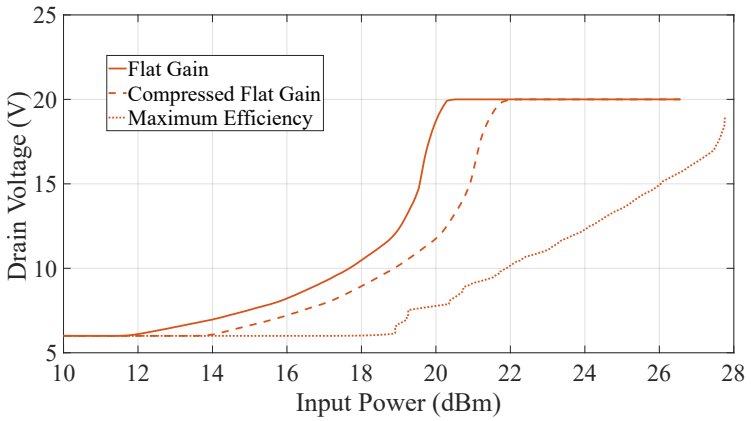


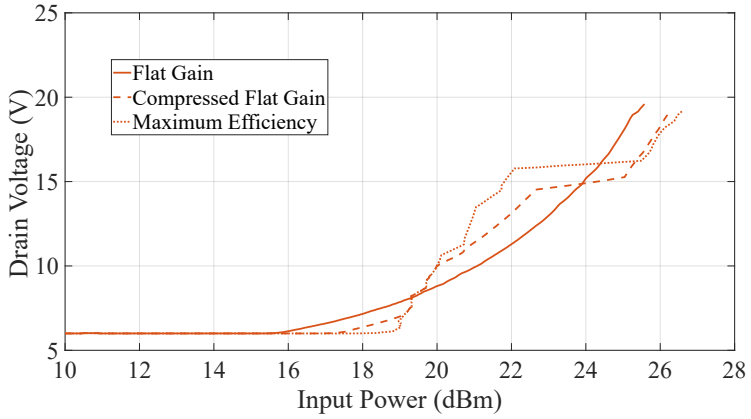
Figure 2.19: Continuous supply modulation phase of the 10 W MMIC PA at 11.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

worst with the maximum efficiency shaping function. Since flat-gain shaping functions linearize the signal's amplitude, if the phase variation is omitted (zero), the EVM can be reduced to nearly zero by using a flat-gain shaping function. However, when the phase variation is included, the EVM is significantly degraded.

At 6.5 GHz in Figs. 2.21a and 2.22a the PAE is the highest with the maximum efficiency shaping function and the lowest with the flat-gain shaping function. The compressed flat-gain shaping function is a compromise between flat-gain and maximum efficiency. By allowing for a larger gain compression range, this shaping function converges to the maximum efficiency case. At 11.5 GHz in Figs. 2.21b and 2.22b, the PAE is nearly identical for the three shaping functions, but the EVM is much lower with the flat-gain shaping function. This effect is evident in the PAE

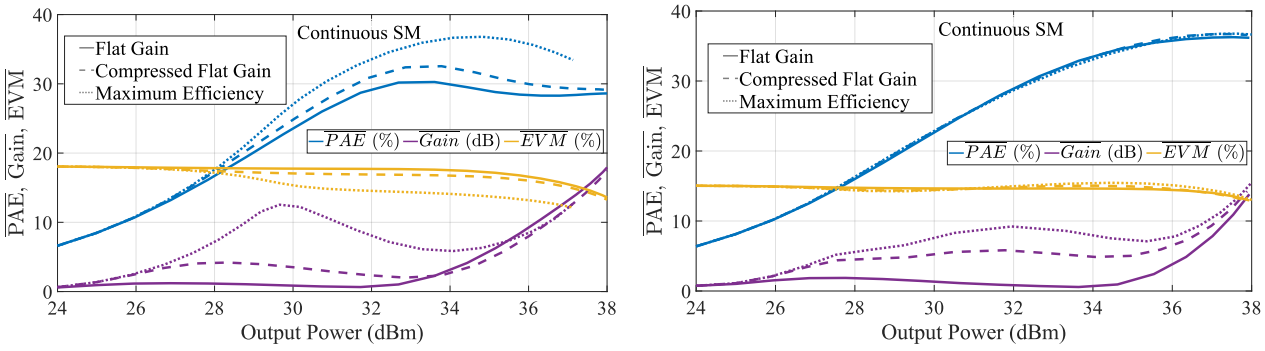


(a)



(b)

Figure 2.20: Continuous shaping function at frequencies of (a) 6.5 GHz and (b)11.5 GHz. Three shaping functions are used at each frequency. The first is flat-gain, the second is compressed flat-gain with 1 dB of compression, and the third is maximum efficiency.



(a) (b)

Figure 2.21: Predicted PAE, EVM, and Gain of the MMIC PA with a continuous dynamic supply amplifying a 64-QAM 67.5 MHz signal at (a) 6.5 GHz and (b) 11.5 GHz. Flat-gain, compressed flat-gain, and maximum efficiency shaping functions are used, and the trajectories are shown in Fig. 2.16 and Fig. 2.17. These results **omit** the phase variation of the PA.

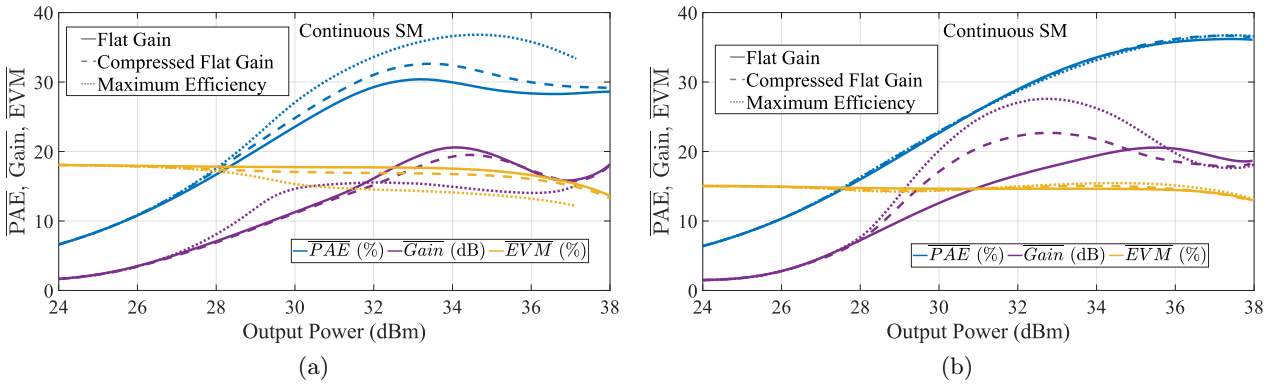


Figure 2.22: Predicted PAE, EVM, and Gain of the MMIC PA with a continuous dynamic supply amplifying a 64-QAM 67.5 MHz signal at (a) 6.5 GHz and (b) 11.5 GHz. Flat-gain, compressed flat-gain, and maximum efficiency shaping functions are used, and the trajectories are shown in Fig. 2.16 and Fig. 2.17. These results **include** the phase variation of the PA.

trajectories shown in Fig. 2.17. This phenomenon occurs because the gain at which the highest drain voltage reaches its maximum efficiency point is equal to the small signal gain at the lowest drain voltage. Additionally, at 6 V the PAE is nearly at its maximum without compressing the gain, likely a result of operating the PA near its knee voltage which generates harmonics without significantly compressing the device. The high efficiency with a flat-gain shaping function occurs coincidentally in this PA. However, this effect can be intentionally designed through careful selection of the source/load impedance to control the gain dependence on drain voltage and compression behavior, which is the topic of chapter 3.

2.4.2 Discrete Shaping Function

The continuous shaping function is discretized into four levels and shown in Fig. 2.23 at 6.5 GHz and 11.5 GHz. The four voltage levels are uniformly spaced at 6 V, 10.7 V, 15.3 V, and 20 V. An analysis on non-uniform voltage level spacing was performed in [66]. However, the improvements in efficiency were marginal, and the best linearity was achieved with the uniform voltage spacing. Therefore, for this section and throughout this thesis, uniform voltage spacing in the discrete supply modulators is used. The PAE and Gain trajectories are shown for each of the discrete shaping functions in Fig. 2.24 and Fig. 2.25 at 6.5 GHz and 11.5 GHz. The discrete

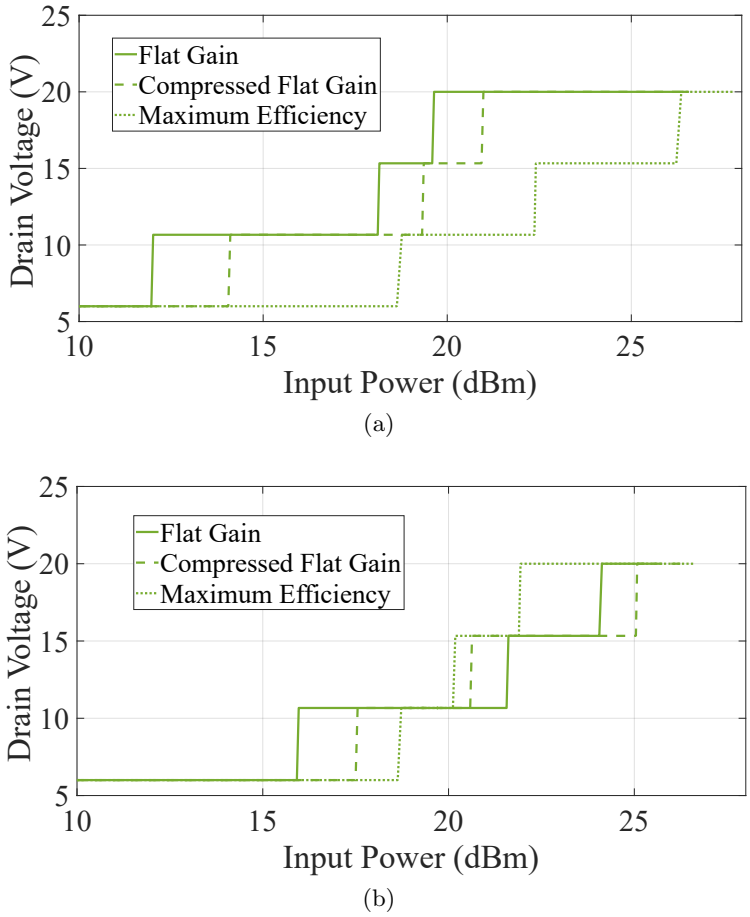


Figure 2.23: Discrete shaping function at frequencies of (a) 6.5 GHz and (b)11.5 GHz. Three shaping functions are used at each frequency. The first is flat-gain, the second is compressed flat-gain with 1 dB of compression, and the third is maximum efficiency.

gain and efficiency trajectories contain discontinuities across output power. This occurs because the shaping functions are generated to be continuous across input power. Since the gain increases with drain voltage, the gain and output power have jump discontinuity when the drain voltage switches to the next level. This adds additional distortion to the signal. The shaping function could be generated to be continuous across output power; however, this would require reducing the input power to compensate for the gain increase when switching to higher voltage levels. Such an approach results in a single input power corresponding to multiple drain voltages and is dependent on the next voltage level transition, thus requiring digital pre-distortion [115]. The discontinuity in gain magnitude and phase that results from the discretely changing drain voltage degrades

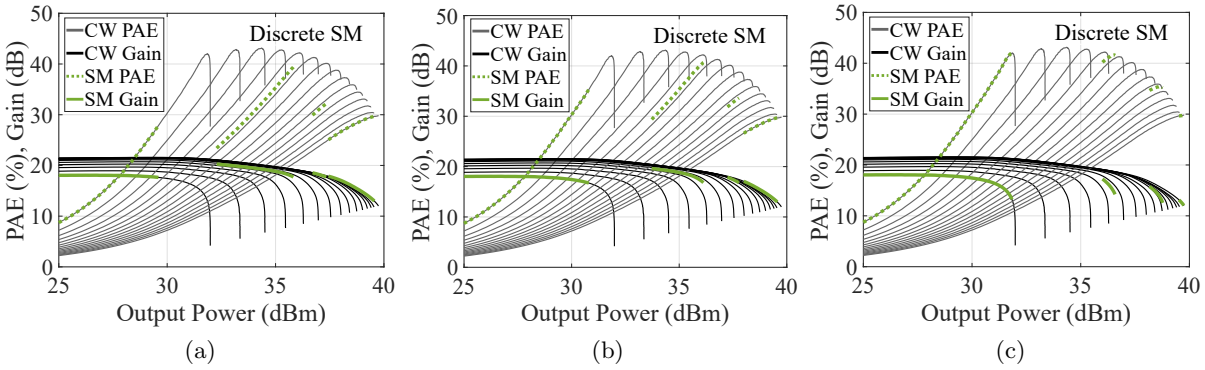


Figure 2.24: Discrete supply modulation trajectories of the MMIC PA at 6.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

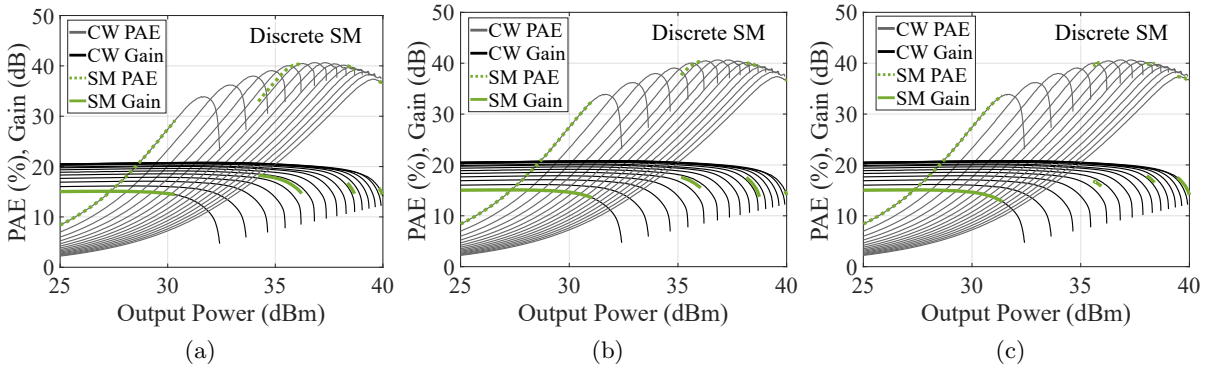


Figure 2.25: Discrete supply modulation trajectories of the MMIC PA at 11.5 GHz with the following shaping functions: (a) flat-gain, (b) compressed flat-gain, and (c) maximum efficiency

the PA linearity. However, this distortion can be minimized through proper selection of the PA input/output impedance and is the topic of chapter 3

The predicted average EVM, PAE, and gain using a discrete supply are shown with the phase variation omitted in Fig. 2.26 and with the phase included in Fig. 2.27 at 6.5 GHz and 11.5 GHz for the discrete shaping functions shown in Fig. 2.23. Here, there are no bandwidth limitations enforced on the discrete supply. The EVM, PAE, and gain with each of the shaping functions and drain waveforms are summarized with the phase variation omitted in Table 2.1 and with the phase included in Table 2.2 at an average output power of 33 dBm.

The linearity improvement we observed using a flat-gain shaping function with the continuous supply is significantly degraded with the discretized approximation. With the phase variation

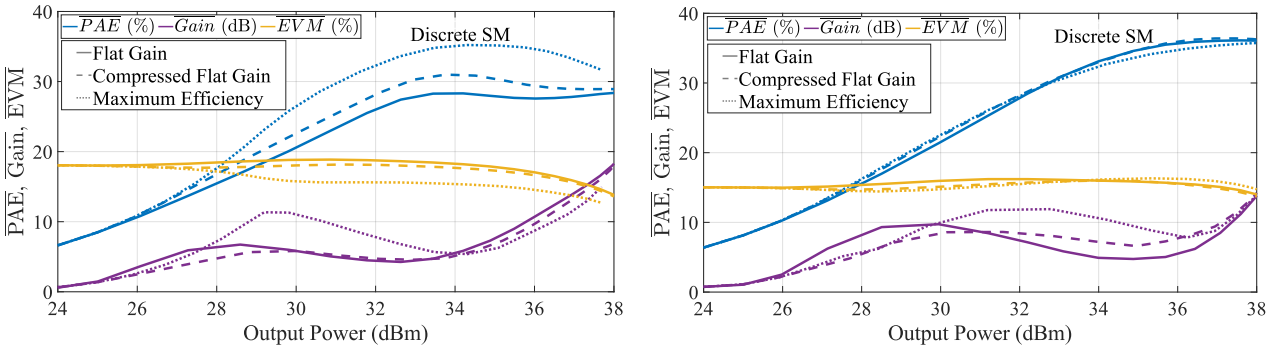


Figure 2.26: Predicted PAE, EVM, and Gain of the MMIC PA with a discrete dynamic supply amplifying a 64-QAM 67.5 MHz signal at (a) 6.5 GHz and (b) 11.5 GHz. Flat-gain, compressed flat-gain, and maximum efficiency shaping functions are used, and the trajectories are shown in Fig. 2.24 and Fig. 2.25.

omitted, at 6.5 GHz and 33 dBm of average output power, the discretized drain voltage increases the EVM by 3% points for the flat-gain case and 2.5% points for the compressed flat-gain case. At 6.5 GHz, the discretized maximum efficiency shaping function actually reduces the EVM by 0.2% points compared to the continuous case. At 11.5 GHz with the phase variation omitted, the linearity degradation from discretizing the shaping function is higher with an EVM increase of 5.2% points, 2.9% points, and 3% points with the discrete flat-gain, compressed flat-gain, and maximum efficiency shaping functions respectively. The PAE is reduced by a maximum of 2.4% points for each case at both frequencies when comparing the continuous and discrete cases.

With the phase variation included, at 6.5 GHz, the discrete supply modulation improves the linearity over the continuous case with the flat-gain and compressed flat-gain shaping functions. This non-intuitive result is likely a result of the phase having a much stronger dependence on drain voltage than power, as seen in Fig. 2.18. With discrete supply modulation, the voltage level is changed less often than with continuous supply modulation, and therefore, the AM-PM distortion is reduced. Furthermore, with the phase included at 6.5 GHz, the flat-gain shaping function linearity is degraded and does not provide clear improvements over the compressed flat-gain and maximum efficiency shaping functions in terms of linearity. When comparing the dynamic supply to the static 20 V case, the efficiency improvement with supply modulation is a minimum of 15.4% points

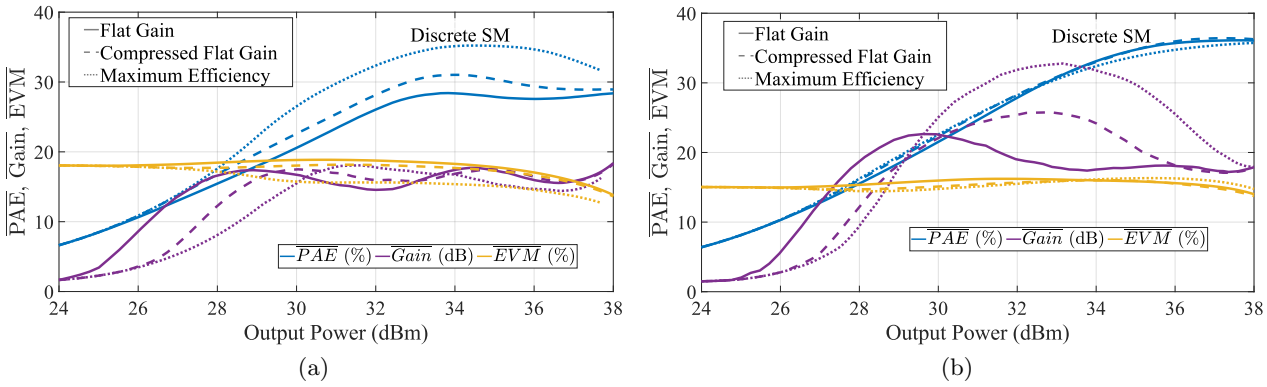


Figure 2.27: Predicted PAE, EVM, and Gain of the MMIC PA with a discrete dynamic supply amplifying a 64-QAM 67.5 MHz signal at (a) 6.5 GHz and (b) 11.5 GHz. Flat-gain, compressed flat-gain, and maximum efficiency shaping functions are used, and the trajectories are shown in Fig. 2.24 and Fig. 2.25.

Table 2.1: Comparison of average PAE, Gain, and EVM for flat-gain, compressed flat-gain, and maximum efficiency shaping functions with continuous, discrete, and static 20 V drain supplies at an output power of 33 dBm with the phase variation **omitted**. There are no bandwidth limitations enforced on the discrete supply.

6.5 GHz							
	Continuous Supply			**Discrete Supply**			**Static Supply**
	FG	CFG	ME	FG	CFG	ME	20 V
PAE (%)	30.4	32.5	35.7	28.0	30.3	34.3	12.6
EVM (%)	1.5	2.0	6.3	4.5	4.5	6.1	7.6
Gain (dB)	17.7	16.8	14.3	18.6	17.9	15.5	19.8
11.5 GHz							
	Continuous Supply			**Discrete Supply**			**Static Supply**
	FG	CFG	ME	FG	CFG	ME	20 V
PAE (%)	31.4	31.4	31.1	30.6	30.8	30.5	13.3
EVM (%)	0.6	5.1	8.8	5.8	8.0	11.8	2.7
Gain (dB)	14.6	15.0	15.3	16.1	15.9	15.9	20.2

higher across each frequency and shaping function. The gain, however, is lower with the dynamic supply and is almost always the tradeoff that supply-modulated systems are confronted with. This analysis demonstrates that moving from a continuous to a discrete supply modulation approach affects linearity more than efficiency. Additionally, discrete supply modulation can still provide clear improvements in PAE over a static drain supply.

Table 2.2: Comparison of average PAE, Gain, and EVM for flat-gain, compressed flat-gain, and maximum efficiency shaping functions with continuous, discrete, and static 20 V drain supplies at an output power of 33 dBm with the phase variation **included**. There are no bandwidth limitations enforced on the discrete supply.

6.5 GHz							
	Continuous Supply			**Discrete Supply**			**Static Supply**
	FG	CFG	ME	FG	CFG	ME	20 V
PAE (%)	30.4	32.5	35.7	28.0	30.3	34.3	12.6
EVM (%)	19.4	17.7	15.4	15.8	15.8	17.1	8.3
Gain (dB)	17.7	16.8	14.4	18.5	17.9	15.5	19.8
11.5 GHz							
	Continuous Supply			**Discrete Supply**			**Static Supply**
	FG	CFG	ME	FG	CFG	ME	20 V
PAE (%)	31.4	31.4	31.1	31.6	31.6	30.8	13.3
EVM (%)	18.3	22.7	27.5	17.8	25.5	32.8	2.8
Gain (dB)	14.6	15.0	15.2	16.1	15.9	15.9	20.2

2.5 Summary

Section 2.2 of this chapter investigates high-efficiency PA design, showing that harmonically tuned PAs, such as the class-F PA, are difficult to implement across a wide bandwidth and impossible for bandwidths equal to or exceeding an octave. Simulated load pull shows that tuning the second and third harmonic impedance does not produce substantial improvements in PAE. Instead, a narrow range of impedances substantially degrade PAE, referred to as "keep-out" regions. Therefore, broadband PA design should focus on avoiding these regions rather than tuning the harmonics for optimum PAE. This is shown through the design and characterization of a 10 W GaN MMIC PA operating from 6 GHz to 12 GHz. Section 2.3 examines continuous and discrete supply modulation approaches in terms of efficiency and bandwidth. Discrete supply modulation can efficiently track higher signal bandwidths than continuous supply modulation because it reduces the number of switching instances at the cost of added distortion to the drain voltage waveform. The baseband bandwidth of discrete supply modulators is limited by parasitic reactance and resistance in the transistor devices and passive interconnect which are a low-pass filter at the output. The

filtering distorts the signal if the supply modulator attempts to generate a drain waveform with high bandwidth. Limiting the maximum switching frequency of a discrete supply modulator can reduce the drain signal bandwidth to avoid this filtering and distortion.

Section 2.4 discusses the relationship between instantaneous drain voltage and input power. A behavioral model of the 10 W MMIC PA is created from CW measurements. The input parameters of this model are complex baseband envelope voltage and drain voltage. The non-linearities of the PA are applied point by point to the complex baseband signal, and the average PAE is calculated. The output parameters of the model are the complex output voltage and PAE. The performance of the 10 W PA amplifying a 67.5 MHz 64-QAM signal is predicted using this model at 6.5 GHz and 11.5 GHz with continuous and discrete supply modulation. The PA is also evaluated with three shaping functions: flat-gain, compressed flat-gain, and maximum PAE with the effect of phase variation investigated as well. For continuous supply modulation, the flat-gain shaping function yields the best EVM, the maximum PAE shaping function yields the highest average PAE, and the compressed flat-gain is a compromise between the two. At an output power of 33 dBm, the predicted performance with a dynamic supply shows at least 15.4% points improvement in PAE over a static 20 V supply. The phase variation substantially degrades the linearity of the PA in each case. When the phase is omitted, using a discretized drain voltage instead of continuous reduces the PAE by a few percentage points but has a larger impact on linearity, degrading the EVM by as much as 5.2% points. Furthermore, when phase is included with discrete supply modulation, the phase is improved in some cases. At 11.5 GHz, the small signal gain magnitude at the lowest drain voltage (6 V) is equal to the compressed gain magnitude at the peak PAE for the highest drain voltage (20 V). This results in the PAE trajectory from a flat-gain shaping function being nearly identical to the PAE trajectory from a maximum efficiency shaping function as shown in Fig. 2.16a. This large signal characteristic of the PA results from an optimal degree of gain variation across drain voltage. Modulated signal simulations with the phase omitted at 11.5 GHz in Fig. 2.21b show that the average PAE is identical for the three shaping functions, but the linearity significantly improved with a flat-gain shaping function. The results in this chapter are reported in [66].

Chapter 3

Source/Load Impedances Study of Discretely Supply Modulated GaN PAs

3.1 Introduction

Chapter 2 introduced the principles of a broadband supply modulation system. One effect that was only briefly discussed in section 2.2.3 is the expansive gain magnitude and phase dependence on drain voltage (V_d) that GaN PAs exhibit. The gain variation has a significant effect on supply modulated PAs as the magnitude can vary by as much as 7.5 dB and the phase by 40° as reported in [60], [110], [47]. This chapter investigates the impact that gain variation has on a supply-modulated PA and introduces a technique to minimize the gain variation through an intentional mismatch of the source and load impedance of a GaN MMIC PA.

To illustrate the origin of this variation, a basic schematic of a PA is shown in Fig. 3.1a. Here the transconductance and input/output impedance depend on V_d [94]. Both the gain magnitude and phase typically increase at higher drain voltages. The increasing gain magnitude is crucial to generating a flat-gain shaping function introduced in chapter 2. This shaping function compensates the PA's power-dependent gain compression with the expansive gain at higher drain voltages, thus resulting in a linear AM-AM response across output power [59, 95, 96, 116, 117]. While the AM-AM response of a PA can be linearized through a flat gain shaping function, the AM-PM response remains distorted due to the gain's phase dependence on drain voltage and input power. Furthermore, since most GaN PAs exhibit an expansive phase as a function of drain voltage and power, it is challenging, if not impossible, to linearize the phase response through a shaping function. Examples of analog compensation of the phase dependence on drain voltage have been demonstrated

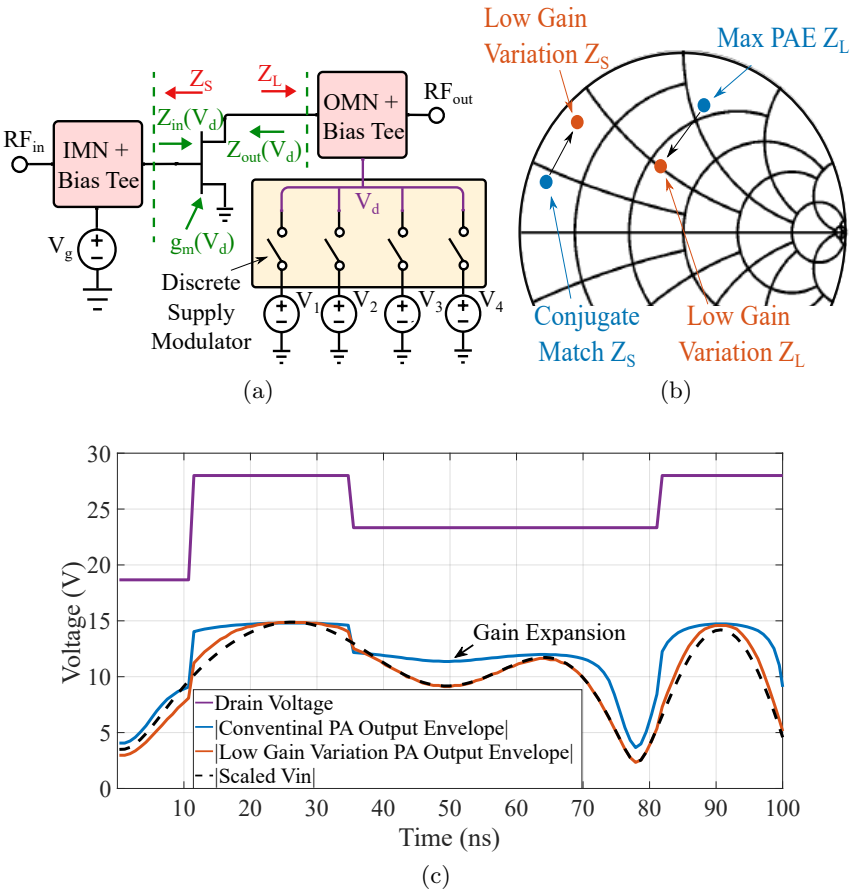


Figure 3.1: (a) Block diagram of a PA with a dynamically changing discrete drain supply voltage. (b) Potential source/load impedances for low gain variation across drain voltage and conventional PA design impedances. (c) Time domain simulation comparing the conventional PA design to the deliberately mismatched PA designed to reduce the gain dependence on drain voltage.

through an input phase shifter with the control voltage tied to the PA drain voltage [118] or mismatch of the input matching network [82], both of which result in a reduced PA gain.

For continuous supply modulation systems, the PA can be designed to minimize gain phase variation to improve AM-PM linearity [82]. The AM-AM response can then be linearized using a flat-gain shaping function. Thus for continuous supply modulation, the degree of gain magnitude variation is insignificant. However, the PA's gain as a function of drain voltage is a key characteristic of discrete supply modulation. Since discrete supply modulation has a limited number of levels and is often bandwidth-limited, the drain voltage deviates from the continuous supply modulation shaping function at instances where the supply does not have enough levels or is not fast enough to

follow the continuous shaping function. At these instances, the PA is dynamically moving between small and large signal operation as the drain voltage and input power are changed. Therefore, if the PA has a high small-signal gain variation with regard to supply voltage, the output signal is distorted, resulting in degraded linearity. The gain variation can be reduced by deliberately mismatching the input and output impedances as shown in Fig. 3.1b. The improvement in linearity from this mismatch is illustrated in Fig. 3.1c, where the output envelope is compared between a conventionally designed PA and a low-gain variation PA with discrete supply modulation. At 50 ns, we see a gain expansion for the conventional PA design when the envelope drops, but the supply voltage remains constant. In contrast, the low gain variation PA amplifies the signal with less distortion. Additionally, the discrete supply introduces voltage ringing upon each switching instance, which mixes with the PA and degrades linearity metrics [3, 83, 84]. This distortion is in addition to known AM-AM and AM-PM compression behavior prevalent in GaN PAs [34], [35], [119]. Any distortion of the output signal degrades out-of-band linearity metrics, such as adjacent channel power ratio, and in-band metrics, such as error vector magnitude. These distortions can be corrected through digital pre-distortion, however, this adds additional complexity, requires more computational power, degrades system efficiency, and has limitations for large signal bandwidths [120], [104], [115].

Mismatching PAs for reduced gain variation was demonstrated for the phase of the gain in [82, 121] and for the magnitude of the gain in [81]. However, an in-depth analysis of the linearity and efficiency trade-offs of different load/source impedances with a dynamically changing discrete drain supply has not been discussed in the literature to the best of the author's knowledge.

The chapter is an expanded version of the work published in [80] and is organized as follows: first, the gain variation across drain voltage at different impedances is shown through source and load pull simulations in section 3.2.1. From these simulations, three loading cases are investigated using continuous and discrete supply modulation in section 3.2.2 using the envelope simulator described in chapter 2. The first case is a conventional PA design. The second case has a mismatched source impedance to minimize phase variation. The third case has mismatched source and load

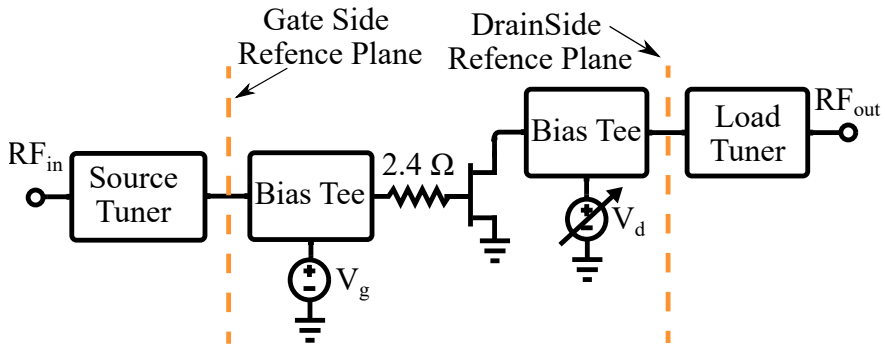


Figure 3.2: Source/load pull schematic. The 2.4 Ω resistor is added to stabilize the transistor.

impedances to minimize gain magnitude variation, which corresponds directly with the impedances realized in the final stage of an experimental MMIC PA presented in 3.3. Next, in section 3.3 the design and characterization of a two-stage 6 to 12 GHz bandwidth 5 W PA is presented. The measured CW data of the PA is used to predict the dynamic drain bias results using the custom envelope simulator. The PA is measured with a dynamic drain signal in section 3.4 and compared with envelope simulation results showing good agreement and validating the results of the envelope simulator.

3.2 Simulation Study

The small-signal gain variation of a GaN MMIC device is investigated through source/load pull simulations. Three different loading cases are identified: a conventional PA design; a design with the input mismatch to minimize the small-signal gain phase variation while maintaining a minimum of 10 dB; and a design that mismatches the source and load for minimal gain magnitude variation. The three cases are then simulated with continuous and discrete supply modulation.

3.2.1 Device source and load pull

The source/load pull simulations are performed with a single transistor at 9 GHz with a drain bias ranging from 14 to 28 V and a fixed gate bias. The transistor is an $8\times100\,\mu$m device in the WIN Semiconductors NP15 150 nm GaN on SiC process, biased with a gate voltage of -1.57 V

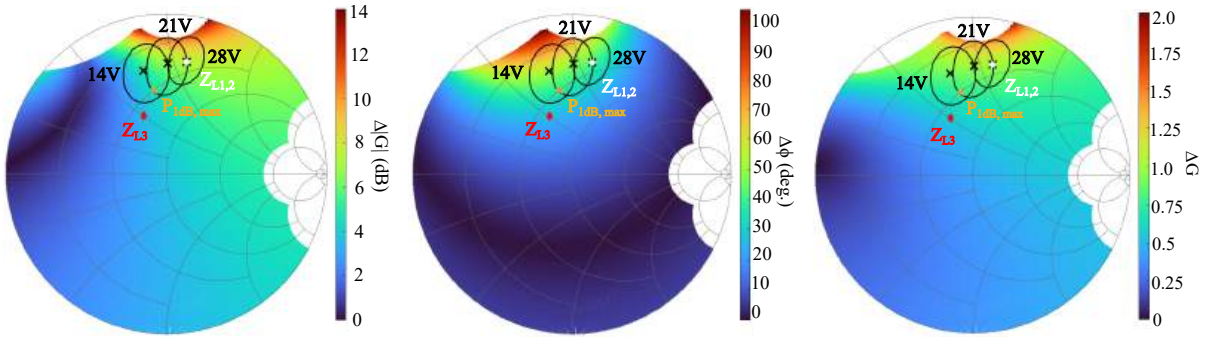


Figure 3.3: Load pull at 9 GHz of a single 8×100 μm device in the WIN NP15 GaN on SiC 150 nm process showing small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) across drain voltages of 14, 21, and 28 V. The PAE contours indicate impedances where the PAE is reduced by 5% from the peak PAE at each drain voltage. Additionally, the impedance which results in the maximum 1 dB compression output power is labeled.

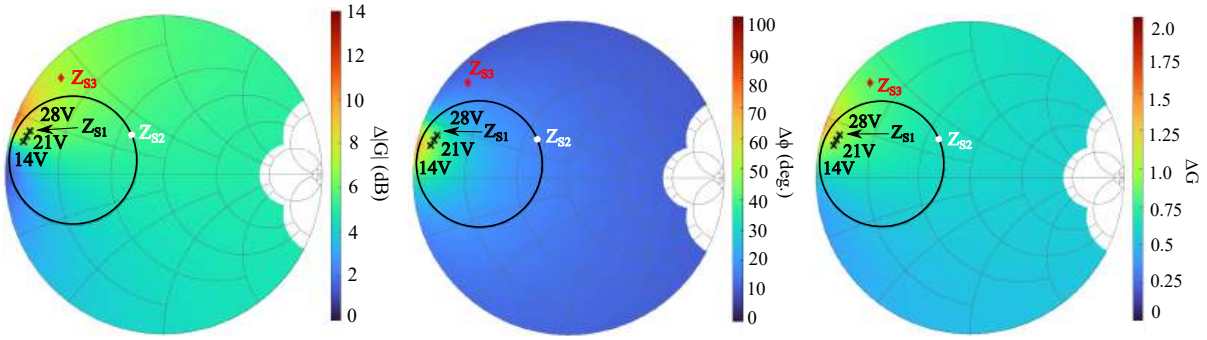
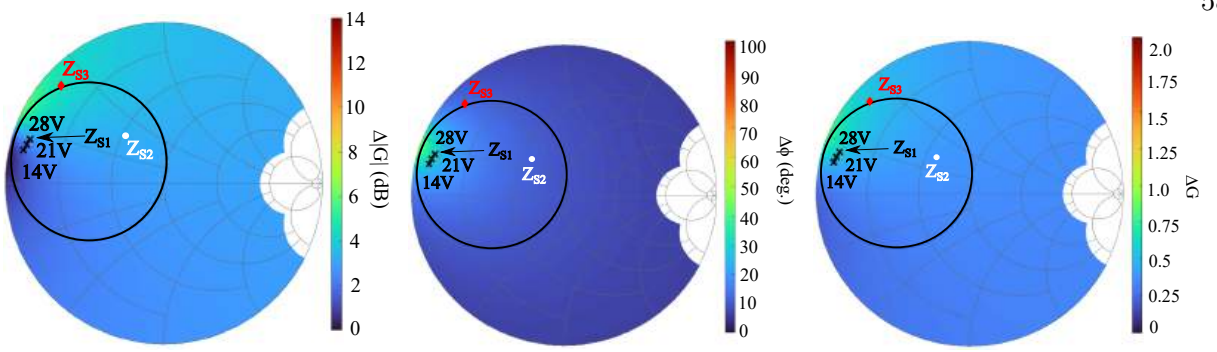


Figure 3.4: Source pull at 9 GHz of a single 8×100 μm device in the WIN NP15 GaN on SiC 150 nm process showing small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) across drain voltages of 14, 21, and 28 V. The load impedance is fixed at the maximum PAE point for a drain voltage of 28 V ($Z_{L1,2}$). The conjugate match points at each drain voltage are labeled along with the 10 dB small signal gain contour at 14 V.



(a) (b) (c)

Figure 3.5: Source pull at 9 GHz of a single $8\times100\,\mu$m device in the WIN NP15 GaN on SiC 150 nm process showing small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) across drain voltages of 14, 21, and 28 V. The load impedance is fixed at the mismatched load impedance (Z_{L3}). The conjugate match points at each drain voltage are labeled along with the 10 dB small signal gain contour at 14 V.

corresponding to 80 mA of quiescent current at the maximum drain voltage (28 V). The two-port S-parameters of the transistor are extracted at three drain voltages of 14, 21, and 28 V from the non-linear model provided by WIN Semiconductors. The load and source pull simulations are performed at each drain voltage using linear network analysis, cascading the transistor S-parameters with the input and output impedances. The standalone transistor is not unconditionally stable. Therefore, loss must be added to the input to stabilize the device as shown in Fig. 3.2 where a 2.4 Ω resistor is added. The load/source pull simulation schematic is shown in Fig. 3.2 with the corresponding reference planes. At each load/source impedance, the gain magnitude and phase of the overall cascaded network are calculated at the three previously stated drain voltages. The gain magnitude variation ($\Delta|G|$), gain phase variation ($\Delta\phi$), and complex gain variation (ΔG) are defined as:

$$\Delta|G| = max(|G(V_{\mathrm{d}m})|/|G(V_{\mathrm{d}n})|) \quad \forall m \neq n, \tag{3.1}$$

$$\Delta\phi = max(\angle G(V_{\mathrm{d}m}) - \angle G(V_{\mathrm{d}n})) \quad \forall m \neq n, \tag{3.2}$$

$$\Delta G = max\left(\frac{|G(V_{\mathrm{d}m}) - G(V_{\mathrm{d}n})|}{|G(V_{\mathrm{d}2})|}\right) \quad \forall m \neq n, \tag{3.3}$$

where $G(V_{\mathrm{d}m}) = |G(V_{\mathrm{d}m})| \exp\left[j\angle G(V_{\mathrm{d}m})\right]$ is the small signal complex gain at a drain voltage index m.

Load pull simulations of the $8\times100\,\mu$m device $\Delta|G|$, $\Delta\phi$, and ΔG are shown in Figs. 3.3a, 3.3b, and 3.3c, respectively. At each load impedance, the input is conjugate matched at a drain voltage of 28 V. The maximum PAE impedance for each drain voltage is shown, along with PAE contours where the efficiency drops by 5 percentage points (pp) from its peak value. Additionally, the impedance which results in the maximum 1 dB compression output power is labeled as well. The 2^{nd} and 3^{rd} harmonics are terminated with an open circuit to yield high efficiency. An analysis of the 2^{nd} and 3^{rd} harmonic termination with this MMIC process is presented in chapter 2. The labeled point $Z_{L1,2}$ shows the maximum PAE impedance at 28 V and Z_{L3} shows the load impedance presented to the output stage of the realized PA, which is a compromise between efficiency and $\Delta|G|$. In Fig. 3.3a, it is apparent that the $\Delta|G|$ can be reduced by matching the output for maximum PAE at the lower drain voltages. However, the $\Delta\phi$ is increased at these impedances, and the overall ΔG is nearly the same. By aggressively de-tuning the load impedance each of these parameters can be improved as shown in Z_{L3}, however, this reduces the efficiency. The tradeoffs between these impedances and their effect on PA performance will be further investigated in section 3.2.2. The $\Delta|G|$ and $\Delta\phi$ can be completely nulled through extreme de-tuning of the load impedance, however, this comes at a significant cost to efficiency and gain. Therefore, the load impedance chosen for the realized PA (Z_{L3}) is a trade-off between improving the $\Delta|G|$ and $\Delta\phi$ while maintaining acceptable gain and PAE.

Source pull simulations of the $\Delta|G|$, $\Delta\phi$, and ΔG are shown with the load impedance fixed for maximum PAE at 28 V ($Z_{L1,2}$) in Fig. 3.4 and with the load impedance mismatched at Z_{L3} in Fig. 3.5. The corresponding conjugate match points at each drain voltage are plotted when the output is loaded with the maximum PAE impedance for the three drain voltages. The labeled point Z_{S1} is the conjugate match at 28 V. Z_{S2} is the mismatched source impedance which results in minimal $\Delta\phi$ while maintaining 10 dB of gain at the lowest drain voltage. The point Z_{S3} is the source impedance presented to the output stage of the realized PA. Interestingly, the region of low

Table 3.1: $\Delta|G|$, $\Delta\phi$, and ΔG of the three matching cases.

Case	$\boldsymbol{Z_L}$	$\boldsymbol{Z_S}$	$\boldsymbol{\Delta|G|}$ **(dB)**	$\boldsymbol{\Delta\phi}$ **(deg.)**	$\boldsymbol{\Delta G}$
1	Z_{L1}	Z_{S1}	7.5	41.4	1.0
2	Z_{L2}	Z_{S2}	5.4	16.7	0.67
3	Z_{L3}	Z_{S3}	4.6	13.1	0.54

$\Delta|G|$ (Fig. 3.4a) near a short circuit corresponds to a region of high $\Delta\phi$ (Fig. 3.4b).

3.2.2 Envelope Simulations of a Single Device

To investigate the impact that different loading conditions have on efficiency, gain, and linearity, three matching cases are identified:

- **Case 1:** A conventional PA design where the load impedance is chosen to maximize PAE at 28 V ($Z_{L1,2}$) with the source impedance conjugate matched (Z_{S1});
- **Case 2:** Similar to the design in [82] where the load impedance maximizes PAE at 28 V ($Z_{L1,2}$) but the source impedance is mismatched to minimize $\Delta\phi$ while maintaining a minimum gain of 10 dB at the lowest drain voltage of 14 V (Z_{S2}); and
- **Case 3:** A low gain variation design where the load and source impedances are significantly mismatched from the conventional design and use the same impedances presented to the final stage of the realized PA presented in section 3.3 (Z_{L3} and Z_{S3}).

The simulated $\Delta|G|$, $\Delta\phi$, and ΔG values for these matching conditions are summarized in Table 3.1. The simulations are performed in Cadence AWR Microwave Office using ideal input and output tuners with identical device sizes and bias points as presented in section 3.2.1. The simulated CW PAE, gain magnitude, and gain phase are shown in Fig. 3.6 for each of the three cases, across drain voltages ranging from 14 to 28 V. These figures also show the continuous and discrete PAE, gain, and phase resulting from max PAE shaping functions.

Since the shaping function is mapped from a continuous range of input powers, there is a discontinuity in gain and output power when switching to higher discrete drain voltages, which

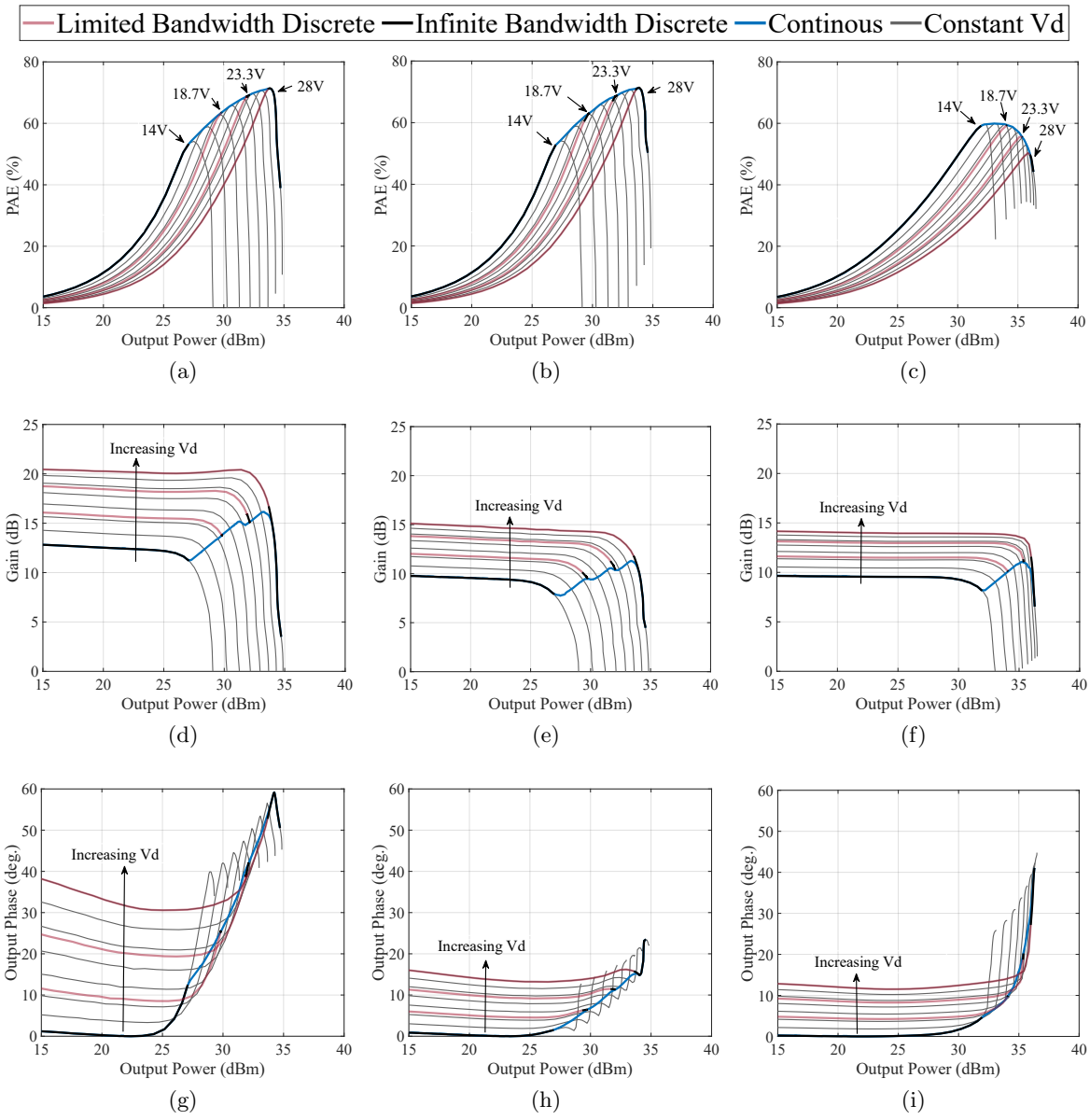


Figure 3.6: CW PAE, gain magnitude and phase plotted vs. output power for three different loading conditions at 9 GHz. The loading conditions are (a) conventional PA design (Case 1), (b) mismatched input impedance for minimal $\Delta\phi$ (Case 2), and (c) PA designed for low gain variation with the source and load mismatched (Case 3). Additionally, the PAE, gain magnitude, and phase resulting from the max PAE shaping function is plotted with an infinite bandwidth supply utilizing continuous (blue) and discrete (black) voltage levels. The performance resulting from bandwidth limitations in the discrete supply (red) is shown where the PA operates in the small and large signal regions.

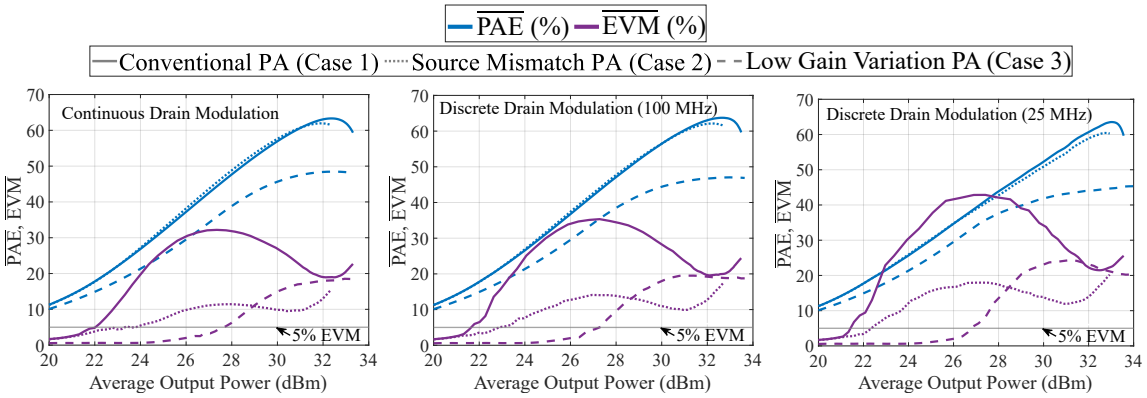


Figure 3.7: Simulated comparison between the three loading conditions in terms of average PAE, Gain, and EVM vs output power at 9 GHz with (a) continuous supply modulation (b) four-level discrete supply modulator with a maximum switching frequency of 100 MHz and (c) discrete supply modulation with a maximum switching frequency of 25 MHz.

degrades linearity. In addition, the bandwidth limitations of the dynamic supply cause deviations from this shaping function, and the PA is constantly switched between small and large-signal operation. This distortion can be minimized by reducing the PA's gain magnitude variation.

The PAE shown for a conventional PA design (Case 1) shown in Fig. 3.6a is nearly identical to the mismatched source impedance design (Case 2) shown in Fig. 3.6b with peak PAE occurring at 28 V, while the PAE of Case 3 (Fig. 3.6c) peaks at 14 V. Furthermore, the $\Delta|G|$ is highest in Case 1 and lowest in Case 3. The advantage of de-tuning the source impedance in Case 2 can be seen clearly in Figs. 3.6h and 3.6i where Cases 2 and 3 have much improved $\Delta\phi$.

To evaluate the performance of each of these cases under dynamic supply modulation conditions, a behavioral model of the PAs is created in MATLAB using the CW PAE, gain magnitude, and phase as a function of input power and drain voltage. Using this model, the AM-AM and AM-PM non-linearities created by the PA can be applied to any signal in the simulation point by point, and the PAE, gain, and linearity are also predicted. The envelope simulator does not include memory effects such as trapping, thermal dependence, and bias line effects. However, the AM-AM and AM-PM distortion is the dominant non-linearity in GaN HEMT PAs. Therefore, this behavioral model works as a first-order approximation of the non-linearities, including the complex

gain variations due to supply modulation [47], [114]. This approach was introduced in chapter 2.

Each case is evaluated with three different drain voltage modulation signals. The first is a continuous drain supply with no bandwidth limitations shown in Fig. 3.7a, the second and third are four-level discrete signals with minimum pulse widths limited to 10 ns (100 MHz) and 40 ns (25 MHz) shown in Figs. 3.7b and 3.7c. Parasitics in the switching devices and circuit layout reduce the slew rate of voltage transitions and set the upper limit on switching frequency. When the signal envelope bandwidth approaches or exceeds this maximum switching frequency, discrete supply modulation deviates from the desired continuous shaping function and has reduced efficiency and linearity [61]. At such points, the drain voltage is higher than the desired shaping function to avoid clipping the signal, and the PA operates in the small signal regime. There is a gain expansion at these instances where the discrete supply is not fast enough to follow the signal envelope or does not have enough levels. This is a direct consequence of the small signal gain variation $\Delta|G|$, and when minimized can improve linearity.

The amplified signal uses a 64-QAM modulation scheme with a baud rate of 50 Msymbols/sec, an initial root-raised cosine filter with a roll-off factor of 0.35 is applied before the signal is amplified, and this digital filter is applied a second time to the sampled output signal. The filtering expands the bandwidth to 67.5 MHz. The signal length is 1000 symbols, and the PAPR is 7 dB. The PAE, gain, and error vector magnitude (EVM) are averaged across one signal period and plotted in Fig. 3.7 as a function of output power for each of the three cases. Here the maximum PAE shaping function shown in Fig. 3.6 is used.

Comparing cases 1 and 2, we can see the advantage of mismatching for minimum $\Delta\phi$. Here the EVM is significantly improved without any drop in PAE and a small reduction in gain. If we compare cases 2 and 3 we can see the advantage of mismatching the source and load impedances. Case 3 shows the best EVM, with a reduction in PAE and gain due to the source and load impedance mismatch. However, to achieve an EVM of 5% with the Case 2 design, it would be necessary to back the PA off by over 4 dB from the output power of Case 3. At an EVM of 5%, Case 3 has a PAE 14% points greater than the PAE of Case 2. Additionally, the performance of Case 3 is less

Table 3.2: Simulated Average PAE, Gain, P_{out}, and EVM for the Three Cases with Static 28 V, Continuous, and Discrete Drain Supplies. The Values are Obtained at a Fixed Output Power of 27 dBm (Left) and a Fixed EVM of 5% (Right).

	Fixed P_{out} of 27 dBm			Fixed EVM of 5%		
Case	$\overline{\boldsymbol{PAE}}$	$\overline{\boldsymbol{Gain}}$	$\overline{\boldsymbol{EVM}}$	$\overline{\boldsymbol{PAE}}$	$\overline{\boldsymbol{Gain}}$	$\overline{\boldsymbol{P_{\text{out}}}}$
Static 28 V Drain Supply						
1	21.1	20.2	4.2	23.4	20.2	27.5
2	21.5	14.3	2.2	31.6	14.0	29.0
3	15.9	13.9	0.9	31.5	13.7	31.5
Continuous Drain Modulation						
1	42.6	13.7	32.2	17.8	12.2	22.0
2	43.7	9.3	11.1	26.3	8.8	23.8
3	34.2	9.3	3.3	36.6	9.25	27.5
Discrete 4-level 100 MHz Drain Modulation						
1	42.1	14.2	35.2	16.1	12.3	21.6
2	42.7	10.2	14.0	21.6	9.2	22.9
3	34.3	9.3	4.0	34.5	9.3	27.1
Discrete 4-level 25 MHz Drain Modulation						
1	39.2	15.0	42.5	15.3	12.3	21.3
2	38.7	10.8	17.8	18.5	9.2	22.2
3	33.9	9.4	5.5	32.4	9.4	26.6

affected by supply modulator bandwidth limitations. At 27.0 dBm of output power, limiting the discrete switching speed to 25 MHz degrades the EVM of Case 1 and 2 by 10.3% points and 6.8% points when compared to the continuous drain voltage, alternatively the EVM of Case 3 is reduced by only 2.2% points. The PAE, gain, P_{out}, and EVM values are summarized in Table 3.2 and evaluated using two criteria. The first is with a fixed output power of 27 dBm, and the second is a fixed EVM of 5%. Note that the signal bandwidth is almost three times greater than the switching frequency of 25 MHz, and these results are obtained without the use of DPD.

The discrete drain voltage amplitude statistics are a function of average input power. At low power levels, the PA operates at its lowest drain voltage level and only switches to higher voltages when necessary. At medium average powers, all four voltage levels are used so the PA sees the full range of gain magnitude and phase variation. Here the EVM peaks and then drops at higher

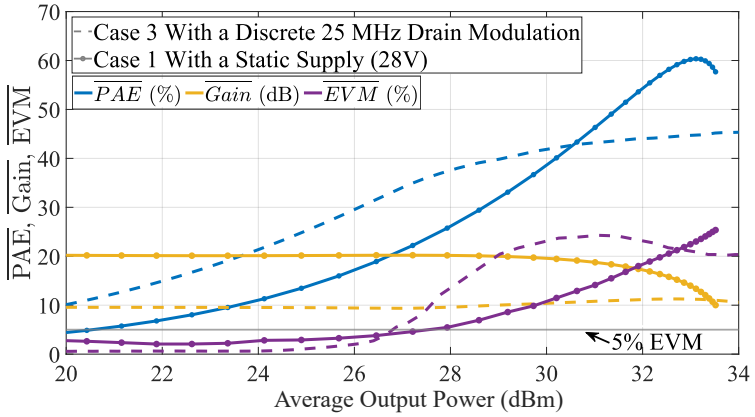


Figure 3.8: Simulated comparison between a conventional PA design (Case 1) with a static drain supply and a low gain variation PA design (Case 3) with a discretely supply modulated supply at a carrier frequency of 9 GHz. The dynamic supply has a maximum switching of 25 MHz.

power levels where the PA operates at the highest voltage for the majority of the time, converging to the static 28 V supply case. However, at these high average power levels, the EVM is beyond an acceptable value.

A comparison between the conventional PA design (Case 1) with a static 28 V supply and a low gain variation design (Case 3) with discrete 25 MHz drain modulation is shown in Fig. 3.8. At 27 dBm of average output power, both cases show the same EVM; however, the PAE of Case 3 is 12.4% points higher. This demonstrates that a PA that is deliberately mismatched for linearity can beat a conventional, efficiency optimized, static supply PA using discrete supply modulation.

3.3 PA Design and Characterization

3.3.1 PA design

The deliberate mismatch approach of the previous sections is now used to design a two-stage GaN MMIC PA covering 6 to 12 GHz with a minimum of 5 W of peak CW output power across the band. Furthermore, since Case 3 gives the best trade-off between PAE and EVM as shown in section 3.2.2, the source and load impedances of the final stage are chosen to minimize small signal $\Delta|G|$ and thus are identical to the impedances of Case 3 at 9 GHz.

The MMIC PA is designed in the WIN Semiconductors NP15 process and is shown in Fig. 3.9.

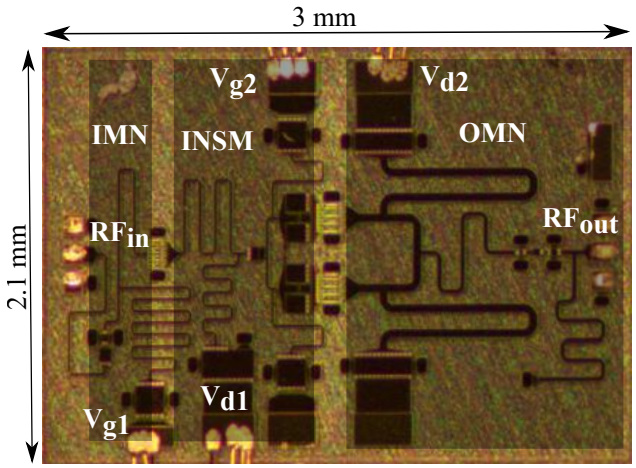


Figure 3.9: Photograph of 6 to 12 GHz MMIC PA fabricated in the WIN Semiconductor GaN on SiC NP15 150 nm process.

This process targets mm-wave power applications through 40GHz. The gate length is 0.15 um and is manufactured on 100 um SiC substrates. A source-coupled field plate design is used to provide the high breakdown voltage required for reliable operation at a V_{ds} of 28 V. This process features two interconnect metal layers, high-reliability MIM capacitors, precision TaN resistors, and through-substrate vias for low inductance ground connections. The periphery of the first stage is a single $8\times50\,\mu$m device biased near class-B operation with 8 mA of quiescent current at a fixed drain voltage of 28 V. The second stage consists of two reactively combined $8\times100\,\mu$m devices, each biased with a current of 80 mA. The staging ratio is 4:1. The PA is designed to operate the first stage with a fixed drain voltage while the second stage drain is supply modulated from 14 to 28 V. Supply modulating only the output stage improves the PA $\Delta|G|$ and $\Delta\phi$. The efficiency is improved by biasing the first stage in deep class-B and reducing the current consumption at backed-off power levels. In addition, by including a first stage with a fixed drain supply, this allows the second stage input to be mismatched through the inter-stage matching network, and the first stage input matched to 50 Ω. Therefore, the total PA is well matched to 50 Ω with an overall low gain magnitude/phase variation. The devices are reactively matched using lumped capacitors and transmission lines. The octave bandwidth output matching network (OMN) is designed using a filter synthesis matching technique which results in minimal insertion loss and incorporates the drain bias line and blocking

capacitor into the OMN as described in [122] [123]. A series resistor is placed at the gate of the first-stage transistor to improve stability and input return loss. The second stage has a parallel RC stability network at the gate of each transistor with an added small series resistor at the gate manifold. Additionally, an odd-mode stability resistor is placed between the gates of these two devices.

3.3.2 Small-Signal Simulations and Measurements

The measured and simulated S-parameters of the PA in Fig. 3.10 at a drain voltage of 28 V show good agreement. The measured $|S_{21}|$ peaks at 7.7 GHz with 25.7 dB of gain, and remains above 15 dB from 5.9 to 12.5 GHz. The measured $|S_{11}|$ is less than -10 dB from 5.6 to 12.7 GHz.

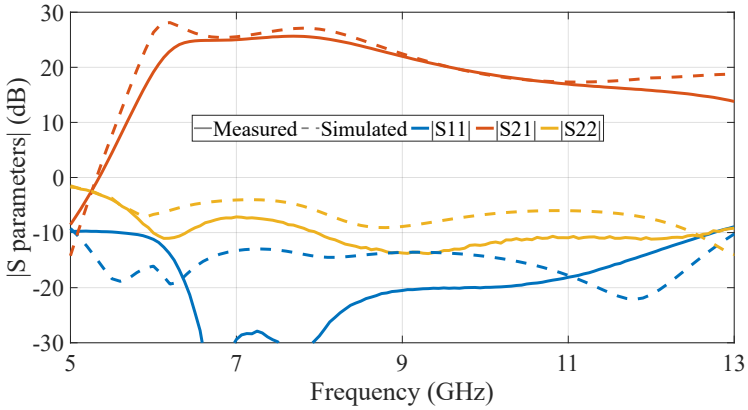


Figure 3.10: Measured and simulated S-parameters of the fabricated low gain variation PA at a drain voltage of 28 V

The simulated and measured gain variation for a supply voltage sweep of 14 to 28 V is shown in Fig. 3.11. At lower frequencies, the $\Delta|G|$ is particularly low and remains below 1 dB from 6 to 7.5 GHz, however, at these frequencies, the $\Delta\phi$ is high. From 8.9 to 13 GHz, the $\Delta\phi$ is low ($<15°$), however the $\Delta|G|$ is higher (>2.2 dB). This seemingly inverse relationship between $\Delta|G|$ and $\Delta\phi$ is consistent with source-pull results in Fig. 3.4 and results in an approximately flat ΔG across frequency as shown in Fig. 3.11c. The $\Delta|G|$, $\Delta\phi$, and ΔG are also predicted from the simulated input and output impedances presented to the final stage of a single device and are shown in Fig. 3.11. The impedances are determined by replacing the final stage PA transistors with

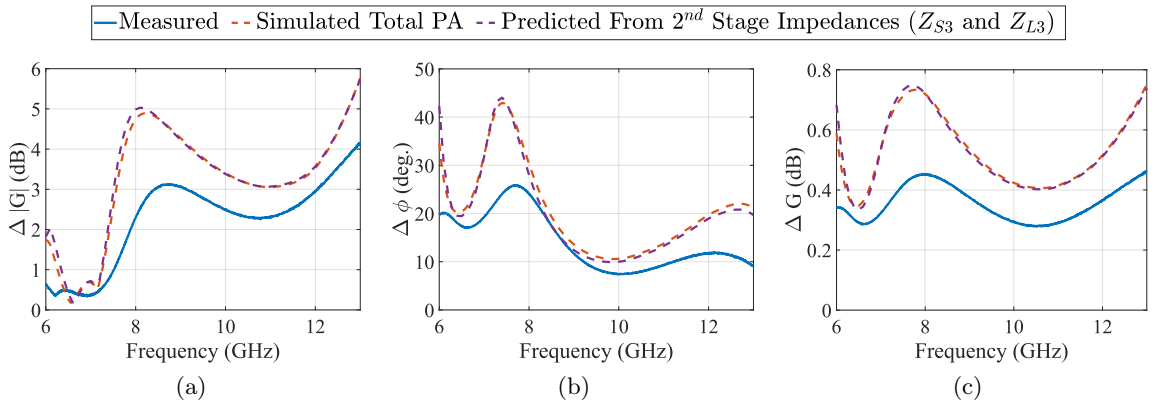


Figure 3.11: Measured and simulated small signal (a) gain magnitude variation ($\Delta|G|$), (b) gain phase variation ($\Delta\phi$), and (c) normalized complex gain variation (ΔG) vs frequency over a 14 to 28 V range. The predicted gain variation is calculated by implementing the input/output impedance as ideal tuners and cascading them with S-parameters of the final stage transistor at multiple drain voltages as described in section 3.2.1.

simulation ports at the gate and drain side. Since the final stage is power combined, the impedance must be determined assuming a symmetrical power split and even mode excitation [124]. Once the impedances are simulated, they are implemented as ideal tuners and cascaded with the transistor S-parameters at multiple drain voltages as demonstrated in section 3.2.1. The input stability network is separately simulated and cascaded so that the loss can be added appropriately and the PAs stabilized. The $\Delta|G|$, $\Delta\phi$, and ΔG are then determined from the total cascaded network. Since the first-stage drain bias is fixed, it does not contribute to the gain variation. The results obtained from this approach are practically identical to the gain variation found from the total simulated S_{21} of the PA (Fig. 3.11), with the small deviations likely caused by the asymmetry in the interstage and output matching networks.

3.3.3 Large-Signal Simulations and Measurements

The PA is mounted on a copper-molybdenum (CuMo) carrier and measured on a probe station. Large-signal amplitude and phase measurements from 6 to 13 GHz in 0.1 GHz steps as a function of input power and drain voltage are shown in Fig. 3.12a when a max-PAE shaping function at 9 GHz is applied. The phase is plotted vs. output power at multiple drain voltages in Fig. 3.12b. The PAE, Gain, output power, and input power are shown vs. frequency in Fig. 3.13

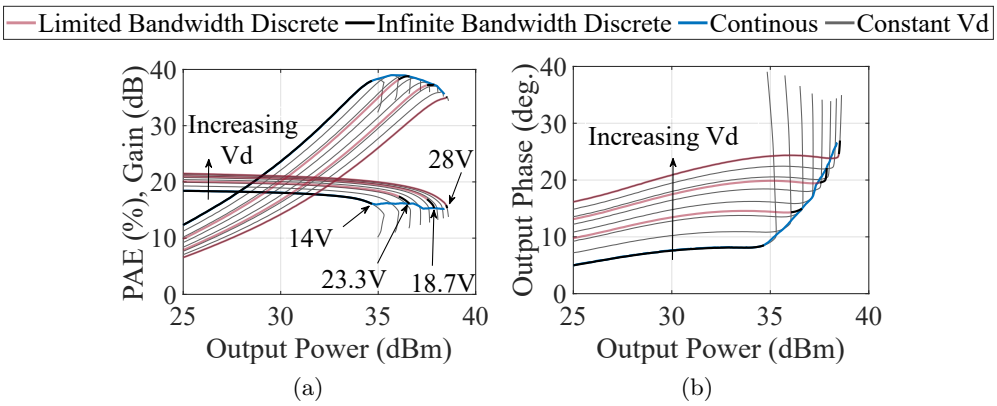


Figure 3.12: Measured CW PAE, gain, and phase plotted vs output power at 9 GHz and drain voltages ranging from 14 to 28 V in 2 V steps.

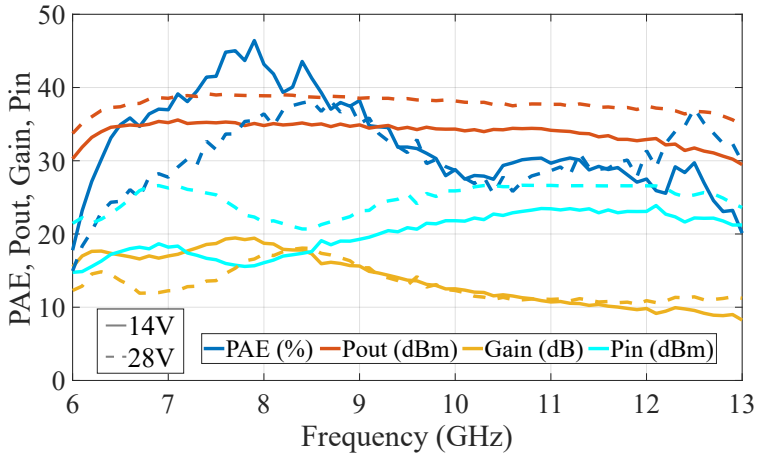


Figure 3.13: PAE, gain, output power, and input power vs frequency at drain voltages of 14 and 28 V. Here the input power is selected to yield the highest PAE at each frequency point.

at drain voltages of 14 and 28 V. At 9 GHz, the PAE peaks at 39.0% at a drain voltage of 16 V. The PAE peaks at a low drain voltage due to the load mismatch. Small-signal trends in $\Delta\phi$ are a good predictor for large-signal behavior, although the large-signal $\Delta\phi$ at 9 GHz of 24.9° is higher than the small-signal value. From 6.2 to 12.6 GHz, the PAE exceeds 25.6% at 14 V, with a peak PAE of 46.4% at 7.9 GHz and the output power is greater than 36.0 dBm at 28 V.

3.4 Modulated Drain Voltage Measurements and Experimental Validation

The PA is next integrated with a discrete 4-level MMIC supply modulator fabricated in the same WIN GaN on SiC process, similar to the architecture in [109]. This discrete supply modulator is a multi-level architecture that uses transistor switches to apply four different externally generated

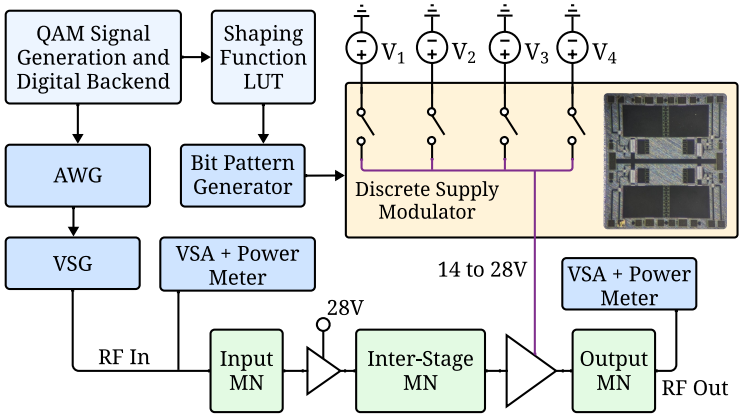


Figure 3.14: System block diagram of the measurement system

voltage levels with over 80% efficiency. The high electron mobility and low parasitics in the MMIC process provide higher switching speeds than commercial off-the-shelf transistors. Thus enabling the modulator to track higher signal bandwidths. The device size of each switch is $23\times100\,\mu$m, chosen as a tradeoff between R_{on} and the input/output capacitance while being large enough to supply a maximum current of 1 A. The modulator is designed to be integrated with a 10 W PA with a maximum drain voltage of 28 V. A block diagram of the testbench with a photo of the MMIC supply modulator is shown in Fig. 3.14. The maximum PAE discrete shaping functions chosen for this PA and used for the measurements reported in the next section are plotted in Fig. 3.15 at 6.5, 9, and 11.5 GHz.

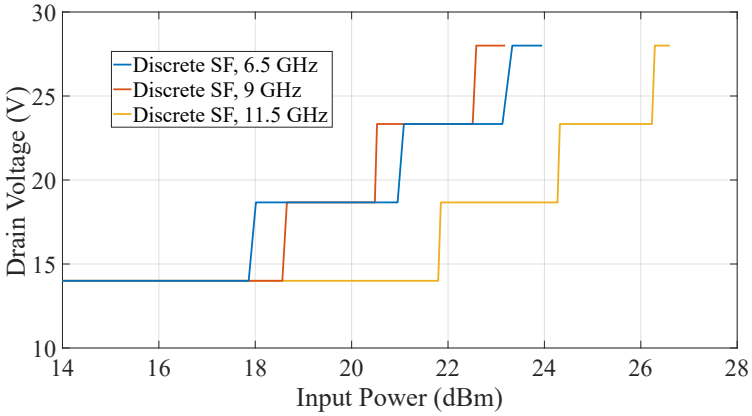


Figure 3.15: Discrete shaping functions of the PA at 6.5, 9, and 11.5 GHz.

A 67.5 MHz 64-QAM signal is generated using an arbitrary waveform generator (AWG), this baseband signal is then upconverted through a vector signal generator (VSG), amplified with a driver, and applied to the input of the PA. Directional couplers on the input and output allow the power, spectrum, and IQ baseband waveforms to be measured. The dynamic drain voltage is programmed into a bit pattern generator that controls the switches of the discrete supply modulator. The output of the supply modulator is connected to the second-stage drain supply of the PA through a low inductance/capacitance interconnect. Additionally, the baseband signal and drain voltage waveforms are aligned by applying a delay to the trigger of the AWG. Details on the alignment process can be found in [46]. The PA is mounted on a CuMo carrier with 50 Ω alumina lines on the input/output. These alumina lines extend to the edge of the CuMo carrier, where micro-strip-to-coax transitions connect. The loss and mismatch due to the alumina lines, bond wires, and transitions result in approximately 1 dB lower gain than when measured on the probe station.

3.4.1 Discrete Supply Modulated Results

The PA is measured with a dynamic drain voltage and compared to the case of a static 28 V drain voltage using the 67.5 MHz 64-QAM signal from section 3.2.2. The efficiency, gain, EVM, and right-side adjacent channel power ratio (ACPR) are shown in Fig. 3.16 plotted vs. output power with the maximum switching frequency of the supply modulator set to 100 MHz. The ACPR is calculated using a 8.85 MHz guard band between 50 MHz channels. The composite power added efficiency (CPAE) takes into account the efficiency of the supply modulator and the PA, and the PAE refers to the efficiency of the PA with the supply modulator losses de-embedded. Both efficiencies are averaged over one signal period. With a dynamic drain supply, the peak PAE and CPAE improvement is 10.6% points and 6.8% points occurring at an output power of 31 dBm while the gain, EVM, and ACPR are degraded by 2.8 dB, 1.7% points, and 3.7 dB, respectively.

Using the custom envelope simulator presented in section 3.2.2, the PAE, gain, output power, EVM, and ACPR can be predicted with high accuracy. In this section, the envelope simulator uses measured CW large-signal probe-station data presented in section 3.3.3. The measured and

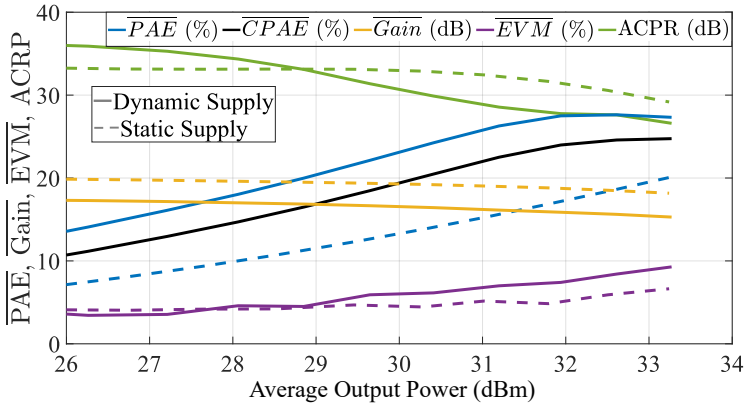


Figure 3.16: Measured PA performance with a static 28 V supply and a dynamically changing supply at 9 GHz is shown in (a).

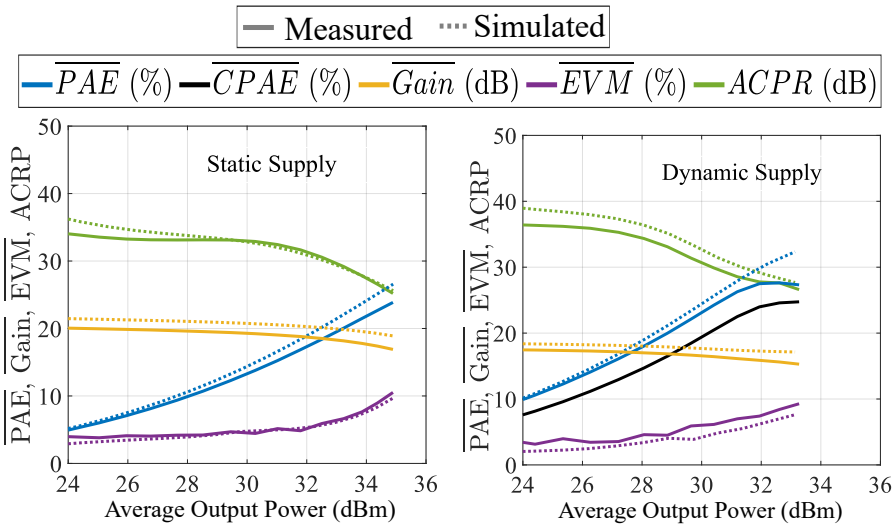
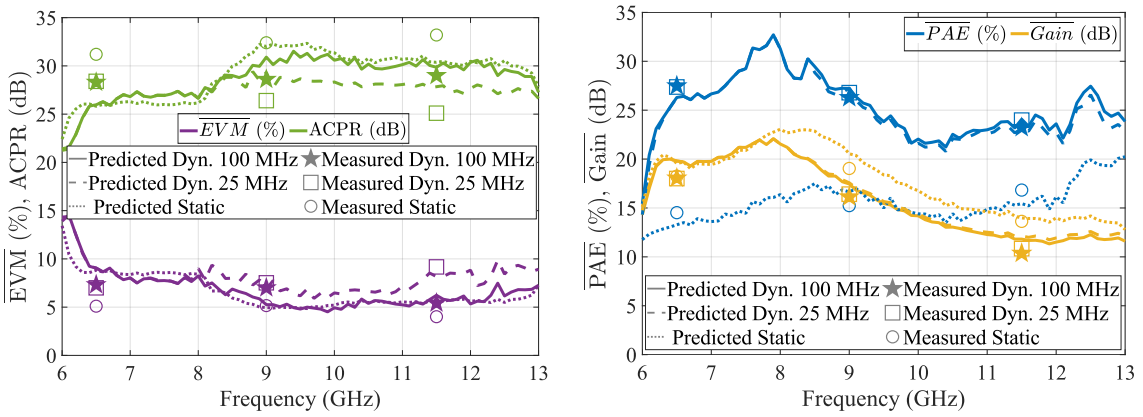


Figure 3.17: Comparison of predicted and measured PA efficiency and linearity at 9 GHz with (a) static 28 V supply and (b) dynamically changing four-level supply with a maximum switching frequency of 100 MHz.

predicted PAE, Gain, EVM, and ACPR are compared to a static 28 V supply in Fig. 3.17a, and dynamic supply switching at a maximum of 100 MHz in Fig. 3.17b. In both cases, we see good agreement between the predicted and measured linearity and PAE. Since the simulated results are derived from large-signal on-wafer measurements, the gain is slightly higher than the measured data, which uses a wire-bonded coaxially-connected MMIC PA.

The envelope simulator is used to predict supply modulation results from 6 to 13 GHz as



(a) (b)

Figure 3.18: Measured and predicted results comparing a static 28 V supply to a dynamically changing drain supply with two maximum switching frequencies of 100 MHz and 25 MHz in terms of (a) linearity and (b) PAE and gain, for a constant output power of 31 dBm. The measured points are plotted at frequencies of 6.5, 9, and 11.5 GHz for the static (circle symbols) and dynamic 100 MHz (star symbol) and 25 MHz (square symbol) drain voltage cases.

shown in Fig. 3.18. Across frequency, the input power is adjusted to obtain a constant output power of 31 dBm. The discrete supply modulator is limited to maximum switching frequencies of 100 MHz (greater than the signal bandwidth) and 25 MHz (about three times lower than the signal bandwidth). The EVM and ACPR are shown in Fig. 3.18a. The PAE and gain are shown in Fig. 3.18b. The measured points are plotted at frequencies of 6.5, 9, and 11.5 GHz for the static and dynamic drain voltage cases. In Fig. 3.18, we see that with a switching frequency of 100 MHz, the EVM is nearly the same as the static supply case across the band, and at some frequencies, shows an improvement in EVM. The PAE is nearly the same for the two switching speeds and is improved at all frequencies over the static case, with the largest improvement occurring at the lower frequencies (6 to 9 GHz). The EVM is degraded with the slower switching speed but remains below 10%.

3.5 Summary

In transmitters that use discrete supply modulation for efficiency enhancement, the bandwidth of the drain supply modulator is often limited. The supply modulator's limited switching

speed and discretized voltage distort the PA gain magnitude and phase, adding to AM-AM and AM-PM non-linearities. This chapter demonstrates that the distortion can be reduced by mismatching the input and output impedance. This is first shown in the simulated source/load pull of a standalone transistor, from which three different matching cases are examined through simulations. Comparing these cases in simulation using a custom behavioral model and a 64-QAM 67.5 MHz signal, it is shown that a PA with intentionally mismatched input and output impedances is more efficient than a conventional PA when using discrete bandwidth–limited supply modulation for the same 5% EVM limit. Additionally, envelope simulations reveal that bandwidth limitations on the supply have a larger impact on error vector magnitude than on PAE, gain, and output power. The comparison between the three cases shows that non-linearities created from bandwidth limitations in the supply can be reduced through mismatching for low gain variation.

To validate simulation results and the advantage of designing for low gain variation, a two-stage 5 W GaN on SiC MMIC PA is fabricated, covering a bandwidth of 6.2 to 12.6 GHz with intentionally mismatched source and load impedances of the final stage. S-parameter measurements show low small signal gain variation across drain voltage, which holds for the entire bandwidth and is accurately predicted from the input/output impedances presented to the final stage of the PA. The PA is measured with a 67.5 MHz 64-QAM signal with a dynamic drain voltage generated from a four-level discrete GaN MMIC supply modulator. The measured PAE, gain, and linearity are compared to predicted results from the behavioral model envelope simulator, which shows good agreement. In conclusion, matching PAs for low gain magnitude and phase variation instead of maximum PAE and gain can improve the linearity and efficiency of a transmitter with discrete supply modulation, even for signals that have a high bandwidth relative to that of the supply modulator and without the aid of digital pre-distortion. The results presented in this chapter are reported in [80].

Chapter 4

High Power Discrete Supply Modulator Design and Characterization

4.1 Introduction

Chapter 3 discussed of design of PAs for high performance in a supply-modulated system. An equally important component of a supply modulation system is the dynamic supply modulator. The requirements of a supply modulator were discussed in chapter 2, but the details of a practical design were not included. Furthermore, supply modulating an array of multiple PAs with a shared drain supply from a single modulator has the additional requirement of high power. Achieving high power, high switching speed (bandwidth), high efficiency, and low distortion requires careful device selection, layout, and thermal management. Each of these topics is discussed in this chapter, which presents a supply modulator designed to deliver a peak output power of 1 kW.

4.1.1 Survey of Published Supply Modulators

The supply modulator architecture and technology choice can have a substantial impact on system performance. To begin the design, a survey of the state-of-the-art high power supply modulators is performed and summarized in Table 4.1. As mentioned in chapter 2, supply modulators can generate continuous or discrete voltage waveforms. Continuous supply modulators such as buck converters have been demonstrated with switching frequencies up to 865 MHz [67,68,70,86,87,125,126]. However, these supply modulators must switch at frequencies a few times greater than the signal envelope bandwidth [112] and the efficiency of all switch-based power supplies drops linearly with frequency. Therefore, tracking high bandwidth signals efficiently using a continuous supply mod-

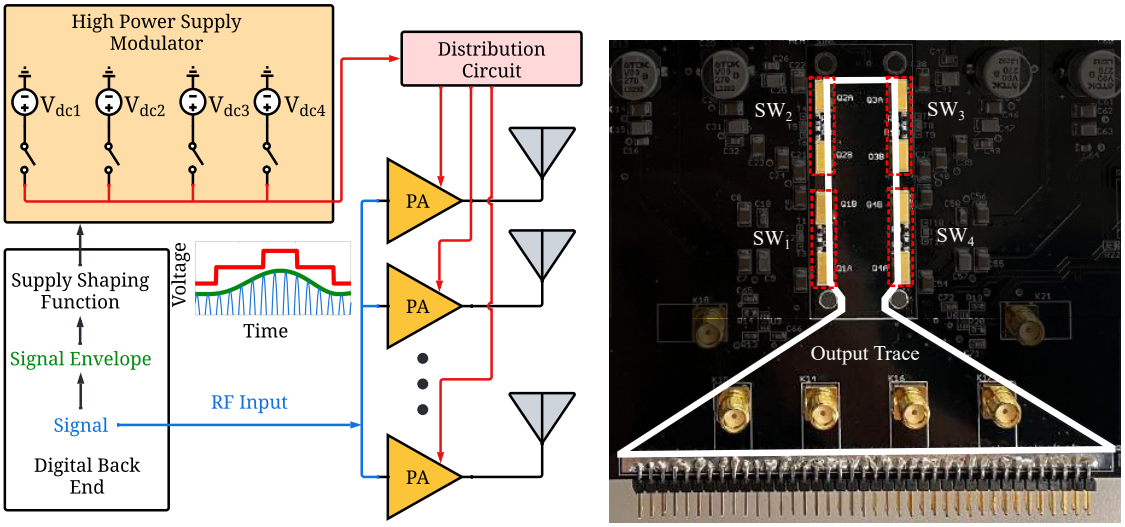


Figure 4.1: (a) Block diagram of a high power supply modulator simultaneously feeding several power amplifiers in parallel. The signal envelope (shown in green) is digitally processed through a shaping function which determines the switch timing and output waveform of the supply modulator. (b) Photograph of the four-level discrete supply modulator with the output trace highlighted and transistor switches labeled. Each switch consists of two transistors in parallel.

ulator becomes challenging. An additional example of a continuous supply modulator is a linear regulator. These typically utilize op-amps and can track high bandwidths. However, linear regulators have very low efficiency and substantially degrade system efficiency.

Discrete supply modulation architectures such as multi-level converters (MLC) [63, 65, 109, 110, 127–132] switch between several discrete voltage levels. The primary advantage of discrete supply modulation is that it has fewer switching instances than continuous supply modulation, which boosts the efficiency of the supply modulator. Furthermore, the discrete waveform has a lower bandwidth than its continuous counterpart and enables accurate tracking of higher signal bandwidths, at the expense of some distortion to the PA, which can be corrected through digital predistortion [65], or by designing the PA for low gain variation as presented in chapter 3. Increasing the number of voltage levels produces a closer approximation to continuous supply modulation. However, a high number of voltage levels adds complexity and increases the number of switching instances which degrades efficiency. Due to the bandwidth and efficiency advantages of discrete supply modulation, a multi-level converter architecture is chosen for this design, which switches

between four externally generated voltages. A block diagram of multiple PAs with a dynamic drain supply being generated from a single discrete supply is shown in Fig. 4.1a. Here, the PAs have a shared drain supply from a single supply modulator, which is controlled digitally. The switches are all connected through an output trace which connects to the PA drain. A photograph of the realized discrete supply modulator is shown in Fig. 4.1b. Here, the output trace outline is highlighted along with the transistor switches.

Supply modulators can be implemented in a monolithic microwave integrated circuit (MMIC) or by using discrete packaged transistors implemented on a printed circuit board (PCB). The transistors used in MMIC foundries are typically designed to be used as common source amplifiers in the microwave frequency range. They have a high electron mobility but are not optimized for low conduction/switching losses when implemented as a switch. Therefore, the switching speed is high, but the overall efficiency is lower than commercial off-the-shelf (COTS) transistors used in conventional power converter designs. MMIC supply modulators [70], [86], [67], [109], [65] can achieve high switching frequencies greater than 100 MHz with an acceptable efficiency typically greater than 80%. However, peak output powers significantly greater than 20 W have not been demonstrated. Higher output powers can be achieved with hybrid PCB topologies [110], [129], [68]; however, this typically comes at the cost of reduced switching speed due to increased parasitics. Therefore, if high power is a priority over switching speed, the PCB hybrid topology is favorable. Some examples of MMIC and hybrid PCB supply modulators are summarized in Table 4.1.

The design and characterization of a high-power discrete supply modulator implemented on a PCB is presented in this chapter. The design requires careful selection of the switching device to optimize switching speed and efficiency, so a survey of commercially available devices is performed in section 4.2. Next, the design of the supply modulator is presented in section 4.3. Measurements of the output voltage waveform revealed significant ringing upon each voltage level transition due to parasitics in the output trace and transistor switches. In order to model this ringing, the S-parameters of the output trace are simulated in a method-of-moments solver and converted to an RLC equivalent circuit in section 4.4. This model is used to accurately predict the ringing of the

Table 4.1: Key specifications of state-of-the-art continuous and discrete supply modulators with peak output powers up to 500 W in GaN and MOSFET technologies

Type	**Tech.**	**Package**	**Peak Pout (W)**	**Eff. (%)**	**Test Signal/Peak Switching Frequency**	**Ref.**
Buck	GaN	MMIC	16	72.5	NA/400 MHz	[86]
Buck	GaN	MMIC	10	> 90	3 MHz WCDMA/40 MHz	[67]
Buck	GaN	Hybrid	50	> 90	NA/1 MHz	[87]
Buck	GaN	Hybrid	68	92.3	20 MHz LTE/25 MHz	[125]
Buck (3 level)	GaN	Hybrid	115	> 90	20 MHz LTE/25 MHz	[68]
Buck	GaN	MMIC	> 7.5	> 80	NA/865 MHz	[70]
MLC (4 level)	GaN	MMIC	3.5*	88.2	20 MHz LTE/40 MHz***	[109]
MLC and LR	GaN	Hybrid	40	75	5 MHz 64-QAM/1 MHz	[127]
8 Level DAC	GaN	Hybrid	159	84.5	10 MHz LTE/NA	[110]
8 Level DAC	GaN	MMIC	20	85-95	20 MHz LTE/NA	[65]
MLC and LR	MOSFET	Hybrid	50	75.5	1 MHz sine/100 kHz	[128]
Multi-Level Buck	GaN	Hybrid	500	93	400 kHz multi-tone/1 MHz	[129]
MLC and LR	MOSFET	Hybrid	50	79.7	300 kHz sine/NA	[130]
MLC (2 level)	GaN	Hybrid	62	82-92	40 MHz OFDM/100 MHz	[131]
MLC (3 level)	GaN	Hybrid	20.6**	NA	120 MHz OFDM/400 MHz***	[63]
MLC (4 level)	**GaN**	**Hybrid**	**800**	**> 94**	**8 MHz 64-QAM/10 MHz**	**This Work**

*average Pout, **average Pout derived from data in paper, ***derived from minimum pulse width, Linear Regulator (LR)

output voltage in LTspice time domain simulations. The supply modulator is then characterized with different load impedances in section 4.5 using a test signal that switches between each level with an equal duty cycle and while tracking the envelope of a 6.25 MHz 64-QAM signal. The peak measured output power is 800 W of peak power at 20 V, with a maximum switching frequency of 10 MHz.

4.2 High Power Transistor Survey and Comparison

The most critical component of a high-power multi-level converter (HPMLC) design is the choice of the switching transistor. It is desirable to use a transistor with a low on-state resistance (R_{on}), minimal input and output capacitance (C_{in}, C_{out}), and small rise/fall times (<10 ns). Furthermore, in high power, low voltage applications, a high maximum drain current ($I_{\text{d-max}}$) is

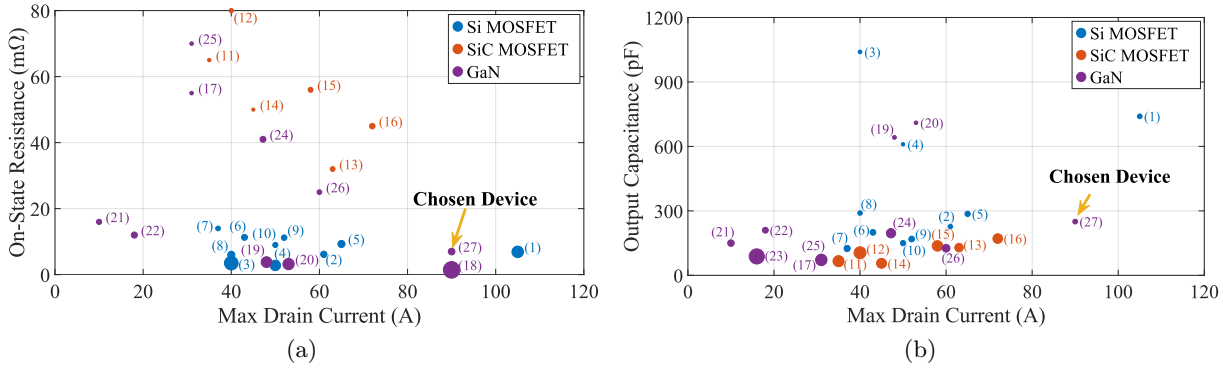


Figure 4.2: (a) On-state resistance vs maximum drain current and (b) output capacitance vs maximum drain current for commercially available transistors in MOSFET, SiC MOSFET, and GaN technologies. The size of each point in (a) is proportional to the device C_{out} and in (b) R_{on}. Numbers refer to TABLE 4.2.

necessary. Unfortunately, these parameters are often at odds with each other. For instance, a low R_{on} with high $I_{\text{d-max}}$ can be obtained by stacking many devices in parallel, however, this increases the capacitance and lowers the switching speed of the device.

In order to weigh these trade-offs, a survey and comparison of commercially available high-power transistors are performed to assist in switching device choice. This study examines silicon (Si) MOSFET, silicon carbide (SiC) MOSFET, and gallium nitride (GaN) HEMT technologies while specifically targeting devices with low C_{out} and R_{on}. The R_{on} is plotted against $I_{\text{d-max}}$ for each surveyed device in Fig. 4.2a where the area of each dot is proportional to the device C_{out}. In addition, the C_{out} is plotted against $I_{\text{d-max}}$ in Fig. 4.2b where the area of each dot is proportional to the device R_{on}. The surveyed devices all have breakdown voltages greater than 25 V, which is consistent with the required drain supply voltage of GaN HEMT power amplifier devices. All the values of the survey were obtained directly from the manufacturer's device datasheet. The specifications of the devices used in this comparison are given in Table 4.2.

From Fig. 4.2, it is apparent that SiC MOSFET devices consistently have the smallest C_{out}. However, they suffer from a relatively large R_{on}. The small C_{out} of SiC devices is partially a result of the capacitance of these devices being specified at very high voltages (>600 V). The Si MOSFET devices are competitive with GaN both in terms of C_{out} and R_{on}, however, the intrinsic

body diode built into the MOSFET structure would result in reverse conduction if used in a multi-level converter. A common approach to preventing reverse conduction due to the body diode is to place an external diode in series with all but the highest voltage level switch [63]. However, for high-current applications, this is not a feasible solution since the losses in a diode scale with current, not voltage and substantially degrade the efficiency, making MOSFET structures an undesirable choice.

An alternative to Si MOSFET devices are E-mode GaN HEMTs which do not have an intrinsic body diode. For GaN devices, reverse conduction can, however, still occur in GaN devices when the gate-drain voltage exceeds the device threshold voltage and the drain-source voltage is negative. Therefore, in order to ensure that reverse conduction does not occur in a device that is intended to be biased off, it is necessary to make the nominal off-state gate voltage less than the lowest voltage level plus the threshold voltage. Unfortunately, GaN devices can fail when they exceed the minimum gate-to-source voltage ($V_{\mathrm{gs,min}}$). This enforces a limit on the range of output voltages which is defined as:

$$\Delta V_{\mathrm{out}} = V_{\mathrm{out,max}} - V_{\mathrm{out,min}} \leq |V_{\mathrm{gs,min}}| + V_{\mathrm{th}}, \tag{4.1}$$

where $V_{\mathrm{out,max}}$ and $V_{\mathrm{out,min}}$ are the maximum and minimum output voltages, respectively and V_{th} is the threshold voltage.

To illustrate this limitation, an example of a two-level modulator with ideal switches is shown in Fig. 4.3 and Fig. 4.4. Here E-mode transistors are used, the threshold voltage is 0 V, and $V_{\mathrm{gs,min}}$ is -10 V. The gate, source, and drain (output) voltages are labeled and referenced to ground. The drain terminal of the transistor switches are connected through the output trace of the supply modulator. A photo of the realized output trace is shown in Fig. 4.1b. The example in Fig. 4.3 violates Eq. 4.1 and switches between 5 V and 20 V, a voltage range of 15 V. In the left-hand case of Fig. 4.3, SW_2 is intended to be biased-on and apply the 5 V level. However, the gate voltage of SW_1 is set to 10 V, so when the output voltage reaches 10 V or lower, SW_1 will turn on because the

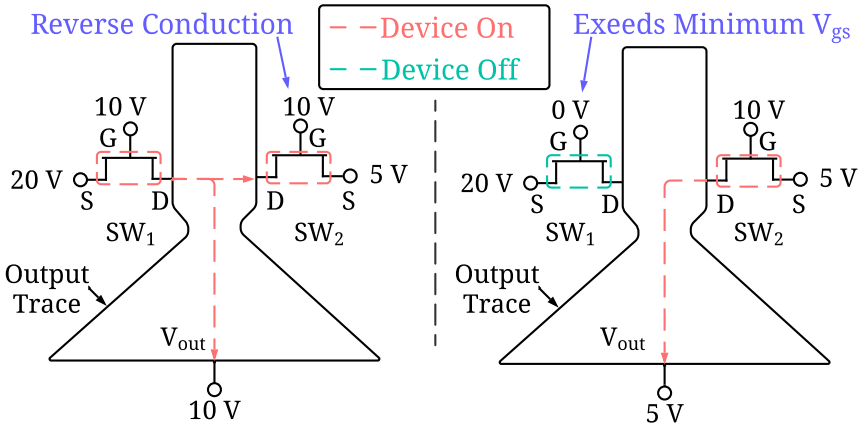


Figure 4.3: Cartoon of a two-level supply modulator switching between 20 V (left) and 5 V (right) voltage levels with $V_{\text{gs,min}}$ equal to 10 V. The modulator fails since ΔV_{out} exceeds $V_{\text{gs,min}}$ and violates Eq. 4.1

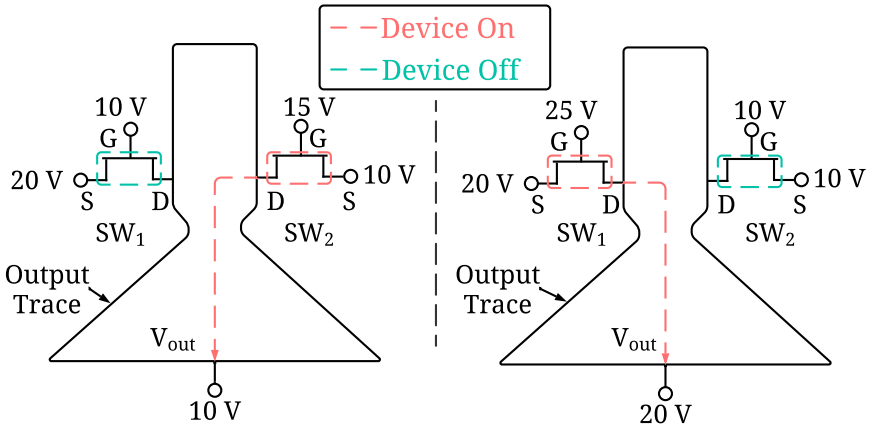


Figure 4.4: Cartoon of a two-level supply modulator switching between 20 V (left) and 10 V (right) voltage levels with $V_{\text{gs,min}}$ equal to 10 V. The modulator operates normally since ΔV_{out} is limited to $V_{\text{gs,min}}$

gate-drain voltage is positive and create reverse conduction in SW_2. This issue could be alleviated by reducing the gate voltage of SW_1 to 0 V as is the case in the right-hand example in Fig. 4.3. However, in this example, the gate-source voltage is -20 V, and below the minimum gate-source voltage of -10 V, which will damage the device. In Fig. 4.4 the voltage range (ΔV_{out}) is limited to 10 V ($|V_{\text{gs,min}}|$) and the converter operates successfully in both switching states, outputting the 10 V level in the left-hand case and the 20 V level on the right-hand case.

Ultimately, the chosen device is a GaN HEMT manufactured by GaN Systems (GS61008T)

Table 4.2: Key parameters of the Si MOSFET, GaN, and SiC MOSFET transistors with $I_{\mathrm{d-max}}$ ranging from 10 to 105 A and a minimum V_{br} of 25 V. The associated R_{on} and C_{out} is plotted vs $I_{\mathrm{d-max}}$ in Fig. 4.2

Technology (# in Fig. 4.2)	$I_{\mathrm{d-max}}$ **(A)**	R_{on} (mΩ)	C_{out} (pF)	C_{in} (pF)	**Volt. of $C_{\mathrm{out/in}}$ Spec. (V)**	V_{br} (V)	$V_{\mathrm{gs-min}}$ (V)	T_{rise} **(ns)**	T_{fall} **(ns)**	**Part #**
Si MOSFET (1)	105	6.9	1900	180	20	150	-20	46	6	IPB083N15N5LF
Si MOSFET (2)	61	6.2	227	1006	12	30	-20	NA	NA	PSMN9R0-30YL,115
Si MOSFET (3)	40	3.5	1040	3595	15	30	-16	17	10	SiS476DN
Si MOSFET (4)	50	2.8	610	4750	20	40	-20	9	9	SiR414DP
Si MOSFET (5)	65	9.3	286	422	15	30	-20	8.2	3.2	CSD17527Q5A
Si MOSFET (6)	43	11.3	200	400	12	25	-8	5.4	4.2	MCP87130
Si MOSFET (7)	37	14	125	545	25	30	-10	12.3	9.8	BUK9M17-30E
Si MOSFET (8)	40	6	291	670	12	25	-20	2.2	1.8	BSZ060NE2LS
Si MOSFET (9)	52	11.2	169	1067	25	40	-10	13	9	BUK9Y12-40E
Si MOSFET (10)	50	9	150	680	25	30	-20	8.2	12.5	TSM090N03E
SiC MOSFET (11)	35	65	66	760	600	1700	-8	8	4	C3M0065090J
SiC MOSFET (12)	40	80	105	2250	1000	1200	-10	9	18	C2M0080170P
SiC MOSFET (13)	63	32	129	3357	1000	1200	-8	18	9	C3M0032120K
SiC MOSFET (14)	45	50	56	3825	800	1200	-30	12	15	GA20JT12-263
SiC MOSFET (15)	58	56	137	1762	800	1200	-5	20	10	NVH4L040N120SC1
SiC MOSFET (16)	72	45	171	3672	1000	1700	-5	20	18	C2M0045170D
GaN (17)	31	55	72	380	400	600	-10	8	15	IGO60R070D1
GaN (18)	90	1.45	1530	2150	15	30	-4	NA	NA	EPC2023
GaN (19)	48	3.8	642	1453	50	100	-4	NA	NA	EPC2053
GaN (20)	53	3.2	710	980	20	40	-4	NA	NA	EPC2015
GaN (21)	10	16	150	220	20	40	-4	NA	NA	EPC2014C
GaN (22)	18	12	210	360	50	100	-4	NA	NA	EPC2016C
GaN (23)	16	150	46	720	480	650	-18	4.5	4	TPH3206PSB
GaN (24)	47.2	41	196	1500	400	650	-20	14	12	TP65H035WSQA
GaN (25)	31	70	72	380	400	600	-10	8	15	IGOT60R070D1
GaN (26)	60	25	126	518	400	650	-10	12.4	22	GS66516T
GaN (27)	**90**	**7**	**250**	**600**	**50**	**100**	-10	**NA**	**NA**	**GS61008T**

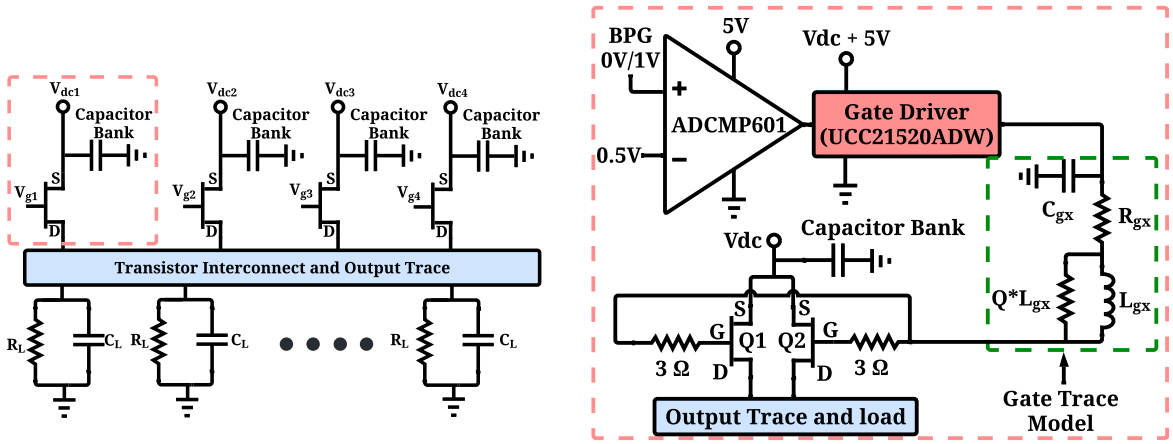


Figure 4.5: (a) Overview schematic of the high power multi-level converter. Each parallel RC circuit represents an individual PA being supply-modulated. (b) Schematic of single switching cell highlighted in the top left of Fig.4.5a. The gate trace is modeled as an RLC circuit with the values extracted from an EM simulation of the trace.

[133]. This device has a $I_{\mathrm{d-max}} = 90\,\mathrm{A}$, $C_{\mathrm{in}} = 600\,\mathrm{pF}$, $C_{\mathrm{out}} = 250\,\mathrm{pF}$, and $R_{\mathrm{on}} = 7\,\mathrm{m\Omega}$. Furthermore, the $V_{\mathrm{gs,min}}$ is $-10\,\mathrm{V}$ and V_{th} is $1.7\,\mathrm{V}$. This device meets the maximum drain current and voltage requirement while maintaining a low input and output capacitance relative to other surveyed GaN HEMTs. Furthermore, the large minimum gate-source voltage that the device can tolerate is much larger than other GaN HEMTs and allows for a dynamic voltage range of the HPMLC of $10\,\mathrm{V}$.

The key specifications of the devices surveyed in Fig. 4.2 are shown in Table 4.2. The GaN devices manufactured by Efficient Power Conversion (EPC) have very low R_{on} values and capacitances competitive with other GaN devices. However, the $V_{\mathrm{gs-min}}$ for EPC devices is $-4\,\mathrm{V}$, which limits the output voltage range of the modulator in the circuit configuration used in this work. Out of all the surveyed GaN devices with a $V_{\mathrm{gs-min}}$ of at least $-10\,\mathrm{V}$, the GaN System device (GS61008T) provides the best R_{on} with reasonable C_{in} and C_{out} values.

Table 4.3: Capacitor, packages, and number of elements in each capacitor bank

Value	**Package**	**Material**	**Number**
33 nF	0805	C0G	2
100 nF	1210	C0G	2
10 µF	1210	X5R	5
270 µF	Radial	Electrolytic	3

4.3 Supply Modulator Design and Simulation

The HPMLC switches between four dc voltage levels, which are generated from external power supplies. A high-level schematic of the HPMLC is shown in Fig. 4.5a; the output is connected to one of four voltage levels by transistor switches. The load consists of N number of parallel RC circuits, each of which represents an individual PA unit. A 10 W PA operating with 50% drain efficiency consumes 20 W of DC power. This supply modulator is designed to feed an array of 50 PA units. Therefore, a target peak instantaneous output power of 1 kW is selected. At a drain voltage of 20 V, this corresponds to 50 A of current required from each transistor switch. The capacitor bank in Fig. 4.5a consists of four different capacitor packages and sizes with the aim of ensuring a stable dc input voltage to each of the GaN devices while the device is switching. The values and part numbers of the implemented bypass capacitors are shown in Table 4.3. By carefully selecting different packages and capacitance values with low equivalent series resistance (ESR) and low equivalent series inductance (ESL), the impedance magnitude seen by the switch devices presented from the capacitor bank remains below 50 mΩ from 300 Hz to 100 MHz.

Fig. 4.5b shows an individual switching cell which is repeated for each of the four voltage levels. Each cell consists of two GaN transistors in parallel. A comparator (ADCMP601) is used to convert the 1 V switch control signal into the 5 V logic level required by the gate driver. The switch control signal is generated externally using a bit pattern generator (BPG) capable of generating synchronized pulses in multiple channels.

The criteria for choosing the gate driver is a required fast rise/fall time (<10 ns) and an output voltage large enough to fully turn on each of the switches (25 V). The chosen gate driver

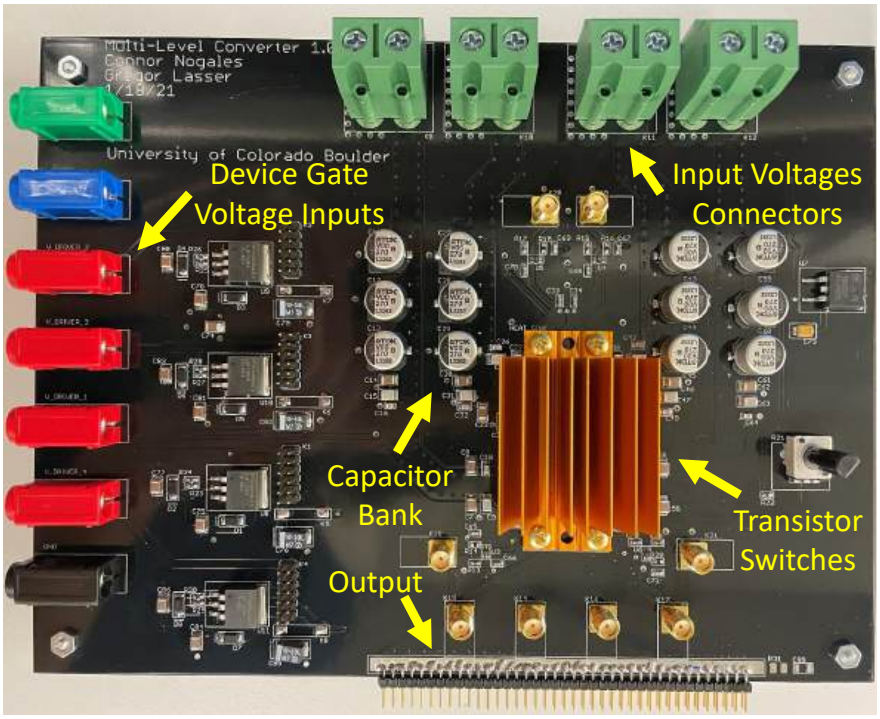


Figure 4.6: Photograph of the high power multi-level converter.

is manufactured by Texas Instruments (UCC21520ADW); it features a rise and fall time of 6 ns and 7 ns respectively with a peak output voltage of 30 V. Furthermore, the input is capacitively isolated from the output, which allows the *on* and *off* output voltages of the gate driver to be set independently of the digital control signal. Thus, for each driver, the *on* voltage is set to 5 V above each switch voltage level and the *off* voltage is set to 10 V in order to ensure that the gate-source voltage does not drop below the minimum of −10 V while also avoiding reverse conduction.

The realized HPMLC shown in Fig. 4.6 is manufactured on a four-layer FR4 board and is populated with commercially available components. In order to maximize current handling and minimize parasitic capacitance and inductance, vias connect the top two layers of the output trace to form the signal path, and the bottom two layers are connected to form the ground path. The GaN switches are located under the bronze-colored heat sink with a sheet of thermal interface material from Laird Technologies (A14692-30) that ensures good thermal contact between the top of the switches and the heat sink.

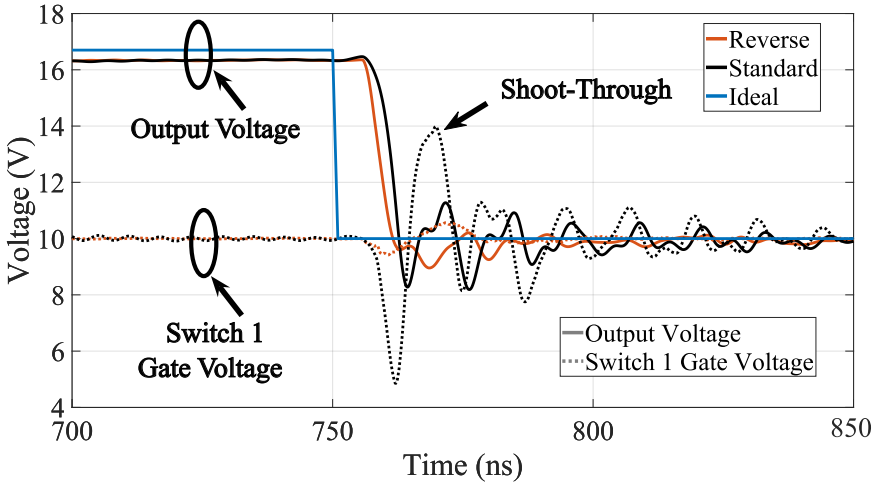


Figure 4.7: Simulated time domain waveforms of the output and switch 1 gate voltages for standard and reverse transistor orientations when transitioning from the switch 2 to switch 4 with an RC load of $(1.25\,\Omega \;||\; 160\,\text{pF})$. Each respective switch voltage is $V_{\text{dc1}} = 20V$, $V_{\text{dc2}} = 16.7V$, $V_{\text{dc3}} = 13.3V$, $V_{\text{dc4}} = 10V$ with the gate turn-on voltage of each switch set to be 5 V above the switch dc voltage.

4.3.1 Reverse Device Operation

In a standard multi-level converter design, the source of each transistor is connected to the output. This topology creates feedback in each device from the output to the gate through the gate-source capacitance. This can create undesired reverse conduction during voltage level transitions when turned-off devices experience a voltage spike on their gate from feedback through the gate-source capacitance. This effect, where two devices are simultaneously biased on is known as shoot-through. From the LTspice model provided by the manufacturer, it is observed that the gate-drain capacitance is an order of magnitude smaller than the gate-source capacitance.

Therefore, in order to investigate the effect that the size of the feed-back capacitor has on the switching waveform, the HPMLC is simulated in a regular configuration with the source connected to the output and in a reverse configuration with the drain connected to the output.

The simulated output voltage, ideal output voltage, and gate voltage of the highest voltage level (20 V) are shown in Fig. 4.7 with the gate and output traces modeled using the technique described in Section 4.4 below. In this simulation, the HPMLC is switched from the second to the highest voltage level (16.6 V) to the lowest level (10 V) and loaded with a medium power load of

1.25 Ω in parallel with 160 pF.

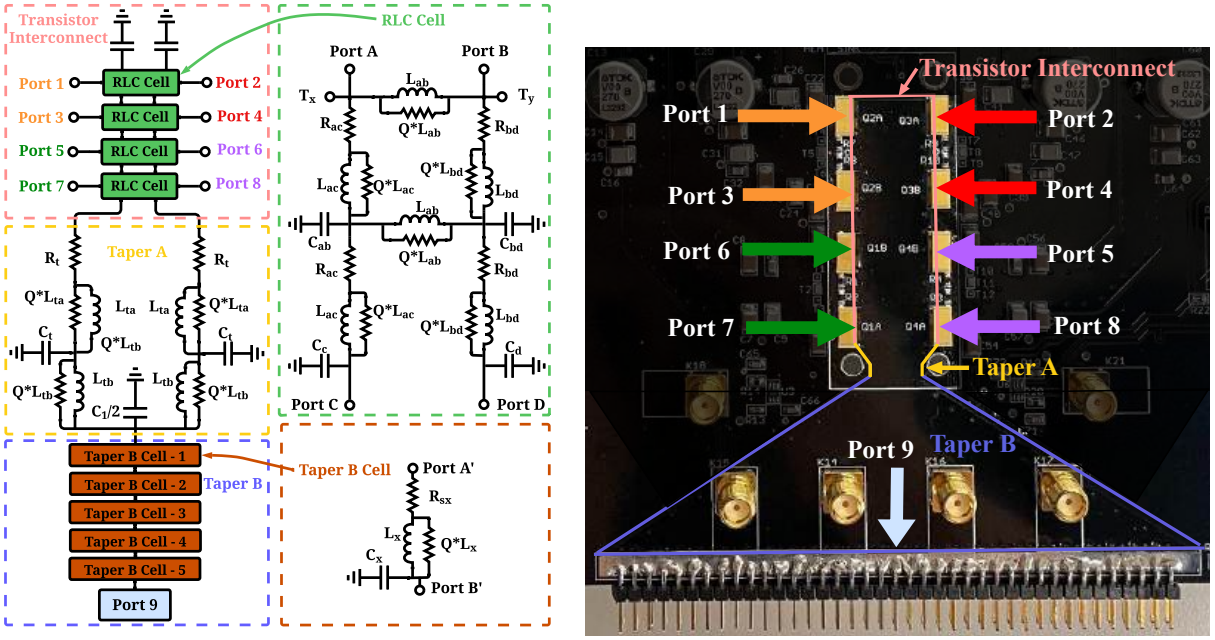
By examining Fig. 4.7 it is clear that when the devices are operated in standard configuration with the source connected to the output, shoot-through occurs when the device is switched to the lowest voltage level. This will distort the output waveform and degrade the efficiency of the converter. In contrast, the flipped configuration results in less feedback from the output to the gate and no shoot-through. Therefore, the HPMLC was designed with the devices implemented in reverse configuration with the drains connected to the output and sources connected to the input dc voltage as seen in Fig. 4.5a.

4.4 Transistor and Output Trace Modeling

The ringing that occurs upon each voltage level transition limits the switching speed of the converter and mixes with the RF signal of the PA. This creates side-bands in the spectrum and degrades the linearity of the PA [3]. The ringing in the HPMLC is created due to parasitics in the transistor and output trace interconnect. If the output trace is modeled as an ideal short, the predicted waveform does not match the measured output voltage as shown in Fig. 4.9a. Therefore, an in-depth model of the output trace is necessary for accurate waveform prediction.

To begin, the output trace was EM simulated in AWR's Axium 2.5D method of moments (MOM) solver from dc to 2 GHz. A port was placed at the location of each transistor and the output, resulting in nine total ports. The aim of this model was to capture the mutual resistance, inductance, and capacitance between each individual transistor and the output. Since the simulated frequency domain S-parameter data cannot be used in time domain simulations in LTspice and automatic extraction of equivalent models did not yield accurate results, the equivalent RLC circuit shown in Fig. 4.8a, with its physical port and section locations shown in Fig. 4.8b was fit to the simulation results in the frequency domain.

The equivalent RLC circuit is split into three parts. Starting from the top of Fig. 4.8b the transistor interconnect is highlighted in pink, followed by taper A which is a bottle neck shaped trace highlighted in yellow, and finally at the bottom is taper B which is a trapezoid-shaped trace



(a) (b)

Figure 4.8: (a) Schematic of RLC output trace model and (b) associated physical location of the ports in the output trace. The trace is split into three parts: the transistor interconnect highlighted in pink, taper A highlighted in yellow, and taper B highlighted in purple

highlighted in purple. Each of these sections is modeled with series resistances, shunt capacitances, and series inductors in parallel with resistors, as shown in Fig. 4.8a. The value of the parallel resistor is the product of the corresponding inductance and a separate Q-factor variable. The Q factor is assumed to be the same across the network in order to reduce the number of variables. The finite Q of the inductors helps the RLC network to match the frequency behavior of the simulated trace, including resonances that occur. The extraction of the RLC values is obtained through two simultaneous goal functions between the EM model and RLC model from dc to 600 MHz. The first fits the S-parameters between the two models in a 50 Ω environment. The second ensures that the dc resistance between ports 1 and 9 matches the simulated dc resistance when ports 2 - 8 are left open.

Since the dc resistance of the trace is critical to accurately predict the dc losses of the HPMLC, it was weighted 15 times higher than the S-parameter goal function. By taking advantage of the vertical symmetry of the output trace, using the same Q value for each parallel RL component, and

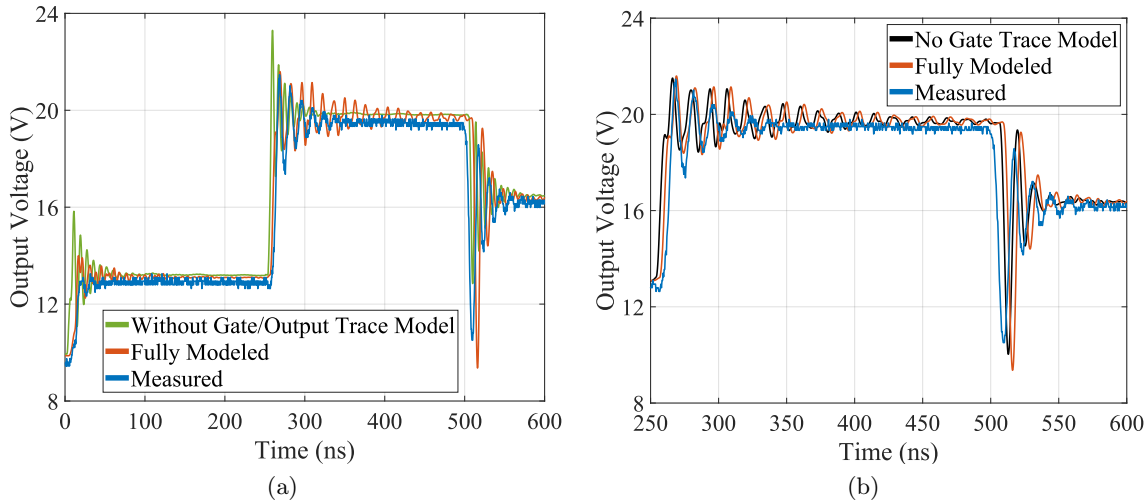


Figure 4.9: (a) Simulated HPMLC (a) output voltage, and (b) gate voltage comparing measurement and simulation using different modeling detail on the interconnects using an RC load of (1.25 Ω || 160 pF).

assuming each of the four RLC cells in Fig. 4.8a are identical, the total number of variables was reduced from 120 to 25. In taper B, a progressive increase in capacitance values and a decrease in inductance values was enforced as the taper moved to larger widths. The interconnects between the gate drivers and the external gate resistors of the switching devices are modeled in a similar fashion using a single RLC network as shown in Fig. 4.5b. These traces are individually EM simulated for each driver to switch interconnect, and the RLC model is fit to this data using the same cost function as for the output trace.

The simulated output voltage of the HPMLC is compared to a measurement in Fig. 4.9a showing the effect of the trace modeling. The converter switches between four equally spaced voltage levels ranging from 10 to 20 V with an equal duty cycle and a switching frequency of 4 MHz. The load is a parallel resistor-capacitor combination with values of 1.25 Ω and 160 pF. In the simulation, the gate drivers are implemented as ideal voltage sources with a rise/fall time consistent with the driver data sheet. The dead time in simulations is 2 ns, consistent with the measurements. For the temperature-dependent transistor models, the thermal resistance to ambient is modeled as 3.5 °C/W. The bypass capacitor bank is modeled to include the series inductance

and resistance parasitics taken from the data sheets of each capacitor.

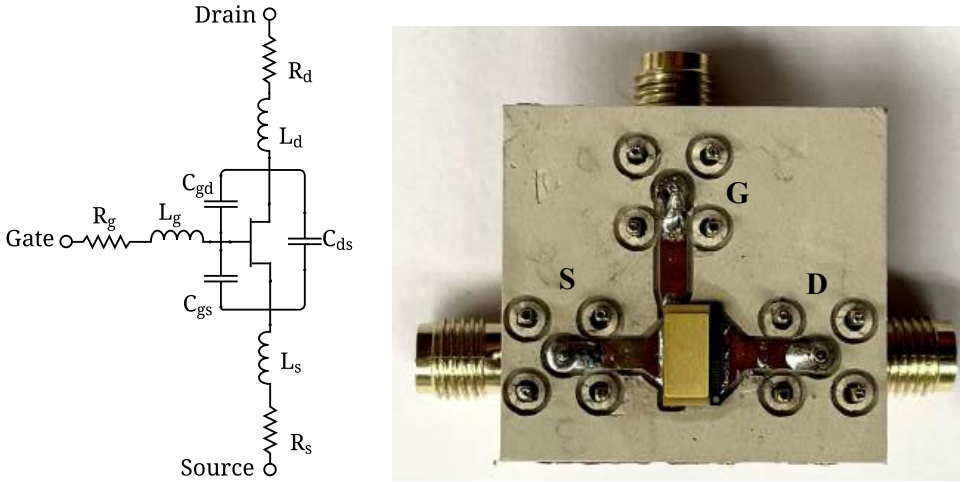
The gate and output traces have a significant effect on the ringing of the waveform. Fig. 4.9a shows that if the traces are not included in the model, the ringing overshoot, frequency, and decay rate are not accurately predicted. By modeling the output trace, the accuracy can be greatly improved. By modeling the gate trace, the accuracy can be improved even further. Fig. 4.9b shows the output waveform with and without the gate trace model, compared to the measured data. It can be seen that the main contribution of the gate trace is a time delay, which results in a better prediction of the waveform in the rise region up to 20 V.

4.4.1 Transistor Model Development

The parasitic capacitance and inductance of each transistor have a significant effect on the ringing that occurs at switch transitions. Since the transistors are implemented in a reverse configuration and operated in conditions not typical for this device, a custom LTspice transistor model is developed. The aim of this new transistor model is to determine if careful measurement of the transistor inductance and capacitance can yield more accurate waveform simulations. A schematic of the transistor model that is fit to measurements is shown in Fig. 4.10a. Additionally, a photograph of the breakout board used to measure the S-parameters of the transistor is shown in Fig. 4.10b.

S-parameter measurements are taken from 10 MHz to 500 MHz with the gate voltage held at 10 V. To determine the gate-drain capacitance, the drain voltage is swept from 10 V to 20 V in 1 V steps. Since the source voltage affects the gate-drain capacitance, the source voltage is stepped to 10 V, 13.3 V, 16.6 V, and 20 V. This helps determine the effect that the source voltage has on the gate-drain capacitance and is plotted in Fig. 4.11c. This process is repeated for the gate-source capacitance and plotted in Fig. 4.11b. These measurements also yield the drain-sorce capacitance at a single gate voltage plotted in Fig. 4.11a.

To generate an accurate model of the transistor, the micro-strip traces connecting the SMA connectors to the transistor must be de-embedded. Therefore, two de-embedding measurements are taken of an unpopulated board from Fig.4.10b with the three ports shorted and then open-circuited



(a) (b)

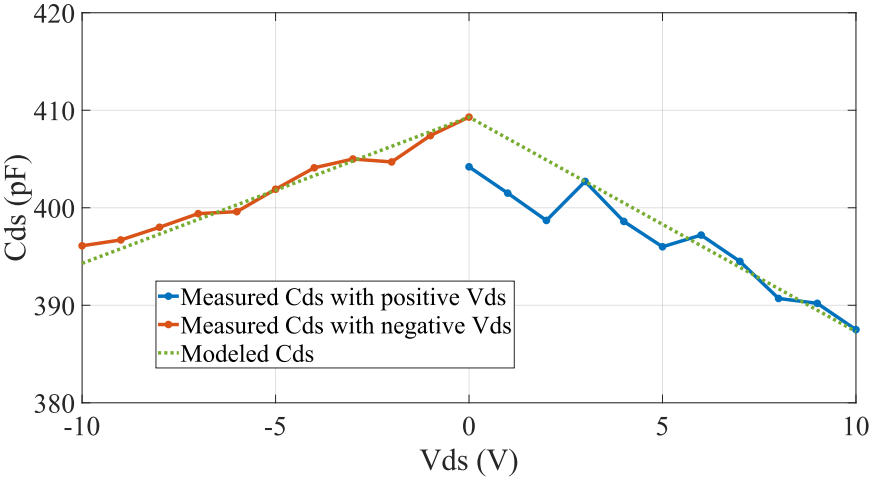
Figure 4.10: (a) Schematic of transistor parasitics. (b) Photograph of measurement board milled in FR-4 used to measure transistor S-parameters for model reactance extraction.

Table 4.4: Intrinsic transistor capacitance as a function of voltage.

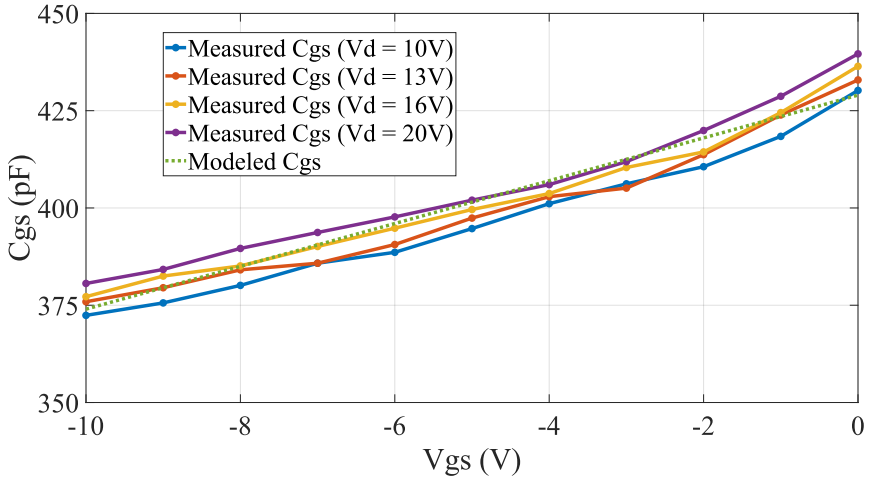
Capacitor	**M (pF/V)**	**B (pF)**
C_{gs}	5.5	429.0
C_{gd}	5.6	173.8
C_{ds} ($V_{\text{ds}} > 0$)	0.75	409.3
C_{ds} ($V_{\text{ds}} < 0$)	-1.1	409.3

where the transistor pads are located. The three traces connecting to the transistor are modeled as ideal lossless transmission lines. The characteristic impedances and electrical lengths are fit to the shorted and open-circuited measurements from 10 MHz to 500 MHz. Next, they are cascaded with the measured transistor S-parameters as lossless transmission lines with negative electrical length.

Additionally, to de-embed the inductance in the transistor, S-parameters are also measured for $V_{\text{gs}} = +5$, with drain and source voltages equal (no current) and swept from 10 to 20 V in 1 V steps. By biasing the device on, the drain-source capacitance is shorted, making it easier to extract the package inductance. The gate, source, and drain series inductances are then determined by fitting these measurements to an LC transistor model with the channel shorted. The capacitance values are extracted by fitting the biased-off S-parameter measurements to an equivalent LC model of the transistor in the off state from 10 MHz to 500 MHz. This is repeated for each voltage combination



(a)



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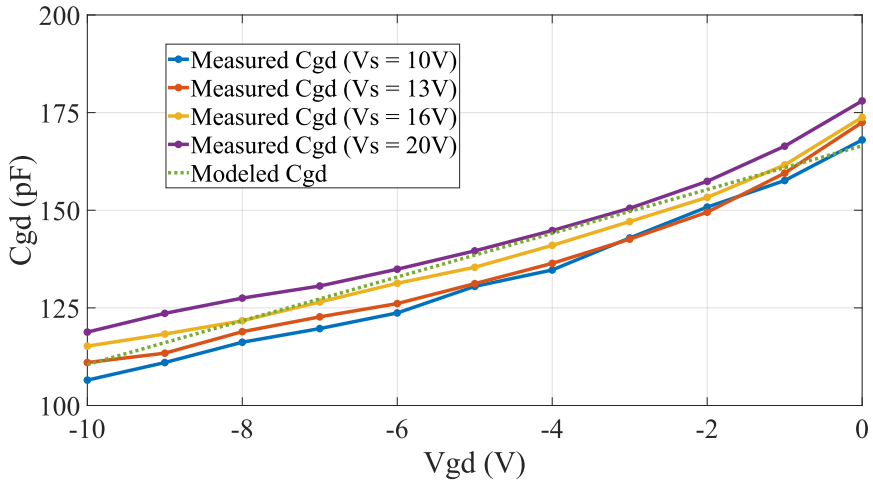


(c)

Figure 4.11: (a) Measured drain-source capacitance. (b) Measured gate-source and (c) gate-drain capacitance. The dotted green line represents the modeled voltage dependence of each respective capacitance implemented in the new LTspice model.

and each of the three intrinsic non-linear capacitors [134]. The capacitance vs. voltage is shown for each capacitor in Fig. 4.11. Note the different y-axis scales for the three plots. The green dotted linear fit line represents the capacitance curve as a function of voltage that is utilized in the LTspice transistor model as a nonlinear capacitor. The slope and y-intercept of the linear fit for each capacitor is shown in Table 4.4. In LTspice, the non-linear capacitors are defined by the charge of the capacitor as a function of voltage. The instantaneous capacitance is determined by taking the derivative of the charge function with respect to voltage. The equation for the linear fit and non-linear capacitor is:

$$C = Mv + B \tag{4.2}$$

$$Q = \frac{M}{2}v^2 \tag{4.3}$$

where v is the voltage across the capacitor, M is the slope, and B is the y-intercept. The capacitance function is implemented with a non-linear capacitor defined by Eq. 4.3 in parallel with a fixed capacitor equal to B

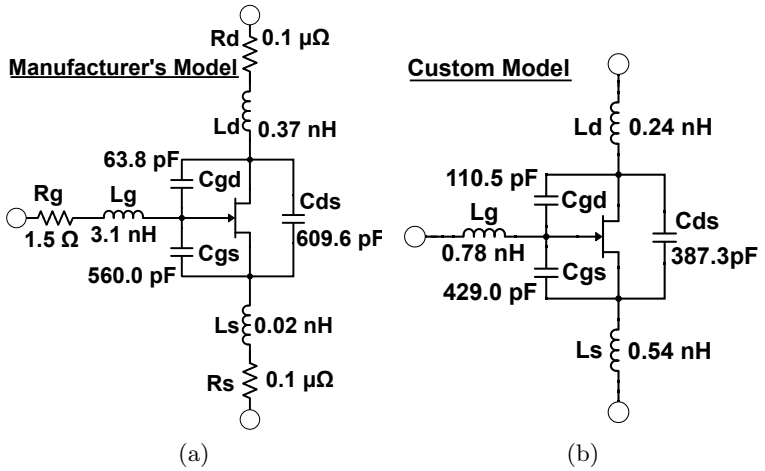


Figure 4.12: Schematic of transistor parasitic elements with Vds = 10V and Vgs = 0V extracted from (a) manufacturer's LTspice model (b) custom model extracted from S-parameter measurements.

Both the manufacturer's and the newly developed model are shown in Fig. 4.12. The manufacturer's model of the voltage-controlled current source with thermal effects is used in both cases.

The biggest difference between the two models is the gate and source inductance values. Additionally, the gate-source and drain-source capacitance differs by a factor of two. The output voltage of the custom model is compared to the manufacturer's model in Fig. 4.13 using the four-level equal duty cycle signal and previously mentioned RC load (1.25 Ω || 160 pF). From Fig. 4.13, it is clear that the custom model does not result in more accurate time domain simulations. This suggests that proper modeling of the PCB gate and output traces or the device's current source has a larger impact on simulation results than detailed modeling of the transistor's intrinsic and parasitic reactances.

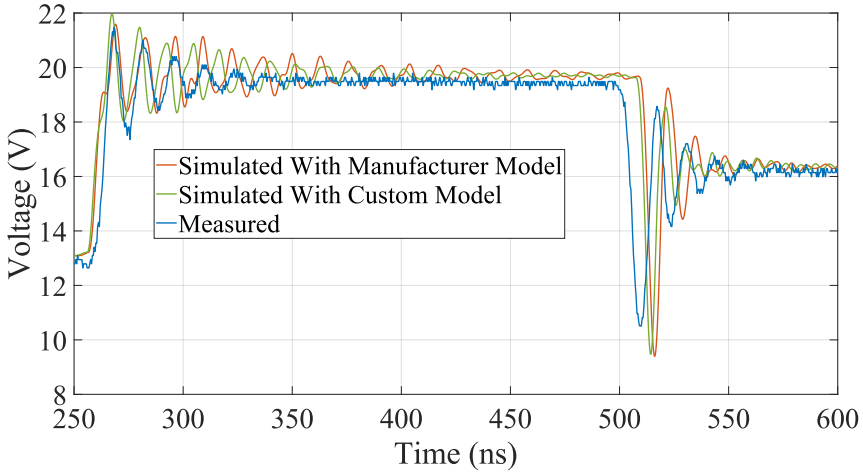


Figure 4.13: Output voltage waveform of supply modulator for an RC load (1.25 Ω || 160 pF) comparing simulations with manufacturer and custom transistor models against measurements.

4.5 Dynamic Supply Measurements

4.5.1 Test Setup

The measurement setup is shown in Fig. 4.14. The bit pattern generator is programmed in MATLAB to output 1 V rectangular pulses from several channels simultaneously with rise/fall times of approximately 70 ps. The BPG is used to independently control each gate driver on the HPMLC and apply dead times. The dc voltage supplies for the gate drivers and four voltage levels are supplied externally. The output voltage waveform is captured using an oscilloscope with

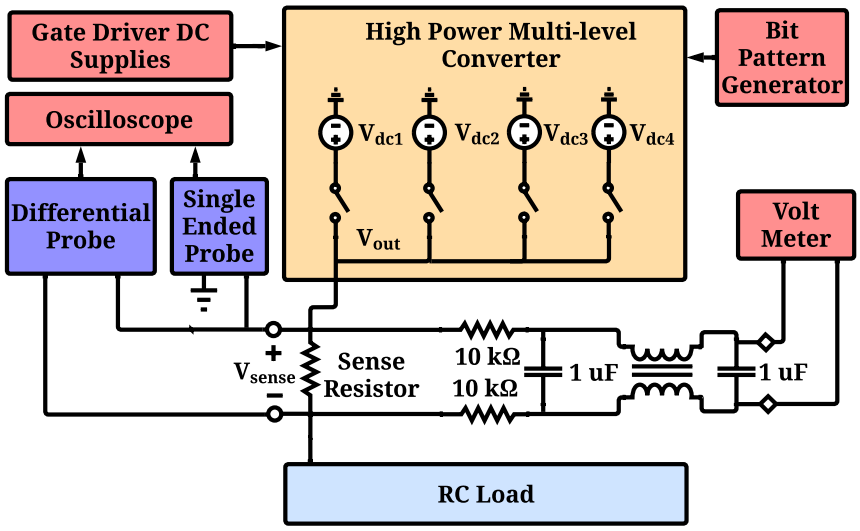


Figure 4.14: Test setup block diagram. The current is measured using a differential probe across the sense resistors. The filtered dc component of the voltage drop is used to calibrate the offset of the differential probe.

a sampling rate of 2.5 Gs/s. The current waveform is measured using a differential voltage probe placed across the sense resistor shown in Fig. 4.14. The current waveform is filtered with a common-mode choke and 1 µF capacitors, and the resulting dc component of the current is measured using a voltmeter. The current waveform measured by the differential probe is then offset such that its average value is equal to the dc current measured by the voltmeter. The sense resistor value is calibrated with the HPMLC supplying 10 V dc and taking the current reading from the dc power supply in conjunction with the voltage across the sense resistor. Finally, the output voltage waveform is measured using a separate high-impedance probe referenced to ground.

The performance of the HPMLC is evaluated using two sets of signals. One signal switches between the four voltage levels periodically with an equal duty cycle. The other is the envelope of a 64-QAM signal transmitting at a baud rate of 5 mega-symbols per second corresponding to a bandwidth of approximately 6.25 MHz with a root raised cosine filter utilizing a roll-off factor of 0.25. The signal length is 1000 symbols and repeats continuously. In order to change the power level of the converter, the load resistance is reduced from 20 Ω to 0.4 Ω in 9 steps.

The load resistance is designed to emulate different numbers of PAs being simultaneously

supply modulated, as illustrated in Fig.4.1a. The single PA unit considered is a 10 W PA similar to the one detailed in [66], operating at a drain voltage of 20 V with 50% drain efficiency, corresponding to a resistance of $R = 20\,\Omega$. For each of the measurements, the purely resistive case is compared to the case of an RC load for an individual PA drain capacitance of $C = 10\,\text{pF}$. For N amplifiers, the load is scaled according to:

$$R_\text{L} = \frac{R}{N} \quad \text{and} \quad C_\text{L} = N \cdot C \tag{4.4}$$

4.5.2 Measured Performance Results

The efficiency of the HPMLC producing a four-level equal duty cycle signal is shown in Fig. 4.15 for different output powers at switching frequencies from 1 MHz to 10 MHz. The results are shown with the parallel RC load described in Eq. 4.4 with N ranging from 1 to 50, as well as the purely restive load of with $C_\text{L} = 0\,\text{pF}$. The efficiency calculations include the power consumption of the entire HPMLC, excluding the BPG. The power consumption of the gate drivers is largely independent of the load and depends heavily on the switching frequency. Therefore, at lower output powers, the efficiency drops significantly since the ratio of the gate-driver power consumption to the total output power dominates. Furthermore, since the nominal *off* voltage of the gate drivers is connected to the 10 V rail, when a switch is turned off, the charge stored in the input capacitance of the device is transferred to the 10 V rail. Therefore, this energy is recycled, and the efficiency gets a slight boost. The efficiency in Fig. 4.15 peaks at approximately 175 W and drops slightly at the higher power levels, likely due to extra losses associated with higher device temperatures. Overall the efficiency remains above 94% across all switching frequencies for power levels exceeding 75 W.

The HPMLC is also evaluated at different power levels while tracking a 64-QAM signal described in section 4.5.1. The ideal target drain signal is chosen for flat gain at 9 GHz based upon CW measurements of the 10 W, 6 to 12 GHz GaN MMIC PA presented in chapter 2. For this HPMLC the minimum pulse width/maximum switching frequency is limited by the ringing duration

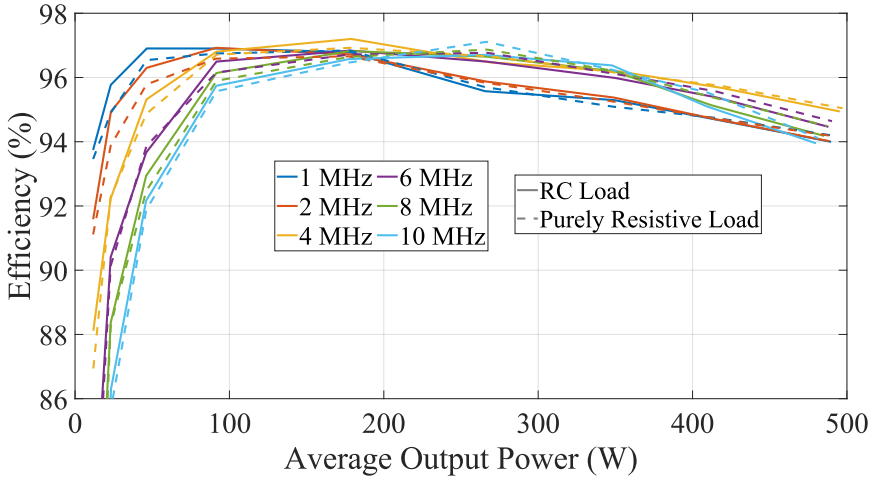


Figure 4.15: Supply modulator efficiency with an equal duty cycle four-level waveform at switching frequencies and average output powers ranging from 1 to 10 MHz and 11.7 W to 497.1 W under purely resistive and RC loads.

upon each switching instance. Therefore, the maximum switching frequency of the HPMLC is set to 10 MHz, corresponding to a minimum pulse width of 100 ns. Across the entire signal length, the discretized drain envelope signal has a minimum pulse width of 100 ns and a maximum pulse width of 228.8 ns.

The efficiency and root mean square error (RMSE) of the HPMLC generating the 64-QAM envelope signal are plotted for different average output powers in Fig. 4.16. The definition of RMSE is given by:

$$RMSE = \sqrt{\frac{\sum_{i=1}^{N} \left(V_{\text{meas.}}(i) - V_{\text{ideal}}(i)\right)^2}{N}}, \tag{4.5}$$

where N is the number of measured points over the entire duration of the signal, $V_{\text{meas.}}$ is the measured waveform, and V_{ideal} is the desired discrete output signal with perfectly sharp transitions and no ringing.

We here use the RMSE to show the deviation of the output trace from an ideal discrete supply modulator to quantify the effects of ringing. To de-embed the voltage drop due to ohmic losses, the ideal drain comparison signal for each load is adjusted to match the measured steady-state voltage of each voltage level. For low output powers (e.g. 10.2 W), the RMSE for the RC load is quite

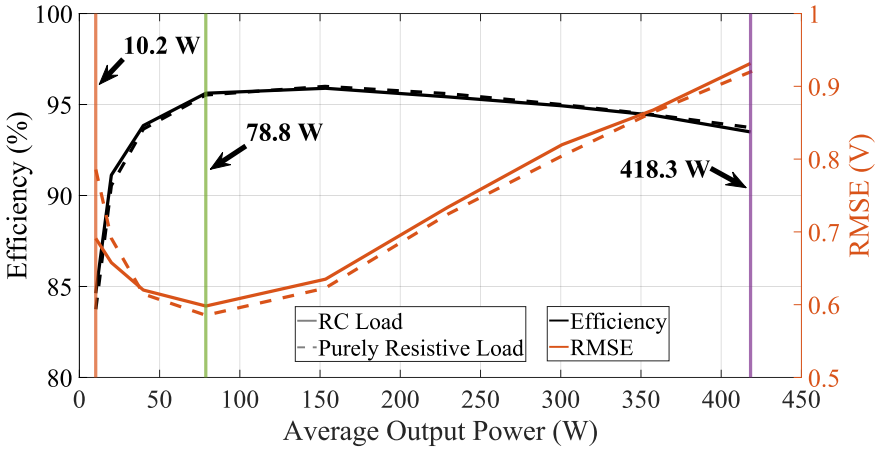


Figure 4.16: Supply modulator efficiency and RMSE while tracking an 6.25 MHz 64-QAM signal between average output powers of 10.2 W and 418.3 W for a purely resistive and RC load.

high due to large ringing at all voltage transitions. The purely resistive load shows an even worse RMSE of 0.79 V. At a load of 78.8 W, it reaches a minimum of 0.59 V and then rises again for higher output powers, with little difference between the purely resistive and RC load.

The output voltage waveform of the HPMLC tracking the 64-QAM signal with average output powers of 10.2 W, 78.8 W, and 418.3 W is shown in Fig. 4.17 under the previously described RC load conditions. The measured waveforms are compared to the ideal drain signal, which has not been adjusted for voltage drop. When switching to higher voltage levels, the ringing between loads of 10.2 W and 78.8 W is nearly identical, however when switching down to the lowest voltage level, the ringing overshoot and duration are significantly lower at 78.8 W. For higher output powers, we observe an increased lag to reach the steady state output voltages, thus resulting in a higher RMSE as shown in Fig. 4.16.

4.6 Summary

The design and characterization of a high-power discrete supply modulator is presented. This four-level modulator is suitable for the efficiency enhancement of multiple PAs with a shared drain voltage, amplifying high peak-to-average power ratio signals in an array. The peak measured output power is 800 W at 20 V, which is the highest reported output power of a supply modulator to the

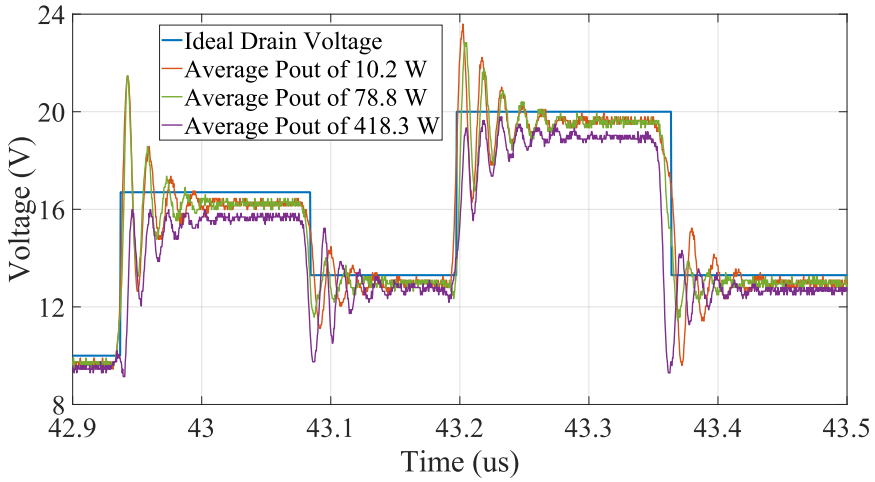


Figure 4.17: Measured output voltage with three different parallel RC loads of (20 Ω || 10 pF - orange), (5 Ω || 40 pF - green), and (0.4 Ω || 480 pF - purple). These waveforms are compared to the ideal drain signal when tracking a 6.25 MHz 64-QAM signal.

best of the author's knowledge. Additionally, for powers exceeding 50 W, the efficiency is greater than 92%, and a maximum switching frequency of 10 MHz is achieved. The high performance is enabled through careful selection of the semiconductor technology and switching transistors to minimize parasitic capacitance and on-state resistance for high current devices.

The primary limitation on the switching speed of the supply-modulator is the ringing in the output voltage waveform that occurs upon each switch transition. The source of the ringing is the parasitic capacitance, inductance, and resistance in the transistors, gate driver, and output trace interconnect, which behave as a low pass filter. Initially, output voltage was simulated in LTspice with a transistor model provided by the manufacturer and an ideal short circuit output interconnect. These simulations did not match the measured results. However, by simulating the S-parameters of the passive output trace in a full-wave electromagnetic simulator and fitting it to an equivalent RLC circuit compatible with LTspice time domain simulations, the ringing was accurately predicted. In an attempt to improve the modeling further, a custom model of the transistors utilizing non-linear capacitors was developed from S-parameter measurements and implemented in LTspice. However, the results of this simulation did not improve output waveform prediction.

The ringing frequency is primarily determined by the reactive parasitics in the transistor,

while the overshoot and decay rate are a strong function of the resistive losses. By modeling the output trace, the ringing frequency was accurately predicted, but the amplitude and decay rate deviate from the measured results. One possible explanation for this is that the resistive losses in the transistor were not accurately predicted. These losses are strongly dependent on the temperature of the transistor. A thermal model is included in the manufacturer's model, and the thermal resistance of the transistor heat sink is implemented. However, precise modeling of the transistor's thermal behavior is difficult and could be addressed in future work.

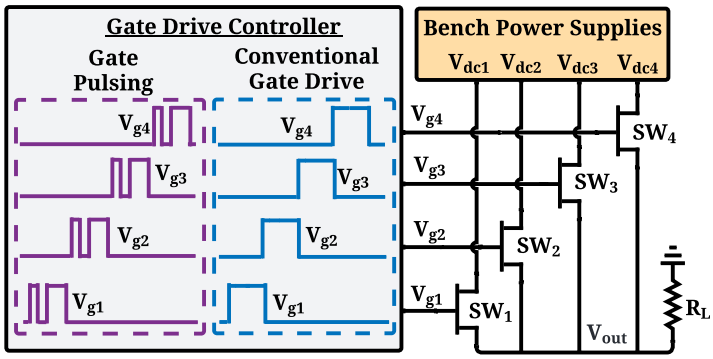
The ringing could potentially be reduced by changing the output trace geometry to minimize parasitic capacitance and inductance. Additionally, by placing two transistors in series instead of parallel, the output capacitance can be halved and the ringing reduced at the cost an increased on-state resistance and lower efficiency. Another technique to reduce ringing is by modifying the gate drive signal used to switch the transistors, which will be the topic of chapter 5. The results in chapter 4 are reported in [83, 135].

Chapter 5

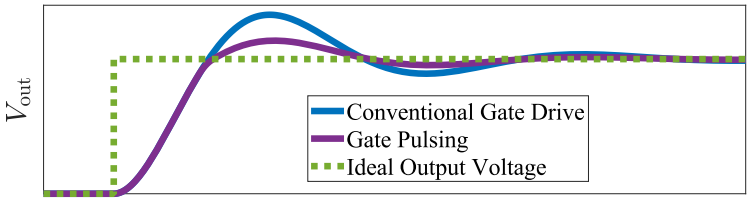
Ringing Reduction Through Gate Pulsing

5.1 Introduction

In chapter 4, an 800 W discrete four-level supply modulator was demonstrated with a max switching speed of 10 MHz. This supply modulator exhibited significant ringing upon each voltage level transition which was accurately predicted through proper modeling of the output trace distributed RLC elements. When implemented with a PA in an envelope tracking system, this ringing



(a)



(b)

Figure 5.1: (a) Schematic and gate drive signals of the high power multi-level converter (b) Example of output voltage ringing comparing the conventional gate drive, gate pulsing, and the ideal cases.

creates spurious mixing products in the nonlinear PA which degrades linearity metrics such as error vector magnitude and adjacent channel power ratio [3,136,137]. Furthermore, the ringing limits the maximum switching speed of the converter [83]. Therefore, minimizing the output voltage ringing is a critical aspect of discrete supply modulator design.

Previous attempts to minimize ringing focus on the reduction of electromagnetic interference (EMI) created by fast switching transients [138]. For supply modulator designs, the output voltage ringing itself is more important than EMI issues, however, the two topics are closely related. Techniques that actively control the switch slew rate are known as active gate drive topologies [139]. Among these are variable gate resistance [140], variable gate current [141], and variable gate voltage circuits [142, 143]. In addition, the dead-time (DT) can also be adaptively optimized to improve efficiency [144] or reduce EMI [145]. These components are typically feedback-controlled through a sensing circuit and dedicated digital control circuitry. This makes the switched supply reconfigurable under changing load conditions, however, the approach is difficult to implement and significantly increases complexity and cost. Ringing can also be reduced through the use of a resonant filter or snubber network, however, a filter reduces the converter bandwidth, while a snubber network decreases the converter efficiency. Alternatively, the ringing can be reduced through a novel technique referred to as gate pulsing where the gate of each switch being turned on is pulsed on and off quickly before ultimately being turned on. Through the use of gate pulsing, the switches undergo an intermediate lossy state which reduces the ringing. This technique is illustrated in Fig. 5.1b. In contrast to previous methods, gate pulsing does not require any additional hardware and can be individually adjusted for different voltage level transitions and loads.

This chapter presents a new pulsed-gate ringing reduction technique compatible with multi-level converter architectures. The technique is compared with two conventional approaches: increasing fixed series gate resistance; and DT optimization. The corresponding schematic and idealized gate drive signals are shown in Fig. 5.2a-c. The gate pulsing technique does not require any additional hardware, is reconfigurable for different loads, and reduces the ringing beyond what increasing gate resistance and DT optimization are capable of, without compromising efficiency.

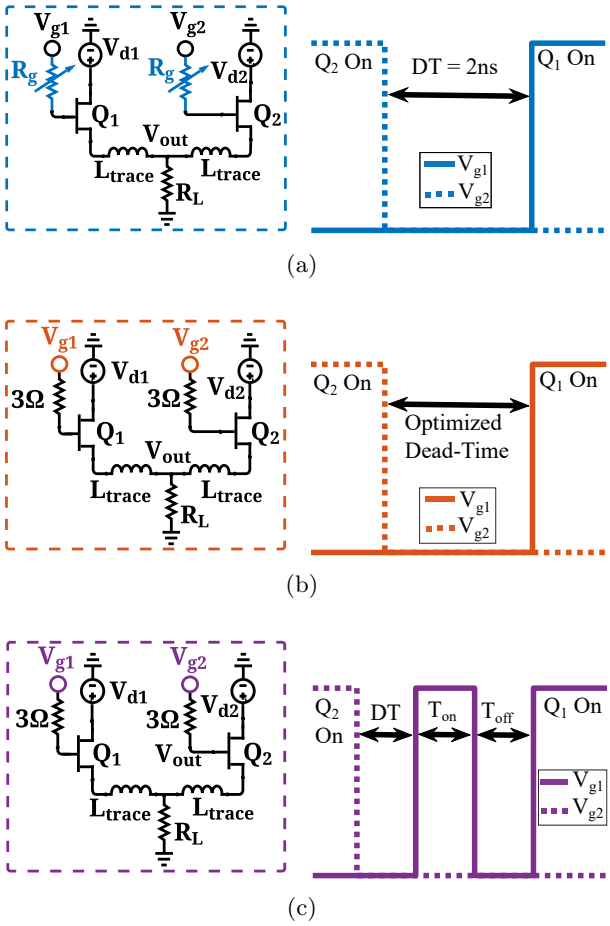


Figure 5.2: Two-level schematics and idealized gate drive signals of the three ringing reduction techniques compared in this work: (a) increased gate resistances (3 – 10 Ω) with a fixed dead-time; (b) dead-time optimization; and (c) gate pulsing.

For the comparison, different techniques are applied to a high power (800 W) multi-level converter (HPMLC) while tracking the envelope of an 6.25 MHz 64–QAM signal.

5.2 Ringing Origins

Any bandwidth limitations of an ideal pulse create ringing and distortion. This is because functions with sharp transitions and discontinuities, such as a pulse, cannot be represented with a finite number of Fourier series harmonics, known as the Gibbs phenomenon [146]. This is illustrated in Fig. 5.3 which shows a pulse waveform with a limited number of harmonics and a period of 100 ns. As the number of harmonics increases, the slew rate goes up and the ringing settling time decreases. Passive interconnects such as the output trace of the HPMLC behave as a low pass filter limiting

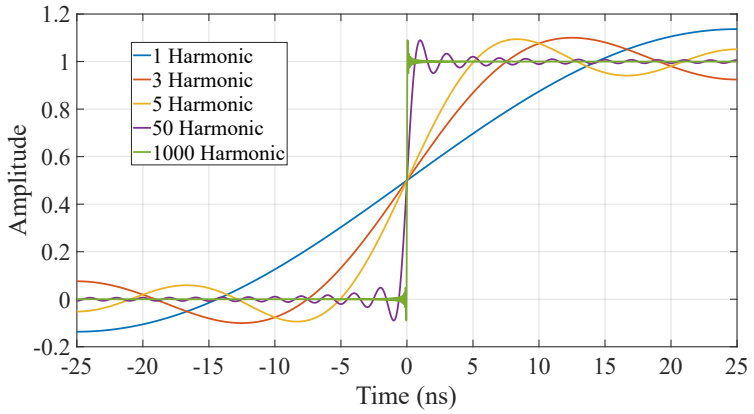


Figure 5.3: Time domain pulse with a limited number of harmonics and period of 100 ns.

the number of harmonics. Therefore, to minimize ringing, it is necessary to design broadband interconnects. In multi-level supply modulators, the transistor parasitics also have a significant impact on ringing and bandwidth limitations. To examine the bandwidth of this HPMLC, the output trace from section 4.4 is loaded with the parasitic inductance and capacitance measured in the GaN transistors (shown in Fig. 4.12b). The schematic of the trace including the transistors is shown in Fig. 5.4. The off transistors are modeled with an open-circuited channel, and the on transistors are modeled with a 0.01 Ω resistor across the drain and source. The magnitude of S_{11} and S_{21} are plotted for the circuit shown in Fig. 5.4 with 1 Ω ports. The circuit behaves as a low-pass filter with a resonance occurring at 81 MHz and the 3 dB cutoff at 47 MHz. This analysis is not a complete explanation for the ringing in discrete supply modulators. For instance, the transient characteristics of the transistors and gate drivers are ignored as well as the non-linear capacitance in each transistor. Additionally, the port impedance has a strong impact on the S-parameters simulation, 1 Ω was chosen to be near the characteristic impedance of the trace at port 2. The remainder of this chapter will focus on methods of reducing this ringing without re-designing the geometry of the output trace.

5.3 Supply Modulator Test Setup

The HPMLC used in this work is presented in chapter 4 and switches between four evenly spaced externally generated dc voltages of 10, 13.3, 16.7, and 20 V. A schematic of the converter is

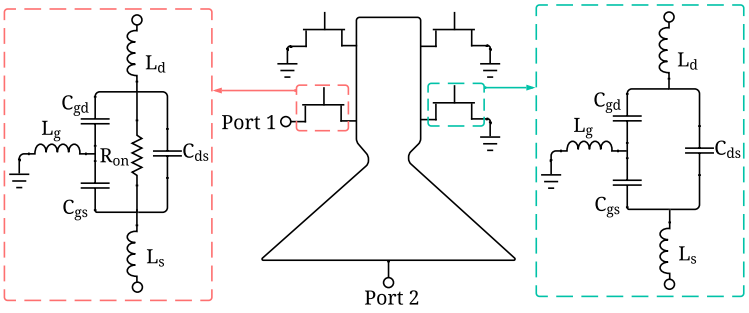


Figure 5.4: Schematic for S-parameter simulation of HPMLC output trace with switch transistors, note that only four transistors are drawn, but each switch consists of two devices in parallel.

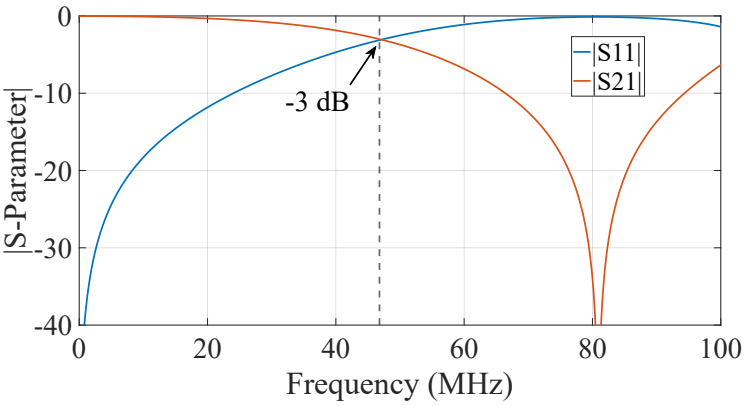


Figure 5.5: Simulated S-parameter magnitude of the output trace including parasitics from the transistors. The schematic for this simulation is shown in Fig. 5.4

shown in Fig. 4.5, and an idealized version is shown in Fig. 5.1a. A fixed surface mount resistor R_g in series with each of the transistor gates limits the gate current during switching transients and prevents damage to the gate drivers.

The converter is evaluated using an 6.25 MHz 64–QAM signal envelope transmitting 5 MS/s with a root-raised cosine filter and a roll-off factor of 0.25. The signal envelope is translated into a discretized four-level signal through a shaping function that relates the instantaneous PA modulated signal input power to a particular drain voltage [66, 83, 112]. The maximum switching speed of the discrete output signal is 10 MHz, corresponding to a minimum pulse width of 100 ns. The output voltage and current are measured using an oscilloscope as in chapter 4. The output power is determined by multiplying the current and voltage waveforms and integrating across the signal duration. The input power is calculated by summing the power supplied from each of the dc supplies, and the efficiency is the ratio of the output and input power. The ringing in the measured

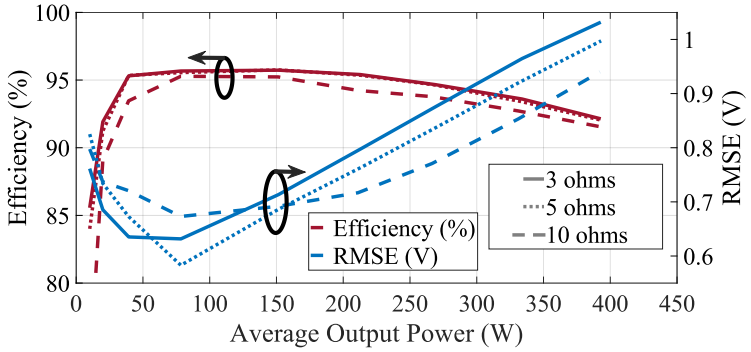


Figure 5.6: Converter efficiency and RMSE while tracking an 6.25 MHz 64–QAM signal with three different series gate resistances.

signal is evaluated by the root mean square error (RMSE), shown in Eq. 4.5.

5.4 Ringing Reduction Comparison

5.4.1 Gate Resistance Study

Increasing the series gate resistance of each GaN transistor switch can potentially reduce the ringing through a decrease in the slew rate. To investigate this, the HPMLC is evaluated with fixed series gate resistance values of 3, 5, and 10 Ω, across nine load resistances ranging from 20 to 0.4 Ω. The efficiency and RMSE of the HPMLC while tracking the 6.25 MHz 64–QAM signal is shown in Fig. 5.6 for the three different gate resistances. For low average power levels below 50 W a gate resistance of 3 Ω results in the lowest RMSE. For medium power levels between 50 W and 150 W the 5 Ω case is best. For high power levels exceeding 150 W the 10 Ω case results in the best RMSE with a small cost to efficiency. The power spectral density (PSD) of the HPMLC output voltage is shown in Fig. 5.7 at a load resistance of 5 Ω (average output power of ∼40 W) with gate resistances of 3, 5, and 10 Ω. From this investigation, it is evident that the optimal series gate resistance is load dependent. For systems with varying loads, e.g. dynamically driven PAs, an adaptable ringing reduction method is required.

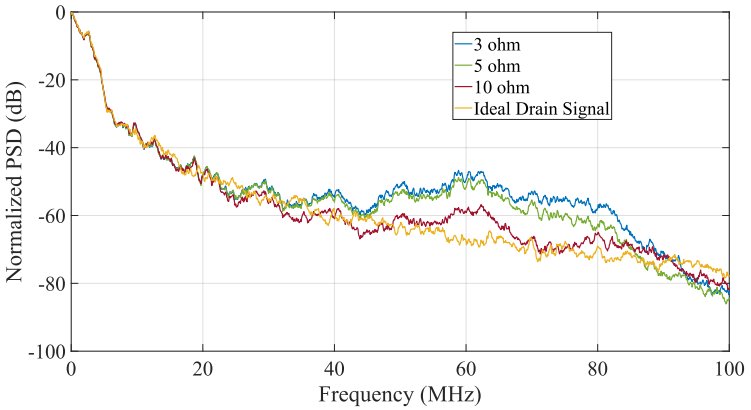


Figure 5.7: Power spectral density of the HPMLC output voltage with gate resistances of 3, 5, and 10 Ω all with a load resistance of 5 Ω.

5.4.2 Gate Pulsing and Dead-Time Optimization

To reduce the ringing that occurs upon each upward transition, the gate of each switch being turned on was pulsed on and off before reaching its final on-state as shown in Fig 5.2c. For this technique to be successful, the pulse parameters T_{on}, T_{off}, and the DT settings must be tuned for each of the six individual voltage transitions. This is necessary to account for variations in the different switches and gate drivers. For instance, varying rise/fall times, threshold voltages, and propagation delays can affect the optimal pulse parameters. Gate pulsing was first investigated in the time domain simulator LTspice with a transistor model provided by the manufacturer and the parasitics from the gate trace and transistor interconnect modeled as *RLC* circuits. This simulation model is validated with measurement data in chapter 4.

The simulated gate and output voltages of the two parallel transistors connected to the 13.3 V level are shown in Fig. 5.8 with and without gate pulsing for the 10 to 13.3 V transition. When the gate is pulsed, the transistors go into a lossy state while switching on. As the output voltage rises, the oscillating energy stored in the reactive elements of the transistors and output trace is converted to heat by the transistor resistance thus the output voltage ringing is dampened. The dissipated power in the transistors is plotted as a function of time in Fig. 5.8. With gate pulsing the average dissipated power from 0 to 70 ns increases from 0.85 to 1.02 W and the total steady-state power delivered to the load is 35.2 W. These simulations illustrate how the gate pulsing technique

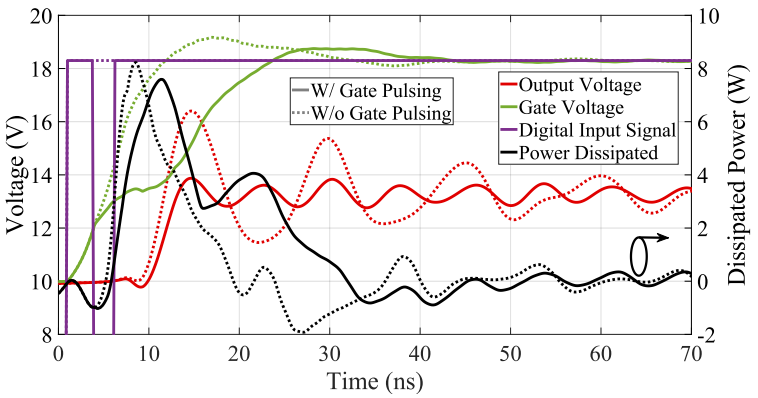


Figure 5.8: Simulated output voltage, gate voltage, digital input signal, and power dissipated in the transistor switch for the 10 to 13.3 V transition with and without gate pulsing.

can significantly reduce output voltage ringing with only a minimal increase in dissipated power.

In order to obtain the optimal pulse and DT settings in measurements, a continuously repeated test signal is used which switches between each of the voltage levels with an equal duty cycle and remains at each voltage level for 10 µs. With this signal, pulse settings T_{on}, T_{off}, and DT are swept for each upward transition and applied only to switches being turned on. At each optimization setting, the ringing is compared to a reference case that has 2 ns of DT, a gate resistance of 3 Ω, and no gate pulsing. For each setting, the output voltage is measured and the RMSE is calculated over a short window that starts when the reference case output voltage initially crosses its steady-state dc voltage at the higher level and ends when the waveform settles. The RMSE at each pulse setting is normalized to the RMSE of the reference case and referred to as the normalized root mean square error (NRMSE). Values less than one indicate an improvement through DT optimization or the gate pulsing technique over the reference case. A coarse sweep of the three pulse parameters (T_{on}, T_{off}, and DT) is measured with T_{on} and T_{off} swept in 1.2 ns steps and DT swept in 0.4 ns steps. After an optimal region of the coarse sweep is selected, the DT is fixed and the (T_{on}) and (T_{off}) values are swept at the finest resolution of the BPG (0.4 ns).

The NRMSE of the coarse sweeps of the 10 to 13.3 V and 13.3 to 16.7 V are shown in Figures 5.9a and 5.10a as a function of the gate pulse settings T_{on} and T_{off} for a fixed optimal DT with a load of 5 Ω. The two markers indicate the optimal T_{on} and T_{off} settings over the

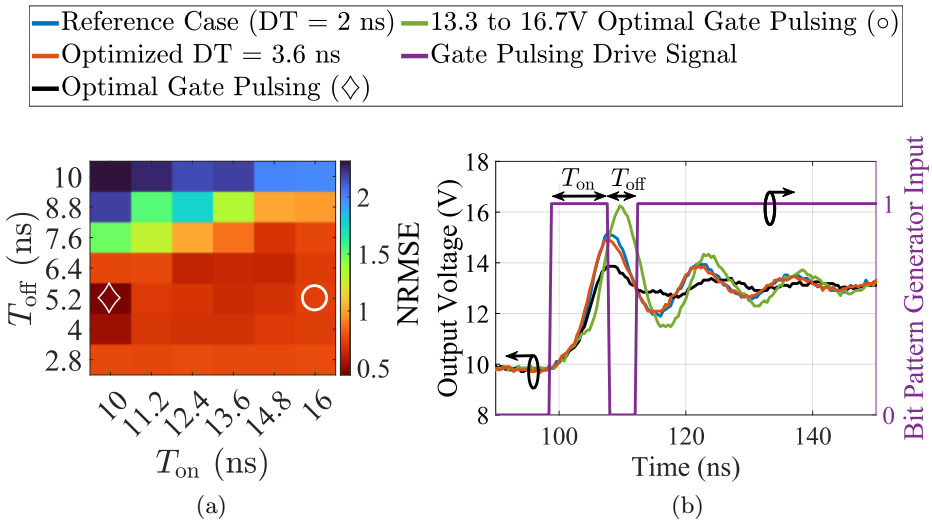


Figure 5.9: Gate pulsing results of the 10 to 13.3 V transition. (a) NRMSE over the gate pulse parameters sweep with a DT of 3.6 ns and (b) time domain waveforms.

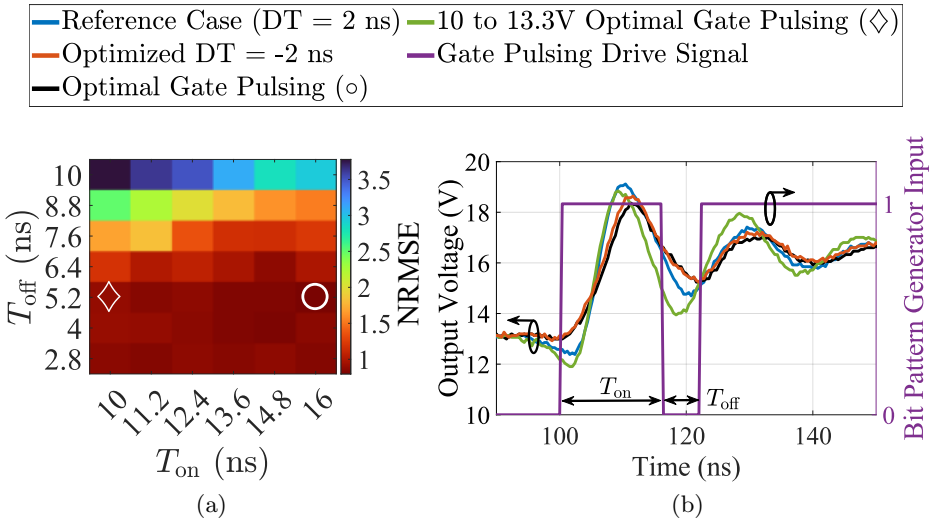


Figure 5.10: Gate pulsing results of the 13 to 16.7 V transition. (a) NRMSE over the gate pulse parameters sweep with a DT of −2 ns and (b) time domain waveforms.

coarse sweep for the 10 to 13.3 V (♢) and 13.3 to 16.7 V (○) transitions. The corresponding time domain waveforms are shown in Figures 5.9b and 5.10b. From these plots, we can see that the gate pulsing can yield significant improvements in ringing over DT optimization. Furthermore, if optimal settings for one transition are applied to another, then the advantage from gate pulsing can be lost, as is the case in Fig. 5.10b or can add even more ringing as is the case in Fig. 5.9b. The optimal settings for each of the six transitions are shown in Table 5.1 for a 5 Ω load resistance. For each transition, the NRMSE can be improved beyond the DT optimization results through the use of gate pulsing.

Table 5.1: Implemented pulse settings, DT, and NRMSE for the DT optimization and gate pulsing techniques with a 5 Ω load.

	DT Opt.		**Gate Pulsing**			
Transition	DT_{opt} **(ns)**	**NRMSE**	T_{on} **(ns)**	T_{off} **(ns)**	DT **(ns)**	**NRMSE**
10-13.3 V	3.6	0.88	9.2	4.4	3.6	0.39
10-16.7 V	5.2	0.76	10	6	6	0.66
10-20 V	6	0.50	10	5.2	6	0.30
13.3-16.7 V	-2	0.75	16	6	-2	0.68
13.3-20 V	-0.8	0.84	10.4	4.8	-0.8	0.59
16.7-20 V	-2	0.76	10.4	4.4	0	0.63

The optimal gate pulsing and DT optimization parameters were implemented in a look-up table and applied to the HPMLC while tracking the envelope of the previously described 6.25 MHz 64–QAM signal at a load resistance of 5 Ω. The resulting converter RMSE and efficiency when using the gate pulsing and DT optimization techniques are compared to fixed gate resistances of 3, 5, and 10 Ω with 2 ns of DT in Fig. 5.11. The reference case of fixed DT without gate pulsing and a gate resistance of 3 Ω yields an RMSE of 0.63 V. Through DT optimization the RMSE is reduced to 0.59 V and through gate pulsing the RMSE is reduced further to 0.55 V with only a 0.9% points cost to efficiency while tracking the 64–QAM signal. The ringing creates additional spectral content between 30 and 80 MHz as shown in Fig 5.12. Through gate pulsing, this spectral content can be attenuated, thus moving closer to the ideal drain signal case.

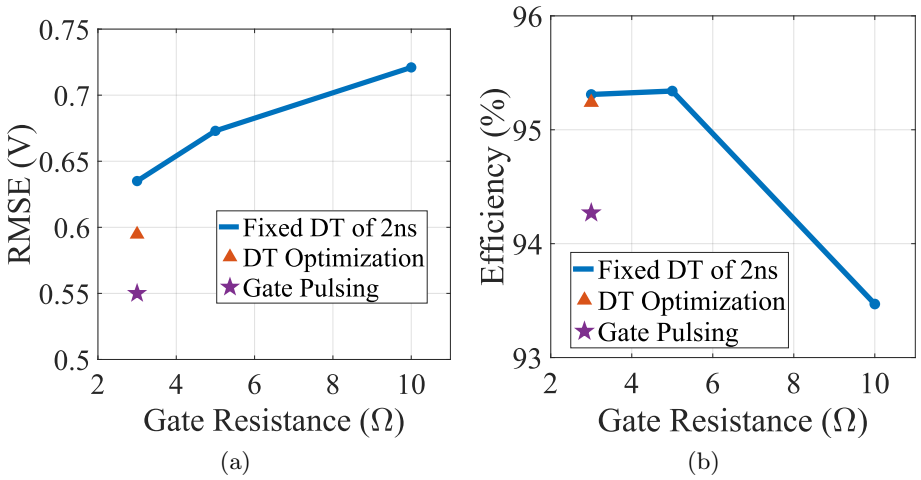


Figure 5.11: (a) RMSE and (b) efficiency vs series gate resistance at a load of 5 Ω while tracking an 6.25 MHz 64–QAM signal.

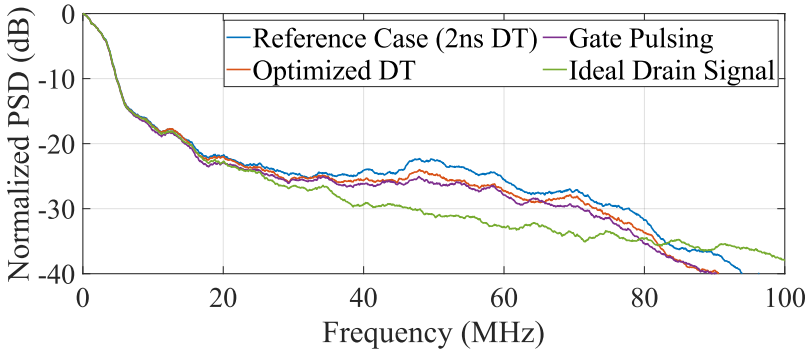


Figure 5.12: Frequency spectrum comparison of the reference case, optimized dead time, gate pulsing method, and ideal drain voltage waveforms while tracking the 6.25 MHz 64 QAM signal each with a gate resistance of 3 Ω.

5.5 Summary

A new ringing reduction technique for multi-level supply modulators is experimentally validated. This gate pulsing technique does not require any additional circuitry and is flexible such that the pulse timing for individual voltage transitions and different power levels can be individually optimized. Gate pulsing reduces the ringing beyond what dead-time and variable gate resistance is capable of with only a small drop in efficiency. This technique is applied to a 800 W multi-level converter while tracking the envelope of an 6.25 MHz 64–QAM signal. When compared to a reference case with conventional gate driving and a gate resistance of 3 Ω, the RMSE is improved by 12.7% with only 0.9% points cost to efficiency when using gate pulsing on each upward transition.

The improvement in RMSE reduces in-band and out-of-band distortion created by the supply modulator in an efficient envelope-tracked wireless transmitter. The limiting factor for the gate pulsing technique is the switching speed of the gate drivers. Utilizing gate drivers with a faster switching speed could provide finer control over the transistor gate voltage and open up the possibility for improved ringing reduction. The results in this chapter are published in [84].

Chapter 6

Dynamic Supply Modulation of an Array

6.1 Introduction

Previous chapters presented the design and measurements of hardware suitable for the supply modulation of an array; for instance, chapter 3 introduces a PA design technique to improve efficiency and linearity with a dynamic drain supply. Chapter 4 investigates the design of a high-power supply modulator suitable for an array of multiple PAs. Chapter 5 demonstrates an active technique to minimize distortion in the drain signal. Dynamic supply modulation of an active array can improve system efficiency, bolster PA linearity, and minimize thermal limitations. Reduced heat dissipation simplifies thermal management systems such as liquid cooling and forced air. This chapter experimentally investigates the supply modulation of an array, specifically focusing on hardware design and measurements.

Previous work on supply modulation is mostly performed with a single PA and computationally applied to the array environment or is entirely theoretical. The results in this chapter are an experimental demonstration of the supply modulation of an array. Theoretical work on supply modulation of an array is reported in [89]. Here, each PA shares a single dynamic continuous drain supply. When a progressive phase shift is applied to the array RF carrier for beam steering, the envelopes of each PA are delayed in time. Since each PA has a shared drain supply, the instantaneous maximum of each envelope must be tracked. As the delay in each envelope grows, the drain signal approximates a static supply. This effect was analyzed in [89] with a two-tone signal. The two-tone input voltage applied to the ith PA is:

$$V_{\mathrm{i}}(t) = 2\cos(2\pi\Delta f(t-\tau_{\mathrm{i}}))\cos(2\pi f_0(t-\tau_{\mathrm{i}})) \tag{6.1}$$

where $f_0 = \frac{f_1+f_2}{2}$, $\Delta f = \frac{f_1-f_2}{2}$, and τ_{i} is the delay in element i. For this analysis, f_1 and f_2 are the two tones. The envelope of the two-tone signal is:

$$V_{\mathrm{env,i}}(t) = |2\cos(2\pi\Delta f(t-\tau_{\mathrm{i}}))| \tag{6.2}$$

for an element spacing of $\lambda/2$ the time delay of the ith PA is:

$$\tau_{\mathrm{i}} = (i-1)\frac{\sin(\theta)}{2f_0} \tag{6.3}$$

where θ is the beam steering angle.

The two-tone envelope of each element and shared supply modulated drain voltage is shown in Fig. 6.1 for a 4-element and 64-element array. The drain voltage tracks the maximum instantaneous envelope across each element in the array. In this example, $f_1 = 8.9\,\mathrm{GHz}$, $f_1 = 9.1\,\mathrm{GHz}$, $f_0 = 9\,\mathrm{GHz}$, $\Delta f = 100\,\mathrm{MHz}$. The amplitude of each tone is $1\,\mathrm{V}$, and $\theta = 60°$. The time delay between the first and last element is $0.17\,\mathrm{ns}$ with 4-elements and $3.7\,\mathrm{ns}$ with 64-elements. In Fig. 6.1a, the effect of time-delayed envelopes has little effect on the drain voltage. However, in Fig. 6.1a, the time delay is so large that supply modulation yields little benefit over a static supply. In order for supply modulation to produce a significant efficiency enhancement, the system must satisfy the following figure of merit first derived in [89]:

$$\frac{\Delta f}{f_0}\sin(\theta)(N-1) \ll \frac{1}{2} \tag{6.4}$$

where N is the number of elements in the array.

Furthermore, if the drain network feeding each individual PA is not symmetric, the physical delay in the lines can create additional misalignment between the drain voltage and input signal for each element. The effect of envelope time delay due to beam steering primarily affects arrays with a large number of elements or a large ratio between the signal bandwidth and fundamental

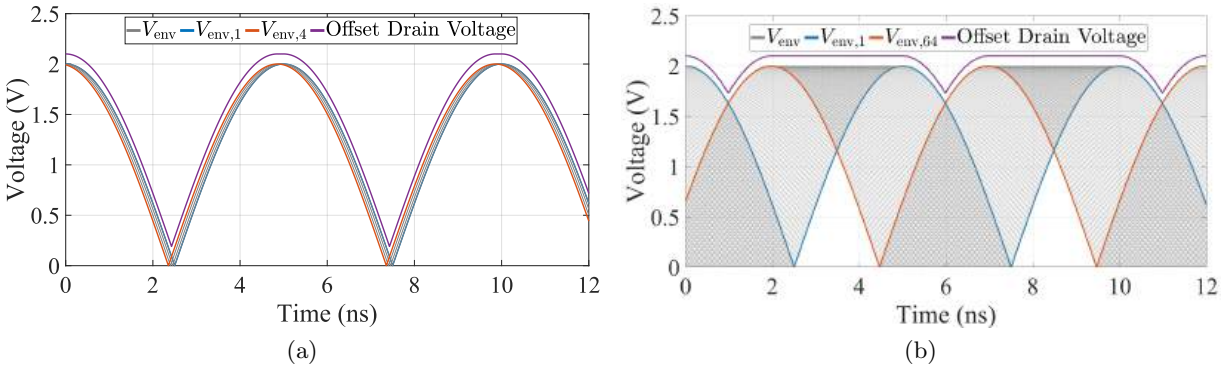


Figure 6.1: Two tone envelope signal and shared supply modulated drain voltage of an array with (a) 4 and (b) 64 elements. $f_1 = 8.9\,\text{GHz}$, $f_1 = 9.1\,\text{GHz}$, $f_0 = 9\,\text{GHz}$, $\Delta f = 100\,\text{MHz}$. The amplitude of each tone is 1 V. The drain voltage tracks the maximum instantaneous envelope, looking at each element across the array, and is offset for visual clarity. This analysis uses a 60° beam steering angle corresponding to a progressive phase shift of 155.8°. The time delay between the first and last element is 0.17 ns in (a) and 3.7 ns in (b).

carrier frequency. This phenomenon is also investigated experimentally with two-level discrete supply modulation in [90]. Here, a single PA is discretely supply modulated at 1.8 GHz using a 120 MHz orthogonal frequency division multiplexing signal. By expanding the pulse width of the discrete supply, similarly to Fig. 6.1, the effect of the envelope time delay was mimicked. From these measurements, the efficiency and linearity were determined as a function of the number of elements and steering angle.

Applying digital pre-distortion is an additional challenge for a supply-modulated array and is investigated in [92] for a MIMO array and in [147] for frequency hopping applications. However, in [92], a single PA is measured and computationally applied to the array environment. Furthermore, in [147], four separate PA/supply modulator units are operated simultaneously from a single FPGA, but each PA is terminated in 50 Ω, and the output is not combined in any way.

A CMOS polar 4x1 transmit array is demonstrated experimentally in [91]. Here, the phase of the complex signal is applied through input RF phase shifters. The phase shifters can also apply a progressive phase shift to achieve beam steering. The amplitude of the complex signal is applied through the drain supply of the PAs, and a separate drain waveform is generated for each PA. The active array in [91] operates from 3 GHz to 7 GHz. The drain efficiency of each PA is greater

than 40% from 4 GHz to 5.5 GHz with an acceptable EVM of approximately 5% while tracking a 40 MHz 64-QAM signal. However, the system efficiency is less than 15%. While polar modulation architectures such as [91] can achieve high efficiency at the PA element, the system efficiency is often low for high signal bandwidths. Furthermore, this approach requires an individual drain modulator for each PA element, which increases complexity.

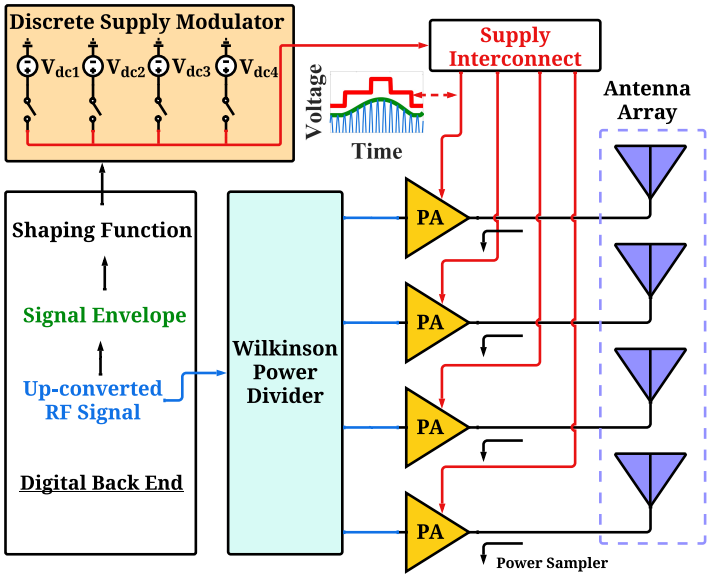


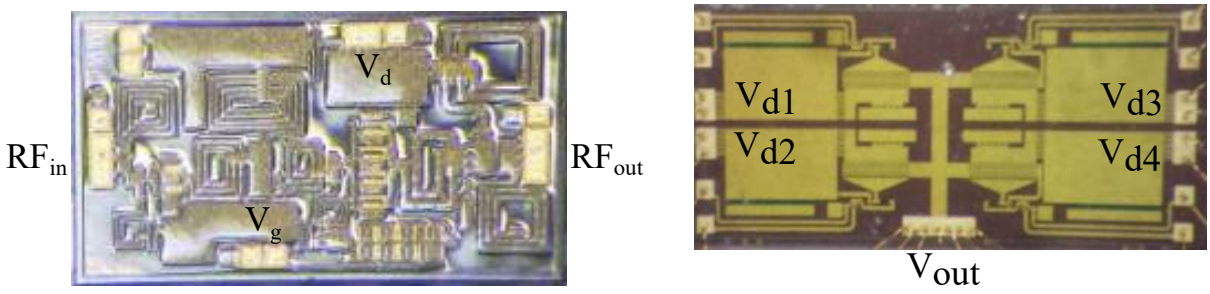
Figure 6.2: Block diagram of a 4-element transmit array with supply modulation for efficiency enhancement of the GaN MMIC PAs, using a single dynamic supply, also implemented as a GaN MMIC. The output of the 4-level discrete supply modulator is time-aligned with the input signal at the PAs. The interconnect network between the supply modulator and the output of the PAs is designed to minimize inductance and capacitance in order to minimize filtering of the signal on the drain bias.

In this chapter, the hardware implementation and characterization of a discretely supply-modulated 4×1 active transmit array is presented. This transmit array has an operating bandwidth from 6 GHz to 12 GHz with 2 W GaN MMIC PAs feeding each antenna element (Fig. 6.7). First, section 6.2 shows the supply modulation of a single PA loaded with 50 Ω and amplifying a 10 MHz noise power ratio signal (described in chapter 1) with PAPR of 10.7 dB. Next, in section 6.3, the feed network, biasing, and drain supply interconnect is discussed. Finally, section 6.4 presents the dynamic supply modulation measurements. The PA performance is characterized with the antenna

loading the PAs and with 50 Ω terminations at the output.

6.2 Supply Modulation of a Single Element

In order to evaluate the effect of the array environment, the performance of a single PA from the array is first characterized independently. The PA used in each element is a commercially available Qorvo GaN MMIC with part number TGA2598. These PAs have a peak output power of 2 W at 25 V drain bias. This PA operates from 6 GHz to 12 GHz with a small signal gain ranging from 24.2 dB at 6 GHz to 21.1 dB at 12 GHz and a PAE of 43% to 28% over the same range at 25 V. The MMIC PA is mounted on a copper-molybdenum (CuMo) carrier, and the GSG pads are bonded to alumina 50 Ω microstrip lines with mechanical transitions to SMA connectors. The supply modulator is a 4-level GaN MMIC implemented in the Qorvo 150-nm GaN on SiC process. This supply modulator was published in [109] and achieved 87.5% overall efficiency while tracking a 10 MHz long-term evolution (LTE) signal with an average output power of 3.5 W. This modulator is capable of providing greater than 30 W of dc power while switching between voltage levels at 100 MHz. A photograph of the MMIC PA and supply modulator is shown in Fig. 6.3.



(a) (b)

Figure 6.3: Photograph of (a) Qorvo TGA2598 2 W GaN on SiC PA and (b) four-level discrete GaN on SiC supply modulator. The figure in (b) is adapted from [3, Figure 5a, pg. 3]

The PAE and gain trajectories that result from supply modulation are shown in Fig. 6.4 for continuous and discrete supply modulation at 6.5 GHz and 11.5 GHz. The CW measurements are taken at drain voltages ranging from 10 V to 24 V in 2 V steps. A compressed flat-gain shaping function is used with a target gain equal to the small signal gain at the lowest drain voltage and

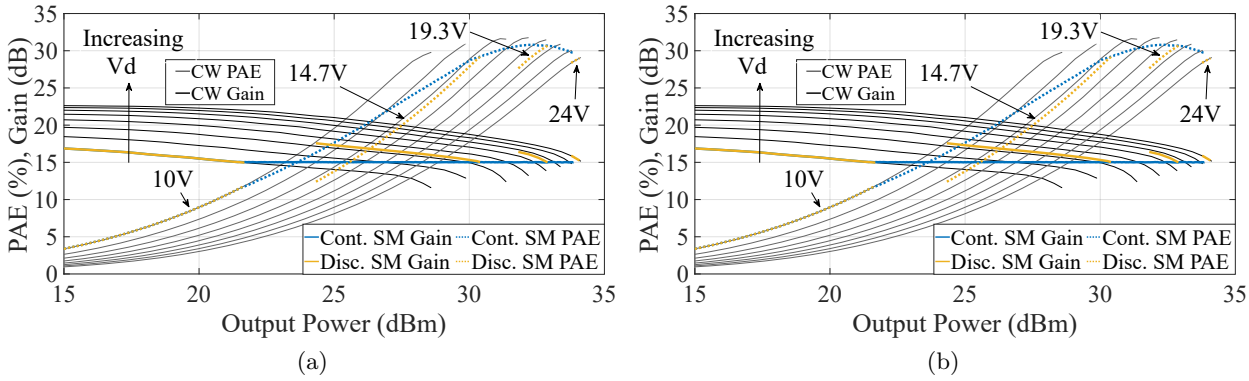


Figure 6.4: Measured PAE and gain trajectories chosen for compressed flat-gain with continuous and discrete supplies at (a) 6.5 GHz and (b) 11.5 GHz.

allowing 2.5 dB of compression to improve PAE.

The test signal used in this chapter is a noise-like signal, which consists of 30,001 equal amplitude, random phase carriers placed inside the 10 MHz signal bandwidth with a notch placed at the center of the band, which is 0.5 MHz wide and 5% of the total bandwidth. This signal is described in chapter 1 and is often referred to as an NPR signal. The normalized power spectral density of this signal is shown in Fig. 1.10a. The linearity of this signal is defined by the ratio of the average power in-band but power outside the notch to the power inside the notch as shown in Eq. 6.5:

$$NPR = \frac{P_{\text{in-band}} - P_{\text{notch}}}{P_{\text{notch}}} \tag{6.5}$$

where $P_{\text{in-band}}$ is the total average power in the 10 MHz signal and P_{notch} is the average power in the 5% notch.

A photograph of the experiment setup measuring a single PA is shown in Fig. 6.5. This setup is similar to the one described in chapter 3 except using the supply modulator shown in Fig. 6.3b and logic level converter board designed for this supply modulator. The baseband NPR signal is generated digitally using an arbitrary waveform generator, then upconverted through a vector signal generator and amplified through a commercial driver before feeding the PA input. The MMIC supply modulator (mounted on the raised PCB breakout board) is controlled using

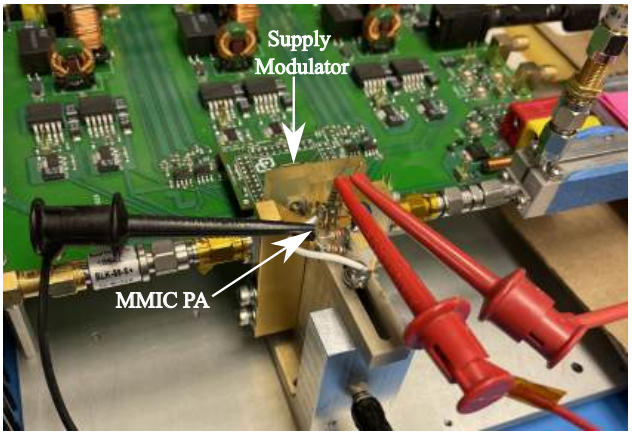


Figure 6.5: Photographs of supply modulation experiment setup for a single PA.

a bit pattern generator, which activates each discrete voltage level. The surrounding circuitry implemented on the main PCB performs logic level shifting between the bit pattern generator and gate drivers of the supply modulator, isolates the gate drive signal from ground, and provides the required auxiliary voltages necessary for the on-chip gate drivers. The input signal is time-aligned with the dynamic drain signal at the plane of the PA based on the measured delay through the drain supply interconnect. The input and output spectrum are both measured using a spectrum analyzer.

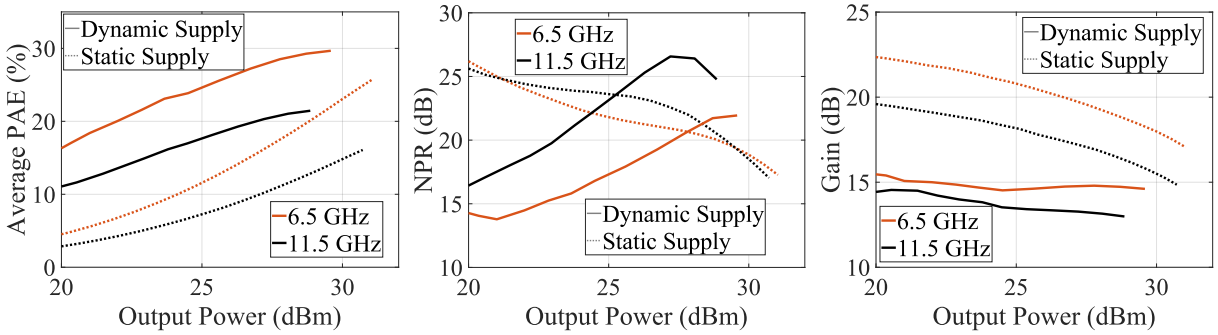


Figure 6.6: Supply modulation measurements of a single device compared to results with a static drain voltage of 24 V at 6.5 and 11.5 GHz. (a) Average PAE; (b) NPR and (c) gain as a function of output power.

Figure 6.6a shows the measured average PAE of the PA when amplifying the 10 MHz NPR at carrier frequencies of 6.5 GHz (orange) and 11.5 GHz (black). A constant drain voltage of 24 V

(dashed) is compared to discrete dynamic supply modulation varying the drain voltage between 10, 14.7, 19.3, and 24 V (solid). In these plots, the efficiency of the supply modulator is not taken into account, and only the PA efficiency is presented. The NPR is shown in Fig. 6.6b and the gain is shown in Fig. 6.6c. Compared to the static 24 V case, the efficiency improvement through dynamic supply modulation is approximately 10% points at both frequencies. At 6.5 GHz, the peak NPR improvement is 2.9 dB and at 11.5 GHz 4.4 dB. While supply modulation improves efficiency and, to some extent, linearity, it lowers the gain, as shown in Fig. 6.6c. This drop in gain is expected from the chosen compressed flat gain shaping function and results from the PA switching to lower drain voltages where decreased gains are observed.

6.3 Experiment Setup

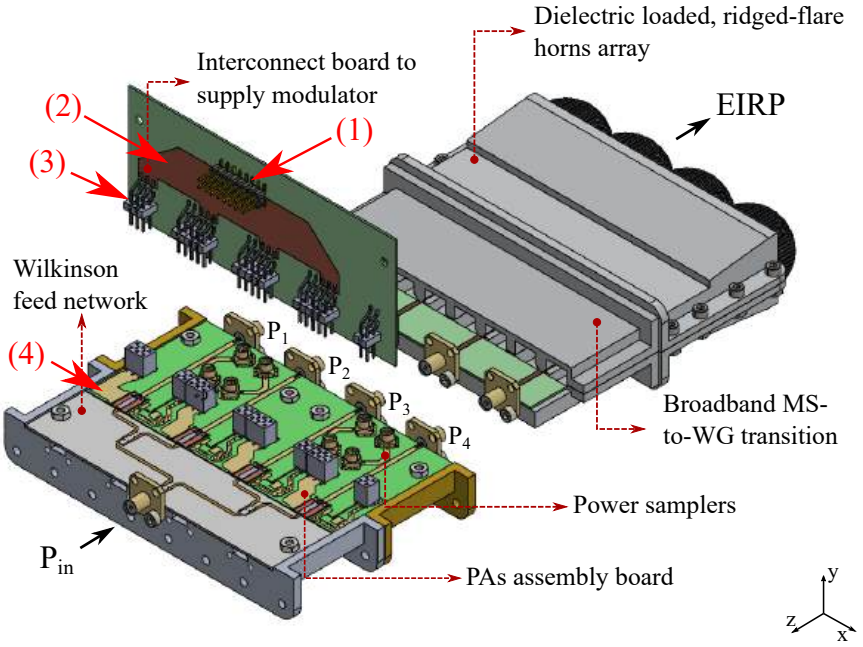


Figure 6.7: 3D view of the modular array showing the broadband Wilkinson feed network, PA assembly board with 4 MMIC PAs, interconnect bias network, microstrip-to-waveguide transitions to the radiators, and back view of a 4-element small-aperture dielectrically-loaded horn array. The modular approach allows characterization of the PAs with 50-Ω loads, as well as with the 4×1 antenna array. The labels (1) through (4) indicate the sections of the drain bias interconnect.

This section describes the design and experiment setup for measurements with the array.

A CAD drawing of the supply-modulated active transmit array is shown in Fig. 6.7 (courtesy of Dr. Laila Marzall). The modulated input signal is split through a four-way 6 to 12 GHz 3-section Wilkinson divider and fed to the individual PAs. The drain signal is supplied to the four PAs simultaneously, using the same four-level discrete supply modulator as in section 6.2. The drain signal is re-aligned at the PA input plane after implementing the array drain bias interconnect, which is modified from the single-PA case. A photograph of the prototype is shown in Fig. 6.8. The antenna array elements are double-ridge flared small-aperture horns designed for operation from 6 to 12 GHz, reported in [148].

The mechanical design of the array is modular in the z-direction (Fig. 6.7), allowing the measurement of output power with 50 Ω loads instead of the antennas. This is relevant since the broadband antennas couple at the lower part of the band, and it is of interest to evaluate the effect of the active reflection coefficient on supply-modulated PA efficiency.

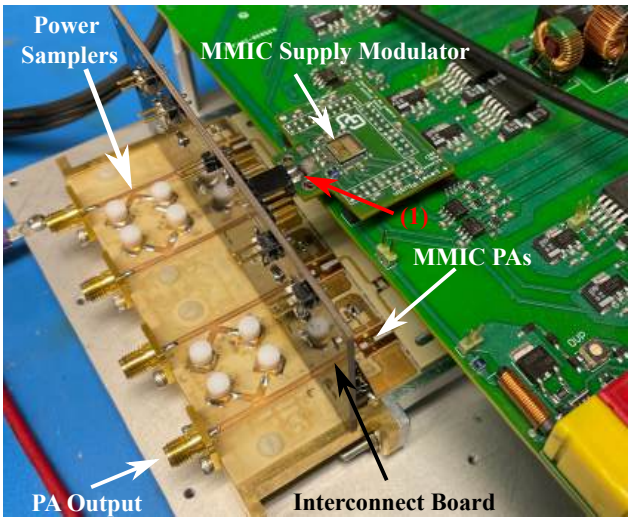


Figure 6.8: Photograph of the array, not showing the antennas for clarity. The bias interconnect network is connected to the 4-level MMIC supply modulator in a QFN package. The calibration power sampler couplers are also shown.

To accurately measure the output power at the PAs, a power sampling network consisting of microstrip directional couplers is inserted in each of the elements at the output of the PAs, pictured in Fig. 6.8. Additionally, a photograph of the Wilkinson divider, PAs, and output power sampler is shown in Fig 6.9 with the vertical bias board and antennas removed for visual clarity. The effect

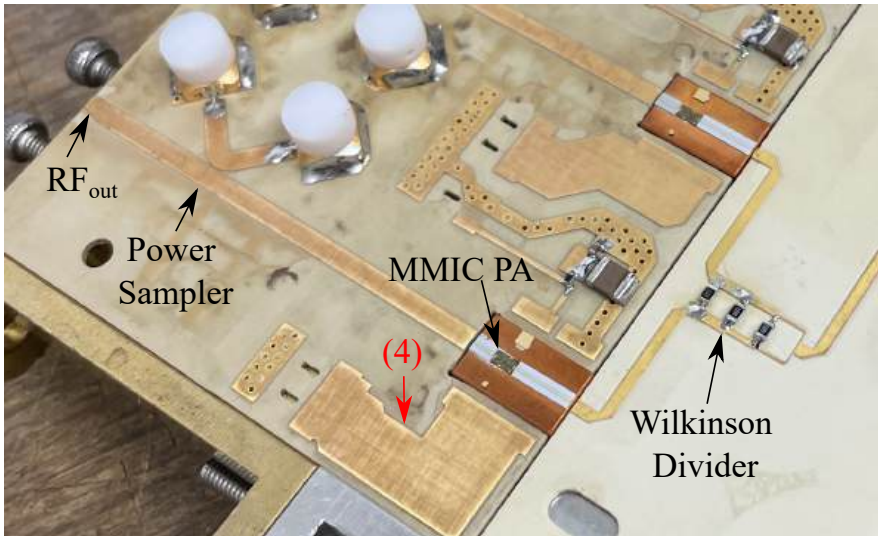


Figure 6.9: Photograph of PAs and beamforming network. The output of each PA is measured through a power sampler directional coupler. In this photo, the vertical biasing PCB is removed for visual clarity.

of the couplers is de-embedded, and the measurement reference plane is at the output of the PAs. The coupling factors of the power sensors are calibrated individually for each element by comparing the PA output power to the coupled power measurement. The loss in the samplers is measured with an identical separate board.

The biasing of the MMICs is accomplished through a co-designed network mounted perpendicularly to the array plane. The drain bias network is critical for supply modulation, requiring minimal inductance and capacitance in order to behave as a low-pass filter with a cutoff frequency beyond the modulation bandwidth [63, 149]. Fig. 6.7 shows the low-inductance interconnect designed to minimize loading between the supply modulator and PA array.

Since the drains of all the PAs use a shared supply and the threshold voltage of each chip varies, it is challenging to bias each PA to the appropriate quiescent current accurately. Therefore, the gate voltages are separated, and each PA gate bias is applied through a tunable potentiometer. Each potentiometer is fed by a common negative voltage, which is increased through the potentiometer since the negative voltage is divided. The potentiometer can be bypassed through manual jumper pins, which shorts the gate voltage to the common negative voltage, thus, pinching off

the PA. The biasing process starts by applying the common negative voltage to each PA (e.g., $-3\,\mathrm{V}$) with the potentiometers bypassed. Then, for one of the PAs, the jumper is removed, and the potentiometer is tuned until the appropriate current is measured through the shared supply. The jumper is returned to that element, bypassing the potentiometer and pinching off the PA but leaving the potentiometer in its tuned position. This process is repeated for each PA, and once each potentiometer is tuned, all the jumpers are removed, and thus, all PAs are biased to their appropriate quiescent current. One downside to this technique is that it does not account for variations in quiescent current due to temperature changes since each PA is biased with 75% less heat dissipation than when each PA is biased.

A photograph of the four PAs loaded with the antenna is shown in Fig 6.10. The outputs of each PA are connected to the antenna array through semi-rigid phase stable cables of equal length. When the PAs are loaded with $50\,\Omega$, the SMA terminations are placed directly at the outputs of the PAs without the cables.

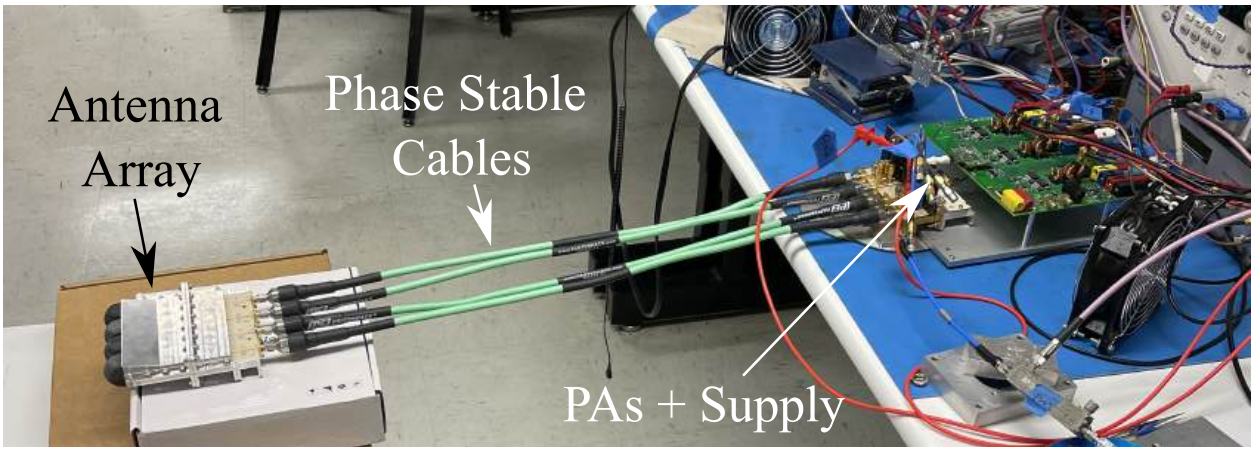


Figure 6.10: Photograph of the experimental setup. The PAs and beamforming network are connected to the antenna array through phase-stable cables of equal length. An absorber (not pictured here) is placed in front of the arrays to approximate operating in free space.

6.4 Dynamic Supply Measurements of an Array

Next, the PA array is characterized following the same procedure as for the single MMIC PA. First, the array is measured under CW excitation at 6.5 GHz in order to evaluate the performance

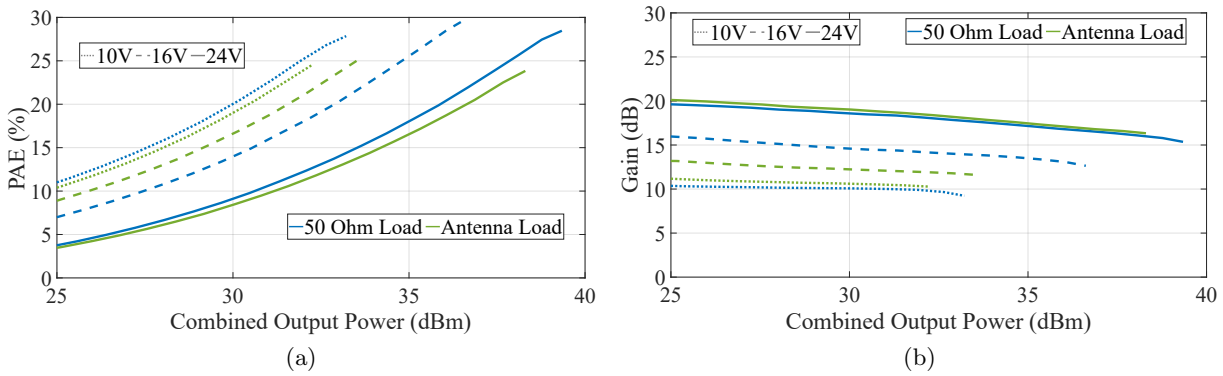


Figure 6.11: Measured CW (a) PAE and (b) gain for the array at 6.5 GHz with the four PAs loaded with 50 Ω loads (blue) and with antenna elements (green) at 10 V, 16 V, and 24 V. The PAE curves for different supply voltages are measured statically and averaged across the 4 PAs.

of the PAs integrated with the array. Fig. 6.11 displays the static characterization for drain voltages of 10 V, 16 V, and 24 V at 6.5 GHz. These values are almost identical to the same measurements for a single PA (not shown here), indicating that the PAs in the array are functioning properly and that the de-embedding through the coupler power samplers is accurate.

A distinct difference between the experiment setup measuring a single PA and the setup measuring an array of multiple PAs is the drain bias interconnect. For the single device setup, the supply modulator output is located a few centimeters from the drain of the PAs. In the array setup, the drain signal path is as follows, labeled in figures 6.7, 6.8, and 6.9:

(1) starts at the output of the supply modulator and connects to the verticle biasing board through a pin header connector.

(2) divided to each of the PAs through the biasing board.

(3) connects to the PA assembly board through right-angle pin header connectors.

(4) travels to the PA drain through wide PCB traces on the PA assembly board.

Although the drain bias line is designed to minimize parasitics, it still has significantly higher parasitic inductance and capacitance than the setup for a single device. This distorts the drain signal as discussed in chapters 4 and 5. Initial tests with similar shaping functions to those used

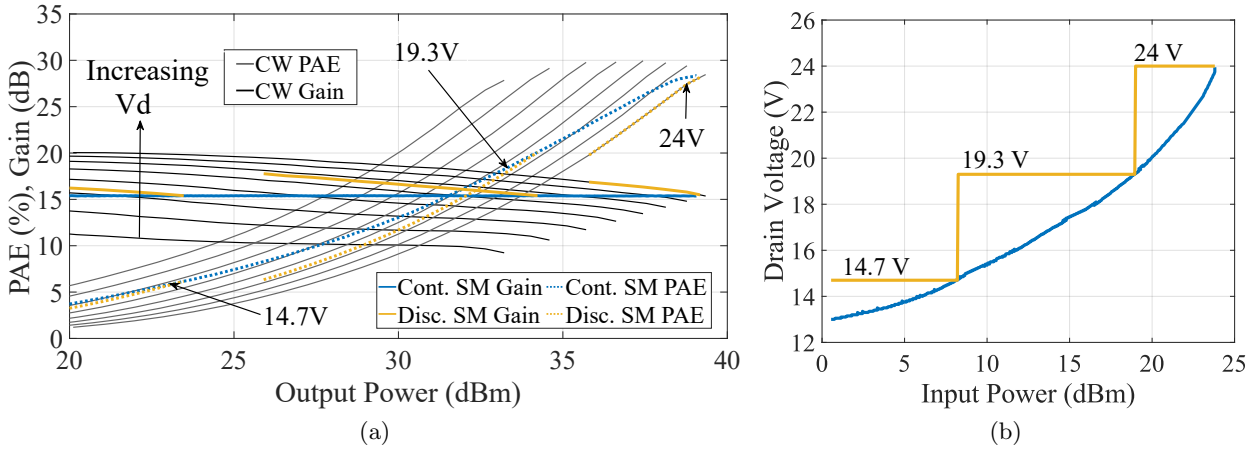


Figure 6.12: Measured PAE and gain trajectories chosen for compressed flat-gain with continuous and discrete supplies at 6.5 GHz when the PAs are loaded with 50 Ω. (b) shows the three-level shaping function.

Table 6.1: Active impedances presented at each port of the array

Freq. (GHz)	Z_1	Z_2	Z_3	Z_4
6.5	40.5+j8.5	38.5+j5.5	43+j21.0	49+j26.0

with the single device showed poor linearity and efficiency. Therefore, in order to reduce the number of switching instances, the number of levels is reduced to three, eliminating the lowest voltage level. This has the added advantage of reducing the gain variation. The total small-signal gain magnitude variation is 7.3 dB from 10 V to 24 V. However, by limiting the voltage range to the three highest voltage levels (14.7 V, 19.3 V, and 24 V), the small signal gain magnitude variation is reduced to 3.3 dB. Additionally, memory effects such as trapping and supply voltage drop-out are induced more frequently when switching to the lowest voltage level than the higher levels. Avoiding the lowest voltage level reduces the impact of these memory effects.

PAE and gain trajectories, which result from a compressed flat-gain shaping function, are shown in Fig 6.12b for continuous and discrete supplies at 6.5 GHz, loaded with 50 Ω. The corresponding shaping function is shown in Fig. 6.12a. A gain target of 17.4 dB was chosen with a compression range of 2 dB.

The supply modulation results of the array at 6.5 GHz are presented in Fig. 6.13 and Fig. 6.14.

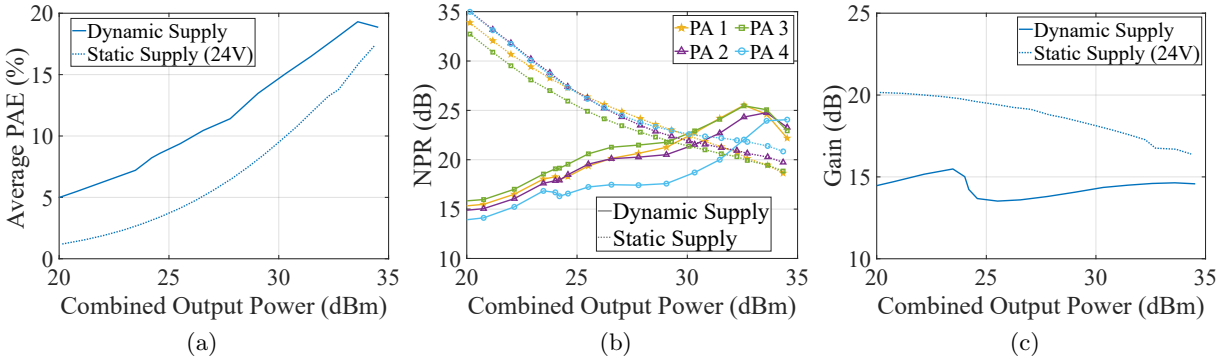


Figure 6.13: (a) Average PAE, (b) NPR, and (c) gain of the 4 combined MMIC PAs with a constant supply voltage of 24 V compared to the supply-modulated case with 10, 14.7, 19.3 and 24 V discrete levels, with **50-Ω loads** connected to each PA output.

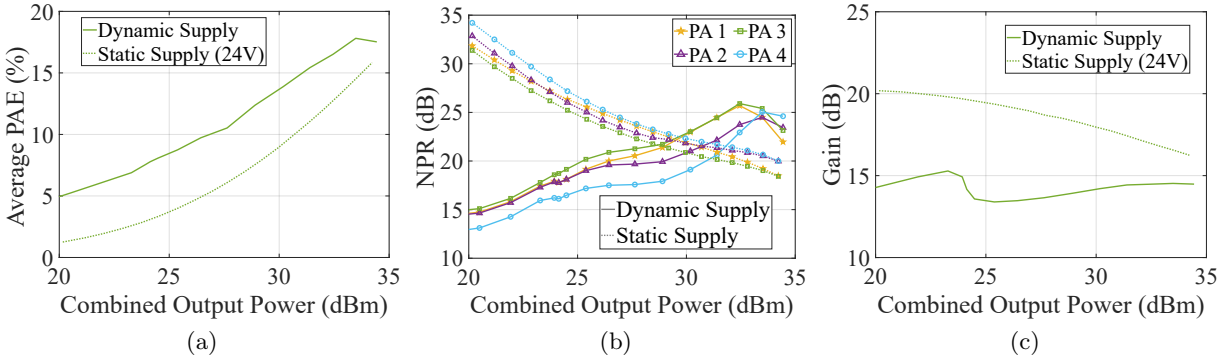


Figure 6.14: (a) Average PAE, (b) NPR at 6.5 GHz, and (c) gain of the 4 combined MMIC PAs with a constant supply voltage of 24 V compared to the supply-modulated case with 10, 14.7, 19.3 and 24 V discrete levels, with **antenna loads** connected to each PA output.

The PAE, NPR, and gain of the array are shown in Fig. 6.13. Here, the modulated dynamic drain voltage is compared to the static drain voltage case when the PAs are loaded with 50 Ω. For the PAE of these measurements, the loss in the supply modulator is de-embedded. Through supply modulation, the PAE and NPR are improved by 3.4%, and at least 2.5 dB at an output power of 33.6 dBm and frequency of 6.5 GHz.

The PA array is then loaded with antennas, and the measurements are repeated. The impedances presented to the PAs are shown in Table 6.1 at 6.5 GHz, measured at the passive antenna ports with the coupler S-parameters cascaded and de-embedded to the outputs of the PAs. Fig. 6.14 shows the results when the PAs are loaded with the antenna. When the PA array is

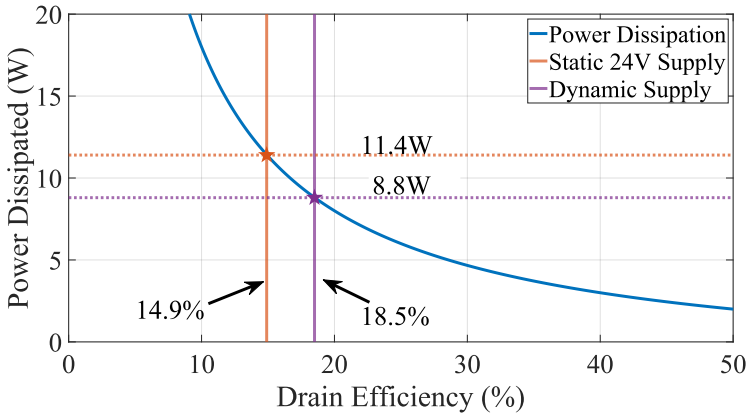


Figure 6.15: Power dissipation vs. drain efficiency with an output power of 2 W. The drain efficiency and power dissipation of the array are shown for a static 24 V and a dynamic supply.

loaded with antennas, a similar improvement in PAE and linearity is observed, while the overall efficiency is lower. Additionally, the NPR of the individual PAs is different due to variations in the MMICs and input/output wire bonding. Likewise, the different load impedances presented to each port by the antenna further affect the NPR of each individual PA.

6.5 Summary

In this chapter, dynamic supply modulation is demonstrated to be a solution for array efficiency and linearity enhancement through the hardware implementation and measurements of an active transmit 4×1 array with an operational bandwidth from 6 GHz to 12 GHz. The array amplifies a 10 MHz noise-like signal with a 10.7 dB PAPR. The array drain bias voltage is generated from a single discrete four-level GaN MMIC supply modulator switching at a maximum speed of 100 MHz. The results are presented at 6.5 GHz when the 2 W GaN MMIC PAs are loaded with 50 Ω loads and compared to loading with a 4-element small-aperture ridge horn array. The dynamic drain voltage measurements of the array are also compared with measurements taken on a single device.

Compared to a static 24 V supply, the PA efficiency is improved by approximately 3% points through dynamic supply modulation. Additionally, the noise-power ratio is improved by nearly 4 dB. The parasitic inductance and capacitance in the drain bias line of the array distorts the

dynamic drain signal. This effect was mitigated by reducing the number of voltage levels from four to three, which reduces the number of switching instances and lowers the gain variation. An alternative approach would be to reduce the maximum switching frequency of the supply modulator.

The efficiency could be improved further by adjusting the shaping function or using all four voltage levels. In both cases, the linearity will be degraded. However, the efficiency improvement reported here is not insignificant in the context of power dissipation. At an output power of 33 dBm, the array achieved a drain efficiency of 14.9% and 18.5% with a static and dynamic drain supply, respectively, when loaded by the antenna. The power dissipation is plotted vs. drain efficiency in Fig. 6.15 comparing the power dissipation at these two drain efficiencies. Through a seemingly small improvement in drain efficiency, the power dissipation in the PAs is reduced by 2.6 W, which is a 23% reduction. The results in this chapter are reported in [88].

Chapter 7

Conclusion, Summary, and Future Work

7.1 Thesis Conclusion

The fundamental challenge this thesis addresses is the efficiency and linearity improvement of PAs when amplifying complex amplitude-modulated signals through discrete dynamic supply modulation. Applying this technique to an active array consisting of multiple PAs requires many supply modulators or a single high-power supply modulator feeding the drains of all the PAs simultaneously. The latter is preferred since it reduces complexity. A high-power supply modulator was designed and fabricated, demonstrating a peak output power of 800 W at 20 V with a maximum switching speed of 10 MHz. This is the highest reported output power in a dynamic supply modulator to the best of the author's knowledge. However, high-power supply modulators have a limited switching speed due to the large parasitic capacitance and inductance in the high-power switching elements and trace interconnects. Furthermore, ringing that occurs while transitioning between discrete voltage levels limits the supply modulator switching speed. Both the limited switching speed and ringing degrades PA linearity.

The ringing is reduced through a novel gate pulsing technique. In this technique, the gates of the switching transistors in the supply modulator are pulsed on and off before reaching their final on-state. This puts the transistors in a lossy resistive state during voltage level transition and dampens the ringing. This technique is demonstrated to reduce ringing with only a 1% point cost to efficiency.

An alternative approach is to reduce the PAs sensitivity to changing drain voltage. It is

demonstrated that by mismatching the source/load impedance of PAs, the gain magnitude and phase dependence on drain voltage can be reduced across an octave RF bandwidth. Furthermore, by reducing this gain variation across the drain voltage of supply-modulated PAs, the linearity degradation due to low supply modulator switching speed is significantly reduced, and the non-linearities generated from ringing in the drain supply are suppressed. Therefore, the two major issues associated with the high-power supply modulator are circumvented by mismatching the power amplifier for reduced gain variation. This dispels the myth that matching supply-modulated PAs for peak efficiency yields the optimal system performance. The work in this thesis opens up the possibility of supply modulating many broadband PA elements in an array simultaneously with a shared drain supply generated from a relatively slow high-power supply modulator, amplifying large signal bandwidths with high efficiency and linearity.

7.2 Thesis Summary

A summary of this thesis for chapters 2-6 is provided below:

Chapter 2:

- This chapter presents an overview of a broadband supply-modulated system. The design and characterization of a two-stage 10 W GaN on SiC MMIC PA operating from 6 GHz to 12 GHz is demonstrated. Here, the PA operates from 6 V to 20 V and is matched for high efficiency at reduced drain voltages to improve average efficiency with a dynamic drain supply. The tradeoffs of continuous and discrete supply modulation are discussed along with the drain voltage to input power relationship referred to as a shaping function.
- A behavioral model of the 10 W MMIC PA is created from CW measurements. The performance of the PA amplifying a 67.5 MHz 64-QAM signal is predicted using this model at 6.5 GHz and 11.5 GHz with continuous and discrete supply modulation. The PA is also evaluated with three shaping functions: flat-gain, compressed flat-gain,

and maximum PAE. For continuous supply modulation, the flat-gain shaping function yields the best EVM, the maximum PAE shaping function yields the highest average PAE, and the compressed flat-gain is a compromise between the two. Using a discretized drain voltage instead of continuous reduces the PAE by a few percentage points but has a larger impact on linearity.

- At 11.5 GHz, the small signal gain magnitude at the lowest drain voltage (6 V) is equal to the compressed gain magnitude at the peak PAE for the highest drain voltage (20 V). This results in the PAE trajectory from a flat-gain shaping function being nearly identical to the PAE trajectory from a maximum efficiency shaping function. This large signal characteristic of the PA results from an optimal degree of gain magnitude variation across drain voltage. Modulated signal simulations at 11.5 GHz show that the average PAE is identical for the three shaping functions, but the linearity significantly improved with a flat-gain shaping function. These contributions are published in [66].

Chapter 3:

- This chapter examines the impact of gain magnitude/phase variation across drain voltage on supply-modulated GaN PAs. Initial load/source pull simulations reveal matching conditions that minimize gain variation. Three simulated PA designs with different source/load impedances are simulated with the CW harmonic balance simulator in AWR, from which a behavioral model is built and used to evaluate the PAs with modulated signals in a custom-built MATLAB envelope simulator. Through these simulations, it is shown that mismatching the source and load impedance for reduced gain variation improves the efficiency and linearity of a supply-modulated PA.
- A broadband application of this approach is realized through the design and characterization of a two-stage 5 W 6 GHz to 12 GHz GaN on SiC MMIC PA. The source and load impedance of this PA is mismatched to reduce the gain magnitude and phase

variation with the first-stage drain supply fixed and the second-stage drain voltage modulated from 14 V to 28 V. The small-signal gain magnitude and phase variation of the PA is low across the bandwidth, and the simulated gain variation of the PA is accurately predicted from the source/load impedances presented to one of the reactively combined second-stage transistors. This PA is measured with a four-level GaN MMIC supply modulator. The dynamic supply measurements with a modulated signal are compared with predicted results from the envelope simulator and behavioral model built from CW power sweep measurements at multiple stepped drain voltages. For a static drain voltage, the agreement is excellent. The error is higher with the dynamic supply but still shows good agreement. This indicates that PA linearity is dominated by the supply voltage and compression characteristics of the PA, and memory effects are a second-order effect.

- In simulations, the PA designed for low gain variation exhibited less linearity degradation than a conventionally designed PA when the maximum switching frequency of the discrete drain supply is reduced from 100 MHz to 25 MHz. Similar results are obtained in measurements of the 5 W PA. This shows that PAs designed for low gain variation are more resilient to bandwidth limitations in the drain supply. This has the potential to enable the supply modulation of PAs, amplifying a high instantaneous signal bandwidth with a much lower bandwidth supply modulator. These results are detailed in [80].

Chapter 4:

- The design and characterization of a high-power discrete supply modulator is presented. This four-level modulator is suitable for the efficiency enhancement of multiple PAs with a shared drain voltage, amplifying high peak-to-average power ratio signals in an array. The peak measured output power is 800 W at 20 V, which is the highest reported output power of a supply modulator to the best of the author's knowledge.

Additionally, for powers exceeding 50 W, the efficiency is greater than 92%, and a maximum switching frequency of 10 MHz is achieved. The high performance is enabled through careful selection of the semiconductor technology and switching transistors to minimize parasitic capacitance and on-state resistance for high current devices.

- The primary limitation on the switching speed of the supply modulator is the ringing in the output voltage waveform that occurs upon each switch transition. Additionally, this ringing mixes with supply-modulated PAs and adds distortion. The source of the ringing is the parasitic capacitance, inductance, and resistance in the transistors, gate driver, and output trace interconnect, which behave as a low-pass filter. By simulating the S-parameters of the passive output trace in a full-wave electromagnetic method of moments simulator and fitting it to an equivalent RLC circuit compatible with LTspice time domain simulations, the ringing is accurately predicted. To improve the modeling further, a custom model of the transistors utilizing non-linear capacitors is developed from S-parameter measurements and implemented in LTspice. However, the results of this simulation did not improve output waveform prediction.
- The ringing frequency is primarily determined by the reactive parasitics in the transistor, while the overshoot and decay rate are a strong function of the resistive losses. By modeling the output trace, the ringing frequency is accurately predicted, but the amplitude and decay rate deviate from the measured results. One possible explanation is that the resistive losses in the transistor are not accurately predicted. These losses are strongly dependent on the temperature of the transistor. A thermal model is included in the manufacturer's model, and the thermal resistance of the transistor heat sink is implemented. However, precise modeling of the transistor's thermal behavior is difficult and could be addressed in future work. Additionally, parasitics and temperature variation in the resistive loads are not modeled and can be a potential source of error. The observations in chapter 4 are detailed in [83, 135].

Chapter 5:

- This chapter experimentally validates a new ringing reduction technique for multi-level supply modulators. This gate pulsing technique does not require additional circuitry and is flexible, allowing the pulse timing for individual voltage transitions and different power levels to be individually optimized.
- Gate pulsing reduces the ringing beyond what dead-time and variable gate resistance are capable of with only a small drop in efficiency. This technique is applied to a 800 W multi-level converter while tracking the envelope of an 6.25 MHz 64–QAM signal. Compared to a reference case with conventional gate driving, the ringing amplitude and duration are reduced with less than 1% point cost to efficiency. The improvement in ringing reduces in-band and out-of-band distortion created by the supply modulator. These contributions are published in [84].

Chapter 6:

- In this chapter, dynamic supply modulation is demonstrated to be a solution for broadband array efficiency and linearity enhancement through the hardware implementation and measurements of a 6 GHz to 12 GHz active transmit 4×1 array. The system is supply-modulated with a four-level discrete MMIC supply modulator. The results are compared when the GaN MMIC PAs are loaded with 50 Ω and a 4-element small-aperture ridge horn array. The performance is degraded when loaded with the antenna array. However, compared to a static 24 V supply, the efficiency and linearity are improved through dynamic supply modulation with each loading case.
- Filtering due to the drain bias interconnect between the supply modulator and PA drains reduced PA performance. By adjusting the shaping function such that the modulator only switches between the three highest levels, the number of switching instances is reduced, and distortion due to the bias interconnect is reduced. An

alternative approach would be to reduce the maximum switching frequency of the supply modulator. Compared to a static 24 V supply, the PA efficiency is improved by approximately 3% points through dynamic supply modulation. Additionally, the noise-power ratio is improved by nearly 4 dB. Dynamic drain measurements with a four-level supply modulator are taken on a single PA and show similar improvements in linearity but significantly higher PAE improvements (nearly 10% points). This is mostly due to the adjusted shaping function only utilizing three voltage levels on the array.

- The array's efficiency could be improved further by adjusting the shaping function or using all four voltage levels, but this would reduce the linearity. However, the efficiency improvement reported here is not insignificant in the context of power dissipation. Through a seemingly small improvement in efficiency, the power dissipation in the PAs is reduced by 23%. These contributions are published [88].

7.3 Future Work

- Future work related to chapter 3 includes examining how different technologies/device sizes affect gain variation. For linearization through flat-gain shaping functions, gain variation is necessary, but the optimal degree of gain variation has yet to be determined. In chapter 2 with the 10 W MMIC PA, the PAE trajectory at 11.5 GHz from a flat-gain shaping function is identical to that of a maximum PAE shaping function. Simulations with a continuous supply and flat-gain shaping function showed nearly perfect linearity ($< 1\%$ EVM) and identical PAE to a maximum PAE shaping function. This opens up the possibility of optimizing the gain magnitude variation and compression characteristics to achieve simultaneous flat-gain and maximum efficiency across output power.

- The limiting factor of the high power supply modulator presented in chapter 4 is the ringing in the output waveform. Different output trace interconnect geometries could designed to

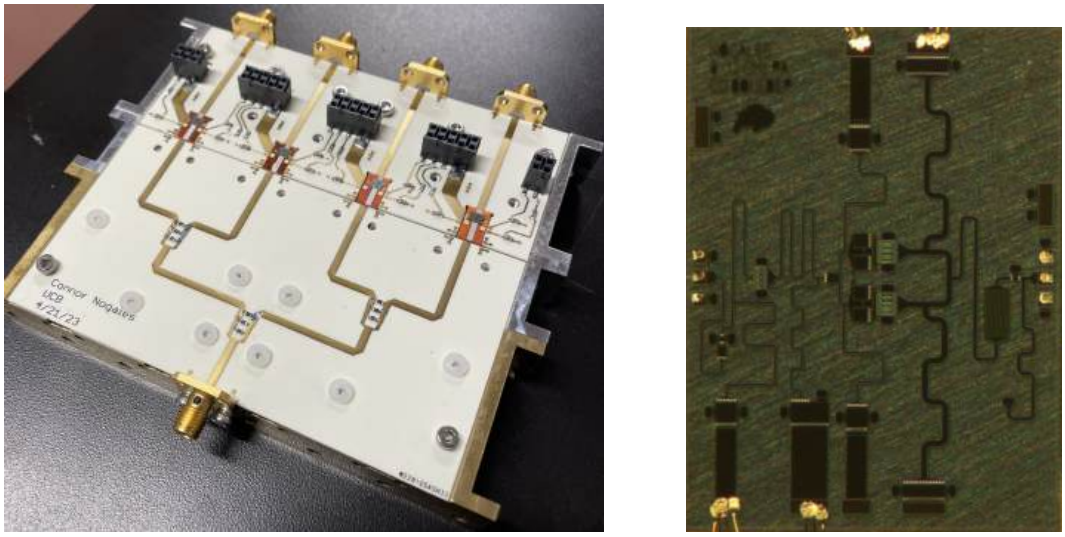
minimize the ringing. Additionally, an RC snubber network on the output trace could be investigated to reduce ringing. A snubber network implementation was attempted with the high power supply modulator. However, the large amount of power dissipated in the surface mount resistor resulted in thermal failure. Successful implementation of a snubber network would require some type of thermal management of the resistor.

- The gate pulsing technique presented in chapter 5 can be extended by integrating it with a PA. In this implementation, the PA drain impedance is the supply modulator load and changes as a function of input power to the PA. Since the pulse parameters change with different load impedances, the pulse parameters would need to be integrated into the shaping function. The look-up-table approach of the pulse parameters would have an added dimension to include the instantaneous power applied to the PA. This requires characterization of the pulse parameters over a wide range of load impedance or in situ optimization. Accurate modeling of the supply modulator and gate driver could allow for the optimal pulse parameters and dead-time to be determined as a function of the PA load impedance without empirical characterization through measurements. Additionally, this gate-pulsing technique could be investigated with a MMIC supply modulator. The gate drivers on MMIC supply modulators have a higher switching speed than PCB implementations. The higher switching speed/slew rate allows for finer control of the gate input drive signal. Therefore, it opens up the possibility of improved ringing reduction.

- In chapter 6, all the measurements of the array are taken with equal phases applied to the PA elements. Beam steering creates additional challenges when a single modulator is used for all the elements in the array. Tracking the envelope of any one PA element creates drain voltage to signal envelope misalignment in the other elements, which increases with more elements, higher beam steering angles, and higher modulation bandwidths. To avoid this issue, the drain modulator must track the maximum instantaneous value between each element. This ensures that the envelope of the elements is not clipped, which would result

in significant distortion. At a given instance, each of the PAs will operate at a different level of compression. Power-dependent amplitude and phase distortion will affect the radiation patterns. Conventional active arrays are subject to this issue. However, the problem is exacerbated with supply modulation since the PAs are continuously saturated. The degree to which this affects the radiation patterns is a question yet to be answered.

- An obvious extension of the work in chapter 6 is to scale to higher power PAs and more elements. The 2 W commercially available Qorvo PAs are not optimized for supply modulation and have a relatively small output power. Thus, the full benefits of supply modulating an array are not observed. Utilizing higher-power PAs designed for supply modulation could yield larger improvements in power dissipation and system efficiency/linearity. The re-designed RF feed network and array assembly board are shown in Fig. 7.1a.

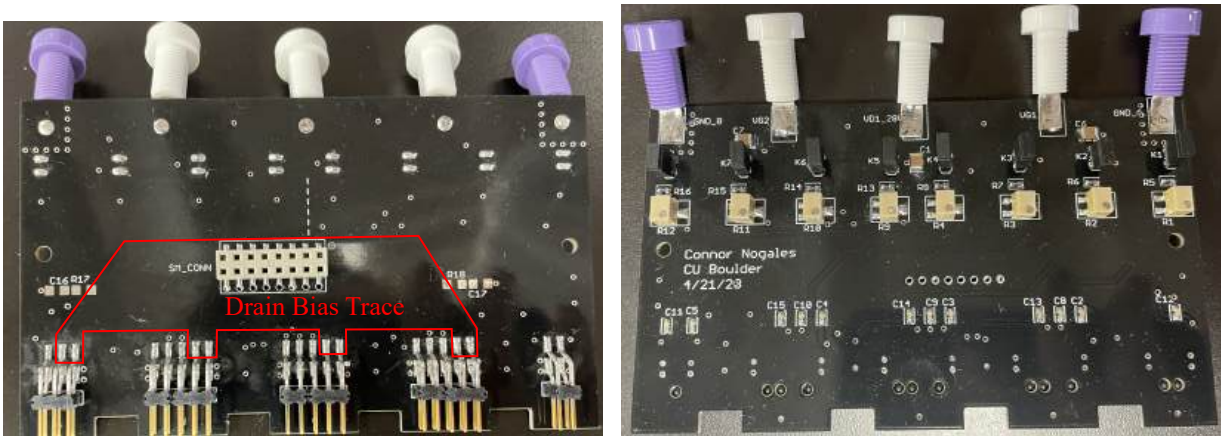


(a) (b)

Figure 7.1: (a) Photo of the re-designed broadband Wilkinson feed network and PA assembly board. (b) Photo of the 5 W MMIC PAs designed for high efficiency with a dynamic supply voltage.

This re-design supports two-stage 5 W GaN PAs designed for supply modulation and photographed in Fig. 7.1b. The performance of these PAs is described in appendix A. The microstrip power samplers used in chapter 6 will be replaced with commercially available external couplers that have a higher directivity and are less sensitive to mechanical manip-

ulation. The vertical biasing board is also re-designed to support independent biasing of the PA's first and second stages. Photographs of both sides of the new biasing board are shown in Fig. 7.2



(a) (b)

Figure 7.2: Photograph of the un-populated re-designed vertical array biasing board. (a) Front side of the board with the drain bias trace outlined in red. (b) Back side of the board with pads for tunable potentiometers used to bias each PA.

- Applying a taper to the power of the elements in an array can reduce side-lobe levels. This is typically implemented by reducing the input power to some PA elements using an attenuator or variable gain amplifier. However, this reduces the efficiency of those PA elements since they are operated in backed-off. The efficiency of these backed-off PAs can be improved with a fixed offset, lowering the average dc voltage applied to the tapered elements.

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Appendix A

A MMIC PA Designed for High Efficiency

In this appendix, the measurements of a 5 W GaN MMIC PA are presented. This PA is designed and fabricated in the WIN Semiconductor NP15 150 nm GaN-on-SiC process and co-designed with the low gain variation PA presented in chapter 3, using the same device sizes and bias points. However, the PA presented in this appendix is designed for high efficiency with a dynamic drain supply and peak efficiency at 19 V instead of low gain variation across drain voltage. The intention of this PA design is to compare with the low gain variation PA. A photograph of the PA is shown in Fig. 7.1b. This PA is mounted on a CuMo carrier, and CW measurements are performed on-wafer with the same setup presented in chapter 2. The large signal CW PAE, gain, output power, and input power are plotted vs. frequency in Fig. A.1 at drain voltages 14 V, 21 V, and 28 V. For these plots the input power at each frequency point is adjusted for peak PAE.

A.1 CW Simulation and Measurements

The measured and simulated PAE is plotted vs. output power in Fig. A.2 at frequencies of 6.5 GHz, 9 GHz, and 11.5 GHz. Additionally, the measured and simulated gain is plotted vs. output power in Fig. A.3 at the same frequencies. For both of these figures, the drain voltage is swept from 10 V to 28 V in 2 V steps at each frequency.

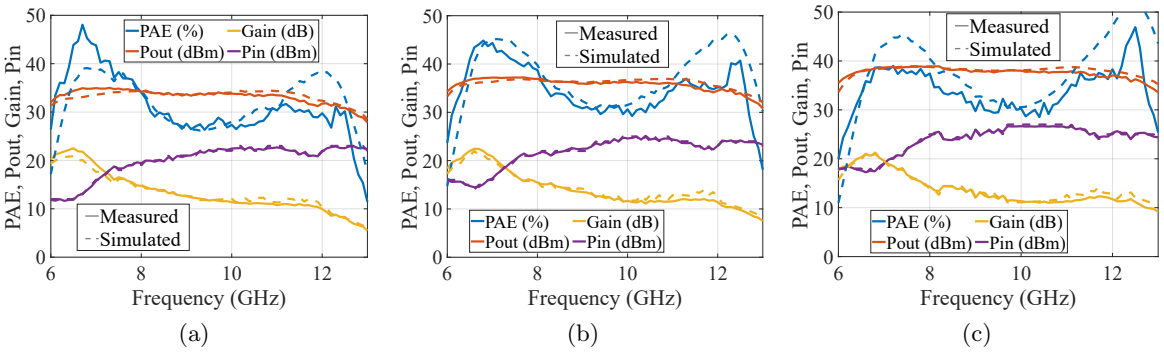

Figure A.1: Simulated and measured large signal performance from 6 GHz to 13 GHz at drain voltages of (a) 14 V, (b) 21 V, and (c) 28 V.

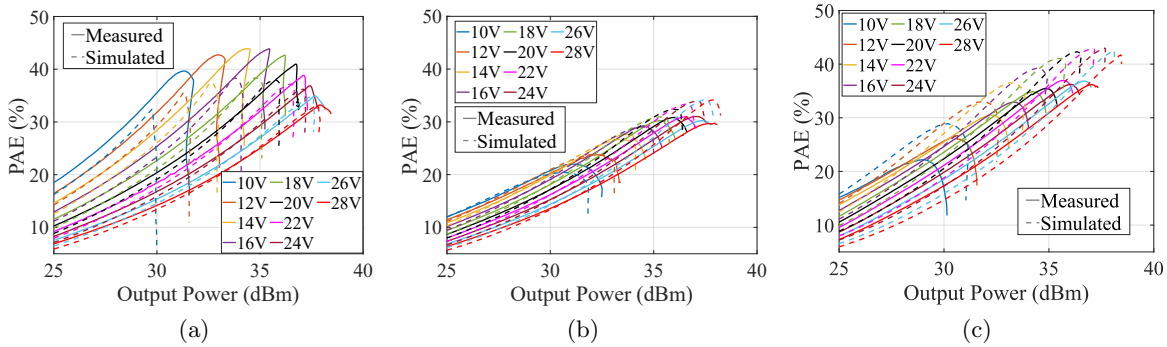

Figure A.2: Simulated and measured CW PAE vs. output power at frequencies of (a) 6.5 GHz, (b) 9 GHz, and (c) 11.5 GHz. At each frequency, the drain voltage is swept from 10 V to 28 V in 2 V steps.

A.2 Modulated Signal Envelope Simulations

The CW measurements are used to build a behavior model of the PA. This model is used to predict modulated signal performance with a dynamic drain supply in the same manner as presented in chapter 3 and 2. The PA is simulated with a 67.5 MHz 64-QAM signal and ideal discrete supply modulation with maximum switching speeds of 25 MHz and 100 MHz. The average input power at each frequency point is selected for a constant output power of 31 dBm from 6 GHz to 13 GHz. The EVM and ACPR are presented in Fig. A.4a. The PAE and gain are shown in Fig A.4b. The dynamic drain supply results are compared with a static 28 V supply. Across the bandwidth, the efficiency is improved through dynamic supply modulation at both switching speeds. Furthermore,

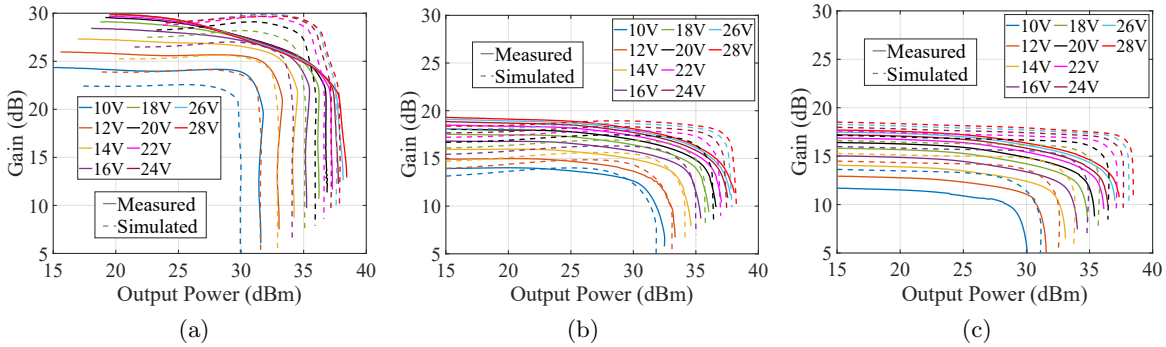

Figure A.3: Simulated and measured CW gain vs. output power at frequencies of (a) 6.5 GHz, (b) 9 GHz, and (c) 11.5 GHz. At each frequency, the drain voltage is swept from 10 V to 28 V in 2 V steps.

the PAE is nearly identical when the maximum switching speed is reduced from 100 MHz to 25 MHz. At the center of the band, with a maximum switching frequency of 100 MHz, the EVM and ACPR are improved over the static case. When the maximum switching speed is reduced, the linearity is degraded much more than the PAE and gain.

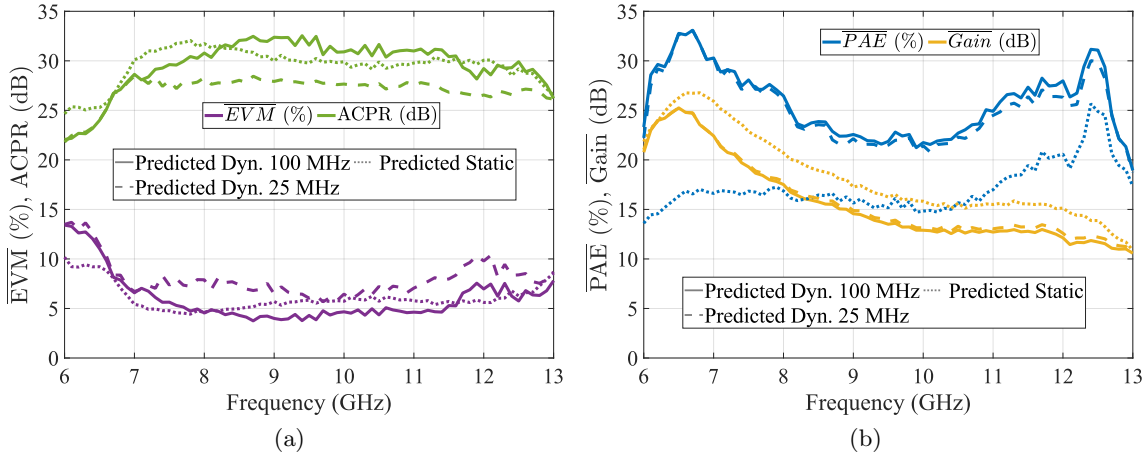

Figure A.4: Measured and predicted results comparing a static 28 V supply to a dynamically changing drain supply with two maximum switching frequencies of 100 MHz and 25 MHz in terms of (a) linearity and (b) PAE and gain, for a constant output power of 31 dBm.

Since this PA was designed for maximum efficiency at 19 V, the source and load impedances are relatively close to the impedances of the low gain variation PA. Therefore, the performance of this PA isn't significantly different from the PA presented in chapter 3. If this PA were designed for

maximum efficiency at 28 V instead, the difference in performance would likely be more pronounced.