GaN MMICs for Millimeter-Wave Front Ends

by

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The body of work presented in this thesis addresses the need for higher-power W-band MMIC circuits to enable communications, radar and sensing at millimeter waves were spectrum allocation is still growing and evolving. This work is funded by the DARPA millimeter wave GaN maturation (MGM) program aiming to scale GaN devices and models for use in amplification and mixed signal circuits. To address the goal of the program, designs of fundamental front end circuits for functions including frequency translation, power amplification (PA), low noise amplification (LNA) and control are realized using 40nm GaN-on-SiC HEMTs. Integration of these different MMIC circuit components is explored to additionally determine the accuracy of the models in a system level operation.

Demonstrated GaN MMIC circuits in the HRL T3 process at W-band include a three stage power-combined balanced amplifier, two frequency doublers, a balanced frequency tripler, 90° and 180° phase shifters, a three stage LNA and an on-chip T/R half duplex front end. The design methodology, device selection, device characterization, MMIC layout and measurement of each of these circuits is analyzed and discussed. A single-HEMT resistive mixer, power detector and full W-band Dicke radiometer are also designed and fabricated but remain to be measured. Results show viable high-performing GaN HEMT MMIC circuits which can be implemented in existing applications to increase power density and performance.

Dedication

For my family.

Pour ma famille.

Dla mojej rodziny.

Acknowledgments

I would like to express my deepest gratitude to Professor Zoya Popović, my advisor, whose guidance, expertise, and unwavering support were instrumental throughout the course of this research. Professor Popović's mentorship has been invaluable, and her commitment to academic excellence has been a source of inspiration. Special thanks to my Ph.D. committee for their insightful feedback and constructive input that greatly contributed to the refinement of this work. Each member played a crucial role in shaping the trajectory of this research, and their collective expertise significantly enriched the quality of this thesis.

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Contents

List of Tables

List of Figures

Chapter 1

Introduction

Contents

The millimeter-wave frequency range includes the free space wavelengths which are on the order of millimeters, from 30 GHz to 300 GHz. Several radar wave guide-bands span the millimeter-wave, all of which are summarized in Table 1.1. Crowding in lower bands, defense interests as well as semiconductor scaling has added new importance to millimeter-wave systems and particularly recently to the W-band and above. The contents of this Thesis will be focused on the millimeter-wave range of the spectrum and primarily the W-band within that, as denoted in Fig 1.2.

Table 1.1: Millimeter-Wave Wave-guide Frequency Bands

Frequency bands	Frequency Range (GHz)
Q	30-50
U	40-60
V	50-75
E	60-90
W	75-110
F	90-140
D	110-170
G	110-300

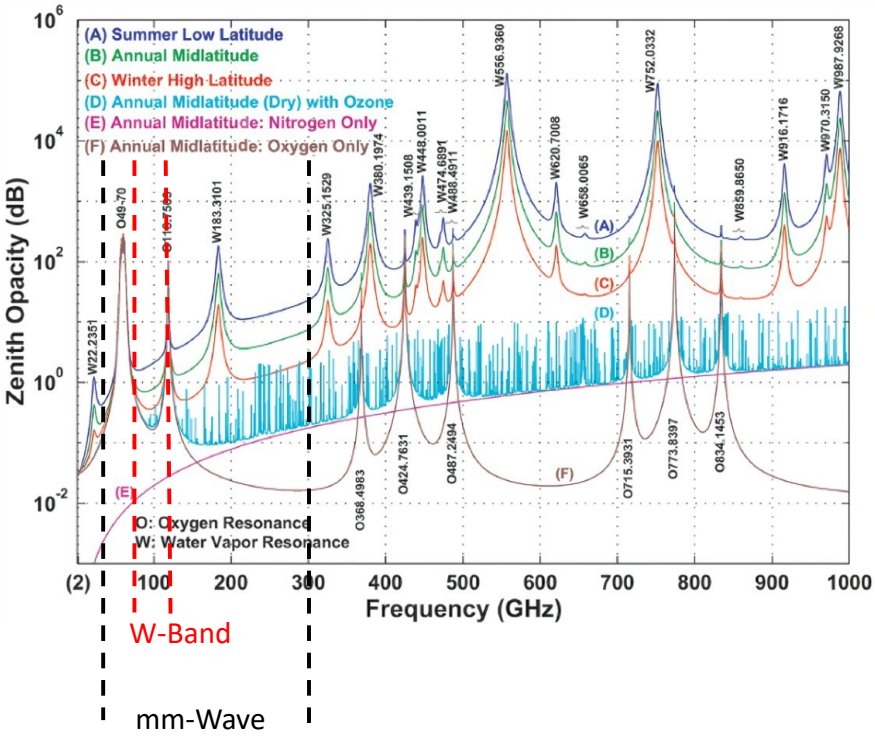


Figure 1.1: Atmosphere attenuation shown for different latitudes, seasons and several molecular concentrations, from [1]. The millimeter-wave frequency span and within that the W-band wave-guide band are highlighted in the spectrum.

1.1 W-Band Applications

Allocation of the spectrum between 50 and 110 GHz is still evolving and growing. Current uses include radar for both military and civilian use, radiometry including radio-astronomy and imaging as well as communication links for terrestrial and space based systems. With over-crowding in lower bands, the large

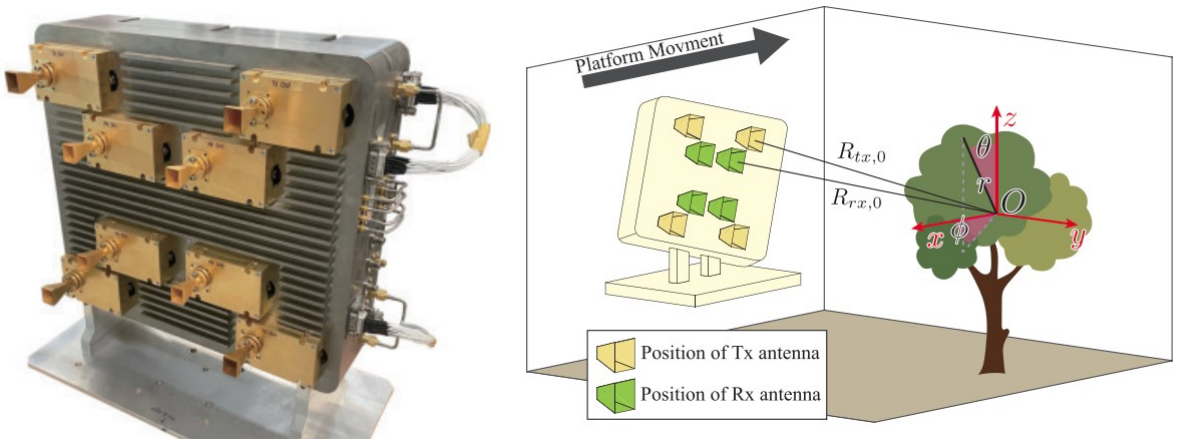
fractional bandwidth available when operating within the V- and W-bands offers an attractive high data transfer possibility and potential for fewer data links.

In the past, wireless communication primarily operated within frequency ranges below 30 GHz, where atmospheric losses are lower, as shown in Fig. 1.2. However, due to the increasing demand for sub 50 GHz spectrum, allocations in V- and W- band become increasingly attractive. Some of these frequency bands include the FCC authorized private sector point-to-point links from 71-76, 81-86, and 92-95 GHz, the automotive radar bands at 76-77 and 77-81 GHz and the FCC unlicensed 57-71 GHz band. Recent data indicates that an increasing amount of radios are being sold at V-band compared to Ka- and Q- band previous models [17] showing the growing trend towards higher millimeter-wave frequency systems.

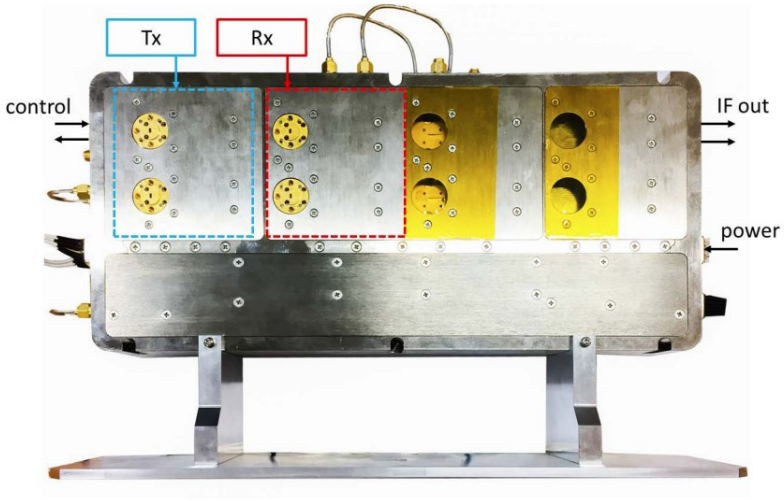
Communications rates of 91.6 Gb/s and 78 Gb/s have been reported using 64QAM on W-band links in [18] and [4] respectively. Use of lower order constellations of 16QAM has also been demonstrated showing data rates of 8 Gb/s at 75 GHz [19]. Less crowding in these bands results in less interference for the desired signal. Smaller component size from millimeter wavelengths allows more phased array elements to be utilized increasing the directivity of the transmitted beam. Using the high absorption of W-band channels as a filter to highly attenuate possible interfering signals coupled with increased directivity aids to secure communications lines [20]. These properties also open the door to emerging applications such as deep space in the aerospace industry.

Various radar platforms have been demonstrated in W-band such as automotive radar, cloud Doppler [21], 3-D imaging and unmanned aerial system (UAS) detection [22]. Imaging at W-band has obtained a measured resolution of 0.14 [3] and 0.33m [2]. The short wavelengths enable this high level of resolution and are useful in applications such as hidden object detection for security scanners [23–26] and automotive radar for automated driving [27]. These applications also benefit from the ability to sense through visibly obstructive environments such as snow, fog and dust as well as materials such as clothing [28, 29].

Cloud Doppler radars have long operated at 94 GHz and benefit from the integrated use of GaN amplifiers which gives the system higher power and increased performance [21]. A 7 KW transmitter was demonstrated by Raytheon at 92 GHz [30] which is the highest published solid-state W-band transmitter and is intended for an active denial weapon. The transmitter spatially coherently combines 8,192 GaN-on-SiC MMIC PAs, each



(a)



(b)

(c)

Figure 1.2: Hardware photographs of several W-band applications: (a) beat frequency division FMCW radar for imaging [2] (b) MIMO radar with simultaneously transmitted orthogonal wave forms for high resolution imaging [3] (c) UAS or Drone detection radarwith four channels [4].

with over 1 W of power and PAE > 20% around 93 GHz. This approach is modular and therefore scalable, with high demonstrated power-combining efficiency.

Radiometry involves the amplification and rectification of inherent electromagnetic radiation from anything above 0 Kelvin. The National Radio Astronomy Observatory (NRAO) has used the W-band for radio-astronomy with cryogenically cooled receivers [31]. Passive imaging requires a single radiometer on a movable mount or an array of multiple radiometers to collect the imaging data. With the large available bandwidths, radiometers at W-band have the benefit of requiring less gain for the same temperature resolution

compared to lower bands. The drawback of passive imaging is reduced resolution at longer distances [32].

1.2 Millimeter-Wave Challenges

The attenuation at millimeter-waves due to atmospheric conditions is higher than at lower microwave frequencies where most satellite down- and up-links currently exist. This can be seen in Fig 1.2 were atmospheric attenuation is shown across the spectrum. Change of elevation, frequency, time and geographical location all have an impact on atmospheric conditions. Several types of free space losses exist when propagating signals at millimeter-waves: atmospheric gases attenuation, precipitation, foliage blockage, scattering effects, and diffraction [33]. Water vapor and oxygen are the primary causes of atmospheric gas attenuation which varies in frequency based on the mechanical resonant frequencies of the gas molecules.A W-band signal propagating through the atmosphere will be attenuated, but can also become depolarized from scintillation or hydrometers which are water droplets or clouds. The refractive index may vary spatially and could cause a change in the direction of propagation. When it comes to scattering effects, the smaller the wavelength is, the more rough the surface will appear and cause more diffused reflection. All of these effects coupled with other weather conditions including temperature, pressure, water vapor density, cloud cover and precipitation create a difficult environment to reliably transmit and receive data at W-band frequencies. As a result, satellite and terrestrial communication links at millimeter-waves will have to be well modeled and characterized before they can be properly utilized [34].

1.3 Motivation

High attenuation of the atmosphere, potential for signal depolarization and lack of devices that can generate the required power has hampered the use of the spectrum at higher millimeter-wave frequencies. Even with proper characterization of W-band satellite links, difficulties arrive in propagating signals through the atmosphere. Overcoming these obstacles can be tackled in digital post processing [34]; however, analog advancements need to be implemented for a sustainable long term solution.

In the past, III-V compound semiconductors lack the power density to be used for millimeter wave

communications. Recently GaN, the largest bandgap semicondcutor used for transistors, has acheived $f_t/f_{max} = 300/500$ and power densities over 6 W/mm [35]. These recent advancements can be used to overcome the challenges involved with operating electromagnetic systems at milimeter-waves and particularly the W-band. With watt-level performance at W-band already demonstrated [36], GaN shows viable power density for applications requiring robust power handling and kilo-Watt power levels.

Silicon-based circuits have shown high-frequency operation with medium level power but fall short of reaching the power density of GaN. A study by [37] compared the number of elements needed for 5G requirements between different semiconductor technologies. Using efficiency values of 20 % for GaN, 15 % for GaAs, and 22 % for CMOS and SiGe, the study found that using GaN PAs requires only 30 % of the array elements needed for CMOS or SiGe MIMO arrays. This reduction in array elements scales with frequency as can be seen in Fig 1.4(b).

GaN has found extensive use in power applications starting at kHz all the way up to recently W-band and above. The high electron velocity, high breakdown voltage and good noise performance combined with the thermal properties of SiC makes the GaN HEMT the best power handling transistor available currently. The inherently broadband nature of the HEMT enables very wide-band circuits to be designed and is a good candidate for other active circuits which require large bandwidths such as frequency translation and amplification circuits.

Figure. 1.3 shows an example heterodyne switched front-end composed of fundamental circuits which are the building blocks of any RF system. These sub-circuits are able to be designed and manufactured monolithically on-chip using GaN HEMTs. The smaller guided-wavelength of W-band allows circuits with smaller footprints making it easier to integrate different MMIC circuits on the same chip. This will reduce the need for lossy, reactive and expensive interconnects. This thesis aims to begin at the individual HEMT level and build circuit components using one or multiple HEMTs. These components will then be integrated on-chip into different front-end single-chip die. The single chip front-ends and some other individual MMIC circuits are then fully packaged into split-block wave-guide modules. This is demonstrated through several different measured MMIC designs fabricated in the HRL T3 GaN process, outlined in the next section.

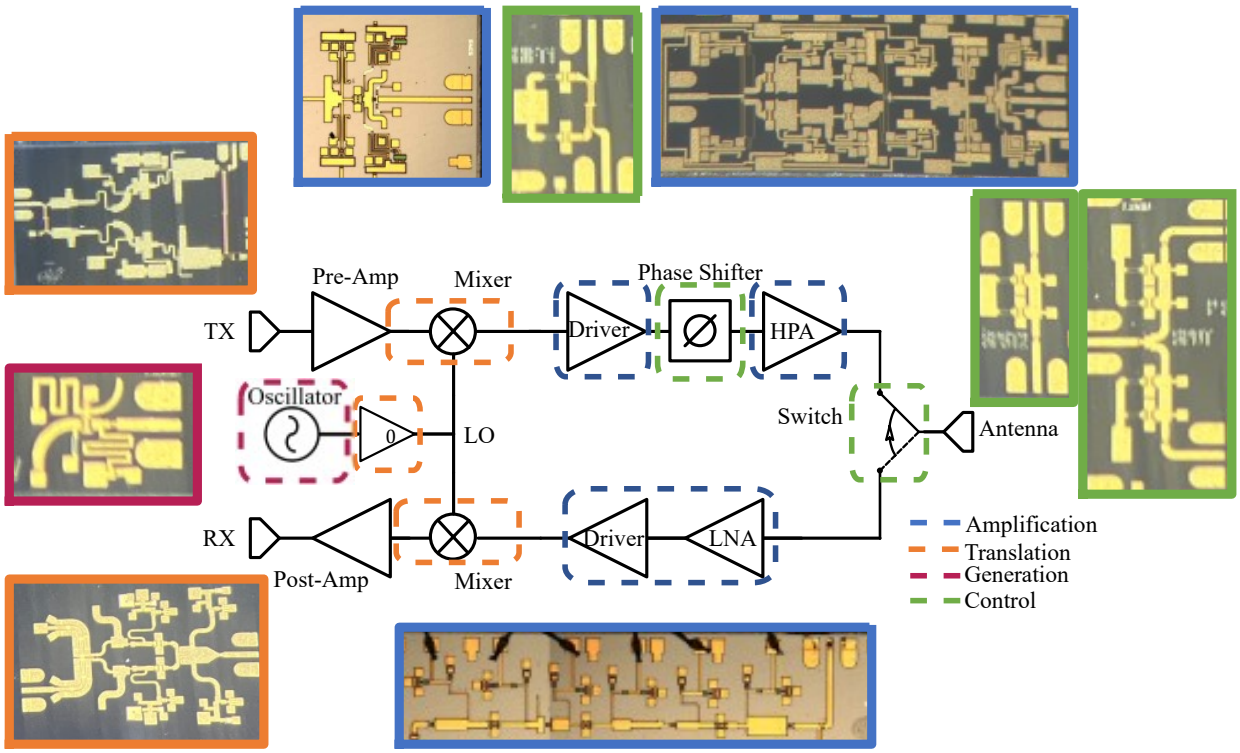
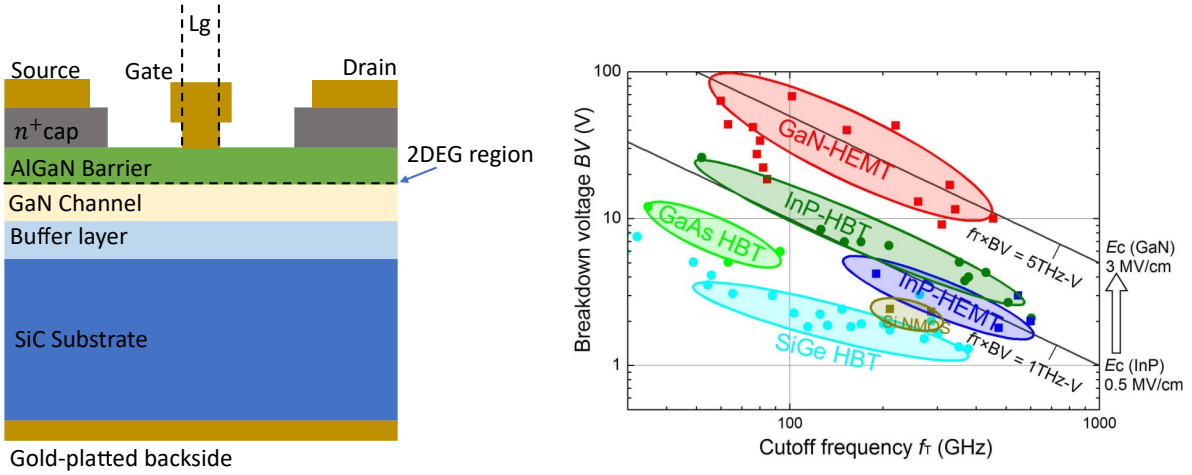


Figure 1.3: Example front end circuit displaying components for amplification, frequency translation, frequency generation and control circuits. Respective GaN MMIC circuits are shown for each of these types of components.

1.4 Millimeter-Wave GaN HEMTs



(a) (b)

Figure 1.4: (a) Typical GaN HEMT stackup (b) Johnson figure of merit shown for GaN, InP, GaAs and SiGe technologies taken from [5].

A HEMT is a transistor in which the channel is formed from the interface of two different semiconductor materials. In the case of GaN HEMTs, the channel or 2DEG region, is formed most commonly using AlGaN and GaN. Shown in Fig. 1.4 (a) is a standard cross-section and of a GaN on SiC HEMT. The one shown is modeled after a 4x37.5μm device in the HRL T3 process which has backside metalization. Not all millimeter-wave processes include backside metal as CPW can be accomplished with only topside metalization which simplifies the fabrication process. Most of the wafer thickness comes from the SiC substrate with the actual channel being very thin itself. Note that the layers are not drawn to scale, they are only a representation of the stackup of the MMIC process.

Johnson figure of merit (JFoM), defined as the product of f_T and BV, with various high-speed device technologies shown in Fig. 1.4(b). What this data indicates is that GaN will outperform any other semiconductor technology in power density and power handling at millimeter waves. A number of recent millimeter-wave GaN processes with gate lengths in the 20–90 nm range have shown high performance across V- and W-bands [38–41]. A considerable number of experimental and commercial GaN millimeter-wave foundries exist and are summarized in Table. 1.2. Note that the number of these foundries is growing as the technology matures.

1.4.1 GaN HEMT Scaling to Millimeter Waves and Beyond

The limitations of HEMT performance at scaled frequency arises from the extremely small mechanical dimensions of the device. The smaller the dimensions, the smaller the maximum voltage the HEMT can handle. Breakdown voltage is critical in power density and power handling. Properly scaling the devices can scale the f_T or the transition frequency (the frequency at which the gain of the device reaches 0) and the f_{max} (maximum oscillation frequency) into the high millimeter wave bands. Important device parameters to consider when scaling are the capacitance between the HEMT terminals (gate, source and drain) and the resistances of the gate and drain: C_{gd},C_{gs},C_{ds}, R_g, R_d. Scaling down the dimensions of a HEMT will severely change these parameters and as a result have a significant impact on the performance.

The gate seen in the stackup, Fig. 1.4 (a), appears to be in the center of the device as would be normal for a switch HEMT. In reality for the HRL process and others focused on use of the HEMTs for amplification, the

Table 1.2: mmWave GaN MMIC Processes

Foundry/ Process	Tech	GL* (nm)	ST$^{\delta}$ (um)	f_T/f_{max}	BV^{+}	PD$^{\triangle}$	ref
QORVO GaN09	GaN on SiC	90	100	$^{145}/_{n/a}$ GHz			[42]
OHMMIC D01GH	GaN on Si	100	100	$^{105}/_{n/a}$ GHz	36 V		[43]
OHMMIC D006IH	GaN on Si	60	100	$^{130}/_{n/a}$ GHz	36 V		[44]
Fujitsu	GaN on SiC	80		$^{150}/_{190}$ GHz			[45]
IAF GaN15	GaN on SiC	150		$^{50}/_{160}$ GHz			[46]
IAF GaN10-20	GaN on SiC	100					[47]
IAF GaN10-20 70nm	GaN on SiC	70					[48]
HRL T2	GaN on SiC	140	50	$^{90}/_{220}$ GHz	40 V		[5]
HRL T3	GaN on SiC	40	50	$^{200}/_{400}$ GHz	40 V		[5]
HRL T4	GaN on SiC	20	50	$^{331}/_{517}$ GHz			[5]
BAE Systems	GaN on SiC	140	55	$^{70}/_{155}$ GHz	80 V		[49]
BAE Systems	GaN on SiC	140	55	$^{70}/_{155}$ GHz	80 V		[49]
Mitsubishi	GaN on SiC	150	50				[50]
Raytheon	GaN on SiC	150	50				[51]
WIN NP15	GaN on SiC	150	100	$^{32}/_{187}$ GHz			[52]
WIN NP12	GaN on SiC	120	50	$^{34}/_{212}$ GHz			[52]
NGC 0.2um	GaN on SiC	200	100	$^{60}/_{200}$ GHz			[53]
NGC 90nm	GaN on SiC	90	50	$^{100}/_{250}$ GHz			[53]
Intel	GaN on Si	30	n/a	$^{300}/_{400}$ GHz			[54]
Intel	GaN on Si	30	n/a	$^{130}/_{680}$ GHz			[55]

* Gate Length, + Breakdown Voltage, δ Substrate Thickness, $\triangle$ Power Density

gate is placed closer to the source terminal than the drain terminal. A longer distance between the gate and the drain allows for a higher breakdown voltage (V_{BR}) which impacts the ON-resistance (R_{ON}) and improves the transconductance (g_m). A shorter distance between the gate and source increases C_{gs} and at the same time reduces the source resistance (R_s). Spacing the gate closer to the source does not have a significant impact on f_T [56]. Gate to drain capacitance is responsible for feedback occurring in the source-grounded operation of the HEMT which negatively impacts linearity, a vital parameter for modern communication and defense systems.

Scaling the gate lengths too aggressively can cause short channel effects [57]. This effect is caused when

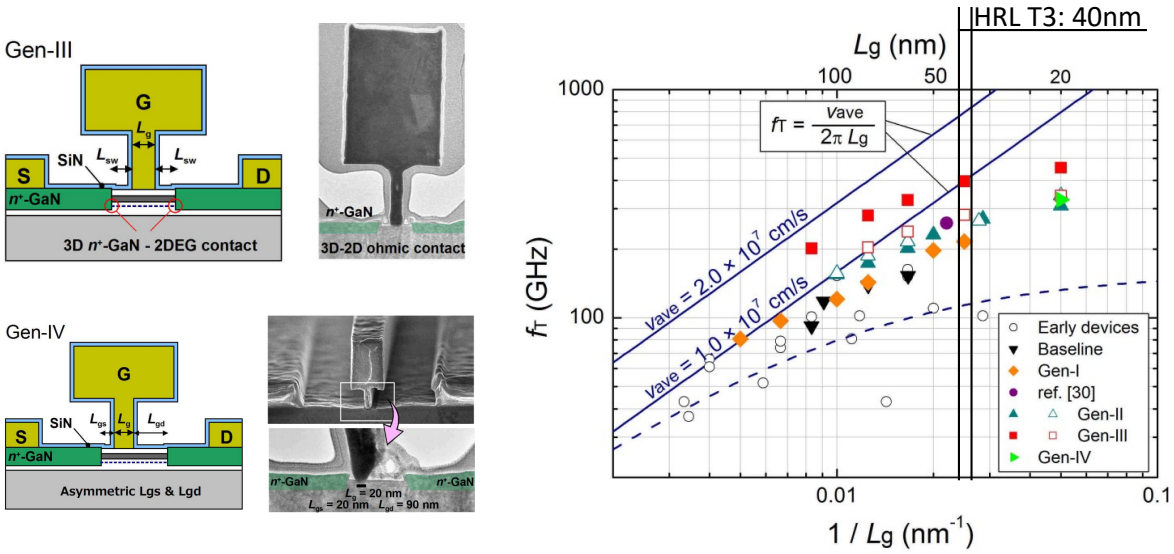


Figure 1.5: T3 GaN HEMT crosssection with a real SEM photograph of a T-gate. The plot shows how the cutoff frequency is limited by the gate length and the scaling limitations. All images are taken from [5].

the gate length (Lg) has been scaled down to a small enough dimension compared to the distance from the gate to the channel. This implies scaling the gate length (Lg) cannot be done without proportionately scaling the layers between the gate and the channel (epitaxial layers). In a solid state context, scaling these layers down to nm range lowers the amount of available states that are available for use in the layers. As a result, important HEMT parameters such as transconductance and intrinsic capacitances do not scale proportionally in this region. This can be seen in the plot in Fig. 1.5.

Proportional scaling of intrinsic and parasitic delay components in GaN HEMTs at HRL significantly enhances both fT and fmax up to 450 and 600 GHz range, respectively [5]. In order to address the aforementioned limitations arising from highly scaled HEMT devices, HRL has developed a four generation scaling approach. The steps of the different generations are summarized in detail in [5]. The HRL GaN process development is able to circumvent these scaling issues with selection of proper materials, material densities, use of a T gate as well as a generational approach to introducing scaled technology to millimeter wave GaN process.

1.4.2 The HRL T3 Process

The scaling of GaN HEMTs has been discussed. It is one component of a GaN process to scale up, it is another to repeatedly fabricate these devices and have them reliably operate in a variety of conditions in the field including space (radiation testing). The HRL T3 process is a recent process compared to other semiconductor technologies with gate lenghts less than 70nm such as GaAs. Available in the process are three metal layers allowing for air bridges, vias, backside metalization, SiN capacitors, TaN and Epi layers available for different sheet resistances and power handling. This 40nm GaN of Silicon Carbide (SiC) process comes with 4 validated scalable models from the foundry. These include validated linear and non-linear models as well as a NF model.

1.5 Thesis Organization

This thesis is organized in the following way. The HRL T3 GaN HEMTs are utilized in different active and passive MMIC circuits which are expanded upon in chapters 2-4. Chapter 2 describes amplification are millimeter waves for both reception and transmission of signals. The transmission section focuses on power amplifiers and large-signal operation of HEMTs, while the reception section focuses on LNAs and small-signal operation. Next, the HEMTs are demonstrated in control circuits in Chapter 3, specifically phase shifters and switches. Chapter 4 outlines frequency multiplier circuit theory while Chapter 5 showcases several W-band MMIC doublers and triplers, including design and measurements. All of the aforementioned HEMT circuits are then integrated into a front end on a single chip, described in Chapter 6. Chapter 7 concludes with highlighted contributions of this thesis, and discusses avenues for future work, including other millimeter-wave GaN MMIC designs as well as packaging of chips in waveguides at millimeter waves.

Chapter 2

W-band GaN MMIC Amplifiers

Contents

In this chapter, GaN HEMTs both for power amplification in transmission and low noise amplification in reception at millimeter waves are described. For large signal operation, the HEMTs are matched using load- and source-pull methods. This is demonstrated on two multi-stage power-combined power amplifiers each using different levels of power-combining to achieve 24 dB of output power over W-band. Low noise amplification is accomplished through small-signal and noise design. A three stage LNA is presented with a de-embeded measured NF of 4–6.6 dB and a small signal gain of 15–22 dB over 75–110 GHz. Measurement methodology and further results are also discussed in this chapter.

2.1 W-band GaN Power Amplifier Design

Reviewing existing designs in the same technology and especially in the same process is a good start in assessing realistic design parameters. Published broadband W-band GaN PAs with various gate lengths, shown

in Fig 2.1(a-c), indicate that an output power of >25 dB over 75-110 GHz is achievable. The performance of these PAs is summarized in Table 2.2 and narrowband GaN W-band PAs are also reviewed in Table 2.1. The goal of the power amplifiers designed in this chapter is to obtain broadband performance while maintaining power density and obtaining sufficient gain up to 110 GHz.

In [58], two three stage unit power amplifiers are combined with a Wilkinson and two of these Wilkinson combined amplifiers are used in a balance configuration with lange couplers. This work was demonstrated on 100nm GaN on SiC and saturated power measurements were done with a waveguide packaged chip and input power of 29 dBm showing a peak saturated power of 37.8 dBm and operates over a narrow 90-97 GHz (7.5% fractional bandwidth). Most of the narrow band PAs have over 1 W of output power, but due to the gain-bandwidth trade-off, the broadband MMIC amplifiers manage to output 1 W over the entire band only with considerable power combining. This can be seen in [36] and [59] where 5 units amps are serially combined using Lange couplers with uneven coupling ratios. Figure 2.1 shows this PA along with several other published W-band broadband PAs along with their respective footprint.

The HRL 40 nm GaN HEMTs are shown to have 3-5 dB of gain under compression implying multiple stages and power-combining will need to be utilized to reach a reasonable amount of saturated gain and output power over a wide bandwidth. For this reason, a three-stage approach with two 4x37.5μm HEMTs reactivily combined on the last stage is chosen. A 4x25um device driving and matched to a 4x37.5μm device form the first two stages and with the power-combined output stage give the amplifier a 1:2:3 staging ratio. This linear increase in periphery over the stages of the PA enable each stage to properly saturate the next and efficiently drive the stage were most of the amplification occurs, the output stage.

2.1.1 Device Characterization for Large-Signal

Biasing of the HEMTs in the amplifier is determined prior to load-pull. For the purposes of this section, only the 4x37.5μm device is considered. Note that the characterization of any other device size is conducted with exactly the same methodology. For the 4x37.5μm HEMT, a gate bias of 0.25 V at a drain potential of 12 V has a corresponding drain current of 200mA/mm. This bias point operates the HEMTs in a class AB amplifier and was selected for maximizing efficiency and output power.

Table 2.1: Comparison of Narrow-band *V*- and *W*-band GaN HEMT Amplifiers

Freq (GHz)	Frac. BW (%)	P_{out} (dBm)	PAE (%)	Gain (dB)	Year Ref.
71-76	6.8%	34.9	27.8%	15.2	2012 [60]
71-86	19.1%	31.4	9.9%	25.8	2018 [61]
84-95	12.3%	29.2	14.7%	19.6	2010 [62]
90-92	2.2%	32.3	11%	15	2011 [63]
77.8-89	13.4%	31	12.3%	17	2016 [64]
86–94	8.8%	30.6	8%	12	2017 [65]
88-93	5.5%	34	14%	15	2017 [66]
90-97	7.5%	37.8	18.3%	15	2020 [58]

Table 2.2: Comparison of Broad-band *V*- and *W*-band GaN HEMT Amplifiers

Freq (GHz)	Frac. BW (%)	P_{out} (dBm)	PAE (%)	Gain (dB)	Year Ref.
6-52	158.6%	28	20%	8-12	2020 [67]
70-105	40%	24.5	6%	16	2012 [68]
80-100	22.2%	35	-	8	2013 [59]
75-100	28.6%	33	-	15	2016 [36]
70-110	44.4%	28.6	6.5%	12	2018 [7]
71-110	43.3%	24.2	6.5%	10	2021 [8]
75-110	**37.8%**	**20**	**8 %**	**11**	**[9]***
75-110	**37.8%**	**25**	**9.6 %**	**15**	**[9]$^{+}$**
75-110	**37.8%**	**27**	**3 %**	**23**	**This work‘**

* Unit-B Amplifier - @ P_{IN} = 9 dBm and 86 GHz
+ Balanced - @ P_{IN} = 10 dBm and 76 GHz
‘ Driver + Serial - @ P_{IN} = 4 dBm and 90 GHz

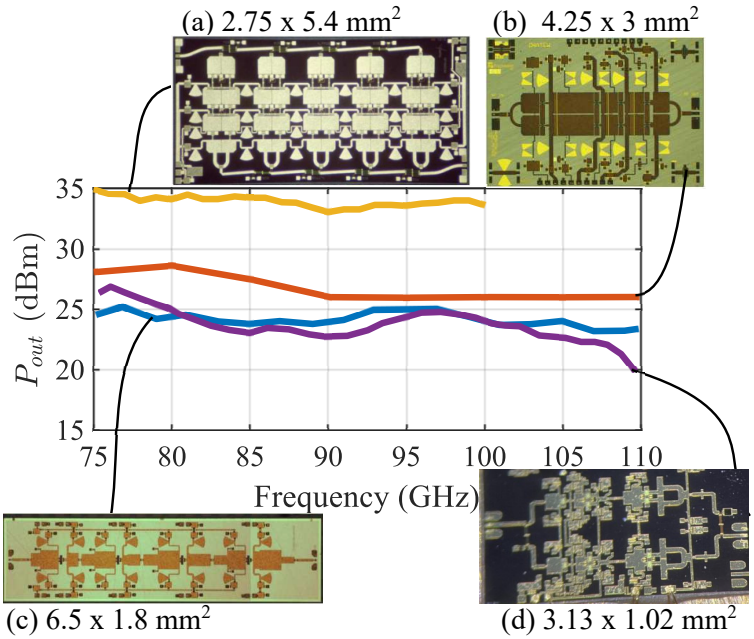


Figure 2.1: State-of-the-art published broadband W-band power amplifiers output power over frequency showing: (a) five serially combined 3-stage unit PAs made in 150 nm GaN on 50 μm SiC [6]; (b) 4-stage power combined 100 nm GaN on 75 μm SiC [7]; (c) 4-stage 100 nm GaN PA [8]; and (d) 3-stage balanced 40 nm GaN on 50 μm SiC PA [9].

Source- and load-pull techniques are used to determine the ideal input and output impedances respectively. These simulations are conducted at the chosen bias and at a single frequency at a time. First, a S_{11} simulation is done to find an initial input match to conduct the first iteration of load-pull. Using this initial match, load-pull is performed on the foundry device model. This results in an output reflection coefficient for a desire metric (PAE, output power). Adding this Γ value to a load tuner on the loadpull simulation allows source-pull to be conducted again for a more refined result. Source- and load-pulled values are then repeatedly updated from previous simulations in the source and load tuners at the gate and drain of the HEMT model. Due to the bilateral nature of HEMTs, this process is conducted several times until simulation results change less than a low percentage between iterations.

Results of this procedure on a 4x37.5μm HEMT model at 92.5 GHz is shown in Fig 2.4. The optimal input power for maximum PAE is 18 dBm and is used for source- and load-pull simulations. At this drive, a maximum of 28 % PAE is possible with 23.5 dB of output power. These maximum points do not coincide on the same spot on the Smith chart implying that a tradeoff between the two will be necessary. Note these

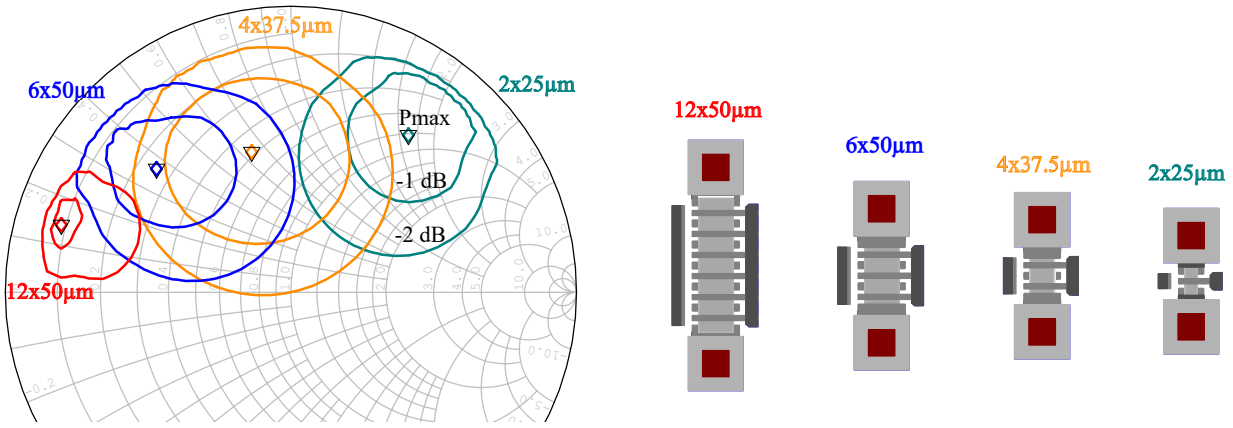


Figure 2.2: Loadpull maximum point and associated contours of the nonlinear device model provided by the foundry (HRL) for the four different validated foundry sizes. The plot displays how the large signal drain impedance moves closer to a short on the smith chart when the device size and total periphery increase.

results are only at a single-frequency, conducting the same procedure at the edge of W-band ,110 GHz, gives a maximum PAE of only 19 %.

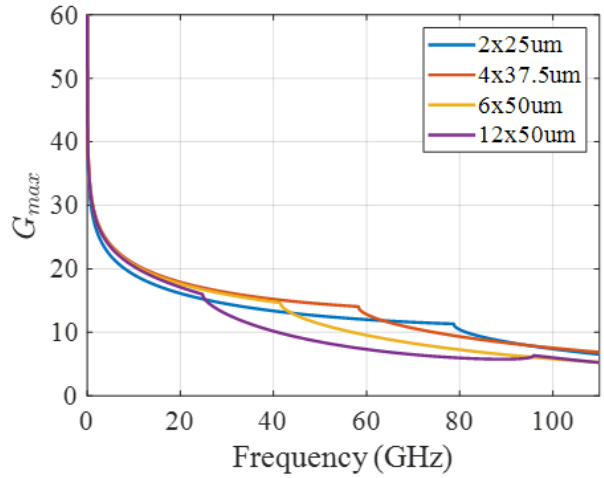


Figure 2.3: Gmax of of all four validated foundry device models shown over frequency from 0-110 GHz.

2.1.2 Broadband Millimeter-Wave Matching Networks

Using the results from source- and load-pull simulations, the matching networks are designed next. This is done by turning the optimal input and output reflection coefficients into equivalent circuits modeling the gate

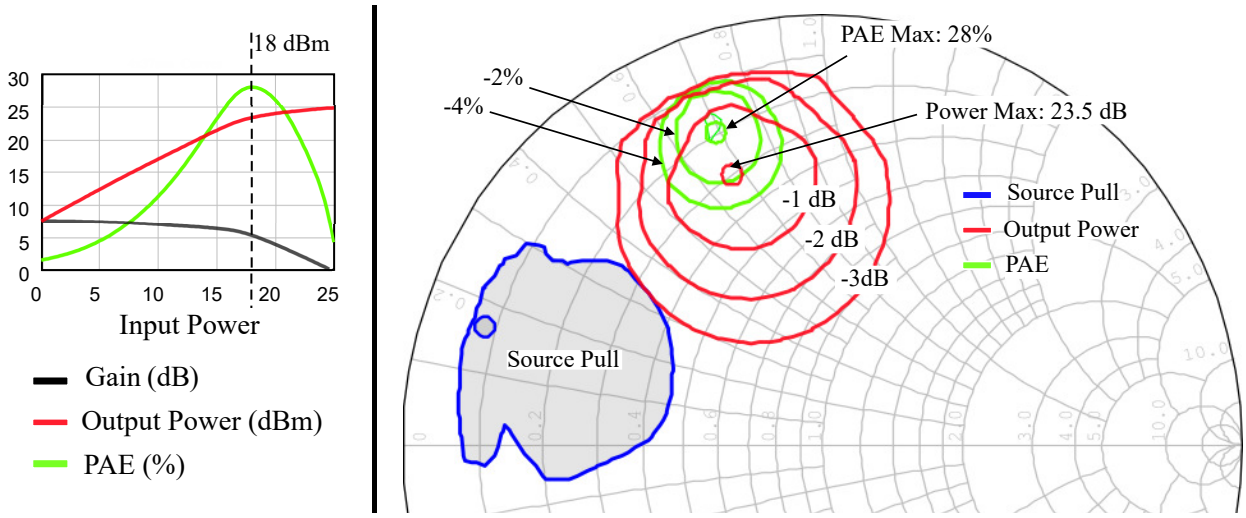


Figure 2.4: Gain, PAE and output power at 92.5 GHz of a 4x37.5um HEMT biased at 0.25 V on the gate and 12 V on the drain with a resulting quiescent current of 200 mA/mm. Load-pull PAE and Output power maximums and contours of the 4x37.5um HEMT at an input drive of 18 dBm.

and drain of the HEMT. The equivalent resistances R_{eq} and capacitances C_{eq}, shown in Fig. 2.5, are found using the following relations. First the source-pulled Γ_{source} is transformed into Z_{source} assuming a 50Ω characteristic impedance. The following equations show how to turn Z_{source} into a series RC network.

$$Y_s = \frac{1}{Im(Z_{source})}, \quad R_{gate} = Re(Z_{source}), \quad C_{gate} = \frac{Y_{source}}{\omega}$$

The drain impedance for optimal PAE found from loadpull Z_{PAE} is then converted into a parallel RC network.

$$Y_{PAE} = \frac{1}{Z_{PAE}}, \quad R_{drain} = \frac{1}{Re(Y_{PAE})}, \quad C_{drain} = \frac{Im(Y_{PAE})}{\omega}$$

With $\omega = \pi f$ this calculation yields a single frequency result. These equivalent circuits form the basis for which the matching networks may be designed as they provide a simple linear model which results in quick simulations [69]. (Add bilarity)

A broadband reactive match is used for all stages to minimize the footprint and reach the desired specifications. The most critical match in the design is the power-combined output match of the last stage. The last stage is compressed for optimal desired performance (PAE, output power). The prior stages may not be operating at the same optimal compression and can lower the overall performance of the PA. The

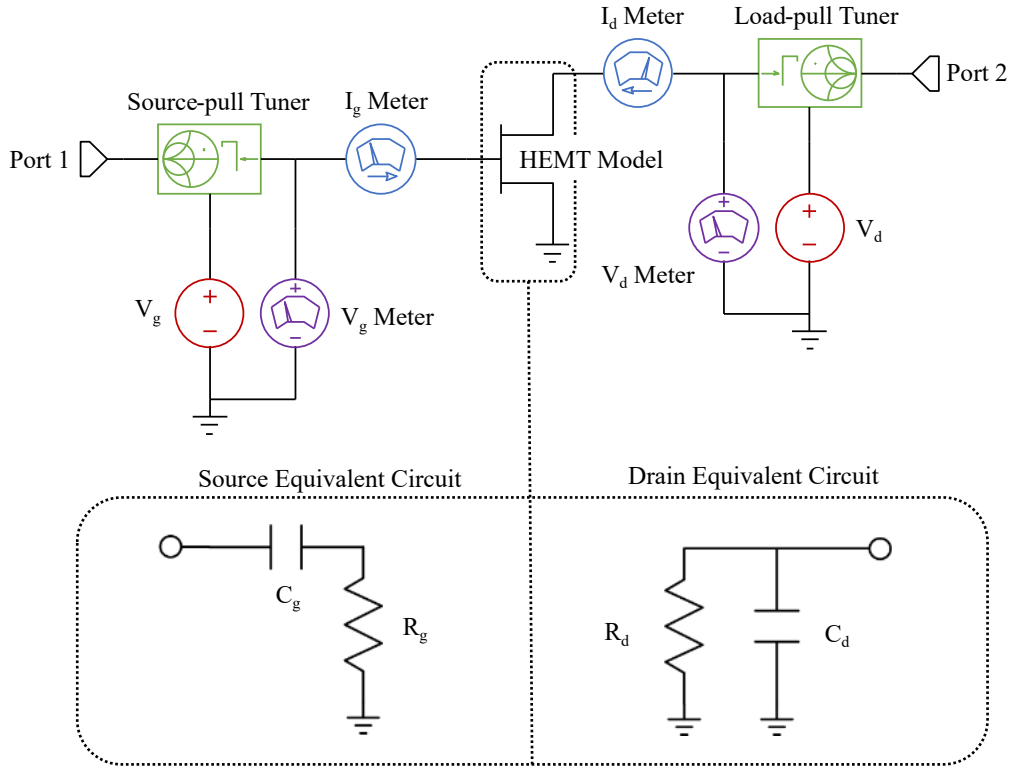


Figure 2.5: Load- and source- pull simulation setup used with the foundry HEMT model (top). Equivalent circuit of the gate and drain right as a result of loadpull results (bottom). Devices are biased at V_{DD}=12 V and $V_{GG} = -0.25$ V.

maximum amount of outpower power produced always falls right at the drain of the output stage HEMTs. After this, no more amplification will occur and so to maximize output power and efficiency it is important to minimize the loss of the output matching network while still maintaining the desired bandwidth.

Microstrip lines are extensively used for matching networks at W-band frequencies. When using microstrip, it is important not to excite unwanted modes in the conductor. If a microstrip lines gets too wide, the currents will begin to flow to the edges of the line and not propagate through the line in the desired manner. A line may also only get as thick as the process allows which changes depending on what metal layer you are designing in. These two factors form the limitations of the usable impedance of the line. For the T3 process, this limitation lies between [23-67] Ω.

2.1.3 Balanced Three-Stage Power Amplifier

To maximize output power and gain, two unit PAs can be power-combined using a balanced amplifier topology. The balanced topology is resilient to changes in input and output load impedance from the 90 degree hybrid coupler employed.

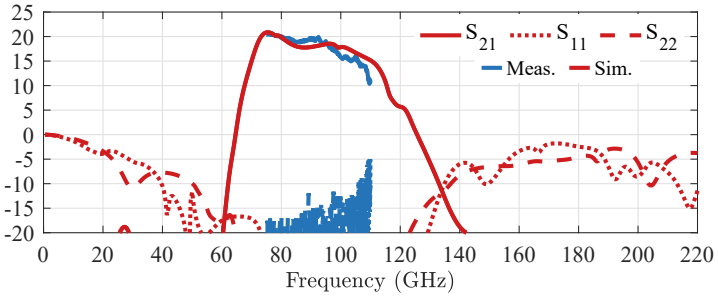


Figure 2.6: Measured and simulated $|S|$-parameters of the balanced power amplifier shown from 0 to 220 GHz. Measurements were conducted across W-band using an HP8510C VNA and W-band frequency extender heads.

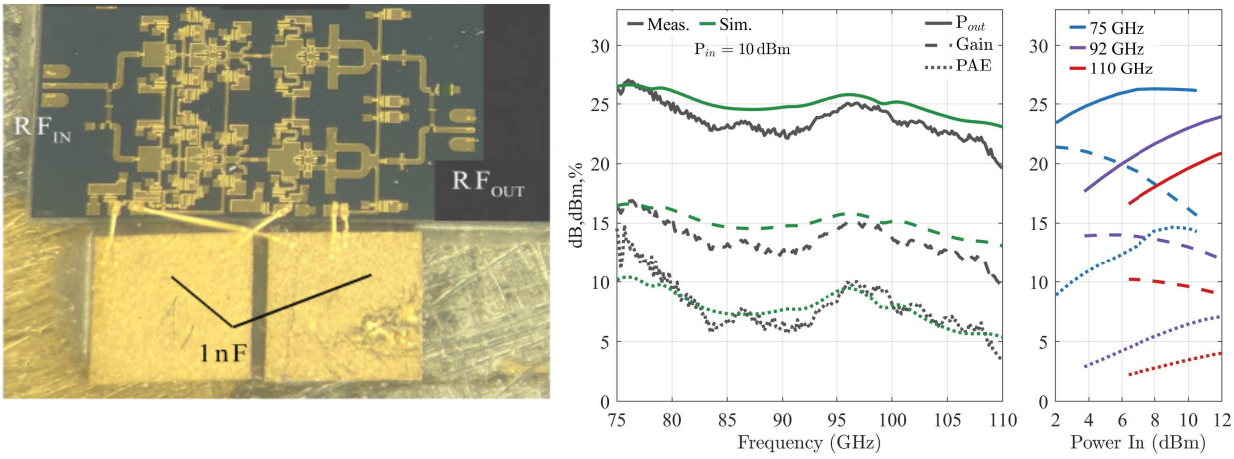


Figure 2.7: Photograph of balanced three-stage PA shown with off-chip MIM and the bond-wire connections (left) and Measured results of the output power, gain and PAE compared to simulations over frequency (middle). Output power at 75, 92, 110 GHz plotted over a 2-12 dbM input power (right). *****Add bias

The multi-stage balanced power amplifier is described in detail in [9]. Briefly, two three stage amplifiers with a 1:2:3 staging ratio are power combined using two Lange couplers. To achieve this staging ratio two HEMT devices sizes are used: 4×25 μm and 4×37.5 μm. The third stage combines two 4×37.5 μm HEMTs with a quiescent drain current of 60 mA. The peak output power is measured to be 26.7 dBm at 77 GHz, and

the peak power added efficiency (PAE) around 14.8 % at 95 GHz. (talka bout gain compression and need for driver)

2.1.4 Single-HEMT Driver Amplifier

A single-HEMT power amplifier is designed as a potential on-chip driver for power amplifiers or other active and passive MMIC circuits. The goal for this design is to have broadband operation (over the entire W-band) with flat output power over that frequency range. For this circuit, a 4×37.5 μm HEMT is used as it is a validated foundry size and is a good compromise between gain, PAE and power. The device characterization described above, Fig 2.4, is used for this design as well. Using the same bias point as other active HEMT circuits facilitates integration in future work.

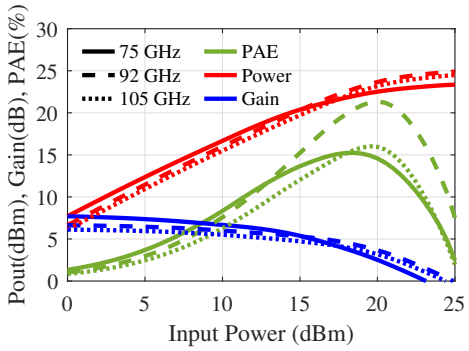


Figure 2.8: Simulated output power, gain and PAE of the single-HEMT driver plotted over an input power of 0–25 dBm for three different frequency points corresponding to the middle and edges of the operating band: 75, 92 and 105 GHz.

Capacitors are prone to process variation and this is especially true at W-band where the necessary capacitors are small and may not be able to be achieved through a MIM capacitor in a MMIC process. For this reason capacitors were only used for DC blocking and biasing. Microstrip transmission lines a well as open and shorted stubs form the basic elements of the matching networks. At the input, a double stub matching network transforms the gate impedance to 50 Ω over the entire W-band. A single stub match with series transmission lines of varying widths match the drain impedance to 50 Ω at the output.

The biasing network of the driver amplifier, Fig. 2.9 is carefully designed to insure stability of the entire trasmit branch of the front-end. Both the drain and gate bias lines are a low-pass coupled line filter topology

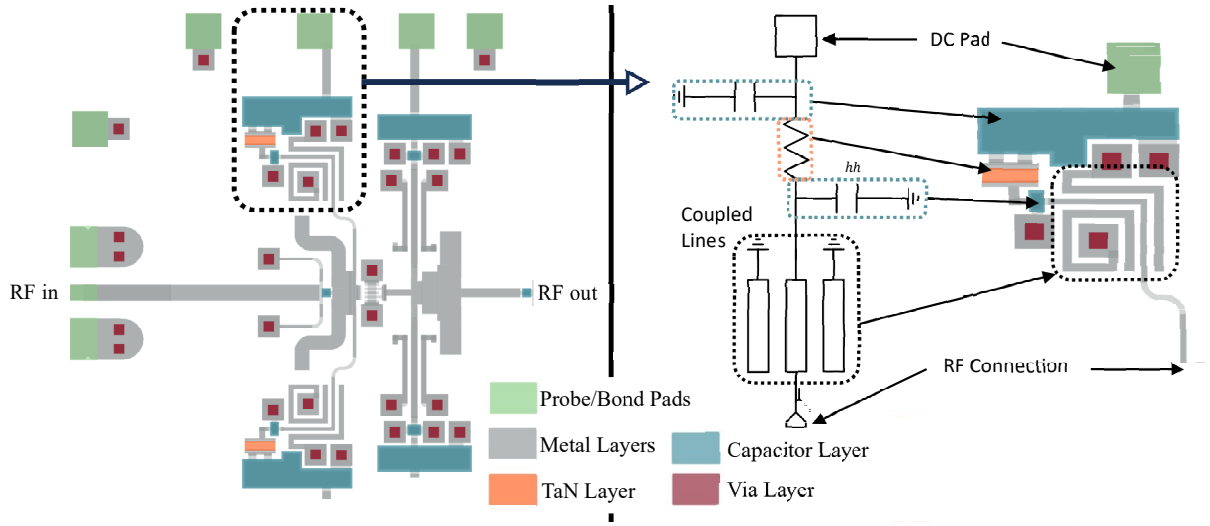


Figure 2.9: MMIC layout of the single-HEMT driver amplifier (left). Schematic and expanded view layout of the gate bias network for the single-HEMT driver amplifier using shunt capacitors, a stability resistor and grounded coupled lines in a low-pass topology. The same topology but without the series resistor is used for the drain bias (right).

with three coupled lines based on [70]. The far ends of the two coupled lines on each side of the signal line are grounded through vias for the low-pass responce. High- and low-frequency bypass capacitors separated by a small stability resistor supress any oscillations. This networks provide below 15 dB of return loss from 65 GHz to above 120 GHz when terminated in 50 Ω. At the input or RF connection to the matching networks, the impedance of the bias line is above 100 Ω over the operational bandwidth of the driver amplifier. Connecting the bias line to a low impedance point on the matching network results in the highest RF-dc isolation [71].

Large-signal simulations of the driver are shown in Fig. 6.4 for a swept input power of 0-25 dBm at three different frequency points corresponding to the edges and middle of the operating band. It can be seen that gain, PAE and output power all drop at the high end of the band at 105 GHz. On-wafer measurements of the single-HEMT driver alone are not conducted as the circuit was with the balanced amplifier and does not have a GSG probe pad on the output.

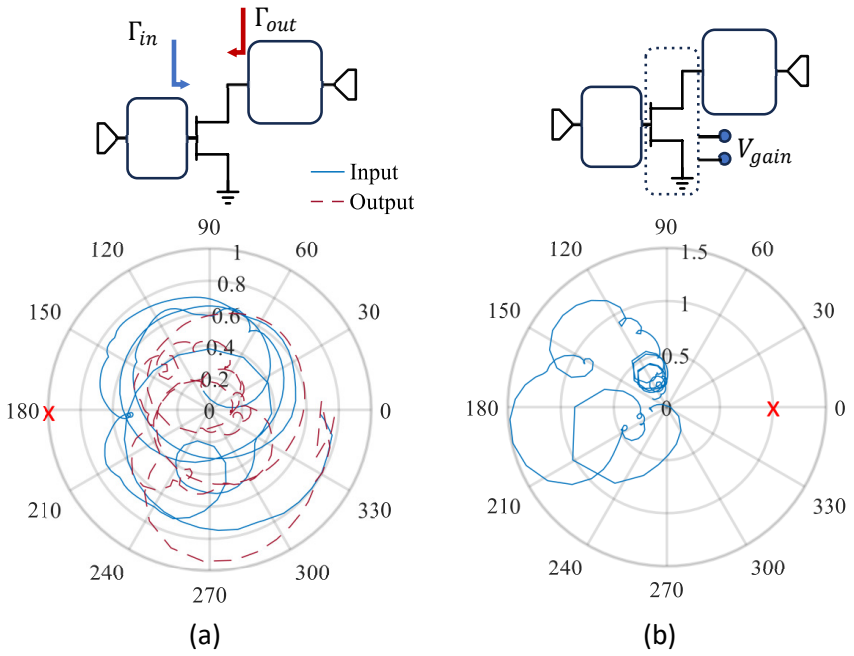


Figure 2.10: Stability analysis of the single-HEMT driver in a 50 Ω environment, not connected to the balanced amplifier, showing (a) Nyquist stability at the plane of the HEMT device in the circuit and (b) loop gain simulation from a linearized angelov model. The red X denotes the point of instability.

2.2 Low Noise GaN MMIC Amplifier

Low noise operation of a HEMT involves biasing and modeling at a certain condition which adds the least amount of noise to the amplified signal. Device characterization must be conducted to determine the optimal performance point for the two main design parameters: noise figure and gain. Since an LNA always operates at small-signal, S-parameter simulations are used to characterize the HEMTs for gain. At the input, optimal noise figure is simulated using the available noise models from the HRL foundry.

Three single-HEMT stages are chosen for the presented LNA with each stage using a $2 \times 50\,\mu$m HEMT as they are the smallest validated device size offered by the process. Shown in fig. 2.11 is the simulated minimum noise figure and maximum gain of the chosen device. Gate bias voltage is swept for two different validated drain voltages of 6 V and 12 V with the respective drain current shown. At a gate bias of 0 V and a drain bias of 6 V it can be seen that there is a dip of 2 dB for the NF and a maximum of 8.5 dB of small signal gain. This bias point corresponds to the chosen quiescent drain current of 12 mA. The biasing of all of the stages of the LNA are kept the same to facilitate external biasing.

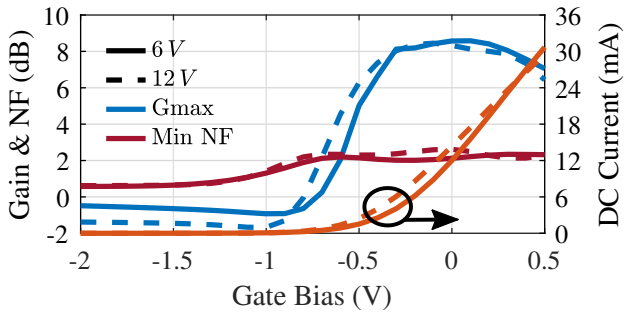


Figure 2.11: Simulated maximum gain and minimum noise figure of the $2 \times 25\ \mu m$ HEMT at 92 GHz plotted over a swept gate bias. Corresponding drain current is shown on the right axis. Simulations are shown for two different validated drain voltages of 6 V and 12 V.

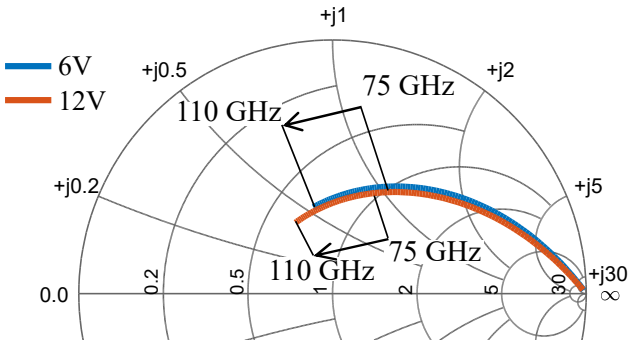


Figure 2.12: Simulated optimal noise input match shown for two different validated drain voltages of 6 V and 12 V plotted over 0-110 GHz. The band of interest to the design is highlighted for each case.

With the chosen bias of the devices, simulations determine the optimal noise and gain match at the input and output of the device respectively. Shown in Fig. 2.12 is the simulated optimal noise input match from 0–110 GHz. This was used to match the input of the first stage for best noise performance while the two later stages are matched primarily for gain as well as noise figure. The input and output of the LNA is designed to be matched to 50 Ω. Simulations of the LNA with and without the switch connected to the input are shown in fig. 6.5.

2.2.0A Noise Measurements and Results

On-wafer 50 Ω noise figure (NF) measurements were collected on the LNA using a custom scalar NF test bench. The MMICs are probed on an MPI TS200 probe station with GGB WR-10 100 μm pitch probes. A QuinStar WR-10 noise diode is connected to the input RF probe through a 90° WR-10 bend, and the output RF

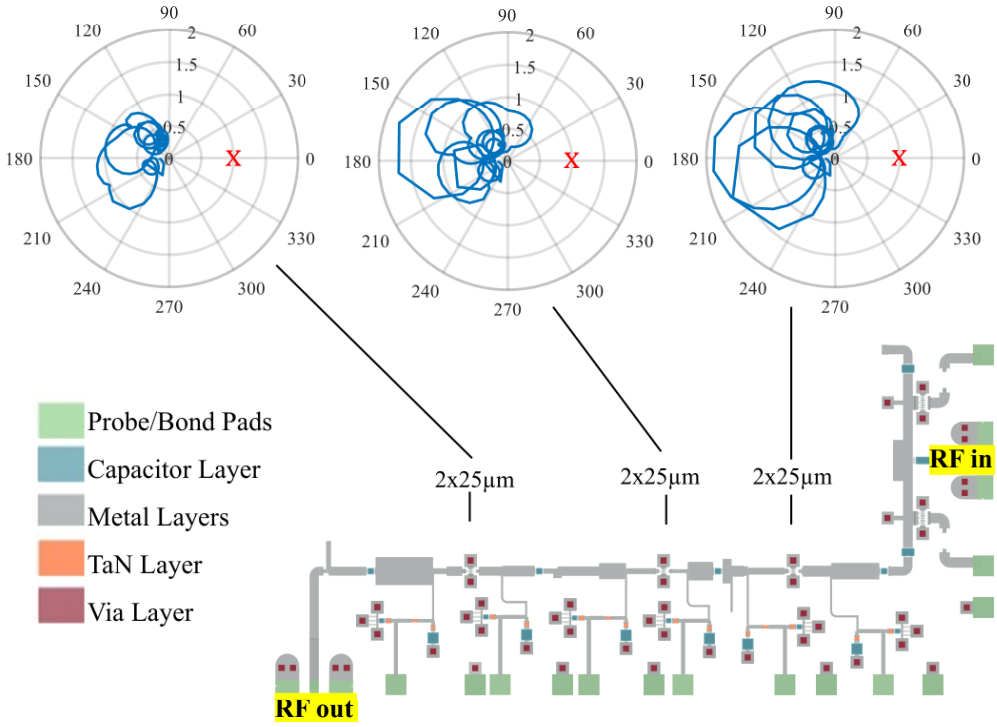


Figure 2.13: Loop gain stability analysis shown for each of the three LNA stages with a layout of the LNA connected to the SPDT HEMT switch. The traces shown indicate the worst-case input and output impedances. The red X denotes the point of instability.

probe is connected to a noise receive chain through a WR-10 S-bend. The noise receive chain is comprised of a commercial LNA, a mixer down converter, a local oscillator (LO) up-converter with a commercial 6× frequency multiplier, and an Agilent E4448A spectrum analyzer with noise figure measurement application. The LO is driven by a Keysight MXG N5183B signal generator. The NF measurements are calibrated to the WR-10 noise diode / WR-10 receive chain reference planes by directly connecting the components and calibrating with the proper noise diode excess noise ratio. Then, the cascaded NF measurement of the input fixture, LNA, and output fixture are measured. Finally, the NF of the LNA is determined by Friis formula with the transducer gain and NF of the fixtures calculated from their respective S-parameter measurements, while the transducer gain of the LNA is calculated from a calibrated S-parameter measurement. The S-parameters of the WR-10 probes are determined with a two-tier calibration. This approach neglects the impedance mismatches between the different reference planes in the cascaded DUT, which is a reasonable approximation for a matched MMIC. A photo of the on-wafer NF measurement test bench is reported in

Fig. 6.9.

Due to the setup mentioned above, only measurements at 80, 85, 90, 95, 100 and 105 GHz are conducted. The measured NF is higher than predicted by the model, shown in Fig. 6.5. Measured NF of the receive path are shown on Fig. 6.10 along with de-embedded NF of the LNA alone, based on measured switch loss from [16]. The measurements show a minimum NF of 5.2 dB at 80 GHz and a peak NF of 7.8 dB at 100 GHz. These results are consistent with measured noise parameter data of individual millimeter-wave GaN HEMTs [72].

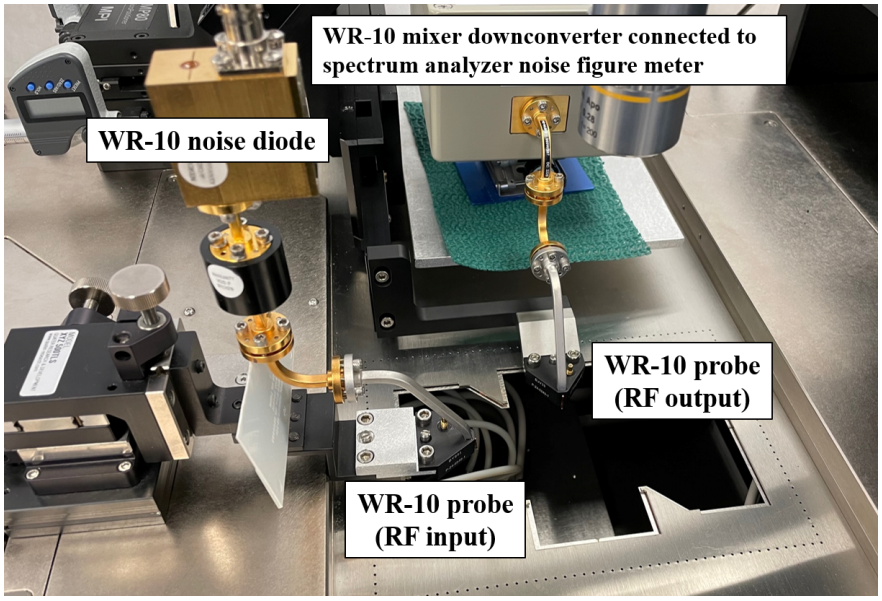


Figure 2.14: On-wafer NF measurement test bench used to characterize the W-band MMIC receive path.

2.3 Chapter Summary

This chapter covered the modeling and design of GaN HEMT power amplifiers and LNAs. For large signal operation, a balanced three stage power-combined power amplifier and single-HEMT driver amplifier are demonstrated. For the balanced power amplifier, the third stage of both unit amplifiers combine two 4×37.5 μm HEMTs with a quiescent drain current of 60 mA. The peak output power is measured to be 26.7 dBm at 77 GHz, and the peak power added efficiency (PAE) around 14.8 % at 95 GHz. A three stage LNA with a measured small-signal gain of 20-25 dB across 70-110 GHz and a minimum NF of 5.2 dB at

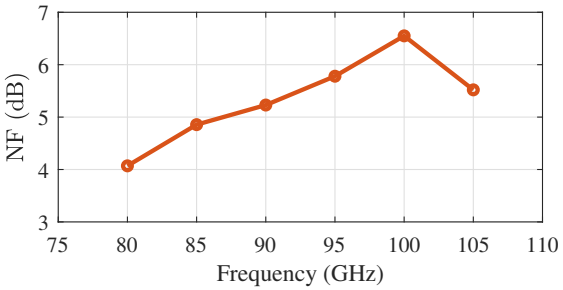


Figure 2.15: De-embedded measured noise figure of the three-stage LNA at a gate bias of 0 V amd a drain bias of 6 V with a total quiescent current of 45 mA using the measured switch results from chapter 3.

80 GHz and a peak NF of 7.8 dB at 100 GHz is also demonstrated. Contributions from this chapter are reported in [73], [74] and [75].

Chapter 3

MMIC Control Circuits at V- and W- Band

Contents

Millimeter-wave MMIC integrated systems require control circuits as essential building blocks. Control circuits are used to control signals in terms of phase, direction and amplitude. These circuits in RF and millimeter wave front ends include switches, phase shifters, attenuators and limitors. This chapter discusses how to use GaN HEMTs to design phase shifters, attenuators and limitors and then will go more in dept into the design and operation of switches at millimeter-waves, covering V- and W- bands.

3.1 Switches

Half-duplex wireless communications, radar, imaging and radiometry rely on switches to route signals through chosen paths. In these on-chip systems, the switch must be low loss, handle high power and have large isolation between ports. At millimeter waves, choice of topology and semiconductor technology is critical to acheiving high performance MMIC switches. Integrated switches have been realized in several

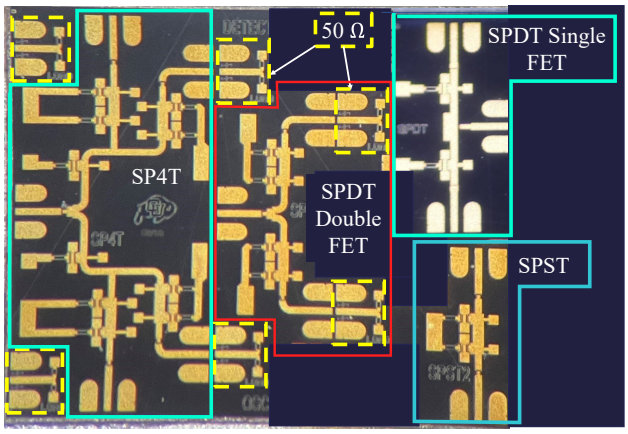


Figure 3.1: Photograph of HEMT switch MMICs in a 40-nm GaN-on-SiC process, showing a SPST, two SPDT and a SP4T switch with a total area of approximately 4 mm × 3 mm.

different semiconductor technologies: CMOS [**?**, 76], SiGe [77, 78], GaAs [79], and graphene [80]. W-band switches implemented in a 180nm CMOS process have a measured 1-dB compression point of 11 dBm [81]. A P_{1dB} = 24 dBm is achieved in SiGe BiCMOS with a PIN diode [82], and P_{1dB} = 22 dBm with SiGe HBT technology in [77]. High 1-dB compression points have been shown up to 300 GHz with P_{1dB} = 14 and 19 dBm for two and one 160-μm periphery transistors in a metamorphic 50 nm GaAs process [83].

When used in a GaN front end, HEMT switches must be able to handle the output power of a high power amplifier as the signal will flow through the switch before arriving to the antenna. Table 3.2 gives a comparison of W-band GaN switches published to date, all using a shunt HEMT topology.

3.1.1 MMIC HEMT Switch Design

This section demonstrates four different switches, shown in Fig. 3.1, that cover 50-110 GHz with high isolation and low insertion loss, showing no signs of compression up to the measured 20 dBm input power. Published GaN HEMT switch results show $P_{1dB} > 24$ dBm demonstrated for a HRL 40-nm GaN SPDT switch [84], and $P_{1dB} > 25$ dBm for an IAF 100-nm GaN HEMT switch with 160 μm periphery [40].

It is possible to connect MMIC switches in several different ways. Transistors can be connected in a series, shunt or a a combination of the two. These transistor configurations can also be cascaded to improve performance. Particularly above 50 GHz, series transistors are avoided as they become too lossy due to the capacitive feed in the off-state and the added loss in the on-state of the switch [76]. For this reason, shunt

Table 3.1: Comparison of *V*- and *W*-band GaN Switches

Freq (GHz)	Type	IL (dB)	ISO (dB)	P_{1dB} (dBm)	Year Ref.
66-134$^{\triangle}$	SPDT*	1.2–2.2	16.8–20	>25	2018 [40]
68-134$^{\triangle}$	SPDT*	1.1–2.1	17.6–21.5	>25	2018 [40]
60-110†	SPST	0.9-1.4	>9	>24	2014 [84]
80-100†	SPDT*	1.3–1.7	>9	>24	2014 [84]
55-110†	SPST	**0.9-3.5**	**25-30**	**>20^{+}**	**This Work**
62-110†	SPDT*	**1-2.2**	**15-20**	**>20^{+}**	**This Work**
55-110†	SPDT$^{\blacksquare}$	**1.8-8**	**30-40**	**>20^{+}**	**This Work**

$^{\triangle}$ 100 nm, † 40 nm, * SPDT single-HEMT, $^{\blacksquare}$ SPDT double-HEMT
$^{+}$ Peak large-signal values @ P_{IN} = 20 dBm and 92 GHz

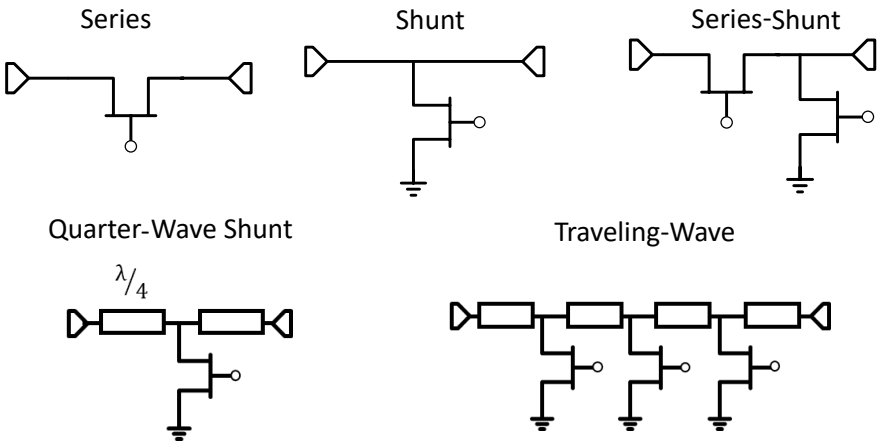


Figure 3.2: Common typologies of HEMT switches showing series, shunt and series-shunt transistor positioning on the top. Further variations of the shunt HEMT position is shown below: travling wave and quarter-wave shunt topology.

transitors are used for MMIC switches at mmWaves. There are two different types of viable shunt-HEMT switch topologies: traveling wave and quater-wave. A traveling wave-topology utilizes the concept of an artificial transmission line to reflect the signal in the off-state and act as a 50 Ω matched transmission line in the on-state. These switches can obtain very wide bandwidths which comes at the cost of more loss compared to the quarter-wave shunt topology.

The chosen topology for the swithces in this work is the quarter-wave shunt topology. A shorted HEMT in the on-state provides a short to the signal which will appear as on open after the quater-wave transmission

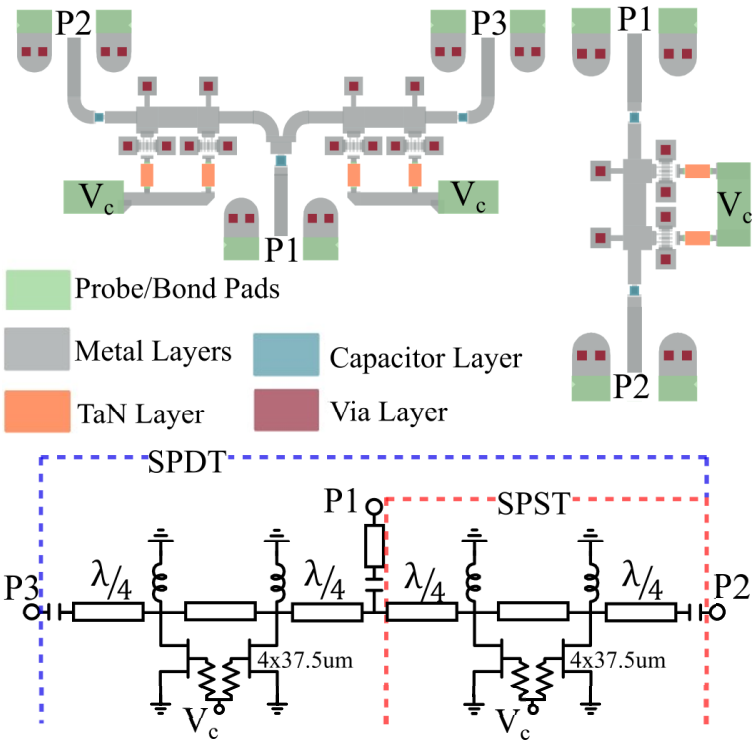


Figure 3.3: Layout (top) and circuit schematic (bottom) of the double-HEMT shunt SPDT switch and the SPST switch.

line. In the off-state, the shorted HEMT is pinched off and acts as a grounded capacitor loading the line. This off-state capacitance is typically resonated out with a shorted inductive stub place directly at the drain. The shorted stub also provides a dc ground at the HEMT drain.

The shorted stub and intrinsic capacitance from the HEMT form a parallel resonant *LC* circuit and with the electrical length of the $\lambda/4$ section results in the main bandwidth limitations [40]. Terminating the quarter wave line with a perfect short is not easily accomplished at millimeter-wave frequencies where ohmic losses and parasitic reactances increase. Using more than one shunt source-grounded HEMT to improve isolation and power handling was demonstrated by InGaAs metamorphic HEMTs, at the cost of insertion loss [79].

Fig. 3.3 shows the circuit diagram and MMIC layout of the double-HEMT SPDT switch from Fig. 3.1, which uses 4×37.5 μm devices in each branch and compensating inductive shorted stubs, which also provides a dc ground to the drains. The switches are operated with a control voltage of -10 V for the ON state and +3 V for the OFF state through a 1.6 kΩ resistor to the gate of the HEMT. In order to be measured on-wafer, the switches are terminated in 100 um GSG pads which were optimized for operation across V- and W- band.

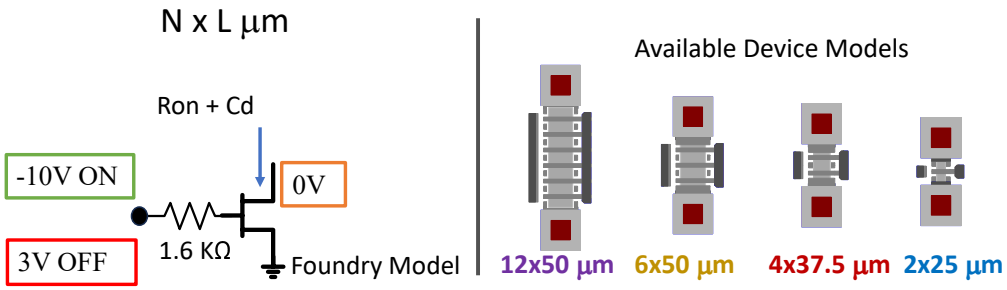


Figure 3.4: Device characterization schematic displaying at what bias and how the R_{on} and C_d parameters are extracted (left). All available validated HEMT models MMIC transistor layout (right).

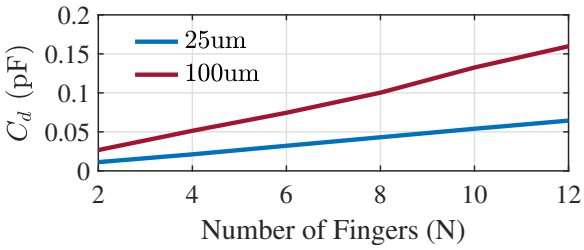
3.1.2 Switch Device Selection

It is well understood that in a millimeter-wave shunt-switch circuit, a HEMT is turn off during the on-state of the switch and therefore is capacitive and loads the through path. Using HEMTs with more fingers and a larger gate periphery results in increased capacitance, but also in increased isolation and power handling. This will result in a higher insertion loss in the on-state compared to smaller peripheries. It is therefore relevant to choose the proper device periphery for the switch with the above tradeoffs in mind.

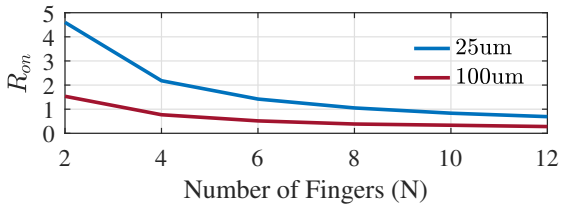
Offered with the HRL T3 process are 4 validated foundry device sizes. Validated models come from direct measurements of that particular size and foundry device sizes between the validated sizes are extrapolations of those measurements. Fig. 3.4 illustrates the available validated foundry models and how the HEMTs are characterized. The characterization of the HEMTs was performed on the devices the same way they would be implemented in a shunt switch which is with a source grounded HEMT with a large resistor (1.6KΩ) at the gate.

The Ron of the considered HEMTs is simulated using the foundry device model at a −10 V bias. The off state capacitance of the HEMTs is simulated when the device is turned off at a gate bias of 3 V. Fig. 3.5 shows a comparison for 2–12 fingers of a 25-μm and a 100-μm wide HEMT, of the extracted parameters. These gate lengths were chosen as they represent the smallest and largest gate length that the HRL T3 process can offer. Plotting these two limits shows the trend for all the gate lengths in the process as they will fall somewhere in between the two.

In the characterization of the HEMTs in Fig. 3.5, two trends can be observed. As the total periphery of



(a)



(b)

Figure 3.5: Simulated (a) Drain capacitance and (b) R_{on} of 40-nm GaN HEMTs as a function of number of gate fingers, for gate widths of 25 μm and 100 μm.

the HEMT increases, the Ron of that device lowers due to the resistance being spread to more parallel finger widths, Fig. 3.5 (b). However, the larger the periphery gets, the larger the drain to source capacitance or off state capacitance of the device increases, Fig. 3.5 (a). Considering this tradeoff, a device size of 4x37.5μm was chosen as a solid compromise between off state capacitance and on state resistance. This device size is also has a validated foundry model and therefore more accurate modeling and simulations than extrapolated sizes is expected.

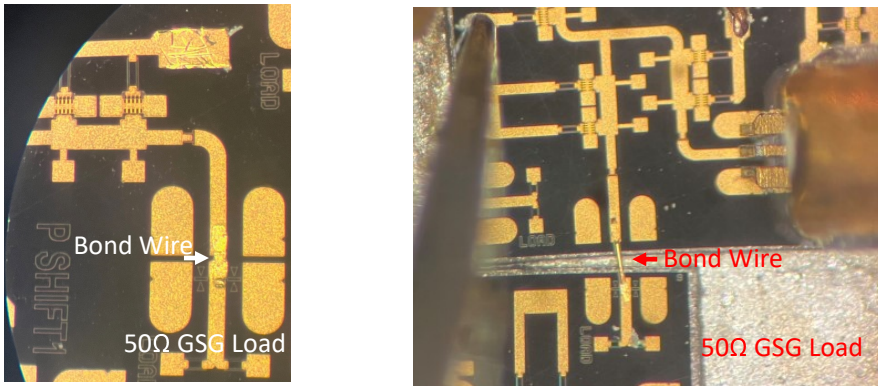


Figure 3.6: MMIC photo of how the SPDT with two shunt HEMTs (left) and the SP4T (right) was terminated during measurements. Labled are the bondwires and GSG temrinations used for this.

3.1.3 Small Signal Measurements and Results

On-wafer small-signal measurements were conducted with an HP8510C VNA with WR-15 and WR-10 frequency extender heads for V- and W-band *S*-parameter characterization, respectively. On-wafer SOLT calibration using 100 μm GSG probes on a W-band impedance standard substrate (ISS) from Cascade Microtech, was done for both bands of interest. The switches which have all adjacent or orthogonal GSG pads are loaded with a 100um GSG probe and V- or W- band termination depending on which measurement is being conducted. The SPDT with two shunt HEMTs and the SP4T have multiple paths in the same direction and therefore a GSG probe cannot be used to load these ports. Instead, a GSG 50Ω on-wafer termination is placed as close as possible to the GSG pad of the switch and a bond-wire is used to electrically connect them, Fig. 3.6.

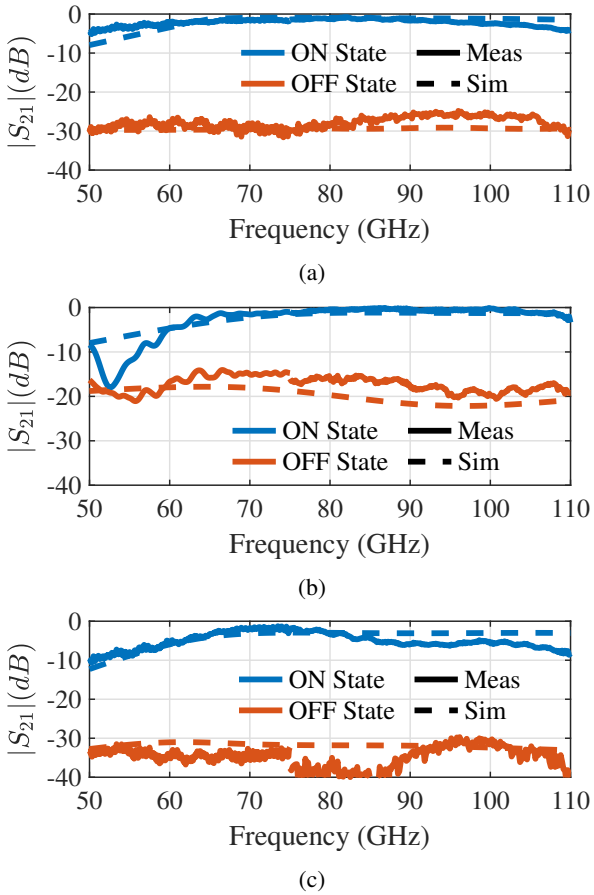


Figure 3.7: Measured and simulated small signal operation of (a) the SPST switch, (b) the SPDT switch with a single shunt HEMT and (c) the SPDT switch with 2 shunt HEMTs.

A summary of measured results from 50 to 110 GHz in small-signal operation and compared with simulated data is shown in Fig. 3.7 for the SPST and SPDT switches. The SPDT switch with a single shunted HEMT in Fig.3.7(b) achieves an isolation of 15–20 dB and an insertion loss of 0.9–3 dB, while that in Fig. 3.7(c) achieves an isolation of 30–40 dB and an insertion loss of 1.2–8 dB. The SP4T switch small-signal measurement results are shown in Fig. 3.8. The SP4T switch can only be measured one path at a time; the path which is at an angle w.r.t. the input port (path A) shows an insertion loss of 3.7–7.5 dB from 50–105 GHz with up to 40 dB of isolation in two symmetrical branches, 3.8(a). The other path (path B) measures an insertion loss of 5.5–10 dB from 68–105 GHz with up to 40 dB of isolation, 3.8(b).

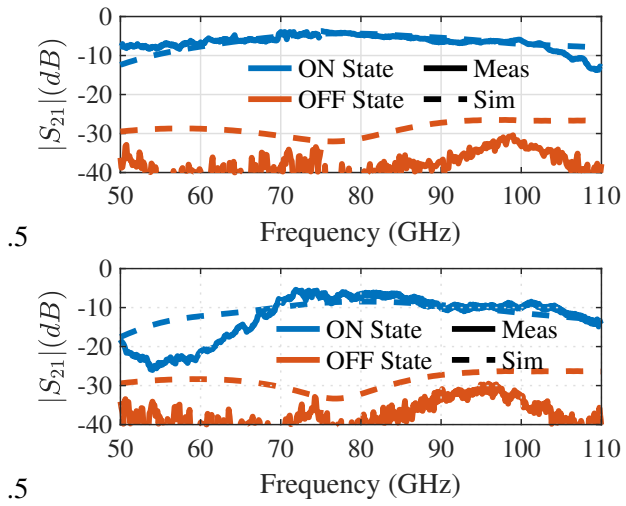


Figure 3.8: Measured and simulated small signal operation of the SP4T switch for (a) path A (b) path B (refer to diagram in Fig. 8).

3.1.4 Large Signal Measurements and Results

Power handling of the switches was measured using a W-band large signal bench consisting of two W-band power amplifiers at the end of the chain to measure up to 20 dBm at the plane of the DUT at 92 GHz. The large-signal measurement setup is shown in Fig. 3.9 and a photo of the real lab test setup is shown in Fig. 3.10. The HP83650A source supplies the starting power to the Ka-band amplifier (QPW-18402020-J0) which drives the passive frequency tripler (QPM-93003W), bringing the CW signal up to W-band. After the tripler, a BPF (QFL-B4SW00) filters out the unwanted harmonics and feeds the CW single-tone signal to the two W-band amplifiers (QPI-W01820-H4W0 and custom W-band HPA). The amplifiers are protected

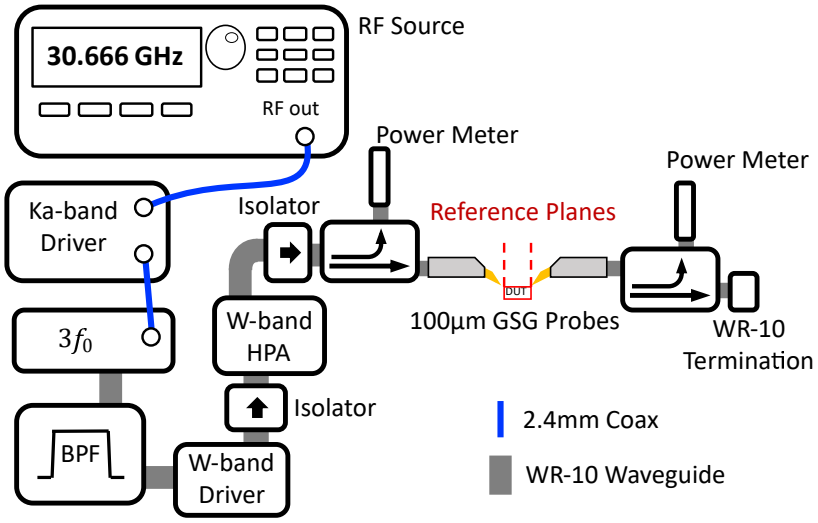


Figure 3.9: Simplified block diagram of the large signal measurement setup for characterizing saturation and power handling of the switches.

with isolators at the output of each and a 20 dB waveguide coupler is used to protect the WR-10 power meter (NRP110TWG). Finally, the CW test signal is brought to the plane of the DUT with several waveguide sections through a 100-μm pitch WR-10 waveguide GSG probe.

At the output, the measured signal is coupled off to another WR-10 power meter through a 10 dB coupler, which is terminated in a WR-10 load. Losses of the passive couplers, isolators, waveguide straight and bend pieces, and probes are measured using the HP8510C VNA and used to de-embed the measurement plane from a calibrated power meter to the GSG probe tips or DUT plane. Power sweeps from 0 to 20 dBm at the DUT were done for each presented HEMT switch at 92 GHz.

The output power of each of these measurements for the SPST and SPDT switches is shown in Fig. 3.11 along with EM-simulated MMIC nonlinear model data. For the SP4T switch, two measurements, one for each of the symmetrical branches, are shown in Fig. 3.12. Nonlinear simulations agree with measurements within the available testing power range, and indicate a 1-dB compression point above 40 dBm for the SPST.

3.2 Phase Shifters

Critical in phased array systems is the control of the phase in each individual element of the array. MMIC phase shifters on MMIC can be realized in several ways shown in Fig 3.13. Discrete phase shifters switch

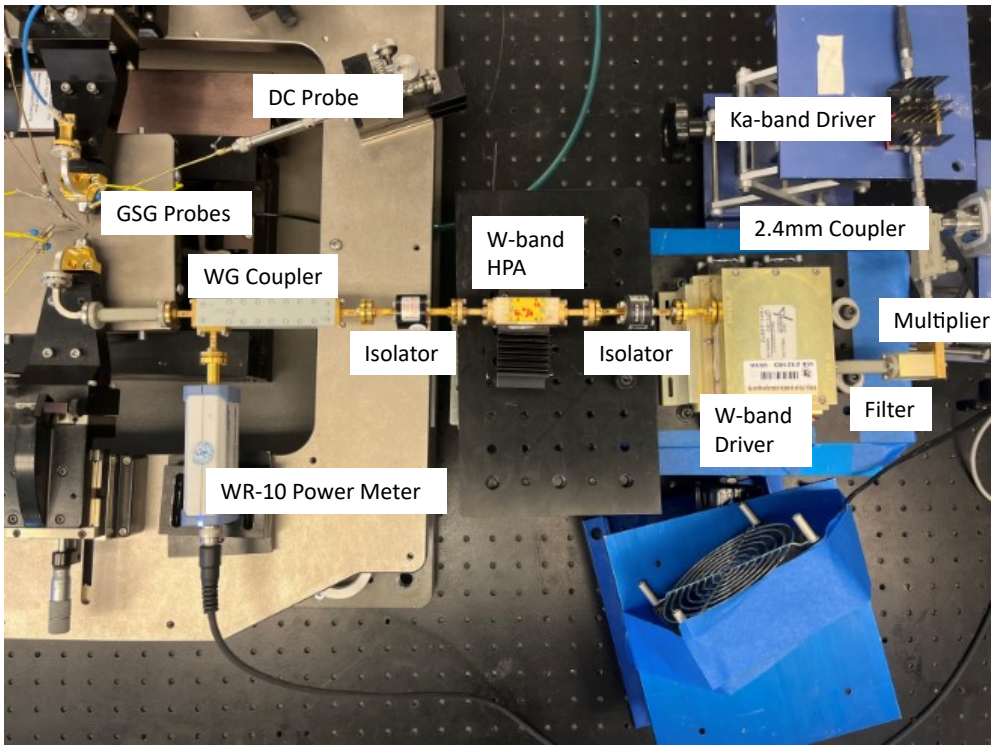


Figure 3.10: Large measurement test-bench setup photograph with labels of each individual component in the test chain.

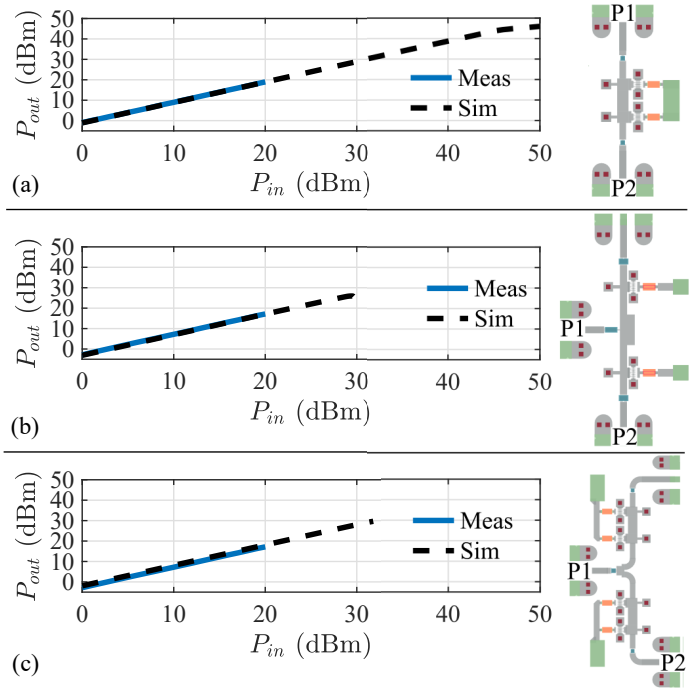


Figure 3.11: Measured and simulated large signal power sweep from 0 to 20 dBm of the (a) SPST (b) SPDT with one HEMT, and (c) SPDT with two HEMTs switches. Simulations shown until convergence is no longer met.

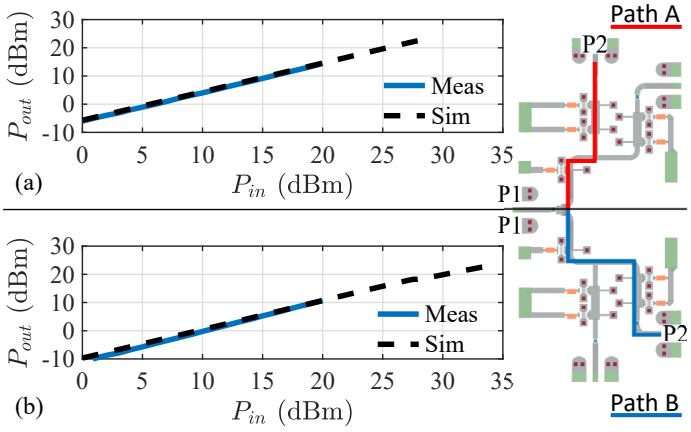


Figure 3.12: Measured and simulated large signal power sweep from 0 to 20 dBm of (a) path A outlined in red (b) path B outlined in blue of the SP4T HEMT switch. Simulations shown until convergence is no longer met.

Table 3.2: Comparison of presented switches in 40-nm GaN

Freq (GHz)	Type	Periphery$^{\triangle}$ μm	IL (dB)	ISO (dB)	P_{1dB} (dBm)	Size mm^2
55-110	SPST	300	**0.9-3.5**	**25-30**	>**20**$^{+}$	0.6
62-110	*SPDT	150	**1-2.2**	**15-20**	>**20**$^{+}$	1.125
55-110	$^{\blacksquare}$SPDT	300	**1.8-8**	**30-40**	>**20**$^{+}$	1.4
-	SP4T	-	-	-	-	3.92
50-105	Path A	300	**3.7-7.5**	**30-40**	>**20**$^{+}$	-
68-105	Path B	300	**5.5-10**	**30-40**	>**20**$^{+}$	-

$^{\triangle}$ Periphery of individual branch of each switch
* SPDT single-HEMT, $^{\blacksquare}$ SPDT double-HEMT
$^{+}$ Peak large-signal values @ P_{IN} = 20 dBm and 92 GHz

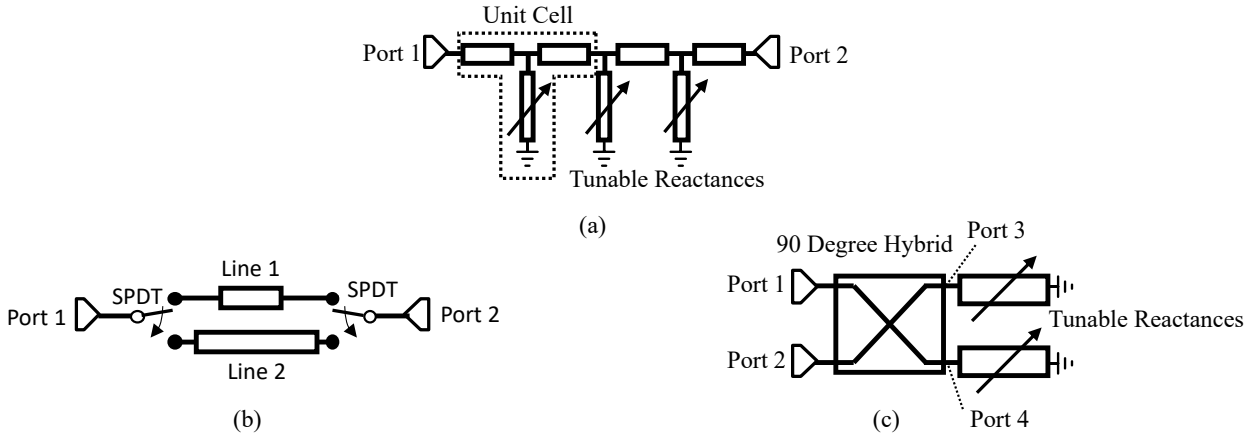


Figure 3.13: Circuit schematics of different phase shifter topologies showing (a) switched line phase shifter, (b) loaded line phase shifter and (c) reflective phase shifter [10].

between discrete phase states, or bits, whereas continuous phase shifters transition between phase states smoothly [10], [85].

From an analog circuit design perspective, the discrete phase shifter can be designed using switches and different lengths of transmission line to create different phase shift states. To obtain the desired phase difference through the phase shifter, the switches are selected in a way that chooses the path with a specific delay that corresponds to the required phase at a specific frequency. The design of continuous phase shifters is slightly more involved. A common topology is using 90 degree hybrid couplers and varying the impedances on ports 3 and 4, Fig 3.13, to change the phase of the signal as it passes through, as thoroughly reviewed in [11].

3.2.1 GaN HEMT Continuous Reflective Phase Shifters

Two continuous reflective phase shifters using GaN HEMTs are briefly presented: a 90° phase shifter and two of these circuits cascaded into a 180° phase shifter. To design a reflective phase shifter two main parts are needed: the 90 degree hybrid coupler and the reflective loads. For both designs, a lange coupler was chosen as the 90 degree hybrid coupler MMIC implementation due to its small footprint at W-band and broadband operation. The reflected load is acheived through gate-bias controlled diode-connected 4x25μm HEMTs as variable reactances. A control voltage of –1 V to +1 V allows a large variable impedance to be

achieved. The drains of these devices are connected to the lange coupler and a large resister at the gate aids in decoupling the control bias from the RF path.

These designs are both shown in Fig. 3.14 along with the measured phase states of each. Greater than 90° phase shift with less than 10 dB loss over the entire range of phase states is achieved over all of V- and W-bands. Power compression measurements were conducted for linearity at 95 GHz and showed a 19 dBm P1dB compression point. The cascaded design utilizing two lange couplers can be dynamically biased with its two separate control voltages to reduce the insertion loss of the circuit. Results indicate that there is strong agreement between the foundry model simulations and the measured results for predicting phase states, but does not predict the power compression characteristics of this type of circuit.

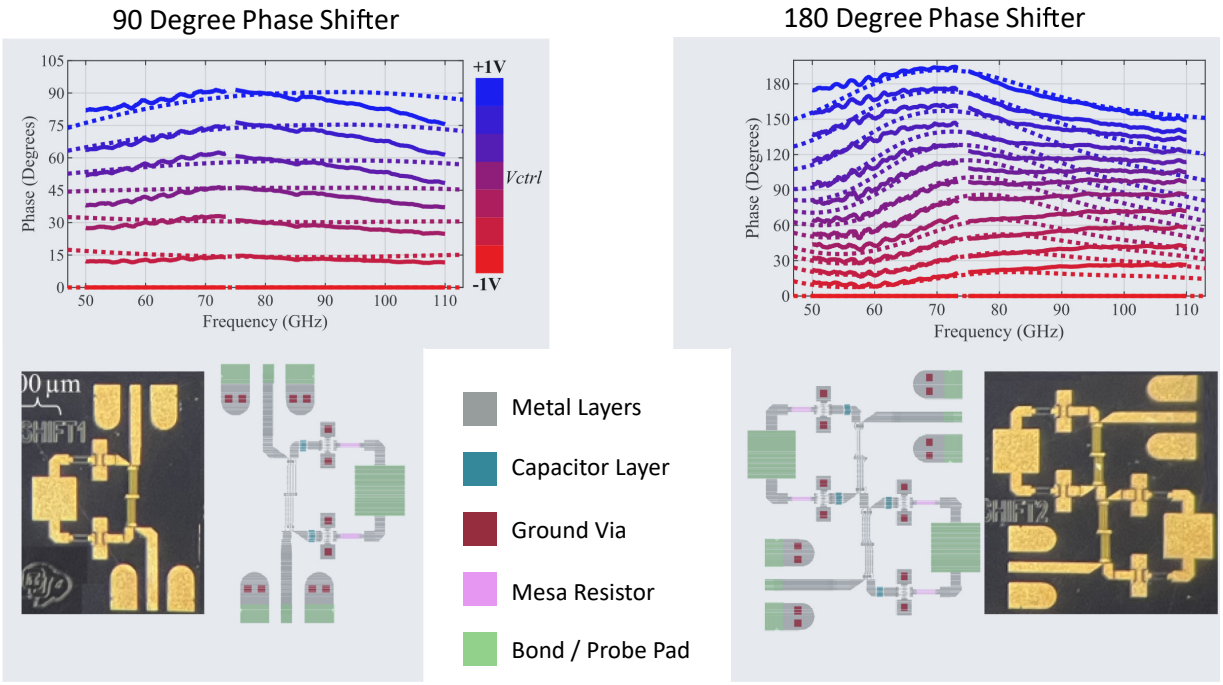


Figure 3.14: Plot of the phase states of each phase shifter along with the layout and photo of fabricated MMIC circuit for the 90 degree phase shifter (left) and for the 180 degree phase shifter (right) [11].

3.3 Chapter Summary

This chapter covered the design and modeling of V- and W- band switches and phase shifters using GaN HEMTs. The HEMTs are used in a source-grounded configuration with a large resistance at the gate where

the control voltage is fed. The quarter-wave shunt switches are biased at -10 V for the on state and 3 V for the off state. The HEMTs in the phase shifters are used as tunable reactances with a continuous control voltage between -1 to 1 V.

Four switches are demonstrated including a SPST, two SPDTs and a SP4T showing tradeoffs in performance based on HEMT periphery selection. None of the switches showed any signs of compression with up to 20 dBm on input power at 92 GHz with simulations indicating compression of the SPST switch occurring after 40 dBm (10W). These switches are fundamental building blocks of other components and systems including switches line phase shifters, Dicke radiometers and switched T/R front ends. The contributions of this chapter are published in [16].

Two continuous reflective phase shifters, one 90 degree and one 180 degree, are designed and validated with measured results. A lange coupler is used for both of the designs with two cascaded lange couplers being used in the 180 degree phase shifter. Large-signal measurements showed a P1 dB compression point of 19 dBm. Phased array systems and test instrumentation are possible applications of these designs. The results on phase shifter MMICs are published in [11] and partially in [75].

Chapter 4

Millimeter Wave Transistor Multiplier Theory and Modelling

Contents

In Chapters 2 and 3, nonlinear circuits such as power amplifiers and switches are described. Although these circuits are nonlinear in the sense that the output is not directly proportional to the input, the input and output signals are at the same RF frequency by design. There is a class of circuits, however, where the input and output frequencies are by design different, and these require high levels of nonlinearity in the circuit components. Examples are in signal generation (oscillators) which convert dc to RF, rectifiers which convert RF to dc, mixers which convert signals at two input frequencies (e.g. the LO and RF) into a signal at a third frequency (e.g. IF), pulse-compression circuits which convert a single-frequency signal to a broadband pulse,

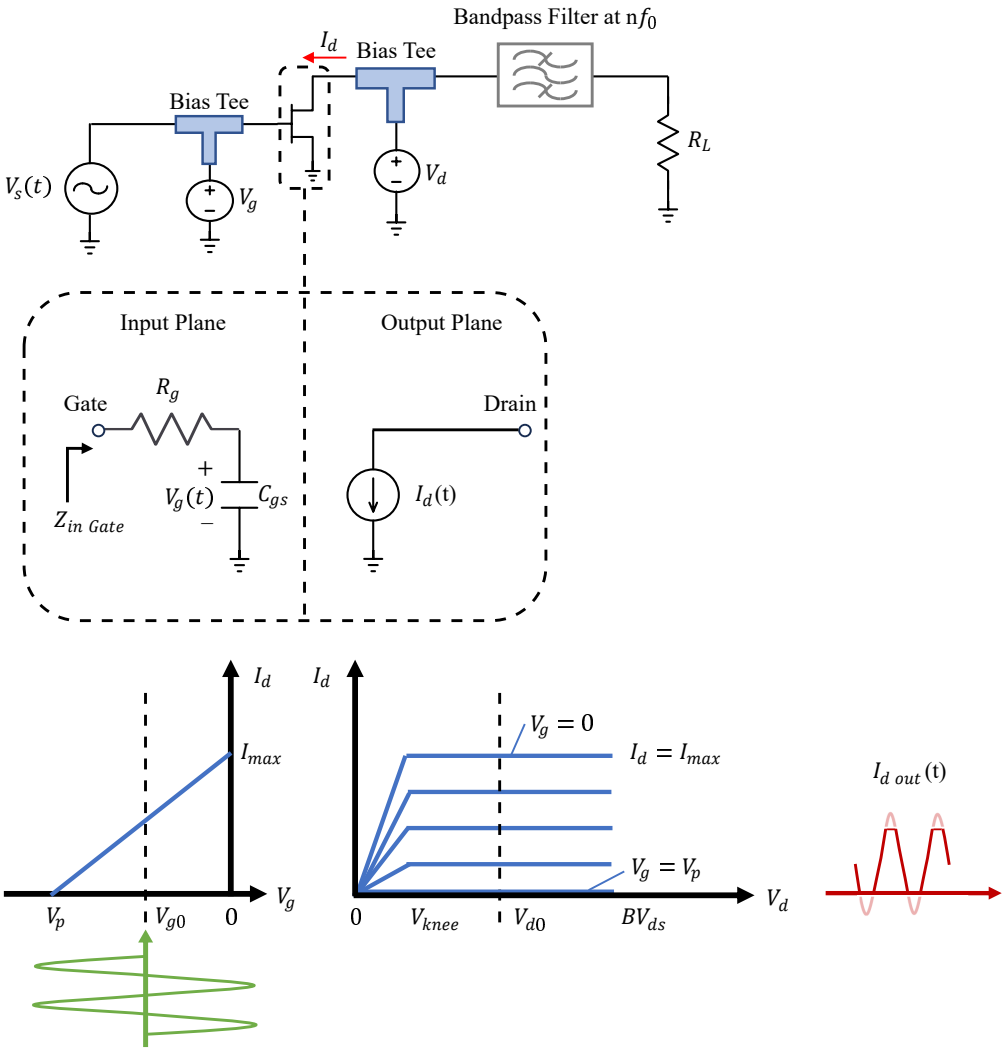


Figure 4.1: Schematic of a HEMT frequency multiplier ideal low frequency model showing the input and output plane. Unwanted harmonics generated at the output can be shorted out, together with the fundamental. The plots on the bottom show a graphical representation of the equivalent HEMT circuit model.

and frequency multipliers which convert a signal at a single frequency to signals at the harmonics. Frequency doublers and triplers, as well as their implementations in GaN MMICs at millimeter-wave frequencies, are discussed next. This chapter covers the theoretical basis for frequency multiplication in nonlinear circuits, while Chapter 5 gives example designs and their performance.

4.1 Harmonic Generation

Harmonic generation of a HEMT circuit is next analyzed at a fundamental level using a simplified equivalent circuit. Beginning with a standard low frequency HEMT model, a simplified model for determining the harmonic content of a frequency multiplier is extracted. As shown in Fig 4.1, the simplified model is reduced to an input plane where the input gate waveform $V_g(t)$ produces a non-sinusoidal drain current I_d with an equivalent resistance at the input R_g which can also be modeled but will be ignored for the following analysis. The output plane consists of a nonlinear current source dependant on the input waveform and trans-conductance of the device defined by:

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{-I_{d\,max}}{V_p} \tag{4.1}$$

Where I_{dmax} is the maximum drain current and V_p is the peak voltage at which the gate can still conduct. Ideal IV curves at the output plane, Fig 4.2, graphically show the limitations of the HEMT model. The maximum input voltage swing the device can conduct or handle falls between the knee voltage V_{knee} and the breakdown drain voltage BV_{ds}. Both of these parameters are process dependant and may change significantly from one semiconductor technology to another. The conduction angle is the portion of the input waveform that conducts during a full cycle given in radians or degrees:

$$\text{Conduction Angle} = \cos(\theta) = \frac{V_p - V_{bias}}{V_{g\ in\ max} - V_{g\ in\ min}} \tag{4.2}$$

Figure 4.2 shows a graphical representation of this definition and Eqn 4.2 gives the mathematical expression. Note that the gate bias gives direct control over the conduction angle. Classes of operation can be determined similar to the case of a FET amplifier except for this design, the emphasis is on biasing for largest harmonic generation instead of fundamental amplification. Table 4.1 summarizes amplifier classes based on their respective conduction angle. Up to a conduction angle of $\pi/2$ radians, the FET is in linear operation and does not generate any harmonic content. Once the input waveform is clipped on the maximum conducting parameters of the model (V_{knee},BV_{ds}) the output waveform becomes a Fourier cosine series described by:

$$I_d(t) = I_{dc} + \sum_{n=1}^{\infty} I_{dn} cos(n\omega t) \tag{4.3}$$

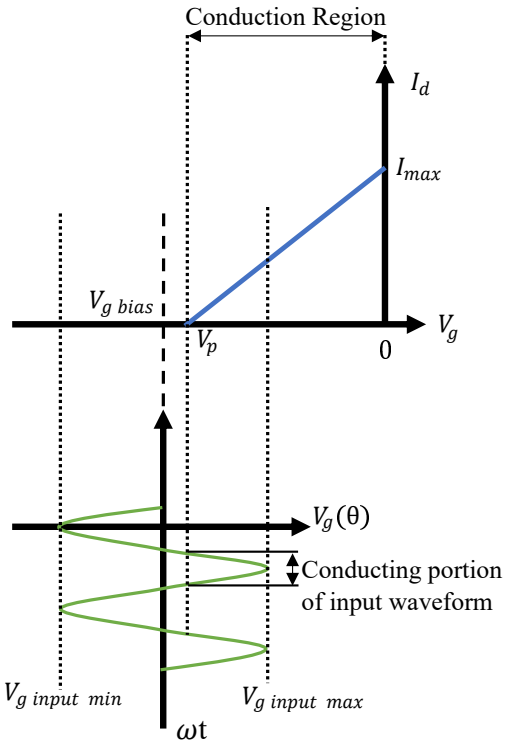


Figure 4.2: Graphical representation of conduction illustrating a green input cosine waveform. The conduction region of the model is shown and the portion of the input waveform which conducts during a single cycle is labeled.

and each individual harmonic component can be written as:

$$I_{dn} = \frac{2I_p}{\pi} \frac{sin(n\theta)cos(\theta) - nsin(\theta)cos(n\theta)}{n(n-1)^2(1-cos(\theta))}, \quad \text{for } n > 1 \quad \text{and } I_p = I_{max}(1 - \frac{V_g}{V_p}) \tag{4.4}$$

where n is the harmonic number and I_p is the peak current the device can handle.

Sweeping the conduction angle θ in Eqn 4.4 leads to a nice graphical method of determining the optimal angle for a desired harmonic, Fig 4.3. In this case the optimal angle for the second harmonic is 1.05 radians and the optimal angle for the third harmonic is 0.7 radians. These harmonic drain current magnitudes are summarized in Table 4.1 along with the fundamental component magnitude.

Table 4.1: HEMT Amplifier Classes of Operation

Class	A	AB	B	C
Conduction Angle	360°	>180°	180°	<180°

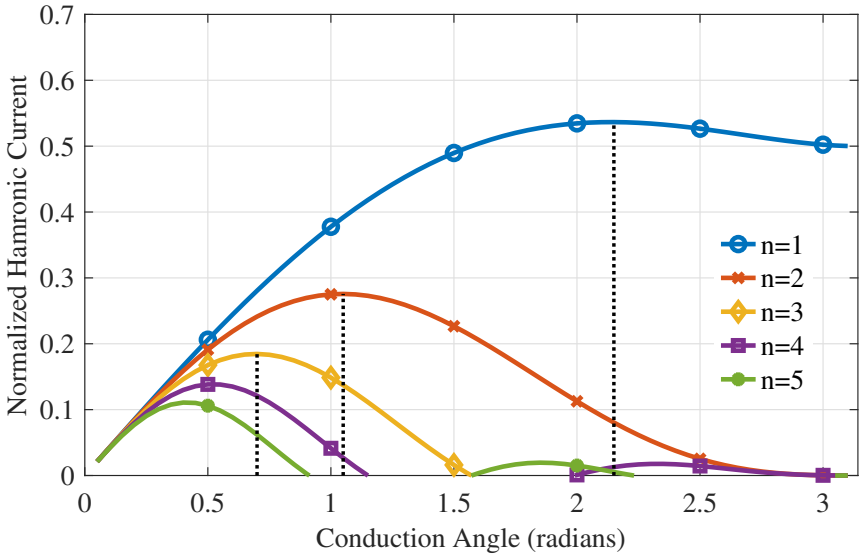


Figure 4.3: Drain current magnitude of the first five harmonic drain current components normalized based on Eqn 4.4. The maximum normalized harmonic current is denoted for the first three harmonics with a dotted vertical line.

At the output of the model, Fig 4.1, the voltage in the load will take the form of Eqn 4.5.

$$V_{dn} = \sum_{n=1}^{\infty} V_d cos(n\omega t) \tag{4.5}$$

To determine the optimal load, R_L, for a multiplier one can use the following relation, shown in Eqn 4.6, for a desired harmonic n.

$$V_L = I_n R_L \tag{4.6}$$

The power at the load of the multiplier is given is by:

$$P_{Ln} = \frac{1}{2} I_{dn}^2 R_L \tag{4.7}$$

Table 4.2: Maximum Harmonic Normalized Current Magnitude and Conduction Angle

$n^{th} Harmonic$	Current Magnitude	Conduction angle
1	0.5365	2.15 rad
2	0.2757	1.05 rad
3	0.1845	0.7 rad

The dc power with be the n=0 harmonic component of the Fourier series of the harmonic power.

$$P_{dc} = V_{d,n=0} I_{d,n=0} = V_{d\,bias} I_{d\,dc} \tag{4.8}$$

In order to maintain conservation of power, the power inputs and outputs can be expressed as Eqn 4.9. The dissipated power at the output, P_{diss}, is composed of the loss converted to heat in the device.

$$P_{in} = P_{out} + P_{diss} \quad \text{where, } P_{in} = P_{RF} + P_{dc} \tag{4.9}$$

Taking into account,

$$Z_{in\,Gate}(\omega) = R_g + \frac{1}{j\omega C_{gs}} \tag{4.10}$$

which is shown in Fig 4.1, the average power at the input may also be computed:

$$P_{av} = Z_{in\,Gate}(\frac{V_g}{\sqrt{2}})^2 = \frac{1}{2}(V_{g\ in\ max} - V_{g\ bias})^2 \omega^2 C_{gs}^2 (R_g) \tag{4.11}$$

The power at the output of the multiplier is at a desired harmonic of the input frequency. In an ideal case, the power at the output can be expressed as:

$$P_{out} = I_{dn}^2 \frac{R_L}{2} \tag{4.12}$$

The dc power is simply the product of drain bias voltage and the resulting dc drain current:

$$P_{dc} = I_{d\,n=0} V_{d\,bias} \tag{4.13}$$

With a perfectly matched source, P_{in} is equal to the average power, Eqn 4.11. All that is left of Eqn 4.9 is the dissipated power. For this we can begin in the time domain and use Parseval's theorem, for an arbitrary variable x as given in [86]:

$$P = \frac{1}{T}\int_0^T |x(t)|^2\,dt = \frac{1}{T}\int_0^T x(t)x^*(t)\,dx = \sum_{-\infty}^{\infty} z_n z_n^*, \quad \text{where } x(t) = \sum_{-\infty}^{\infty} z_n e^{j\omega nt} \tag{4.14}$$

The total average power of $x(t)$ is the sum average of its phasor components, z_n. Parseval's theorem applied to the dissipated power:

$$P_{diss} = \frac{1}{T}\int_0^T I_d(t) V_d(t)\,dt = \sum_{-\infty}^{\infty} I_{dn} V_{dn} \tag{4.15}$$

With the dc and average power determined, it is now possible to define efficiency for frequency multipliers. Commonly used efficiencies are defined by:

$$\eta_{drain} = \frac{P_{nf_0}}{P_{f_0}} \tag{4.16}$$

$$\eta_{total} = \frac{P_{nf_0}}{P_{f_0} + P_{dc}} \tag{4.17}$$

$$\eta_{dc} = \frac{P_{nf_0}}{P_{dc}} \tag{4.18}$$

$$PAE = \frac{P_{nf_0} - P_{f_0}}{P_{dc}}, \quad for \;\; n > 1 \tag{4.19}$$

Where P_{f_0} is the output power at the fundamental, P_{nf_0} is the output power at the $n^t h$ harmonic. Note that the efficiency of frequency multipliers will always be lower than an amplifier and several of these efficiencies may results in negative values, if the conversion gain is less than 1.

4.1.1 High frequency nonlinear effects

In reality, in addition to the g_m nonlinearity, the capacitance at the gate and drain, C_{gs} and C_{gd} as well as C_{ds} are also nonlinear. In GaN, C_{gd} is the dominant nonlinearity. Ideal capacitors contain no charge at 0 V; however, due to the voltage drop at the source resistance and intrinsic charges in HEMTs, the ideal assumption does not hold (integration constants are not zero). The capacitances in the device can more accurately be expressed as a Fourier series shown as a phaser representation in Eqn 4.20 as a function of voltage.

$$C(V) = \sum_{n=0}^{\infty} C_n e^{jn\omega t} \tag{4.20}$$

$$Q(V) = \int C(V)\, dV \tag{4.21}$$

In order to consider feedback, the harmonics are reflected back to the gate of the device. Considering a desired output harmonic n, the (n+1) and (n-1) terms are fed back to the gate. The assumption is made that all mixing products as a results of the feedback are in phase at the output and contribute to the output power at the desired harmonic P_n. Defining a harmonic feedback coupling coefficient M_n, power gain of frequency multiplication from the fundamental to the desired n^{th} harmonic G_m and large signal amplification of the n^{th}

harmonic that is fedback G_n, and the conversion gain of the mixing products of the fedback content G_{conv}, the power at the harmonic becomes:

$$P_n = (1 - M_n)[P_0 G_M + P_n M_n G_n + (P_{n-1} M_{n-1} + P_{n+1} M_{n+1}) G_{conv}] + \ldots \tag{4.22}$$

Where P_0 is the output power at the fundamental. To consider feedback we can use S parameters and the same stability criterion that is used for power amplifiers.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} > 1 \tag{4.23}$$

From the approximation of high frequency effects, it can be seen that it becomes increasingly difficult to analytically design a frequency multiplier. For this reason, in practice, there is a heavy reliance on device modeling and simulation using computational tools. This realistic modeling of GaN HEMTs at W-band will be outlined below but still rely on the basic principles stated above to operate. In reality phase of mixing products will not be ideal, especially at millimeter waves.

4.2 Single-Ended Frequency Multipliers

Single-ended active frequency multipliers can be implemented in any of the biasing schemes discussed above using a single transistor. As long as clipping of the waveform occurs, harmonics are generated. This principle is shown in Fig 4.4 using a 4x37.5 μm device model driven with 15 dBm of input power at 40 GHz. The plot of the spectrum indicates that harmonics are generated at this condition for a drain bias of 12 V and a gate bias of -1 V (Class B). The question then becomes what is the best class of operation for a frequency multiplier. In practice, Fig 4.3 can be used as a starting point for determining biasing for a desired harmonic n. Asymmetrically distorting the output waveform will generate even harmonics and symmetrical distortion will generate odd harmonics. For ideal performance, undesired fundamental and harmonic content must be shorted out as shown in Fig 4.1 with a bandpass filter. Single-ended frequency multiplier design using GaN HEMTs will be covered in Chapter 5.

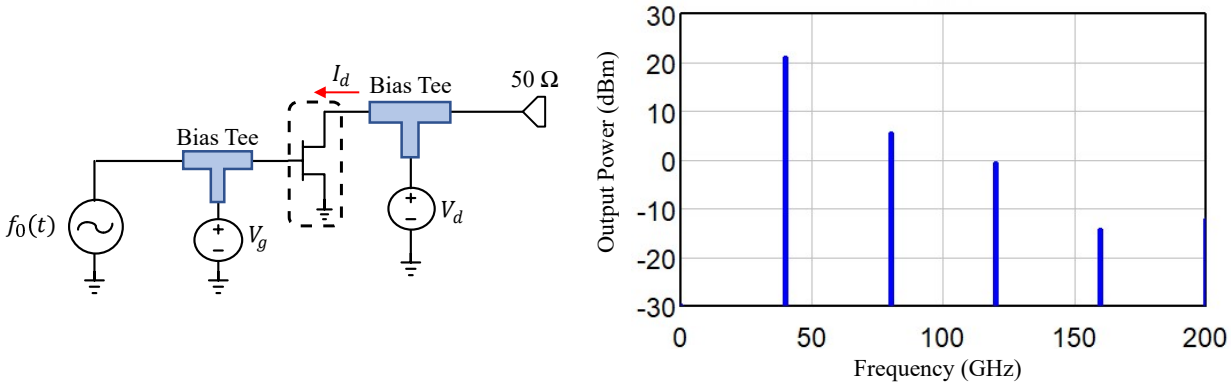


Figure 4.4: Schematic of a HEMT being driven with 15 dBm input power at 40 GHz (left) and the resulting spectrum indicating harmonics are generated at drain bias of 12 V and a gate bias of -1 V (Class B).

4.3 Balanced Frequency Multipliers

A balanced circuit topology inherently cancels the unwanted frequency content, while the power at the desired harmonic adds constructively at the output. With two identical multiplying branches in a balanced approach, the output power can be increased by up to 3 dB compared to the single-ended case, given the transistors in the two branches are saturated.

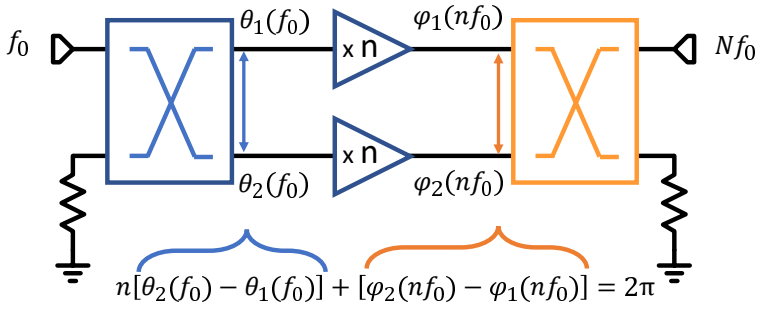


Figure 4.5: Schematic of balanced frequency multiplier circuit topology with labeled phase differences between the ports.

Balanced frequency multipliers require proper analysis of the phase difference between the balanced ports at all relevant harmonics. The method for determining the phases at the coupler output ports is well documented in [87]. The phase difference between the output ports at the n^{th} harmonic is given by Eqn 4.24.

$$\Delta\Phi_n = n[\theta_2(f_0) - \theta_1(f_0)] + [\varphi_2(nf_0) - \varphi_1(nf_0)] \tag{4.24}$$

where $\theta_2(f_0) - \theta_1(f_0)$ is the phase difference between the two balanced ports of the input coupler at the fundamental and $\varphi_2(nf_0) - \varphi_1(nf_0)$ is the phase difference between the input ports of the output coupler at the n-th harmonic, refer to Fig 4.5. The rejection of the n^{th} harmonic at the output is given by:

$$L_n = 10\log\left[\cos^2\left(\frac{\Delta\Phi_n}{2}\right)\right] \quad \text{(dB)} \tag{4.25}$$

This formulation does not take into account any amplitude or phase imbalances of the input and output couplers, or the rejection of the fundamental by the individual multipliers in both branches. The above relations yield several useful configurations for frequency multiplication which will be considered further for designs in GaN. In this thesis, two cases of the balanced configuration are used for a balanced doubler and tripler design. Multiplication factors of 4 or more will not be considered as multipliers that offer higher orders are generally a combination of doubling and tripling circuits. The chosen phases for the couplers in the multipliers demonstrated here are summarized in Table 4.3 along with several possible MMIC implementations.

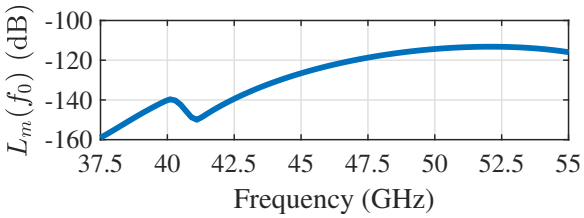
Table 4.3: Considered Configurations of Balanced Frequency Multipliers

	Doubler	Tripler
$\Delta\theta(f_0)$	180°	90°
$\Delta\varphi(nf_0)$	0°	90°
Possible MMIC Implementations	**Balun**$^+$	**Lange**$^+$
	Rat Race	Branch Line
	Tandem X	Hybrid

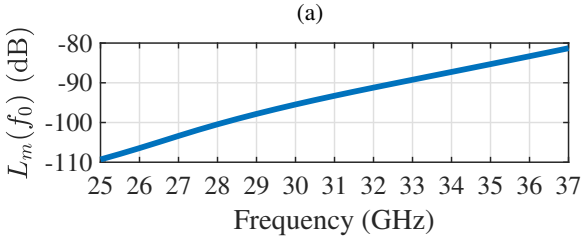
$^+$ Chosen coupler topology for each respective multiplier

A Marchand balun and Lange coupler are the chosen couplers for the balanced doubler and tripler respectively. The effect of the imbalance on harmonic rejection of the fundamental, L_1, is examined in Fig. 4.6 for the phase and amplitude imbalance of the Marchund balun and Lange couplers used in the designs detailed in Chapter 5. From these plots, it is seen that the balun and coupler designs are capable

of 80 dB rejection of the fundamental over their entire band of operation. Further, with this amount of suppression offered by the couplers alone, the matching networks in both of the balanced branches can be tuned for maximum desired harmonic output and does not need to focus on filtering or shorting the fundamental over a broad bandwidth.



(a)



(b)

Figure 4.6: Rejection of the fundamental, L_1, calculated using simulated phase mismatch of (a) the Marchand balun of the balanced doubler design; and (b) Lange couplers used in the balanced tripler design. The simulated phase imbalanced of the couplers is shown in Fig. 5.4 and Fig. 5.6.

4.4 HEMT Loadpull Harmonic Characterization

Generating the maximum amount of desired harmonic power from a HEMT is vital to achieving conversion gain in an active multiplier. Characterization of the HEMT begins with the bias selection, followed by harmonic loadpull nonlinear simulations to determine device harmonic performance within the accuracy of the nonlinear models. The harmonic loadpull simulation was performed for up to 5 harmonics of the input fundamental frequency in order to capture HEMT power output beyond the cutoff frequency of the device. In this section, the loadpull simulations of two device sizes of the HRL T3 process are considered and analyzed in terms of harmonic generation: a $4 \times 37.5\,\mu$m and a $4 \times 25\,\mu$m periphery HEMT.

The $4 \times 37.5\,\mu$m HEMT model is validated through measured data by the foundry, for drain supply voltages of 2, 6 and 12 V. The device has a sufficiently small periphery, and thus a low intrinsic capacitance while still providing enough gain and output power to achieve conversion gain. To determine which drain

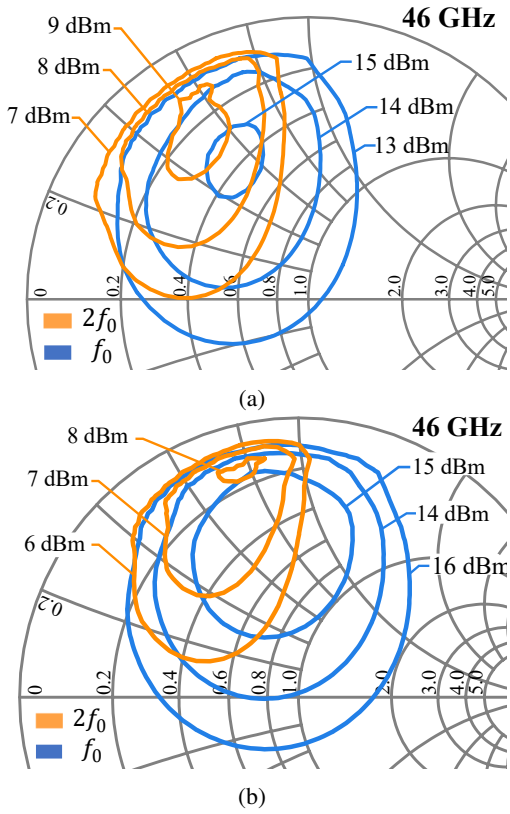
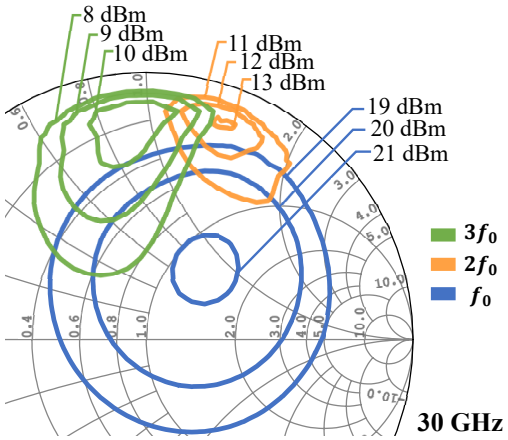


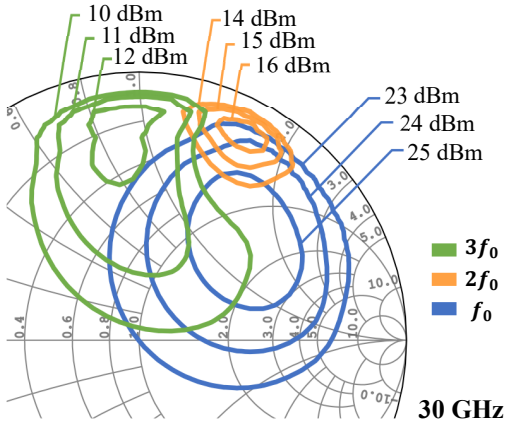
Figure 4.7: Simulated loadpull of fundamental 46-GHz and 2nd harmonic output power of the $4 \times 37.5\,\mu$m device matched for the fundamental source impedance on the gate and for maximum power at the second harmonic for two values of drain bias: (a) 6 V and (b) 12 V at an input power of 10 dBm. Both of the loadpull setups are matched for maximum power at the second harmonic at the drain of the device for their respective drain voltages and conjugate matched at the input for the fundamental source pull impedance.

voltages give better performance for harmonic generation, loadpull is conducted at a class-B gate bias of -1 V, at both the 6 V and 12 V drain supply voltage points, shown in Fig. 4.7 (a) and Fig. 4.7 (b), respectively. A mid-band fundamental frequency of 46 GHz is used for the simulations. Each of the loadpull setups are matched for maximum second harmonic power at the drain of the device for their respective drain voltages and conjugate-matched at the input for the fundamental source pull impedance.

The results show a 9 dBm output power at the 2nd harmonic for a 6 V drain supply, 1 dBm greater than at the 12 V drain bias for the same input drive of 10 dBm. At the 6 V supply voltage, less fundamental power is generated than at 12 V, making circuit design for fundamental rejection easier. The 6 V bias contours extend over a larger impedance range than the 12 V bias contours, resulting in an easier match. Therefore, a supply voltage of 6 V is a better choice for a balanced doubler to take advantage of the larger range of



(a)



(b)

Figure 4.8: Simulated loadpull of fundamental, 2nd and 3rd harmonic output power of the 4×25 μm device at 30 GHz showing (a) 6 V drain bias and (b) 12V drain bias for an input power of 20 dBm. Both of the loadpull setups are matched for maximum power at the 3rd harmonic at the drain of the device for their respective drain voltages and conjugate matched at the input for the fundamental source pull impedance.

impedances that provide a good match for output power, Fig. 4.7 (a). A -1.7 V gate bias point near pinch off is a good option for a single ended design whereas the optimal gate bias of a balanced design should be held at -1 V. The resulting low quiescent drain current of both doubler bias offers an advantage for efficiency, accompanied by a rich harmonic content of which the 2nd desired harmonic is the largest in magnitude.

The 4×25 μm HEMT is an extrapolated device model from the 2×25 μm HEMT. The HEMT is biased in class-A operation at $V_g = 0.5$ V, with I_d =30 mA, which results in high fundamental power and increasingly more odd-harmonic power as the device becomes over-driven and the waveform clipping increases [88]. Harmonic loadpull at both the 6 V and 12 V drain bias is conducted at an input drive of 20 dBm for the class A bias mentioned above. Results shown in Fig. 4.8 indicate 2 dBm more 3rd harmonic output power can be

obtained at the 12 V bias over the 6 V bias and consequently the 12 V drain bias optimal for a tripler. The fundamental and 2nd harmonic may be significantly larger than the desired 3rd harmonic, but are filtered out by design of the matching networks and the balanced topology. This loadpull data specifies impedances for the designs presented in the next chapter.

4.5 Chapter Summary

This section covers the theoretical basis for frequency multiplers using a simplified HEMT model. Harmonic generation is characterize for an ideal HEMT multiplier. Equations modeling ideal harmonic output power, multiplier efficiency amd harmonic rejection. are presented and discussed. Two HRL T3 GaN HEMTs are then harmonically characterized for frequency multiplication using load-pull simulations. A $4 \times 37.5\,\mu$m HEMT is characterized for optimal second harmonic generation for both a single ended design and a balanced design. A $4 \times 25\,\mu$m extrapolated device size is characterized for largest third harmonic generation for a balanced design, determining optimum load impedances for design of frequency doublers and triplers. The contributions of this chapter are partially presented in [89].

Chapter 5

Millimeter-Wave GaN Frequency Multiplication Circuits

Contents

Frequency multiplication is the shifting of a signal from one frequency to an integer multiple of that frequency. At higher millimeter-wave frequencies, frequency multiplication is one way to provide sufficient local oscillator power for mixers, and drive power for power amplifiers. This section will outline the active HEMT circuit topologies capable of this function expanding upon and validating the theory discussed in Chapter 4. Two different frequency doubler MMICs are designed, measured and compared. A full W-band tripler is also demonstrated.

5.1 Active Frequency Multipliers

Frequency multipliers require a nonlinearity in order to generate harmonics of the input signal. Not only is this non-linearity used, but it is maximized in order to get the best conversion gain possible. Frequency multipliers can be designed from nonlinear microwave components such as diodes and transistors. At W-band, passive and active multipliers have been demonstrated in various technologies. Diode GaAs Schottky [90–92], varactor [93] and nMOS [94] doublers have conversion loss that varies with bandwidth and frequency range, with demonstrated MMIC loss between 4 and 34 dB. These passive multipliers require relatively large input powers and result in typical efficiencies below 30%. GaAs doublers covering a very wide bandwidth from 50 to 128 GHz with about 12 dB conversion loss are described in [95]. Transistor multipliers require generally lower input powers and can have conversion gain. Table 5.1 gives a comparison of demonstrated W-band multiplier using diodes and transistors where some of the designs include multiplier chain topologies with added amplification between stage. A higher frequency octupler (100–140 GHz) [96] and a 70–110 GHz quadrupler [97], both with post-multiplication amplifier stages, in SiGe BiCMOS technology demonstrated 15 and 10 dB conversion gain, respectively. Technologies such as CMOS [98, 99] and InP [100, 101] show W-band conversion loss between 7 and 3 dB.

A number of HEMT multiplier chains are presented in [102, 103], e.g. in [103] a GaAs sixtupler with output power of over 7 dBm and a conversion gain of more than 6 dB in a 3-dB-bandwidth of 78 to 104 GHz is reported. Other GaAs MMIC multipliers include a $\times 4$ cascaded doubler with two gain stages at the end of the chain [104], a 68-80 GHz GaAs pHEMT doubler with a maximum output power of 10 dBm with -6 dB of conversion gain [105]. InP HBT multipliers have also been demonstrated [100] with a doubler/quadrupler chain integrated with a V-band VCO. A traveling-wave topology in [106] shows a frequency doubler utilizing four FETs designed in a 0.1 μm GaAs pHEMT MMIC process and a measured peak conversion gain of 3.2 dB from 85 to 100 GHz and a peak saturated output power of 9 dBm. A traveling wave doubler was realized in a 0.15 μm GaAs pHEMT process using 6 FETs measured a peak conversion gain of -4.3 dB and maximum output power of 7.1 dBm at W-band [107]. Lower frequency active doublers have also been demonstrated, e.g. a hybrid GaAs 10 – 20 GHz using a class-E topology with conversion gain up to 7 dB and 42.7% peak

drain efficiency [108]. The only published GaN multiplier, to the best of the authors' knowledge, is a doubler demonstrated at 77 GHz with −5 dB conversion gain and 10 dBm output power in [109].

Here we demonstrate two GaN doublers with conversion gain at an input power of 10 dBm and a tripler with 8.6–11.5 dBm output power at 19 dBm input accross W-band. The MMIC mutlipliers are implemented in an advanced 40-nm GaN on SiC process with f_T/f_{max} =200/400 GHz [116], in several circuit architectures shown in Fig. 5.1. Both of the doubler MMICs use two identical HEMTs, one in a single-ended and the other in a balanced topology. In order to achieve gain and fundamental suppression, an amplifier stage is added after the multiplier stage, as shown in Fig. 5.1 (a), while combining two doublers can be used to achieve increased output power, as shown in Fig. 5.1 (b). An investigation of these two-transistor topologies shows tradeoffs in combining the two approaches for best performance, with a goal of achieving W-band conversion gain with simultaneous increased output power and high fundamental frequency suppression. The tripler MMIC is design in a balanced architecture with two identical multiplying branches for power combining, Fig.5.1(c). In addition to the high-power handling capability of GaN, these multipliers can be monolithically integrated with other demonstrated circuits, such as watt-level power amplifiers [117, 118], phase shifters [119], switches and LNAs [120]. These active multipliers can be operated from the same high supply voltage as other front-end GaN circuit components.

5.2 Design Methodology

5.2.1 Single-Ended Doubler Topology

The single-ended topology is composed of a doubling stage followed by an amplifier stage at the 2nd harmonic. Since a single HEMT can provide 9 dBm of 2nd harmonic power at a 10 dBm input drive at 46 GHz, the circuit will benefit more from the second device operating as a post-multiplication amplifier as opposed to a fundamental driver amplifier for the doubler. The post-multiplication amplifier stage is biased at 12 V for higher output power and this is used for the doubling HEMT as well.

The doubling device is matched to the fundamental source pull impedance using microstrip transmission lines. The interstage match converts the drain impedance at the 2nd harmonic of the doubling HEMT to the

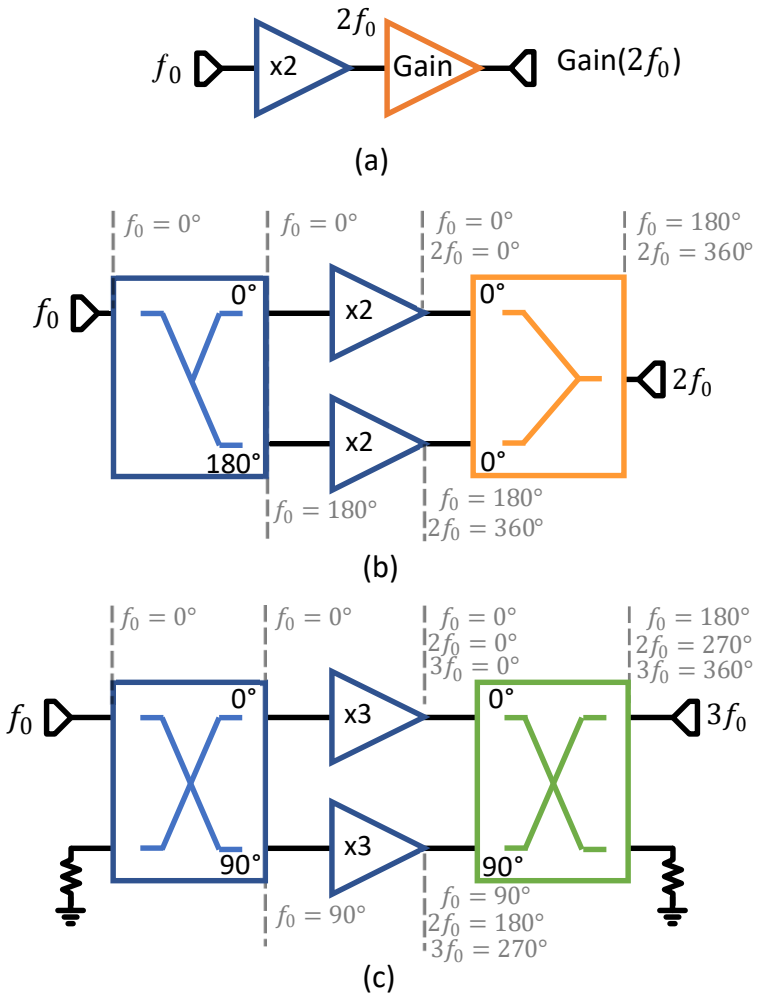


Figure 5.1: Different transistor-based frequency multiplier topologies demonstrated in this paper in GaN MMIC designs with output frequency nf_0 in W band: (a) single-ended frequency doubler with post-multiplication amplifier (b) balanced frequency doubler and (c) balanced frequency tripler.

2nd harmonic source impedance of the amplifying device matched to 50 Ω at the output. The layout of the fabricated MMIC is shown in Fig. 5.2, with bias lines that alternate in position to allow enough room for the stability networks discussed below.

The multiplying HEMT is biased in class-C to generate harmonics while the second amplifying HEMT is biased in class-AB is to achieve maximum output power at the second harmonic. The second stage device periphery is chosen such that the power of the output signal from the first stage can compress the second stage. This allows better efficiency out of the second stage amplifier. In the interstage a small series capacitor which isolates gate and drain voltages, allows for high-pass response and suppression of the fundamental frequency that is still generated by the first stage. The output impedance of the second stage is chosen to be

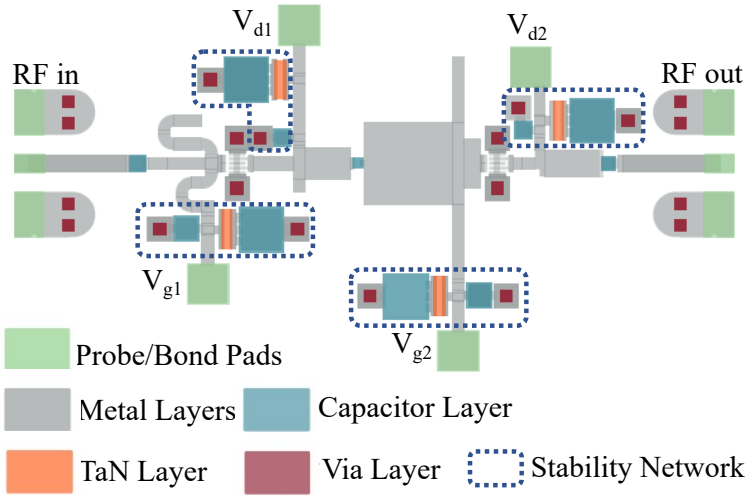


Figure 5.2: MMIC layout of the single ended frequency doubler with a total layout size of 2,000 μm $\times$ 950 μm. Shown in the figure are the main metal, capacitor and resistive layers. Several process layers have been removed for clarity.

the loadpull impedance that achieves maximum output power of the 2nd harmonic of the doubling device.

5.2.2 Balanced Doubler Topology

In an ideal balanced topology, the fundamental frequency content is perfectly shorted when combined at the output. The 2nd harmonic currents are in phase at the output and combine in magnitude [121]. Since a balanced topology is used, 3 dBm more input drive will be necessary to compress the individual HEMTs compared to the single-ended topology. Biasing the individual multiplying branches in class B allows more harmonic generation at lower input drive levels then a class C bias.

The input coupler of the balanced doubler topology requires a 180° phase shift and even power split of the input signal at the two balanced ports. Several approaches to this coupler have been realized, e.g, a Lange coupler combined with a CPW phase shifter in [113], a 180° rat-race in [122], and a planar Marchand balun in [123]. The millimeter-wave operating frequency of the circuit enables implementation of a planar balun in a reasonable footprint. With the three metalization layers and airbridges in the HRL T3 process, a planar Marchand balun is designed as shown in Fig. 5.3.

Traditional planar Marchand baluns utilize two coupled lines with the ends of one of the lines tied to ground through vias. Planar baluns which contain only one grounded line tend to have more leakage fields,

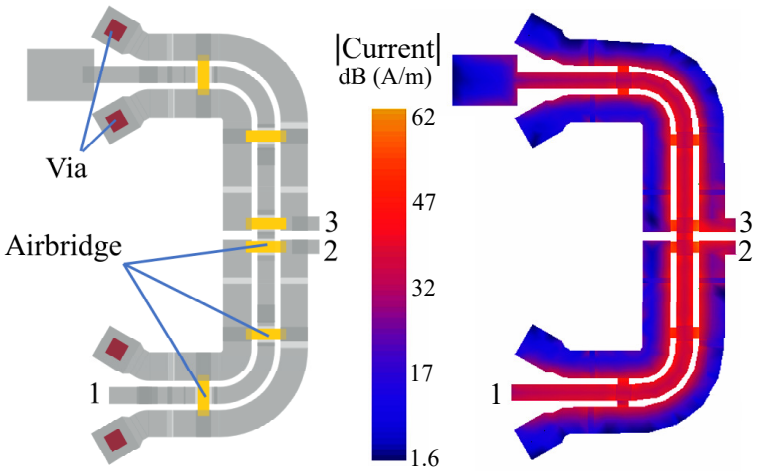
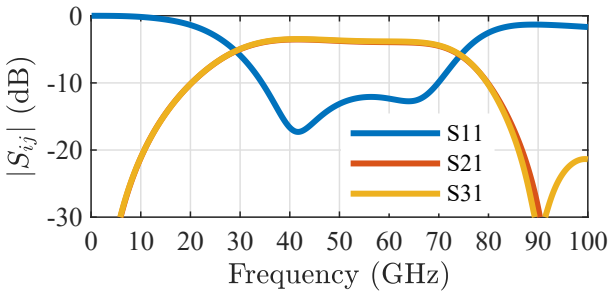


Figure 5.3: MMIC layout of modified marchand balun. The current density distribution at 44 GHz is shown. The warmer red colors indicate higher current concentrations, confirming the desired even excitation of the balun.

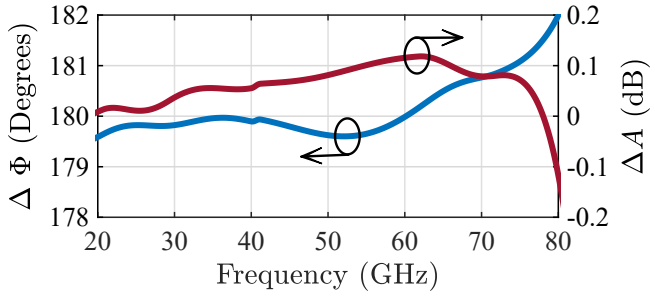
creating additional loss. A third coupled line is added to the planar balun to minimize this leakage field and lower through-loss in the signal path, as in [124]. Furthermore, to increase coupling between the grounded edge quarter-wave lines of the balun, air bridges are used at three different places along each branch [95]. This helps maintain an even power split and 180° phase split over a broad frequency range. The quarter wave coupled lines are curved to make the circuit fit in a 2100 μm × 1200 μm footprint and with GSG pads that allow aligned probing. The layout of the curved planar Marchand balun is shown in Fig. 5.3 along with the RF surface current magnitude distribution at 44 GHz.

The balun is design for fundamental input frequencies from 37.5 to 55 GHz. Since an even phase shift and power split are essential for canceling the fundamental and properly combining the 2^{nd} harmonic at the output, special care is taken to minimize the phase and amplitude error. Small-signal S-parameters of the three coupled-line planar Marchand balun are displayed in Fig. 5.4 (a) and Fig. 5.4 (b) showing the phase and amplitude imbalance. Simulations of the balun reveal a 180° phase shift across the operating bandwidth of the doubler with a phase variation of ±0.5°. An amplitude imbalance of ±0.1 dB is realized across that same band.

A supply voltage of 6 V is chosen for the balanced doubler to take advantage of the larger range of impedances that provide a good match for output power, Fig.4.7(a). To preserve symmetry, the bias lines do not cross the virtual ground plane in the middle of the circuit. For this reason, the HEMTs of the balanced



(a)



(b)

Figure 5.4: Simulated performance of the planar Marchand balun. (a) S-parameters up to 100 GHz; and (b) phase and amplitude imbalance from 20 to 80 GHz.

doubler are biased separately from each side of the chip through their own off-chip capacitors.

Reactive matching converts the 50 Ω balun impedance to the fundamental source impedance of the HEMT. The same input matching network is used for both devices, and the drains of the doubling HEMTs are reactively power-combined and matched to 50 Ω at the output. The drain impedance found from loadpull is used to create the initial match and large signal simulations of nonlinear Angelov models are used to tune the network for optimized performance. The layout of the balanced doubler is shown in Fig. 5.5 with highlighted stability networks which will be discussed in further sections.

5.2.3 Balanced Tripler Topology

The 25–33 GHz input of the balanced tripler is fed through a 90° coupler, creating the two balanced branches. The fundamental harmonic component remains 90° out of phase between the multiplying branches as it passes through. The 2nd harmonic voltages are 180° out of phase after the multiplying HEMTs, while the 3rd harmonic voltages are 270° out of phase. The 90° output hybrid then combines all the harmonic powers

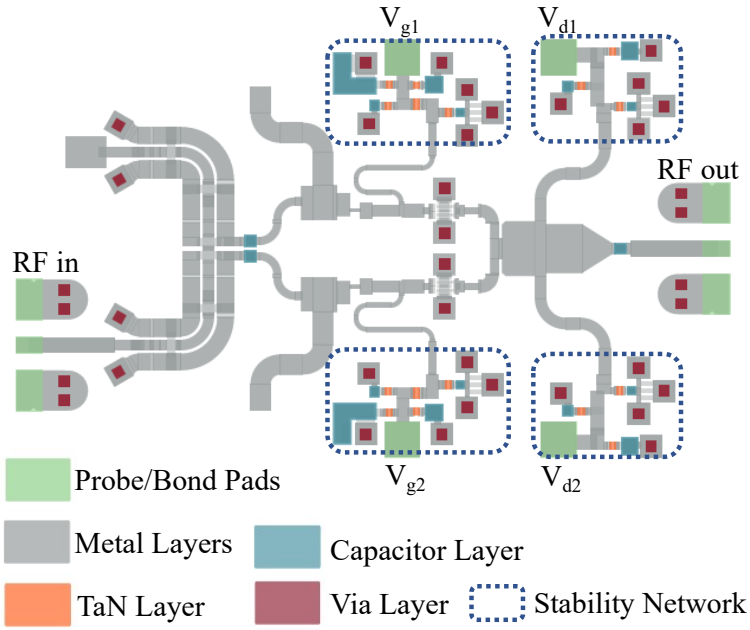


Figure 5.5: MMIC layout of balanced frequency doubler with a total layout size of 2100 μm $\times$ 1200 μm. Shown in the figure are the main metal, capacitor and resistive layers. Several process layers have been removed for clarity.

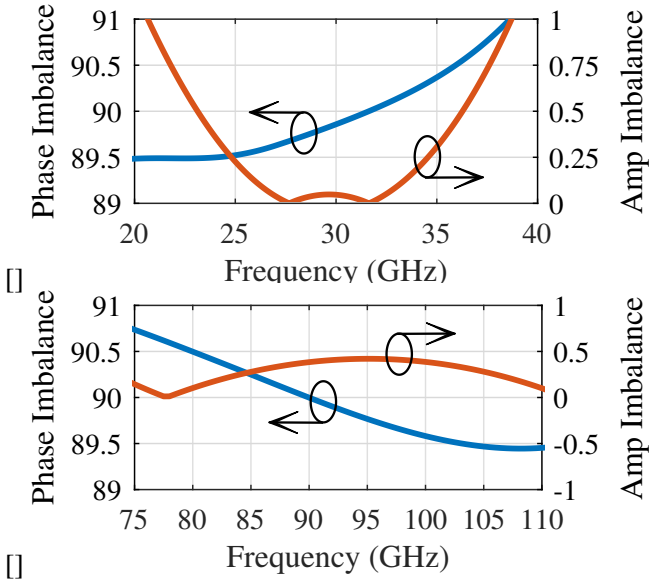


Figure 5.6: Simulated amplitude and phase imbalance for: (a) K-band input Lange coupler; and (b) W-band output Lange coupler.

from the balanced multiplying branches resulting in the 3rd harmonic component combined in phase, the 2nd harmonic to be 90° out of phase, and the fundamental to distructively interfere.

The input and output couplers need to have a 90° phase shift through their respective bands of operation.

There are several possible MMIC implementations for such couplers, listed in Table 4.1. The ideal coupler offers a perfect phase shift and amplitude split over a broad frequency range while having a small footprint on a MMIC layout. A Lange coupler is chosen due to its broadband properties and compact form factor. Any deviation from 90° phase difference or 3 dB power split between output ports results in degradation of the performance of the balanced topology as the harmonics will no long combine properly. The simulated amplitude and phase imbalance of the implemented couplers is shown in Fig. 5.6.

5.2.4 Stability Analysis and Simulated Performance

W-band HEMTs have high gain at lower frequencies, therefore stability needs to be carefully analyzed from dc to several harmonics of the output frequency. Small stability resistors at the gates of the HEMTs increase loss, lower conversion gain and lower efficiency, and are therefore avoided for all circuit designs. Alternatively, potential instabilities are corrected through stability networks for stability up to the 3^{rd} harmonic. These networks consist of capacitors and RC networks added to the bias lines which present a short to ground at lower frequencies where gain of the device is high. Resistors are added in between the capacitors in the bias lines ranging from 5–30 Ω to attenuate resonances which may occur between the reactive components. K-factor, Nyquist stability criterion and loop gain were analyzed for frequencies up to the third harmonic. The Nyquist polar plots in Fig. 5.8, Fig. 5.9 (b) and the loop gain simulation plots in Fig. 5.9 (a) show stable operation of the circuits up to 330 GHz.

Further stability analysis with swept input and output reflection coefficients allows instabilities arising from input and output mismatch to be found and corrected. Additionally, modeling bond wires with full-wave analysis, as well as including modeled off-chip capacitor networks at the bias pads of the circuits for both large- and small-signal simulations helps in revealing potential parasitic resonances in the bias networks.

Fig. 5.10 shows the simulated output power of the 2^{nd} harmonic and unwanted fundamental as a function of the input power for all the presented circuit topologies as well as the 3^{rd} harmonic for the tripler. The single-ended doubler has a maximum simulated power of 21 dBm at an input drive of 15 dBm. The fundamental suppression varies between 25 to 55 dBc up to the 100 GHz upper edge of the operating band, and decreases to 15 dBc at 110 GHz. The balanced doubler has more power at a lower input drive and

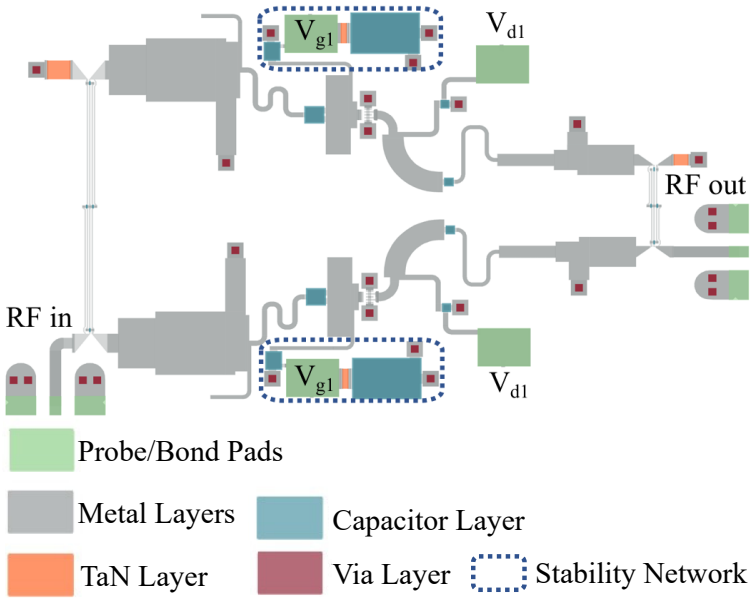


Figure 5.7: MMIC layout of the frequency tripler with a total layout size of 2800 μm $\times$ 1550 μm. Shown in the figure are the main metal, capacitor and resistive layers. Several process layers have been removed for clarity.

saturates at 15 dBm output power. Fundamental suppression is approximately constant across power and frequency at $\simeq$ 30 dBc. A maximum simulated output power of 11.8 dBm accross W-band is shown for the tripler at an input drive of 25 dBm.

5.3 Experimental Characterization

Measurements are conducted on a Summit 9000 probe station for both small- and large-signal measurements.

5.3.1 Small Signal Measurements

The chip die and off-chip capacitors are epoxied using Epo-Tek H20 on a gold-nickel coated copper-molybdenum (CuMo) carrier plate, Fig.5.11 (a). The off-chip capacitors are arranged in a ladder configuration with the smallest capacitors wire-bonded to the on-chip bias pads. DC probes are landed on the largest of the off-chip capacitors and connected to the dc power supplies through a low-frequency parallel RC filter to eliminate potential ground loops occurring in the probe station. Photographs of the two doubler chips are shown in Fig. 5.11.

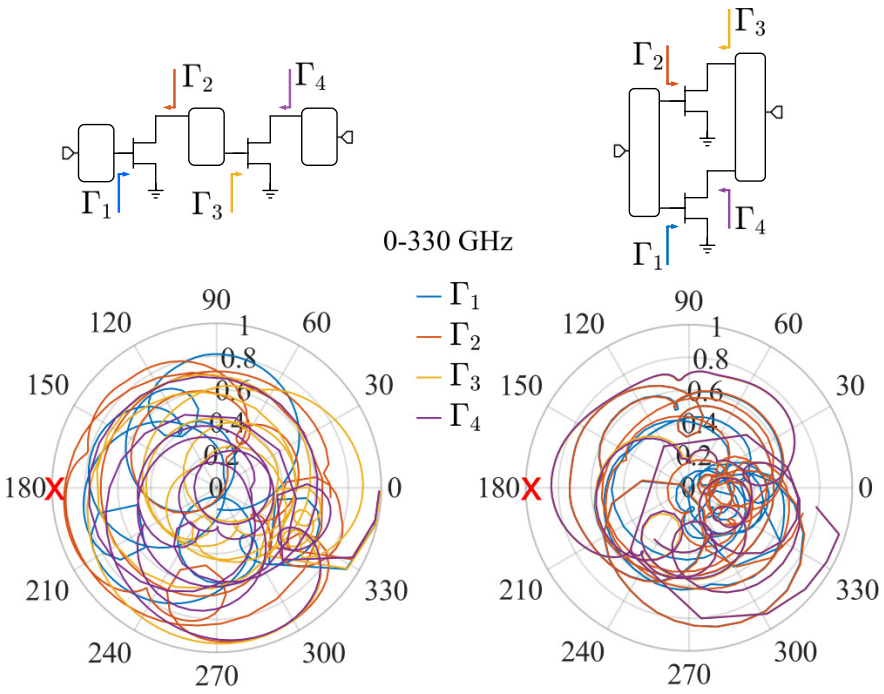


Figure 5.8: Nyquist stability criterion of both the single-ended (left plot) and balanced doubler (right plot) from 0-330 GHz. Both plots show stable operation of the doublers up to the third harmonic of the output spectrum. The different colored lines correspond to Nyquist analysis in various stages of the circuits as indicated with corresponding colors. The red cross indicates the Nyquist instability avoided in the designs.

The small-signal output match is measured with a HP8510C network analyzer with W-band extenders while the input is loaded with a 2.4 mm 50-Ω load at the probe. The input match is measured with an Agilent E8364C PNA while the output is held at 50 Ω with a WR-10 waveguide load and probe. All small-signal on-wafer measurements were calibrated with a TOSM calibration using impedance standard substrates (ISS) 101-190 and 104-783 from Cascade Microtech for the fundamental input and harmonic output matches, respectively. With this measurement setup, the input and output match of the active multipliers is measured in their respective frequency bands, and the small-signal measured results are shown in Fig. 5.12 and compared to simulated data.

5.3.2 Large Signal Measurements

The on-wafer measurement setup including both the fundamental and harmonic measurement is summarized in Fig. 5.13. A HP83650A synthesized swept-signal generator provides the 37.5-50 GHz or 25-36.6 GHz input signals and drives the HP83050A system amplifier. A 10 dB, directional coupler connects directly to

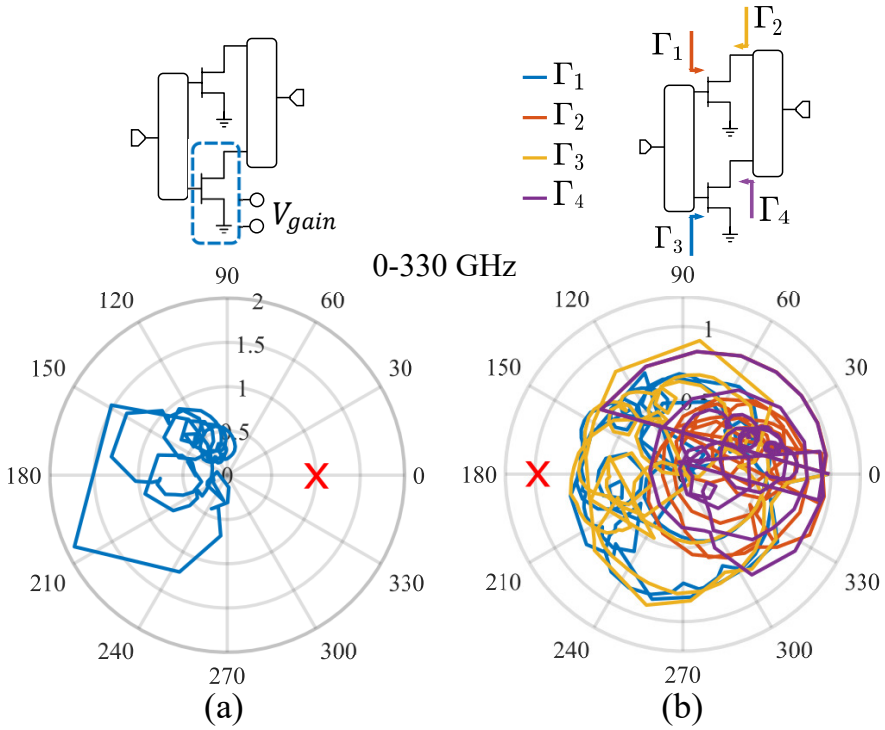
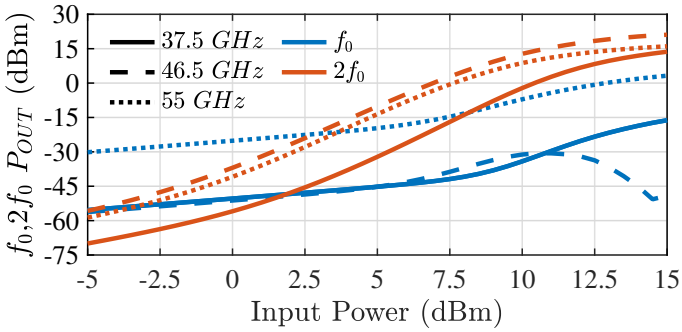


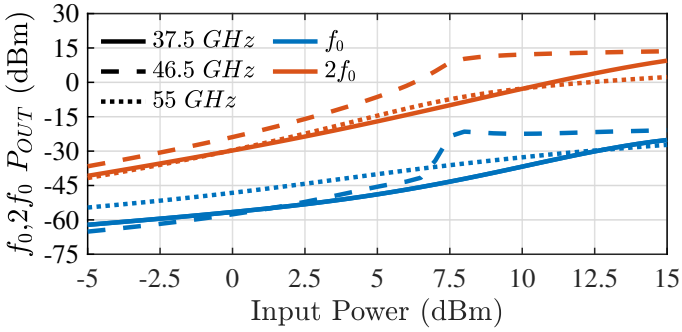
Figure 5.9: Stability analysis performed on the balanced tripler: (a) Loop gain from 0-330 GHz and (b) Nyquist stability criterion from 0-330 GHz. Both plots show stable operation of the tripler up to the third harmonic of the output spectrum. The different colored lines correspond to Nyquist analysis in various stages of the circuits as indicated with corresponding colors. The red cross indicates the Nyquist and loop gain instability avoided in the designs.

the 100 μm GSG probe to bring the RF CW test signal to the DUT input reference plane. Since the source is limited to 50 GHz, it is only possible to test up to 100 GHz at the 2^{nd} harmonic output for the doublers. An on-wafer *through* calibration on a standard alumina substrate from Cascade Microtech is used to calibrate the losses of the probes. The loss of the 2.4 mm coaxial 10 dB coupler is measured, and along with the measured losses of the cables and probes, a power calibration is performed to the reference plane of the DUT at the input and output.

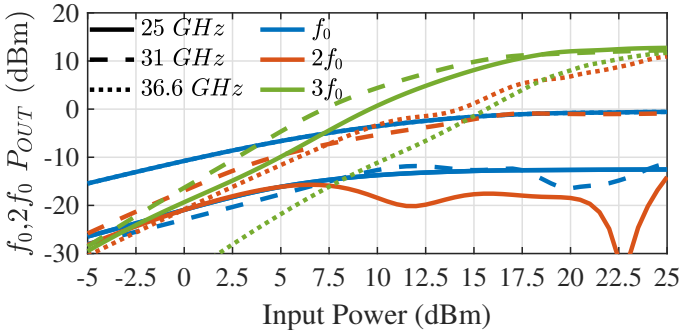
The output power at the fundamental is measured using a HP8565E spectrum analyzer with a 100 μm coaxial GSG probe. To test the 2^{nd} harmonic output, the spectrum analyzer is replaced with a W-band waveguide power meter for the doublers and a V-band waveguide power meter for the tripler. The power meter is connect to a WR-10 or WR-8 waveguide coupler, which is in turn connected to the GSG probe through a 1 mm coax transition and cable. Due to limitations in the test setup, the input drive is limited to 10 dBm and 19 dBm at the device plane for the doublers and tripler, respectively.



(a)



(b)



(c)

Figure 5.10: Simulated fundamental and 2^{nd} harmonic output power of a) single ended and b) balanced frequency doublers. In c) simulated 3^{rd} harmonic is also shown for the frequency tripler . Results from the center and edges of the input frequency band are shown across an input power range of -5 dBm to 15 dBm for the doublers and -5 dBm to 25 dBm for the tripler.

5.4 Results and Analysis

Measured results of the single-ended doubler show a maximum 2^{nd} harmonic output power of 11.5 dBm at an input power of 10 dBm at 81.5 GHz. The balanced doubler achieves a maximum 2^{nd} harmonic power of 13.79 dBm at the same input power. Frequency multiplication (conversion) gain for the doublers is defined

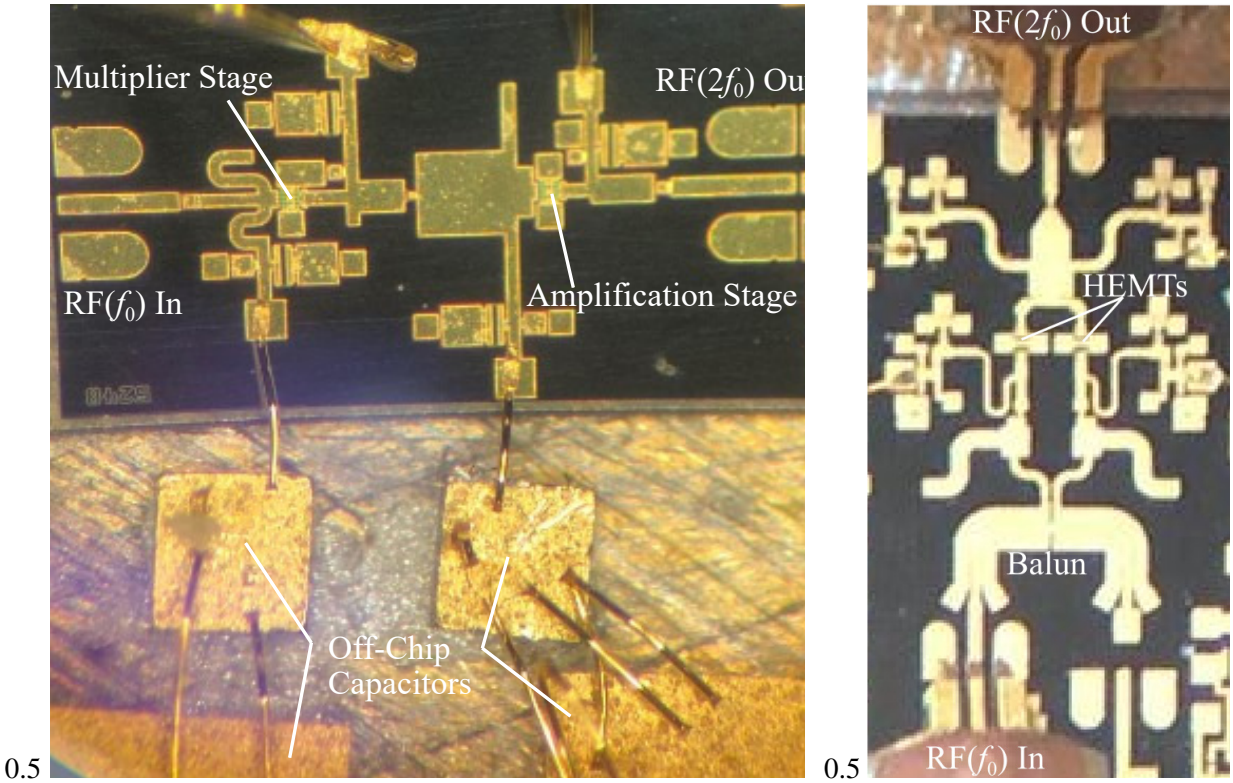


Figure 5.11: Photograph of the MMIC doublers for (a) single ended circuit with bond wires and off-chip capacitors and (b) balanced doubler circuit.

as:

$$G_c = \frac{P_{out}(2f_0)}{P_{in}(f_0)} \tag{5.1}$$

where $P_{out}(2f_0)$ is the output power at the 2^{nd} harmonic and $P_{in}(f_0)$ is the fundamental input power. Both doublers achieve conversion gain. The single-ended topology has a maximum conversion gain of 1.5 dB at a 10 dBm input drive and the balanced attains 3.8 dB at the same input power. The balanced doubler measures conversion gain from 92-100 GHz with over 13.7 dBm of output power at an input of 10 dBm. The measured conversion gain of both of the doublers is shown in Fig. 5.14 (a). Fundamental suppression is calculated for both doublers based on the measured output powers of the fundamental and 2^{nd} harmonic. Fig. 5.14 (b) shows the fundamental suppression for an input power of 10 dBm across frequency. The single-ended and balanced doublers have better than 55 dBc fundamental suppression.

The measured large signal performance at the 1^{st}, 2^{nd} and 3^{rd} harmonic of the tripler is shown in Fig. 5.15. At a drive power of 19 dBm, the balanced tripler produces a 3^{rd} harmonic output power of

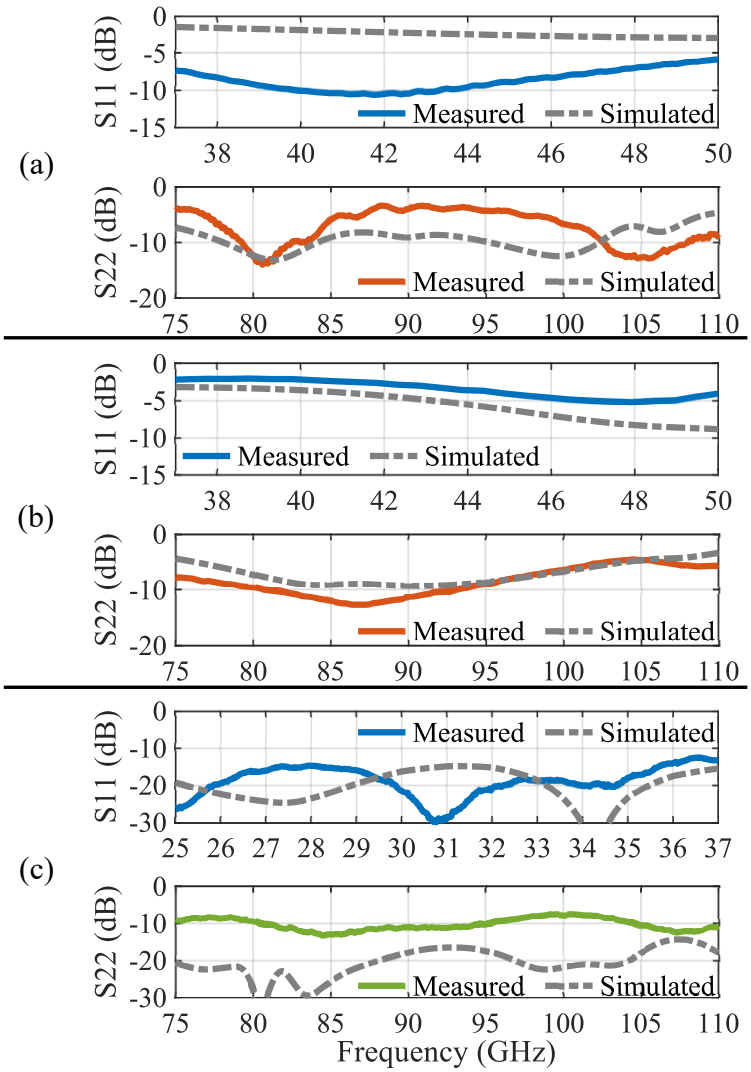


Figure 5.12: Input and output match of (a) single ended doubler, (b) balanced doubler and (c) balanced tripler. All measurements are performed with the Keysight E8364C and HP 8510C network analyzers.

10±1.5 dBm across W-band, with a measured maximum 3^{rd} harmonic output power of 11.68 dBm at 105.6 GHz. Measured harmonic suppression can be calculated from Fig. 5.15 with maximum suppression of 29 and 29.5 dBm for the tripler's fundamental and second harmonic. The suppression of the harmonics lowers near the ends of the band of operation to -15 dBc and -18 at 25 GHz and 36.6 GHz, respectively. The balanced doubler demonstrated a broadband performance with over -7 dBm of measured conversion gain from 75–100 GHz compared to 77.5–87.5 GHz for the single-ended. A broadband performance is also demonstrated for the tripler circuit measuring a conversion gain of over -10.4 dBm from 75-110 GHz. The broadband performance of the balanced designs stems from the inherent harmonic cancellation in the

couplers allowing for the matching networks to be designed for a broadband match. For operation at higher input drive levels, the single-ended doubler will provide more output power as the amplifying HEMT in the circuit is driven close to saturation.

Although each of the circuits exhibit similar maximum measured power, they use different amounts of dc current. Fig. 5.16 shows the measured dc power consumed by the multipliers over their output frequency range. The single-ended doubler has a higher bias current, most of which originates from the gain stage. Biasing the balanced douber near pinch off results in a low drain current, which together with the lower drain voltage bias offers significantly lower power consumption than the single ended doubler. Since the tripler is biased near class A, it will draw a high drain current.

5.5 Chapter Summary

This work presents a single-ended frequency doubler, a balanced frequency doubler and a balanced frequency tripler implemented in the HRL T3 40 nm GaN process. The tripler measures an output power of 10±1.5 dBm for an input power of 19 dBm from 75–110 GHz. Both doublers achieve conversion gain and over 11 dBm output power in the W-band frequency range. Reactive matching and cascading of a post-multiplication amplifier stage allows the single ended topology to exhibit conversion gain and high fundamental suppression. Balanced topologies implemented with broadband couplers allows high harmonic suppression with a wide-

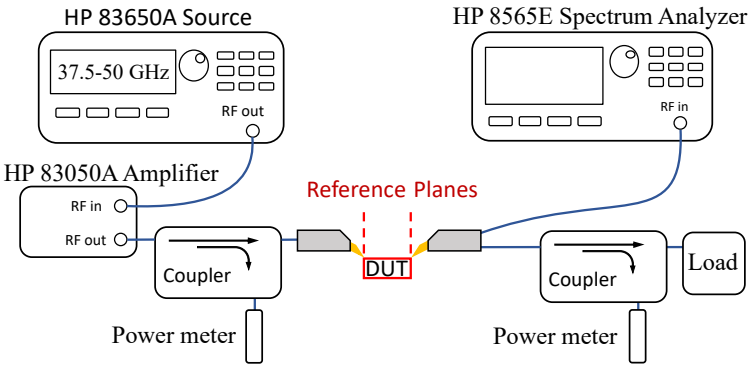
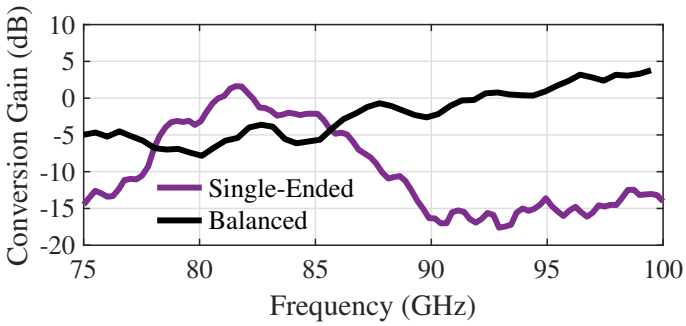
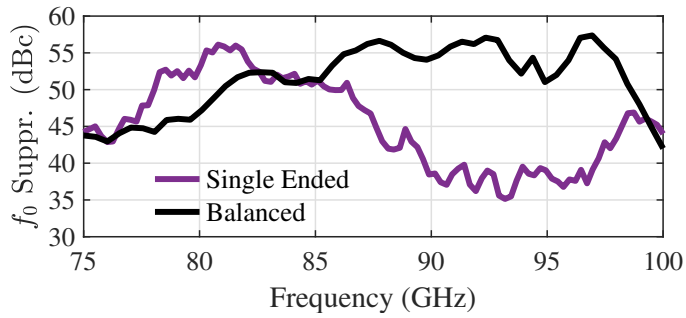


Figure 5.13: Schematic of the large-signal test setup. The output of the HEMT is measured with the spectrum analyzer and W-band power meter separately. 2.4 mm cables are used for all the connections of the driving test equipment, while WR-10 or WR-8 waveguide is used to connect the output probe to the waveguide power meter.



(a)



(b)

Figure 5.14: (a) Measured conversion gain of both the single ended and balanced frequency doublers shown across the output frequency band at an input driver of 10 dBm. (b) Fundamental suppression for both the single-ended and balanced topology plotted over the output frequency spectrum at an input drive of 10 dBm.

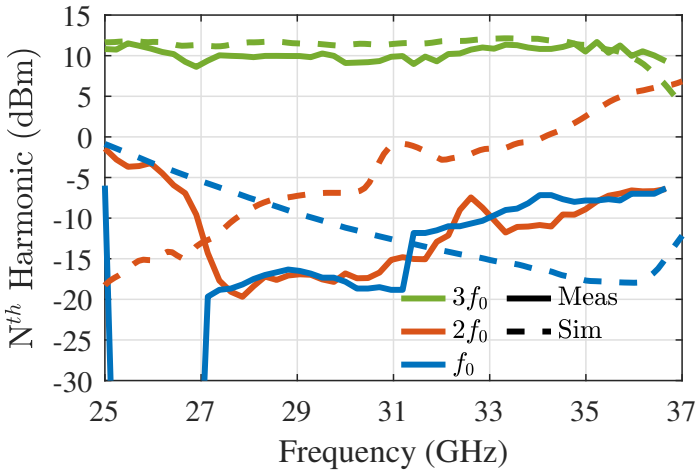


Figure 5.15: Measured and simulated 1^{st}, 2^{nd} and 3^{rd} harmonic of the balanced tripler shown over the fundamental frequency range of 25 to 36.6 GHz. All the measurements and simulation are done at an input power of 19 dBm.

band conversion gain. The W-band GaN doublers are compared to other active multipliers in the same frequency range in Table 5.2. To the best of the authors' knowledge, this is the first demonstration of GaN MMIC W-band doublers with conversion gain.

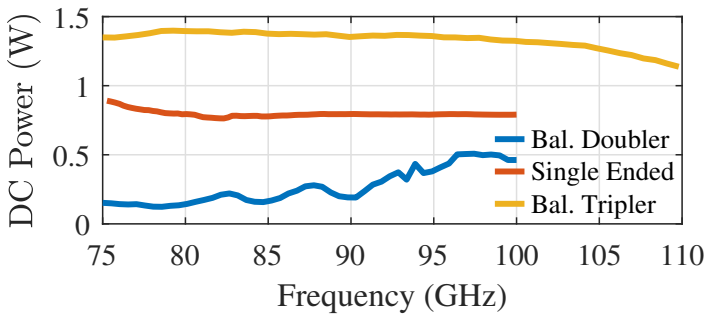


Figure 5.16: Measured DC power consumed by the single ended doubler, balanced doubler and balanced tripler shown over measured output frequency.

The single-ended and balanced doubler have similar performance in suppressing the fundamental. The post-amplifying HEMT along with the output matching network provide excellent fundamental suppression of over 35 dBc over the entire output band and over 50 dBc over 78 to 87 GHz. A combination of the two doubling topologies would likely achieve best conversion gain and fundamental suppression. A multiplier circuit arranged in a balanced configuration with a post-multiplication amplifier benefits from the power-combining providing increased output power and the post-amplification providing additional second harmonic power and fundamental suppression. The contributions of this chapter are reported in [89].

Table 5.1: Comparison of Transistor Frequency Multipliers

Type	Technology	N	Output Freq	Conv. Gain
Diode	-	-	-	-
[90]	GaAs Schottky	x2	93-95 GHz (sim)	-6.5 dB
[91]	GaAs Schottky	x2	75-80 GHz	-16 dB
[92]	GaAs Schottky	x2	80-84 GHz	-4 dB
[110]	GaAs Schottky	x2	70-78 GHz	-5 dB
[93]	GaAs Schottky	x2	70-78 GHz	-5 dB
[111]	GaAs Schottky	x2	67-78 GHz	-6.6 dB
[93]	GaAs Varactor	x2	92-95 GHz	-11 dB
[95]	GaAs	x2	50-128 GHz	-12.5 dB
[112]	GaAs	x2	50-128 GHz	-12.5 dB
[94]	nMOS	x2	93-123 GHz	-34 dB
Transistor	-	-	-	-
[102]	GaAs mHEMT	x8	78-100 GHz	8.9 dB
[102]	GaAs	x12	84-101 GHz	2.5 dB
[113]	GaAs pHEMT	x2	75-88 GHz	2 dB
[100]	InP HBT	x2	83-104 GHz	-4.5 dB
[105]	GaAs pHEMT	x2	68-80 GHz	-4 dB
[105]	GaAs pHEMT	x3	69-84 GHz	-4.3 dB
[105]	GaAs pHEMT	x4	74-78 GHz	-7.5 dB
[104]	GaAs mHEMT	x4	92-96 GHz	6 dB
[114]	GaAs mHEMT	x12	77-106 GHz	3.8 dB
[106]	GaAs pHEMT	x2	85-110 GHz	3.2 dB
[103]	GaAs mHEMT	x6	78-104 GHz	6 dB
[107]	GaAs pHEMT	x2	88-99.5 GHz	-4.3 dB
[109]	GaN HEMT	x2	75-78.5 GHz	-5 dB
[101]	InP DHBT	x2	DC-86 GHz	-3 dB
[99]	CMOS	x8	84-98.4 GHz	-7.12 dB
[96]	SiGe BiCMOS	x8	100-140 GHz	15 dB
[115]	GaAs mHEMT	x8	86.4-91.2 GHz	4.5 dB
[98]	CMOS	x9	88-99.5 GHz	-5.7 dB
[97]	SiGe BiCMOS	x4	70-110 GHz	10 dB

Table 5.2: Comparison of W-band GaAs and GaN HEMT Frequency Multipliers

Freq. (GHz)	Device Technology	$P_{in}(f_0)$ (dBm)	Max $P_{out}(2f_0)$ (dBm)	Conv. Gain (dB)	Max f_0 Supp. (dBc)	P_{DC} (mW)	Year Ref.
95-108	GaAs mHEMT	n/a	1.8 dBm	n/a	15 dBc	50	2020 [125]
68-80	0.15 μm AlGaAs/InGaAs/GaAs pHEMT	10 dBm	6 dBm	-4 dB	20 dB	n/a	2001 [105]
75-100	0.13 μm AlGaAs/InGaAs/GaAs pHEMT	13 dBm	15 dBm	2 dBm	45 dBc	n/a	2004 [126]
92-96	130 nm GaAs mHEMT	n/a	11 dBm	6 dB (chipset)	n/a	(sim only)	2019 [104]
78-100	100 nm InAlAs/InGaAs mHEMT	n/a	-1.5 dBm	n/a	23 dBc (chipset)	280	2011 [102]
84-101	100 nm InAlAs/InGaAs mHEMT	n/a	6.9 dBm	n/a	20 dBc (chipset)	600	2011 [102]
85-110	0.1 μm GaAs pHEMT	5 dBm	8.2 dBm	3.2 dB	37 dBc	56	2014 [106]
88-99	0.15 μm GaAs pHEMT	n/a	7.1 dBm	-4.2 dB	28 dBc	110	2019 [107]
75-78.5	100 nm AlGaN/GaN on s.i. HEMT	12 dBm	10 dBm	-5 dB	n/a	80	2011 [109]
77-86	**40 nm AlGaN/GaN HEMT**	**10 dBm**	**11.5 dBm**	**1.5 dB**	**55 dBc**	900	**This work**$^{+}$
86-100	**40 nm AlGaN/GaN HEMT**	**10 dBm**	**13.8 dBm**	**3.8 dB**	**55 dBc**	500	**This work***

$^{+}$ Single ended topology
* Balanced Topology

Chapter 6

Integrated T/R Half-Duplex W-band GaN MMIC

Contents

Individual MMIC components generally serve one purpose and have limited functionality on their own. Millimeter-wave systems require multiple connected circuits to achieve transmit and receive operation. The inter-connects between these circuits may be realized in different levels from fully packaged waveguide ports to inter-MMIC wire bonds or flip chip all the way down to on-chip integration. Integrating multiple circuits on a single MMIC holds several advantages including smaller footprint and eliminating lossy interconnects. This chapter covers the integration of the various active and passive circuits discussed in the previous sections in to an on-chip switched T/R front end.

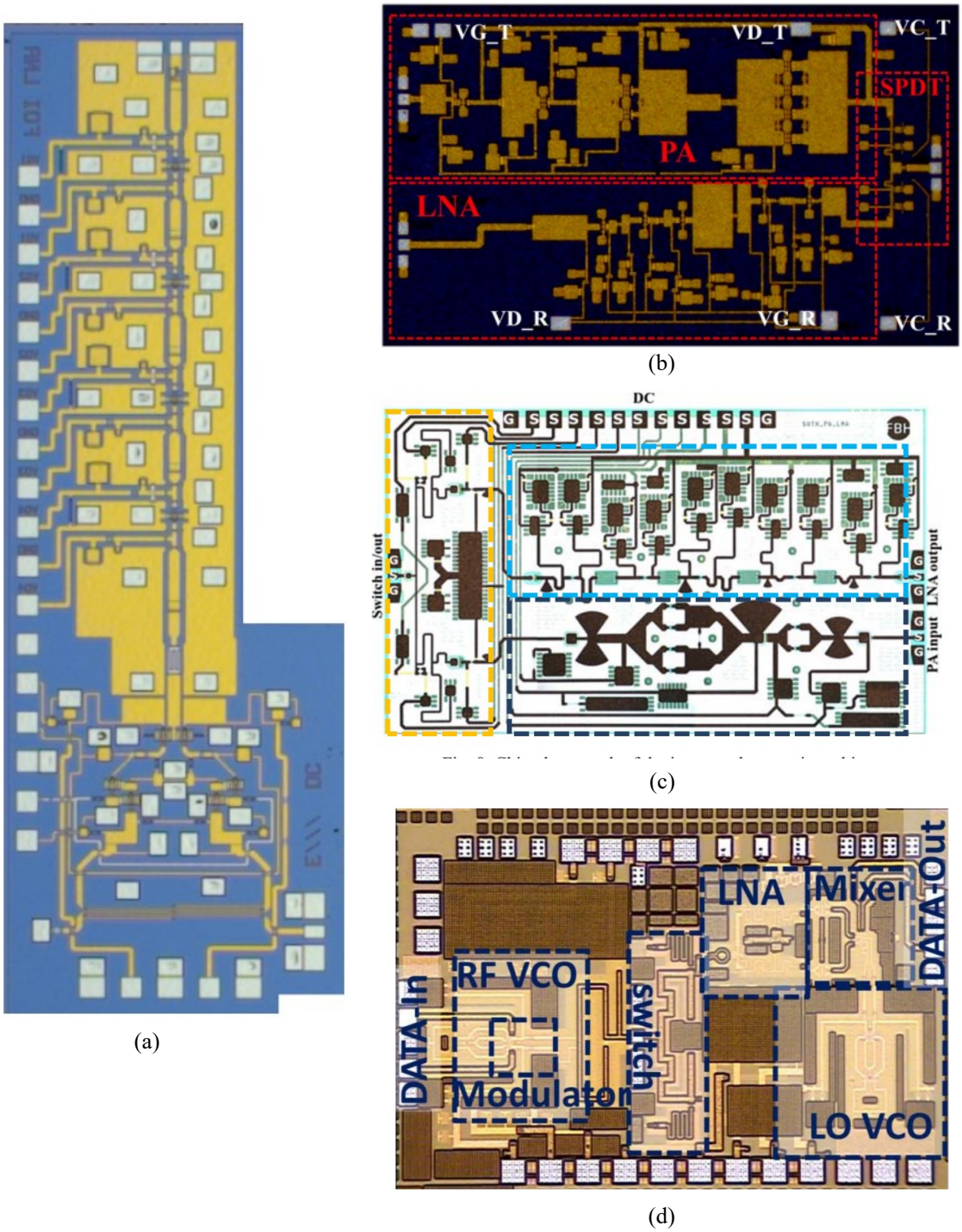
6.1 Background

Typically, front end T/R modules are assembled from several separate LNA, PA, SPDT switch chips as shown for example in GaAs at W-band [127], requiring multi-chip packaging. Generally, silicon processes have demonstrated higher integration levels with lower output powers. For example, a fully-integrated 77 GHz automotive radar in 65-nm CMOS demonstrated 6.4 dBm of output power and 23 dB of small signal gain on the receive path with a noise figure (NF) of 14.8 dB [128]. In [129], using 90-nm standard CMOS, a 77 GHz automotive radar with 6.3 dBm output power and an LNA with NF = 6.8 dB is shown. A SiGe HBT single-chip receiver was demonstrated over 75-100 GHz with a conversion gain of 6 dB and NF = 10 dB [15]. GaAs single-chip front ends have existed at W-band since the 1990s [130], [131]. An InP T/R chip fabricated in a 0.8-μm InP-DHBT technology showed a switch that compressed at 15 dBm and with the transmit PA with 16 dBm saturated output power at 18% efficiency, while the receive LNA showed 30 dB gain with NF <9 dB [14]. Several front end MMICs in V and W-band have been realized in GaN: a 71-77 GHz T/R MMIC with a saturated output power of 30.6–31.5 dBm and NF = 4.7–5.5 dB with 18–20 dB receive gain is demonstrated in [13]; and W-band heterodyne receivers fabricated in a 60-nm GaN-on-Si process are presented in [12]. Figure 6.1 summarizes these published integrated front ends.

Recently, there has been increasing interest in STAR or true full duplex, but this is still an area of active research (cite kens book). Current T/R front ends use freuqnecy separation when simultaneously transmitting and receiving (eq. in cellular or sattalite) or time domain separation with half-duplex switching between T/R. The former does not use the spectrum efficiently and needs expensive diplexers. The latter is useful in radar as were in comms but limits capacity. At W-band the absolute BW is large, so TDM can still have high data through-put. The reward of this chapter discusses single-chip t/r (half-duplex) front end.

6.2 W-band switched T/R module

A single-chip transmit-receive (T/R) front end covering (70-110) GHz is implemented. The transmit path consists of the balanced power amplifier and the single-HEMT driver presented in Chapter 2. The receive



(a)

(b)

(c)

(d)

Figure 6.1: Published W-band front ends in (a) W-band heterodyne receiver MMIC in a 60 nm GaN-on-Si process (OMMIC). NR of 4.4-5.5 dB at 90-95 GHz with s 0-7.4 dB/0-6.4 dB at 75-91 GHz when the LO/2 power is 20.5 dBm (IF=5 GHz/2 GHz) 3.68x1.19mm^2 [12] (b) 71-77 GHz switched on chip front end implemented in a 130 nm 18 V drain bias Gan on SiC process. 4.3 x 2.5mm^2 footprint noise figure >5.5 dB >1 W output power [13] (c) W-band switched front end in 80 nm InP-DHBT process. 16 dBm saturated output power at 90 GHz. >9 dB of NF with >30 dB small signal gain from 75-110 GHz. 2.5x1.5mm^2 [14] (d) Entire radar receiver front end integrated in a 90 nm SiGe process (Global Foundries SiGe 9HP) 75-110 GHz 10 dBm NF 6 dB conversion gain 2.2x1.4mm^2 [15] .

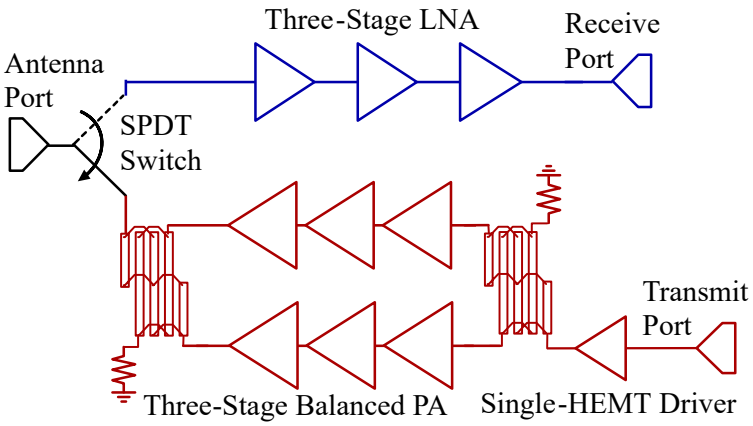


Figure 6.2: Block diagram of the switch T/R front-end with labled individual components.

path consists of the three stage low-noise amplifier also discussed in Chapter 2. The SPDT single-HEMT shunt switch from Chapter 3 selects either the transmit or receive paths creating the half-duplex operation. A circuit schematic diagram of the front end is shown in Fig 6.2.

6.2.1 Integrated SPDT Switch Design

The single-pole double-through (SPDT) switch between transmit and receive paths is a quarter-wave shunt topology, chosen for a good tradeoff in insertion loss and isolation. In contrast, a single-shunt switch has lower isolation, while a double shunt topology has higher insertion loss [79]. The SPDT switch integrated into the T/R MMIC is discussed in detail in Chapter 3 and is designed at a center frequency of 92 GHz. When the switch HEMT is biased to conduct, the resulting short is transformed to an open through a quarter-wave transmission line thus creating the OFF-state of the switch. Turning on the switch path requires fully pinching off the shunt HEMT, thereby eliminating the shorted signal path. The HEMT then acts as a capacitor loading the line and is compensated for with inductive stubs at the drain of the device which also provides a ground path.

The switch demonstrated in Chapter 3 is slightly modified for connection between transmit and receive paths. Figure 6.3(a) shows the separate SPDT switch circuit with GSG probe pads on each port used to measure the performance prior to including it in the T/R MMIC design. Shown in Fig. 6.3(b) is the modified switch implemented in the presented front end. A comparison of the simulated performance between the

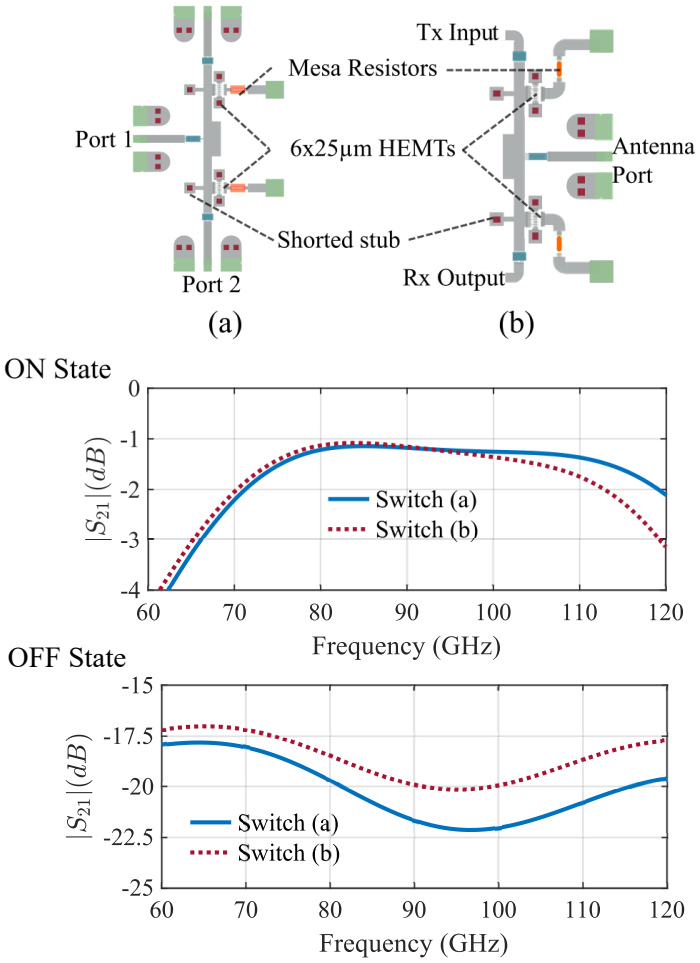


Figure 6.3: Layout of (a) SPDT switch with GSG pads from (cite switch paper) and (b) modified layout of SPDT switch used for FE MMIC. Below plots of the (a) SPDT on and off state S21 measured and simulated S parameters and measured output power handling are shown in the top and bottom plots respectively.

two switches is shown in the two plots in Fig. 6.3. In the modified version, the transmit and receive ports are bent to fit with the rest of the circuit in Fig. 6.2. The slight degradation in performance can be attributed to the longer lengths of line de-tuning the match and causing more loss at the higher end of the band.

6.2.2 Integrated Power Amplifier

To maximize output power and gain, the three-stage balanced amplifier topology is driven with the single-HEMT driver, both individually discussed in Chapter 2. These cascaded power amplifiers compose the transmit power amplifier. The balanced topology is resilient to changes in input and output load impedance which can occur in, e.g., phased array antennas as the beam is scanned. The driver stage aids in saturating

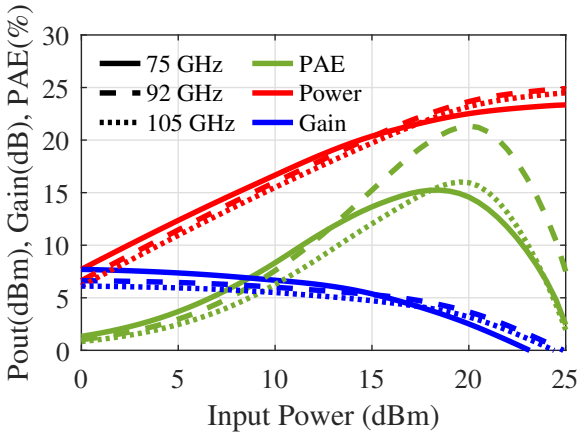


Figure 6.4: Simulated output power, gain and PAE of the single-HEMT driver plotted over an input power of 0-25 dBm for three different frequency points corresponding to the middle and edges of the oeprating band: 75, 92 and 105 GHz.

the balanced power amplifier, which requires 3 dB more input power than the single-ended branch PA. The addition of a driver also reduces the input power requirements facilitating measurements and integration.

The separate multi-stage balanced power amplifier is validated prior to integration in the T/R MMIC as described in detail in Chapter 2. Briefly, two three-stage amplifiers with a 1:2:3 staging ratio are power combined using two Lange couplers. To achieve this staging ratio two HEMT devices sizes are used: 4×25 μm and 4×37.5 μm. The third stage combines two 4×37.5 μm HEMTs with a quiescent drain current of 60 mA. The highest measured output power is 26.7 dBm at 77 GHz, and the peak power added efficiency (PAE) around 14.8 % at 95 GHz.

To fully compress the balanced PA and reach peak power, a driver amplifier is integrated on chip. Designing the driver power amplifier requires several considerations. First, the output of the amplifier must be well matched to the 50-Ω input impedance of the balanced PA. At the input, the driver PA needs to handle reflections from the input connection. Since the balanced PA covers all of W-band, the driver should have a minimum bandwidth equal to the balanced PA with sufficient gain. In order to simplify biasing of the entire transmit side of the T/R MMIC, the driver is biased at the same gate and drain voltage as the balanced PA.

Designing the driver power amplifier requires several considerations. First the output of the amplifier must be well matched to 50Ω as that is the input impedance of the balanced PA. The driver PA is directly connected to a transition in a module or system and thus should also be able to handle reflections occurring

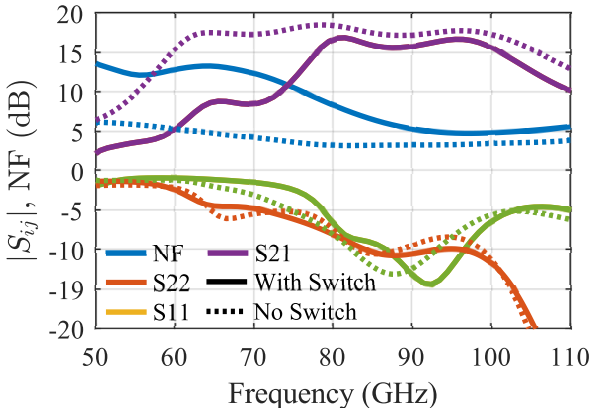


Figure 6.5: Simulated S-parameter and noise figure performance of the receive LNA shown for two cases: with and without the SPDT shunt HEMT switch connected to the input.

from those connections. Since the balanced PA covers all of W-band, the driver will have to be equally as wide-band. In order to simplify biasing of the entire transmit side of the FE, the driver should be biased at the same gate and drain voltage as the balanced PA.

6.2.3 Integrated LNA Design

The individual LNA in the front end is discussed in detail in Chapter 2 but will be briefly summarized here for context. Biasing at 0 V on the gate and 6 V on the drain of the HEMT corresponds to a quiescent drain current of 12 mA. This bias is chosen to maximise gain while adding the lowest noise possible. Similarly to the case of the driver PA on the transmit side, the biasing of all of the stages of the LNA are kept to the same bias to facilitate external biasing in a module or system.

Since both the input of the LNA and switch ports are designed to be 50 Ohms, the circuits are directly connected on-chip. Simulations of the LNA with and without the switch connected to the input are shown in fig. 6.5 and show the degradation of performance when the switch is attached to the LNA input. Loss before the LNA amplification begins will directly increase the noise of the receive path but is unavoidable in this front end architecture.

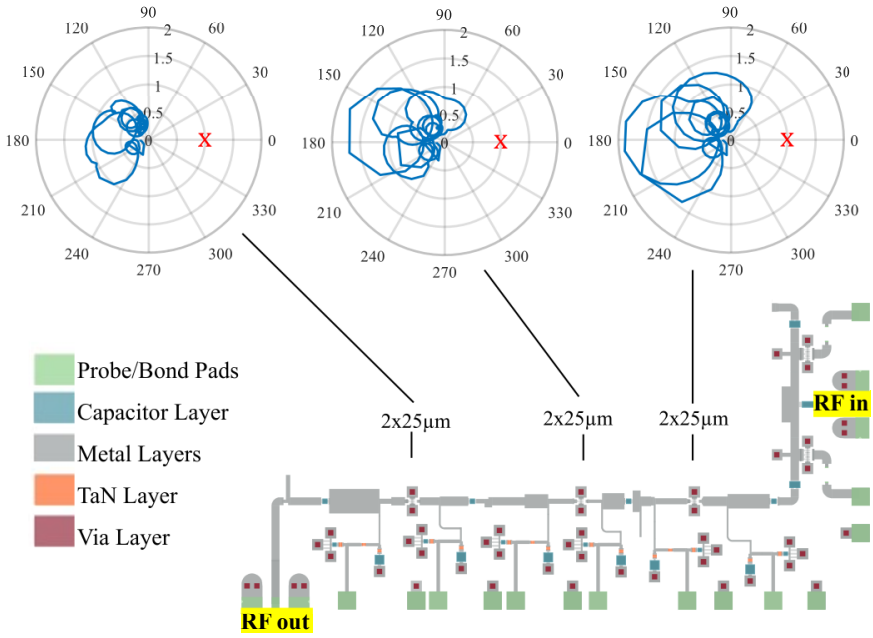


Figure 6.6: Loop gain stability analysis shown for each individual 2x25 um HEMTs of the three stage LNA with a layout of the LNA connected to the SPDT HEMT switch. The traces shown indicate the worse case input and output impedance of the three-stage LNA. The red X denotes the point of instability.

6.2.4 Stability of Combined Active Circuits

With several active circuits consisting of many HEMT devices operating at millimeter-waves, stability must be carefully analyzed for each individual HEMT starting from dc up to and past the cutoff frequency. Since the active circuits are all connected through a switch, possible reflections can occur between the T and R paths. For this reason, careful stability analysis is done across a wide range of impedances and bias conditions. For example, the SPDT switch is not an active device, but does operate with a biased HEMT and therefore could present variable impedances to both the transmitting PA and receiving LNA.

Loop-gain and Nyquist stability analysis are conducted throughout the design (from linear elements to full-wave EM). The loop-gain analysis of the LNA is shown in Fig. 6.6 for each of the three stages with a layout diagram of the circuit for reference. Even though these devices do not have gain past the second harmonic, stability is considered from 0 to 330 GHz, or the third harmonic of the highest in-band frequency component. Stable operation is shown across this range as denoted by the red X.

Since the balanced amplifier stability has already been considered for a range of input and output

impedances [9], the driver stability is emphasized in the integrated design. Off-chip capacitors and bond-wire connections are modeled both as linear circuit elements, as well as full 3D EM structures, and these models then used in stability simulations. Custom linearized HEMT models of the 2×25 μm, 4×25 μm and 4×37.5 μm HEMTs are extracted at the design bias and drive levels from available foundry Angelov models. These linear models allow process variations to be taken into account by varying the HEMT trans-conductance (±30%), drain-to-source capacitance (±30%) and gate-to-drain capacitance (±30%). This step ensures that even with the largest possible process variations, the amplifiers remain stable. All active HEMTs in the amplifiers have a phase margin of greater than 60° in each of their loop-gain simulations across swept input and output port impedances.

6.3 Measurement Setup and Results

The MMIC characterization is conducted on-wafer. Both small-signal and scalar large-signal measurements are performed with a Summit 9000 probe station, while noise measurements are conducted on a separate probing setup described below.

6.3.1 Small-Signal Chracterization

An HP8510C VNA with V- and W- band frequency extenders is used for on-wafer small-signal measurements. Two 100 μm GSG probes bring the measurement plane from the frequency extenders to the DUT. Calibration up to the plane of the DUT is done using a W-band impedance standard substrate (ISS) from Cascade Microtech. The front end MMIC is then measured in both transmit and receive operation. Both sides are biased through an off-chip bias network ladder composing of several MIM capacitors connected through bond wires. Measurement results compared to simulations are shown in Fig. 6.7 for the transmit path and in Fig. 6.8 for the receive path. Note the measurement discontinuity at 75 GHz arising from two different wave-guide band measurements.

For the transmit path, the peak small-signal gain is 25 dB at 75 GHz sloping down to 19 dB at 108 GHz. The receive path shows a peak small-signal gain of 22 dB at 77 GHz with over 16 dB gain from 70–105 GHz.

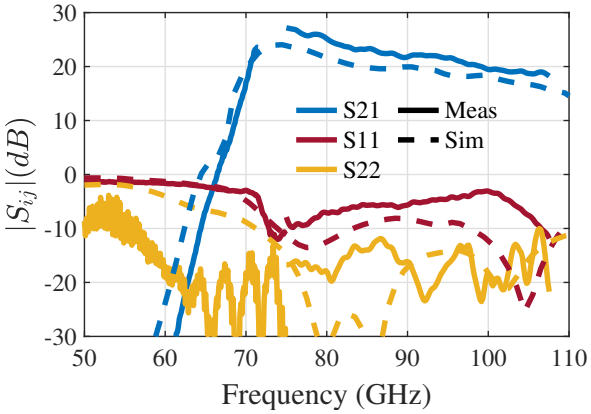


Figure 6.7: Measured and simulated S-parameter performance of the front end transmit path across 50–110 GHz when all stages of the balanced amplifier and driver stage are biased at $V_g = 0.25$ V and $V_d = 12$ V with a resulting total drain current of 250 mA. The switch in the transmit path is turned on with the HEMT gate biased at -10 V while the other switch path is turned off at a HEMT gate bias of 0 V

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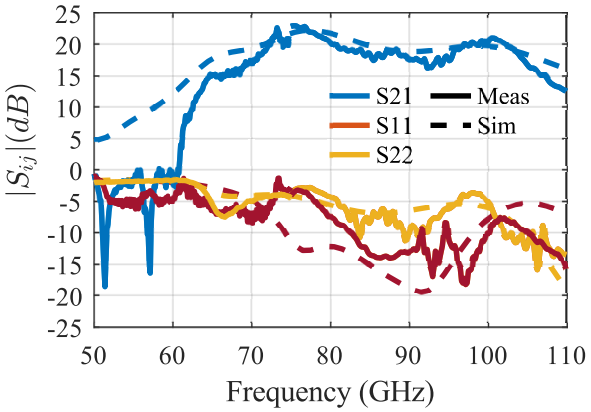


Figure 6.8: Measured and simulated S-parameter performance of the front end transmit path from 50–110 GHz when all the stages of the LNA are biased at $V_g = -0.6$ V and $V_d = 6$ V with a resulting total $I_d = 47$ mA. The SPDT switch on the receive path is fully turned on with a -10 V control voltage and the other SPDT switch path is turned off at 0 V.

The measured and simulated $|S_{21}|$ agree within 1.5 dB across the entire W-band. The simulated and measured results in the transmit path deviate more, especially below 70 GHz, since this path was designed for best large-signal gain.

6.3.2 Noise Figure Measurements

On-wafer 50 Ω noise figure (NF) measurements were collected on the LNA using a custom scalar NF test bench. The MMICs are probed on an MPI TS200 probe station with GGB WR-10 100 μm pitch probes. A QuinStar WR-10 noise diode is connected to the input RF probe through a 90° WR-10 bend, and the output RF probe is connected to a noise receive chain through a WR-10 S-bend. The noise receive chain is comprised of a commercial LNA, a mixer down converter, a local oscillator (LO) up-converter with a commercial 6× frequency multiplier, and an Agilent E4448A spectrum analyzer with noise figure measurement application. The LO is driven by a Keysight MXG N5183B signal generator. The NF measurements are calibrated to the WR-10 noise diode / WR-10 receive chain reference planes by directly connecting the components and calibrating with the proper noise diode excess noise ratio. Then, the cascaded NF measurement of the input fixture, LNA, and output fixture are measured. Finally, the NF of the LNA is determined by Friis formula with the transducer gain and NF of the fixtures calculated from their respective S-parameter measurements, while the transducer gain of the LNA is calculated from a calibrated S-parameter measurement. The S-parameters of the WR-10 probes are determined with a two-tier calibration. This approach neglects the impedance mismatches between the different reference planes in the cascaded DUT, which is a reasonable approximation for a matched MMIC. A photo of the on-wafer NF measurement test bench is reported in Fig. 6.9.

Due to the setup mentioned above, only measurements at 80, 85, 90, 95, 100 and 105 GHz are conducted. The measured NF is higher than predicted by the model, shown in Fig. 6.5. Measured NF of the receive path are shown on Fig. 6.10 along with de-embedded NF of the LNA alone, based on measured switch loss from [16]. The measurements show a minimum NF of 5.2 dB at 80 GHz and a peak NF of 7.8 dB at 100 GHz. These results are consistent with measured noise parameter data of individual millimeter-wave GaN HEMTs [72].

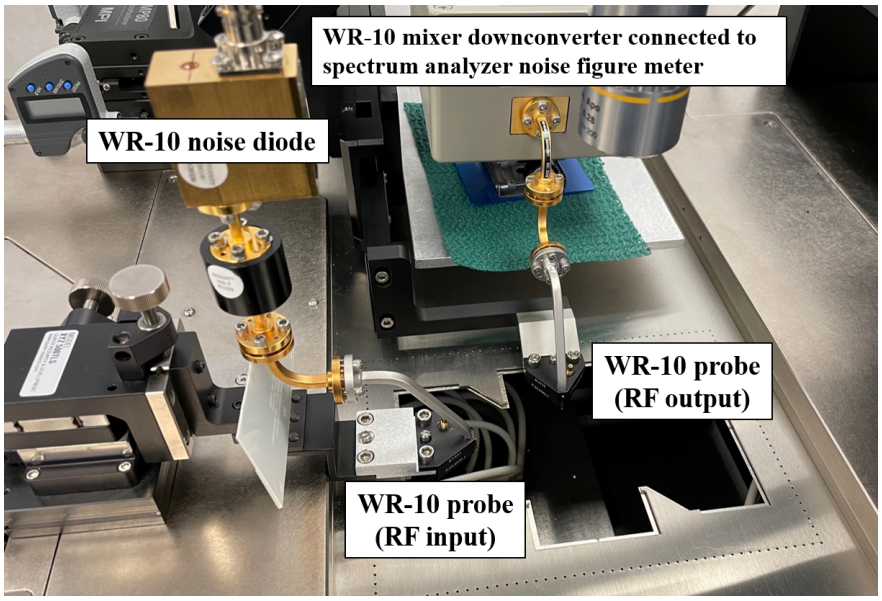


Figure 6.9: On-wafer NF measurement test bench used to characterize the W-band MMIC receive path.

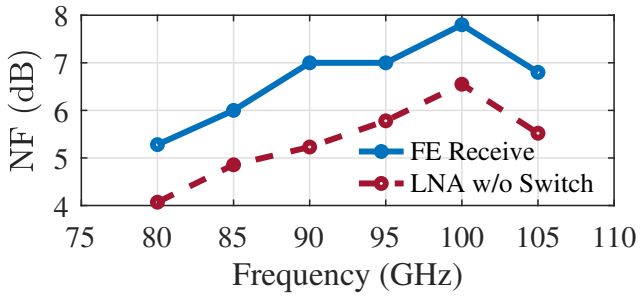


Figure 6.10: Measured NF of front end receive chain plotted over frequency shown along with a de-embedded NF of the LNA without the switch using measured results from [16].

6.3.3 Large-Signal Characterization

On-wafer large signal measurements are conducted with a power-calibrated scalar test bench. To reach up to 20 dBm of power at the DUT, a custom W-band solid-state PA is driven by a QPI-W01820-H4W02 W-band power amplifier. Isolators are used between the solid-state amplifiers for protection, but add ~ 1.5 dB of loss. An HP83650A sweeper generates a 25-36.6 GHz CW signal. After this, a Ka-band QPW-18402020-J0 power-amplifier drives a passive QPM-93003W diode tripler followed by a QFL-B4SW00 low-pass filter to provide an up-converted 75–110 GHz CW signal to the W-band test-bench power-amplifiers.

The W-band test-bench amplifiers are connected to the 100 μm input GSG probe through several standard

straight waveguide sections and a 20 dB WiseWave coupler. On the output of the DUT, a 20 dB coupler, terminated wave-guide attenuator and the WR-10 GSG probe complete the scalar measurement setup. W-band power meters attached to both 20-dB couplers are used to measure and calibrate the large-signal setup, using VNA-measured losses of all the passive interconnecting components.

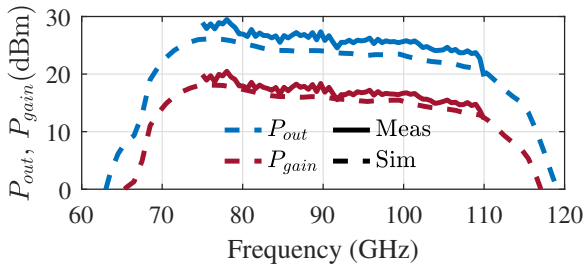
Two separate large signal measurements are conducted on the transmit branch of the MMIC. The custom solid-state PA operates in the 90–95 GHz band and is used to conduct single frequency power sweeps at 92 GHz providing 0 to 20 dBm at the plane of the DUT. The QPI-W01820-H4W02 W-band power amplifier operates from 75-110 GHz and is used to measure large-signal performance across the entire W-band at a power of 9 dBm at the DUT.

An output power of >29 dBm at 75 GHz gently sloping down to 24 dBm at 108 GHz is measured at an input power of 9 dBm. These results along with the large-signal gain of the transmit side are shown in Fig. 6.11(a) along with simulated results. The measurement of the 0–20 dBm power sweep at 92 GHz is shown in Fig. 6.11(b).

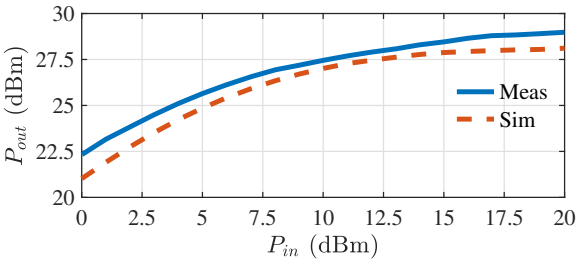
The measured current draw of the transmit path is plotted over frequency in Fig. 6.12 and compared to simulation. Over 75–110 GHz, the dc drain current ranges between 580 and 650 mA. Since the bias point is fixed to a single drain and gate voltage for the entire transmit path, each of the PA stages may not compress to the optimal level. This results in some disagreement between simulation and measurement.

6.4 Chapter Summary

In summary, the integration of a power amplifier with a driver, SPDT switch and LNA is demonstrated on a single GaN-on-SiC 5 mm×3 mm die that operates over the entire W band (75–110 GHz). The transmit path consists of a three-stage power combined balanced amplifier with a single-HEMT driver. An SPDT switch using a quarter-wave shunt HEMT topology is used as the connection between the antenna port and the PA output and 29 dBm of output power is measured at the output of the switch at the 92 GHz center of the band. Including the switch loss, the receive path with a 3-stage LNA demonstrates a noise figure that ranges from 5.2–7.8 dB across the band, with 15–22 dB gain. The switch does not show compression at peak PA output



(a)



(b)

Figure 6.11: (a) Measured and simulated output power and power gain of the front end transmit path at an input power of 9 dBm. (b) Measured output power compared to simulation of the MMIC at 92 GHz with 0–20 dBm input drive.

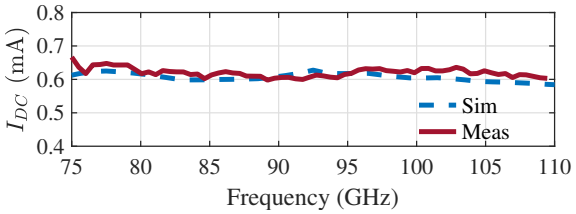


Figure 6.12: Measured compared to simulated DC current draw of the large signal measurement over frequency of the transmit branch of the front end. Data taken from same measurement as Fig 6.11.

power. The results from this Chapter are reported in [73], [16], [75] and [74].

The demonstrated performance is suitable for use in communications, radar and sensing. For such applications, the presented front end chip T/R module can also be assembled heterogeneously with other technologies to complete the MMIC into a fully packaged module (MECA) [132]. For phased array applications, integration with phase shifters such as [133] can also be accomplished monolithically. Future work includes packaging the MMIC into a wave-guide module with antennas. Additionally, characterization of with modulated signals.

Chapter 7

Future Work and Summary

Contents

This thesis begins at the individual GaN HEMT level and demonstrates control circuits, frequency multipliers, LNAs, and power amplifiers at millimeter waves frequencies up to 110 GHz. A balanced PA with a single-HEMT driver is then integrated with a SPDT switch and LNA to create a single-chip T/R front end. Directions for future work from here include MMIC design of other front end components which were not covered such as oscillators, limiters, mixers and more integrated GaN MMIC circuits such as a radiometer or full duplex front end. Packaging of the designed MMIC chips is an area which has been explored but still needs to be expanded upon.

7.1 Future Work

Out of the 10 multi-project wafer (MPW) runs in the DARPA GaN Maturization program, that supported this thesis work, many circuits are left to be measured and integrated in future designs. MMICs that have been designed but not yet fully characterized are summarized below. MMICs must also interface with other

components in a system meaning that packaging is a necessary aspect of MMIC design. At millimeter waves, particularly above 50 GHz, a significant amount of package interface come in the form of wave-guide flanges. Directions for continuation of this work is detailed in several subsections below.

7.1.1 MMIC to Waveguide Transition

Packaging MMICs at millimeter waves requires transitioning the propagating wave from a microstrip quasi-TEM wave to a TE_{10} mode in a rectangular waveguide. Transitioning from a microstrip or CPW environment on-chip to a waveguide environment can be accomplished through several different methods. Many of these methods involve a transition probe printed on a microwave substrate or incorporated into the MMIC chip itself. This probe shapes the fields in a certain way in the metal confinement of the waveguide to propagate the wave with the lowest loss and least amount of reflections from the interface. A MMIC-to-waveguide transition is designed and fabrication of the probe is attempted. Figure 7.1 shows the design in a full wave EM simulator (HFSS) along with the simulated S-parameters from the microstrip port to the waveguide port. The design is created by depositing $>1\mu$m of gold on the front- and back-side of the 100μm thick Si04 (fused silica) substrate.

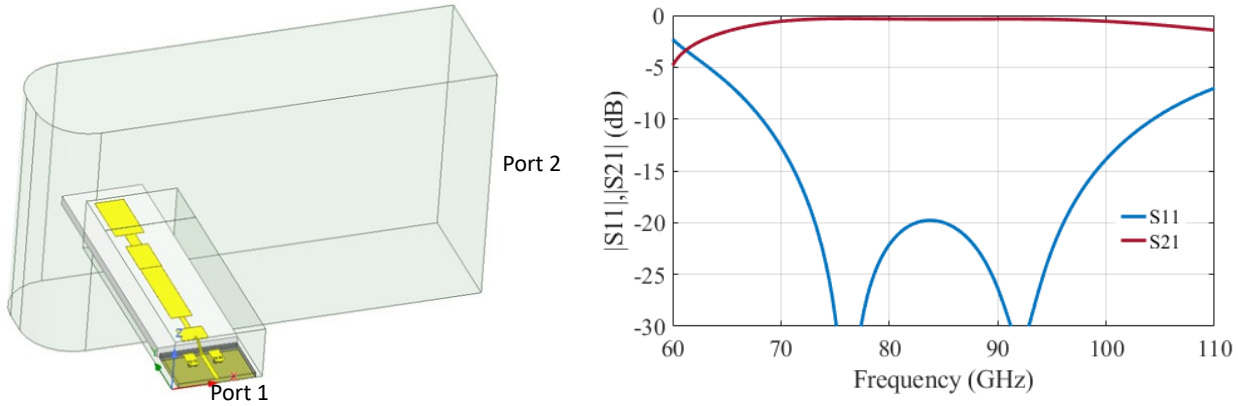


Figure 7.1: Simulation setup of the MMIC-to-waveguide transition using 100μm thick Si04 (left). The S parameter HFSS simulation from the labeled port (right).

The design shown in Figure 7.1 is the best case design considered if fabrication of the transition turns out perfectly. Incorporating tolerances from the fabrication and assembly processes involved is necessary to assess the resilience of the design to possible parameter changes. Important considered design parameters

from tolerances arising from fabrication, sub-dicing and metal machining include:

- Sawstreet dicing margin: 200-150 μm
- Metal Deposition margin: +/- 1 μm
- Bond wire variations (length and height): 2-3 μm
- Metal machining margin: 200-400 μm
- Spacing between MMIC and transition 30-70 μm

Sweeping these variables leads to a tolerance study shown in Fig. 7.2. The simple design of the transition itself leads to a robust design resilient to possible variations in fabrication and assembly. Bond wire variations account for the most change in performance and is also the hardest parameter to control if done by hand.

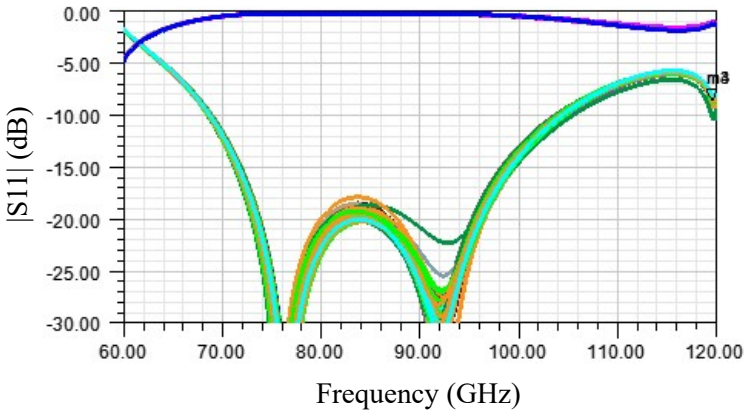


Figure 7.2: Tolerance study of the MMIC-to-waveguide transition from 7.1 showing variation of metal deposition, wafer sub-dicing, spacing between transition and metal encasing and metal machining of the WG cavity and feed.

For manufacturing, the MMIC-to-waveguide transition is tiled on a 3 inch wafer using CAD software, Fig 7.3. The design is then sent in to an experimental university foundry to be metalized. During the metalization process, the thin brittle wafer was cracked in several places. The deposited metal came out nonuniform as can be seen in Fig 7.4. As a result, measurements and further work were not possible. Directions for continuation of this work include choosing a different or thicker substrate and a change in the fabrication considerations and limits. Note that changing the substrate or the thickness of the substrate will require a redesign or significant modification of the current design.

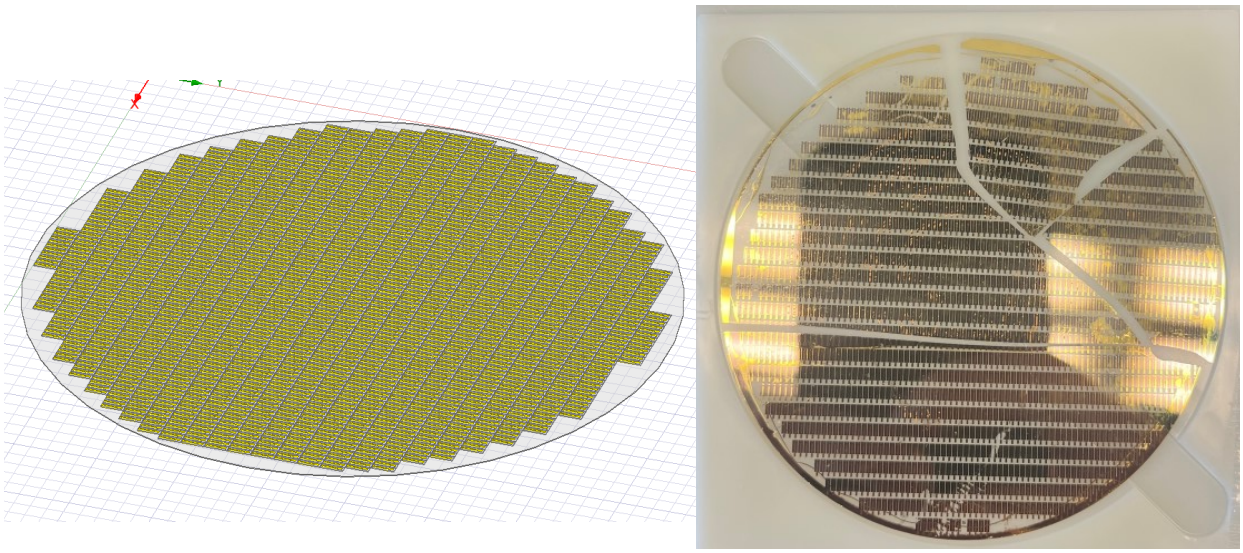


Figure 7.3: MMIC to waveguide transition wafer run CAD drawing and fabricated wafer which was cracked during processing.

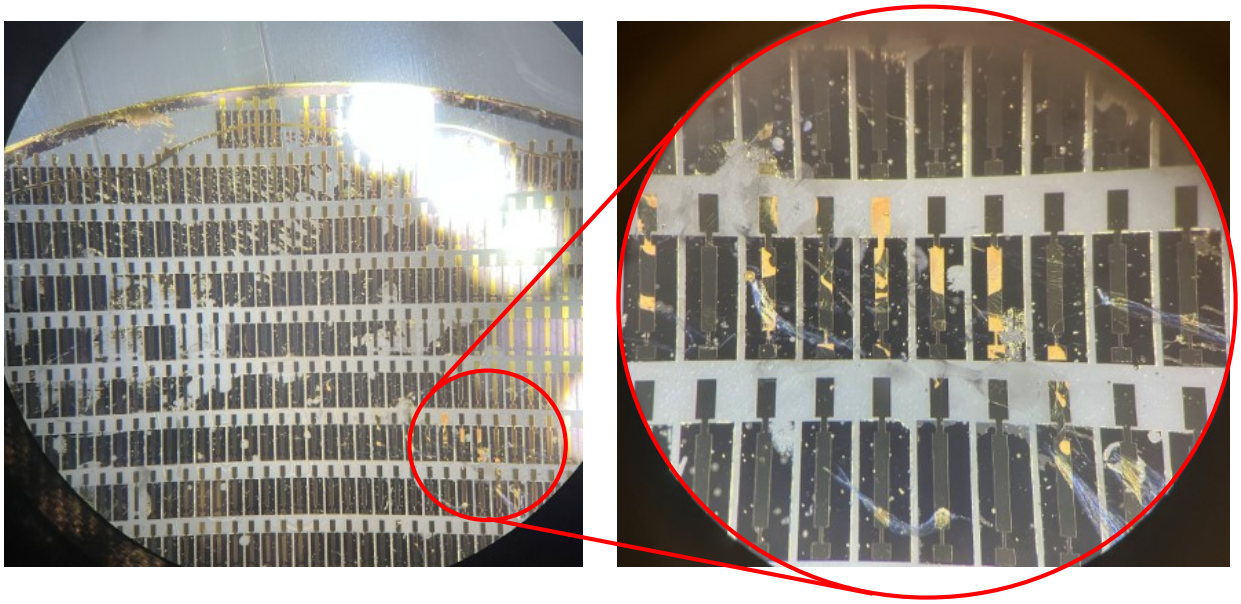


Figure 7.4: MMIC to waveguide transition wafer run top and backside metalization defects.

7.1.2 Split Block MMIC Packaging

At millimeter waves, waveguides provide the lowest loss environment and offer a standardized connection widely adopted in practice. Packaging of GaN circuits for W-band has been initiated for the front-end MMIC discussed in Chapter 6. The split block design can be seen in Fig 7.5 along with off-chip MIM caps next to

the bare die for stability and the dc biasing PCB. The design takes into account the mechanical tolerances from the available machine shops as well as from the dicing process of the MMIC-to-waveguide transition. Continuation of this work will involve tuning the design for new MMIC-to-waveguide transitions and the fabrication of the split-block package itself.

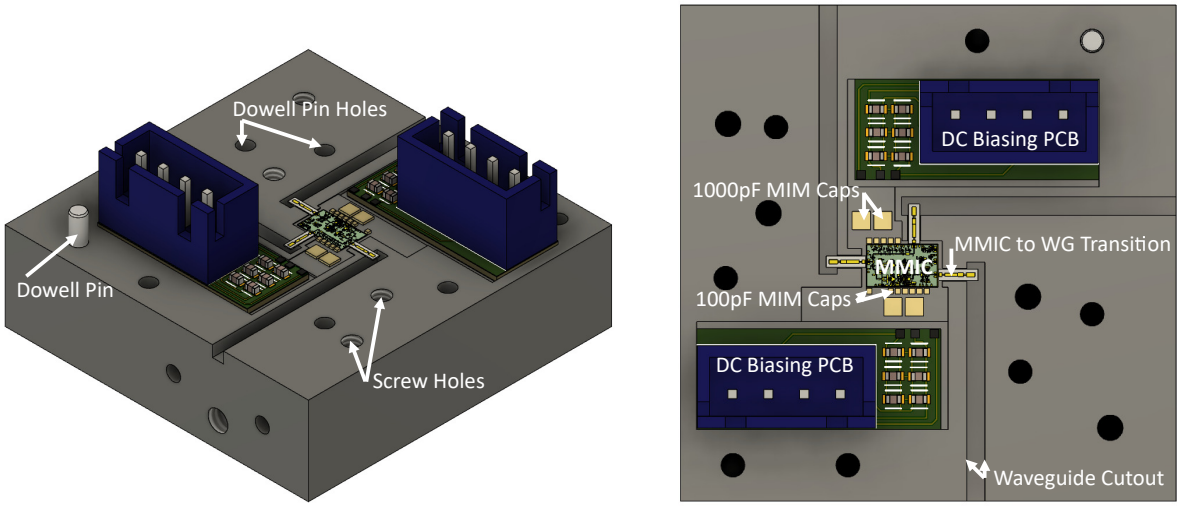


Figure 7.5: Split block package design of front end MMIC from Chapter 6 showing MMIC die, dowell pin, off-chip MIM capacitors, PCB biasing board and screw holes.

7.1.3 Biasing PCB for Packaged MMIC

To properly bias all the active components involved in the front end, a PCB with a PIN-header connection is designed to interface between the MMIC bare die and the dc power supply. The board is designed using CAD software and since the board is designed for dc, the PCB substrate was chosen based on price as RF performance is not necessary. The design of the board is done in parallel with the split-block enclosure in order to ensure all components fit into place. The layout of the board is shown in Fig. 7.6 along with a 3D view of the populated PCB. The PCB was designed to work for both the transmitting and receiving side of the front end MMIC. The PCB remains to be fabricated, populated and validated through measurements.

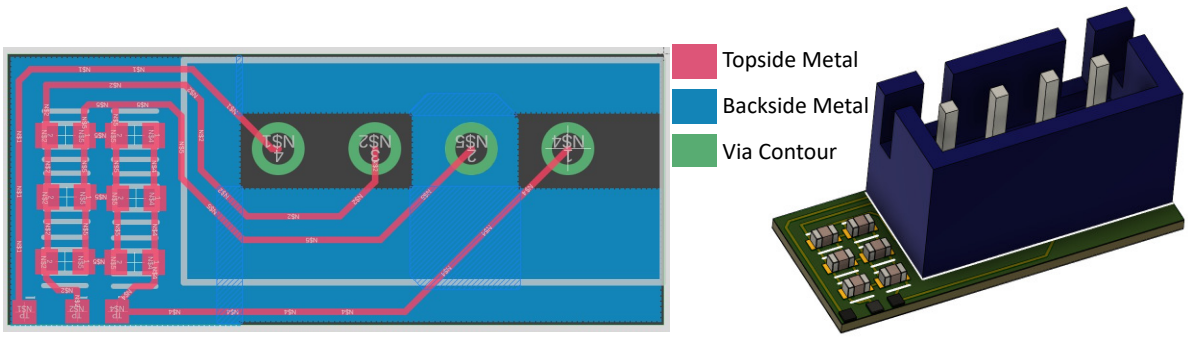


Figure 7.6: PCB Layout of the dc biasing board for the split block enclosure shown in Fig 7.5 and 3D view of the populated board.

7.1.4 Limiters

Used to protect the receiver in RF and microwave systems, a limiter is a control circuit which allows signals below a certain power level to pass through with low loss and attenuate the signals above a threshold power level. In particular, the limiter is commonly used to protect LNAs in radar as incoming pulses could damage the LNA which can only handle up to a certain amount of input power. Solid state limiters are often realized using diodes (Pin, varactor or Schottky) or transistors (amplifiers or switches). Amplifiers are inherently limiters as they saturate at a certain input power level and will reach a point where they do not output anymore power even as the input power increases.

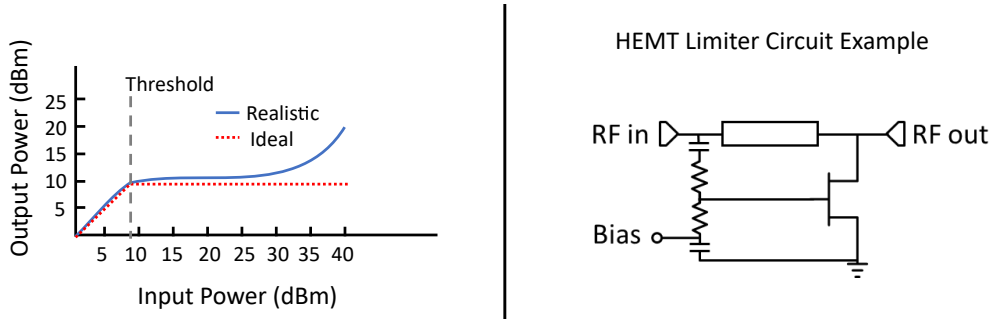


Figure 7.7: Plot representing the ideal and real or practical responce of a millimeter wave limiter circuit (Left). Circuit example of a MMIC HEMT limiter (Right) [10].

Shown in Fig. 7.7 is the ideal characteristics of a limiter as well as a more realistic performance adjustment. Also shown is an example of a possible MMIC circuit limiter topology. Using a HEMT to design a limitor is done by placing the HEMT in shunt with a matching line (50Ω) and connecting the gate bias in such a

way that the device turns on as the input power increases. At the threshold power level when the device has fully turned on, the input power will begin to reflect back and less power will flow through the circuit. Demonstration of this type of circuit remains to be shown in HRL T3 GaN at W-band.

7.1.5 GaN HEMT Oscillators and VCOs

Frequency generation is also explored in this research using GaN HEMTs. An oscillator circuit designed in the HRL T3 process at 44 GHz is shown with a measured spectrum in Fig 7.8 from [75]. Integration with frequency multipliers is a pathway to creating high power mmillimeter wave sources using GaN technology. Continuation of this work includes design of VCOs in single HEMT as well as other circuit topologies to be integrated into future front end MMICs.

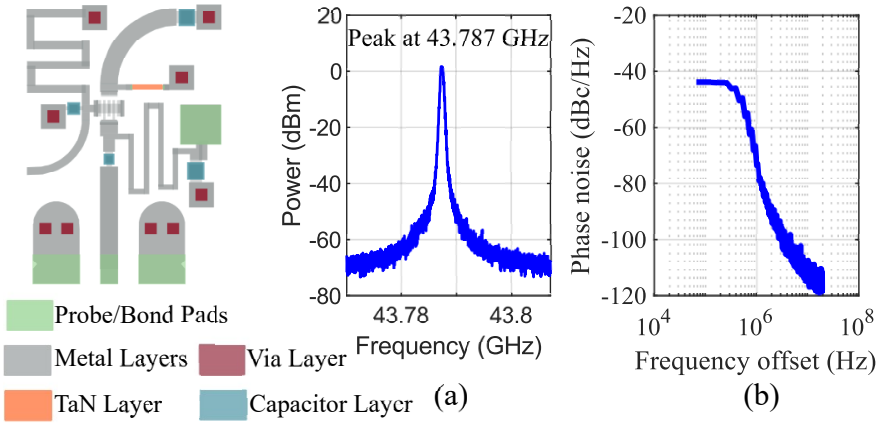
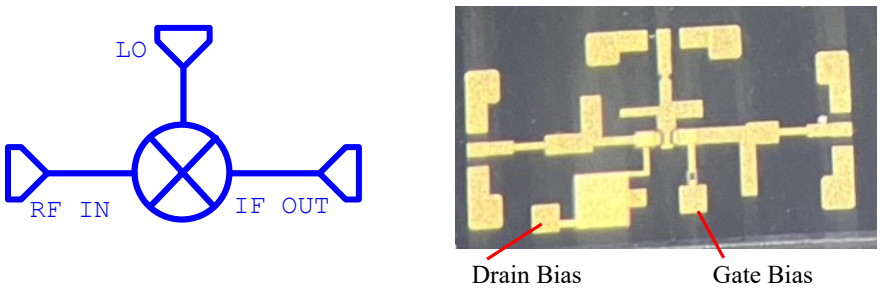


Figure 7.8: Fixed oscillator using a 4×37.5 μm HEMT at a 12 V drain bias. The gate of the device is shorted to ground through a resistor. Measured results using a HP8565E spectrum analyzer are shown: (a) power spectrum of the oscillator and (b) calculated associated phase noise.

7.1.6 GaN HEMT Mixers

Mixers are a frequency conversion component which can also be implemented in GaN HEMTs. This is demonstrated with a resistive HEMT design covering 75-110 GHz. Figure 7.9 shows a single-HEMT GaN mixer that was designed in HRL T3. This MMIC has not been measured or characterized. Continuation of this work involves large signal measurements and integration with other components such as oscillators to form heterodyne receivers.



(a) (b)

Figure 7.9: Schematic representation of a mixer with labeled ports (a) and a photograph of the fabricated single HEMT mixer (b).

7.1.7 W-band Dicke Radiometer

A full 75-110 GHz Dicke switched radiometer is designed and fabricated. A SPDT switch from Chapter 3 is integrated with a three stage LNA and power detector to form the radiometer. Switching the SPDT switch between the input port and a matched 50 Ω load allows the gain fluctuation calibration. The MMIC still needs to be measured and characterized. Figure 7.10 shows a photograph of the fabricated MMIC Dicke radiometer mounted on a CuMo carrier plate.

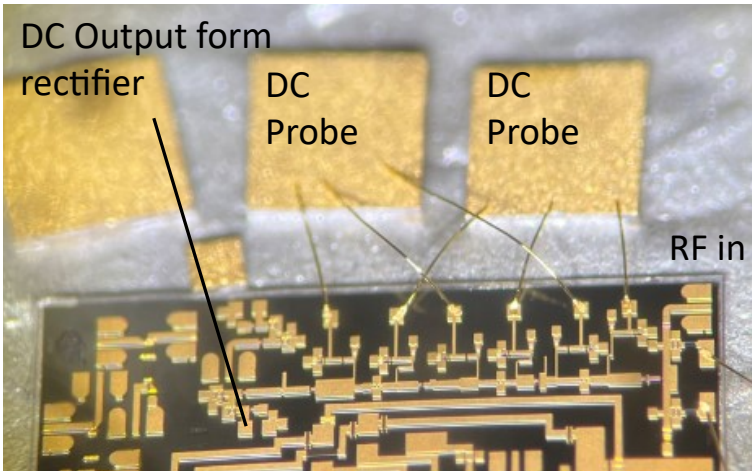


Figure 7.10: Dicke swithed radiometer designed by integrating a SPDT switch, three stage LNA and power detector. Measurements and characterization still need to be done on this MMIC.

7.2 Summary of Contributions

In summary, the work presented in this thesis covers the modeling and design in millimeter wave GaN of several important front end components and their system level integration on-chip. This section briefly summarizes the work and contributions from Chapters 2-6.

- Chapter 2: This chapter covered the modeling and design of GaN HEMT power amplifiers and LNAs. For large signal operation, a balanced three stage power-combined power amplifier and single-HEMT driver amplifier are demonstrated. For the balanced power amplifier, the third stage of both unit amplifiers combine two 4×37.5 μm HEMTs with a quiescent drain current of 60 mA. The peak output power is measured to be 26.7 dBm at 77 GHz, and the peak power added efficiency (PAE) around 14.8 % at 95 GHz. A three stage LNA with a measured small-signal gain of 20-25 dB across 70-110 GHz and a minimum NF of 5.2 dB at 80 GHz and a peak NF of 7.8 dB at 100 GHz is also demonstrated. Contributions from this chapter are reported in [73], [74] and [75].

- Chapter 3: Four switches are demonstrated including a SPST, two SPDTs and a SP4T showing tradeoffs in performance based on HEMT periphery selection. None of the switches showed any signs of compression with up to 20 dBm of input power at 92 GHz with simulations indicating compression of the SPST switch occurring after 40 dBm (10W). These switches are fundamental building blocks of other components and systems including switched line phase shifters, Dicke radiometers and switched T/R front ends. Results of the switches are published in [16]. Two continuous reflective phase shifters, one 90 degree and one 180 degree, are designed and validated with measured results. lange couplers are used for both of the designs with two cascaded lange couplers being used in the 180 degree phase shifter. Large-signal measurements showed a P1 dB compression point of 19 dBm. Phased array systems and test instrumentation are possible applications of these designs. The results of the phase shifter MMICs are published in [11] and partially in [75].

- Chapter 4: This chapter covers the theoretical basis for frequency multiplication using a simplified HEMT model. Equations which aid in design and bias selection are shown and discussed. High

frequency effects are also discussed and result in reliance on computer aided computation software and Angelov foundry models. HRL T3 GaN HEMTs are then harmonically characterized for frequency multiplication using load-pull simulations. Results of load-pull simulation characterization give optimum load impedances for design of frequency doublers and triplers. The contributions of this chapter are partially presented in [89].

- Chapter 5: A single-ended frequency doubler, a balanced frequency doubler and a balanced frequency tripler implemented in the HRL T3 40 nm GaN process. The tripler measures an output power of 10±1.5 dBm for an input power of 19 dBm over 75–110 GHz. Both doublers achieve conversion gain and over 11 dBm output power in the W-band frequency range. Reactive matching and cascading of a post-multiplication amplifier stage allows the single ended topology to exhibit conversion gain and high fundamental suppression. Balanced topologies implemented with broadband couplers allows high harmonic suppression with a wide-band conversion gain. To the best of the authors' knowledge, this is the first demonstration of GaN MMIC W-band doublers with conversion gain. The single-ended and balanced doubler have similar performance in suppressing the fundamental. The post-amplifying HEMT along with the output matching network provide excellent fundamental suppression of over 35 dBc over the entire output band and over 50 dBc over 78 to 87 GHz. The contributions of this chapter are reported in [89].

- Chapter 6: The integration of a power amplifier with a driver, SPDT switch and LNA is demonstrated on a single GaN-on-SiC 5 mm×3 mm die that operates over the entire W band (75–110 GHz). The transmit path consists of a three-stage power combined balanced amplifier with a single-HEMT driver. An SPDT switch using a quarter-wave shunt HEMT topology is used as the connection between the antenna port and the PA output and 29 dBm of output power is measured at the output of the switch at the 92 GHz center of the band. Including the switch loss, the receive path with a 3-stage LNA demonstrates a noise figure that ranges from 5.2–7.8 dB across the band, with 15–22 dB gain. The switch does not show compression at peak PA output power. The results from this Chapter are reported in [73], [16], [75] and [74].

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