ECEN 5014, Spring 2024, Active Microwave Circuits
Prof. Zoya Popovic and Prof. Laila Marzall

PROJECT 1: IMPEDANCE MATCHING

Assigned	January 16th (Tuesday)	Goals: Design and investigate several matching circuits that you can use later; Review Cadence/AWR Microwave Office or Keysight ADS in this context; Hopefully learn a few new tricks.
Due	January 25th (Thursday)	

Part 1 – Impedance matching with lumped elements, stubs and quarter-wave lines

For all cases below, chose a center frequency of 3 GHz and match to the standard 50Ω impedance. The match at 3 GHz should be better than -20dB. The percentage bandwidth is here defined as the ratio of the frequency range over which the match is -10dB or better, to the design frequency. Choose a suitable frequency range and number of points that you can use for all the plots so that a fair comparison can be made. For all of the examples in this project, use ideal transmission lines (no specific implementation is given).

1.1. Lumped elements: match the input impedance of a transistor $Z_L = 10 - j15\Omega$ using a *LC* network. Determine the values required for the inductor and capacitor, assuming ideal elements. Make a plot and measure the percentage bandwidth.

- Find commercially available parts for your lumped elements. It is possible that you will not be able to find the correct values, and you may have to redo the design. After you chose the components, find .s2p files or an equivalent circuit model and check the quality of your match. Comment on your findings.

1.2. Transmission-line matching: Design a transmission-line matching network and compare in terms of bandwidth and loss. Use a Rogers RO4350C substrate, 30-mil thick. No need to use only 50-ohm lines. If you are doing this in MWO, you will need the substrate definition using the MSUB block, and in ADS you define the stack for the whole project.

- In your previous classes you learned about a single-stub (and maybe also double-stub) matching technique. We will not repeat it here. Answer the following questions:
  (a) What are disadvantages of the method?
  (b) What is a situation when it is appropriate to use it?

Part 2 – Impedance matching range of slug and single-line matching

2.1. Slug matching: Assuming two slugs with electrical lengths of 90° at the design frequency, determine the impedance matching range (region of Smith chart that can be matched) if the relative permittivity of the slug dielectric is $\varepsilon_r = 3$. Determine the slug distances that match a 200-Ω load and find the percentage bandwidth. How does it compare to your values from Part 1?

2.1. Single line matching: Assuming that the characteristic impedances at your disposal are limited to the 20 - 90Ω range (as in, e.g. most microstrip lines). Use a circuit simulator to show the region in the Smith chart that can be matched with a single section of line. Describe a

procedure for determining Z and θ of the line. When does this reduce to the well-known (and not repeated here) quarter-wave match?

Part 3 – Broadband matching

3.1. Tapered line: Match a 200Ω impedance to a 50-Ω line using several sections of intermediate impedance lines. You can start with several quarter-wave sections, and then make them electrically shorter and increase their number. In the limit, you can have a linear (or some other) taper in impedance, the total line length will get larger and therefore in real life have higher loss. Investigate the bandwidth of such matching using lossless lines.

3.2. Coaxial transformer: Use an ideal coaxial model in the simulator to plot the performance of a 4:1 coaxial transformer. Does changing the line length (delay) change performance?

***For PhD students only**

Part 4 – Couplers: In your other classes, you analyzed couplers using the standard method of odd and even modes. Here we will understand this method through simulations.

Use the same substrate as in Part 1.2. For a Z_0=50Ω and a coupling coefficient of 10dB, find the odd and even mode impedances of a single-section quarter-wave coupled line coupler operating at 6 GHz. Here is how to do it:

- First calculate Zodd and Zeven from the known coupling coefficient. These will define your coupled-line parameters.
- Connect a 50-ohm input port to an ideal 2-port in-phase power splitter.
- Connect a coupled-line ideal element (e.g. CLIN in MWO) to ports 2 and 3 of the splitter. Set the coupled line parameters to what you calculated above, at 6GHz center frequency.
- In one of the power splitter branches (e.g.. connected to port 3 of the splitter), insert an ideal phase shifter element between the splitter output power and coupler input port. This will allow you to define an odd or even mode.
- Simulate the input impedance a phase shift to 0° (even mode) and 180° (odd mode). What impedance do you get in each case? What do these values mean?
- To obtain a 10-dB design that can be fabricated, next you will optimize the physical parameters of the coupled-line section. Use MCLIN for the simplest microstrip coupled-line block. Start with a reasonable line separation and line widths and lengths. You then parameterize the physical parameters as variables with reasonable limits. Then configure the optimizer to achieve the correct impedance transformation.
- Once you have the impedances, resimulate the coupled-line coupler and confirm that you have a good design.

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Project 2: Small-signal Amplifier Design for High Gain

Assigned	January 25th (Thursday)	**Goals:** Learn how to de-embed a small-signal FET model from measured S-parameters; design a gain-matched stable small-signal amplifier with bias lines. Download WIN GaAs pdk and use device models provided for the GaAs HEMTs.
Due	February 6th (Tuesday)	

Part 0 – Installing the WIN PQG3-OC GaAs pdk

Download the pdk from here:
https://drive.google.com/drive/folders/1-xe91rTVOCPKiO2IchLOs2UFii8ncGfV
Half of the class will do Project 2 in Microwave Office, and the other half in ADS. For the next project you will switch. Therefore, you may wish to download the pdk in both tools now. After the first two projects, you will be able to choose your simulator.

Part 1 – De-embedding small-signal intrinsic model

1.1. You will find a zip file called "3.Measurement_Data" inside the main folder. Please look for the S-Parameters for the 4x75µm E-mode HEMT device (EMS - Enhanced-Mode, Microstrip device). The device has the MDF extension, a compilation of S-Parameters for many bias conditions.
1.2. Choose a bias point close to Vd=4V, Vg=+0.5V and import the s2p file. Remember to state your chosen bias point.
1.3. Low-frequency model: extract the intrinsic model at the lowest simulated frequency. Quantify the approximations you make.
1.4. Extract the intrinsic model at 10 GHz. You will need to make some assumptions because you are likely to have more equations than unknowns. State your assumptions clearly.
1.5. Plot the S-parameters of your intrinsic 10-GHz model and compare to the s2p file that you started from.

Part 2 – Small-signal gain-matched amplifier design at 10GHz using the GaAs HEMT

2.1. Considering the device parameters, make a list of reasonable specifications for a final small-signal amplifier designed for 10GHz. Explain your choices.

2.2. Input and output matching:

- Design two separate matching networks (assuming you will later implement them in microstrip), one to match the input impedance (a s1p file) and one to match the output impedance (another one-port network, i.e. complex load). This effectively means that you are assuming a unilateral transistor. You can do the design on paper (Smith chart), or

using a CAD tool. In your report, the matching circuit performance should include $|s_{11}|$ and $|s_{22}|$ on the same plot.
- Connect the matching networks at the input and output of the transistor and simulate the performance. Discuss the results.
- Now re-design your amplifier as a bilateral device, so that it is matched for gain at 10GHz. This means that you meet your specs at the design frequency and in your specified band. Plot the S-parameters and summarize the performance in a table.
- Is the design stable? To check stability, you will need to plot the S-parameters of your amplifier design to a high frequency, wherever the device might have gain (in this case, perhaps 50GHz). Observe the S-parameters for any indications of instability.
- Plot the standard K and mu/delta stability factors.

2.4. Bias lines:

Design a realistic bias-Tee network for an amplifier that operates at 10 GHz with a 10-20% bandwidth.

- To design a bias line, you will need to prevent the DC to flow to the RF input port using a blocking capacitor. The value should be a low series impedance at 10GHz.
- To complete the bias line design, you will also need to prevent the RF from flowing into the DC input port. This is done either with a lumped element inductor (choke) or with a quarter-wave shorted line.
- Plot the three-port S-parameters of the bias tee from DC to 40 GHz.
- Is your design affected when different impedances are connected to the supply (DC input) port? This is important because you will generally not know the power supply RF impedance. If your design is not robust, this will lead to instabilities.

Now add your bias lines to the amplifier design from above. The bias lines can be connected in different places in the input (gate) and output (drain) networks. Investigate the best position for adding the bias lines. Plot your final amplifier S-parameters and discuss the performance.

***For PhD students only**

3. More about Stability:

For this exercise, we will assume that we dice the transistor and mount it on a microstrip circuit. In fact, manufacturers provide discrete transistor die for this purpose (see e.g. https://www.qorvo.com/products/discrete-transistors/gan-hemts). In this case, there can be extra inductance in the source, as well as bond wire connections. We need a three-port model for the transistor with the source not grounded. This inductance typically has values between 0.2 and 1nH, depending on the substrate thickness and device package. Re-simulate your amplifier for 0.1, 0.5 and 1nH values of the source inductance. Discuss the results, especially stability. For a 0.5-nH source inductance, re-design your amplifier for best match and gain at the design frequency. This is just an adjustment to the design from the previous part when the inductance is taken into account. Plot all relevant S-parameters vs. frequency using the most informative scales on the vertical axis.

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Project 3: Broadband Amplifiers

Assigned	February 7th
Due	February 20th

The goal of this project is to design several broadband amplifiers. The report will be in slide format. You can make your own choices as to what to include on 20 slides maximum. For PhD students, the derivation in 3.3 can be done by hand and turned in or scanned.

Part 1- Balanced Amplifier

1.1. Design a gain-matched amplifier with the same device as in Project 2 and for a frequency range of 8-12GHz (X band). We are going to start with the full model that needs biasing. Use the device model and attach voltage sources to your bias Tees. It is a good idea to also monitor the current at the gate and drain.

Simulate the small-signal performance of the amplifier and summarize it, you will use this as a benchmark.

1.2. Design a coupled-line 3-dB coupler with a center frequency of 10GHz. You can also design a branch-line hybrid or Wilkinson divider with a comparable bandwidth if you prefer. Describe your circuit and design method. Plot all relevant parameters.

1.3. Next, design a balanced amplifier with two coupled-line couplers and amplifiers from above. Start by simulating two couplers back-to-back, then add just the transistor with no matching circuits, and then include the full amplifier from part 1.1. Summarize your simulations in one or two plots. Investigate what happens if the two amplifiers are a bit different (for example, you can change biasing or matching), or if the loads are not perfect.

Part 2- Resistive feedback amplifier

Next you will use the same device to design a feedback amplifier with as much bandwidth as you can (let's see who gets the most!). Use both series and parallel feedback, with a larger resistor between the gate and drain, and a smaller resistor in the source. You will need to think about biasing – adding a blocking capacitor between gate and drain in series with the feedback resistor.

First, only put the series resistor (on the order of 100Ω) in the feedback between drain and gate. Simulate the performance and provide all relevant simulation plots and associated comments in your report. Make sure you are clear about your bandwidth definition.

Part 3- Distributed / Traveling-wave Amplifiers

3.1. Search the literature for at least 5 references for distributed amplifier and traveling wave amplifiers in the last 10 years, and summarize their performance in a table. Give a brief summary of your favorite one.

3.2. Simulate a distributed amplifier using the simple model we did in class (Lecture 6). De-embed g_m, C_{gs} and C_{ds} from your device S-parameters at some relatively low frequency, using the Y-parameter method. You can use your values from Project 2. After finding the capacitances, chose inductor values and simulate the performance as a function of number of stages. For your favorite number of stages, now add some reasonable value of R_{ds}, and discuss how this changes the behavior.

For PhD students:

3.3. Derive the expression for the gain of a distributed amplifier from the simple equivalent circuit we did in class, as a function of the number of elements.

- Start by finding the expression for the drain current as a sum of current sources from each section, not forgetting that a part of the current will go towards each load.
- Assume the delay between each element can be found from the propagation constant of the drain line (β_d).
- Next express the voltages across the gate-line capacitors, assuming the gate line is lossless and that the delay between the elements can be found from the propagation constant of the gate line (β_g).
- Simplify the expression for the total drain current. Assume that $Vin=V_g/2$ for a matched generator.
- From the expression for the current, find the power dissipated in the matched load Z_L on the drain output side.
- Find the expression for the gain, assuming the available power from the generator is $V_g^2/4Z_L$.
- You can next simplify this expression assuming the gate and drain line propagation constants are almost the same ($\beta_d \rightarrow \beta_g$) and using the series expansion for sin(x).
- Comment on the expression you get as a function of number of stages N. What approximations were incorrect and how would you fix them in principle?

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Project 4: Low-Noise Amplifiers

For this project, you will make a slide presentation. Suggestions for slides are given as a guideline, but you should also choose what you feel is important.
If you wish to use ADS for this project, a noise analysis template can help you get started. In MWO, there is an example LNA (go to file – open example – LNA_5GHz.emp).

Assigned	February 22nd 2024
Due	March 5th, 2024

Part 1. Benchmark gain-matched amplifier

For this part, use ideal elements with the device model that includes noise parameters. In the next part, you will do a MMIC layout using pdk elements.

1) First, find at least 2 low-noise amplifiers operating in X-band from different manufacturers and summarize the basic performance in a table (frequency range, type of active device, noise specifications given in the data sheet, gain, packaging, etc.). **(Slide 1)**
2) Using WIN PQG3-0C EMS 2X25 biased at Vd = 2V and Id = 50 mA/mm (you will need to adjust Vg to get the correct Id for the given periphery), plot noise parameter data from 5-50GHz. Compare with the model handbook information and summarize the relevant device specs in your report (a table might be the best). **(Slide 2)**
3) At this bias point, design a small-signal gain-matched amplifier (as before) using first ideal components. Then make a second schematic where you replace ideal with real components from the PDK. You will probably have to tweak your design to adjust the performance and you will use this design for later comparisons. **(Slides 3-4)**.
4) Orient and place the component layouts to form your first MMIC layout **(Slide 5)**.

Part 2. LNA design (input and output match, effect of attenuators)

5) Start from your small-signal gain matched design. Modify the input match to a noise match and see the effect on the noise performance. Go to:
3. Measurement_Data\3.Measurement_Data\Noise\EMS folder to find the information or use simulation tools to find Γ_{opt} at the design frequency of 10GHz. Do not change the output match. Simulate the noise figure and S-parameters and provide relevant plots. Compare to the amplifier in Part 1. **(Slides 6-7)**
6) Change the output match to get better gain and quantify the gain improvement. Comment on the effect on the noise figure and plot the amplifier parameters. **(Slide 8)**
7) Add an attenuator to the input of the noise-matched amplifier. Change the value of attenuation and observe the effect on noise figure. Repeat for attenuator placed only at the output. Discuss your results and provide relevant plots. **(Slide 9)**
8) Design the MMIC layout. Run DRC check and clean up errors. **(Slide 10)**

Part 3. Noise of cascaded amplifiers

Use your low-noise design matched at the output to 50 ohms and cascade it with your gain-matched design. Plot the gain and noise figure. Compare to values obtained by the theoretical cascade formula. (**Slide 11)**

For PhD students only:

Part 4. Read the paper on noise models by Marion Pospieszalski and summarize the most important conclusions in in 1-2 slides. (**Slides 12-13**)

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Project 5: Power Amplifiers

Assigned	March 7, 2024
Due	March 22, **electronically**

The goal of this project is to design a power amplifier and learn how to do nonlinear harmonic balance simulations and understand the limitations of the models. An additional goal is to learn how to do EM analysis in a MMIC. Please turn in electronically slides for what would be a 20-min conference presentation (that means ~20 slides or less).

Part 1. Importing a nonlinear model and verifying DC IV Curves, S-parameters

Use the nonlinear model for an E-mode 6x100 μm device from the WIN PQG3-0C PDK.

1.1. IV-curves: The first step is to verify that the IV curves look reasonable. Simulate the IV curves and verify against the plot in the WIN Model handbook, page 5 for a device at room temperature. Remember that Ids is in mA/mm. Observe the Vds and Vgs ranges.

Notes:

- *In MWO, use the "IVCURVE" element found in "MeasDevice" and connect the "Step" and "Sweep" ports to the gate and drain, respectively. Create a new graph and add the "IVCurve" measurement found in "Nonlinear"->"Current"->"IVCurve".*
- *In ADS, use "Design Guide" > Amplifier > DC IV curves and follow the example.*

Find Ids,max and multiply by Vds at the quiescent point (4V) to find Pdc. Multiply by the approximate PAE on page 8 in the WIN handbook when the device is loaded with 50Ω. This will give you an initial approximation of the maximum output power.

1.2. Large-signal model: To find large-signal scattering parameters of the nonlinear model will require harmonic balance simulations. In a simulator, most harmonic balance tracing functions are performed under nonlinear measurement commands. The transistor model must be DC-biased at the gate and drain the desired bias point.

Create two schematics with the same device and discrete frequency points f0 = {6, 6.2, …,12} GHz. Use an idealized bias tee (1H ideal inductor and 1F ideal capacitor) to avoid the complexity of the bias tee design for this first step and place a volt meter between the drain and ground and a current meter in series with drain terminal (check direction). Place an annotation to read Idq (quiescent current at the drain). Place a 50-Ω power port at the input and a 50-Ω termination at the output on one of the schematics and small-signal terminations (PORT) only on the other.

Find S_{21} (small signal) at 10GHz and use it as a first guess for the gain (maybe a few dB less because of compression). Calculate the required input power to achieve saturation based on the maximum output power calculated in the previous section, divided by the gain.

Trace large-signal S-parameters (in AWR, you will need 3 schematics to trace S11, S12, S21, S22) on the compressed Smith Chart over the frequency points initially, at compression and compare with the small signal results of the small-signal schematic. Please compare these in the same plot. Reduce the input power until the equivalent curves are close, this will be the linear regime. Now, you have the range of input powers to trace the next plots.

Notes:

- *Vgg used in the measured S-parameter file will likely produce a different drain current in the model. Adjust Vgg to achieve the correct current.*
- *In MWO right click on the schematic name and select "Add Annotations", then choose "DCIA" to show DC currents into each node on the schematic (useful for verifying quiescent bias point).*

Part 2. Large signal device analysis

For this part, use large signal schematics set @ f0 = {8, 10, 12} GHz.

2.1. Use the IV curves from Part 1 and the procedure from class or any PA book to find Ropt for deep AB class bias point, and make a clear statement about it. Trace the dynamic load line for 50-Ω and Ropt impedance terminations at the output port. Play with the input power, see what happens, and write your comments. Where is Ropt connected (is it at the virtual drain)?

2.2. Put a tuner in the input set for a conjugate match (for gain).

2.3. Plot the harmonic content for the three frequencies. You can start by choosing 10 harmonics for the simulation settings and test convergence with fewer.

2.4. Trace the drive-up curves (output power, power gain, PAE vs. Pin) at the three frequencies.

2.5. Plot the output voltage and current waveforms and compare them with the dynamic load line – it looks interesting. Explain it to yourself – why is it not a line? Drive the device harder – look at the output voltage waveform, dynamic load line, and harmonics. Write your conclusions.

Part 3. Class-AB Power Amplifier

3.1. Run load-pull and source simulations at the previous bias point at 10 GHz, using the input power level found for the maximum PAE in the last section. Plot the source-pull and load-pull contours on a Smith chart.

3.2. Design the bias/stabilization circuit using the PDK elements, fitting the layout to pass DRC and run EM simulations, keeping the tuners at the source- and load-pull values. You will find that EM simulation will add losses to the circuit. What does that mean for stability and efficiency?
Note: Use linear and nonlinear Nyquist plots to evaluate stability over DC-40 GHz.

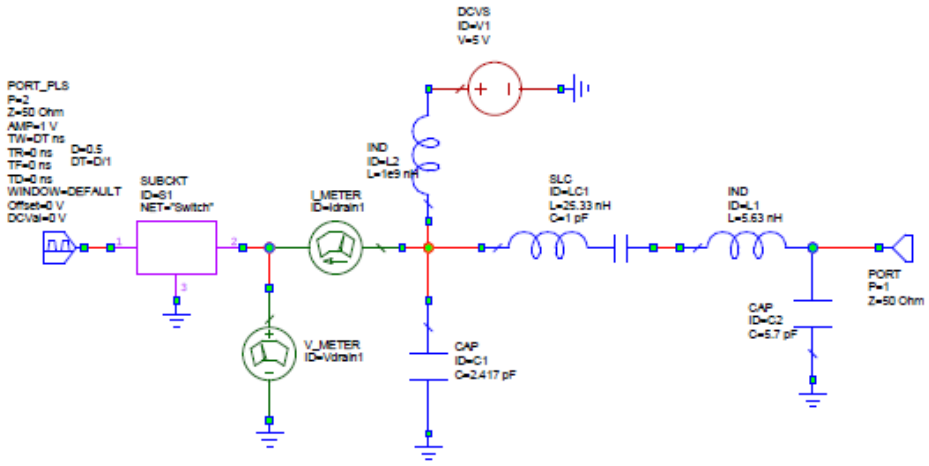
3.3. Now you have to adjust the input and output tuners so that the impedances presented at the input and output device planes are the ones given by the source- and load-pull simulations. Use the impedance probes placed at the gate and drain terminal.

3.4. Design the output matching network, adjust the input tuner, and design the input matching network in full layout and simulate using full-wave EM.

3.5. Plot the final performance using the plots from Parts 2.3 – 2.5.

PhD students only:
Part 4. Ideal Switch Class-E PA

(1) The output capacitance is found from Cds in parallel with Cgd or estimated from device model simulations. What is the output capacitance and the class-E max frequency of operation for this device? Use an ideal switch in parallel with the output capacitance (as in the lecture) to model an ideal class-E amplifier at a frequency where you think you can reach class-E operation. Use the currents and voltages from the DC simulation in Part 1. Your circuit should look like the one below, approximately.



In ADS, the switch can be found in the parts under System Switch and Algorithmic component. It specifies the on and off resistance and a finite slope during turn-on. To get close to an ideal switch, you need to set the voltages V1 and V2 close to each other – this means that the voltage waveform is changing only between these values and is closer to an ideal step.

In Microwave Office, there is a relatively new ideal switch element under *Circuit Elements-Libraries-AWR web site-APLAC-Switch_AP*. To modify all the parameters, you need to click on "show secondary" in the parameter tab.]

(2) Calculate the elements of the output class-E network (lumped is ok, even if it is not realistic – in a real design we would convert to transmission lines). Use a series resonant circuit as the open for all higher harmonics.
(3) Perform a harmonic-balance simulation (HB) with 10 harmonics. Use a sinusoidal voltage drive for the switch (V-1tone under the frequency domain source component in ADS)
(4) Plot the current and voltage of the switch in time domain. To do that, you have to add a current probe. This is under the probe component, note that it has a direction.
(5) Plot the harmonics of the output power. What is the ratio of the drain bias to the output voltage across the real part of the class-E load?
(6) Find out how the number of harmonics in HB affects your results. How many harmonics are sufficient to simulate this circuit?
(7) Calculate the output efficiency and simulate it to see that it is what you expect.

A few other things you can do are:

- Compare with a nonlinear model simulations where you bias the device in class B and drive it hard.
- Change the load by 5% for both real and imaginary parts and examine the effect on the efficiency and time-domain waveforms.

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Project 6: Oscillators and Mixers

Assigned	March 26, 2024
Due	April 11, 2024 – Electronically – up to 20 slides

The goals of this project are:

- Compare the Q-factor for different resonators.
- Design an oscillator and a mixer at an operating frequency between 8 and 12 GHz integrated into an MMIC, using the WIN Semiconductor InGaAs PQG3-0C, 4-mil PDK, E-mode CPW transistors.
- Understand the small-signal characterization of oscillators and the essential conditions to maintain oscillation.
- Understand oscillator large-signal simulation – how to set probes and calculate output power and phase noise.

NOTE: We will use AWR for this project.

Part 0. Oscillator and mixer specifications

1. Find the specifications of at least 2 commercially available oscillators operating in X-band and summarize the specifications. Observe if the primary design purpose is output power, tunability or phase noise in each case.
2. Do the same for mixers. The goal is to familiarize yourself with what industries specifies for their customers.
3. Read parts 1, 2, and 3 of the assignment. Based on your experience with the PQG3-0C process and on the topologies described in each part, propose the initial specifications for your designs. Example: Define the oscillator output power between 0-10 dBm.

Part 1. Resonators design

1.1. Make a schematic with an LC ideal parallel tank circuit to resonate at 10 GHz. Assign a high-quality factor for the capacitor (10000) and a Q = 50 to the inductor. Ground one of the ends and connect a 50-ohm port to the other. Plot the reflection coefficient on the Smith chart. You should see an open circuit close to 10 GHz.

1.2. Place a series capacitor between the port and the tank circuit. Adjust the capacitor and the LC resonator to match 50 ohms at some point close to 10 GHz (the Q will not vary much over the frequency range). Now, your resonator is critically coupled.

1.3. Plot $|S_{11}|$ (dB) in a rectangular plot. To get a Q-factor of 50, what is the reflection coefficient magnitude that defines the fractional bandwidth?

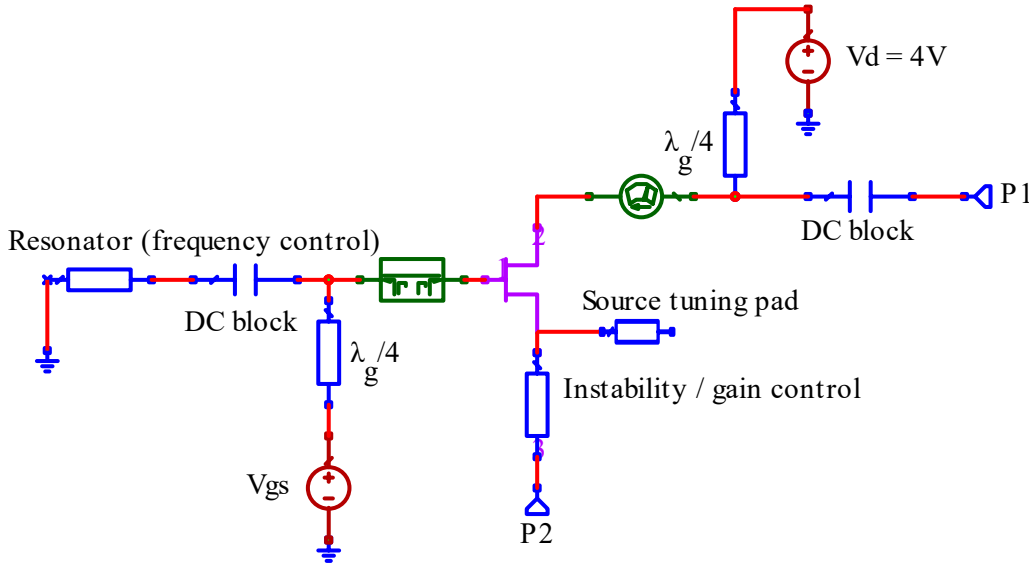
1.4. Do the same for a quarter-wave short-circuited resonator at 10 GHz. You will need to change the electrical length based on your coupling capacitor value. Compare the values obtained with the PDK model and EM simulation. You can use an ideal capacitor for the coupling.

This video may help you: https://www.youtube.com/watch?v=5DgmH9XsfLA

Part 2. Oscillator design

2.1. Define the size of the transistor to generate 10-15 dBm of output power as an oscillator. You can do it by tracing the IV curves of different devices with a 10-Ω resistor between the source ground. Multiply the saturation drain (Vgs = 1.6 V) current by the nominal supply voltage of 4 V, or find it in the model handbook. Show your calculations. Consider a 10% DC-to-RF conversion efficiency dimension.

2.2. **Oscillator schematic:** we start with the transistor without the grounded source (CPW model). Then a resonator is included in the circuit to determine the oscillation frequency. In the circuit in Fig. 1, a microstrip resonator is connected to the gate (input) terminal. You need to choose the length and type of this microstrip resonator (impedance, coupling, short or open, etc.). The drain terminal will be one of the outputs and should be connected to a 50-Ω port. The source terminal is connected to a 50-Ω port, and it can be used for injection locking or just connected to the ground. The second stub at the source represents a pad that you would solder a source lead to in a circuit using a device with two source leads and is helpful for tuning. After you are happy with your design, you can terminate the source in a fixed impedance.



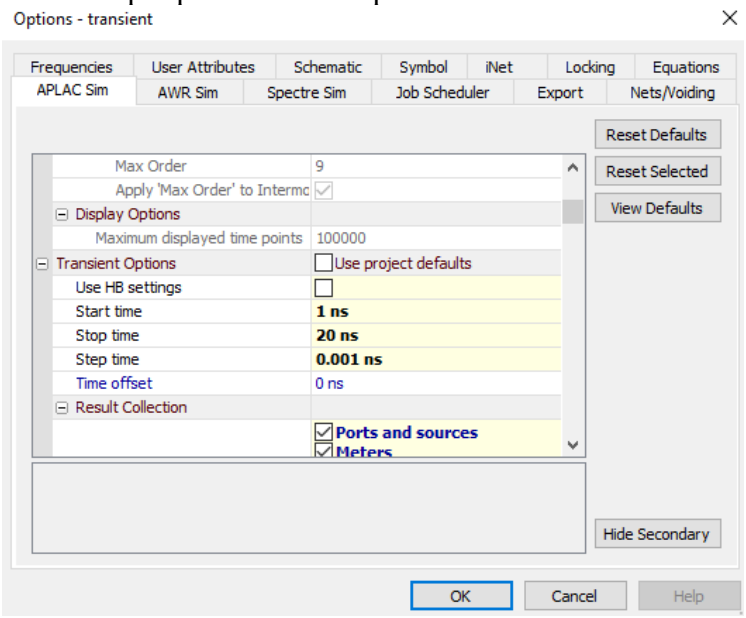
2.3. **Negative resistance small-signal simulation:** Plot the amplitude and phase of reflection coefficients at the drain and source ports. You will need a radius larger than 1 on the Smith chart. In MWO, the way to get a Smith chart with a radius larger than 1 is as follows: go to a Smith chart graph, right-click on it, and go to Properties-Grid-Size-Compressed. On the Smith chart, the highest amplitude of a counter-clockwise loop determines the oscillation frequency. Note: you may need to adjust bias lines to achieve a counter-clockwise loop and change the P2 port impedance (or simply put a load instead of P2). If you leave P2 as a port, you should get the same oscillation frequency on the two ports, but different magnitudes. Plot the Smith chart(s) in your report and label the oscillation point.

Next you will use GProbe to calculate the resonator and device impedances and check the condition Re {Zin, dev} > Re {Zin, res} and Im{Zin, dev} = Im{Zin, res}. Implement the following equations on output equations:

s_res = negative_resistance.AP:GAM_GP2(GPROBE2.GP1,1,50,0)
z_res=(1+s_res)/(1-s_res)
z_res=z_res*50
z_res:
s_dev = negative_resistance.AP:GAM_GP2(GPROBE2.GP1,2,50,0)
z_dev=(1+s_dev)/(1-s_dev)
z_dev=z_dev*50
z_dev:

Plot the real and imaginary parts of $Z_{in,dev}$, and $Z_{in,res}$, in a single plot. Find the frequency where the oscillation condition is met. Does it agree for the two impedances?

2.4. **Transient analysis.** Duplicate the schematics and set the frequency grid to a single point close to the potential oscillation frequency. Initially, set the transient option parameters as shown in the figure below. Plot the transient Itime function (APLAC Trans) at P1, and observe what happens when you add loss to the resonator and change the gate bias level. Plot Ptime at P1. Is the output power at the expected levels?



2.5. **Small-signal loaded open-loop gain**. Duplicate the schematic and replace the GProbe with the OscProbe block. Plot the amplitude and phase of S_{21} in rectangular coordinates. Locate the maximum gain and the frequency at which that phase crosses zero. How long is the gate resonator, measured in electrical degrees, at your design frequency? How do the other parameters of the circuit affect the response? Describe the dependence on source lead short stub and any variations you do in the drain circuit. Note: Configure OSCTEST as shown below, and set the frequency grid with 50% BW at the central frequency and steps of 0.1 GHz.

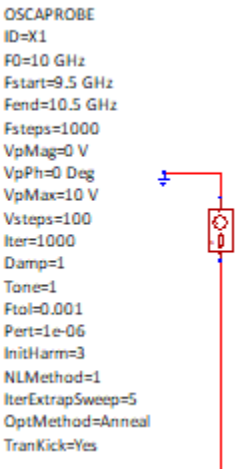
Element Options: OSCTEST - Oscillator Open-Loop Element (Closed Form) Properties (Showing 3 of 3)

Parameters | User Attributes | Symbol | Layout | Model Options

Yield

Name	Value	Unit	Tune	Optimize	Constrain	Lower	Upper	Step Size	Hide	Hide Label	Description
ID	O1								☐	☐	Element ID
FC	_FREQ*1e-9	GHz							☐	☐	f1 < fc < 2*f1
Z0	50	Ohm	☐	☐	☐				☑	☐	Port 1 and 2 impedance

2.6. **Large signal, oscillation frequency, spectrum, and phase noise**. Duplicate the first schematic (negative resistance) and set the frequency grid to one point close to the expected oscillation point. Replace P2 with a resistor with the same impedance. Remove the GProbe block, connect an OSCAPROBE block at the gate, set a reasonable frequency range, and reduce the voltage if necessary. The best approach is to make all parameters visible and play with them to obtain convergence by changing parameters such as the Vstep and optimization method..



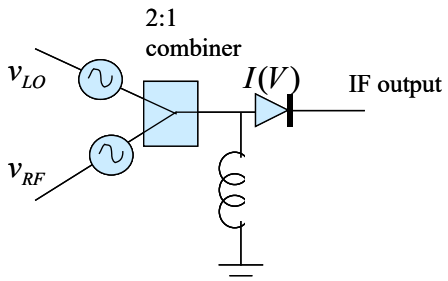
For PhD students only:

2.7. Matching at the output port. Design a matching network at the output port to maximize output power. Study the trade-offs between phase noise, resonator quality factor, and output power.

Part 3: Single-Ended Mixer Design

3.1. In this part of the project you will use harmonic balance to simulate a simple single-ended mixer, shown in figure below. Choose the PDK diode. Simulate the mixer output when ideal sources are used for the RF (at 10 GHz) and LO, with an IF of 100MHz. You can change the number of harmonics taken into account in the harmonic balance analysis. Start with 7 harmonics and simulate the circuit for increasing numbers of harmonics until you reach some level of convergence that you are happy with.

Here is a very useful AWR on-line book on mixers: https://resources.system-analysis.cadence.com/i/1325428-rf-electronics-design-and-simulation/140?



3.2. Answer the following questions about your design:

- What is the conversion loss of the mixer?
- How many other frequencies show up and what would you do with them?
- Change the IF bandwidth to smaller and larger than the initial 100MHz. What effect does the IF bandwidth have on the number of required harmonics for harmonic balance?

Some of the LO and RF power is reflected off the un-matched diode, increasing the conversion loss. Match the input of the diode to improve conversion loss, and add an ideal IF filter at the output. Compare to the mixer in part 1.

For PhD students only, EXTRA CREDIT

Part 4. Mixer with Oscillator from Part 1 as LO

Use your oscillator from Part 1 as the LO for the mixer. Investigate the frequency content on all ports you have access to (this depends on the design of your oscillator). Compare performance to above mixer with ideal LO. Plot the phase noise of the oscillator up to>1MHz offset and discuss.

ECEN 5014, Spring 2024, Active Microwave Circuits
Profs. Zoya Popovic and Laila Marzall

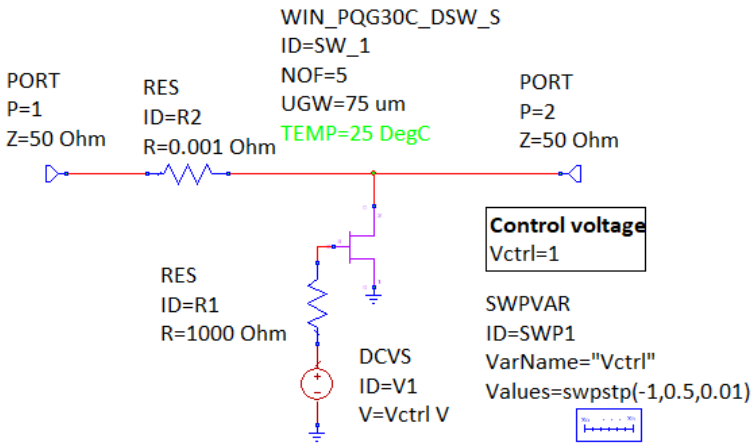
Project 7: Switch

Assigned	April 11, 2024
Due	April 18, 2024 – Electronically – up to 10 slides

The goals of this project are to design a simple switch, and then to use it in another circuit of your choice. You can use your preferred CAD tool for this last project.

Part 1. SPST single-transistor switch

1. To design the switch, you will use a special transistor. Although any transistor works, these devices are optimized for switching applications. You will find this in Libraries/Actives/Switch (Single Gate Switch Scalable Large Signal Model).
2. Make a shunt switch with a variable DC control voltage source and large resistor (e.g. 1kΩ) in the gate, grounded source and a small (0.001 Ω) series resistor in the input line.



3. Plot S-parameter magnitude on a rectangular plot at 10 GHz over Vctrl for a 3x15 µm device and a 5x75 µm device.
4. Compare the matching, insertion loss and isolation for the two devices.
5. Find C_off, R_off, C_on, R_on at 10 GHz for both devices. Relate this to the S-parameter performance in 3.
6. Plot the complex S_{11} and S_{22} on the Smith chart. Design a matching network for the 5x75 µm device so that the switch is matched to 50Ω when the path is "on" and an open when the path is "off". Please show all circuit schematics and justify your matching network choice.
7. Plot the S-parameters for the final designed SPST switch for the "on" and "off" states (paths) from 8-12 GHz.

Part 2. Additional problem – PICK ONE.

A and B are for MS students, C and D for PhD students.

A. Repeat above for a series switch and compare. Present some conclusions.

B. Design a SPDT switch with one of the devices from above. First make specifications and then explain why you picked a specific architecture.

C. Design a switched-line phase shifter with 2 bits, centered at 10GHz. Set your specifications. If you want, you can extend to more bits.

D. Design a continuous reflection-mode phase shifter using transistors as variable loads.