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GaN MMIC RF Switches for In-Band Full-Duplex Phased Array Calibration

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***Abstract*—This paper presents three reflective-type, single-pole double-throw (SPDT) switch topologies intended for a switch feedback network in a full-duplex phased array module. The MMIC switches are implemented in a 250 nm GaN on SiC process, with a design frequency range of 2.5 to 3.5 GHz. Due to the relatively low design frequency, lumped elements are used for the passive networks, and the design procedure is described. The reported switch topologies demonstrate an insertion loss below 2 dB across the desired bandwidth with varying isolation based on the topology. Measured performance is compared with simulations using foundry transistor models.**

***Index Terms*—Switch Feedback Network, SPDT, MMIC, full-duplex, half-duplex, SIC**

I. Introduction

Transmit-receive (TR) phased arrays can operate in half or full duplex modes. When transmitting in half duplex, as done in pulsed radar systems, a switch is used to route the signal from the final stage power amplifier (PA) to the antenna, reducing the available receive-mode time [1]. Alternatively, a diplexer can be used between the antenna and TR module where the array transmits in an up-link frequency band, which is either closer or farther separated from the receive down-link band. In this case, the spectrum is not used efficiently and the diplexer can be relatively large and expensive, e.g. in cell phones [2]. Full duplex, or simultaneous transmit and receive arrays, usually require circulators, which are bulky, lossy and limited in bandwidth. Additionally, circulators have limited isolation which can be degraded when the impedance of the antenna changes during scanning [3]. Another approach, considered in this paper and illustrated in Fig. 1 is to use switches in each TR module, but use a fraction of the array elements for transmitting, while the remaining elements receive [4] . This digitally-scanned array architecture is reconfigurable in terms of number of T and R elements.

For an in-band full-duplex phased array, a limiting factor is the isolation between the transmitter and receiver paths, which causes a part of the transmit power to leak into the receiver and saturate the LNA, or the analog-to-digital converter (ADC) in the downconversion path. This can be improved with self-interference cancellation (SIC) techniques, which can be implemented in the propagation domain [5], [6], analog domain [7], or/and the digital domain [8], [9]. In most in-band full-duplex systems, multiple SIC techniques are required to achieve significant isolation between transmit and revive paths. For example, the antennas are orthogonally-polarized for lower coupling and digital cancellation is also applied in [10].

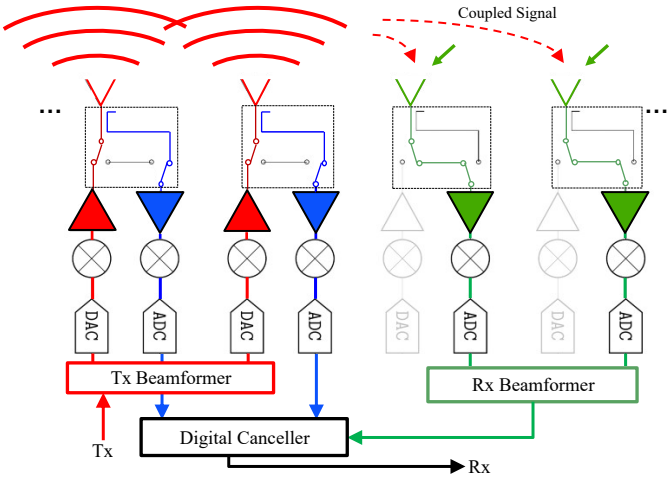

Fig. 1. In-band full duplex digitally-scanned phased array block diagram, where transmitting elements in the front end are shown in red, while the receiving ones are shown in green. The receive path of the transmitting elements, shown in blue, couples a part of the transmitted signal and provides information on self-interference coupling to the digital cancellation circuit.

Figure 1 shows a SIC technique similar to those demonstrated in [11] and [12]. Both propagation and digital domain SIC is incorporated, for a reconfigurable in-band full-duplex phased array with $\lambda_0/2$ spacing at the center frequency, as discussed in [4]. In this architecture, each element-level TR module is either in transmit or receive mode, determined by the switch. In the transmitting elements (shown in red in the figure), the feedback network samples a portion of the transmitted signal and routes it to the transmit-element receiver (shown in blue). After down-conversion, the sampled feedback signal is compared in the digital domain with the received (green) down-converted and sampled signal. The feedback

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network can have several architectures, all requiring high-quality switches that can be easily integrated into the front end elements.

Some examples of published work on RF switches include devices demonstrated in [13] and [14], which show multiple topologies and performance focused on low insertion and high isolation. In this paper, we focus on similar switch topologies, but with performance parameters tailored to the feedback network application. This requires low insertion loss and a specific level of isolation and compression that depend on TR module parameters, e.g. the output power of the transmit PA. Several switches are designed for the purpose of comparison, and then implemented in a 250-nm Qorvo GaN on SiC MMIC process using foundry models.

II. Switch Topologies and Design

For the front-end feedback circuit from Fig. 1, the switches need to meet three key performance metrics. First, the isolation between T and R ports needs to be high to protect the receiver chain while transmitting, but sufficiently low to allow transmit signal sampling for digital cancellation. The switch insertion loss from the antenna port to either R or T ports needs to be low to maintain low noise figure of the receiver. Finally, the switch footprint should be as small as possible to be integrated into the front-end TR module.

The design and fabrication of several switch topologies is performed in Qorvo's 250-nm GaN on SiC process, which has good performance around the deign frequency of 3 GHz. A 3×75 μm switch device, with gate control voltages of 0 V and -30 V for a shorted and open device, respectively, is used to compare the three topologies. Fig. 2 shows the simulated complex impedance between the drain and source for the two states of the RF-grounded gate switch HEMT, obtained from the foundry transistor linear model.

A simple reflective switch using a shunt transistor, shown in Fig. 3(a), requires an impedance transformer, usually implemented with a quarter-wavelength microstrip line. At 3 GHz, this is prohibitively large, so a lumped-element Π network with shunt capacitors and a series inductor is designed, with element values given by [15] and [16]:

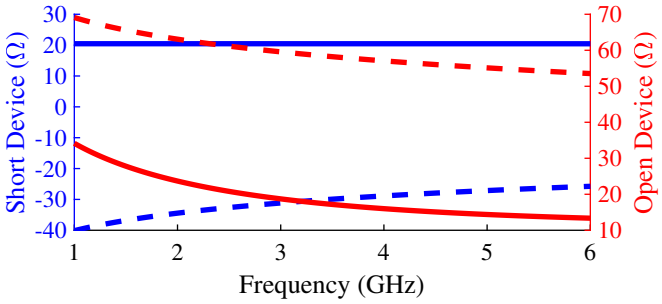

Fig. 2. Impedance of a 3×75 μm switch HEMT in the Qorvo GaN25 process for the shorted device biased at 0 V (blue) and open device biased at -30 V (red). The real part is shown in solid line, and the imaginary in dashed line.

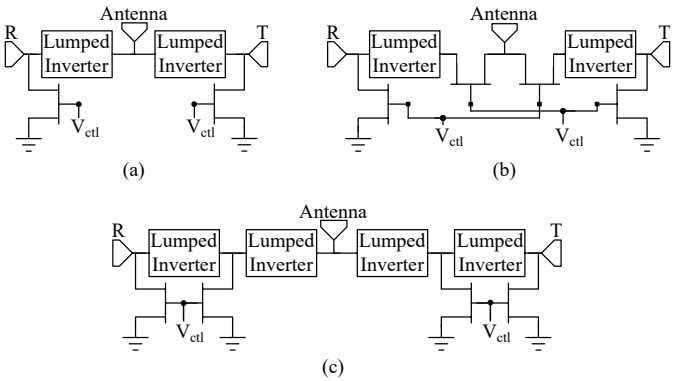

Fig. 3. Circuit schematics of the three switch topologies: (a) simple reflective switch; (b) series-shunt HEMT switch; and (c) dual-shunt HEMT switch.

$$C_{shunt} = \frac{1}{2\pi f_0 Z_0} \quad \text{and} \quad L_{series} = \frac{Z_0}{2\pi f_0}. \qquad (1)$$

These expressions are used to determine values of an inverter that transforms 42+j1.8 Ω to 60-j2.5 Ω and 27-j2.5 Ω to 94-j2 Ω for the ON an OFF states at 3 GHz, respectively. This results in C_{shunt} = 1.1 pF and L_{series} = 2.7 nH. The input impedance $Z_{in} = Z_0^2/Z_L$ is found for the ON and OFF states. For the ON case, looking into the tee network while transmitting, the inverter is loaded with 50 Ω in parallel with an open circuit from the receive path, resulting in Z= 42+j1.8 Ω, found from full-wave simulations. For the OFF case, the receive path is shorted, resulting in Z_L=27-j0.5 Ω. The two values of Z_{in} are then found to be 60-j2.5 Ωs and 94-j2 Ω, respectively. Full-wave simulated Z_{in} for both load impedances is shown in Fig. 4.

Three switch designs are compared using the above impedance transformer, and shown in Fig. 3. In addition to the simple reflective switch consisting of a symmetric single shunt HEMT with an added lumped-element impedance inverter, Fig. 3(a), a symmetric reflective dual-shunt device switch shown in Fig. 3(b) is designed using the same lumped-element inverters. The third design shown in Fig. 3(c) consists of a

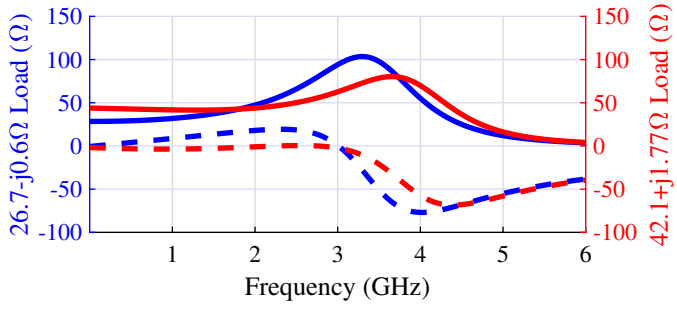

Fig. 4. Lumped-element inverter impedance with C_{shunt} = 1.1 pF and L_{series} = 2.7 nH, showing a zero imaginary part at the design frequency of 3 GHz. These results are obtained with full-wave electromagnetic simulations of the inverter layout.

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symmetric single series and single shunt HEMT, with inverters between the series and shunt device. This topology allows testing of a series and shunt device combination, as well as the biasing networks required for a series and shunt configuration.

The three circuits are then designed in the MMIC process to obtain the smallest footprint, as shown in Fig. 5. The simple shunt switch requires the smallest area ($0.9\times0.9\,\text{mm}^2$), while the shunt-series switch is the largest ($1.4\times0.9\,\text{mm}^2$). The series inductor is the limiting component for reducing the size of the die, resulting in the lumped-element impedance inverter of $0.4\times0.3\,\text{mm}^2$ in size. Due to the tight layout, full-wave electromagnetic simulations are essential and are performed using the 2.5D Cadence AWR Axiem tool. Layouts of the switch and GSG pads take ease of probing into account. For example, no two GSG pads can be on the same side of the die for probing. The grounds of the GSG pads are rotated to decrease the die area. For both circuits in Fig. 5(b) and Fig. 5(c) four DC bias pads are required, and for easier probe measurements the drain biases are tied together. The circuit in Fig. 5(b) consists of a series-shunt configuration, and a bridge and underpass are required for the drain terminals to be connected together.

III. Measured Performance

The MMICs are measured on-wafer using a network analyzer calibrated with Alumina SOLT 2-port standards, with ports aligned and across from each other, while the third port is terminated in a 50 load. The measurements are performed from 1 to 6 GHz to check the broadband performance around the 2.5 to 3.5 GHz operating frequency range. Fig. 6 displays the measured S-parameters compared to the simulated ones. The plotted data shows key performance metrics for the switch feedback network application in the full-duplex array from Fig. 1. Red traces display the insertion loss of the ON path from the transmitter power amplifier to the antenna feed. Blue traces display the isolation between T and R while transmitting, giving a sample of the transmitted signal used as the feedback for self-interference cancellation. Green traces show the isolation of the OFF path from the antenna feed to the transmitter during receiving. Finally, the black curves show the return loss at the antenna feed port in receiving mode of operation.

The measured and simulated performance of the simple shunt switch is shown in 6(b), showing good agreement overall, with only the measured isolation about 5 dB lower than predicted. 6(c) shows performance of the series-shunt switch MMIC, which displays the best match between simulated and measured performance. A low insertion loss, ranging from 1.2 dB to 1.3 dB across the desired bandwidth is measured, along with a return loss better than 10 dB. With an isolation better than 20 dB in the frequency range of operation (2.5 to 3.5 GHz), this configuration allows measurement of a sample of the transmitted signal which is required for the switch feedback network. The improved isolation can be thought of as a filter that only allows the desired signal to be sampled. Finally, Fig. 6(d) shows performance of the dual-shunt configuration.

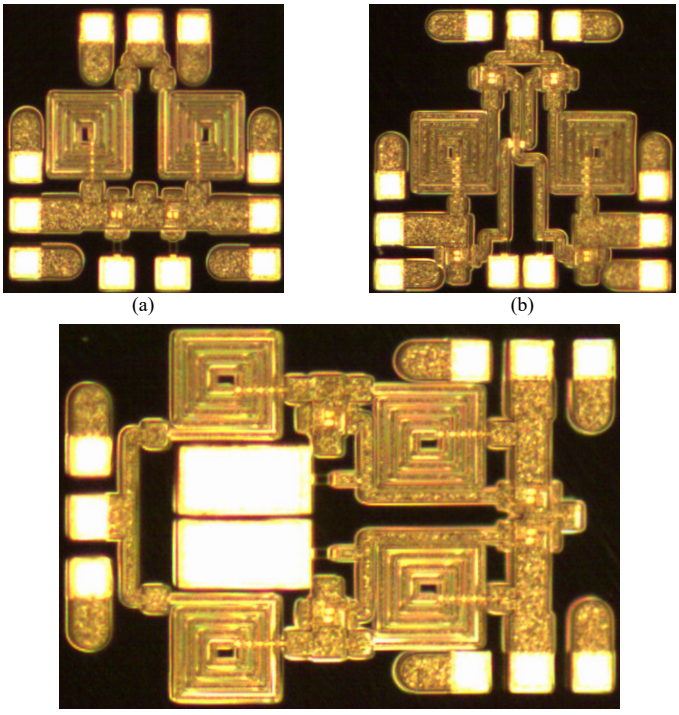

Fig. 5. Photographs of the three fabricated SPDT switch MMICs corresponding to the topologies in Fig. 3: (a) simple reflective switch with an area of $0.9\times0.9\,\text{mm}^2$; (b) shunt-series switch with an area of $1\times1\,\text{mm}^2$; and (c) dual-shunt switch $1.4\times0.9\,\text{mm}^2$ in size.

Measured insertion loss and isolation matches the simulations, however the return loss deviates considerably. A possible cause for this is a poor termination on the third port, which will be determined by repeating the measurements.

IV. Conclusion

In summary, this paper presents three reflective-type, single-pole double-throw (SPDT) MMIC switches designed for operation from 2.5 to 3.5 GHz and intended for a switch feedback network in a phased array module. Due to the relatively low design frequency, lumped elements are used for the passive networks, resulting in compact designs. The reported switch topologies demonstrate an insertion loss below 2 dB across the desired bandwidth with varying isolation based on the topology. Measured performance is compared with simulations, validating foundry transistor and passives models. Depending on the input power sampled from the transmit path, and compression level of the receiver chain, a switch can be designed for desired feedback network performance, with a desired level of isolation.

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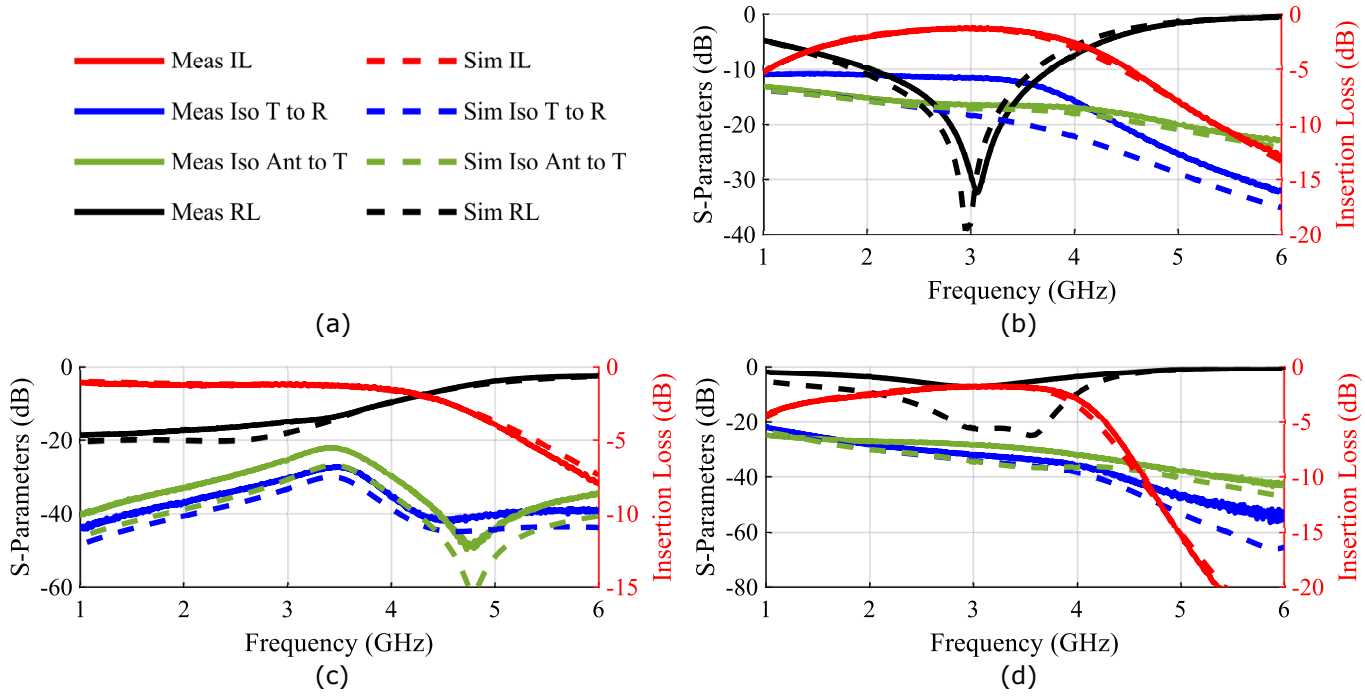

Fig. 6. (a) Key parameters for switch performance. Measured (solid lines) and simulated (dashed lines) performance of the single shunt switch (b), series-shunt switch (c) and dual-shunt switch (d).

REFERENCES

[1] G. W. Stimson, "Introduction to airborne radar, ed," 2014.

[2] G. Hueber and R. B. Staszewski, *Multi-mode/Multi-band RF transceivers for wireless communications: Advanced techniques, Architectures, and Trends*. John Wiley & Sons, 2011.

[3] L. Marzall, S. Verploegh, T. Cappello, M. Roberg, and Z. Popović, "Active mmic circulator performance in a phased-array-like environment," in *2020 50th European Microwave Conference (EuMC)*. IEEE, 2021, pp. 1186–1189.

[4] K. E. Kolodziej, G. A. Brigham, M. A. Harger, B. A. Janice, A. I. Sands, I. Weiner, W. W. Pierre-Francois, J. P. Doane, and B. T. Perry, "Scalable array technologies for converged-rf applications," in *2022 IEEE Radar Conference (RadarConf)*. IEEE, 2022, pp. 1–5.

[5] M. A. Elmansouri, L. B. Boskovic, and D. S. Filipovic, "Compact wideband dual-polarized in-band full-duplex antenna subsystem," *IEEE Transactions on Antennas and Propagation*, vol. 69, no. 11, pp. 7166–7172, 2021.

[6] L. Laughlin, C. Zhang, M. A. Beach, K. A. Morris, and J. Haine, "A widely tunable full duplex transceiver combining electrical balance isolation and active analog cancellation," in *2015 IEEE 81st Vehicular Technology Conference (VTC Spring)*. IEEE, 2015, pp. 1–5.

[7] K. E. Kolodziej, J. G. McMichael, and B. T. Perry, "Multitap rf canceller for in-band full-duplex wireless communications," *IEEE Transactions on Wireless Communications*, vol. 15, no. 6, pp. 4321–4334, 2016.

[8] A. Balatsoukas-Stimming, "Non-linear digital self-interference cancellation for in-band full-duplex radios using neural networks," in *2018 IEEE 19th International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*. IEEE, 2018, pp. 1–5.

[9] K. E. Kolodziej, B. T. Perry, and J. S. Herd, "In-band full-duplex technology: Techniques and systems survey," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3025–3041, 2019.

[10] H. Li, J. Van Kerrebrouck, O. Caytan, H. Rogier, J. Bauwelinck, P. Demeester, and G. Torfs, "Self-interference cancellation enabling high-throughput short-reach wireless full-duplex communication," *IEEE Transactions on Wireless Communications*, vol. 17, no. 10, pp. 6475–6486, 2018.

[11] J. P. Doane, K. E. Kolodziej, and B. T. Perry, "Simultaneous transmit and receive with digital phased arrays," in *2016 IEEE International Symposium on Phased Array Systems and Technology (PAST)*. IEEE, 2016, pp. 1–6.

[12] ——, "Simultaneous transmit and receive performance of an 8-channel digital phased array," in *2017 IEEE International Symposium on Antennas and Propagation & USNC/URSI National Radio Science Meeting*. IEEE, 2017, pp. 1043–1044.

[13] C. F. Campbell and D. C. Dumka, "Wideband high power gan on sic spdt switch mmics," in *2010 IEEE MTT-S International Microwave Symposium*. IEEE, 2010, pp. 145–148.

[14] B. Y. Ma, K. S. Boutros, J. B. Hacker, and G. Nagy, "High power algan/gan ku-band mmic spdt switch and design consideration," in *2008 IEEE MTT-S International Microwave Symposium Digest*. IEEE, 2008, pp. 1473–1476.

[15] M. M. Elsbury, "Broadband microwave integrated circuits for voltage standard applications," Ph.D. dissertation, University of Colorado at Boulder, 2010.

[16] F. Noriega and P. J. González, "Designing lc wilkinson power splitters," *RF interconnects/interfaces*, vol. 18, 2002.

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