Analog Components for Wireless Power Transfer Systems

by

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Wireless power transfer (WPT) is a method of power delivery in which energy is sent from one point to another using electromagnetic fields without conductors. There are many applications in which delivering power through a direct, wired connection is not a viable solution. Some examples include delivering power to areas in which infrastructure has been damaged or charging of unattended sensors hidden behind or within walls and other difficult to reach places. The work presented in this thesis aims to address individual components that are critical to the overall efficiency of a wireless power beaming system. By introducing state-of-the-art and experimental technologies, materials, and design techniques, the key components of a wireless power beaming system are designed and characterized. First, the receiving end is addressed through the design and characterization of a flexible and scalable 10 GHz rectenna array designed using low-cost and unconventional microwave materials. Arrays are scaled to a variety of sizes up to $1\,\mathrm{m} \times 1\,\mathrm{m}$ and demonstrated with weather exposure and ESD protection. Addressing the transmit side of a WPT system, a novel design approach for several multi-watt, high-efficiency Ka-band power amplifiers using on-chip power combining is detailed. Further contributions include the characterization from dc to 50 GHz of a novel and experimental packing technology intended for heterogeneous integration.

Dedication

To Tiffany and Johnny, my ever-supportive mom and dad.

To Spencer, my brother and lifelong friend.

To Rick, Pat, Becky, and Ed, my loving grandparents.

To every single friend and family member who has loved and supported me all these years. I cannot even begin to express my gratitude towards you all. Just know that I will always hold you close in my heart.

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These acknowledgments would be incomplete if I did not express how grateful I am towards my fellow graduate students who have become some of my closest friends. We may not all have began our journeys at the same time, but I count myself incredibly lucky for the time I've gotten to spend with you all. Good times and bad, we have always been there for each other. Thank you for for always encouraging me to be myself and for helping me to build some of my happiest memories. And I hope for many more happy memories to come.

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Chapter 1

Introduction

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1.1 Background and Motivation

Wireless power transfer (WPT) is a method of power delivery in which energy is sent from one point to another using electromagnetic fields without conductors. Between 1886 and 1889, Heinrich Hertz conducted a series of experiments using a spark-gap transmitter and a receiving loop antenna to validate James Clerk Maxwell's prediction of electromagnetic waves [1]. These experiments became the first documented demonstrations of propagating electromagnetic waves between a dedicated transmitter and receiver. In the 1890's, Nikola Tesla began conducting experiments in wireless power through near-field capacitive and inductive coupling using resonant transformers known as Tesla coils [2]. Tesla's method of resonant inductive coupling has since been adapted to many consumer devices in the modern day, including common appliances like wireless phone chargers. However, it was not until William Brown's invention of the rectenna at Raytheon

in 1964 that the first ever long-range, demonstrations of directed power-beaming were performed [3]. In 1975 William Brown was the technical director of a JPL-Raytheon program in which over 30 kW of dc power was collected at a large rectenna array consisting of dipole antenna elements integrated with Schottky diodes [4]. RF power at 2.388 GHz was beamed over a distance of 1.54 km and rectified with a conversion efficiency of 84% [5]. Fig 1.1 gives visual representation to these innovations over history.

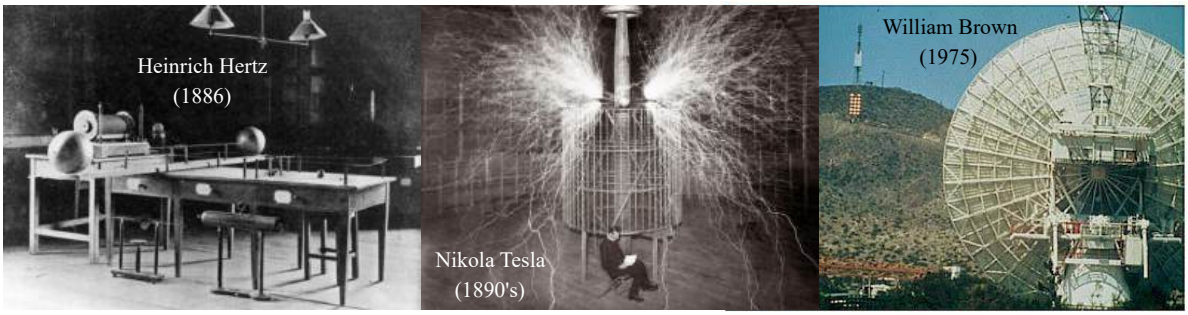


Figure 1.1: (a) Photograph of a tabletop setup used by Heinrich Hertz in his experimental proof of electromagnetic radiation. (b) Photograph of one of the high voltage resonant transformer, or Tesla coil, that Nikola Tesla used to wirelessly transmit power. (c) Photograph of the Goldstone antenna used by Raytheon and JPL to beam 30 kW toward a rectenna designed by William Brown 1.5 km away.

WPT is particularly useful when a wired connection is either impractical or impossible, e.g. for a device embedded within a wall or a device that rotates. Where it is possible to implement wired-connections, especially over short distances where cable loss is minimized, it is almost always more efficient to do so. However, there are many applications where delivering power through a direct, wired connection is not a viable solution. For example, emergency relief power can be delivered to key areas via drone-mounted transmitters in areas where natural disasters have struck and potentially damaged infrastructure normally used for power transmission. In such scenarios, it is important that power can be delivered quickly and to difficult-to-reach areas. Similarly, contested environments such as forward military camps need a means of emergency power delivery to operate communication equipment in the event of outages [6, 7]. Another application is integration with

unattended sensors embedded in walls or other difficult-to-reach places that are often powered using batteries. By integrating low-power harvesting rectennas, batteries can be continuously charged without the need for maintenance or direct cable connections [8]. Additionally, more directive directive power beaming with a dedicated transmitter can also be used to periodically charge such devices by temporarily scanning a beam over them. As hinted at by the applications discussed above, there are several different types of WPT ranging from near-field to far-field. There are also some examples of mid-field WPT, specifically for medical applications in which RF is propagated through the body. Mid-field WPT is unlike near-field WPT in the sense that transmitted energy is primarily carried in propagating modes instead of evanescent, exponentially decaying fields [9].

Near-field WPT occurs at distances where power is reactively coupled to both the transmitter and receiver, generally at distances much smaller than the Fraunhofer distance:

$$d_F = \frac{2D^2}{\lambda_0}, \tag{1.1}$$

where D is the largest dimension of the radiator and λ_0 is the wavelength. Methods of near-field WPT rely primarily on either inductive or capacitive coupling across very short distances compared to those of far-field WPT. Applications range from relatively low power levels such as charging a cellphone or an electric toothbrush, to very high power levels such as charging an electric vehicle. As in the case of power beaming, these systems are typically narrow-band and focus on achieving the highest possible system efficiency. Near-field WPT systems are best suited for applications where direct electrical connections are detrimental such as for moving or rotating mechanical components or to prevent short-circuits in situations where exposure to moisture is expected, such as charging stations for underwater ROVs.

Far-field WPT refers to any case in which the received power can be thought of as a plane wave and there is no reactive coupling between the source and the receiver. This includes both power beaming and low-power harvesting. Power beaming involves a dedicated power transmitter and power receiver in the form of a rectenna integrated with power management circuitry. A rectenna is

a type of antenna integrated with one or more rectifiers intended to receive RF energy and convert it into dc power. Both the transmitter and rectenna are usually designed to be narrow-band and directional to maximize the efficiency of power transfer over a long distance. In contrast, power harvesting requires no dedicated transmitter and instead aims to rectify the low level of ambient microwave energy from various sources in the environment. Rectennas designed for harvesting generally have a wide bandwidth and are not directional. This is done to maximize the amount of power rectified across the available frequency and angle of incidence.

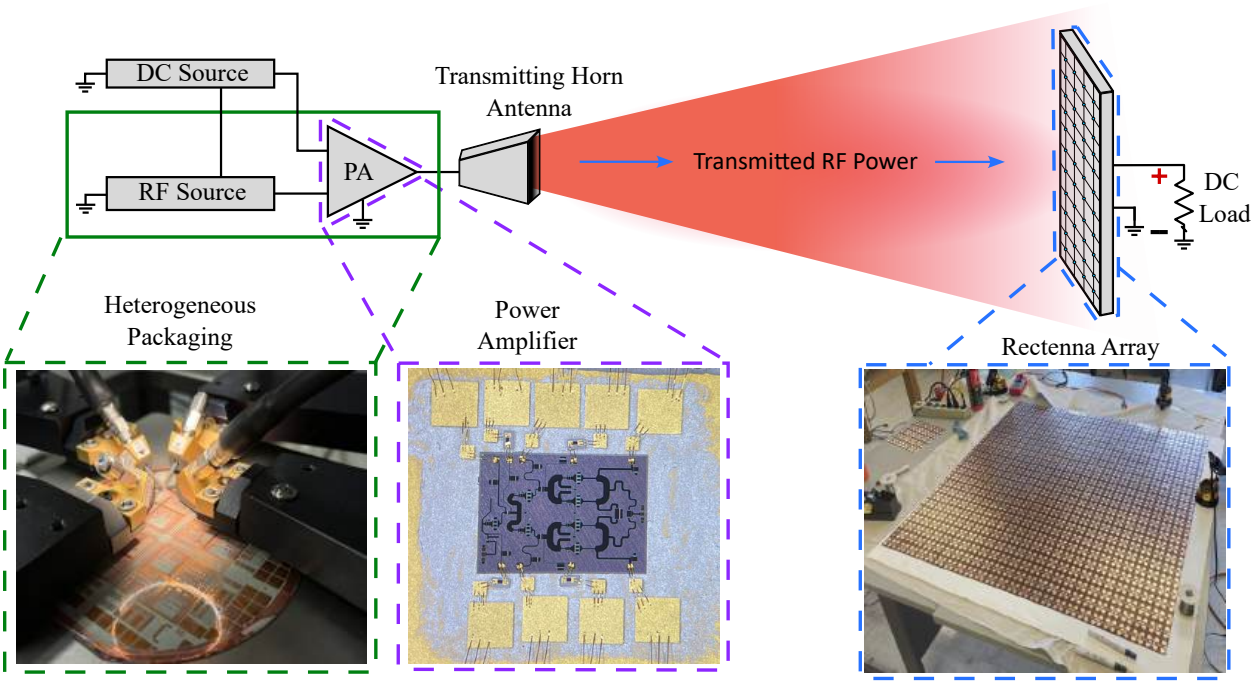


Figure 1.2: Diagram of a wireless power transfer system highlighting key components that are further discussed in subsequent chapters. These components include the following: (1) a rectenna array which is discussed in Ch. 2 and Ch. 3; (2) solid-state power amplifiers used in the transmit chain which are discussed in Ch. 5 and Ch. 6; and (3) packaging intended for heterogeneous integration of technologies in a solid-state system which is discussed in Ch. 4.

The mode of wireless power transfer most relevant to the topics discussed in this thesis and depicted in Fig. 1.2 is far-field power beaming. As seen in the figure, there are several key components of this simplified WPT system that are highlighted, including the rectenna, solid-state power amplifiers, and low-loss packaging. The remainder of this chapter will cover the importance

of each of these components to the overall system, and the subsequent chapters will discuss each of these topics in much greater detail.

1.2 Rectennas

Rectennas or "rectifying antennas" are a crucial component of any far-field WPT system. As mentioned previously, rectennas consist of one or more antenna elements integrated with one or more rectifying elements and are designed to capturing incident RF energy and convert it into dc power. Given this broad definition, it is easy to imagine the vast amount of variation across rectenna designs, and how they can be tailored to best fit specific applications. For example, a rectenna designed for power harvesting over a broad bandwidth would likely make use of an array of broad-band, low-gain antenna elements such as the spiral arrays discussed in [10] and displayed in Fig 1.3a. Alternatively, arrays of narrower bandwidth and more directional antenna elements are better suited for long-range power beaming, such as the patch antenna arrays discussed in [11] and displayed in Fig 1.3b.

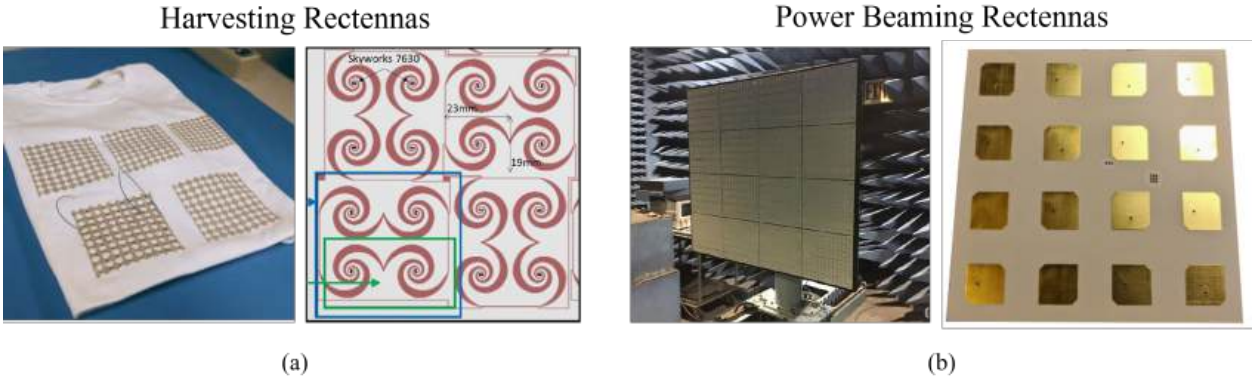


Figure 1.3: (a) Two examples of rectennas designed for low-power harvesting. On the (left) is a 2-5 GHz textile-based bowtie array [12] and on the (right) is a 2-8 GHz spiral rectenna array [10]. (b) Two examples of 10 GHz patch-based rectenna arrays designed for long range power beaming. The design on the (left) is discussed further in [11] and the design on the (right) in [13].

Both of the examples given in the figure describe arrays of planar elements, but rectennas do not have to consist of an array of elements, and can be implemented using any type of antenna from

horns, to reflectors, to Vivaldis, to dipoles and monopoles. Indeed, it is the case that most examples of rectennas are planar arrays, and this is for the same reasons that other forms of electromagnetic power harvesting, such as solar, are as well. Primarily, it is advantageous to cover a wide surface area to capture as much incident power as possible, and planar elements provide low form factor and the potential for conformability. Furthermore, arrays of many elements imply scalability, and can be more easily adapted to the size required for a specific application.

Beyond the selection of antenna elements, the choice of rectifiers and how they are integrated is an important consideration. Based on published literature, a majority of rectennas make use of Schottky diodes as their rectifying elements. Schottky diodes are very well suited for rectification at microwave frequencies due to their low junction capacitance, which results in low loss and fast switching speeds (tens of nanoseconds to as low as picoseconds). This is owed to the metal-semiconductor junction of the Schottky barrier, which means that the diode operates with majority charge carriers (electrons) only and, in principle, has no reverse recovery time unlike p-n junction diodes [14]. Fig. 1.4 shows both a simple schematic for a diode-based rectifier circuit and a photograph of one implemented in microstrip with surface-mount components as a test circuit for work discussed in Chapter 2.

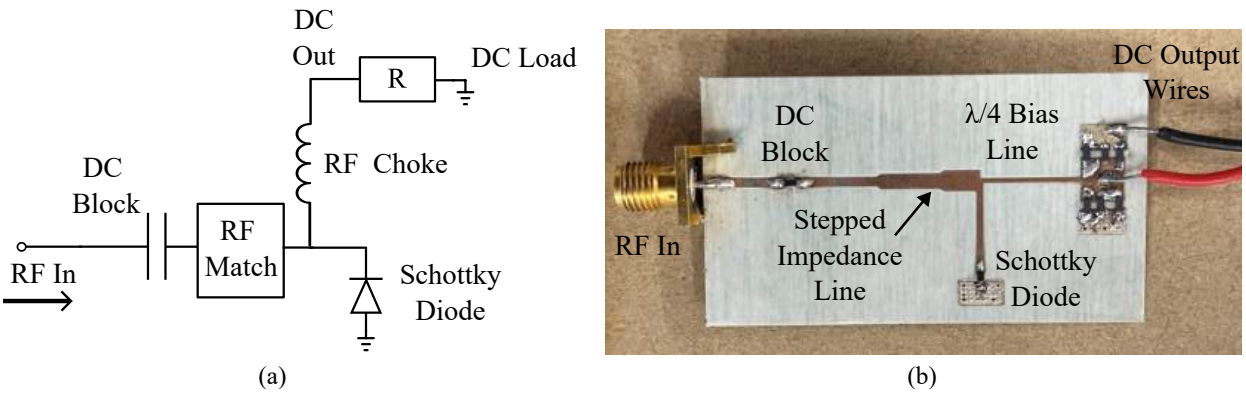


Figure 1.4: (a) Simple schematic of a rectifier circuit using a Schottky diode. (b) Photograph of a 10 GHz rectifier circuit implemented in microstrip with surface mount components.

An alternative to Schottky diodes, and diodes in general, is the use of transistor rectifiers.

Transistor rectifiers, specifically ones based off of a principle referred to as "time-reversal duality", can be used to operate at the same frequencies and power levels as high-performance power amplifiers. The central idea is that a power amplifier can be operated in reverse as a rectifier with the PAs nominal RF output functioning as the RF input, and the drain bias line functioning as the dc output. This principle is discussed in greater detail in [15] for dc-to-dc converts and in [16] for high-efficiency power amplifiers. In essence, an RF-to-dc conversion efficiency is approximately equivalent to the PAE of the converted PA at an RF input power equal to the nominal output power of the converted PA. Furthermore, such a rectifier can be made self-synchronous by implementing a highly reflective termination at the PA input and coupling a small amount of power from the drain to the gate of the transistor. This type of rectifier is best suited for higher incident power densities than Schottky diodes and can achieve high conversion efficiencies up to millimeter-wave frequencies. However, these rectifiers are more complex to integrate, are generally more costly than diodes, and require external dc power supplies for gate biasing. Fig 1.5 shows a simple schematic and photograph of a GaAs MMIC self-synchronous transistor rectifier at X-band that achieves 60% conversion efficiency from [17].

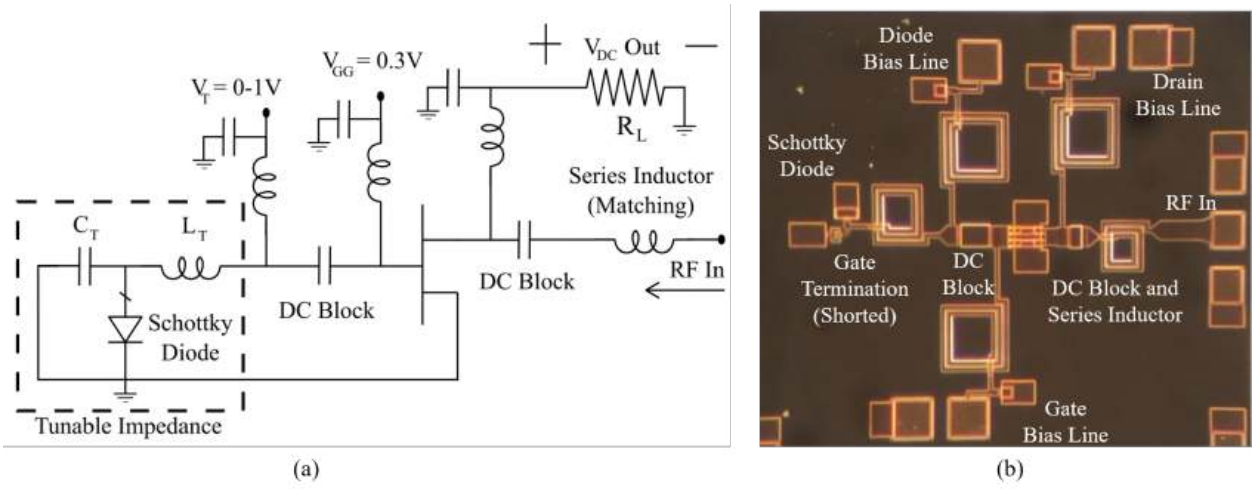


Figure 1.5: (a) Schematic of a PA-based self-synchronous transistor rectifier designed at X-band. (b) Photograph of GaAs MMIC implementation of the transistor rectifier from [17].

The rectenna arrays discussed in Ch. 2 and Ch. 3 of this thesis are scalable and mechanically

flexible patch antenna arrays designed to operate at 10 GHz. A photograph of a fabricated 1 m × 1 m array can be seen on the receive side of the system diagram in Fig 1.2.

1.3 Packaging and Heterogeneous Integration

Packaging is an important part of any RF system, be it for WPT, radar, or communications. In all high-frequency applications it is desirable to have low-loss packages and interconnects to allow the critical components of a system to interface with one another. In the case of the simple WPT system detailed in Fig. 1.2, low-loss packaging is critical to allow different solid-state components to interface with one another. As mentioned previously, efficiency is arguably the most important metric for a directive power beaming system. Not only is the efficiency of each individual component critical, such as power amplifiers, RF sources, and rectifiers, but the loss in each interconnect between components degrades overall system efficiency. This is particularly relevant for the power amplifiers connected to the transmitter; only 1 or 2 dB of loss in the transitions between the power amplifier output(s) and the antenna(s) can result in significant power dissipation. Furthermore, different technologies used for different components such as the RF source in the form of a GaAs HBT local oscillator and high-power GaN power amplifiers can be integrated together using a technique known as heterogeneous integration.

Heterogeneous integration, or HI, is an advanced form of packaging that is intended to combine separate RF components made using different technologies and manufacturing processes into a single higher-level assembly. Advantages of HI include: (1) directly interfacing multiple technologies best suited for their specific function with one another; (2) the ability to save valuable chip space by offloading passive components such as filters and matching networks to the packaging process; and (3) compact integrated circuits and PCBs using low-loss interconnects. Some examples of heterogeneous integration technologies described in previous work are shown in Fig. 1.6.

The work discussed in this thesis is focused on the design and characterization of low-loss, grounded coplanar waveguide (GCPW) interconnects using a novel and experimental packaging technology useful for off-chip combining. Specifically, Chapter 4 describes the State-of-the-art

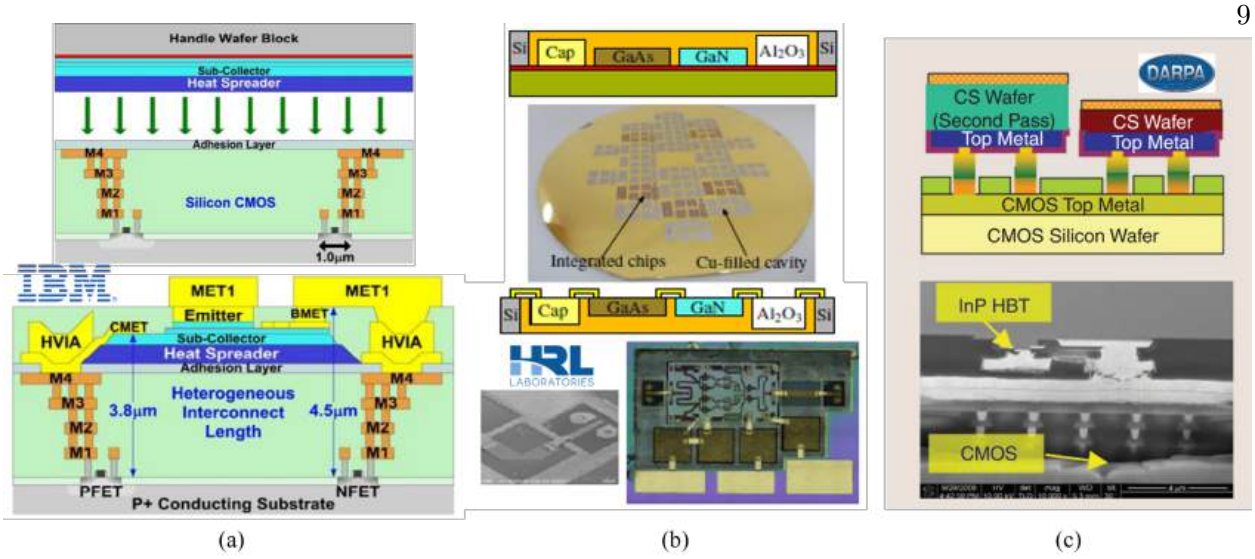


Figure 1.6: Diagarams showing the different layers of multiple different heterogeneous integration technologies including; (a) an InP DHBT integrated on an RF-CMOS process developed by IBM [18]; (b) the metal-embedded chip assembly (MECA) developed by HRL [19]; and (c) the micrometer-scale assembly DAHI/COSMOS program from DARPA [20, 21, 22].

Heterogeneous Integration Process, or SHIP, developed by Applied Materials and Qorvo. This is a 6-metal layer packaging process designed to operate from dc to 50 GHz. The chapter discusses in detail multiple GCPW-based interconnects in addition to several other structures including couplers and filters. A photograph of a SHIP wafer under test is shown on the left of Fig 1.2.

1.4 GaN-on-SiC Multi-Watt Power Amplifiers

A critical component in the transmit end of a long-range power beaming system are high-efficiency power amplifiers capable of high output power. In the recent past, many high-output power transmitters for WPT have made use of vacuum tube amplifiers as RF power amplifiers or sources for high-power transmitters, e.g. in [23]. For such high-power applications, technologies such as klystrons and crossed-field amplifiers are commonly used, as can be seen in Fig 1.7. Although more than 100 years old, vacuum tube technology continues to be relevant in high-power microwave applications to their high power density and good efficiency [24]. However, recent advances in milimeter-wave technologies using III-V compound semiconductors have helped to make a case for

using solid-state power amplifiers instead. In particular, new gallium-nitride (GaN) technologies have made possible output powers on the order of 10 W CW at Ka-band from single chips only a few square millimeters in area [25]. Fig 1.8 from [26] shows the trend of saturated output power for various PAs across frequency for different semiconductor technologies.

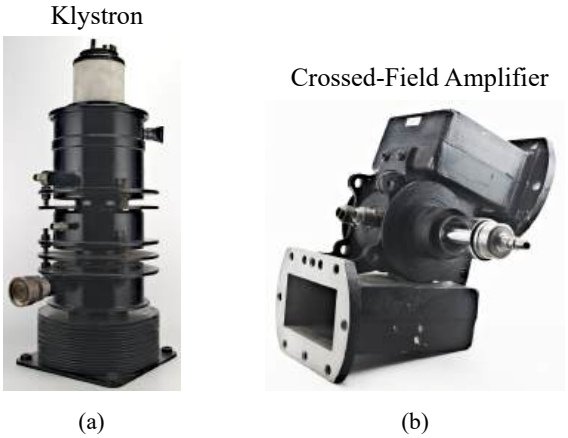


Figure 1.7: Photographs of two different types of vacuum tube amplifier. (a) features a klystron amplifier and (b) features a cross-field amplifier. Both are capable of kilowatts of output power in CW operation.

While the efficiencies of solid-state power amplifiers are comparable to the efficiencies of many tube amplifiers, the output power of a single chip is nowhere near that of tube amps. However, there are still several advantages of solid-state technologies that, combined with recent advances in power density, make them competitive.

(1) One of the biggest advantages of chip-based power amplifiers is scalability. Using off-chip power combining in the form of low-loss packaging as mentioned previously, or waveguide power combiners which will be discussed as future work for this thesis, allows scaling of any number of PAs to suit the application.

(2) Because many of these devices are often combined together, solid-state combined PAs have the added benefit of graceful degradation. This means that even if a handful of chips stop working, the system as a whole will not fail.

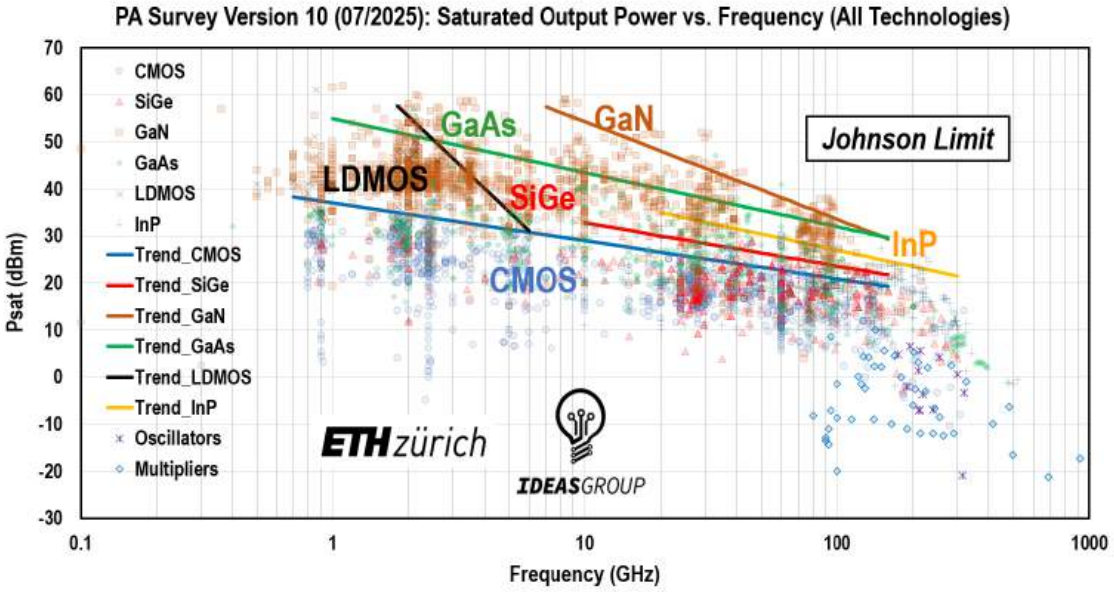


Figure 1.8: Graph showing the saturated output power of various power amplifiers between 500 MHz and 1 THz across different technologies [26].

(3) Finally, solid-state technologies are more compact and lighter than vacuum tube technologies. Depending on the number of chips combined for an application, this could mean a much smaller overall form factor, even taking into account external dc power supplies. Low volume and weight are additionally important for any power amplifier installed on an aircraft such as a drone or satellite, both for WPT and communications systems.

The solid-state power amplifier designs discussed in this thesis each have a narrow bandwidth centered around 32 GHz. Although these designs were originally intended for use in deep-space satellite communication, their high output power and efficiency make them perfectly suited for power beaming at Ka-band. An example of a fabricated chip that is discussed in further detail in Chapter 5 can be seen in the middle of Fig. 1.2.

1.5 ICP Reactive Ion Etching for Semiconductor Manufacturing

An additional important factor, not featured in Fig. 1.2, is semiconductor manufacturing used for diodes and transistors. In particular, one of the critical steps in the manufacturing process

involves etching the semiconductors to selectively remove material and create patterning. Reactive ion etching (RIE) is one method of semiconductor etching that uses plasma to remove unwanted material through the bombardment of energetic ions as described in [27, 28]. RIE systems typically work by using ignition coils to generate an inductively-coupled plasma (ICP) which serves as the reactive ion source. Fig. 1.9a shows a photograph of a commercial RIE plasma etching machine from Lam Research. Reactive ion etching is highly anisotropic compared to chemical etching, allowing for a high degree of precision for structures with large vertical aspect ratios and avoiding undercut [29] as shown in Fig. 1.9b.

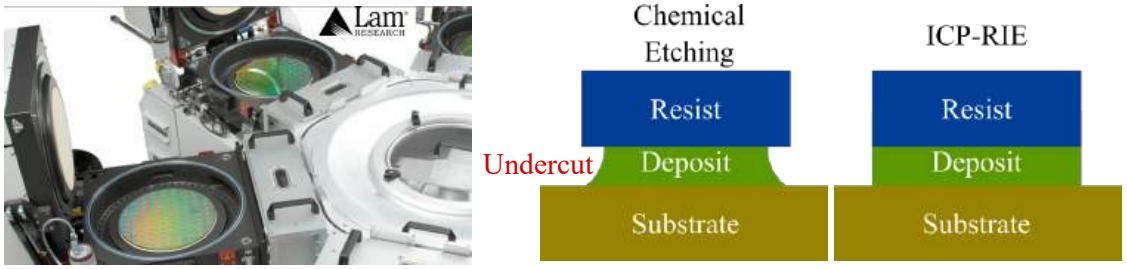


Figure 1.9: (a) Photograph of a RIE plasma semiconductor etching machine sold by Lam Research. (b) Graphic showing the lack of undercut when using RIE compared to chemical etching.

Demands on semiconductor devices, including higher voltages, faster switching speeds and higher efficiency, translate to requirements for more precise manufacturing processes such as deeper etching, higher aspect ratios and better wafer uniformity [30]. Each of these demands is relevant to the motivation of this thesis, and one way to help meet them is by improving the RIE plasma system.

Although not a main section of this thesis, Chapter A, the appendix, describes work done to improve the uniformity and efficiency and uniformity of the ignition coils for an ICP RIE system developed by Lam Research.

1.6 Thesis Outline

The work presented in this thesis aims to address individual components that are critical to the overall efficiency of a wireless power beaming system. Through the use of state-of-the-art and experimental technologies and techniques, the key components highlighted in Fig 1.2 are designed and characterized.

Chapter 2 presents the design and characterization of a scalable, and flexible 10 GHz rectenna subarray using unconventional microwave materials. The rectenna is designed to be low cost and durable, with a detailed description of the design process provided.

Chapter 3 details the scaling of the subarrays presented in Ch. 2 to full rectenna arrays up to $1\,\mathrm{m} \times 1\,\mathrm{m}$. Various experiments with the arrays are discussed including weather and ESD proofing, varying dc combining schemes, and two-tone signal testing.

Chapter 4 presents work done using an experimental packaging technology designed for heterogeneous integration. Design, simulation, and measurements of various interconnects and test structures from dc to 50 GHz are discussed.

Chapter 5 describes two Ka-band 5 W power amplifiers designed using the WIN Semiconductors 120 nm GaN-on-SiC process. Measurement details for the first design are provided and inform decisions made for the second design.

Chapter 6 presents three different Ka-band PA designs using bus-bar power combiners using both the Qorvo Qgan15 150 nm and HRL T3L 40 nm GaN-on-SiC processes. Comparison of devices and design choices are compared across technologies.

Chapter 7 summarizes the thesis and details future work for each of the topics discussed.

Appendix A presents the design and simulation of a pair of ignition coils for an inductively coupled plasma etching system for improved efficiency and field uniformity.

Chapter 2

A 10 GHz Scalable and Rugged Rectenna Array

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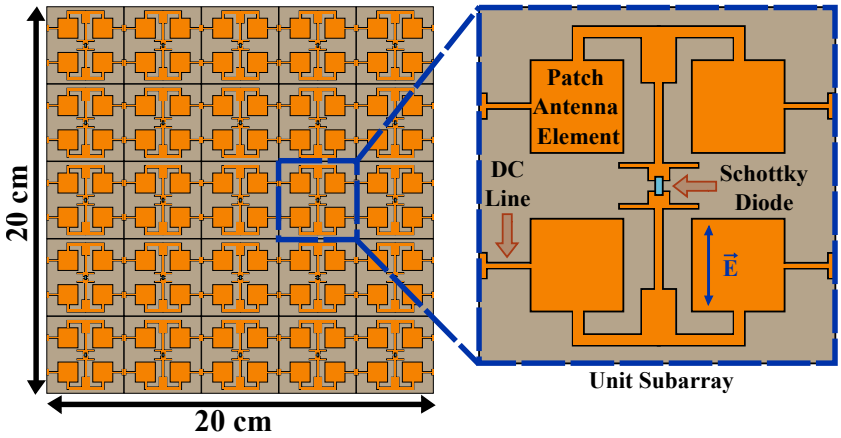
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2.1 Introduction

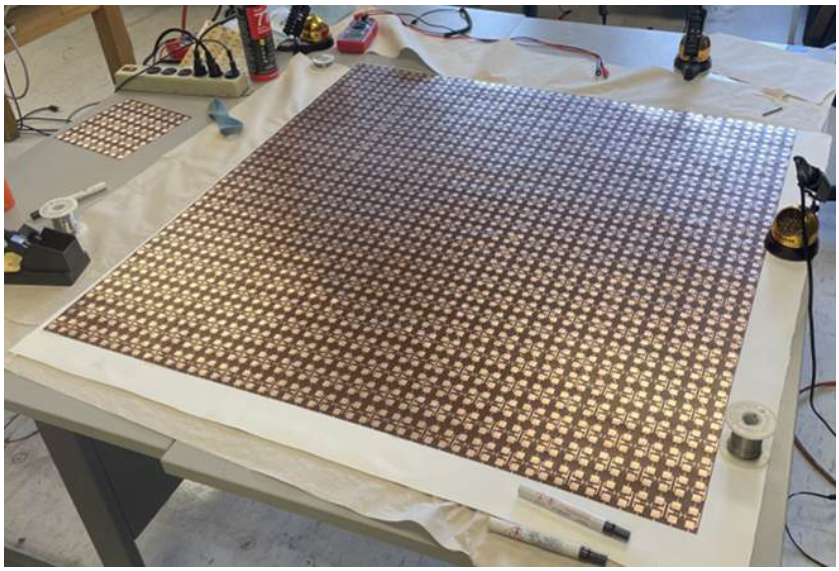
In the past few decades, many authors have published on rectenna arrays for a wide range of far-field wireless powering applications, including terrestrial and space-based power beaming and low-power harvesting for unattended sensors and internet of things (IoT). Summaries of the technology and analysis methods for these systems can be found in e.g. [31, 32, 33]. Depending on the application, requirements for power handling, frequency of operation and bandwidth can vary, and a variety of receiving rectifier antennas and arrays have been demonstrated.

The majority of demonstrations are narrowband at lower microwave frequencies at or below 5.8 GHz [34, 35, 36, 37]. A greater than octave bandwidth textile-based wearable rectenna array for 2–5 GHz harvesting is discussed in[12]. Higher-frequency arrays include an early broadband 2–18 GHz harvesting array [38] with 64 dual-circularly polarized spiral rectennas demonstrating 20% efficiency at a 100 μW/cm^2 power density. At a higher power density of 10 mW/cm^2 a conformal 10-GHz patch rectenna array for powering piezoelectric tomography sensors on aircraft showed 50% efficiency [39]. Another example of a flexible/conformal X-band rectenna array is described in [**?**], achieving up to 55% conversion efficiency with 100 mW/cm^2 incident power density at 8.7 GHz. A planar 3-element array in [40] at 9.3 GHz demonstrates 21% efficiency at 245 μW/cm^2 power density using a rectenna fabricated on FR4, a comparatively low-cost RF substrate. A 16-element circularly-polarized patch array feeding a single rectifying element measured 50% conversion efficiency at a very low incident power density of 5 μW/cm^2 for harvesting power from satellites [13]. Work done for a similar application with scalable arrays for satellite-to-earth power beaming at 10 GHz using higher power densities achieves 39% conversion efficiency at 1 W/m^2 power densities [11]. Additionally, a very high-power (1.6 kW) terrestrial beaming demonstration is reported in [23] showing conversion efficiencies up to 73% at X-band. A limited number of rectennas and rectenna arrays have been reported above X-band, and some examples include [41, 42, 43].

In this research, we demonstrate the design and characterization of a scalable 10-GHz rectenna subarray as shown in greater detail in Fig. 2.1. The arrays are fabricated on foam supporting a flex single-sided metalized substrate, with a copper fabric ground plane, making scaling of flexible arrays possible. The primary motivation for such a rectenna array is emergency power delivery from an airborne transmitter (e.g. a UAV) to a distant energy-denied environment (e.g. earthquake region at night). In such a scenario, it is desired to have easy deployment, low cost and easy storage. Scalability is also important to accommodate varying power densities and electrical load needs. Fig. 2.1a shows a 25-rectifier array with a 4-antenna unit subarray shown in more detail, and Fig. 2.1b shows a photograph of a fabricated 625-rectifier array. The remainder of this chapter discusses in detail the design methodology and characterization of the rectenna unit subarrays



(a)



(b)

Figure 2.1: (a) Layout of a 10-GHz 5×5 rectenna array featuring 25 modules. Each rectenna module includes 4 antenna elements and a single Schottky diode rectifying element. The dc collection lines are connected to the RF nulls of the linearly-polarized patch antennas. (b) Photograph of 1m by 1m scaled array with 625 diodes.

and the following chapter discusses environmental considerations and scaling to larger array sizes including $(6.7\lambda)^2$, $(20\lambda)^2$, and $(33.3\lambda)^2$ arrays with 25, 225 and 625 rectifying elements, respectively.

2.2 Unit Subarray Design

For energy-denied environments, deployable and rugged power receivers that can be powered from UAVs are a promising means of delivering emergency power. Materials used for most rectenna arrays to date are not flexible or weather-resistant, and the designs are not always scalable. Therefore, new unconventional materials are of interest, and new types of designs required. The design starts with nonlinear rectifying device characterization nonlinear and the design of the dc collection network, followed by antenna design.

2.2.1 Material Selection

Our solution uses a stack-up of flexible materials that can be rolled like an exercise mat for storage, and quickly unrolled to a flat surface when deployed as shown in Fig. 2.2. The requirement to make this design resistant to outdoor elements and easily manufacturable limits the choice of substrates and circuit connections. A number of different material choices were initially considered. Fig. 2.2 shows that there are four layers in the stack-up to consider: (1) a layer of conductive traces which will form the antennas and matching networks; (2) a thin dielectric layer on which the conductive traces will be etched; (3) a thicker, bulk dielectric layer; (4) a conductive ground plane. The first bulk dielectric explored was a very low-density, commercial packing foam chosen for its very low cost and low loss due to being mostly air. However, the mechanical strength of the foam proved too much of a detriment both in terms of tear, heat, and water resistance. Instead, a PTFE (polytetrafluoroethylene) based foam is selected to make up for the lack of resilience of the packing foam without compromising significantly in terms of loss. Copper fabric is selected as the ground plane material for its high degree of flexibility, tear resistance, and high conductivity. Initially, the copper fabric was also used to fabricate prototype antenna elements that were adhered to a foam substrate. However, it was found that the level of precision and repeatability of these copper fabric elements (shown in Fig 2.3) were not sufficient for X-band arrays, and therefore focus was shifted to thin, metallized substrates which can be milled or etched. For this purpose, polyimide is a suitable

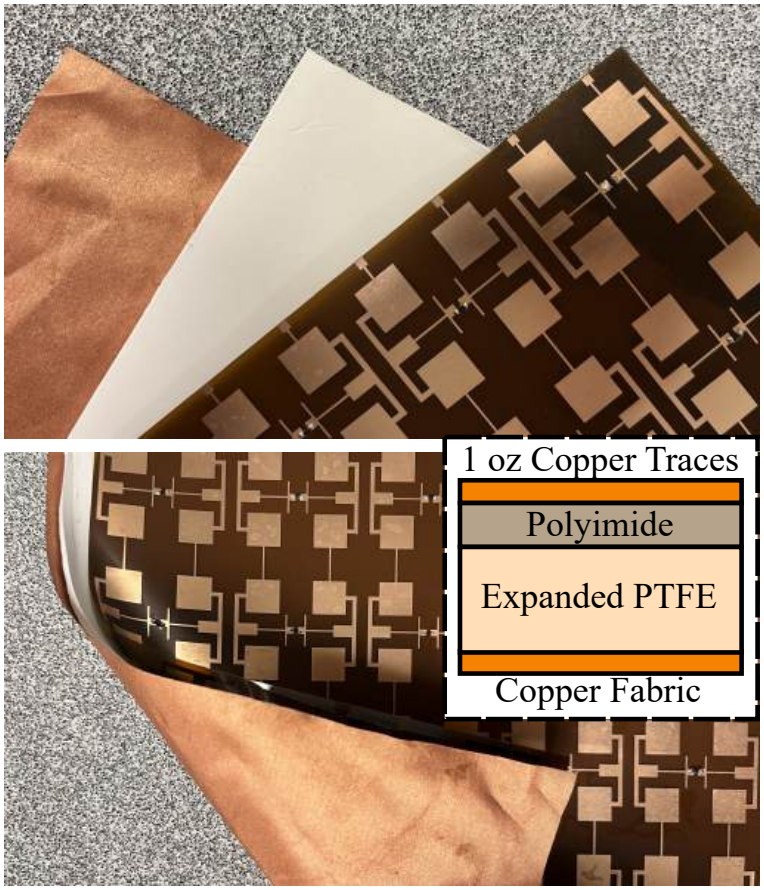


Figure 2.2: Photographs showing layers of rectenna materials from left to right: copper fabric ground plane, EPTFE support substrate, polyimide substrate with milled 1 oz copper and the flexibility of the materials used to construct the rectenna. A single patch element size is 10 mm by 10 mm. A diagram of the material stackup is also included for reference.

choice due to its use in flexible circuit boards and its well-known electrical properties at X-band. Further details regarding the selected materials and construction of the stack-up are as follows:

- ♣ A 5 mil thick, flexible polyimide substrate (Panasonic RF770) with single-sided 1 oz copper cladding is milled to create the antenna and microstrip feeding elements for the rectifying diode to be soldered to. The relative permittivity and loss tangent of the polyimide substrate at X-band are 3.2 and $\tan\delta = 0.002$, respectively.

- ♢ The flexible support substrate, between the polyimide and the ground plane, is 2-mm expanded PTFE (EPTFE) foam, which has a relative permittivity of approximately 1.4 and



(a) (b)

Figure 2.3: Photographs of simple copper fabric patch antennas adhered to a low-density packing foam substrate. (a) Shows an edge-fed patch with a single transmission line feed while (b) shows a segmented transmission line feed connected to a slot-loaded patch antenna. The black substance is a conductive glue used to connect pieces of copper fabric.

$\tan\delta = 0.002$ at X-band. This material is hydrophobic and commonly used for water-tight gaskets, and can also withstand extreme temperatures found in an outdoor environment.

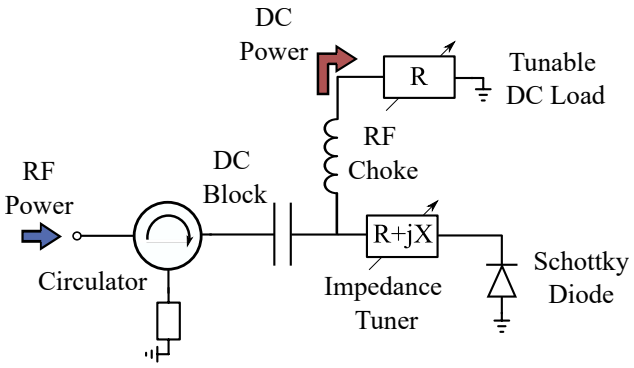
♠ The ground plane is composed of flexible copper fabric, approximately 50 μm thick. It is adhered to the bottom of the EPTFE support substrate using 3M spray-on adhesive. The thin polyimide layer is adhered to the top of the support substrate.

♡ Packaged Si Schottky diodes (Skyworks SMS7621-079) are soldered to the metal traces of the polyimide layer. This diode is chosen for its frequency range (up to 24 GHz) and its low turn-on voltage enabling unbiased rectification. Additionally, the SMS7621-079 is one of few Schottky diodes with a nonlinear model at X-band.

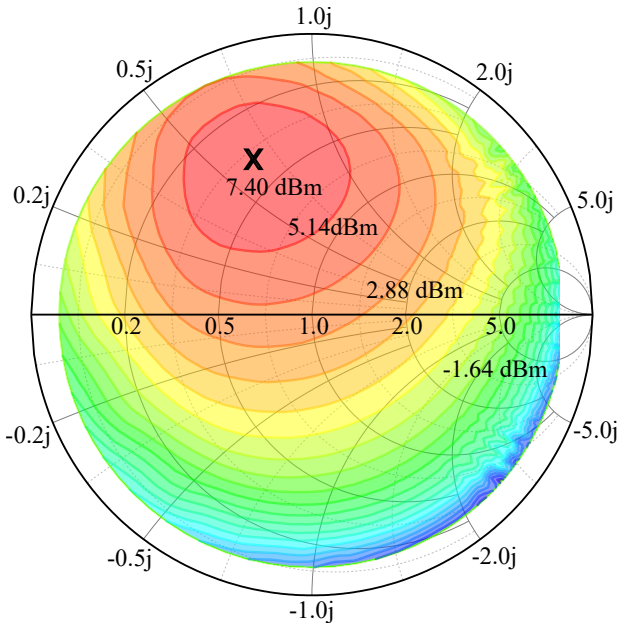
2.2.2 Rectifier Diode Characterization

The first step in the design, which influences all subsequent steps, is characterizing the chosen rectifying element. Here the Skyworks SMS7621-079 Schottky diode is characterized through

simulated load pull using Cadence AWR harmonic balance with a Modelithics nonlinear model. The simulation schematic is shown in Fig. 2.4a and is used to determine both the optimal RF impedances and dc loads across input power that result in the highest RF-dc conversion efficiencies.



(a)



(b)

Figure 2.4: (a) Schematic of a simulation setup for characterizing a diode as a rectifier. For a fixed frequency and input power, both the dc load and presented RF impedance are swept to determine the point of optimal efficiency. (b) Example simulated source pull contours at 10 GHz of the Skyworks SMS7621-079 Schottky diode showing dc output power increasing from blue to red. The cross shows the RF impedance presented to the diode for maximum dc output power at an RF input power of 10 dBm and a dc load of 270 Ω, resulting in 55% conversion efficiency.

For a set frequency, input power, and dc load, the RF impedance presented to the diode is

swept to generate source pull contours as shown in Fig. 2.4b. This process is iterated over many different combinations of dc load resistance and input power level to determine where the diode operates with the highest conversion efficiency at the design frequency of 10 GHz. For example, the simulated optimal impedance to present to the diode that results in 55% conversion efficiency is $Z_{\text{diode}} = 25 + j35\,\Omega$ assuming 10 mW of input power with a dc load of 270 Ω.

2.2.3 Antenna and Subarray Design

After characterizing the rectifying element, antenna elements are chosen to both suit the application and to present the ideal RF impedance to the rectifying element. Additionally, the antenna element can be chosen to provide RF isolation for dc extraction by utilizing built-in RF nulls. Antennas are backed by a ground plane and the geometry and full-wave simulated electric field magnitude in the plane immediately below the metalization are shown in Fig. 2.5. Antenna element designs exhibit RF nulls that can be exploited for dc extraction. The patch antenna elements are chosen for a single linearly-polarized design focusing on RF combining 4 antenna elements to a single diode per unit subarray.

All design and simulation of antenna elements are done using ANSYS HFSS full-wave 3D solver. Initial designs focus on patch antenna elements for their simplicity. At its resonant frequency, a linearly-polarized patch antenna has a near-zero electric field magnitude along its centerline, parallel to the feeding edge as shown in Fig. 2.5. If a dc-tap line is placed along this null, RF current will not be able to flow, creating a dc-only path where rectified power can be extracted.

With a range of impedances gathered through simulated source pull of the diode model, patch antennas are designed using the material stackup discussed previously with a target frequency of 10 GHz. It is found that with the chosen stackup, a patch antenna that resonates at 10 GHz corresponded (conveniently) to approximately 10 mm × 10 mm with an edge impedance of 235 Ω. All subarray designs include 4 patch antenna elements, to maintain symmetry and ease of scaling, separated by $\lambda_0/2$. This spacing is chosen to maximize directivity at boresight while keeping sidelobes at a reasonably low level.

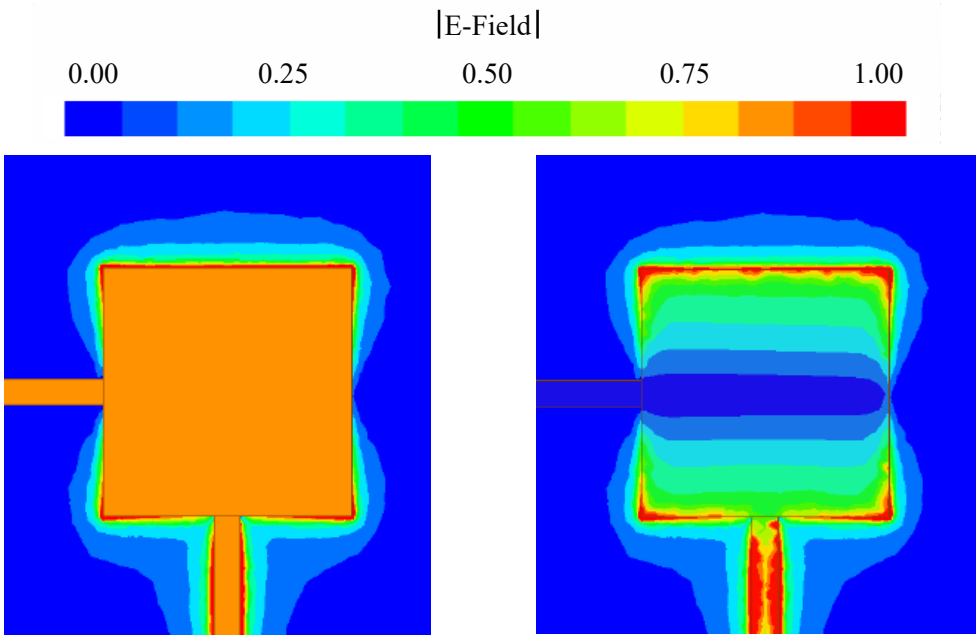


Figure 2.5: The patch antenna elements used in the subarray design: with metallization (left) and without metallization (right). The full-wave simulated normalized magnitude of the electric field at 10 GHz on the substrate surface immediately below the metallization illustrates the element operation.

Another important design choice is the lack of any metallized vias. Although vias are commonly used to feed patch antenna arrays, these designs do not use them for the following reasons: (1) the rectenna arrays are designed to be flexible, and vias could be damaged or unreliable with repeated bending; (2) the addition of vias would complicate and lengthen manufacturing, especially when scaling to large rectenna areas; and (3) because metal structures only exist on the top polyimide layer and no vias are used, perfect layer alignment is not important. Several different methods of feeding and dc extraction were explored for patch subarrays before the final design was reached.

The rectifying circuit needs to referrence the copper fabric ground plane as the RF and dc ground. This is accomplished in early designs through "ground tabs" which consist of copper fabric from the ground plane folded up over the edge of the subarray as shown in Fig. 2.6.

Grounding the diodes in this way implies that rectifying diodes should be placed close to

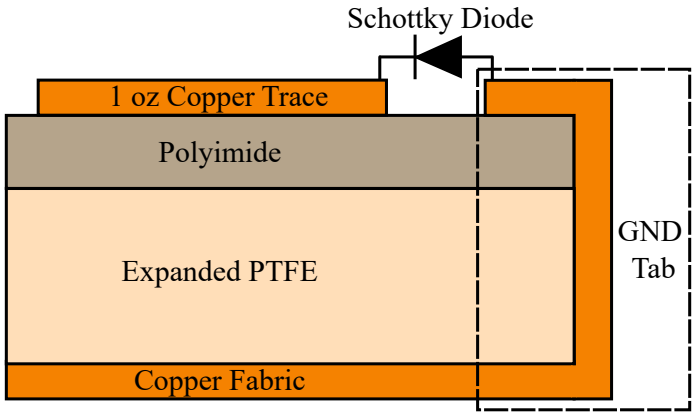


Figure 2.6: Diagram of material stackup showing the edge of the copper fabric ground plane folded up over the top of the stackup to provide a path to ground for the rectifying diode.

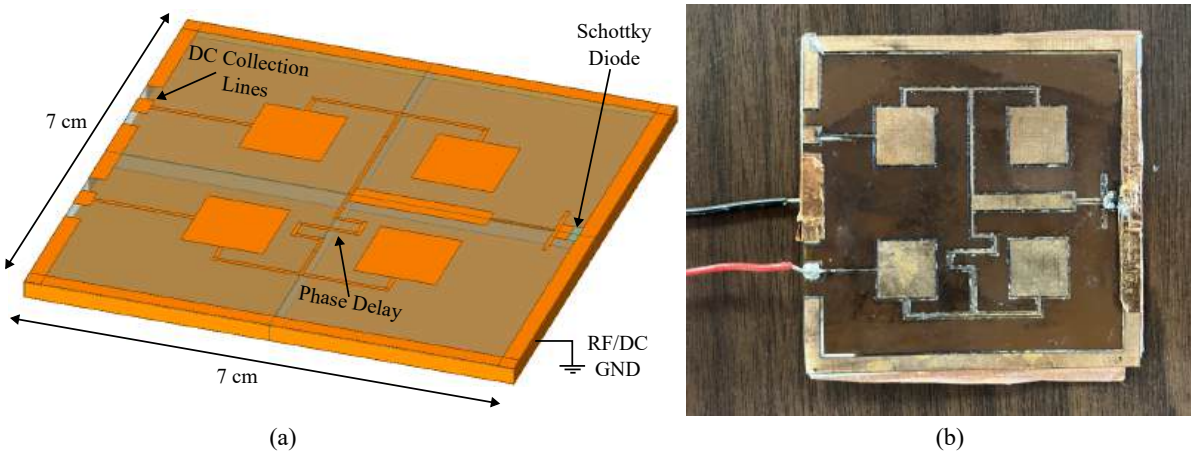


Figure 2.7: (a) Single linearly-polarized subarray feeding a single Schottky diode referrenced to the ground plane using a copper fabric tab. (b) Photograph of a fabricated 7 cm × 7 cm unit subarray.

the edge of the subarray to avoid long ground tabs which introduce unwanted parasitics as well as altering the radiation pattern of the subarrays by introducing additional coupling. To this same point, the ground tab method, implemented with a single rectifier diode per 4-antenna subarray, introduces assymetry to the subarray. Patch subarrays using two rectifying diodes, one per every two antenna elements, were explored as an alternative for their more symmetric layouts. However, this approach was eliminated in favor of combining more antenna elements per diode, ensuring better diode saturation at low incident power densities. An example of one early design, including

a photograph of a fabricated subarray with ground tabs can be found in Fig. 2.7a and Fig. 2.7b respectively. Early testing of fabricated subarrays showed that implementing the ground tab feeding method outside of simulation was not consistent and resulted in unreliable performance. Because of these poor results, an alternative feeding method is implemented.

The subarray uses a differential feeding approach to combine the RF power of 4 antenna elements at a single diode as shown in Fig. 2.8. The diodes are not referenced to the RF ground plane of the antenna elements. Instead, they are soldered between two pairs of patch antennas that are 180° out of phase with each other as demonstrated in [11, 44, 45]. This approach results in a compact and symmetric unit subarray without the need for the rectifying diode to be referenced to the copper fabric ground plane. In order to implement the differential feed, the subarray is designed with an integrated matching network to transform the impedance of the antenna elements to the desired impedance presented at the diode plane (shown in Fig.2.4b). Additionally, the matching networks act as reactive combiners for the RF power of multiple antenna elements. Because the integrated matching networks are on the same plane as the antenna elements, coupling effects that impact both the gain pattern and the impedance match are taken into account using full-wave EM simulation. Two patch antenna elements are edge-tapped and then reactively combined using a stepped-impedance transmission line matching network on either side of the differential feed. By reactively combining the outputs of two patch antenna elements, the relatively high edge impedance that needs to be transformed to match the diode is brought significantly lower and made simpler to match using the stepped transmission line. A diagram showing the integrated matching network and differential feed can be seen in Fig. 2.8. This specific feed/matching network was designed using an iterative process using both ANSYS HFSS and Cadence AWR. The antenna feed impedance simulated in HFSS is exported as an S-Parameter file into AWR and a simple microstrip matching network using the custom polyimide, foam, and copper fabric stackup is designed to match the source pulled diode impedance. The matching network is then imported back into HFSS and simulated when integrated with the antenna elements. This process is repeated until the desired match and antenna performance is achieved.

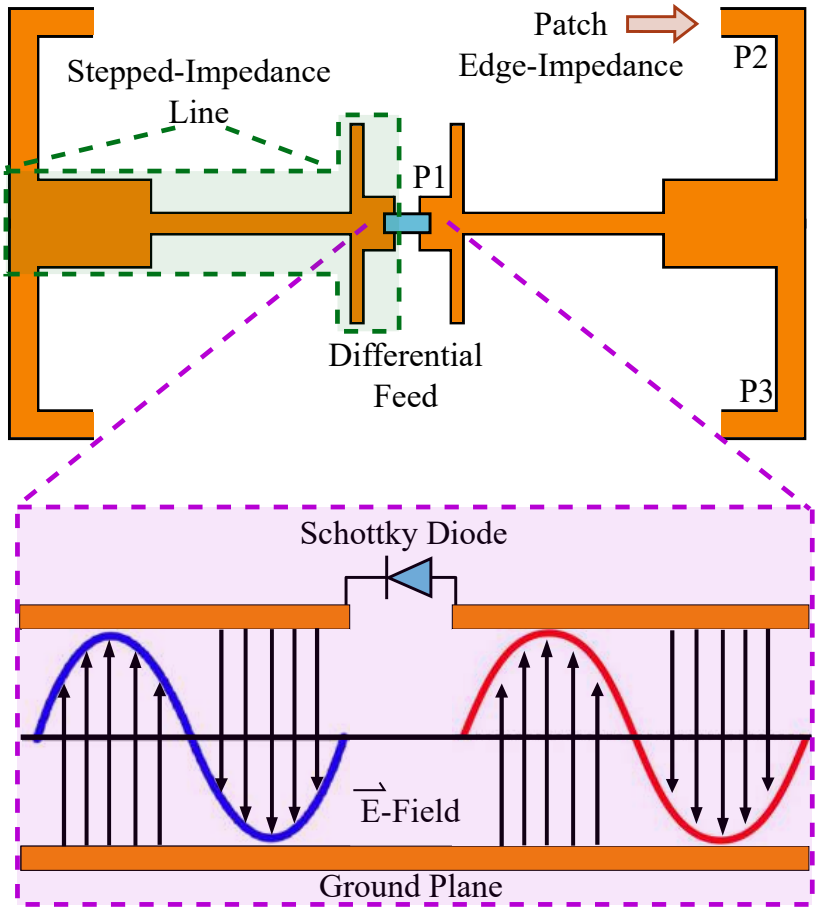


Figure 2.8: Diagram of showing two sets of 3-port (indicated by P1,P2, and P3) stepped-impedance matching networks integrated on the subarray (top) and closeup diagram of differential feed (bottom). Each matching network transforms the edge-impedance of two patch antennas to the diode conjugate match.

The simulated impedance at the rectifier device plane is shown in Fig. 2.9 from 8-12 GHz, showing the optimal impedance for the diode found by source-pull at 10 GHz. Since the rectifier impedance is complex and varies over power and dc-load, the impedance at the reference plane is chosen as a compromise between expected values of input power and load voltage at the design frequency. Fig. 2.10 shows the simulated radiation patterns at 10 GHz for a unit subarray with fully integrated feed and matching networks.

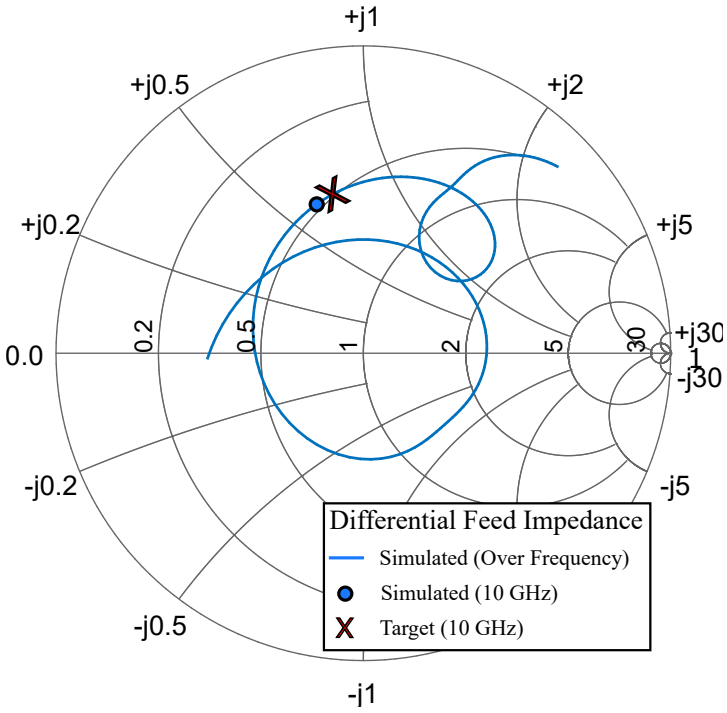


Figure 2.9: Simulated input impedance at the diode reference plane of the unit subarray plotted on a 50 Ω Smith Chart from 8-12 GHz. The target input impedance (as determined in Fig. 2.4b) is shown with an ×. The input impedance at 10 GHz is marked with a blue point.

2.3 Manufacturing of Unit Subarrays

With the unit subarrays 3D modeled and full-wave EM simulated using ANSYS HFSS, they are assembled as follows:

(1) First, unwanted copper from the metallized polyimide substrate is removed. This includes everything apart from the antenna elements, matching networks, and diode feeds, leaving one side of the polyimide completely bare and the other side with only the desired copper traces. Removal of unwanted copper can be done using a variety of techniques including milling, laser cutting, and chemical etching. First the unit subarrays manufactured in-house, a combination of milling and chemical etching is used. First, an outline of the desired metal traces is carved into the copper-clad polyimide using a milling machine. Then a coating of etching resist is applied over the outline before the polyimide is submerged in

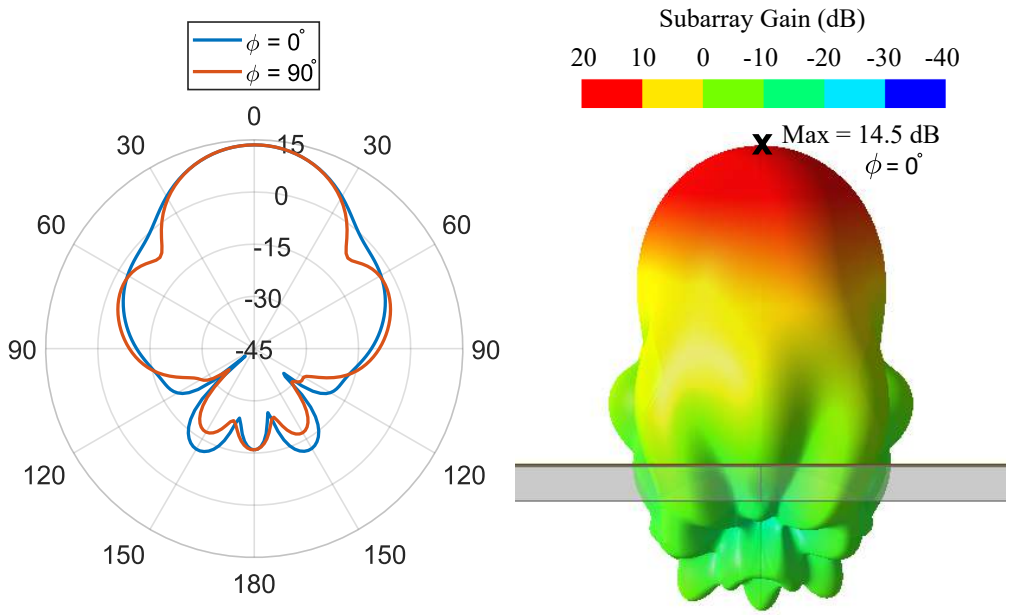


Figure 2.10: Simulated radiation patterns for the patch subarray on a polar plot (left) and 3D heat map (right). The elevation patterns are plotted at $\phi = 0$ ° and $\phi = 90°$. The subarray has a maximum gain at boresight of 14.5 dB and a 3 dB beamwidth of $\pm 18°$.

a ferric chloride solution to remove any uncoated copper.

(2) Squares of copper fabric and EPTFE foam are cut to match the etched polyimide layer and adhered together using 3M heavy duty adhesive spray. It is important to note that the EPTFE foam layer is first abraded with sandpaper to strengthen the bond to the coper fabric and polyimide. This is done because PTFE is a very chemically stable material and requires preparation in the form of abrasion or chemical treatment in order to form strong bonds.

(3) With all layers adhered together, the final step is to attach the rectifying elements and dc wiring. The SMS7621-079 Schottky diodes are soldered between the feed lines and the output wire are soldered to the dc tap traces.

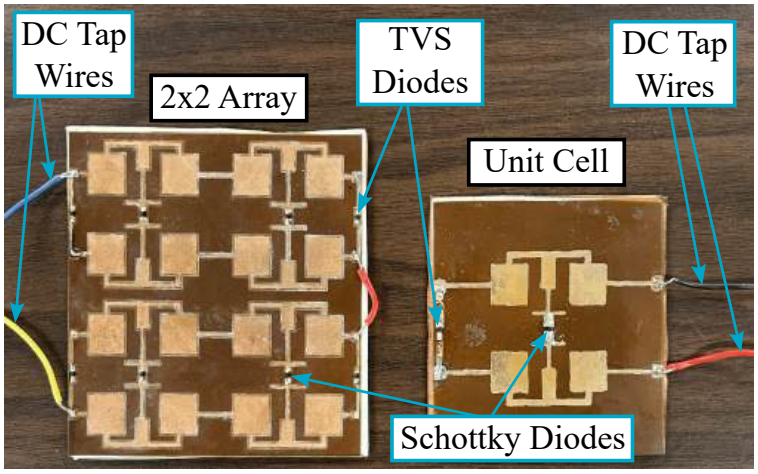


Figure 2.11: Patch unit subarray (right) and a scaled 2 × 2 element array (left). Two pairs of parallel-connected unit subarrays within the 2 × 2 array are dc combined in series with one another using an external wire.

2.4 Subarray Experimental Results

Using the materials discussed in Section 1.2.3 and the manufacturing techniques discussed in Section 1.3, the rectenna unit subarray is designed and fabricated. A photograph of a manufactured differential patch subarray is shown in Fig. 2.11 on the right, with a scaled 2 × 2 array shown on the left. The 2 × 2 array will be discussed further in the following chapter.

Before scaling to larger arrays, the subarray is characterized in terms of efficiency as a function of power density, angle of incidence, and dc load. Because it is not possible to measure the RF input power directly at the rectifiers, we first define the conversion efficiencies used to quantify subarray performance.

2.4.1 Conversion Efficiency Definitions

The RF-to-dc conversion efficiency is calculated in two ways to determine an upper and lower bound. The simulated passive antenna gain results in an upper bound [46]:

$$\eta_c' = \frac{P_{\mathrm{dc}}}{S_{\mathrm{inc}} \cdot A_{\mathrm{eff}}} = \frac{4\pi P_{\mathrm{dc}}}{S_{\mathrm{inc}} \cdot G_{\mathrm{sim}} \lambda^2} \quad . \tag{2.1}$$

To find the lower bound on rectenna efficiency, which is also more applicable to scaled arrays, the geometric subarray area is used:

$$\eta_c = \frac{P_{\mathrm{dc}}}{S_{\mathrm{inc}} \cdot A_{\mathrm{G}}} \quad . \tag{2.2}$$

To test the efficiency of the unit subarray, the incident power density S_{inc} is first determined. The two-antenna method is used with identical X-band horn antennas placed 81 cm apart with the gain G_H at broadside determined from measurements to be 14.9 dB. The incident power density is calculated from:

$$S_{\mathrm{inc}} = \frac{P_{\mathrm{T}} G_{\mathrm{H}}}{4\pi r^2} \quad , \tag{2.3}$$

where P_{T} is the transmitted power from one horn antenna r away from where the rectenna subarray is placed. After the incident power density is determined, the dc output voltage V_{DC} is measured across a variable dc load R_{load}, and the rectification efficiency determined from either (2.1) or (2.2). Fig. 2.12 shows the test range used to characterize the unit subarray.

2.4.2 Measurement Results

Figure 2.13 shows a plot of the RF-to-dc conversion efficiency over a varying dc load resistance of a single rectenna subarray for a low ($150\,\mu\mathrm{W/cm^2}$) and a higher incident RF power density ($840\,\mu\mathrm{W/cm^2}$), discussed in more detail in [6]. The differential subarray maintains above 30% peak efficiency in all cases. Both lower and higher indecent power densities result in about the same level of conversion efficiency, demonstrating 7.5 dB of dynamic range without any degradation in performance. However, the ideal dc-load is dependent upon input power, with higher input powers demanding a lower dc-load resistance for maximum efficiency. This can be seen in Table 2.1 which shows maximum conversion efficiencies using both incident power densities as well as geometric and effective rectenna areas.

The radiation pattern of a realized rectenna is a function of antenna gain $G(\theta, \phi)$ and the

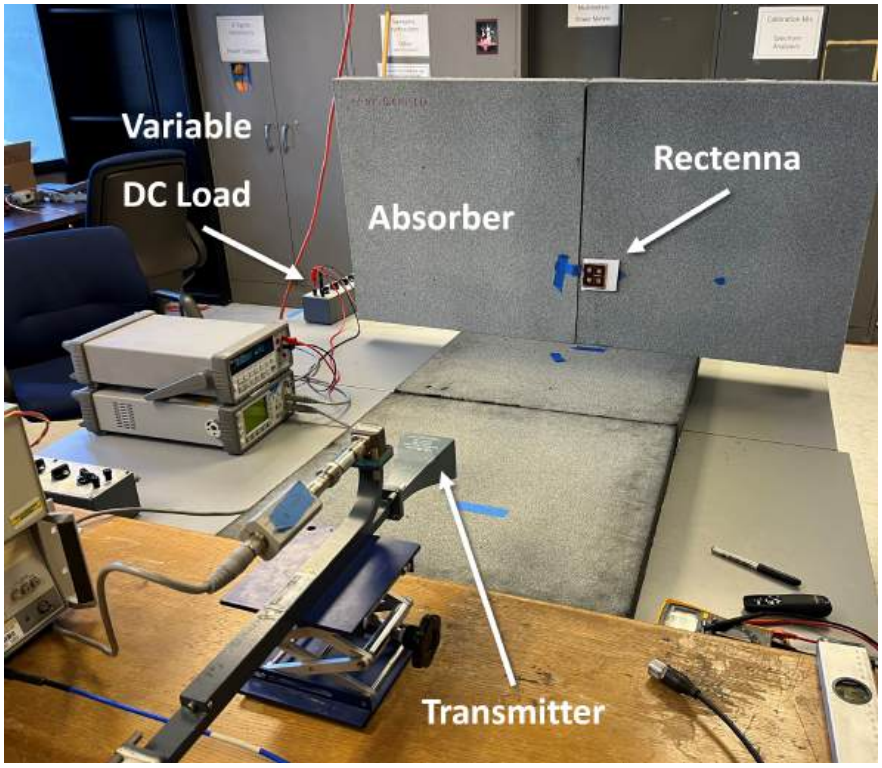


Figure 2.12: Test range used to characterize the differential subarrays.

Table 2.1: Peak Efficiencies of Unit Subarray.

Rectenna Area	Incident Power Density	DC Load	Peak Efficiency
Effective	$840\,\mu\mathrm{W/cm}^2$	220	34.3%
	$150\,\mu\mathrm{W/cm}^2$	370	34.9%
Geometric	$840\,\mu\mathrm{W/cm}^2$	220	31.7%
	$150\,\mu\mathrm{W/cm}^2$	370	32.3%

rectifier efficiency, η_c. This makes the pattern dependent not only on incident angle (θ, ϕ), but also on RF input power to the rectifier and the dc load. The radiation patterns of the subarrays, shown in Fig. 2.14, are quantified for two orientations, corresponding to E and H planes for the linearly-polarized patch subarray.

An important consideration for rectennas is the effective"narrowing" of the antenna gain due to the nonlinearity of the rectifier. It is an effect that can be seen if the passive antenna gain is scaled

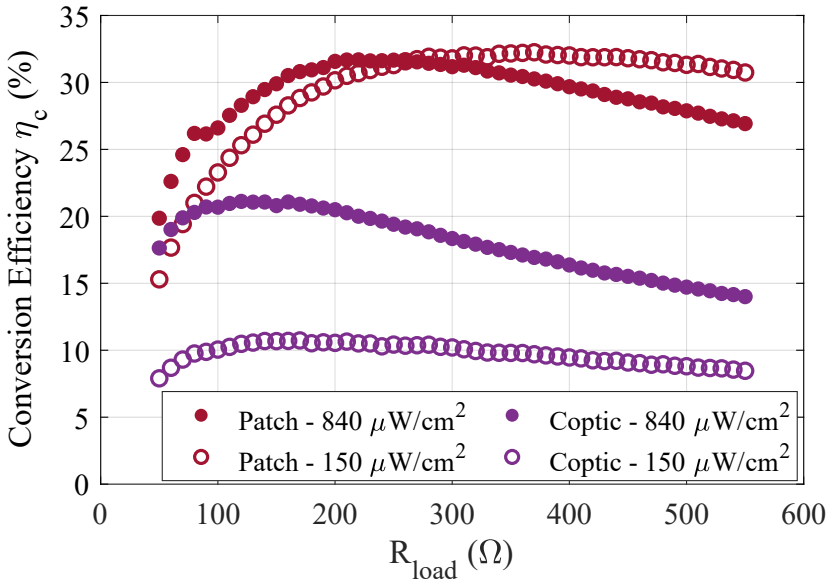


Figure 2.13: Conversion efficiency of the patch/differential and Coptic-cross subarrays as a function of R_{load}, using Eq. (2.2) (solid) for 840 μW/cm^2 and 150 μW/cm^2 incident power densities.

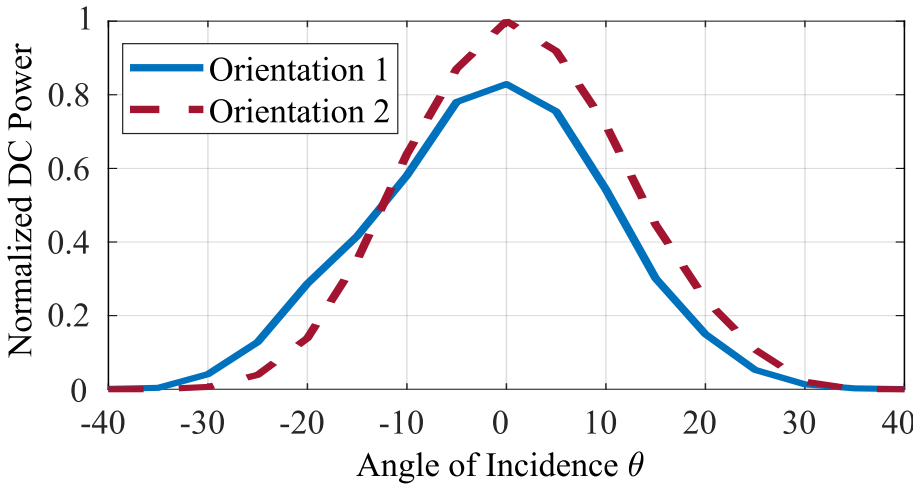


Figure 2.14: Single differential rectenna module normalized rectified dc power across a 250 Ω load plotted across angle of incidence of transmitted RF power for both linear polarizations.

by the power-dependent conversion efficiency of the rectifier. This is done by mapping the simulated linear gain over angle of incidence of the unit subarray, G_{lin}, to some maximum at boresight. A corresponding set of conversion efficiencies, η_{Gnorm}, are calculated based on rectenna measurement

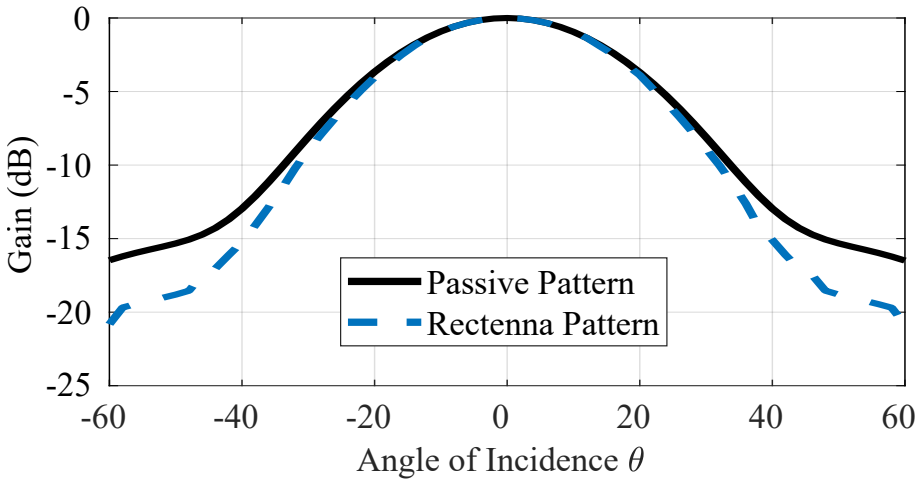


Figure 2.15: Plot of normalized passive subarray antenna gain (solid) and rectenna gain (dashed) which includes rectification efficiency for different power levels corresponding to different incidence angles. Narrowing of the main beam is observed as expected due to the lower efficiency at higher incident angles. The rectenna gain is normalized to an incident power density of 2,240 μW/cm^2, which is sufficient to saturate the diodes.

over incident power and normalized to the simulated linear subarray gain. The effective dc-gain of the subarray can then be calculated using Eq. 2.4.

$$G_{dc} = 10\log_{10}(G_{lin} \cdot \eta_{Gnorm}) \quad . \tag{2.4}$$

The power delivered to the rectifier from the antenna drops noticeably with higher incidence angles, resulting in the narrowing of the dc radiation pattern. This can be seen in Fig. 2.15 which compares the simulated passive gain and calculated dc-gain normalized to their maximum values.

2.5 Chapter Conclusions

This chapter presents the design and fabrication methodology for a rugged, low-cost, and flexible 10 GHz rectennna subarray using unconventional materials. Several different materials are considered including low-density packing foam, expanded PTFE foam, copper fabric, and metallized polyimide substrate. Multiple initial subarray designs are discussed, with the final design consisting of four combined patch antenna elements and a single differentially fed Schottky diode. This design

avoids the need for vias for either the diode feed or dc extraction and are fabricated using a simple and low-cost process. Additionally, the fabricated subarrays are characterized over input power and dc-load, demonstrating a maximum conversion efficiency of 35% at 10 GHz and a conversion efficiency above 32% over a dynamic range of 7.5 dB. Angle of incidence tests are performed for both E and H-planes of the subarray and a brief analysis of the dc vs. passive RF gain patterns is presented. The following chapter will discuss in detail the scaling of these subarrays up to a 25×25 array with 2500 antenna elements and 625 rectifier diodes. The results presented in this chapter are reported in [6] and [7].

Chapter 3

Scaled Measurements and Environmental Protections for 10 GHz Rectenna Arrays

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3.1 Introduction

In order to adapt the unit subarrays designed in the previous chapter to higher transmit power levels over longer distances, many of them can be combined together to form larger arrays. The subarrays are designed to be combined together through their dc outputs, allowing them to be combined in a straightforward manner. Because the individual subarrays are designed to be combined only through dc connections, the receiving beamwidth of the rectenna does not decrease as it is scaled in size. This means that a bigger array can receive a larger portion of the available transmitted power without the concern of greatly narrowing its field of view. Additionally, unlike in a standard phased array, it is primarily only the coupling between the RF-combined elements that

is relevant. While neighboring subarrays can interact and change the impedance presented to the rectifying diodes, this is a secondary effect and is taken into account in simulation. Fig. 3.1 shows the simulated S_{11} which corresponds to the normalized complex impedance presented to one of the four Schottky diodes by the differential feed. This is compared to the same case, but instead when all 4 differential feeds are excited simultaneously (active). While the coupling between subarrays does affect the presented impedance when they are excited, the shift in impedance at the design frequency is minimal and not enough to compromise performance.

The differential subarrays are first scaled up to 2×2 arrays using different dc combining schemes. The subarray is then scaled further to 5×5 $(6.7\lambda)^2$, 15×15 $(20\lambda)^2$, and 25×25 $(33.3\lambda)^2$ arrays in order to test higher power densities over larger areas of incidence. The patch subarray design is chosen for scaling to larger area rectennas because the differential feeding scheme enables easy dc combining in large numbers.

3.1.1 2×2 Differential Arrays

The 4-element arrays are shown in Fig. 2.11 and are characterized using the same test setup as in the case of the unit subarrays, but with a larger dynamic range. The array is tested in both the E-plane and H-plane. The results of the 2×2 array characterization are shown in Fig. 3.2. It is seen that the conversion efficiency of the differential 2×2 array reaches a maximum of about 50% excluding the two outlier points. Conversion efficiencies greater than 40% are maintained over a dynamic range of 8.5 dB and greater than 25% over a dynamic range of 15.3 dB. At high incident power densities, the differential array exhibits high fluctuations in the measurement of output power for larger dc loads. This is possibly caused by the output voltage of the rectenna arrays exceeding the rated reverse-breakdown voltage of the Schottky diodes. For the same incident power densities, these fluctuations only occurred at high dc load values which resulted in the highest dc output voltage. This conclusion is drawn after repeating the measurement multiple times under the same conditions.

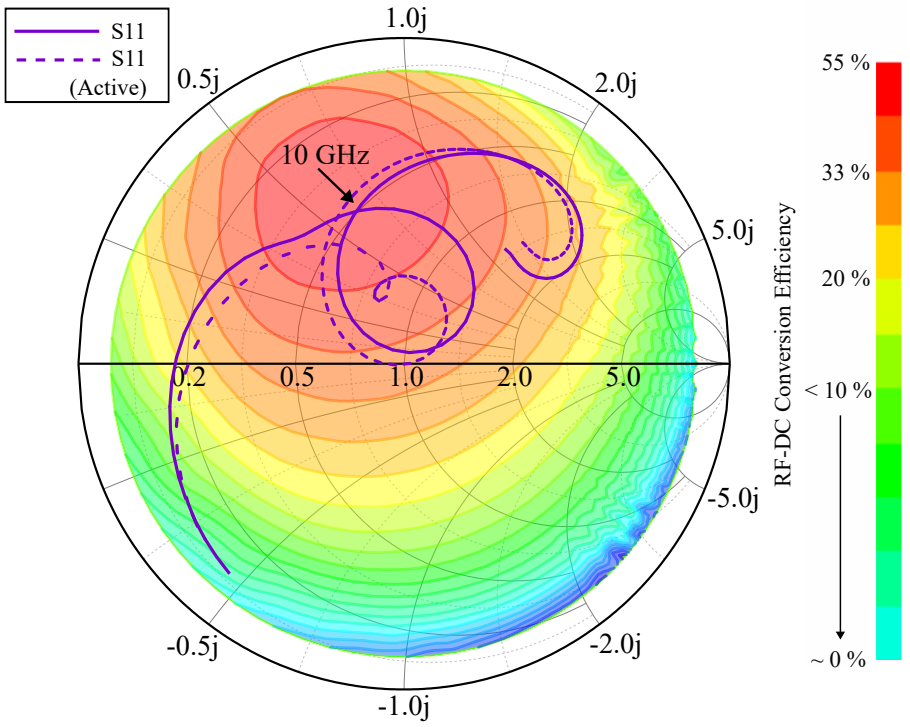


Figure 3.1: 50 Ω Smith chart plot showing S11 both with and without all four diode feeds excited simultaneously for a 2×2 array.

3.1.2 Larger Differential Patch Arrays

Figure 3.3 shows scaling of a patch unit subarray with one rectifying diode to 5×5, 15×15, and 25×25 arrays with 25, 225, and 625 rectifying diodes, respectively. The testing setup shown on the left-hand side of Fig. 3.4 consists of a wooden mount used to position a transmitting horn 2 m above the rectenna arrays under test. In addition, the necessary RF source, driver amps, and dc supplies are mounted near the transmitting horn to minimize cable loss. A photograph of a $1\,\text{m} \times 1\,\text{m}$ rectenna array positioned for testing is also shown on the right-hand side of Fig. 3.4.

Figure 3.6a shows the measured dc output power and the maximum conversion efficiency of 5×5, 15×15, and 25×25 rectenna arrays as a function of the dc load voltage. This measurement is carried out with a constant power of 5.7 W radiated by the horn antenna at a distance of 2 m. As shown by the graph, the total dc output power increases with the size of the array because more of the available transmitted power is incident on the array. However, both the 15×15 and 25×25

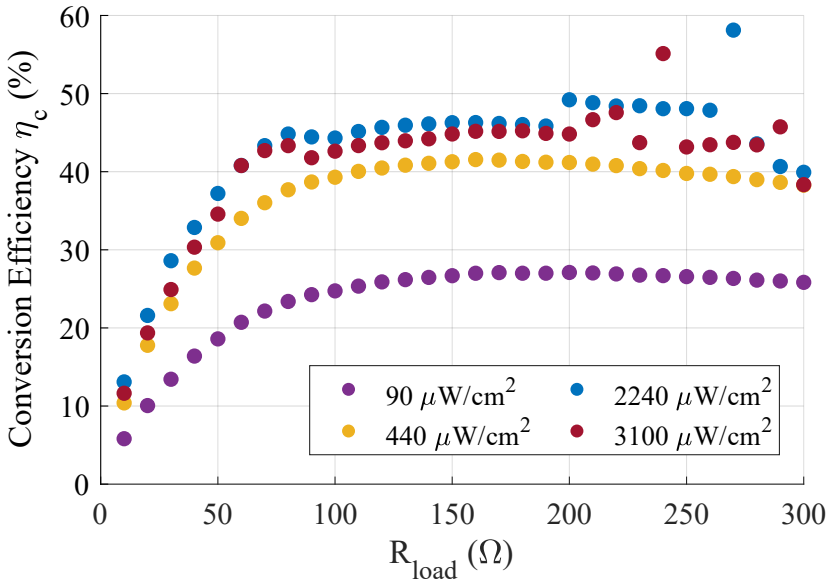


Figure 3.2: Measured conversion efficiency of the 2 × 2 differential array as a function of R_{load}. Efficiency is calculated using incident power densities of 90 μW/cm^2, 440 μW/cm^2, 2240 μW/cm^2, and 3100 μW/cm^2.

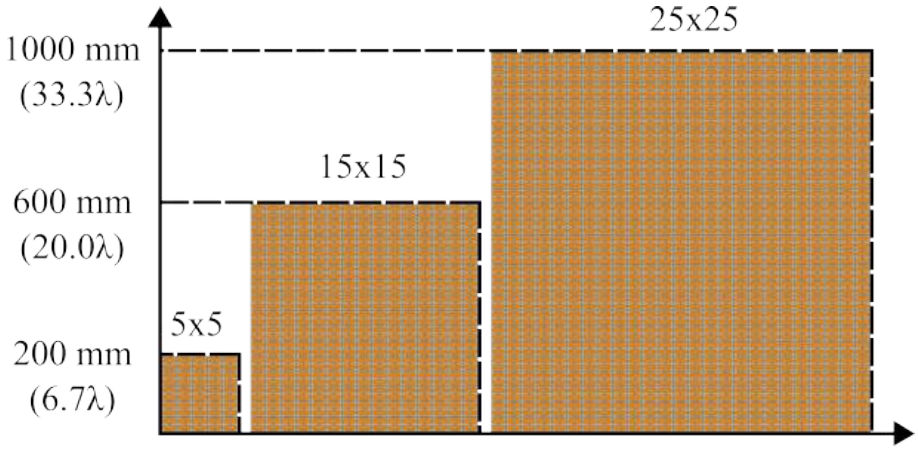


Figure 3.3: Illustration of array scaling, where the smallest 25 rectifying element array is scaled up to 225 and 625 elements. Side-length dimensions are shown both in millimeters and in free-space wavelengths at 10 GHz. The 25 × 25 array is shown in Fig. 2.1b, while the 5 × 5 array is shown in Fig. 2.1a and in Fig. 2.2.

arrays show a significant decrease in conversion efficiency compared to the 45% demonstrated by the 5 × 5 array. This is due to two main factors. The first is the increasing non-uniformity of

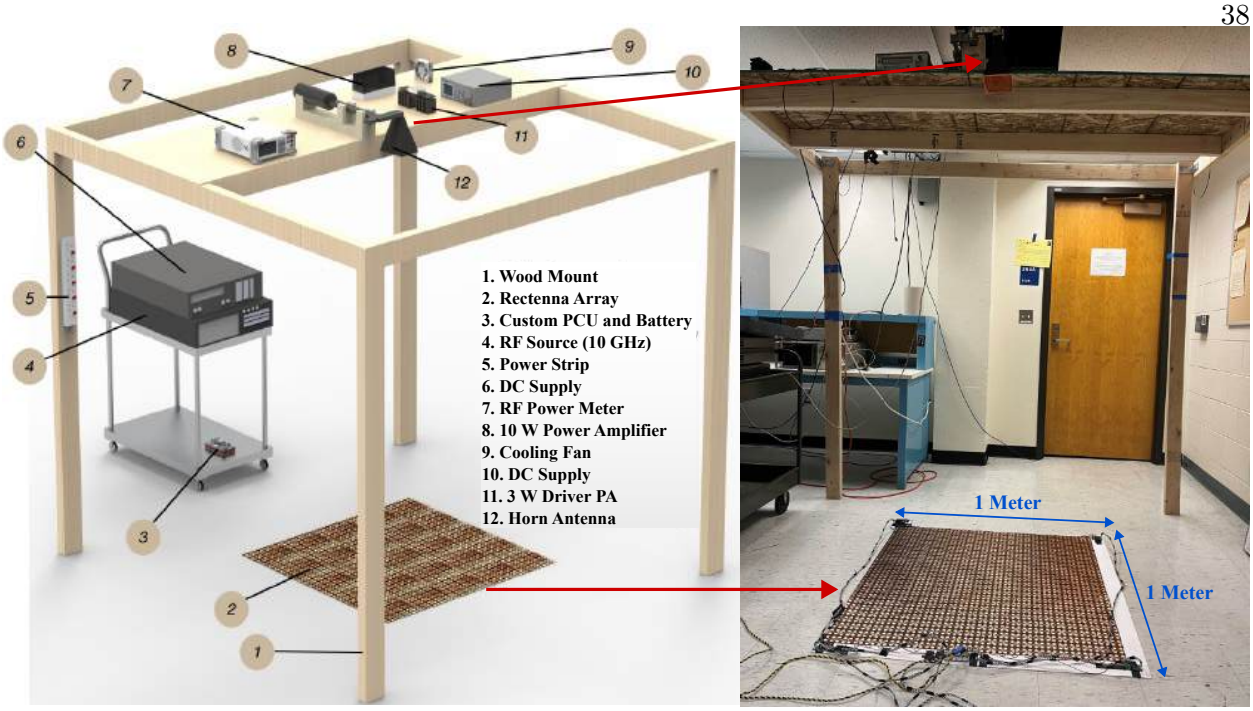


Figure 3.4: (Left) Diagram of testing setup for scaled rectenna array including 2 m tall wooden mount, transmitter horn with RF source, PA, and dc supply positioned above the rectenna array. (Right) Corresponding photo of test setup.

incident power density as the array size increases as can be seen in Fig. **??** which shows uniform power density over surface area from the transmitter antenna placed 2 m away. The three black squares in the center of the plot represent the three tested array sizes, showing that the two larger arrays experience significant non-uniformity. This causes the elements in the center of the array to saturate, while diodes in the outer elements do not receive sufficient power to operate efficiently. This point is illustrated by the simplified diode IV-cruves showin in 3.5. A very low input power, as seen by the outer edges of the larger arrays, does not produce a large enough voltage swing to drive the rectifier diodes enough into nonlinear operation and little to no rectification takes place.

The second factor contributing to reduced efficiency is static electricity buildup on the EPTFE foam substrate. It is observed that increasing the size of the array increases the amount of accumulated static charge between the copper ground plane and the copper traces where the diodes are mounted. During the construction of the arrays a significant number of Schottky diodes are damaged, leading to reduced efficiency. Several different arrays are constructed and it is determined that

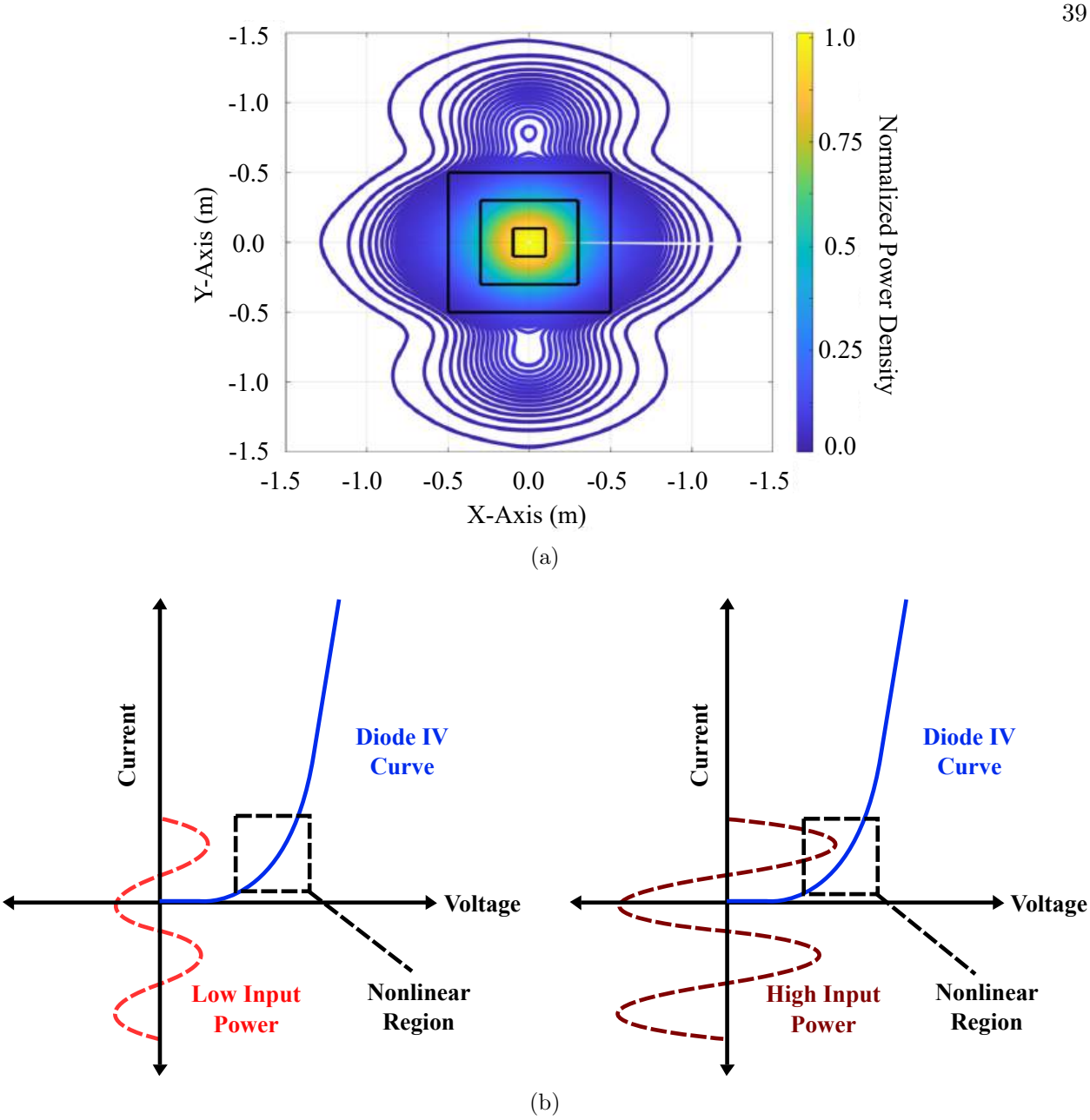


Figure 3.5: (a) Normalized power density plot for the transmitting horn antenna positioned 2 m fromt he rectenna. The black squares represent areas of $0.25\,\mathrm{m}^2$, $0.5\,\mathrm{m}^2$, and $1\,\mathrm{m}^2$.(b) Simplified plot of a general diode IV curve with (Left) low input RF power; and (Right) high input RF power. Without external dc biasing, the low-power RF is not enough to properly excite the diode into its deeper nonlinear region of operation.

protection from ESD is necessary to avoid damaged diodes during fabrication. However, even with damage to a number of diodes and a nonuniform incident power density, the 15×15 and 25×25

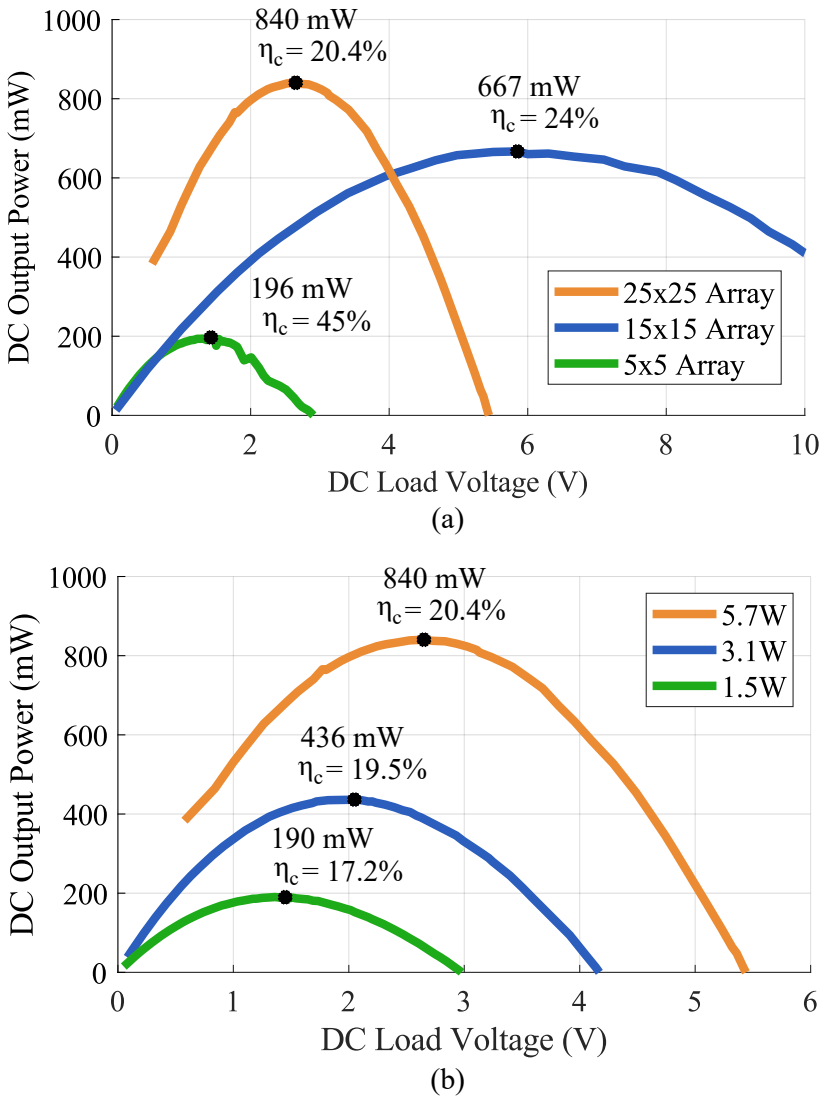


Figure 3.6: (a) DC output power vs. dc load voltage of different sized scaled arrays using a constant transmitted power of 5.7 W from a 2 m distance. (b) DC output power vs dc load voltage of largest array (25×25 subarray units) for three transmitted power levels between 1 and 6 W.

rectenna arrays achieve conversion efficiencies above 20%. The problem of static accumulation and ESD, as well as a solution to it, is discussed further in Section 3.2.2.

Another impact on scaled array conversion efficiency is the approach to dc power combining [47]. By default, the dc output lines of the individual rectenna subarrays are connected in parallel when they are combined into progressively larger arrays. Although this is the simplest combining approach, it is not the most efficient. In larger arrays, the incident power density is likely non-

uniform, which results in different potentials across the subarrays, which in turn lead to stray currents and excess power dissipation across portions of the array. Additionally, a high number of subarrays combined in parallel results in a low optimal dc load that approaches a short circuit for large arrays. In contrast, combining unit subarrays in series leads to high voltages in larger arrays which can lead to damage of rectifying elements and challenges in power management.

Therefore, a combination of series and parallel connections improves efficiency while maintaining reasonable dc load voltages in large arrays. Fig. 3.7a shows the dc output power as a function of dc load voltage at a constant incident power density is plotted for 15×15 rectenna arrays using 3 different dc combining schemes where:

(1) All unit subarrays are connected in parallel;

(2) all unit subarrays in each row are connected in parallel while a the subarrays in every three columns are connected in series (referred to as "Combo 1");

(3) all unit subarrays in each row are connected in parallel and all unit subarrays in each column are connected in series, resulting in equal parallel and series connections (referred to as "Combo 2").

Each of the three combinations described are visually represented in 3.7b. All series connections are realized using external jumper wires while the parallel connections are built into the subarrays as copper traces. However, it is simple to integrate an equal number of parallel and series dc connections without altering the design of the subarrays or complicating construction. Fig. 3.8 shows that this can be done for a 2×2 array with a single metal trace along the center, connecting the dc output lines of opposite polarity between subarrays. This design is scalable and has the added advantage of maintaining an approximately constant optimal dc load, regardless of array size. As shown by the measurements in Fig. 3.7a, dc output power and conversion efficiency increase with a higher proportion of series connections. Additionally, even with a large $1\,\mathrm{m} \times 1\,\mathrm{m}$ array, the dc-load voltage at maximum conversion efficiency remains at an easily manageable $6\,\mathrm{V}$.

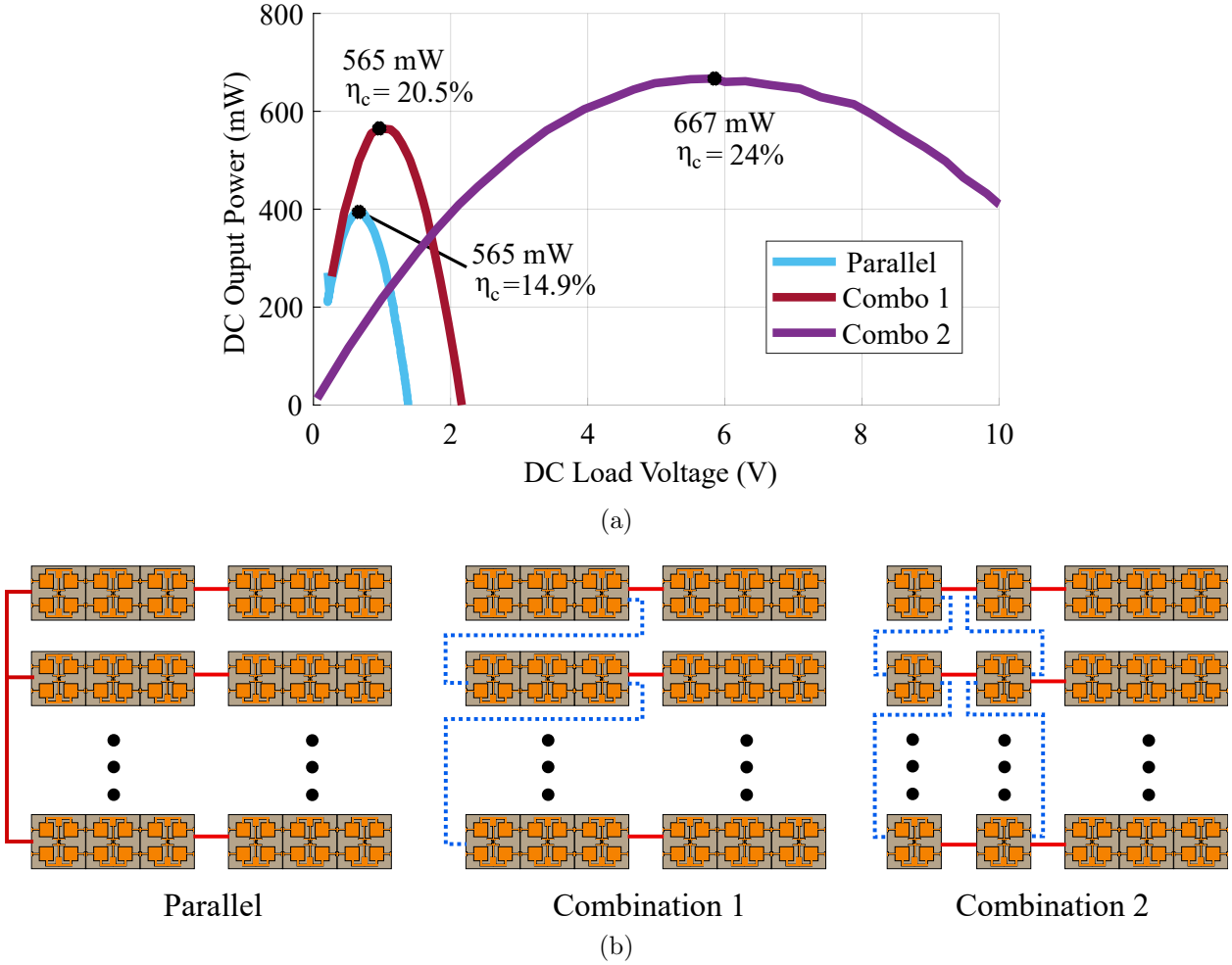


Figure 3.7: Measured conversion efficiency of the 2 × 2 (a) dc output power vs. load voltage of a 15×15 rectenna array using different dc connection methods and with a constant transmitted power of 5.7 W from 2 m away. (b) Diagram showing each of the three tested dc combining schemes. Paarallel connections are shown by solid red lines while series connections are shown by dotted blue lines.

3.2 Environmental Considerations

When in operation, the rectenna arrays can receive other signals within the band of operation from multiple transmitters, or a single multi-frequency modulated transmitter. In this section, characterization data for a two-tone signal is presented. Further, since the rectenna arrays are designed for robust operation in an outdoor environment, test data in different weather conditions is shown. Dry weather and storms result in electrostatic charge buildup in larger arrays, requiring

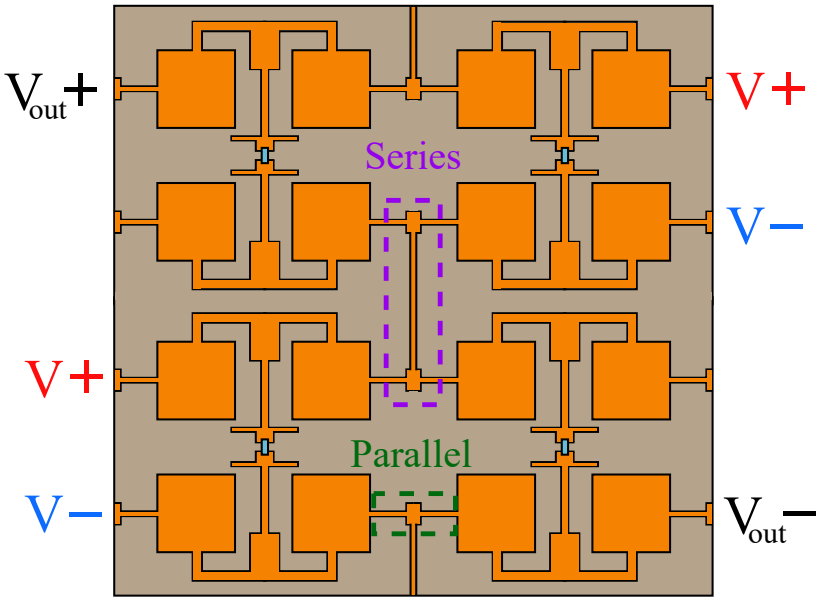


Figure 3.8: Diagram of a 2×2 array with built-in parallel and series dc connections.

a rectifier-protection circuit which is included in the design.

3.2.1 Two-Tone Measurements

Modulated signal wireless powering was investigated experimentally in early work with a broadband 2–18 GHz 64-element array [10]. In the experiments, 10,000 randomly generated pairs of widely-spaced two-tone signals with frequencies between 2 and 8 GHz and incident power densities varying between 0.1 μW/cm^2 and 0.1 mW/cm^2 were rank-order normalized to show in all cases improvement in rectification efficiency compared to a single tone with the same total power and to the sum of the rectified powers from the individual signals. Subsequent work with modulated signals, including multi-tone, have shown similar effects with limited theoretical treatment [48, 49]. A more detailed analysis of the rectifying diode IV nonlinear characteristic, leading to improved understanding of the rectification process for multi-tone signals, is shown in [50].

For the narrowband arrays discussed here, RF-dc conversion efficiency is measured for both 2×2 rectenna topologies across a varying dc load using two tones centered around 10.2 GHz. Measurements are conducted for high and low incident power densities, varying relative power

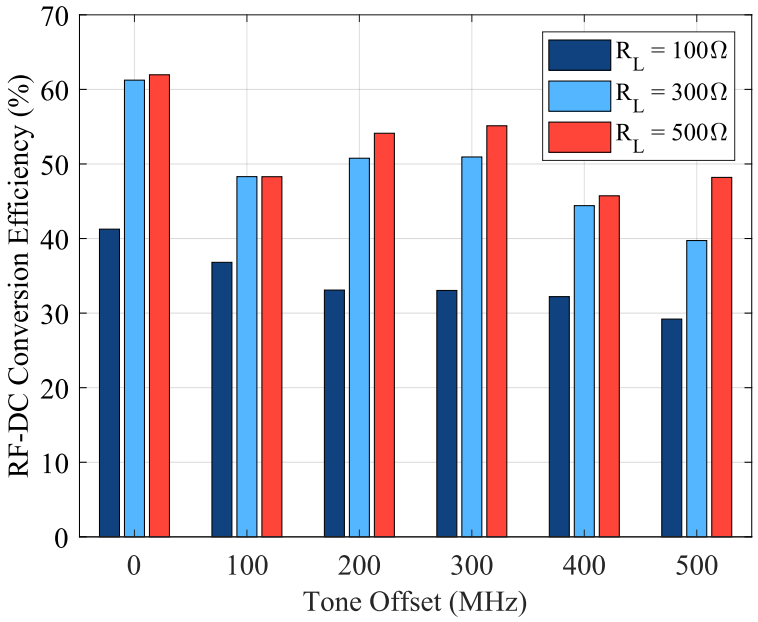


Figure 3.9: Measured conversion efficiency of the 2 × 2 differential array for tone spacings ranging from 0-500 MHz in increments of 100 MHz. The three columns per grouping show rectification efficiency for three dc load resistances: 100 Ω, 300 Ω, and 500 Ω.

levels between tones, with a tone spacing between 0.1–1 GHz. Figure 3.9 shows a histogram of the measured conversion efficiency over different tone spacings for a two-tone transmitted signal. Efficiency is calculated using the average power contributed by both tones. The array is narrowband and the tone spacing is much smaller than in e.g. [10], and the incident power is higher. The resulting conversion efficiency for the 2-tone signals with peak-to-average power ratios (PAPR) of 3 dB is lower than for a single tone with the same average power. We believe that the reason for lower efficiency in the two-tone cases is the narrowband nature of the rectenna arrays. As the tone spacing increases, the impedance presented to the two tones diverges from the high-efficiency target, and the resulting mismatch decreases efficiency.

3.2.2 Weather and ESD Protection

Other environmental events, such as various weather conditions, can contribute to performance degradation. In order to understand the robustness of the rectenna arrays, it is necessary to

test performance before and after exposure to outdoor conditions. To this end, a 5×5 differential rectenna array is placed outside on the roof of the lab for two weeks. During this time, the array was directly exposed to two separate rainstorms, one of which was an electrical storm (the lab is at 1,655 m in elevation). After the first week, the array was brought inside for testing and then returned to the roof for another week. Tests were performed indoors after exposure to protect lab test equipment.

Performance of the 5×5 array after the first and second weeks of exposure can be seen in Fig. 3.10 which shows the normalized dc output power plotted against angle of incidence. After the first week, where the rectenna was exposed to rain and direct sunlight, the performance of the rectenna did not degrade from the nominal case. However, in the second week, the performance of the rectenna decreased substantially due to a number of diode outages as a result of lightning storms that occurred only in the second week of exposure. These storms likely induced ESD within the rectenna and destroyed several diodes.

Static accumulation and ESD events can pose serious problems when using sensitive diodes such as those encountered when fabricating large-scale arrays. Because ePTFE is a good electrical insulator, it can easily build up enough charge to threaten diode integrity; this problem becomes greater as rectennas are scaled and their surface area increases. To protect the sensitive Schottky diodes, transient voltage suppression (TVS) diodes are implemented. TVS diodes are a type of avalanche diode designed to protect other electronic components from voltage spikes by using the avalanche breakdown effect to rapidly conduct large amounts of current and dissipate excess energy. Avalanche breakdown occurs when electrons in a lightly doped semiconductor are accelerated due to a high-voltage event and collide with atoms with enough energy to ionize them, causing an exponential rise in current. This is a distinctly different effect from Zener breakdown which refers to the quantum-mechanical effect of valence electrons tunneling to the conduction band which occurs only heavily doped semiconductors and at lower voltages than avalanche breakdown, as shown by Fig. 3.11.

Some key parameters of TVS diodes are the maximum reverse standoff voltage (MRSV)

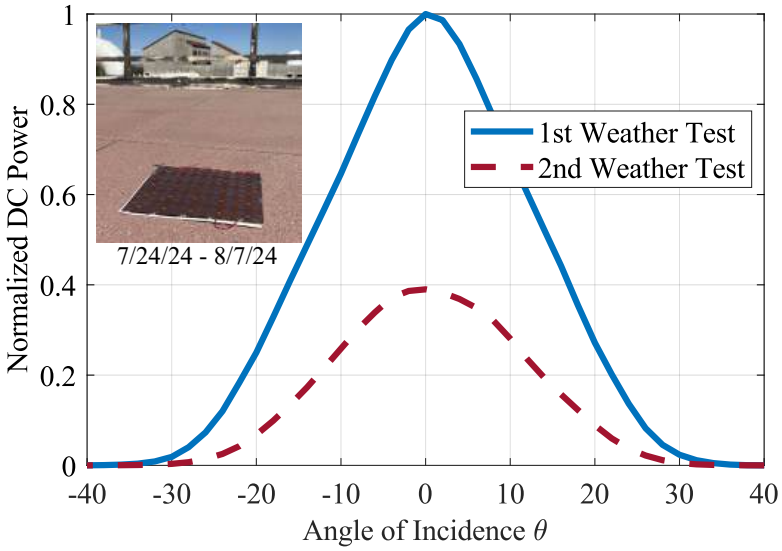


Figure 3.10: Normalized dc output power of a 5 × 5 rectenna array plotted over angle of incidence after exposure to outdoor events during 2 weeks. Week 1 saw only rain and sunlight, showing no performance degradation. Week 2 saw lighting storms which caused the drop in efficiency by inducing ESD events, damaging the rectifying diodes. The inset shows a photo of the array on the lab roof.

which is the maximum reverse voltage at which no significant current is conducted; the reverse breakdown voltage (RBV) which is the voltage at which significant current begins to conduct; and the clamping voltage (V_c) which is the voltage at which the device conducts the maximum current it is rated for. Additionally, the junction capacitance and parasitics are relevant for determining the response time and how much the diode reactively loads the circuit it is protecting. For these reasons, lower values of are ideal, especially for integration with high-frequency components. Because the intended use in this project is for ESD protection, which is typically a very fast an high-voltage impulse, the exact MRSV is not critical as long as it is higher than the output voltage of the rectifying diodes. However, the response speed and the maximum power handling of the diode are important to consider. After testing several different TVS diodes, the ESD321DYAR is selected as the most reliable and integrated in parallel with the dc extraction lines of the subarrays (shown

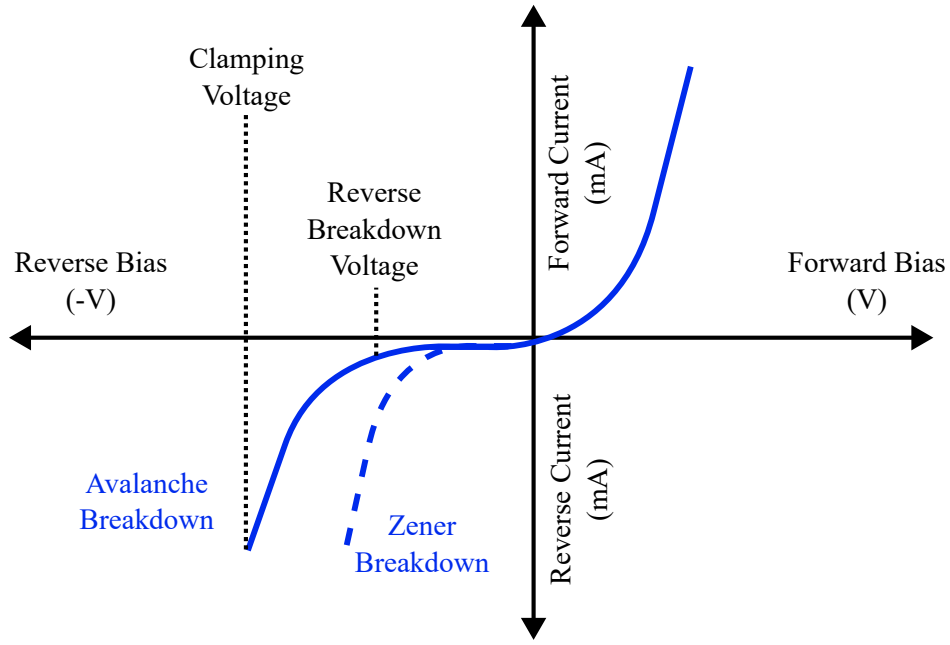
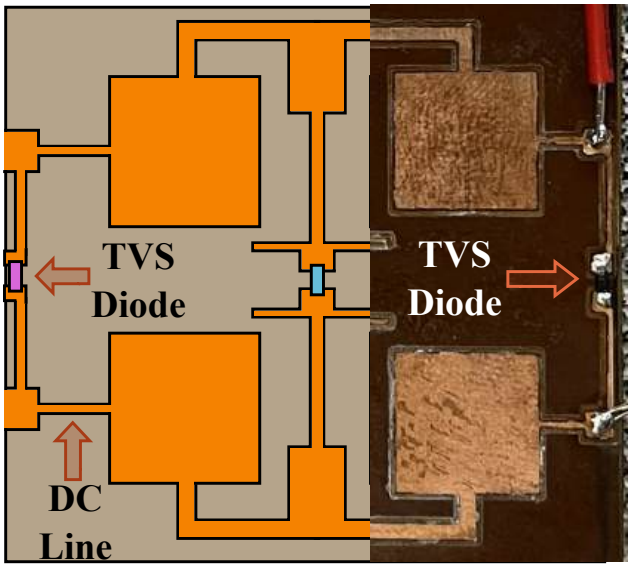


Figure 3.11: (a) IV curve of a protection diode which highlights the different voltages at which avalanche and Zener breakdown occur. In TVS diodes, which are lightly doped, only avalanche breakdown will occur. (b)

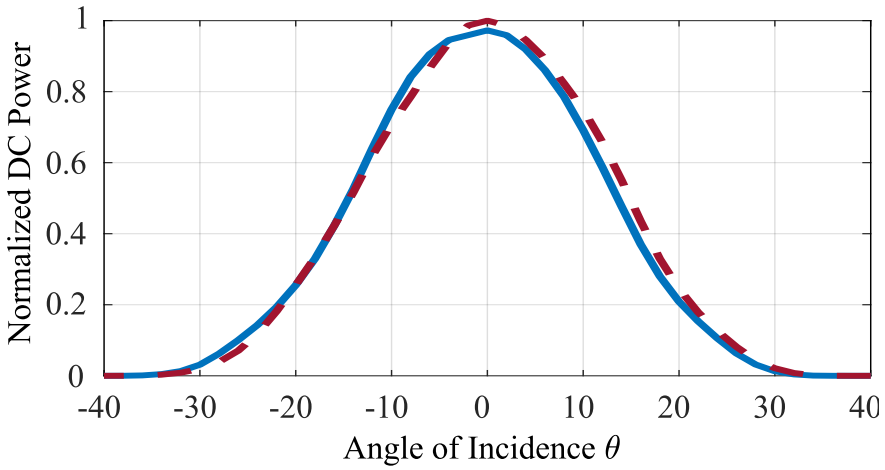
in Fig. 3.12a), where they do not affect the RF path by altering the impedance presented to the Schottky diodes. To test the protection capability, the ground of a Van de Graaff generator with a discharge voltage up to a 100 kV is connected to one dc terminal of the array, while the discharge electrode is brought close to the diodes until air ionization, which greatly exceeds the natural charge accumulation. There was no observed performance degradation, as shown by the measured data in Fig. 3.12b. This experiment is repeated across several subarrays, both with and without the integrated TVS diodes. In all cases without protection, the rectifying diodes were destroyed.

3.3 Chapter Conclusions

This chapter presents the experimental results on scalable and deployable 10 GHz rectifier antenna arrays. The arrays are fabricated on a low-cost, flexible stack of ePTFE, metalized polyimide, and copper fabric, for ease of deployment in energy-denied environments. The unit subarrays are scaled up to a 25×25 array with 2500 antenna elements and 625 rectifier diodes and characterized



(a)



(b)

Figure 3.12: (a) Layout of a unit subarray with added TVS diodes in the dc extractions lines for ESD protection. (b) Normalized rectified power over angle of incidence before (solid blue line) and after (red dashed line) applying a 100 kV discharge from a Van de Graaff generator.

for conversion efficiency at 10 GHz and for different dc load configurations. The peak measured efficiency is 62% at 10.2 GHz for a 2×2 array of patch unit subarrays (16 antennas and 4 rectifiers). Additionally, a dynamic range of 8.5/,dB is demonstrated for conversion efficiencies above 40%. The peak output power of 0.84 W was measured for the largest (25×25) patch array.

The fabricated arrays also demonstrate resilience to water and temperature exposure after

repeated testing in outdoor conditions over several weeks. To prevent diode destruction from ESD events, TVS diodes are placed in parallel with the dc path of the rectennas. The TVS diodes allows for survivability from exposure to 100 kV static discharges from a Van de Graaff generator. To conclude, this work extends existing research in X-Band rectification by demonstrating that scalable, efficient, and rugged rectenna arrays can be constructed from low-cost and non-conventional microwave materials. The results presented in this chapter are reported in [7].

Chapter 4

Experimental Packaging Process for Heterogeneous Integration

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4.1 Introduction

Heterogeneous integration (HI) of different semiconductor and passive technologies has been of interest in the past decade as overviewed in e.g. [51, 22, 20] with the goal to improve performance and reduce chip size. For example, silicon chips can be used for mixed-signal and digital functions, and implemented in the same process with GaAs or InP circuits for good noise performance, and GaN integrated circuits for high power handling at microwave frequencies [21], [52]. Heterogeneous integration can also help lower the required area needed for a MMIC or RFIC chip by offloading

passive components to the packaging technology instead of taking up expensive die space. This can include components such as off-chip matching networks, filters, couplers, and interconnects. In particular, passive structures that can be implemented using grounded coplanar waveguide (GCPW) or interceonnects that transition between GCPW and microstrip modes are particularly useful to integrate with active circuits. This is owed primarily to the fact the RF input and output of most MMICs and RFICs use ground-signal-ground (GSG) pads. Utilizing GCPW interconnects helps maintain a uniform mode between the package and the die (shown in Fig 4.1), potentially improving losses at the die-package-interface and higher-order mode suppression, particularly at millimeter-wave frequencies.

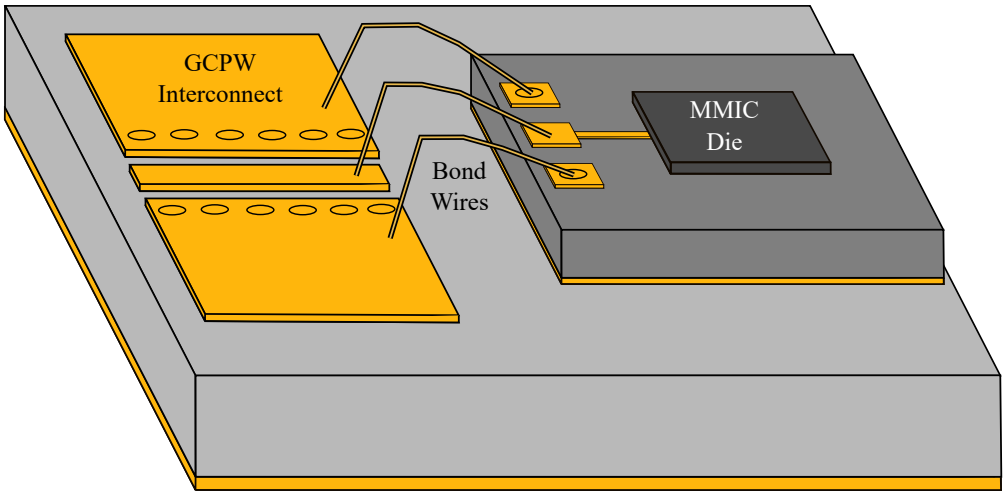
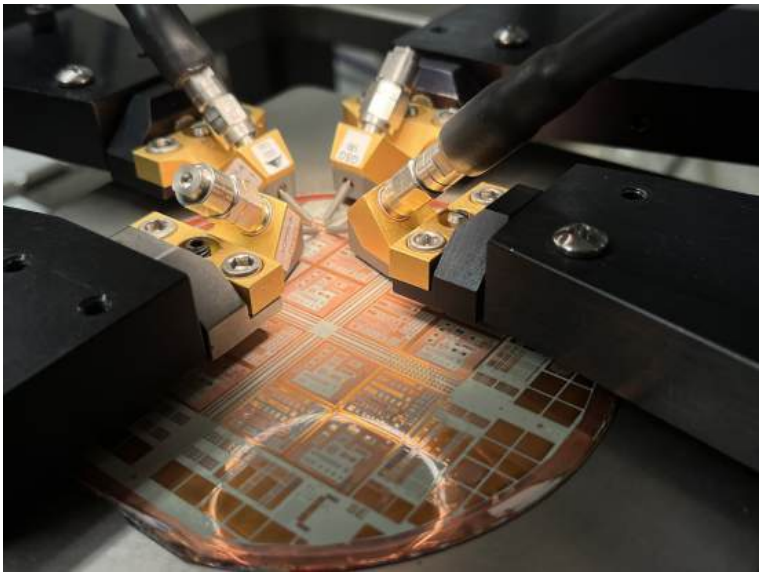


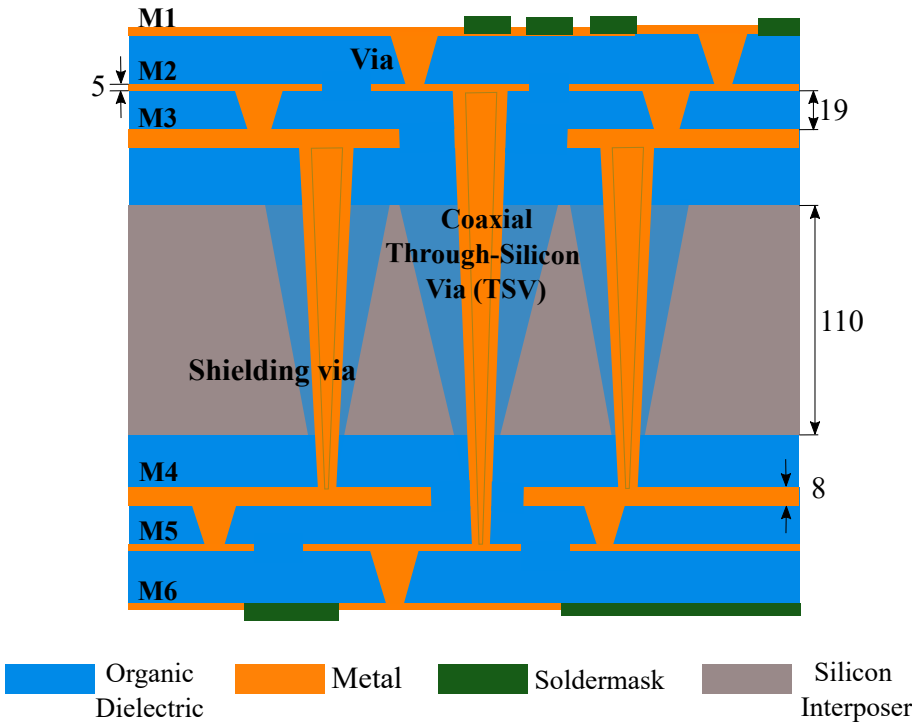
Figure 4.1: Diagram of a MMIC die mounted onto an external substrate and wire-bonded to a GCPW off-chip transmission line.

Previous published HI processes are summarized in Table 4.1. Multiple organic layers with no interposer are used in [53] to demonstrate a flip-chip bonded SiGe LNA integrated with a ribbon-bonded GaAs mixer around X-band. Other HI processes are used to create compact built-in components such as high-frequency interconnects for CMOS integration with InP [18] and CMOS with InGaAs PIN diodes with through-interposer vias [54].

A fine-pitch integration method utilizing a solderless interconnect through thermal compression bonding is demonstrated in [55]. In another approach, the HRL Metal-Embedded Chip Assem-



(a)



(b)

Figure 4.2: (a) Photograph of a 10-cm (4-inch) wafer with 6 organic dielectric layers on a Si interposer. (b) Sketch of the cross-section of the wafer, showing dielectric and metal layers of the stack-up and metalized vias between all layers. Approximate dimensions are given in μm. The thicknesses of layers M1, M2, M5 and M6 are the same, as well as those of M3 and M4.

bly (MECA) process [56], ceramic capacitors and couplers are integrated with a GaN Monolithic Microwave Integrated Circuit (MMIC) power amplifier (PA) on a single-layer alumina substrate using a gold interconnect layer, showing improved efficiency and gain of the PA compared to on-wafer tests [57].

A fan-out through-substrate interconnect using copper redistribution layers is demonstrated in a polymer substrate up to 10 GHz in [58], while similar wafer-level fan-out interconnects on a flexible organic interposer are demonstrated in [59]. Alternatively, integration using both sides of a wafer can also be achieved through the use of larger vias extending through the wafer core or interposer made from glass, as demonstrated in [60]. Silicon interposers can also be used for wafer-level integration using through-interposer vias. This is demonstrated using through-silicon-hole (TSH) and through-silicon-via (TSV) interconnects in [61] and [62], respectively. These allow for low-loss and broadband signal paths between both sides of a two-sided packaging process, resulting in a compact multichip package.

Table 4.1: Packaging Techniques with Heterogeneous Integration

Ref	**Description**	**Specifics**
[53]	SiGe/GaAs, organic substrate	LNA/mixer 4-15 GHz interconnect IL= 0.5 dB (10 GHz)
[18]	Wafer-scale, InP DHBTs and RF-CMOS	DHBTs (f_T = 300 GHz) integrated with 130 nm RF-CMOS technology
[54]	Wafer-scale, InGaAs image sensors and Si readout	1024×1024 array of InGaAs PIN diodes bonded to SOI
[55]	Si dielets, Si interconnect fabric, solderless thermal compression	10 μm pitch with 100 μm spacing between dielets
[56]	GaN w/ alumina, Metal Embedded Chip Assembly (MECA)	10-GHz MMIC PA, gold interconnects, thermal/RF/dc ground
[58]	Polymer substrate interposer using high density fan-out (HDFO) interconnects	Insertion loss of 0.9 dB/mm for through-interposer fan-out interconnects
[59]	Flexible organic substrate using fan-out wafer level packaging (FOWLP)	Integration of 1 mm^2 Si and InGaN LED dielets in a 10×20 array
[60]	Low-cost 180 μm glass interposer using 50 μm pitch through-package-vias (TPVs)	Insertion loss of glass interposer TPVs range from 0.3-0.5 dB/mm at 10 GHz
[61]	Low-cost silicon interposer using through-silicon-hole interconnects (TSH)	Simulated insertion loss of 0.05 dB at 10 GHz per TSH
[62]	3D HI of GaAs LNA with hot vias on silicon interposer using TSVs	Insertion loss of 1.8 dB at 10 GHz for TSV transitions

In this chapter, the design and characterization of several passive structures in an experi-

mental process intended for HI is presented. The goal of developing this high-frequency process is to integrate various chips on different layers and connect them using low-loss, multi-layer interconnects. Therefore, transmission lines that use the various layers are important for understanding the capabilities of this packaging technology. In particular, GCPW transmission lines are used in a variety of passives, including couplers, filters, and interconnects. All passives are designed to be matched to a characteristic impedance of $Z_0 = 50\,\Omega$. The process consists of 3 resin-filled organic dielectric layers laminated on both sides of a 110-μm thick rigid silicon interposer, enabling 6 potential metal layers. A photograph of a 10-cm (4-inch) wafer with numerous GSG probes for testing is shown in Fig. 4.2a. A cross-section of the wafer in Fig. 4.2b shows the 6 low-dielectric constant organic dielectric layers, the 6 metal layers and various metalized vias between layers. The passive structures designed using this experimental technology are a means of investigating process performance up to 50 GHz, and initial results of several interconnects are reported in [63, ?].

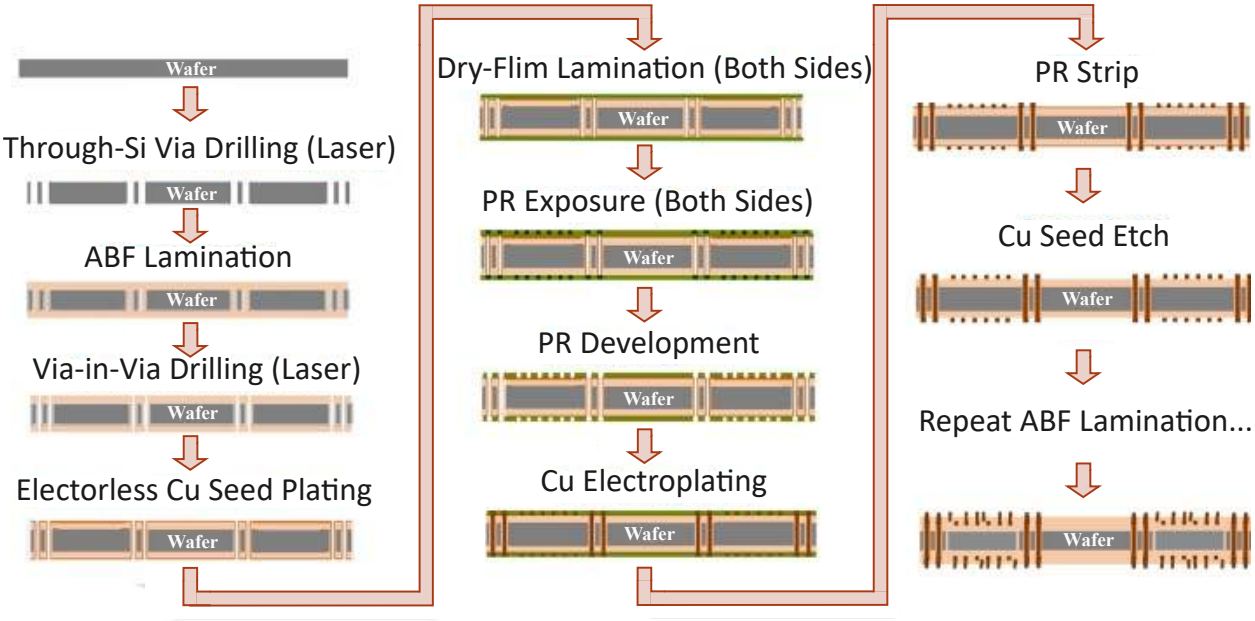


Figure 4.3: Process flow for fabricating Si-core substrates with organic laminated layers and metallization, courtesy of Applied Materials.

The HI process used in this work is discussed in greater detail here. Figure 4.3 shows the steps

in the wafer assembly process, starting with a Si wafer that is thinned down to 110 μm thickness. The first step is laser drilling of the through-wafer vias. In the next step, the wafer is laminated on both sides with ABF (Ajinomoto Build-up Film GL102) which fills the through vias. After this, a second laser drilling is performed to define smaller vias within the initial silicon through vias, so that there is ABF insulation on the via sidewalls. The next step is an electroless Cu seed layer plating on the ABF-coated surfaces. This is a conformal process that deposits roughly 200 nm of Cu everywhere. Following this, a dry-film photoresist is laminated on both sides and then exposed with deep-blue 400 nm wavelength light to create the pattern. Then, the photoresist is developed and the next step is electroplating the Cu inside the masked wafer with the seed layer as the contact electrode. After electroplating, the photoresist is stripped followed by seed-layer etching. This process is then repeated for subsequent Cu layers.

4.2 Broadband GCPW Interconnects

This section discusses the design, simulation, and measurement of a GCPW-to-microstrip (GCPW-MS) assymetric interconnect which makes use of all the metal layers available above the silicon interposer (M1, M2 and M3). Additionally, a symmetric version using an additonal transition back to GCPW (GCPW-MS-GCPW) is also discussed. Interconnects are designed and simulated using the Ansys HFSS 3-D full-wave electromagnetic solver.

4.2.1 Design and Simulations

Figure 4.4a shows the 3-dimensional view of the asymmetric GCPW-MS interconnect. The interconnect is made asymmetric because it is often most useful as a transition between GCPW and microstrip modes when, for example, bonding to an on-chip GSG pad. The test structure is 1610 μm by 800 μm and connects a GCPW on M1 to a microstrip line on M2. The grounds on metal M1 are connected to the common ground on M3 through cascaded vias from M1 to M3. The GCPW grounds on M1 are tapered away from the signal line at the transition which is flared to allow for a via to connect the signal line to the microstrip on M2. By carefully monitoring the

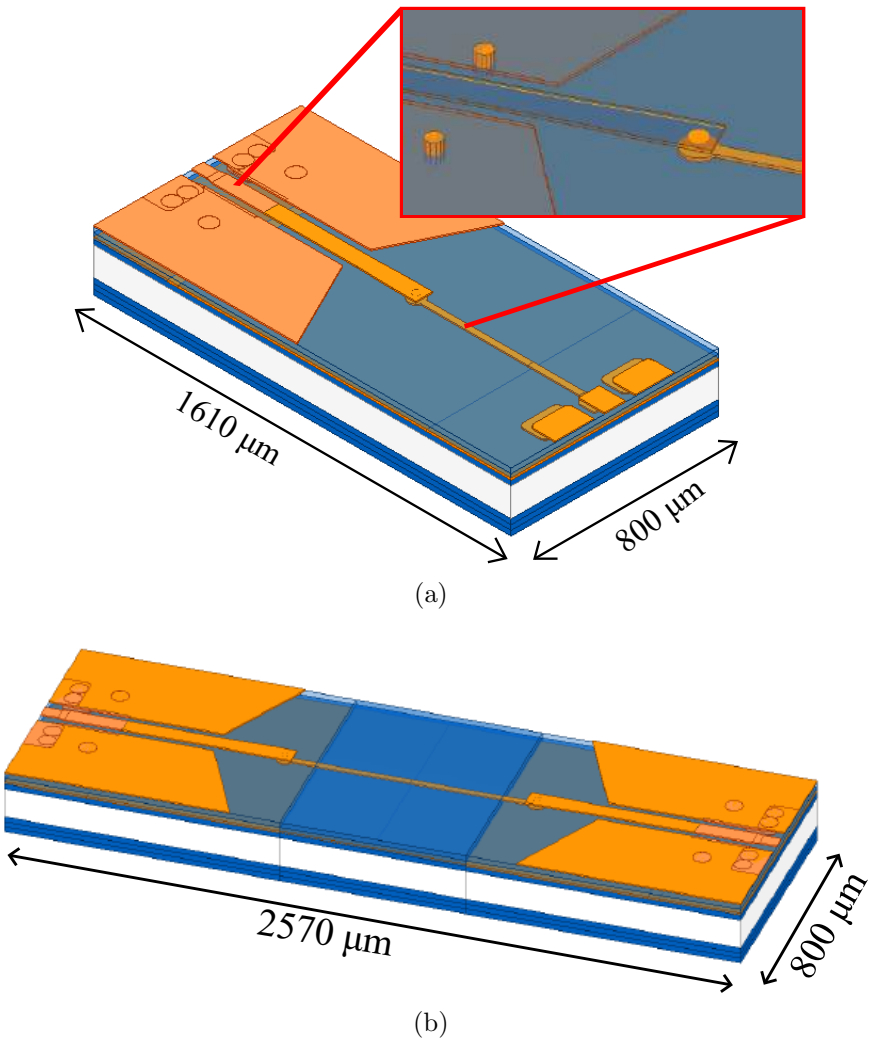


Figure 4.4: (a) Three-dimensional view of GCPW-to-microstrip interconnect, with transitions from M1-M3 GCPW to M2-M3 microstrip using one via through dielectric layer 1 and tapering the coplanar grounds. (b) Three-dimensional view of GCPW-to-microstrip-to-GCPW interconnect, with transitions from M1-M3 GCPW to M2-M3 microstrip and back again.

$\vec{E}$-field and currents along the transition, both the GCPW and microstrip segments are made long enough to properly establish both modes of transmission. On the microstrip end of the interconnect test structure, the GSG pad is the same as the ones used in the MS-MS and MS-SL interconnects, consisting of a cascaded pad with vias connecting metal M1 to metal M2 where the microstrip line is located. On the GCPW side, the GSG is embedded in the test structure, with a tapered signal line for impedance matching. The launcher ground pads are connected to the global ground

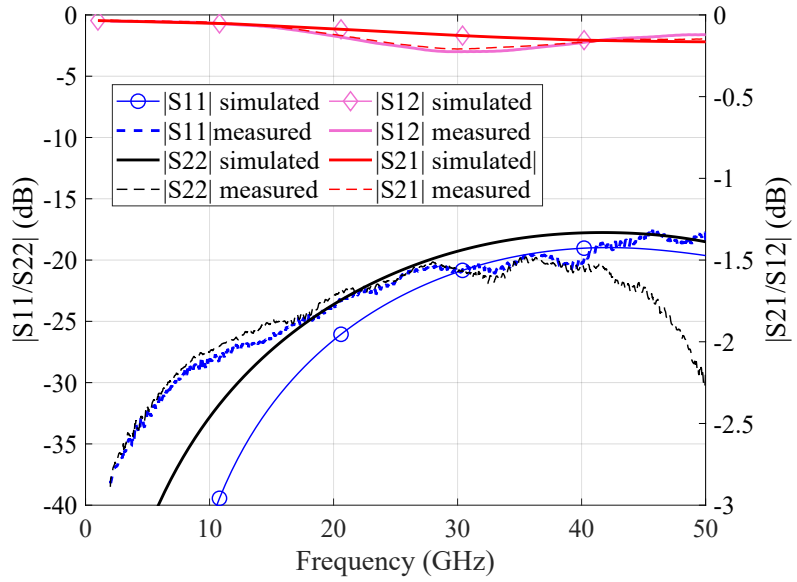
with similar cascaded vias as the ones described earlier. Fig. 4.4b shows a symmetric version of this interconnect that transitions from GCPW to microstrip and then back to GCPW. Like the asymmetric version, each segment of transmission line is made long enough to properly transition between modes. Because the symmetric version includes two transitions, it is about 60% longer and therefore expected to be slightly lossier.

4.2.2 Calibration and Measurements

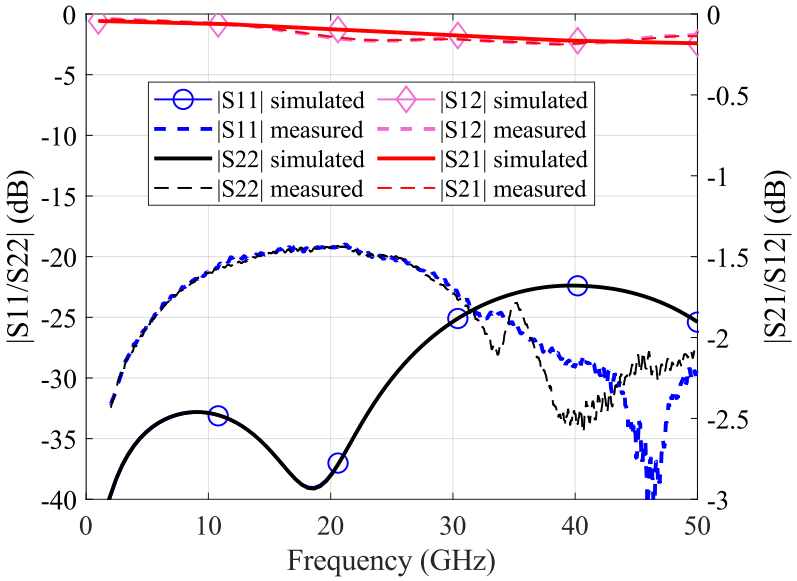
Measurements are performed using an Agilent 38343C PNA and a Summit 9000 probe station with FormFactor ACP-50-A-GSG-150 probes. Calibration is performed using the Cascade Microtech 101-190C off-chip set of alumina 50 Ω SOLT calibration standards. Although on-chip calibration TRL standards are included on the wafer, they do not let us know how close our designs are to 50 Ω, and so an off-chip reference is used. Each interconnect structure is fabricated a total of 16 times across two wafers, and all were measured. The plotted results presented in this section are from interconnects showing average performance among those tested.

First, measured compared to simulated results for the assymetric interconnect is plotted in Fig. 4.5a. Results show a return loss better than 20 dB across a majority of the band and better than 17 dB across the entire band. Measured insertion loss is below 0.3 dB across the frequency range. As shown, measurements agree well with simulation save for an increase in measured insertion loss between 20 and 40 GHz. Fig. 4.5b. shows simulated and measured performance for the symmetric interconnect. Although the simulated and measured return loss do not agree well at lower frequencies, the measured return loss is still better than 20 dB across a majority of the band. The measured insertion loss is less than 0.16 dB across the band and agrees well with simulation. Notably, the dip in insertion loss centered at 30 GHz in the asymmetric design is not present in the symmetric back-to-back GCPW interconnect. One potential cause of this discrepancy is that the assymetric interconnect uses a cascaded GSG pad, shown boxed in blue in Fig. 4.6, to launch the M2-M3 microsrip mode, while the symmetric one uses GCPW pads on both sides.

To further investigate the increased insertion loss of the assymetric design, a Through-Reflect-



(a)



(b)

Figure 4.5: Simulation and measurement results from 2 to 50 GHz for the (a) GCPW-to-microstrip interconnect and the (b) GCPW-to-microstrip-to-GCPW interconnect .

Line (TRL) calibration is performed using both a M1-M2 and a M2-M3 microstrip calibration kit designed and manufactured on the same wafer. $|S_{11}|$ of the reflect standards (in this case short

circuits) are measured and compared between both M1-M2 and M2-M3 as shown by the plot in Fig. 4.6. A 0.1 dB difference is seen between M2-M3 and M1-M2 at 30 GHz, leading to the conclusion that the dip in insertion loss seen across the interconnect measurements is at least in part due to the cascaded pads that were designed out-of-house by Qorvo. This can be mitigated in future designs by more detailed full-wave EM simulation and a redesign of the pads.

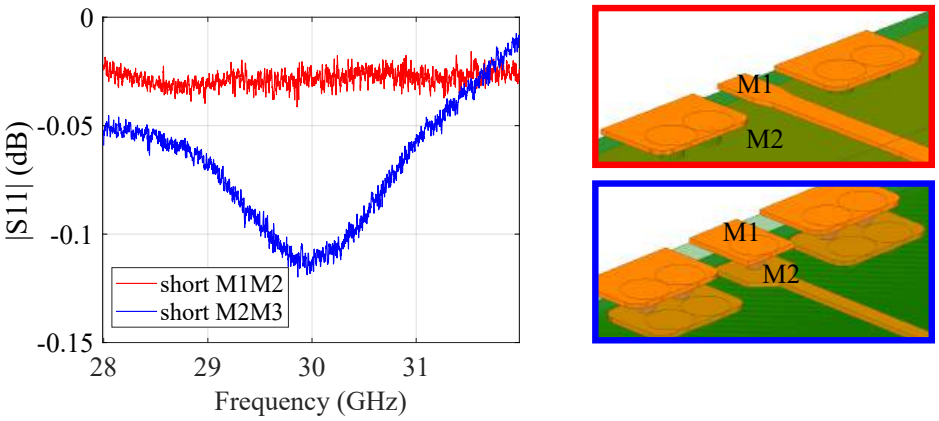


Figure 4.6: Measured reflection coefficient of M1-M2 and M2-M3 "short" standards between 28 and 32 GHz.

4.3 Repeatability Analysis

The fabricated wafer is divided into four larger quadrants, including two repeated layouts labeled "a" and "b". The northwest quadrant is quadrant 1 while the southeast is 4. The label system shown in Fig.4.7a is used to associate measurement results to exact test structures sites on the wafer. On each wafer, there are 8 MS-MS, 8 MS-SL, 8 GCPW-MS interconnects and 16 coaxial TSV interconnects, a total of 80 test structures across a high-resistivity (HRS) and a low-resistivity silicon (LRS) wafer which discussed in further detail in [64]. However, this chapter focuses only on the GCPW interconnects.

Measurement results are collected for the majority of the test structures on both wafers, leading to the two colored maps shown in Fig. 4.7b, which shows quadrant 1 for both the high and low resistivity wafers. Based on repeated measurements across quadrants, it is possible to

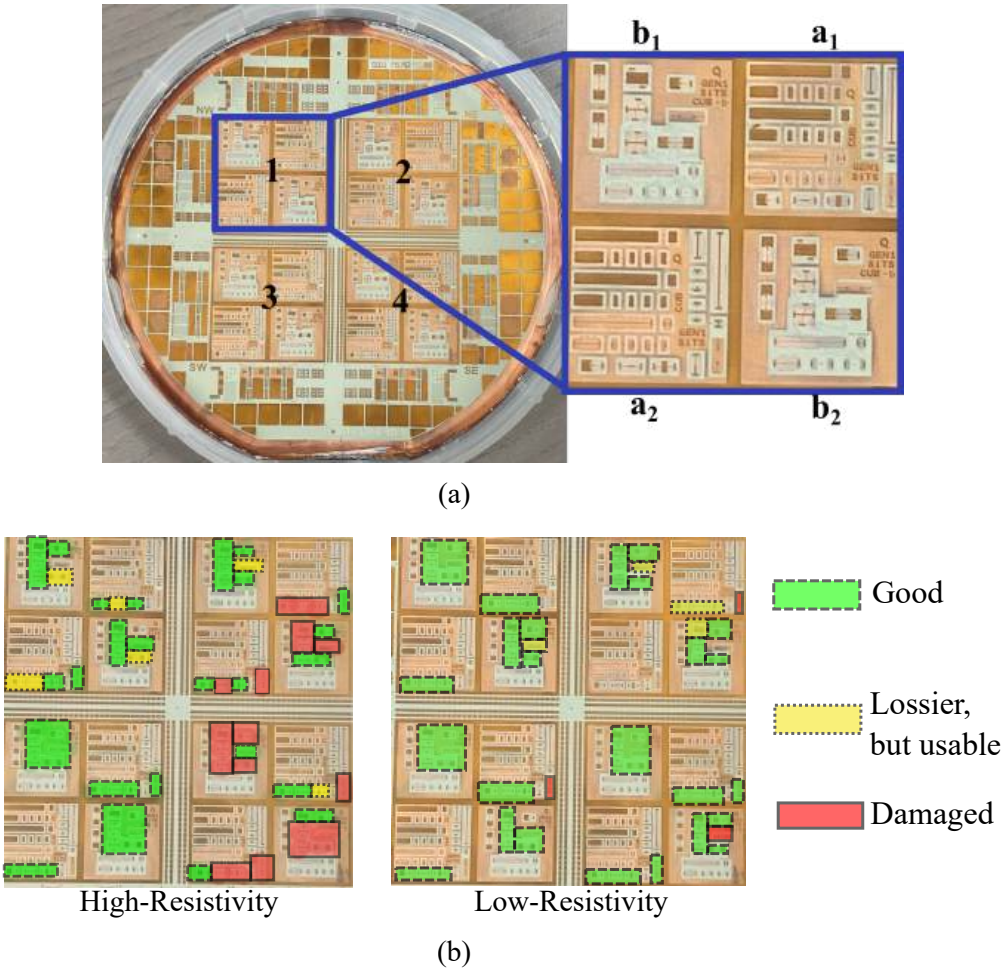


Figure 4.7: (a) Map of the wafer is sectioned in 4 quadrants; each quadrant consists of 2 different layouts a and b with various test structures, some repeated across the layout and others unique to each quadrant. The quadrants are organized as b1,a1 going left to right on the top row and a2,b2 on the bottom row. (b) One quadrant of the high-resistivity silicon wafer (left) and low-resistivity silicon wafer (right), showing good, usable and damaged sites on each quadrant of the wafer. The damaged sites are due to defects in the fabrication or assembly of the wafer.

identify when a defect in fabrication affected a test structure. The affected areas of the wafer are labeled as "damaged", while the non-affected areas are "good". A is site considered damaged if the S-parameters behave much differently compared to both simulations and other measured sites. An example of this can be seen in Fig. 4.8, showing heavily degraded performance especially at low frequencies. Plots showing measurements for both return loss and insertion loss of undamaged GCPW-to-microstrip interconnects are shown in Fig. 4.9. Additionally, there is a third category

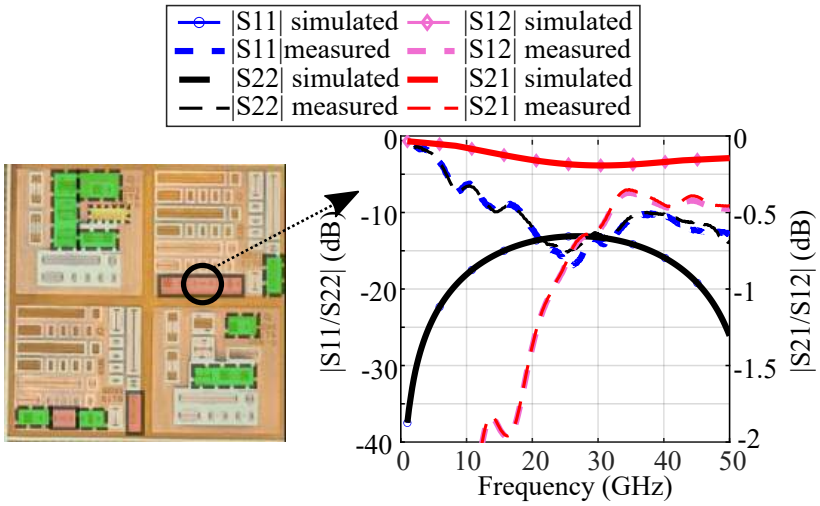


Figure 4.8: Measurement results on damaged site, located on quadrant 2 layout a1 on HRS wafer.

of site that is lossier, but is still deemed usable. An example of this is site 2a1 shown in Fig. 4.9. Overall, measurements of undamaged sites show good agreement in performance across the wafer.

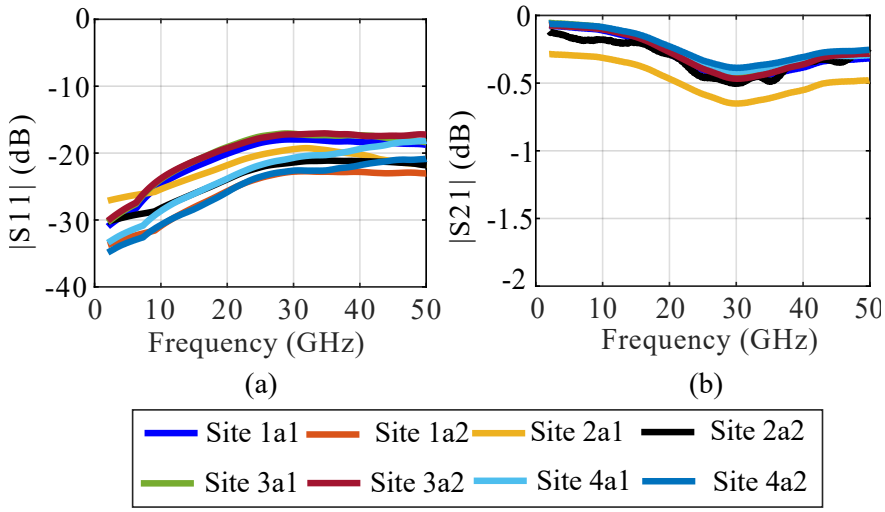


Figure 4.9: Return loss and Insertion loss measured for GCPW interconnect test structures on the "a" quadrants on LRS wafer.

4.4 Multilayer Passive Circuits

In addition to the transmission lines and interconnects described above, a number of other test structures are also designed. Included in the wafers discussed so far (generation 1) are a set of GCPW and microstrip corss-overs designed to evaluate cross-coupling between metal layers. Additionally, a set of broadside GCPW-to-microstrip couplers as well as substrate-integrated-waveguide (SIW) band-pass filters are included in a second set of sub-diced wafers (generation 2).

4.4.1 Generation 1 Cross-Overs

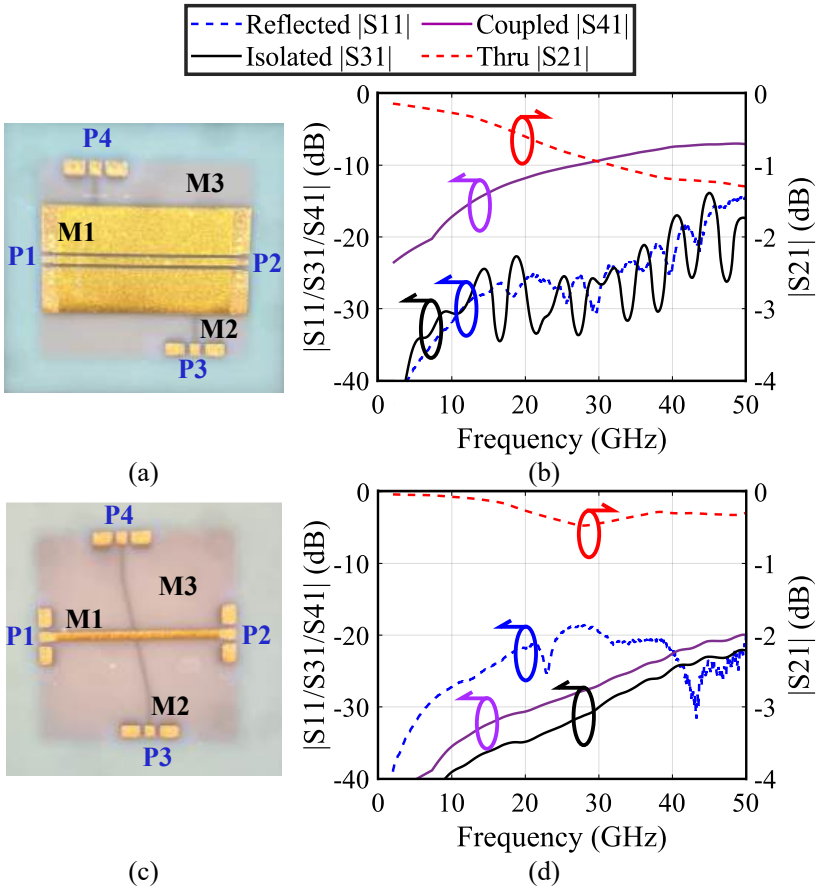


Figure 4.10: (a) M1-M3 GCPW line above a M2-M3 microstrip line with (b) corresponding measured S-parameters. (c) M1-M3 microstrip line above a M2-M3 microstrip line and (d) corresponding measured S-parameters.

Both microstrip and GCPW transmission lines use metal layers 1 and 2 with metal layer

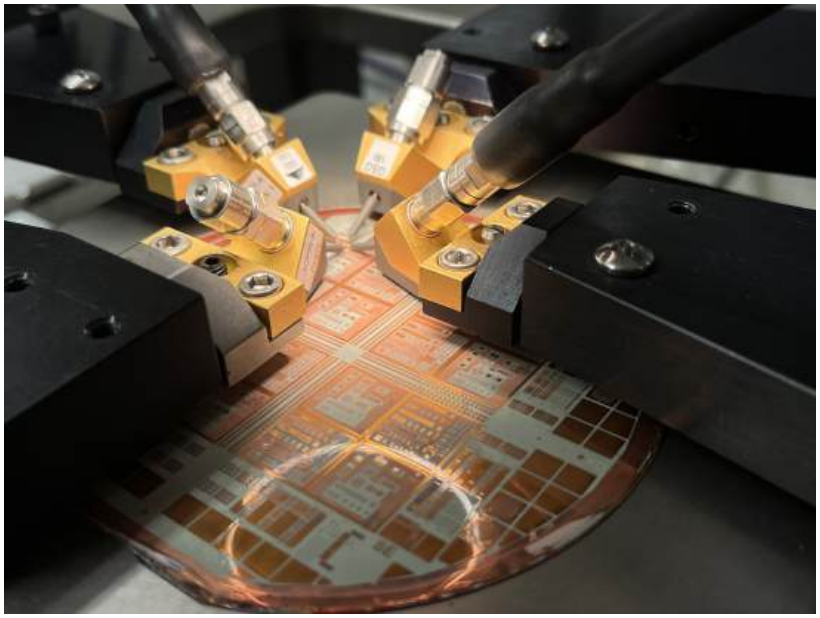


Figure 4.11: Measurement setup for cross-coupling test structures. 4-port S-parameter measurement setup using an Agilent 38343C PNA with a Summit 1000 probe station. Two ports at a time are terminated with SMA 50 Ω loads, and $2 \times$,2 S-matrices are combined in post-processing to form the 4×4 S-matrix of the test structure.

3 serving as a ground plane. These 50 Ω lines are fabricated as shown in Fig. 4.10 in order to investigate the level of "cross-talk" or unwanted coupling between lines on different layers. Two structures are shown: one with a M2-M3 microstrip line under a M1-M3 GCPW line (Fig. 4.10a); and the other with a M2-M3 microstrip line under a M1-M3 microstrip line (Fig. 4.10c). Each of these pairs of lines is treated as a poor 4-port coupler and measured using the setup shown in Fig. 4.11. The fraction of input power that is seen at the "coupled" port directly corresponds to the amount of cross-talk between the lines. In the GCPW case, the lower-level microstrip line is oriented parallel and directly under the center conductor, similarly to a broadside coupler, to demonstrate a case in which significant cross-talk would be present, Fig. 4.10b. This results in considerably more coupling than in the case of the nearly perpendicular orientation shown for the two microstrip lines, Fig. 4.10d, with less than 20 dB coupling up to 50 GHz.

4.4.2 Generation 2 SIW Filter

Several other passive circuits are designed for a second-generation wafer, shown in Fig. 4.12. The first example is a substrate-integrated waveguide (SIW) 37-40 GHz band-pass filter, chosen for its unique architecture that uses different metal and dielectric layers, Fig. 4.14a. The design consists of a pair of tapered M1M3 microstrip lines leading up to a copper sheet on metal layer M1.

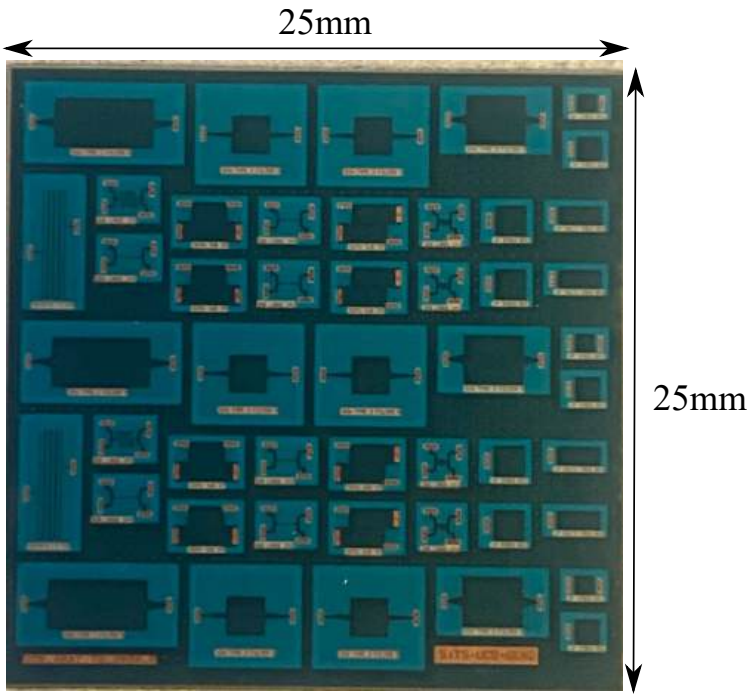


Figure 4.12: Photograph of the second-generation SHIP RF 25 mm by 25 mm reticle. The layout includes passive circuits (resonators, filters and couplers), fabricated on the stack-up with cross-section shown in Fig 1(b).

The side edges of the copper sheet are connected through a via wall to metal layer M3, forming the M1M3 SIW. The dimensions of the SIW are chosen to align the cut-off frequency with the lower end of the desired band. The SIW is then converted from a high-pass filter to a band-pass filter with the inclusion of the resonant slots in metal layer 1, similar to the complimentary split-ring resonators shown in [65]. The functionality of these slots in- and out-of-band is illustrated in

Fig. 4.14a through the normalized electric field magnitude between the metal layers of the SIW. The simulated and measured S-parameters in Fig. 4.14b show minimum insertion loss of about 2.8 dB and 3.8 dB respectively. As seen by the figure, there is significant drop in return loss and increase in insertion loss accompanied by a 2 GHz shift in center frequency between simulation and measurement. The measured return loss reveals that this is the result of a wider double resonance which shifts the center frequency and negatively impacts the 50 Ω match. A preliminary tolerance study has been conducted on the critical dimensions of the SIW filter, such as the resonator slot width. However, additional future work is required to determine the exact cause of the discrepancies between measurement and simulation.

To better understand the behavior of the SIW filter, simulations are used to analyze its loss mechanisms. For any amount of power entering the SIW filter through either port and not exiting again, there are 3 ways this power can be lost: (1) Power is dissipated in the dielectric; (2) power is dissipated due to conduction loss; and (3) power escapes the structure as radiation. Fig. 4.13a plots the S-parameters of the SIW filter when it is lossless, has dielectric loss, has conduction loss in the copper, and has both dielectric and conduction loss. The third mechanism is also illustrated in Fig. 4.13b which plots the percentage of power lost to radiation over frequency. As shown, radiation loss is highest in the pass-band of the filter, but still remains just over 3%. Overall, the most significant source of loss in the system is the conduction loss which sits at about 82% of the total lost power.

4.4.3 Generation 2 GCPW Broadside Couplers

The second example, shown in Fig. 4.15, is a set of 3-dB and 6-dB broadside coupled-line couplers designed to couple between GCPW and microstrip lines on different metal layers. The couplers consist of GCPW lines and microstrip lines on metal layers M1 and M2 respectively. Both types of transmission lines share a ground plane on metal layer M3 and run parallel, GCPW directly above microstrip, to form the coupling region. The primary difference between the 3-dB and 6-dB couplers is the larger gap between the GCPW signal lines and parallel ground plates in the case of

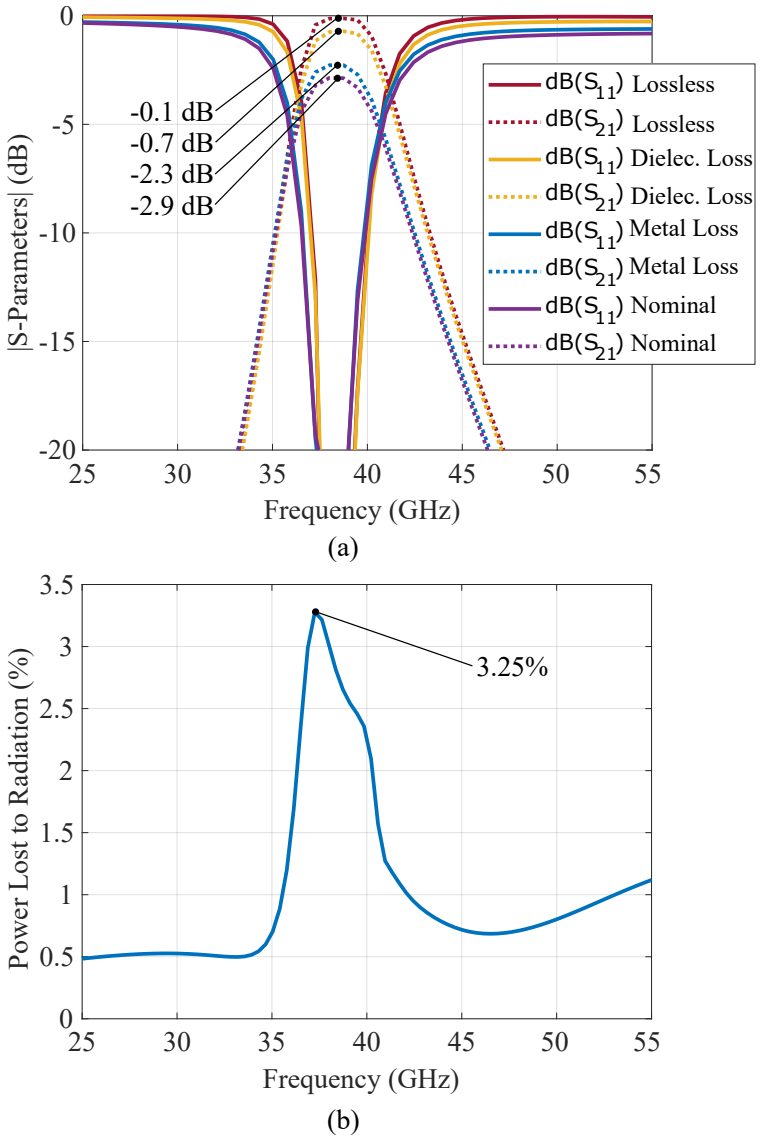
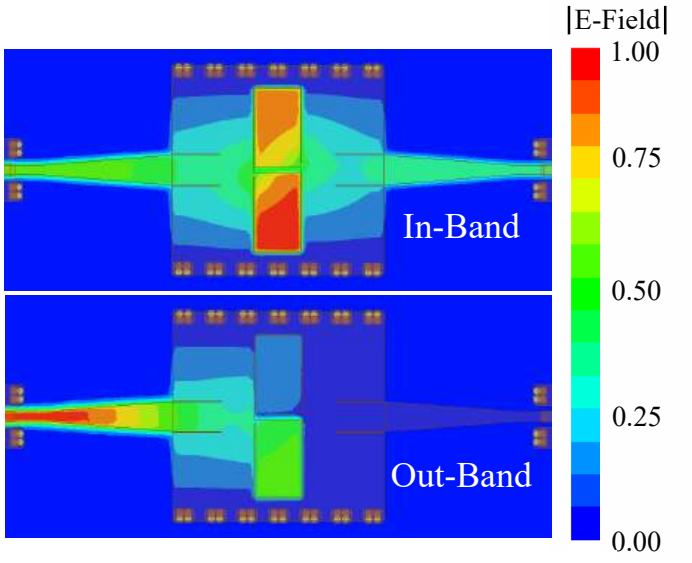
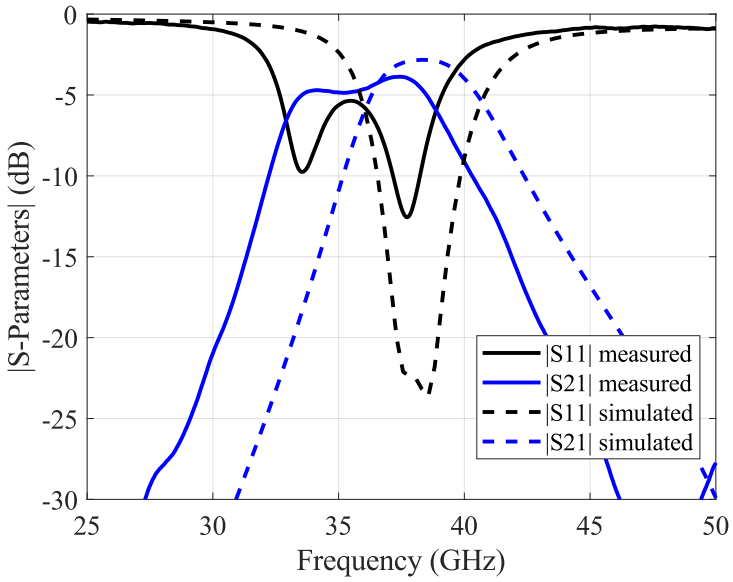


Figure 4.13: (a) Simulated $|S_{11}|$ and $|S_{21}|$ of the SIW filter for cases when it is lossless, has dielectric losses, has conduction losses, and has both dielectric and conduction losses. (b) Simulated percentage of power lost to radiation over frequency of the SIW filter.

the 3-dB coupler. In addition to the gap, the widths of both the GCPW and microstrip signal lines are widened to account for the change in impedance. Both the larger gap and the wider signal lines lead to an increased amount of coupling between the lines. Fig. 4.15 shows simulated performance for both couplers and measured performance of the 6-dB coupler, showing good agreement across frequency with the exception of increased loss. Unfortunately, the manufacturing of the 3-dB coupler prevented it from being properly probed and so it was not measured.



(a)



(b)

Figure 4.14: (a) Three dimensional illustration of a substrate integrated waveguide (SIW) filter designed on wafer. The normalized magnitude of the electric field inside the SIW is shown for both an in-band frequency (38 GHz) and an out-of-band frequency (33 GHz). (b) Simulated and measured performance of (37-40 GHz) SIW filter.

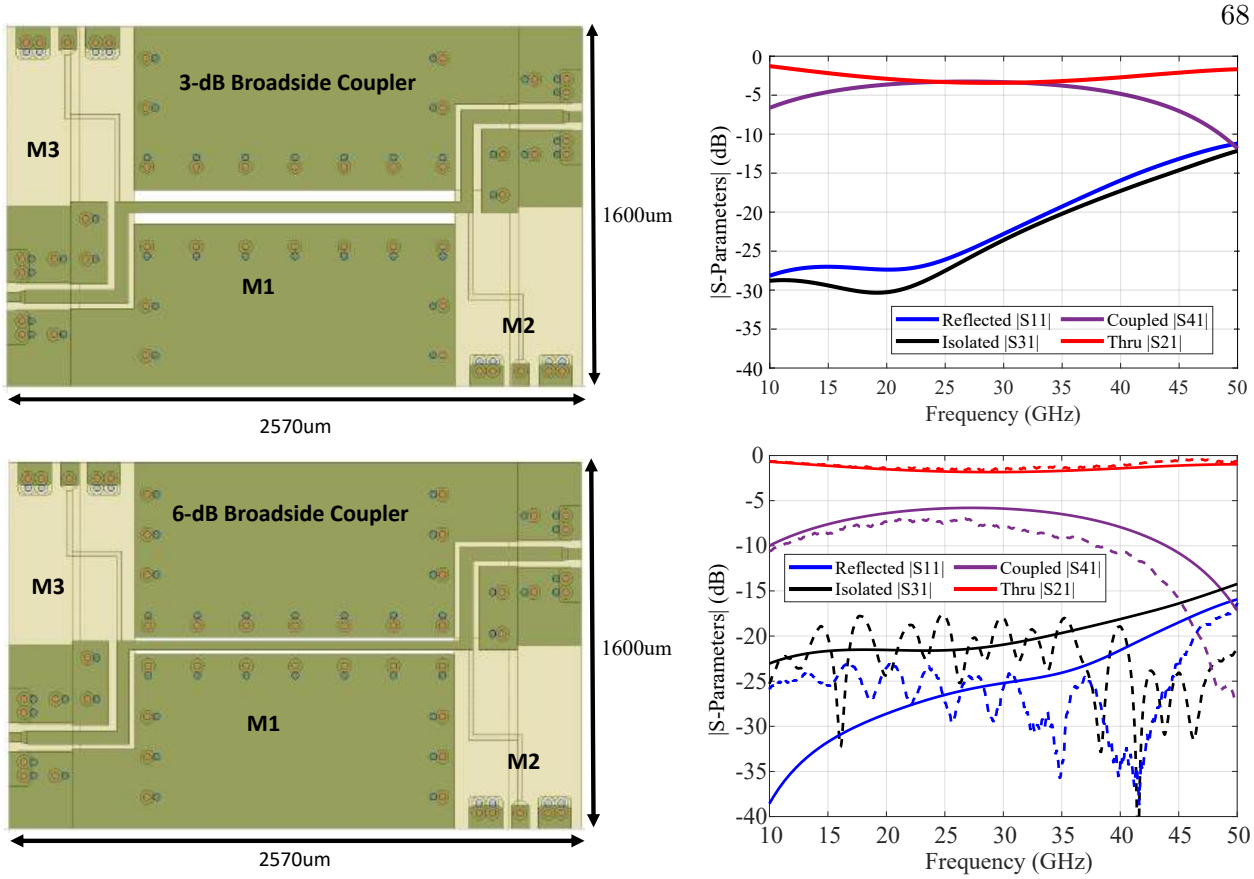


Figure 4.15: A (top left) 3-dB and a (bottom left) 6-dB Grounded Coplanar Waveguide (GCPW) broadside coupler. The couplers are coupled-line couplers with a GCPW on top metal M1 with the signal line coupling to microstrip line directly underneath, on M2. Both lines share a ground on M3. Simulated S-parameters of the 3-dB and 6-dB GCPW-MS couplers are shown on the (top right) and (bottom left) respectively. Measured S-parameters are also shown for the 6-dB coupler as dashed lines.

4.5 Chapter Conclusions

In conclusion, this chapter presents a variety of broadband, low-loss interconnects designed on an experimental process that includes 6 organic resin-filled dielectric layers, a central silicon interposer and 6 metal layers to use for design purposes. Measurements are presented from 2 to 50 GHz for 2 GCPW-to-microstrip interconnects using 3 metal layers. The first interconnect is assymetric, transitioning from GCPW on M1M3 layers to microstrip on M1M2, showing an insertion loss less than 0.3 dB across the band. The second interconnect is symmetric and includes

an additional transition back to M1M3 GCPW, showing an insertion loss less than 0.16 dB across the band. Additionally, cross-over lines are designed and characterized to evaluate cross-coupling between lines on different metal layers. Although the interconnect designs are meant to operate from dc to 50 GHz and are measured to 50 GHz, the interconnects presented are simulated to 110 GHz to investigate how performance degrades. Figure 4.16 shows the simulated S-parameters of the GCPW-MS interconnect from dc to 110 GHz, pointing to a predicted degradation in both insertion and return loss with increasing frequency. Additionally, the degradation in return loss suggests that interconnects can be redesigned for a better impedance match at higher frequencies.

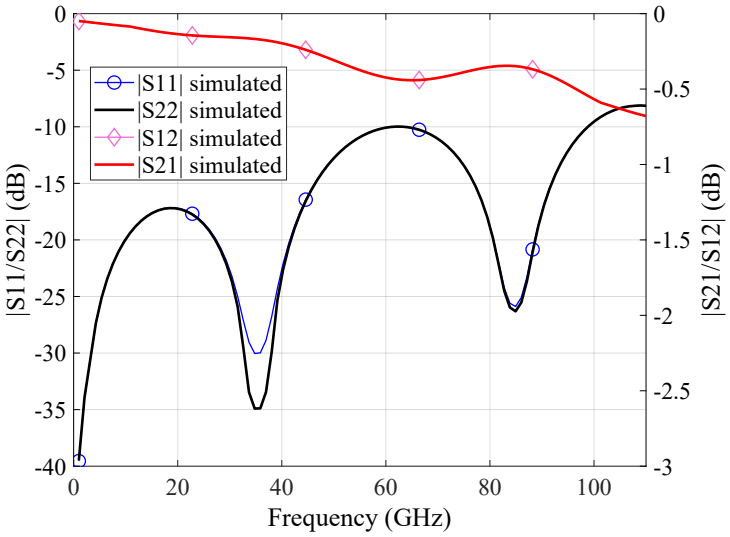


Figure 4.16: Simulated performance of the microstrip-to-GCPW interconnect up to 110 GHz.

Several more complex structures are also simulated and measured for the second generation of the process,including a multi-layer, Ka-band, SIW filter is simulated and measured. An analysis of the loss mechanisms for the SIW filter is also presented, showing 82% of lost power is a result of conduction loss. Additionally, both a 3-dB and 6-dB version of a GCPW-to-microstrip broadside coupler are designed and characterized. Generally, measurements show good agreement with simulations and are repeatable across multiple iterations of each passive structure. The demonstrated circuits show a path to high-density low-loss passives and interconnects at millimeter-wave

frequencies. The results discussed in this chapter are reported in [63, 66, 64].

Chapter 5

A 5-W Ka-band GaN-on-SiC Power Amplifier

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5.1 Introduction

Radio-frequency communications play an essential role in space exploration and space science [67]. For future deep space missions, communications at Ka-band carrier frequencies can significantly increase the data rate and measurement resolution to maximize the scientific return when compared with current S and X-bands. In addition to high data rates, long-range transmitters in deep space demand high output power levels and high efficiency. An additional application of high-power, high-efficiency Ka-band PAs is in wireless power transfer at and above 30 GHz [68] [69] [70]. The primary motivation behind moving to higher frequencies for power beaming is the reduction in antenna size which leads to more compact systems. For example, the rectenna arrays discussed in Ch. 2 and Ch. 3 could be re-designed to operate at Ka-band using a nearly identical topology with higher frequency rectifying diodes and smaller antenna elements. Several published works already demonstrate high-efficiency rectification at Ka-band [71] [72], highlighting a demand

for efficient solid-state sources on the transmitting side of a WPT system in the same frequency range. The goal of the PA designs presented in this chapter is to enhance the efficiency and output power at the MMIC level. Then, with subsequent external power combining, these chips can be suited for improved solid-state transmitters for applications including deep-space communications and wireless power transfer.

Examples of published Ka-band GaN PAs that demonstrate more than 1 W of output power include implementations in 200-nm processes with up to 10 W of output power at 31.5 GHz with 25 dB of gain and 36% PAE[25]. In a smaller 150-nm node, output power up to 40 W is shown in pulsed operation with 30 dB of gain and 25.9% PAE [73]. These excellent results do not report simulated large-signal performance, and in [25], the small-signal measured performance is shifted 2 GHz ($> 6\%$) lower in frequency. Here we present a 3-W 3-stage Ka-band PA designed in a new 120-nm GaN HEMT process, and compare the performance to nonlinear simulations using two generations of device models. Due to its smaller gate length, this process could potentially offer higher gain at Ka-band or a better trade-off between gain and efficiency. A comparison summary with the state-of-the-art Ka-band PAs found in literature is given in the conclusion of this chapter.

5.2 Design Considerations

The PA is designed in the WIN 120 nm GaN-on-SiC process using Cadence AWR. This 50μm thick GaN-on-SiC process features a 120 nm gate length and an f_t of approximately 40 GHz. It has 3 metal layers, both thin-film and mesa resistors, edge-lifted capacitors and 91 μm$\times$61 μm back-vias. A scaled nonlinear HEMT device model is provided, with the 2$\times$25 μm, 2$\times$50 μm, 4$\times$50 μm, and 6$\times$50 μm sizes validated experimentally.

In order to reach sufficient gain and output power, the PA is designed with 3 stages and a staging ratio of 1:2:4 with the final stage consisting of 4 devices with 6$\times$100 μm periphery. Fig. 5.1 shows a photograph of one such MMIC power amplifier along with a simple diagram of its 3 stages. The devices have a drain bias of 28 V and are operated in Class AB with 60 mA of quiescent current each to maintain a balance between gain and efficiency.

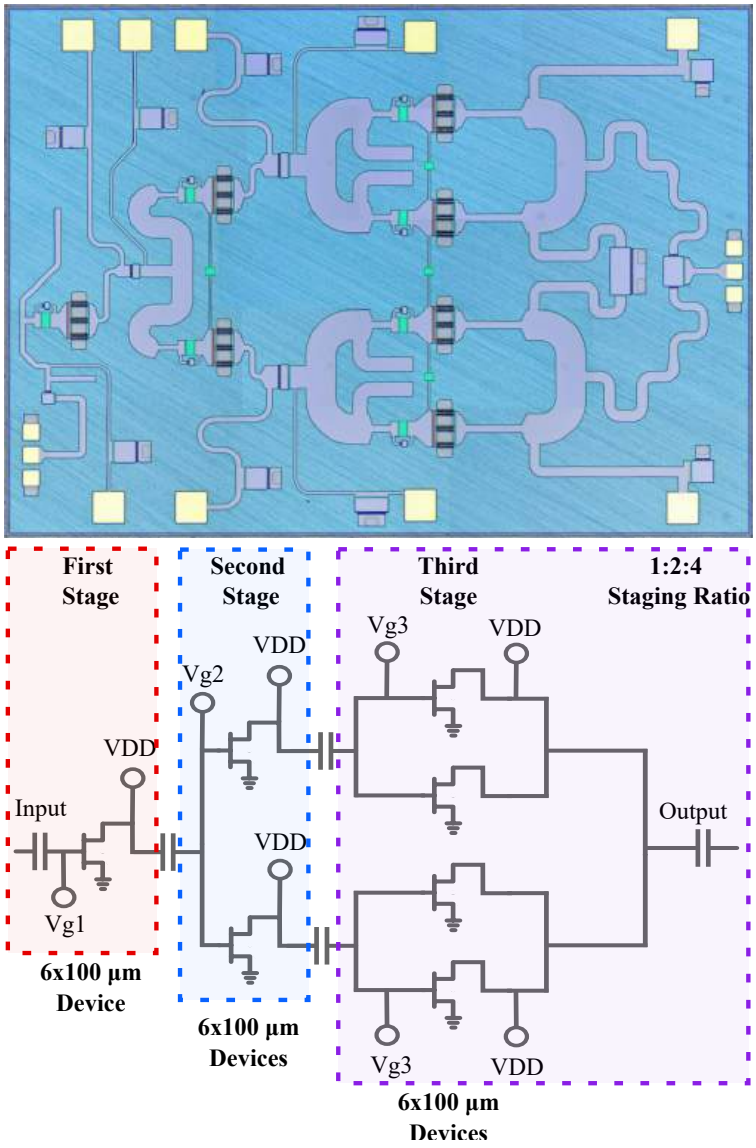


Figure 5.1: Photograph of the MMIC PA with sketch of staging.

Numerous device sizes, ranging from $4\times50\,\mu$m to $8\times100\,\mu$m, including validated and non-validated device sizes, are load pulled in simulations at 32 GHz over a range of input powers and bias conditions. A Smith chart plot showing the impedances and output power that result in maximum PAE for each of these device sizes can be found in Fig. 5.2. Ultimately a 6 finger device with a 100 μm gate width is chosen and used for all three stages. Although it is just outside of the validated range of device sizes, simulations show it as the best compromise between output power and PAE when

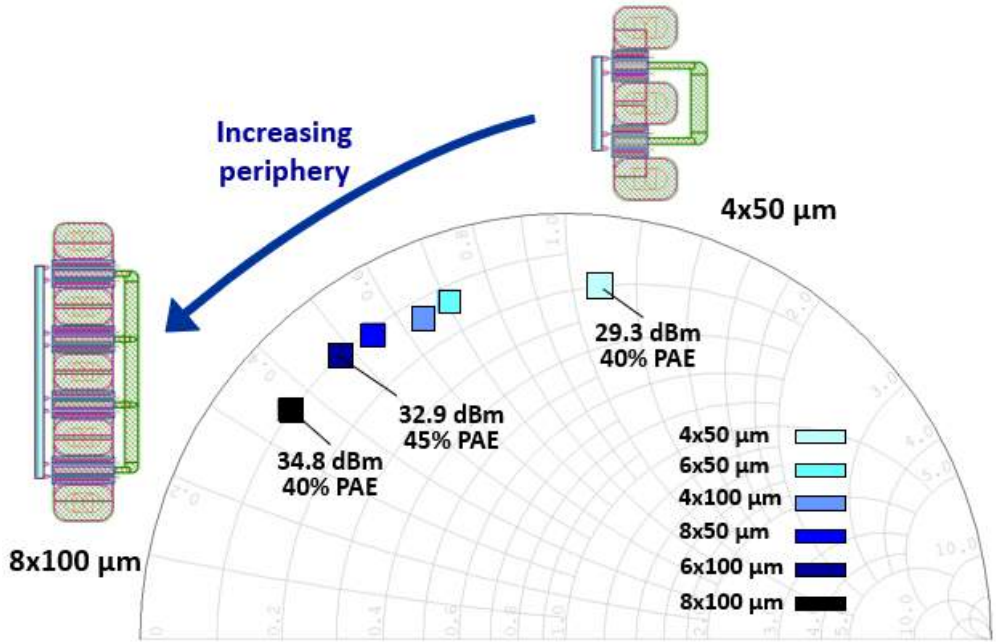


Figure 5.2: Loadpull points for a range of device sizes showing impedances that result in maximum PAE for each device size. The plot also shows the output power that results in highest efficiency at those impedances. Devices range from $4\times50\,\mu$m to $8\times100\,\mu$m peripheries and the Smith chart is normalized to $50\,\Omega$. The $4\times100\,\mu$m, $6\times100\,\mu$m, and $8\times100\,\mu$m devices are scaled models and not experimentally validated.

biased in class AB. The equivalent resistance and capacitance values for the $6\times100\,\mu$m device under the chosen conditions are determined to be $137\,\Omega$ and 0.19 pF respectively. These values are then used to build an ideal 2-port matching network using lumped-element inductors and capacitors. In the case of the output matching network, where 4 devices will be combined in-phase, the two port matching network transforms Z_L=$50\,\Omega$ to the equivalent resistance and capacitance of 4 devices in parallel as shown in Fig. 5.3a. The 2-port matching network is then expanded into a 3-port, 2-way and then 5-port, 4-way combiner/matching network by splitting the lumped components into multiple parallel components and scaling inductance and capacitance appropriately. An equivalent 2-way combiner with lumped elements is shown in Fig. 5.3b. This method for designing corporate combined matching networks is discussed in greater detail in [74].

The ideal lumped element ouptut network is then converted into microstrip by transforming series inductor and shunt capacitor Π and T sections into equivalent short lengths of transmission

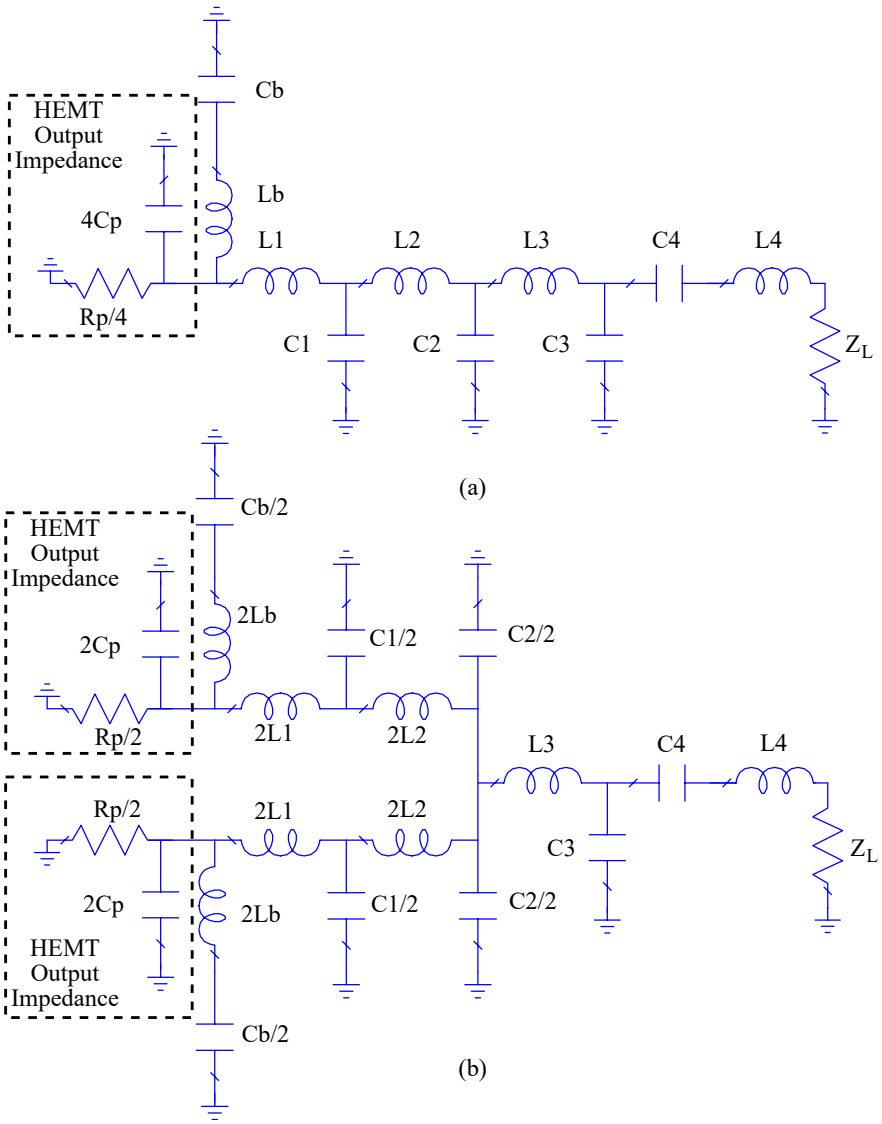


Figure 5.3: (a) Schematic of a 2-port matching network made from lumped element components. (b) Scaled version of matching network to also become a 3-port 2-way combiner. Inductor values are doubled and capacitor values are halved.

lines. This process is also repeated for the inter-stage matching networks but with 3 ports instead of 5 and with complex impedances presented at every port given they are not matching to 50 Ω. In the case of lumped-element capacitor values too large to realize through segmented transmission lines, open stubs are used to compensate. Examples of these open stubs can be seen in some of the inter-stage combiners in Fig. 5.4. Additionally, bias lines, initially represented as inductors,

are converted into $\lambda/4$ lengths of line (centered at 32 GHz) terminated in a large shunt capacitor. Quarter wavelength bias lines are a good option given the low fractional bandwidth and high output power of this design. The drain bias lines in the output stage are designed to be 70 μm wide to handle the necessary high dc current draw. Another important addition to the output matching network are the "dummy bias" lines terminated in a large shunt capacitor that can be seen at the center of Fig. 5.4. They are added to maintain symmetry between the inner and outer pairs of transistors in the combiner due to unequal loading, which could deteriorate performance and cause odd-mode instability. The dummy lines are designed to be of equivalent length to the actual bias lines and both terminate in a single shunt capacitor which is twice the value of the ones used in either bias line.

Throughout the design process, stability criteria are repeatedly checked. Small-signal S-parameters and both linear and nonlinear Nyquist stability are simulated over a range of port impedances and bias conditions across the modeled frequency range. Stability networks are realized in the layout in the form of parallel RC high-pass filters at the gates of each device. The resistor and capacitor values are 25 Ω and 0.3 pF, respectively. Additionally, 37.5 Ω resistors are connected between the gates of the transistors in each stage to help prevent odd-mode oscillations. Finally, all passive components are full-wave simulated within the final layout using the AWR Axiem 2.5D EM solver.

5.3 Comparison of Experimental and Simulated Results

Once the fabricated chip is received, it is mounted on a CuMo carrier and the bias lines are wire-bonded to off-chip 100 pF and 1000 pF single-layer capacitors as shown in Fig. 5.5. Additionally, the gate pads are bonded directly to a series 50 Ω surface mount resistor for further protection against instability in the bias lines.

The power amplifier is characterized in both large and small-signal and compared with simulated performance. Fig. 5.6a. shows a comparison between the simulated and measured large signal performance over frequency. As shown by the figure, there is an approximately 800 MHz

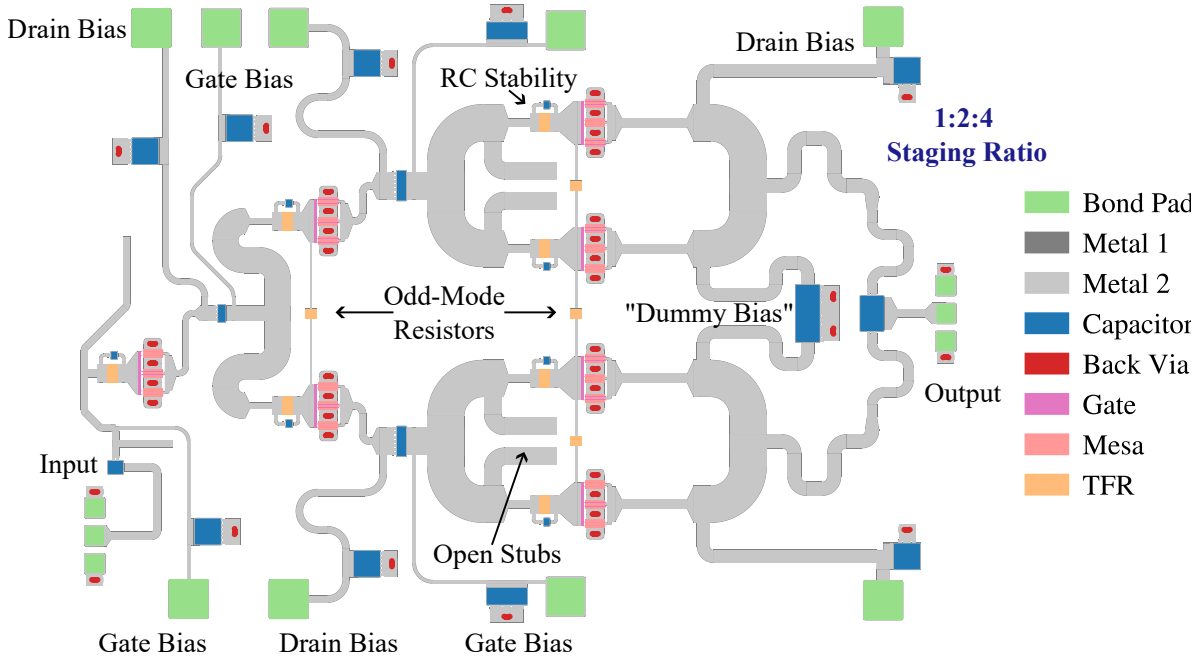


Figure 5.4: Final layout of the first PA design with key components highlighted. The total chip dimensions are 5 mm × 3 mm.

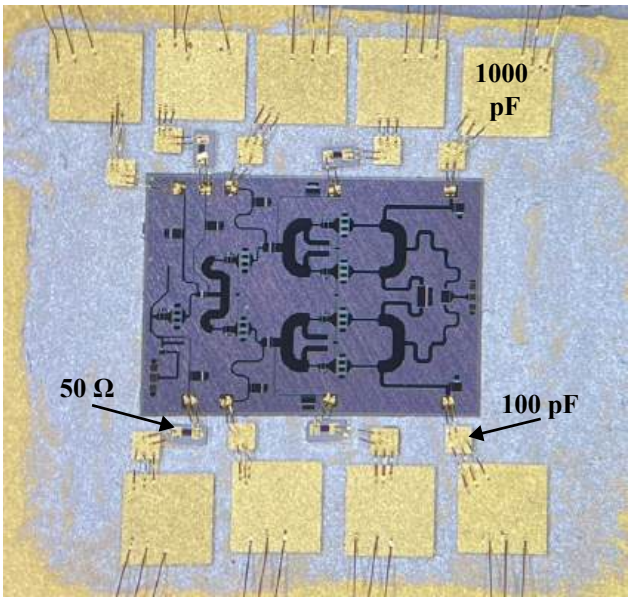


Figure 5.5: Photograph of fabricated PA mounted on a CuMo carrier and bonded to off-chip 100 pF and 1000 pF capacitors for dc-biasing. Each gate pad is also bonded to a 50 Ω series resistor to help with stability. The chip in the center of the photograph is 5 mm × 3 mm.

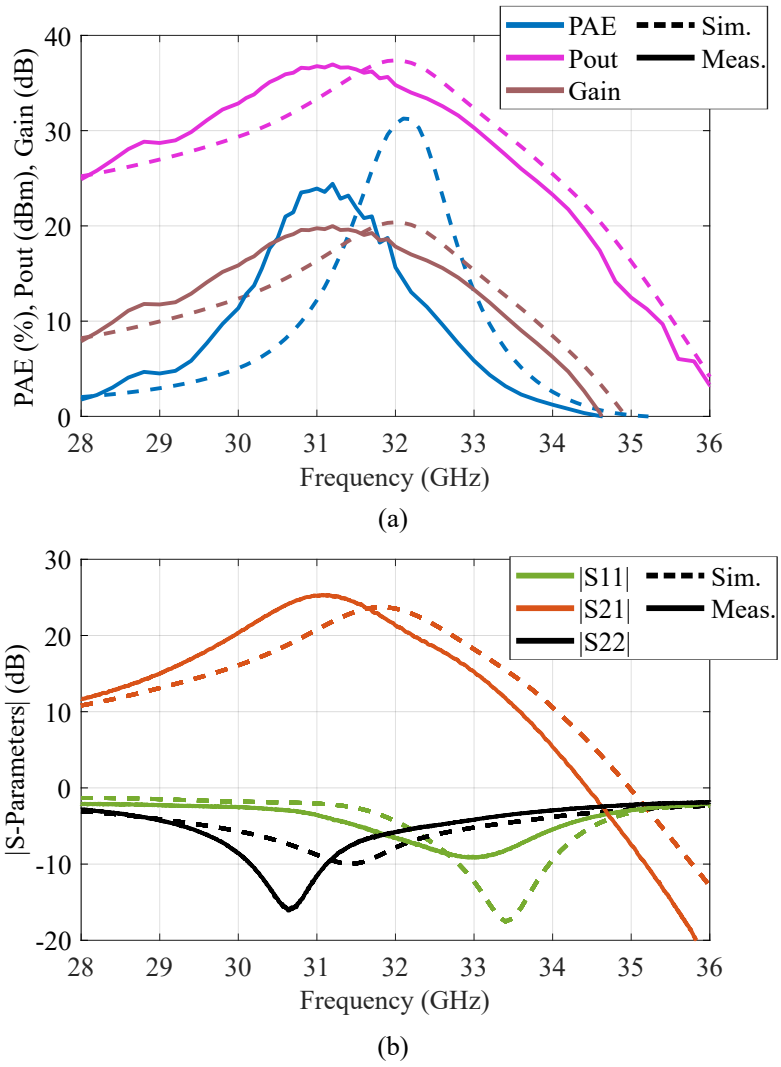


Figure 5.6: Measured vs. simulated (a) large-signal performance at 17 dBm input power and (b) small-signal performance over frequency, at V_{DS} =28 V. The total quiescent current for all devices is 420 mA, and all stages are biased at the same current as in the simulations.

(2.5%) shift downwards in frequency between the simulated and measured results. We also see a significant reduction in PAE without a corresponding loss of gain, indicating an increase in dc power consumption compared to simulation. At an input power of 17 dBm, the measured gain is 20 dB and the maximum PAE is 24.5% at 31.2 GHz. Fig. 5.7 compares the drive-up performance across input power. Because the simulated and measured peak performances are at different fre-

quencies, they are each plotted at their respective frequency of operation (32 GHz in simulation and 31.2 GHz in measurement). As shown by the figure, the measurement outperforms simulations at lower input power levels. This is also supported by the measured and simulated small-signal S-parameters plotted in Fig. 5.6b. Although shifted down in frequency, the peak small-signal gain is observed to be higher in measurement than in simulation.

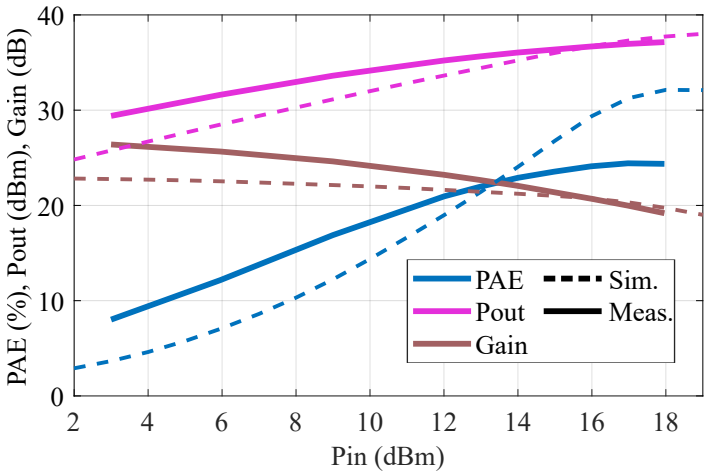


Figure 5.7: Measured vs. simulated drive-up curves of first iteration of PA. Both the measured and simulated data is plotted at the frequency of maximum PAE (32 GHz for the simulation and 31.2 GHz for the measurement). The bias point is the same as in Fig. 5.6.

As the PA is pushed further into compression, both measured gain and output power drop relative to simulated values but not significantly. However, the measured PAE shows a much greater difference compared to simulation than would be suggested by the gain compression, indicating an increased dc current draw not predicted in simulation. One thing that is not accounted for in simulations of this design is that the device heats up due to the large dc current draw. An increase in device temperature can reduce gain and increase current draw, both of which result in reduced efficiency. Fig. 5.8 compares simulated large signal performance for device temperatures of 25° C and 80° C under the same bias and drive conditions, showing reduced efficiency at higher temperatures.

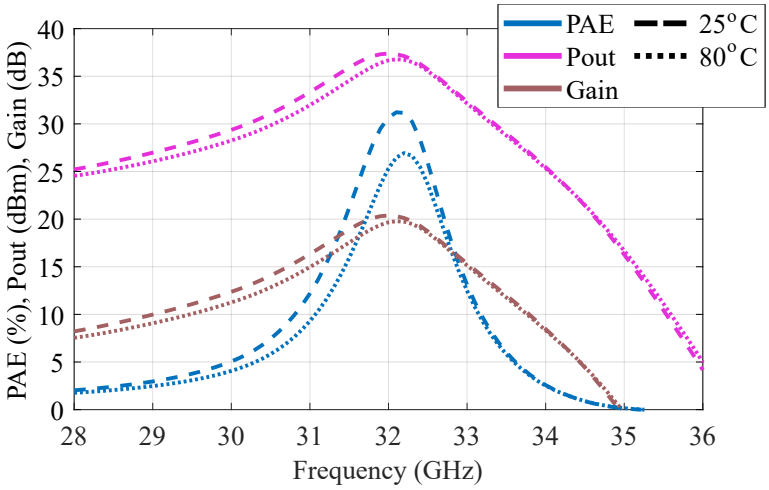


Figure 5.8: Simulated large signal performance over frequency for 17 dBm drive power for the original design at both 25° C and 80° C device temperature. Quiescent current is kept same at both temperatures.

5.4 Redesign and Simulations

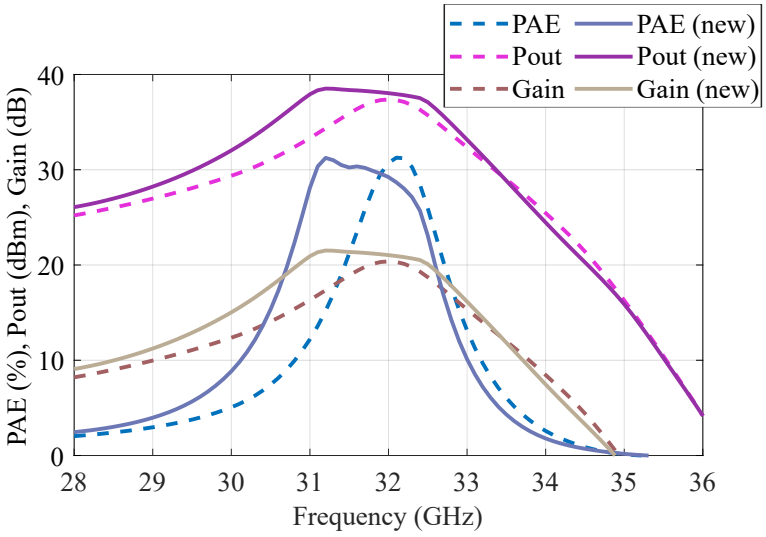


Figure 5.9: Simulated large-signal performance over frequency of first PA iteration using the initial and improved transistor models at 17 dBm input power.

In order to improve the PA performance and address discrepancies between measurement

and simulation, the circuit is redesigned using a similar layout and an updated PDK nonlinear model for the WIN NP12 GaN on SiC process. First, a comparison is made between the device models from the new PDK and those from the initial PDK. Both versions of the device model are integrated with the same EM-simulated, passive layout used in the initial PA design. A large-signal comparison between the two models under the same bias and drive conditions is shown in Fig. 5.9. While not accounting for the full 800 MHz shift seen in measurement, the updated models do show a downward trend in frequency when compared to the initial simulations. However, the comparison does not show the reduction in PAE seen in measurement.

In order to understand this discrepancy, the temperature dependence of the new models are adjusted to more closely reflect expected temperatures in CW measurements. Although the models are not experimentally validated above 25° C, designing the power amplifier for a higher temperature could help account for increased current draw at higher input power levels. The ambient temperature for each device is set to 60° C instead of 25° C, and all passives are re-tuned for the new impedances presented by the device models. The overall layout is preserved, but transmission line lengths and widths are adjusted. Although 60° C is not as hot as the device is likely to get under CW measurement, it is chosen as a compromise on account of the device models not being validated at higher ambient temperatures.

In addition to the changes already discussed, the staging ratio is adjusted to 1:3:6 by reducing the size of the first stage device to $4\times100\,\mu$m. It was determined that the device did not need to be $6\times100\,\mu$m in order to deliver the necessary power to saturate the second stage. The changes in the layouts between the original and redesigned PAs are shown in Fig. 5.10. Reducing the size of the device has two notable benefits: (1) The saturated gain of the amplifier is increased from the first design because it requires a lower input power to efficiently drive the first stage; and (2) the capacitance of the first stage transistor is reduced, resulting in a better input match. Both of these effects can be seen in Fig. 5.11.a and Fig. 5.11.b, which show simulated large and small-signal performance, respectively. This version is designed with maximum PAE at 32.3 GHz instead of 32 GHz with the measured performance anticipated to still shift down in frequency by

200-300 MHz. As shown, at 3-W of output power, the saturated gain is 23 dB and the PAE is 32%. Additionally, the new design shows a much better tolerance to increases in device temperature, as shown by Fig. 5.12. Simulations show a maximum PAE above 30% between 25° C and 80° C which is about 3.5 pp better than the original design while also demonstrating 4 dB higher gain.

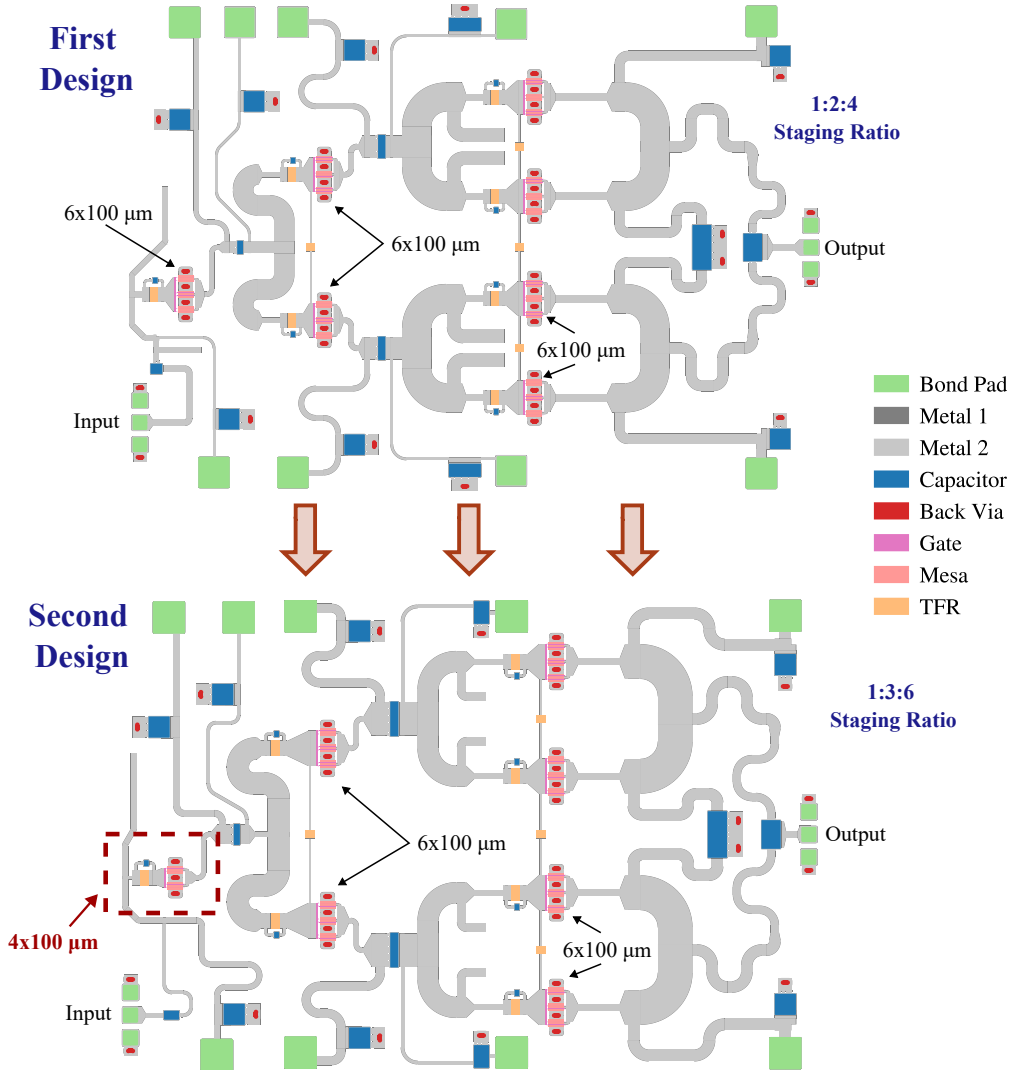


Figure 5.10: Visual comparison between original and redesigned layouts. In addition to adjusting existing matching networks for new device impedances, the first stage device is changed from $6\times100\,\mu$m to $4\times100\,\mu$m.

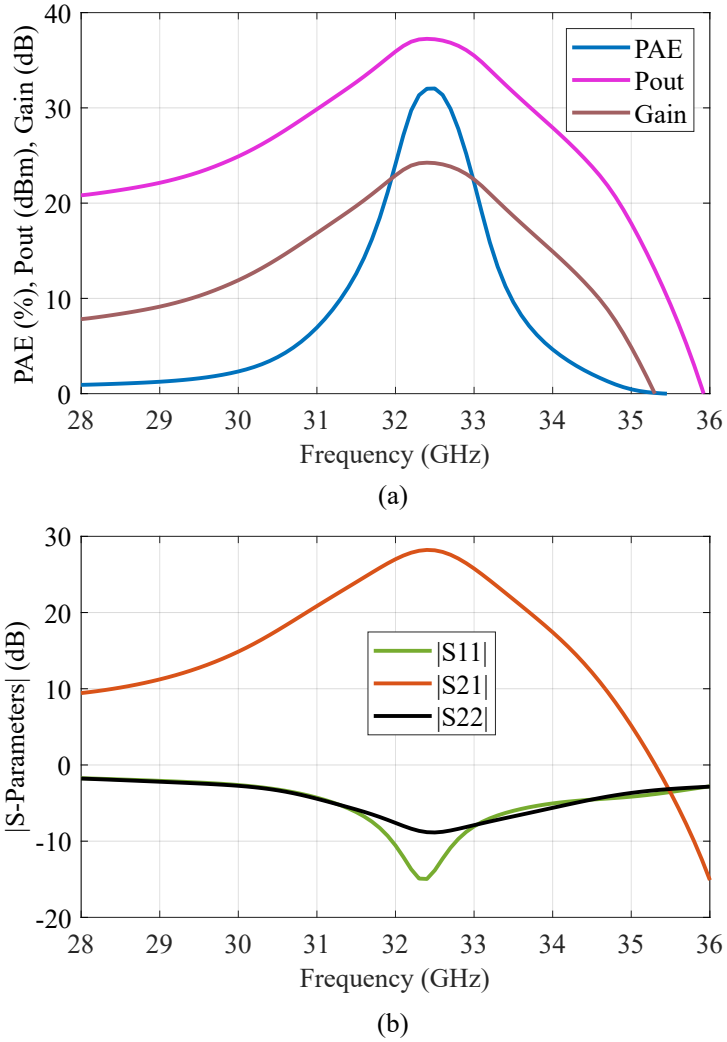


Figure 5.11: Simulated (a) large-signal performance with 13 dBm of drive power, and (b) small-signal performance over frequency for the second iteration of the power amplifier with ambient temperature set at 60° C.

5.5 Chapter Conclusions

This chapter presents two narrowband 3-W Ka-band power amplifiers designed using the WIN 120-nm GaN-on-SiC process in Cadence AWR. Measured results of the first design show a frequency shift of maximum performance from 32 GHz to 31.2 GHz with a saturated gain of 20 dB and PAE of 24.5%. Comparison to simulations show that in saturation, the PA is drawing more

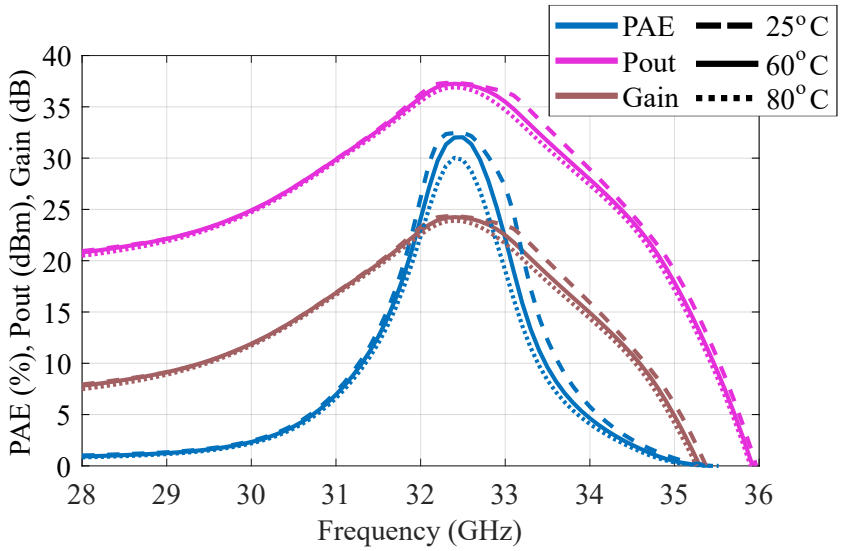


Figure 5.12: Simulated large signal performance over frequency for 13 dBm drive power for the redesign with device temperatures set to 25° C, 60° C and 80° C.

dc current than predicted, resulting in 6 pp lower maximum PAE. Simulations using the thermal model of the device indicate that heating is likely a significant contributor to the increased dc current draw and reduced efficiency.

A second iteration of the PA is designed using the same process with updated transistor models. The new transistor models are compared to the previous versions using the same EM simulated layout. Simulations show that the new transistor models partially account for the 800 MHz downward frequency shift seen in measurements. The new version is designed at a slightly higher frequency (32.3 GHz) and uses the built-in thermal models of the simulated devices to design for performance at higher temperatures. The updated design reaches the same saturated output power of 3 W with a saturated gain of 23 dB and a peak PAE of 32% with ambient device temperature set to 60° C. Under higher temperatures (80° C), the redesigned PA shows 3.5 pp higher PAE than simulations for the original design while also demonstrating 4 dB higher gain. Table 5.1 shows comparisons of the measured PA performance with the state of the art in Ka-band GaN MMIC power amplifiers with > 1 W output power. The simulated performance of the redesigned PA is

also included for comparison. The results dsicussed in this chapter are reported in [75].

Table 5.1: Ka-band PA Comparisons

Ref.	Freq. (GHz)	Process	VDD	PAE	Pout (dBm)	Gain (dB)
[76] *	35	200 nm GaN	28 V	41% *	37.7 *	25
[25]	31.5	200 nm GaN	28 V	36%	40	25
[73] *	28	150 nm GaN	28 V	25.9% *	46.2 *	30
[77]	30	100 GaN	13 V	30%	39	20
[78]	30	150 nm GaN	20 V	30%	40.4	28
[79] *	28	100 GaN	15 V	25% *	39.6 *	20
[80]	30	- GaN	24 V	25.5%	35.6	15
This Work	**31.2**	**120 nm GaN**	**28 V**	**24.9%**	**37**	**20**
Redesign	**32.3**	**120 nm GaN**	**28 V**	**32%**	**37**	**23**

* Measured in pulsed mode.

Chapter 6

Design and Simulation of Additional Ka-band GaN-on-SiC Power Amplifiers

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6.1 Introduction

With the PA designs using the WIN 120 nm GaN-on-SiC described in Ch. 5 as a baseline, three additional Ka-band power amplifiers are designed and simulated. The first is a 3-stage power amplifier designed using the Qorvo 150 nm Gan-on-SiC process. Because the Qorvo 150 nm process has a larger node size compared to the WIN process used in the previous chapter, this technology is chosen for a PA intended to provide higher output power (10 W) at the cost of reduced PAE. The final two PAs, one 2-stage and one 3-stage, use the HRL 40 nm T3L GaN-on-SiC process. The much smaller node size of this technology makes it well-suited for active circuits operating beyond Ka-band and into V-band and W-band. This also results in much higher gain at Ka-band compared to both the WIN and Qorvo processes, making the HRL process appropriate for PA designs focusing on higher gain and PAE at the expense of lower output power. Additionally, it is important to

note that the maximum drain voltage for the Qorvo process is 28 V while the maximum for the HRL T3L process is 12 V. All three PAs discussed in the chapter are designed and simulated using Cadence AWR and were taped out prior to the time of writing this thesis, but are still in fabrication as of September 2025.

In order to reach output power levels on the order of 10 W from a single MMIC at Ka-band, the output stages of each design in this chapter combine the power of eight devices. Accommodating twice the number of devices in the output stage within the same chip size, requires an alternative combining topology to the standard corporate combiner used to combine four devices in Ch. 5. The proposed type of combiner used for the designs discussed in this chapter is referred to as a bus-bar combiner [81]. Fig. 6.1 shows examples of 4 and 8-element bus-bar combiners integrated with transistors and stability networks. As the bus-bar is scaled from 4 to 8 elements, a second section is cascaded with the first as can be seen in Fig 6.1c and 6.1d. This cascading is done to maintain symmetry across all devices in the combiner. Fig 6.2a uses a heat map to highlight the current distribution of an 8-element bus-bar while Fig. 6.2b shows a magnified view of the $\hat{X}$ and $\hat{Y}$ current components. Due to the symmetry of the bus-bar, current does not flow between the drive ports assuming that they are driven in phase with equal power distribution. Some examples in the literature featuring similar combiners for multi-watt MMIC PAs include GaAs X-band MMIC PAs with output powers of about 5 W [82] [83]; a 10 W GaN X-band PA [84]; a 4 W GaAs K-band PA [85]; and a 1 W GaAs Ka-band PA [86].

The primary advantages of using bus-bar combiners are as follows.

(1) Bus-bar combiners are compact and allow combining of large numbers of devices in a much smaller footprint than a distributed transmission line combiner or Wilkinson splitter.

(2) Direct bus-bar connection between all devices in a given stage allows for dc biasing from either or both sides of the chip. This is especially useful for high dc currents in multi-watt power amplifiers.

(3) The short length (much less than a wavelength) of connections between devices helps to

eliminate odd-mode instabilities that can arrise in power-combined PA architectures.

In order to maximize the number of power-combined devices, and therefore power density in the output stage, bus-bars are used for each of the three designs discussed in this chapter.

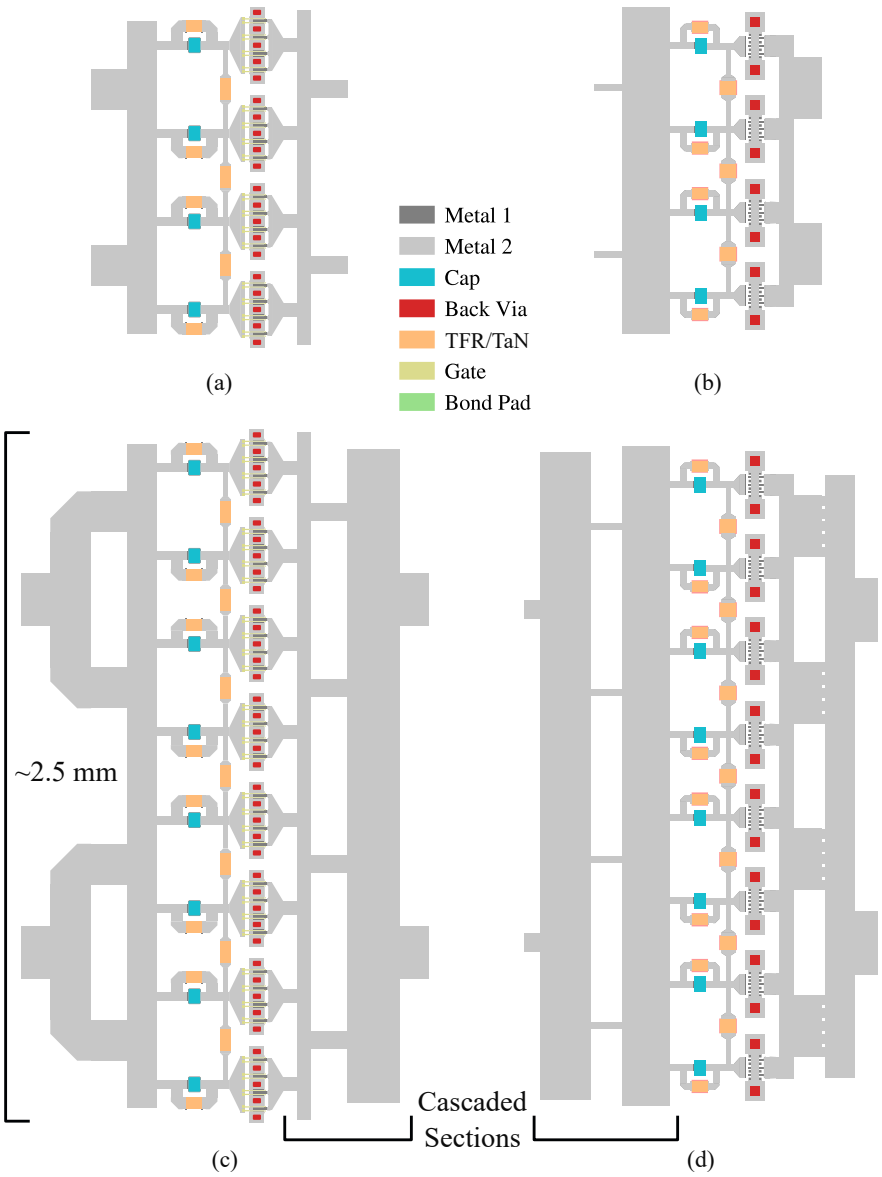


Figure 6.1: Layout of several different sized bus-bar combiners used for PAs discussed in this chapter. (a) and (b) show 4-element bus-bar combiners with integrated transistors and stability networks using the Qorvo and HRL processes respectively. (c) and (d) show corresponding scaled 8-element bus-bars. Both of the 8-element bus-bar structures are on the order of 2 mm tall and 1 mm wide.

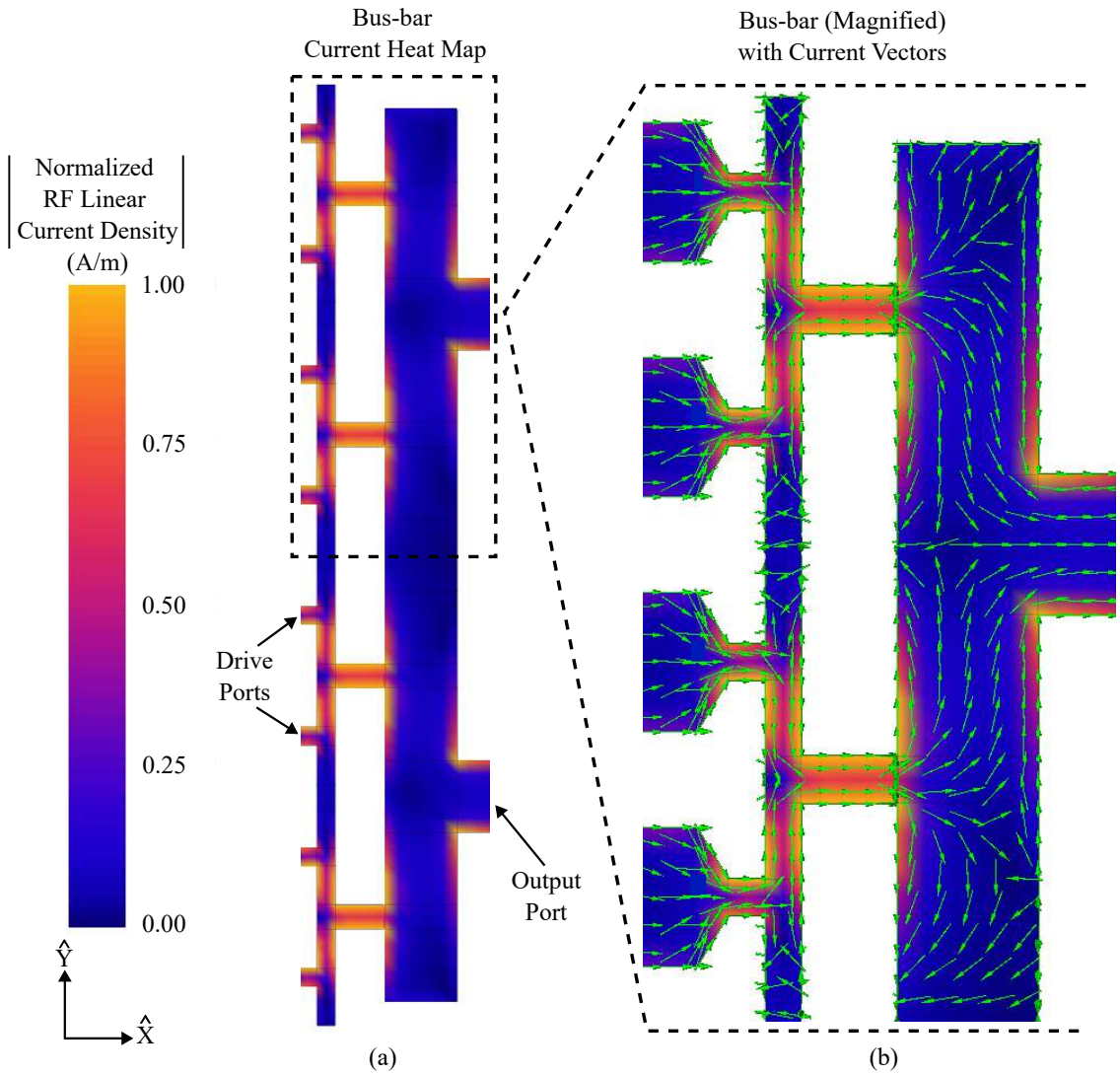


Figure 6.2: (a) Layout of bus-bar with overlaid heat map of normalized linear RF current density at 32 GHz. (b) Zoomed in section of bus-bar with vectors indicating the $\hat{X}$ and $\hat{Y}$ components of the RF current. Each drive port is is driven in phase with equal power.

6.2 3-Stage PA Designed Using the Qorvo 150 nm Process

The first PA uses the Qorvo 150 nm GaN-on-SiC process and consists of three stages with a 1:2.8:8 staging ratio. The staging ratio is realized using eight $8\times50\,\mu$m devices in the output stage, four $8\times35\,\mu$m devices in the second stage, and two $8\times25\,\mu$m devices in the first stage. $8\times50\,\mu$m is one of two validated device sizes for this process, the other being $10\times75\,\mu$m. Through load pull,

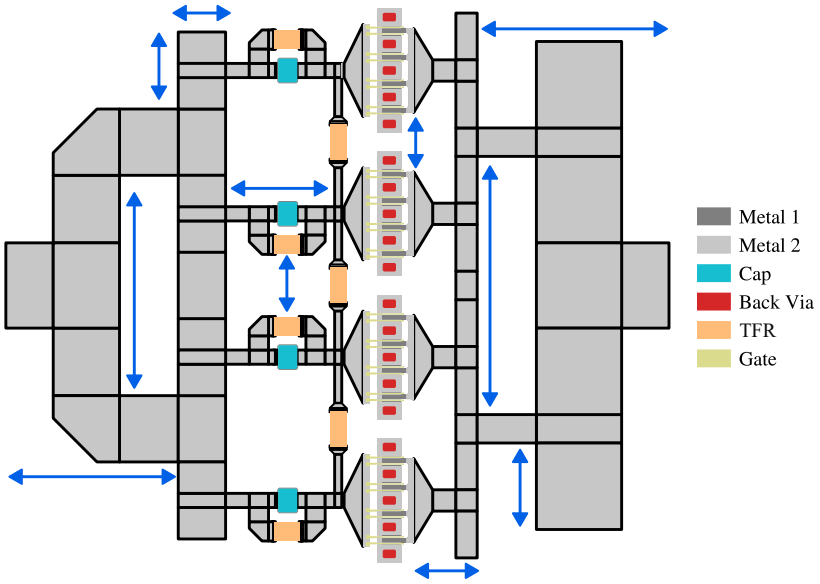


Figure 6.3: Zoomed-in portion of the 8-element bus-bar from Fig. 6.1c showing the level of parameterization. Each of the transmission line elements outlined in black, in addition to the resistors and capacitors, have adjustable widths and lengths. The blue arrows highlight some of the dimensions of the bus-bar that can be adjusted.

$8\times50\,\mu$m devices are ultimately chosen for the output stage as a good compromise between high output power and efficiency. Eight of the chosen devices are then integrated into the architecture shown in Fig. 6.1c. Many small lengths of transmission line are used to form the bus-bar, and are fully parameterized so that they can be adjusted for impedance matching. Additionally, each transistor is integrated with parallel RC high-pass filters and shunt resistors between devices for stability. The stability networks are also fully parameterized and can be adjusted throughout the design process. As illustrated by Fig. 6.3, the dimensions of each parameterized element are controlled using design equations, allowing the seamless adjustment of all bus-bar dimensions, including device spacing. The entire integrated bus-bar and stability structure can now be treated similarly to a single, large transistor. Analogous to the initial selection of device size, a range of permutations of the entire structure are load pulled to determine both the optimal bus-bar dimensions, and the required impedance of the output matching network.

The same design process is repeated for both the interstage and driver stage. Both device

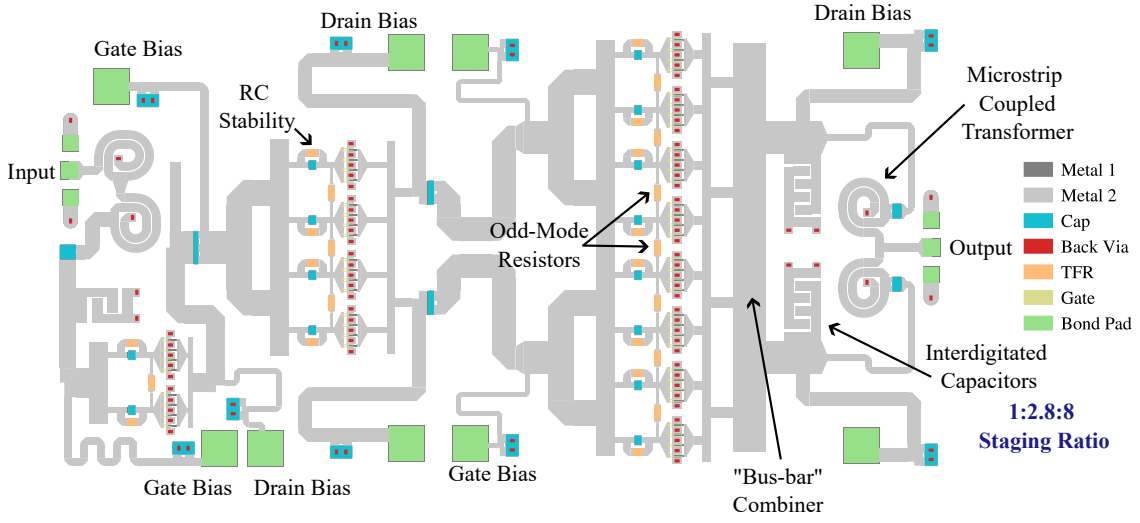


Figure 6.4: Final layout of the 3-stage power combined PA designed using the Qorvo 150 nm GaN on SiC process. The device peripheries used in each stage are as follows: two $8\times25\,\mu$m devices in the first stage; four $8\times35\,\mu$m devices in the second stage; and eight $8\times50\,\mu$m devices in the final stage. The total design dimensions are 5 mm $\times$ 2.5 mm.

size and the number of devices for each of these stages are determined by the minimum drive power needed to saturate the output stage. A worst case of 1-2 dB of loss is assumed to occur in each interstage matching network and is factored into the gain budget for the first and second stage. Although this is an overestimate of the loss in each matching network, it also acts as a buffer for gain reduction at higher device temperatures. Fig. 6.4 shows the finalized layout of the 3-stage PA. As shown, bus-bar combiners are implemented at both the gate-side and drain-side of each stage, allowing for compact combining of each device. In order to accurately capture the response of each bus-bar, EM simulations using either full-wave 3D solvers or 2.5D solvers are required. In this case, the AWR's Axiem 2.5D method of moments solver is used. Because bus-bars consist of short, wide, and closely spaced segments of microstrip, the transmission line elements used in the circuit model do not completely predict coupling and parasitics that influence the flow of RF current through the structure. For this reason, all bus-bars are EM-simulated before designing any supplementary matching networks.

Another important feature of the input and output matching networks shown in the figure are

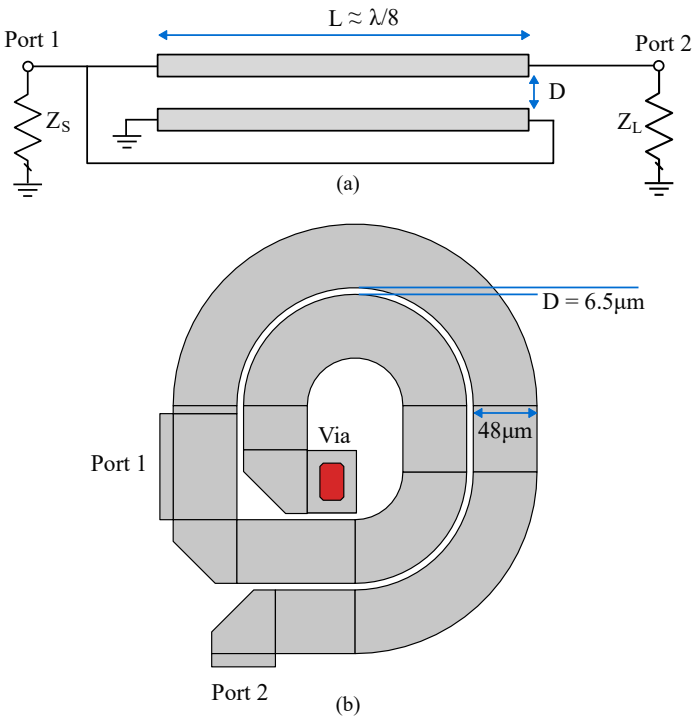


Figure 6.5: (a) Schematic of $\lambda/8$ coupled line transformer. (b) Layout of realized transformer using two coupled microstrip lines with a backside grounding via.

the pairs of coupled-line transformers. Each of these transformers consists of two, approximately $\lambda/8$ at 32 GHz, coupled microstrip lines. As shown in the schematic in Fig. 6.5a, one line directly connects Z_s to Z_L, while the other line is short-circuited at one end, and connected to Z_S at the other. Given a specific target impedance, Z_0, the circuit can function as a 4:1 transformer where $Z_S = Z_0/2$ and $Z_L = 2Z_0$ as detailed in [87]. In order to realize the schematic of the coupled-line transformer, the microstrip lines are coiled in on themselves, as shown in Fig 6.5b, with a backside via serving as the ground connection. The transformers present a compact method for matching the low output impedances presented by many devices combined in parallel, which is relevant for bus-bar implementation.

One transformer is connected to each of the two output branches of the bus-bar combiner. The shunt interdigitated capacitors and series transmission lines transform the complex impedance presented by each output branch (~ 4+j30 Ω) to approximately 25 Ω. Interdigitated capacitors are

used here due to their resilience to process variation and the need for low ($\leq 1\,\text{pF}$) capacitance values. From there, the outputs of both 4:1 transformers present $100\,\Omega$ which are then reactively combined through a T-junction to the $50\,\Omega$ output. Additionally, a similar pair of transformers are cascaded in series as part of the input matching network. Like the PAs discussed in Ch. 5, stability criteria are repeatedly checked throughout the design process. Parallel RC high-pass filters at the gates of each device are realized with $60\,\Omega$ and 0.5 pF resistors and capacitors respectively and $30\,\Omega$ odd-mode resistors are connected between the gates of the transistors in each stage.

Fig. 6.6a shows the simulated small-signal S-parameters over frequency of the 3-stage amplifier with all passive elements EM simulated, demonstrating an unsaturated gain of 33 dB at 32 GHz. The large-signal performance over frequency is shown in Fig. 6.6b, demonstrating 40 dBm (10 W) of output power, 28% PAE, and 25 dB of saturated gain at 32 GHz. In addition to characterization over frequency, Fig. 6.7 shows the simulated PAE, gain, and output power over input power. Two of the Qorvo PAs discussed in this section were taped out side-by-side on a single $5\,\text{mm} \times 5\,\text{mm}$ chip, meaning that close to 20 W could be extracted from a single die with efficient off-chip power combining and substantial heat-sinking.

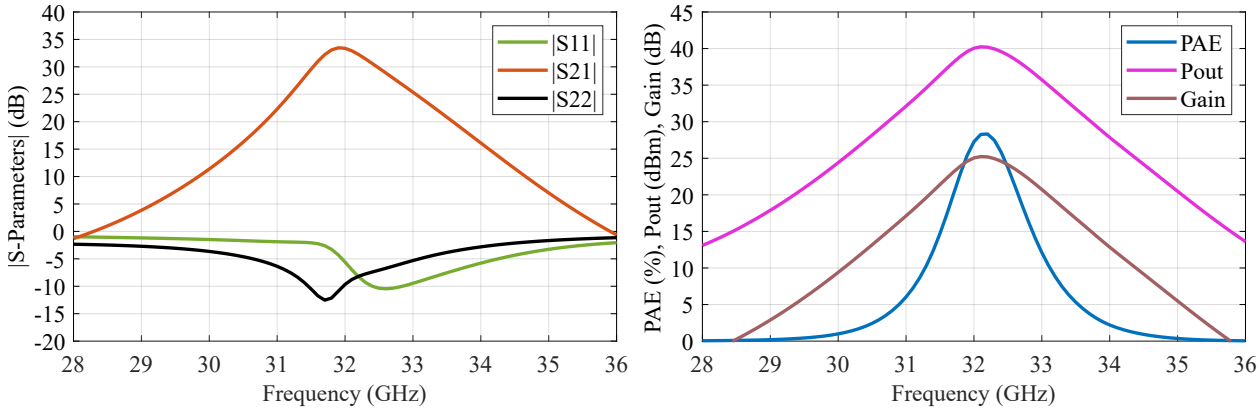


Figure 6.6: (a) Simulated small signal S-parameters over frequency for the 3-stage Qorvo PA showing small signal gain of 33 dB at 32 GHz. (b) Simulated large signal performance of the same PA, showing 40 dBm of output power, 28% PAE, and 25 dB of saturated gain at 32 GHz.

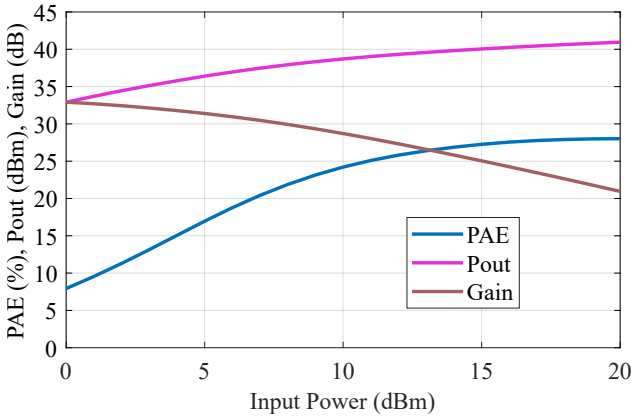
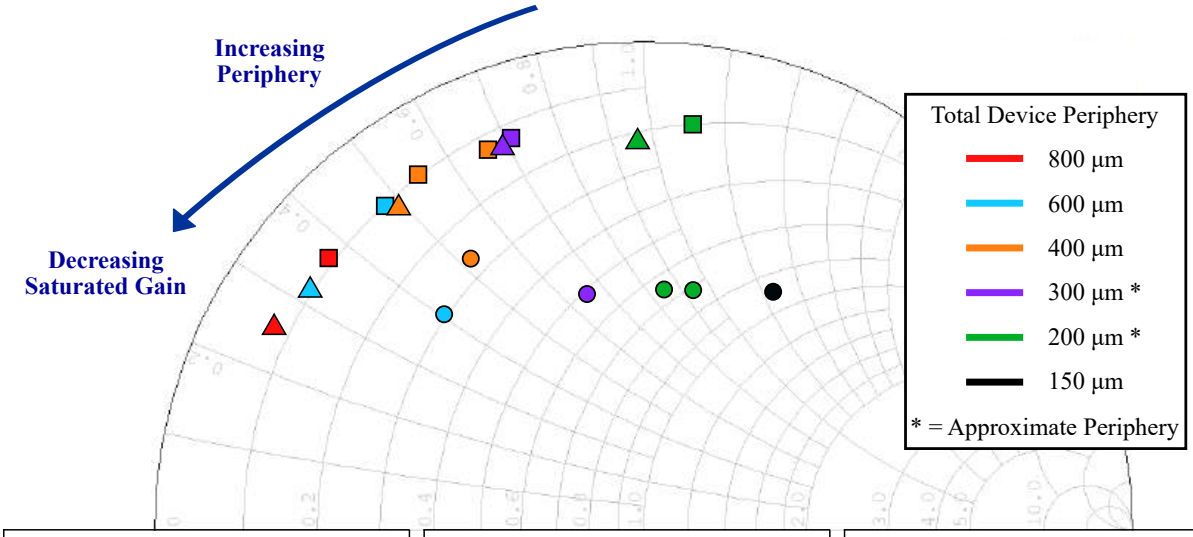


Figure 6.7: Simulated drive-up curves of the 3-stage Qorvo PA at 32 GHz. The bias point is the same as in Fig. 6.6.

6.3 2-Stage and 3-Stage PAs Designed Using the HRL 40 nm Process

The HRL 40 nm T3L GaN-on-SiC has a process node less than 1/3 of that for the Qorvo process discussed earlier in this chapter, making it well-suited for much higher frequency operation (V and W-band). Furthermore, the validated device sizes in the HRL process have smaller periphery than the Qorvo devices. Both of these factors influence the designs using this technology, and they are aimed towards higher gain and higher PAE at lower output powers than the WIN and Qorvo designs discussed previously. To further illustrate this point, Fig. 6.8 shows a 50 Ω Smith chart with load pull data at 32 GHz from many different device sizes, and across multiple GaN-on-SiC technologies, including WIN, Qorvo, and HRL. Each of the devices in the figure are biased in class AB with quiescent currents of 150 mA/mm. As shown by the figure, the HRL devices, indicated by the circle-shaped markers, have significantly larger real components in their output impedances than the WIN and Qorvo devices. The smaller gate length of these devices results in reduced output capacitance and a higher maximum operating frequency for the process. Although the output power levels are lower for HRL devices of similar periphery compared to devices using the other two technologies, PAE is consistently 5 pp higher. Additionally, the lower output capacitance of the HRL devices imply more easily realizable impedance matching networks and the potential



□ WIN 120nm □		
Periphery	PAE	Output Power
4 x 50 µm	44%	29.3 dBm
6 x 50 µm	43%	31.2 dBm
4 x 100 µm	50%	31.7 dBm
8 x 50 µm	45%	32.6 dBm
6 x 100 µm	49%	33.5 dBm
8 x 100 µm	42%	34.6 dBm

△ Qorvo 150nm △		
Periphery	PAE	Output Power
8 x 25 µm	48%	31.1 dBm
8 x 35 µm	48%	32.4 dBm
8 x 50 µm	47%	33.7 dBm
8 x 75 µm	42%	34.7 dBm
8 x 100 µm	36%	35.8 dBm

○ HRL 40nm ○		
Periphery	PAE	Output Power
4 x 37.5 µm	55%	26.3 dBm
4 x 50 µm	55%	27.8 dBm
6 x 37.5 µm	55%	28.1 dBm
6 x 50 µm	55%	29.3 dBm
4 x 100 µm	54%	30.5 dBm
6 x 100 µm	54%	32.6 dBm

Figure 6.8: Simulated load pull data for different device peripheries and different technologies on a 50 Ω Smith chart. Each point is the impedance that results in maximum output power when each device is driven at its most efficient compression point. Every device is biased in class AB with 150 mA/mm quiescent current. A table of device size and performance for all three technologies is also included.

for harmonic manipulation.

In this chapter, two different power amplifiers using the HRL process are discussed, one being a 2-stage design, and the other a 3-stage design. The two-stage PA is designed and simulated first, and the 3-stage PA is designed later by modifying and extending the already existing 2-stage version. This choice was made primarily due to chip size restrictions. The initial design was given a 3 mm × 3 mm reticle space and therefore did not have sufficient room for a 3-stage version of the PA. However, a subsequent run with a 5 mm × 3 mm reticle, affording enough space for the 3-stage version.

6.3.1 Design and Simulation of 2-Stage PA

Similar to the Qorvo and WIN designs discussed previously, design begins with the output stage and the selection of device periphery between two different validated sizes: $4\times37.5\,\mu$m and $6\times37.5\,\mu$m. As shown by the load pull comparison table in Fig. 6.8, the maximum PAE is the same for both device sizes, but the output power is about 2 dB higher for the $6\times37.5\,\mu$m device. Both the 6-finger and 4-finger models are scalable, and load pull for larger peripheries show higher output power without significant tradeoff in PAE. However, the validated $6\times37.5\,\mu$m device is ultimately chosen for higher confidence in the model because the T3L process is relatively new.

The chosen devices for the output stage are then integrated into the combined stability network bus-bar shown in Fig. 6.1d. From there, the design process follows that of the Qorvo design very closely, only with a focus on higher PAE and gain. However, higher gain at W-band, V-band, and importantly Ka-band also implies a higher gain at all lower frequencies as well. This means that extra care must be taken to ensure stability, both in and out-of-band, throughout the design process. Fig. 6.9a shows the layout of part of the driver stage and highlights key stability components. Notably, this design includes $25\,\Omega$ series resistors on the gate bias lines, $90\,\Omega$ odd-mode resistors, and more aggressive parallel RC stability networks using $100\,\Omega$ resistors and 0.15 pF capacitors.

Figure 6.9b plots $|S_{21}|$ over frequency for both the Qorvo and HRL parallel RC networks, highlighting the increased attenuation in the HRL RC networks in and below the band of operation. Once the design is finalized and all passive components are fully EM-simulated, stability is checked again using the same methods discussed in Ch. 5 for the WIN designs. Fig. 6.9c shows one linear and one nonlinear Nyquist polar plot, demonstrating that the unstable regions, marked by red dots, are not encircled. These plots only show one example of stability under specific drive, bias, and loading conditions; in practice, many more iterations are needed to establish confidence in a stable design.

Figure 6.10 shows the full layout of the finalized 2-stage design. As seen in the layout, a pair

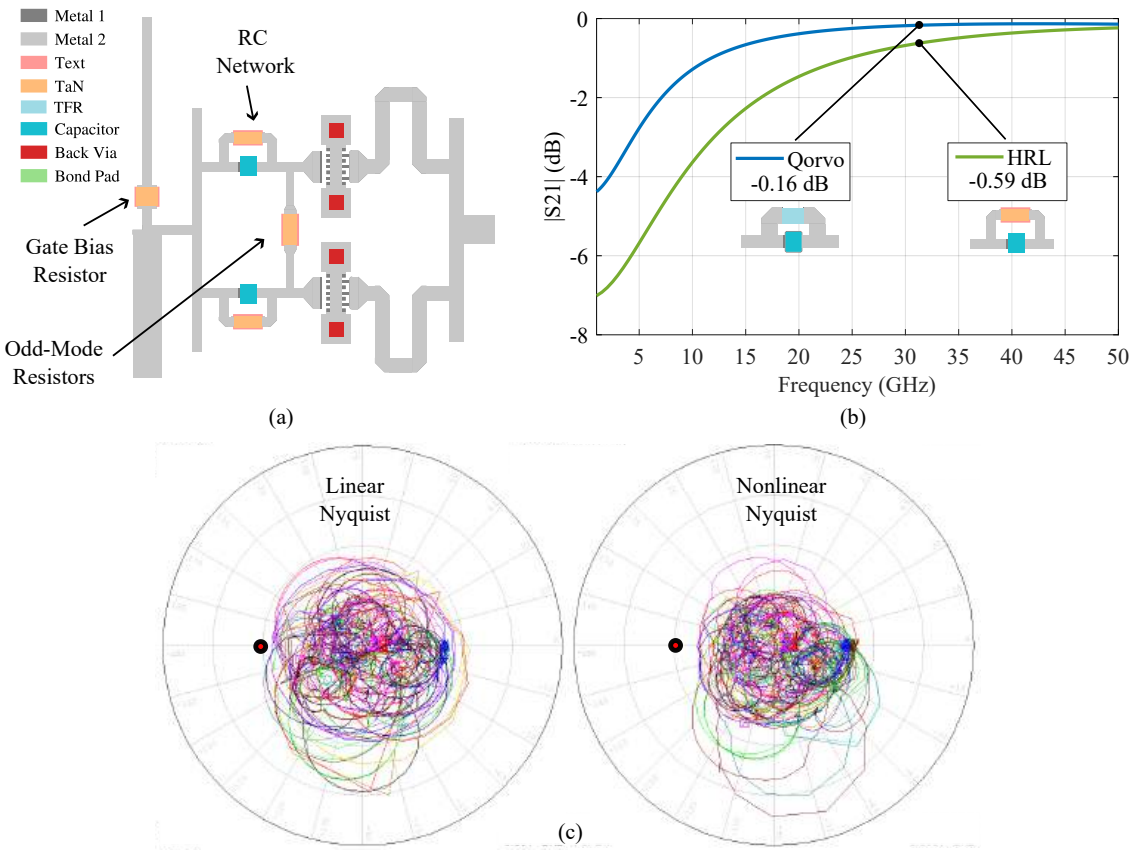


Figure 6.9: (a) Layout of a section of the driver stage of the HRL 2-stage PA showing the integrated stability networks. (b) Comparison of $|S_{21}|$ between fully EM-simulated parallel RC networks for both used in the Qorvo and HRL designs. (c) Examples of both a linear and nonlinear Nyquist stability plot over frequency for the fully EM-simulated 2-stage PA.

of shunt capacitor output matching networks, similar to the ones used in the Qorvo design, are implemented after the bus-bar. However, due to the more manageable output impedances of the devices used in this design, the coupled-line transformers are not needed. Notably, the output stage has two sets of bias lines for both the gate and the drain while the driver stage only has one of each. This is done primarily to maintain symmetry in the bus-bar combiner, but the direct connection between devices allows biasing from either side.

Fig. 6.11a shows the fully EM-simulated small-signal S-parameters over frequency, demonstrating an unsaturated gain of 20 dB at 32 GHz. Fig. 6.11b shows simulated large signal performance over frequency, demonstrating 35 dBm (3 W) of output power, 41% PAE, and 17 dB of

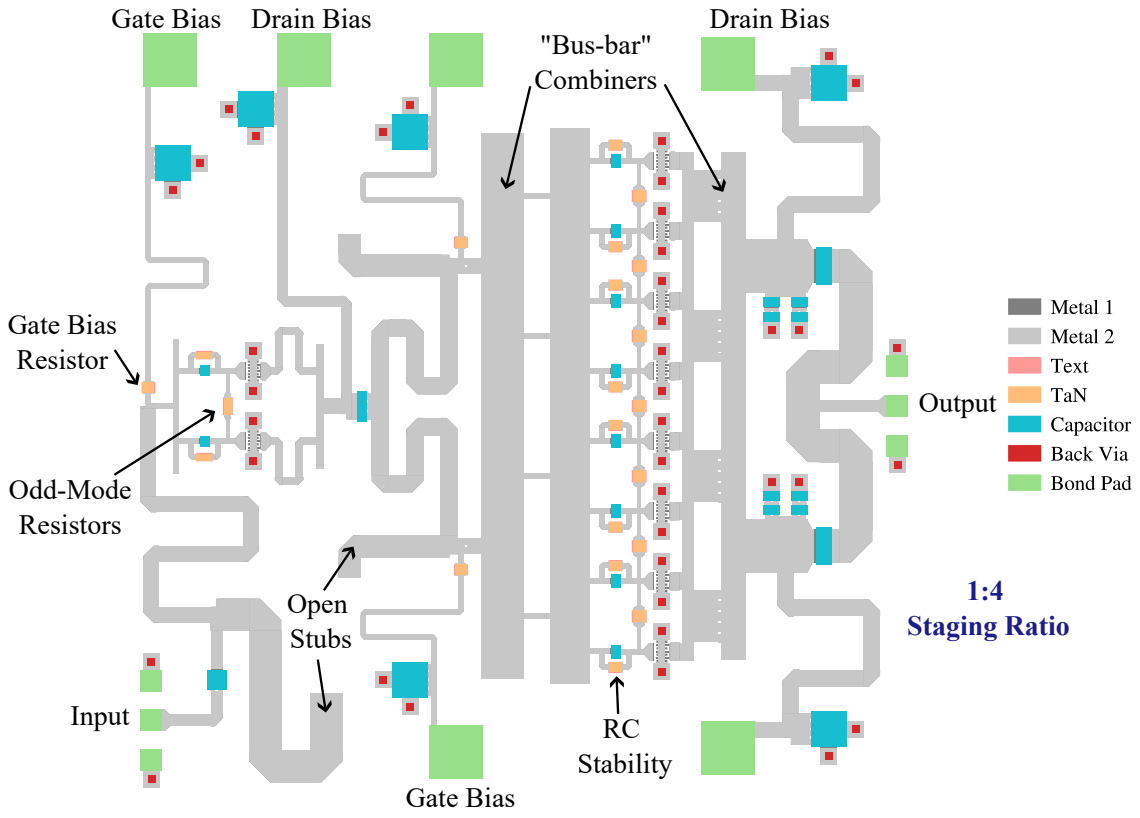


Figure 6.10: Final layout of the 2-stage power combined PA designed using the HRL 40 nm GaN on SiC process. The device peripheries used in each stage are as follows: two $6\times37.5\,\mu$m devices in the first stage; and eight $6\times37.5\,\mu$m devices in the final stage. The total design dimensions are $3\,\text{mm}\times3\,\text{mm}$.

saturated gain at 32 GHz. Drive-up curves are given in Fig. 6.12 which shows the simulated PAE, gain, and output power plotted over input power.

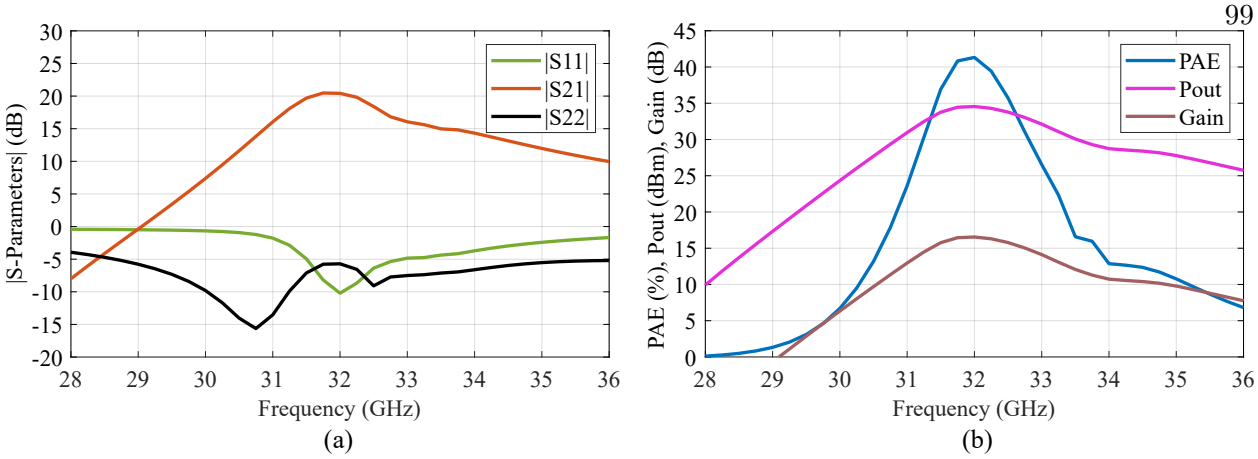


Figure 6.11: (a) Simulated small signal S-parameters over frequency for the 2-stage PA using the HRL process showing small signal gain of 20 dB at 32 GHz. (b) Simulated large signal performance of the same PA, showing 35 dBm of output power, 41% PAE, and 17 dB of saturated gain at 32 GHz.

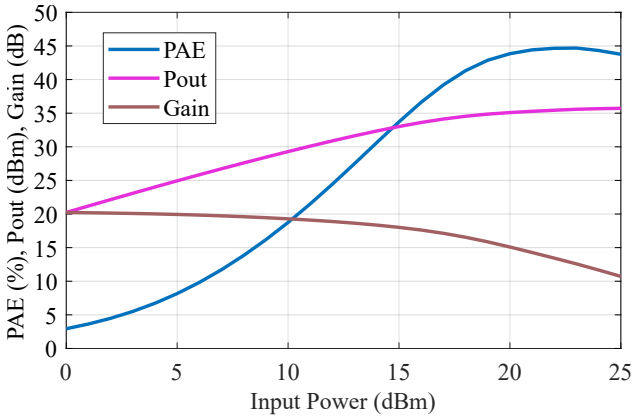


Figure 6.12: Simulated drive-up curves of the 2-stage PA using the HRL process at 32 GHz. The bias point is the same as in Fig. 6.11.

6.3.2 Design and Simulation of 3-Stage PA

The final power amplifier discussed in this chapter is a 3-stage design that modifies and builds on the 2-stage version detailed in the previous subsection. With an extra 2 mm of chip length to work with, the aim of this design is to maintain the PAE and output power of the 2-stage version while achieving a saturated gain of ∼10 dB higher by adding an additional driver stage. Fig 6.13a shows the finalized layout of the 3-stage PA. The staging ratio is 1:2:8 with $6\times37.5\,\mu$m used in each

stage. Comparing Fig 6.13a with Fig 6.10, it can be seen that the output stage of the amplifier remains largely unchanged. However, the interstage biasing and matching network between the output stage and second stage is changed significantly, as seen in Fig 6.13b.

With extra design space available, the interstage network is lengthened by about 200 μm; most notably the meandered lines connecting to the output bus-bar. Furthermore, these lines are not combined together before the dc-isolation capacitor as they were in the previous design. Instead, each line feeds directly into one of the two devices in the driver stage and has its own dc-isolation capacitor and drain bias line. Finally, a short bus-bar connection is implemented between the two devices in the driver stage, providing a direct path between them to aid in the suppression of odd-mode oscillations and to allow dc biasing from either side of the chip. In addition to providing a better interstage match, these changes improve spatial symmetry in the matching network and eliminate any asymmetric coupling that could occur. An example of potential asymmetric coupling is the region highlighted by the dashed, red box in Fig 6.13b. Finally, the widths and lengths of the open stubs are adjusted in accordance with the other aforementioned changes.

To add an additional stage, the input match of the original design is replaced by a second interstage network consisting of an open-stub match to a single 6×37.5 μm device. The input utilizes a similar open-stub matching network to 50 Ω. Single stub matching is well suited here due to its compactness and the narrow-band nature of the power amplifier. One final change to the design is the inclusion of three grounded bond pads sprinkled throughout the layout. These pads do not contribute anything in simulation; instead, they provide a means of bonding to the ground plane of an off-chip package. Doing this can improve grounding of the chip and potentially interrupt any feedback loops through the ground that could cause instability. Similarly to the 2-stage version, the three dc bias pads along the bottom of the chip are redundant and used primarily to provide symmetric loading to the power amplifier. Although this means the amplifier can be biased from the top pads alone, the additional drain lines in the second driver and output stages are helpful in distributing high dc currents.

Fig. 6.14a shows the simulated small-signal S-parameters over frequency of the full 3-stage

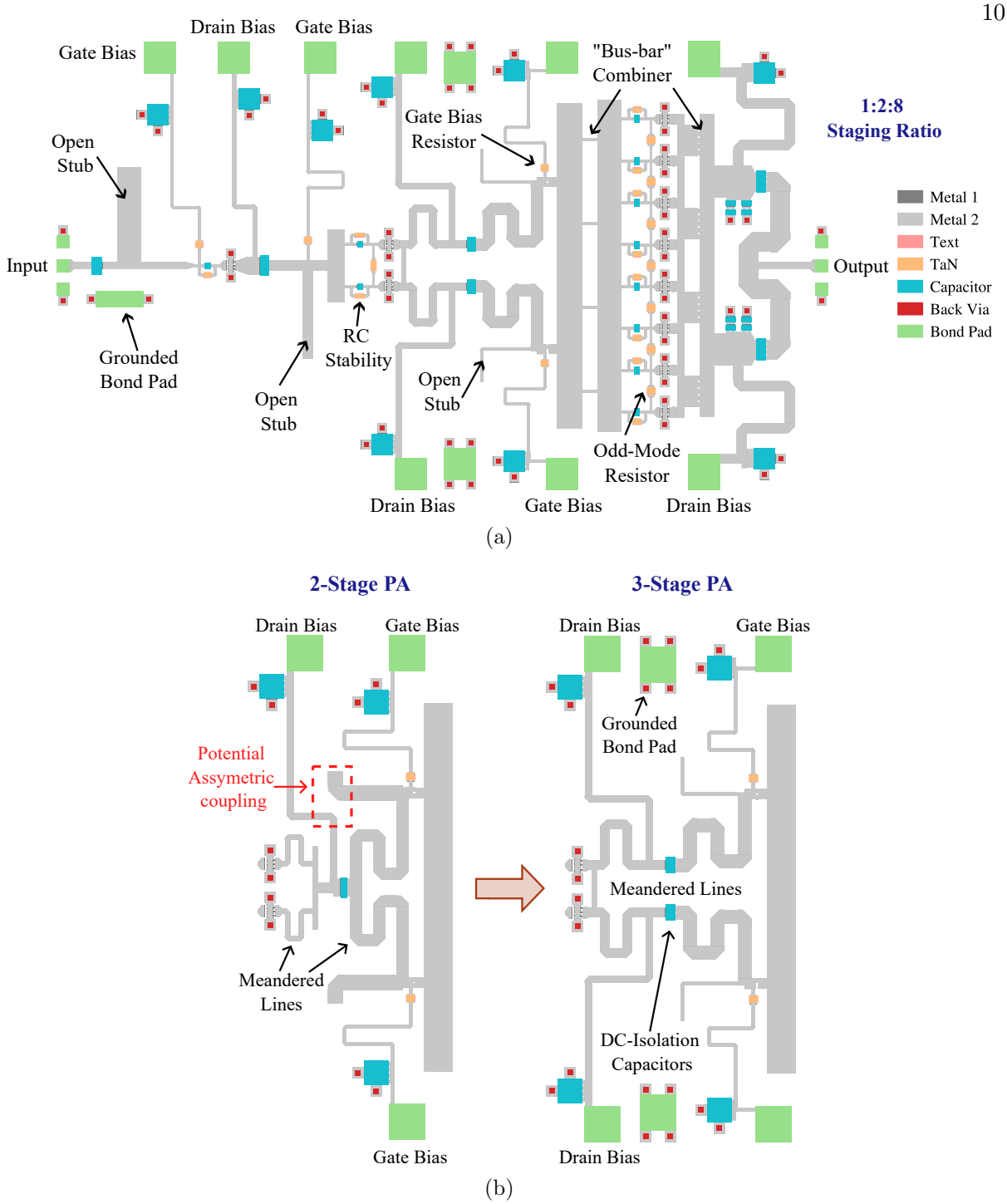


Figure 6.13: (a) Final layout of the 3-stage power combined PA designed using the HRL 40 nm GaN on SiC. The devices used peripheries of each stage are as follows: one $6\times37.5\,\mu$m devices in the first stage; two $6\times37.5\,\mu$m devices in the second stage; and eight $6\times37.5\,\mu$m devices in the final stage. The total design dimensions are $5\,\text{mm}\times3\,\text{mm}$. (b) Layouts of the interstage matching network connecting to the output stage for both the 2 and 3-stage HRL power amplifiers.

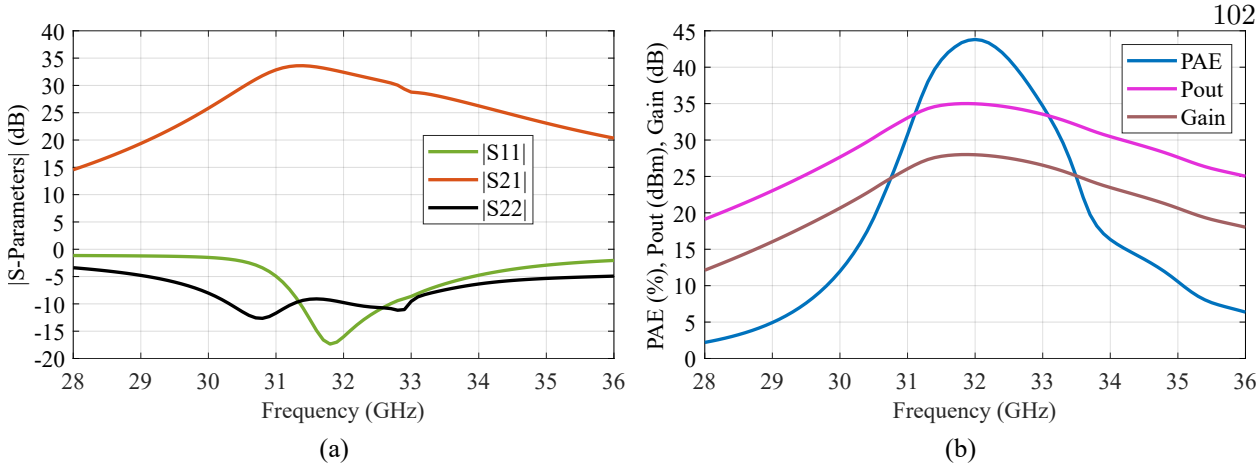


Figure 6.14: (a) Simulated small signal S-parameters over frequency for the 3-stage PA using the HRL process showing small signal gain of 33 dB at 32 GHz. (b) Simulated large signal performance of the same PA, showing 35 dBm of output power, 44% PAE, and 28 dB of saturated gain at 32 GHz.

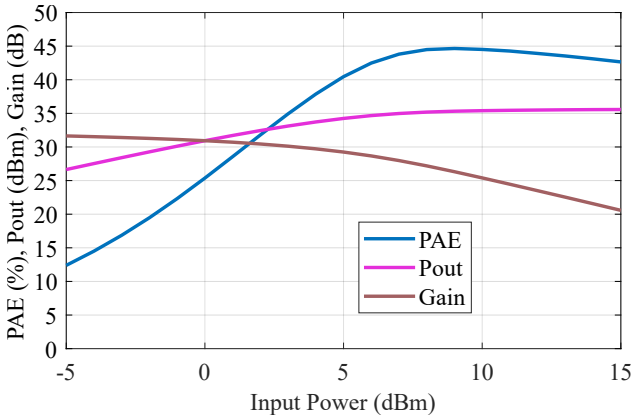


Figure 6.15: Simulated drive-up curves of the 3-stage PA using the HRL process at 32 GHz. The bias point is the same as in Fig. 6.14.

amplifier, demonstrating an unsaturated gain of 33 dB at 32 GHz. This is more than a 10 dB increase in gain compared with the original design. Additionally, the small signal input and output return loss is improved significantly from 10 dB to 15 dB and 5 dB to 10 dB, respectively. Simulated large signal performance over frequency is plotted in Fig. 6.14b, demonstrating 35 dBm of output power, 44% PAE, and 28 dB of saturated gain at 32 GHz. The updated 3-stage design maintains the same 3 W output power as the original design while achieving 3 pp higher PAE and 11 dB higher saturated gain. Drive-up curves for PAE, output power, and gain over input power are plotted ing

Fig. 6.15. An important takeaway from this figure is that this design operates at peak large signal performance with a drive power of only 7 dB. This is 8-11 dB lower than the Qorvo and 2-stage HRL designs discussed earlier in this chapter and 6 10 dB less than original and redesigned WIN PAs discussed in Ch.5 respectively.

6.4 Chapter Conclusions

In conclusion, this chapter presents the design and simulation of three multi-watt, Ka-band power amplifiers. The first is a 3-stage, 10 W PA designed using the Qorvo 150 nm GaN-on-SiC process. This design is focused on high output power at the expense of lower PAE due to the larger gate length and high drain voltage (28 V) of this technology. Additionally, two instances of this design were taped out side-by-side on the same chip, potentially allowing for off-chip power combining to extract close to 20 W from a single chip. The HRL T3L 40 nm Gan-on-SiC process is used to design the remaining two power amplifiers. Due to the much smaller gate length and lower maximum drain voltage (12 V), designs using this process are focused toward high PAE and gain. One 2-stage and one 3-stage PA are designed and simulated, resulting in both producing 3 W of output power with over 40% PAE at 32 GHz. A summary of large-signal performance for each design at 32 GHz is given in Table 6.1. Each of the designs discussed in this chapter is competitive with the state of the art, as shown by Table 5.1 in Ch. 5.

Table 6.1: Large-Signal Results at 32 GHz

Process	Number of Stages	Drain Voltage	PAE	Output Power	Saturated Gain
Qorvo 150 nm	3	28	28%	40 dBm	25 dB
HRL 40 nm	2	12	41%	35 dBm	17 dB
HRL 40 nm	3	12	44%	35 dBm	28 dB

Furthermore, all three designs discussed in this chapter make use of one or more bus-bars to combine multiple devices together within a compact structure. The output stage of each PA

is designed using a technique in which all devices are combined within a bus-bar integrated with stability networks as shown by Fig 6.1. The entire structure is fully parameterized and treated similarly to a single, large device for the purposes of load pull. In this way, the bus-bar structure is treated as a kind of pre-match which can be adjusted as needed and potentially simplify the design of the remaining output matching network. There is also the added benefit of the short and direct segments of connecting transmission line between devices in the bus-bar combiner. These segments help to simplify dc-biasing and can aid in the suppression of odd-mode oscillations. Although bus-bar combiners are not proposed first here, their demonstration in high-power GaN PAs at Ka-band and above has not been shown. The work discussed in this chapter is planned to be published in the IEEE TMTT journal after the die are delivered and measured.

Chapter 7

Conclusions and Future Work

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7.1 Thesis Summary

The focus of this thesis is to address individual components that are critical to the overall efficiency of a wireless power beaming system by introducing state-of-the-art and experimental technologies, materials, and design techniques.

Chapters 2 and 3 focus on the receiving end of a WPT system, detailing design and measurement of a 10 GHz rectenna array. In Chapter 2, the design, fabrication methodology, and characterization for a rugged, low-cost, and flexible 10 GHz rectennna subarray is presented. The subarray is designed using unconventional microwave materials including low-density packing foam, expanded PTFE foam, copper fabric, and metalized polyimide substrates. Multiple initial subarray designs are discussed, with the final design consisting of four combined patch antenna elements and

a single differentially fed Schottky diode. Tests of the initial fabricated iterations of the subarray demonstrate a maximum conversion efficiency of 35% at 10 GHz and a conversion efficiency above 32% over a dynamic range of 7.5 dB. In Chapter 3, the unit subarrays described in Chapter 2 are scaled up to 5×5, 2×2, 15×15, and 25×25 arrays with up to 2500 antenna elements and 625 rectifier diodes. The scaled arrays are characterized for conversion efficiency at 10 GHz and for different dc load configurations. The peak measured efficiency is 62% at 10.2 GHz for a 2×2 array of patch unit subarrays (16 antennas and 4 rectifiers). Additionally, a dynamic range of 8.5/,dB is demonstrated for conversion efficiencies above 40%. The peak output power of 0.84 W was measured for the largest (25×25) patch array. The arrays were also tested after being exposed to outdoor conditions, including rain, and transient voltage suppression diode were integrated along dc lines to protect against ESD events.

Chapters 4, 5, and 6 focus primarily on the transmit side of a WPT system by presenting interconnects and test structures using novel packaging process and multi-watt MMIC PAs designed using state-of-the-art GaN-on-SiC technologies. In Chapter 4, a variety of broadband, low-loss interconnects designed on an experimental packaging process, intended for heterogeneous integration, are presented. Design, simulation, and measurement of numerous structures including interconnects, couplers, and filters are discussed in detail. Interconnects and couplers discussed in this chapter are focused on low-loss GCPW transitions designed for integration with MMIC circuits such as the Ka-band GaN-on-SiC power amplifiers discussed in Chapters 5 and 6. Simulated results for interconnects up to 110 GHz are also briefly discussed. The demonstrated circuits show a path to high-density low-loss passives and interconnects at mm-wave frequencies. Chapter 5 presents two narrow-band 3-W Ka-band power amplifiers designed using the WIN 120-nm GaN-on-SiC process in Cadence AWR. Measured results of the first design show a frequency shift of maximum performance from 32 GHz to 31.2 GHz with a saturated gain of 20 dB and PAE of 24.5%. A second iteration of the PA is designed using the same process with updated transistor models. The new iteration is designed at a slightly higher frequency (32.3 GHz) and uses the built-in thermal models of the simulated devices to design for performance at higher temperatures. The updated design

reaches the same saturated output power of 3 W with a saturated gain of 23 dB and a peak PAE of 32% with ambient device temperature set to 60° C. Finally, Chapter 6 presents the design and simulation of three multi-watt, Ka-band power amplifiers using two different GaN-on-SiC technologies with different process nodes. The first is a 3-stage, 10 W PA designed using the Qorvo QGaN15 150 nm process, and is focused on high CW output power. Two instances of this design were taped out side-by-side on the same chip, potentially allowing for off-chip power combining. The HRL T3L 40 nm process is used to design the remaining two power amplifiers. One 2-stage and one 3-stage PA are designed and simulated, resulting in both producing 3 W of output power with over 40% PAE at 32 GHz. Additionally, all three designs use bus-bars to combine multiple devices together within a compact structure. The output stage of each PA is designed using a technique in which all devices are combined within a fully parameterized bus-bar structure integrated with stability networks and treated similarly to a single large device.

7.2 Future Work

There are multiple extensions to improve the designs detailed in this thesis. Some of this work is already ongoing, but requires substantial manufacturing time and additional measurements for previously unfabricated designs. These extensions are discussed in greater detail in the following subsections.

7.2.1 10 GHz Rectenna Improvement

As mentioned in Chapter 3, dc combining schemes have a significant impact on the overall conversion efficiency of the scaled rectenna arrays. In general, using a combination of series and parallel connections between unit subarrays is shown to result in higher conversion efficiencies than purely parallel connections. For these tests, external series connections had to be introduced in the form of jumper wires. Relying on external dc connections between unit subarrays not only complicates and lengthens fabrication, but also compromises the flexibility and durability of the arrays. However, a very simple solution is given for a 2×2 array in Fig. 3.8 in Chapter 3 by

introducing vertical copper traces connecting between the dc output lines between each subarray. This technique is easily extended to much larger array sizes as shown by the simulated HFSS model in Fig. 7.1.

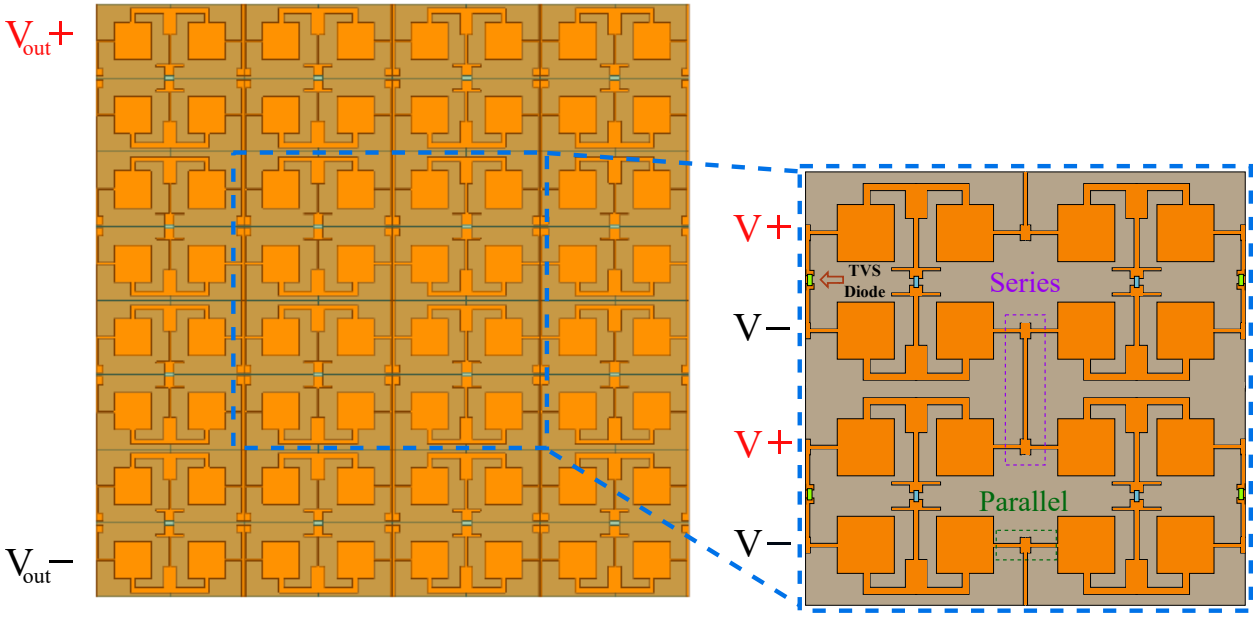


Figure 7.1: Layout of a 4×4 array with built-in parallel and series dc connections, demonstrating ease of scaling to larger array sizes.

By using the connection scheme shown in the figure, there will be an equal number of series and parallel connections if a square array is assumed. An equal number of subarrays combined in series and parallel implies that the optimal dc load is relatively independent of array size. Even if subarrays are arranged into different array shapes such as rectangles, triangles, or hexagons, this method of dc combining still results in far less variation of optimal load values over array size than purely parallel or series connections. Through full-wave simulation in ANSYS HFSS, it is determined that the addition of these series connections has no significant impact on the impedance or radiation pattern of the subarrays.

Additional work involving the 10 GHz rectenna arrays is the integration of TVS diodes with larger array sizes and further long-term weather testing with integrated TVS diodes. Furthermore, although it has ben demonstrated that the rectennas are not degraded by exposure to rain or

moisture in general, it is important to prevent the copper from oxidizing and water from pooling on the antennas during operation. One way to achieve both of these goals with minimal impact on the design and performance of the arrays, is to apply a thin layer of hydrophobic coating. This could be achieved through a simple aerosol spray after fabrication and would cause water to bead up and roll away if the rectenna is placed on a slight incline. Additionally, the thin barrier would protect any exposed metal from oxidation. Because the thickness of hydrophobic cpating typically being only a few tens of nanometers, it is expected to have little to no impact on array performance. However, further measurement is still required.

7.2.2 Ka-band Rectenna

Taking into consideration the five different high-power, high-efficiency Ka-band power amplifier designs discussed in Chapters 5 and 6, there is ample motivation for a Ka-band rectenna array to test a full WPT system. Although designed for a different frequency, there is no reason why the rectena design discussed in Chapters 2 and 3 could not be scaled up to 32 GHz. While this design would need to be matched to a higher frequency rectifier element and would likely use different materials, the differentially fed patch subaray would still be a simple and effective design for scaling to larger Ka-band arrays. Schottky diodes that operate well beyond Ka-band such as the MACOM MA4E1317 GaAs Schottky diode have already been demonstrated as efficient rectifying elements in the literature. Alternatively, there is the possibility of integrating a transistor-based rectifier based off of one of the several detailed power amplifier designs.

7.2.3 Ka-band Waveguide-Based Power Combiner

As a means to further connect the different aspects of this thesis together, a Ka-band waveguide combiner is designed for the purpose of power combining multiple MMIC power amplifiers discussed in Chapters 5 and 6. Scaling a WPT system to long distances often requires a large amount of RF power at the transmit end. Considering that getting more than 10 W CW out of a single chip at Ka-band is a significant challenge, low-loss power combining of multiple chips is the

best way to achieve output powers in the range of multiple tens, or hundreds, or even thousands of watts CW [88, 89]. Waveguides are a commonly used technology for off-chip power combining, particularly at millimeter-wave frequencies, due to their low loss and high power handling capabilities [79, 90, 91]. There are many different architectures of waveguide power combiners, one of which is a waveguide traveling-wave power combiner (WTWPC), which can generally be thought of as two waveguide sections short-circuited on opposite ends and in parallel with one another. Each waveguide section has slots cut along its side for microstrip probes to be inserted to couple power between the two waveguide sections, as seen in Fig. 7.2a. Metal irises inside the waveguide help to minimize any reflection due to the probes.

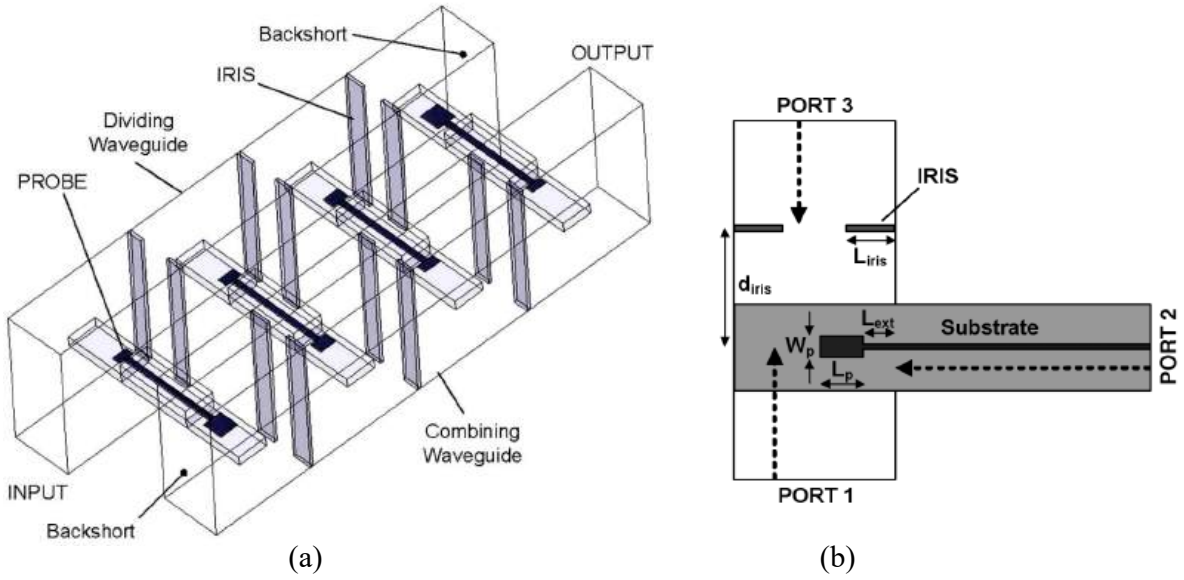


Figure 7.2: (a) Diagram of a WTWPC combiner showing both the input and output waveguides with PAs and microstrip probes in between. (b) 2D diagram of a 3-port section of the combiner with a microstip probe inserted into the waveguide and a metal iris used to minimize reflections. Here, port 1 is the input port, port 2 is the coupled port, and port 3 is the through port. Both diagrams are from [92].

Each probe is designed to couple a different amount of power depending on its position along the waveguide. Taking into account the diagram in Fig. 7.2b from [92], if the 3-port section is the i^{th} section counting from the shorted end towards the input, then the following power considerations would apply:

$$\frac{P_{reflect}}{P_T} = 0 \tag{7.1}$$

$$\frac{P_{coup}}{P_T} = \frac{1}{i} \tag{7.2}$$

$$\frac{P_{thru}}{P_T} = \frac{(i-1)}{i} \tag{7.3}$$

where P_T is the total input power, $P_{reflect}$ is the reflected power from the input port, P_{coup} is the power coupled to the microstrip probe, and P_{thru} is the power transmitted through the waveguide section and into the next. This means that a 4-section traveling wave combiner would couple $\frac{1}{4}$ of the input power into the first probe, $\frac{1}{3}$ of the remaining power into the second, $\frac{1}{2}$ of that remaining power into the third, and finally all remaining power into the fourth. If done in this way, all four microstrip probes will ideally deliver the same total power to each combined PA. In order to extract power from the PAs, the same structure used for the input divider is simply reversed and used as the output combiner as can be seen in Fig. 7.2a. Traveling waveguide combiners have a number of key advantages including low insertion loss, compact volume, ease of scaling to a desired number of elements, broad bandwidth, and overall simplicity of fabrication. Although broad bandwidth is not a necessary quality for WPT systems, the other advantages of WTWPCs are desirable.

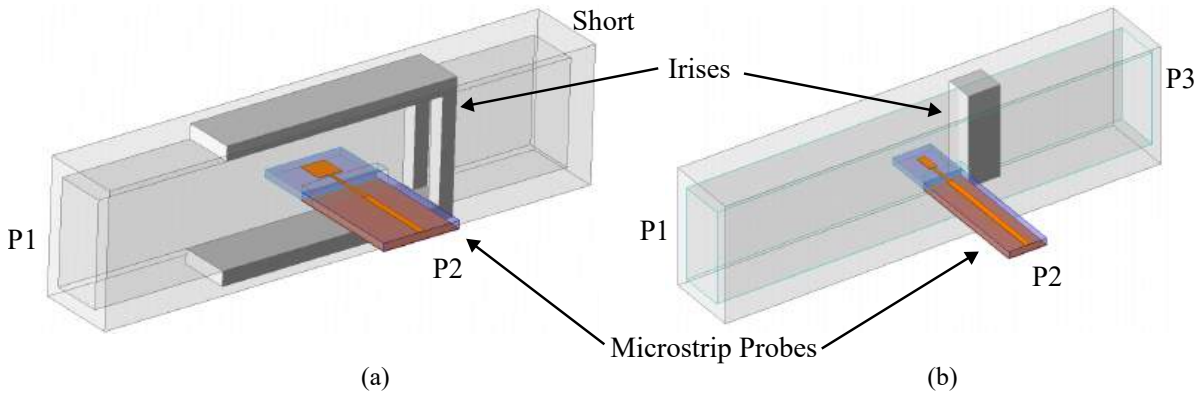


Figure 7.3: 3D models in made in ANSYS HFSS of (a) 2-port shorted section and (b) a 3-port section of the traveling wave combiner using a alumina microstrip probes and WR-28 waveguide dimensions.

The combiner is designed by first building a simplified model of a WR-28 section of waveguide in ANSYS HFSS. The inner dimensions of a WR-28 waveguide are approximately 7.1 mm × 3.6 mm and supports frequencies between 26.5 GHz and 40 GHz. Next, a simple microstrip probe is designed and parameterized using alumina substrate. Alumina is a commonly used substrate for waveguide transitions due to its low loss tangent at high frequencies (about 0.0002 for 96% alumina). From here, the alumina probe and waveguide section are integrated to form a 3-port structure as shown by Fig. 7.3a. Another 2-port version with one end of the waveguide shorted is also modeled and shown in Fig. 7.3b. The slot in which the micorstrip probe is inserted is kept narrow, both in height and width to minimize radiation loss in the structure. The normalized electric field magnitude is plotted for both the 2 and 3-port versions in Fig. 7.4, highlighting the difference in operation between the two structures. Using these two structures, each section of the traveling waveguide can be designed independently by taking into account equations 7.1, 7.2, 7.3, and then cascading them together as described in [93].

A distinguishing feature of the WTWPC discussed in this work, compared to others designed at Ka-band [**?**, 93, 94, 95], is that this design is not intended for split-block implementation. This means that the waveguide and irises will be a single solid component, with the microstrip probes designed to be slotted into into the back wall of the waveguide as shown in Fig. 7.5 using a secondary mechanical support slot. The reason for these design choices is that the waveguide components are intended to for plastic 3D printing and subsequent copper coating. Using additive manufacturing to 3D print and copper coat these waveguide components has several key benefits:

(1) 3D printing waveguide components is generally much less expensive than machining them out of solid aluminum or copper which is the standard procedure for split-block manufacturing.

(2) There is a significant reduction in weight and volume between the metalized plastic of the 3D printed structure vs the solid metal of most split-block implementations. This is particularly relevant for system integration. This is a very important advantage for any

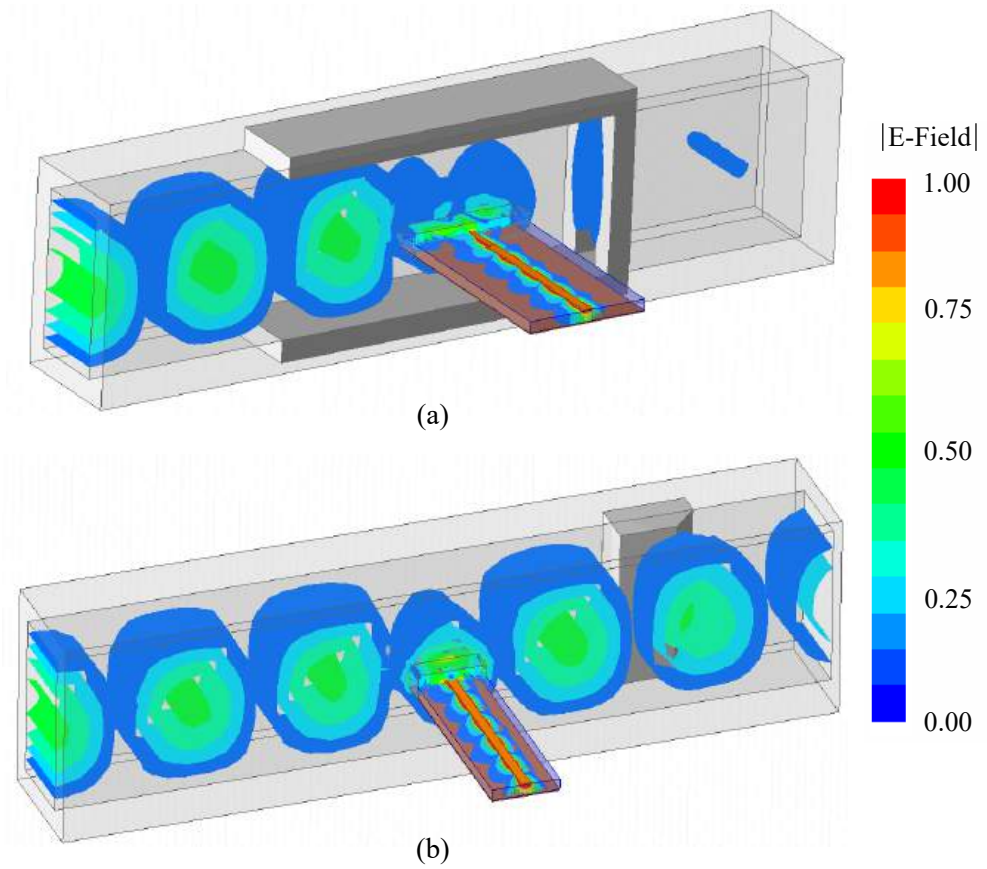


Figure 7.4: Normalized magnitude of the electric field shown inside the waveguide and microstrip probes for the (a) 2-port shorted section and (b) a 3-port section. The electric field magnitudes in the different portions of waveguide and probe clearly demonstrate the different coupling ratios between them.

application of wireless power beaming using drone or satellite mounted transmitters which have strict limitations regarding weight and volume.

(3) 3D printing of components allows for rapid prototyping and troubleshooting, making it quicker, easier, and cheaper to fabricate and test multiple iterations of a single design.

However, in order to 3D print any component, the model must meet certain criteria. For example, structures that hang over an empty space must either be self-supporting or include support structures that must be removed once the print is complete. In general, it is best to avoid support structures when possible for any components where surface roughness is relevant. In the case of the waveguides detailed here, no dedicated support structures are used, meaning that all features of the

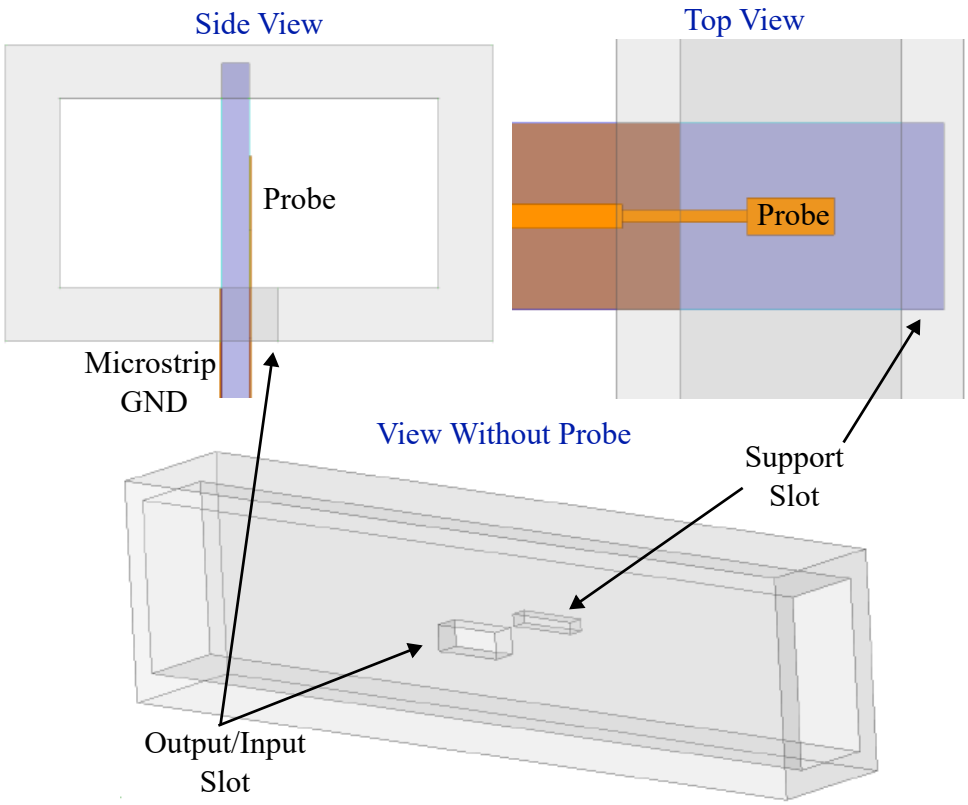


Figure 7.5: 3D models in made in ANSYS HFSS of (a) 2-port shorted section and (b) a 3-port section of the traveling wave combiner using a alumina microstrip probes and WR-28 waveguide dimensions.

model must be self-supporting. An unmodified length of waveguide is a self-supporting structure on its own assuming that it is printed vertically from end to end. However, the slots and irises introduced to the interior of the waveguide are not self-supporting by default. Fig 7.6 highlights the changes needed to make both the slots and the irises self-supporting.

First, the iris is modified by including a 45° section slanting down towards the interior wall of the waveguide. It is crucial that this 45° portion is angled downward towards the base of the print so that the resin can gradually build its way up and out with each layer. Although this is a simple change, it does significantly impact the dimensions of the iris, necessitating re-tuning in simulation with the new form. Because the slots along the sides of the waveguide are already quite narrow (1 mm across in the smallest dimension), there is a much simpler solution to make them self-supporting. As seen in the figure, the corners of the slot are given fillets with a constant radius

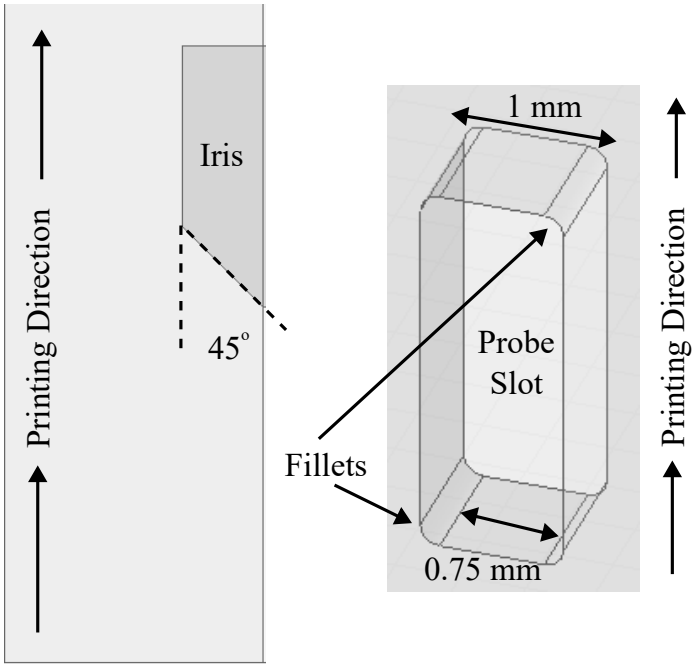


Figure 7.6: Diagram of adjustments made to the irises (left) and slots for the microstrip probes (right). The iris is given a wedge shape with a 45° slant downward towards the waveguide wall. The corners of the slots are given 150 μm radius of curvature fillets to approximate a semi-circle.

of curvature of 150μm. Because the minimum resolution of an average DLP printer is about 750 μm, the unsupported vertical edges of the slot appear to be semi-circles (a self-supporting structure) to the printer.

Remaining work for this design involves the following:

(1) Finish tuning each section of waveguide for a 4-way combiner, keeping in mind modifications made for 3D printing.

(2) Conduct a brief surface roughness analysis using HFSS, keeping in mind that the average surface roughness for an 8k resolution DLP printer is about 2 - 4 μm rms.

(3) 3D print and metalize waveguide sections and have alumina probes fabricated and sub-diced.

(4) Assemble combiner and test both with passive through-lines and using Ka-band PAs from Chapters 5 and 6.

7.2.4 Measurement of Ka-band Power Amplifiers

As discussed in Chapters 5 and 6, there are four power amplifiers designed using three different GaN-on-SiC technologies that are still in fabrication as of September 2025. The four amplifiers in question include:

(1) the redesigned PA in the WIN 120 nm process using improved transistor models and simulated at higher device temperatures;

(2) the 3-stage 10 W power amplifier designed in the Qorvo 150 nm process;

(3) the 2-stage PA designed in the HRL T3L 40 nm process for over 40% PAE;

(4) and the 3-stage PA designed in the HRL T3L 40 nm process for over 40% PAE and high gain (28 dB).

Each of these designs are also candidates be integrated with the traveling wave combiner discussed in the previous subsection. Additionally, as mentioned in Chapter 6, the die with the 10 W PA design contains two side-by-side iterations. Both PAs can be bonded to an off-chip power combiner, as seen in Fig. 7.7, to extract close to 20 W of output power CW. However, given the significant power dissipation in the 5 mm $\times$ 5 mm, special care will need to be taken to ensure proper heat sinking, possibly including coupled EM and thermal simulations.

7.3 Summary of Contributions

Contributions to research areas including rectenna design and fabrication, low-loss interconnects and packaging, and MMIC PA design are summarized below.

Chapter 2: A detailed description of the design and characterization of a scalable, flexible rectenna using unconventional and low-cost materials. Scaling and durability tests are discussed in Chapter 3. Results are reported in [6] and [7].

Chapter 3: Subarrays discussed in Chapter 3 are scaled as large as 1 m $\times$ 1 m. Scaled arrays are tested after exposure to harsh weather conditions including rain and thunderstorms and

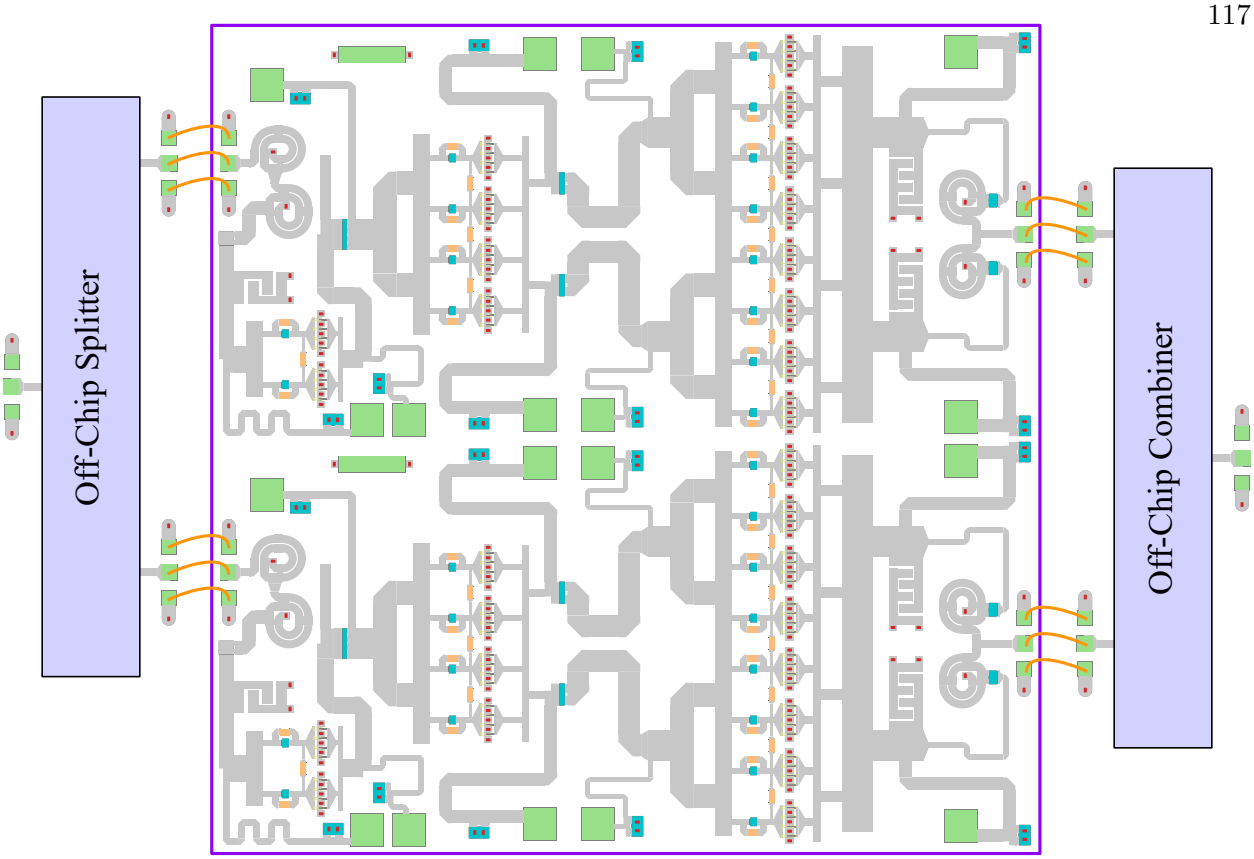


Figure 7.7: Diagram of the die under fabrication using the Qorvo 150 nm process. The PAs can be bonded to off-chip power amplifiers for increased output power.

integrated with TVS diodes for ESD suppression. Results are reported in [7].

Chapter 4: The design of low-loss interconnects and other test structures from dc to 50 GHz using a novel and experimental packaging process intended for heterogeneous integration is presented. Results are reported in [63, 66, 64].

Chapter 5: A Ka-band 5 W power amplifier using the WIN Semiconductors 120 nm GaN-on-SiC process is designed and measured. A redesign is presented that takes into account thermal effects and new transistor models. Results are reported in [75].

Chapter 6: Three Ka-band PAs using two different state-of-the-art GaN-on-SiC technologies are designed using a unique method involving parameterized bus-bar combiners for high output power. Results are planned to be published in the IEEE TMTT journal after the die are delivered and measured.

Chapter 8

Appendix: Electromagnetic Design of Excitation Coils for an Inductively-Coupled Plasma Etching System

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8.1 Introduction

Semiconductor manufacturing is continuously developing as demands on device performance increase, as can be seen in reviews from 2001 [96] and 2012 [97]. One of the processing steps involves etching semiconductors using RF plasma, which has been developed for material processing since the 1960's, e.g. [98]. More recent reviews of RF plasma etching can be found in [99] and [100]. Demands on semiconductor devices, including higher voltages, faster switching speeds and higher efficiency, translate to requirements for more precise manufacturing processes such as deeper etching. Higher aspect ratio etching requires more uniform silicon etch processes in order to create trenches that feature aspect ratios upwards of 60:1 [30]. Without a high degree of etch uniformity it would not be possible to achieve this level of resolution.

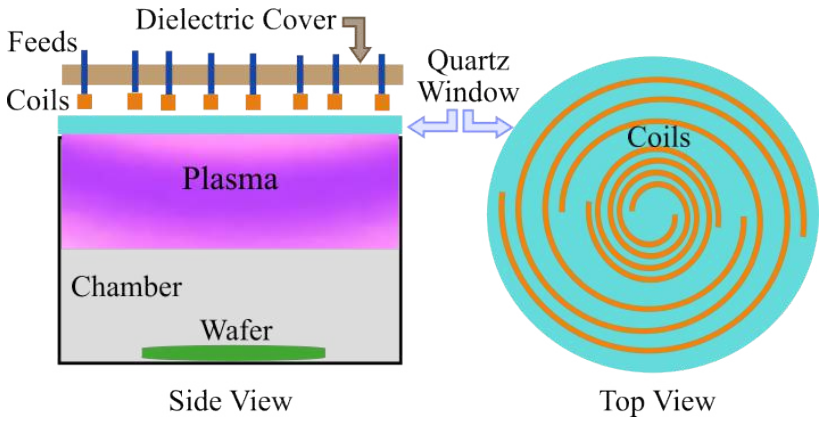
Manufacturing equipment for semiconductor processing, including plasma etching, is reviewed in [101]. In most of these systems, magnetic coupling to a plasma is used for etching, and is implemented with kW power levels in the Industrial, Scientific and Medical (ISM) bands. An example configuration which employs concentric copper coils at 13.56 MHz is the Syndion ICP machine [30]. The goal is to produce a uniform, inductively coupled plasma (ICP), which in turn requires a uniformly distributed magnetic field in the plasma itself.

In addition to semiconductor etching, ICPs have been used in a number of other applications over the last 60 years, including thermal plasmas for material processing, atomic emission spectroscopy, and mass spectrometry [102]. ICP is a type of plasma in which the supplied energy is transferred through the electromagnetic fields generated by the flow of RF currents in a coil in a configuration sketched in Fig. A.1(a). Electrons in the supplied gas are accelerated by the induced electric field and collide with one another and other particles. Some commonly used gases are argon, hydrogen, oxygen and certain fluorine or chlorine compounds. The plasma is created and sustained through Joule losses resulting from these rapid collisions which assist in etching the patterned semiconductor wafer placed below the plasma [103] [104].

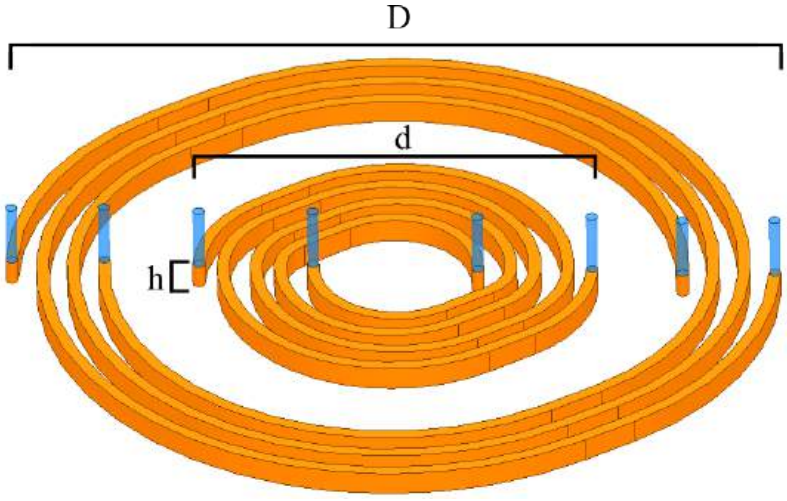
The goal of the research presented in this chapter is the design and optimization of a 13.56 MHz ICP system, specifically focused on the electromagnetic design of the RF excitation coils, Fig. A.1(b). The two prioritized areas of improvement are: (1) reduced conduction loss in the coils; and (2) a uniformly distributed magnetic field in the plasma [105, 106]. A uniform magnetic field ensures a more uniform plasma and, in turn, consistent etching across the entire semiconductor wafer. Coil designs are simulated and compared under these metrics using the Ansys HFSS 3D full-wave electromagnetic solver.

8.2 Coil Design and Modification

The original design consists of two pairs of concentric coils or two “outer coils” and two “inner coils” with rectangular cross sections as shown in Fig. A.1(b). The coils are suspended above a quartz window which separates them from the interior of the etching cavity illustrated in



(a)



(b)

Figure 8.1: (a) Simplified diagram of inductively-coupled plasma (ICP) etching system highlighting relevant components. (b) Model of the excitation consisting of a pair of copper inner coils with diameter d and a pair of outer coils with diameter D, both having rectangular cross sections. The dimensions are approximately $d \approx 0.25\,\mathrm{m}$, $D \approx 0.5\,\mathrm{m}$ and $h \approx 1\,\mathrm{cm}$.

Fig. A.1(a). Additionally, the coils are covered by a dielectric shield made from polyetherimide with a slot cut out for the feed lines. Restrictions on coil optimization include maintaining alignment of coil feed lines along a single axis and constraining the position of the coils between radii of 40 mm and 200 mm from the center of the cavity. These constraints are determined by the feed network used in the current Syndion system [30].

8.2.1 Coil Cross Section

First, the coil cross section shape is changed from rectangular to several other shapes, such as circular, tee-shaped, folded, bridge-shaped, etc. The skin depth in copper at 13.56 MHz is about 18 μm, so we consider the loss due to surface current. Without taking into account the surface current density distribution, it might seem that a larger surface area, such as in the case of a tee cross section, will result in lower loss due to the increased surface area. However, simulations show that edge effects override the benefits from increased surface area due to current confinement on the corners resulting in increased conduction losses.

The circular cross-section removes corners from the coils which reduces the effects of current bunching. The surface loss density (in W/m^2) is compared along one coil using a rectangular cross section of approximately 6 mm$\times$13 mm and one with a circular cross section with a radius chosen to maintain a diameter of similar size to the width of the rectangular coils. The comparison of the simulations is shown in Fig. A.2. Mapping the surface loss density over the coils highlights areas of high conduction loss and current distribution. By comparison, a cross-section with no sharp corners results in the least total conduction loss while having less total surface area than the rectangular shaped coil. Although the loss reduction is small, the rounded cross section has the additional advantage of requiring less copper to manufacture. This advantage is even more pronounced with a hollow conductor with no noticeable increase in loss due to skin depth.

8.2.2 Dielectric Cover

The dielectric cover on top of the chamber seen in Fig. A.1(a) mechanically protects the coils and is a safety feature. The distance of the dielectric cover to the coils (on the order of a centimeter) has an impact on performance and can be adjusted. Moving the cover further away from the coils results in an increase of RF power transferred to the plasma. Starting from a nominal distance of 10 mm from the coils, the system is simulated with the dielectric cover moving between 10 mm and 40 mm from the coils. The effects on the amount of power dissipated in the plasma, as well as

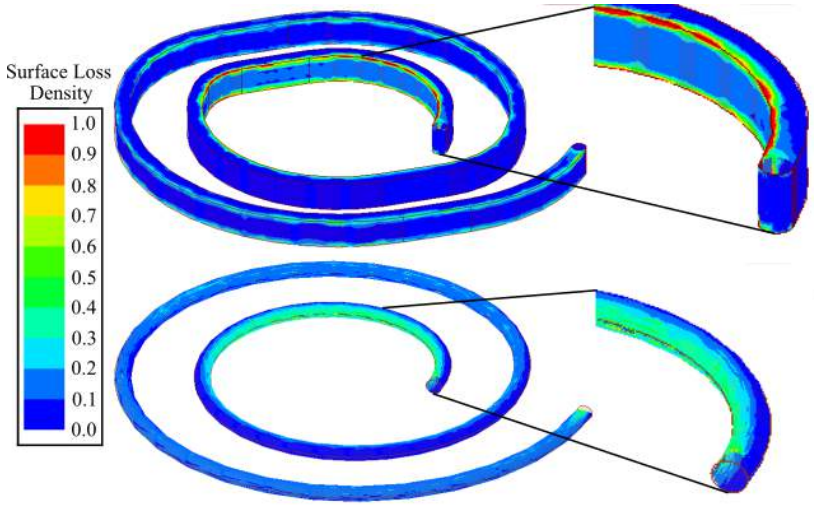


Figure 8.2: Normalized surface loss density (W/m^2) along an inner coil for rectangular and circular cross sections at 13.56 MHz. Areas of high conduction loss on the rectangular coil are contrasted with the more uniform circular coil.

conduction loss in the coils, are plotted in Fig. A.3. It is shown that in addition to improved power transfer to the plasma, shown by the improvement in power transfer efficiency, conduction loss in the coils also decreases significantly as the cover is moved further away.

As shown by the figure, the overall power transfer efficiency to the plasma is high in general, making improvements appear marginal. However, because this is a high-power system, the dissipated power due to conduction loss in the coils is still on the order of 15-20 W. Therefore the percent change in conduction loss, shown on the right hand side of Fig. A.3, represents a non-negligible reduction in wasted energy.

The improved performance is partially a result of less energy coupling into the polyetherimide cover which is supported by simulations showing reduced Joule loss in the cover with increased distance from the coils. However, the reduced conduction losses in the copper coils suggests that their distance from the top cover may also impact the magnetic flux through the coils as well as the capacitance through the cover to ground.

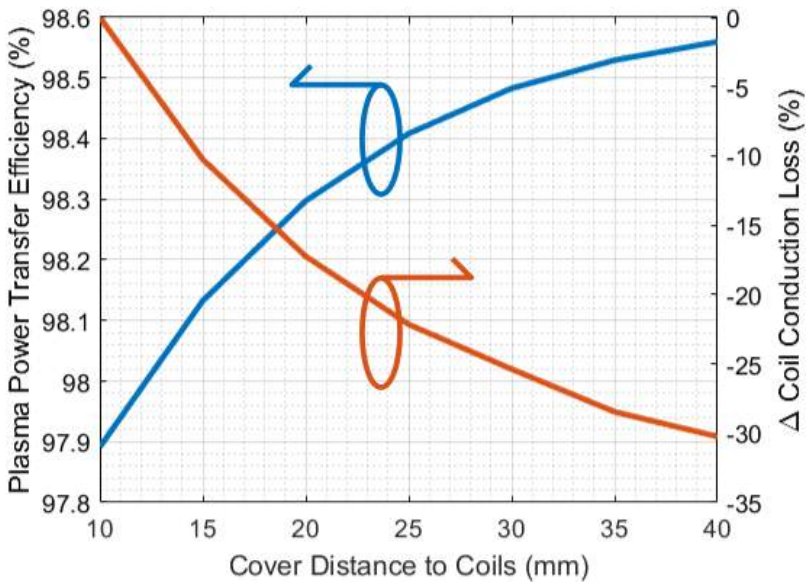


Figure 8.3: Efficiency of power transfer to the plasma (blue) and associated change in coil conduction loss (red) at 13.56 MHz as the distance between the dielectric cover and the coils increases from the baseline of 10 mm.

8.2.3 Magnetic Field Uniformity

Finally, in order to improve the uniformity of the generated magnetic field, the distance between inner and outer coils and the spacing between turns or the coil "ring width" are adjusted. This is shown in Fig. A.4 with two different coil configurations as examples. In order to quantify the differences in field uniformity between coil variations, the magnitude of the complex magnetic field is sampled across the horizontal cross-section in the chamber immediately below the quartz window. Figure A.5 shows the magnetic field magnitude plotted as a function of distance from the chamber axis. It is important to note that the magnetic field magnitude in the center of the chamber is not of concern because the inflow of gas in this region compensates for the lower field strength. With this in mind, the chosen area of investigation lies between radii of 50 mm and 150 mm from the center of the chamber at 1 cm distance below the quartz window.

If the majority of the RF power is channeled through the outer two coils (by tuning the matching circuit), it is determined that increasing the spacing between turns in the outer coils

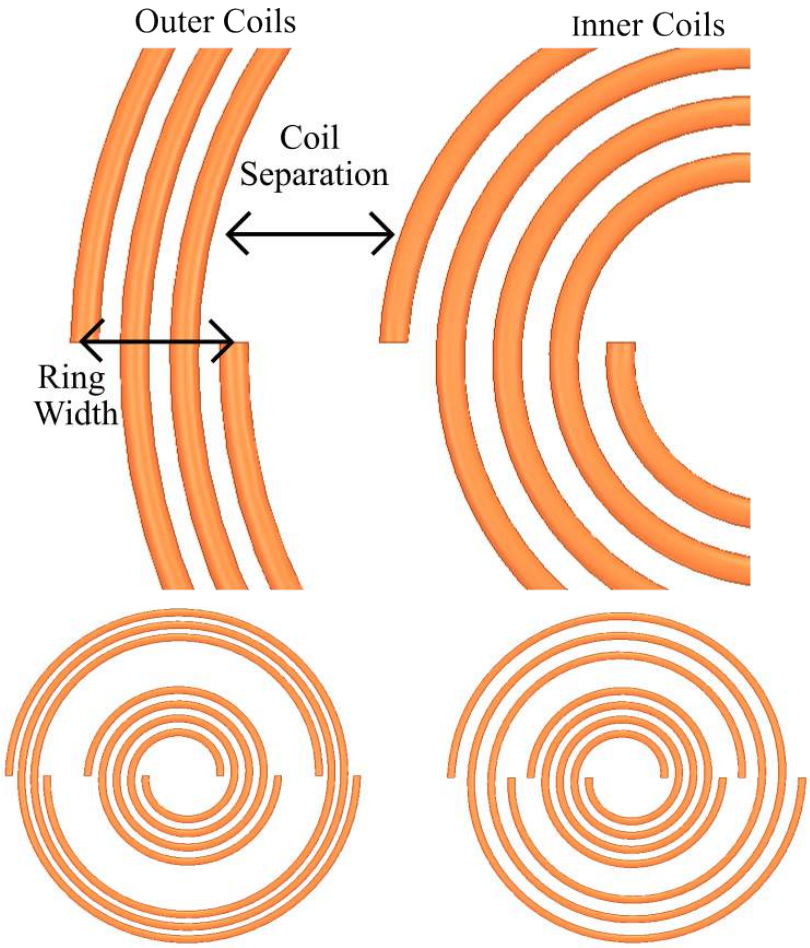


Figure 8.4: Diagram showing the two dimensions in which the outer coils are adjusted to improve magnetic field uniformity: (i) the ring width; and (ii) the distance separating the inner and outer coils. Two example configurations are shown.

while maintaining the turn spacing of the inner coils improves uniformity. As shown in Fig. A.5, the amount of variation decreases significantly moving from case 1 to case 5, corresponding to an increase in spacing between outer coil turns and reduced coil separation as listed by Table A.1. The table also lists standard deviations of the magnetic field magnitude for each of the five cases. However, if a majority of RF power is channeled through the inner two coils, the simulated results mirror those shown in Fig. A.5 if the turn spacing or "ring width" of the inner coils is increased instead of the outer coils. Additionally, it is found that adding a slight vertical taper to the inner coil, causing it to form a short conical helix, can improve the uniformity of the magnetic field at

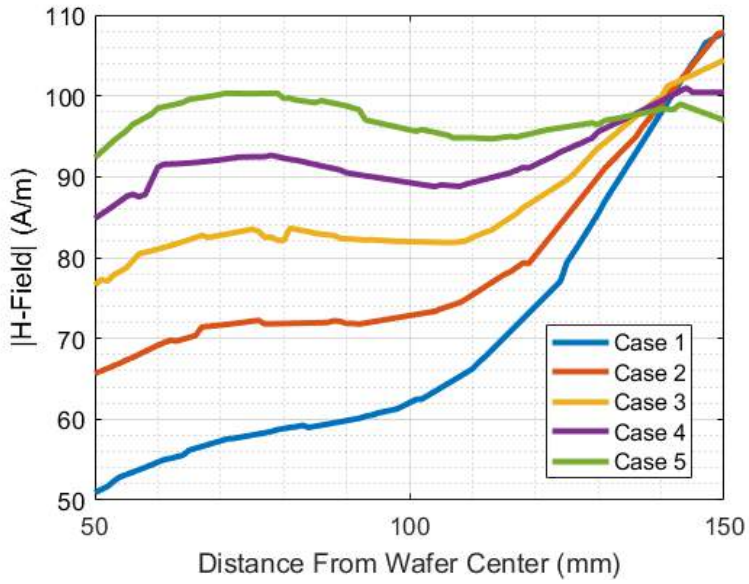


Figure 8.5: Plot of the complex magnetic field magnitude at points between 50 mm and 150 mm from the center of the chamber and 1 cm below the quartz window, for the 5 cases described in Table A.1.

the cost of reduced efficiency as shown by Fig A.6.

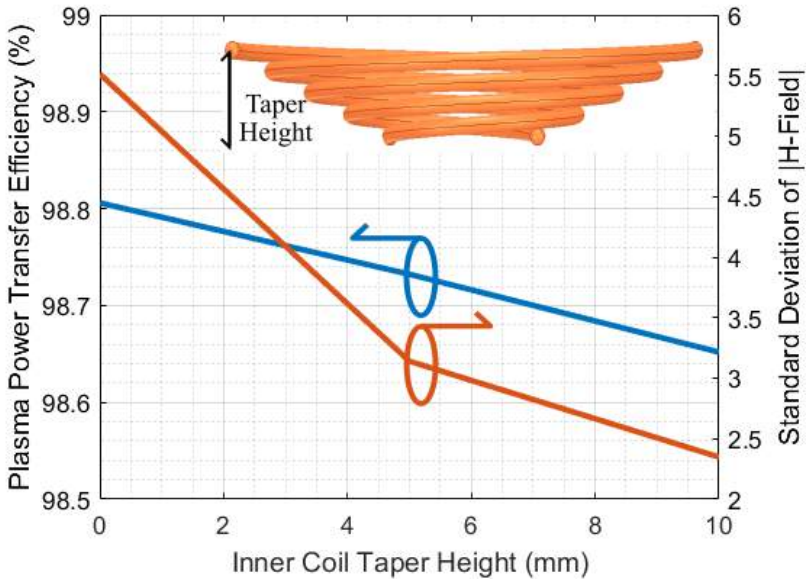


Figure 8.6: Efficiency of power transfer to the plasma (blue) and standard deviation of magnetic field magnitude corresponding to the range of distances from 50 to 100 mm (orange), as the height of the conical taper is increased from 0 mm to 10 mm.

Table 8.1: Outer Coil Size & Position

Case	***Ring Width***	***Coil Separation***	$\sigma(\|H\|)$
1	42 mm	45 mm	16.41
2	48 mm	39 mm	11.62
3	54 mm	33 mm	7.46
4	60 mm	27 mm	3.89
5	66 mm	21 mm	1.96

For the final design of the coil, each of the previously discussed techniques are combined to improve both magnetic field uniformity and power transfer efficiency regardless of which pair of coils carries a majority of the input power. The improved coil is simulated and compared with the original under both excitation conditions. A map of the magnetic field distribution at a fixed 1-cm distance below the quartz window is shown in Fig. A.7 for the original (left) and redesigned configuration (right) with the location of the semiconductor wafer indicated by the black dotted circle. Fig. A.7a represents the case when the majority of the RF input current flows through the outer two coils, while Fig. A.7b is the case when the inner coils carry most of the current. As shown for both cases, the magnetic field strength distribution of the improved coil design is significantly more uniform over area compared to the original.

8.3 Conclusion

In summary, this chapter presents the simulated performance of an existing 13.56 MHz ICP system used by Lam Research for semiconductor etching. We then compare it with an improved design which achieves a 98.5% efficiency of RF power delivered to the plasma and 28% reduced conduction loss. Additionally, the new coil design maintains a magnetic field distribution with a 22% lower standard deviation in magnitude across the area of interest. These percentage improvements are a result of averaging between two drive cases with different matching networks; one in which the majority of current flows through the outer coils, and the other where it is concentrated in the inner coils.

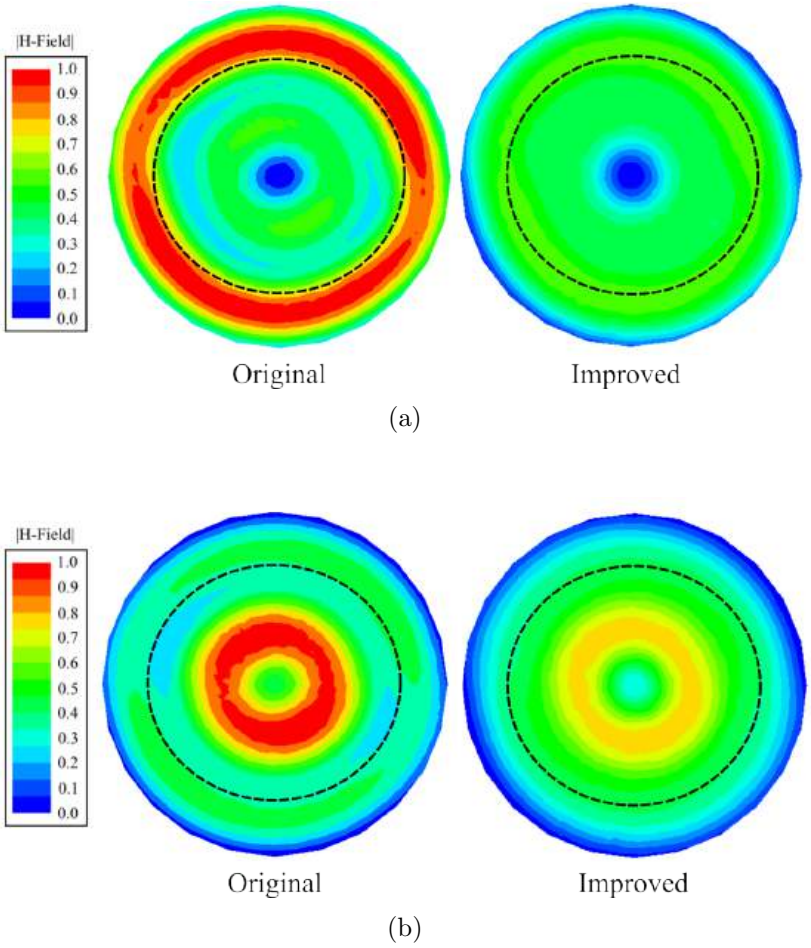


Figure 8.7: (a) Simplified diagram of inductively-coupled plasma (ICP) etching system highlighting relevant components. (b) Model of the excitation consisting of a pair of copper inner coils with diameter d and a pair of outer coils with diameter D, both having rectangular cross sections. The dimensions are approximately $d \approx 0.25\,\mathrm{m}$, $D \approx 0.5\,\mathrm{m}$ and $h \approx 1\,\mathrm{cm}$.

Acknowledgment

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Appendix A

Appendix: Electromagnetic Design of Excitation Coils for an Inductively-Coupled Plasma Etching System

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A.1 Introduction

Semiconductor manufacturing is continuously developing as demands on device performance increase, as can be seen in reviews from 2001 [96] and 2012 [97]. One of the processing steps involves etching semiconductors using RF plasma, which has been developed for material processing since the 1960's, e.g. [98]. More recent reviews of RF plasma etching can be found in [99] and [100]. Demands on semiconductor devices, including higher voltages, faster switching speeds and higher efficiency, translate to requirements for more precise manufacturing processes such as deeper etching. Higher aspect ratio etching requires more uniform silicon etch processes in order to create trenches that feature aspect ratios upwards of 60:1 [30]. Without a high degree of etch uniformity it would not be possible to achieve this level of resolution.

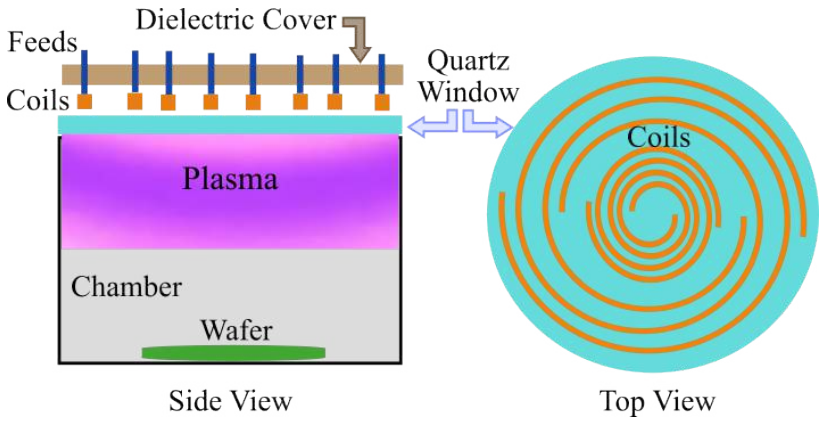
Manufacturing equipment for semiconductor processing, including plasma etching, is reviewed in [101]. In most of these systems, magnetic coupling to a plasma is used for etching, and is implemented with kW power levels in the Industrial, Scientific and Medical (ISM) bands. An example configuration which employs concentric copper coils at 13.56 MHz is the Syndion ICP machine [30]. The goal is to produce a uniform, inductively coupled plasma (ICP), which in turn requires a uniformly distributed magnetic field in the plasma itself.

In addition to semiconductor etching, ICPs have been used in a number of other applications over the last 60 years, including thermal plasmas for material processing, atomic emission spectroscopy, and mass spectrometry [102]. ICP is a type of plasma in which the supplied energy is transferred through the electromagnetic fields generated by the flow of RF currents in a coil in a configuration sketched in Fig. A.1(a). Electrons in the supplied gas are accelerated by the induced electric field and collide with one another and other particles. Some commonly used gases are argon, hydrogen, oxygen and certain fluorine or chlorine compounds. The plasma is created and sustained through Joule losses resulting from these rapid collisions which assist in etching the patterned semiconductor wafer placed below the plasma [103] [104].

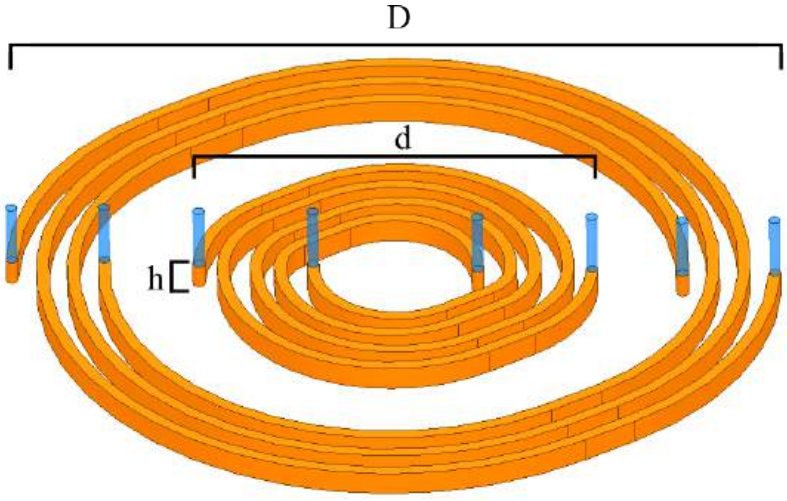
The goal of the research presented in this chapter is the design and optimization of a 13.56 MHz ICP system, specifically focused on the electromagnetic design of the RF excitation coils, Fig. A.1(b). The two prioritized areas of improvement are: (1) reduced conduction loss in the coils; and (2) a uniformly distributed magnetic field in the plasma [105, 106]. A uniform magnetic field ensures a more uniform plasma and, in turn, consistent etching across the entire semiconductor wafer. Coil designs are simulated and compared under these metrics using the Ansys HFSS 3D full-wave electromagnetic solver.

A.2 Coil Design and Modification

The original design consists of two pairs of concentric coils or two "outer coils" and two "inner coils" with rectangular cross sections as shown in Fig. A.1(b). The coils are suspended above a quartz window which separates them from the interior of the etching cavity illustrated in



(a)



(b)

Figure A.1: (a) Simplified diagram of inductively-coupled plasma (ICP) etching system highlighting relevant components. (b) Model of the excitation consisting of a pair of copper inner coils with diameter d and a pair of outer coils with diameter D, both having rectangular cross sections. The dimensions are approximately $d \approx 0.25\,\mathrm{m}$, $D \approx 0.5\,\mathrm{m}$ and $h \approx 1\,\mathrm{cm}$.

Fig. A.1(a). Additionally, the coils are covered by a dielectric shield made from polyetherimide with a slot cut out for the feed lines. Restrictions on coil optimization include maintaining alignment of coil feed lines along a single axis and constraining the position of the coils between radii of 40 mm and 200 mm from the center of the cavity. These constraints are determined by the feed network used in the current Syndion system [30].

A.2.1 Coil Cross Section

First, the coil cross section shape is changed from rectangular to several other shapes, such as circular, tee-shaped, folded, bridge-shaped, etc. The skin depth in copper at 13.56 MHz is about 18 μm, so we consider the loss due to surface current. Without taking into account the surface current density distribution, it might seem that a larger surface area, such as in the case of a tee cross section, will result in lower loss due to the increased surface area. However, simulations show that edge effects override the benefits from increased surface area due to current confinement on the corners resulting in increased conduction losses.

The circular cross-section removes corners from the coils which reduces the effects of current bunching. The surface loss density (in W/m^2) is compared along one coil using a rectangular cross section of approximately 6 mm$\times$13 mm and one with a circular cross section with a radius chosen to maintain a diameter of similar size to the width of the rectangular coils. The comparison of the simulations is shown in Fig. A.2. Mapping the surface loss density over the coils highlights areas of high conduction loss and current distribution. By comparison, a cross-section with no sharp corners results in the least total conduction loss while having less total surface area than the rectangular shaped coil. Although the loss reduction is small, the rounded cross section has the additional advantage of requiring less copper to manufacture. This advantage is even more pronounced with a hollow conductor with no noticeable increase in loss due to skin depth.

A.2.2 Dielectric Cover

The dielectric cover on top of the chamber seen in Fig. A.1(a) mechanically protects the coils and is a safety feature. The distance of the dielectric cover to the coils (on the order of a centimeter) has an impact on performance and can be adjusted. Moving the cover further away from the coils results in an increase of RF power transferred to the plasma. Starting from a nominal distance of 10 mm from the coils, the system is simulated with the dielectric cover moving between 10 mm and 40 mm from the coils. The effects on the amount of power dissipated in the plasma, as well as

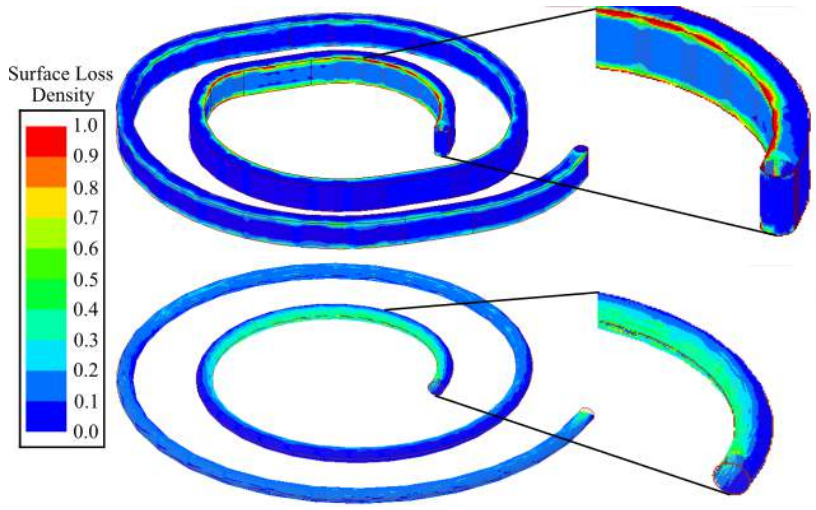


Figure A.2: Normalized surface loss density (W/m^2) along an inner coil for rectangular and circular cross sections at 13.56 MHz. Areas of high conduction loss on the rectangular coil are contrasted with the more uniform circular coil.

conduction loss in the coils, are plotted in Fig. A.3. It is shown that in addition to improved power transfer to the plasma, shown by the improvement in power transfer efficiency, conduction loss in the coils also decreases significantly as the cover is moved further away.

As shown by the figure, the overall power transfer efficiency to the plasma is high in general, making improvements appear marginal. However, because this is a high-power system, the dissipated power due to conduction loss in the coils is still on the order of 15-20 W. Therefore the percent change in conduction loss, shown on the right hand side of Fig. A.3, represents a non-negligible reduction in wasted energy.

The improved performance is partially a result of less energy coupling into the polyetherimide cover which is supported by simulations showing reduced Joule loss in the cover with increased distance from the coils. However, the reduced conduction losses in the copper coils suggests that their distance from the top cover may also impact the magnetic flux through the coils as well as the capacitance through the cover to ground.

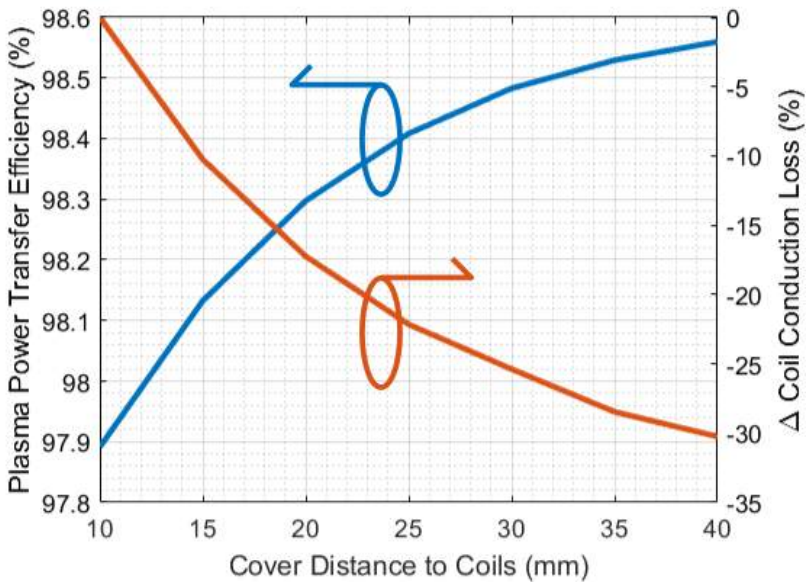


Figure A.3: Efficiency of power transfer to the plasma (blue) and associated change in coil conduction loss (red) at 13.56 MHz as the distance between the dielectric cover and the coils increases from the baseline of 10 mm.

A.2.3 Magnetic Field Uniformity

Finally, in order to improve the uniformity of the generated magnetic field, the distance between inner and outer coils and the spacing between turns or the coil "ring width" are adjusted. This is shown in Fig. A.4 with two different coil configurations as examples. In order to quantify the differences in field uniformity between coil variations, the magnitude of the complex magnetic field is sampled across the horizontal cross-section in the chamber immediately below the quartz window. Figure A.5 shows the magnetic field magnitude plotted as a function of distance from the chamber axis. It is important to note that the magnetic field magnitude in the center of the chamber is not of concern because the inflow of gas in this region compensates for the lower field strength. With this in mind, the chosen area of investigation lies between radii of 50 mm and 150 mm from the center of the chamber at 1 cm distance below the quartz window.

If the majority of the RF power is channeled through the outer two coils (by tuning the matching circuit), it is determined that increasing the spacing between turns in the outer coils

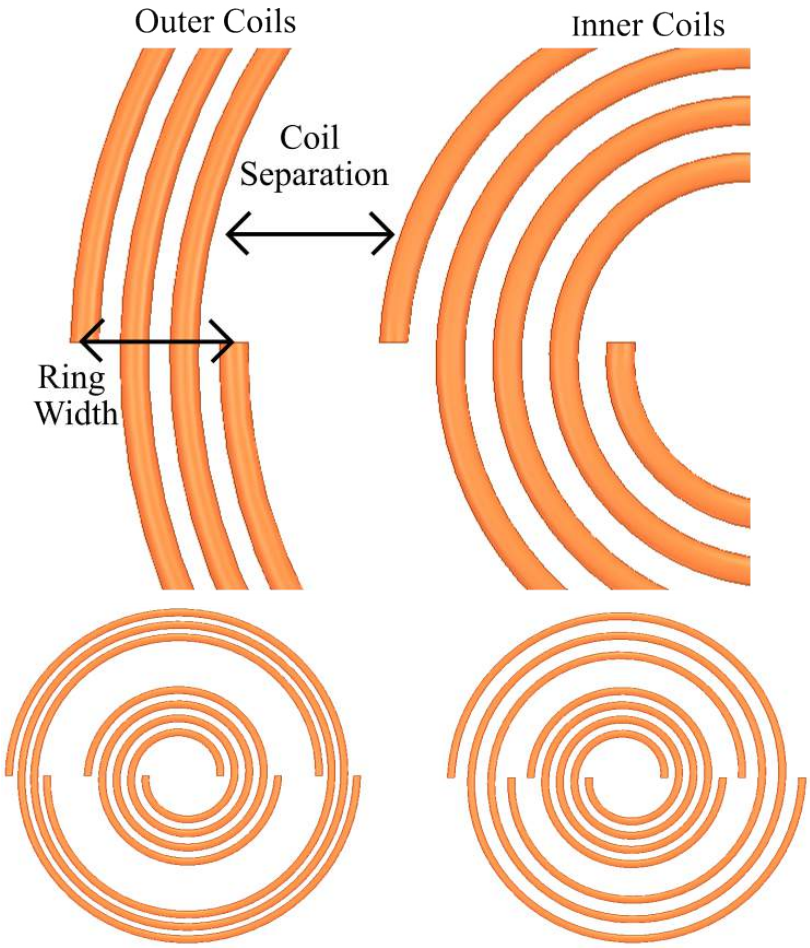


Figure A.4: Diagram showing the two dimensions in which the outer coils are adjusted to improve magnetic field uniformity: (i) the ring width; and (ii) the distance separating the inner and outer coils. Two example configurations are shown.

while maintaining the turn spacing of the inner coils improves uniformity. As shown in Fig. A.5, the amount of variation decreases significantly moving from case 1 to case 5, corresponding to an increase in spacing between outer coil turns and reduced coil separation as listed by Table A.1. The table also lists standard deviations of the magnetic field magnitude for each of the five cases. However, if a majority of RF power is channeled through the inner two coils, the simulated results mirror those shown in Fig. A.5 if the turn spacing or "ring width" of the inner coils is increased instead of the outer coils. Additionally, it is found that adding a slight vertical taper to the inner coil, causing it to form a short conical helix, can improve the uniformity of the magnetic field at

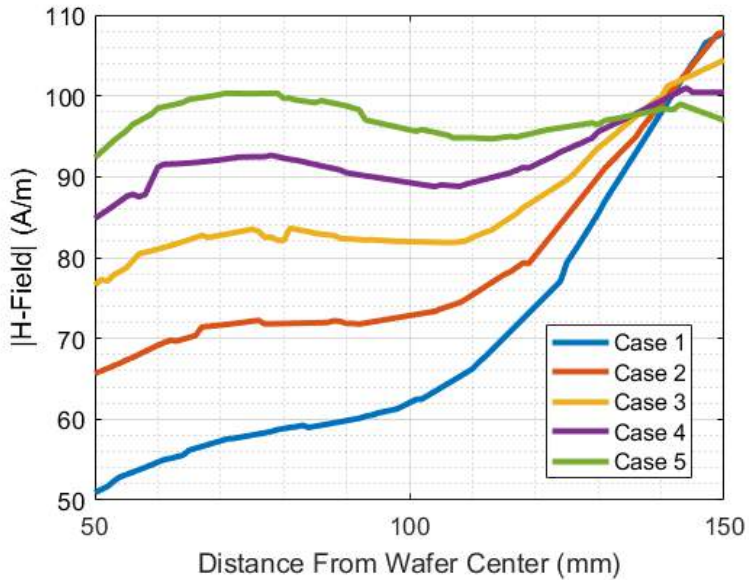


Figure A.5: Plot of the complex magnetic field magnitude at points between 50 mm and 150 mm from the center of the chamber and 1 cm below the quartz window, for the 5 cases described in Table A.1.

the cost of reduced efficiency as shown by Fig A.6.

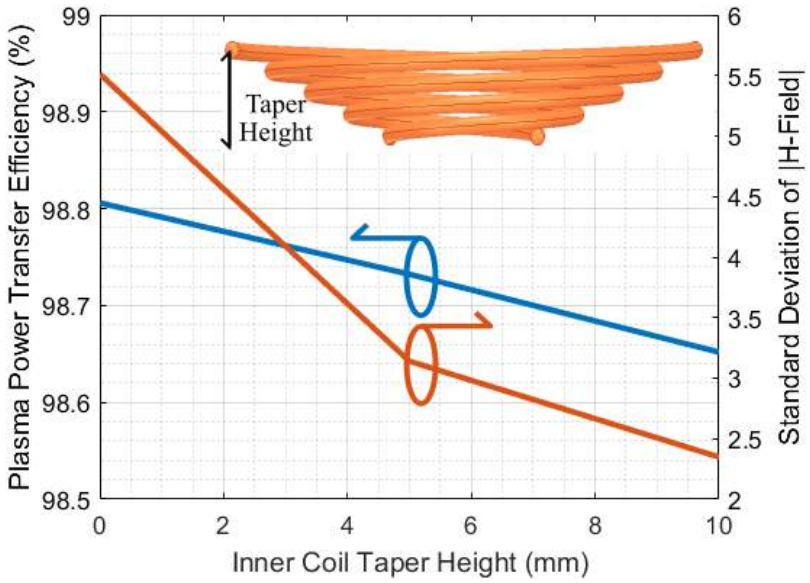


Figure A.6: Efficiency of power transfer to the plasma (blue) and standard deviation of magnetic field magnitude corresponding to the range of distances from 50 to 100 mm (orange), as the height of the conical taper is increased from 0 mm to 10 mm.

Table A.1: Outer Coil Size & Position

Case	***Ring Width***	***Coil Separation***	$\sigma(\|H\|)$
1	42 mm	45 mm	16.41
2	48 mm	39 mm	11.62
3	54 mm	33 mm	7.46
4	60 mm	27 mm	3.89
5	66 mm	21 mm	1.96

For the final design of the coil, each of the previously discussed techniques are combined to improve both magnetic field uniformity and power transfer efficiency regardless of which pair of coils carries a majority of the input power. The improved coil is simulated and compared with the original under both excitation conditions. A map of the magnetic field distribution at a fixed 1-cm distance below the quartz window is shown in Fig. A.7 for the original (left) and redesigned configuration (right) with the location of the semiconductor wafer indicated by the black dotted circle. Fig. A.7a represents the case when the majority of the RF input current flows through the outer two coils, while Fig. A.7b is the case when the inner coils carry most of the current. As shown for both cases, the magnetic field strength distribution of the improved coil design is significantly more uniform over area compared to the original.

A.3 Conclusion

In summary, this chapter presents the simulated performance of an existing 13.56 MHz ICP system used by Lam Research for semiconductor etching. We then compare it with an improved design which achieves a 98.5% efficiency of RF power delivered to the plasma and 28% reduced conduction loss. Additionally, the new coil design maintains a magnetic field distribution with a 22% lower standard deviation in magnitude across the area of interest. These percentage improvements are a result of averaging between two drive cases with different matching networks; one in which the majority of current flows through the outer coils, and the other where it is concentrated in the inner coils.

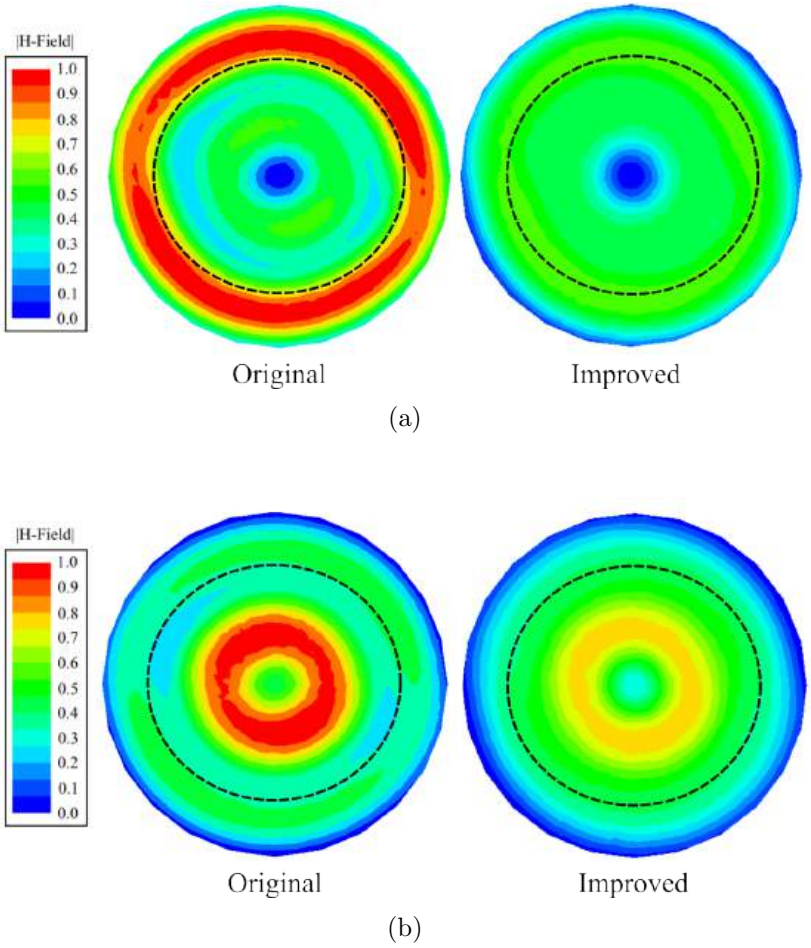


Figure A.7: (a) Simplified diagram of inductively-coupled plasma (ICP) etching system highlighting relevant components. (b) Model of the excitation consisting of a pair of copper inner coils with diameter d and a pair of outer coils with diameter D, both having rectangular cross sections. The dimensions are approximately $d \approx 0.25\,\mathrm{m}$, $D \approx 0.5\,\mathrm{m}$ and $h \approx 1\,\mathrm{cm}$.

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