Low Phase Noise MMIC Oscillators for Microwave Chip-Scale Atomic Clocks

by

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B.S., Michigan State University, 2019

M.S., University of Colorado Boulder, 2023

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical, Computer, and Energy Engineering

2026

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Accurate timing is critical in many industries, from time-stamping grocery receipts to facilitating stock market transactions and supporting precise navigation, localization, and guidance. High levels of precision are currently achieved using physically large, power-hungry atomic clocks that rely on energy level transitions in a chosen atomic species. Recently, commercially available chip-scale atomic clocks (CSACs) have emerged, offering atomically precise timing in a compact, low-power package that can be operated on a battery for extended periods. Such clocks have important applications in underwater timing for oil and gas exploration, enhanced GPS receivers, and are being adopted for application to the energy grid, where large clocks are impractical. These devices contain a microwave local oscillator (LO) that generates the RF frequency used to interrogate the atoms and, once locked to the atomic resonance, serves as the clock output. This thesis begins by reviewing the background of oscillators in microwave CSACs, with a focus on the engineering requirements for compact, low-power microwave LOs used to lock to the atomic transition. In the next two chapters, the metrics used to evaluate the effects of the LO on CSAC performance are reviewed, and several different LO designs are surveyed and compared in terms of power consumption, phase noise and suitability for use in miniaturized clocks. Chapters 5 and 6 present a set of low-phase noise MMIC oscillators designed in InGaP/GaAs HBT, which utilize standard on-chip resonators, non-uniform transmission line resonators, and high-Q off-chip glass-embedded resonators. Then, the MMIC oscillators from chapter 6 are tested with a miniaturized beam clock at NIST as a proof of concept. In Chapter 7, a set of balanced MMIC oscillators are presented, with plans to be implemented in a fully integrated chip-scale atomic beam clock. Finally, conclusions and future work are discussed, including a 231 GHz oscillator designed in GaN.

Dedication

To my friends, my family, and future wife, Marlena, who have taught me everything I know and loved me always. Thank you.

Acknowledgements

My years at the University of Colorado Boulder would not have been the same without the countless people who have taken time from their own lives to help me with my own. I owe special thanks to my advisor, Prof. Zoya Popović, who has shown me how to work with unwavering faith and dedication. You have helped me expand my horizons by fostering my growth as a researcher, exposing me to new parts of the world, and giving me the confidence to succeed. Thank you for providing me such a transformative opportunity. I am also extremely grateful to my committee members and mentors, especially Dr. William McGehee and Prof. Laila Marzall, who have been a great source of technical knowledge, personal support, and immense help in experiments.

I am so thankful for the hilarious, thoughtful, and maddening moments I have shared with my fellow graduate students: Stefan, Reyes, Georgia, Joel, Paul, Jooeun, Jack, Seth, Ben, Jori, Yaqub, Grace, Ricky, Allie, Songyi, Sofia, Joseph, Molly, Arunima, Ariana, Marcus, Aadesh, and so many more I omit due to space. This department is full of character—and unforgettable characters. It has been a privilege to spend my time among them. I have laughed enough for a lifetime.

This journey would not be complete without acknowledging my dearest friends, Paz, Tony, Will, Kisil, Gamero, Joe (both), Colin, Bill, Vince, Rakesh, Karl, Bianca, Ellie, and so many more skiing, Michigan, and Melee related friends. Your unwavering support has meant the world to me, and I will never forget the amazing conversations I've had with all of you. I am the luckiest.

Thank you to my Mom for showing me that artistry, mastery, and love come in many forms. Thank you, Dad, for instilling resilience and always believing in me. Thank you to my Grandparents, for letting me stand on your shoulders. Finally, thank you to my fiancée Marlee, who has taught me that love and going outside are all you need. I cannot wait for our adventures to come.

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Chapter 1

Introduction

1.1 An Overview of Chip-scale Atomic Clocks and their Applications

Time keeping plays a critical role in many high-volume applications, e.g. navigation and stock-market business transactions. In the field of metrology, time and frequency standards provide the most precisely measurable unit, the second, which subsequently underpins other dimensional metrology units, such as the meter, kilogram, and Ampere [1]. The high level of precision required for metrology and other applications is currently obtained using large and power-hungry atomic clocks which use electromagnetic waves at optical or microwave resonance frequencies to cause energy-level transitions in an atomic species. This accurately kept time is then often distributed via GPS, internet and radio to various platforms around the world. In the last 20 years, miniaturized low-power atomic clocks referred to as chip-scale atomic clocks (CSACs) using microwave atomic transition frequencies have been a topic of research and development, becoming especially important in GPS denied environments such as the deep ocean and space where they are currently in use. A simplified CSAC is illustrated in Fig. 1.1a, showing the microwave local oscillator, control circuits, quartz crystal, glass vapor cell containing alkali atoms (Cs or Rb), photodetector, and semiconductor laser, mounted on a printed circuit board. This clock provides an atomically defined 10 MHz output.

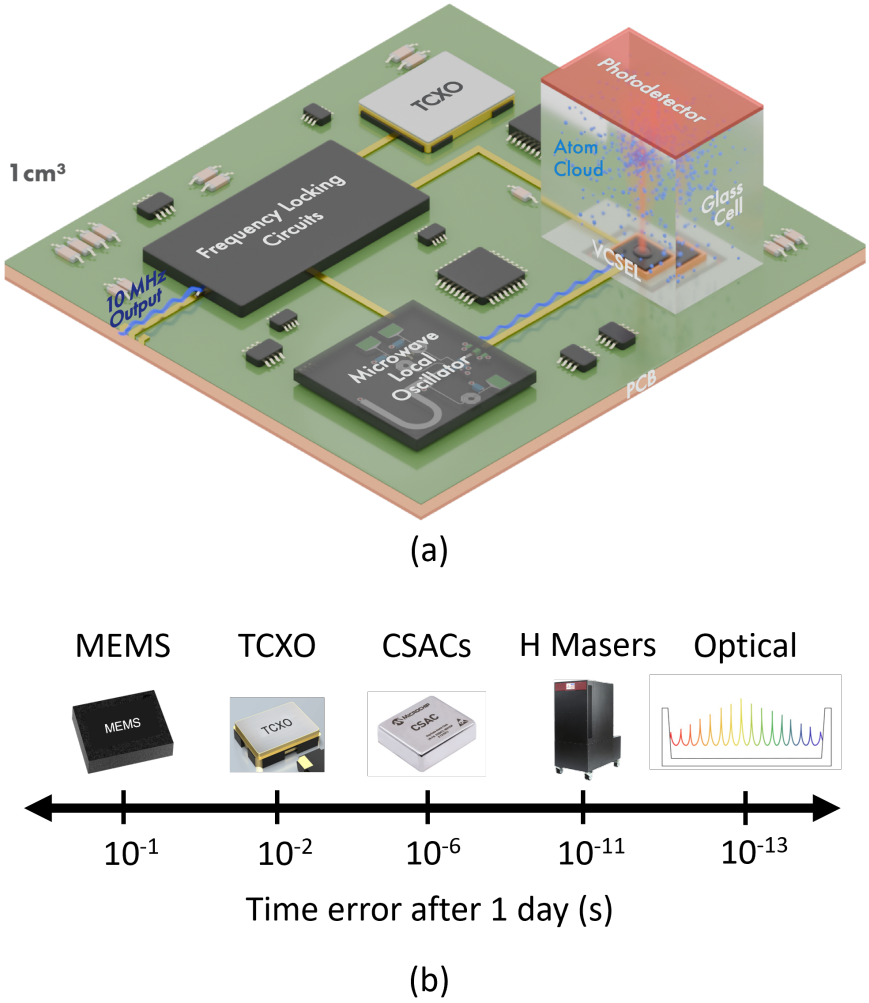


Figure 1.1: (a) Simplified illustration of a vapor cell chip-scale atomic clock (CSAC) based on a coherent population trapping (CPT) interrogation scheme. This architecture is the most prevalent in commercialized CSACs. (b) Time error after 1 day in (s), representative for MEMS, TCXO, CSACs, Hydrogen Masers, and Optical clocks based on [2,3].

Atomic clocks [4–6] are based on transitions in atoms whose frequencies depend largely on the laws of quantum mechanics and fundamental constants of nature such as the fine structure constant and the Bohr magneton. As a result, unlike classical resonators, every isolated atom of a given species has exactly the same transition frequency leading to excellent reproducibility in the output from clock to clock. In addition, the weak dependence of the clock frequency to external perturbations implies good long-term frequency stability and high accuracy, compared

to, for example, mechanical resonators like quartz crystals. There are several types of atomic clocks: large-scale fountain; optical lattice; and optical ion clocks, among others. These achieve timing errors equivalent to 1 ns over many decades but are large, consume high amounts of power, and are difficult to build and operate [7]. More compact clocks achieve correspondingly worse precision (1 ns to 1 μs over one day) but are less expensive, more reliable and have a size, weight and power suitable for deployment in a far greater range of application spaces. Figure 1.1b illustrates a stability comparison between different types of atomic clocks, which realize the second, underlie satellite-based navigation systems such as GNSS (Global Navigation Satellite System) [8], provide a backbone for secure communication [9], and can be used for deep-space navigation [10, 11]. The most common of these clocks are based on microwave transitions in alkali atoms, with transition frequencies in the GHz range.

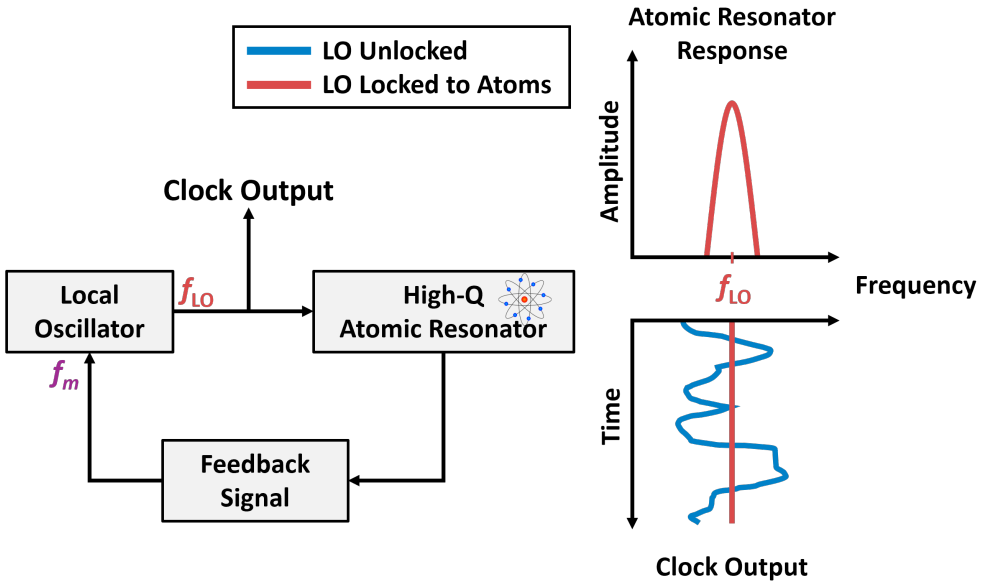


Figure 1.2: High-level microwave atomic clock block diagram showing process of locking to a high-Q atomic resonator. On the right side is an example of an atomic resonator response as well as oscillator frequency disciplined by the atoms.

Passive atomic clocks, a sub-category of atomic frequency standards that includes CSACs,

operate using a local oscillator (LO) that interacts with an ensemble of atoms. The atoms act as a high-Q frequency discriminator, generating an output signal that varies with LO frequency near the atomic resonance, as shown in Fig. 1.2a. This signal is then fed back to the LO in a control loop, locking its frequency to the atomic transition and thereby imparting the atoms' stability onto the LO.

1.2 Background on Chip-scale Atomic Clocks

The properties of the local oscillator play an important role in determining the clock performance. Often, the short-term ($< 1\,\mathrm{s}$) fractional frequency stability of the microwave LO is considerably better than that of the atoms and as a result can determine the short-term stability of the clock as a whole, as well as the time window for locking the LO to the atomic transition. Other properties of the LO such as the frequency drift and noise can also affect the stability of the clock, for example by intermodulation and aliasing effects [12]. There are many types of microwave atomic clock designs, and each has its own set of LO requirements. High-performance atomic clocks require correspondingly high-performance LOs, while more compact, lower-power atomic clocks require LOs which balance performance with additional size, weight, power and cost (SWaP-C) requirements. In the past 20 years, a new generation of low-power atomic clocks have been developed [3, 13–15] based on optical interrogation of alkali vapor cells in micro-machined vapor cells without the need for bulky microwave cavities. Typical atomic species used in these microwave clocks are ^{133}Cs and ^{87}Rb due to their high vapor pressure, large hyperfine splitting, simple electronic energy level structure, and availability of compatible semiconductor lasers. These types of CSACs have been successfully commercialized [16] and are currently making an impact across a range of application spaces from underwater seismology [16] to space [17]. They typically require under $200\,\mathrm{mW}$ of dc power to operate and have a total volume on the order of 1 to $20\,\mathrm{cm}^3$.

Figure 1.3b shows a more detailed block diagram of an example CSAC based on a coherent population trapping (CPT) atomic interrogation scheme [18, 19], which are the dominant type of commercially available chip-scale clocks [2, 3]. For CPT-based schemes, instead of exciting the

hyperfine transition in the atoms directly using a microwave field as is done in a traditional cesium beam clock, a pair of optical fields separated in frequency by the hyperfine splitting illuminates the atoms. Hyperfine coherences are generated through the nonlinear response of the atom to this pair of optical fields. Exciting the atoms using CPT-based methods has an advantage over traditional microwave clocks by removing the need for bulky microwave resonators which are usually at least one-half of the wavelength of the microwave signal, on the order of 3 cm for ^{133}Cs. Instead, CPT interrogation can rely on modulating the injection current of a vertical cavity surface emitting laser (VCSEL) diode [20, 21] to create sidebands on the emitted optical signal at spacings equal to the full ground-state hyperfine transition frequency (9.192 GHz for ^{133}Cs), or subharmonics of that transition (4.596 GHz for ^{133}Cs) [22]. These VCSELs can be fabricated in GaAs-based semiconductors at wafer scale, and, for example, can emit $\sim$1 mW of narrow linewidth light at 852 nm for the ^{133}Cs D2 optical transition, while only occupying a few 100 μm^2 in individual size [3,20,21,23,24]. The components related to CPT such as the VCSEL, optics, and atomic sources are usually grouped together in what is referred to as a "physics package", shown in Fig. 1.3b, along with a small photo detector (PD) [25]. The components related to RF synthesis required for modulation of the VCSEL such as the microwave-frequency voltage controlled oscillator (VCO), phase-locked loop (PLL), voltage controlled quartz crystal oscillator (VCXO), and amplitude control circuits are grouped together and defined here as parts of the microwave local oscillator.

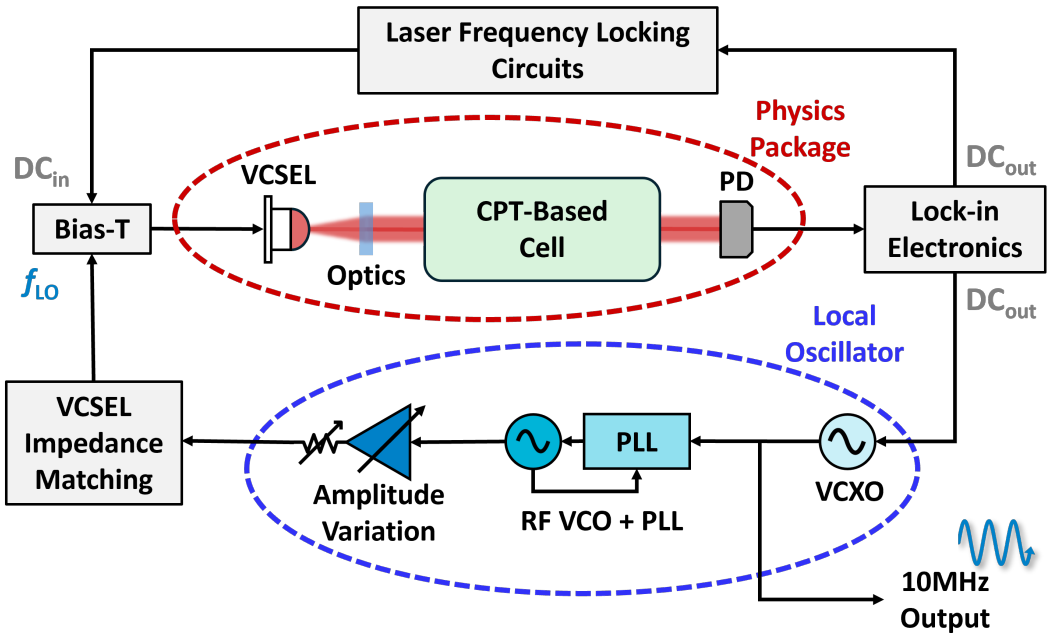
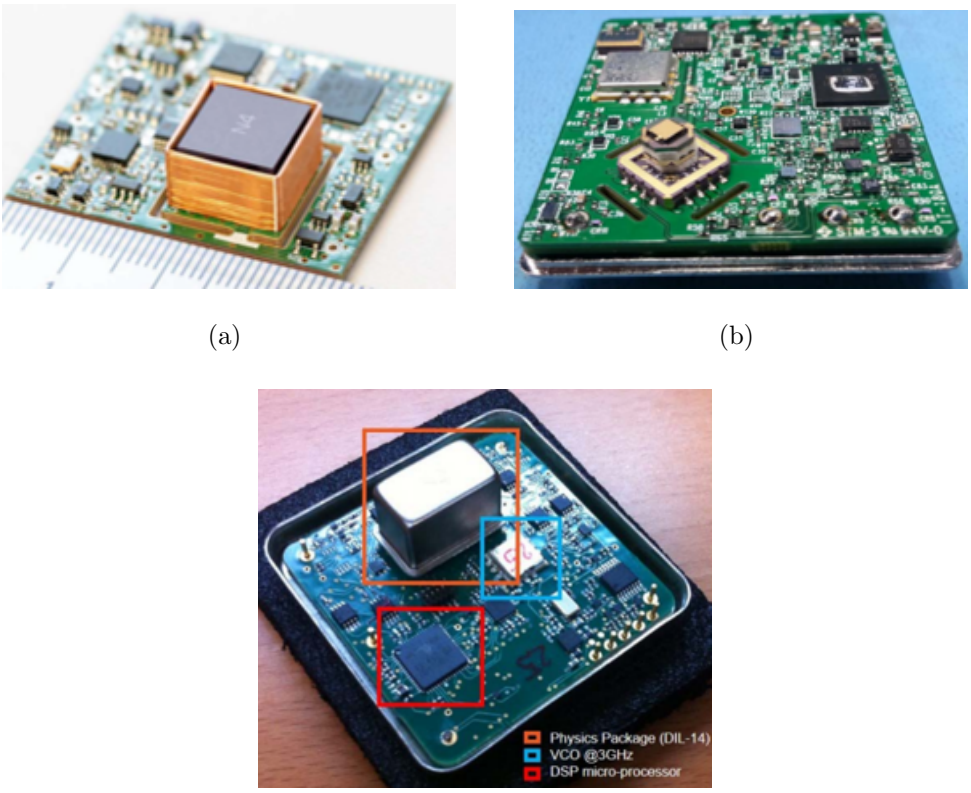


Figure 1.3: Block diagram of a generic chip-scale atomic clock (CSAC) based on coherent population trapping (CPT), highlighting different parts of the microwave-frequency synthesis chain. Here, the "physics package" is defined as circled in red, while the microwave local oscillator is circled in blue. Remaining abbreviations explained in main text.

Figure 1.4 shows a few photographs of published CSACs along with their corresponding volumes. On all of the pictured printed circuit boards (PCBs), the physics packages can be clearly identified as the taller, vertically-oriented structures mounted on the board. The remaining PCB area is populated with electronics related to dc power generation, control circuits, and the RF synthesizer chain. As of 2024, there are several commercial companies offering chip-scale atomic clock products such as Microchip [26], Teledyne [27], Taitien [28], and Safran [29].



(a) (b)

(c)

Figure 1.4: (a) Photo of the "ULPAC: Ultralow-Power Atomic Clock", a Cs CPT-based clock using an LO integrated in 65 nm CMOS, with a total P_{dc} =59.9 mW in a size of 15 cm^3 [30]. (b) Photo of the published chip-scale atomic clock "SA65s", a commercial Rb CPT-based clock from Microchip with a total P_{dc} =120 mW in a size of 17 cm^3 [31]. (c) Photo of the published "mRO^{TM}", a commercial miniaturized Rb clock from SAFRAN based on double resonance spectroscopy, with a total P_{dc} =350 mW in a size of 50 cm^3 [32].

The IEEE time-domain metric for an oscillator's frequency instability is defined as a two-sample deviation called the Allan deviation (ADEV), $\sigma_y(\tau)$ [33–35]. For example, the commercial Microchip "SA65" CSAC cites an ADEV of $\sigma_y = 3.0 \times 10^{-10}$ at a $\tau = 1$ s time interval [26]. This means that between two measurements separated by 1 second, there has been 0.003 Hz root mean square (RMS) of frequency deviation from the nominal 10 MHz output. Figure 1.5 shows a comparison of Allan deviations versus integration time for a few different physically compact

and relatively lower power frequency standards, including chip-scale atomic clocks, Rb vapor cells, oscillators based on microelectromechanical systems (MEMS), cesium beams, and hydrogen maser clocks. It can be seen in Fig. 1.5 that CSACs are still largely outperformed by larger and more power-hungry frequency standards by a few orders of magnitude, which limits their use to low-power applications that can still operate with less precise clocks. To address this issue, new architectures and advancements to existing CSACs are being developed [36–41], which show promise for better short-term ($\tau \sim 1$ s) and long-term ($\tau > 1000$ s) stability. As these new clocks gain stability improvements through either systematic refinement or new atomic interrogation schemes, they can become limited by low LO performance, and this must be addressed to further improve the overall frequency stability for future microwave CSACs. This will be further addressed in Chapter 2.

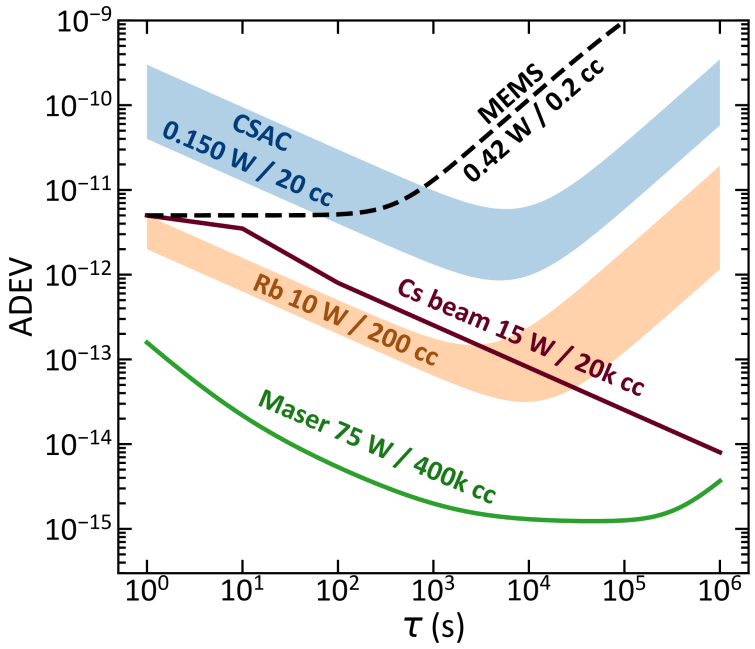


Figure 1.5: Comparison of common commercial atomic clock technologies. The clock performance (here shown as fractional frequency stability (ADEV) versus integration time τ) and drift rates generally improve as power consumption (W) and size (cm^3) increase. The shaded regions for CSACs and Rb vapor cell clock indicate the range of published performances. Recent advances in MEMS clocks are presented for context.

1.3 Introduction to Microwave Oscillators

Microwave oscillators, at their basic function, are nonlinear circuits acting as DC-to-AC converters. Oscillator circuits in general are often simplistically modeled using the feedback circuit shown in Fig. 1.6, where the output of an amplifier with a frequency dependent loop-gain $G(j\omega)$ passes through a feedback network with a frequency dependent transfer function $H(j\omega)$. The output (V_{out}) is then added back to the input (V_{in}) [42].

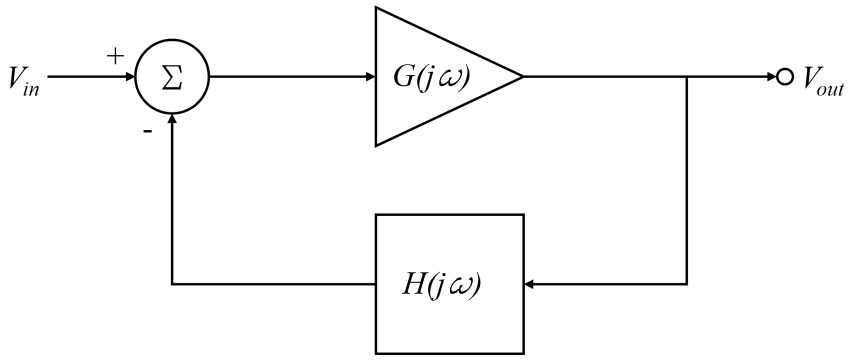


Figure 1.6: Block diagram of a simple oscillator model consisting of an amplifier with frequency dependent loop gain $G(j\omega)$ and a frequency dependent feedback circuit with transfer function $H(j\omega)$.

The output voltage is then given by:

$$V_{out} = \frac{V_{in}G(j\omega)}{1 + G(j\omega)H(j\omega)} \tag{1.1}$$

An important implication of Eqn. 1.1 is that if the denominator is equal to 0 at a specific frequency ω, the output voltage V_{out} becomes non-zero even with zero input voltage V_{in}. This condition is commonly referred to as the *Nyquist criterion* [43]. Another straightforward interpretation of the same model is if the loop-gain is unity, and the feedback circuit has a total phase shift of 180° at frequency ω, an oscillation at ω will occur. Voltage controlled oscillators (VCOs) exploit this same oscillation condition, with a voltage-tunable feedback dependent circuit for $H(j\omega)$,

allowing for control of the oscillator's output frequency. This idea has been explored for over a century to create a number of different oscillator circuits for use in applications such as wireless communications [44], radar [45], and atomic clocks [46].

Although this model is useful for understanding the basic causes of oscillation, it fails to capture the fact that practical oscillators fluctuate in frequency and in amplitude. These fluctuations are due to a combination of many noise sources, some of which include flicker, thermal, and shot noise. Generally, the output voltage of a practical oscillator can be formulated as [47]:

$$v_{out}(t) = V_{out}[1 + A(t)] \cdot cos[\omega_0 t + \theta(t)] \tag{1.2}$$

Where V_{out} is the maximum voltage swing and $A(t)$ and $\theta(t)$ represent fluctuations as functions of time for the amplitude and phase respectively. The real-world result of these formulated fluctuations is referred to as oscillator *phase noise*, which are random frequency domain fluctuations of a periodic signal. The phase noise power spectral density (PSD) $S_\varphi(f)$ is defined in units of rad^2/Hz, and is related to the commonly used single-sided phase noise $\mathcal{L}(f)$ in units of dBc/Hz by the relation $\mathcal{L}(f) = \frac{1}{2}S_\varphi(f)$. It is also worth noting that phase noise quantified in the frequency domain and the previously defined Allan deviation in the time domain are both measures of an oscillators instability, and can be calculated from one-another [35]. The practical consequences of such noise are relevant to nearly all fields listed previously that require the use of a precise oscillator [48]. The resulting effects of the microwave oscillator phase noise, specifically of interest to atomic clocks related to this thesis are described in detail in Chapter 2.

1.4 Conclusion

This chapter presents a brief explanation of atomic clocks and chip-scale atomic clocks based on the microwave transitions of alkali atoms. The practical use-cases of such clocks are presented as a motivation for research in CSACs, with a contrast to larger and more stable clocks. The common components for miniaturized clocks are shown and presented with real-world examples

manufactured by various institutions. Finally, a description of oscillators and oscillator stability is shown, providing an understanding of both time and frequency domain metrics which will be relevant for oscillator discussions in the following chapters.

Chapter 2

Oscillator Metrics for Chip-scale Atomic Clocks

In this chapter, we review how the performance of the microwave LO affects the overall clock metrics, including frequency stability, power consumption, and the phase noise of the clock output signal. First, it is important to understand how the stability of a free-running oscillator changes compared to the stability after locking to the atomic resonator. Figure 2.1 shows how the ADEV of a free-running oscillator is, somewhat surprisingly, typically better than that of the atoms at low integration times, but starts increasing after some time ($\tau = 10^2$ s in the example) due to random walk FM, frequency shifts, and other environmental shifts such as pressure, temperature, aging, etc. [49]. Conversely, the ADEV of the atoms is often initially worse than the free-running LO, and afterwards generally improves with some $\sqrt{\tau}$ dependence, providing orders of magnitude improvement over the free-running oscillator at long integration times. Based on these stability traces, for the most stable clock possible at short and long-term integration times, an appropriate lock time must be chosen to lock the LO to the atomic resonance line (t_{lock}) at the integration time at which it becomes more unstable than the atoms. This allows the system to take advantage of the best stability from the free running oscillator and the atoms.

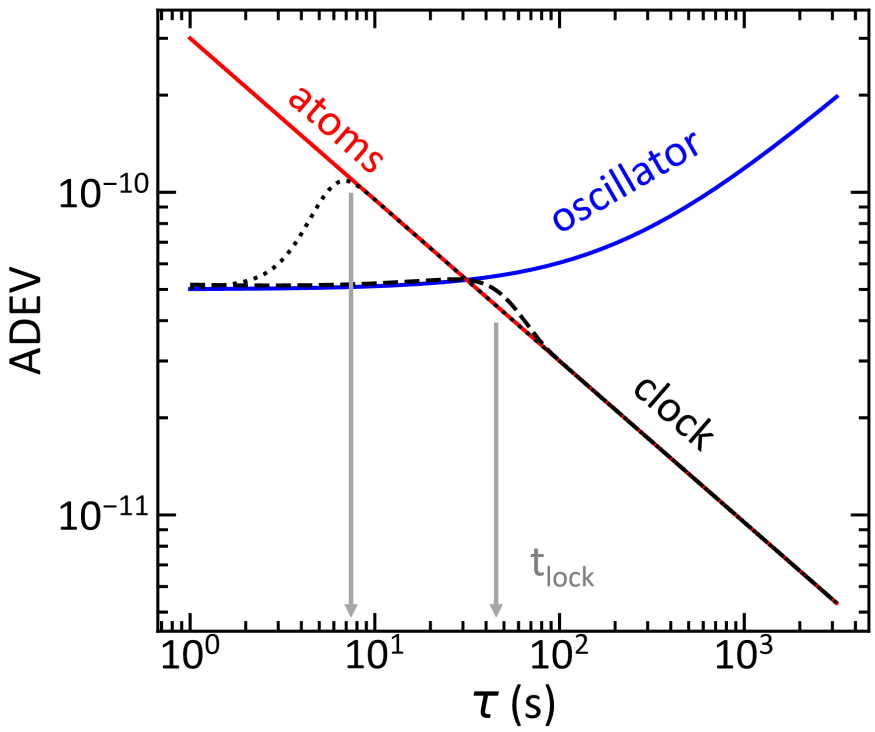


Figure 2.1: Example stability of a drifting oscillator disciplined by an atomic clock. Here, the oscillator (blue line) has good short-term stability but drifts at long integration times, and the atoms (red) have relatively poor short-term stability but do not drift. The integration time (t_{lock}) at which feedback acts on the oscillator can impact clock performance, as shown in the dotted (shorter t_{lock}) and dashed (longer t_{lock}) lines

.

Importantly, Fig. 2.1 also shows how the choice of t_{lock} can degrade the stability of the clock, even when using the same high-performance LO. In addition to frequency stability considerations stated here, figures of merit related to the LO such as size, power consumption, and output power are often at odds with each other, resulting in complex trade-offs for any LO design.

2.1 Effects of LO Phase Noise, Stability, and Modulation on Total Allan Deviation

Microwave oscillators can be simplistically modeled using an ideal gain element, such as an amplifier, connected to a resonant circuit which determines the oscillation frequency, ν_0 as shown previously in Chapter 1. Ideally, this oscillator operates as a DC-to-RF converter, producing an impulse function at a single frequency. In reality, oscillators exhibit spectral broadening in the form of phase noise due to circuit- and device-related noise sources. To first order, the phase noise of such a free-running microwave oscillator can be explained by the Leeson effect [50]. A well-known conclusion of Leeson's linear time-invariant (LTI) phase noise model is that an increase in the loaded resonator quality factor (Q_L) will provide a quadratic improvement in phase noise $\mathcal{L}(f)$ as:

$$\mathcal{L}(f) = 10\log_{10}\left[\frac{FkT}{2P_s}\left(1+\left(\frac{\nu_0}{2Q_L f}\right)^2\right)\left(1+\frac{f_c}{f}\right)\right] \tag{2.1}$$

Here $\mathcal{L}(f)$ is the single-sideband noise power spectral density (PSD) in dBc/Hz, which is related to the phase noise PSD S_φ in dB$\,rad^2$/Hz by $\mathcal{L}(f) = \frac{1}{2}S_\varphi(f)$, F is an empirical noise parameter of the device, k is Boltzmann's constant, T is temperature in Kelvin, P_s is the power dissipated in the resistive element of the resonator, ν_0 is the oscillation frequency, Q_L is the loaded Q factor of the resonator, f is the frequency offset from the carrier, and f_c is the flicker corner of the active device.

Many publications have shown that the phase noise of the LO at specific frequency offsets, related to the atomic interrogation scheme, can limit the clock's total frequency stability [12] [51]. The two major effects of LO phase noise that limit the achievable clock frequency stability are described by the "Dick effect", which is an aliasing effect for systems using pulsed interrogation schemes, and the "intermodulation effect" for continuous interrogation [51] [52]. These effects arise from a nonlinearity caused by the atomic resonator interrogation process, which exists in many types of passive frequency standards [53]. This nonlinearity causes frequency translation of spectral noise in the LO output into the frequency bands of the atomic resonator response. In

this chapter, we mainly focus on the intermodulation effect specific to continuous interrogation schemes, as these are more prevalent in the current literature on chip-scale clocks. The formulation of the intermodulation effect is dependent on the modulation frequency f_m, and type of modulation function $g(t)$ which is used to scan the atomic resonance line [54] [55]. The most commonly used sinusoidal and square-wave modulation functions are respectively given by:

$$g(t) = \begin{cases} m \cdot \sin(2\pi f_m t) & \text{for sinusoidal modulation} \\ m \cdot \mathrm{sgn}(\sin(2\pi f_m t)) & \text{for square-wave modulation} \end{cases} \tag{2.2}$$

where m is the modulation depth. The generic formulation and derivation of the intermodulation effect can be found in [12]. For the two common cases in Eq. 2.2, the limits on total clock frequency stability due to the phase noise power spectral density (PSD) of the LO output are given by:

$$\sigma_{yLO}(\tau) \approx \sqrt{\left(\frac{f_m}{\nu_0}\right)^2 \cdot \frac{S_\varphi(2f_m)}{4}} \cdot \tau^{-1/2} \tag{2.3}$$

$$\sigma_{yLO}(\tau) = \sqrt{\sum_{n=1}^{\infty} \left[\frac{f_m}{\nu_0} \cdot \frac{2n}{(2n-1)(2n+1)}\right]^2 S_\varphi(2nf_m)} \cdot \tau^{-1/2} \tag{2.4}$$

where σ_{yLO} is the limit on the total clock stability due to the LO evaluated at an integration time (τ), f_m is the LO modulation frequency, ν_0 is the fundamental RF frequency of the LO, and S_φ is the phase noise PSD of the LO output in $\mathrm{rad}^2/\mathrm{Hz}$, keeping in mind the commonly used phase noise $\mathcal{L}(f)$ in (dBc/Hz) is related by $\mathcal{L}(f) = \frac{1}{2}S_\varphi(f)$. Eq. 2.3 is for sinusoidal modulation and Eq. 2.4 is for square-wave modulation.

The intermodulation effect reviewed here requires a quasi-static assumption $f_m \ll \Delta f$, where Δf is the linewidth of the atomic reference line. For any atomic passive frequency standard, the choice of f_m has an upper bound determined by the width of the atomic reference line, and a lower bound determined by the $1/f$ noise in the detection system. Within these bounds, the f_m is typically chosen to minimize the effect of the LO phase noise on the total Allan deviation, determined either theoretically based on the equations above or experimentally for a specific clock.

As a theoretical example, applying Eq. 2.3 and using an arbitrary $f_m = 1\,\text{kHz}$, a short-term stability limit of $\sigma_y = 1 \times 10^{-12}$ at $\tau = 1$ hour can be achieved as long as the LO phase noise $\mathcal{L}(f)$ is below $-68\,\text{dBc/Hz}$ at a $2\,\text{kHz}$ offset from a $4.6\,\text{GHz}$ carrier frequency.

The effects of LO phase noise on clock stability for pulsed interrogation schemes, although not as popular in current CSACs, can be described by the Dick effect shown for convenience in Eq. 2.5:

$$\sigma_{yLO}(\tau) = \sqrt{\frac{1}{\nu_0^2}\sum_{n=1}^{\infty}\left[\frac{\sin\left(n\pi T/T_c\right)}{n\pi T/T_c}\right]^2 (2nf_s)^2 S_\varphi(2nf_s)} \cdot \tau^{-1/2} \tag{2.5}$$

where all other variables are the same as Eq. 3 and 4, with f_s being the sampling frequency and T/Tc being the dead time between cycles. Additional research on the Dick effect specific to pulsed CPT-based clocks can be found in [56].

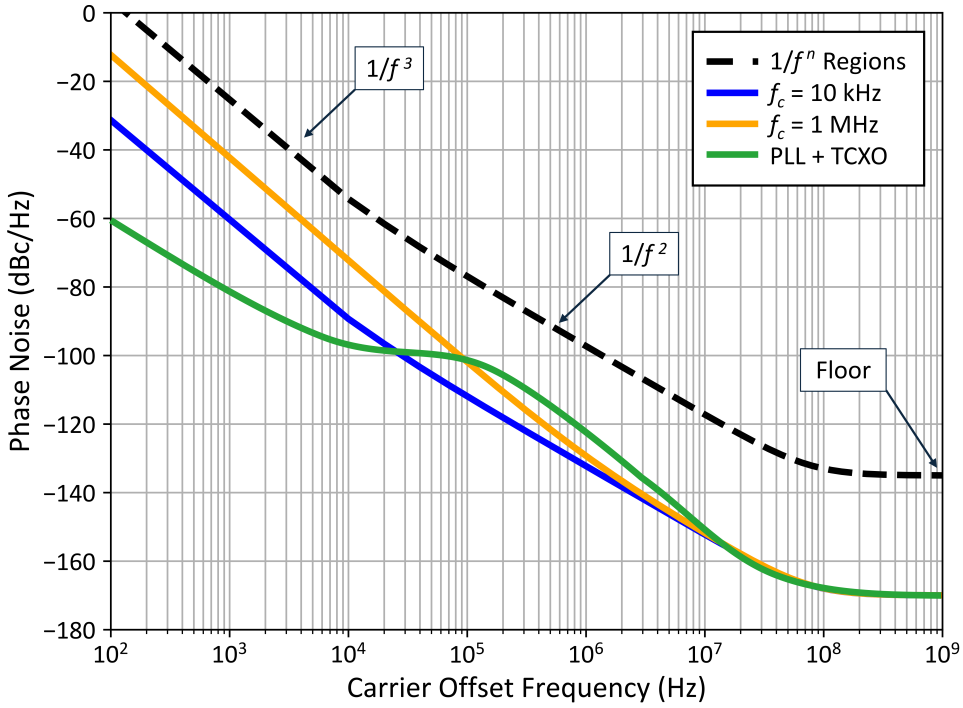


Figure 2.2: Qualitative phase noise $\mathcal{L}(f)$ profiles comparing two free-running 4.6 GHz microwave oscillators with different corner frequencies, where $f_c = 1$ MHz corresponds to the order of magnitude for HEMTs and FETs, while $f_c = 10$ kHz corresponds to oscillators with bipolar devices such as SiGe or InGaP/GaAs HBTs. The profiles are calculated using Leeson's equations. The dashed line indicates the $1/f^n$ regions as a guideline. The green curve is a qualitative profile for a PLL-stabilized oscillator using a quartz crystal. Other variables in Leeson's equations are kept the same for comparison (Q factor, RF power, carrier frequency, noise factor, temperature).

To help exemplify why these equations are important for determining the LO specifications, a sketch of some example phase noise profiles for a generic 4.6 GHz microwave LO are shown in Fig. 2.2. The dashed line corresponds to a phase noise profile of a free-running oscillator described using Leeson's equations which provide a useful model for the phase noise of an LO based on its Q-factor and flicker corner frequency [50]. The flicker corner frequency f_c tied to the inherent LO semiconductor properties separates the white phase noise from flicker phase noise and other progressively increasing noise slopes $(1/f, 1/f^2, 1/f^3, ...)$ at lower offset frequencies [57]. The two

other Leeson's phase noise profiles compare free-running microwave oscillators with different corner frequencies, where $f_c = 1\,\text{MHz}$ corresponds to the order of magnitude for high-electron-mobility transistor (HEMTs) and field effect transistor (FET) devices such as in CMOS or GaN technologies, while $f_c = 10\,\text{kHz}$ corresponds to oscillators with bipolar devices such as silicon bipolar, SiGe or InGaP/GaAs heterojunction bipolar transistors (HBTs) [58–60]. The green curve is a qualitative profile for a PLL-stabilized 4.6 GHz VCO locked to a relatively more stable 10 MHz quartz oscillator, reducing the phase noise at low frequency offsets below an arbitrary loop filter bandwidth of 10 kHz. This is highly relevant for improving the overall atomic clock stability, as generally offsets below about 10 kHz have a dominant effect on the stability performance, as explained previously.

On top of the intermodulation and Dick effects, the microwave LO also has a general stability requirement based on the low-offset phase noise. This requirement is typically for phase-noise offsets around 1 Hz, which corresponds to the ADEV at 1 s, and therefore one should consider if this limits the stability of the overall clock. Furthermore, low performing LOs can exhibit high temperature sensitivity or large phase-noise slopes below 100 Hz, which would make locking to an atomic cell difficult and possibly change the required locking bandwidth to the atoms.

For some practical published examples of how LO phase noise and modulation scheme can affect the total frequency stability in CPT-based vapor cell CSACs, the LO in [61] has a measured phase noise of $-85\,\text{dBc/Hz}$ at 2 kHz offset frequency and a corresponding measured Allan deviation for the clock of $\sigma_t = 5 \times 10^{-11}$ at 1 s when modulated with a square-wave modulation function of $f_m = 1\,\text{kHz}$. In [30] the phase noise $\mathcal{L}(f)$ of the VCO is $-62\,\text{dBc/Hz}$ at $2f_m$ and this gives a total short-term stability for the clock of $\sigma_t = 6.71 \times 10^{-11}$ at 1 s using a square-wave modulation function of $f_m = 71.4\,\text{Hz}$. Both LOs were implemented using integrated CMOS PLLs locked to a quartz VCXO, which consumed only 10-20 mW of dc power.

2.2 Effects of LO Output Power on Allan Deviation

In addition to LO phase noise, the LO RF output power can also limit the frequency stability of atomic clocks, depending on the architecture. In CPT-based atomic clocks, for instance,

frequency modulation of the VCSEL can induce light shifts that can degrade the overall frequency stability. Typically for these types of clocks, the LO modulates the VCSEL at either full or half of the ground-state hyperfine transition frequency for the atomic species. In the first case, the carrier and a first-order sideband are used to drive the targeted transition and the LO RF power controls the relative strength of the relevant optical fields. In the second case of the half-hyperfine frequency, two first-order sidebands separated by the full-hyperfine frequency drive the transition. In this case, the LO RF output power controls the power balance between the resonant and off-resonant optical fields. In both cases, frequency instability at the clock output can be generated through variation of the RF power [62, 63], and operational LO powers can be identified which reduce the clock sensitivity to overall optical power. Figure 2.3 shows an example of the optical frequency spectrum of the VCSEL for both modulation schemes, with the RF LO power controlling the strength of the relevant sidebands.

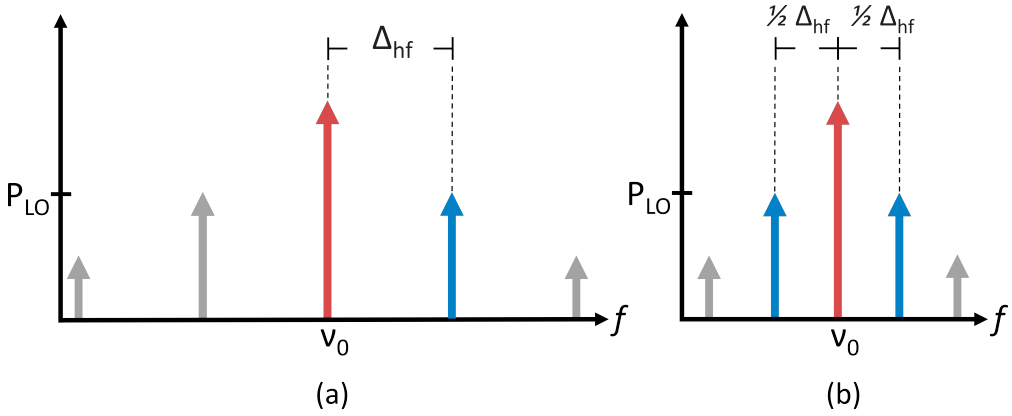


Figure 2.3: Sketch of the optical frequency spectrum of a VCSEL while being frequency modulated by a microwave LO in a CPT-based atomic interrogation scheme. P_{LO} is the RF output power of the LO which controls the relative strength of the optical sidebands. (a) Sketch of the optical carrier and first-order sideband separated by the full-hyperfine transition frequency and (b) two first-order sidebands each separated by half of the hyperfine frequency.

The specific values of these powers are subject to each individual atomic interrogation scheme,

but are often on the order of -5 to 10 dBm of RF power for CPT-based CSACs using VCSELs [3]. In summary, the atomic interrogation process requires variable RF output power control *and* output power stability, which can be done in numerous ways, such as VCO supply modulation, buffer-amplifier supply modulation, or controllable attenuators and is discussed in Chapter 4.

2.3 Effect of LO on Total Clock DC Power Consumption

Another figure of merit especially important for the low SWAP-C applications of small atomic clocks, differing from their physically larger more frequency-stable counterparts, is the total dc power consumption (P_{dc}). A significant percentage of this total power is often dedicated to the LO chain used to generate the atomic interrogation signal. Figure 2.4 shows the P_{dc} for a few integrated microwave LOs compared to the total P_{dc} of their respective clock systems. For instance, in [30] the microwave LO and driving circuits account for $\approx 23.5\,\%$ of the total P_{dc} (59.9 mW), with over 11.2 mW for the LO/driver and an additional 2.9 mW for the VCXO in the PLL. In [64], the prototype clock system consumes 42 mW (without vacuum and heating circuits), with the LO chain consuming $> 50\%$ of the total power (26 mW). In most CSAC implementations, the peak power consumption for the microwave LO is dictated by the RF output power requirements for the optimal optical sideband power in that respective system, which sometimes require additional high-power amplifier stages to reach.

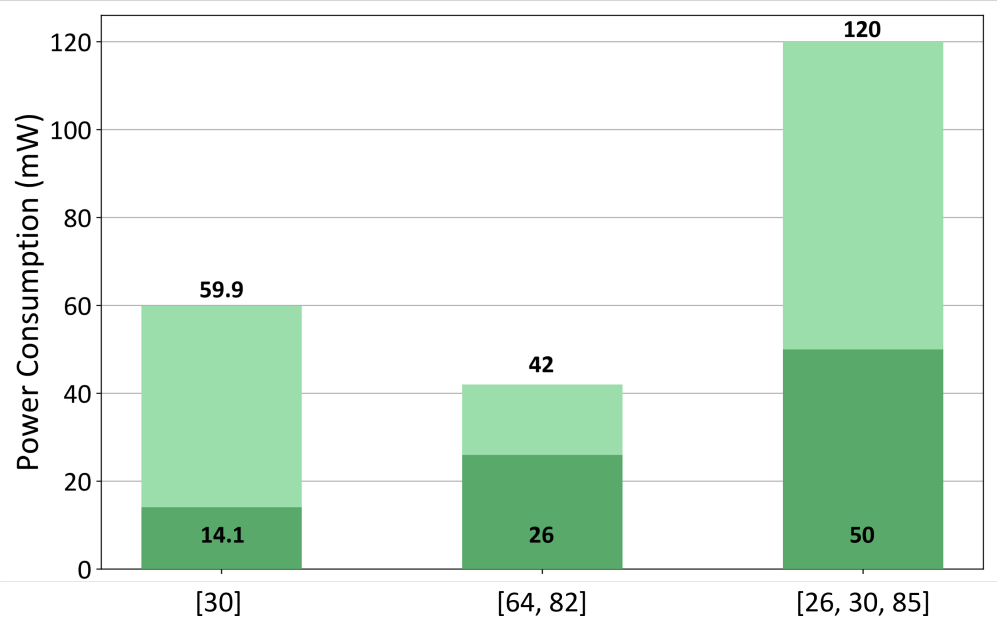


Figure 2.4: Comparison of LO and total clock P_{dc} (in bold) for three integrated clock systems in literature. [30] does not distinguish between locking circuits and VCO. [64] does not include P_{dc} related to heating and vacuum systems.

Since RF oscillators usually consume more power (higher current) for lower phase noise, and there is a trade-off between phase noise and conversion efficiency, it is difficult to reduce the LO power consumption below a few mW without sacrificing stability [65]. Efforts have been made to reduce the power consumption from the LO to the furthest extent while maintaining high performance. These include operating the RF VCO in different modes [30], improved VCO circuit architectures [66] new types of high-Q RF resonators [67], new heterogeneous packaging technologies [68], and improvements to the power consumption of PLL circuits, all of which are discussed in Chapter 4.

2.4 Servo Electronics

As explained earlier, the main feedback loop in microwave atomic clocks consists of a RF LO whose output frequency is tuned near the targeted atomic transition frequency, causing the power

transmitted through an atomic cell to change. Using CPT-based clocks as an example, the optical power of the VCSEL modulated by a LO is incident on a photodetector whose output voltage is used to create a feedback signal for the LO to change its output frequency, in what is called a frequency-locked loop (FLL). This is the main servo loop used to discipline the LO to the targeted hyperfine transition, in turn creating a relatively long-term stable oscillator. To create this FLL, usually a number of additional control loops are used: a wavelength-locked loop (WLL) which locks the VCSEL optical wavelength to the appropriate optical atomic transition; a second loop to maintain the appropriate VCSEL and atomic cell temperatures; another loop to control the RF LO power incident on the VCSEL; and finally a phase-locked loop (PLL) to further stabilize the RF VCO and provide a 10 MHz clock output often using a quartz crystal oscillator. The electronics required for these feedback loops are frequently combined in a single application-specific integrated circuit (ASIC) which allows for increased efficiency in a very small footprint. Due to the desire for a high level of integration of all electronics required for a CSAC, including the RF LO, it is worthwhile to briefly discuss how each of these servo loops impact the electronics design as a whole. Significant progress in miniaturizing these electronic control circuits has been shown in recent years, including a number of commercial products [26–28].

The design of a WLL primarily involves controlling the output wavelength of a VCSEL by adjusting its drive current, which proportionally tunes its wavelength as long as the temperature is stabilized. Using the drive current as a control knob, the optical wavelength can be locked to a point corresponding to maximum absorption through the atomic cell. To detect this operating point, the dc drive current of the VCSEL is swept in combination with a small ac modulation current that produces two measurement values from the photodetector. The signal can then be demodulated by mixing it with the same AC frequency, generating an error signal. This error signal can then be minimized by adjusting the DC current - incrementing it if the error signal is positive, or decrementing it if the error signal is negative.

An example block diagram of a WLL is shown in the bottom section of Fig. 2.5. The sensitivity of a typical VCSEL's optical frequency to changes in bias current is around $\approx 200\,\mathrm{GHz/mA}$,

while the linewidth of a collisionally-broadened optical resonance in a microfabricated vapor cell is on the order of $\approx 1\,\mathrm{GHz}$ [69]. It's of critical importance that the WLL must be able to lock the VCSEL frequency within the linewidth of the optical resonance. A current source with low noise and minimum current steps on the order of a few nA is required to achieve a symmetric lock to the resonant frequency. Such current sources have been realized by using a reference current generator, where the voltage reference is replaced by a digitally controllable voltage source, such as a resistive DAC (R-DAC) [70, 71], or by programming the reference resistor [72, 73]. R-DACs are known to suffer from process, voltage and temperature variations, which must be accounted for using trimming or calibration. An alternative approach is to generate a temperature stabilized reference current [74, 75] and mirror the current using a programmable current bank [30]. Noise in the current source, particularly low-frequency flicker noise, can be controlled by sizing of the transistors. Sensitivity to power supply variations can be controlled by increasing the impedance of the current sources through cascoding.

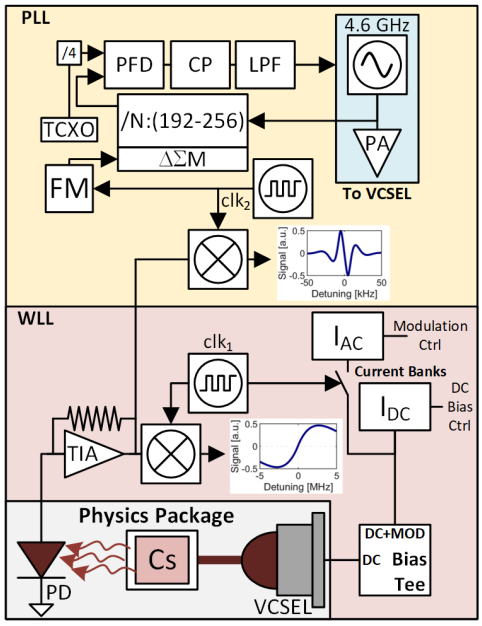


Figure 2.5: Block diagram schematic showing the WLL and the PLL forming servos to control the physics package in a CPT-based chip-scale atomic clock.

Use of PLLs in CSACs provides two major benefits for the RF LO: one by providing a means to have a 10 MHz output as to interface with other systems, and second in the improved phase noise of the RF VCO below the PLL loop filter bandwidth where the phase noise is most relevant. Often, the frequency control of the LO used in the FLL is tightly integrated within the digital electronics of the PLL, and this can help dictate which PLL architecture is best. For example, due to the relatively narrow width of the atomic response being tuned over in CPT-based CSACs, a frequency resolution of only a few mHz is needed [30]. To achieve this level resolution, a fractional-N PLL is commonly used, and since there are no practical frequency references that operate down to a few mHz, integer-N PLLs become impractical. An example of a fractional-N PLL is shown in the upper portion of Fig. 2.5 [76]. In most PLL designs, a frequency reference with good short-term stability, such as a temperature compensated crystal oscillator (TCXO), is input to the PLL consisting of a phase-frequency detector (PFD), a charge-pump (CP), a loop-filter (LF), a voltage-controlled oscillator (VCO) and a divider controlled by a $\Delta\Sigma$-modulator. In the PLL example shown, the fractional division ratio is realized by dithering between two (or more) integer division ratios (e.g., $M = 229$ and $P = 230$) to realize an effective division ratio (e.g., $N = 229.81579425$) that is between M and P. The $\Delta\Sigma$-modulator shapes the frequency error with a high-pass response. In terms of phase noise, the PLL has a low-pass response for noise from the divider of the PFD, and a high-pass response for noise from the VCO where the cut-off frequency is set by the loop filter bandwidth. When optimizing the loop bandwidth of the PLL, there is an optimal bandwidth where noise contributions from the VCO, the $\Delta\Sigma$ and the frequency reference are balanced [77]. In a fractional-N PLL, the reference noise tends to dominate at low frequencies, while the $\Delta\Sigma$-modulator noise and VCO noise dominate at higher frequencies. In terms of control, the frequency resolution of a fractional-N PLL is determined by the number of bits in the $\Delta\Sigma$-modulator where the number of bits, K, is given by:

$$K = \log_2\left[\frac{f_{\text{ref}}}{f_{\text{step}}}\right] \tag{2.6}$$

where f_{ref} is the frequency of the reference oscillator and f_{step} is the required frequency resolution.

Finally, in the FLL servo loop used to lock to the atomic response, the VCO frequency needs to be modulated at some frequency f_m before it is applied to the VCSEL. Similar to the mechanism for the WLL, the measurement of two signals that can be demodulated by mixing the recovered signal with the same frequency is used to create an error signal. This error signal can be minimized by incrementing the VCO frequency by changing the divider ratio or the reference frequency by tuning it with a varactor, which is often built-in.

2.5 Effects of LO on Clock Output Phase Noise

While ADEV is the central metric for representing a clock's stability in the time domain, it can be useful to examine the same stability in the frequency domain by looking at the phase noise of the final clock output. The output frequencies for clocks are routinely selected to be 10 or 100 MHz to be compatible with most external electronics, much lower than the microwave atom transition frequency of the atomic species used in CSACs. To facilitate this lower frequency output, the signal is regularly taken directly from the TCXO or oven controlled crystal oscillator (OCXO) within the PLL of the microwave LO. Alternatively, the RF VCO operating at the atom transition frequency can be used as the output [14], with additional frequency division circuits to resolve the lower frequency.

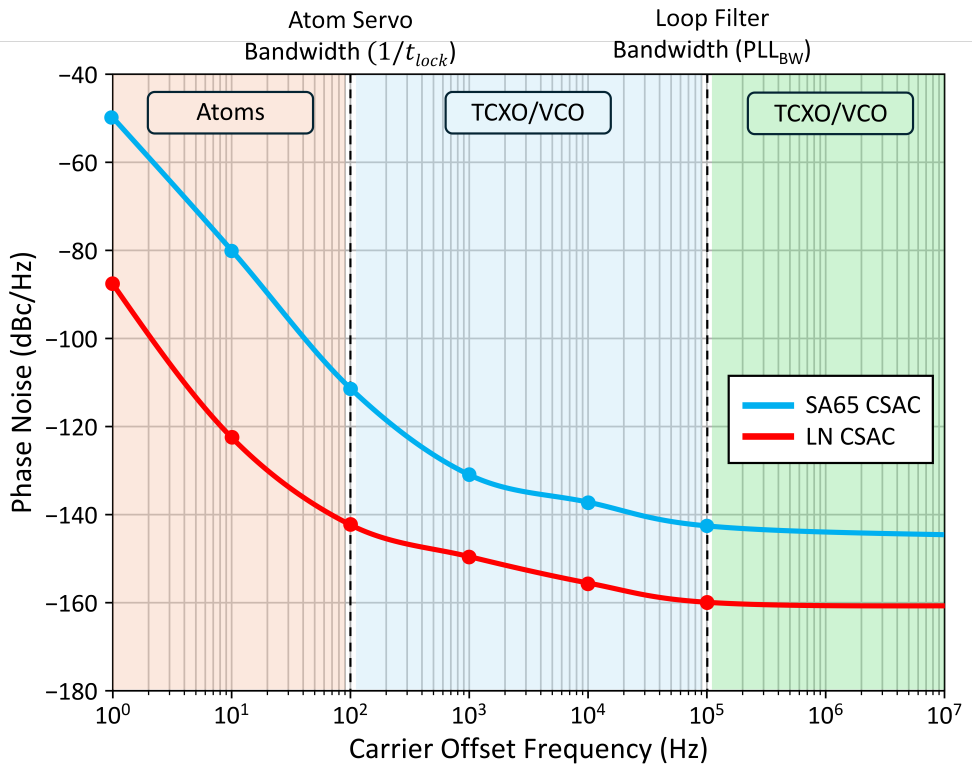


Figure 2.6: Phase noise $\mathcal{L}(f)$ of the final 10 MHz output for the "SA65" and "Low-Noise" CSACs commercially available from Microchip [26,78]. The three colored regions illustrate how phase noise is dominated by different sources: the atoms, TCXO/OCXO and/or VCO. At low offsets, below the atom servo bandwidth, the phase noise is dominated by the stability of the physics package. At higher frequency offsets, the phase noise is dominated by either the TCXO/OCXO or VCO, depending on which is used for the clock output.

Figure 2.6 shows the phase noise $\mathcal{L}(f)$ of the 10 MHz output signals for the "SA65" and "Low-Noise (LN)" CSACs commercially available from Microchip [26, 78]. In both clocks, the output signal is taken from the quartz crystal oscillator used in the internal PLL, removing the need for additional frequency division circuits. The improved phase noise for the LN-CSAC comes from the use of an OCXO in the PLL compared to the traditional TCXO used in the "SA65", improving the phase noise for a small size and power consumption increase [79]. The shaded regions show how the noise at the different frequency offsets is determined to first-order by the atomic stability of the physics package (red) and the TCXO/VCO stability (blue/green). The regions in this frequency-

domain plot are analogous to the regions in Fig. 2.1, represented in time domain. The width of the region dominated by the atoms is determined by $1/t_{lock}$, the chosen attack time of the servo loop that stabilizes the LO to the atoms. A distinction between the two TCXO/VCO regions in blue and green at a frequency equal to the PLL loop filter bandwidth is shown to represent how the phase noise profile of the clock output can change based on where in the microwave LO the output is taken. For example, if instead a RF VCO within a PLL is used as clock output instead of a TCXO/OCXO, the clock output phase noise will be determined by the noise properties of the VCO disciplined with the PLL. This could result in a reduction of the higher offset phase noise beyond the loop filter bandwidth compared to the TCXO/OCXO example in Fig. 2.6, due to the improved phase noise at high frequency offsets of the RF VCO relative to the TCXO/OCXO, with similar shape to the "PLL+TCXO" line shown previously in Fig. 2.2. Some laboratory CSACs discussed in later sections do this and instead use the RF VCO alone as the output, with no PLL or TCXO, and externally stabilize the RF resonator to achieve the required stability.

2.6 Conclusion

This chapter presents an comprehensive review of how the microwave local oscillator commonly used in chip scale atomic clocks impacts the overall clock metrics, including the frequency stability, dc power consumption, and phase noise of the clock output signal. By reviewing the conceptual operation of CPT-based CSACs and how the effects of the microwave local oscillator are quantified, this chapter provides a concise foundation for discussion of microwave LOs for CSACs in future chapters. The work discussed throughout this chapter is originally reported in our review paper [80].

Chapter 3

State-of-the-art for Oscillators in Chip-scale Atomic Clocks

The first LOs for CSACs in the 2000's were designed on PCBs using discrete silicon bipolar transistors on physically large substrates, taking up areas on the order of ($> 1\,\mathrm{cm}^2$) [81]. This allowed for the use of high-Q resonators that could be integrated on substrate such as ceramic coaxial resonators, further improving LO phase noise. In the last 10 years, the state-of-the-art for LOs in CSACs have been dominated by integrated circuit (IC) implementations in CMOS or SiGe BiCMOS, using on-chip resonators as a means to save power and volume [61].

Some important distinctions come from reviewing Table 5.1, especially when looking at the relative power consumption and size of each of the LOs related to the chosen technology for fabrication and RF resonator type used. Most of the compact, highly integrated systems are all achieved in CMOS technologies using on-chip LC resonators (Q_u <40), phase locked to VCXOs using an integrated PLL. These CMOS-based clocks represent the state of the art in terms of trade-offs between size and power consumption while maintaining decent short and long-term stability. Also seen from the table, other avenues show promise in further reducing LO power consumption metrics through the use of high-Q RF resonators (Q from 300-1000s), eliminating the use of PLLs or VCXOs and therefore the dc power required to operate them. While promising, these oscillators still have engineering challenges that must be addressed before integration into a full commercial CSAC is possible, namely shifts in RF frequency caused by temperature and vibration. These topics among others related to the design of the LOs themselves will be discussed.

Physically large LOs bigger than a few square centimeters or power hungry synthesizers

Table 3.1: Comparison of Published RF LOs and ADEVs for Small, Low-power Microwave Clocks

LO Freq. (GHz)	**RF P_{out} (dBm)**	**P_{DC} (mW)**	**Phase Noise (dBc/Hz@Hz)**	**Volume (mm^3)**	**Tech.**	**Lock Type / Resonator**	**FoM_C @1 kHz (dBc/Hz)**	**σ_y @ 10^0s ($\times 10^{-11}$)**	**σ_y @ 10^3s ($\times 10^{-11}$)**	**σ_y @ 10^5s ($\times 10^{-12}$)**	**Ref.**
4.6	-8 to 6	14.1	-62 @150	1.5x1.7x0.3	65-nm CMOS	PLL / LC	*-212.7	6.7	0.8	2.2	[30]
4.6	-10 to 0	12	-85 @2000	0.7x0.7x0.3	130-nm CMOS	PLL / LC	-226	5	0.8	N/A	[61, 82]
3.4	0 to 10	26	-70 @150	2.1x2.3x0.3	0.18-μm CMOS	PLL / LC	-229.9	6	*2.5	30	[64, 83]
4.6	-6 to -1	8.3	-40@1000	1.6x1.6x0.3	0.13-μm SiGe BiCMOS	PLL / LC	-188.4	*8.5	N/A	N/A	[84]
4.6	-10 to 0	*50	-75@1000	*4x4x0.3	N/A	PLL / LC	*-225.2	30	1	*320	[26, 30, 85]
3.4	*-15	9	-50 @1000	1x0.6x0.3	65-nm CMOS	None / FBAR	-210.2	2.1	N/A	N/A	[68, 86]
$^{\diamond}$231	*-9.6	71	-65 @222 k	1.25x4x0.3	65-nm CMOS	PLL / LC	*235.4	5.4	*6.5	N/A	[87, 88]
4.6	-3	10	-53 @300	*10x10x2	Discrete Si-BJT	None / FBAR	N/A	N/A	N/A	N/A	† [89]
3.4	-5	2.8	-33 @100	7x7x2	Discrete Si-BJT	None / Coax	-203.2	24	N/A	N/A	[81, 90]
3.4	*-0.7	15	-70 @150	10x10x0.2	Discrete	Inj. Lock / LC	*-235.8	10	1	N/A	[91]
4.6	3 to 10	$> 1k$	-105 @1000	N/A	N/A	None / HBAR	N/A	6.6	2	N/A	[92, 93]
3.4	N/A	*140	N/A	36x23x10	Discrete	PLL / LC	N/A	3.66	1.65	N/A	[94, 95]
3	N/A	N/A	N/A	N/A	Discrete	PLL / LC	N/A	4	*1	*5	[29, 32]
4.6	N/A	60	N/A	<2000	N/A	PLL / LC	N/A	16	*0.55	*5	[14]
3.4	-15.3	3.2	-67 @300	N/A	Discrete Si-BJT	None / HBAR	-241	N/A	N/A	N/A	† [96]

* Represents Estimated Value Based on Figures — † Not tested with a physics package — $^{\diamond}$ Sub-THz Molecular Clock ($^{16}O\,^{12}C\,^{32}S$)

consuming >100 mW are not listed in this table as they are not optimized for the topic of CSACs, with the exception of [92, 93] in Table 5.1 which is more focused on the miniaturization of the RF resonator. Beyond this list, there remain many promising alternative ways to generate clean and stable RF frequencies in this range, but they are currently too complex, large, or power-hungry to be implemented in CSACs. Some examples of these alternatives include down-conversion to RF using optical combs [97, 98], multiplication to RF from more stable low frequency sources using nonlinear transmission lines (NLTLs) or step recovery diodes (SRDs) [6, 99–104], sampling mixers used to phase lock dielectric resonator oscillators [105], optically stabilized RF oscillators [106–108], and oscillators involving extremely high-Q resonators cooled to cryogenic temperatures [109–111]. Depending on future advancements in these fields of research, some of these methods may become viable for use in a next-generation small, low-power microwave clock.

Table 5.1 presents a performance comparison between local oscillators used in published microwave chip-scale clocks. With the exception of [87, 88] and [32], all use CPT-based interrogation schemes, at a sub-harmonic of the half-hyperfine splitting frequencies for ^{133}Cs or ^{87}Rb atoms which are around 4.596 and 3.417 GHz, respectively. The types of microwave resonators used in the RF VCO designs range from traditional on-chip inductor and capacitor implementations (LC), to external resonators such as quarter-wave ceramic-coaxial resonators or thin-film acoustic MEMS resonators. The latter include Thin-film Bulk Acoustic Resonators (FBAR) and High-Overtone Bulk Acoustic Resonators (HBAR). Many of these LOs are designed using RF VCOs at the half-hyperfine frequency within a PLL, phase locked to a more stable VCXO in the MHz range. The PLL loop-filter improves the LO's close-offset phase noise and short term stability, at a small cost of power consumption and size. All of the listed figures of merit in Table 5.1 are presented factoring in the entire synthesis chain, including any quartz oscillators, digital circuits, or later amplifier gain stages used in the RF synthesis process. Also in Table 5.1 is a list of the measured ADEVs for the complete atomic clock systems at increasing time scales. Comparing these listed ADEVs with the long-term stability of the best OCXOs, CSACs have been shown to have better long-term performance even among rapid temperature changes [112]. However, OCXOs still maintain advantages

over CSACs in both phase noise and short-term stability [113].

3.1 RF LOs for Better Clocks

In typical CMOS or SiGe VCO literature, a figure-of-merit (FoM) is used for performance comparisons between designs, factoring in fundamental frequency, phase noise at 1 MHz offset, tuning bandwidth, and DC power consumption [114] [115]. Similarly, VCOs in III-V semiconductors often use a FoM which accounts for fundamental frequency, phase noise at 1 MHz offset, tuning bandwidth, and output power or efficiency [116, 117]. Most of these FoM's are not as useful for comparisons between VCOs designed for CSACs because they are usually meant to describe utility in communications or radar systems where wide tuning bandwidths and low phase noise at higher frequency offsets are crucial. In contrast to communication systems, wide VCO tuning ranges and high tuning gains (Hz/V) are not desired in CSACs due to the relatively small target frequency tuning range of the atomic resonator response, which often on the order of <10 kHz. Instead of wide tuning bandwidths, VCOs for CSACs target low phase noise at lower frequency offsets (<20 kHz), much lower than the commonly cited 1 MHz offset used in the aforementioned FoM's. Additionally, the typical output power requirements of physics packages discussed in Chapter 3 require a LO output power on the order of -5 to 10 dBm to ensure the lowest instability is achieved when modulating the VCSEL. Therefore, for a given RF output power determined by the physics package, there should be a major importance placed on the overall efficiency of the RF synthesis chain, including subsequent amplification and locking circuits. These complex requirements for properly modulating the VCSEL along with the tight volume restrictions necessitate a slightly more specialized VCO design than can be achieved from commercial off-the-shelf (COTS) systems.

Based on the discussion above, an appropriate FoM for CSACs favors higher RF output power, lower dc power consumption and lower phase noise at a low offset frequency. Therefore, we choose to adopt a FoM similar to FoM_2 from [117], using a relatively low offset frequency of 1 kHz:

$$FoM_C = \mathcal{L}(f_{\text{offset}}) - 20\log\left(\frac{f_{\text{osc}}}{f_{\text{offset}}}\right) + 10\log\left(\frac{P_{\text{out}}}{P_{\text{diss}}}\right) \tag{3.1}$$

where $\mathcal{L}(f_{\text{offset}})$ is the phase noise in dBc/Hz at the specified offset of 1 kHz, f_{osc} is the LO output frequency in Hz, f_{offset} is the specified 1 kHz frequency offset, P_{out} is the RF LO output power in W, and P_{diss} is the total dissipated dc power in W. Each of the FoM entries in Table 5.1 are calculated using this equation.

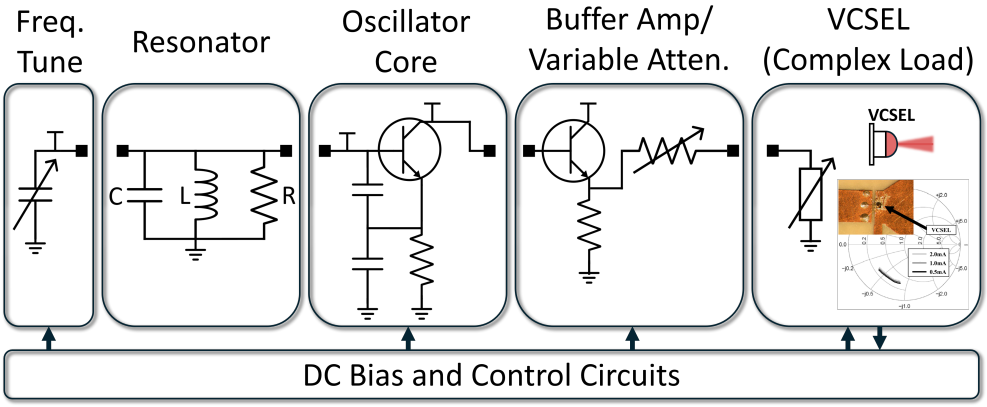


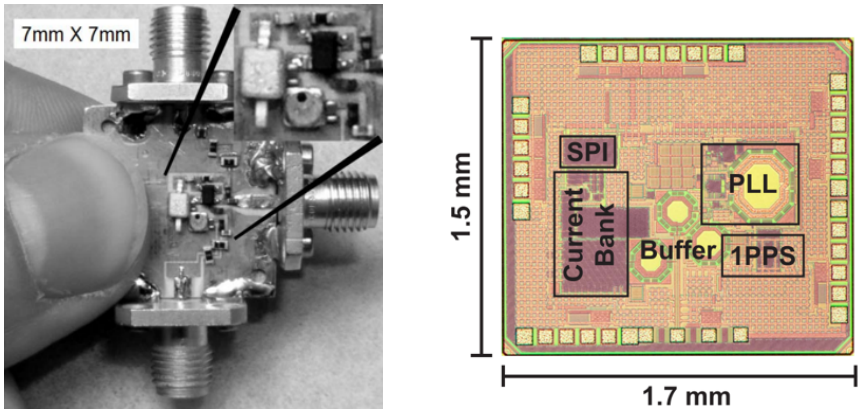
Figure 3.1: Block diagram of a generic RF Colpitts VCO using an LC resonant tank for determining the resonance frequency, tunable capacitance via a varactor diode for frequency tuning, transistor with feedback for the oscillator core, buffer amplifier/attenuator for amplitude control and output load pull isolation, and finally the VCSEL which is a bias and temperature dependent load [118]. The rest of the power, control, and feedback circuits are abstractly represented below.

Fig. 3.1 shows a block diagram of a generic microwave LC oscillator driving and modulating the injection current of the VCSEL required for creating optical sidebands at the hyperfine frequency of the interrogated atoms in a CPT-based cell. The VCSEL impedance at microwave frequencies is usually complex and can often be a function of temperature and bias current [119]. Impedance matching and coupling the RF VCO to the complex impedance of the VCSEL is a critical step to achieving a low loss interconnect that compensates for any packaging parasitics of the semiconductor laser, provides a bias-T for DC bias to the laser, and thermally isolates the VCSEL from the

oscillator [61].

3.1.1 Technology and Integration

Choice of technology for LO design is critical due to its effects on nearly all LO performance metrics and integration with other clock components. In early CSACs, LOs were implemented in low-cost hybrid technologies on large PCB substrates, often using discrete silicon bipolar transistors due to their low $1/f$ noise and moderate size, e.g. [90]. Since then, most LOs for state-of-the-art CSACs have been implemented in integrated circuits (ICs) using CMOS or SiGe BiCMOS due to their ease of integration with digital control circuits while maintaining reasonable RF performance, as shown in Table 5.1.



(a) (b)

Figure 3.2: (a) PCB photograph of a VCO developed for the first CSAC at NIST, implemented on a Rogers substrate with discrete silicon bipolar transistors and a high-Q ceramic coaxial resonator, consuming a few mW of a dc power in a $7\,\mathrm{mm}^2$ area [90]. (b) Die photograph of a LO developed for a state-of-the-art CSAC called the "ULPAC", integrated on-chip in CMOS taking up less than $1.7\,\mathrm{mm}^2$ in area [30]

Comparison studies on measured $1/f$ noise in different transistors for ICs and III-V monolithic microwave integrated circuits (MMICs) have shown that heterojunction bipolar transistors (HBTs)

achieve the lowest phase noise at fundamental frequencies relevant to miniaturized clocks [120, 121]. Of the commercially available options, SiGe HBT/BiCMOS [122, 123] and InGaP/GaAs HBT [124] become attractive options for the design of low phase noise VCOs, with SiGe having the additional advantage of easier integration with CMOS. Due to the output power requirements (-5 to $+10$ dBm), a relatively higher breakdown-voltage semiconductor such as InGaP/GaAs HBT provides an advantage as it does not require subsequent gain stages which consume power and could possibly contribute to the additive (residual) phase noise. This comes at the cost of generally higher power consumption for the VCO individually and more complex integration [125,126]. Nonetheless, CMOS and SiGe BiCMOS technologies have been used to produce the lowest power commercially available CSACs because of the large importance of integration.

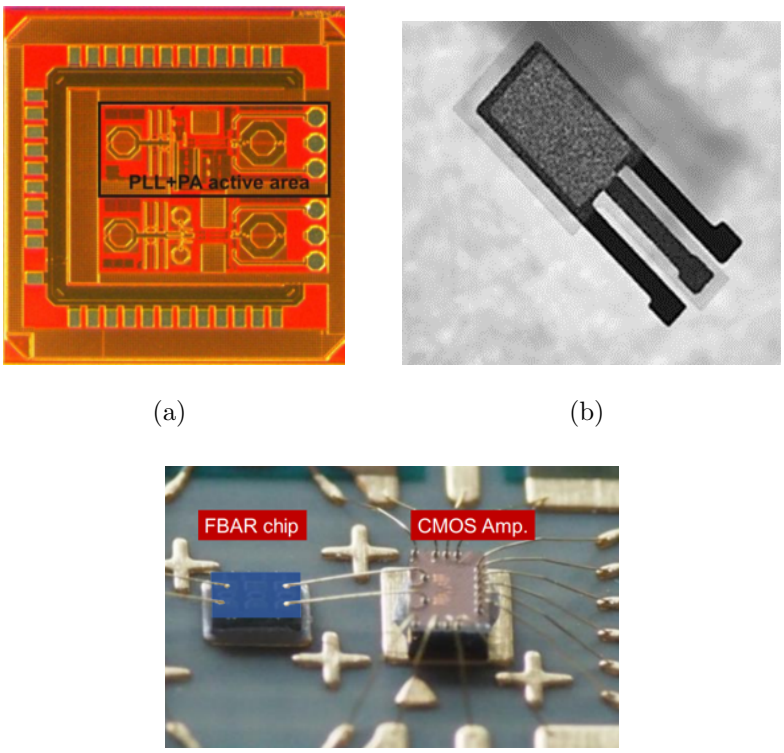
Figure 3.2 shows two examples of oscillators designed for use in CSACs. Figure 3.2a shows a prototype from the earliest CSACs developed at NIST, designed using a ceramic coaxial resonator with $Q \approx 300$ and tested without a PLL. Figure 3.2b is a fully integrated IC in CMOS representing an example of the current state of the art, and contains an LC oscillator, PLL, and buffer amplifier on-chip. Both VCOs locked to a miniaturized physics package resulting in a highly stable and small atomic clock, with the corresponding measured ADEVs listed in Table 5.1.

3.1.2 Phase Noise, Free-running Stability, and RF Resonators

The design of low phase noise RF oscillators has been the subject of many books, papers, and theses throughout the years, resulting in a number of different noise theories with experiments to match [42, 48, 127, 128]. For CSACs, having a LO with good free-running stability and phase noise as described in previous chapters is imperative for improving the overall clock stability. This free-running phase noise of the LO is largely determined by a combination of the RF resonator Q_L, the technology choice as described earlier, as well the chosen circuit topology.

As stated previously in Chapter 3, Leeson's LTI model in Eq. 2.1 is sufficient for discussing the impact of RF resonator Q on VCO phase noise to first order. While it is tempting to maximize the resonator Q at all costs, this desire can often contradicts with system SWAP-C requirements due

to an RF resonators relationship to its wavelength [129]. Furthermore, most systems require some tuning range which is often achieved with lossy on-chip varactor diodes, decreasing the realistically achievable Q [130].



(a) (b)

(c)

Figure 3.3: (a) Die Photograph (0.7mm^2) of a fully integrated 4.6 GHz LO in CMOS for a CSAC including a VCO using an on-chip LC resonator, PLL, and Power Amplifier (PA). LC resonators in CMOS typically have an unloaded Q of Q_u <40 [61]. (b) Photograph of an HBAR resonator ($< 1\,\text{mm}^2$) with Q_u=19000 used in a hybrid CSAC prototype oscillator [96]. (c) Photograph of an FBAR resonator ($< 1 \times 0.67\,\text{mm}^2$) with a Q_u=1100 integrated with a CMOS oscillator for use in a low power PLL-free CSAC [68].

Fig. 3.3 shows a few examples of small RF resonators used in VCOs for published CSACs including an integrated LC resonator, a film bulk acoustic wave resonator (FBAR), and a high-overtone bulk acoustic resonator (HBAR). Of these examples, LC and microstrip resonators are

by far the most common, highly integrated, and straightforward options for VCO design's at these frequencies, providing a planar implementation with a Q_u of normally ≈ 45 or less and can take up less than $1\,\mathrm{mm}^2$ of space [131, 132]. The Q factor limitations of these on-chip resonators are due to radiation, dielectric and surface resistance loss mechanisms inherent to planar IC designs [133]. Considering off-chip implementations at these frequencies, FBAR and HBAR resonators are both piezoelectric-based acoustic MEMS resonators which can provide Q's in the 1000's or many 10000's respectively in a volume of just a few mm^2, at the expense of more complex integration and larger frequency dependence with temperature [134, 135]. Additionally, HBAR resonators present challenges due to their over-moded nature as they require supplementary filtering and gain stages for operation, increasing the size and complexity [136]. Surface acoustic wave (SAW) resonators have become a mainstay in RF applications below $\approx 3\,\mathrm{GHz}$, but are increasingly difficult to manufacture for higher frequency ranges due to limitations in the miniaturization of interdigital transducers [137]. Beyond these options, there exist a number of high-Q resonators in this frequency range that won't be discussed in detail due to their size, temperature dependence or technology readiness level. Some examples include dielectric resonant oscillators (DROs) [138], larger traditional high Q cavities [139], whispering-gallery mode resonators [140], miniaturized loop-gap resonators [141,142], spoof surface plasmon resonators [143], and ultra-thin 3-D resonators in photo-etchable glass [144]. Progress in practical application of any of these technologies could lead to large improvements in phase noise for VCOs in CSACs.

Along with choosing a low flicker corner semiconductor technology and improving resonator Q, circuit design techniques leveraging insights from time-variant phase noise theories can allow for further improvements to cyclostationary phase noise [145] [146]. Some examples of these circuit topologies include balanced or differential Colpitts [115, 147, 148], Class-C harmonic [149], tail current-shaped [150] and G_m-boosted [151] VCOs which provide improved phase noise performance often with the trade-off of increased complexity or potential start-up difficulties. A few of these circuit topologies have already been leveraged in CSAC systems [30, 82]. In addition to improvements from these generic circuit architectures, component level design practices such as reducing

varactor modulation and dc biasing noise can also have a large impact in reducing VCO phase noise [152]. For example, due to the relatively small (<10 kHz) required VCO tuning range set by the atomic resonance line, VCOs in CSACs have the advantage of only necessitating a low tuning gain K_{VCO} (MHz/V), which can help to lessen varactor modulation induced noise. Practically, the tuning gain should not be too small as to account for systematic frequency deviations from the desired hyperfine frequency. Use of low current noise dc supplies such as batteries or low-noise linear dropout regulators (LDOs) along with constant current supply circuits like current mirrors or operational amplifiers can also help reduce dc bias noise as much as possible [153].

3.1.3 RF Output Power, RF Amplifiers, and VCSEL Matching

As discussed in Chapter 3, the LO needs to provide an RF power level to the VCSEL around -5 to $+10$ dBm that can be finely controlled based on requirements set by the individual VCSEL, interrogation scheme, and physics package design. To achieve this range of tunable power levels, LOs commonly use either a digitally controlled dc bias of an RF amplifier or variable attenuator at the output of the RF VCO as shown in Fig. 3.1, which also provides a buffer from potential frequency load-pulling [14, 30, 154]. This digital control of the output power can then be easily interfaced with the rest of the digital and feedback control circuits. While these are relatively standard solutions implemented in RF synthesizers, challenges arise for LO designers when trying to maximize the trade-off between efficiency of the RF synthesis chain and maintaining a suitable phase noise metric [126]. This can be especially true if the RF VCO output power is well below the desired range, as further amplification stages are required which place a larger emphasis on the additive phase noise of the amplifier stages. RF amplifier phase noise has been demonstrated to be the summation of terms related to white phase noise and flicker noise, written in [155] as:

$$S_{\varphi} = b_0 + \frac{b_{-1}}{f} \qquad [\mathrm{rad}^2/\mathrm{Hz}] \tag{3.2}$$

where the term b_{-1} is the flicker coefficient of the amplifier which is primarily determined by the semiconductor technology. The white noise term b_0 is defined as:

$$b_0 = \frac{FkT_0}{P_0} \qquad [\text{rad}^2/\text{Hz}] \tag{3.3}$$

with F being the amplifier noise figure, P_0 the input RF power to the amplifier, k the Boltzmann constant and T_0 the temperature in Kelvin.

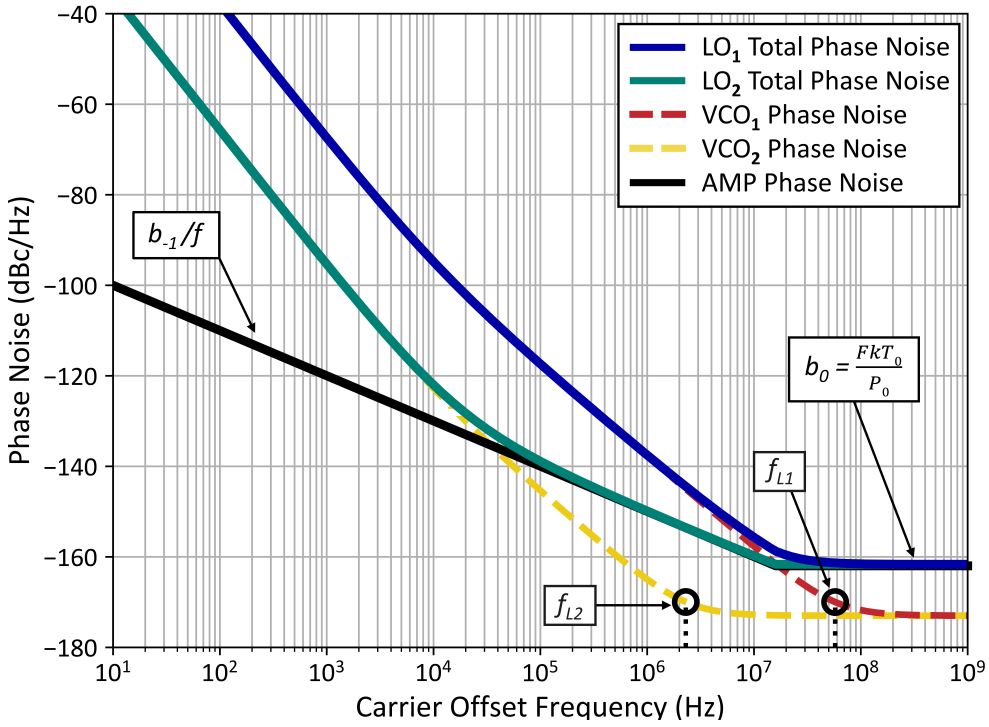


Figure 3.4: Example of the effects of additive phase noise for a RF power amplifier (AMP) operated in mild compression, amplifying the output of a generic 4.6 GHz VCO in two cases. VCO_1 represents an oscillator with a LC resonator with Q_L=40 and VCO_2 using a high-Q RF resonator with Q_L=1000. The resulting total LO phase noise is found by adding the amplifier and VCO phase noise in each case is shown, with degradation at medium to high frequency offsets. The Leeson frequencies, f_L, are also shown.

A generic example of how this formulated additive phase noise of a high-efficiency power amplifier can degrade the total phase noise of the LO is shown in Fig. 3.4. The amplifier shown here is assumed to have a flicker noise component of $b_{-1} = -90\,\text{dBc/Hz}$ and a noise figure of 2 dB

in compression while being driven with an input power of -10 dBm from a VCO, which is reasonable given most CSAC LOs are designed in relatively low-power CMOS technologies. In Fig. 3.4 there are also Leeson phase noise profiles for two different 4.6 GHz VCOs with identical characteristics except for Q_L, with VCO_1 using a high-Q resonator of $Q_L = 1000$ which is a reasonable value that could be accomplished with some of the off-chip resonators reviewed previously, and VCO_2 with $Q_L = 40$ representing a value using a simple on-chip LC resonator. The corresponding total output phase noise for each of these VCOs is represented by LO_1 and LO_2. Additionally, the Leeson frequency $f_L = \nu_0/2Q_L$ is provided for added context [156]. Because the low frequency offset phase noise of the LO (< 20 kHz) is often the region of interest due to the Dick/intermodulation effects, it can be seen here that the effect of the amplifier's additive phase noise on the total LO performance depends mostly on the b_{-1} flicker noise term for the amplifier relative to the low offset phase noise of the VCO. Fig. 3.4 also shows that when using these Q-factors, the added noise from a highly efficient amplifier can be mostly neglected at low frequency offsets (< 20 kHz) as long as the flicker noise (b_{-1}) of the amplifier is sufficiently low when operated in compression. For higher performing LOs using low phase noise quartz crystal oscillators in a PLL or high-Q external resonators, the additive flicker noise of a highly efficient amplifier could likely limit the LO phase noise. Commonly, the VCO and the amplifier gain stages are implemented on-chip with a PLL in a single semiconductor process, meaning the VCO and amplifier will have similar flicker noise characteristics.

Notably, some experimental evidence has shown marginally efficient amplifiers driven into mild compression can maintain their low-flicker (b_{-1}) performance independent of output power [157]. Nonetheless, the effects on the (b_{-1}) flicker noise for different kinds of highly non-linear, efficient amplifiers has not been well studied to the authors' knowledge, and in many cases has shown degradation in the (b_{-1}) flicker noise region based on how the amplifier is operated [158–161]. The use of a highly non-linear amplifier will still result in degradation in the white noise (b_0) region of the LO due to the increased noise figure, which could potentially be relevant.

Beyond analyzing the amplifier additive phase noise, emphasis should also be placed on

determining the impedance of the load driven by the LO at the hyperfine frequency, in this case the VCSEL, and matching this impedance to the LO output. This will provide maximum RF power transfer to the VCSEL, reducing further unnecessary loss. Previous works have shown that the VCSEL impedance can be marginally sensitive to bias current and temperature, which should be accounted for when designing a matching structure [118]. An example of a calibrated impedance measurement for a VCSEL is shown in Fig. 3.5, showing the complex RF impedance of a 795 nm VCSEL from 3-4 GHz across a range of bias currents.

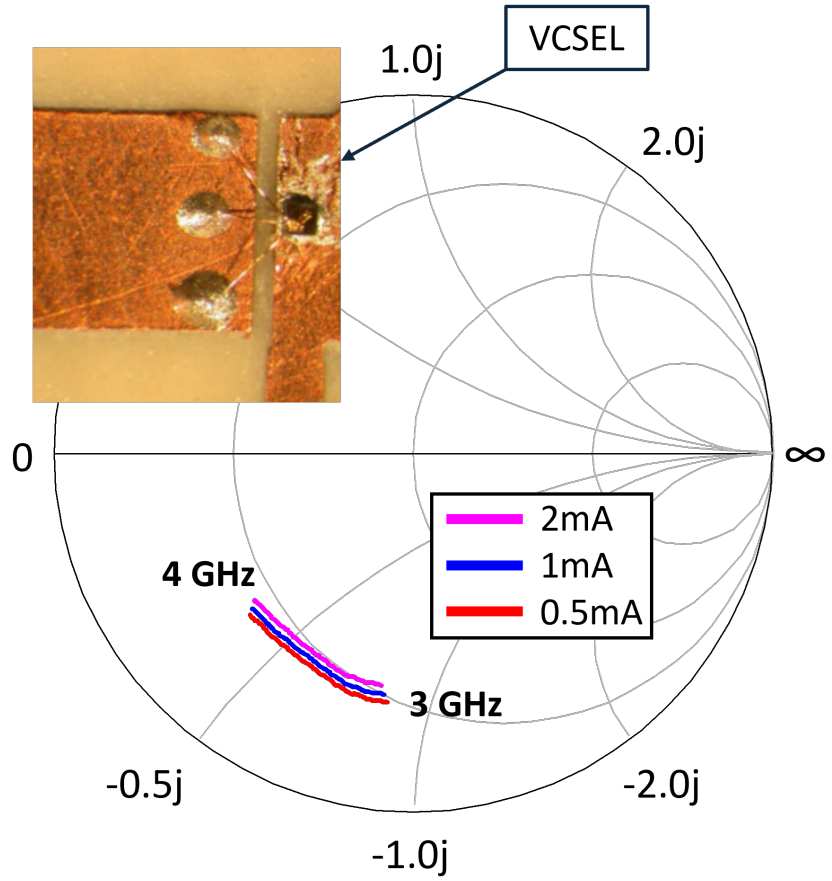


Figure 3.5: Calibrated RF impedance measurement of a VCSEL from 3-4 GHz for multiple dc bias currents, showing a complex measured impedance plotted on a 50 Ω Smith chart [118] At 3.4 GHz, the impedance at the wirebond reference plane is $Z = 16 - j32\,\Omega$.

3.1.4 Control Electronics

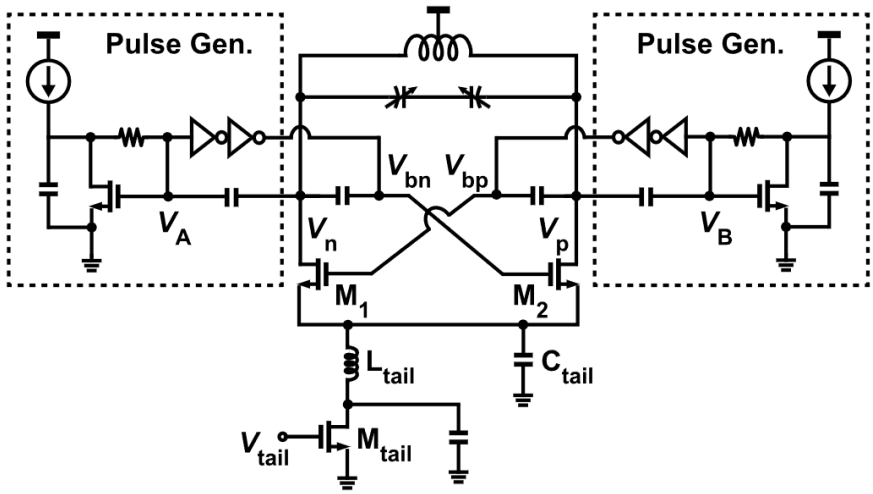
PLLs have become nearly ubiquitous in RF synthesizers, especially in high-performance situations where stability is imperative. Namely, improvements in calibration for all digital PLLs (AD-PLLs) have enabled significantly reduced footprints [162], which coupled with the enhanced noise performance help enable fully integrated CSACs [30]. Exciting opportunities for future implementations are the use of frequency multipliers and multiplying delay-locked-loops (DLLs) that are currently achieving outputs near 10 GHz, which could be used to drive the atomic transitions [163, 164]. Sub-THz PLLs implemented in CMOS have demonstrated promise for chip-scale molecular clocks operating up to 231 GHz. This was achieved using a 28.9 GHz VCO locked to an 80 MHz VCXO, which was then multiplied to reach the sub-THz transition frequency, all while maintaining a power consumption of less than 80 mW [88].

Because the output frequency of a CSAC is typically generated using a quartz crystal within a PLL, its frequency stability is fundamentally limited by the crystal's short-term stability, which typically does not exceed 1×10^{-13} at 1 s for TCXOs [2]. To help improve the clock's short-term stability, emphasis could be placed on finding more accurate, low-power, portable 10 MHz sources, such as MEMS or low-power OCXOs [25, 79].

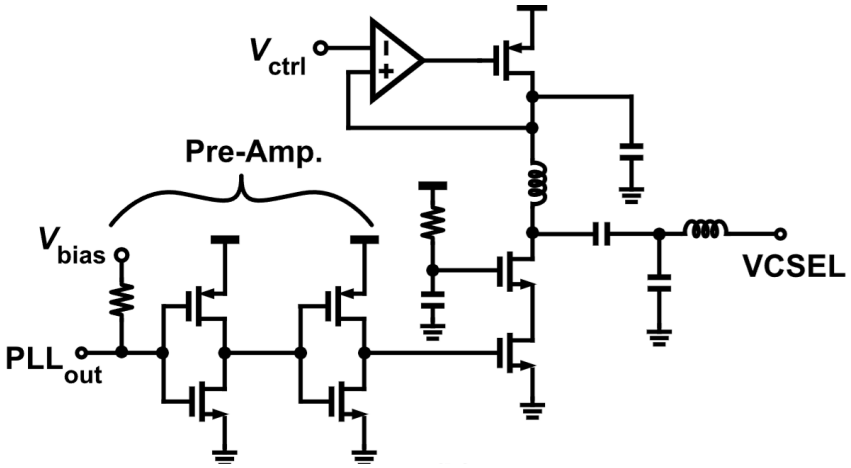
3.1.5 Power Consumption and Efficiency

The total power consumption and efficiency of the microwave LO is discussed last here due to its dependence on nearly all of the previously mentioned design considerations. Often the resulting total power consumption of the LO is merely an amalgamation of trade-offs from previous design choices such as the RF output power requirements, selected technology, etc. Nonetheless, it is one of the most critical performance metrics for consumers as CSACs are often desired in portable, battery operated systems where dc power comes at a premium. As such, a significant amount of the LOs in CSACs are focused on reducing the power consumption or increasing the efficiency of the RF VCO and any RF amplifiers as much as possible through circuit design techniques, while

trying to maintain decent phase noise performance. Figure 3.6a shows an example of a low-power RF VCO architecture referred to as a pulse VCO as a part of a modern CSAC [30, 165]. This low-power oscillator is then fed through a programmable class-E power amplifier shown in Fig. 3.6b, additionally acting as a buffer amplifier, with a peak power efficiency of 47% and peak output power of 5.8 dBm, allowing for a digitally controllable RF power level delivered to the VCSEL. Other than this specific example there are numerous VCO architectures designed for many different frequency ranges, which may provide a benefit in future CSACs. These VCOs leverage output waveform shaping, dynamic biasing, and current re-use techniques, which can result in very low-power or high-efficiency VCOs with increased complexity or slightly degraded phase noise [166–170]. Other than increasing the DC-to-RF VCO efficiency, there remain a number of power added efficiency (PAE) enhancing amplifier architectures that could result in a narrow-band, low-power, low-additive phase noise gain stage [171].



(a)



(b)

Figure 3.6: (a) Example of a Pulse VCO as a part of the LO in the "ULPAC" [30]. This VCO architecture uses cross-coupled transistors with waveform shaping via dc bias to increase the DC-to-RF efficiency with the penalty of increased complexity. (b) The VCO output is then fed into a digitally controllable (-8 to 5.8 dBm) class-E switch-mode power amplifier with a peak efficiency of 47.3%.

Beyond circuit design improvements, reducing the total LO power consumption depends on creating an effective link budget for the RF power required to drive the VCSEL, as well as the additive phase noise and PAE of any additional RF amplifiers that may be needed. When designing

a very low power consumption, low RF output power VCO and amplifying that output signal using highly efficient switching power amplifiers, one must still consider the effects of the additive phase noise of those efficient amplifiers and ensure the total phase noise of the LO is below the limits determined by the Dick or intermodulation effects.

3.2 Conclusion

This chapter explains the state-of-the-art for microwave local oscillators designed for chip-scale atomic clocks. A review table for such oscillators is presented, showing comparisons across a variety of oscillator metrics and semiconductor technologies. Next, insights are provided into potential improvements for future microwave oscillator designs. The discussed improvements relate to alternative semiconductor processes, new RF resonator technologies, analysis of amplifier gain stages for VCSEL RF drive, control electronics, and improving total RF generation efficiency. The work discussed throughout this chapter and in the previous two chapters is originally reported in our review paper [80].

Chapter 4

InGaP/GaAs HBT Single-Ended Colpitts Oscillator MMICs for a Chip-scale Atomic Beam Clock

Previous chapters have discussed the fundamental operation of CSACs, quantifying the impact of microwave oscillators in the context CSACs, and reviewing the state-of-the-art. The remainder of this thesis reports on the design of such oscillators specific to a new type of chip-scale atomic beam clock as a part of a joint project. In particular, the focus of the next few chapters will be on the design of low power and low phase noise MMIC oscillators based on InGaP/GaAs heterojunction bipolar transistors. New types of miniaturized resonators are also presented, showing a potential improvement in Q-factor while maintaining small volumes. The first resonators compared in this chapter are on-chip implementations, representing an example of relatively low Q-factors while being highly integrated and reproducible. These oscillators using novel on-chip resonators are designed for integration with an external controls ASIC, which will allow for modulation of a VCSEL in the same manner as described in previous chapters. A high-level block diagram of such a microwave clock is shown in Fig. 4.1.

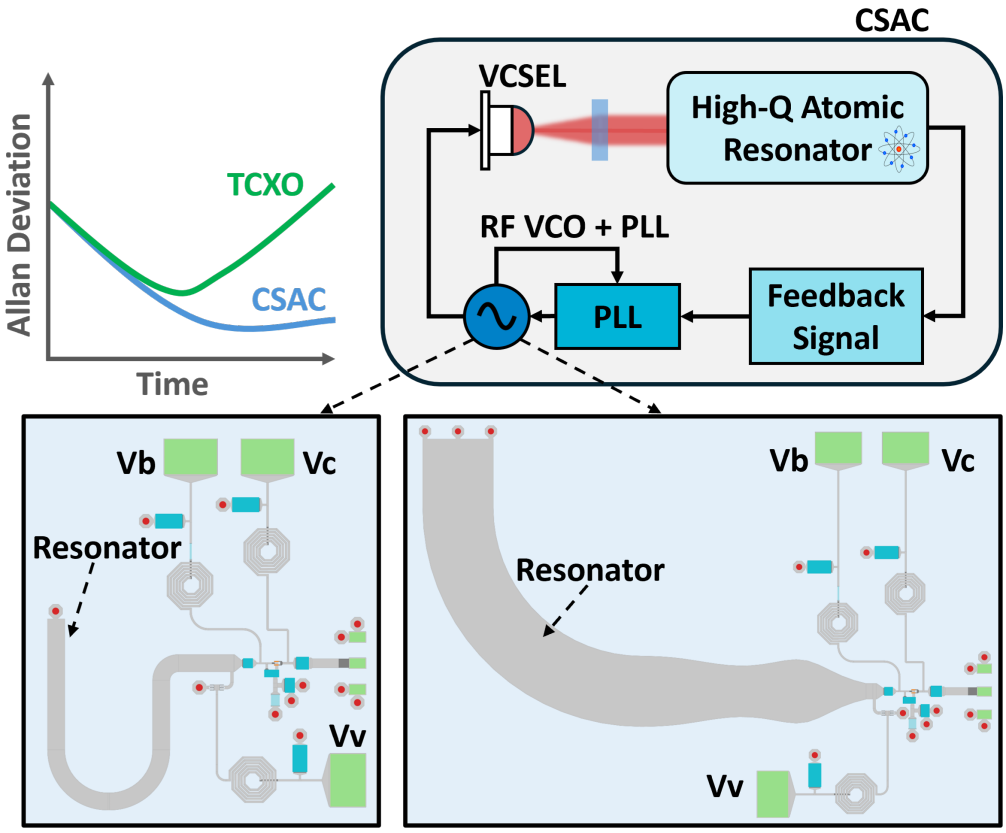


Figure 4.1: High-level block diagram of a generic microwave chip-scale atomic clock (CSAC). The microwave VCO operating at the half-hyperfine transition of ^{133}Cs is stabilized by a high-Q atomic resonator in a feedback loop, resulting in an increased long-term stability compared to a temperature compensated crystal oscillator (TCXO).

4.1 Small Efficient Atom Beam (SEABeaST) Project

The Small and Efficient Atom Beam Stabilized Timing (SEABeaST) project is a part of a larger program which seeks to develop small, low dc power consumption clocks which can maintain microsecond timing precision for a week without GPS fixes [38]. The physics package for this new type of miniaturized chip-scale beam clock is being developed at NIST, showing a potential quantum-noise limited fractional frequency stability of up to $\approx 9\times10^{-12}/\sqrt{\tau}$, potentially improving the long-term stability of the current generation CSACs [36]. The team tasked with the miniaturization of the local oscillator required to modulate the VCSEL laser includes CU Boulder for the

voltage controlled oscillator, and Virginia Polytechnic Institute and State University for design of the phase-locked loop and control circuits. HRL Laboratories is leading system integration and wafer-level fabrication of the atom beam devices [172]. An example of a miniaturized Cesium beam device developed at NIST is shown in Fig. 4.2 [173].

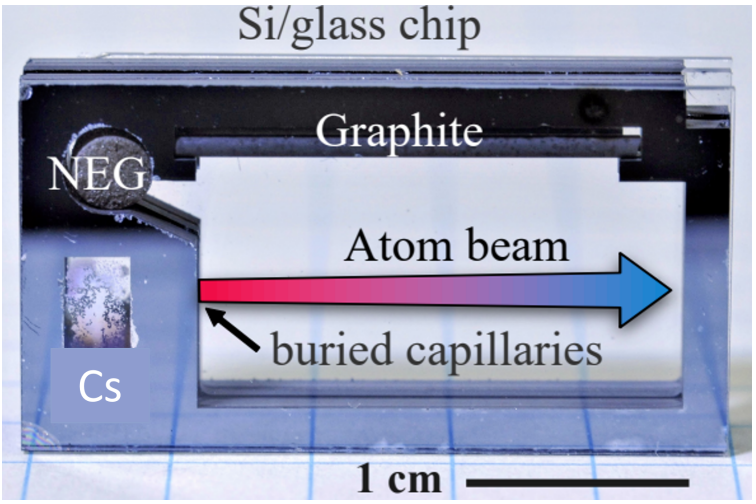


Figure 4.2: Photograph of an atomic beam device developed at NIST Boulder [173]. A few of the internal components are labeled including the location of the atomic beam, shown by the arrow.

This chapter details a set of these voltage controlled oscillator (VCO) MMICs which utilize a synthesized on-chip nonuniform transmission line (NTL) resonator, designed for phase 1 of the project. A full wafer of these VCO MMICs, fabricated in a WIN Semiconductors InGaP/GaAs heterojunction bipolar transistor (HBT) process, were designed as an initial step towards a fully integrated chip-scale atomic beam clock. Near the half-hyperfine frequency of ^{133}Cs (4.596...GHz), the NTL oscillator provides a peak RF output power up to +14 dBm, modulating a laser diode used to interrogate the atoms inside the clock. The measured DC-to-RF conversion efficiency is 25.5% (39.2 mW), and the phase noise is -81.8 dBc/Hz at a 10 kHz offset. A 2nd VCO is designed using a uniform on-chip transmission line resonator for comparison, showing the NTL VCO provides a 1.8 dB measured improvement in phase noise at the same bias. An additional bias point is reported, only consuming 9.8 mW, while degrading the phase noise to -77.7 dBc/Hz at 10 kHz. The

NTL resonator is synthesized to maximize unloaded quality factor, achieving a final simulated value of 41 and 48 with and without the varactors, respectively.

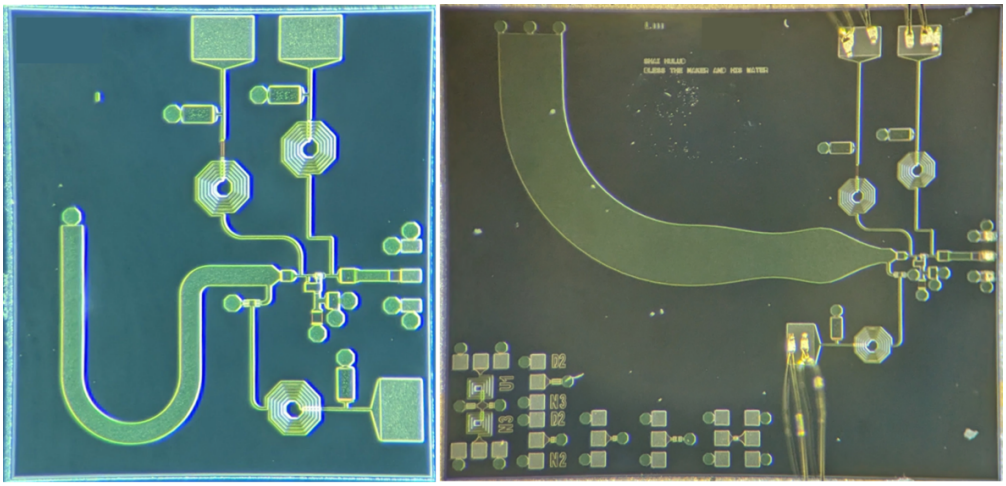
4.2 InGaP/GaAs HBT Oscillator MMIC with NTL resonator

As the long-term stability improves from the atomic side, the phase noise of the microwave LO limits the overall long-term frequency stability of the clock, due to the non-linear up-conversion of LO phase noise through the atomic resonator [51]. This introduces a difficult trade-off between dc power consumption, phase noise, and size for the LO design. The VCO performance goals, Table 6.1, are based on the specific requirements for the small atom beam clock, with the RF output power requirements being set by VCSEL operating points corresponding to reduced light shifts.

Table 4.1: VCO Design Targets for the Chip-scale Atom Beam Clock

f_0 (GHz)	Tuning Gain	Phase Noise @ 10kHz	Output Power	P_{dc} (mW)
4.596	100 MHz/V	-80 dBc/Hz	0 to 12 dBm	50

One significant design consideration in achieving minimal VCO phase noise is to maximize the unloaded quality-factor, Q_u [130]. Conventional solutions use off-chip, high-Q cavities but at the expense of a system size and weight that is undesirable for CSACs. Therefore, use of an on-chip resonator such as a shunt transmission line is desirable for this type of VCO. To achieve this, a novel nonuniform transmission line (NTL) resonator is presented which is designed to maximize Q_u at the nominal frequency of operation. This design is performed using the NTL synthesis method akin to that of [174] where an approximate loss model is included in the procedure. The final transmission line, Fig. 4.3(b), is a tapered line with minimized conduction losses–similar to the approach of [175]. The resulting phase noise between a VCO with a uniform microstrip line resonator, Fig. 4.3(a), is compared with a VCO with the synthesized NTL resonator, Fig. 4.3(b).



(a) (b)

Figure 4.3: Photographs of (a) VCO chip, 2.1×2.3 mm in size, with a 37-Ω microstrip shorted resonator and (b) VCO chip, 4.2×3.5 mm in size, with a NTL shorted resonator.

This chapter presents a low phase noise InGaP/GaAs HBT MMIC VCO designed at the half-hyperfine transition frequency of ^{133}Cs (4.596 GHz), as a step towards an integrated microwave LO. Eventually, off-chip integration with an additional buffer amplifier, variable attenuator, and ASIC, including a phase-locked loop (PLL), control, and feedback circuits will be used to modulate the VCSEL and interrogate the atoms in the chip-scale atomic beam clock.

4.2.1 Circuit Design

When designing a VCO, the key factors in Leeson's equations, the flicker corner of the chosen technology (f_c) and the resonator Q [50], are considered. The low phase noise (¡−80 dBc/Hz at 10 kHz) and output power (+12 dBm) requirements specific to the small atomic beam clock dictate a technology such as InGaP/GaAs HBTs [176]. This technology has a higher breakdown voltage compared to CMOS or SiGe HBT-BiCMOS, commonly used in CSACs due to their ease of integration [61]. The designs in this chapter are implemented in WIN Semiconductors' H01U-G3 InGaP/GaAs HBT process and simulated in Cadence AWR's harmonic balance solver, with foundry transistor models.

Figure 4.4 shows a schematic of the oscillator. A Colpitts-like topology characterized by good

cyclo-stationary phase noise [145, 147] is selected for both designs, with a near-critically coupled quarter-wave shunt transmission line as the resonator. For the uniform design, Fig. 4.3 (a), the resonator width and length, as well as coupling capacitor, are chosen for the highest loaded Q_L using traditional techniques, while still adhering to the other metrics in Table 6.1. The main feedback capacitors *C1* and *C2* are designed with a 0.3 Colpitts ratio while maximizing the capacitor Q in order to reduce their impact on phase noise. Base and emitter resistors are included to decrease sensitivity to thermal and bias fluctuations. The HBT transistor is a 2-finger $1.6 \times 20\,\mu$m device, chosen as a trade off between the desired maximum output power of +12 dBm, dc-to-RF efficiency, and simulated phase noise. Specified frequency tuning of 100 MHz/V is achieved via two back-to-back 2-finger $8 \times 10\,\mu$m shunt hyper-abrupt varactor diodes. The VCO is coupled to a $50\,\Omega$ load, where it is further divided off-chip into the PLL and VCSEL matching circuits. The NTL synthesis similar to the approach of [177, 178] is used to design a shorted resonator with an impedance Z_c(x) that varies along its length and as a result has an increased Q.

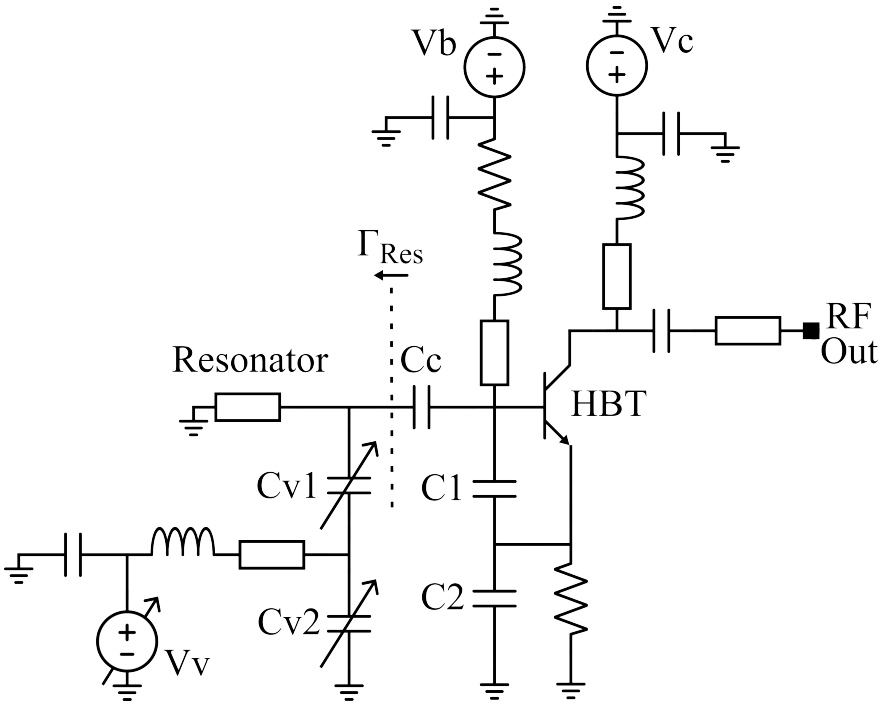


Figure 4.4: Circuit Schematic of the Colpitts-like 4.596 GHz VCO.

The design goal in this work is to maximize the unloaded quality factor of the resonator with the varactor. This equates to minimizing $|S_{11}|$ at the nominal operating frequency 4.596 GHz, as well as a frequency f_0 shifted upwards to account for the varactor loading. Additionally, $|S_{11}|$ is maximized at the adjacent frequency points f_{low} and f_{high}:

$$f_{low} = f_0 \left(1 - \frac{1}{2Q_u}\right) \quad \text{and} \quad f_{high} = f_0 \left(1 + \frac{1}{2Q_u}\right)$$

where $Q_u = 51$ is the target unloaded quality factor of the NTL. To include loss, the TEM line parameters are extracted from S-parameters in simulations by varying the width of a microstrip line. After converting S to ABCD parameters, the complex characteristic impedance and propagation constant are found as $Z = \sqrt{B/C}$ and $\gamma = (\cos A)/\ell$, where $\gamma = \alpha + j\beta$ and ℓ is the physical length of the microstrip line used in the extraction process. The real part of the NTL characteristic impedance is constrained to $13 - 80\,\Omega$ and the input terminal impedance set to 37Ω, the same impedance as the uniform transmission line resonator. Synthesis is carried out by: 1) finding the line length; 2) finding a suitable linear impedance taper; and 3) sequentially adding harmonic content to the impedance function. Once a suitable impedance function is found, the transmission line is converted to an equivalent microstrip NTL, which can be physically large and meandering is required to fit it in the MMIC footprint, and can be done analytically [178]. The microstrip structure is then segmented into differential bends based on a parameter which relates the line width to the radius of curvature.

To validate the Q of the NTL resonator, two VCOs are fabricated: one with a uniform resonator and the other with the NTL resonator, Fig. 4.3. The VCO core and coupling capacitor design between both circuits is kept as similar as possible to provide a fair performance comparison. Circuit simulations show that the two Q factors, without including the varactor losses, are 48 and 45.5 for the NTL VCO and the uniform VCO respectively.

4.2.2 VCO Measurements

To validate the impact of the resonator Q on VCO phase noise, dc power consumption, and RF output power, both MMICs are mounted on CuMo pedestals with minimal off-chip capacitors on the bias lines for additional stability and probed using 150μm GSG probes. All measurements are captured using a Keysight E5505A SSA-X signal source analyzer and low current noise dc power supplies internal to the SSA-X.

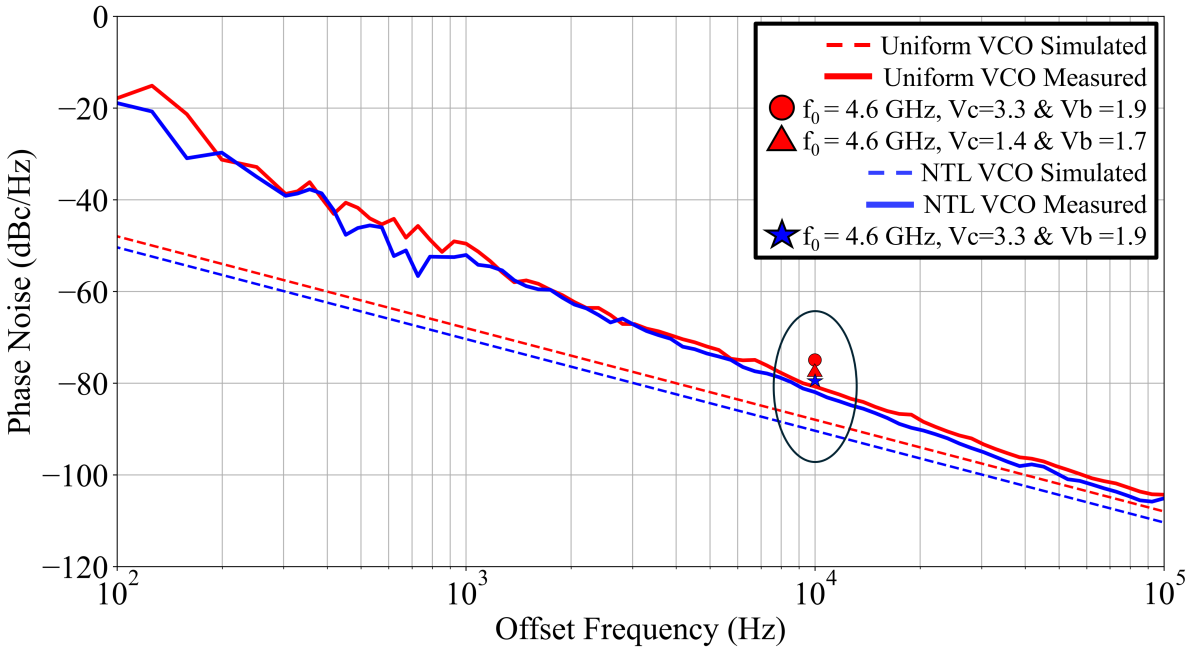


Figure 4.5: Measured phase noise comparison at f_0 =4.56 GHz. PN at 10 kHz = −80.45 dBc/Hz, −81.80 dBc/Hz, with $V_b = 2.1V, V_c = 2.8V$. Foundry transistor models do not include flicker corner for phase noise simulations, which is the major cause for simulation discrepancy at low frequency offsets. Symbols are added to show a slight degradation in phase noise at different biases when oscillating at 4.6 GHz.

Figure 4.5 shows the measured phase noise for both oscillators tuned to 4.56 GHz with a tuning voltage of 5 V, both at identical dc biases of V_b = 2.1 V (I_b = 25 μA) and V_c = 2.8 V

(I_c = 14 mA) resulting in an RF ouptut power of +10dBm and P_{dc} of 39.2 mW for both VCOs. The phase noise is plotted from 100 Hz to 100 kHz offset frequencies, showing reasonable agreement with simulations near a 100 kHz offset frequency where the phase noise is more accurately modeled due to the absence of the flicker corner in the foundry device model. The measured phase noise at a 10 kHz offset for the VCO with a uniform microstrip line resonator is −80.45 dBc/Hz, while the VCO with the NTL resonator is −81.80 dBc/Hz. Overall, the improvement in phase noise from simulation of 2.5 dB was reduced to a measured 1.3 dB improvement, consistent over multiple chip-to-chip measurements. Circled in black is the 10 kHz offset frequency where the VCO specification is defined. Phase noise measurements at a 10 kHz offset from 4.6 GHz with a higher bias (V_b = 1.9 V, V_c = 3.3 V) are plotted, showing a degradation to −75.7 dBc/Hz and −78.7 dBc/Hz for the uniform and NTL VCO, respectively. A lower bias point V_b = 1.7 V (I_b = 8 μA) and V_c = 1.4 V (I_c = 7 mA) is also noted for the uniform VCO, resulting in a measured phase noise of -77.7dBc/Hz at a 10 kHz offset with 2.5 dBm of output power at f_0 =4.596 GHz, consuming only 9.8 mW.

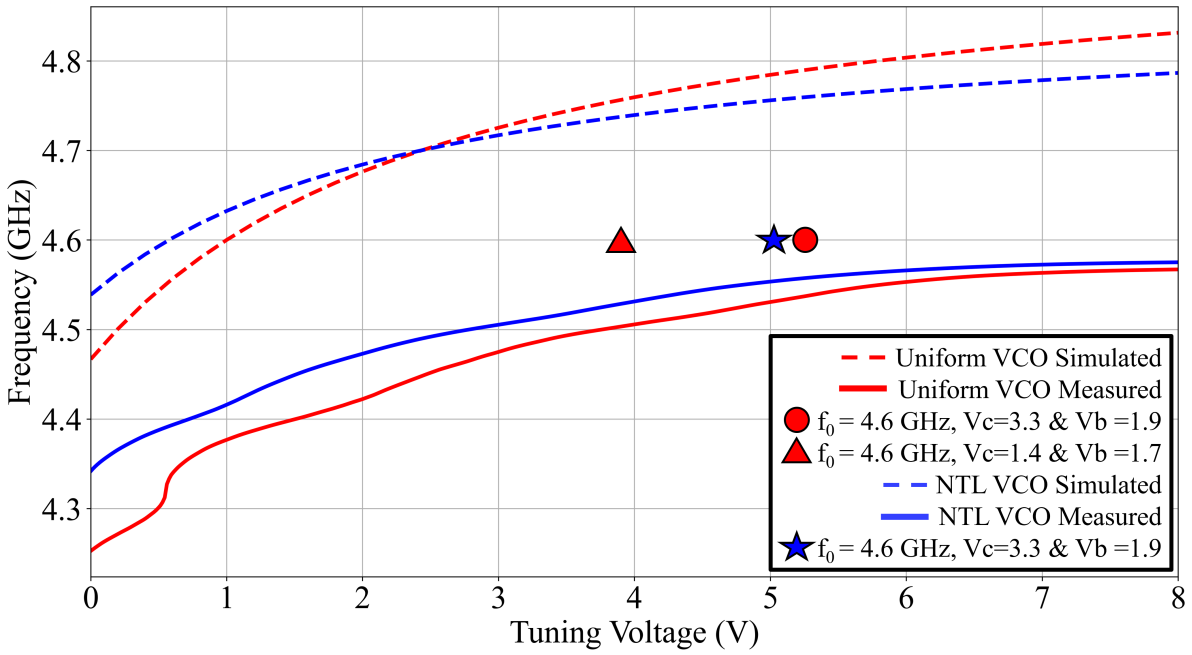


Figure 4.6: Measured oscillation frequency versus varactor tuning voltage compared between the uniform and NTL VCO. Symbols are added to show the measured VCO frequency at 4.6 GHz at different bias points.

Figure 4.6 shows the simulated and measured frequency versus varactor bias voltage for the two VCOs at nominal bias. The NTL VCO ($V_b = 2.1\,\mathrm{V}$ and $V_c = 2.8\,\mathrm{V}$) has a frequency range of 4.34 to 4.58 GHz over 8 V of tuning, resulting in an average tuning gain of ≈30 MHz/V. Symbols show the corresponding change in frequency to 4.6 GHz at a bias of $V_b = 1.9\,\mathrm{V}$, $V_c = 3.3\,\mathrm{V}$. For both VCOs, The output power and dc-to-RF efficiency vary with collector voltage, reaching a peak output power of +14 dBm with a peak efficiency of 27%, with $V_c = 5\,\mathrm{V}$. The output power has a maximum variation of 0.5 dB across frequency. At the bias point with lowest phase noise for a 10 kHz offset at $f_0 = 4.56\,\mathrm{GHz}$ presented in Fig. 4.5, the RF output power is +10 dBm and the efficiency is reduced to around 25.5%, resulting in a total dc power consumption of 39.2 mW for both VCOs. A comparison to a few other reported VCOs for chip-scale atomic clocks is given in Table 4.2.

Table 4.2: Performance Comparison of some reported VCOs for CSACs without PLLs. *Represents Estimated Value Based on Figures

	Tech.	**Freq. (GHz)**	**PN @ 10 kHz (dBc/Hz)**	**DC Power (mW)**	P_{out} **(dBm)**
[30]	65 nm CMOS	4.6 GHz	*-68	<11.2	-8 to -6
[61]	130 nm CMOS	4.6 GHz	*-60	<12	-10 to 0
[179]	65 nm CMOS w/ FBAR Resonator	3.4 GHz	*-90	9	N/A
This Work†	InGaP/GaAs HBT	4.6 GHz	-81.8	39.2	0 to 14
This Work◇	InGaP/GaAs HBT	4.6 GHz	-77.7	9.8	2.5

† represents the NTL VCO and ◇ represents the uniform VCO

4.3 Conclusion

This chapter presents the design, measurement, and comparison of two low phase noise MMIC VCOs in an InGaP/GaAs HBT process for use in a new type of chip-scale atomic beam clock. Overall, the VCO designed using a novel on-chip resonator synthesis method provides an improvement in phase noise of 1.8 dB at 10 kHz at the same bias condition, at the expense of a minor increase in chip area. Other metrics for the chip-scale atomic beam clock such as an output power of over +14 dBm, VCO tuning range of 30 MHz/V, and dc power consumption of 39.2 mW provide a path towards miniaturization of the first prototype microwave beam clock. The work presented in this chapter is presented in [180].

Chapter 5

InGaP/GaAs HBT Oscillators with Hybrid Integrated Glass Embedded Resonators

This chapter describes the design and measurements of an additional 4.596 GHz InGaP/GaAs low-phase noise MMIC oscillator, utilizing an off-chip glass-embedded resonator for use in a chip-scale atomic beam clock. The glass embedded LC resonators alone achieve a peak measured $Q_u = 107$ at a resonant frequency of 8.8 GHz or $Q_u = 52$ at a resonant frequency of 7.1 GHz, depending on measurement condition. The hybridly integrated oscillator utilizes the high-Q glass-embedded resonators to achieve a measured free-running phase noise of -58 dBc/Hz at an offset of 1 kHz from the half of a hyperfine transition frequency of ^{133}Cs when biased at $V_c = 4.1\,\text{V}, I_c = 22.2\,\text{mA}$ and $V_b = 2.8\,\text{V}, I_b = 270\,\mu\text{A}$. The oscillator also achieves a minimum phase noise of -140 dBc/Hz at a 1 MHz offset when biased at a different operating point. The oscillator's output frequency is adjusted with an on-chip varactor diode with a tuning gain of 2 MHz/V near the desired output frequency. The output power reaches a peak of 13 dBm, set by the requirements of the atomic interrogation scheme of the chip-scale beam clock. The total dc power consumption for the MMIC oscillator is 91 mW. The oscillator is tested with a miniaturized Cs beam clock using a commercial off-chip phase-locked loop as a proof of concept. The demonstrated overlapping Allan deviation from the beam clock is white-noise limited from 1-100 s, and averages as $\sigma_y \approx 3.3 \times 10^{-10}/\sqrt{\tau}$ when operated using the PLL-locked MMIC VCO.

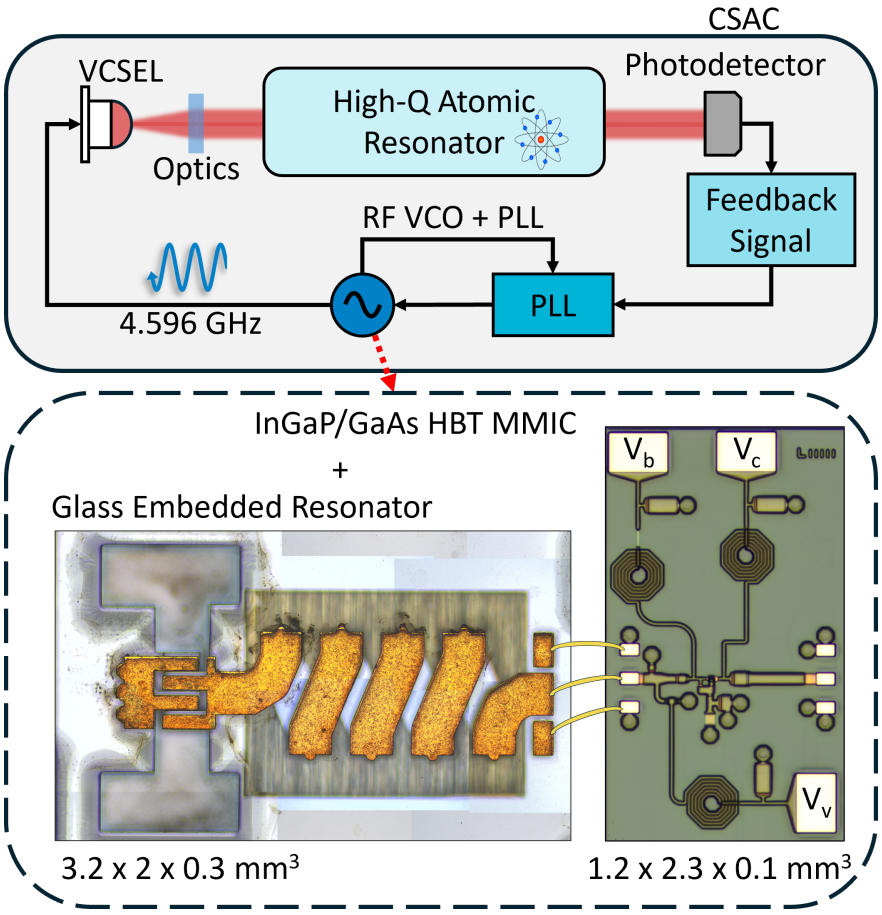


Figure 5.1: High-level block diagram of a microwave chip-scale atomic clock based on ^{133}Cs atoms. The MMIC VCO described in this chapter ($1.2 \times 2.3 \times 0.1\,\mathrm{mm}^3$) is pictured on the bottom right and produces a low phase noise 4.596 GHz output by integrating a glass embedded resonator ($3.2 \times 2 \times 0.3\,\mathrm{mm}^3$) via bond wire, which has a measured $Q_u > 50$.

Figure 5.1 shows a high-level block diagram of a chip-scale atomic clock along with photographs of the InGaP/GaAs HBT MMIC and the glass embedded resonator, which are integrated in this chapter to create the RF (VCO). As described in the previous chapter, the initial target specifications for the RF VCO after integration with a PLL are a peak output power of +12 dBm, a phase noise of -60 dBc/Hz at an offset of 500 Hz from a 4.596 GHz tone, a tuning gain < 10 MHz/V, and a dc power consumption < 100 mW.

A large portion of this chapter tackles the most critical factor in improving the phase noise

of an oscillator by using a higher-Q resonator, which is often at odds with other system level requirements such as volume constraints [48, 50]. The oscillator designs such as those shown in the previous chapter employ relatively low-Q on-chip resonators within the integrated circuit due to their consistent fabrication and compact nature. The on-chip Q-factors of such resonators are bounded by loss mechanisms inherent to 2-D integrated circuit design, including substrate losses, resistive metal losses, and radiative loss [133]. Therefore, in order to achieve better phase noise performance in a miniaturized size, research on small ($< 2 \times 2\,\mathrm{mm}^2$) off-chip resonant structures has been conducted, such as the use of acoustic wave resonators in oscillators operating below 10 GHz [134]. Acoustic wave resonators have the benefit of comparatively high Q-factors (> 1000), but suffer from temperature dependence of the resonant frequency, complex coupling structures, and difficult fabrication at certain frequencies [137].

Driven by these requirements for low-volume high-Q RF components and heterogeneous integration, Photo-Sensitive-Glass (PSG) substrates have emerged as excellent candidates for low-loss off-chip structures due to their low dielectric loss, low surface roughness, and adjustable coefficient of thermal expansion (CTE) comparable with Silicon [181]. Low-loss through glass vias (TGVs) utilizing these PSG processes have become an important area of research for combining different integrated circuit technologies within a single module via heterogeneous integration [182–184]. As an extension of the work on TGVs, 3-D inductors fabricated in PSG have been demonstrated with individual Q-factors >70 and inductance densities of $>45\,\mathrm{nH/mm}^2$ [185, 186]. This approach has also been successfully extended to complex filter and resonator designs, such as planar half-mode substrate-integrated waveguides and coupled-line filters [187, 188].

In this chapter, an LC resonator using TGVs in PSG which is then hybridly integrated with an InGaP/GaAs MMIC oscillator is presented. To the best of the authors' knowledge, this is the first demonstration of a compound-semiconductor oscillator MMIC directly integrated with a glass-substrate resonator. The integrated oscillator is measured and used as the VCO in a demonstration with a chip-scale atomic beam clock, as shown in Fig. 5.1. The chapter is organized as follows. The next portion details the design and characterization of the 3-D glass-embedded resonators. Then,

the design of the 4.596 GHz InGaP/GaAs heterojunction bipolar (HBT) tunable oscillator chip, with measurements of the integrated VCO are shown. Finally, proof-of-principle locking to the atomic transition of a miniaturized Cs beam clock is demonstrated.

5.1 Glass Resonator Designs and Measurements

The components in PSG used in this work are fabricated by 3DGlass Solutions, allowing for creation of complex 3-D metalized structures in a 300 μm tall glass substrate by means of low-loss TGVs [189]. A photograph of several inductors and resonators designed and fabricated in this process are shown in Fig. 5.2.

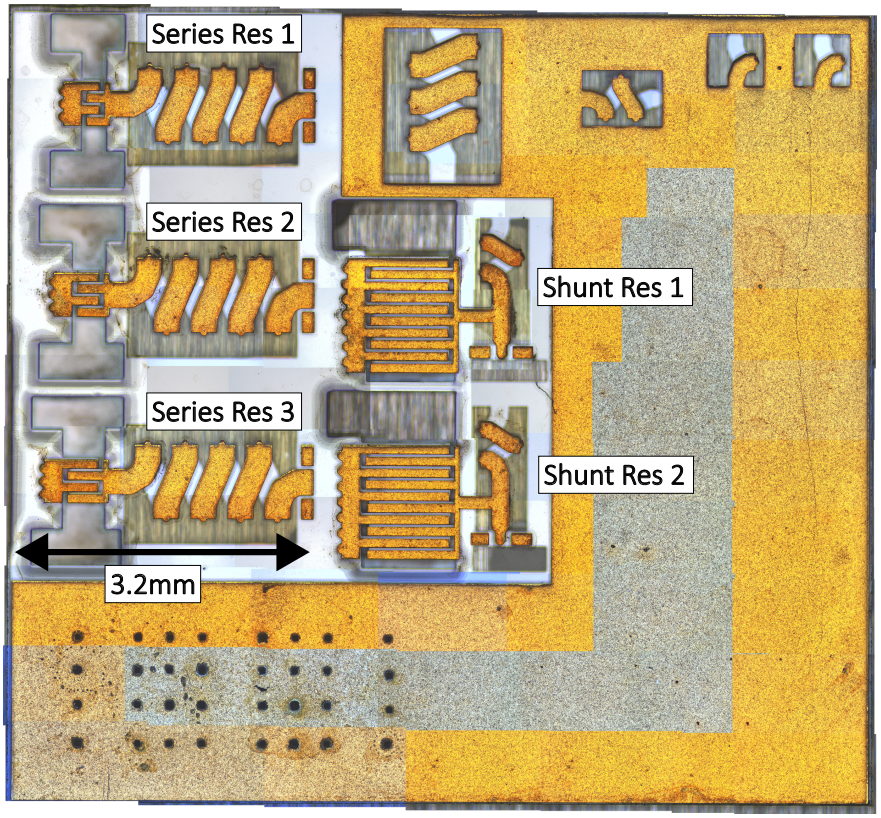


Figure 5.2: Photo-Sensitive-Glass die photograph containing multiple resonators and inductors designed using through glass vias. Labels for the 3 series resonators and 2 shunt resonators are included for reference to measurements presented.

All structures are designed using full-wave ANSYS HFSS simulations, with an example 3-D view shown in Fig. 5.3, with labeled components. Some structures are initially designed using foundry provided PDK elements, such as the inductive spirals, while other elements such as the the interdigitated capacitors designed with custom geometries. Parametrized sweeps of conductor width, length, number of turns, and separation are performed to improve component Q factor and to obtain the desired resonant frequency. For the simulation parameters, a permittivity of $\epsilon_r = 6.4$ and a loss factor of $\tan\delta = 0.014$ is used for the glass, while the metal is gold-plated copper with a thickness of $10\,\mu$m and conductivity of $\sigma = 5.8 \times 10^7\,$S/m. A $20\,\mu$m-thick polyamide layer with $\epsilon_r = 3.4$ and loss factor $\tan\delta = 0.019$ is also included for passivation.

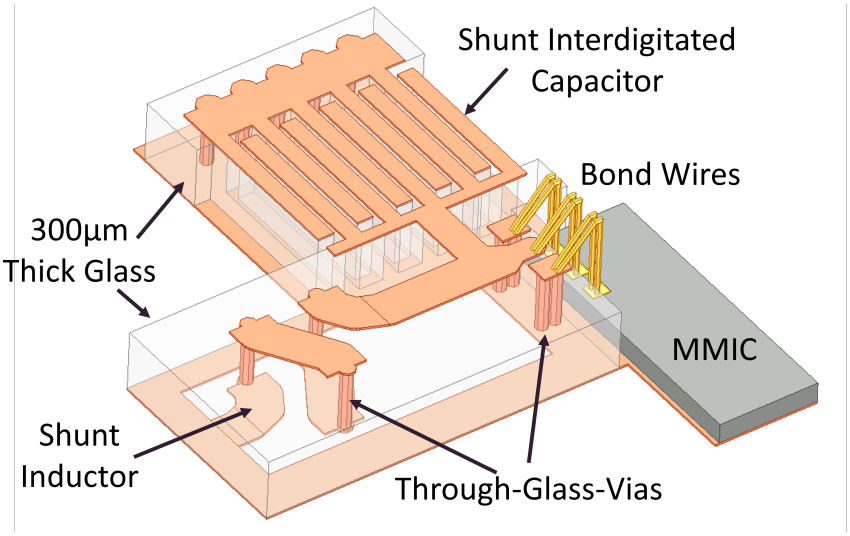


Figure 5.3: 3D model used for full-wave simulation of the glass-embedded resonators in ANSYS HFSS. Bond wire simulations to the InGaP/GaAs MMIC die are performed to aid in accurate co-design.

Resulting from the experimental fabrication process, the glass die exhibits several unintended visually identifiable defects, such as metal overhanging the glass substrate, non-uniform trace widths, and misaligned TGVs illustrated in Fig 5.4. These defects are then re-introduced into the HFSS models to see any impact on performance from the nominal simulation case.

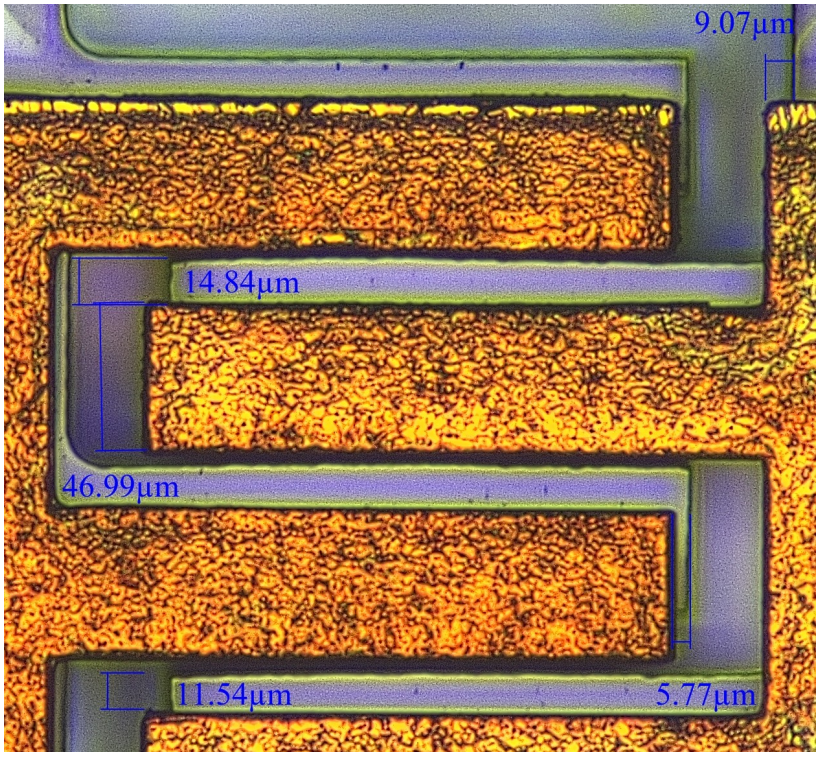


Figure 5.4: Close-in die photograph and estimated measurements of defects seen after experimental fabrication process. Defects are not consistent from die to die.

Multiple resonators are taped out and designed with various resonant frequencies between 5-8.5 GHz, which when integrated with the oscillator MMIC allows for operation at 4.596 GHz as described later. The resonator S-parameters are first measured without the oscillator MMICs using the 200 μm input GSG pads on the top of the glass substrate, with a standard probe station with the die placed directly on the metal chuck ground. The measurements are made using a Keysight E8364C Vector Network Analyzer (VNA) and are calibrated using an Alumina SOLT calibration standard. The resonators were not simulated with the metal chuck. Therefore, the resonators' S-parameters are subsequently measured using a double-sided probe station (DSPS), in order to characterize the resonators with air boundary conditions on both sides of the die. A photo of the custom 3D-printed mount and underside probing is shown in Fig. 5.5.

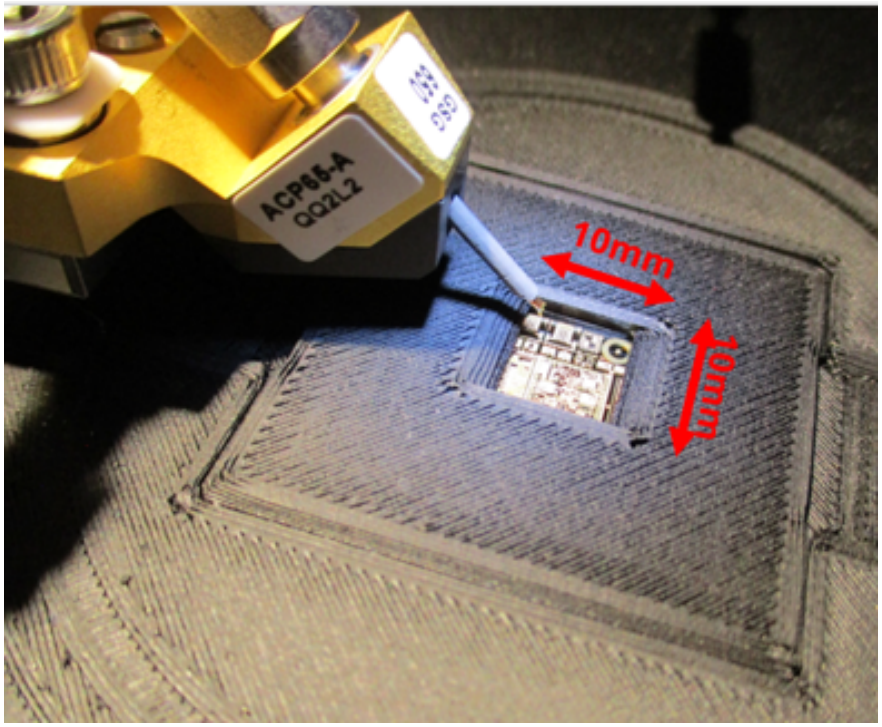


Figure 5.5: Photograph of a die containing glass-embedded circuits held in a custom 3-D printed mount on a double-sided probe station.

The simulated and measured S-parameters for the shunt and series resonators are shown in Figs. 5.6 and 5.7, respectively. Because the resonator coupling components are integrated on the MMIC and the resonators lack a standard $50\,\Omega$ match, the performance is plotted using an approximated impedance to achieve critical coupling. The unloaded Q_u is calculated using the full-width half-max (FWHM) method and shown next to the trace data. The simulated S-parameters are referenced to the resonators alone, with no bond wires or MMIC integration.

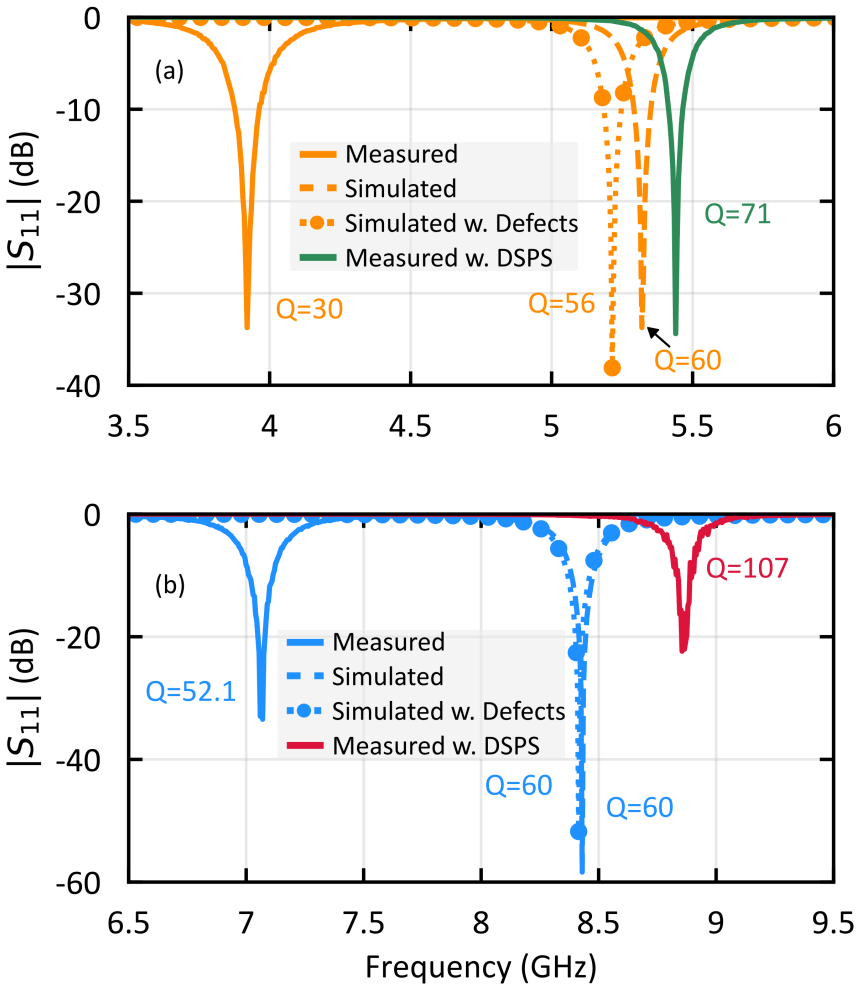


Figure 5.6: Measured and simulated $|S_{11}|$ versus frequency for "Series Resonator 2" when ideally critically coupled. Simulations including visually identifiable defects are shown with symbols. Measurements using the double-sided probe station (DSPS) are shown in red and green. The top plot (a) shows results for the resonator coupled into a series resonant mode, while the bottom (b) corresponds to the resonator coupled into the "series-shunt" resonant mode.

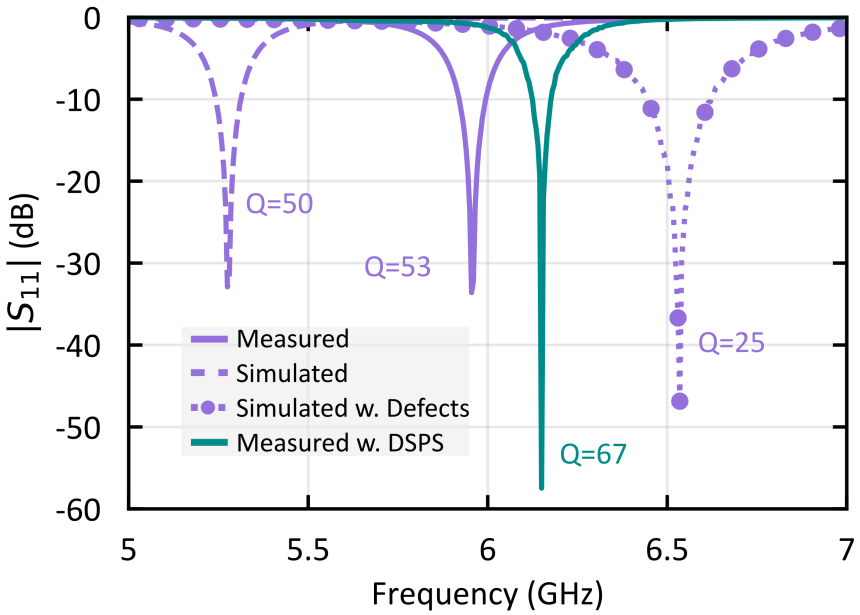


Figure 5.7: Measured and simulated $|S_{11}|$ versus frequency for "Shunt Resonator 1" when ideally critically coupled. Simulations including visually identifiable defects are shown with symbols. Measurements using the double-sided probe station (DSPS) are shown in teal.

Due to a combination of the visually identifiable defects, loading from the probe station ground plane, and possibly other internal defects within the glass die, a down-shift in frequency and Q for all resonators is found. For the series resonators shown in Fig. 5.6, a second shunt resonant mode is also measured, referred to here as "series-shunt" mode plotted in blue and red. This mode has a higher Q than the original series resonant mode plotted in orange and green. The measurements of the series-shunt resonance represent the highest Q_u factor seen in the glass resonators reported here, with measured Q_u =52.1 for the metal boundary condition using the single-sided probe station, and Q_u =107 for the air boundary condition using the double-sided probe station.

Additionally, a simple yield analysis is done using the standard single-sided probe station to characterize performance variation across multiple die from the wafer. Figure 5.8 shows a deviation of measured resonant frequencies and Q_u values across the wafer, likely due to the experimental

embedded glass resonator fabrication. A trend line is presented based on observation, showing that generally the series resonator Q_u when operating in the series-shunt resonant mode increases linearly with frequency. This behavior is not seen for the shunt resonators. For the oscillator and clock measurement results in this chapter, the highest performing series resonator, operated in the series-shunt mode, is selected to show proof of concept for the technology.

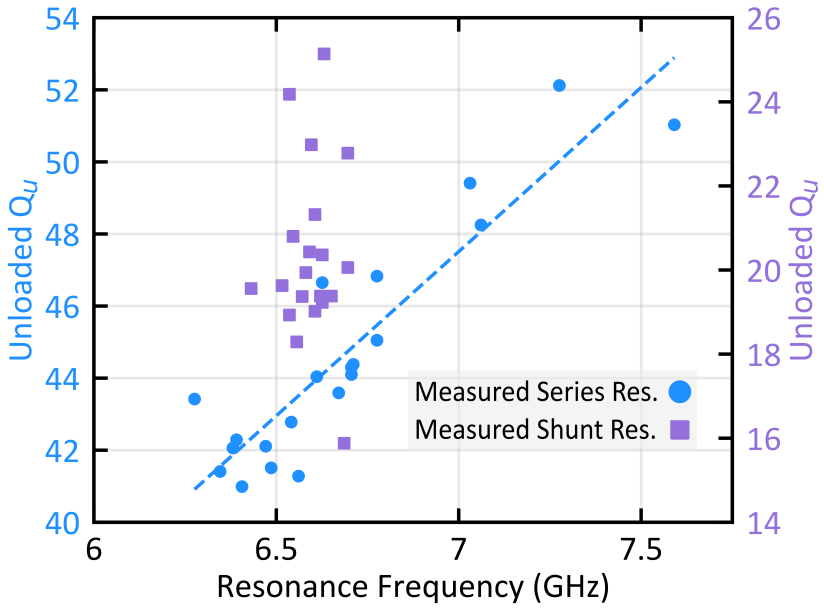


Figure 5.8: Repeated resonator measurements across multiple die from the wafer, showing a spread in unloaded Q_u factor and resonant frequency. A trend line for the series resonators is presented. Measurements are of "Shunt Resonator 1" and "Series Resonator 2" when coupled to the "series-shunt" resonant mode.

5.2 RF Oscillator Circuit Co-Design

The resonators described earlier are co-designed in parallel with a set of low-phase noise oscillators in Cadence AWR and fabricated using WIN Semiconductor's H01U-G3 process, a low phase noise InGaP/GaAs HBT technology [120, 124]. The VCO core used in this design employs a simple Colpitts-like feedback with the same circuit topology previously described in [180], but

with the on-chip resonator removed and replaced with 150 μm GSG pads. The HBT transistor is a two-finger $1.6 \times 20\,\mu$m device, chosen based on the desired maximum output power. Importantly, this Colpitts-like feedback implementation uses on-chip metal-insulator-metal (MIM) capacitors with Q factors > 100 at 4.6 GHz, with a Colpitts ratio of 0.3, which should not cause a limitation on the phase noise when compared to the glass resonators. An additional 0.4 pF shunt capacitor is added to slightly adjust the resonant frequency of the oscillators to the target frequency. Voltage tuned frequency control is achieved with two weakly coupled back-to-back two finger $8 \times 10\,\mu$m shunt hyper-abrupt varactor diodes, with a simulated component Q of > 100 when biased between 5-10 V at 4.6 GHz. The resonators are coupled to the VCO core using an on-chip 0.8 pF capacitor with simulated component Q of Q=500 at 4.6 GHz. A diagram of the $1.2 \times 2.3\,\text{mm}^2$ MMIC layout without the glass resonators is shown in Fig. 5.9, with the resonator GSG pads on the left side and the RF oscillator output GSG pads on the right side. Note that the bond wires and coupling structure are accounted for in the co-simulations.

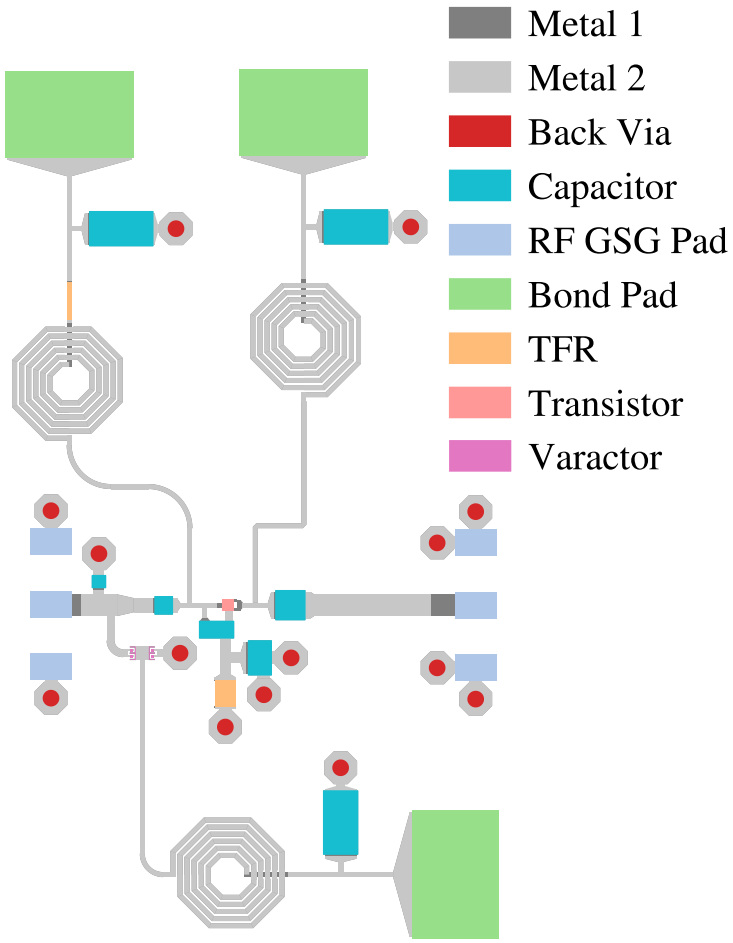


Figure 5.9: Layout of InGaP/GaAs oscillator MMIC without glass-embedded resonators. The HBT transistor is a two-finger $1.6 \times 20\,\mu$m device, chosen based on the desired maximum output power.

5.3 Oscillator Measurements

For the hybrid integration, the glass die is first mounted onto a copper molybdenum (CuMo) carrier. Then the MMIC die are affixed on top of the open gold-plated area of the glass die, with TGVs providing ground to the bottom metal layer of the glass which is then placed onto the probe station chuck. The GSG on the MMIC die containing the oscillator core are then wire bonded to the GSG of the glass embedded resonators. The mounting described here is chosen due to ease of fabrication, resulting in the resonators being loaded by CuMo carrier on one side which is tied to ground. Alternative mounting schemes where the resonators have air boundary conditions on both

sides, such as a cavity, are possible but not explored in this work. An example photograph of the bond wire integration is shown in Fig. 5.10.

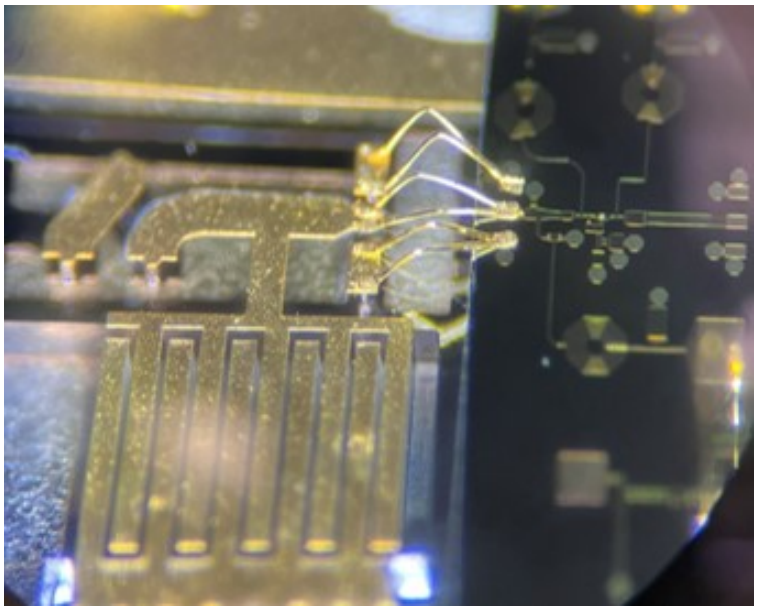


Figure 5.10: Photograph of the hybridly integrated InGaP/GaAs MMIC Oscillator and glass-embedded resonator via bond wire.

The free-running integrated oscillators are characterized using a Rohde-Schwarz FSWP8 phase noise analyzer, and powered by the instrument's internal low-noise dc power supplies. The oscillators are directly measured using a standard vibration-isolated probe station with dc probes and 150 μm RF probes landed on the MMIC die. Measurements are repeated over various dc bias points to find improved operating points. At a bias point of $V_c = 4.1\,\mathrm{V}, I_c = 22.2\,\mathrm{mA}$ and $V_b = 2.8\,\mathrm{V}, I_b = 270\,\mu\mathrm{A}$ the output frequency is tuned through the hyperfine transition of ^{133}Cs (4.596 GHz) with an output power of +12.7 dBm. The total dc power consumption of the oscillator is 91 mW. The oscillation frequency, tuning gain (MHz/V), and output power versus varactor voltage are shown in Figs. 5.11 and 5.12. The phase noise at various offset frequencies from 4.596 GHz is swept over the varactor voltage range is shown Fig. 5.13.

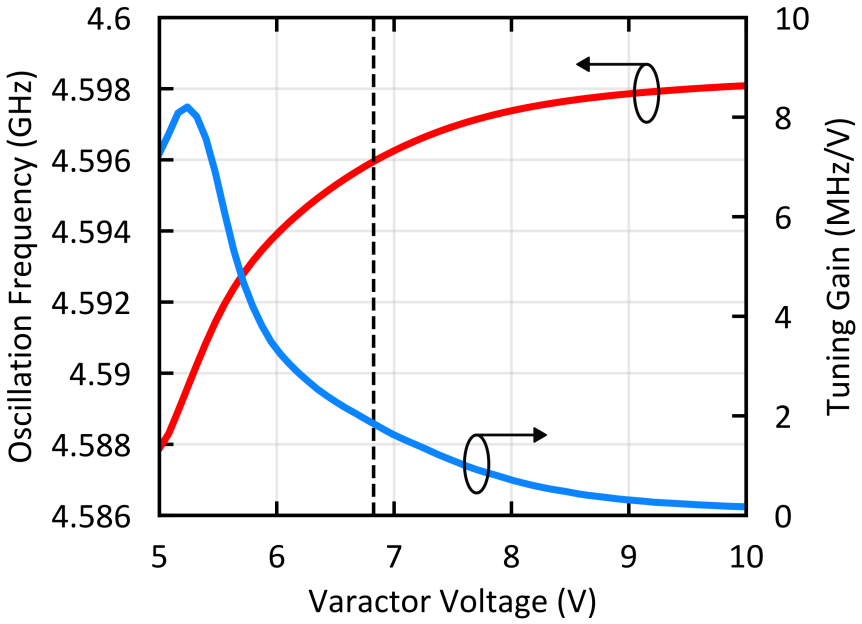


Figure 5.11: Measured oscillation frequency and tuning gain (MHz/V) swept over varactor voltage when biased at $V_c = 4.1\,\mathrm{V}, I_c = 22.2\,\mathrm{mA}$ and $V_b = 2.8\,\mathrm{V}, I_b = 270\,\mu\mathrm{A}$.

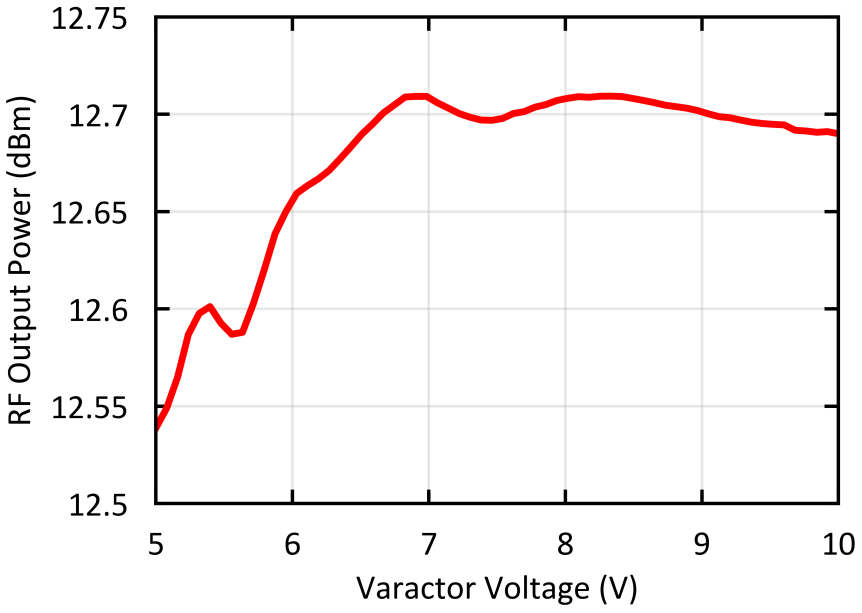


Figure 5.12: Measured output power versus varactor voltage when biased at $V_c = 4.1\,\mathrm{V}, I_c = 22.2\,\mathrm{mA}$ and $V_b = 2.8\,\mathrm{V}, I_b = 270\,\mu\mathrm{A}$.

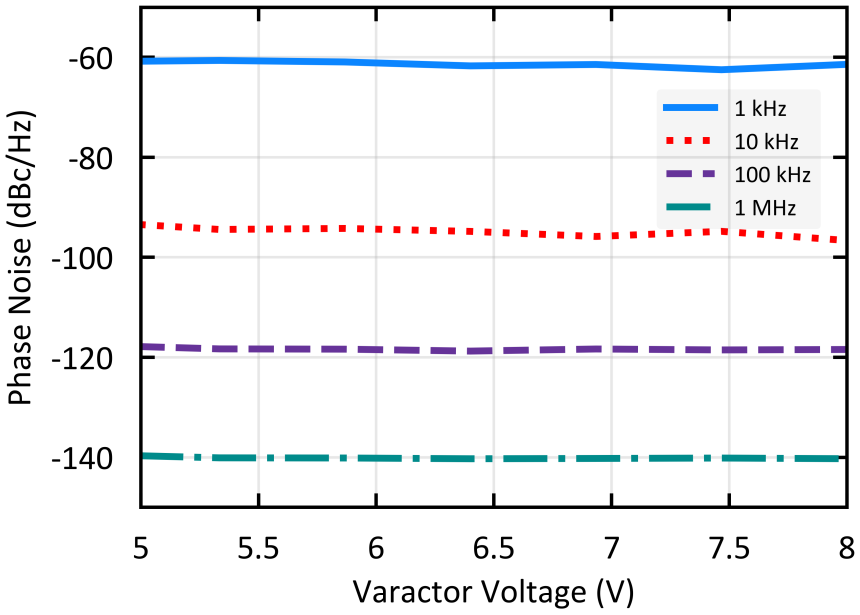


Figure 5.13: Measured phase noise at various offset frequencies from 4.596 GHz versus varactor voltage, when biased at $V_c = 4.1\,\mathrm{V}, I_c = 22.2\,\mathrm{mA}$ and $V_b = 2.8\,\mathrm{V}, I_b = 270\,\mu\mathrm{A}$.

The measured phase noise versus offset frequency of the free-running integrated oscillators operating at two different bias points is shown in Fig. 5.14, with the best reported phase noise shown in blue at a slightly different output frequency (4.641 GHz). The alternative bias point is $V_c = 3.3\,\mathrm{V}, I_c = 15\,\mathrm{mA}$ and $V_b = 2.2\,\mathrm{V}, I_b = 45\,\mu\mathrm{A}$. Simulated phase noise results are shown in dashed lines, noting that the foundry models do not provide data on added noise past the flicker corner. Also presented on the same plot is the reported free-running and PLL-locked oscillator phase noise from the "ULPAC" [30], which represents an example of the state-of-the-art in oscillators for CSACs. At the cost of higher power consumption, the oscillators reported here provide up to a 40 dB improvement in phase noise noise for the free-running oscillator case compared to the "ULPAC" oscillator.

Table 5.1 shows a comparison to a few other free-running oscillators for CSACs and RF front-ends for communications. The oscillators presented here are all integrated circuit implementations, occupying a few mm^3 with most consuming $< 100\,\mathrm{mW}$ dc power. In order to compare the

performance between different architectures, the following figure of merit (FoM) is adopted:

$$\mathrm{FoM} = \mathcal{L}(f_{\mathrm{offset}}) - 20\log\left(\frac{f_0}{f_{\mathrm{offset}}}\right) + 10\log\left(\frac{P_{\mathrm{dc}}}{1\,\mathrm{mW}}\right) \tag{5.1}$$

Note that this commonly used figure of merit does not include tuning range or RF output power.

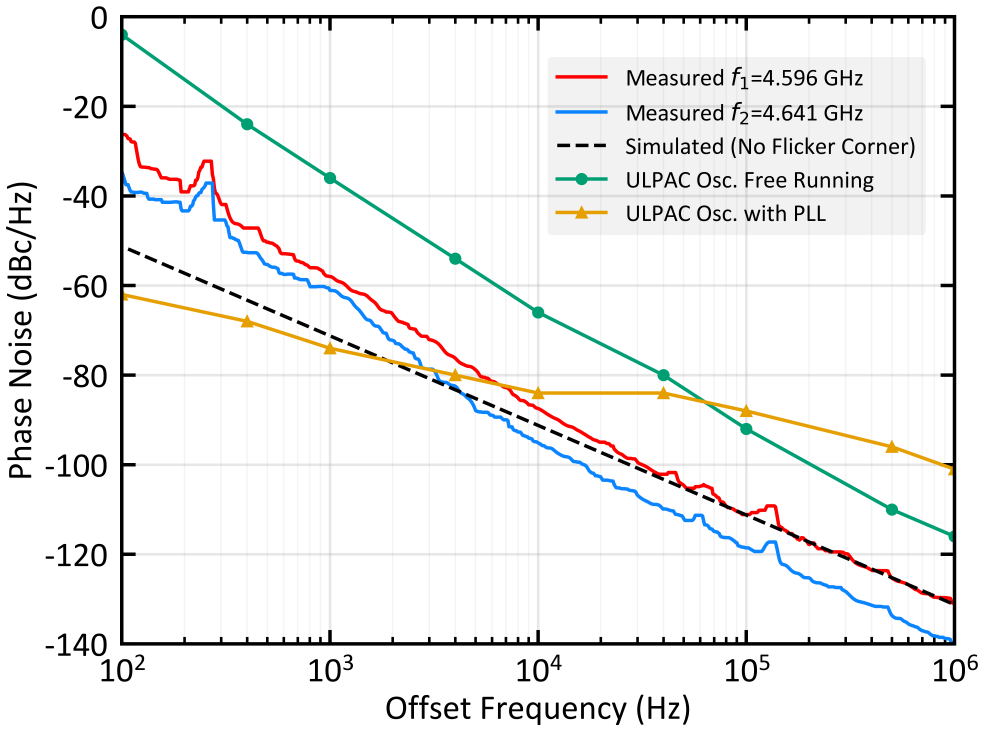


Figure 5.14: Measured and simulated phase noise versus offset frequency. When biased at $V_c = 4.1\,\mathrm{V}, I_c = 22.2\,\mathrm{mA}$ and $V_b = 2.8\,\mathrm{V}, I_b = 270\,\mu\mathrm{A}$, the oscillator outputs is at 4.596 GHz. An alternative bias point is presented showing a phase noise improvement at a different output frequency. Additional traces are provided using data from [30] as an example of the state-of-the-art for VCOs in CSACs.

Table 5.1: Comparison of Free-running Oscillators

Technology	f_0 (GHz)	f_{BW} (%)	P_{dc} (mW)	PN @ 1kHz (dBc/Hz)	PN @ 10kHz (dBc/Hz)	PN @ 1MHz (dBc/Hz)	P_{out} (dBm)	FoM (dBc/Hz)	Ref.
InGaP/GaAs HBT	4.596	0.04	91	-58	-87	-131	12.7	-185	This Work
InGaP/GaAs HBT	4.641	0.04	55	-61	-95	-140	11.1	-196	This Work
65-nm CMOS	4.596	N/A	14.1	-36*	-68*	-116*	6	-178	[30]
65-nm CMOS	4.596	8.7	1	-45	-70	-120	N/A	-194	[165]
InGaP/GaAs HBT	4.56	5	39.2	-52	-81	N/A	14	N/A	[180]
65-nm CMOS+FBAR	3.417	0.01	9	-55*	-90*	-140	-15*	-201	[86]
65-nm CMOS+FBAR	2	N/A	0.35	-70*	-97*	-140*	-20	-211	[190]
65-nm CMOS+FBAR	3.4	N/A	20	-80	-110	-153*	-12	-211	[191]
130-nm CMOS+FBAR	1.925	N/A	1.6	-88.3	-116	-146	0*	-210	[192]
InGaP/GaAs HBT	3.74	23	400	N/A	-85	-135	11	-180	[124]
InGaP HBT	9.05	14.3	N/A	-40*	-75*	-130*	7	N/A	[58]
InGaP HBT	9.2	N/A	N/A	-60*	-87*	-139*	7	N/A	[58]

* Estimated from published figures

5.4 Clock Integration Tests with Miniaturized Beam Clock

As a proof of concept for the oscillator's ability to lock to the atomic transition of Cs in the experimental atom beam clock, the free-running oscillator is mounted on a probe station and stabilized using an Analog Devices ADF-4007 phase locked loop (PLL) evaluation board with an external loop filter. The oscillator's dc bias is provided by a pair of low noise, battery supplied low-dropout regulator boards. The PLL board uses a AD9956 direct digital synthesizer (DDS) as it's tunable internal reference, and the DDS is finally referenced to a hydrogen MASER as shown in Fig.5.15.

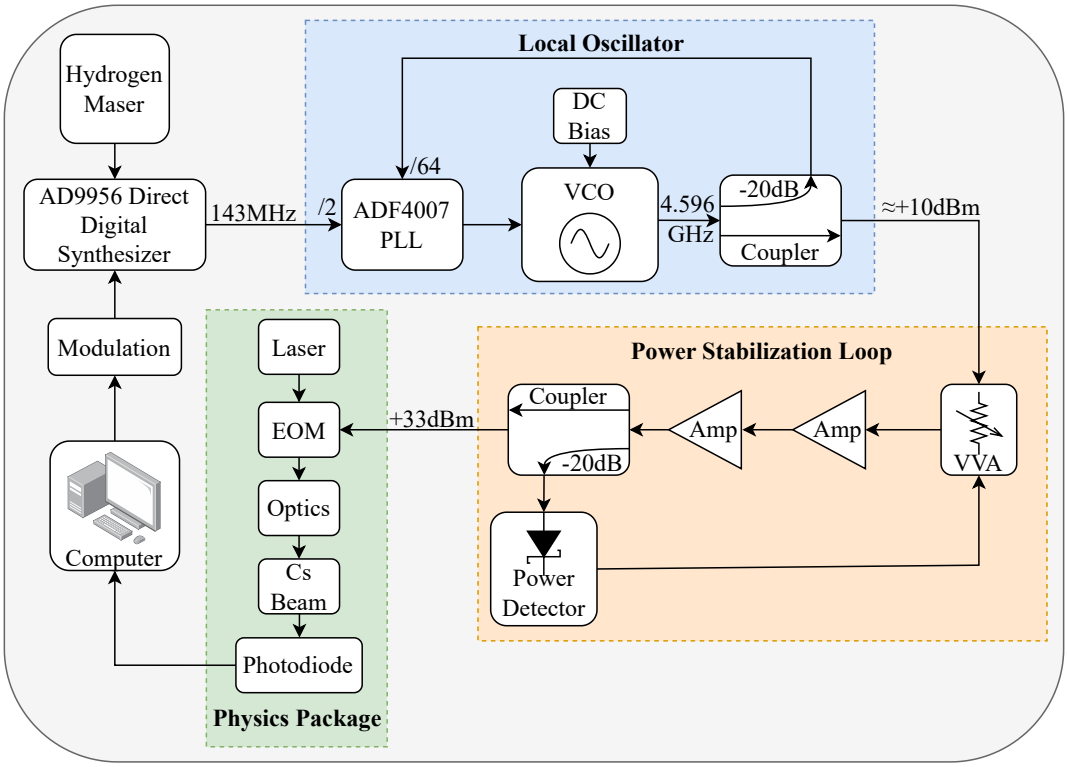


Figure 5.15: Block diagram of the MMIC VCO testing with the chip-scale atomic beam clock. The VCO output is used to drive a fiber-optic EOM to generate sidebands on a laser beam which are resonant with the desired Cs transition. Fluorescence from the atoms is used to discipline the PLL reference frequency input.

Corrections while maintaining a lock to the atomic resonance are then applied directly to the DDS, which in turn tunes the oscillator via the PLL board. In a fully integrated chip-scale clock, the PLL would likely be integrated with a voltage controlled quartz oscillator (VCXO) instead of a tunable DDS and the VCO output would be used to modulate the current of low-power vertical cavity surface emitting laser (VCSEL) instead of driving the fiber-optic EOM used in this demonstration.

The measured oscillator phase noise for both free-running and PLL modes while in the experimental beam clock test setup are shown in Fig 5.16. The previous measurement is shown in red for comparison. A small reduction in phase noise performance is seen, due to difference in dc biasing, lack of vibration isolation, increased noise, and probe setup. When locked within the PLL referenced to a hydrogen MASER, the theoretical limitation on the total clock stability due to the oscillator via the intermodulation effect is between $\sigma_y = 10^{-11}/\sqrt{\tau}$ and $10^{-12}/\sqrt{\tau}$ for modulation frequencies between 0.1 kHz and 10 kHz. The free-running oscillator can support $\sigma_y = 10^{-10}/\sqrt{\tau}$ over most of this modulation frequency range.

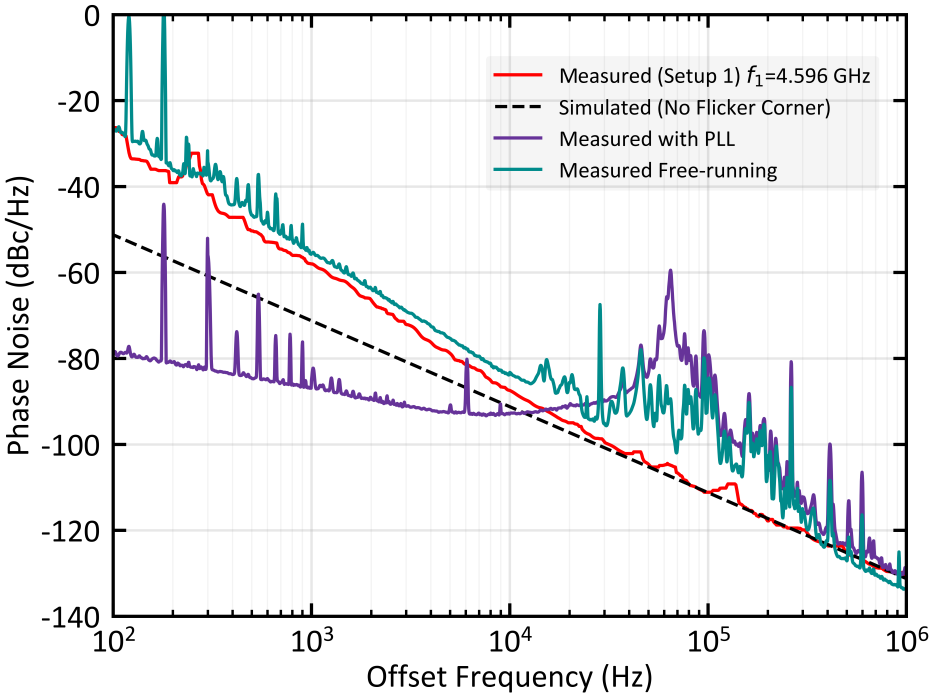


Figure 5.16: Measured and simulated phase noise versus offset frequency at an output frequency of 4.596 GHz for free-running and PLL-locked conditions. A previous measurement is shown in red from Fig. 5.14 for comparison, showing a degradation in phase noise due to the test setup.

Feedback using the atomic beam signal is realized by interrogating a magnetic field insensitive transition between the ground state levels of atomic Cs near 9.192 GHz using two-zone (Ramsey) coherent population trapping (CPT) spectroscopy similar to the work presented in [36]. The transition is driven by two laser fields created using the ± 1 order sidebands from a phase modulated laser whose frequency difference is resonant with the CPT transition. These sidebands are generated using a fiber EO phase modulator, driven by the PLL-stabilized MMIC VCO drive near $f_0 \approx 4.596$ GHz as shown in Fig. 5.15. An example of the CPT resonance interrogated in this fashion is shown in Fig. 5.17 where the atomic fluorescence varies with the MMIC VCO frequency relative to the two-photon resonance.

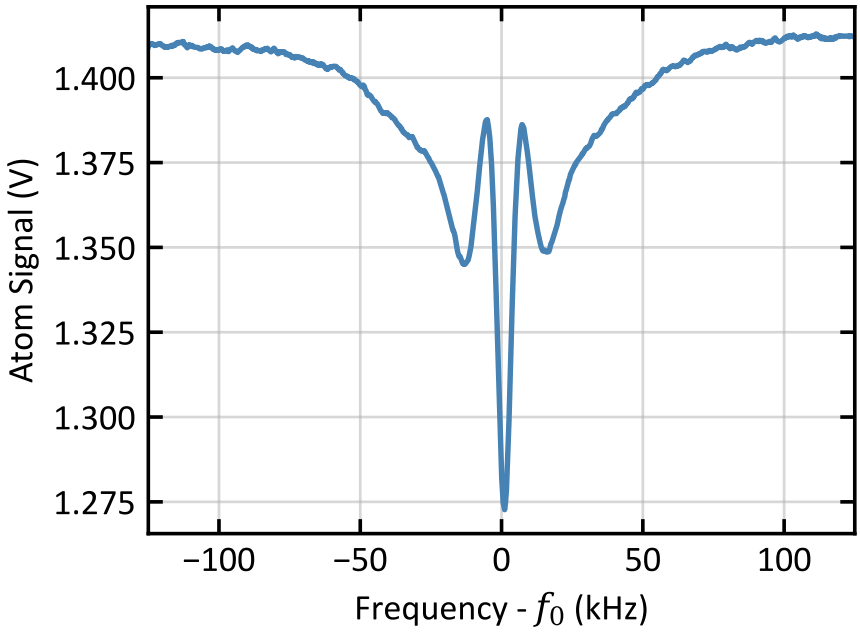


Figure 5.17: Measured atomic fluorescence from the chip-scale Cs atomic beam using the MMIC+PLL to scan over the clock CPT Ramsey fringe, where f_0 = 4,596,315,885 Hz is half the ground state hyperfine splitting of Cs.

The narrow resonance feature near f_0 is the clock signal with a width of ≈ 10 kHz. The center of this resonance is lock-in detected using square-wave frequency shift-keying the oscillator frequency by ±2.5 kHz at a modulation frequency $f_{\mathrm{mod}} \approx 200\,\mathrm{Hz}$. The difference in atomic fluorescence measured at the two frequencies is used to form an error signal which updates the center frequency of the reference DDS for the PLL using digital feedback. The performance of this feedback loop is limited by the detection SNR of the atomic signal, which can vary with the atomic flux, properties of the fluorescence collection, and probing power. A typical clock stability is shown in Fig. 5.18, where the fractional frequency stability is measured using the overlapping Allan deviation method. The clock demonstrates white-noise limited performance from 1-100 s, averaging as $\sigma_y \approx 3.3 \times 10^{-10}/\sqrt{\tau}$ using a laboratory frequency synthesizer to drive the EOM. Driving with the PLL-locked MMIC VCO yields the same clock stability, and no degradation using this approach is observed.

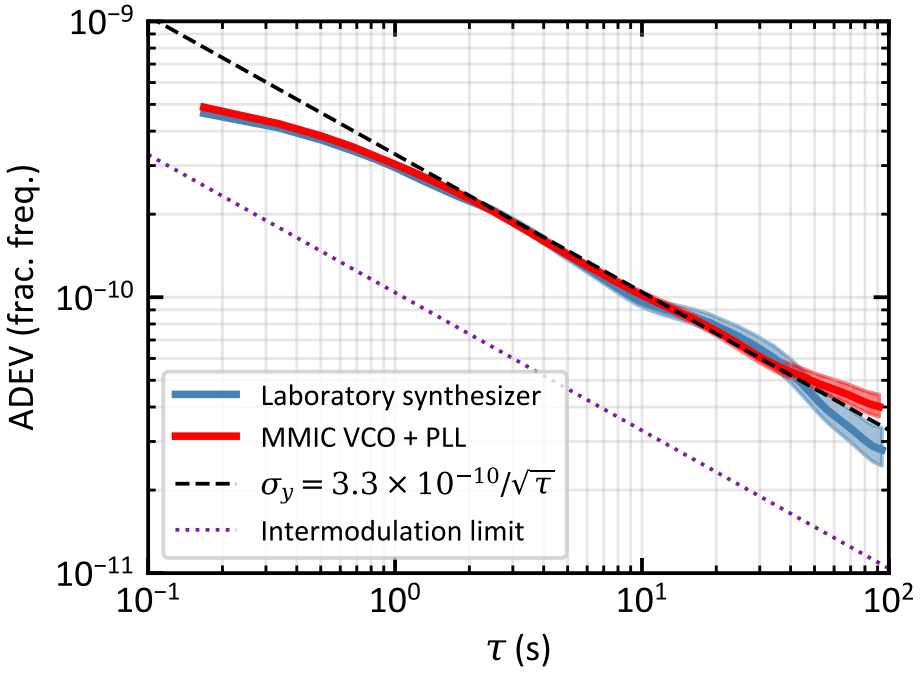


Figure 5.18: Comparison of the clock stability (overlapping Allan deviation) using the PLL-locked MMIC VCO (red) and a laboratory synthesizer (blue) to interrogate the clock transition in the chip-scale atomic beam device. No reduction of performance is observed using the MMIC VCO, and white-noise limited averaging (dashed line) is shown out to 100 s of integration time. The intermodulation noise limit for the free-running oscillator (dotted purple line) is shown for $f_{\text{mod}} =$ 200 Hz, where phase noise is ≈ -50 dBc/Hz. Shaded ares indicated the standard uncertainty for the ADEV data.

5.5 Conclusion

This chapter presents the design and measurements of a novel InGaP/GaAs HBT oscillator for a chip-scale atomic beam clock, integrated in a hybrid scheme with a relatively higher Q 3-D glass-embedded resonator when compared to on-chip resonators. The resonators themselves achieve a maximum unloaded quality factor of $Q_u = 107$ at a resonant frequency of 8.8 GHz. The oscillator after integration with the 3-D resonator results in a measured free-running phase noise of -58 dBc/Hz at an offset of 1 kHz and -140/,dBc/Hz at an offset of 1 MHz from the half of a

hyperfine transition frequency of ^{133}Cs, depending on bias condition. The output power reaches a peak of +13 dBm while consuming a dc power of 91 mW. The VCO is then tested with an off-chip commercial PLL to drive an experimental chip-scale atomic beam clock as a proof of concept for a future highly integrated timing system. Measured ADEV on the order of $\sigma_y \approx 3.3 \times 10^{-10}/\sqrt{\tau}$ from 1-100 s is presented, showing no degradation in stability compared to a commercial bench-top synthesizer. The work in this chapter has been submitted for review in [193].

Chapter 6

Balanced Oscillator InGaP/GaAs HBT MMICs for CSACs

During integration testing of the single-ended MMIC oscillators from Chapter 5 and the external CSAC control board ASIC, changes in system-level specifications, such as a reduction in tuning voltage, were identified for a new iteration of the MMIC VCO design. The new target design goals are presented in Table 6.1 and include a reduced oscillator frequency tuning gain (MHz/V), a lower required maximum voltage to create a 4.596 GHz oscillation frequency, and a lower RF output power.

Table 6.1: Second-iteration VCO design target specifications for the chip-scale atomic beam clock

f_0 (GHz)	Tuning Gain	Phase Noise @ 10kHz	Output Power	Temperature Variation	P_{dc} (mW)
4.596	17 MHz/V	-80 dBc/Hz	0 to +4 dBm	0.5 MHz/°C	50

An additional priority is to improve the consistency of the oscillator performance over the required frequency tuning range. In order to meet these requirements, the balanced Colpitts oscillator topology is selected for the second MMIC VCO design, due to its ability to reject common-mode noise. This topology has been used to demonstrate some of the lowest reported phase noise oscillators from K to X-band, at the cost of higher dc power consumption [176, 194, 195]. To realize this circuit, two transistors share a common node, which acts as a virtual ground between the two devices. Each half of the balanced circuit is designed to oscillate 180° out of phase relative to the

other oscillating transistor. When the two differential branches are combined using an external 180° combiner circuit, the desired oscillation mode combines constructively, while any common-mode noise cancels. The InGaP/GaAs HBT process used for the balanced MMIC VCOs presented in this chapter is the same as that used for the previous single-ended Colpitts oscillator MMICs.

6.1 Balanced Colpitts Oscillator MMIC Circuit Design

The initial schematic topology is based on the circuit design equations presented in [58]. The final circuit is shown in Fig. 6.1, and the initial component values for a target resonator impedance (Z_c), oscillation frequency (ω_0), component quality factor (Q) and capacitance division ratio (n), are calculated using the following equations [58]:

$$L_{\text{tank}} = \frac{Z_c}{\omega_0}, \qquad C_1 = \frac{1}{Z_c\omega_0(1-n)}, \qquad C_2 = \frac{1}{Z_c\omega_0 n}, \qquad R_e = QZ_c n, \tag{6.1}$$

where the design frequency is chosen as $\omega_0 = 2\pi f_0 = 2\pi \cdot 4.596\,\text{GHz}$. In the design presented here, eqns. (6.1) result in the initial component values, given a target division ratio of $n = 0.3$ and resonator impedance of $Z_c = 9.5\,\Omega$. These initial component values are then adjusted to the final values used in the design layout based on transistor, varactor, and interconnect impedances to $C_1 = 4.9\,\text{pF}$ and $C_2 = 5.7\,\text{pF}$, an emitter degeneration resistor value of $R_e = 100\,\Omega$, and a tank inductance $L_{\text{tank}} = 0.3\,\text{nH}$. The selected transistor is a 2-finger $10 \times 1.6\,\mu\text{m}$ device, sized based on the desired output power requirements and foundry validated transistor models. Narrowband frequency control is achieved using a 2-finger $8\times10\,\mu\text{m}$ hyper-abrupt varactor diode coupled through a series 2 pF capacitor C_v, providing a tuning gain of 17 MHz/V. The base and varactor diodes are resistively biased using $R_b = 5.5\,\text{k}\Omega$ and $R_v = 1.5\,k\Omega$ resistors respectively. The RF output is coupled through 0.5 pF series capacitors to differential $150\mu\text{m}$ GSGSG pads. The resulting circuit schematic is shown in Fig. 6.1.

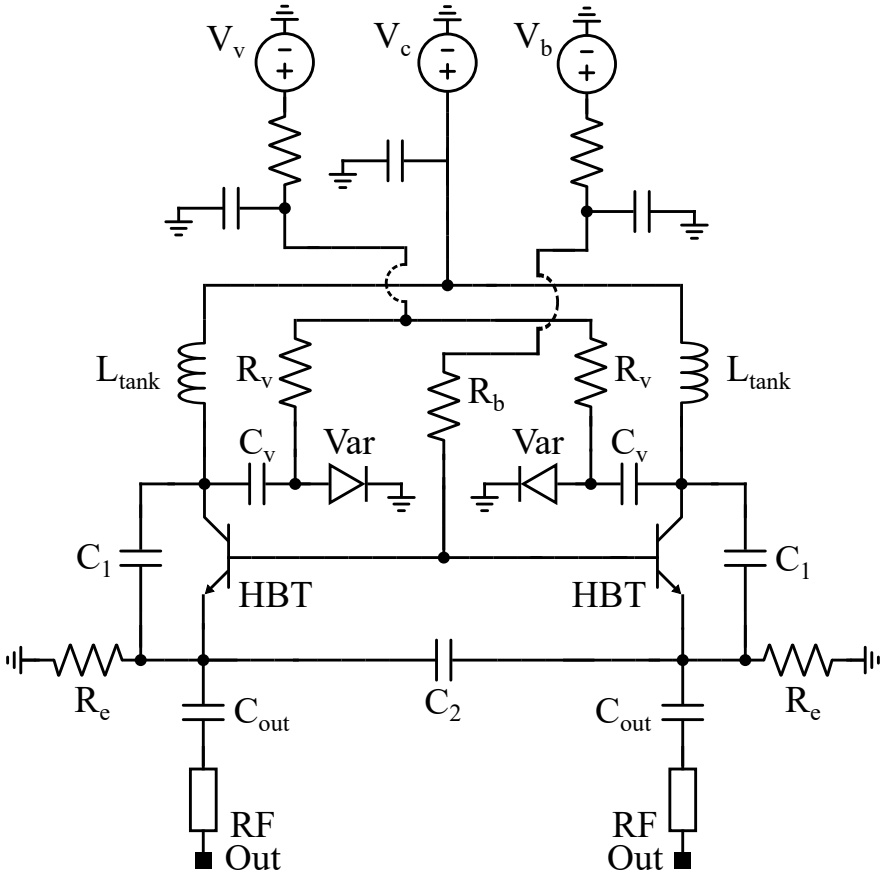


Figure 6.1: Balanced Colpitts circuit schematic, where the initial values of the elements C_1, C_2, L_{tank} and R_e are given by eqns. 6.1.

The design is full-wave simulated in Cadence AWR using foundry nonlinear models for the H01U-G3 InGaP/GaAs HBT process provided by WIN Semiconductors. Steps are taken to reduce the circuit layout area as much as possible, such as bending the metal layers of the Colpitts feedback capacitor around the transistors to reduce interconnect length and using both capacitor metal layers for nodal connections to R_e and C_{out}. The width of the tank inductor is optimized in simulation to maximize Q-factor at the oscillation frequency, while still being reasonably sized for meandering around the transistors and connecting the two differential branches together. Careful simulation and sizing of the inductor air bridges is performed to reduce the effect of coupling between metal layers. As an added step to reduce potential noise from the power supply coupling into the tank inductor, the bias resistance for both V_b and V_v is separated into two parts before and after the

inductor air bridge. Additional 5 pF shunt decoupling capacitors are added near all dc bias pads for additional power supply filtering. An attempt to maintain symmetry between the balanced branches is conducted throughout the layout process where possible. The full layout occupies $1.2 \times 1.5\,\text{mm}^2$, and is shown in Fig. 6.2.

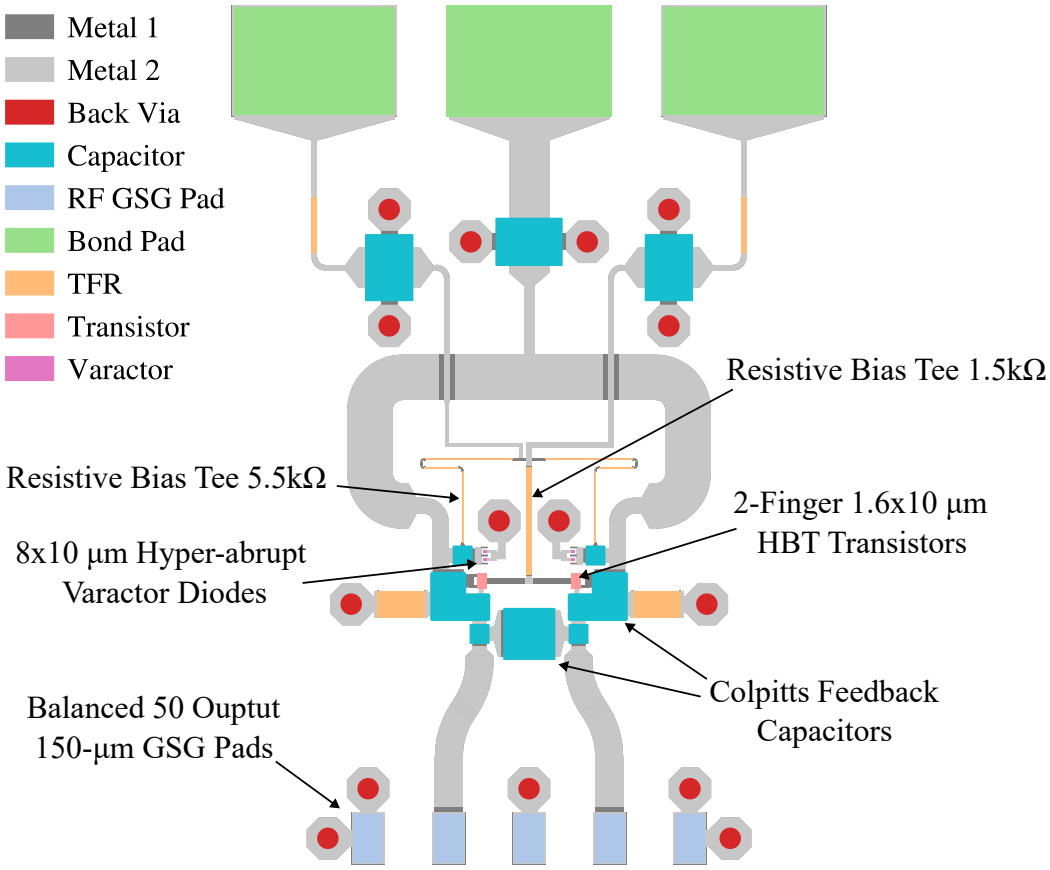


Figure 6.2: Balanced VCO MMIC layout in the WIN Semiconductors' H01U-G3 InGaP/GaAs HBT process. The entire circuit is 1.2 mm×1.5 mm in size.

6.1.1 Design Variations

One of the design challenges towards meeting the specifications in Table 6.1 is the reduced tuning gain and tuning voltage, motivated by the CMOS controls ASIC, effectively reducing the entire tuning range to 43 MHz at a fundamental output frequency of 4.596 GHz. Therefore, in

addition to the standard design shown in Fig. 6.2, a second design is fabricated using capacitors with interconnects that can be trimmed post-fabrication. An example of the layout for such a capacitor within the oscillator layout is shown in Fig. 6.3.

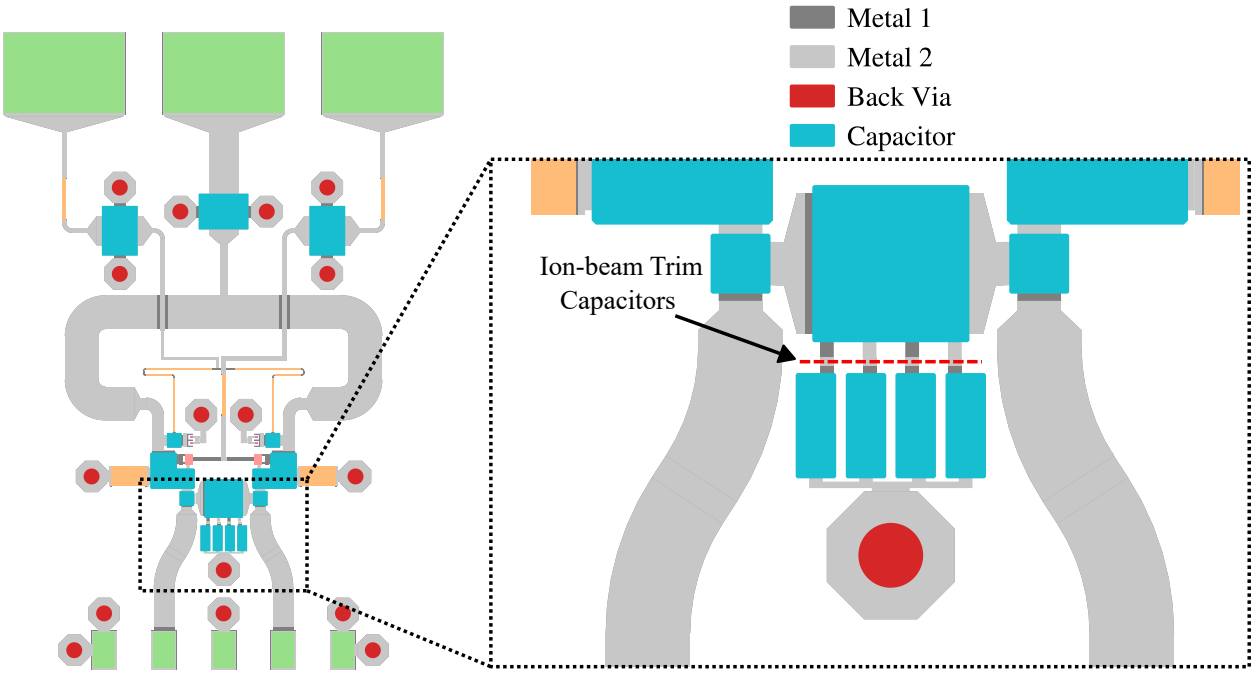


Figure 6.3: Detail of the balanced oscillator MMIC layout iteration using ion-beam trimmable capacitors to ensure that the output oscillation frequency is in the specified narrow range. The full layout on the left is identical to Fig. 6.2 besides the trimmable capacitors. A red dash line indicates the trim location.

Each of these capacitor interconnects can be disconnected from the circuit using ion beam trimming, changing the capacitor value of C_2 by 0.6 pF for each trim. This tunes the design $\approx$ 25 MHz per capacitor interconnect removed, for a total of approximately 100 MHz of post-fabrication tuning per design iteration. Therefore, any frequency shifts caused by component tolerances or model inaccuracies can be adjusted post-fabrication. In the final wafer distribution shown in Fig. 6.4, 32 design iterations are shown in the reticle layout with varying resonator lengths to ensure a final design can tune through the narrowband half-hyperine frequency with only 43 MHz

of total tuning range, as required by the CMOS locking circuit. Of these 32 designs, the bottom 10 layouts contain the trimmable capacitor designs. Using these added design iterations and post-fabrication trimmable capacitors results in a total simulated frequency coverage of 1 GHz, or 4.596 GHz ±500 MHz. The full wafer reticle layout is shown in Fig. 6.4.

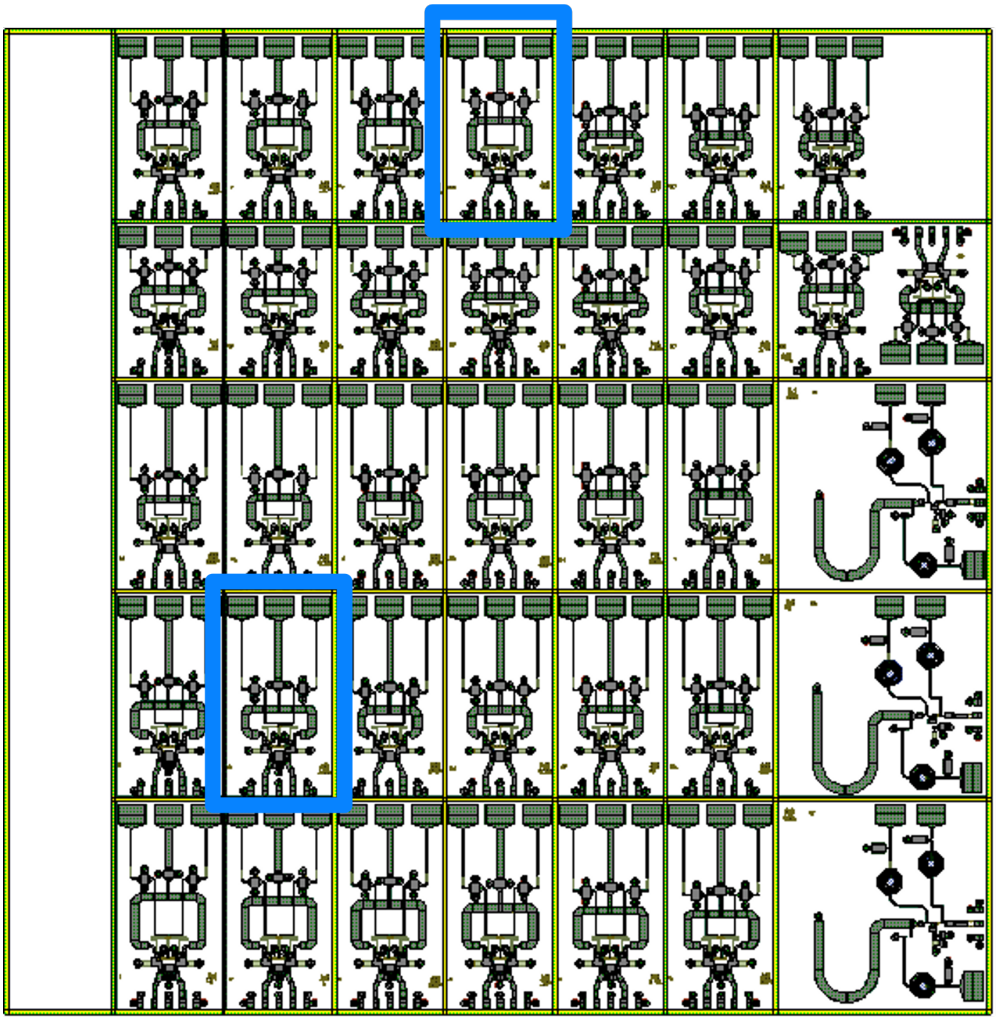
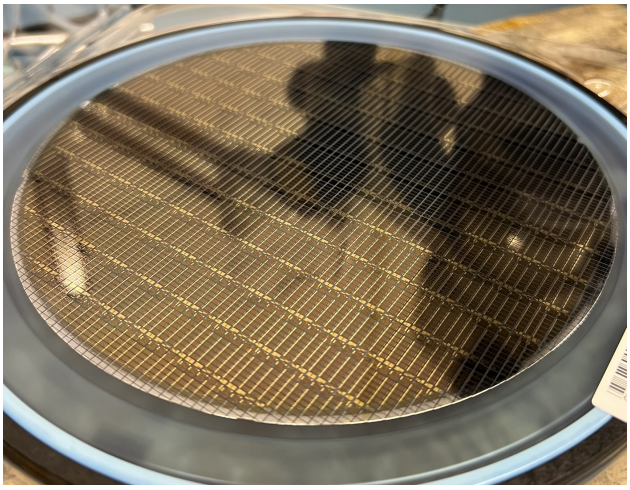


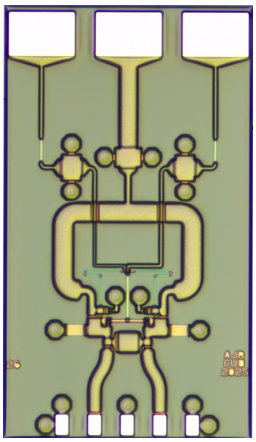
Figure 6.4: InGaP/GaAs HBT reticle layout including 32 VCO designs. Each design varies the differential resonator length, in order to adjust the output frequency. The bottom 10 layouts include trimmable capacitors. The three larger chips in the right-most column are repeated designs from Phase 1, included for comparison. The layouts highlighted in blue rectangles are the two die which are able to tune through 4.596 GHz, one with trim capacitors and one without.

6.2 Balanced VCO MMIC Measurements

The fabricated 6-inch InGaP/GaAs HBT wafer containing the 32 design iteration reticle shown in Fig. 6.5a. A close up photo of an individual MMIC die is shown in Fig. 6.5b.



(a)



(b)

Figure 6.5: (a) Photograph of 6-inch InGaP/GaAs HBT wafer showing the repeated reticle with 32 oscillator designs. (b) Photo of a characteristic single 1.6 mm×1. mm balanced MMIC VCO die.

All testing for the balanced oscillator MMICs is done on a standard probe station using a Keysight E5056A Signal Source Analyzer with a 150-μm GSGSG probe. All measurements are

converted from differential to the single ended input of the SSA using a 180-degree hybrid coupler, which has a measured loss of 2.3 dB and is de-embedded post-measurement. The MMIC is biased using the low-noise power supplies internal to the SSA, as shown in the sketch of the measurement setup in Fig. 6.6.

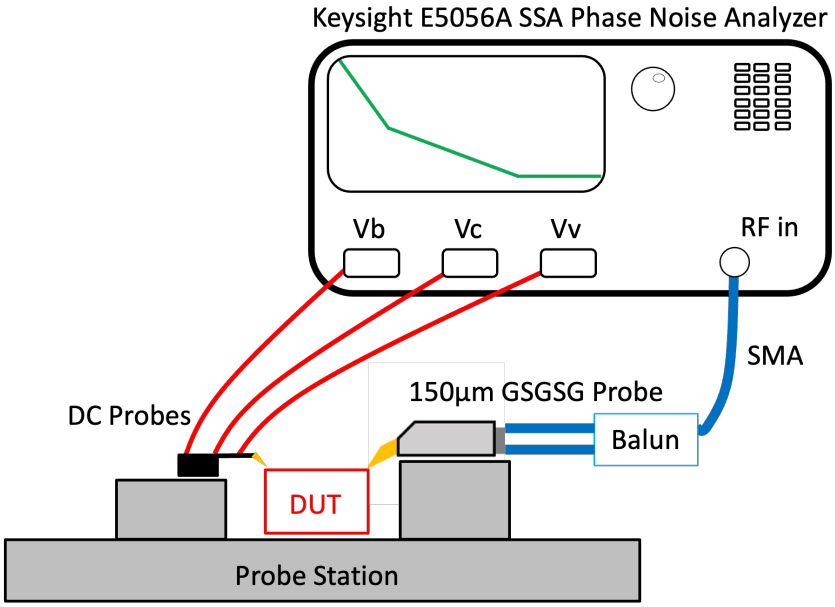


Figure 6.6: Sketch of measurement setup used to characterize the MMIC VCOs highlighted in blue rectangles in Fig. 6.4. Internal low-noise supplies of the phase noise analyzer are used for the collector (V_c) and base biases (V_b), as well as the varactor tuning voltage V_v. We thank Keysight for the loan of the E5056A SSA Phase Noise Analyzer.

First, each die was tested to identify which design iterations could tune through 4.596 GHz given the requirements. Two designs from the reticle are identified to have oscillation frequencies tunable through 4.596 GHz, one with and one without trimmable capacitors. For reference, these die are outlined in blue in Fig. 6.4, with Die 28 being the target design iteration used in the future chip-scale atomic beam clock. All three dc supplies (collector and base bias, as well as varactor control voltage) are swept while measuring phase noise, dc power consumption, RF output power, and output frequency. Fig. 6.7 shows the phase noise at 10 kHz vs. dc power consumption and

carrier output power for bias points with an output power greater than -2 dBm. Each measurement point is a different dc bias using the same individual die. This data shows the expected maximum and minimum noise and power consumption performance the VCO can provide, while providing the expected output power to the PLL. A Pareto front is also presented in teal, outlining points that are non-dominated, meaning these data points cannot be improved without making at least one other measurement variable worse. For this particular die, the maximum RF output power is +5 dBm. The power consumption and phase noise at a 10 kHz offset ranges from 15 to 90 mW and -57 to -83 dBc/Hz respectively, depending on bias condition. The data in Fig. 6.7 is filtered to only include bias points that tune through 4.596 GHz using the 0–2.5 V of tuning voltage (predicted for the CMOS ASIC) and is shown in Fig. 6.8.

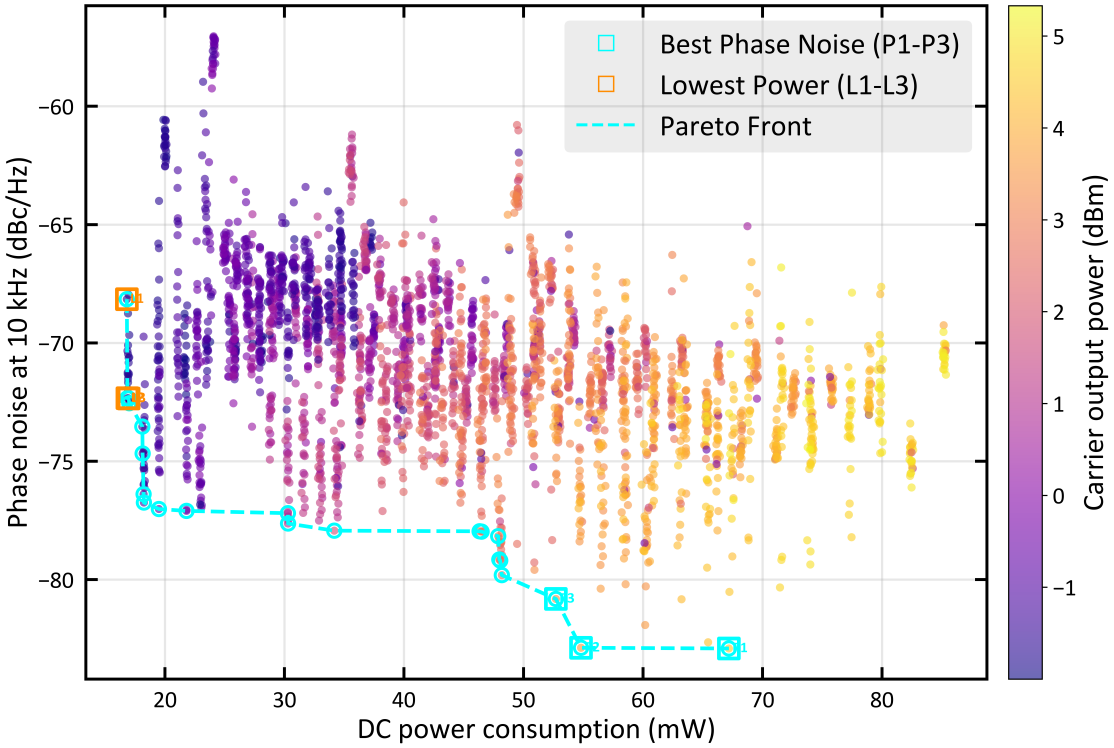


Figure 6.7: Measured phase noise vs. power consumption and RF output power at various oscillation frequencies for the balanced VCO MMIC Die 28. Measurements are performed across a bias range from 1.6 to 2.5 V for V_b, 1.6 to 3.5 V for V_c, and 0 to 2.5 V for V_v. The blue line presents a Pareto front of data points, meaning no other single data point is better than them in every metric. Three points also highlighted in orange/blue squares, depicting the highest performing bias points for phase noise and power consumption.

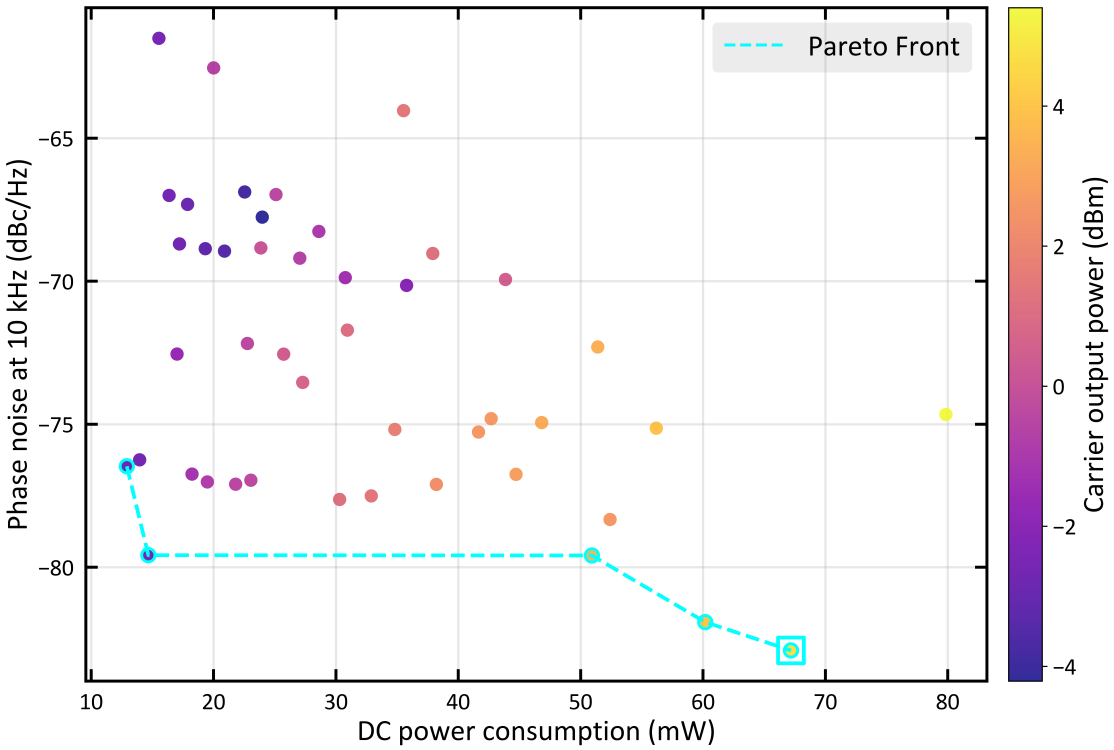


Figure 6.8: Measured phase noise vs. power consumption and RF output power at $f_0 = 4.596\,\text{GHz}$ for the balanced VCO MMIC Die 28. Measurements are performed across a bias range from 1.6 to 2.5 V for V_b, 1.6 to 3.5 V for V_c, and 0 to 2.5 V for V_v. The blue line presents a Pareto front of data points, meaning no other single data point is better than them in every metric.

This data represents the same MMIC VCO performance shown previously, but only for bias points that result in an oscillation frequency at the Cs hyperfine frequency of 4.596 GHz. The maximum RF output power remains around +5 dBm. The power consumption from 15 to 80 mW and phase noise at a 10 kHz offset ranges from -61.5 to -83 dBc/Hz, depending on bias condition. For future operation with the CMOS ASIC PLL, the optimal bias point for the VCO MMIC will be selected based on the results of future integration testing (see Chapter 7).

Of the bias points presented in Fig. 6.8, two bias points are selected as an example of expected performance in a high and low dc power consumption use-case. Further phase noise measurements for these two bias points to characterize the MMIC VCO phase noise vs. simulation are shown in

Fig. 6.9. A summary of the performance at these two selected bias points is shown in Table 6.2 for comparison.

Table 6.2: Balanced VCO Die 28 measured results summary at two bias points at $f_0 = 4.596\,\text{GHz}$

V_B	I_B	V_C	I_C	V_V	**PN @ 10 kHz**	**PN @ 1 MHz**	**Output Power**	**DC Power**
1.7 V	120 μA	1.8 V	8 mA	2.1 V	-79.6 dBc/Hz	-126 dBc/Hz	-2.5 dBm	13.6 mW
2.2 V	230 μA	3.5 V	19 mA	1.6 V	-83 dBc/Hz	-129 dBc/Hz	4.7 dBm	67 mW

Fig. 6.9 shows the measured (solid) and simulated (dashed) phase noise versus offset frequency from 4.596 GHz for both bias points. Both measurements show good agreement with simulation at higher frequency offsets beyond the flicker corner, which is not provided in the foundry transistor models. The phase noise for the higher power consumption bias point is better by nearly 3 dB across the offset frequency range, as expected. Overall, the phase noise shows a 1–5 dB improvement, depending on bias conditions, over the single-ended Colpitts oscillator MMICs from Chapter 5.

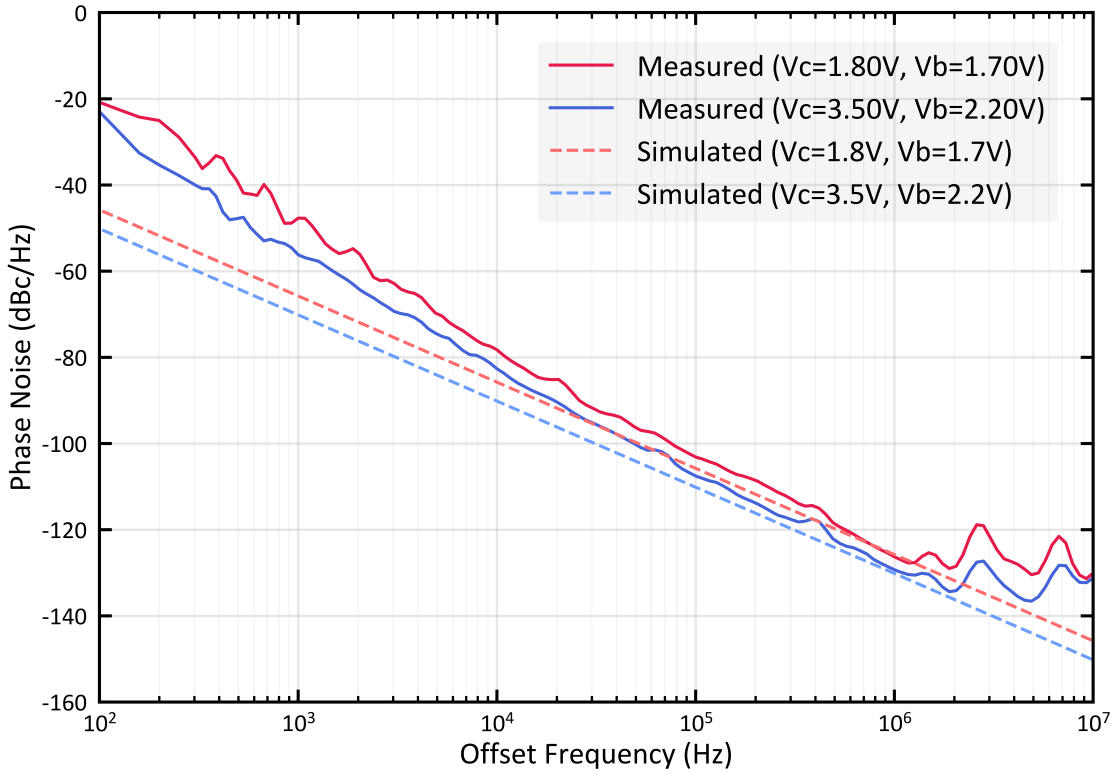
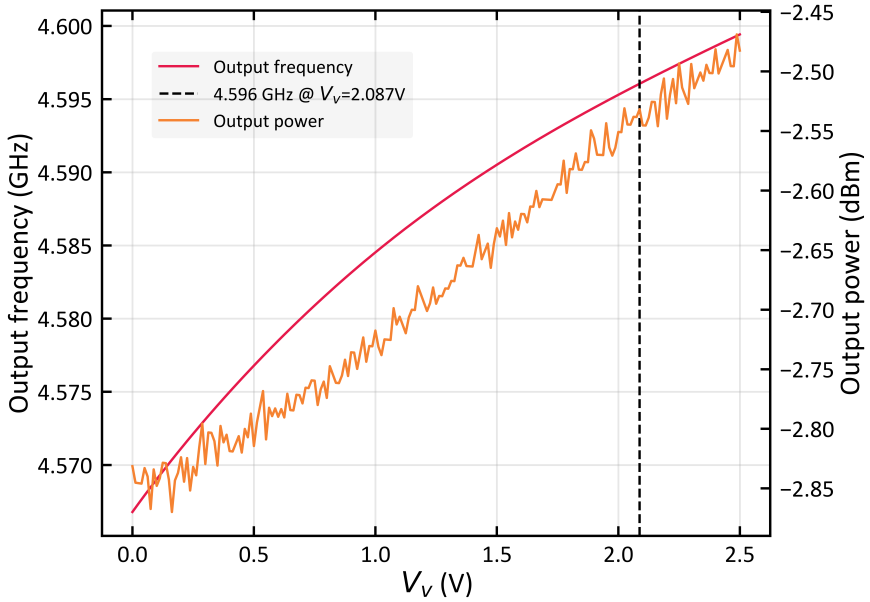
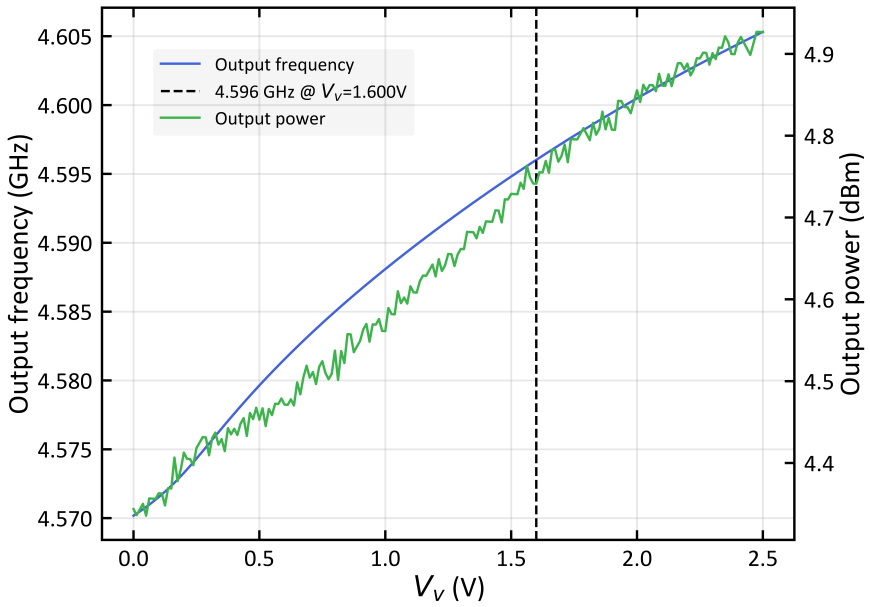


Figure 6.9: Measured (solid) and simulated (dashed) phase noise vs. offset frequency for two bias points: $V_b = 1.7V$, $I_b = 120\,\mu$A and $V_c = 1.8V$, $I_b = 8\,$mA in red; and $V_b = 2.2V$, $I_b = 230\,\mu$A and $V_c = 3.5V$, $I_b = 19\,$mA in blue. Models do not include the flicker corner. These measurements are performed with instrument averaging of 2, and trace smoothing of 1%.

As stated earlier, an important priority of the balanced VCO MMIC designs is consistent performance across the frequency tuning range. Figs. 6.10a and 6.10b show the measured output frequency and RF output power over the varactor tuning range (V_v) for the two chosen bias points presented previously, with the lower power consumption in red and orange and higher power consumption in blue and green. Both the RF output power and output frequency have a linear predictable increase across the 2.5 V tuning range. The lower power consumption bias point shows a linear 10% power variation from -2.8 to -2.35 dBm, while the higher power consumption case shows a 15% variation from 4.3 to 4.9 dBm. A vertical dashed line indicates the varactor control voltage (V_v) that corresponds to an output frequency of 4.596 GHz for each point.



(a)



(b)

Figure 6.10: (a) Output frequency (left, red) and output power (right, orange) vs. V_v for $V_b = 1.7V$, $I_b = 120\,\mu$A and $V_c = 1.8V$, $I_b = 8\,$mA. A dashed line shows the V_v value corresponding to 4.596 GHz. (b) Output frequency (left, blue) and output power (right, green) vs. V_v for $V_b = 2.2V$, $I_b = 230\,\mu$A and $V_c = 3.5V$, $I_b = 19\,$mA. A dashed line shows the V_v value corresponding to 4.596 GHz.

Another important metric identified from the integration testing of the MMICs in Chapter 5 was the VCO tuning gain, which is measured and presented for both bias points in Fig 6.11. For the lower power consumption bias point in red, the measured tuning gain when near 4.596 GHz is 8.5 MHz/V, while for the higher power consumption operating point in blue is is 12 MHz/V. Compared with the MMICs presented in Chapter 5 which had a tuning gain of 30-100 MHz/V depending on bias, the oscillators presented here show a major reduction in tuning sensitivity.

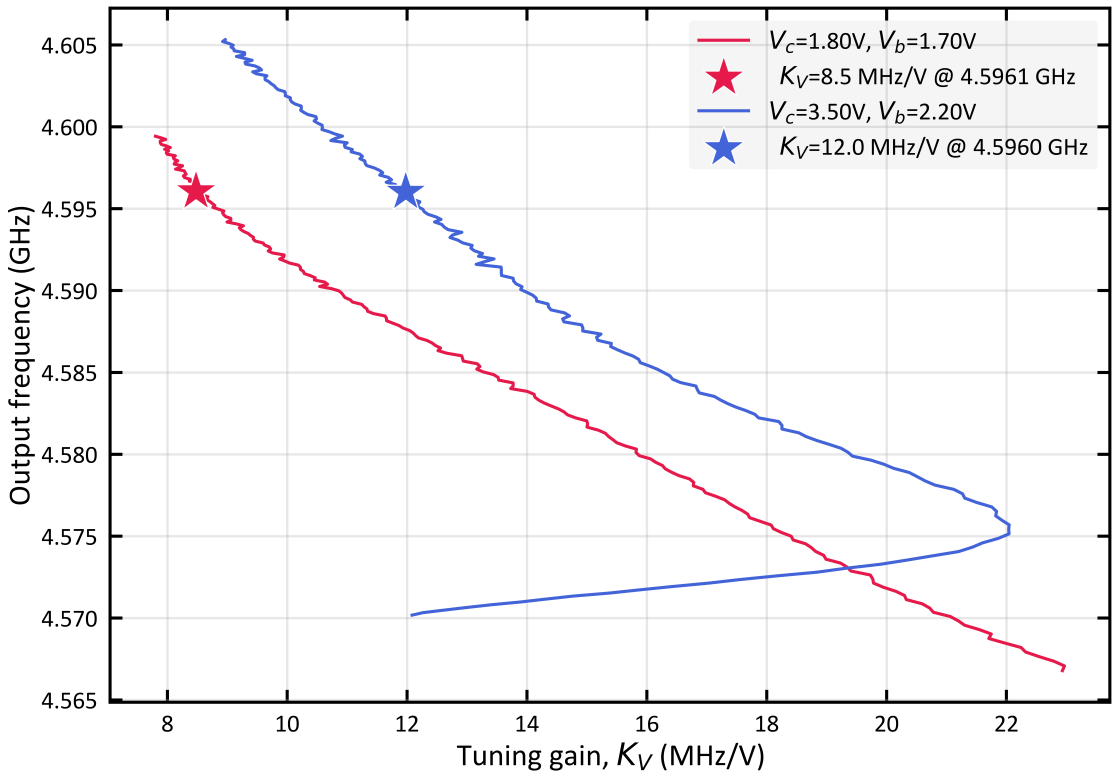
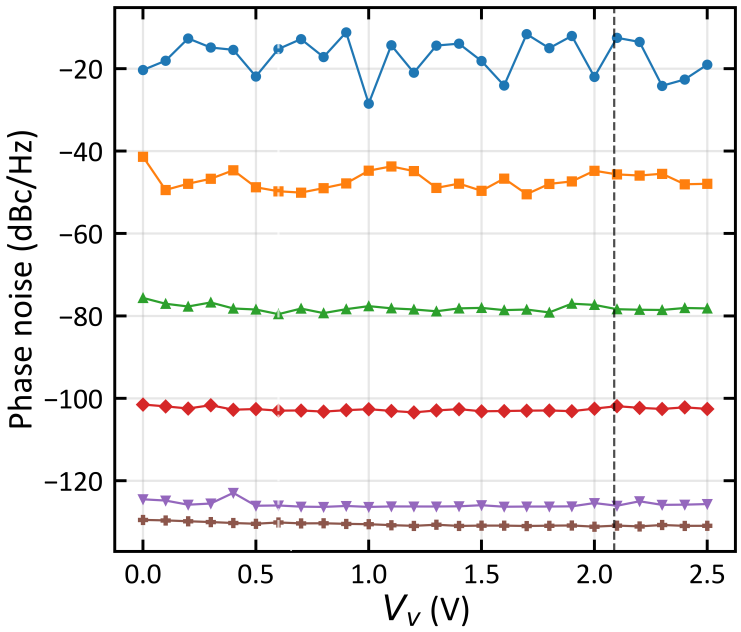


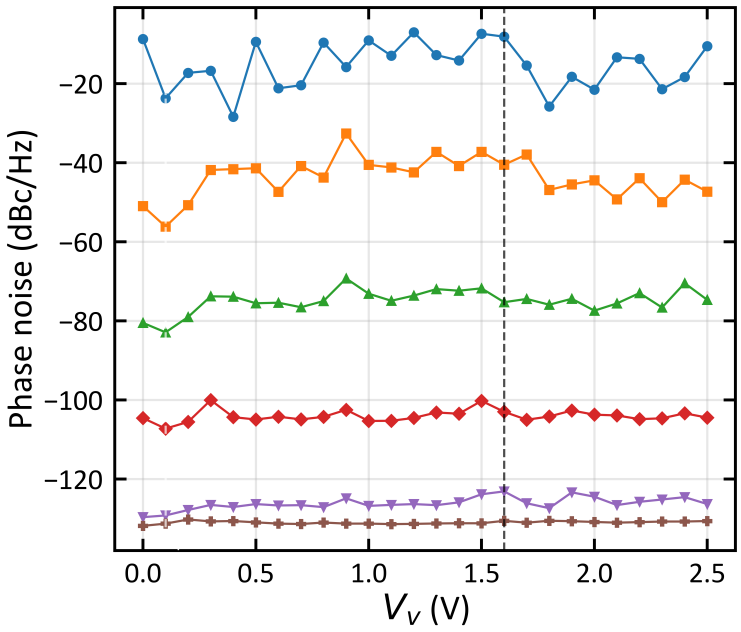
Figure 6.11: Measured output frequency vs. tuning gain (MHz/V) for $V_b = 1.7V$, $I_b = 120\,\mu$A and $V_c = 1.8V$, $I_b = 8$ mA in red, and $V_b = 2.2V$, $I_b = 230\,\mu$A and $V_c = 3.5V$, $I_b = 19$ mA in blue. Stars indicate the tuning gain when the output frequency is 4.596 GHz.

Finally, the measured phase noise versus V_v is shown in Fig 6.12 for both bias points. The lower bias point is shown on the left plot, showing the phase noise is mostly flat across the control voltage range. The higher bias point on the right has slightly more phase noise deviation across

the range, but is still generally flat. The phase noise at lower frequency offsets often shows more variation, due to the relative power levels for the carrier and close offset phase noise.



(a)



(b)

Figure 6.12: Measured phase noise for various offset frequencies from 4.596 GHz vs. V_v for two bias points: (a) $V_b = 1.7\,\mathrm{V}$, $I_b = 120\,\mu\mathrm{A}$, $V_c = 1.8\,\mathrm{V}$, $I_c = 8\,\mathrm{mA}$. (b) $V_b = 2.2\,\mathrm{V}$, $I_b = 230\,\mu\mathrm{A}$, $V_c = 3.5\,\mathrm{V}$, $I_c = 19\,\mathrm{mA}$. A dashed black line is presented for both, showing the V_v corresponding to a 4.596 GHz output frequency.

Further measurements on the temperature variation and output load pulling are yet to be performed due to equipment availability. When varying the transistor junction temperature using the large-signal foundry models in simulation over a temperature range from 20 to 100 °C , the balanced VCO output frequency shows a deviation of -0.02367 MHz/°C. The simulated effects output load pulling, assuming a 20 dB return loss with random phase, are ±2.5 MHz from the nominal output frequency.

6.3 Conclusion

In summary, this chapter presents the design, simulation, and measurements of a balanced MMIC VCO fabricated in an InGaP/GaAs HBT process for practical use in a new type of integrated Cs chip-scale atomic beam clock. These MMICs are designed as an extension of the VCOs designed in Chapter 5, based on integration results that resulted in modified specifications. Two different designs are taped out, resulting in 32 variations across the wafer reticle in order to meet the narrowband tuning requirements. Of these 32 variations, two individual die in the reticle are identified with tunable output frequencies including 4.596 GHz given a 2.5 V tuning range with a reduced target tuning gain of 17 MHz/V. One of these designs includes additional post-fabrication tuning capacitors which can be removed via ion beam trimming for additional frequency tuning if needed. Measured results show a 1–5 dB bias-dependent enhancement in phase noise from the single-ended oscillator MMICs shown in Chapter 5. The maximum output power for the balanced VCO MMICs is scaled back nearly 10 dB from the previous chips, resulting in an overall lower power consumption design while maintaining high performance in all metrics. The tuning gain, output power, and phase noise across the varactor tuning voltage range have been adjusted to be consistent across the range. Importantly, the MMIC oscillators presented here meet all of the system level requirements for the chip-scale atomic beam clock and have plans to be integrated into the full system in the future.

Chapter 7

Conclusions and Future Work

7.1 Thesis Summary

As microwave chip-scale atomic clocks continue to improve, potential for their application in many size- and power-constrained environments become available. Currently, these applications range from GPS receivers, oil exploration, to the energy grid. A key component of these CSACs is the microwave local oscillator, which has been identified as a potential limiting factor in new types of atomic interrogation schemes. This thesis begins by explaining the background of chip-scale atomic clocks and microwave oscillators. The impact of the local microwave oscillator performance on the system level performance of CSACs is reviewed and explained in detail. This concise introduction lays the foundation for the next section, which starts with a comprehensive review of the state-of-the-art for miniaturized LOs in published CSACs. Each of the metrics explained in the beginning of the thesis are then revisited, with examples and descriptions of how improvements can be made to existing microwave generation schemes used in CSACs.

Following this quantitative review, details of initial MMIC VCO designs and measurements are presented as intended for use in a new type of chip-scale atomic beam clock developed for the DARPA H6 SEABeaST program. The single-ended oscillators using on-chip resonators are then compared with VCOs in Chapter 5 designed with the same VCO core, but utilizing relatively higher-Q miniaturized off-chip glass-embedded resonators. The hybridly integrated oscillators are tested with a miniaturized atomic beam cell developed at NIST, as a proof of concept toward a future chip-scale beam clock.

A second MMIC VCO design iteration is fabricated using the same InGaP/GaAs HBT technology with improvements based on lessons learned during integration testing with the previous MMIC oscillators. A balanced Colpitts architecture and the measured results represents the culmination of insights resulting from this thesis. Finally, future work is discussed throughout this chapter, aiding in a path towards a new type of chip-scale atomic beam clock.

7.2 Future Work

7.2.1 Next-Generation CSACs

Next-generation microwave chip-scale atomic clocks employing different physics principles beyond currently commercialized CPT-based vapor-cell CSACs are being developed by a number of institutions to overcome fundamental limitations of the current physics architectures [2, 196]. Some of these alternative interrogation schemes include the miniaturized Cesium beams discussed throughout this thesis [36], double resonance in alkali atoms which resulted in a product mRO [29], and trapped ions in ytterbium or mercury [197]. Most prototypes are focused on reducing the size of the atomic cell, and use a large rack-mounted or off-the-shelf synthesizer which does not meet SWAP-C for a small clock. Here, a brief review of some of these new frequency standards are presented to understand the landscape of miniaturized clocks, in reference to the chip-scale atomic beam clock discussed in this thesis.

The clock architecture in this thesis mainly pertains to a new type of CPT-based atomic interrogation scheme, based on a $25 \times 19 \times 5\,\mathrm{mm}^3$ chip-scale Rb/Cs beam clock [36, 38, 198]. These are still actively being researched, with a projected stability limit of $\approx 9 \times 10^{-12}/\sqrt{\tau}$, limited by quantum projection noise. Because this clock targets the standard 4.596 GHz hyperfine transition frequency of ^{133}Cs and has similar RF requirements to vapor-cell CSACs, much of the LOs reviewed in this thesis prove the feasibility of creating a small microwave LO for this new type of clock.

A promising alternative to CPT-based small clocks are molecular clocks based on rotational transitions using microwave cavities. For example, the $^{16}O^{12}C^{32}S$ molecular clock which targets a

231-GHz transition is described in [88, 199]. In this approach, a metal waveguide cavity (WR-4.3) is filled with $^{16}O^{12}C^{32}S$ molecules and probed using a millimeter-wave 65 nm CMOS PLL with a chip-to-waveguide transition. This clock architecture does not require any lasers or accompanying optics, uses low-power heaters and less magnetic shielding, reducing the overall power consumption. The high millimeter-wave frequency also reduces the size of the clock compared to lower frequency transitions. The performance of this new type of clock is comparable to current commercial CSACs [87]. An analysis of the potential stabilities for chip scale molecular clocks is shown in a recent publication [200], also analyzing different options for molecular gasses which have various transition frequencies in the G-band frequency range.

In terms of miniature trapped-ion standards, mercury Hg^+ clocks targeting 40 GHz microwave transitions [201–203], e.g. the M2TIC prototypes, have reached the 10^{-14} stability level in 1 day with a SWaP of 1.1 L, 1.2 kg, and under 6 W of power, comparable to rack-mounted Cs beam standards. Future integration is planned with a 1 mm^2 40.5 GHz 65 nm-CMOS synthesizer operating from a 40-mW dc power supply [204]. Yb^+ clocks using microwave transitions at 12 GHz have also been demonstrated after preliminary miniaturization efforts [197, 205–207], with a cell sizes around 60x60x110 mm^3. The microwave signals for these clocks are at present generated using two large synthesizers and a large antenna. A different trapped-ion clock with a smaller size (3 cm^3) package is still a bench-top prototype, but shows promising stability results [208, 209]. Yet, to reach these low instabilities (10^{-14}) in a chip-scale package would require a high performance 40 GHz or 12 GHz LO to not limit the stability, which at present could dominate the size or power consumption.

Looking past microwave atomic clocks, large-scale optical clocks have continued to set new records for frequency stability, with a planned switch for the definition of a second from microwave to optical standards seeming imminent [210]. Since the 2000s, large optical clocks have achieved state-of-the-art fractional frequency uncertainties close to 10^{-18} [211], orders of magnitude better than microwave clocks due to the higher frequency atomic transitions. While the lowest uncertainties have been achieved with very physically large and stable setups, there has been great initial progress in miniaturized and portable optical clocks, such as the ones based on the two-photon optical

transition in Rb. These clocks incorporate micro-resonator frequency combs for optical frequency division in a small package [39, 212], but are still in early phases. Nonetheless, compact optical frequency standards would have a fundamental advantage in terms of frequency stability, but still have a number of challenges to overcome for commercial miniaturization. Work is continuing on such clocks, with great progress [213].

7.2.2 Chip-scale Beam Clock Integration Testing

As a next step towards a fully integrated chip-scale atomic beam clock, further multi-component testing is planned for all systems that are a part of the H6 SEABeaST project. First, tests of the balanced VCO MMICs presented in Chapter 6 in conjunction with a CMOS control ASIC will be performed with both chips mounted on a larger printed circuit board (PCB). This PCB is mainly used to support the many I/O pins on the CMOS ASIC, while providing transmission line trace routing for the interconnect between the VCO MMIC and the ASIC to test the PLL. A layout photo of the PCB developed for this project at Virginia Polytechnic Institute and State University (Prof. J. Walling group) is shown in Fig. 7.1, with an example bonding diagrams in orange for the VCO MMIC.

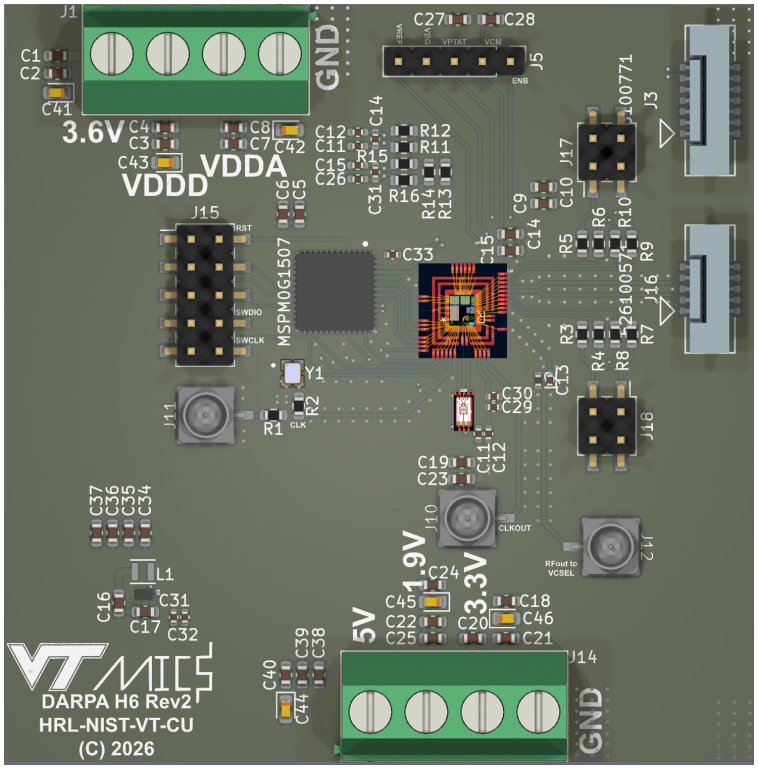


Figure 7.1: Integration PCB connecting the balanced MMIC VCO discussed in Chapter 7 with the CMOS ASIC and external physics package. This PCB is developed by collaborators Prof. J. Walling and J. Lee at Virginia Polytechnic Institute and State University, who also designed the CMOS ASIC. In orange and black are the proposed locations and bonding diagrams for the VCO MMIC and CMOS ASIC.

The specific goals of these first tests are to demonstrate a stable PLL which can finely tune around 4.596 GHz and explore the functionality of the digital control circuits. The digital control circuits are critical for clock functionality, including magnetic field, laser, frequency, and RF amplitude control. Once a working stable PLL is demonstrated at the PCB level using these two chips, next steps will be taken to drive the atomic transition of Cs within a traditional vapor cell using a VCSEL as shown in Fig. 7.2.

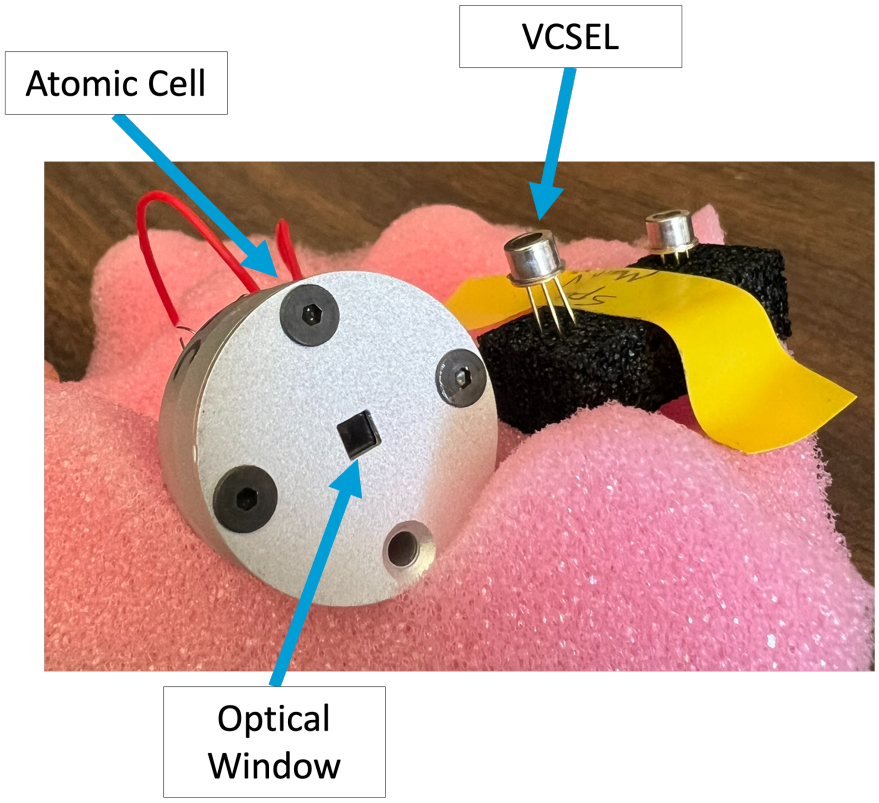


Figure 7.2: Atomic vapor cell containing Cs with transparent optical window for atomic interrogation using a VCSEL. All components here are developed and provided by HRL Laboratories. The Cs vapor cell will be mounted for PCB-level integration with the circuits shown in Fig. 7.1.

These components will be held within small optical mounts attached to a separate and smaller PCB, allowing for fine tuning of the alignment between optical components. This will provide a testbed for measurements of the control loop stability for the parameters described earlier. Feedback using the vapor cell signal will be realized in a similar manner to the chip-scale beam clock testing shown in Chapter 6, by interrogating the magnetic field insensitive hyperfine transition using Ramsey CPT spectroscopy. This integration testing emulates the operation of the RF and controls electronics with the eventual Cs beam cells by using a more simple substitute for the physics package akin to that of traditional vapro cell CSACs. After successful testing with the Cs vapor cells pictured here, further experiments with the miniaturized cesium beam cells is the logical

next step towards demonstrating a fully miniaturized beam clock.

Wafer-level fabrication and packaging of the fully integrated device including the atomic beam cells is also being explored at HRL Laboratories [172]. With the addition of the wafer-level fabrication of the atomic beam cells, all system components including the VCO MMICs discussed in this thesis are focused on wafer level fabrication before final CSAC assembly. Further details of packaging, integrated clock testing, and operation over various environmental conditions are outside the scope of this thesis and topics of future research.

7.2.3 G-band GaN MMIC Oscillator for a Chip-scale Molecular Clock (CSMC)

As described in Section 7.2.1, there are a number of promising alternatives to microwave vapor-cell CSACs based on alkali atoms, including chip-scale molecular clocks (CSMCs), which rely on a $f_0 \approx 230\,\text{GHz}$ high frequency RF oscillator to drive rotational transitions in molecules such as $^{16}\text{O}^{12}\text{C}^{32}\text{S}$. Generating energy on-chip at these frequencies often carries significant penalty in performance, due to reduced transistor gain and power handling at higher frequencies [214]. In the literature so far, high-frequency chip-to-waveguide coupling structures have been used to drive the molecules trapped in a WR 4.3 waveguide cavity, which can carry a hefty (6 to 11 dB) insertion loss penalty in RF loss at higher frequencies [215]. The frequency generation schemes for these clocks have so far involved frequency multiplication techniques, multiplying CMOS oscillators with fundamental outputs at lower frequencies (58 GHz) [216]. The frequency multiplication achieved in these works has so far been done using traditional nonlinear transistor amplifiers with harmonic terminations, which can result in reasonable multiplication efficiencies, but potentially worsens the phase noise of the fundamental oscillator output beyond the standard $20log(n)$ multiplication penalty [126]. In contrast, nonlinear transmission line multipliers such as the one described in this chapter have been shown to have near ideal additive phase noise, and have been used in phase noise sensitive applications such as atomic clocks [217]. Additionally, oscillators and amplifiers designed in CMOS technologies can have difficulty producing higher power levels due to the relatively low breakdown voltage of silicon transistors. This becomes especially true as output frequencies increase

above 200 GHz, potentially becoming a limiting factor in future chip-scale molecular clocks and other sub-THz applications.

This provides the research motivation for the future research presented in this section. A 76 GHz fundamental-frequency oscillator is co-designed with a nonlinear transmission line frequency tripler in HRL's T3L high-frequency GaN-on-SiC process. GaN transistors have the advantage of much larger breakdown voltages compared to CMOS, SiGe, and InP technologies often used in other high-frequency MMICs. This characteristic allows for higher power densities and therefore higher output powers for a fixed system size, providing a potential path for producing more output power above 200 GHz in a small size compared with CMOS techniques. Transistor-based GaN oscillators have been demonstrated at W-band with fundamental output frequencies > 70 GHz, at output power levels in the +20 dBm range [218]. Most of demonstrated GaN oscillators focus on maximum output power and dc-to-RF conversion efficiency, with the acknowledgment of poor output phase noise due to the technologies' relatively mediocre flicker noise [219]. Therefore, the oscillator described in this chapter is designed with a trade-off between these three metrics to balance the semi-conductor technology advantages and disadvantages.

The 76 GHz fundamental oscillator is designed using a balanced Colpitts topology similar to that in Chapter 6. The main difference from the circuit architecture presented in Chapter 6 and the W-band oscillator in this chapter is the removal of the varactor control circuits. These are omitted due to lack of dedicated varactor models in the foundry provided PDK, added layout complexity, and potential phase noise performance degradations due to the varactor tuning. Narrowband frequency control can be achieved through control of the gate and drain voltages, as a proof of concept for tunability. The design goals for the simulated performance are to achieve an output power of > 10 dBm while maintaining as low of a phase noise and dc power consumption as possible. These are chosen based on the potential application to a miniaturized molecular clock, where low dc power consumption and low phase noise are desirable, similar to the microwave CSACs discussed in the rest of this thesis. A second version of the oscillator including a co-designed Marchand balun is also included in order to provide an option for a single-ended RF output. Both layouts of the

W-band oscillator without the frequency multiplication chain are shown in Figs. 7.3 and 7.4.

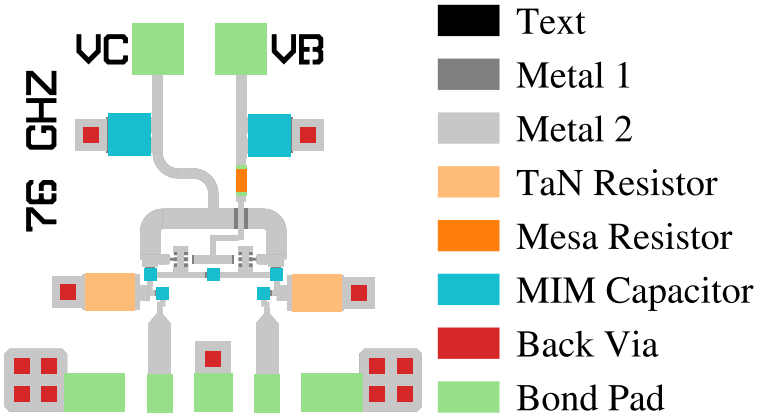


Figure 7.3: Layout of the 76 GHz balanced Colpitts MMIC oscillator designed in HRL's T3L high frequency GaN process. The differential GSGSG outputs are located on the bottom, while dc bias is provided at the top at the labeled locations. The total die size is $1 \times 1\,\mathrm{mm}^2$.

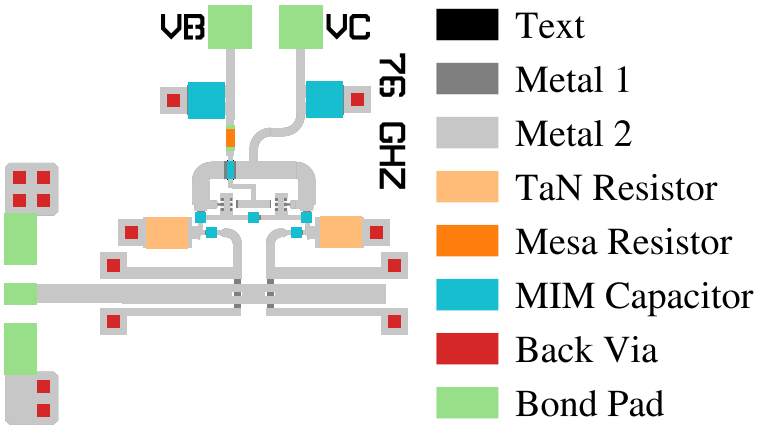


Figure 7.4: Layout of the 76 GHz balanced Colpitts MMIC oscillator with integrated Marchand balun designed in HRL's T3L high frequency GaN process. The single-ended GSG outputs are located on the bottom-left, while dc bias is provided at the top at the labeled locations. The total die size is $1 \times 1\,\mathrm{mm}^2$. Acknowledgments to Stefan Stroessner and Tim Sonnenberg for the co-designed Marchand balun.

Two $2 \times 25\,\mu$m transistors are used for the VCO core, selected based on approximate power required to drive the molecular transition given a lossy frequency tripler and chip-to-waveguide transition, as well as limited transistor size availability for the foundry validated device sizes. The oscillator is designed and EM simulated in Cadence AWR using the AXIEM solver. The dc input voltages are planned to be provided by bondwire at the top bond pads labled V_c and V_B, while the output $50\,\Omega$ differential GSGSG outputs are at the bottom. For the oscillator with the integrated Marchand balun, the output GSG is on the bottom left. The total size for both W-band oscillator layouts is $1 \times 1\,\text{mm}^2$.

Fig. 7.5 shows the simulated phase noise performance of the 76 GHz oscillator with the integrated Marchand Balun when biased at a drain bias of $V_d = 12\,\text{V}$, $I_d = 34\,\text{mA}$ and gate bias of $V_g = -1\,\text{V}$. The flicker corner is not provided in the foundry transistor models. In simulation, this phase noise corresponds to -92 dBc/Hz at a 1 MHz offset from a 76 GHz output frequency. Fig. 7.6 shows the oscillator's simulated output frequency (red) and output power (orange) versus the gate voltage (V_g), providing evidence for nearly 250 MHz of narrowband tunability around 76 GHz using dc bias voltage. The simulated output power ranges from 13.5 to 14 dBm across a -2 to 0 V gate voltage tuning range. The total simulated dc power consumption of the oscillator is 408 mW at these output powers, with the potential to decrease the total power consumption if less power after being tripled is required.

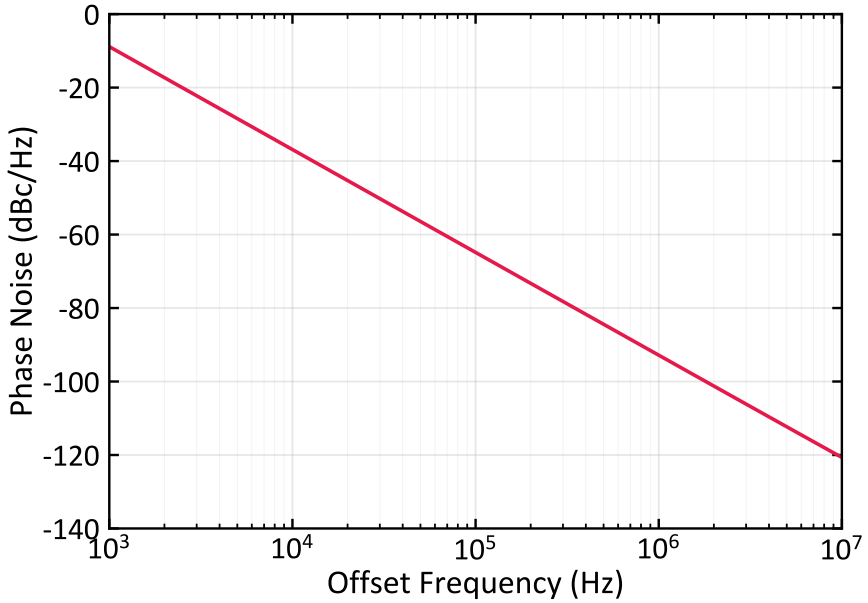


Figure 7.5: Simulated phase noise versus offset frequency for the 76 GHz oscillator with integrated Marchand Balun when biased at $V_d = 12\,\mathrm{V}$, $I_d = 34\,\mathrm{mA}$ and $V_g = -1\,\mathrm{V}$. The flicker corner is not included in the foundry provided transistor models.

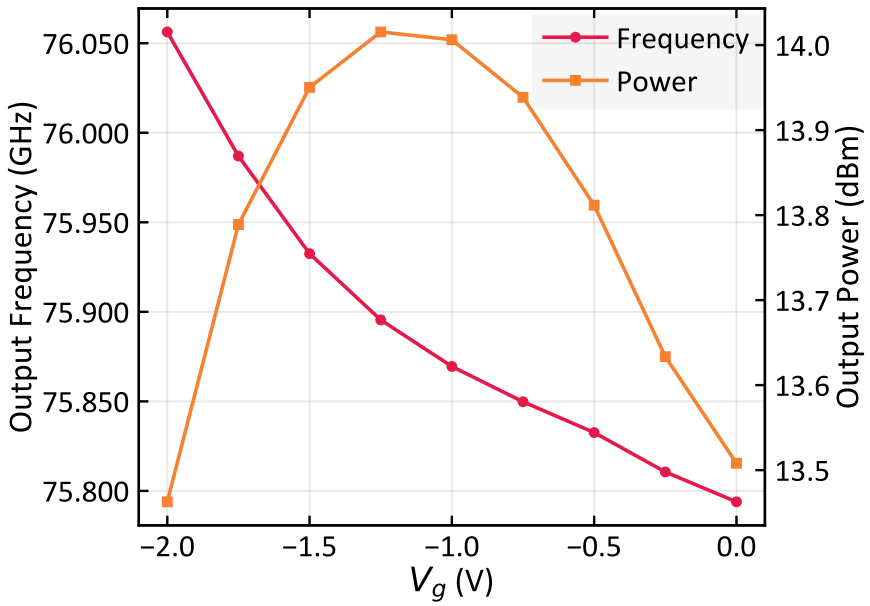


Figure 7.6: Simulated output power and output frequency versus gate voltage (V_g) for the 76 GHz oscillator with integrated Marchand Balun, biased at $V_d = 12$ V.

On-chip frequency multiplication is implemented using a nonlinear transmission line frequency tripler designed by a fellow student, Joel Johnson. Nonlinear transmission lines have been shown to have near-ideal additive phase noise with decent conversion efficiencies when compared to various other frequency multiplication techniques, making them an interesting candidate for the phase noise sensitive application briefly presented here [220]. The multiplier design briefly discussed in this chapter is based on a previous GaN design in [221], providing a lower-frequency proof of concept. The multiplier input is designed for a 50 Ω single-ended input provided by the 76 GHz oscillator with integrated planar Marchand balun. An example of the W-band VCO integrated on-chip with the nonlinear transmission line tripler is shown in Fig. 7.7. Further details of the co-designed frequency multiplication chain are outside the scope of this thesis, and will be published in future collaboration works. An example of the complete die with multiple iterations is shown in Fig. 7.8.

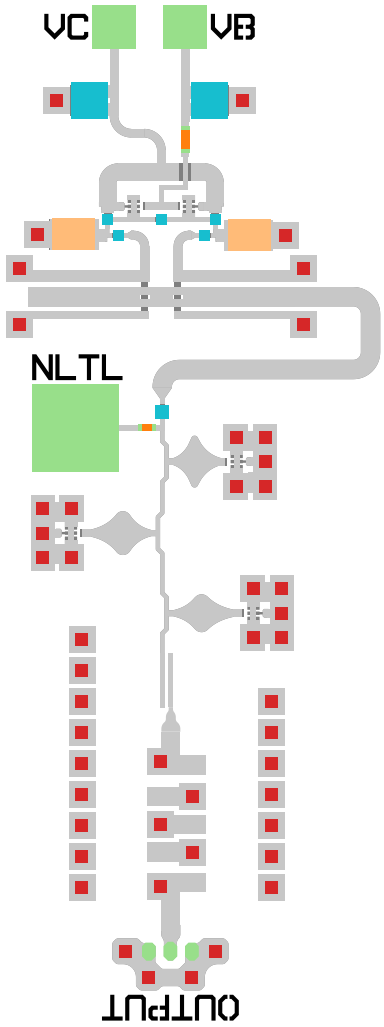


Figure 7.7: Layout of the 76 GHz W-band oscillator with Marchand Balun (top) and the nonlinear transmission line frequency multiplier (bottom) used to multiply up to ≈ 230 GHz. The nonlinear transmission line tripler is designed by Joel Johnson.

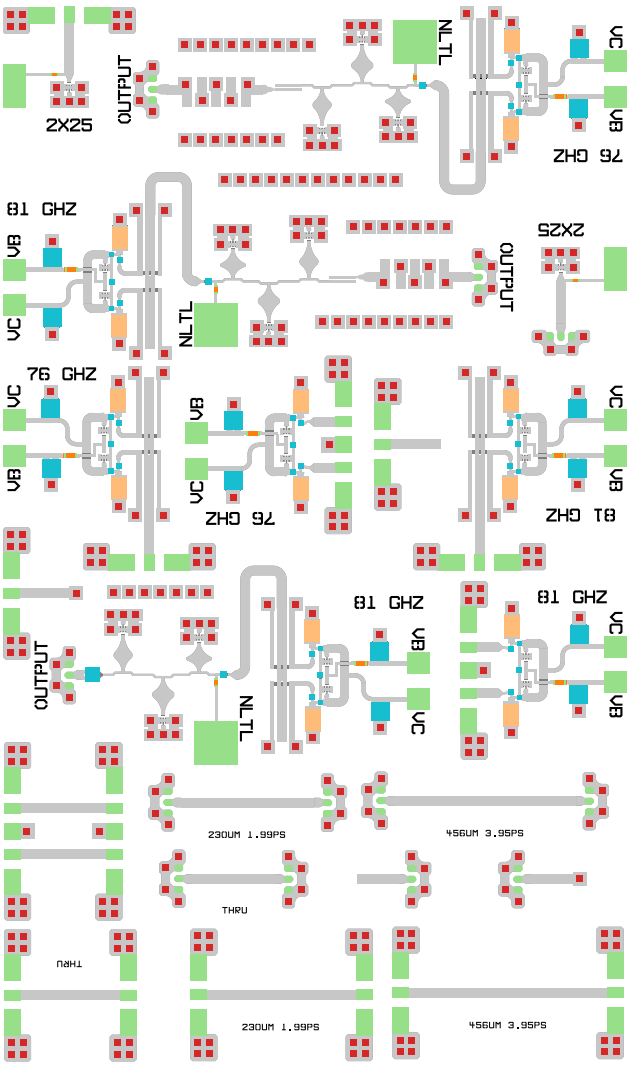


Figure 7.8: Layout of the full HRL T3L reticle, showing multiple design iterations for the W-band oscillators, nonlinear transmission lines multipliers, and integrated G-band frequency sources. Additional TRL and test structures are included for measurements. Reticle assembled by Joel Johnson.

7.3 Summary of Contributions

Chapter 1 explains the concept of microwave chip-scale atomic clocks and their real-world applications. A description of how these miniaturized clocks fit into the landscape of clocks of various sizes, power consumption,s and timing performances are shown. The constituent parts of

microwave CSACs are described in detail, with examples from literature and commercial products. Finally, a generic explanation of microwave oscillators, phase noise, and feedback is provided. This chapter provides the bedrock for the state-of-the-art reviews, designs, and measurements shown throughout this thesis.

Chapter 2 provides a holistic overview of the metrics for microwave oscillators in chip-scale atomic clocks, diving into each of the relevant performance metrics for phase noise, stability, RF power, dc power consumption, and servo electronics. This chapter provides an original and concise summation of how these metrics affect any type of microwave atomic clock, which is useful for parameterizing oscillator designs for clock systems. The metric analysis is reported in [80].

Chapter 3 presents the first state-of-the-art review specific to microwave oscillators designed for chip-scale-atomic clocks. Many different designs from literature are compared and contrasted to identify trends in design choices, as well as identify research gaps that could result in higher performance RF generation methods in CSACs. The comparison analysis is reported in [80]. Furthering on this review, discussions are repeated for each of the metrics identified in Chapter 2 given the context of this state-of-the-art review, explaining how each metric could be improved in future oscillator designs.

Chapter 4 begins by describing the chip-scale atomic beam clock project that is the overarching system related to the oscillators in this Thesis. Following this introduction, the first oscillators in an InGaP/GaAs HBT MMIC process designed specifically for CSACs are shown. Circuit design, layout, and measurements are addressed for two types of oscillators, one of which leverages an on-chip novel co-designed non-uniform transmission line resonator. Comparisons of these two designs show a reasonable improvement in phase noise with little on-chip area increase, and are reported in [180].

Chapter 5 demonstrates a hybridly integrated InGaP/GaAs HBT MMIC oscillator with a miniaturized glass-embedded resonator for use in the previously described chip-scale atomic beam clock project. The resonators are designed in a photo-sensitive glass process, allowing for the fabrication of higher-Q structures compared to on-chip resonators at the cost of minor volume

increase. The oscillators are then measured, showing large phase noise improvements compared to other oscillators utilizing on-chip resonator structures. This represents the first time such structures have been directly combined with an integrated circuit oscillator. The VCOs are then used in a demonstration with a prototype chip-scale atomic beam cell, showing a working clock prototype with no degradation in stability performance. This illustrates the first integrated experiments with such a clock and is reported in [193].

Chapter 6 presents a balanced Colpitts oscillator in the same InGaP/GaAs HBT MMIC process presented in previous chapters, with improvements learned via component integration testing. A detailed fabrication tolerance solution is presented, with multiple design iterations and potential for post-fabrication frequency tuning. The oscillators presented in this chapter are more mature than the previous, showing improvements in phase noise, tuning gain, and size. These chips represent performance comparable to the state-of-the-art for InGaP/GaAs MMICs in literature, with evidence that a path to integration with an off-chip CMOS ASIC and atomic beam cell are possible in a step towards a completely integrated chip-scale atomic beam device.

Chapter 7 wraps up the Thesis with an overview of alternate CSAC architectures that present potential advantages over current commercial microwave vapor cell CSACs based on Rb and Cs. One of such frequency standards are chip-scale molecular clocks which utilize transitions in molecules using frequencies in G-band. As a potential alternative to the CMOS frequency generation schemes in literature, a co-designed $\approx 230\,\text{GHz}$ GaN frequency source consisting of a $76\,\text{GHz}$ balanced Colpitts oscillator and nonlinear transmission line frequency multiplier are outlined. Pending future measurements, this would represent one of the highest frequency on-chip GaN sources in literature, with potential use-cases in G-band systems such as sub-THz molecular spectroscopy in chip-scale molecular clocks. Additionally, the paths towards further integration testing of the chip-scale atomic beam clock are described in detail as direct next steps to the research presented in this Thesis.

Bibliography

[1] David B Newell and Eite Tiesinga. The international system of units (SI): 2019 edition. Technical Report NIST SP 330-2019, National Institute of Standards and Technology, Gaithersburg, MD, August 2019.

[2] Bonnie L. Schmittberger Marlow and David R. Scherer. A Review of Commercial and Emerging Atomic Frequency Standards. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 68(6):2007–2022, 2021.

[3] John Kitching. Chip-scale Atomic Devices. Applied Physics Reviews, 5(3), 2018.

[4] H. Lyons. The Atomic Clock,", Vol. 22, Pp. 133-135, 174, December 1949. Instruments, 22:133–135, 1949.

[5] L. Essen and V. I. Parry. An Atomic Standard of Frequency and Time Interval. Nature, 176:280–284, 1955.

[6] Jacques Vanier and Claude Audoin. The Quantum Physics of Atomic Frequency Standards. CRC Press, 1989.

[7] J. Grotti, I. Nosske, S.B. Koller, S. Herbers, H. Denker, L. Timmen, G. Vishnyakova, G. Grosche, T. Waterholter, A. Kuhl, S. Koke, E. Benkler, M. Giunta, L. Maisenbacher, A. Matveev, S. Dörscher, R. Schwarz, A. Al-Masoudi, T.W. Hänsch, Th. Udem, R. Holzwarth, and C. Lisdat. Long-distance chronometric leveling with a portable optical clock. Physical Review Applied, 21(6):L061001, June 2024.

[8] Bernardo Jaduszliwer and James Camparo. Past, Present and Future of Atomic Clocks for GNSS. GPS Solutions, 25:1–13, 2021.

[9] J.R. Vig. Military Applications of High Accuracy Frequency Standards and Clocks. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 40(5):522–527, 1993.

[10] John D. Prestage and Gregory L. Weaver. Atomic Clocks and Oscillators for Deep-space Navigation and Radio Science. Proceedings of the IEEE, 95(11):2235–2247, 2007.

[11] Todd A Ely, Eric A Burt, John D Prestage, Jill M Seubert, and Robert L Tjoelker. Using the Deep Space Atomic Clock for Navigation and Science. IEEE transactions on ultrasonics, ferroelectrics, and frequency control, 65(6):950–961, 2018.

[12] C. Audoin, V. Candelier, and N. Diamarcq. A Limit to the Frequency Stability of Passive Frequency Standards Due to an Intermodulation Effect. IEEE Transactions on Instrumentation and Measurement, 40(2):121–125, 1991.

[13] S. Knappe, V. Shah, P. D. D. Schwindt, L. Hollberg, J. Kitching, L. A. Liew, and J. Moreland. A Microfabricated Atomic Clock. Applied Physics Letters, 85(9):1460–1462, 2004.

[14] R. Lutwak, A. Rashad, M. Varghese, G. Tepolt, J. Leblanc, M. Mescher, D. K. Serkland, K. M. Geib, G. M. Peake, and S. Romisch. The Chip-scale Atomic Clock - Prototype Evaluation. In Precise Time and Time Interval (PTTI) Meeting, pages 269–290, 2007.

[15] D. W. Youngner, L. M. Lust, D. R. Carlson, S. T. Lu, L. J. Forner, H. M. Chanhvongsak, and T. D. Stark. A Manufacturable Chip-scale Atomic Clock. In TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference, pages 39–44, 2007.

[16] A. T. Gardner and J. A. Collins. Advancements in High-performance Timing for Long Term Underwater Experiments A Comparison of Chip Scale Atomic Clocks to Traditional Microprocessor-compensated Crystal Oscillators. In MTS/IEEE Oceans Conference, pages 1–8, 2012. Gardner, Alan T. Collins, John A.

[17] Todd Ely, Zaid Towfic, and Dana Sorensen. Formulation and Characterization of One-way Radiometric Tracking with the Iris Radio Using a Chip-scale Atomic Clock. NAVIGATION: Journal of the Institute of Navigation, 71(1):navi.633, 2024.

[18] G. Alzetta, A. Gozzini, L. Moi, and G. Orriols. Experimental-method for Observation of Rf Transitions and Laser Beat Resonances in Oriented Na Vapor. Il Nuovo Cimento, 36(1):5–20, 1976.

[19] E. Arimondo and G. Orriols. Non-absorbing Atomic Coherences by Coherent 2-photon Transitions in a 3-level Optical-pumping. Lettere Al Nuovo Cimento, 17(10):333–338, 1976.

[20] Darwin K Serkland, Gregory M Peake, Kent M Geib, Robert Lutwak, R Michael Garvey, Mathew Varghese, and Mark Mescher. VCSELs for Atomic Clocks. In Vertical-Cavity Surface-Emitting Lasers X, volume 6132, pages 66–76. SPIE, 2006.

[21] D. K. Serkland, K. M. Geib, G. M. Peake, R. Lutwak, A. Rashed, M. Varghese, G. Tepolt, and M. Prouty. VCSELs for Atomic Sensors. In Vertical-Cavity Surface-Emitting Lasers XI, volume 6484, pages 48–57. SPIE, February 2007.

[22] Ennio Arimondo. V Coherent Population Trapping in Laser Spectroscopy. In Progress in optics, volume 35, pages 257–354. Elsevier, 1996.

[23] Florian Gruet, Ahmed Al-Samaneh, Eric Kroemer, Laura Bimboes, Danijela Miletic, Christoph Affolderbach, Dietmar Wahl, Rodolphe Boudot, Gaetano Mileti, and Rainer Michalzik. Metrological Characterization of Custom-designed 894.6 Nm VCSELs for Miniature Atomic Clocks. Optics express, 21(5):5781–5792, 2013.

[24] Eric Kroemer, Jaroslaw Rutkowski, Vincent Maurice, Rémy Vicarini, Moustafa Abdel Hafiz, Christophe Gorecki, and Rodolphe Boudot. Characterization of Commercially Available Vertical-cavity Surface-emitting Lasers Tuned on Cs D_\textrm1 Line at 894.6 Nm for Miniature Atomic Clocks. Applied Optics, 55(31):8839–8847, November 2016.

[25] Svenja Knappe. Emerging Topics: MEMS Atomic Clocks. Number 3. Elsevier (Netherlands), NL, 2007-11-01 2007.

[26] Microchip. SA65 Chip Scale Atomic Clock, CSAC-SA65 Datasheet. `https://www.microchip.com/en-us/product/csac-sa65#document-table`. Accessed: 2024-08-28.

[27] Teledyne. Teledyne Chip Scale Atomic Clock (TCSAC) Datasheet. `https://www.teledyne-e2v.com/en-us/Solutions_/Documents/2018+11+05_e2v_TSAC+SpecSheet_v3.pdf`. Accessed: 2024-09-16.

[28] Taitien. Https://www.taitien.com/wp-content/uploads/2024/02/taitien-low-power-atomic-oscillator-dta-450.pdf.

[29] SAFRAN. MRO-50, Miniature, Ultra-portable High Precision & Performance Atomic Frequency Source. Datasheet, 2020.

[30] Haosheng Zhang, Hans Herdian, Aravind Tharayil Narayanan, Atsushi Shirane, Mitsuru Suzuki, Kazuhiro Harasaka, Kazuhiko Adachi, Shigeyoshi Goka, Shinya Yanagimachi, and Kenichi Okada. ULPAC: A Miniaturized Ultralow-power Atomic Clock. IEEE Journal of Solid-State Circuits, 54(11):3135–3148, 2019.

[31] Peter Cash, Will Krzewick, Paul Machado, K. Richard Overstreet, Mike Silveira, Matt Stanczyk, Dwayne Taylor, and Xianli Zhang. Microsemi Chip Scale Atomic Clock (CSAC) Technical Status, Applications, and Future Plans. In 2018 European Frequency and Time Forum (EFTF), pages 65–71, 2018.

[32] J. Gouloumet, B. Leuenberger, C. Schori, S. Grop, and P. Rochat. Progress Towards a Compact and Low-power Miniaturized Rubidium Oscillator (mro™). In 2020 IEEE/MTT-S International Microwave Symposium (IMS), pages 876–879, 2020.

[33] IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology–Random Instabilities. IEEE Std 1139-2022 (Revision of IEEE Std 1139-2008), pages 1–60, 2022.

[34] D.W. Allan. Statistics of Atomic Frequency Standards. Proceedings of the IEEE, 54(2):221–230, 1966.

[35] Enrico Rubiola and François Vernotte. The Companion of Enrico's Chart for Phase Noise and Two-Sample Variances. IEEE Transactions on Microwave Theory and Techniques, 71(7):2996–3025, July 2023.

[36] Gabriela D Martinez, Chao Li, Alexander Staron, John Kitching, Chandra Raman, and William R McGehee. A Chip-scale Atomic Beam Clock. Nature Communications, 14(1):3501, 2023.

[37] Cash Peter, Boschen Dan, Gandham Ramesh, and Mailoux David. Low Noise Chip Scale Atomic Clock (LNCSAC). In 2014 IEEE International Frequency Control Symposium (FCS), pages 1–4, 2014.

[38] DARPA H6 Program, 2024.

[39] Zachary L. Newman, Vincent Maurice, Tara Drake, Jordan R. Stone, Travis C. Briles, Daryl T. Spencer, Connor Fredrick, Qing Li, Daron Westly, B. R. Ilic, Boqiang Shen, Myoung-Gyun Suh, Ki Youl Yang, Cort Johnson, David M. S. Johnson, Leo Hollberg, Kerry J. Vahala, Kartik Srinivasan, Scott A. Diddams, John Kitching, Scott B. Papp, and Matthew T. Hummon. Architecture for the Photonic Integration of an Optical Atomic Clock. Optica, 6(5):680–685, May 2019.

[40] Cheng Wang, Xiang Yi, James Mawdsley, Mina Kim, Zihan Wang, and Ruonan Han. An On-chip Fully Electronic Molecular Clock Based on Sub-terahertz Rotational Spectroscopy. Nature Electronics, 1(7):421–427, 2018.

[41] Cheng Wang, Xiang Yi, Mina Kim, Yaqing Zhang, and Ruonan Han. A CMOS Molecular Clock Probing 231.061-ghz Rotational Line of OCS with Sub-ppb Long-term Stability and 66-MW DC Power. In 2018 IEEE Symposium on VLSI Circuits, pages 113–114, 2018.

[42] Ulrich L Rohde, Ajay K Poddar, and Georg Böck. The Design of Modern Microwave Oscillators for Wireless Applications: Theory and Optimization. John Wiley & Sons, 2005.

[43] H. Nyquist. Regeneration theory. The Bell System Technical Journal, 11(1):126–147, January 1932.

[44] John G Proakis and Masoud Salehi. COMMUNICATION SYSTEMS ENGINEERING. Prentice Hall, Upper Saddle River, NJ, 2 edition, 2002.

[45] Merrill I. Skolnik. Introduction to Radar Systems, 3rd Edition. McGraw-Hill, New York NY USA, 2001.

[46] R. E. Beehler, R. C. Mockler, and J. M. Richardson. Cesium Beam Atomic Time and Frequency Standards. Metrologia, 1(3):114, July 1965.

[47] Ali Hajimiri and Thomas H Lee. The Design of Low Noise Oscillators. Springer Science & Business Media, 2007.

[48] David B. Leeson. Oscillator Phase Noise: A 50-Year Review. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 63(8):1208–1225, August 2016. Conference Name: IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control.

[49] James A Barnes. The Measurement of Linear Frequency Drift in Oscillators. In Proceedings of the 15th Annual Precise Time and Time Interval Systems and Applications Meeting, 1983.

[50] D.B. Leeson. A Simple Model of Feedback Oscillator Noise Spectrum. Proceedings of the IEEE, 54(2):329–330, 1966.

[51] G. Santarelli, C. Audoin, A. Makdissi, P. Laurent, G.J. Dick, and A. Clairon. Frequency Stability Degradation of an Oscillator Slaved to a Periodically Interrogated Atomic Resonator. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 45(4):887–894, 1998.

[52] C. Audoin, V. Candelier, and N. Diamarcq. A Limit to the Frequency Stability of Passive Frequency Standards. In Conference on Precision Electromagnetic Measurements, pages 93–, 1990.

[53] G Kramer. Noise in Passive Frequency Standards. In 1974 Conf. Precision Electromagnetic Meas, pages 157–159, 1974.

[54] C.A. Greenhall and G.J. Dick. Local Oscillator Limited Frequency Stability for Passive Atomic Frequency Standards Using Square Wave Frequency Modulation. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 47(6):1593–1600, 2000.

[55] J.Q. Deng, G. Mileti, D.A. Jennings, R.E. Drullinger, and F.L. Walls. Improving the Short-term Stability of Laser Pumped Rb Clocks by Reducing the Effects of the Interrogation Oscillator. In Proceedings of International Frequency Control Symposium, pages 438–445, 1997.

[56] Jean-Marie Danet, Michel Lours, Stéphane Guérandel, and Emeric De Clercq. Dick Effect in a Pulsed Atomic Clock Using Coherent Population Trapping. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 61(4):567–574, 2014.

[57] Enrico Rubiola. Phase Noise and Frequency Stability in Oscillators. Cambridge University Press, 2008.

[58] Dan Kuylenstierna, Szhau Lai, Mingquan Bao, and Herbert Zirath. Design of Low Phase-noise Oscillators and Wideband Vcos in InGaP HBT Technology. IEEE Transactions on Microwave Theory and Techniques, 60(11):3420–3430, 2012.

[59] G. Niu. Noise in SiGe HBT RF Technology: Physics, Modeling, and Circuit Implications. Proceedings of the IEEE, 93(9):1583–1597, 2005.

[60] Clemente Toro Jr. Improved 1/f Noise Measurements for Microwave Transistors. Thesis, Dept. Elect. Eng., Univ. South Florida, Tampa, FL., 2004.

[61] Yazhou Zhao, Steve Tanner, Arnaud Casagrande, Christoph Affolderbach, Luc Schneller, Gaetano Mileti, and Pierre-André Farine. CPT Cesium-cell Atomic Clock Operation with a 12-mw Frequency Synthesizer ASIC. IEEE Transactions on Instrumentation and Measurement, 64(1):263–270, 2015.

[62] M. Zhu and L. S. Cutler. Theoretical and Experimental Study of Light Shift in a Cpt-based Rb Vapor Cell Frequency Standard. In Proceedings of the 32th Annual Precise Time and Time Interval Systems and Applications Meeting, pages 311–324, November 2000.

[63] F. Levi, A. Godone, and J. Vanier. The Light Shift Effect in the Coherent Population Trapping Cesium Maser. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 47(2):466–470, March 2000.

[64] Jacques Haesler, Laurent Balet, Jacques-André Porchet, Thomas Overstolz, Jörg Pierer, Rony Jose James, Sylvain Grossmann, David Ruffieux, and Steve Lecomte. The Integrated Swiss Miniature Atomic Clock. In 2013 Joint European Frequency and Time Forum and International Frequency Control Symposium (EFTF/IFC), pages 579–581, 2013.

[65] Milos Jankovic, Alan Brannon, Jason Breitbarth, and Zoya Popovic. Design Method for Low-power, Low Phase Noise Voltage-controlled Oscillators. In 2007 European Microwave Integrated Circuit Conference, pages 199–202, 2007.

[66] Yi-Pei Su, Wei-Yi Hu, Jia-Wei Lin, Yun-Chung Chen, Sakir Sezer, and Sao-Jie Chen. Low Power Gm-boosted Differential Colpitts VCO. In 2011 IEEE International SOC Conference, pages 247–250. IEEE, 2011.

[67] Gayathri Pillai and Sheng-Shian Li. Piezoelectric MEMS Resonators: A Review. IEEE Sensors Journal, 21(11):12589–12605, 2020.

[68] M Hara, Y Yano, M Kajita, H Nishino, Y Ibata, M Toda, S Hara, A Kasamatsu, H Ito, T Ono, et al. Micro Atomic Frequency Standards Employing an Integrated FBAR-VCO Oscillating on the 87 RB Clock Frequency Without a Phase Locked Loop. In 2018 IEEE Micro Electro Mechanical Systems (MEMS), pages 715–718. IEEE, 2018.

[69] F. Levi, A. Godone, J. Vanier, S. Micalizio, and G. Modugno. Line-shape of dark line and maser emission profile in cpt. The European Physical Journal D - Atomic, Molecular, Optical and Plasma Physics, 12(1):53–59, 09 2000.

[70] R.F. Wolffenbuttel. Digitally Programmable Accurate Current Sources for Logarithmic Control of the Amplification or Attenuation in a Gain Cell. IEEE Journal of Solid-State Circuits, 23(3):767–773, 1988.

[71] M. Ghovanloo and K. Najafi. A Compact Large Voltage-compliance High Output-impedance Programmable Current Source for Implantable Microstimulators. IEEE Transactions on Biomedical Engineering, 52(1):97–105, 2005.

[72] Moo-Young Kim, Jinwoo Kim, Tagjong Lee, and Chulwoo Kim. 10-bit 100-ms/s Pipelined ADC Using Input-swapped Opamp Sharing and Self-calibrated V/I Converter. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 19(8):1438–1447, 2011.

[73] Moo-Young Kim, Hokyu Lee, and Chulwoo Kim. PVT Variation Tolerant Current Source with On-chip Digital Self-calibration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 20(4):737–741, 2012.

[74] Yuji Osaki, Tetsuya Hirose, Nobutaka Kuroki, and Masahiro Numa. 1.2-V Supply, 100-nw, 1.09-V Bandgap and 0.7-V Supply, 52.5-nw, 0.55-V Subbandgap Reference Circuits for Nanowatt CMOS Lsis. IEEE Journal of Solid-State Circuits, 48(6):1530–1538, 2013.

[75] Charalambos M. Andreou, Savvas Koudounas, and Julius Georgiou. A Novel Wide-temperature-range, 3.9 Ppm/c° CMOS Bandgap Reference Circuit. IEEE Journal of Solid-State Circuits, 47(2):574–581, 2012.

[76] T.A.D. Riley, M.A. Copeland, and T.A. Kwasniewski. Delta-sigma Modulation in Fractional-n Frequency Synthesis. IEEE Journal of Solid-State Circuits, 28(5):553–559, 1993.

[77] M.H. Perrott, M.D. Trott, and C.G. Sodini. A Modeling Approach for /spl Sigma/-/spl Delta/ Fractional-n Frequency Synthesizers Allowing Straightforward Noise Analysis. IEEE Journal of Solid-State Circuits, 37(8):1028–1038, 2002.

[78] Microchip. Low-noise Chip-scale Atomic Clock, LN CSAC Datasheet. `https://ww1.microchip.com/downloads/en/DeviceDoc/00003046A.pdf`. Accessed: 2024-08-28.

[79] Peter Cash, Igor Kosvin, Hoklay Park, Matt Stanczyk, and Mike F. Wacker. Low Phase Noise Low Power Atomic Clocks. In 2022 Joint Conference of the European Frequency and Time Forum and IEEE International Frequency Control Symposium (EFTF/IFCS), pages 1–5, 2022.

[80] Alec Russell, William McGehee, John Kitching, Travis Autry, Jeffery Sean Walling, and Zoya Popović. RF Local Oscillators for Low-Power Chip-Scale Atomic Clocks. Proceedings of the IEEE, pages 1–20, 2026.

[81] Alan Brannon, M Jankovic, J Breitbarth, Z Popovic, V Gerginov, V Shah, S Knappe, L Hollberg, and J Kitching. A Local Oscillator for Chip-scale Atomic Clocks at NIST. In 2006 IEEE International Frequency Control Symposium and Exposition, pages 443–447. IEEE, 2006.

[82] Yazhou Zhao, Steve Tanner, Pierre-André Farine, and Arnaud Casagrande. A 4.6-ghz, 15-mw Frequency Synthesizer CMOS ASIC with Milli-hertz Frequency Resolution for Miniature Atomic Clocks. In 2011 Joint Conference of the IEEE International Frequency Control and the European Frequency and Time Forum (FCS) Proceedings, pages 1–4, 2011.

[83] David Ruffieux, Jacques Haesler, Laurent Balet, Thomas Overstolz, Jörg Pierer, Rony Jose James, and Steve Lecomte. Towards Portable Miniature Atomic Clocks. Frequency References, Power Management for SoC, and Smart Wireless Interfaces: Advances in Analog Circuit Design 2013, pages 83–99, 2014.

[84] J. S. Humble, R. A. Philpott, B. K. Gilbert, E. S. Daniel, and R. Lutwak. A Low-power 4.6 Ghz VCO for Chip-scale Atomic Clocks. In 2010 IEEE International Frequency Control Symposium, pages 112–115, 2010.

[85] R. Lutwak. Principles of Atomic Clocks. Tutorial Material of the IEEE Frequency Control Symposium, 2011.

[86] M Hara, Y Yano, M Kajita, H Nishino, Y Ibata, M Toda, S Hara, A Kasamatsu, H Ito, T Ono, et al. Microwave Oscillator Using Piezoelectric Thin-film Resonator Aiming for Ultraminiaturization of Atomic Clock. Review of Scientific Instruments, 89(10), 2018.

[87] Mina Kim, Cheng Wang, Lin Yi, Hae-Seung Lee, and Ruonan Han. A Sub- Thz CMOS Molecular Clock with 20 Ppt Stability at 10,000 S Based on Dual-loop Spectroscopic Detection and Digital Frequency Error Integration. In 2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 115–118, 2022.

[88] Cheng Wang, Xiang Yi, James Mawdsley, Mina Kim, Zhi Hu, Yaqing Zhang, Bradford Perkins, and Ruonan Han. Chip-scale Molecular Clock. IEEE Journal of Solid-State Circuits, 54(4):914–926, 2019.

[89] Stefania Romisch and Robert Lutwak. Low-power, 4.6-ghz, Stable Oscillator for CSAC. In 2006 IEEE International Frequency Control Symposium and Exposition, pages 448–451. IEEE, 2006.

[90] Alan Brannon, Jason Breitbarth, and Zoya Popovic. A Low-power, Low Phase Noise Local Oscillator for Chip-scale Atomic Clocks. In IEEE MTT-S International Microwave Symposium Digest, 2005., pages 1535–1538. IEEE, 2005.

[91] JF DeNatale, RL Borwick, C Tsai, PA Stupar, Y Lin, RA Newgard, RW Berquist, and M Zhu. Compact, Low-power Chip-scale Atomic Clock. In 2008 IEEE/ION Position, Location and Navigation Symposium, pages 67–70. IEEE, 2008.

[92] Rodolphe Boudot, Gilles Martin, Jean Friedt, and Enrico Rubiola. Characterization of High-overtone Bulk Acoustic Resonators: Applications to Ultra-low Noise Microwave Oscillators and Miniature Atomic Clocks. In Microwave Technology and Technique Workshop, 2017.

[93] Thomas Daugey, Jean-Michel Friedt, Gilles Martin, and Rodolphe Boudot. A High-overtone Bulk Acoustic Wave Resonator-oscillator-based 4.596 Ghz Frequency Source: Application to a Coherent Population Trapping Cs Vapor Cell Atomic Clock. Review of Scientific Instruments, 86(11), 2015.

[94] Jianye Zhao, Ping Guo, Haoyuan Lu, Ruiyuan Liu, Chaoquan Wang, Jingzhong Cui, and Hongling Meng. New Progress Towards Chip-scale Atomic Clock in Peking University. In 2018 IEEE International Frequency Control Symposium (IFCS), pages 1–3, 2018.

[95] Jianye Zhao, Ping Guo, Lin Dan, and Hongling Meng. Advances of Chip-scale Atomic Clock in Peking University in 2019. In 2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF), pages 1–4, 2020.

[96] Hongyu Yu, C-Y Lee, Wei Pang, Hao Zhang, Alan Brannon, John Kitching, and ES Sok Kim. Hbar-based 3.6 Ghz Oscillator with Low Power Consumption and Low Phase Noise. IEEE transactions on ultrasonics, ferroelectrics, and frequency control, 56(2):400–403, 2009.

[97] Tara M Fortier, Matthew S Kirchner, F Quinlan, JCBJ Taylor, JC Bergquist, T Rosenband, N Lemke, A Ludlow, Y Jiang, CW Oates, et al. Generation of Ultrastable Microwaves Via Optical Frequency Division. Nature photonics, 5(7):425–429, 2011.

[98] Tara M Fortier, Craig W Nelson, Archita Hati, Franklyn Quinlan, Jennifer Taylor, Haifeng Jiang, Chin-Wen Chou, Till Rosenband, Nathan Lemke, Andrew Ludlow, et al. Sub-femtosecond Absolute Timing Jitter with a 10 Ghz Hybrid Photonic-microwave Oscillator. Applied Physics Letters, 100(23), 2012.

[99] Bruno Francois, CE Calosso, JM Danet, and Rodolphe Boudot. A Low Phase Noise Microwave Frequency Synthesis for a High-performance Cesium Vapor Cell Atomic Clock. Review of Scientific Instruments, 85(9), 2014.

[100] B François, CE Calosso, M Abdel Hafiz, Salvatore Micalizio, and R Boudot. Simple-design Ultra-low Phase Noise Microwave Frequency Synthesizers for High-performing Cs and Rb Vapor-cell Atomic Clocks. Review of Scientific Instruments, 86(9), 2015.

[101] Fernando Ramirez-Martinez, Michel Lours, Peter Rosenbusch, Friedemann Reinhard, and Jakob Reichel. Low-phase-noise Frequency Synthesizer for the Trapped Atom Clock on a Chip. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 57(1):88–93, 2010.

[102] Wenbing Li, Yuanbo Du, Hui Li, and Zehuang Lu. Development of Low Phase Noise Microwave Frequency Synthesizers for Reducing Dick Effect of Cs Fountain Clocks. AIP Advances, 8(9), 2018.

[103] MACOM. MLPNC-7100 NLTL Comb Generator. Datasheet, 2025.

[104] Muhammad Adnan and Ehsan Afshari. Efficient Microwave and Millimeter-wave Frequency Multipliers Using Nonlinear Transmission Lines in CMOS Technology. IEEE Transactions on Microwave Theory and Techniques, 63(9):2889–2896, 2015.

[105] G.D. Rovera, G. Santarelli, and A. Clairon. Frequency Synthesis Chain for the Atomic Fountain Primary Frequency Standard. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 43(3):354–358, 1996.

[106] Jacques Millo, Michel Abgrall, Michel Lours, EML English, Haifeng Jiang, Jocelyne Guéna, André Clairon, Michael E Tobar, Sébastien Bize, Yann Le Coq, et al. Ultralow Noise Microwave Generation with Fiber-based Optical Frequency Comb and Application to Atomic Fountain Clock. Applied Physics Letters, 94(14), 2009.

[107] S Weyers, B Lipphardt, and H Schnatz. Reaching the Quantum Limit in a Fountain Clock Using a Microwave Oscillator Phase Locked to an Ultrastable Laser. Physical Review A—Atomic, Molecular, and Optical Physics, 79(3):031803, 2009.

[108] Burghard Lipphardt, Vladislav Gerginov, and Stefan Weyers. Optical Stabilization of a Microwave Oscillator for Fountain Clock Interrogation. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 64(4):761–766, 2017.

[109] John G Hartnett, Nitin R Nand, and Chuan Lu. Ultra-low-phase-noise Cryocooled Microwave Dielectric-sapphire-resonator Oscillators. Applied Physics Letters, 100(18), 2012.

[110] D Chambon, Sébastien Bize, Michel Lours, F Narbonneau, Harold Marion, André Clairon, Giorgio Santarelli, Andre Luiten, and Michael Tobar. Design and Realization of a Flywheel Oscillator for Advanced Time and Frequency Metrology. Review of Scientific Instruments, 76(9), 2005.

[111] Damien Chambon, Michel Lours, Frederic Chapelet, Sebastien Bize, Michael E. Tobar, Andre Clairon, and Giorgio Santarelli. Design and Metrological Features of Microwave Synthesizers for Atomic Fountain Frequency Standard. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 54(4):729–735, 2007.

[112] Microchip. Chip-scale Atomic Clock (CSAC) Perfromance During Rapid Temperature Change White Paper. White Paper, 2021.

[113] Tomas Bagala, Adam Fibich, Peter Kubinec, and Vladimir Stofanik. Improvement of Short-term Frequency Stability of the Chip Scale Atomic Clock. In 2016 IEEE International Frequency Control Symposium (IFCS), pages 1–4, 2016.

[114] Peter Kinget. Integrated Ghz Voltage Controlled Oscillators. In Analog Circuit Design: (X) DSL and other Communication Systems; RF MOST Models; Integrated Filters and Oscillators, pages 353–381. Springer, 1999.

[115] R. Aparicio and A. Hajimiri. A Noise-shifting Differential Colpitts VCO. IEEE Journal of Solid-State Circuits, 37(12):1728–1736, 2002.

[116] Seong-Sik Myoung and Jong-Gwan Yook. Low-phase-noise High-efficiency MMIC VCO Based on InGaP/GaAs HBT with the LC Filter. Microwave and Optical Technology Letters, 44(2):123–126, 2005.

[117] Shinwon Kang, Jun-Chau Chien, and Ali M Niknejad. A W-band Low-noise PLL with a Fundamental VCO in SiGe for Millimeter-wave Applications. IEEE Transactions on Microwave Theory and Techniques, 62(10):2390–2404, 2014.

[118] Milos Jankovic. Phase Noise in Microwave Oscillators and Amplifiers. PhD thesis, University of Colorado at Boulder, 2010.

[119] Wissam Hamad, Marwan Bou Sanayeh, Mustapha M. Hamad, and Werner H. E. Hofmann. Impedance Characteristics and Chip-parasitics Extraction of High-performance VCELSs. IEEE Journal of Quantum Electronics, 56(1):1–11, 2020.

[120] Herbert Zirath, Harald Jacobsson, M Bao, Mattias Ferndahl, and Rumen Kozhuharov. Mmic-oscillator Designs for Ultra Low Phase Noise. In IEEE Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC'05., pages 4–pp. IEEE, 2005.

[121] A.K. Kirtania, M.B. Das, S. Chandrasekhar, L.M. Lunardi, G.J. Qua, R.A. Hamm, and Li-Wu Yang. Measurement and Comparison of 1/f Noise and G-r Noise in Silicon Homojunction and III-V Heterojunction Bipolar Transistors. IEEE Transactions on Electron Devices, 43(5):784–792, 1996.

[122] D.L. Harame, D.C. Ahlgren, D.D. Coolbaugh, J.S. Dunn, G.G. Freeman, J.D. Gillis, R.A. Groves, G.N. Hendersen, R.A. Johnson, A.J. Joseph, S. Subbanna, A.M. Victor, K.M. Watson, C.S. Webster, and P.J. Zampardi. Current Status and Future Trends of SiGe BiCMOS Technology. IEEE Transactions on Electron Devices, 48(11):2575–2594, 2001.

[123] Jean-Guy Tartarin and King W Wong. X-band and K-band Low-phase-noise Vcos Using SiGe BiCMOS Technology. Semiconductor science and technology, 22(1):S195, 2006.

[124] Corrado Florian, Sara D'Angelo, Davide Resca, and Francesco Scappaviva. A Chip Set of Low Phase Noise MMIC Vcos at C, X and Ku Band in InGaP-GaAs HBT Technology for Satellite Telecommunications. In 2017 IEEE MTT-S International Microwave Symposium (IMS), pages 1148–1151, 2017.

[125] M Achouche, S Kraus, T Spitzbart, M Rudolph, D Rentner, F Brunner, E Richter, T Bergunde, P Heymann, P Wolter, et al. InGap/GaAs Power Hbts for L-band Applications. In Compound Semiconductors 1999, pages 297–300. CRC Press, 2000.

[126] Jason Breitbarth and Joe Koebel. Additive (residual) Phase Noise Measurement of Amplifiers, Frequency Dividers and Frequency Multipliers. Microwave Journal, 51(6):66, 2008.

[127] Pankratz, Erik and Sánchez-Sinencio, Edgar. Survey of integrated-circuit-oscillator phase-noise analysis. International Journal of Circuit Theory and Applications, 42(9):871–938, 2014.

[128] Jason Breitbarth. Design and Characterization of Low Phase Noise Microwave Circuits. PhD thesis, University of Colorado at Boulder, 2006.

[129] Simon Ramo, John R Whinnery, and Theodore Van Duzer. Fields and Waves in Communication Electronics. John Wiley & Sons, 1994.

[130] George D Vendelin, Anthony M Pavio, Ulrich L Rohde, and Matthias Rudolph. Microwave Circuit Design Using Linear and Nonlinear Techniques. John Wiley & Sons, 2021.

[131] Olebogeng Bone Kobe, Joseph Chuma, Rodrigo Jamisola Jr, and Matthews Chose. A Review on Quality Factor Enhanced On-chip Microwave Planar Resonators. Engineering Science and Technology, an International Journal, 20(2):460–466, 2017.

[132] Behzad Razavi. Design of Millimeter-wave CMOS Radios: A Tutorial. IEEE Transactions on Circuits and Systems I: Regular Papers, 56(1):4–16, 2009.

[133] Thomas H Lee. Planar Microwave Engineering: a Practical Guide to Theory, Measurement, and Circuits, volume 1. Cambridge university press, 2004.

[134] Ken-ya Hashimoto. RF Bulk Acoustic Wave Filters for Communications. Artech House, 2009.

[135] Rodolphe Boudot, Gilles Martin, Jean-Michel Friedt, and Enrico Rubiola. Frequency Flicker of 2.3 Ghz Aln-sapphire High-overtone Bulk Acoustic Resonators. Journal of Applied Physics, 120(22), 2016.

[136] Marco G Beghi. Modeling and Measurement Methods for Acoustic Waves and for Acoustic Microdevices. BoD–Books on Demand, 2013.

[137] Tetsuya Kimura, Yutaka Kishimoto, Masashi Omura, and Ken-ya Hashimoto. 3.5 Ghz Longitudinal Leaky Surface Acoustic Wave Resonator Using a Multilayered Waveguide Structure for High Acoustic Energy Confinement. Japanese journal of applied physics, 57(7S1):07LD15, 2018.

[138] S.J. Fiedziuszko and S. Holmes. Dielectric Resonators Raise Your High-Q. IEEE Microwave Magazine, 2(3):50–60, 2001.

[139] AG Mungall and H Daams. Cesium Beam Frequency Standard Cavity Design. Metrologia, 6(2):60, 1970.

[140] SaettaLabs. Sapphire Loaded Cavity Oscillator Data Sheet, 8.0, 10.0, 10.24 Ghz. `https://saettalabs.com/pdfs/saetta-slco-datasheet-v1.0.pdf`. Accessed: 2024-08-28.

[141] Yuanyan Su, Christoph Affolderbach, Matthieu Pellaton, Gaetano Mileti, and Anja K. Skrivervik. A Wide-frequency-tuning Micro-loop-gap Resonator for Miniature Rubidium Vapor-cell Atomic Frequency Standards. IEEE Transactions on Microwave Theory and Techniques, 71(12):5135–5146, 2023.

[142] Maddalena Violetti, Matthieu Pellaton, Christoph Affolderbach, Francesco Merli, Jean-François Zürcher, Gaetano Mileti, and Anja K. Skrivervik. The Microloop-gap Resonator: A Novel Miniaturized Microwave Cavity for Double-resonance Rubidium Atomic Clocks. IEEE Sensors Journal, 14(9):3193–3200, 2014.

[143] Wen Xuan Tang, Hao Chi Zhang, Hui Feng Ma, Wei Xiang Jiang, and Tie Jun Cui. Concept, Theory, Design, and Applications of Spoof Surface Plasmon Polaritons at Microwave Frequencies. Advanced Optical Materials, 7(1):1800421, 2019.

[144] Min Suk Kim, Markondeya Raj Pulugurtha, Venky Sundaram, Rao R. Tummala, and Hobie Yun. Ultrathin High- Q 2-D and 3-D RF Inductors in Glass Packages. IEEE Transactions on Components, Packaging and Manufacturing Technology, 8(4):643–652, 2018.

[145] A. Hajimiri and T.H. Lee. A General Theory of Phase Noise in Electrical Oscillators. IEEE Journal of Solid-State Circuits, 33(2):179–194, 1998.

[146] Behzad Razavi. A Study of Phase Noise in CMOS Oscillators. IEEE journal of Solid-State circuits, 31(3):331–343, 1996.

[147] P. Andreani, Xiaoyan Wang, L. Vandi, and A. Fard. A Study of Phase Noise in Colpitts and Lc-tank CMOS Oscillators. IEEE Journal of Solid-State Circuits, 40(5):1107–1118, 2005.

[148] Thomas W. Brown, Farhad Farhabakhshian, Ankur Guha Roy, Terri S. Fiez, and Kartikeya Mayaram. A 475 Mv, 4.9 Ghz Enhanced Swing Differential Colpitts VCO with Phase Noise of -136 dBc/Hz at a 3 Mhz Offset Frequency. IEEE Journal of Solid-State Circuits, 46(8):1782–1795, 2011.

[149] Andrea Mazzanti and Pietro Andreani. Class-c Harmonic CMOS Vcos, with a General Result on Phase Noise. IEEE Journal of Solid-State Circuits, 43(12):2716–2729, 2008.

[150] B. Soltanian and P.R. Kinget. Tail Current-shaping to Improve Phase Noise in LC Voltage-controlled Oscillators. IEEE Journal of Solid-State Circuits, 41(8):1792–1802, 2006.

[151] Jong-Phil Hong and Sang-Gug Lee. Low Phase Noise G_m-boosted Differential Gate-to-source Feedback Colpitts CMOS VCO. IEEE Journal of Solid-State Circuits, 44(11):3079–3091, 2009.

[152] Randall W Rhea. Discrete Oscillator Design: Linear, Nonlinear, Transient, and Noise Domains. Artech House, 2010.

[153] C.K. Boggs, A.D. Doak, and F.L. Walls. Measurement of Voltage Noise in Chemical Batteries. In Proceedings of the 1995 IEEE International Frequency Control Symposium (49th Annual Symposium), pages 367–373, 1995.

[154] R. Lutwak, A. Rashed, M. Varghese, G. Tepolt, J. Leblanc, M. Mescher, D.K. Serkland, and G.M. Peake. The Miniature Atomic Clock - Pre-production Results. In 2007 IEEE International Frequency Control Symposium Joint with the 21st European Frequency and Time Forum, pages 1327–1333, 2007.

[155] Rodolphe Boudot and Enrico Rubiola. Phase Noise in RF and Microwave Amplifiers. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 59(12):2613–2624, 2012.

[156] Rubiola, Enrico. The Leeson effect-Phase noise in quasilinear oscillators. arXiv preprint physics/0502143, 2005.

[157] G. Cibiel, M. Regis, O. Llopis, A. Rennane, L. Bary, R. Plana, Y. Kersale, and V. Giordano. Optimization of an Ultra Low-phase Noise Sapphire-SiGe HBT Oscillator Using Nonlinear CAD. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 51(1):33–41, 2004.

[158] N. Garmendia and J. Portilla. Study of PM Noise and Noise Figure in Low Noise Amplifiers Working Under Small and Large Signal Conditions. In 2007 IEEE/MTT-S International Microwave Symposium, pages 2095–2098, 2007.

[159] Jason Breitbarth, Srdjan Pajic, Narisi Wang, and Zoya Popovic. Additive Phase Noise in Linear and High-efficiency X-band Power Amplifiers. In 2006 IEEE MTT-S International Microwave Symposium Digest, pages 1871–1874, 2006.

[160] G. Cibiel, L. Escotte, and O. Llopis. A Study of the Correlation Between High-frequency Noise and Phase Noise in Low-noise Silicon-based Transistors. IEEE Transactions on Microwave Theory and Techniques, 52(1):183–190, 2004.

[161] William Loh, Siva Yegnanarayanan, Rajeev J. Ram, and Paul W. Juodawlkis. Unified Theory of Oscillator Phase Noise II: Flicker Noise. IEEE Transactions on Microwave Theory and Techniques, 61(12):4130–4144, 2013.

[162] Salvatore Levantino. Calibration Techniques in Phased-locked Loops: Theoretical Basis and Practical Applications. IEEE Solid-State Circuits Magazine, 16(3):37–44, 2024.

[163] Hangil Choi and SeongHwan Cho. A 7.5-ghz Subharmonic Injection-locked Clock Multiplier Featuring a 120× Multiplying Factor and 92.3-fs RMS Jitter Including Reference Spur. IEEE Journal of Solid-State Circuits, 59(12):3928–3937, 2024.

[164] Qiaochu Zhang, Shiyu Su, Cheng-Ru Ho, and Mike Shuo-Wei Chen. A Fractional-n Digital MDLL with Background Two-point DTC Calibration. IEEE Journal of Solid-State Circuits, 57(1):80–89, 2022.

[165] Haosheng Zhang, Hans Herdian, Aravind Tharayil Narayanan, Bangan Liu, Rui Wu, Atsushi Shirane, and Kenichi Okada. A- 194 dBc/Hz Fom VCO with Low-supply Sensitivity for Ultra-low-power Atomic Clock. In 2018 Asia-Pacific Microwave Conference (APMC), pages 788–790. IEEE, 2018.

[166] Marc Tiebout. Low Power VCO Design in CMOS, volume 20. Springer Science & Business Media, 2006.

[167] Fei Yu. A Low-voltage and Low-power 3-ghz CMOS LC VCO for S-band Wireless Applications. Wireless Personal Communications, 78(2):905–914, 2014.

[168] Luca Fanori and Pietro Andreani. Highly Efficient Class-c CMOS Vcos, Including a Comparison with Class-b Vcos. IEEE Journal of Solid-State Circuits, 48(7):1730–1740, 2013.

[169] Masoud Babaie and Robert Bogdan Staszewski. A Class-f CMOS Oscillator. IEEE Journal of Solid-State Circuits, 48(12):3120–3133, 2013.

[170] Yu-Teng Chang and Hsin-Chia Lu. A K -band High-efficiency VCO Using Current Reused Technique. IEEE Microwave and Wireless Components Letters, 27(12):1134–1136, 2017.

[171] Steve C Cripps et al. RF Power Amplifiers for Wireless Communications, volume 250. Artech house Norwood, MA, 2006.

[172] Megan Lauree Kelleher, Konrad Ziegler, Jeremy Robin, Lianxin Huang, Mitchel Button, Liam Mauck, Judith Olson, Peter Brewer, Danny Kim, John Kitching, Ruwan Senaratne, William R. McGehee, and Travis M. Autry. Wafer-Scale Micro-Knife Sealed Vacuum Cells for Quantum Devices, April 2026. arXiv:2602.00390 [physics].

[173] Alexander Staron, Gabriela Martinez, Nicholas Nardelli, Travis Autry, John Kitching, and William McGehee. Doppler Shift Mitigation in a Chip-Scale Atomic Beam Clock, December 2025. arXiv:2512.04905 [physics].

[174] Mohammad Khalaj-Amirhosseini. Wideband or multiband complex impedance matching using microstrip nonuniform transmission lines. Progress In Electromagnetics Research, 66:15–25, 2006.

[175] H. SHIRAI. Tapered Transmission Line Resonators and Their Application to Filters. The 3rd Asia-Pacific Microwave Conference Proceedings, 1990, 1990.

[176] H. Zirath, R. Kozhuharov, and M. Ferndahl. Balanced Colpitt oscillator MMICs designed for ultra-low phase noise. IEEE Journal of Solid-State Circuits, 40(10):2077–2086, October 2005. Conference Name: IEEE Journal of Solid-State Circuits.

[177] Paul Flaten and Zoya Popović. Broadband GaN Power Amplifier MMIC with a Nonuniform Transmission Line Output Network. In 2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), pages 70–73, January 2024.

[178] Paul Flaten and Zoya Popović. Automated Design of Nonuniform Transmission Lines for Practical Microwave Circuits. IEEE Transactions on Microwave Theory and Techniques, 73(10):7809–7821, October 2025.

[179] Motoaki Hara, Yuichiro Yano, Hiroyuki Ito, Masaya Toda, Takahito Ono, Masatoshi Kajita, Shinsuke Hara, Akifumi Kasamatsu, and Tetsuya Ido. FBAR Oscillator Stabilized by Rb Atomic Resonator for SHF/EHF-Band Wireless Devices. In 2018 IEEE International Ultrasonics Symposium (IUS), pages 1–9, Kobe, October 2018. IEEE.

[180] Alec Russell, Paul Flaten, and Zoya Popović. Low Phase Noise InGaP/GaAs HBT MMIC VCO With Nonuniform Transmission Line Resonator for a Chip-Scale Atomic Beam Clock. IEEE Microwave and Wireless Technology Letters, 35(8):1222–1225, August 2025.

[181] Libo Qian, Jifei Sang, Yinshui Xia, Jian Wang, and Peiyi Zhao. Investigating on Through Glass via Based RF Passives for 3-D Integration. IEEE Journal of the Electron Devices Society, 6:755–759, 2018.

[182] Tobias Chaloun, Susanne Brandl, Norbert Ambrosius, Kevin Kröhnert, Holger Maune, and Christian Waldschmidt. RF Glass Technology Is Going Mainstream: Review and Future Applications. IEEE Journal of Microwaves, 3(2):783–799, April 2023.

[183] Chen Yu, Shaocheng Wu, Yi Zhong, Rongbin Xu, Tian Yu, Jin Zhao, and Daquan Yu. Application of Through Glass Via (TGV) Technology for Sensors Manufacturing and Packaging. Sensors, 24(1), December 2023.

[184] Vijay Sukumaran, Tapobrata Bandyopadhyay, Venky Sundaram, and Rao Tummala. Low-Cost Thin Glass Interposers as a Superior Alternative to Silicon and Organic Interposers for Packaging of 3-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2(9):1426–1433, September 2012.

[185] Manyu Wang, Limin Liu, Yuwen Hu, Tian Yu, Shiwei Huang, Chen Yu, Hengxiang Zhang, Xiao Luo, Qi Chen, Wenbiao Ruan, and Daquan Yu. Research on high inductance and quality factor embedded 3D inductors using ultra-high aspect ratio TGV technology. Materials Science in Semiconductor Processing, 192:109388, June 2025.

[186] Guanyu Zhou, Libin Gao, Yuzhe Chen, Hongwei Chen, Wenlei Li, Chao Zhang, Jinxu Liu, and Jihua Zhang. High Inductance Density Glass Embedded Inductors for 3-D Integration. IEEE Microwave and Wireless Technology Letters, 33(6):679–682, June 2023.

[187] Arian Rahimi, David E. Senior, Aric Shorey, and Yong-Kyu Yoon. In-Substrate Resonators and Bandpass Filters with Improved Insertion Loss in K-Band Utilizing Low Loss Glass Interposer Technology and Superlattice Conductors. In 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), pages 1322–1328, May 2016.

[188] Gapyeol Park, Kyungjun Cho, Kyungjune Son, Hyunwook Park, Daehwan Lho, Seongguk Kim, Taein Shin, Youngwoo Kim, Joungho Kim, Atom Watanabe, Pulugurtha Markondeya Raj, Venky Sundaram, and Rao Tummala. Design and Measurement of a 28 GHz Glass Band Pass Filter based on Glass Interposers for 5G Applications. In 2019 Electrical Design of Advanced Packaging and Systems (EDAPS), pages 1–3, December 2019. ISSN: 2151-1233.

[189] Jeb Flemming, Kyle McWethy, Rob Hulsman, and Mohamed Basha. 3DGS 3D Heterogeneous Integrated RF Multi-Layers Glass-Interposer System-in-Package. In 2025 IEEE/MTT-S International Microwave Symposium - IMS 2025, pages 761–764, June 2025. ISSN: 2576-7216.

[190] Jabeom Koo, Keping Wang, Richard Ruby, and Brian P. Otis. A 2-GHz FBAR-Based Transformer Coupled Oscillator Design With Phase Noise Reduction. IEEE Transactions on Circuits and Systems II: Express Briefs, 66(4):542–546, April 2019.

[191] Rich Ruby, Martha Small, Frank Bi, Don Lee, Lori Callaghan, Reed Parker, and Steve Ortiz. Positioning FBAR technology in the frequency and timing domain. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 59(3):334–345, March 2012.

[192] Kannan Sankaragomathi, Lori Callaghan, Richard Ruby, and Brian Otis. A 220dB FOM, 1.9GHz oscillator using a phase noise reduction technique for high-Q oscillators. In 2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pages 31–34, June 2013. ISSN: 2375-0995.

[193] Alec Russell, Christopher Nordquist, Alexander Staron, William McGehee, and Zoya Popovic. MMIC Oscillator Using High-Q Glass Embedded Resonator for a Chip-Scale Atomic Beam Clock (Submitted). IEEE Transactions on Microwave Theory and Techniques, 2026.

[194] Jeong-Geun Kim, Dong-Hyun Baek, Sanghoon Jeon, Jae-Woo Park, and Songcheol Hong. A K-band InGaP/GaAs HBT balanced MMIC VCO. IEEE Microwave and Wireless Components Letters, 13(11):478–480, November 2003. Conference Name: IEEE Microwave and Wireless Components Letters.

[195] Thanh Ngoc Thi Do, Szhau Lai, Mikael Horberg, Herbert Zirath, and Dan Kuylenstierna. A MMIC GaN HEMT Voltage-Controlled-Oscillator with High Tuning Linearity and Low Phase Noise. In 2015 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), pages 1–4, October 2015. ISSN: 2374-8443.

[196] Travagnin M. Next-generation Chip Scale Atomic Clocks - Assessing the Emerging Physical Platforms: Microwave Transitions in Cold Atoms and in Trapped Ions, and Optical Transitions in Warm Vapours. (KJ-NA-31003-EN-N (online)), 2022.

[197] Michael A. Trigatzis, Martin Knapp, Sean Mulholland, Gary I. Hockley, Geoffrey P. Barwood, Guilong Huang, Hugh A. Klein, and Patrick Gill. Progress Towards a Transportable Laser-cooled Yb+microwave Clock. In 2024 European Frequency and Time Forum (EFTF), pages 120–122, 2024.

[198] John Kitching, Matt Hummon, William McGehee, Ying-Ju Wang, and Susan Schima. Next-generation Chip Scale Atomic Clocks. In Journal of Physics: Conference Series, volume 2889, page 012015. IOP Publishing, 2024.

[199] Mina Kim, Cheng Wang, Zhi Hu, and Ruonan Han. Chip-scale Terahertz Carbonyl Sulfide Clock: an Overview and Recent Studies on Long-term Frequency Stability of OCS Transitions. IEEE Transactions on Terahertz Science and Technology, 9(4):349–363, 2019.

[200] William F. McGrew, James Greenberg, Keisuke Nose, Brendan M. Heffernan, and Antoine Rolland. Terahertz Molecular Frequency References: Theoretical Analysis of Optimal Instability. IEEE Transactions on Terahertz Science and Technology, 15(6):1068–1074, 2025.

[201] Thai M Hoang, Sang K Chung, Thanh Le, Sehyun Park, Sung-Jin Park, J Gary Eden, Christopher Holland, Hao Wang, Omeed Momeni, Russell Bradley, et al. Micro Mercury Trapped Ion Clock Prototypes with 10^{-14} Frequency Stability in 1-liter Packages. Scientific reports, 13(1):10629, 2023.

[202] Thai M Hoang, Sang K Chung, Thanh Le, John D Prestage, Lin Yi, Robert L Tjoelker, Sehyun Park, Sung-Jin Park, J Gary Eden, Christopher Holland, et al. Integrated Physics Package of Micromercury Trapped Ion Clock with 10^{-14}-level Frequency Stability. Applied Physics Letters, 119(4), 2021.

[203] Thai M. Hoang, Sang K. Chung, Thanh Le, John D. Prestage, Lin Yi, Robert I. Tjoelker, and Nan Yu. Performance of Micro Mercury Trapped Ion Clock. In 2019 Joint Conference of the IEEE International Frequency Control Symposium and European Frequency and Time Forum (EFTF/IFC), pages 1–2, 2019.

[204] Hao Wang and Omeed Momeni. A Charge Pump Current Mismatch Compensation Design for Sub-sampling PLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(6):1852–1856, 2021.

[205] S Mulholland, HA Klein, GP Barwood, S Donnellan, PBR Nisbet-Jones, G Huang, G Walsh, PEG Baird, and P Gill. Compact Laser System for a Laser-cooled Ytterbium Ion Microwave Frequency Standard. Review of Scientific Instruments, 90(3), 2019.

[206] Sean Mulholland. Development of a Portable Laser-cooled Ytterbium Ion Microwave Atomic Clock. PhD thesis, University of Oxford, 2019.

[207] Peter Schwindt. Development of (miniaturized) Trapped Yb Ion Clocks. Technical report, Sandia National Lab.(SNL-NM), Albuquerque, NM (United States), 2017.

[208] DA Thrasher and PDD Schwindt. Performance of $3\,\mathrm{cm}^3$ Ion Trap Vacuum Package Sealed for 10 Years. Applied Physics Letters, 126(13), 2025.

[209] Peter DD Schwindt, Yuan-Yu Jau, Heather Partner, Adrian Casias, Adrian R Wagner, Matthew Moorman, Ronald P Manginell, James R Kellogg, and John D Prestage. A Highly Miniaturized Vacuum Package for a Trapped Ion Atomic Clock. Review of Scientific instruments, 87(5), 2016.

[210] William F McGrew, Xiaogang Zhang, H Leopardi, RJ Fasano, Daniele Nicolodi, Kyle Beloy, Jian Yao, Jeffrey A Sherman, Stefan A Schaeffer, Joshua Savory, et al. Towards the Optical Second: Verifying Optical Clocks at the SI Limit. Optica, 6(4):448–454, 2019.

[211] Andrew D. Ludlow, Martin M. Boyd, Jun Ye, E. Peik, and P. O. Schmidt. Optical Atomic Clocks. Rev. Mod. Phys., 87:637–701, Jun 2015.

[212] Zachary L. Newman, Vincent Maurice, Connor Fredrick, Tara Fortier, Holly Leopardi, Leo Hollberg, Scott A. Diddams, John Kitching, and Matthew T. Hummon. High-performance, Compact Optical Standard. Opt. Lett., 46(18):4702–4705, Sep 2021.

[213] Jonathan D. Roslund, Arman Cingöz, William D. Lunden, Guthrie B. Partridge, Abijith S. Kowligy, Frank Roller, Daniel B. Sheredy, Gunnar E. Skulason, Joe P. Song, Jamil R. Abo-Shaeer, and Martin M. Boyd. Optical clocks at sea. Nature, 628(8009):736–740, April 2024.

[214] Timothy Sonnenberg, Shane Verploegh, Mauricio Pinto, and Zoya Popović. W-Band GaN HEMT Frequency Multipliers. IEEE Transactions on Microwave Theory and Techniques, 71(10):4327–4336, October 2023.

[215] James P. Mawdsley. Terahertz frequency synthesis in CMOS for a chip-scale molecular clock. PhD thesis, Massachusetts Institute of Technology, 2019.

[216] Minah Kim. Design and Analysis of High-Stability THz Molecular Clock System. PhD thesis, Massachusetts Institute of Technology, September 2022.

[217] Rodolphe Boudot, StÉphane Guerandel, and Emeric de Clercq. Simple-Design Low-Noise NLTL-Based Frequency Synthesizers for a CPT Cs Clock. IEEE Transactions on Instrumentation and Measurement, 58(10):3659–3665, October 2009. Conference Name: IEEE Transactions on Instrumentation and Measurement.

[218] Timothy Sonnenberg, Anthony Romano, Shane Verploegh, Mauricio Pinto, and Zoya Popović. V- and W-Band Millimeter-Wave GaN MMICs. IEEE Journal of Microwaves, 3(1):453–465, January 2023.

[219] Szhau Lai, Dan Kuylenstierna, Mustafa Ozen, Mikael Horberg, Niklas Rorsman, Iltcho Angelov, and Herbert Zirath. Low Phase Noise GaN HEMT Oscillators With Excellent Figures of Merit. IEEE Microwave and Wireless Components Letters, 24(6):412–414, June 2014.

[220] Picosecond Pulse Labs. A New Breed of Comb Generators Featuring Low Phase Noise and Low Input Power, May 2006.

[221] Joel Johnson, Cody Scarborough, and Zoya Popović. Nonlinear Transmission Line GaN MMIC Frequency Comb Generator. IEEE Transactions on Microwave Theory and Techniques, 73(6):3075–3084, June 2025.

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