**Linear and Efficient Power Amplifiers from *S*- to *V*-Band**

by

**Reyes K. Lucero**

B.A., Coe College, 2021

M.S., University of Colorado Boulder, 2023

A thesis submitted to the

Faculty of the Graduate School of the

University of Colorado in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

Department of Electrical And Computer Engineering

2026

Committee Members:

Zoya Popović, Chair

Prof. Tommaso Cappello

Prof. Taylor Barton

Dr. Scott Schafer

Prof. Laila Marzall

Dr. Marc Vanden Bossche

Lucero, Reyes K. (Ph.D., Electrical Engineering)

Linear and Efficient Power Amplifiers from $S$- to $V$-Band

Thesis directed by Prof. Zoya Popović

The modern era of global connectivity has impacted humanity in broad and intangible ways, which we are only beginning to understand. One definite impact has been on radio hardware, where the demand for wirelessly delivered digital information has forced a shift to higher frequencies, with wide instantaneous bandwidths (IBWs) and more digital architectures. New modulation protocols have allowed higher bit-rates but, combined with higher frequencies and wider IBWs, have negatively impacted the power efficiency of radio hardware. The opposing requirements of high linearity to support these communications protocols, as well as high efficiencies for mobile and embedded applications, have spurred innovation, particularly in power amplifiers (PAs). This thesis focuses on GaN-on-SiC power amplifiers for linear and efficient wireless communications from $S$- through $V$-Band (2.25-65 GHz). A variety of GaN technologies are used, from commercial 250, 150, and 120 nm processes, as well as a research millimeter-wave (mmW) 40 nm process. This thesis begins with an efficiency enhancement technique, known as supply modulation or envelope tracking. Improvements to the technique are demonstrated. In particular, a new method for optimizing device size to maximize the efficiency enhancement technique, as well as the integration of a highly-efficient flying capacitor-based supply modulator with a $C$-band hybrid PA. The following chapter presents a similar technique for linearity improvement, known as gate-modulation, which is demonstrated by a $Ku$-band PA integrated with an analog gate-modulator with measured linearity improvements with signals up to 1 GHz in IBW. The next chapters focus on the characterization of PAs under modulated excitation, including a novel technique, known as network emulation, to directly measure a matching network response on a nonlinear device, without nonlinear simulations or models. Finally, the last chapter returns to PA architectures, specifically load-modulation, and an extension to network emulation to include load-modulated architectures is demonstrated.

## Dedication

For my family.

## Acknowledgements

The phrase "it takes a village" probably originated in a doctoral program. I cannot hope to properly acknowledge all of the help and support I have received to reach this point. First and foremost, I thank my advisor, Prof. Zoya Popović, who has given me immeasurable support throughout my time in the program. Her unwavering dedication to students is truly incredible. Prof. Gregor Lasser and Dr. Jeanne Quimby also deserve sincere thanks for helping me through my first semester and setting a strong foundation. An enormous thank you is also owed to Dr. Marc Vanden Bossche. His tireless efforts to bring new measurement capability to the lab, along with many years of patient explanation and guidance, were instrumental to my work.

Thank you to my fellow graduate students. Connor Nogales and Paul Flaten, in particular, deserve special recognition for being my office mates and for handling nonstop questions every day for two years with grace and patience. I am also grateful to current and alumni group members—Laila Marzall, Jooeun Lee, Devon Donahue, Seth Johannes, Alec Russell, Joseph Dunbar, Jori Platt, Yaqub Mashud, Joel Johnson, and Ben Cross—for their high-quality technical discussions and for deepening my understanding. Thank you to the entire RF and microwave research group for the camaraderie, entertainment (you know who you are), and sense of community. Finally, thank you to all of the friends and family who have supported me every step of this journey.

Alec, Seth, Conner—do you have your skis, boots, poles, and pass?

# Contents

**Chapter**


**1** Introduction **1**

1.1 Background and Motivation . . . 1

1.1.1 Wireless Communications . . . 2

1.2 Efficient and Linear Power Amplifier Architectures . . . 3

1.2.1 Signal Impact on PA Performance . . . 9

1.2.2 Efficiency Enhancement Techniques . . . 16

1.2.3 Linearity Enhancement Techniques . . . 18

1.3 Thesis Outline . . . 20

**2** Supply Modulation for Efficiency Enhancement **22**

2.1 Introduction . . . 22

2.2 Efficiency Improvement through Periphery Optimization . . . 23

2.2.1 Power Amplifier Design . . . 25

2.2.2 Simulated Dynamic Performance . . . 26

2.2.3 Measured Performance . . . 29

2.2.4 Periphery Optimization Conclusion . . . 32

2.3 Hybrid PA integration with Highly Efficient Discrete Supply Modulator . . . 34

2.3.1 Design and Characterization of $C$-band Hybrid PA . . . 35

2.3.2 Integration with DSM . . . 35

2.3.3 Results . . . 39
2.4 Conclusion . . . 42

**3 Gate Modulation for Linearity Enhancement** **44**
3.1 Integration of a Ku-Band GaN PA with GaAs Gate Modulator . . . 46
3.2 GaN MMIC Power Amplifier . . . 48
3.2.1 CW PA Characterization . . . 49
3.3 Envelope Detector GaAs MMIC . . . 52
3.4 Envelope Co-Simulations . . . 55
3.4.1 System Performance Considerations . . . 56
3.5 MMIC Integration . . . 57
3.6 Transmitter Measurements and Linearization Results . . . 58
3.6.1 Two-Tone Measurements . . . 58
3.6.2 ACPR and EVM . . . 66
3.7 Conclusion . . . 68

**4 Multi-tone signals for Nonlinear Power Amplifier Characterization** **70**
4.1 Introduction . . . 70
4.2 Description of Experimental Setup . . . 71
4.2.1 Device Selection . . . 72
4.2.2 Calibration . . . 73
4.3 Transistor Pre-Characterization . . . 75
4.3.1 Harmonic Impedance Control . . . 75
4.3.2 Baseband Impedance Control . . . 77
4.3.3 CW load pull Response and Model Comparison . . . 78
4.4 Signal Generation . . . 79
4.5 Modulated Transistor Characterization . . . 81
4.5.1 Varying PAPR . . . 84

4.5.2 Varying Bandwidth . . . 86
4.5.3 Weighted PDF Implications . . . 88
4.6 Linearity . . . 90
4.7 Discussion and Conclusions . . . 93

**5 Network Emulation for PA Design for Communications Applications 96**
5.1 Tuner Validation . . . 98
5.2 Equivalent Source Method for 2-Port Network Emulation . . . 101
5.3 Equivalent Source Method for N-Port Network Emulation . . . 104
5.4 Demonstration of Network Emulation . . . 109
5.4.1 Hardware and Circuit Design . . . 110
5.4.2 Results . . . 113
5.5 Discussion and Conclusions . . . 114

**6 Emulation of Load Modulated Power Amplifiers 117**
6.1 Principles of Wideband Arbitrary Load Modulation (WALM) . . . 118
6.1.1 Real Time Active Load Pull . . . 119
6.1.2 WALM Theory . . . 121
6.2 Validation Measurements . . . 128
6.3 Conclusion . . . 133

**7 Conclusions and Future Work 136**
7.1 Thesis Conclusion . . . 136
7.2 Thesis Contributions . . . 137
7.3 Future Work . . . 139
7.3.1 *V*-Band Doherty Amplifier . . . 140
7.3.2 Emulated Doherty PA . . . 142

**Bibliography** **148**

# Tables

**Table**

2.1 Maximum Simulated PAE Values for Different Peripheries . . . . . 26

3.1 Summary of GaN PAs Covering all or Part of Ku-Band . . . . . 50

3.2 Summary of Recent Analog Linearizers . . . . . 63

3.3 Measured EVM for a 100 MHz 5G Signal with and without Dynamic Gate Modulation 68

5.1 Results of Source and Load Pull . . . . . 101

5.2 Error between Emulation and Measurement in Power Sweep . . . . . 115

6.1 RMS errors for Different Polynomial Fit Orders . . . . . 126

6.2 RMS Errors for Different Signal Thresholds . . . . . 126

7.1 Summary of Recent *V/E*-Band GaN Doherty Amplifiers . . . . . 142

7.2 Transmission Line Lengths in Doherty Emulated Networks . . . . . 145

# Figures

**Figure**


1.1 Terrestrial Mobile Data Usage Forecast . . . 2

1.2 Simplistic Model of a Single-Stage FET-Based Power Amplifier. . . . 4

1.3 Time-Domain Waveforms of Different PA Classes . . . 5

1.4 Performance over Conduction Angle . . . 7

1.5 Linearity vs. Efficiency . . . 8

1.6 Histogram of Various Cellular Standards . . . 8

1.7 PA Class Performance over Backoff . . . 10

1.8 Load-Line Model Output Power and Drain Efficiency . . . 10

1.9 Load-Line Model Gain and Linearity . . . 11

1.10 Load-Line Model Synthetic Benchmarks . . . 12

1.11 Linearity, Efficiency, Gain Venn Diagram . . . 13

1.12 A General Communications Transmitter . . . 15

2.1 Commercial Envelope Tracking . . . 23

2.2 Device Scaling PA Photomicrographs . . . 25

2.3 Maximum PAE $\Gamma_{LS}$ for the Different Peripheries . . . 27

2.4 Device Sizing Drive Up . . . 28

2.5 Device Sizing Simulated Performance . . . 28

2.6 Small Signal Results for DSM PAs . . . 29

2.7 Large Signal Results for DSM PAs . . . 30
2.8 DSM Test Bench . . . 32
2.9 Device Sizing Dynamic Performance at 67 MHz . . . 33
2.10 Photograph of the 10 W Hybrid Power Amplifier . . . 34
2.11 Large-Signal Performance of Hybrid PA over Frequency . . . 36
2.12 Large-Signal Performance of Hybrid PA over $P_{out}$ . . . 36
2.13 Photograph of the DSM Measurement Setup . . . 37
2.14 Block Diagram of the Measurement System . . . 38
2.15 Aligned DSM and RF PA . . . 39
2.16 PAE with Dynamic and Static $V_{ds}$ . . . 40
2.17 $P_{diss}$ with Dynamic and Static $V_{ds}$ . . . 41
2.18 ACPR with Dynamic and Static $V_{ds}$ . . . 41
2.19 Instantaneous gain for Hybrid PA with FCML . . . 42
2.20 Frequency Spectra in Static and Dynamic Cases . . . 43

3.1 High-level Block Diagram of Gate-Modulation Analog Linearization Approach. . . . 45
3.2 Linearity, Efficiency, and Gain with Gate Modulation Trajectory . . . 46
3.3 Gain and Linearity for Drain and Gate Modulation and Static Load-Line Cases. . . . 47
3.4 Drain Efficiency and LEG benchmark for Drain and Gate Modulation and Static Load-Line Cases. . . . 47
3.5 System Level Analog Gate Modulation Diagram . . . 48
3.6 Layout and Photograph of GaN *Ku*-Band PA . . . 49
3.7 Ku-Band PA Small-Signal Performance . . . 50
3.8 Ku Band PA Large-Signal PA Performance . . . 51
3.9 Ku-Band PA Static AM-AM and AM-PM . . . 52
3.10 Layout and Photomicrograph of Envelope Detector MMIC . . . 53
3.11 Ku-Band Envelope Detector 2-tone Measurement Results . . . 54

3.12 Ku-Band Envelope Detector LTE Signal Measurement Results . . . . . 54
3.13 Ku-Band Envelope Detector Small-Signal RF Performance . . . . . 55
3.14 Ku-Band Envelope Simulation Linearization Results . . . . . 57
3.15 Fully Assembled Ku-Band Envelope Tracking Linearization System . . . . . 59
3.16 Experimental Setup for Characterizing Gate-Tracked Linearization System . . . . . 60
3.17 Measured detector voltage response when loaded with the PA gate. . . . . 60
3.18 Large Signal System CW Performance . . . . . 61
3.19 HFSS PCB-to-MMIC Transition Modeling . . . . . 61
3.20 HFSS PCB-to-MMIC Simulated Performance . . . . . 62
3.21 $IMD_3$ Suppression and Corresponding $\tau, A$ coefficients . . . . . 63
3.22 Measured $IMD_3$ Improvement for Different Optimization Strategies . . . . . 64
3.23 Large-Signal System Performance with and without Gate-Modulation Applied . . . . 65
3.24 Measured ACPR Improvement with a 100 MHz 5G Signal . . . . . 67
3.25 AM-AM and AM-PM for a 100 MHz 5G signal with and without Gate-Modulation Applied . . . . . 68

4.1 Block Diagram of the Vector Passive Load Pull System . . . . . 71
4.2 Photograph of the Measurement System . . . . . 72
4.3 TRL Standard and DUT Mounting Fixture . . . . . 73
4.4 Diagram of the Harmonic Trap and Bias-Tee Board . . . . . 74
4.5 Measured Circuit Response of Bias Tee and Harmonic Traps . . . . . 76
4.6 Validation of the Load Pull System . . . . . 77
4.7 Excess Kurtosis and PAPR Plotted Across Number of Tones in a Multi-Tone . . . . 79
4.8 PDFs of Multi-Tone Test Signals . . . . . 81
4.9 Phase-Skew of Passive Tuner . . . . . 82
4.10 Difference in PAE and $P_{out}$ between CW and Multi-Tone Excitation . . . . . 83
4.11 Difference in $\Gamma_L$ for Maximum PAE and $P_{out}$ between CW and Multi-Tone Excitation 84

4.12 Difference in PAE and $P_{out}$ between CW and 2-Tone Excitation . . . . . 86

4.13 Difference in $\Gamma_L$ for Maximum PAE and $P_{out}$ between CW and 2-Tone Excitation . 87

4.14 Unweighted and Weighted Probability Density Functions of a Multi-Tone Signal . . 90

4.15 Unweighted and Weighted Probability Density Functions of a 2-Tone Signal . . . . . 91

4.16 NPR at $\Gamma_L$ Points for Maximum PAE and $P_{out}$ . . . . . 92

4.17 am-am and am-pm for 2 Multi-Tone Excitations . . . . . 93

4.18 am-am and am-pm for Two 2-Tones of Different IBWs . . . . . 93

5.1 Network Emulation of a Single-Stage Amplifier . . . . . 97

5.2 Outline of the Process and Layers that Compose Network Emulation. . . . . 99

5.3 Wideband Active Load Pull Validation . . . . . 100

5.4 Small-Signal Circuit for Demonstrating Network Emulation . . . . . 102

5.5 Network Equivalent Source . . . . . 103

5.6 Emulated and Simulated Small-Signal Response . . . . . 103

5.7 Conceptual Circuits Used in the Network Emulation Process. . . . . 104

5.8 Coupling Paths Accounted for by Network Emulation. . . . . 106

5.9 Network Emulation Block Diagram . . . . . 109

5.10 Photo of the Measurement System Used to Perform Network Emulation . . . . . 111

5.11 Emulation and Measurement Physical Setup . . . . . 112

5.12 Comparison of $\Gamma_{in}$ and $G_t$ between Emulation and Measurement . . . . . 113

5.13 Large-Signal Comparison between Emulation and Measurement . . . . . 114

6.1 Load Modulation with Two Current Sources Driving a Common Load . . . . . 118

6.2 CW RTALP in Frequency . . . . . 118

6.3 CW RTALP on the Smith Chart . . . . . 119

6.4 General Diagram of Two Devices Connected Together for Load-Modulation . . . . . 121

6.5 WALM Procedure . . . . . 123

6.6 Polynomial Fits to a Doherty Load Modulation Trajectory . . . . . 124

6.7 Main and Auxiliary Waveforms for Doherty Load Modulation . . . . . 125

6.8 Frequency Spectrum of Doherty Main and Auxiliary Stages . . . . . 127

6.9 Threshold vs. Polyfit . . . . . 129

6.10 Measured Two Tone $R_L(t)$ and $X_L(t)$ . . . . . 130

6.11 Measured Two Tone $R_L(t)$ and $X_L$ over Drive Power . . . . . 131

6.12 Measured Gain and $\eta$ Under Static and Load-Modulated Conditions . . . . . 132

6.13 Measured $\Gamma_L$ at the Internal and External Planes . . . . . 133

6.14 Ambiguity at Low Power Levels Due to Noise . . . . . 134

7.1 HRL T3 Doherty Reticle . . . . . 140

7.2 *V*-Band Doherty Layout . . . . . 140

7.3 *V*-Band Doherty Simulated Performance . . . . . 141

7.4 Emulated Doherty CW Large-Signal Response . . . . . 143

7.5 Emulated Doherty Matching Networks . . . . . 144

7.6 Impedance Trajectory of Main and Aux. in Emulated Doherty . . . . . 145

7.7 Large-Signal Response of main and Aux. in Emulated Doherty . . . . . 146

# Chapter 1

# Introduction

This thesis addresses the challenge of simultaneously achieving high efficiency and linearity in radio frequency (RF) power amplifiers (PAs) for modern wide-bandwidth, high peak-to-average-power ratio (PAPR) communication signals. It demonstrates that an inherent tradeoff exists between efficiency and linearity, which can only be mitigated at the expense of gain—the fundamental purpose of amplification. The work presents contributions spanning a range of efficiency- and linearity-enhancement techniques, along with new characterization methodologies for nonlinear communications PAs. These techniques are evaluated in the context of the overarching objective of realizing amplifiers that provide both linear and efficient gain, seeking to improve one metric with minimal degradation of the other, typically at some cost in gain. The proposed characterization methodologies aim to better quantify this tradeoff and to enable design tools that expose it more clearly at early stages of the PA design process.

## 1.1 Background and Motivation

The first electrical transatlantic communications occurred in 1858 via an undersea telegraph cable. While generally considered unsuccessful for the purpose of communicating information, this accomplishment marked an important first in creating an informationally connected world. The traditions of this first cable are continued today to a remarkable extent with 463 exabytes of information sent daily around the globe over physical electrical and optical cabling [31].

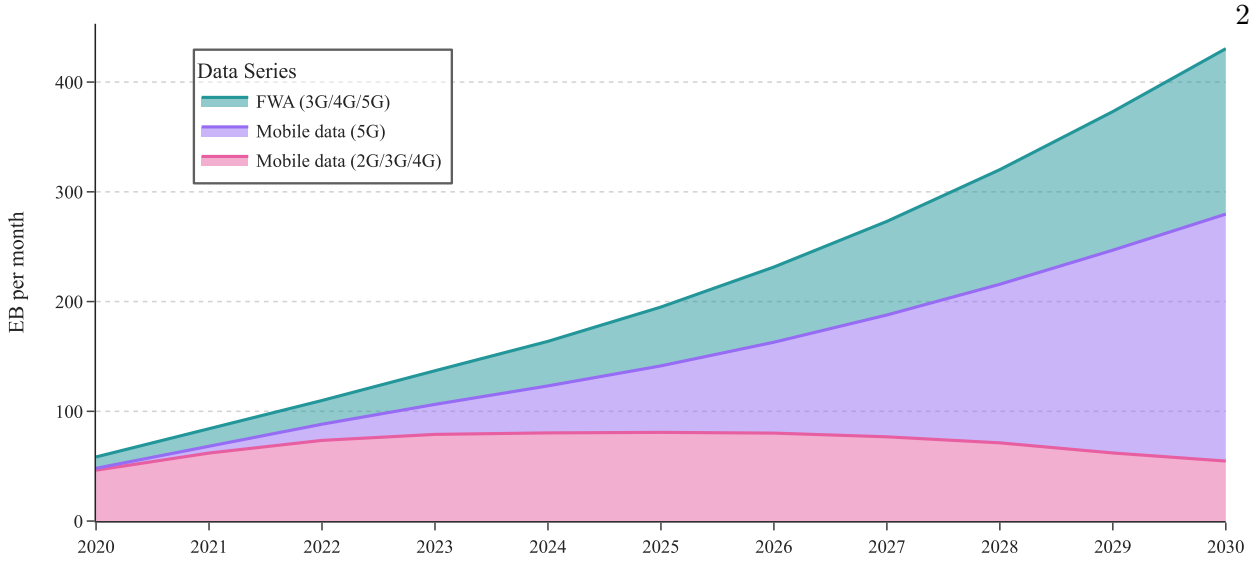



Figure 1.1: Terrestrial mobile data forecast from [117], demonstrating a dramatic predicted increase in the demand for mobile data. Note that this does not include direct-to-cell satellite communications, which is rapidly rising in popularity.

### 1.1.1 Wireless Communications

The current era of the internet and the mobile phone has created a seemingly insatiable demand for digital data capacity, seen in Fig.1.1. Mobile devices, in particular, have created a paradigm shift in how this data is delivered. Numerous factors and enabling technologies, from batteries to displays, to Moore's law, may be credited with placing devices with capabilities unimaginable a few decades ago into the hands of 5 billion people around the world [107]. One clear result of this is that mobile devices are poorly suited to cabled interconnects and require a wireless connection to the outside world.

Starting in the late 1970's with the first generation of mobile networks, the last-mile of global inter-connectivity began to be handled wirelessly. Presently, these networks have reached unprecedented affordability, traffic, and scope, necessitating incessant strides to support this increased demand.

A more recent, yet highly consequential paradigm shift in our communications networks is underway, which is the shifting of wireless links backwards from last-mile delivery to the backbone

of communications. Recent standards have included provisions for "wireless backhauls", the links between cell-towers (base-stations), a job traditionally relegated to high-speed fiber connections.

An even more modern shift unfolding is direct-to-user satellite data links. While most of this infrastructure still serves as a link between a mobile device and the existing cabled systems, there is demand to enable fully wireless device-device links with a satellite constellation intermediary between them.

There are hard physical limits that ensure that fiber-optics remain the dominant modality of information transfer. Additionally, many of the high-bandwidth fixed-wireless backhaul links, both terrestrial and inter-satellite, will likely be served optically. However, the present and future impact of wireless communications on RF and microwave hardware cannot be overstated.

The staggering complexity of achieving these links is multi-disciplinary, even within the field of microwave engineering. Fast digital signal processing, data converters, stable local oscillators (LOs), and fully digital phased arrays are just a few of the electrical challenges to enabling these links.

This thesis focuses on improvements to the power amplifier (PA) in particular. The PA is typically the last active (transistor-based) circuit before the antenna in a transmitter. A PA must have gain, be linear so as not to distort the communication signal, and be power-efficient, as it is typically the circuit with the highest power consumption in an analog front-end.

## 1.2 Efficient and Linear Power Amplifier Architectures

A power amplifier (PA) is typically the last active component in a transmit chain before the antenna. A simplified diagram of a PA is shown in Fig.1.2. Its purpose is to amplify a signal to a high enough power level that the signal it transmits can be received with a certain signal-to-noise ratio (SNR) some distance away. What constitutes a "high enough" power level is application dependent; however, due to its placement as the final amplifier, the PA handles the highest power in the analog front end. As a result, its power efficiency plays a large role in the overall front-end's efficiency. The key parameters of a PA are:

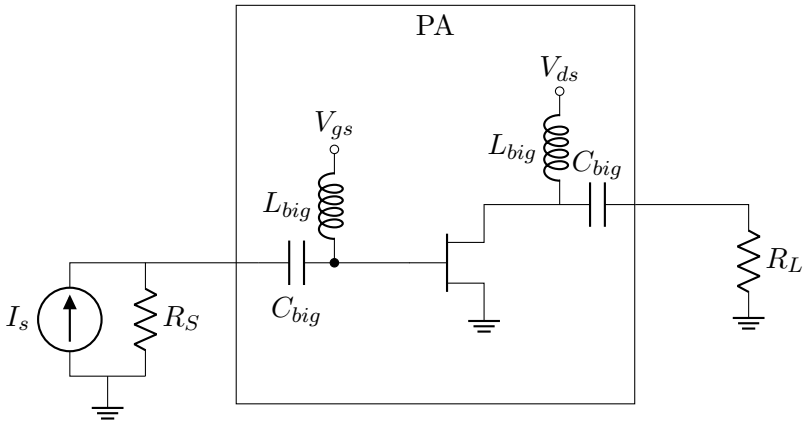



Figure 1.2: Simplistic model of a FET-based power amplifier. A FET is configured in a common-source configuration, with a "bias-tee" at the gate and drain nodes. The bias-tee is made up of a series capacitor ($C_{big}$), which is assumed to be infinitely large to pass all frequencies other than dc, and a shunt inductor ($L_{big}$), which is again assumed to be infinitely large so that only dc may pass through this branch. The inductor can then be connected to a dc supply to bias the amplifier. In this schematic, A current source is placed at the input to drive the PA, and a load resistance ($R_L$) is placed at the output. In general, a PA must also have "matching networks" placed at the source and drain to maximize the power delivered to the transistor and the load, respectively. In this simplistic model, we assume that $R_S, R_L$ are chosen such that the PA is matched for maximum power transfer. *Note that many simple-models, including the load-line analysis used here, assume a resonant structure in the output so that all of the harmonics are shorted; this is not shown for brevity.

$$\mathrm{G} = \frac{\mathrm{P_{out}}}{\mathrm{P_{in}}}, \quad \eta = \frac{\mathrm{P_{out}}}{\mathrm{P_{dc}}}, \quad \mathrm{PAE} = \frac{\mathrm{P_{out}} - \mathrm{P_{in}}}{\mathrm{P_{dc}}}.$$

Where G is the gain of the amplifier and represents how much larger the output signal is compared to the input, and $\mathrm{P_{in}}$, $\mathrm{P_{out}}$ are the RF input and output powers, respectively. Power efficiency can be expressed in several ways, including drain efficiency ($\eta$), the ratio of $\mathrm{P_{out}}$ to the consumed dc power ($\mathrm{P_{dc}}$), and power added efficiency (PAE), which also considers the amount of $\mathrm{P_{in}}$ required. This is useful because it includes both the gain and the power efficiency in one metric. As a rule of thumb, if G > 10dB, then PAE $\simeq \eta$.

Linearity is more difficult to define, and applications usually have specific linearity metrics. We do not define a linearity metric here as a result. Rather, we point out that nonlinear distortion to a signal results from a gain that is not constant, but rather varies as a function of $\mathrm{P_{in}}$. This is

discussed in greater detail in the following subsection.

From the perspective of a circuit designer, it is imperative to have some model for all of the components in a circuit. Most passive components, capacitors, resistors, inductors, and transmission lines, are linear and can be accurately modeled with simple and even closed-form models. The behavior of active devices, such as transistors, diodes, and vacuum tubes, cannot be fully captured by linear models and require additional complexity to represent their behavior. Modeling is a vast and comprehensive field, [27,35,118], and modern nonlinear transistor models are, in general, quite complicated.

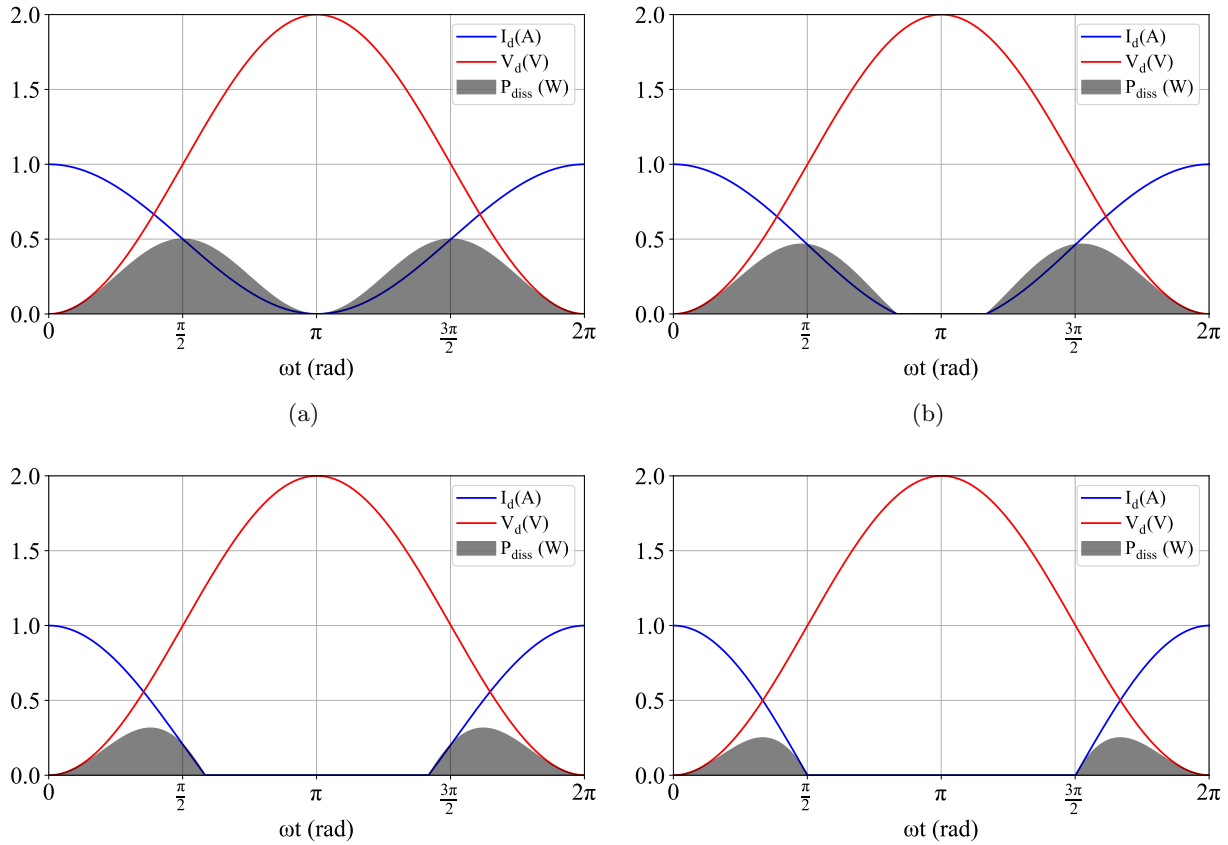



Figure 1.3: Time-domain representations of the drain voltage and current waveforms of an ideal load-line amplifier at maximum $P_{out}$, plotted for (a) 360°, (b) 300°, (c) 210°, and (d) 180° conduction angles. Note that as $\alpha$ is reduced, $P_{diss}$ also reduces, corresponding to an increase in $\eta$. However, the device is conducting for a smaller portion of a period, and therefore, the gain is also reduced.

Instead, we use a highly simplistic model here, the Cripps load-line model [26]. This models the transistor as an ideal voltage-controlled current-source, and we do not include any additional considerations (such as $V_{knee} \neq 0$). This allows us to analyze the performance of a PA quickly at an idealized level.

One of the most important considerations in designing an amplifier is the amplifier's class. The operational class impacts both the design and how to achieve a particular class of operation, as well as the circuit-level response. Here we consider only a few classes of amplifier, termed the "linear classes" classes A, AB, B, and briefly C.

For a FET-based amplifier, the distinction between these classes is made by changing the quiescent dc offset ($V_q$) applied at the gate. In a FET, there is some threshold voltage that must be exceeded for the device to begin conducting current. Here we assume that the threshold is 0 V. To achieve a class-A bias, which is defined as the device always conducting, $V_q$ is set so that the input waveform is sufficiently offset such that the voltage never drops below 0 V. If the input is a 1 V pk-pk sinusoid, for example, $V_q = 0.5$ V so that the waveform is never less than 0 V. This is visualized in Fig.1.3, where (a) shows the drain voltage and current waveforms for class-A.

In general, $V_q \in \Re(-\infty, 0.5]$ where 0.5 indicates a class-A bias, between (0.5,0) represents an AB-bias, 0 is a class-B bias, and $V_q < 0$ is a class-C bias point. $V_q$ is related to the conduction angle ($\alpha$) at maximum current swing (and therefore output power) by:

$$V_q = \frac{\cos(\alpha/2)}{\cos(\alpha/2) - 1}$$

Class B is defined such that the device conducts for exactly half of the cycle, shown in 1.3d. Class-AB is defined as any bias condition conducting more than half the cycle but less than the full cycle, shown in 1.3b,c. Finally, class-C conducts for less than half of a cycle.

One of the large differences between the different amplifier classes is their efficiency. Again, looking toward Fig.1.3, the power dissipated in the transistor is shown as the grey-shaded areas. As the conduction angle is reduced from class-A toward class-B, the efficiency increases from 50 % to

78.5 %. This comes at the expense of gain, with class-B having $\frac{1}{4}$ (-6dB) of the class-A gain. This is exemplified in Fig.1.4, which shows how the gain, $P_{out}$, and $\eta$ change as the conduction angle is varied at the maximum output power for each point. Note that class-C biases have significantly reduced gain and output power. In addition, class-C has a nonlinear gain response across $P_{in}$. As a result, most communications amplifiers are biased in Classes A, AB, or B.

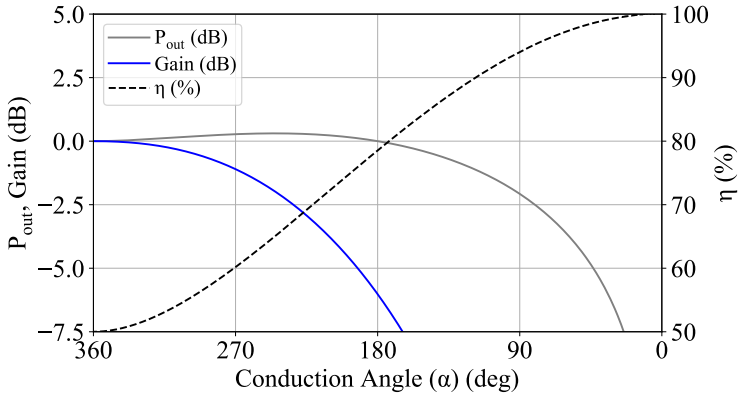



Figure 1.4: Load-line model demonstrating how $\eta$, $P_{out}$, and gain change as a function of conduction angle at peak $P_{out}$. Gain decreases monotonically as $\alpha$ is reduced from the class-A condition, at the limit, when $\alpha = 0°$, at the limit of class-C, both gain and $P_{out}$=0. There is a slight improvement in output power in the AB biases, due to the different $R_{opt}$ in these biases. Finally, $\eta$ increases monotonically, from 50 % in class-A up to 100 % at the limit of class-C.

Another consideration is the semiconductor technology of a transistor. The technologies used for RF and microwave circuits are broad and include Silicon (Si) [94], Gallium Arsenide (GaAs) [28], Indium Phosphide (InP) [16], and Gallium Nitride (GaN) [75]. In this thesis, we focus on GaN PAs and specifically GaN-on-SiC technology nodes. The SiC is a base-layer, termed a "substrate", which provides much of the bulk of the semiconductor. SiC is advantageous due to its relative inexpensiveness and good thermal conductivity, compared to earlier substrates, such as sapphire and even diamond. Recent advances in GaN-on-Si are promising, but are limited in their application due to significantly reduced thermal conductivity.

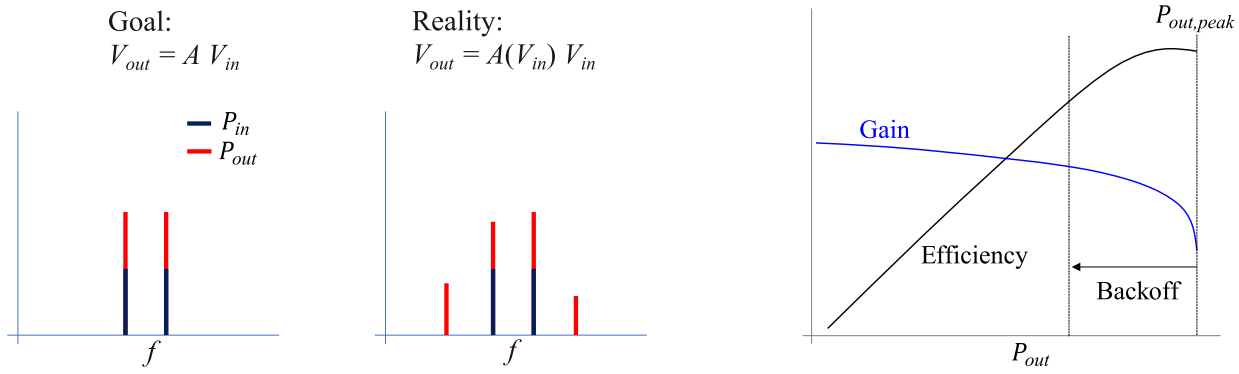



Figure 1.5: Cartoon showing that for a standard AB PA, linearity can be readily achieved by operating the PA far in back off, where gain (only magnitude shown) is flat at the expense of power efficiency. Conversely, the amplifier can be operated at the $P_{sat}$ point and achieve high power efficiency, but this distorts the signal to a flat amplitude, reducing data throughput to near zero. In practice, PAs are typically operated at or near the highest possible point where the linearity still meets the system requirements; this results in both degraded linearity and efficiency as a tradeoff.

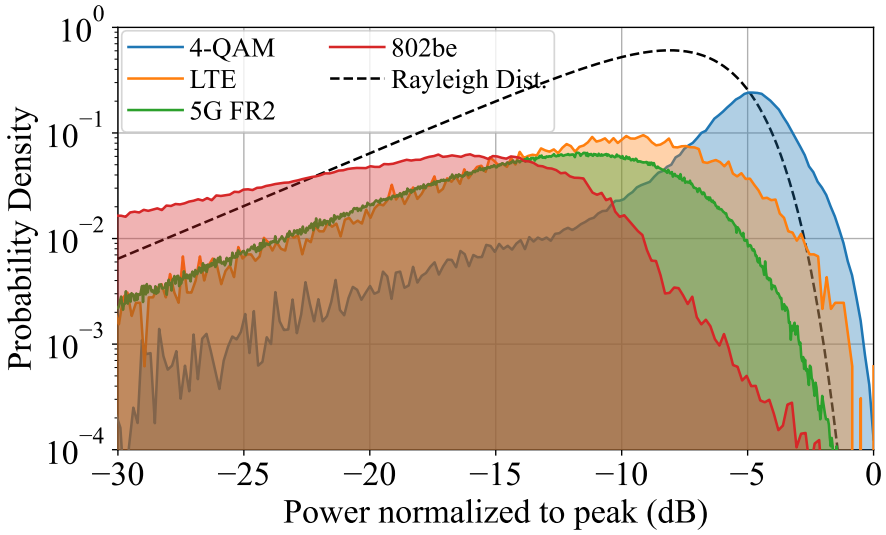



Figure 1.6: Histograms of various wireless communications standards utilizing both amplitude and phase modulation, in order of approximate introduction (4-QAM, LTE, 5G FR2, Wi-Fi 7), demonstrating an increasing PAPR over time to increase throughput. The 3 ratified standards, LTE, 5G, and Wi-Fi 7, are OFDM signals that have an approximately Rayleigh power distribution to maximize data rate. However, these modulations all require very high linearity to maintain allowable BER (bit error rate), which severely degrades PA drain efficiency.

### 1.2.1 Signal Impact on PA Performance

One of the challenges faced in modern wireless communications is that a PA is most power efficient at a single point near its maximum output power ($P_{sat}$). This point also coincides with the most nonlinear operating point of the amplifier, shown in Fig.1.5. As a result, PAs are almost always run backed-off from this peak, which results in increased thermal dissipation (heat) and under-utilization of the transistor. Compounded with this is the increasing use of encoding information in both the phase and **amplitude** of a signal. The result of amplitude modulation is that the magnitude of the signal to be amplified changes rapidly in time. The peak power of a modern signal is now many times the average power. This is exemplified in Fig.1.6, which shows that the peak-to-average-power ratio (PAPR) has steadily increased over time and is now approaching 15 dB with 802be (Wi-Fi 7). As a result, modern amplifiers are operated far in back-off on *average* to ensure faithful amplification of the sparse peaks in the signal.

To understand the magnitude of a signal's impact on performance, as well as the trade-off between linearity and efficiency, it is useful to return to load line analysis. Fig.1.7 illustrates how the efficiency and gain change over input power backoff from maximum drive for (blue) class-A, (orange) class-AB, and (green) class-B. Class-A provides the highest gain but an $\eta < 10\,\%$ at 10 dB of backoff. Conversely, class-B provides the highest backoff efficiency of $> 20\,\%$ but has the lowest gain. The class-AB bias point seems to be at an optimal, closely tracking the class-A gain and the class-B efficiency. However, note that the AB gain is power-dependent and causes signal distortion. Additionally, no bias-point maintains high efficiency in backoff.

Another way to visualize this is shown in Fig.1.8a, where the output power in normalized units is plotted as a heatmap with $V_q$ on the y-axis, and the input power backoff from the full-swing drive level on the x-axis. This plot allows one to analyze how different bias-points and power backoff's affect circuit-level metrics, such as PAE, gain, linearity, etc.

Fig.1.8b, for example, shows how drain efficiency degrades rapidly in all classes as the power is backed off. If, for example, we take the 15 dB PAPR of the Wi-Fi 7 signal, a Class-B amplifier

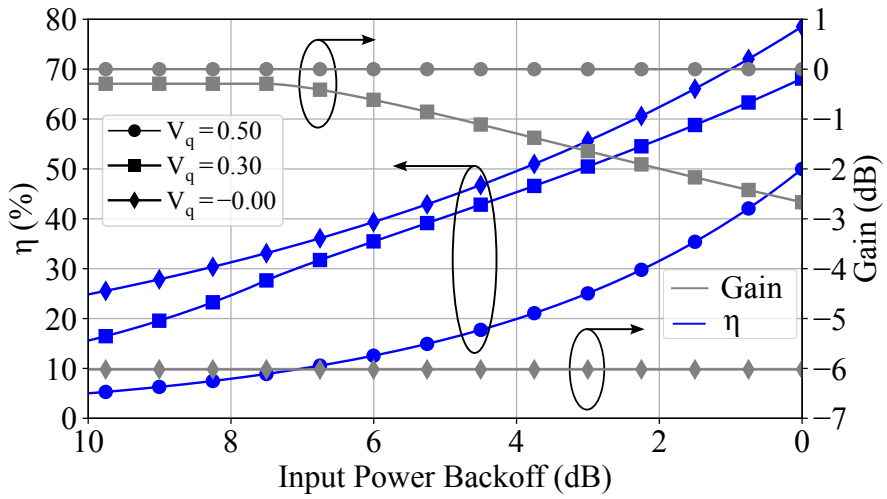



Figure 1.7: This figure demonstrates how the gain and $\eta$ change for a class-A ($V_q = 0.5$), AB ($V_q = 0.3$), and B ($V_q = 0$) bias point over input power backoff. Note that in this figure, $V_q$ and not the conduction angle is specified. This is because $\alpha$ changes dynamically with backoff for a class-AB and C bias condition. Note that the gain with the AB bias is inherently non-linear and changes dynamically with the input power backoff.

yields an average efficiency of $< 30\,\%$, while a Class-A PA has an average efficiency below $< 10\,\%$. This motivates the need for efficiency enhancement techniques to recover efficiency and reduce dc power consumption with communication signals.

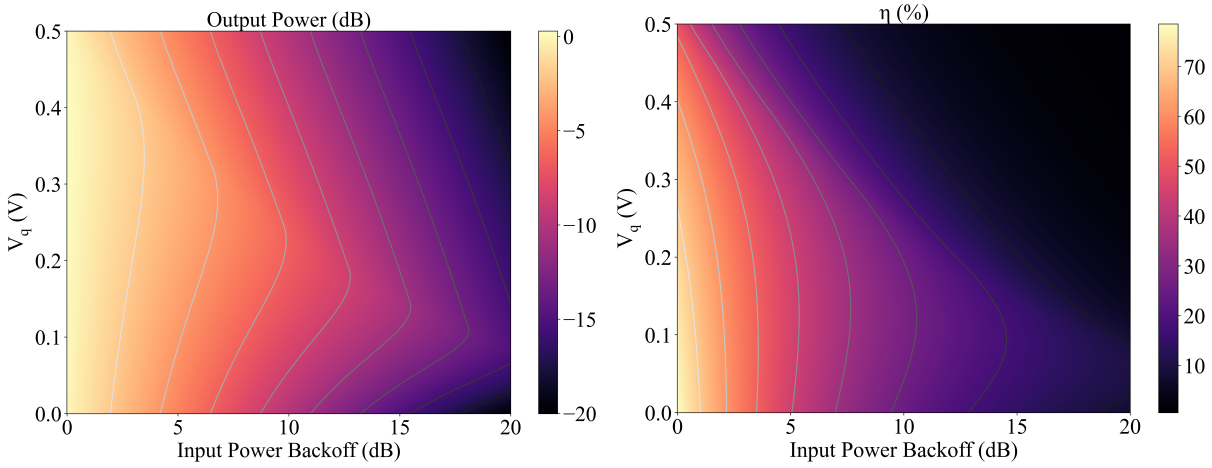



Figure 1.8: Load-line based analysis showing (a) output power and (b) drain efficiency as a function of both $V_q$ and input power back-off.

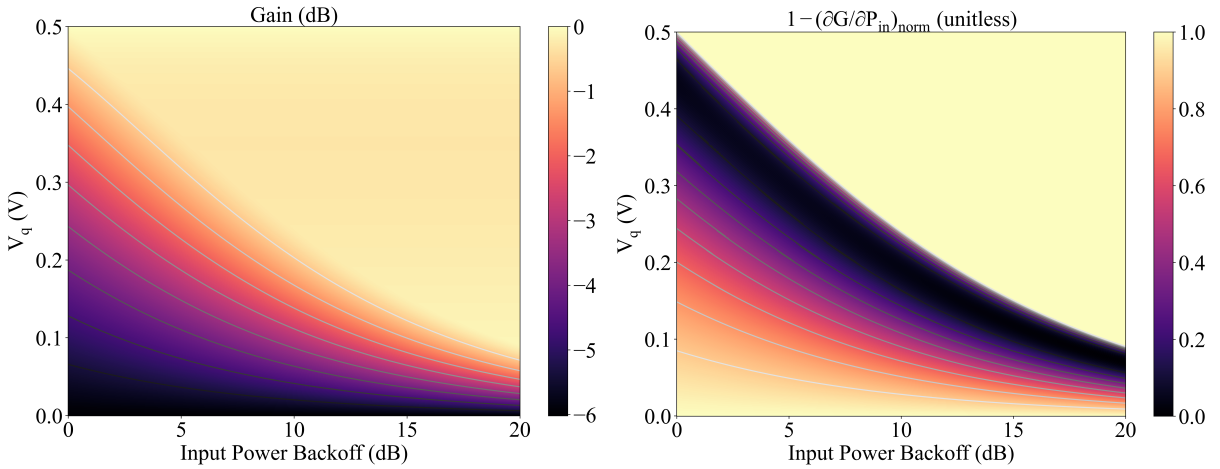



Figure 1.9: Load-line based analysis showing (a) gain and (b) linearity, defined as (1.1), as a function of both $V_q$ and input power back-off. Gain is not constant across back-off due to a changing conduction angle for any of the AB bias conditions. This leads to a distortion of any signal with a time-variant envelope.

Similarly, it is of interest to see how gain changes as a function of drive level and $V_q$. This is shown in 1.9a. A few things are important to note: firstly gain at maximum drive level decreases monotonically as bias is reduced from class-A to a 6 dB reduction in class-B, secondly, for all of the class-AB bias points, the gain is a function of the drive power. This is due to a conduction angle that varies dynamically with the drive level. As a result, the gain is a function of the input drive level, which distorts the signal. To analyze this distortion more closely, 1.9b shows linearity, calculated as:

$$\mathrm{L} = 1 - \left(\frac{\partial \mathrm{G}}{\partial \mathrm{P_{in}}}\right)_{norm} \tag{1.1}$$

which ensures that high values indicate better linearity, and where the normalization is taken to be:

$$x_{norm} = \frac{x - x_{min}}{x_{max} - x_{min}} \tag{1.2}$$

so that the result is between 0 and 1. This demonstrates that no AB bias is free of gain variation. Interestingly, however, in this idealized analysis, deeper class-AB biases (closer to class-B) are more linear than those closer to class-A.

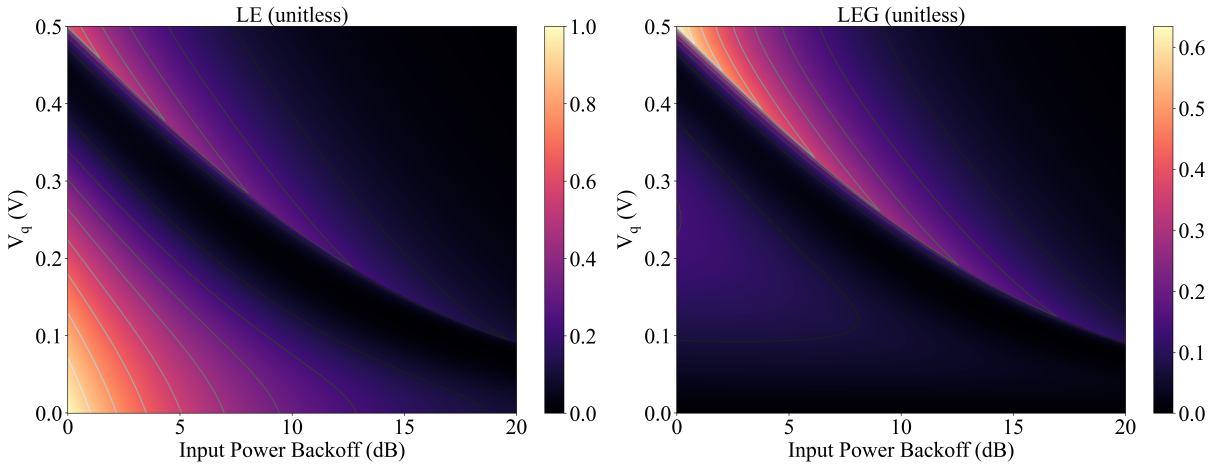



Figure 1.10: Synthetic benchmarks for (a) linearity and efficiency (LE) defined by (1.3) and (b) linearity, efficiency, and gain (LEG), defined by (1.4). No static operating condition yields high performance far into back-off.

Now, we have plots for linearity and efficiency, and it is of interest to see their product, the regions where a PA may be both linear and efficient. Fig.1.10a shows the product of linearity and efficiency:

$$\text{LE} = \text{L} \cdot \eta_{norm} \tag{1.3}$$

where each is normalized using (1.2). There is a small region near class-B which seems to satisfy our requirement for simultaneous linearity and efficiency; however, this does not extend beyond a few dB in backoff, which rules it out as a perfect solution for modern high PAPR signals. Additionally, Fig.1.10b adds gain so that the colormap is calculated using:

$$\text{LEG} = \text{L} \cdot \eta_{norm} \cdot G_{norm} \tag{1.4}$$

where the normalization is again calculated using (1.2). From this figure, it is clear that no *static* load/bias condition readily satisfies the opposing requirements of simultaneous linearity, efficiency, and gain.

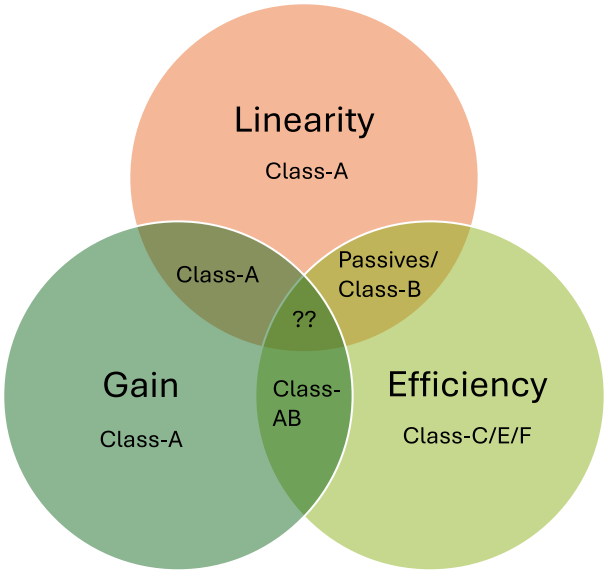



Figure 1.11: Venn diagram showing the three key communications PA metrics: linearity, efficiency, and gain. Any two can be readily simultaneously achieved. However, no known current PA class or efficiency/linearity enhancement technique allows for all three to be achieved without significant compromise.

The challenge of linearly amplifying a signal while also minimizing power consumption and heat is a challenge that has existed for nearly 100 years, since the widespread adoption of broadcast radio stations. To understand why this challenge is still an active area of academic research, while commercial and defense systems are actively being fielded with increasingly complicated signals, it is helpful to look to Fig.1.11. This figure shows a Venn diagram of the three key parameters that a communications amplifier must maximize: gain, linearity, and power efficiency. There are well-known solutions to achieve two of the three, but nothing that achieves all three simultaneously. A few points to note:

(1) An ideal class-B might operate near the center of this diagram as it would be perfectly linear and highly efficient; however, even an ideal class-B PA has 6 dB lower gain than class-A, and practical implementations are nonlinear.

(2) Most *linearity* and *efficiency* enhancement techniques have been demonstrated, which minimally impact the other; however, a degradation in gain is nearly always seen. Gain is the

only reason that a PA is necessary, with efficiency and linearity being side effects that must be managed. Therefore, it is important to be cognizant of this implicit gain degradation.

(3) In practice, a class-AB PA is nearly always used as it provides dramatic efficiency improvement compared to class A, with less gain reduction than the 6 dB of class-B. Linearity is handled in most modern radios by digitally predistorting (DPD) the signal so that it counteracts the nonlinearity of the PA. This technique is highly effective, but comes at the expense of increased power consumption in the digital domain and reduced gain.

(4) RF carrier frequencies are increasing to allow for wider instantaneous bandwidths. The gain, and therefore the output power of a transistor, decreases as a function of frequency. Additionally, the loss in matching networks, cabling, and antennas' increases with frequency. This results in increased design complexity and performance degradation at high frequencies.

Another way to view this tradeoff is to think about the link budget of a radio link:

$$P_r = P_t G_t G_r \left(\frac{\lambda_0}{4\pi d}\right)^2$$

Where $P_r$ and $P_t$ are the received and transmitted powers, respectively. $G_r$ and $G_t$ are the gains of the respective receiving and transmitting antennas. Finally, $\lambda_0$ is the wavelength of the RF carrier in free-space, and d is the distance between the antennas. This demonstrates that $P_r$ decreases with the square of d. If we assume the best case scenario, an ideal lossless channel with no multi-path or other effects, we can therefore also state that the signal-to-noise ratio (SNR) also decreases with the square of d. This SNR must be above some value to ensure reliable reception of the transmitted signal. If the SNR is sufficiently degraded, an advanced wireless link may reduce the complexity of the modulation type, restoring the radio link at the expense of throughput. Otherwise, the information in the signal is lost. SNR is relevant to the discussion because the distortion from nonlinear elements can be analyzed in a similar way to thermal noise [24, 43, 105]. As a result, from (1.5), by increasing the transmitted power ($P_t$), we can increase the $P_r$, and therefore the SNR.

However, if by increasing $P_t$, the nonlinear distortion is also increased, the SNR at the receiver may actually degrade because the SNR of the transmitted signal is itself degraded.

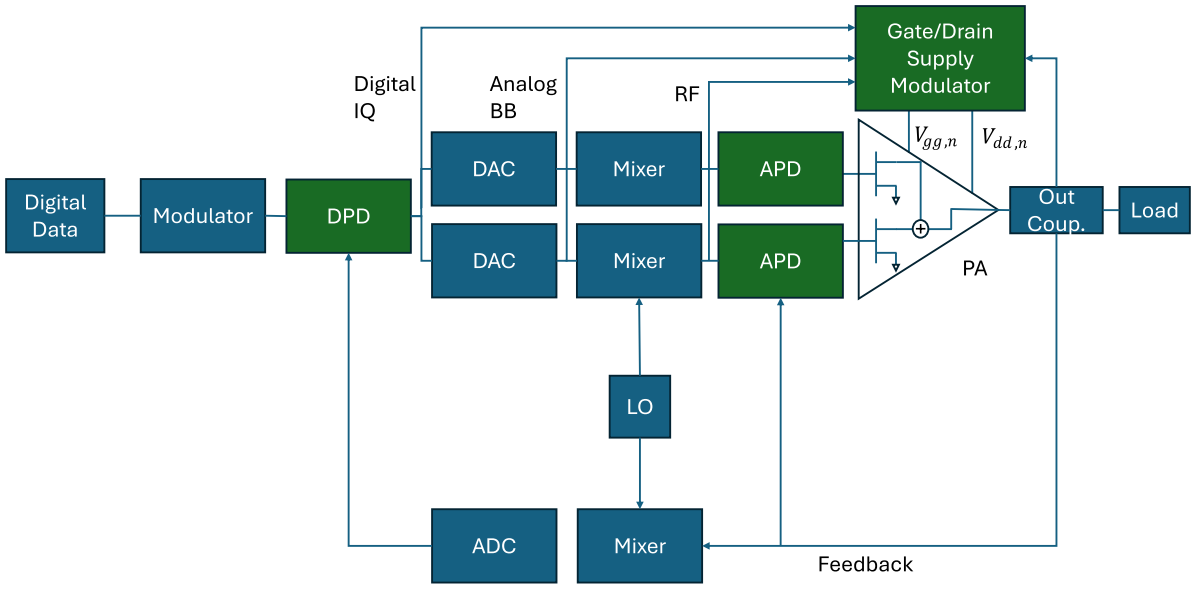



Figure 1.12: A generalized diagram for a transmitter with feedback demonstrating the PA and necessary drive circuitry, including common PA enhancement techniques, including gate/drain modulation, load-modulation, digital and analog predistortion, and a dual-RF drive architecture. The load is nominally an antenna, but may include additional circuitry, such as circulators/isolators, antenna tuners, gain control, and filters. Note that this diagram is not comprehensive; feedforward architectures and analog phased arrays are common applications that deviate from this general architecture.

A generic transmitter for communications is shown in Fig.1.12. Although not comprehensive of all PA and transmitter architectures, the figure is generic to demonstrate a system that contains linearization in the digital (DPD) or analog (analog predistortion (APD), gate modulation) domains. Additionally, efficiency enhancement may be achieved in this diagram through either drain modulation or some load modulation mechanism represented by the dual drive PA architecture and generic summing at the drain node. Common to all of these is some feedback mechanism. The coupler at the output of the figure taps off some portion of the output signal. This can either be compared in the analog domain, shown with the path from the coupler to the gate/drain modulator, or in the digital baseband domain. This is represented by the additional mixer and analog-to-digital

converter (ADC) in the figure. This graphic intends to convey that the PA is one component out of many in a transmission chain, yet many of those components exist to handle the non-idealities of the PA. Additionally, many different approaches can be taken to design a transmitter to satisfy overall system specifications. The two main effects that must be accounted for and driven by the PA are detailed below.

### 1.2.2 Efficiency Enhancement Techniques

Efficiency enhancement techniques for communications applications can be grouped broadly into three main categories: drain-modulation, load-modulation, and harmonic injection. This should not be taken to be a comprehensive list. Architectures such as polar amplifiers have received renewed interest [71, 72]. Additionally, the categories are not always well defined and span a broad range of architectures. Finally, some techniques used at lower frequencies and for CW/RADAR applications are not included, but may find future applicability in the communications space [55, 91, 92, 104].

Active load modulation refers to a variety of techniques that dynamically change the load impedance seen by the transistor as a function of the input signal. Typically, this is done by using two or more devices with a non-isolating combiner at the output. The most well-known of these types of amplifier is the Doherty amplifier, which can maintain high efficiency across 6 dB of input power backoff [32]. This amplifier has become extremely popular in literature, and numerous extensions to the classical Doherty amplifier have been presented. A more recent load modulation architecture is the load-modulated balanced amplifier (LMBA). This topology has numerous potential advantages over the Doherty configuration. Chiefly, the LMBA has demonstrated efficiency much further in backoff and can have much wider bandwidths due to utilizing broadband couplers as the output combiner [66, 102, 113].

Another method, which we include under load-modulation, is outphasing. This technique is notable since it allows for the amplification stages to be generally nonlinear, while still achieving linear amplification. This is termed linear amplification with nonlinear components (LINC) [25].

Note that LINC is a more general term and includes architectures beyond outphasing, including those not intended for efficiency enhancement.

Technically, outphasing refers to a broader set of topologies, some of which do not incorporate load-modulation [8]. As a brief overview, outphasing PAs have two-parallel active devices that are run in constant amplitude operation with some phase difference between the two branches. At the output, the signals are recombined, and the output power of the signal is determined by how the signals recombine.

Next, harmonic injection refers to the concept of explicitly injecting harmonic content into the drain of a transistor to shape the voltage/current waveforms and reduce dissipated power [29]. This bears similarity to, e.g., Class-F PAs, with the chief difference being that the PA can itself be operating in a linear region with little harmonic content being generated. The primary difficulty in these architectures is to efficiently generate the harmonic content. Additionally, a diplexer structure is necessary at the output to inject the harmonic content at the drain of the device, which adds complexity and loss.

Finally, drain modulation is a technique where the drain voltage of a field-effect transistor (FET) is dynamically varied as a function of the instantaneous input voltage magnitude (this technique has been demonstrated with other active devices, but is only be discussed within the context of FETs, e.g., drain voltage) [5, 78, 85, 88].

It is interesting to note that many of these techniques have a common similarity; all inject an additional excitation into the drain of the PA. While the frequencies at which these techniques operate differ—drain modulation acting at baseband, load modulation at the fundamental frequency $f_0$, and harmonic injection at integer multiples $Nf_0$—they share a common underlying objective. Although the mechanisms used to achieve active injection in each case are distinct, this allows for a common characterization framework, provided that the injection circuit is treated as a black box.

### 1.2.3 Linearity Enhancement Techniques

Linearity enhancement techniques are more ambiguously categorized than efficiency enhancement techniques; therefore, we broadly categorize them into analog domain and digital domain solutions. Analog domain approaches may be digitally controlled, but any method whose method of linearization takes place in the analog domain (after the digital-to-analog converter (DAC)) are considered analog.

Digital linearization here refers chiefly to digital pre-distortion (DPD). DPD is a highly effective method that has been one of the key technologies enabling the modern wireless communications boom [45]. DPD uses a model of the PA nonlinearity and applies the inverse of that response to the input signal. This adds a step that must be performed after the signal is modulated and before it goes to the DAC.

The major disadvantage of DPD is this additional processing step, which adds complexity to the modem and increases its dc power consumption. There exists a tradeoff between the complexity of the model of the PA used and the accuracy of the linearization. A more complete model offers better linearization, but requires more costly hardware and greater power consumption as a result. Additionally, the hardware complexity and power consumption also scale with the instantaneous bandwidth of the signal. For emerging applications, DPD faces some significant challenges:

(1) Fully digital phased arrays are becoming the norm for many new systems. This results in many smaller PAs, each of which must be individually linearized. Each PA only contributes a small amount to the overall RF power, but each consumes the same amount of power for modulation. Thus, there exists a scaling problem for DPD. Compounding this is that, in general, the PA is loaded by the rest of the array. Thus, the nonlinearity is also a function of the operating conditions of the rest of the array, adding another factor for the DPD algorithm to consider.

(2) The instantaneous bandwidth of the signal is strongly correlated with the power consumption of DPD; broader bandwidth signals require a faster digital processor to perform the

transformation to the signal, which consumes more power.

(3) There exists in DPD a tradeoff between the accuracy of the model and the dc power consumed. More advanced DPD models with more terms, or including memory effects (e.g., Volterra), require more complicated digital hardware, which consumes more power.

(4) Satellite communications appear to be the next frontier of mobile communications. Due to the large physical-length of the links, as well as the enormous line-of-sight distances which are feasible between satellites, "bent-pipe" repeaters have traditionally been used in satellite communications. These repeaters receive a signal from one node and then amplify and retransmit it with no demodulation step. This is a simple and efficient method to boost the SNR of a link, but, because there is no demodulation, it cannot be used with DPD.

(5) Some reduction in gain is inherent to DPD.

This is not meant to dismiss DPD; it is almost certainly the most ubiquitous linearization technique used today. Rather, it is to point out that DPD is not infallible, and there is merit in researching other methods for PA linearization.

Analog linearization is a field where numerous topologies have arisen. Here we introduce only two: analog pre-disistortion and gate-modulation.

In most analog approaches, linearization is performed using analog predistorters (APDs), which apply a diode or transistor-based nonlinearity before the input of the PA to cancel its distortion [50]. This method can offer high IBW performance without digital control but typically introduces additional loss. Recently, APD has been applied to include wideband signal handling [13], in Doherty PAs [87], in millimeter-wave traveling wave tube amplifiers (TWTAs) [30], and for E-band amplifiers [42]. However, APDs remain lossy and difficult to tune across varying operating conditions, which limits widespread adoption. Analog linearization via baseband impedance modulation has also been explored [7, 98], along with other techniques like feedforward and derivative superposition [4, 53].

Early demonstrations of gate bias tracking for linearization were reported in [46], which demonstrated up to 10 dB of third-order intermodulation distortion ($IMD_3$) improvement with a 1 MHz two-tone for a GaAs metal–semiconductor field-effect transistor (MESFET) amplifier using a fully analog gate modulator. Subsequently, digitally controlled gate modulators [23] achieved up to 8 dB of adjacent channel power ratio (ACPR) improvement with a 1.22 MHz code division multiple access (CDMA) signal. [44] demonstrated up to 7.7 dB of ACPR improvement and 4.9 pp error vector magnitude (EVM) improvement with a 1 MHz 16 quadrature amplitude modulation (QAM) signal. In [73], 6 dB of ACPR improvement is achieved for a 2 MHz 16 QAM signal. In [58], independent gate trajectories for a 2-stage PA were investigated and achieved up to 4.7 dB of normalized mean square error improvement, and 7.9 dB of ACPR improvement with a 5 MHz long-term evolution (LTE) signal. Recently, a fully integrated PA and gate tracking system was shown at W-band with a theoretical 3 dB baseband bandwidth of 5.5 GHz; however, no measured modulated results were demonstrated [51].

## 1.3 Thesis Outline

The work presented in this thesis outlines methodologies of PA design for different power levels, communications signals, and output power requirements.

**Chapter 2:** Supply Modulation is a well-known and proven technique to improve the power efficiency of a PA. In short, the drain supply voltage to a PA can be dynamically varied proportionally with the instantaneous amplitude of the input signal to maintain the PA at a more constant level of saturation. In practice, achieving a practical implementation of this requires careful design of the circuit, which provides the dynamic drain voltage signal. In this chapter, firstly, a technique to improve efficiency under a constrained difference between the maximum and minimum voltage levels is presented. The second part demonstrates the characterization of a highly efficient dynamic supply architecture.

**Chapter 3:** Gate modulation is another well-known technique that bears similarity to drain modulation and dynamically varies the gate voltage to improve linearity. This chapter presents

a GaN PA and a GaAs circuit with a coupler and envelope detector for wideband analog gate modulation. The circuits are integrated with a biasing/baseband conditioning PCB, and measured results demonstrate greater than 17 dB of $IMD_3$ suppression at 100 MHz and $IMD_3$ suppression above 4 dB up to 1 GHz of instantaneous bandwidth.

**Chapter 4:** This chapter investigates the impact of modulation on transistor performance. In particular, how the optimal impedance matching points for e.g., PAE, gain, and linearity, change as a function of the signal excitation. The applicability of multi-tone signals as a surrogate for modern communications signals is investigated.

**Chapter 5:** This chapter introduces a novel hardware-in-the-loop circuit analysis technique, termed "network emulation". In this technique, a nonlinear model of the device is replaced with physical measurements of the DUT. This has broad applicability from applications where a model is not available or validated, to extreme environmental conditions. Because the network emulation method shared hardware requirements with wideband active load pull, the technique scales well to design for wideband modulated signal conditions. A PA is designed, and measurements of the PA are compared against emulation, with excellent agreement.

**Chapter 6:** Building on the network emulation concept of the previous chapter, here we present a method to achieve wideband arbitrary load modulation (WALM) on a physical device. The load modulator can be treated as a black box in this approach, which allows an additional degree of freedom compared to traditional load-modulated design flows. A main stage of a Doherty is emulated, with an arbitrary load modulator providing the waveforms necessary to achieve standard Doherty operation. Practical considerations, including bandwidth, dynamic range, and noise, are considered.

**Chapter 7:** A summary of the thesis is presented within. Additionally, opportunities for future work are discussed.

# Chapter 2

# Supply Modulation for Efficiency Enhancement

## 2.1 Introduction

Supply modulation is a well-known and demonstrated method for improving the efficiency of power amplifiers operating with time-varying envelopes. One of the key benefits of supply modulation is that, ideally, the average efficiency with a modulated signal can be improved while maintaining linearity and gain. Thus, in principle, we can readily achieve our goal of simultaneous linearity, efficiency, and gain from an amplifier. In practice, supply modulation negatively impacts linearity and gain, compared to an amplifier with a static supply, while falling short of recovering efficiency to constant-envelope conditions. Nevertheless, supply modulation has found adoption in commercial and defense applications, as seen in Fig.2.1.

For a FET-based amplifier, supply modulation refers to a technique where the drain voltage supplied to the amplifier is varied synchronously with the instantaneous envelope of the input signal. When the envelope peaks, the drain voltage is brought to its maximal value, and when the envelope is at a minimum, the drain voltage is similarly reduced to a minimum value. This allows the amplifier to operate in a constant state of compression independent of the input signal.

One of the major practical limitations of supply modulation is the circuit that enables the dynamic drain voltage, the supply modulator. If this circuit is realized as a linear envelope amplifier, then the dynamic drain signal exactly follows the envelope of the input signal and the PA efficiency is maximized, while minimally impacting linearity and gain. However, the overall system efficiency will be significantly lower than without supply modulation, due to the power dissipated

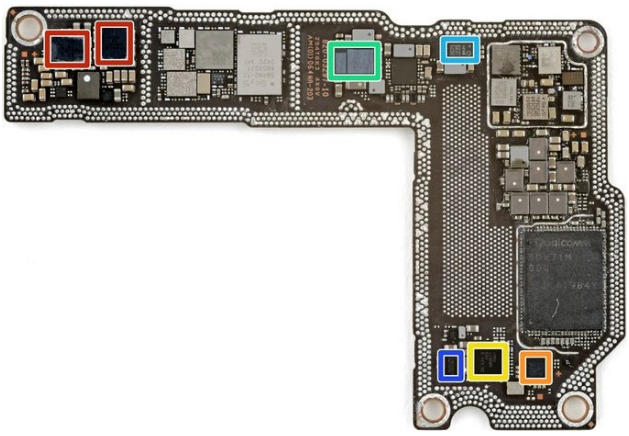


Figure 2.1: Photograph of the RF board of a smartphone released in 2024, from [116]. The top right green and teal chips are envelope tracking supplies from Qualcomm and Qorvo, respectively. Very limited public information is available about these ICs; however, the Qualcomm supply has a claimed 100 MHz bandwidth and is intended for 5G FR1 applications [115].

in the envelope amplifier, which is operating in a linear class. Therefore, most practical envelope modulators are realized with efficient switching architectures and follow a discretization of the envelope. Additional practical limitations, such as envelope bandwidth reduction and current collapse within the device near the knee-voltage must also be considered when creating a supply modulation trajectory [14, 33].

In this section, two contributions to the field of supply modulation are shown. The first is a technique to maximize the relative voltage swing for range-limited supply modulators. The second is the supply modulation of a $C$-band hybrid power amplifier using a highly efficient flying-capacitor supply modulator, similar to the supply modulator architecture first demonstrated in [15].

## 2.2 Efficiency Improvement through Periphery Optimization

We introduce an approach aimed at further optimizing the efficiency of discrete drain supply modulated Gallium Nitride (GaN) PAs through transistor sizing. By employing larger periphery transistors, we obtain equivalent output power at lower drain voltages. This capability facilitates a wider relative swing between the highest and lowest dynamic drain voltages, consequently leading

to improved back-off efficiency. To validate this methodology, we design and measure two 10 GHz Monolithic Microwave Integrated Circuit (MMIC) PAs, with one employing a larger periphery transistor. Experimental results demonstrate a 5 percentage point (pp) enhancement in average Power Added Efficiency (PAE) when amplifying a 67.5 MHz 64-QAM signal using the larger device. Moreover, the measured average gain exhibits a significant improvement of 4 dB with the larger periphery amplifier, while maintaining an unaffected Error Vector Magnitude (EVM) at 5 %.

The efficiency and linearity of microwave transmitters for communications and radar are dominated by the power amplifier (PA). The transistors in the final stage of the PA are faced with increasingly difficult requirements as modulation standards become more demanding in terms of bandwidth, peak-to-average power ratio (PAPR), and linearity. Transmitter architectures used to efficiently amplify high PAPR signals include the Doherty, outphasing (Chireix), and load-modulated balanced PAs [9, 52, 102]. Supply modulation, often referred to as envelope tracking, is a carrier-frequency agnostic technique for efficiency enhancement that has been demonstrated for high PAPR signals [114], multiple simultaneous signals [34], wide RF bandwidth [81], and signal bandwidths up to 250 MHz [57]. For a high-efficiency PA, the instantaneous bandwidth of a signal that can be efficiently amplified with a supply-modulated (SM) PA is limited by the large-signal bandwidth of the SM, which is described by its slew rate.

Discrete level supply modulators (DSMs) typically have a fixed difference, $\Delta V$, between the highest and lowest voltage levels [74, 82]. This limits how far the PA can be backed off in output power ($P_{out}$) while maintaining high efficiency. The highest achievable output power is dictated by the maximum drain supply voltage, $V_{dd,max}$. A larger periphery transistor requires a lower $V_{dd,max}$ for the same average $P_{out}$ which allows for more relative variation, $\Delta V/V_{dd,max}$ for a fixed $\Delta V$.

DSM architectures that place no practical limit on $\Delta V$, still benefit, as a smaller $\Delta V$ gives more voltage resolution. A smaller $\Delta V$ limits the linearity degradation due to gain and phase variation with $V_{ds}$ [59]. Two 10-GHz GaN MMIC PAs, shown in Fig. 2.2, are designed to demonstrate this method.

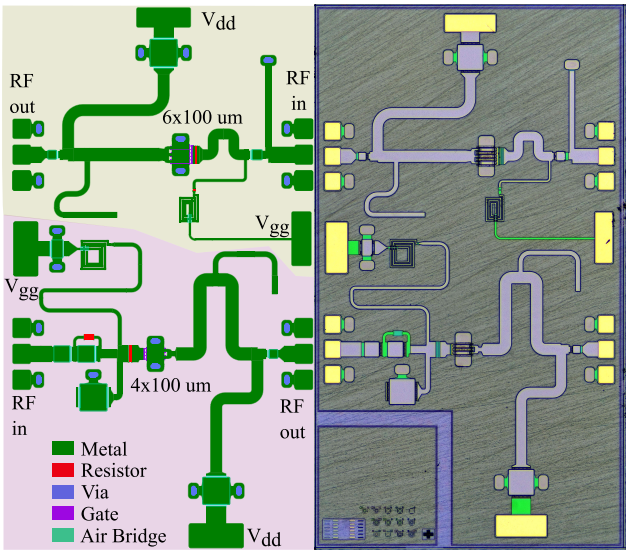



Figure 2.2: Schematic and photograph of two single-stage MMIC PAs with different device peripheries, designed to be operated with drain supply modulation and to achieve the same output power. MMIC dimensions are 1.8x3.2 mm.

### 2.2.1 Power Amplifier Design

To evaluate how device size impacts back-off efficiency, we begin with harmonic balance load-pull simulations in the WIN Semiconductor NP15 GaN-on-SiC MMIC process. This is advantageous because of the wide variety of available devices. We load-pull a reference device and record the maximum Power Added Efficiency (PAE) at the maximum drain voltage, as well as the $P_{out}$ at which this occurs. For this process, a reference device size of $4\times100$ µm and the highest recommended drain voltage, $V_{dd,max}$=28 V are chosen. Additionally, the maximum PAE with the $V_{ds}$=$V_{dd,max}$−10 V when $P_{out}$ is backed-off by 6 dB is recorded. Once these reference values are obtained, we load-pull two larger periphery devices at lower drain voltage ranges to determine the optimal over-sizing ratio for a 6 dB PAPR signal. The simulated load-pull is performed using ideal load tuners and terminating the $2^{nd}$ and $3^{rd}$ harmonics at the gate and drain of the devices to maximize PAE. In this analysis, the periphery scaling is achieved by changing the number of fingers of the FET only. An additional trade-space is available by changing the gate width of the FET.

The results of this analysis can be seen in Table 2.1. Maximum PAE values from load-pull

simulations using the foundry nonlinear model are shown, for an output power of 33.5 dBm and a total drain voltage range of 10 V. The table additionally shows PAE at 27.5 dBm output power (6-dB backed-off). Different peak and back-off drain voltages are used to maintain a peak output power of 33.5 dBm and a maximum voltage range of 10 V. The 6×100 µm device maintains PAE > 70 % in back-off, a 12 pp increase compared to the reference 4×100 µm. The 8×100 µm device is too large, and the required drain voltages operate the device too close to the knee, resulting in degraded efficiency both at peak and back off. Furthermore, gain usually drops at lower drain voltages, which decreases PAE. Therefore, this technique is intended for improving back-off efficiency at frequencies where the process enables sufficient gain and output power.

After determining that the reference and oversized peripheries are 400 and 600 µm, respectively, two single-stage PAs are designed with a center frequency of 10 GHz to demonstrate the additional efficiency enhancement with a larger device periphery. The matching networks for the reference PA are designed first and then adapted to the oversized amplifier. This is done to minimize the effect that matching network topology has on the performance difference between the two amplifiers. The target load impedances are found by load-pull simulations to maximize the PAE at an output power that is 6 dB below the maximum, at the lowest intended $V_{ds}$.

Table 2.1: Maximum simulated PAE values for different peripheries

| Device | Voltage Range | PAE at 33.5 dBm | PAE at 27.5 dBm |
|---|---|---|---|
| 4×100 µm | 18-28 V | 74.0 % (28 V) | 58 % (18 V) |
| 6×100 µm | 12-22 V | 72.5 % (22 V) | 70 % (12 V) |
| 8×100 µm | 9-19 V | 68.5 % (19 V) | 64 % (9 V) |

### 2.2.2 Simulated Dynamic Performance

The two amplifiers have comparable simulated performance, as seen in Fig. 2.4, and this provides a reasonable point of comparison to evaluate the impact of device sizing on PA performance. Both amplifiers maintain a PAE above 50 % across their respective drain voltage ranges. Both amplifiers also achieve a $P_{out,max}$ of approximately 32 dBm. However, the larger periphery amplifier

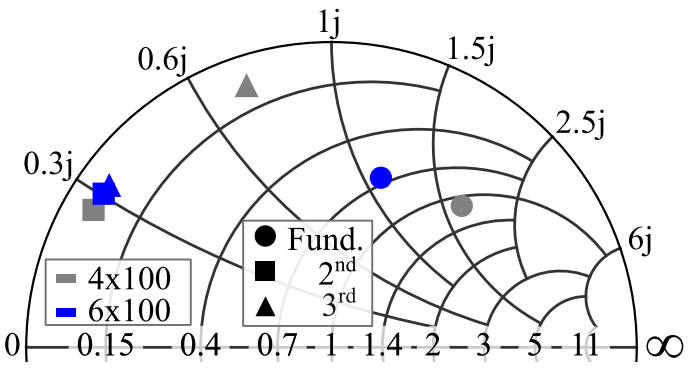



Figure 2.3: Simulated maximum PAE $\Gamma_L$s for the different peripheries at 10 GHz. The devices are terminated up to the third harmonic with the impedances shown to obtain the results in Table 2.1.

maintains efficiency above 50 % backed-off to 26.4 dBm, compared to 27.6 dBm for the reference PA.

To estimate how well the PAs will perform under dynamic supply modulated conditions, a custom envelope simulator, written in MATLAB, is used. These envelope simulations use the simulated CW complex gain and $P_{dc}$ of the PA, as functions of both $V_{ds}$ and $P_{in}$, to estimate the output response of the PA. This simulator is validated in detail in [79]. A 64-QAM test signal with a PAPR of 7 dB is used to evaluate the dynamic performance of both PAs. Both PAs are simulated with ideal dynamic supplies with 4 levels linearly spaced from 18–28 V for the reference PA and 12–22 V for the larger periphery amplifier. A look-up table (LUT), referred to as a shaping function, is generated from CW simulations of PAE and gain. This relates the instantaneous input power to a drain voltage to achieve some desired performance from the PA, which in this case maximizes $\overline{\text{PAE}}$. The simulated discrete drain modulated performance for both amplifiers is shown in Fig. 2.5. The PAE, gain, and error vector magnitude (EVM), are all improved in nearly all cases for the larger device. As seen in the PAE and gain curves over $P_{out}$, the PA with the 600 µm device has intrinsically higher gain. The cause of the linearity improvement is less obvious and is due to lower variation in the AM-PM response of the larger-periphery amplifier. The improvement in PAE, however, can only be attributed to the device sizing and the associated improved back-off efficiency. The maximum improvement in PAE is about 5 pp at $\overline{P_{out}} = 25$ dBm. This is a reasonable operating

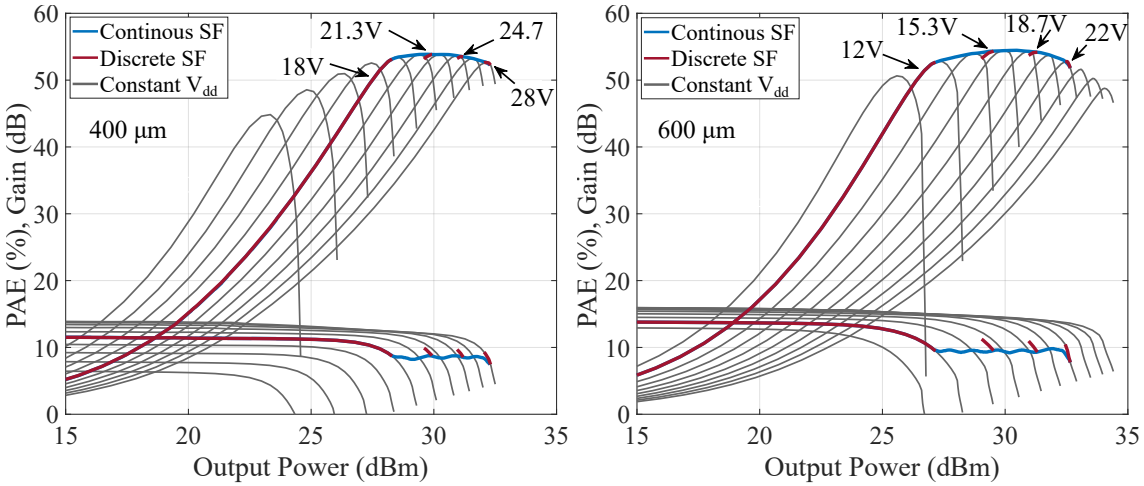



Figure 2.4: Simulated gain and PAE curves over $P_{out}$ at 10 GHz for the (a) 400 µm amplifier, and (b) the 600 µm amplifier.

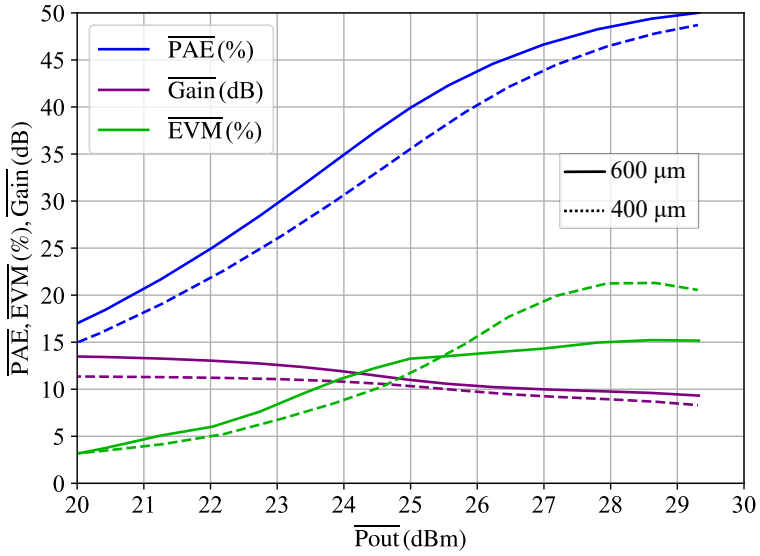
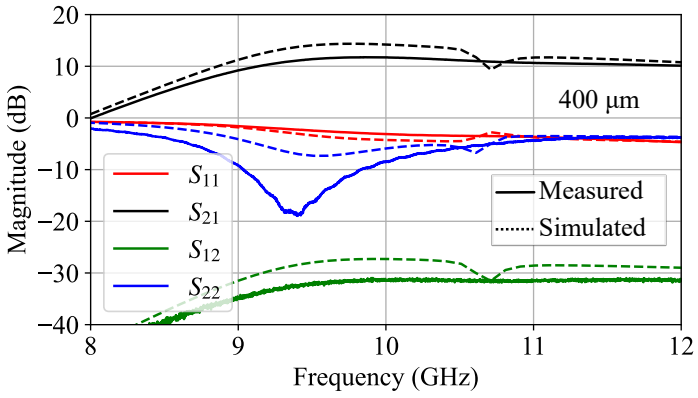



Figure 2.5: Simulated dynamic performance obtained from a MATLAB-based envelope simulator under ideal discrete 4-level supply modulation at 10 GHz.

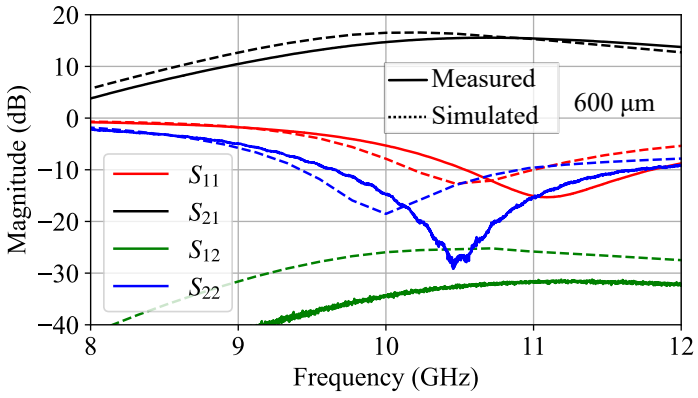
point for both amplifiers because the peak power is near their peak $P_{out}$ of 32 dBm. While the $\overline{\text{EVM}}$ is quite high at 12 %, and 14 % for the larger and reference PAs, respectively, this could be significantly reduced using digital pre-distortion (DPD) or using a flat-gain shaping function.

### 2.2.3 Measured Performance

Static characterization in CW is performed for each drain supply voltage level, while dynamic characterization is performed with two 64-QAM signals.




(a)




(b)

Figure 2.6: Simulated and measured S-parameters for (a) the 400 µm amplifier and (b) the 600 µm amplifier.

#### 2.2.3.1 Static Measurements

To evaluate the performance of the two MMIC amplifiers, we begin by measuring the small-signal performance using a VNA and a probe station. The small signal response for both PAs compared to simulation can be seen in Fig. 2.6 and demonstrates reasonable agreement with the model. Both PAs demonstrate $> 10$ dB of small signal gain and a return loss higher than 3 dB at 10 GHz.

The large-signal performance across frequency, input power ($P_{in}$), and $V_{ds}$ is measured with the VNA configured with an external test set and with an additional absolute power calibration using a power meter at port 1. This setup allows us to obtain both large-signal phase and magnitude data, which is essential for building the shaping functions for supply modulation. While not shown for brevity, the reference PA shows significant deviation from simulation at 10 GHz in large-signal, and we instead choose to do our analysis at 9.7 GHz, where both PAs have high efficiency and agree well with simulation. The measured performance across output power for both PAs across their intended drain voltages can be seen in Fig. 2.7. The PA with the larger device periphery demonstrates significantly better performance and much closer agreement to simulation compared to the reference device. It is unclear why the oversized amplifier's measured performance agrees more closely with simulations since both amplifiers are designed in the same process and are co-located on the same die.

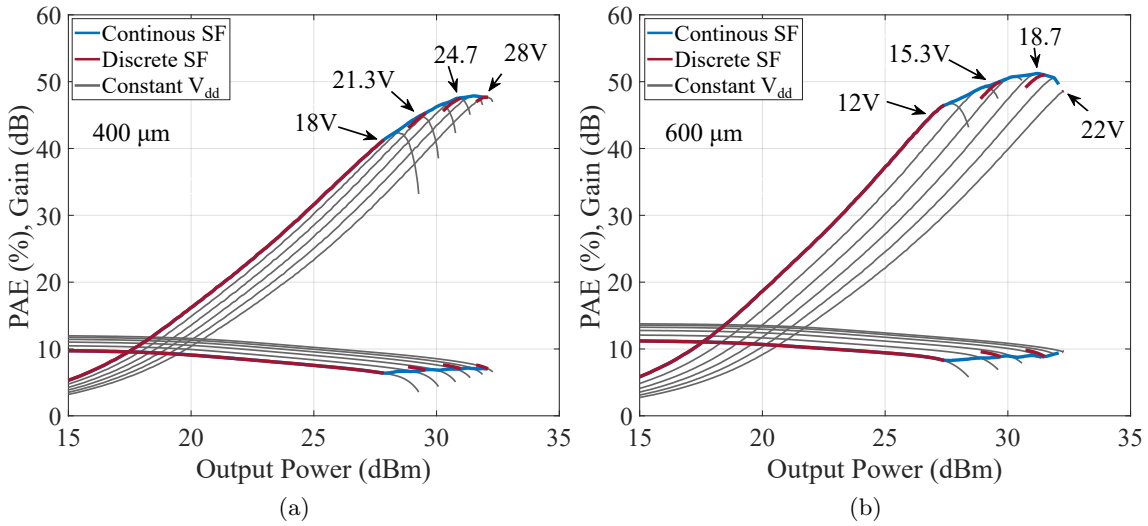


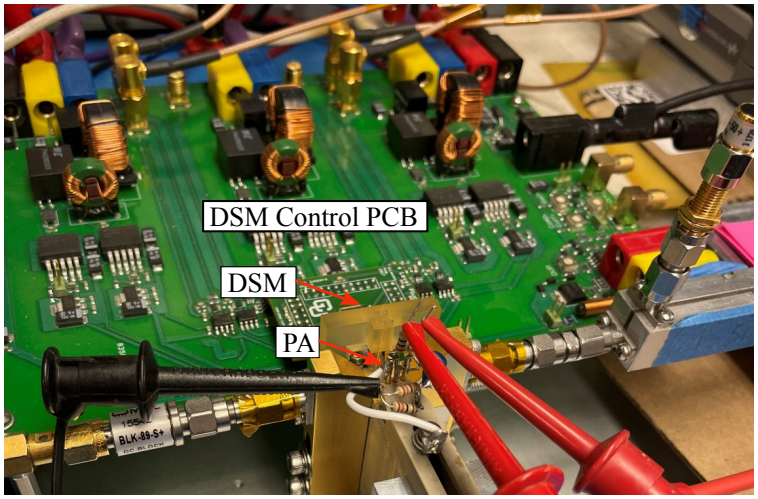

Figure 2.7: Measured gain and PAE curves over $P_{out}$ at 9.7 GHz for the (a) 400 µm amplifier, and (b) the 600 µm amplifier.

#### 2.2.3.2 Measured Dynamic Performance

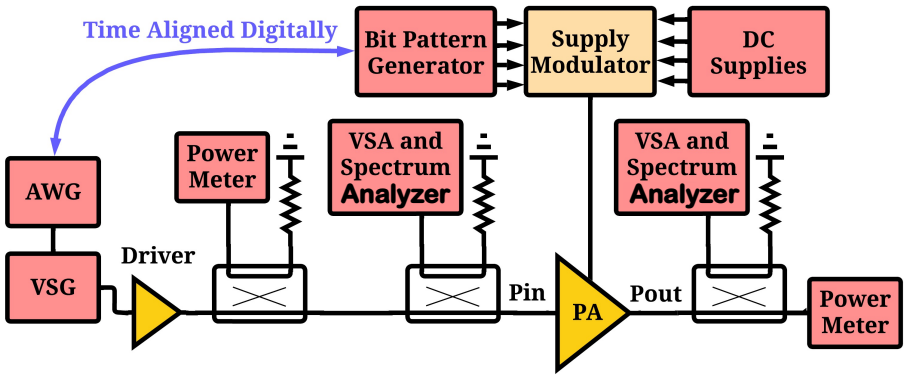
To validate predicted results from the envelope simulator, the performance of both PAs with modulated signals and discrete dynamic drain voltages are measured. The MMIC supply modulator is a discrete multi-level converter designed in the Qorvo 150 nm GaN-on-SiC process, which uses transistors to switch between four externally generated dc voltages, similar to [99]. The DSM is capable of supplying over 30 W of peak power at a switching speed of 100 MHz. The transistor switches in the DSM are controlled digitally through a bit-pattern-generator, which produces synchronous pulses out of multiple channels. The baseband signal is generated using an arbitrary waveform generator (AWG) and then upconverted through a signal generator. The spectrum, IQ signal, and average power are measured at the input and output using a spectrum analyzer, signal analyzer, and power meters. The drain waveform and input signal are aligned at the input of the PA by adding a delay in the trigger of the AWG. The shaping functions are used to determine the timing of the switch between the four voltage levels.

The test bench incorporates an Agilent E8267D PSG and an 1.25 GS/S Keysight N8241A AWG to generate the baseband QAM signal, as shown in Fig.2.8. The supply modulator is controlled via a Sympuls 8x3G Bit Pattern Generator (BPG), which turns on and off the 4 levels based upon the baseband signal uploaded to the AWG. The input and output waveforms are sampled using directional couplers, and their IQ data are sampled using an Agilent N9030A signal analyzer and a SPDT switch. Power meters are connected at the input of the system through a coupler and at the output through an attenuator and are de-embedded to provide absolute average power levels.

Both PAs are measured on the test bench with 6.75 and 67.5 MHz 64-QAM signals that have PAPRs of 7 dB. Average input power is swept from 0 to 22 dBm which ensures that the small-signal response and the compressed behavior of the amplifier are captured. As seen in Fig. 2.9a, the PA with the larger-periphery device has significantly improved PAE and gain while maintaining nearly identical linearity compared to the reference amplifier. The larger-device PA achieves a $\overline{\text{PAE}}$ of




(a)



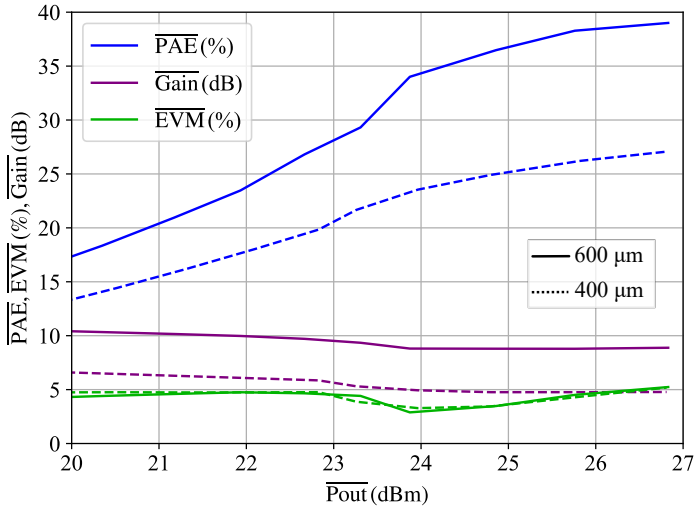

(b)

Figure 2.8: (a) Photograph and (b) schematic of the DSM experimental setup.

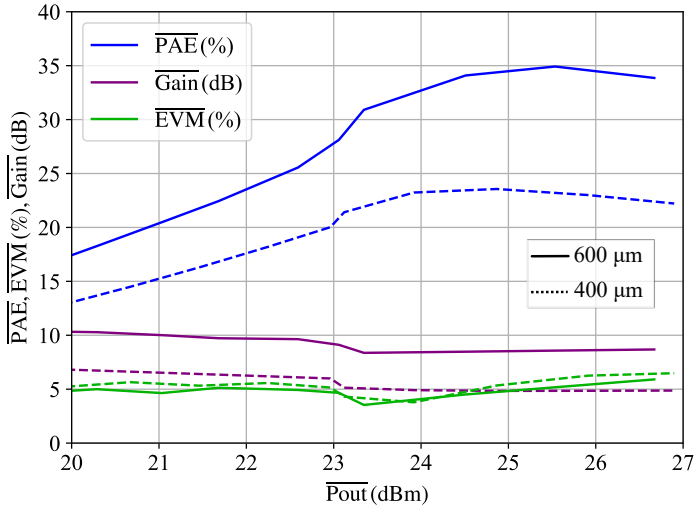
38%, $\overline{\text{gain}}$ of 9 dB, and $\overline{\text{EVM}}$ of 5% at 26.8 dBm out. This represents an efficiency enhancement of $> 10$ pp and a gain improvement of 4 dB compared to the reference PA with the 400 µm device.

### 2.2.4 Periphery Optimization Conclusion

A technique to further improve the efficiency of PAs operating under supply modulation is demonstrated in simulation and measurement. A PA designed with a larger-periphery device operated with lower drain voltages is shown to extend the region of efficiency enhancement further into back off. Namely, a transistor with a larger periphery introduces more relative variation




(a)




(b)

Figure 2.9: Measured dynamic performance of the two PAs at 9.7 GHz with a (a) 6 MHz, and (b) 67.5 MHz 64-QAM signal.

$\Delta V/V_{dd,max}$ by reducing the $V_{max}$ needed to achieve a particular $P_{out}$. Two 10 GHz MMIC PAs are compared and demonstrate a PAE improvement of 5 pp and $>$ 10 pp in simulation and measurement, respectively. Additionally, gain and linearity are maintained or improved with the technique.

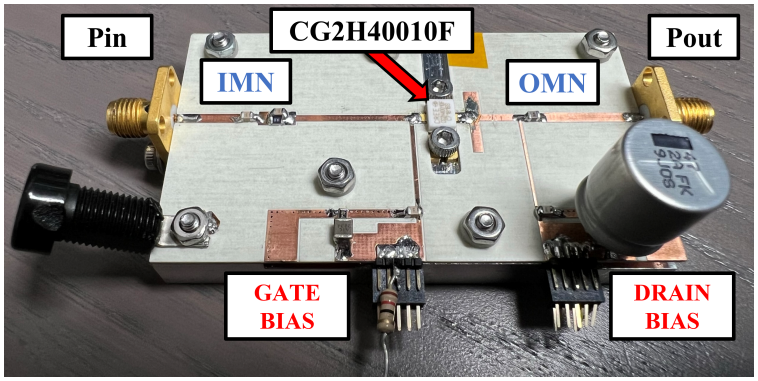



Figure 2.10: Photograph of the 10 W hybrid power amplifier designed for 500 MHz of RF bandwidth, centered at 4.35 GHz. The bias lines are integrated into the matching networks, which are manufactured on Rogers 4350B substrate. The matching networks and the transistor are mounted onto an aluminum base for mechanical stability and thermal dissipation. Note that the large electrolytic capacitor is removed from the drain line to avoid filtering of the drain modulation signal.

## 2.3 Hybrid PA integration with Highly Efficient Discrete Supply Modulator

The supply modulator used in the previous section is designed in the Qorvo 150 nm MMIC process and is based on a simple multi-level converter (MLC) architecture. The supply modulator described in this section is based on a flying capacitor multi-level (FCML) topology, [15], and is designed by collaborators from the Colorado Power Electronics Center (CoPEC). The circuit and control are described in detail in [19], [20]. In short, this architecture has a few significant advantages:

(1) Only two supply voltages to define $V_{max}$ and $V_{min}$ are required for 4 levels. The MLC architecture used above requires M voltages for M levels. The FCML, in principle, could be extended to an arbitrary number of levels between $V_{max}$ and $V_{min}$, at the expense of increased drive complexity as well as a reduction in $\eta$ and switching speed.

(2) The static $\eta$ of the FCML is $> 99\%$ and dynamic $\eta > 95\%$ with a 35 MHz 16 QAM signal when switching speed ($f_{sm}$) $< 15$MHz. Both cases assume a purely resistive PA load, $R_{PA} = 25\Omega$.

(3) No magnetics are required in the implementation of the voltage converter

(4) The control system for the FCML is more integrated and does not require additional external instrumentation to drive the converter.

The main disadvantage of this FCML implementation is that the discrete GaN switching devices used lower the switching frequency to 35 MHz, compared to $>$ 100 MHz for the MLCs. Additionally, the architecture is a true switching power supply and some ripple in the output voltage at intermediate levels is necessarily present.

To test the system performance of the DSM with an RFPA, a *C*-band hybrid PA is used.

### 2.3.1 Design and Characterization of *C*-band Hybrid PA

We designed a 10 W hybrid PA to operate with 500 MHz of bandwidth from 4.1-4.6 GHz shown in Fig.2.10. The hybrid amplifier uses a Wolfspeed CG2H40010F 10 W packaged GaN HEMT, and the matching networks are designed on Rogers 4350B substrate. The input and output impedances are obtained by load-pull for a tradeoff between maximum output power and PAE at a class-AB bias. The harmonics are not terminated specifically. Stability networks consist of a parallel RC in the gate network as well as a capacitor bank with different capacitance values in various packages on the gate/drain bias lines.

The PA performance is first evaluated in CW operation from 4–5 GHz. As seen in Fig. 2.11, the gain and output power correspond closely to simulation with over 10 W out and greater than 8 dB of large-signal gain across the band. Additionally, measured PAE agrees within 5 pp of simulation and demonstrates PAE>50% across the 500 MHz band. The PA performance is also characterized as a function of output power. The measured performance in Fig. 2.12 demonstrates both high efficiency across $V_{ds}$, as well as good control of the compression level of the PA across $P_{out}$ by changing drain voltage.

### 2.3.2 Integration with DSM

Integration of the Hybrid PA with the DSM, Fig 2.13, proved to be a challenging endeavor as the measurement system used provides no trigger and the DSM has no provision to accept a

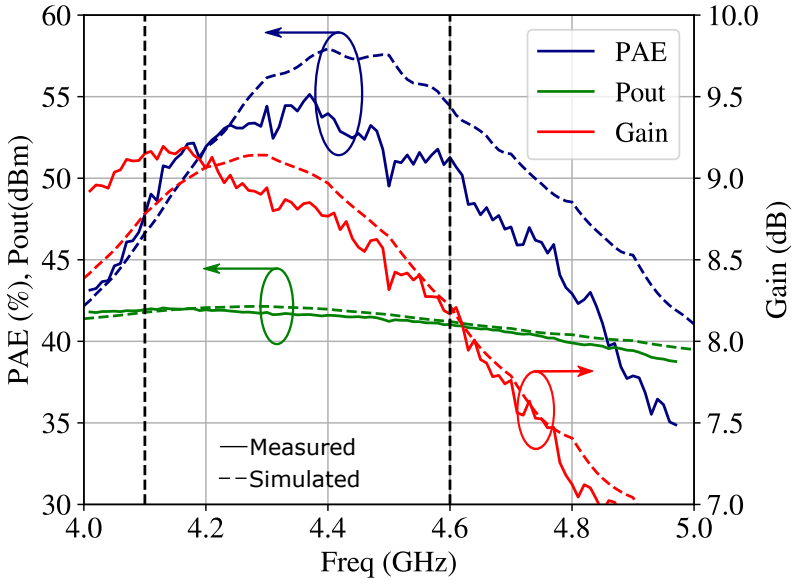



Figure 2.11: Measured (solid) and simulated (dashed) large-signal CW performance versus frequency for the 10 W hybrid PA at $P_{in}$=34 dBm.

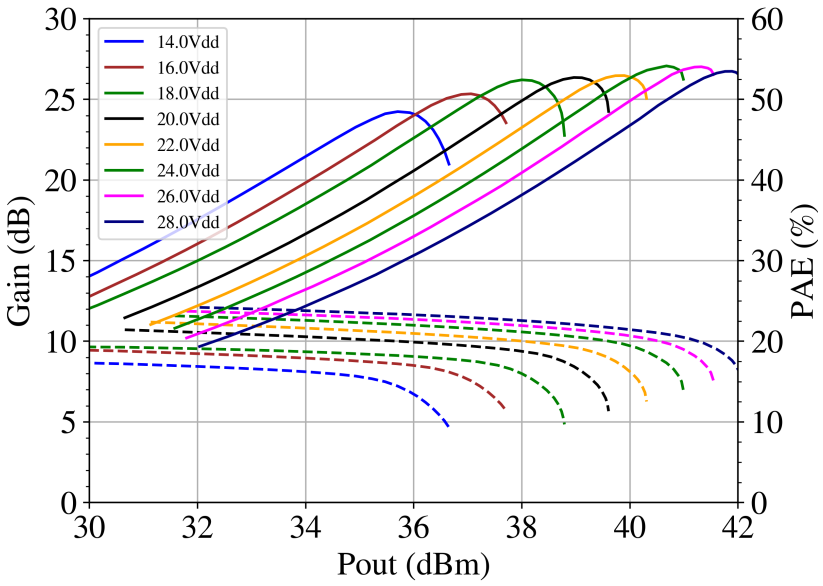



Figure 2.12: Measured PAE and gain as a function of output power and $V_{ds}$ for the hybrid PA from Fig. 2.10 at 4.25 GHz.

trigger input. Thus, time alignment of the baseband RF signal and the DSM output is challenging.

A previous integration attempt was not successful as there was no way to share a 10 MHz reference

between the two systems. The DSM was redesigned to have a faster control FPGA to improve switching speed and an input for an internal 10 MHz reference, which allows the systems to be locked together.

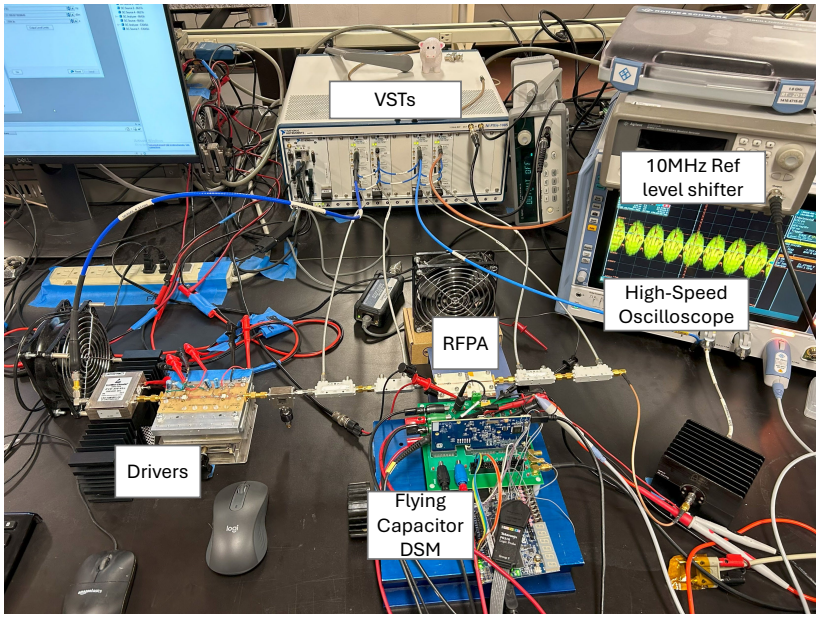



Figure 2.13: Photograph of the DSM measurement setup. The VST-based LSNA provides the wideband RF modulation and calibrated signal analysis for the PA. The DSM is shown in the foreground. The high-speed oscilloscope is used for aligning the DSM and RF waveforms.

The simplified system diagram of the timing and alignment of the two systems is shown in Fig. 2.14. The 10 MHz reference from the measurement system is shared with the DSM via an ARB acting as a logic level shifter between the 1 $V_{pp}$ output of the PXI-e chassis and the 5 $V_{pp}$ input to the DSM FPGA.

The 10 MHz shared reference guarantees synchronization between the two systems, but does not guarantee that the two systems are aligned in time. Both systems act asynchronously with individual internal triggers. As a result, an external instrument is necessary to measure the delay between the DSM and the waveform. A Rhode and Schwarz RTP 8 GHz real-time oscilloscope is used to look at both the signal coming out of the PA and the DSM synchronously. The supply modulator waveform is measured using a RT-ZD10 high impedance probe, and the waveform is

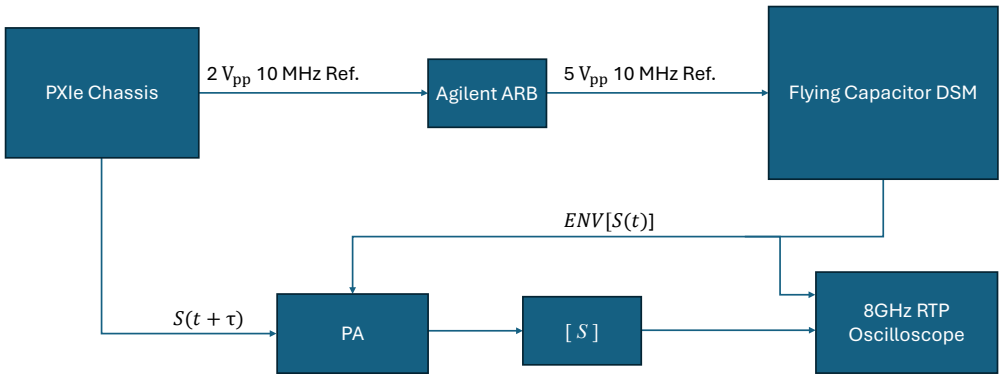



Figure 2.14: Block diagram of the measurement system.

de-embedded to the probe plane by the instrument. However, the RF waveform from the PA is connected via a 50 Ω network. As a result, the RF waveform from the oscilloscope must be manually de-embedded to the output of the PA using the measured $S$-parameters of the output network of the measurement system. Note that the two waveforms are still at slightly different reference planes; the DSM waveform is measured near the output pad of the DSM PCB, while the reference plane for the RF waveform is at the coaxial connector output for the PA. However, given the relatively slow switching speeds of the converter, up to 35 MHz, the IBWs of the test waveforms are relatively modest. This slight offset in reference planes is acceptable, given the bandwidth limitations.

As both the DSM and RF waveforms are periodic, we can, in principle, directly align the two signals. By taking the de-embedded RF output, calculating the power envelope, and then correlating the two signals, we can directly determine the delay. This delay can then be fed to the ARB of the measurement system to align both paths. However, applying the delay to the ARB of the VST causes the waveform to restart and be delayed with respect to some internal trigger. As a result, the delay cannot be directly compensated. Instead, the alignment algorithm runs in a loop until alignment within some tolerance (1 ns in this case) is achieved. This method is slow without the ability to directly change the delay, but it allows for good alignment with limited options to fully align and synchronously trigger both systems. Another important limitation of this alignment approach is that the alignment must be re-run if the waveform output by either ARB changes. A

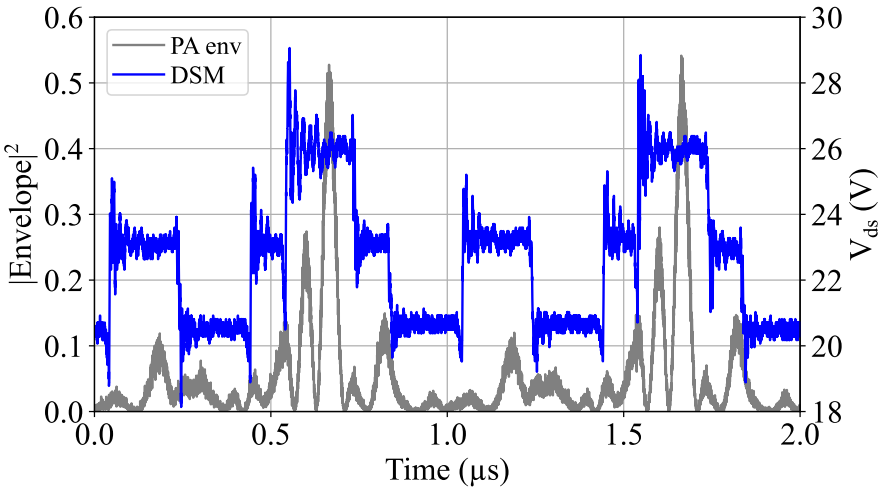



Figure 2.15: Aligned DSM and RF PA. The DSM in this case is switching at 10 MHz with 4-levels. The RF signal is a 20 MHz multi-tone with 27 dBm $P_{avs}$ and 10 dB PAPR.

waveform after alignment can be seen in Fig. 2.15.

The FCML DSM is programmed to follow a direct discretization of the RF signal power envelope, similar to [34]. To extract the FCML levels, the power envelope is discretized using *np.digitize* in Python3. The input envelope is normalized to a maximum voltage level and the number of bins used for discretization is equal to the number of voltage levels, N. In the case shown here, the 18 V level is unused, and the converter acts as a 3-level supply.

### 2.3.3 Results

After a tracking function has been generated and the two systems aligned, the composite results can be obtained. Peak input power ($P_{in,pk}$) is swept from 1-33 dB in 2 dB steps. The signal used is a 20 MHz wide signal with a PAPR of 10 dB. The signal has 18 active tones and 3 inactive tones in the center to form a notch. The static case is obtained with the supply modulator outputting a 26 V constant drain bias. The dynamic case is obtained from the supply modulator outputting the $V_{ds}$ waveform seen in Fig. 2.15 between 20 and 26 V.

The PAE with both a dynamic and static $V_{ds}$ is shown in Fig.2.16 along with the delta PAE in pp. The PAE in both cases is a composite and includes the dc power consumption of

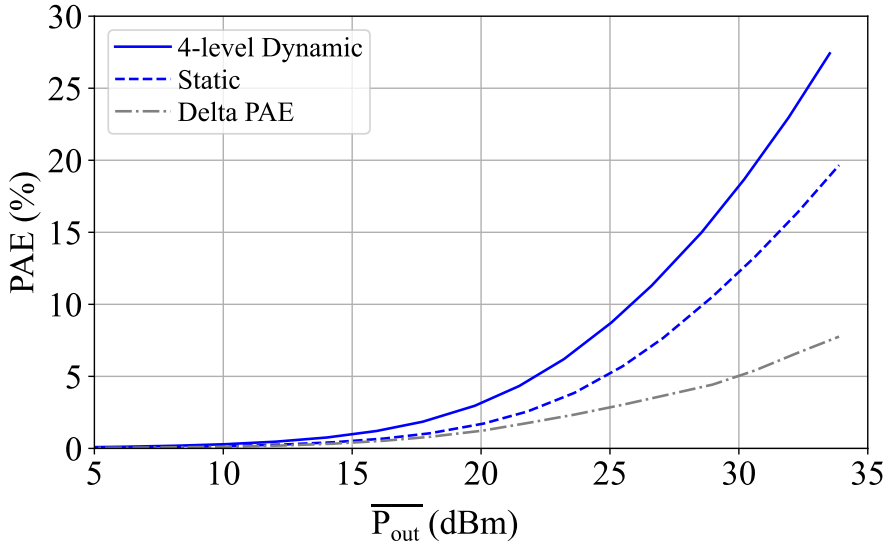



Figure 2.16: PAE across average $P_{out}$ for (dashed) a fixed $V_{ds}$=26 V and (solid) dynamic $V_{ds}$. The improvement in PAE (pp) is shown with the gray dash-dotted line. The signal is a 20 MHz multi-tone with 10 dB PAPR and the FCML is switching at 10 MHz in the dynamic case.

the FCML dynamic supply. The improvement in PAE is consistent across output power, with a peak improvement of $>$ 7 pp at an average output power of 34 dBm. It is also of interest to look at the dc power consumption, Fig 2.17. The dynamic case consumes 5.23 W of output power, whereas the static case dissipates 8.73 W, corresponding to a 3.5 W, or 40 % reduction. These composite improvements to efficiency and dc power consumption validate that the supply modulator is maintaining high efficiency when presented with the complex and time-varying load of the PA. They additionally validate the power envelope tracking trajectory used.

As discussed throughout this thesis, efficiency enhancement alone is not sufficient for communications applications and must be achieved without a significant degradation of linearity. For applications where linearity is not a concern, switched-mode or tube-based solutions will still offer better efficiency. Fig. 2.18 shows the ACPR results with and without the dynamic supply. The ACPR is significantly degraded at low average $P_{out}$ levels by $>$ 10 dB due to the distortion caused by the discrete voltage steps and the ringing illustrated in Fig. 2.15. However, at higher power levels, the ACPR results tend to converge, and similar linearity is obtained in both cases.

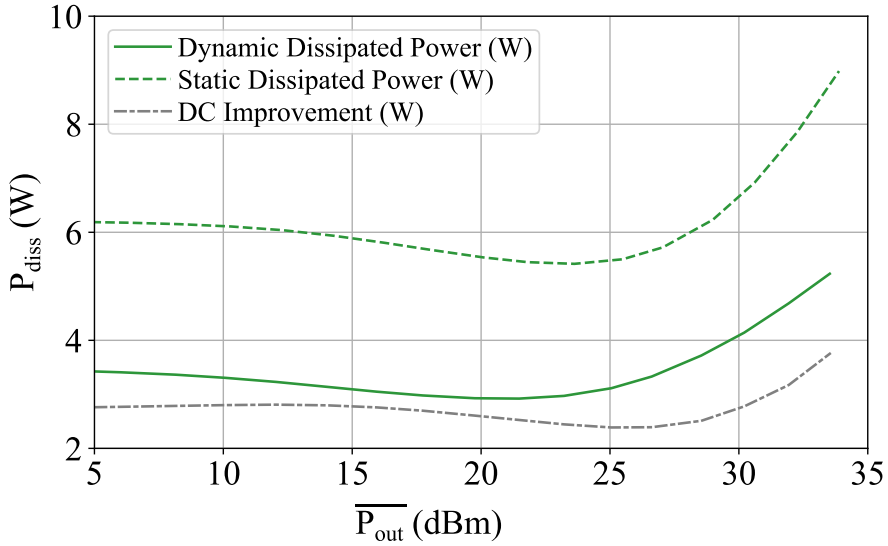



Figure 2.17: $P_{diss}$ across average $P_{out}$ for (dashed) a fixed $V_{ds}$=26 V and (solid) dynamic $V_{ds}$. The improvement in dc power consumption (W) is shown with the gray dash-dotted line. The signal is a 20 MHz multi-tone with 10 dB PAPR and the FCML is switching at 10 MHz in the dynamic case.

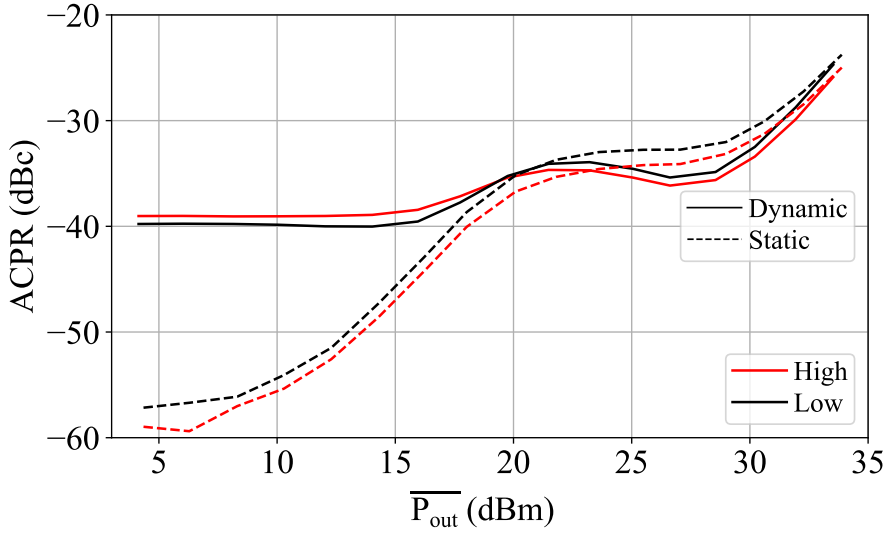
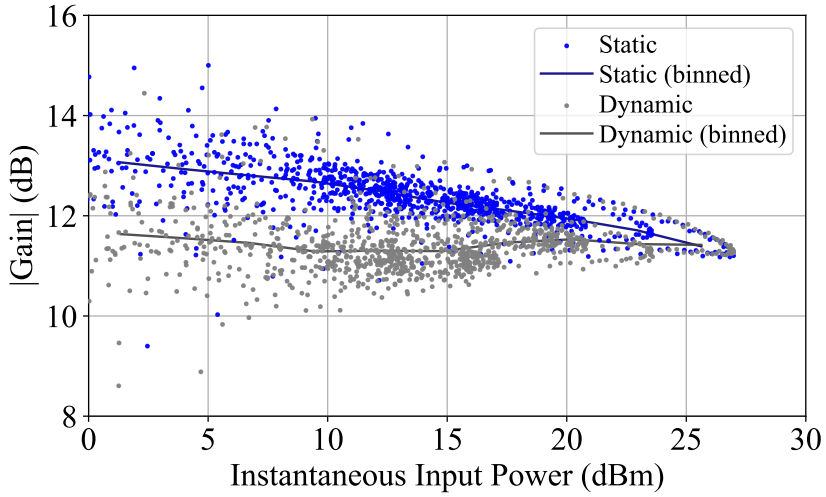
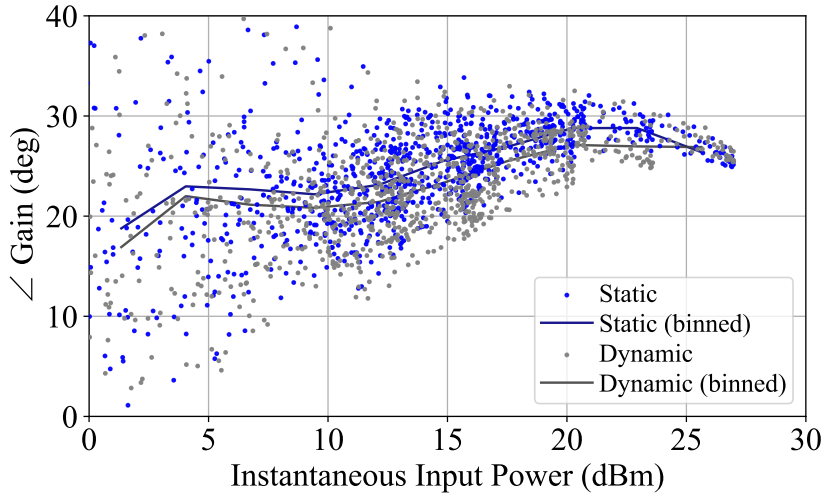



Figure 2.18: ACPR (red) high and (black) low across average $P_{out}$ for (dashed) a fixed $V_{ds}$=26 V and (solid) dynamic $V_{ds}$. The improvement in ACPR (dB) is shown with the gray dash-dotted line. The signal is a 20 MHz multi-tone with 10 dB PAPR and the FCML is switching at 10 MHz in the dynamic case.

This convergence in the linearity at high $\overline{P_{out}}$s is corroborated by Fig. 2.19 which shows the instantaneous gain magnitude and phase for both static and dynamic $V_{ds}$ at $P_{in,pk}$=27 dBm. Both




(a)




(b)

Figure 2.19: Instantaneous Gain (a) magnitude and (b) phase for hybrid PA with FCML demonstrating similar behavior between the two cases

the instantaneous gain magnitude and phase follow similar trajectories, and the dynamic case is free of drastic discontinuities, which can occur at the voltage transition. The output spectrum of the PA shown in Fig. 2.20, also shows very similar output spectra in both cases.

## 2.4 Conclusion

This chapter explores two contributions to the concept of dynamic supply modulation for power amplifiers to improve efficiency under modulated signal excitations. Supply modulators

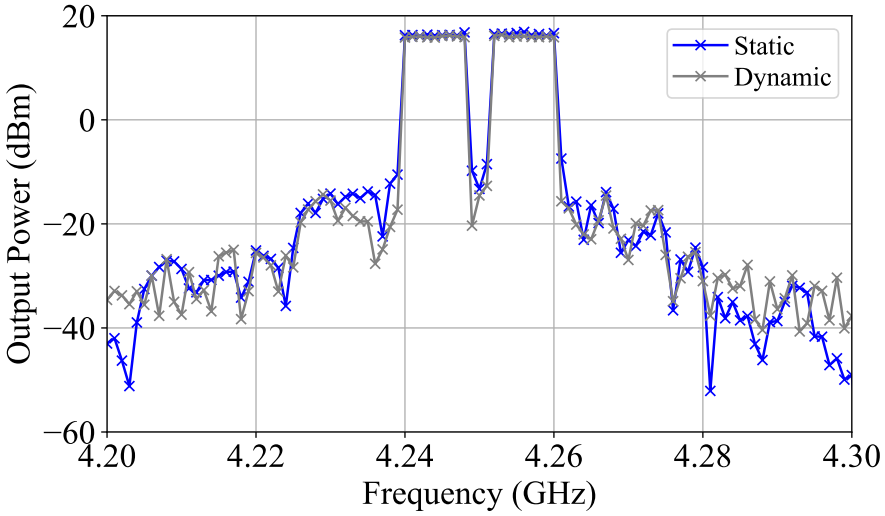



Figure 2.20: Frequency spectra in (blue) static and (grey) dynamic operation for a $P_{in,pk}$=27 dBm. The signal is a 20 MHz multi-tone with 10 dB PAPR and the FCML is switching at 10 MHz in the dynamic case.

are typically realized with switching architectures due to their higher efficiency. Switched-mode architectures, like the MLC, can be limited in the maximum difference in voltage between their maximum and minimum output voltages. This reduces the back-off efficiency enhancement that can be obtained. In modern GaN processes which exhibit both high power density and MSG at a particular $f_c$, a tradeoff can be made by utilizing larger periphery devices with a lower $V_{ds}$, to increase the relative difference between the maximum and minimum voltages. This results in higher average efficiencies with a modulated signal, at the expense of gain and a lower power density. The results of this analysis are available in [62]. Additionally, an FCML discrete supply modulator, designed by collaborators from CoPEC, is integrated with a hybrid $C$-Band PA. Experimental results demonstrate efficiency improvements of up to 7 % and $>$ 3 W of reduction in dissipated power at $\overline{P_{out}}$ = 33 dBm with a multi-tone signal with 10 dB PAPR and 20 MHz of IBW.

# Chapter 3

## Gate Modulation for Linearity Enhancement

As demand for mobile data continues to grow, the emerging FR3 band (7–24 GHz) offers significantly higher throughput than FR1 while reducing cost and complexity compared to FR2 millimeter-wave transceivers [1]. Ku-band is also of interest in satellite communications, including commercial direct-to-user satellite services. A key limitation in achieving high data rates is the linearity of the transmitter power amplifier (PA) [93]. While digital predistortion (DPD) is widely used to address this, its power consumption becomes prohibitive for wide instantaneous bandwidth (IBW) signals [12], and requires knowledge of the baseband signal, rendering it impractical for applications such as satellite repeaters. This motivates the need for a low-power analog linearization technique.

Gate modulation is a technique that shares many commonalities with drain modulation, discussed in the previous chapter. Gate modulation dynamically adjusts the gate bias of the transistor in response to the input envelope, enabling real-time gain shaping without disturbing the RF path, shown in Fig. 3.1. At a basic level, both techniques seek to dynamically change an amplifier's operating point in response to the instantaneous input signal. Dynamic modulation of the drain is typically associated with improving efficiency under modulated conditions, while gate modulation is regarded as a method to improve linearity. However, these two are rarely independent in a common-source FET amplifier. As demonstrated in [80], and as will be further substantiated in this chapter, a simultaneous enhancement can be achieved with either technique.

Another attractive feature of gate modulation is that driving the gate of a device with an AC

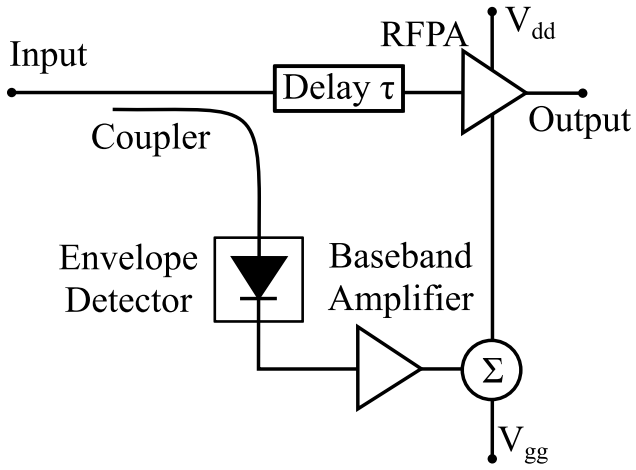



Figure 3.1: High-level block diagram of the gate-modulation analog linearization approach. A portion of the input signal is fed to an envelope detector and controls the gate bias of the power amplifier. The delay, $\tau$, ensures that the gate control and input signal are synchronous, while the baseband amplifier is used to adjust the amplitude of the gate modulation signal. A dc offset, $V_{gg}$, may be applied to achieve some nominal bias-point.

signal is a substantially easier task when compared to driving the drain. While the drain presents a mostly real low-impedance AC load, which provides most of the power for RF-dc conversion, the gate is ideally an open circuit, and while in practice, the parasitic capacitances must be accounted for, the gate may be driven with a small linear amplifier with little impact on overall system efficiency. The possibility of driving the gate with a linear baseband amplifier, rather than a digitally driven or digitized version of the input signal, opens up the possibility for efficient, fast, and simple, fully analog gate-tracking systems. It is worth noting, however, that for very large instantaneous bandwidth signals or devices with large gate-source or gate-drain capacitances, the power consumption of the envelope amplifier can become significant from a system perspective.

To understand the theoretical appeal of this technique, we must consider Fig.3.2, which returns to the synthetic linearity, efficiency, and gain (LEG) benchmark for an ideal load-line PA model, introduced in Ch.1. A trajectory that maximizes this benchmark at each input power back-off point is also plotted. As a continuous function of $V_q$ over input power back-off, this trajectory can be readily achieved via gate modulation. This trajectory physically corresponds to

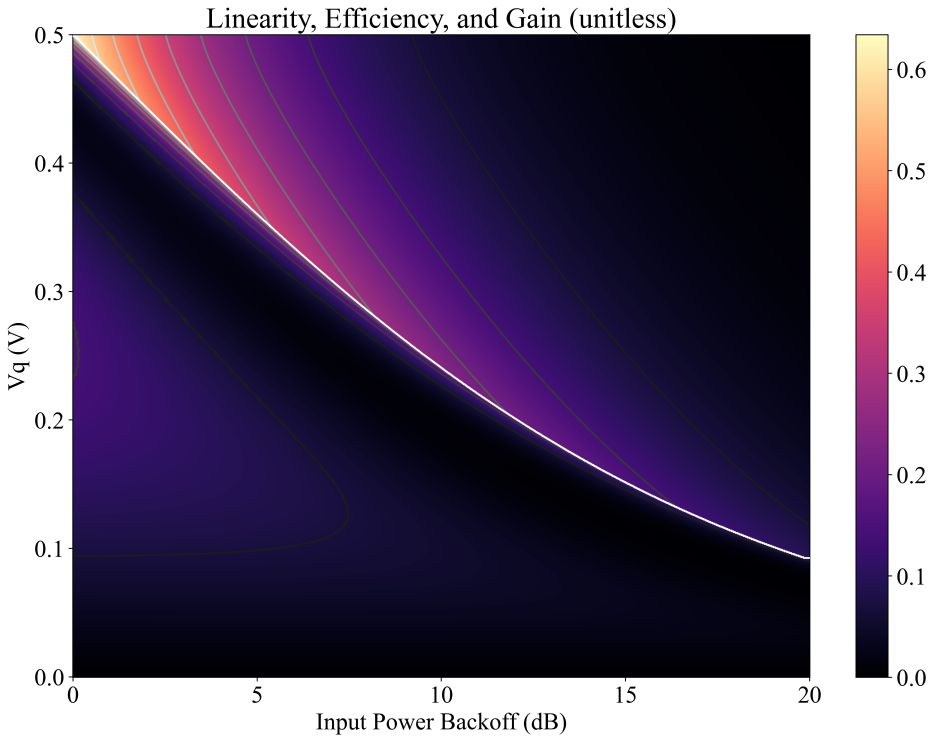



Figure 3.2: LEG synthetic benchmark shown as a function of operating point ($V_q$) and input power back-off; compared to previous chapters, the $R_{opt}$ is held fixed at the value for Class-A and B operation (1 Ω) and does not change across $V_q$. A trajectory that maximizes this metric at each back-off level is shown in white and can be readily achieved using gate modulation.

the lowest $V_q$ at a particular operating power, which maintains a 360° conduction angle. Thus, we can maintain class-A gain and linearity, Fig.3.3, while also substantially improving the back-off efficiency compared to a static class-A bias. Therefore, with this idealized static drain and load load-line model, gate-modulation provides a way to maximize this benchmark across input power back-off, shown in Fig.3.4.

## 3.1 Integration of a Ku-Band GaN PA with GaAs Gate Modulator

In this chapter, we present the first gallium nitride (GaN)-GaAs hybridly integrated analog gate-modulated linearization system for Ku-band amplifiers, achieving the widest measured linearization bandwidth reported for any analog solution, to the best of the authors' knowledge. The single-gate control architecture for continuous envelope modulation delivers efficient broadband

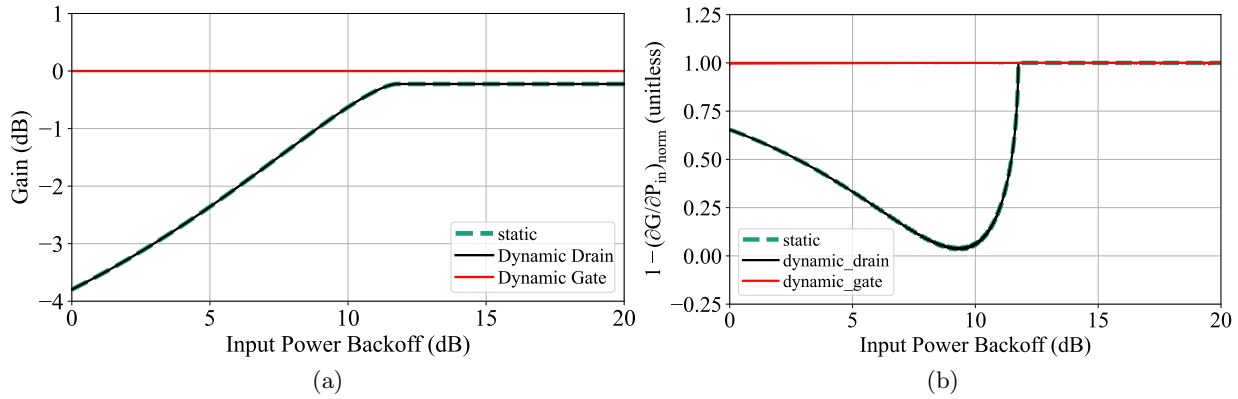



Figure 3.3: Comparison of (a) gain and (b) linearity for static and dynamic drain with a fixed $V_q$ corresponding to a conduction angle of 210° at $P_{sat}$ with gate modulation. Both the static and dynamic drain cases suffer from rapidly changing gain at higher drive levels, which reduces linearity. The gate modulated case, following the trajectory shown in Fig.3.2, maintains class-A gain across all input power levels. Note the slightly degraded gain in back-off compared to gate-modulation for drain-modulation and static cases, which is due to a slightly mismatched $R_{opt}$ for the operating class. The dynamic-gate case is shown with a constant $R_{opt}$ for class-A operation.

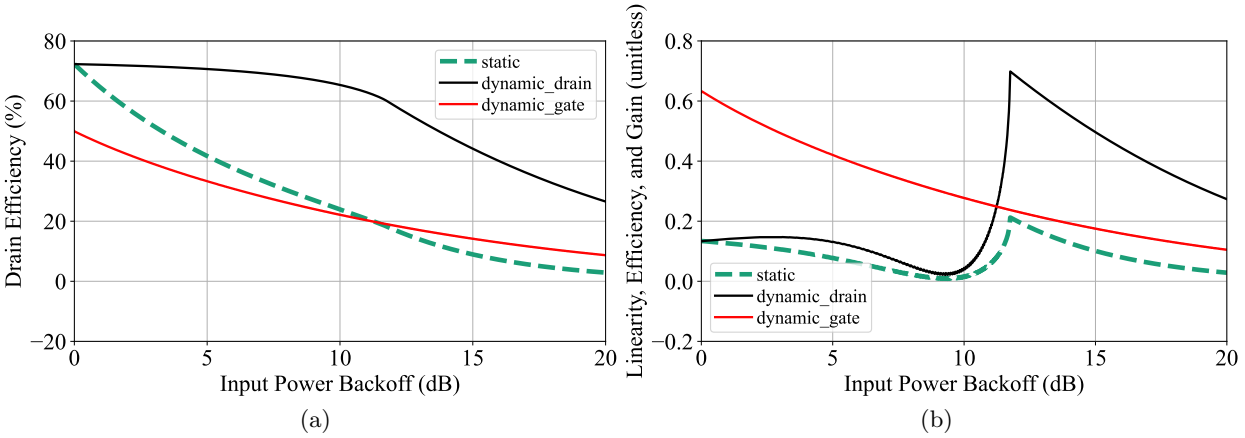



Figure 3.4: Comparison of (a) drain efficiency and (b) LEG for static and dynamic drain with a fixed $V_q$ corresponding to a conduction angle of 210° at $P_{sat}$. Efficiency is better in both the static and drain modulated cases for most back-off levels due to the dramatic difference in operating class in this example. LEG is best for gate modulation, while drain modulation and static cases see a peak in back-off where the load-line model returns to a 360° conduction angle, allowing gain and linearity to recover to their maximal values.

linearization with low RF loss and minimal dc power consumption, without any digital overhead.

The equivalent system diagram is shown in Fig. 3.5, which shows the core functionality of the GaAs

and GaN MMICs as well as the integration PCB. The decision to use GaAs instead of GaN for the envelope detector arises from the smaller devices available in many GaAs processes, as well as lower cost. In principle, however, the two MMICs could be monolithically integrated.

The goals of this chapter are to:

(1) demonstrate an integrated gate-modulation linearization approach with low power and loss; and

(2) evaluate the achievable linearity in a class-AB multi-stage PA with gate bias modulation of a single gate.

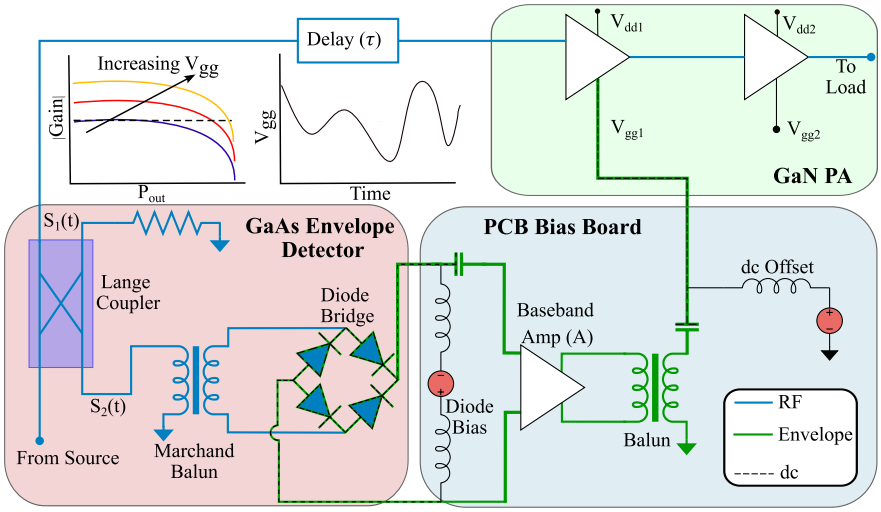
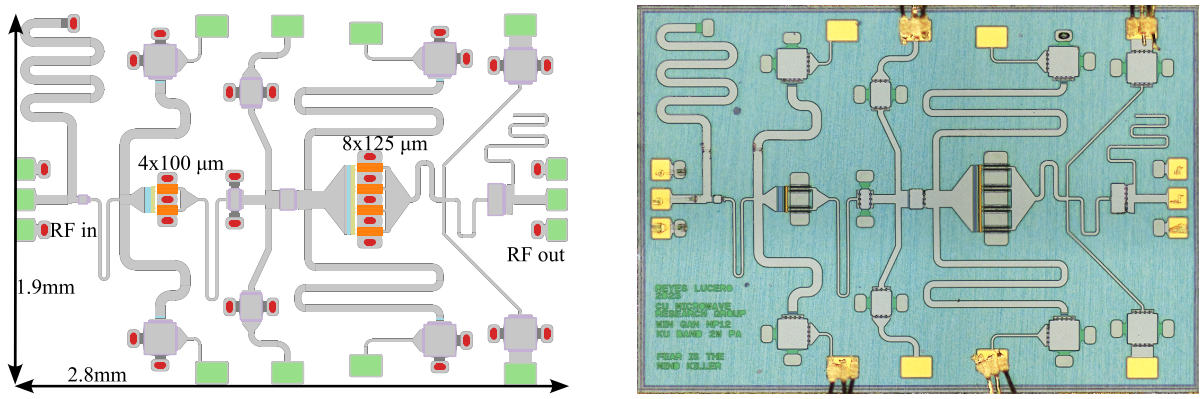



Figure 3.5: System level diagram of the GaN PA with the GaAs envelope detector for integrated analog-domain gate modulation.

## 3.2 GaN MMIC Power Amplifier

To demonstrate the linearization of analog single-gate tracking, a class-AB 2-stage PA is designed with minimal shunt capacitance in the first-stage gate bias. This is to avoid filtering the baseband gate signal as well as to ensure unconditional stability across a wide range of biases.

The PA design goals are to cover all of Ku-Band with $P_{out} > 2\,W$, $|S_{21}| > 20\,dB$, and $PAE > 30\,\%$. The design is implemented in the WIN Semiconductors 120 nm GaN-on-SiC 28 V process, with a




(a) (b)

Figure 3.6: (a) Layout and (b) photomicrograph of the GaN MMIC PA.

first and second stage periphery of 400 and 1000 $\mu$m, respectively. The bias lines are duplicated on the top and bottom of the chip (Fig. 3.6) to facilitate integration. The on-chip bypass capacitors on the gate bias lines have a capacitance of 5.3 pF to minimize filtering of the gate modulation signal. Additionally, stability, without the need for external capacitance, is validated through Nyquist stability simulations across a wide range of first-stage gate voltages.

### 3.2.1 CW PA Characterization

The measured $S$-parameters for a range of $V_{gg,1}$ biases, Fig. 3.7, show a gain above 20 dB for higher gate biases, although it does roll off at the upper end of the band (>17 GHz). At lower biases, $|S_{11}|$ < -10 dB, but the match is degraded below 13 GHz and at higher bias levels, while $|S_{22}|$ < -5 dB for all but the lowest bias across the band.

Next, the PA is measured using a Maury Microwave MT2000 mixed-signal active load-pull system, which allows for calibrated large-signal vector measurements needed to fully characterize the gain magnitude and phase response across input power. As seen in Fig. 3.8, the PA output power exceeds 2 W across the band. The gain and PAE are lower than predicted by simulations in the upper edge of the band (>17 GHz). Overall, the amplifier exhibits >16 dB of saturated gain and PAE > 30 % at 19 dBm input power and from 11.5-16 GHz, which corresponds to a fractional

bandwidth of 33 %. Table 3.1 presents a favorable comparison with other GaN Ku-band PAs with analog linearization.

Table 3.1: Summary of GaN PAs covering all or part of Ku-Band

| Ref. | Frequency (GHz) | $L_{gate}$ ($\mu$m) | PAE (%) | Chip Area (mm$^2$) | $P_{out}$ (dBm) |
|---|---|---|---|---|---|
| [90] | 13.7–15.3 | 0.25 | 29–40* | 4.96 | 36.6–37.7 |
| [60] | 15–24 | 0.14 | 19–31 | 30.0 | 41.7–43 |
| [119] | 11–17.5 | 0.15 | 18–34 | 6.4 | 34.0–36.2 |
| [49] | 6–18 | 0.15 | 25–40 | 14.0 | 40.2–42.5 |
| [This Work] | 11–18 | 0.12 | 20–33 | 5.3 | 33.9–34.9 |

$*$: Drain Efficiency (DE)

To evaluate how well the amplifier can be linearized by modulating the first-stage gate bias, vector large-signal measurements are taken across gate voltage, power, and frequency. The measured gain amplitude response, shown in Fig. 3.9a, is readily linearizable by increasing the gate voltage proportionally with input power. Any class-AB amplifier experiences an increase in conduction angle as it is backed off, until it is operating in class-A. By dynamically reducing the gate

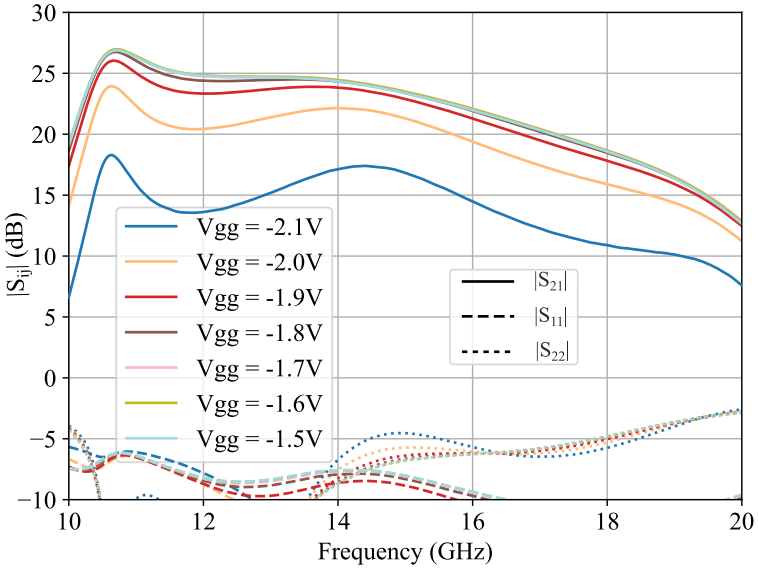



Figure 3.7: Measured $S$-parameters of the PA over frequency and gate voltage demonstrating low return loss and high gain across Ku-band at a nominal drain voltage of 28 V. The PA also demonstrates consistent gain control by varying $V_{gg,1}$.

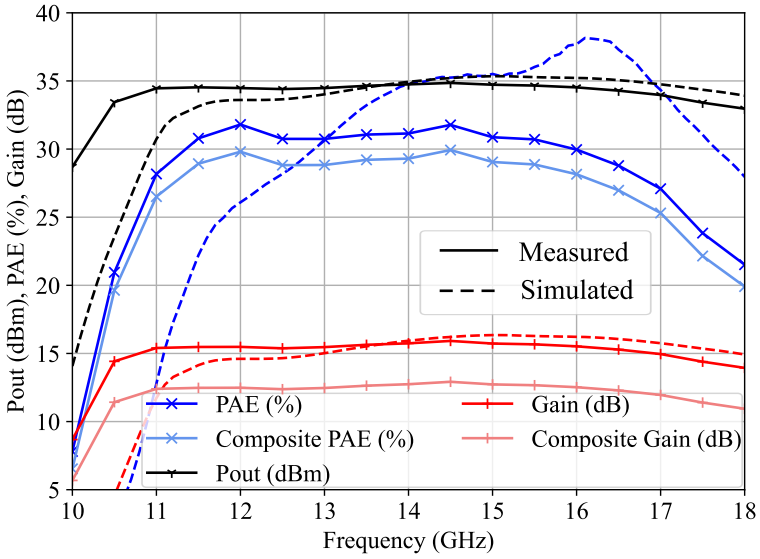
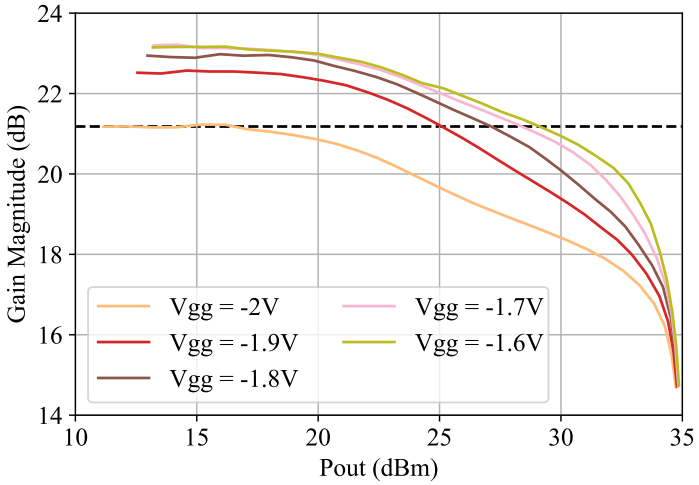


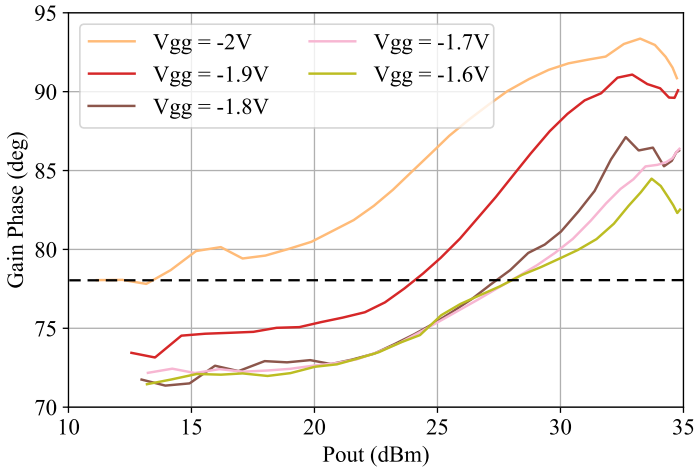

Figure 3.8: Measured and simulated large-signal performance of the amplifier across Ku-Band with a first stage gate bias of -1.7 V and an available source power of 19 dBm.

voltage with back off, gate-modulation allows the amplifier to maintain a more constant conduction angle, which reduces the variation in the complex gain. The horizontal dashed line in the plot shows an example flat-gain trajectory across output power; by changing the gate voltage as a function of input power, the gain magnitude can be kept at a constant value of 21.7 dB from back off to a peak power of $\sim$ 29 dBm.

The gain phase response, Fig. 3.9b, can be linearized in a similar manner; increasing the gate voltage with input power can provide a flat gain phase of $\sim 78^\circ$ from small-signal to $P_{out}\sim$ 28 dBm. However, the trajectories for flat gain magnitude and phase are, in general, different. Here, we focus on tracking a linearly scaled representation of the signal envelope using a single gate bias. In [58], it is shown that this is not sufficient for fully linearizing a memory-less nonlinearity, but is significantly simpler for an analog integrated solution than a dual-gate bias control solution. Additionally, [56] discusses tradeoffs in tracking functions for a digitally driven single-gate tracked PA.




(a)

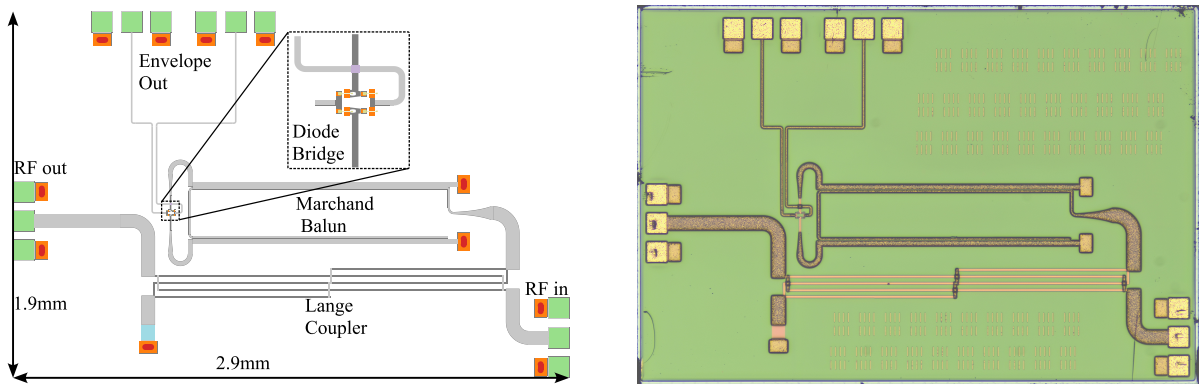



(b)

Figure 3.9: Measured instantaneous gain (a) magnitude and (b) phase response of the PA at 14 GHz over $P_{out}$ at multiple $V_{gg,1}$ bias points.

## 3.3 Envelope Detector GaAs MMIC

Analog-domain envelope detection is implemented using a custom GaAs MMIC to enable integrated gate modulation for linearity enhancement. At the circuit input, a 10 dB Lange coupler splits the RF signal into two paths (Fig. 3.10). One path feeds the power amplifier input, while the other is routed to a diode bridge envelope detector. Before detection, the signal is converted from single-ended to differential using an on-chip Marchand balun in order to drive the bridge detector symmetrically. The use of a diode bridge, rather than a single-diode configuration, doubles the




(a) (b)

Figure 3.10: (a) Layout and (b) photomicrograph of the GaAs MMIC bridge envelope detector.

responsivity. The detector is designed using field-effect transistors (FETs) from the WIN Semiconductors PQG30C GaAs process, configured as diodes. The transistors have a small periphery of 5 $\mu$m to minimize parasitic effects and save die area. The baseband output from the detector is intended to be buffered off-chip using an external amplifier mounted on the PCB.

The envelope detector performance is evaluated using two-tone signals with tone spacings ranging from 10 to 800 MHz. The diodes are biased at 1.7 V, corresponding to a quiescent current of approximately 1 mA. Output voltages are measured using a differential oscilloscope probe with 800 MHz of bandwidth. The resulting peak-to-peak open-circuit voltage responses are shown in Fig. 3.11. These measurements are not de-embedded; therefore, the influence of the oscilloscope input coupling (including dc-block effects) and the diode-bridge bias network may impact the observed results.

While two-tone signals provide a simple and controlled test case, their statistical characteristics differ significantly from practical communication waveforms. To assess performance under more realistic conditions, the detector is also tested with a 20 MHz LTE signal centered at $f_0 = 14$ GHz and $\overline{P_{in}} = 13$ dBm. The time-domain response is shown in Fig. 3.12, w with both signals normalized to a mean value of 1, and indicates that the detector can reasonably track the varying envelope. However, there is some error in the detected envelope, which will limit the gate-modulator's ability to perfectly track the input signal.

The small-signal parameters of the RF path of the GaAs envelope detector are also of interest due to their impact on the overall RF performance of the system. As seen in Fig. 3.13, the input and output return loss are above 10 dB across the whole band, while the insertion loss is only 2.3 dB. The Lange response is shown to be broadband, and we assume that the detector response varies minimally across the RF bandwidth.

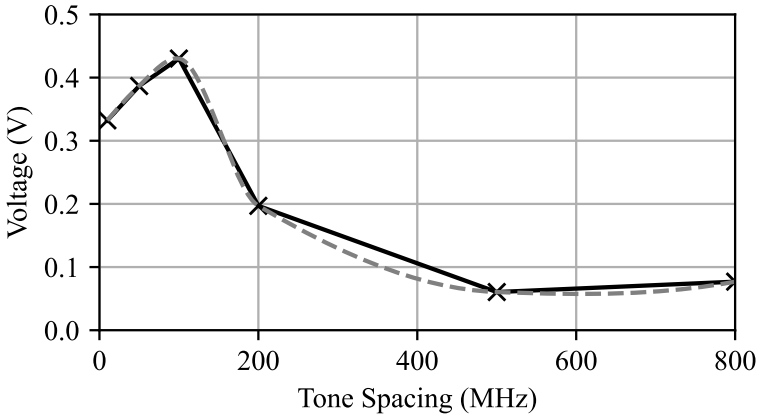



Figure 3.11: Open-circuit voltage response of the envelope detector across the tone spacing of a two-tone signal at $f_0 = 14$ GHz. The measured data with a linear fit is shown in black, and a spline fit is shown with the gray dashed line.

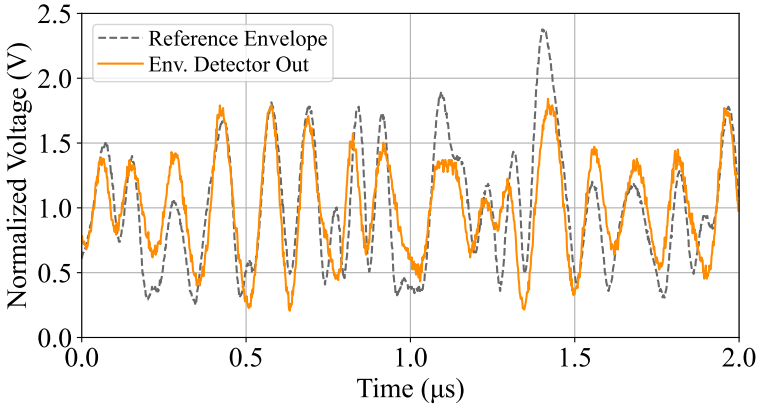



Figure 3.12: Measured time-domain response of the GaAs envelope detector with a 20 MHz LTE signal with 13 dBm of average available source power at $f_0 = 14$ GHz. The ideal envelope is shown with the gray dashed trace, and the measured detector response is shown in orange. The reference envelope is taken as $|I^2 + Q^2|$ directly from the baseband output of SMW200A. The signals are aligned in post-processing using cross-correlation.

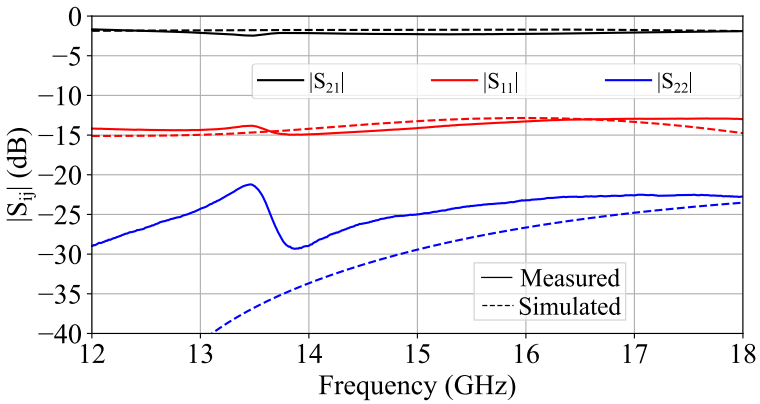



Figure 3.13: $S$-parameters of the *through* path on the GaAs chip measured on wafer, demonstrating insertion loss below 3 dB, and an input and output return loss above 10 dB from 12–19 GHz.

## 3.4 Envelope Co-Simulations

The measured large-signal complex gain of the MMIC PA can be used alongside the open-circuit voltage response of the diode detector to perform envelope simulations and determine the linearization potential of the system. This analysis makes the following assumptions:

(1) the response of both circuits is independent of signal bandwidth;

(2) neither circuit exhibits any memory;

(3) the envelope detector operates solely in the square-law regime; and

(4) the gate of the PA is approximately an open circuit.

These assumptions enable the use of a traditional envelope simulation approach, which allows us to determine an upper bound on the expected linearization.

After characterizing the PA and envelope detector MMICs, their measured responses are used to construct a Python-based time-domain envelope simulation. The large-signal CW measurements of the PA and the two-tone measurements of the detector provide the basis for verifying the gate modulation method under modulated excitation. The amplifier's gain, measured at discrete frequencies and power levels for various values of $V_{gg,1}$, is first gridded and interpolated for each

frequency point. Similarly, the detector's two-tone response at 100 MHz is used to construct an interpolated mapping between $P_{in}(t)$ and $V_{gg}(t)$.

A 300-tone time-domain signal with a 100 MHz bandwidth and 9 dB peak-to-average power ratio (PAPR) is then generated and applied to the simulation. At each time step, the instantaneous input power determines the gate voltage, and together these values are used to find the amplifier gain at $f_0 = 14$ GHz. The complex gain, computed from the voltage magnitude and $V_{gg,1}$, is multiplied by the input waveform to produce the composite system response. Finally, the detector response is linearly scaled to represent a baseband gain, and a dc offset is added. The scaling factor and offset are optimized to minimize the simulated ACPR.

The results of this simulation are seen in Fig. 3.14, which shows the spectrum with and without gate modulation applied. In both cases, $\overline{P_{out}}$ is approximately 23 dBm. ACPR in the static case is -27 dBc and -36 dBc with gate modulation. This 9 dB improvement represents a significant linearization and validates the feasibility of using analog single-gate tracking for multi-stage amplifiers.

### 3.4.1 System Performance Considerations

Although gate tracking is an attractive option for low-power wideband linearization, as with any linearization technique, some performance degradation of the transmitter is unavoidable. In our system, the gain is 2.3 dB lower than that of the PA alone due to loss through the coupler at the input of the GaAs MMIC, shown in Fig. 3.13. In addition, a buffer amplifier is needed to isolate the envelope detector and the first-stage PA gate. In Fig. 3.8, the composite gain and PAE are shown, which include the reduction in gain and $P_{dc}$=0.3 W for the ADA4960 baseband driver amplifier. The envelope detector quiescent power consumption is negligible from a system perspective at 1.7 mW. Gain is degraded by 2.3 dB, and PAE is lower by about 2 percentage points (pp). This trade-off is acceptable, considering the simulated linearity improvement.

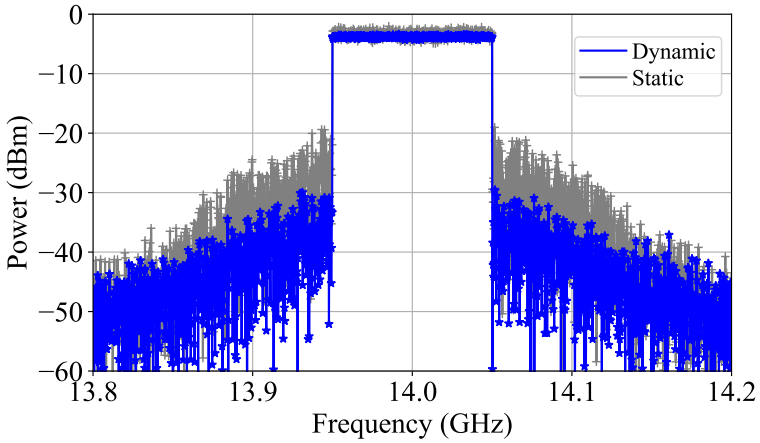



Figure 3.14: 100 MHz 300-tone envelope simulations based on measured CW PA and two-tone envelope detector responses with (dynamic) and without (static) gate modulation, demonstrating 9 dB of ACPR improvement from -27 dBc to -36 dBc with $\overline{P_{out}}$=23 dBm.

## 3.5 MMIC Integration

After characterizing the individual MMICs and verifying linearization using envelope simulations, an integration PCB is designed to perform system-level integrated measurements. The PCB uses a 0.254 mm thick Rogers 4350B substrate and is designed in two parts as seen in Fig. 3.15; a "ring" board which interfaces with the connectors and includes 50 Ω lines which route the RF signal to/from the "main" PCB. The main PCB has cutouts for the MMICs, which are mounted onto a copper-molybdenum (CuMo) base. The main PCB is divided into an RF section, which includes both MMICs as well as a 50 Ω termination for the GaAs envelope detector, and the baseband (BB) section, which includes bias tees for the diode detector, baseband amplifier, and the radio frequency power amplifier (RFPA). The BB section also has an ADA4960 amplifier for buffering and amplifying the gate modulation signal and a Coilcraft JA4220AL transformer for converting the signal from differential to single-ended. The PA input can be written as:

$$S_1(t) = AS_2(t+\tau) \tag{3.1}$$

where $S_2(t+\tau)$ is the RF signal input to the envelope detector. In general, some time shift, $\tau$, will

need to be applied between the PA and envelope detection paths to align them at the transistor plane. Additionally, the amplitude of the gate tracking signal must be scaled by some factor, $A$, to maximize the achievable linearization. This leads to the relation between the two signals shown in (3.1). In principle, this relationship could be achieved by introducing a delay line between the GaAs MMIC and the PA, and the amplitude scaling through adjustments to the gain of the baseband amplifier. The ADA4960 amplifier has a gain that is adjusted by changing the value of a discrete RC network. In our implementation, the two chips are fed by separate SMW200A signal generators with synchronous ARB BB sources, as seen in Fig. 3.16. This allows for the time and amplitude offsets to be digitally set during measurement for best linearization. While our goal is to demonstrate an integrated single-input method for analog linearization, this approach is representative of the performance under that condition, while allowing arbitrary $\tau$ and $A$ offsets to be applied.

The amplitude dispersion of the envelope path was characterized by measuring the response of the envelope detector and PCB baseband path response when loaded with the PA gate, shown in Fig. 3.17. The response exhibits roughly 3 dB of variation over 10–300 MHz. However, the 120 pF dc-blocking capacitors in the detector output path restrict the detection of low-frequency envelope components, while the overall response begins to attenuate beyond 300 MHz. Accurate simulation of the amplitude distortion and group delay is intractable, as it would require computationally intensive transient analyses that simultaneously capture RF and harmonic content along with near-dc envelope behavior spanning widely separated time scales.

## 3.6 Transmitter Measurements and Linearization Results

### 3.6.1 Two-Tone Measurements

To evaluate the linearization potential of the integrated system, a test bench is set up, shown in Fig. 3.16, with 2 Rhode and Schwarz SMW200A signal generators with IBWs up to 2 GHz. These generators have the baseband ARBs synchronized via a 10 MHz reference, a shared trigger, and

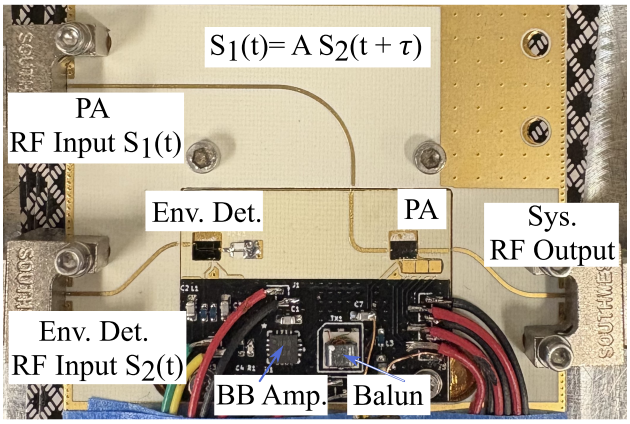



Figure 3.15: Image of the two MMICs integrated into the PCB, comprising the full linearized system. The two RF inputs are to allow a linear scaling and time offset between the two MMICs.

are run in a controller-responder configuration. This allows the two generators to be synchronous at baseband. The local oscillator (LO) is also shared, even though strict RF alignment is not necessary, as gate modulation is only affected by the envelope alignment between the two paths.

We begin by verifying the MMIC PA CW performance when integrated on the PCB. As seen in Fig. 3.18, both gain and PAE are significantly lower when integrated on PCB compared to on-wafer performance. Finite element method (FEM) simulations in High-Frequency Structure Simulator (HFSS) of a 20 mm long 50 Ω line on PCB wire bonded to a 3 mm long 50 Ω line on SiC, Fig.3.19, indicate an insertion loss of 0.7 dB and a return loss of 14.6 dB at 14 GHz shown in Fig.3.20. This suggests that the raw dielectric material, manufacturing, or assembly issues caused higher loss than predicted in simulation. Regardless, the MMIC PA has sufficient performance to determine the efficacy of the integrated analog linearization system. The integrated PA performs best at the lower frequencies, which suggests that the realized loss is higher than simulated and the measurements in this section are all taken at a $f_c$=14 GHz. The GaAs gate modulator is demonstrated to be wideband and linearization results at 14 GHz are representative of performance across Ku-band.

Next, we evaluate the ability of this gate modulation implementation to reduce the $IMD_3$ products of a two-tone signal. 30 tone spacings are used, which are logarithmically arranged

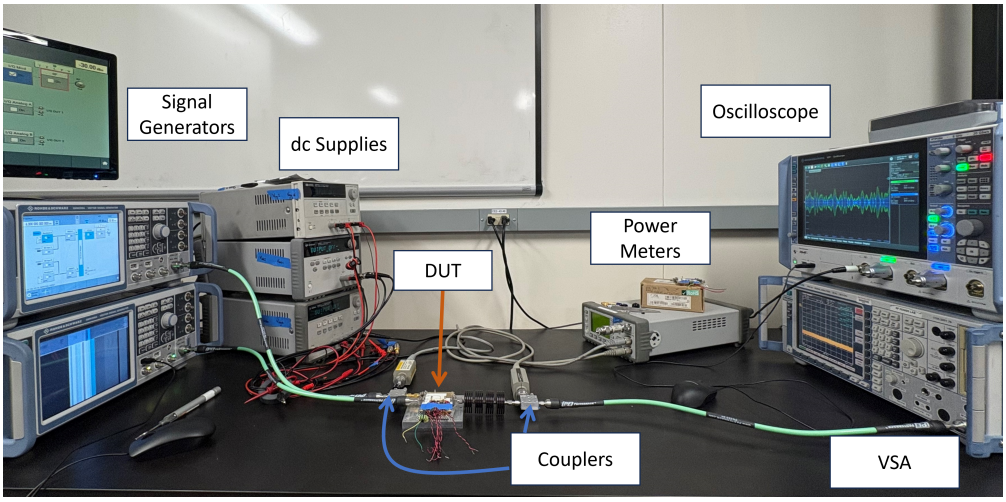



Figure 3.16: Photograph of the experimental setup.

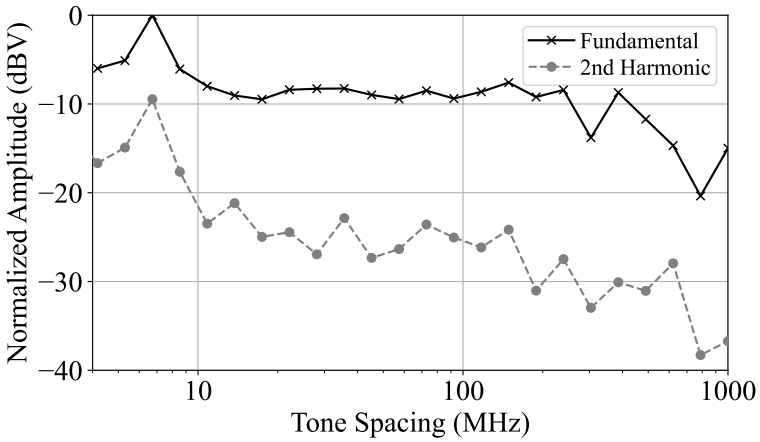



Figure 3.17: Measured detector voltage response when loaded with the PA gate.

between 10 and 1000 MHz. The baseline PA performance is first established by debiasing the baseband amplifier and the diode detector. Next, a Bayesian optimizer is used to find the optimal $\tau$ and $A$ offsets between the gate-modulator and the PA for each tone spacing at a $P_{in,pk}$=10 dBm. The results of this analysis are shown in Fig. 3.21a, which demonstrates $IMD_3$ reduction for IBWs from 10-1000 MHz. The improvement is $<$ 10 dB at 10 MHz and improves out to $\sim$15 dB for both the upper and lower $IMD_3$ tones from 20 - 300 MHz. Beyond 300 MHz, the $IMD_3$ improvement degrades with tone spacing, to a minimum value $<$ 5 dB at 1000 MHz. The $\tau$ and $A$ coefficients found

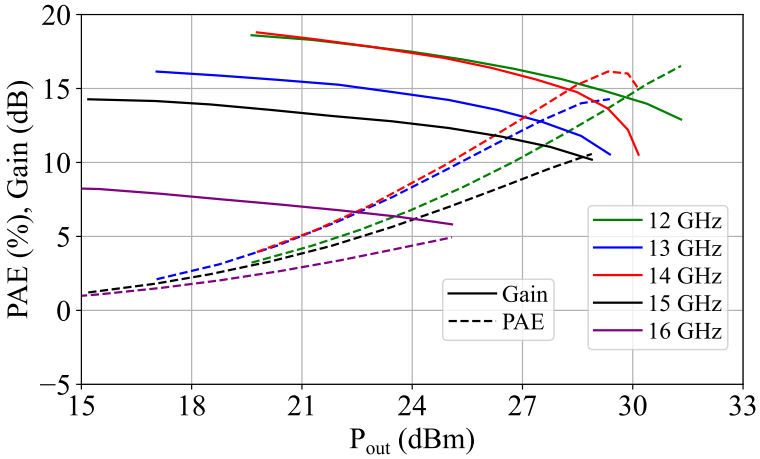



Figure 3.18: CW performance of the PA measured within the PCB. The performance is degraded relative to that of the PA measured on wafer (Fig. 3.8).

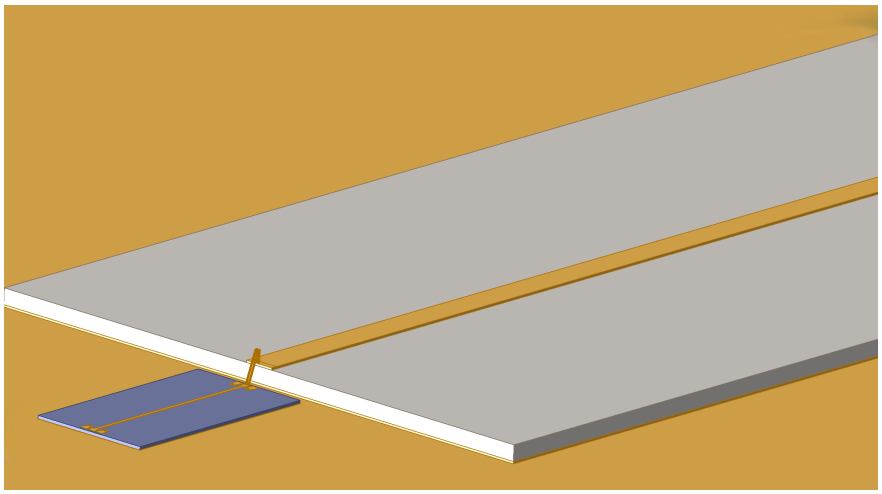


Figure 3.19: Geometry of the modeled bondwire interconnect from a 20 mm long 50Ω line on 10 mil RO4350B to a 3 mm long line on 2 mil SiC in HFSS to investigate potential mismatch of the interconnect and loss of the PCB substrate at Ku-band.

through optimization can be seen in Fig. 3.21b. The bounds on optimization are $A \in [-15, 5]$ dB and $\tau \in [-20, 10]$ ns. Overall, the circuit demonstrates ∼10 dB of linearization improvement from 10-600 MHz.

While the previous section describes the best improvement our system can deliver with optimized $\tau$ and $A$ offsets between the two paths, it is also of interest to see how well this linearization

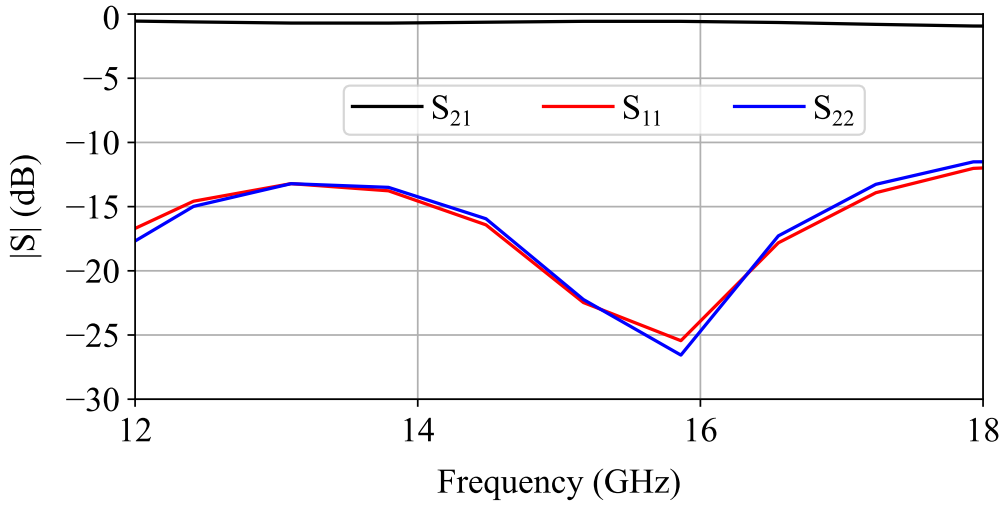



Figure 3.20: Simulated results of the MMIC-to-PCB transition demonstrating low-insertion loss and high return loss across Ku-band, suggesting a reasonably well-matched interconnect free of moding or resonances.

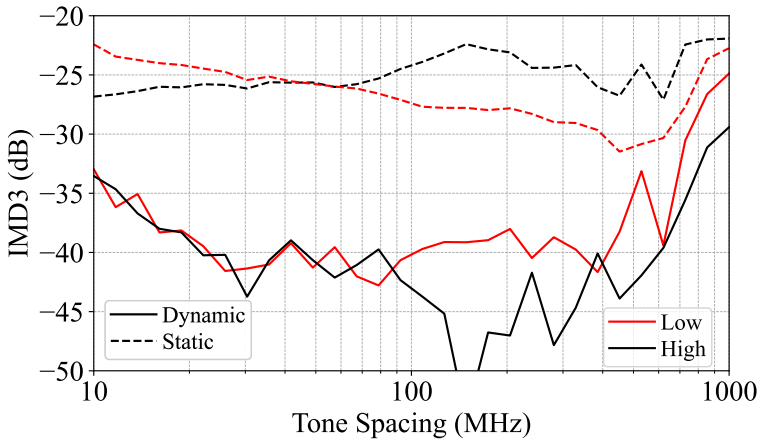
system works in a constant configuration across bandwidth. To that end, we also analyze how the system performs with constant values of $\tau$ and $A$, seen in Fig. 3.22. In this case, the mean of the $IMD_3$ tones is taken and compared to the static configuration with the detector and baseband amplifier unbiased. The test case where both $\tau$ and $A$ are optimized for a specific bandwidth performs significantly better than any other configuration, due to significant variation over frequency of the designed baseband path. Optimizing only $A$ does provide meaningful linearization up to 200 MHz before the timing requirements become too stringent and linearity degradation is observed. Optimizing only $\tau$ provides some linearity improvement at the higher tone spacings and matches the fully optimized case at $\sim$ 450 MHz. Finally, constant values of $\tau$ and $A$ are used to evaluate how a fully integrated system with limited reconfigurability might perform. The fixed values of $\tau$ and $A$ are chosen to be the mean of the optimized values across bandwidth. This fully constant case generally demonstrates $IMD_3$ degradation across tone spacing, with a $\sim$ 5 dB improvement at 600 MHz. This demonstrates a need for dynamically adjusting $A$ and reducing dispersion in the baseband envelope path.

Aside from being able to linearize signals with wide IBWs, gate modulation also has the

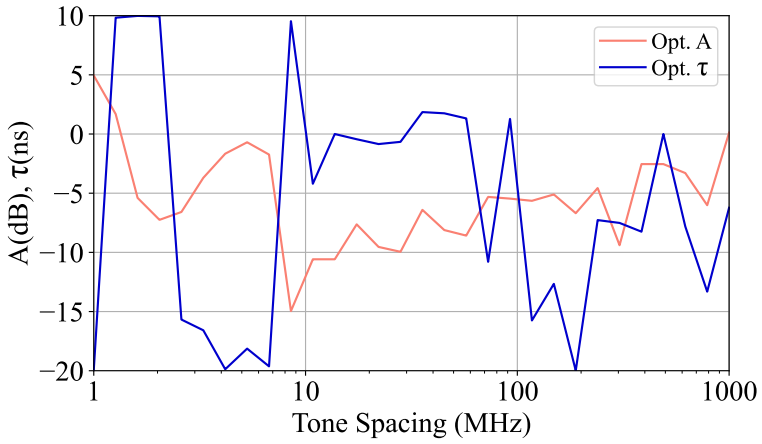
Table 3.2: Summary of recent analog linearizers

| Ref. | Signal BW (MHz) | Linearity Improvement (dB) | Loss (dB) | $P_{dc}$ (mW) |
|---|---|---|---|---|
| [108] | 20 | $7.2 - 12.9^{\star}$ | 6-9 | 200 |
| [77] | 0.01-200 | $20 - 24^{\triangle}$ | 1.5-10 | 9 |
| [87] | 50 | $7.3 - 9.6^{\square}$ | 9 | 0 |
| [13] | 750 | $4.5 - 9.8^{\star}$ | 3-8 | NR |
| [This Work] | 10-1000 | $4.3 - 17.7^{\triangle}$ | 2.25 | 307 |
| [This Work] | 100 | $3.2^{\star}$ | 2.25 | 307 |

$\star$: ACPR, $\triangle$: $IMD_3$, $\square$: ACPR for Doherty PA




(a)




(b)

Figure 3.21: (a) Measured two-tone $IMD_3$ suppression over bandwidth with the (dashed) static case and (solid) dynamic case at a $P_{in,pk}$=10 dBm. The $IMD_3$ high and low tones are shown in black and red, respectively. (b) The corresponding $\tau, A$ coefficients to obtain the results in (a). The constraints on $A$ for optimization are [-15,5] dB and $\tau$ [-20,10] ns.

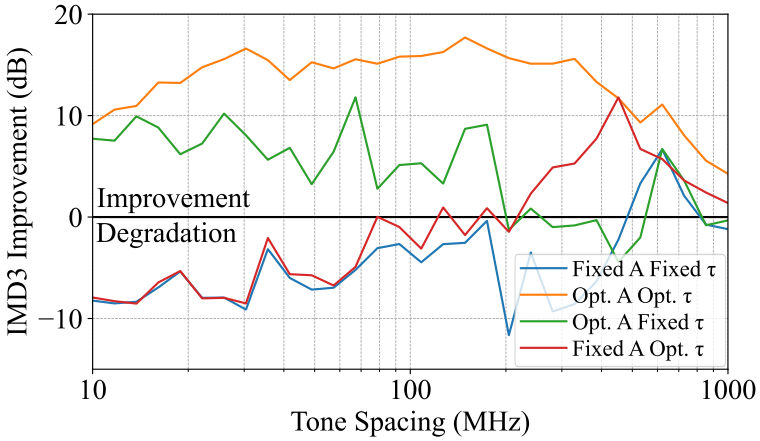


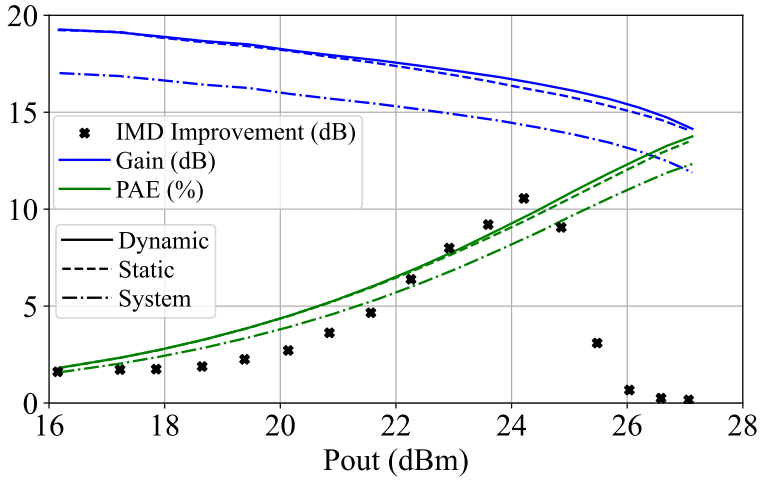

Figure 3.22: Measured $IMD_3$ improvement/degradation when (orange) both $\tau$ and $A$ are optimized, (green) only $A$ is optimized, (red) only $\tau$, and (blue) static $\tau$ and $A$, at a $P_{in,pk}$=10 dBm.

potential to minimally impact other system metrics such as PAE and gain. To investigate this, a two-tone with 500 MHz tone spacing is used, and $P_{in,pk}$ is swept from 0-16 dBm. Fig. 3.23a shows the system-level performance with a fixed $\tau, A$ across $P_{in}$. The $\tau$ value remains constant across power levels; however, the $A$ should be varied to maintain optimal linearization. In the unoptimized case, the $A$ value is taken as the mean value across power. The gain and PAE with the baseband path biased, demarcated with dashed lines, are marginally higher at all points when compared to the static case, which is demarcated with solid lines. The composite case is also shown (dash-dotted traces) which includes the power consumption of the diode detector and the baseband amplifier, as well as 2.3 dB of input-referred loss from the through path of the envelope detector. The composite system gain reflects the 2.25 dB of input loss, and the PAE is $\sim$ 2 pp lower at peak output power due to both the lower gain and the higher power consumption.

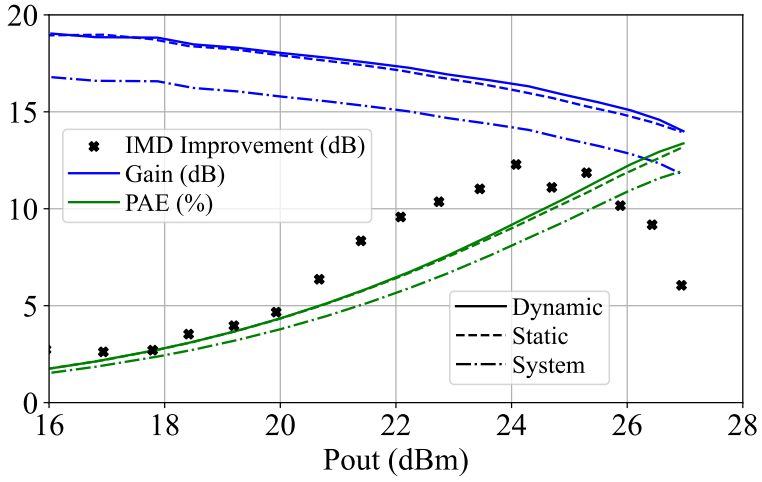
The system performance is also measured with $A$ optimized at each power level to maximize the linearization performance, seen in Fig. 3.23b. The dynamic and composite system gain and PAE are essentially unchanged when compared to the unoptimized case.

The average high and low $IMD_3$ improvement in the unoptimized case reaches a peak value of 11 dB at $\overline{P_{out}} \sim$ 24.3 dBm with a greater than 5 dB improvement from $\overline{P_{out}}$= 22–25 dBm. The

optimized case has a slightly higher peak $IMD_3$ improvement of $\sim 13\,dB$ and is able to maintain more than 10 dB improvement for $\overline{P_{out}} = 23$–$26\,dBm$. This demonstrates that a static amplitude offset can be used for applications where $\overline{P_{out}}$ levels are expected to remain fairly constant. In systems with more variable requirements, a baseband amplifier can be used to set $A$ to maximize linearity for a given $\overline{P_{out}}$.




(a)




(b)

Figure 3.23: Measured system performance (PAE, gain, $IMD_3$) over $\overline{P_{out}}$ for a 500 MHz two-tone signal. The (a) fixed case is without amplitude optimization at each power level, and the (b) optimized case is with $A$ optimization at each point.

### 3.6.2 ACPR and EVM

Two-tone measurements are both well known and desirable for quantifying how well the detector system performs across baseband frequencies, due to the single envelope frequency component. However, modern communications signals have significantly different statistical distributions compared to two-tone, as well as multi-spectral frequency components. To that end, the 3GPP "NR-FR2-TM3.1a" 100 MHz 256 QAM signal 5G FR2 test model signal is generated in MATLAB and used to evaluate the system's linearization potential.

As with the previous two-tone measurements, we optimize the $\tau$ and $A$ offsets between the RF signals to the PA and the envelope detector to minimize the ACPR. The measured spectrum with and without the gate-modulation linearizer turned on can be seen in Fig. 3.24 at $P_{in,pk}$=11 dBm. The linearized system demonstrates a modest ACPR improvement of 3.2 dB. $\overline{P_{out}}$ is essentially unaffected at 20.3 dBm, and the composite PAE is 3.9 %, representing a 0.5 pp degradation with the gate-tracking applied. A comparison of the linearization of this work and recent APD literature is shown in Table 3.6.1 for two-tone $IMD_3$ and wideband ACPR results.

The degradation in linearization performance with the 5G signal ACPR compared to two-tone $IMD_3$ at the same bandwidth is due to multiple factors, listed below.

- The baseband path has significant amplitude and phase variation across bandwidth (Fig. 3.11), which is disadvantageous for a signal with many baseband spectral components.
- The PAPR of the 5G signal (10.6 dB) is much higher than the PAPR of a two-tone, which is 3 dB.. The dynamic range of the diode bridge may be insufficient. This can be seen in Fig. 3.12, where the detector's response is generally more accurate for the signal peaks compared to the lower amplitude components.

Error vector magnitude (EVM) is perhaps the most demanding and important linearity metric for a communications signal, as it directly relates to the bit error rate (BER) in a noiseless channel. The linearization ability of the system with regard to EVM is evaluated with the 5G signal described above. Because the baseband in-phase quadrature (IQ) data of the signal is generated

and demodulated in the Matlab 5G toolbox application, there is no way to directly optimize for EVM. Instead, the $\tau$ and $A$, which were previously found to minimize ACPR, are used. The resulting EVM with and without linearization is presented in Table 3.3, which demonstrates a small, yet measurable improvement to EVM with the baseband path turned on, for $P_{in,pk}$ values from 9–13 dBm.

At input powers beyond 13 dBm, EVM is degraded by the linearization system. Fig. 3.25, which shows the normalized instantaneous gain magnitude and phase responses, with the 5G signal at $P_{in,pk}$=11 dBm, explains the discrepancy between linearization quantified as EVM and as ACPR. Both the *average* gain magnitude and phase, shown with solid lines, are significantly flattened when the gate modulation is applied. The gain magnitude variation is improved from ∼2.5 dB to ∼1.25 dB, and the phase from ∼ 10° to ∼ 3°. However, the gate modulation increases the spread in the gain magnitude and phase at any *instantaneous* input amplitude. For example, at a relative amplitude of 0.4 V, the variation in gain magnitude increases from ∼ 1 dB to ∼ 1.25 dB, and the phase variation increases from ∼ 5° to ∼ 10°. The gate modulator is providing some linearization improvement on average while also increasing the instantaneous variation, due to dispersion and distortion in the envelope path.

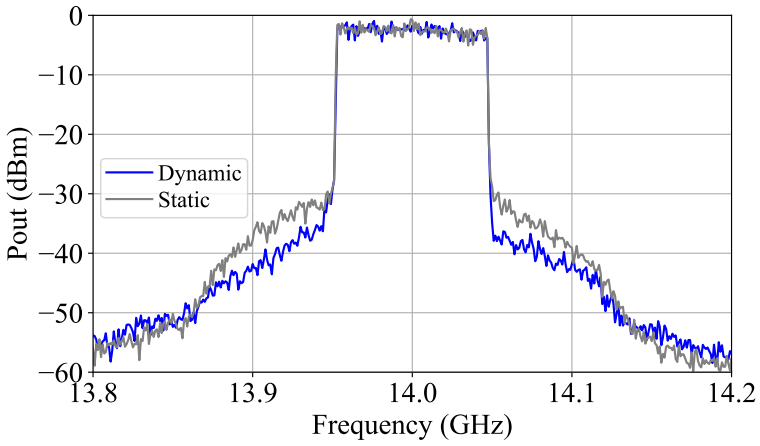
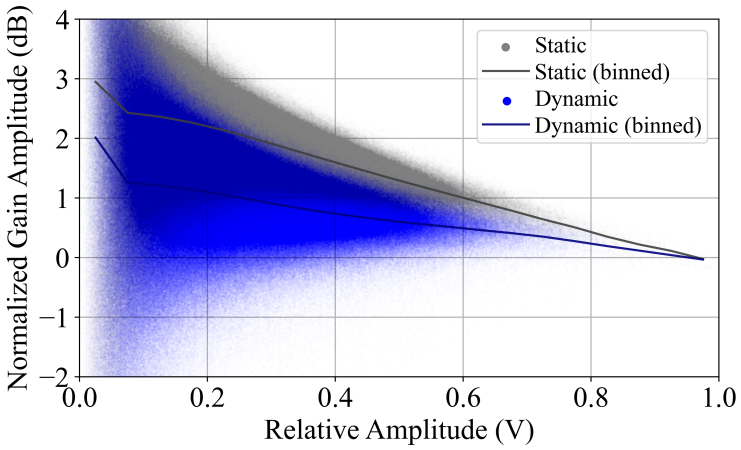


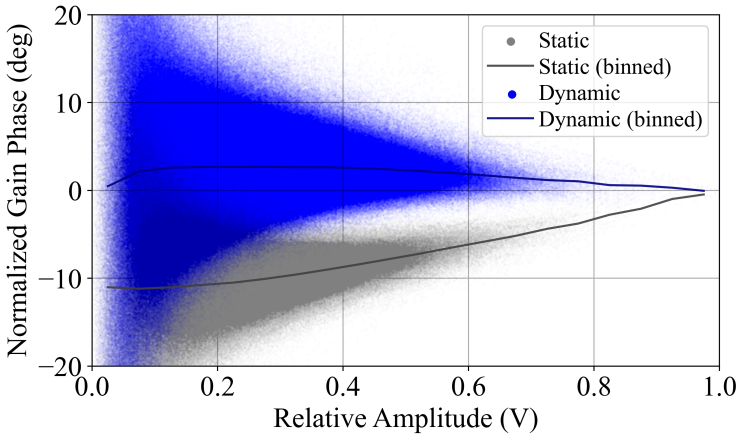

Figure 3.24: Measured ACPR improvement with a 100 MHz 5G signal at a $P_{in,pk}$=11 dBm for the (gray) static case and (blue) with gate-modulation applied.

Table 3.3: Measured EVM for a 100 MHz 5G signal with and without dynamic gate modulation.

| $P_{in,pk}$ (dBm) | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|
| EVM Dyn.(%) | 4.29 | 4.89 | 5.57 | 6.27 | 6.57 | 9.51 | 9.28 |
| EVM Stat.(%) | 4.5 | 5.2 | 5.68 | 6.25 | 6.66 | 7.41 | 8.17 |




(a)




(b)

Figure 3.25: AM-AM and AM-PM for a 100 MHz 5G signal for the (gray) static case and (blue) with gate-modulation applied at a $P_{in,pk}$=11 dBm.

## 3.7 Conclusion

This work demonstrates a fully integrated, analog gate-modulated linearization system for wideband Ku-band power amplifiers. To the best of the authors' knowledge, this is the first implementation of single-gate analog linearization in a multi-stage GaN amplifier architecture, as well

as the widest-reported IBW envelope detector specifically designed for wideband analog linearization. The architecture consists of two custom-designed and characterized MMICs: a GaN-on-SiC PA covering 11.5–16 GHz and a GaAs envelope detector and gate modulator operating across all of Ku-band. The PA achieves PAE > 30 % and $P_{out} > 35$ dBm across the band, while the gate modulator exhibits 2.25 dB RF through-path loss and supports envelope detection up to 1 GHz instantaneous bandwidth.

Envelope-domain simulation using a 100 MHz, 300-tone signal predicts up to 9 dB of ACPR improvement with the measured detector response. Experimental measurements verify linearization of third-order intermodulation distortion ($IMD_3$) across 10 MHz–1 GHz bandwidth, achieving a 17.7 dB reduction at 150 MHz tone spacing. With a 100 MHz 5G NR signal, the measured ACPR improves by 3.22 dB to –33.81 dBc. Other system metrics remain largely unaffected by gate modulation: gain is reduced by 2.25 dB due to the modulator insertion loss, and overall PAE decreases by approximately 2 pp. However, for wideband modulated signals, dispersion and distortion in the baseband path significantly degrade the achievable linearization, limiting performance relative to the 2-tone and simulated results. Even so, the overall system demonstrates the underlying potential of single-gate tracking with minimal loss and hardware complexity.

A key advantage of the proposed architecture is its reconfigurability. Because the gate modulator operates independently of the RF path, the system can be adapted across output power levels without retuning the amplifier. Two-tone measurements demonstrate that the gate control path can be adjusted to optimize linearization performance dynamically while maintaining RF performance across $\overline{P_{Avs}}$.

In an iteration of the baseband topology with low group delay, a fixed delay line could be used along with a VGA to tune the amplitude response to the desired $\overline{P_{out}}$. Additional future work will focus on incorporating a feedback mechanism to maximize the linearization potential of the system across varying operating conditions, including temperature and process variation. An additional topic would be to investigate the tradeoffs of single-gate tracking of the $N^{th}$ stage of a multi-stage PA.

# Chapter 4

# Multi-tone signals for Nonlinear Power Amplifier Characterization

## 4.1 Introduction

While it is well known that PAs are commonly operated under highly dynamic conditions, the PA design process is still predominantly based on static performance. Classical amplifier theory, such as that related to amplifier classes of operation and load-line based design, assumes constant operating conditions [26]. Many nonlinear models do not support dynamic effects over a wide range of time constants [95], although recent research efforts extend model capabilities, e.g. [97,110]. The model limitations are partly due to the difficulty of accurately simulating the thermal conditions of the operating PA [54]. Furthermore, standard harmonic balance methods are inefficient with broadband RF excitation, and a hybrid harmonic balance and time-domain envelope simulation is typically required. These limitations result in uncertainty regarding how well the PA is designed for dynamic operation until the testing phase.

In this chapter, we investigate the behavior of GaN microwave power transistors when excited with modulated signals, using the passive load pull setup illustrated in the block diagram of Fig. 4.1. load pull under modulated conditions has the potential to give useful information related to device behavior beyond single-sinusoid CW performance. Previously published results used active load pull systems to characterize transistors under signal excitation [2,3,18,39,68]

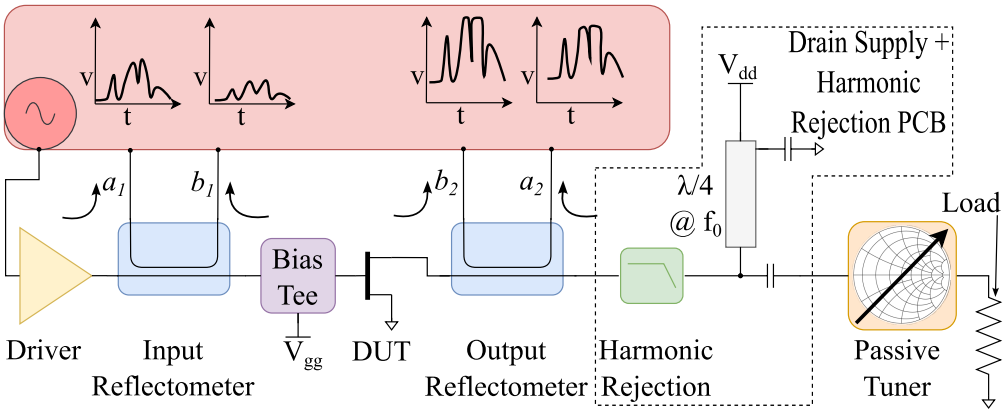



Figure 4.1: Block diagram of the vector passive load pull system

## 4.2 Description of Experimental Setup

Two devices are measured with the setup: device-under-test (DUT) A is a packaged GaN transistor, while DUT B is a wire-bonded GaN die. This section describes the passive load pull system and the relative and absolute calibration methodologies used.

The load pull analysis is performed using a large-signal measurement system. This system utilizes four NI PXIe-5840 vector signal transceivers (VSTs) with directional couplers as shown in Fig. 4.2. The system allows for vector measurements of the incident ($a_n$) and reflected ($b_n$) waves coming into and out of the PA at both the input and output. Here $n = 1, 2$ and refers to the port number. This system can be viewed as a large-signal Vector Network Analyzer (LSNA) with a wide instantaneous bandwidth of 500 MHz at $f_0$=2 GHz [112]. The $f_0$ is chosen to facilitate a future inclusion of the full waveform, including up to the third harmonic at 6 GHz, which is the highest frequency the 5840 VST supports. The VSG modulated output drives a Mini-Circuits ZVE-3W-83+ driver amplifier, while a Focus Microwave CCMT 1816 fundamental-frequency load pull tuner is connected at the output following couplers and a harmonic termination network and drain bias tee.

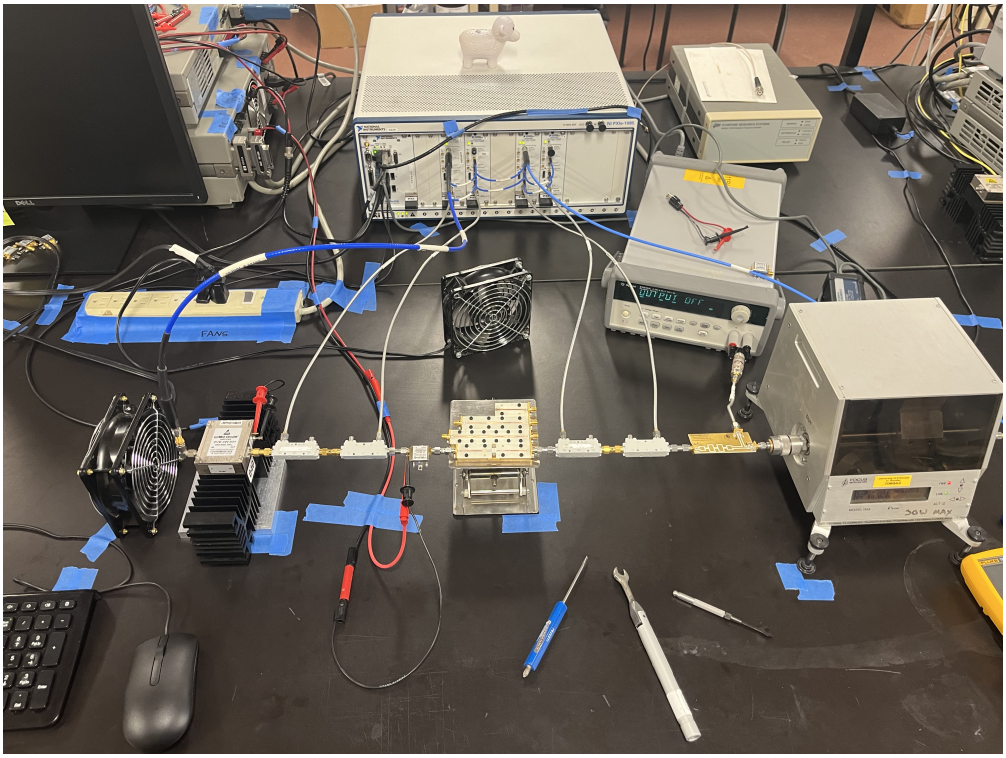


Figure 4.2: Photograph of the measurement system with the corresponding block diagram shown in Fig. 4.1. The PXI-e chassis is shown in the background with 4 5840-VSTs for sampling the $a$ and $b$ waves at the input and output of the DUT. The driver amplifier and input reflectometer are shown on the left. The DUT and TRL standards are shown in the center of the image. The output reflectometer, bias and harmonic trap PCB, and load-tuner are shown cascaded on the right. Note that the drain bias is supplied to the bias board through a short section of coaxial cable to minimize inductance.

### 4.2.1 Device Selection

To determine the impact of modulation on the performance and target load impedances of GaN-on-SiC microwave transistors, two commercial transistors are chosen. The goal is not to compare the performance between the two manufacturers but rather to identify commonalities and differences between modulated and CW load pull. The devices chosen are the MACOM CG2H4006P (DUT A) and the Qorvo TGF-2023-02-01 (DUT B). Both are marketed as 6 W devices and are fabricated in GaN-on-SiC processes, with a $V_{dd,max} = 28\,V$ for DUT A and $V_{dd,max} = 32\,V$ for DUT B. DUT A is packaged in a ceramic-pill package with flanges for soldering directly to a PCB and has a recommended maximum operating frequency of 6 GHz. DUT B is an unpackaged

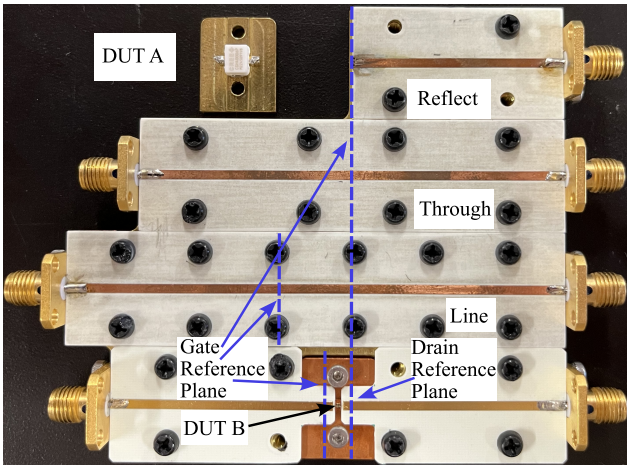



Figure 4.3: TRL standard and DUT mounting fixture. The *reflect* standard is in the top right, a non-zero length *through* is the next lowest standard, and finally, the *line* standard is third from the top. DUT B is shown in the bottom center, mounted onto a copper pedestal. DUT A is shown in the top left. Note that due to the smaller size of DUT B, as well as the difficulty of de-embedding bond wires, the reference plane lies slightly outside of the DUT.

MMIC transistor with pads at the gate and drain for wire-bonding to a PCB and has a maximum recommended operating frequency of 18 GHz. DUT A is soldered to a brass carrier, and DUT B is attached with silver epoxy to a copper base. As shown in Fig.4.3, both bases are then mechanically attached to a single brass carrier for the devices and the TRL calibration standards.

### 4.2.2 Calibration

The simplest load pull experimental setup is scalar and utilizes directional couplers and power meters to measure the input and output power of the DUT and a pre-characterized passive tuner to change the load impedance seen by the DUT. This method has limited accuracy and flexibility. Namely, this type of load pull system must have all components after the load of the DUT pre-characterized on a VNA, including the tuner. A mapping that relates the tuner slug's physical position to the synthesized impedance must be created; repeatability is influenced by the precise positioning of the slug and environmental changes, and accuracy is limited by the reflection coefficient of the load placed after the tuner. A better method is to use a vector-calibrated system,

which is capable of measuring the $a, b$ waves at the gate and drain of the DUT. This allows for the impedance presented by the tuner to be measured directly in situ across frequency and has the additional advantage of flexibility in choosing power or transducer gain definitions.

The VST system is calibrated using a standard TRL calibration kit, Fig. 4.3, to calibrate to the device planes and establish the relative relationships between the measured $a, b$ waves. An additional 1-port SOL calibration is performed after the output couplers to provide an auxiliary connectorized reference plane for the absolute calibrations. One of the VSTs is configured to behave as a comb generator, and its output is placed at the auxiliary reference plane to establish phase coherence between the receivers. A power meter is then placed at the auxiliary plane to calibrate the absolute power levels measured by the system. With this approach, the system can be fully calibrated to the transistor planes.

The calibration allows for establishing reference planes at the package plane of DUT A. However, as seen in Fig. 4.3, DUT B is an unpackaged MMIC and shorter in length; this creates a slight offset in the reference plane compared to the drain of the DUT. Additionally, the gate and drain must be wire-bonded, which introduces an additional shift of the reference plane. While this creates minor disagreement with the model, it does not affect the conclusions because all modulated results are compared against measured CW performance. The dc reference plane must

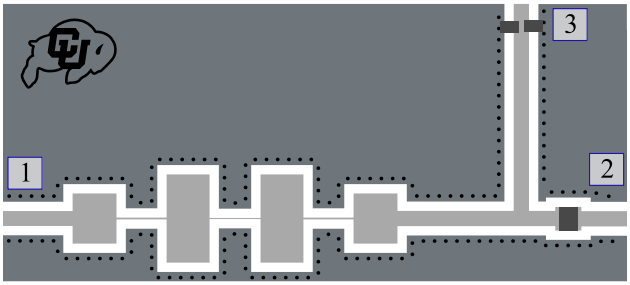



Figure 4.4: Diagram of the harmonic trap and bias-tee board. The stepped impedance lowpass filter is the left-most structure. The stub is $\frac{\lambda}{4}$ at 2 GHz and shorted with two 20 pF 0805 capacitors in parallel to present an open at the fundamental. The dc block is similarly implemented with two parallel 20 pF capacitors. The top metal in dark gray is shorted to the ground plane using a via fence, which is shown in black.

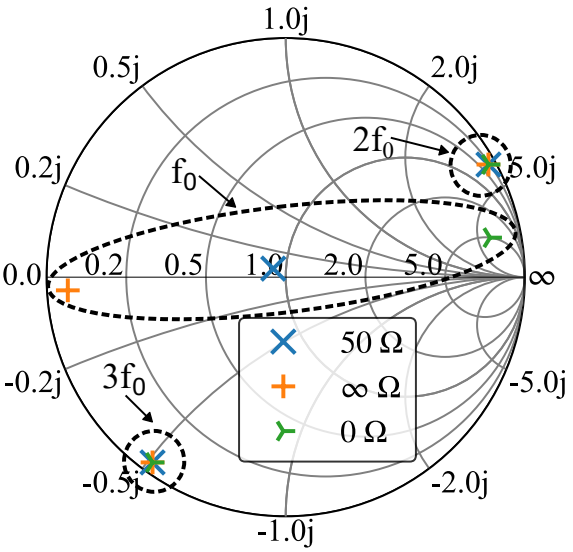
also be shifted to the device plane. For the gate, it is assumed that the current draw is negligible, and the raw voltages and currents from the meter are used. For the drain, however, an ohmmeter is used to determine a dc resistance of $4\,\Omega$ between the output of the power supply and the PCB launcher near the device plane. We assume that the shunt current is minimal and use the dc resistance value to calculate the voltage drop along the drain bias network. The drop is then subtracted from the nominal supply voltage to obtain the dc voltage at the drain reference plane.

## 4.3 Transistor Pre-Characterization

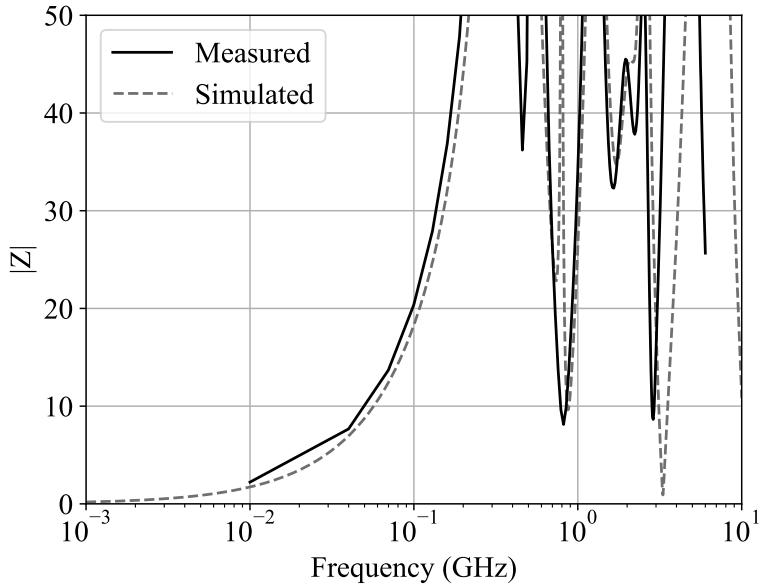
The first step is to pre-characterize the device under CW excitation, which provides validation of the experimental setup and the nonlinear models. For the ultimate goal of characterization under modulated signal excitation, it is also important to have the knowledge and/or control of the baseband and harmonic-frequency impedances presented to the device.

### 4.3.1 Harmonic Impedance Control

A limitation of single-slug, fundamental-only load tuners is that the impedance presented at the harmonics is not constant as the fundamental impedance is swept. This can have a significant effect on the results as the load pull contours and maximum value points will be dependent on the fundamental impedance as well as N harmonic impedances, where N is the highest harmonic supported by both the load pull system and the DUT [37]. It is therefore desirable to isolate the harmonic impedances from the tuner. In this analysis, a stepped-impedance low-pass filter, shown in Fig.4.4, is used to provide a high $\Gamma_L$ at the harmonics with negligible influence from the load impedance, similar to the approach taken in [48]. Fig.4.5a shows the measured $\Gamma_{\text{in}}$ of the filter PCB at $f_0$, $2f_0$, and $3f_0$. The measured $\Gamma_{\text{in}}$ is then cascaded with an ideal short and open at the output. As desired, the fundamental impedance is strongly affected by the loading impedance, while the harmonics are unaffected. Note that no attempt is made to terminate the harmonics in any specific impedance.

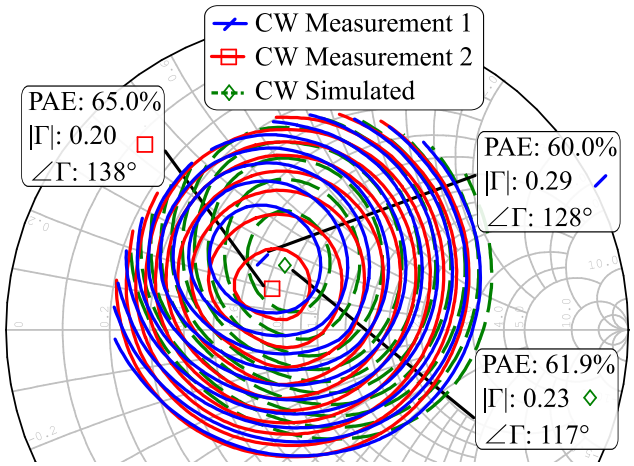



(a)

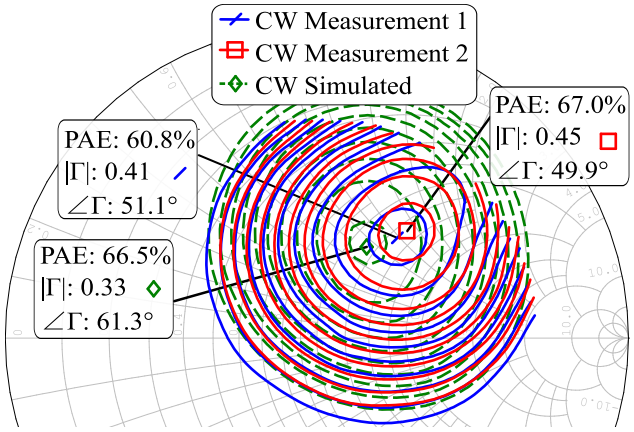



(b)

Figure 4.5: Measured fundamental, as well as 2nd and 3rd harmonic reflection coefficients looking into port one of the filter and bias tee board, when terminated in a broadband short, open, and 50 Ω load. The measurement is taken by capturing the 3-port $S$-parameters for the bias tee with $Z_{ref} = 50\,\Omega$. (a) The s-parameters are then cascaded with an ideal short and open at port 2 in post-processing. (b) The simulated and measured input impedance of the bias-tee demonstrates good agreement between measurement and simulation and a baseband impedance below 10 Ω up to 57 MHz.




(a)




(b)

Figure 4.6: Validation of the load pull system for DUT A (a) and DUT B (b). PAE contours as well as maximum values for two measurements are shown and compared with a load pull simulation using the nonlinear model.

### 4.3.2 Baseband Impedance Control

While designing a wide-bandwidth PA is mainly determined by creating a higher-order matching network for the desired range of carrier frequencies, enabling wide instantaneous, or video, bandwidth for an amplifier is largely a function of the baseband impedances presented to the transistor. Namely, a high baseband impedance at the drain will cause a voltage drop along the bias line, which reduces the power available to the transistor and therefore both system output power and efficiency. Additionally, linearity is significantly affected by the presented baseband drain impedance [11]. It has also been suggested in [6] that the baseband impedances presented to the

gate also affect performance under time-varying stimulus.

We therefore set out to design a bias circuit that presents a low impedance up to the maximum baseband frequencies, which is used for characterization. For the analysis herein, this bias tee is only used at the drain, and a commercial bias tee is used at the gate. A typical $Z_c = 50\,\Omega$ $\frac{\lambda}{4}$ shunt stub is shorted with 2 parallel ATC 600F 20 pF capacitors to present an open circuit at $f_0$ and a low impedance at baseband, seen in Fig.4.4. As demonstrated in [84], the $\frac{\lambda}{4}$ shorted stub topology is not an optimal solution for achieving broad baseband terminations. However, this topology is sufficient since the measurement bandwidth is primarily limited by the passive tuner. The bias line is connected via a $50\,\Omega$ coaxial cable to the drain supply to better control the response of the circuit in the measurement setup. With this configuration, the baseband impedance presented at the drain of the device is effectively controlled and kept below $10\,\Omega$ up to 57 MHz. This conclusion follows from Fig.4.5b showing the complex impedance for the bias-tee circuit.

### 4.3.3 CW load pull Response and Model Comparison

It is important to validate that the device mounting and reference planes are correct. CW load pull provides an excellent validation point as it requires accurate relative and absolute calibration, as well as a consistently mounted and biased device to achieve agreement with the nonlinear model. To accurately replicate the experimental conditions in simulation, the test bench is first excited from port 1 ($a_1$), and the $(a_2, b_2)$ waves are measured at 4 and 6 GHz to determine the in-situ harmonic load impedances presented to the DUT. The corresponding $\Gamma_L$ values are then set fixed in the load pull simulations where only the fundamental impedance is swept. As seen in Fig. 4.6, the PAE contours and maximum values for DUT A and B align very closely. Two measurements are presented that demonstrate a high degree of repeatability for the experimental setup. The largest deviation between measurement and simulation is -5.7 percentage points (pp) and 3.1pp for DUT A and B, respectively. Additionally, the largest difference between simulation and measurement for DUT A is $\Delta\Gamma_L = |0.06|\angle 11°$, and for DUT B, $\Delta\Gamma_L = |0.12|\angle -11.4°$. These measurements demonstrate that the relative and absolute calibrations are correct and the devices are performing

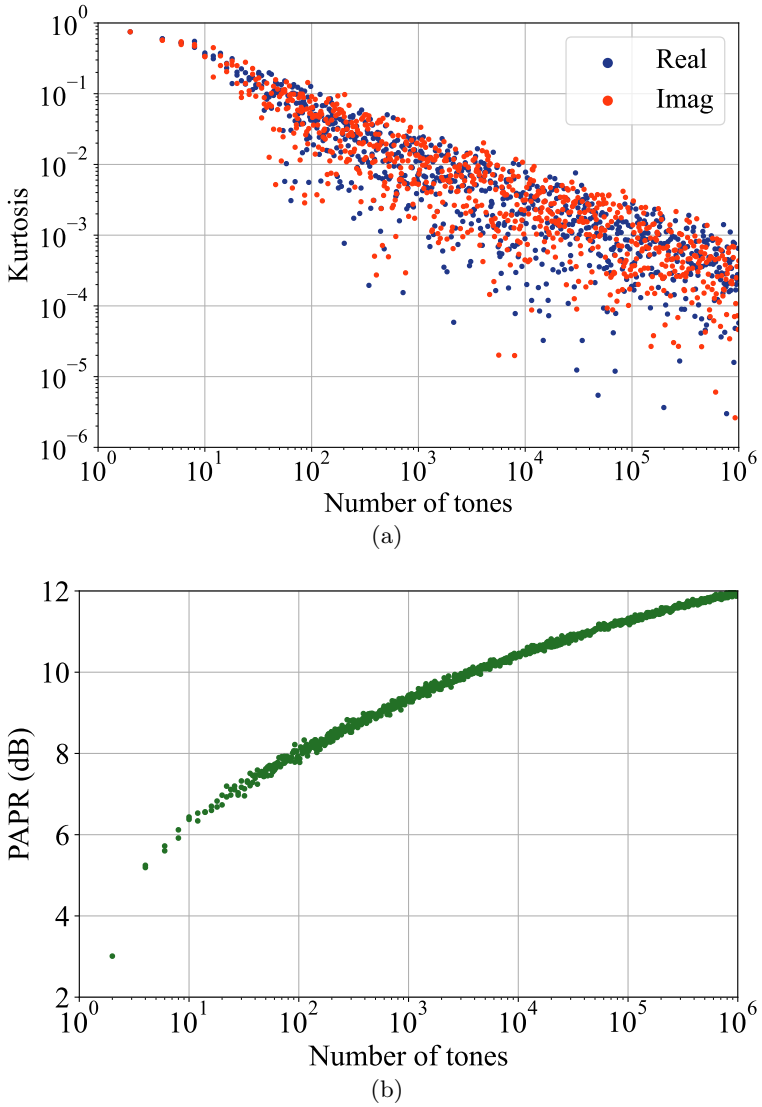



Figure 4.7: Excess kurtosis, used as a metric of normality for the real and imaginary components of the signal, plotted over the number of tones in a random-phased, equal-amplitude, multi-tone signal (a). PAPR plotted over the number of tones (b).

as predicted by the models.

## 4.4 Signal Generation

In this section, we present an analysis of the viability of using random-phased multi-tone signals to mimic the signal statistics of a modern OFDM-like communications protocol signal. Signal standards are rapidly changing, which makes comparison difficult from a hardware test

perspective, in that the output voltage is dependent on both the modulation standard and the bit sequence used. For reproducible results, we use multi-tone signals which are completely specified by their random phases and amplitudes. Neither the center frequency nor the tone spacing affects the theoretical signal statistics. The amplitudes can also be assumed to be equal with little loss of generality. NPR test signals are a well-known application of a standard-independent test signal with relevant statistical properties.

As outlined in [100], a modulation that maximizes information transfer for a given bandwidth has the statistical properties of band-limited Gaussian white noise. In [86], it is shown that the real and imaginary components of white noise are Gaussian in distribution, and the envelope magnitude will have a Rayleigh distribution. This demonstrates that the instantaneous power statistical distribution of a modulated signal should be Rayleigh in distribution.

We desire to synthesize a standard-agnostic multi-tone signal that closely mimics the statistical properties of an OFDM-like signal. To determine how many random-phased, equal-amplitude tones are necessary to effectively represent band-limited Gaussian white noise, we generate random phased multi-tones with N tones ranging from 2 to 1 million, in 1000 logarithmically spaced steps. Because the statistical properties of the signal are dependent on the random phases, for each number of tones, N, we generate M=1000 signals to determine an average response. For each N, M, the PAPR, and excess kurtosis ($K_e$) of the real and imaginary components are recorded. Excess kurtosis is a statistical quantity that describes the tails of a distribution compared to a standard distribution [17]. Therefore, the $K_e$ of the real and imaginary components can be used as a metric to compare how close the components of a multi-tone signal resemble a Gaussian distribution. At the limit where $K_e \rightarrow 0$, the real and imaginary components have a perfectly Gaussian distribution, and therefore the magnitude of the signal is Rayleigh distributed. The $K_e$ for the real and imaginary components of the averaged N-tone multi-tones can be seen in Fig.4.7a. The $K_e$ drops exponentially as the number of tones is increased. An acceptable level of $K_e$ is difficult to quantify, and a value less than 0.1 is chosen for this analysis, and 300-tone multi-tones are used to represent an arbitrary modulation.

By looking at kurtosis over the number of tones, it is apparent that only:

$$\lim_{N\to\infty} K_e \to 0.$$

This implies that an ideal modulation requires an infinite number of tones. However, as seen in Fig.4.7b, it is evident that the PAPR also increases monotonically with N. An ideal modulation would therefore have an infinitely high PAPR.

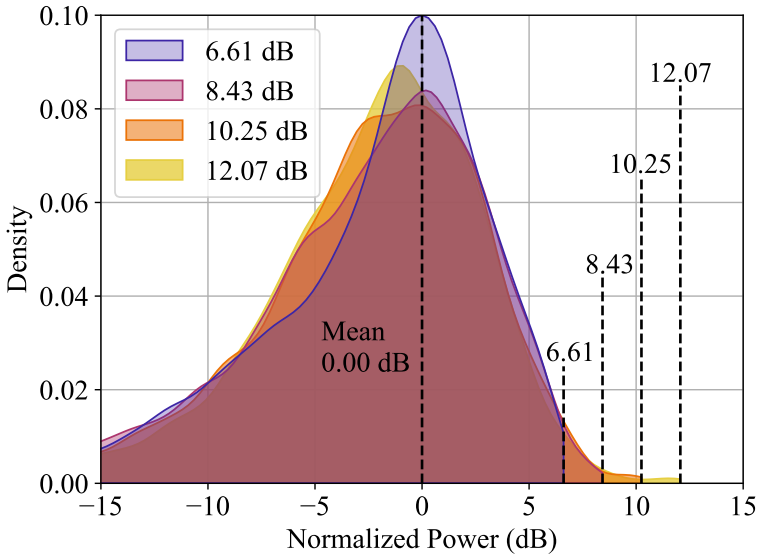



Figure 4.8: Instantaneous power distributions for four of the multi-tone test signals used herein. Each signal is normalized to have a mean power of 0 dB, and the peaks are demarcated by dashed lines.

## 4.5 Modulated Transistor Characterization

The CW characterization is used to validate the load pull system and the calibration, as well as to provide reference values for comparison to the modulated measurements outlined in this section. To investigate the effect that PAPR and bandwidth have on HEMT modulated performance, two experimental procedures are created. The first utilizes the multi-tone test signals described above. Different sets of random phases for the same number of tones can yield different signal statistics and therefore different PAPRs. This allows us to test the effect that the signal probability density function (PDF) has on performance while keeping the number of tones, tone-spacing, and hence

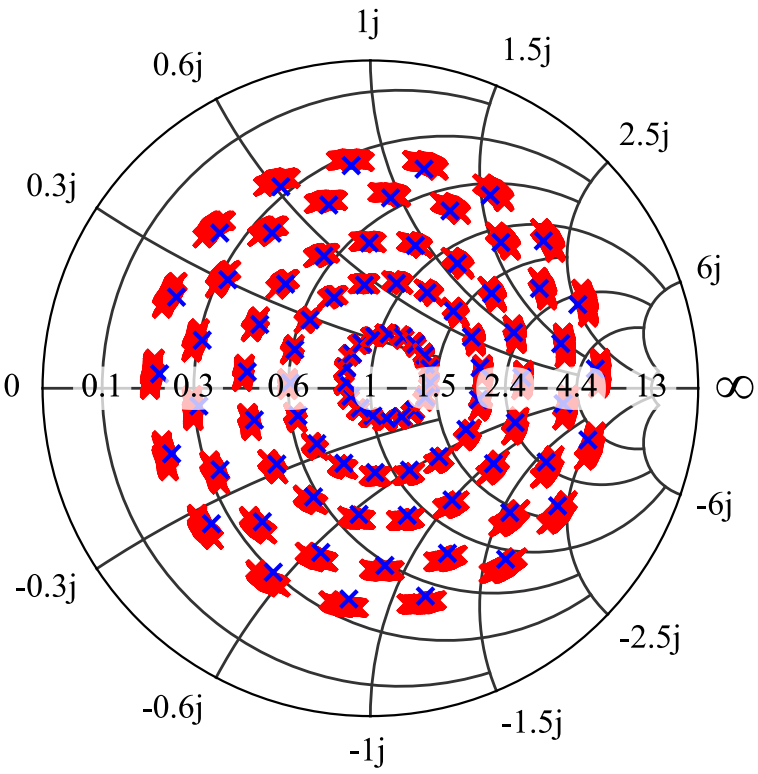


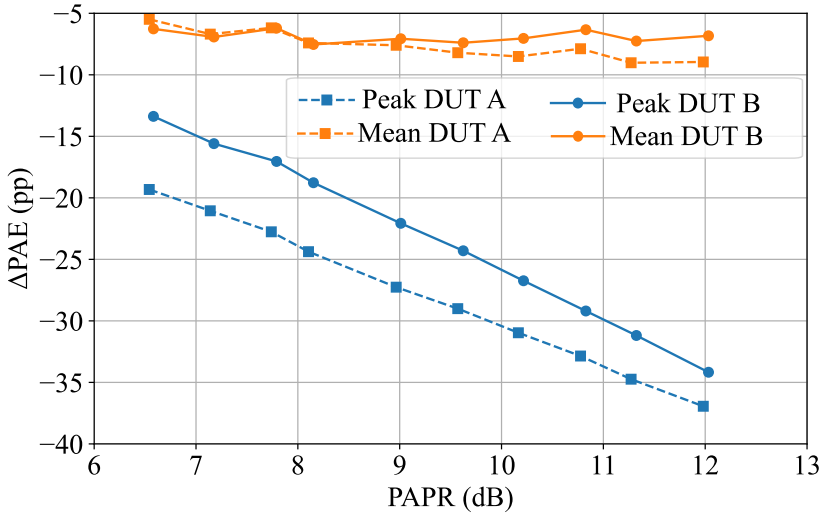

Figure 4.9: Measured 2 GHz CW load-impedances (blue) and the impedances across the 6.18 MHz bandwidth of the 300-tone test signals (red), illustrating the phase skew of the passive tuner over a relatively narrow bandwidth.

bandwidth constant. To investigate the full range of achievable statistics with the same number of tones, we generate 10,000, 300-tone multi-tones with different random phases and equal amplitude. We then sort the generated signals by PAPR and select 10 sets of random phases equally spaced across the achievable range. The chosen PAPRs of the 6.18 MHz 300-tone random phased NPR test signals shown in Fig.4.8 are: $\{6.6, 7.2, 7.8, 8.4, 9.0, 9.6, 10.3, 10.9, 11.5, 12.1\}$ dB.

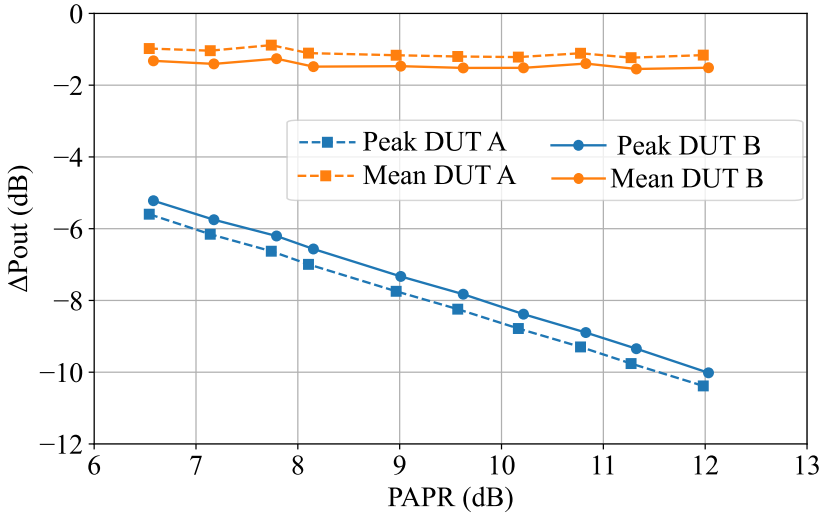
The second experimental procedure seeks to isolate the effect that bandwidth has on modulated performance. To achieve this, the bandwidth of a 2-tone signal, with a constant PAPR of 3 dB is swept from 20 kHz to 10.24 MHz in 10 logarithmic steps as:
$\{20, 40, 80, 160, 320, 640, 1280, 2560, 5120, 10240\}$ kHz.

While the LSNA is capable of supporting bandwidths up to 500 MHz at $f_0$=2 GHz, any passive tuner has an inherently low instantaneous bandwidth. As seen in Fig.4.9, the tuner presents

different impedances across the bandwidth of a signal. This phenomenon is known as *phase skew* and presents a significant challenge to performing wideband load pull measurements with a passive tuner.

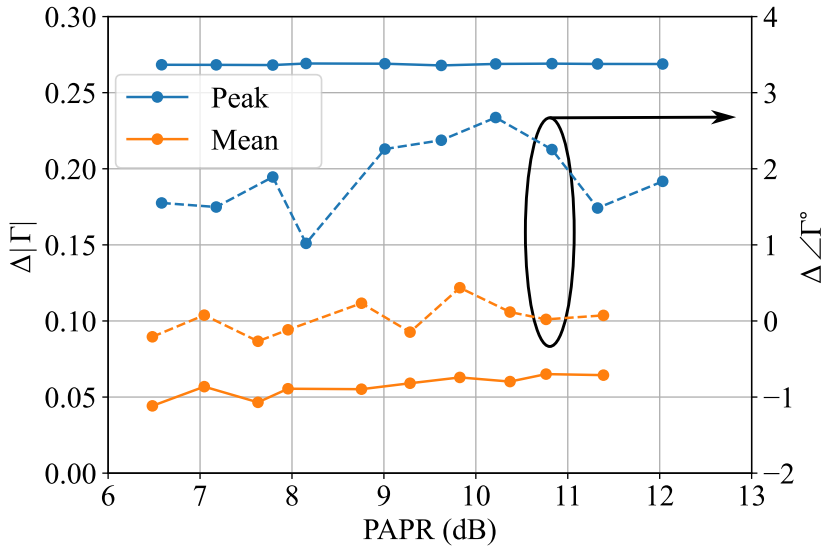



(a)

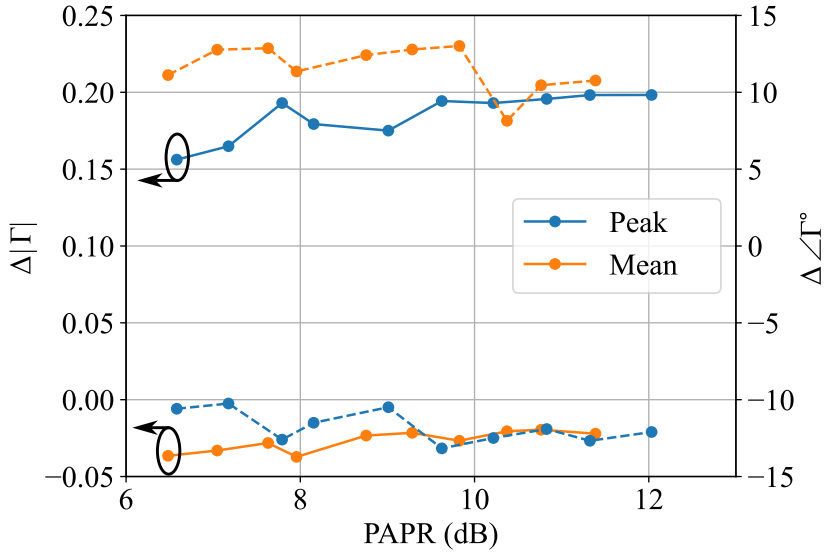



(b)

Figure 4.10: Difference in maximum PAE (a), $P_{out}$ (b) between CW and modulated excitation, where peak power is held constant (blue) or where average power is held constant (orange). This difference is plotted as a function of the PAPR of the modulation signal.




(a)




(b)

Figure 4.11: Difference in $|\Gamma_L|$ and $\angle\Gamma_L$ for PAE (a), $P_{out}$ (b) between CW and modulated excitation, where peak power is held constant (blue) or where average power is held constant (orange). This difference is plotted as a function of the PAPR of the modulation signal. Results are shown for DUT B.

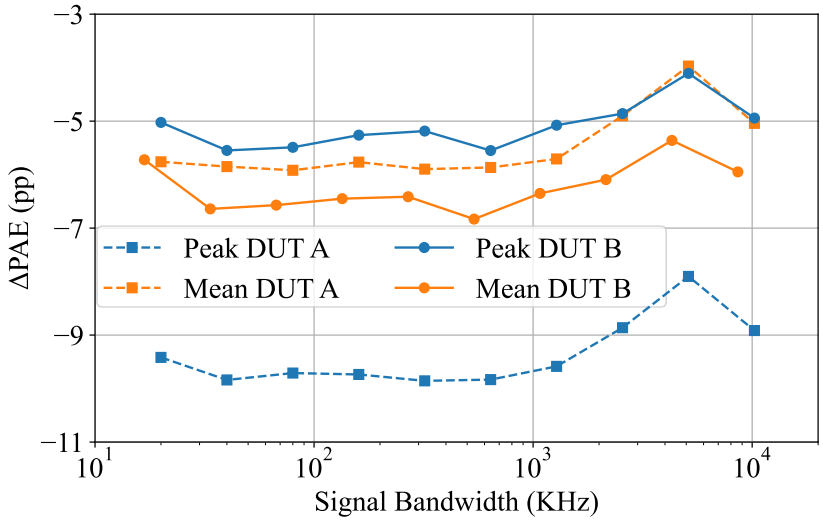
### 4.5.1 Varying PAPR

It is not immediately obvious how the PAPR of a signal will affect a transistor's performance. For example, it seems intuitive that the average power will dictate average performance metrics such as PAE and $P_{out}$. However, as seen in Fig.4.8, the mean power is significantly different from

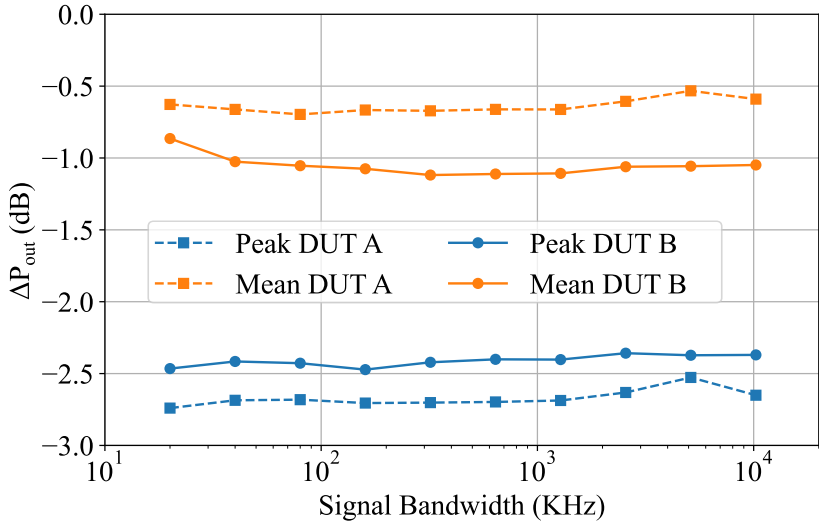
the mode and median power due to the skewness of the Rayleigh distribution. Additionally, while the peak power has a very low probability of occurring, it seems feasible that the peak power will dominate the nonlinear effects and excite significant memory effects, which will dominate the behavior of the device.

To investigate if peak and/or mean power are good predictors of modulated performance, both DUTs are load pulled with the 10 test signals. The DUTs are load pulled twice, once enforcing a constant mean power and once enforcing a constant peak power. This is done at $P_{in}$= 24 and 18 dBm for DUT A and B, respectively. These power values compromise between compressing the devices to unity gain when used as the mean, while ensuring some compression when used as the peak. As seen in Fig.4.10, the modulated performance of the DUTs compares very closely to their mean power CW performance across a broad range of PAPR values. Maximum modulated PAE deviates by less than 10 pp from the CW peak PAE value across the range of test-signal PAPRs, when mean power is compared to CW. Similarly, maximum modulated $P_{out}$ across the range of PAPRs deviates by less than 2 dB from the maximum $P_{out}$ value achieved under CW excitation. While these differences are not insignificant, mean power provides a much better estimate of modulated performance. Further, it is not a strong function of PAPR, while, in contrast, the peak modulated PAE and $P_{out}$ decrease monotonically with PAPR.

It is also of interest to investigate how significantly the optimal load impedances change in the peak and mean cases when compared with CW operation. In Fig.4.11, the difference in the magnitude and phase of the optimal $\Gamma_L$, for peak PAE (a) and $P_{out}$ (b) are shown. In all cases, the mean power $\Gamma_L$ deviates by less than 0.07 in magnitude and 1°. The mean behavior of the transistor when amplifying the 300-tone modulated signal is nearly identical to its behavior when amplifying a single sinusoid with the same mean power. This suggests that CW characterization is sufficient for obtaining a reasonable estimate of performance under narrowband modulation.




(a)

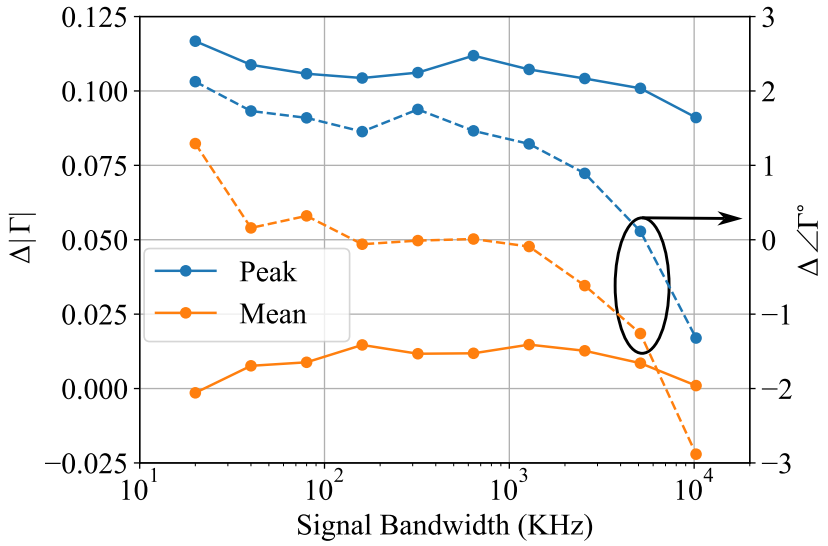



(b)

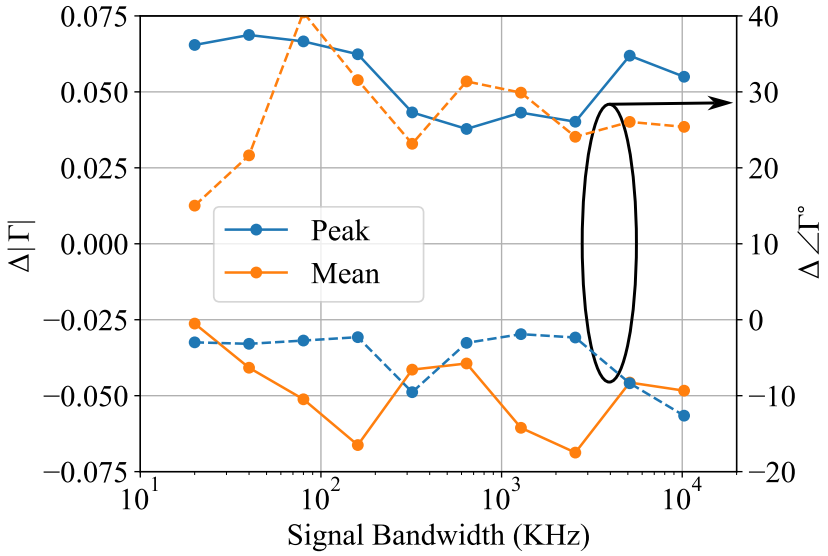
Figure 4.12: Difference in maximum PAE (a), $P_{out}$ (b) between 2-tone excitation, where peak power is held constant (blue) or where average power is held constant (orange), and CW. This difference is plotted as a function of the bandwidth of the 2-tone signal.

### 4.5.2 Varying Bandwidth

In this section, the effect of bandwidth on transistor performance is investigated. The bandwidth of a two-tone signal is swept from 20 kHz to 10.24 MHz in ten logarithmic steps, and both devices are load pulled with each signal. The statistics of a 2-tone signal are independent of tone-spacing; therefore, this analysis isolates the effects of bandwidth from the signal's statistical




(a)




(b)

Figure 4.13: Difference in $|\Gamma_L|$ and $\angle\Gamma_L$ for PAE (a), $P_{out}$ (b) between 2-tone excitation, where peak power is held constant (blue) or where mean power is held constant (orange), and CW. This difference is plotted as a function of the bandwidth of the 2-tone signal. Results are shown for DUT B.

properties. This analysis is also limited to a maximum bandwidth of 10.24 MHz due to the intrinsic narrow instantaneous bandwidth of passive slug tuners.

The analysis where bandwidth is swept is performed similarly to the above analysis across PAPR. The device is load pulled twice for each signal bandwidth, which allows both peak and

mean power to be compared to CW. Again, the peak and mean power levels are 24 dBm for DUT A and 18 dBm for DUT B. As seen in Fig.4.12, the peak values of both PAE and $P_{out}$ obtained across bandwidth with two-tone excitation compare quite closely with the measured CW values. However, for DUT A, comparing CW power with the peak modulated power yields a slightly smaller discrepancy between CW and modulated performance. Additionally, looking at both the peak and mean cases for both devices demonstrates a negligible change in $P_{out}$ across the bandwidth range. PAE does slightly improve at higher bandwidths by $\sim$1pp, but this may be due to the passive tuner presenting different impedances to each tone as the bandwidth is increased.

Similarly, as with CW and modulated performance across PAPR, it is also important to consider how the impedances to achieve the peak values differ between CW and modulated operation. Fig.4.13 shows the change in $|\Gamma_L|$ and $\angle\Gamma_L$ between CW and 2-tone across bandwidth for DUT B. As with the maximum PAE and $P_{out}$ values, the impedances that achieve those values are not as clearly aligned at mean power with CW values as for the 300-tone multi-tones. In particular, good agreement of the $\Gamma_L$ magnitude and angle is achieved when comparing mean power to CW for maximum PAE values. However, for the maximum $P_{out}$ impedances, neither comparing mean nor peak power to CW has a clear advantage. In particular, $|\Gamma_L|$ deviates by $\sim 0.05$ for both cases across bandwidth, and $\angle\Gamma_L$ deviates by significantly less ($\sim 10^\circ$ compared to $\sim 20^\circ$) as well.

### 4.5.3 Weighted PDF Implications

It is evident that an unweighted PDF in linear power units, e.g., Fig.4.14, appears to be quite different from a PDF in decibels, e.g., Fig.4.8. Here, we prove that a PDF expressed in decibels is implicitly a linearly power-weighted PDF. We start by defining a function $g$ which is a mapping between linear and decibel units and its inverse $g^{-1}$:

$$g(x) = y = 10 \cdot \log_{10}(x)$$

$$g^{-1}(y) = x = 10^{y/10}$$

The probability density function change of variables is then defined as [96]:

$$f_Y(y) = f_X(g^{-1}(y)) \cdot \left| \frac{d}{dy}(g^{-1}(y)) \right|$$

We can then substitute the definition for $g^{-1}$ to obtain:

$$f_Y(y) = f_X(10^{y/10}) \cdot \left| \frac{d}{dy}(10^{y/10}) \right|$$

After taking the derivative, we obtain the following:

$$f_Y(y) = f_X\left(10^{(y/10)}\right) \cdot 10^{(y/10)} \cdot 10^{-1} \cdot \ln(10)$$

Finally, we can neglect the constants and again use the definitions in (4.1) to obtain:

$$f_Y(y) \propto x \cdot f_X(x)$$

which demonstrates that a PDF in logarithmic units is proportional to the linearly power-weighted PDF in linear units, not the standard unweighted PDF.

This concept of a weighted PDF is important for predicting transistor behavior under modulated excitation. Specifically, a PDF alone is a small signal model, in that it assumes that all power levels have equal impact on the transistor response. The linearly power-weighted PDF is a better way to look at the system excitation by including the input power.

This can be observed in Fig.4.14, where the unweighted and the linearly power-weighted PDF are plotted together for the 8.43 dB PAPR 300-tone multi-tone. It is evident from the plot that the mode of the weighted PDF is co-located with the mean of the unweighted PDF. We have already demonstrated that the behavior of the transistor under this excitation is well predicted by the equivalent CW performance at the mean power of the signal. The weighted PDF provides a visual tool for understanding why the transistor's behavior is primarily dictated by the mean power and essentially unaffected by the peak power, for the case of Rayleigh distributed OFDM-like signals.

It is also of interest to look at the unweighted and weighted PDFs for a two-tone signal. As seen in Fig.4.15, the unweighted PDF has a bimodal distribution, with one mode near zero and one near the peak power. The weighted PDF, however, has a single mode near the peak power. This

suggests that a transistor's behavior should be primarily dictated by the peak power. However, the measurements do not support this conclusion. This is because the 2-tone distribution is not well constrained around the peak power and has relatively high probabilities of powers lower than peak occurring.

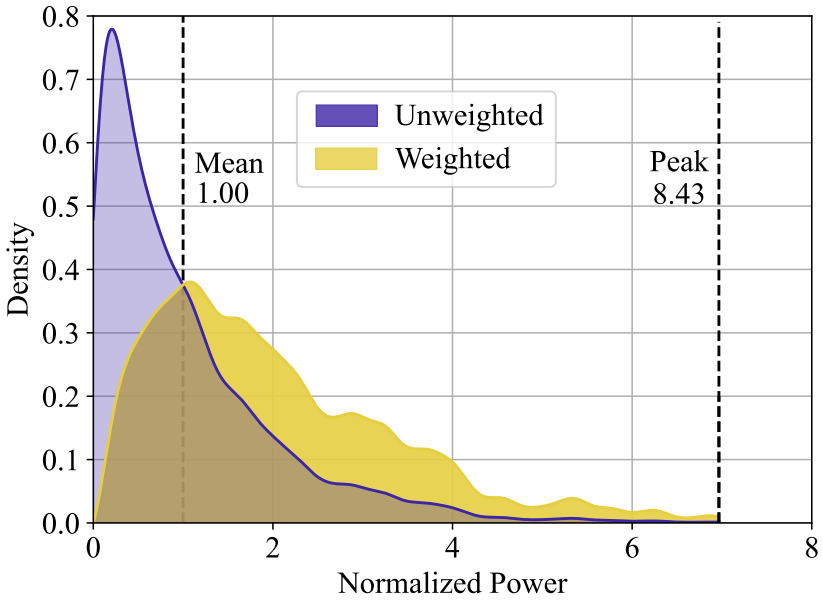



Figure 4.14: Unweighted and weighted probability density function of a 300-tone multi-tone signal with random phases and equal amplitude and a PAPR of 8.43 dB. The simulated time-domain power is normalized to have a mean of 1.

## 4.6 Linearity

A unique advantage of performing load pull under modulated conditions is the ability to directly determine linearity metrics. While linearity can also be estimated from CW measurements by measuring at multiple power levels and determining the AM-AM and AM-PM response, this is cumbersome and ignores any potential dynamic effects of the device.

To investigate how linearity is affected by excitation signal PAPR, we calculate noise-power-ratio (NPR) from the measurements described above. As seen in Fig.4.16, NPR is shown when both peak and average power are held constant for both devices at the maximum PAE (a) and maximum $P_{out}$ (b) points. As expected, NPR is higher (better) when peak power is held fixed

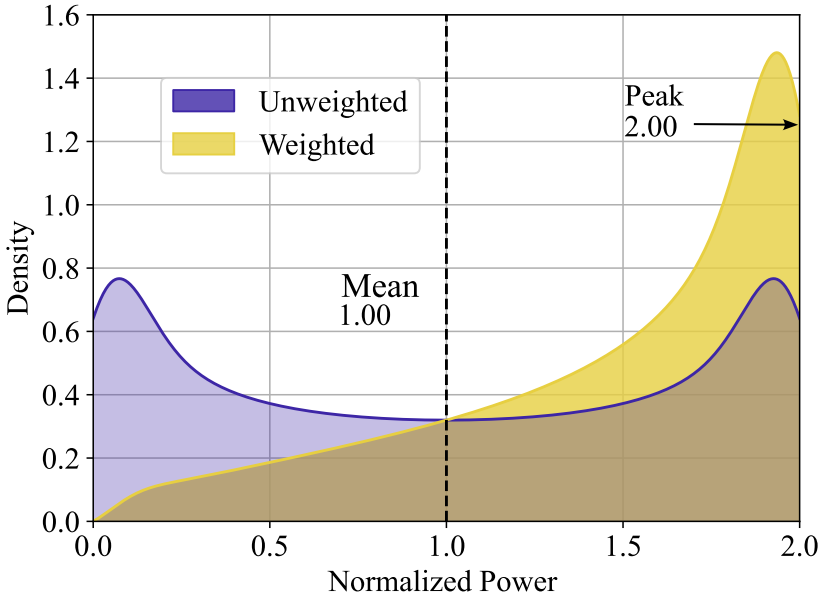
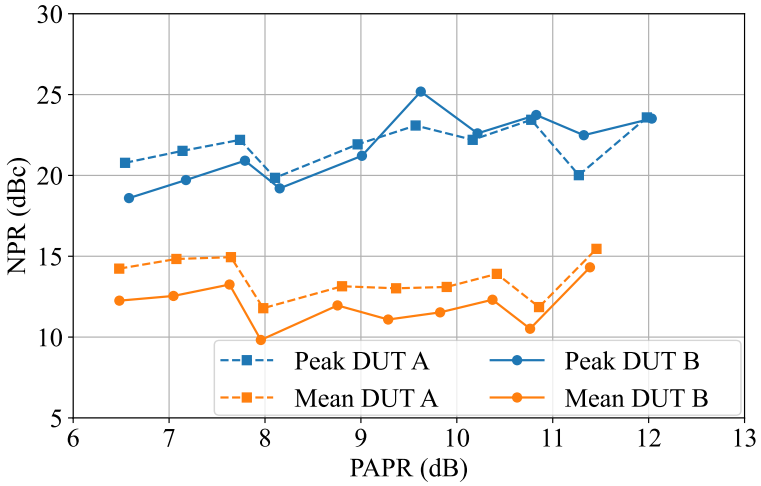



Figure 4.15: Unweighted and weighted probability distributions for a two-tone signal, with simulated instantaneous power normalized to a mean of 1.

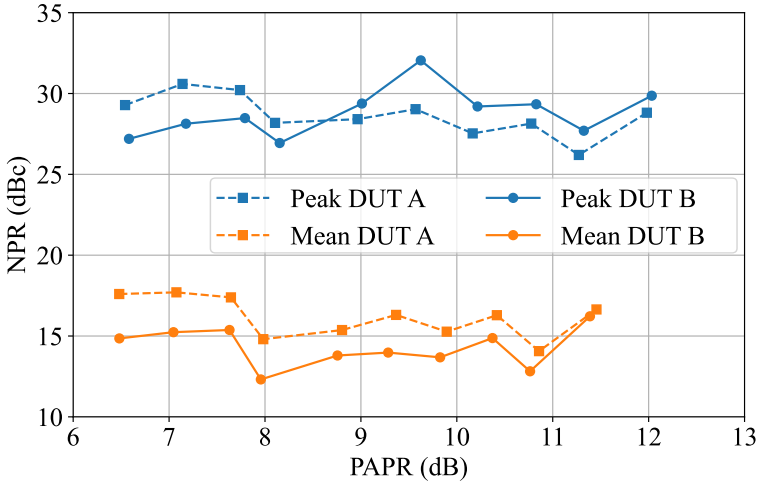
at 24 and 18 dBm for DUT A and B, respectively. It is also interesting to note that NPR is not strongly affected by PAPR when either mean or peak power is held fixed. The reason for this is as follows: 1) mean power primarily dictates NPR. 2) In the case where peak power is held constant, a change in NPR over PAPR is expected. However, the mean power point for the different PAPRs lies sufficiently into back-off for the response to be nearly constant.

It has been shown in [106] that error vector magnitude and NPR are directly related. This suggests that NPR is a complete in-band measure of linearity. It is, however, still insightful to look at the device's response in time. As shown in Fig.4.17, the instantaneous gain magnitude (a) and phase (b) are shown for DUT B with mean power held fixed and when $Z_L = 50\,\Omega$. The instantaneous gain magnitude and phase are plotted for the lowest and highest PAPR signals and demonstrate that the trajectories are very similar for both cases, and that little memory effects occur in either case. Furthermore, the figure shows that the transistor is not operating far into compression at 18 dBm of incident power. This also validates that the mean power of the device is in a linear regime at this operating point.

The instantaneous gain magnitude and phase response are shown in Fig.4.18 for the 20 kHz and 10.24 MHz 2-tone signals. It is evident in the gain magnitude that there is significant hysteresis for the 10.24 MHz two-tone. The gain begins to exhibit hysteresis 1 dB back from the mean power and increases to a deviation of $\sim$ 1.5 dB 7 dB in back-off. Interestingly, this hysteresis is not observed in the phase of the gain.




(a)




(b)

Figure 4.16: Linearity measured as NPR at the maximum PAE (a), $P_{out}$ (b) points, where peak power is held constant (blue) or where average power is held constant (orange). The NPR is plotted as a function of the PAPR of the modulation signal.

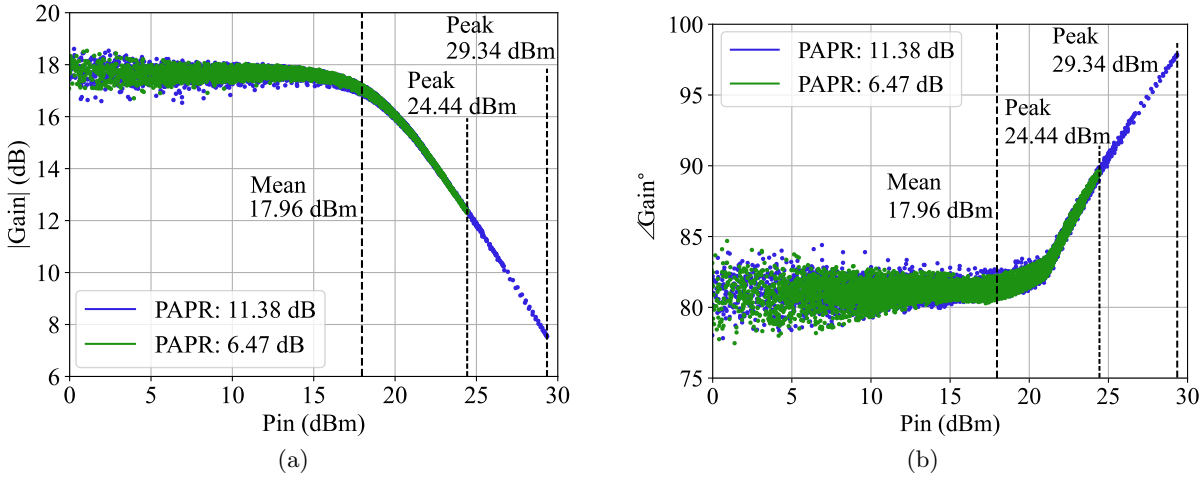



Figure 4.17: 300-tone instantaneous gain magnitude (a) and phase (b) for DUT B with a common 50 Ω load impedance.

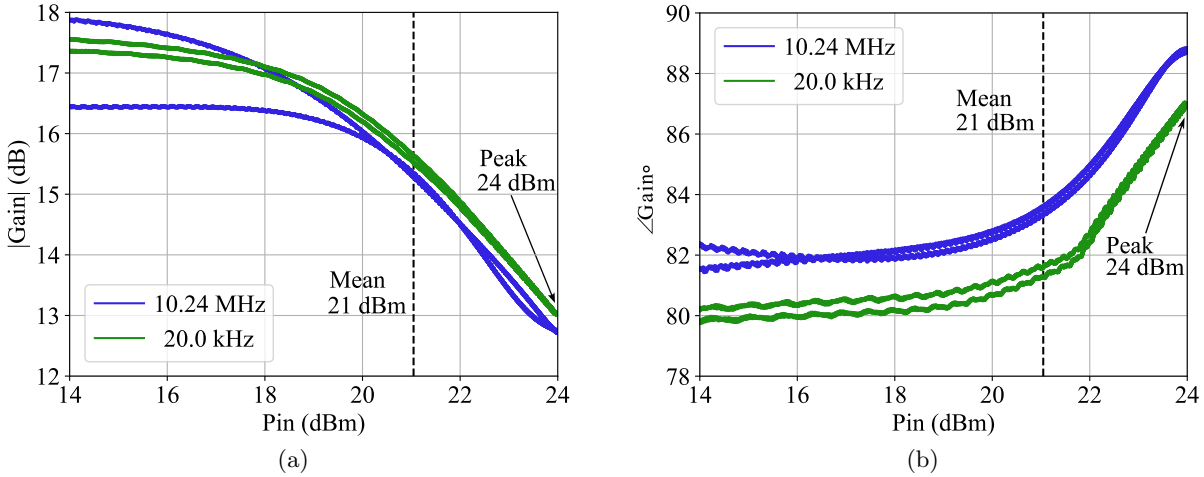



Figure 4.18: Two-tone instantaneous gain magnitude (a) and phase (b) for DUT B with a common 50 Ω load impedance.

## 4.7 Discussion and Conclusions

In summary, this chapter addresses measurement-based characterization of GaN HEMT power transistors under modulated signal excitation. Signal standards are rapidly changing, and it is impractical to design transmitter amplifiers individually for each new signal. From a hardware test perspective, with a specific modulated signal, the output voltage is dependent on both the modulation standard and the bit sequence. Rather than characterizing a device with a specific

modulation, in this chapter, we attempt to describe signals by their statistical properties to determine which characteristics of the signal have the most impact on transistor behavior. To this end, we use an OFDM-like multi-tone signal with 300 tones that can vary in phase with equal amplitudes. Using a large-signal vector network analyzer-based passive load pull system, two GaN-on-SiC transistors are measured at $f_0 = 2\,\text{GHz}$. The PAPR of the multi-tone signal is swept, and bandwidth is held constant to demonstrate that PAPR does not significantly affect the PAE, $P_{out}$, or linearity measured via NPR.

Additionally, the bandwidth of a two-tone excitation with a constant PAPR is swept from 20 kHz to 10.24 MHz, which demonstrates that, for narrow relative excitation bandwidths, the PAE, and $P_{out}$ remain nearly constant. Because a two-tone signal does not have a Rayleigh distribution, using mean power for comparing performance to CW is not appropriate. Furthermore, because the PDF deviates substantially from an OFDM-like (Rayleigh) distribution, conclusions from a two-tone analysis have limited utility for predicting performance with modern communications signals.

Furthermore, this analysis demonstrates that traditional CW-validated models are adequate for designing an amplifier intended for communications applications with OFDM-like signals. Crucially, it is demonstrated that the mean power of a Rayleigh distributed signal dominates average response metrics like NPR, PAE, $P_{out}$, Gain, etc. The linearly power-weighted PDF is used to explain this conclusion and constrain its applicability to signal excitations with a Rayleigh distribution, such as OFDM. It is further shown that the power-weighted PDF is implicitly commonly used in the form of a PDF expressed in logarithmic units.

The characterization under modulated signals is performed with passive load pull at the fundamental carrier frequency, with arbitrarily terminated but known harmonic impedances. To fully describe device behavior, a systematic control of harmonic impedance under modulated conditions would be a useful extension of this work. Further, for wide instantaneous bandwidths, passive load pull tuner impedance varies significantly, described as *phase skew*. Active or hybrid-active load pull methods can provide improved impedance control and eliminate this problem, provided sufficient

linear power and bandwidth are available from the instrument sources.

# Chapter 5

## Network Emulation for PA Design for Communications Applications

This chapter introduces a hardware-in-the-loop design approach, termed Microwave Network Emulation. Practically, this represents an alternative to nonlinear simulations by directly measuring a nonlinear device's response with the relevant sources, loads, and matching networks all *emulated* with a vector calibrated measurement system and vector signal sources. Modern microwave design is typically conducted using a nonlinear model and a harmonic balance solver. Harmonic balance is the preferred method as it is a frequency domain solution and is typically much faster for high-frequency circuit design than a time-domain solver, such as Spice. However, running a harmonic balance simulation with a modulated signal can be challenging. To extract metrics relevant for communications, such as PAE under modulated stimulus or time domain metrics, such as EVM, another solution is required. Transient simulations are unwieldy as the time constants of the fundamental frequency and its harmonics are typically vastly different than the envelope bandwidth of the modulated signal. As a result, envelope simulations are commonly used. These are time-domain simulations performed at the envelope or baseband signal frequencies. Envelope simulations can be successfully used to extract EVM and other metrics, but typically make assumptions about the nonlinear device. Some of these assumptions are discussed in Chap.3, for the envelope simulations performed there.

To address these challenges, we present network emulation—a hardware-in-the-loop (HITL) approach to circuit analysis that eliminates the need for a nonlinear device model. Network emulation is a method where the electrical environment of a passive network is replicated around

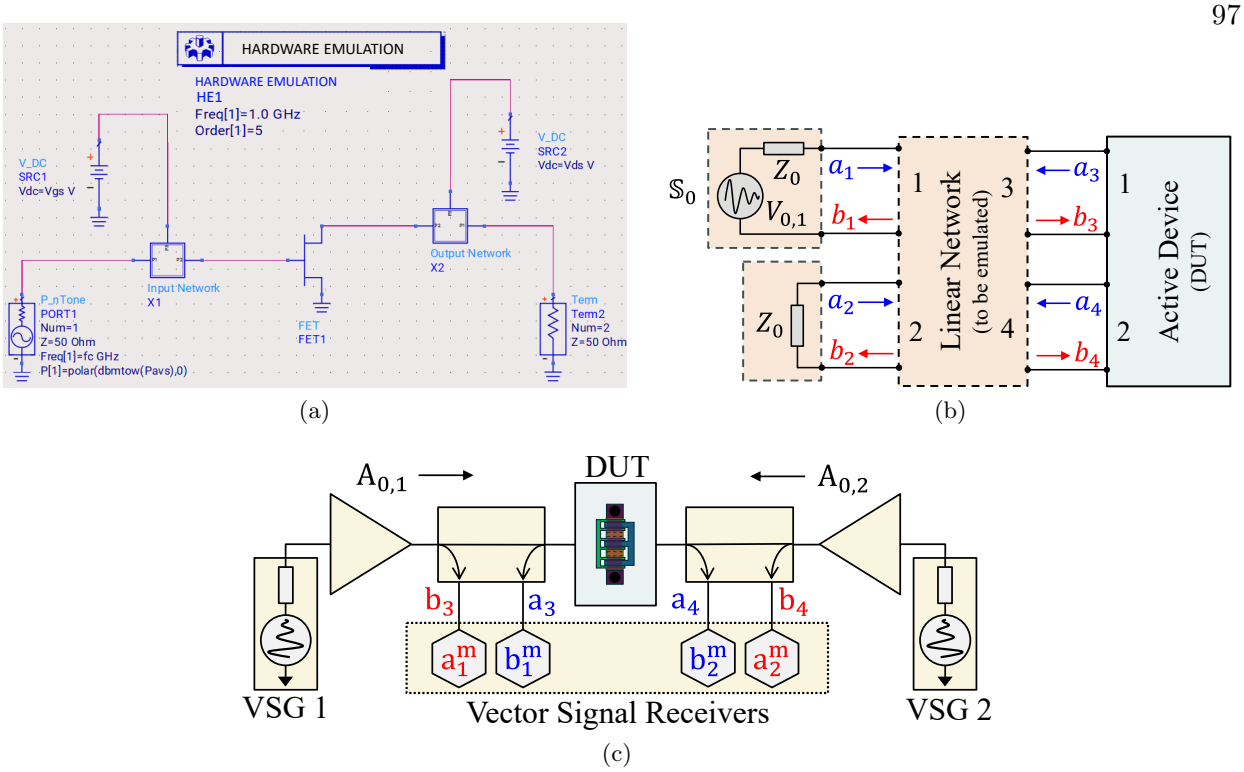



Figure 5.1: Network emulation of a single-stage amplifier. (a) Circuit as described in a design tool; (b) equivalent circuit diagram; (c) implementation on the active device using a vector signal transceiver measurement system. Power waves are referenced to the network, except for the measured power waves $a_1^m$, $b_1^m$, $a_2^m$, and $b_2^m$, which are referenced to the device under test.

a physical device. Fig. 5.1 illustrates the process for a single-stage amplifier. The process begins with a circuit design, as shown in Fig. 5.1(a), including linear networks, active devices, and sources/loads. These elements are reorganized into the equivalent block diagram in Fig. 5.1(b), which is used to determine the corresponding excitations for the active device. These excitations are then applied to the physical device via the measurement system shown in Fig. 5.1(c). The measurement system records the response of the device under test (DUT) and returns it to the network model. The unknown power waves in the circuit are then determined by re-embedding the linear network, completing the analysis with the full circuit response. Although not explicitly shown in Fig. 5.1(a), coupling between networks (e.g., feedback or electromagnetic coupling) is supported by this technique.

It is important to note that the emulation method demonstrated here resembles active source

and load pull, and indeed, it uses any open-loop active source/load-pull measurement system. However, the key distinction is that load/source-pull is fundamentally a *device-level* characterization tool [38]. In contrast, the emulation method characterizes a physical transistor within a virtual matching network, allowing for *circuit-level* characterization. It may therefore be tempting to conclude that the technique is a simple linear embedding; however, the virtual linear networks necessarily change the excitation to the non-linear device, due to, e.g., dispersion, loss, coupling, and feedback. This change in excitation leads to a different (nonlinear) device response and therefore cannot be described by a linear embedding model. As a result, it may be useful to think of this as a harmonic balance analog that uses a physical transistor, rather than a model, to determine the non-linear response of a circuit.

From the circuit designer's perspective, using network emulation does not change how the design process is carried out. Figure 5.2 illustrates the high-level process of network emulation, which starts when the user triggers circuit analysis in the CAD tool. Since any microwave CAD tool can be used in this step, it is not discussed in detail in this chapter. The designer simulates the passive network $S$-parameters, e.g., a load-pull tuner or matching network, and hands the $S$-parameters and desired circuit excitations over to the network emulator. The network emulator uses this information to determine the equivalent excitations for the device under test, i.e., the nonlinear device, and sends it to the test bench. The test bench applies the excitations to the DUT and returns its measured response to the network emulator. The network emulator computes the excitations at the circuit ports of interest using the network $S$-parameters and given excitations. Finally, the CAD tool reports the overall circuit performance to the user. This process is repeated iteratively until the desired performance is achieved.

## 5.1 Tuner Validation

The hardware level abstractions and general active wideband source/load tuner method used in this section and the remainder of the thesis are discussed in detail in [41] and will not be repeated here. To provide context, the tuner method splits the excitation $A_{0,n}$ coming from the sources, as

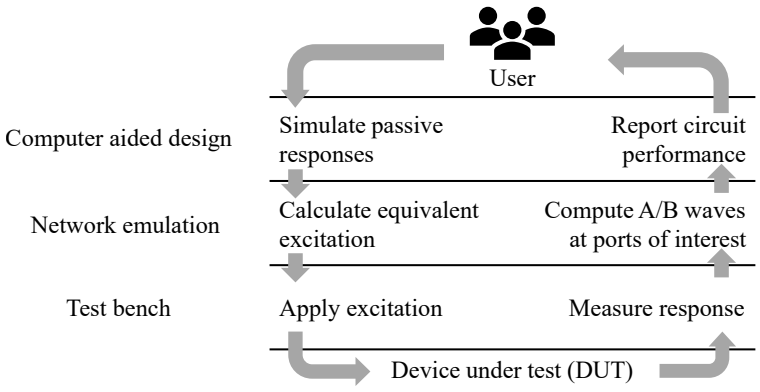



Figure 5.2: Outline of network emulation process, showing the different layers starting from the CAD tool at the user level, to the hardware at the nonlinear DUT level.

indicated in Fig. 5.1c, into two separate components, $\mathbb{S}_{0,n}$ and $T_{0,n}$. This is a convenient abstraction to make because the total excitation $A_0$ of a tuner can be thought of as some signal being used to excite the system ($\mathbb{S}_0$) and some reflection ($T_0$). In the case of load pull, for example, there is no excitation to the circuit coming from the load and ($\mathbb{S}_0 = 0$). Conversely, in source pull, if the source is already matched to the system impedance, then there is no reflection and $T_0 = 0$.

This section presents two validation cases, which will be used to demonstrate both the tuner methods and their applicability to network emulation. Each validation example uses a source and load pull tuner to present impedances to a non-zero length *thru* standard. The source-pull tuner uses a 300 MHz, 300-tone signal excitation with a 6.5 dB peak to average power ratio (PAPR) and a peak available source power of 10 dBm.

The first validation case is to individually load and source pull a matched *thru*. This is a useful validation case because the expected response of a *thru* with different source/load reflection coefficients is well known and trivial to calculate. Fig. 5.3a illustrates the constellation of reflection coefficients used by each tuner in this example. First, source pull is performed over the constellation illustrated in Fig. 5.3a while maintaining a $\Gamma_L = 0$. Next, load pull is performed over the same constellation while setting $\Gamma_S = 0$. The maximum reflection coefficient magnitude of the constellation is 0.9. Table 5.1 illustrates the maximum and average errors in reflection coefficient

and transducer gain as defined in [89]. The measured transducer gain is calculated as:

$$\mathrm{G_{t,measured}} = \frac{P_{out}}{P_{avs}},$$

$$P_{out} = \frac{|b_2|^2 - |a_2|^2}{2Z_0} \quad \text{and} \quad P_{avs} = \frac{|\mathbb{S}_0|^2}{2}\frac{|1-\Gamma_S|^2}{1-|\Gamma_S|^2},$$

where $\Gamma_S$ is measured using (5.1).

$$\Gamma_S = \frac{a - \mathbb{S}_0}{b - \mathbb{S}_0} \tag{5.1}$$

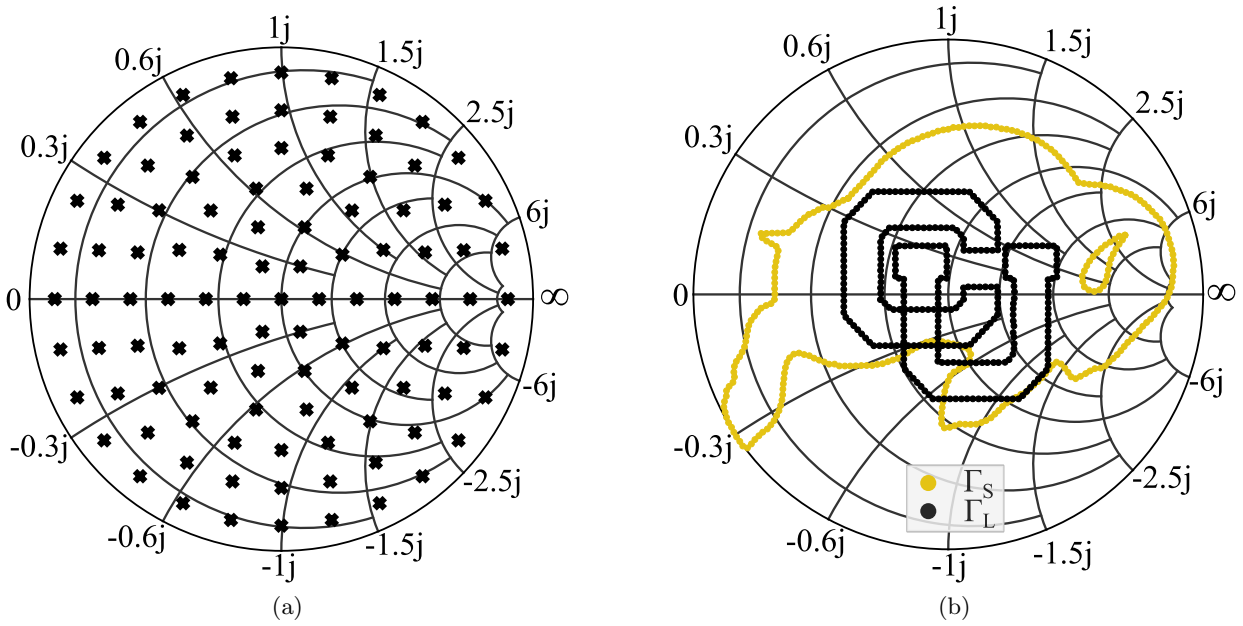



Figure 5.3: (a) Single point gamma targets used for wide-band active load and source pull validation. (b) Measured simultaneous source, i.e., gold buffalo, and load pull, i.e., black "CU" logo, $\Gamma$ trajectories measured on a *thru*. Each point corresponds to a single tone in a 300-tone signal. Some error is evident in the straight lines of the "CU" logo.

The second validation case demonstrates *simultaneous* wide-band active load and source pull validation on a *thru*. The final, measured reflection coefficients are plotted in Fig. 5.3b. The yellow buffalo trace is the source impedance trajectory, and the black, "CU" logo is the final load impedance trajectory. Each point in the trajectories presented here is a tone in the wide-band signal, and both trajectories are presented simultaneously. The final root-mean-square (RMS) error

Table 5.1: Results of source and load pull.

| | Err. Γ (dB) | | | Err. Gain (dB) | | |
|---|---|---|---|---|---|---|
| | Min | Mean | Max | Min | Mean | Max |
| Source Pull | -30.9 | -23.8 | -20.4 | -28.3 | -24.1 | -16.6 |
| Load Pull | -34.3 | -26.8 | -21.7 | -28.5 | -24.2 | -19.5 |

Error in the reflection coefficient and transducer gain of the single point constellation load and source pull. The tuner convergence threshold is set to -20 dB for expediency.

in source and load reflection coefficient is -29.9 dB and 31.2 dB, respectively. This demonstrates the efficacy of this approach to simultaneous and wideband active load and source-pull for arbitrary impedance trajectories.

## 5.2 Equivalent Source Method for 2-Port Network Emulation

We begin the discussion of network emulation with the example circuit shown in Fig. 5.4, with two sets of reference planes:

(1) **Measurement planes**, which are the *physical* locations where power waves are observed on the device under test (DUT); and

(2) **Circuit-port planes**, which are the *virtual* planes where boundary conditions—such as excitations and loads—are applied.

Modulated load-pull techniques enable the presentation of arbitrary impedance trajectories over a wide instantaneous bandwidth. In the case presented here, the trajectories include the matching networks together with possible dispersion, loss, and coupling associated with these networks.

Techniques such as the one in [10] focus only on the power waves at the load measurement plane. Extending active load-pull to hardware-in-the-loop design requires that: (1) circuit performance metrics are evaluated at the circuit-port planes where they are relevant, rather than the measurement planes; and (2) excitations are transformed through the matching network to include

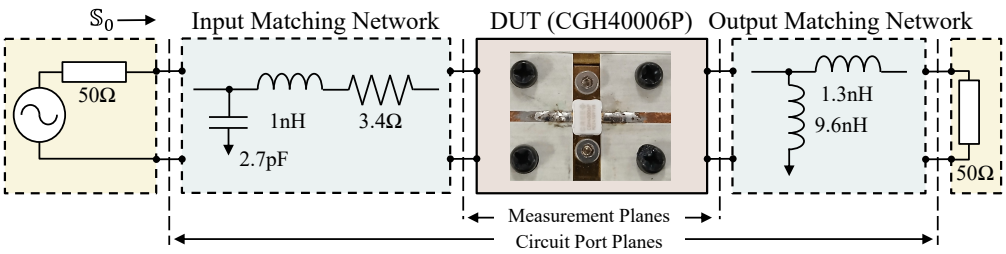



Figure 5.4: Circuit used to demonstrate small-signal two-port network emulation from 2.1–2.4 GHz with a MACOM CGH40006P packaged GaN HEMT. The lumped-element matching circuits are used to compare emulation and simulation in a straightforward manner.

dispersion and loss at the DUT reference plane.

To satisfy these requirements, the abstraction necessary for network emulation is the network equivalent source, which we introduce here in the context of a 2-port network and a corresponding simulation source which is assumed to be matched ($Z_s$=$Z_0$), e.g., Fig. 5.5(a). The linear network is modeled by an $S$-parameter matrix with its second port connected to the DUT.

$\mathbb{S}_0$ at the tuner abstraction level becomes $\mathbb{S}_{eq}$. From Thévenin's Theorem, $\mathbb{S}_{eq}$ is the open-circuit excitation:

$$\mathbb{S}_{eq} = \frac{\mathbb{S}_0}{1 - s_{22}}, \tag{5.2}$$

assuming that port 2 of the network is at the DUT. The corresponding total excitation becomes:

$$A_0 = \mathbb{S}_{eq} + T_0, \tag{5.3}$$

where $T_0$ is the tuner excitation corresponding to $\Gamma_S = s_{22}$.

Once the total excitation is set, the corresponding power waves at the circuit port plane (Fig. 5.5(a)), $a_n$ and $b_n$ are:

$$a_n = \frac{a - bs_{22}}{s_{21}} \quad \text{and} \quad b_n = \frac{as_{11} - b\Delta}{s_{21}},$$

where $\Delta = s_{11}s_{22} - s_{21}s_{12}$.

To validate this method, Fig. 5.6 compares the $s_{11}$ and $s_{21}$ parameters obtained from simulation and emulation for the circuit shown in Fig. 5.4. This small-signal comparison serves as a

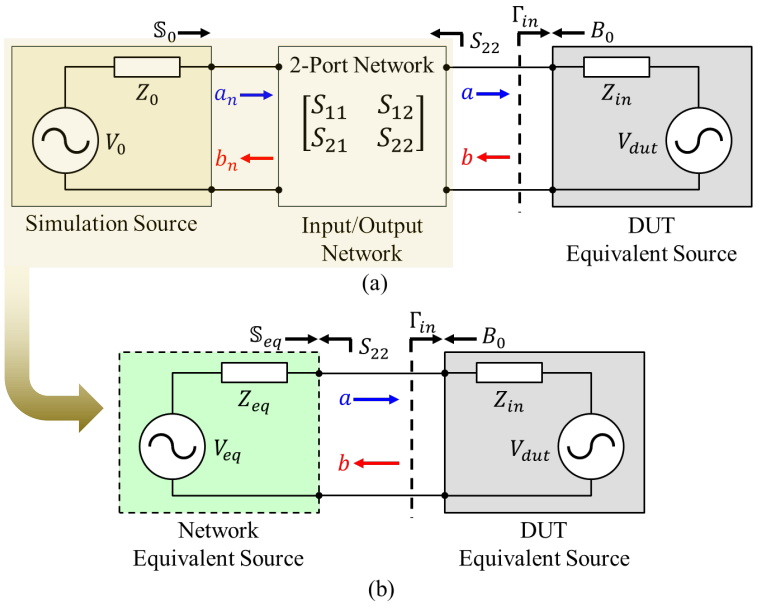



Figure 5.5: A (a) 2-port network and (b) its equivalent source.

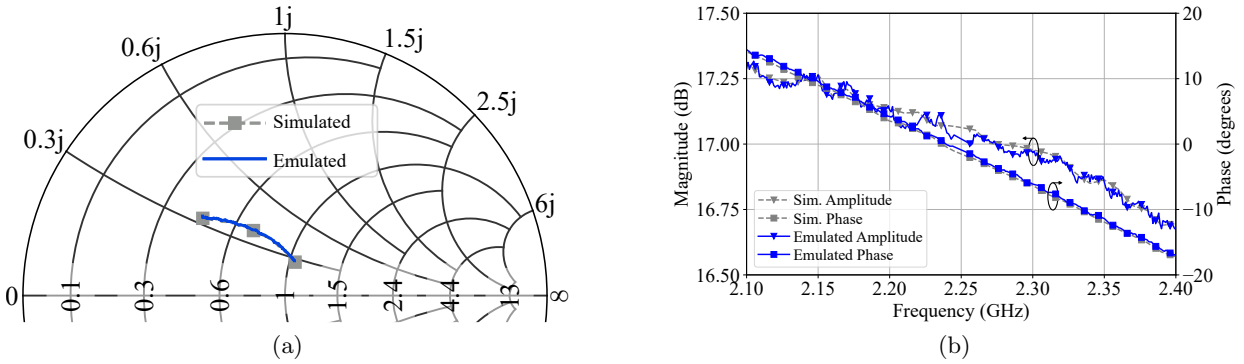



Figure 5.6: Comparison of the (a) $s_{11}$ and (b) $s_{21}$ simulation and emulation results of the circuit illustrated in Fig. 5.4.

valuable demonstration that the responses of the emulated and simulated circuits are virtually identical with a peak relative error in $s_{21}$ and $s_{11}$ of 1.6% and 8.2%, respectively, thereby validating the effectiveness of the method in small-signal. However, this 2-port approach is incapable of handling more complicated behaviors such as feedback and coupling between networks. Later, we address these limitations by expanding this approach to generalized N-port networks with coupling.

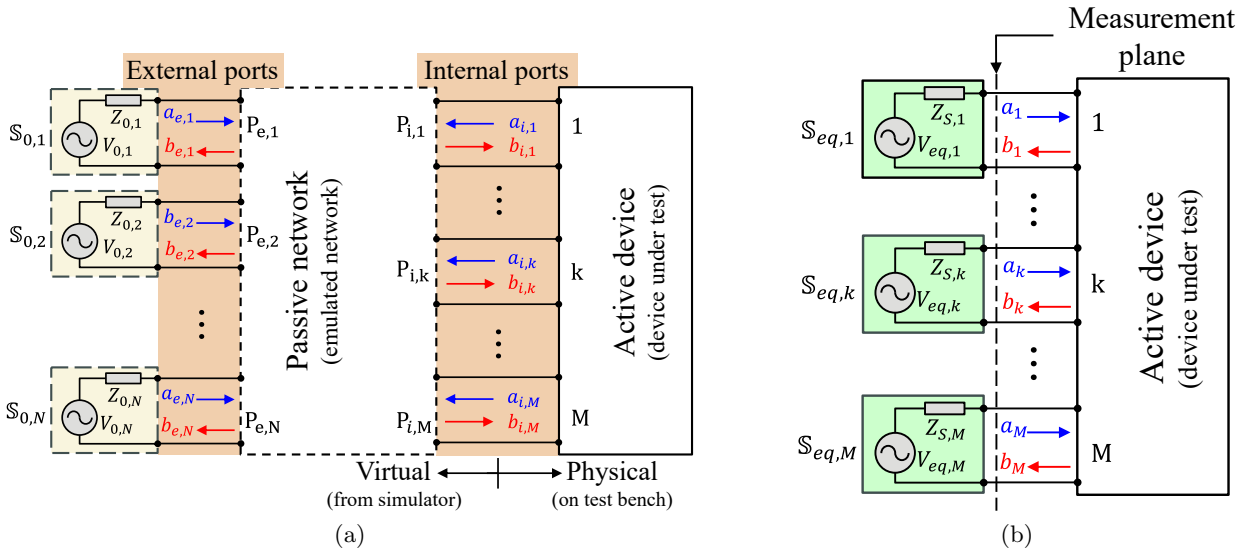



Figure 5.7: Conceptual circuits used in the network emulation process. (a) Setup of the problem with a passive network and circuit excitations where the sources and network are virtual, and the active device is physical. (b) The passive networks and sources from (a) are replaced with Thévenin equivalent sources. Note that the orientation of the $a$ and $b$ waves is aligned to the passive networks in (a) and to the active device in (b).

## 5.3 Equivalent Source Method for N-Port Network Emulation

Fig. 5.7 shows the two equivalent networks discussed in this section. Fig. 5.7(a) illustrates a block diagram of the circuit under analysis. In this figure, there are two port groups: *external* and *internal*. The external ports, $P_{e,k}|_{k\in[1,2,\ldots,N]}$, are where the signal excitation(s), $\mathbb{S}_{0,i}$, and load impedance(s), $Z_{S,i}$, are presented to the circuit. These ports define the electrical interface to the rest of the system, and therefore, all relevant performance metrics are evaluated at this plane. The active device is connected to the internal ports, $P_{i,k}|_{k\in[1,2,\ldots,M]}$, where the physical $a$ and $b$ waves are observed in measurement. In Fig. 5.7(a), the sources on the external ports and the passive network are virtual, i.e., they only exist in simulation, while the active device and hardware equivalent sources on the measurement plane in Fig. 5.7(b) are physical.

Fig. 5.7(b) illustrates the electrical equivalent to Fig.5.7(a) with respect to the internal port plane. In this figure, the sources and passive network are replaced with the network equivalent sources that drive the emulation process. The derivation of these sources and their application

towards network emulation is presented in the next section.

The simulator sources, i.e., the sources located at the external port plane of Fig. 5.7(a), form the boundary conditions for the nonlinear circuit analysis problem. These sources consist of a signal excitation, $\mathbb{S}_{0,k}$, and a port impedance $Z_{S,k}$. The passive network is described with a $(N+M) \times (N+M)$ $S$-parameter matrix, where $N$ and $M$ are the numbers of *external* and *internal* ports, respectively. Here, this scattering matrix is represented with four $S$-parameter sub-matrices:

$$S = \begin{bmatrix} S^{ee} & S^{ei} \\ S^{ie} & S^{ii} \end{bmatrix}, \tag{5.4}$$

where $S^{ee}$ is a $N \times N$ matrix describing the network coupling between external ports, $S^{ei}$ is a $N \times M$ matrix describing the network couplings from internal ports to external ports, $S^{ie}$ is a $M \times N$ matrix describing the network coupling from external ports to internal ports, and $S^{ii}$ is a $M \times M$ matrix describing the network coupling between internal ports. For example, a 4-port network where ports 1 and 2 are external ports and ports 3 and 4 are internal ports has the corresponding sub-matrices:

$$S^{ee} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}, \quad S^{ei} = \begin{bmatrix} s_{13} & s_{14} \\ s_{23} & s_{24} \end{bmatrix},$$

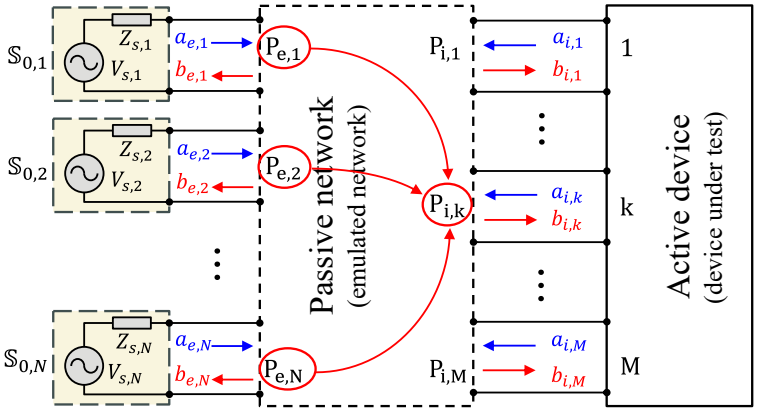
$$S^{ie} = \begin{bmatrix} s_{31} & s_{32} \\ s_{41} & s_{42} \end{bmatrix}, \quad S^{ii} = \begin{bmatrix} s_{33} & s_{34} \\ s_{43} & s_{44} \end{bmatrix}.$$

The $S$-parameters in (5.4) are generalized so that the reference impedances of the external ports are equal to the corresponding $Z_{S,k}$, while the reference impedance of all internal ports is equal to that of the measurement system, e.g. $50\,\Omega$. The generalized S-parameters can be found from [22], and ensure that $a_{e,k} = \mathbb{S}_{0,k}$ given $k \in [1, 2, ..., N]$ for the external ports, as discussed in the next section.

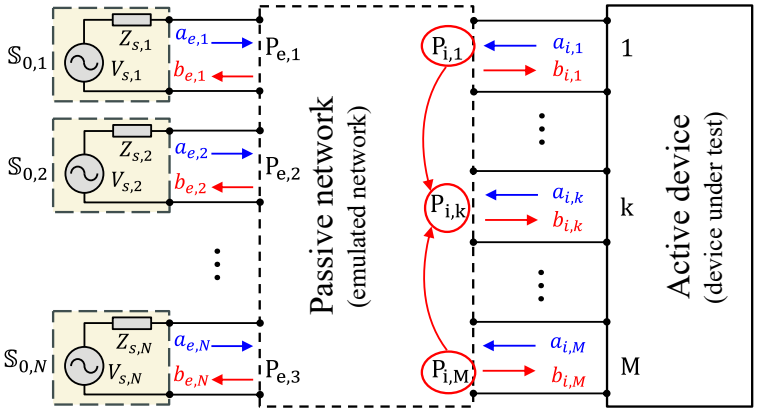
Fig. 5.8 illustrates the primary internal-port coupling paths: (a) external to internal ports via the passive network; (b) internal to internal ports via the passive network; and (c) internal to internal ports via the active device under test. The equivalent source representation of the passive network will handle cases (a) and (b) directly. Case (c) is handled implicitly during the implementation of the tuner equivalent source, i.e., as $B_{0,k}$.

From (5.4) the $b$-waves of all ports are:

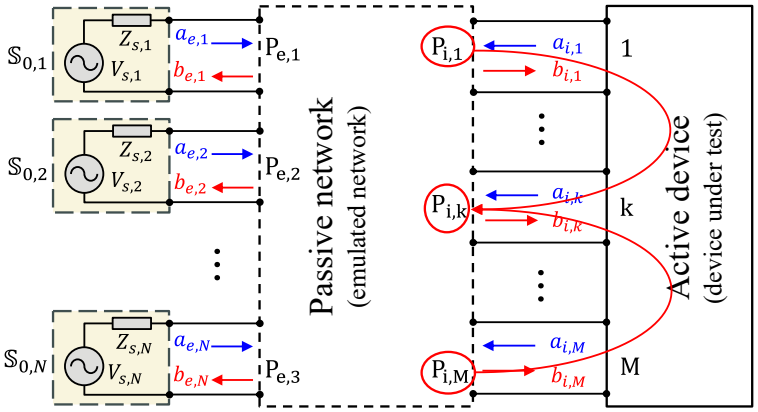
$$\begin{bmatrix} b_e \\ b_i \end{bmatrix} = \begin{bmatrix} S^{ee} & S^{ei} \\ S^{ie} & S^{ii} \end{bmatrix} \begin{bmatrix} a_e \\ a_i \end{bmatrix}, \tag{5.5}$$




(a)




(b)




(c)

Figure 5.8: The three coupling paths to port $N + x$ of the emulated network: (a) from external ports through the network, (b) from internal ports through the network, and (c) from internal ports through the DUT.

where $a_e$ and $b_e$ are an $N$-element column vectors representing the $a$ and $b$ waves at the external ports. Likewise $a_i$ and $b_i$ are $M$-element column vectors of internal $a$ and $b$-waves, respectively. From (5.5), the $k^{th}$ internal port ($P_{i,k}$) power wave, $b_{i,k}$, is realized as:

$$b_{i,k} = \sum_{x=1}^{N} a_{e,x} s_{kx}^{ie} + \sum_{x=1, x\neq k}^{M} a_{i,x} s_{kx}^{ii} \ ,$$

where $s_{kk}^{ii}$ is the $k^{\text{th}}$ element of the passive network's internal port S-parameters, $s^{ii}$. Because the passive network from Fig. 5.7(a) is represented by generalized $S$-parameters this equation becomes

$$b_{i,k} = \sum_{x=1}^{N} \mathbb{S}_{0,x} s_{kx}^{ie} + \sum_{x=1, x\neq k}^{M} a_{i,x} s_{kx}^{ii} \ . \tag{5.6}$$

Equation (5.6) shows that the $b$-waves at each internal port depend on the $a$-waves at all other internal ports. This implies that an iterative approach is required to achieve the proper $\mathbb{S}_{eq}$ which satisfies (5.6). The error in the internal port powers is defined here as the difference between the computed ($b_{i,k}^{calc}$) (5.5) and measured ($b_{i,k}^{meas}$) waves:

$$\text{Error} = \sqrt{\frac{1}{M} \sum_{k=1}^{M} \left| b_{i,k}^{meas} - b_{i,k}^{calc} \right|^2}, \tag{5.7}$$

which defines the total error associated with network emulation internal port coupling.

With the port coupling behavior defined, we now present the generalized network equivalent source definition. As was the case for the external port sources, each equivalent source has an equivalent excitation, $\mathbb{S}_{eq,k}$, and port impedance, $Z_{eq,k}$, where $k \in [1, 2, ..., M]$. The equivalent source impedance, $Z_{eq,k}$, is simply the open-circuit impedance:

$$Z_{eq,k} = Z_0 \frac{1 + s_{kk}^{ii}}{1 - s_{kk}^{ii}}, \tag{5.8}$$

where each equivalent source is coupled.

Referring to the $k^{\text{th}}$ port of Fig. 5.7(b), the equivalent source excitation is:

$$\mathbb{S}_{eq,k} = \frac{b_{i,k}}{1 - s_{kk}^{ii}}$$

Substituting (5.6) for $b_{i,k}$ results in:

$$\mathbb{S}_{eq,k} = \frac{\sum_{x=1}^{N} \mathbb{S}_{0,x} s_{kx}^{ie} + \sum_{x=1,x\neq k}^{M} a_{i,x} s_{kx}^{ii}}{1 - s_{kk}^{ii}} \tag{5.9}$$

This excitation can be split between components belonging to external port excitations and internal port excitations:

$$\mathbb{S}_{eq,k} = \mathbb{S}_{eq,k}^{e} + \mathbb{S}_{eq,k}^{i}, \tag{5.10}$$

Where $\mathbb{S}_{eq,k}^{e}$ is the equivalent port excitation due to the sources at the external plane in Fig. 5.7(a) and $\mathbb{S}_{eq,k}^{i}$ is the equivalent port excitation due to the adjacent internal sources, i.e. feedback at adjacent internal ports from the device under test. Inferring from (5.9) these excitations are:

$$\mathbb{S}_{eq,k}^{e} = \frac{1}{1 - s_{kk}^{ii}} \sum_{x=1}^{N} \mathbb{S}_{0,x} s_{kx}^{ie} \tag{5.11}$$

$$\mathbb{S}_{eq,k}^{i} = \frac{1}{1 - s_{kk}^{ii}} \sum_{x=1,x\neq k}^{M} a_{i,x} s_{kx}^{ii} \tag{5.12}$$

The reason for distinguishing (5.11) and (5.12) from (5.9) is that (5.11) only needs to be updated when the external source excitations or the passive network changes and (5.12) requires updating after each measurement.

With the network equivalent sources defined, we proceed to the discussion of the network emulation procedure. Before the process can begin, the emulator requires an $S$-parameter definition of the network, a designation of the internal and external ports, and the simulation source configuration, i.e. signal excitation and port impedance. A tuner is assigned to each internal port.

Once initialized, the emulator begins the process outlined in Fig. 5.9. The tuners on each internal port are assigned a reflection coefficient, and external excitations are generated from the provided simulation source information. The process begins by assuming all internal ports are decoupled, i.e., $\mathbb{S}_{eq,k}^{i} = 0$. This information is sent to the tuner, which determines the excitation $T_0$ required to generate the reflection coefficient at each port. Each internal port tuner is sequentially and iteratively updated until the desired reflection coefficients are obtained.

When complete, the port coupling error (5.7) is evaluated. If the coupling error is below the specified threshold, e.g. -20 dB, the process is assumed to be complete and the emulator

returns. If the threshold is not satisfied, the excitations associated with the internal port coupling are updated, i.e. (5.12), and the total equivalent excitation is recomputed for each port. The emulator then updates the tuners again and returns to the task of iteratively updating each tuner. The process of updating $\mathbb{S}_{eq}$ and resetting the tuners to the desired $\Gamma_S$ continues until either the emulator runs out of iterations or the convergence error criteria falls below the specified threshold.

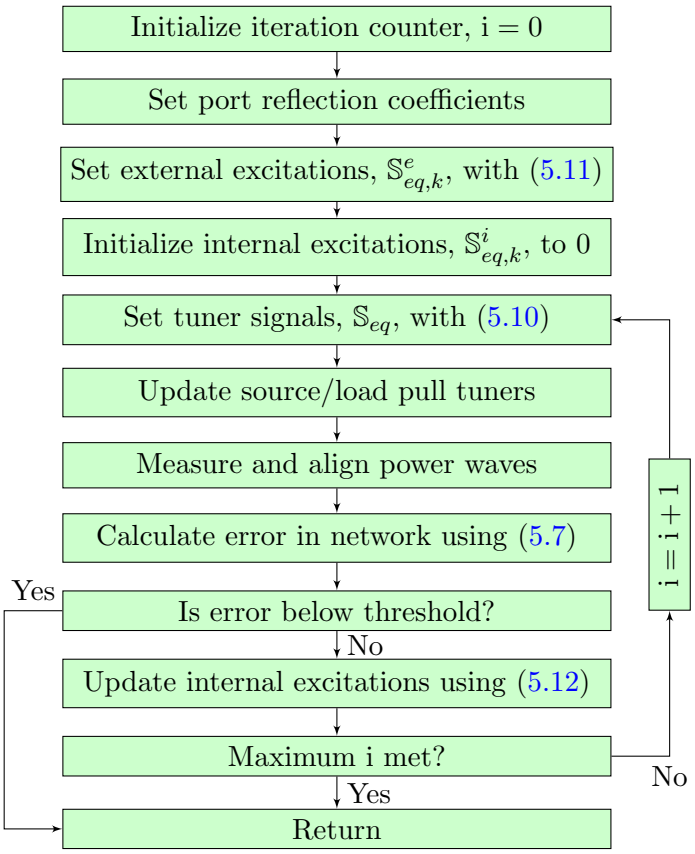



Figure 5.9: Block diagram for network emulation by updating the transmitter within the network equivalent source model.

## 5.4 Demonstration of Network Emulation

The network emulation method is demonstrated on a vector active source and load pull system designed in collaboration with NI, similar to the system presented in [40]. In principle, any

open-loop vector wideband active load/source pull system can support this concept, provided the software can implement the algorithms described above.

### 5.4.1 Hardware and Circuit Design

The setup consists of 4 NI 5840 VSTs, which provide the 4 receivers for measuring 2-port $a, b$ waves at the fundamental frequency. Additionally, 2 of the VST RF sources are used to provide the necessary excitations at $P_1$ and $P_2$ of the DUT, Fig. 5.10. The local-oscillators (LOs) are daisy-chained independently between the VST sources and receivers. An alignment pre-characterization is performed, which allows the receivers and sources to be synchronous. The necessity of having phase-locked sources to perform WALP is well known, e.g. [67]. The sources and receivers are individually synchronous; however, the sources are not coherent to the receivers. This necessitates using $A_0$ as a fixed reference to align the measured $a, b$ waves and enable relative updates to the sources.

The local oscillators (LOs) are daisy-chained separately for the VST sources and for the receivers, giving each group a shared LO. A pre-characterization step ensures synchronization within each group. As noted in [67], phase-locked sources are required for WALP. The sources and receivers are each synchronous, but the TX and RX LOs are independent. Therefore, $A_0$ is used as a fixed reference to align the measured $a, b$ waves and enable relative source updates.

AR 60S1G3 60 W amplifiers with $\sim 50$ dB of gain are used as drivers for $P_1$ and $P_2$. 4 directional couplers are used to sample the $a, b$ waves, and a circulator is placed after both drivers to maintain a constant $\Gamma_{S0}$ and avoid inadvertently load-pulling the driver amplifiers. A spectrum analyzer is connected to the 3rd port of the $P_2$ circulator to provide a visual (uncalibrated) verification of the DUT's $b_2$ behavior.

A coaxial SOLT calibration of the system is performed at $f_0 = 2.25$ GHz, over the 5840s 1 GHz of instantaneous bandwidth. Additional absolute amplitude and an absolute phase calibrations are performed, using an external power meter and one of the unused VST sources outputting a 1 GHz impulse as an assumed ideal comb-generator for the respective calibrations.

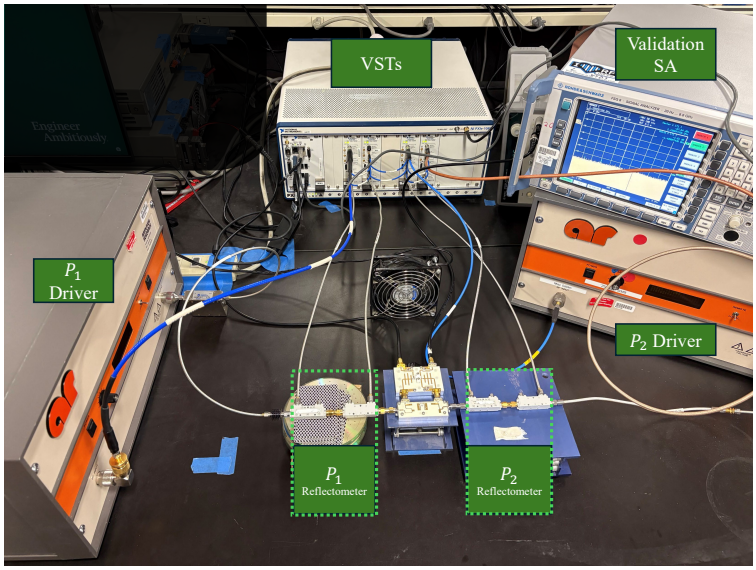



Figure 5.10: Photo of the measurement system used to perform network emulation.

Fig. 5.11 illustrates the designed device under test (DUT) and the corresponding matching network used for large signal microwave network emulation. The DUT has a MACOM CGH40006P GAN HEMT transistor, quarter-wavelength bias network, and trapping networks for the second and third harmonics. The integration of the bias and harmonic trapping networks is implemented as a part of the DUT because the present system does not have enough VSTs to operate at these frequencies. With more transceivers, the capability could be extended to operate in this capacity as well [69]. Including the baseband and harmonic responses as part of the DUT allows for consistency between the emulated and measured cases, as the DUT is only impacted by the impedances and excitations presented at the fundamental frequencies.

The matching network to be emulated consists of two simple transmission line matching networks with a resistive feedback path to introduce between -34 to -28 dB of coupling, shown in Fig. 5.11. A high-pass network is placed in the feedback path to attenuate low-frequency, out-of-band coupling while the in-band coupling is set as high as possible without causing the DUT to oscillate. After assembly, the matching network and the 90° hardline bends are measured on an Agilent E8463C PNA with a 4-port test set and phase-stable RF cables to obtain the $S$-parameters. A high degree of accuracy is required in these measurements, as any error will result

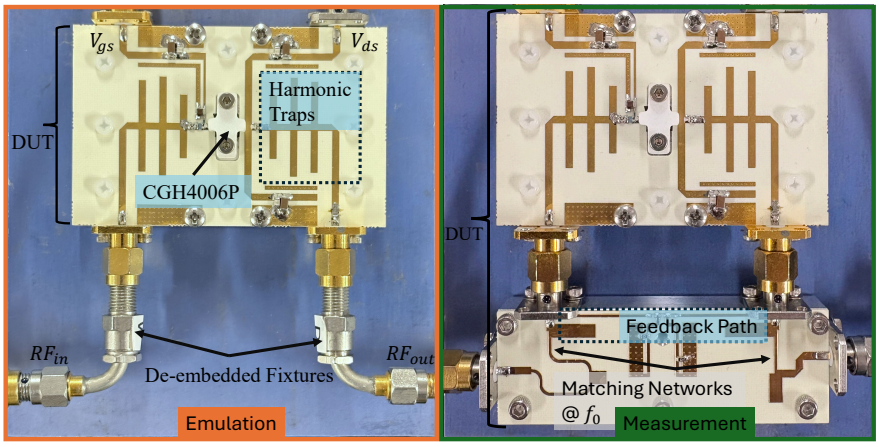



Figure 5.11: The DUT along with de-embedded fixtures (emulation case) and the physical matching network (measurement case), providing the two cases for validating the network emulation approach.

in disagreement between the measured and emulated circuit responses. These $S$-parameters are used in the emulation case to obtain the results detailed below.

To test the accuracy of the proposed emulation algorithm, an available source power sweep is applied to the circuit of Fig. 5.11. The signal used to excite the circuit is the 309 MHz, 300-tone signal used in the two-port circuit example of Section 5.2. The PAPR of the signal is 6.5 dB, and the average available source power is swept from -6.5 to 23.5 dBm. Measurement is performed first with the physical passive network attached to the DUT. Wideband active source and load pull are used to minimize mismatch from the system and perform source leveling during measurement.

Following the measurement, the physical network is removed from the DUT, and the fixtures are connected to the DUT. The fixture $S$-parameters are provided to the measurement system for *in-situ* de-embedding. Then the network $S$-parameters are loaded into the emulator, and the associated external and internal port assignments are established. External ports are assigned to a network port index, signal excitation, $\mathbb{S}_0$, and impedance, $Z_0$. The RF input external port is loaded with the signal from the measurement test while the RF output external port is loaded with a null signal, i.e. $\mathbb{S}_0 = 0$. The internal ports are assigned to a network port index and tuner equivalent source instance. Once initialized, the network is emulated on the DUT using the

procedure outlined in Fig. 5.9. Between emulations, the available source power of external port one is iteratively updated from -6.5 to 23.5 dBm.

### 5.4.2 Results

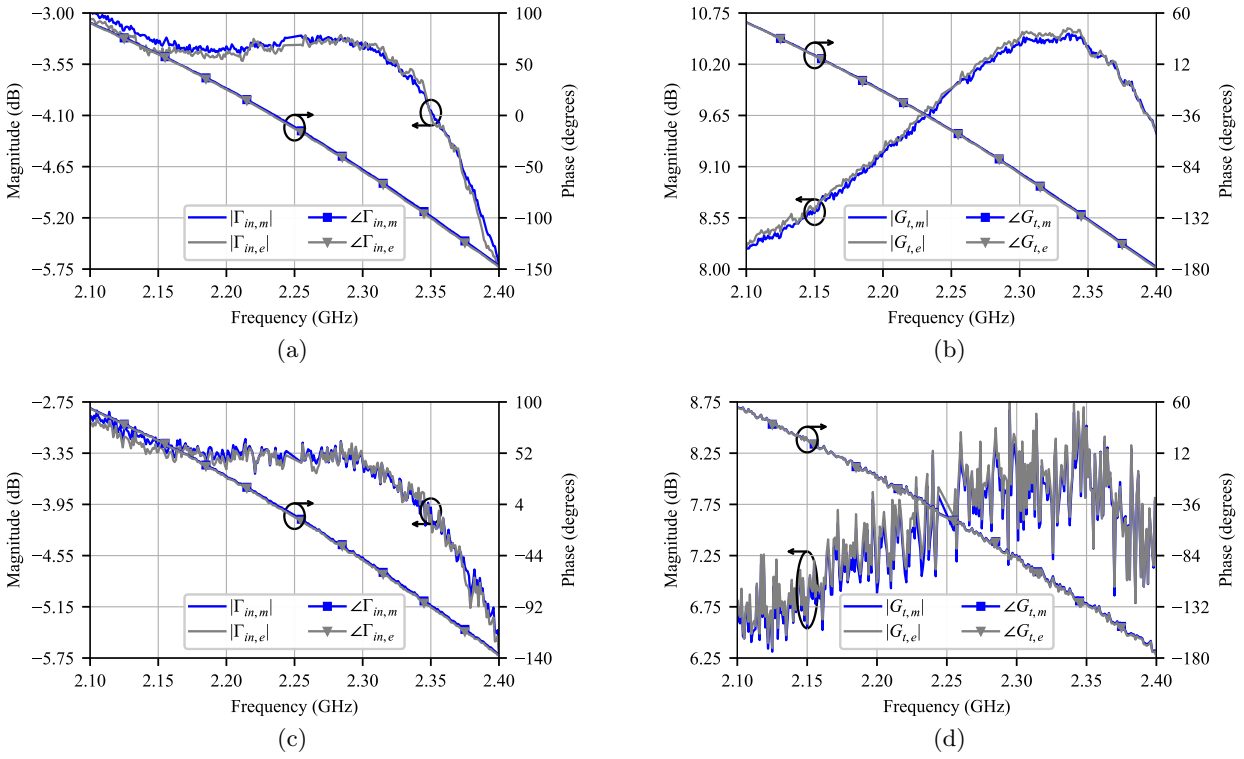



Figure 5.12: Comparison of the observed input reflection coefficient, $\Gamma_{in}$, and transducer gain, $G_t$, for each tone in the signal excitation. (a) and (b) reflect the behavior in small-signal ($P_{avs} = -6.5$ dBm) while (c) and (d) reflect the behavior of the circuit in large signal ($P_{avs} = 23.5$ dBm). Measurement results are plotted with a blue trace and the $m$ subscript. Likewise, results from emulation are demarcated with a gray trace and $e$ subscript.

Fig. 5.12 compares the measured and emulated behavior of the circuit across frequency for average available source powers of -6.5 and 23.5 dBm. Figs. 5.12a and 5.12c illustrate the input reflection coefficients of the circuit with maximum relative errors of 4% and 4.2%, respectively. Likewise, Figs.5.12b and 5.12d compare the transducer gain with corresponding maximum relative errors of 3% and 2.9%, respectively. These traces correspond to the instantaneous response of the circuit over the entire signal excitation. The noisy appearance of the gain magnitude in Fig. 5.12d

is due to in-band inter-modulation products.

Fig. 5.13 reports circuit performance of the emulated and measured results for the power sweep. Table 5.2 summarizes the bounds on the relative and absolute errors between emulation and measurement. Fig. 5.13a reports the DC power consumption of the DUT during emulation and measurement. The corresponding variation in drain current is less than 1 mA at all power levels. Fig. 5.13b-5.13d report the efficiency, transducer gain, and adjacent channel power ratio (ACPR).

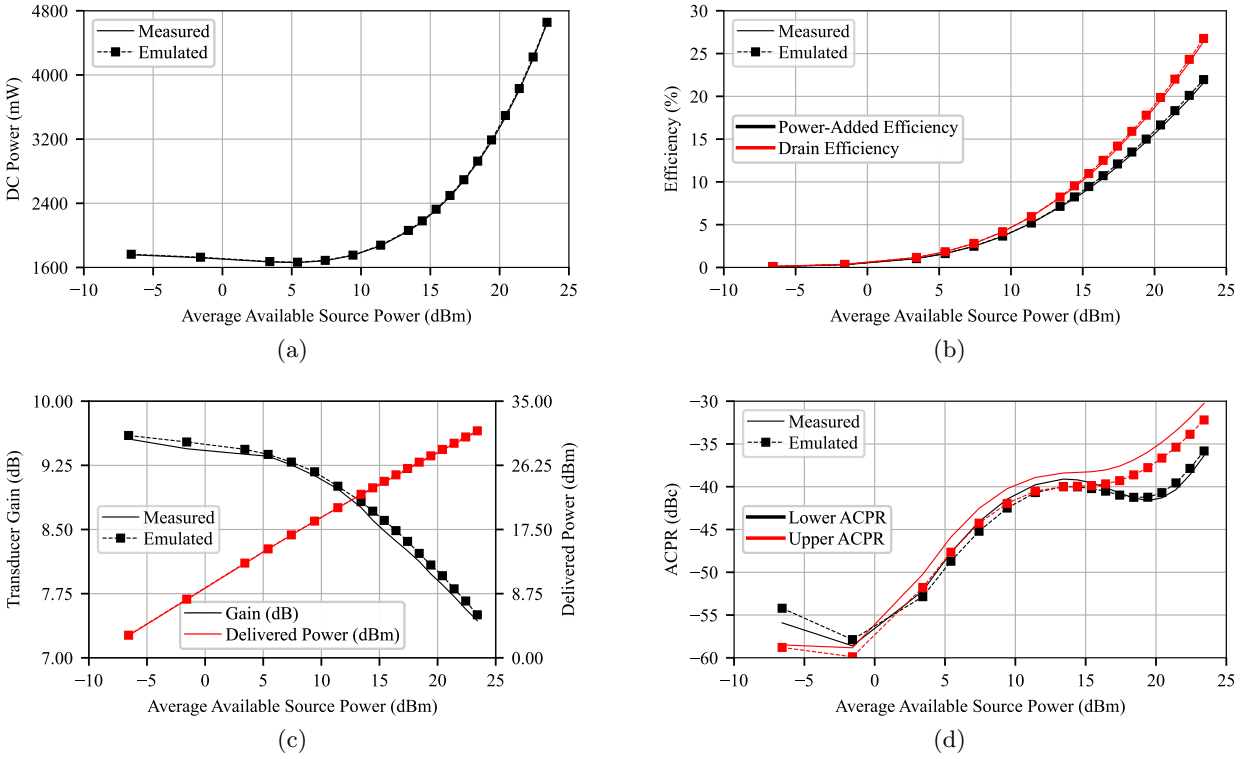



Figure 5.13: Comparison of the device under test under measurement and emulation for (a) dc power, (b) DE and PAE, (c) Gain and Delivered Power, and (d) ACPR. The results demonstrate excellent agreement backed off, at the compression corner, and in heavy compression.

## 5.5 Discussion and Conclusions

This chapter presents an approach to emulating high-frequency networks as an alternative path to circuit analysis. A tuner equivalent source determines an appropriate value for $A_0$, which results in the same power waves as an equivalent system with excitation $\mathbb{S}_0$ and physical reflection

Table 5.2: Error between emulation and measurement in power sweep.

| Measurement (unit) | Absolute (unit) | | Relative (%) | |
|---|---|---|---|---|
| | min | max | min | max |
| Drain Current (mA) | 0.15 | 0.89 | 0.25 | 0.72 |
| DC Power (mW) | 3.52 | 24.92 | 0.20 | 0.72 |
| Gain (dB) | 0.02 | 0.12 | 0.23 | 1.47 |
| Delivered Power (dBm) | 0.02 | 0.12* | 0.12 | 1.33 |
| PAE (%) | 0.00 | 0.42† | 0.11 | 2.84 |
| Drain Efficiency (%) | 0.00 | 0.40† | 0.06 | 2.36 |
| Lower ACPR (dBc) | 0.07 | 1.70* | 0.17 | 3.04 |
| Upper ACPR (dBc) | 0.30 | 1.93* | 0.51 | 6.38 |

* dB † pp
Absolute errors are rounded to two decimal places.

coefficient, $\Gamma_S$. Next, the network equivalent source determines what the excitation $\mathbb{S}_0$ should be in the tuner equivalent source if the system is replicating physical network behaviors such as coupling, loss, and dispersion. Finally, the measured $a, b$-waves at the DUT plane are embedded within the larger networks to determine the response at the external plane(s) of the circuit.

Both small and large signal examples are provided to demonstrate the viability of the approach. First, a simple demonstration comparing emulator performance against small signal simulations of a single-stage amplifier with lossy and dispersive networks over a 300 MHz instantaneous bandwidth is shown. The relative error is less than  for both $s_{11}$ and $s_{21}$ across the bandwidth of analysis.

A second, large-signal, demonstration is also presented, which compares emulated results to measured results over the same 300 MHz bandwidth. To accommodate limited test and measurement hardware, baseband and harmonic traps are used to ensure that the corresponding terminations do not change between the measurement and emulated test conditions. The emulated network is a matching network with a feedback network to demonstrate the procedure's capacity to accommodate phenomena such as electromagnetic coupling and intentional feedback. The circuit, i.e., network plus DUT, is then assessed through direct measurement and through emulation. The results of this analysis demonstrate excellent agreement in dc power consumption, efficiency,

delivered power, gain, and ACPR which, except in the case of the upper ACPR, does not exceed a relative error of 3.1%.

The purpose of this chapter is to present a fundamental and general approach towards microwave network emulation. Ongoing and future research efforts are presently directed towards expanding the scope of this algorithm towards harmonic and baseband microwave network emulation, introducing near-band impedance control (presenting the network impedance at tones adjacent to the signal), and the virtualization of multiple devices to emulate larger systems, e.g., a multistage amplifier, load-modulation (i.e., Doherty), or array of transmitters.

# Chapter 6

## Emulation of Load Modulated Power Amplifiers

This chapter describes how to enable the design and test of load-modulated power amplifier (PA) architectures using network emulation on an active load pull test bench. Here we show a technique to load modulate a single transistor with a black box load modulator. This can be used, for example, for characterizing a single branch of a classical load-modulated architecture, e.g., Doherty. Additionally, however, this can be used to synthesize arbitrary load modulation trajectories which may or may not be physically realizable with a practical load-modulated PA. In this chapter, a load modulation trajectory refers to the change in $Z_L$ as a function of $V_{out}$. In general, this is different for each branch of a load-modulated PA. Typically, only the real part of $Z_L$ changes to ensure maximal voltage swing. The theory presented within is general and can work for any conceivable trajectory, provided the measurement hardware can faithfully reproduce it. Some practical limitations will be discussed within.

The goal is to show how emulation and active tuner theory handle the addition of an additional excitation applied to the DUT, like that shown in Fig.6.1. This is demonstrated with load modulation due to system limitations; the physical hardware is limited to the fundamental frequencies, and classical load modulation does not require harmonic/baseband frequency control. The general concept of applying an additional excitation for efficiency/linearity improvement demonstrated here can be directly applied to other architectures, such as gate/drain modulation, harmonic injection, array loading, and any MISO/SIMO/MIMO architecture. In the case of fundamental only load modulation, demonstrated here, a desired load-modulation trajectory is specified

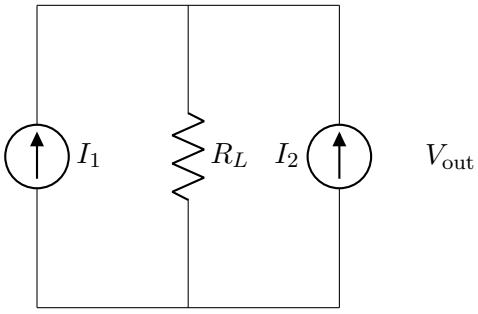



Figure 6.1: Load modulation with two current sources driving a common load. Note that, in general, $I_1$ and $I_2$ may be at different frequencies.

as a function of output voltage, and the secondary source providing the actively synthesized load impedance can be used to synthesize a load impedance that is a function of the instantaneous output power. Results are demonstrated using the load-modulation trajectory of the Doherty main branch using a Cree CGH4006P 6 W packaged GaN transistor, which demonstrates an RMS error in the synthesized impedance trajectory below 1 % for a 20 MHz 2-tone signal.

## 6.1 Principles of Wideband Arbitrary Load Modulation (WALM)

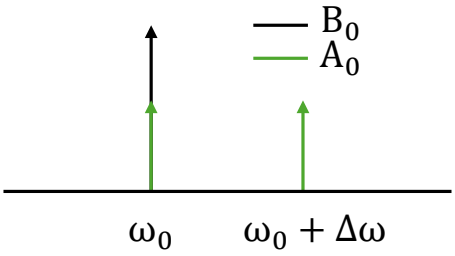



Figure 6.2: CW RTALP demonstration showing the frequency domain response required to achieve a time-variant $\Gamma_L$, which can be utilized to obtain load pull data instantaneously, without the need to measure at every point discretely.

Load modulation is an excellent demonstration of active load pull and of network emulation's ability to be used as a design tool beyond transistor characterization. However, it may not be immediately apparent how to achieve a time-varying $\Gamma_L$. The next section will discuss a well-known CW technique to achieve this.

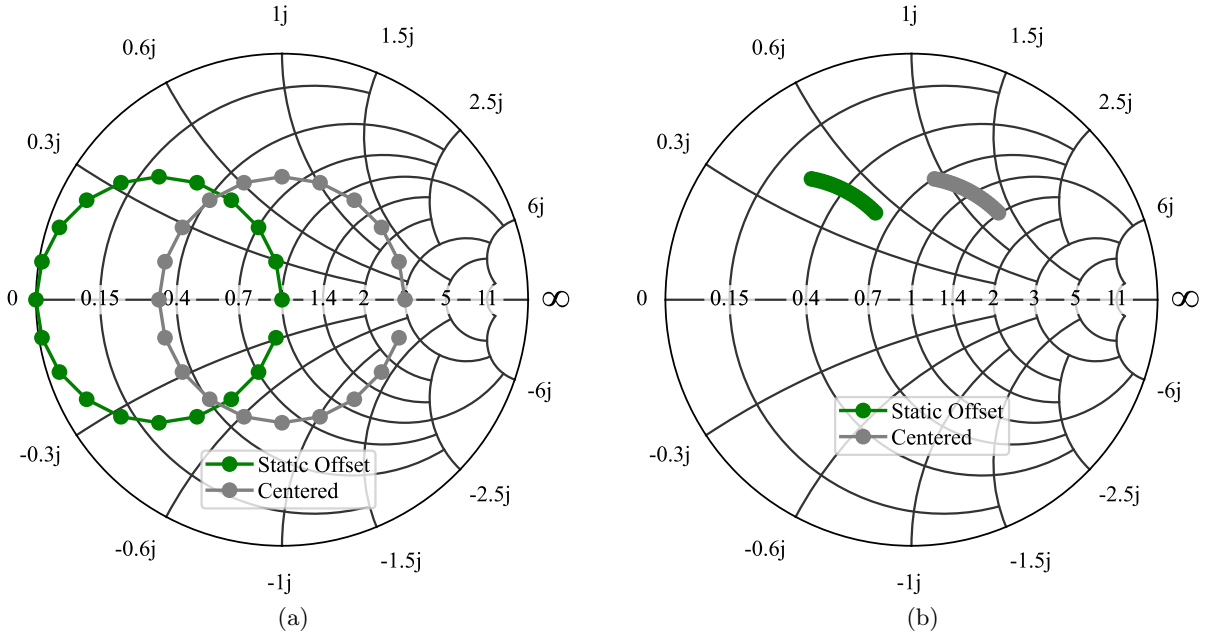



Figure 6.3: (a) full contour circles of simulated RTALP constellations (gray) with no static offset and (green) with some static offset $\Gamma_L$ applied. (b) demonstrates partial contour circles obtained by reducing $\Delta\omega$ to below the inverse of the system acquisition time. Additionally, in (b), $\phi_2 = \frac{\pi}{4}$ to provide some offset from the real axis.

### 6.1.1 Real Time Active Load Pull

Open-loop active load pull can be thought of as injecting a coherent version of the signal multiplied by a complex constant out of the PA back into the DUT to achieve a desired $\Gamma_{in}$ of the load:

$$b_1 = \Gamma_{in} a_1 \tag{6.1}$$

Note that here all $a, b$ waves are referred to some network after the DUT, and the port connected to the DUT is referenced as port 1. As a result, the reflection coefficient referenced is looking into the network ($\Gamma_{in}$) and not the reflection coefficient presented to the transistor ($\Gamma_L$). Wideband and frequency-dependent $\Gamma_{in}$ are well-documented extensions to basic CW active load pull [40, 67, 70]. Arbitrary load-modulation is an extension of this, where $\Gamma_{in}$ is now a function of output RF voltage. Practically, this requires a time-variant $\Gamma_{in}$. Prior works have discussed how to

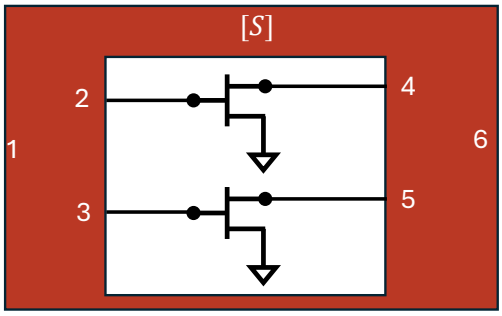
achieve a time-variant reflection coefficient in the context of emulation of load modulation [36,47,83], but do not provide a detailed description of the mechanisms to achieve it. Additional considerations, such as bandwidth and dynamic range reduction, are also not discussed.

A concept known as *Real-Time Active Load Pull* (RTALP) is introduced in [95, 111], which uses a frequency slightly offset from the fundamental to create a time-variant load impedance, and provides a basis for the WALM technique. The major advantage of RTALP is that data from multiple impedance points can be captured in a single measurement, compared to individual measurements at each point in the load pull constellation. The basic CW RTALP equation for determining the necessary $b_1$ is:

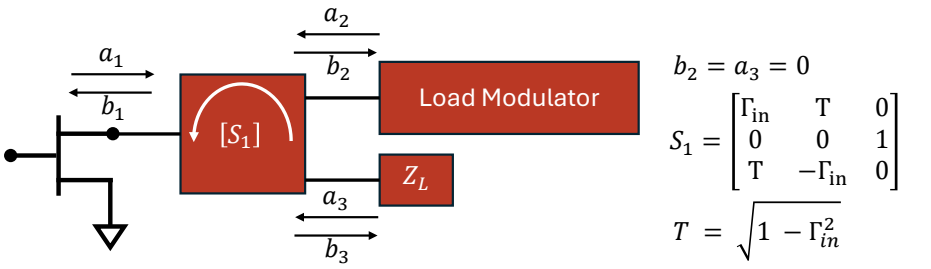
$$b_1 = M_1 e^{j(\omega_0 t + \phi_1)} + M_2 e^{j[(\omega_0 + \Delta\omega)t + \phi_2]}$$

The first term is the same as in active load pull, with $M_1, \phi_1$ determining the magnitude and phase of the synthesized *static* $\Gamma_{in}$, respectively. The second term introduces a secondary tone offset from the fundamental by some positive $\Delta\omega$. The value of $\Delta\omega$ is arbitrary and determines how quickly $\Gamma_{in}$ will change in time. $M_2$ determines the magnitude of the *dynamic* $\Gamma_{in}$ traced about the static $\Gamma_{in}$ point. $\phi_2$ determines the offset of the dynamic trajectory from the real axis. A frequency domain representation of the waveforms is shown in Fig.6.2.

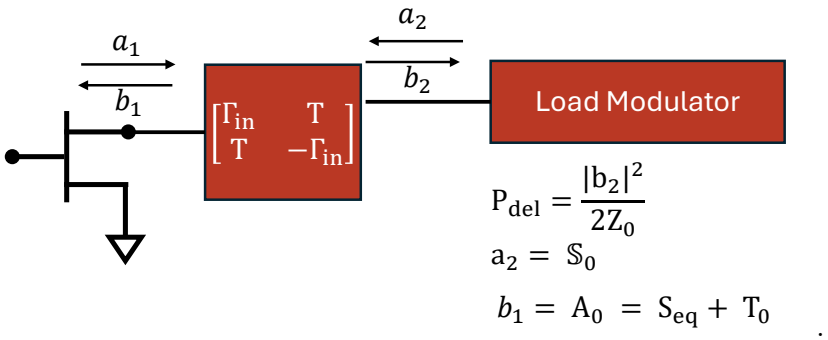
This can be useful if $\Delta\omega$ is less than the inverse of the system acquisition time (usually specified by the tone spacing). In this case, a partial circle can be drawn on the Smith chart, centered about the static point, with length specified by $\Delta\omega$ and starting from an angle specified by $\phi_2$. This can be seen in Fig. 6.3 where (a) shows full contours which can be instantaneously measured (green) with and (gray) without a static offset. Fig. 6.3b shows a similar case with a much smaller $\Delta\omega$ to trace a partial trajectory, with $\phi_2 = \frac{\pi}{4}$ to provide some rotation. Note that this leads to interesting questions regarding the impacts of relatively slow dynamic nonlinear effects (bias, memory) on the measurement results obtained from a load pull system, which presents a $\Gamma_{in}$ varying proportionally to $\Delta\omega$, but will not be discussed here.




(a)




(b)




(c)

Figure 6.4: (a) generic load modulated architecture with two active devices connected through a non-isolating output combiner. (b) An equivalent circuit for one of the devices in a load-modulated architecture, e.g., the Doherty main branch. (c) A further simplification of (B), which can be readily realized with a wideband active tuner.

### 6.1.2 WALM Theory

The realization that a varying $\Gamma_{in}$ can be achieved by applying an excitation at the output ($b_1$) which has different frequency content from the PA ($a_1$) provides the key for wideband arbitrary load-modulation (WALM) as well as some challenges which are described in detail.

To understand the utility of this technique, it is useful to start with a general block diagram of a load-modulated PA, shown in 6.4a. Two active devices are connected through a 6-port linear network. Load modulated architectures can be more complicated, e.g., the load modulated balanced amplifier [101] and Chireix outphasing [8], but this represents the most basic system. In general, the input network is isolating ($s_{23} = s_{32} = 0$), and the output network is non-isolating so that $s_{45} = s_{54} \neq 0$, which enables the devices to interact and therefore change the $\Gamma_L$ seen by each of the devices. For analysis, this can be challenging because both the matching and the load modulation are tightly coupled and dependent on the specific active devices in both branches.

Instead, we can look at the impact that load modulation has on a single device using a system like that shown in Fig.6.4b, where the DUT is a single transistor, connected to an arbitrary load-modulator and an ideal load through an element which functions like a circulator and also presents some power-invariant reflection coefficient, termed $\Gamma_{L,stat}$ to the DUT. This is advantageous because it simplifies the problem to a single DUT and allows for the load-modulation, termed $\Gamma_{L,dyn}$ and power-invariant $\Gamma_{L,stat}$ to be varied independently. For example, a "trajectory-pull" could be performed with the arbitrary load-modulator outputting a variety of trajectories to determine which yields desired performance. Alternately, the trajectory can be fixed, with the $\Gamma_{L,stat}$ swept to the best match under load-modulated conditions. The load pull and trajectory pull sweeps can additionally be nested to fully characterize the DUT under load-modulated conditions. Provided that the trajectories are constrained to those that can readily be achieved with a physical load-modulator, the WALM approach provides a valuable intermediate design step in the design process, which is not readily available with current simulation tools. Additionally, as with network emulation, this process is essentially excitation signal agnostic, provided the measurement hardware has sufficient bandwidth and dynamic range.

The block diagram of Fig.6.4b can be further simplified with a few assumptions. If the load-modulator and system termination are both matched to $Z_0$, then $b_2, a_3 = 0$. Therefore, we can connect ports 2 and 3 with no loss of functionality. The linear combiner and matching network is simply a tuner cascaded with an ideal circulator. Since $b_2, a_3 = 0$, $S_1$ reduces to:

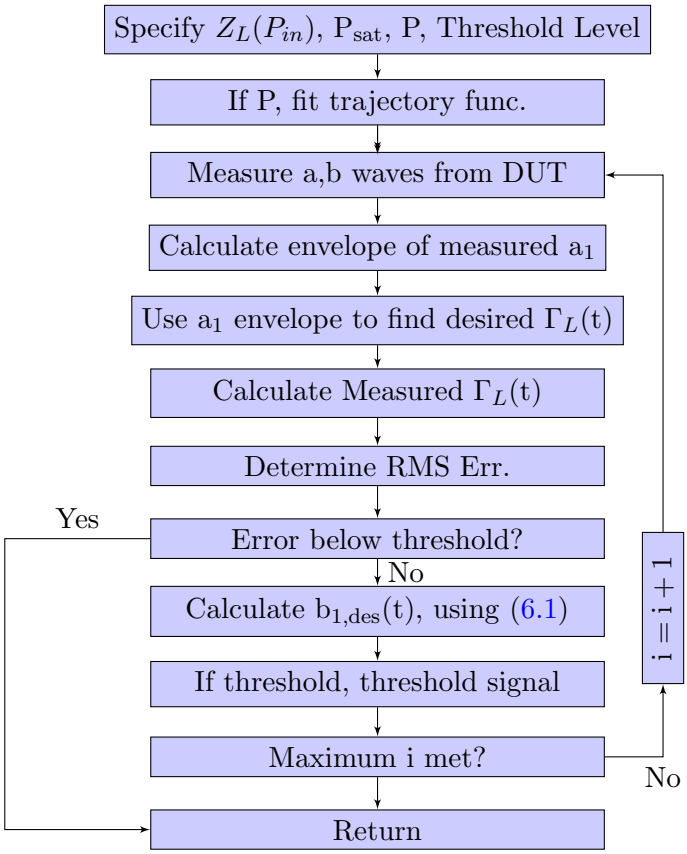



Figure 6.5: WALM procedure.

$$\begin{bmatrix} \Gamma_{in} & T & \emptyset \\ \emptyset & \emptyset & 1 \\ T & -\Gamma_{in} & \emptyset \end{bmatrix} = \begin{bmatrix} \Gamma_{in} & T \\ T & -\Gamma_{in} \end{bmatrix}$$

which is simply the $S$-matrix of an ideal tuner. Therefore, we can use the further simplified diagram of Fig.6.4c to characterize a DUT operating under load-modulated conditions fully. Note that this is identical to the network equivalent source introduced in [41]. Therefore, we can now use that framework. This is a convenient abstraction since the tuner from Ch.5 already accounts for two excitations comprising the impressed wave ($A_0$), $T_0$, and $S_0$. We can therefore use $T_0$ to represent the necessary injected signal to achieve the power independent load and then iterate to determine the necessary $S_0$, the signal from the arbitrary load modulator, to converge to the desired trajectory.

We label this method wideband arbitrary load-modulation (WALM) to emphasize that any load-modulation trajectory, even active trajectories, are possible for periodic modulated signals.

The analysis herein is done at an arbitrary 2.25 GHz with a 10 MHz IBW two-tone. The WALM method is independent of center frequency and instantaneous bandwidth, limited only by the hardware on which it is performed.

The procedure for emulating an arbitrary power-dependent load is outlined in Fig.6.5. Firstly, a desired load trajectory must be specified along with a fixed value for the saturated output power of the transistor. Next, the power delivered from the amplifier is measured, and the envelope is calculated. At each time step of the envelope, the specified $Z_L(V_{out,inst})$ is used to construct a desired $\Gamma_L(t)$ trajectory. Note that it is desired to have the $\Gamma_L(t)$ vary with the envelope of the signal and not the RF carrier for load-modulation applications. Thus, we can use (6.1) to determine the $\mathbb{S}_0$ necessary to inject into the DUT.

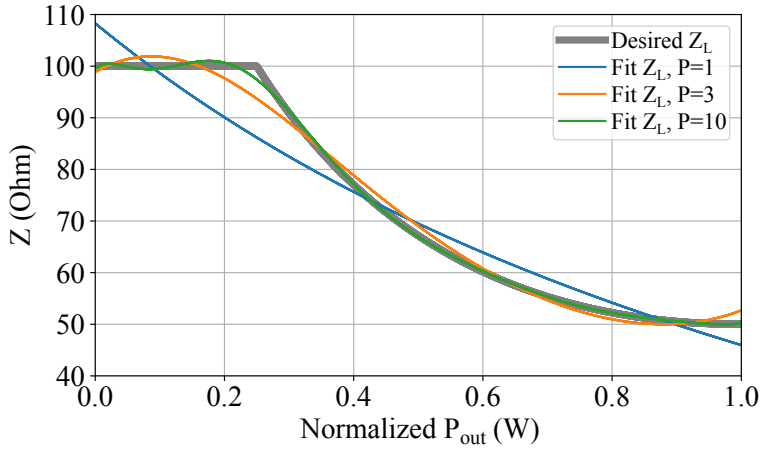



Figure 6.6: Doherty-like load modulation trajectory (gray), exact and (blue, orange, green) when fit using polynomials of order 1, 3, 10, respectively. The low-order approximations recreate the trajectory less faithfully, while reducing the necessary system bandwidth and dynamic range requirements.

To prove this technique, we begin by using the trajectory seen by the main branch of a

Doherty PA, shown in Fig.6.6 and defined by:

$$Z_L(V_{in}) = \begin{cases} Z_0(4(V_{in,n}-1)^2+1) & V_{in,n} >= 0.5 \\ 2 * Z_0 & V_{in,n} < 0.5 \end{cases}$$

where,

$$V_{in,n} = \frac{V_{in}}{V_{MAX}}$$

and $V_{MAX}$ being the highest expected voltage for the DUT.

Next, simulations with a 2-tone signal are performed, with Fig.6.7 showing the main envelope, the derived $Z_L(t)$, and the necessary $\mathbb{S}_0$ envelope. It is readily apparent that the $\mathbb{S}_0$ has a significantly expanded bandwidth compared to the input two-tone. This bandwidth expansion presents a practical limitation to the WALM approach. Seen in Fig.6.8a, the Doherty trajectory introduces an infinite bandwidth expansion to the signal to be injected. This bandwidth expansion must be managed to enable practical WALM on current measurement equipment.

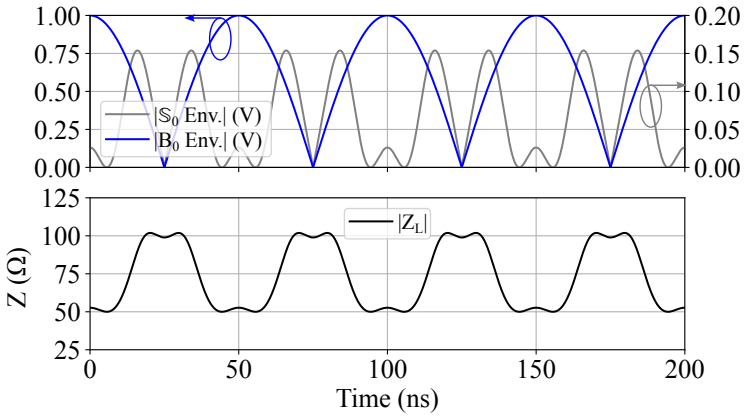



Figure 6.7: Main and auxiliary waveforms necessary to achieve a Doherty operation mode using a 3rd order approximation and a 20 MHz two-tone signal.

#### 6.1.2.1 Bandwidth Reduction

Two approaches to bandwidth reduction are explored. The first is a simple frequency domain thresholding approach, and the second involves polynomial-fitting the load-modulation trajectory.

Table 6.1: RMS errors for different polynomial fit orders.

| Poly. Order | 1 | 3 | 5 | 7 | 9 |
|---|---|---|---|---|---|
| RMS Err. (Ω) | 5.08 | 1.74 | 1.20 | 0.73 | 0.45 |

Table 6.2: RMS errors for different signal thresholds.

| Threshold Level (dB) | 10 | 20 | 30 | 40 | 50 |
|---|---|---|---|---|---|
| RMS Err. (Ω) | 3.5 | 0.66 | 0.12 | 0.02 | 0.06 |

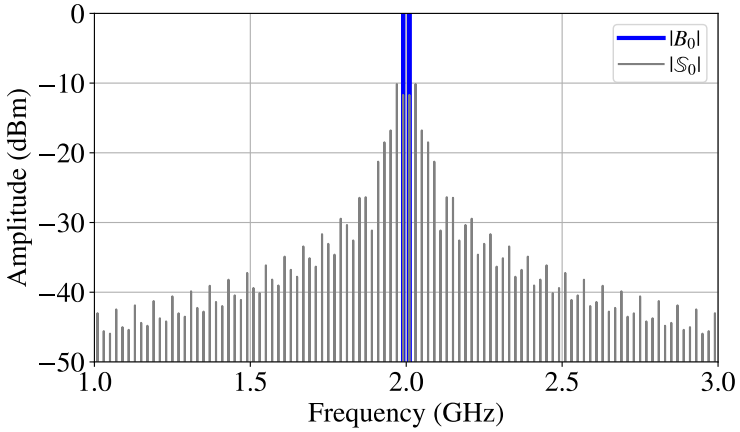
The spectrum in 6.8a can be readily reduced in both bandwidth and required source dynamic range by omitting tones below a certain threshold relative to the maximum. For example, a 10 dB threshold would limit the bandwidth expansion to a relatively modest 4x increase for a two-tone signal. The error for thresholds from 10–50 dBc are shown in Table 6.2 for a two-tone signal. This bandwidth is still significant and limits the applicability of WALM to measurement systems with IBWs much wider than the expected signal bandwidth. However, an RMS error of 0.12Ω for a 30 dB threshold represents low error with a reasonable dynamic range readily achieved in most measurement systems.

The second approach involves approximating the load-modulation trajectory using a polynomial fit. This can be seen for a variety of polynomial orders in Fig.6.6. The errors can be seen in Table 6.1 for a two-tone signal, and the output for a 3$^{\text{rd}}$ order fit can be seen in Fig.6.8b. The bandwidth expansion in this case is still significant and is expressed as:

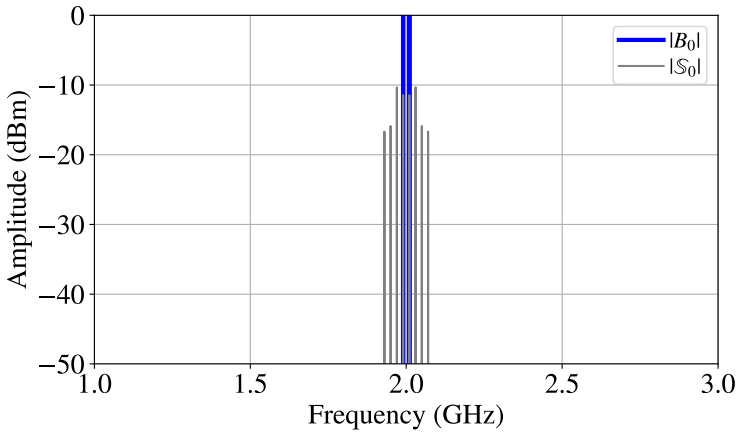
$$BW_{walm} = (P+1)BW_0$$

where $\text{BW}_{\text{walm}}$ represents the bandwidth necessary to recreate the fit trajectory, $\text{BW}_0$ is the original signal bandwidth, and $P$ is the polynomial order. As expected, if the polynomial order is 0, representing a static load, the bandwidths are equal.

Compared to thresholding, the polynomial fit has some significant advantages. Firstly, the exact trajectory is known a priori, i.e., the thresholding is applied to the output signal, whereas




(a)




(b)

Figure 6.8: Spectrum of simulated two-tone signal and necessary auxiliary signal to achieve the (a) ideal and (b) 3$^{rd}$ order polynomial fit for a Doherty load-modulation trajectory shown in Fig.6.6

the fit function is applied to the desired response. Additionally, the approximation is well defined. Fig.6.9 compares the instantaneous (a) resistance and (b) reactance for a 20-tone signal. The thresholded approximation is strongly dependent on the envelope and does not follow a well-defined path. The fit trajectory is consistent and additionally does not introduce any undesired reactance. However, the figure demonstrates that for a similar approximation complexity, the thresholding offers a more faithful representation of the desired trajectory.

In practice, in our system, both methods are present. The function is first poly-fit to reduce the bandwidth and dynamic range requirements of the injected WALM signal, and a secondary

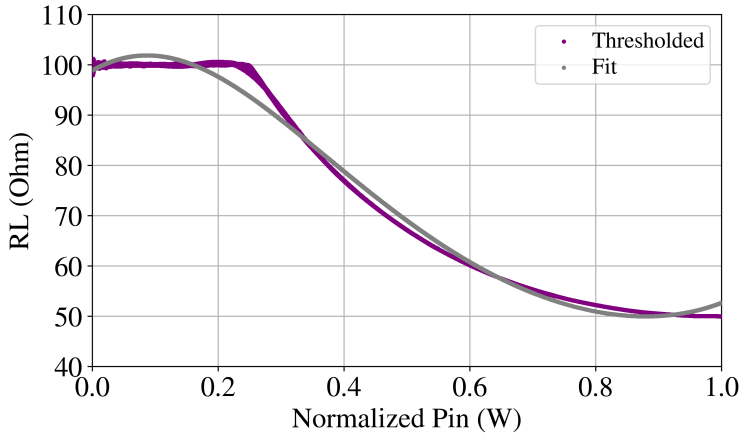
thresholding is intrinsic to the active load pull implementation to avoid causing convergence issues in the active tuners due to tones below the system's capability to reasonably control. Additionally, later, the impact of noise on the measured response will be discussed. It is also important to note that both techniques must be considerate of the underlying hardware. For example, specifying a threshold of -110 dBc is unachievable by most test and measurement equipment, with a more achievable threshold set either explicitly or implicitly by another aspect of the hardware. Similarly, even if the system bandwidth can support a eg. $10^{\text{th}}$ order fit of the trajectory, note that in Fig.6.8a the tone amplitudes of $\mathbb{S}_0$ decay exponentially away from $f_0$ and will encounter a similar implicit dynamic range limitation imposed by the hardware.

## 6.2 Validation Measurements

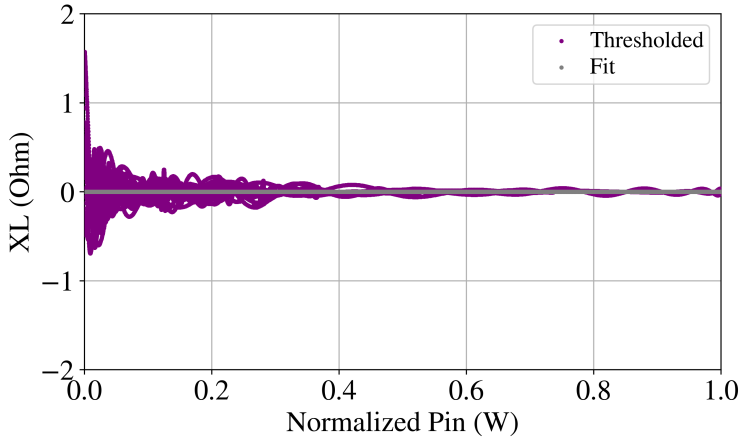
After validating the veracity of the technique through simulation, measurements using the experimental setup described in Chapter 5 are performed using the same 2-tone signal with a bandwidth of 20 MHz at a $f_0$=2.25 GHz. The DUT is again the MACOM CGH4006P 6 W GaN-on-SiC transistor embedded within a linear network consisting of harmonic traps and bias tees at both the gate and the drain. The load modulation trajectory chosen to emulate is that of the Doherty main branch, fit with a $3^{\text{rd}}$ order polynomial approximation. Since the device is unmatched, some static $\Gamma_L$ must be applied first to match the device.

The resulting $\mathrm{R_L}$ and $\mathrm{X_L}$, plotted as a function of time, are shown in Fig.6.10, which shows good agreement with the expected value, with the notable inclusion of some undesired reactance. A similar trend is observed in Fig.6.11, which demonstrates good convergence to the correct trajectory and a small measured reactance at low power levels. Note that these are shown embedded after the matching network and therefore do not include the influence of the power independent portion of $\Gamma_L$, but only the component from the load modulator. Additionally, the shape of $R_L$ in time has a slightly different shape compared to Fig.6.7. This is because the trajectory applied is referenced to $V_{out}$, which, near $P_{sat}$, includes some nonlinear distortion from the DUT.

To explain the reactance and why it occurs in the measured results despite having chosen the



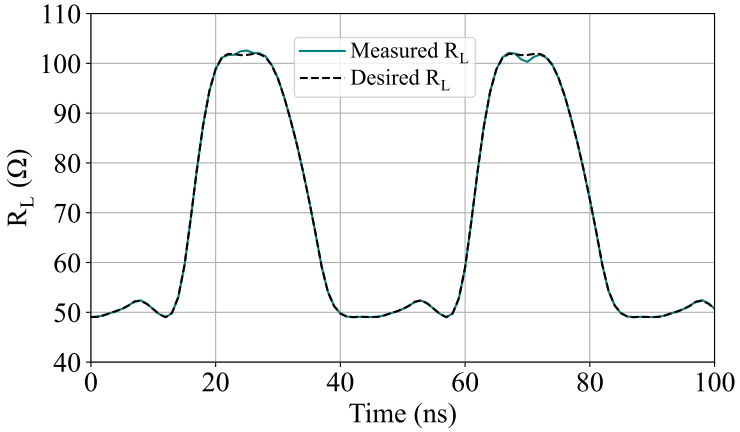

(a)



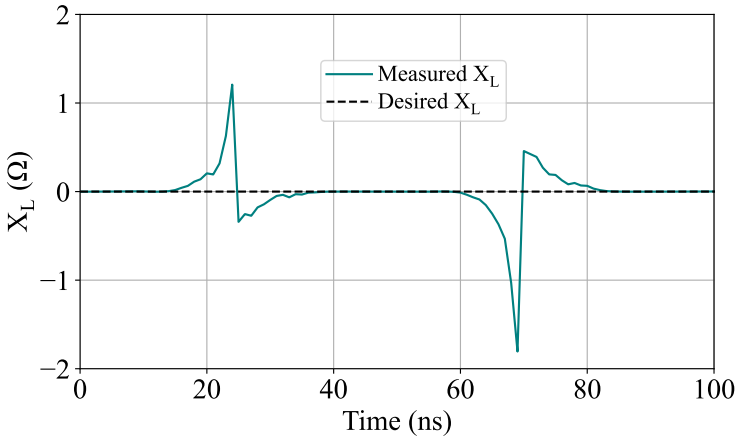

(b)

Figure 6.9: Thresholded and Polyfit Doherty trajectory showing a trade-space between the two approaches. The thresholding approach more closely approximates the Doherty trajectory. However, the thresholding approach has more random variation and introduces a time-varying reactance.

polynomial fitting method to reduce the problem complexity, which does not impact the imaginary part of the $\Gamma_L$, we must consider an additional phenomenon, which was not accounted for in the earlier simulations, noise. In this analysis, we model the noise as Gaussian white noise, representative of both thermal and quantization noise. A two-tone signal is created to represent some ($a_1$) and then is multiplied by some real constant to create an ($b_1$). Then gaussian white noise is added to both signals, and a noisy $\Gamma_L$ can be found. This is plotted in Fig.6.14, which demonstrates the exact behavior that is observed in Fig.6.11b. Note that the system noise will also be present in the real component of $\Gamma_L$. This demonstrates that in a lossy system, the trajectory near zero power




(a)




(b)

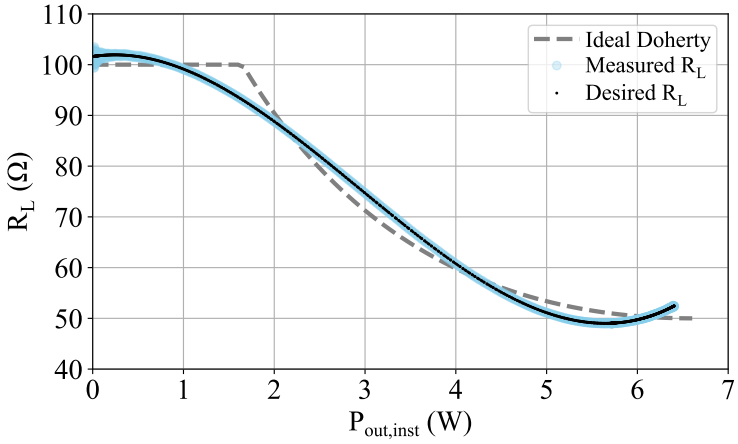
Figure 6.10: Two tone measured (a) $R_L$ and (b) $X_L$ in time.

will have significantly more variation from the ideal case when compared to higher power levels. A few important takeaways:

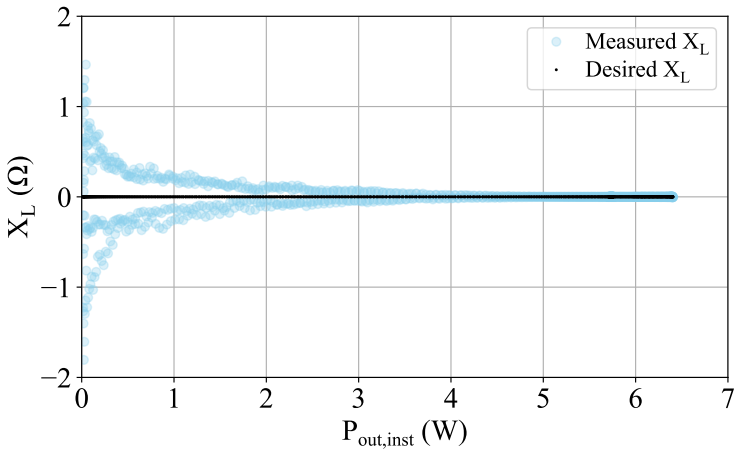
(1) The measured response is a worst-case estimate as it includes both the noise added by the sources and the receivers; and

(2) this phenomenon will also be present in a real load-modulated architecture.

Finally, we can look at the $\Gamma_L$ measured at both the internal (between the transistor and the matching network) and external (after the matching network, assuming $Z_0 = Z_L$) reference planes. These are shown in red and black, respectively, in Fig.6.13, and show that the load trajectory is




(a)

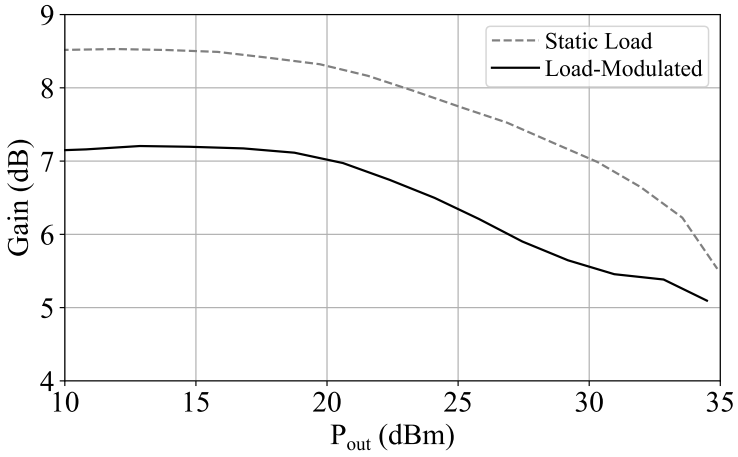



(b)

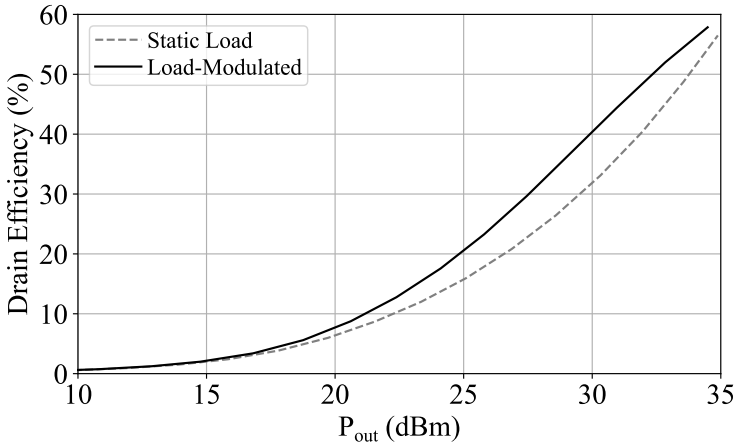
Figure 6.11: Two tone measured (a) $R_L$ and (b), $X_L$ with (grey-dashed) the ideal Doherty trajectory (black) a third order approximation and (blue) the measured response as a function of instantaneous output power. Note that in (b), the fit and ideal case are equivalent, and therefore, the ideal is not shown.

correct at both planes, with the external following the specified trajectory and the internal being $\Gamma_{L,stat} + \Gamma_{L,dyn}$. Note that the external reflection coefficient is more ideal than what is measured at the internal plane. This is due to a current limitation in the implementation of the network emulation.

When the DUT response is transformed to the response at the external plane (after the matching network), $a, b$ at the internal plane, and $S$ are known, and we would like to solve for $a, b$ at the external plane. However, the $S$-parameters are defined as:




(a)




(b)

Figure 6.12: Two-tone measured (a) gain and (b) $\eta$ as a function of average output power for both the static and load-modulated cases.

$$b = \mathbf{S}a$$

To more readily solve this for the external waves, the external excitation ($a$) is assumed to be known. Since $S$ and $a$ are assumed to be known, it becomes straightforward to solve for $b$. This is reasonable because the explicit convergence steps ensure that the error in the external $a$ is minimized. The second assumption made is that the load impedance must be equal to the reference of the system, e.g., $50\,\Omega$. ABCD parameters are a common solution to this type of problem, but are limited to 2-port networks. There are sufficient known variables to fully solve this problem, but

the implementation remains future work.

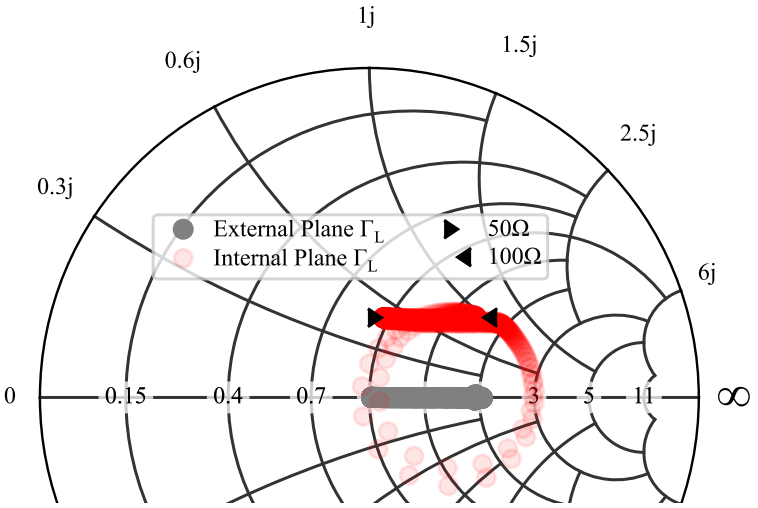



Figure 6.13: $\Gamma_L$ trajectory shown at both the (black) external, and (red) internal planes of the device.

After validating that the load modulation is being applied correctly, we can look at metrics such as drain efficiency ($\eta$) and gain to validate that the response has changed between applying a power invariant load and load modulation. As seen in Fig.6.12a, the gain is different by $> 1\,dB$ at low power levels, while converging to the static case near $P_{sat}$ as expected. Note that the gain convergence at $P_{sat}$ results from using the same $\Gamma_{L,stat}$ in both cases; in a real load modulated design, the $\Gamma_{L,stat}$ would likely be changed to improve overall performance. Additionally, Fig.6.12b demonstrates an improvement in $\eta$ of 8 percentage points (pp) at an average $P_{out}$=30 dBm while converging within 2 pp near $P_{sat}$. More efficiency enhancement could be achieved with a different choice for $\Gamma_{L,stat}$, but this example nevertheless demonstrates the WALM technique.

## 6.3 Conclusion

This chapter presents a novel arbitrary load modulation characterization tool based on measurements of a physical transistor, termed WALM. This technique can be utilized after obtaining a static matching impedance from simulation or load pull measurements with a "trajectory pull", or synchronously to determine both the static match and dynamic trajectory desired. This ap-

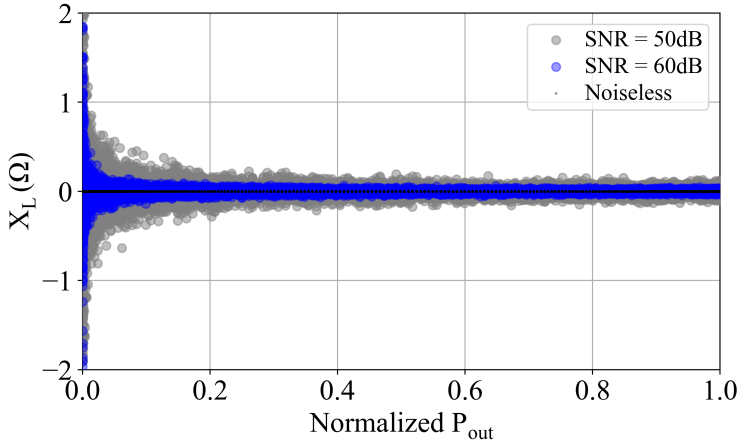



Figure 6.14: Reactance for a simulated static, purely real, $\Gamma_L$ across $P_{out}$, using a two-tone signal, demonstrating that SNR of either the source or receivers causes ambiguity in the measured response at low output power levels.

proach opens new avenues in design for load modulation by allowing for the load modulator to be treated as a black box to be realized independently. Additionally, while hardware limitations of the CU WALP bench prevent active injection of baseband or harmonic waveforms in addition to the fundamental, the concept of a virtual black box modulator opens avenues in other advanced PA architectures, such as gate and drain modulation.

We demonstrated that an arbitrary impedance trajectory can be readily synthesized coherently with the measured output of an active device using an injected signal with spectral content that differs from that of the original signal. Additionally, two techniques to account for the bandwidth expansion and dynamic range considerations that may be encountered with the signal to be injected are discussed. A simple frequency domain approach is discussed, which allows for realizable signals at the expense of determinism. Additionally, the trajectories may be fit to a $P^{th}$ order polynomial to constrain the bandwidth, resulting in slightly lower faithfulness to the original trajectory but a more repeatable response.

Measurements of the synthesized load modulation are demonstrated. Time domain responses validate that the measured response tracks closely with the desired response and includes the nonlinear content from the active device. The load trajectory is shown at the external reference

plane as well as the internal reference plane, which is not commonly accessible in measurements of load-modulated amplifiers. Finally, system-level parameters, gain, and $\eta$ are compared to the static load case, demonstrating higher efficiency and lower gain as expected.

# Chapter 7

# Conclusions and Future Work

## 7.1 Thesis Conclusion

This thesis addresses techniques for obtaining simultaneous linearity and efficiency in RF communications amplifiers from traditional RF to millimeter wave frequencies. Due to the large trade space and wide variety of applications that communications amplifiers are employed in, there is not one singular solution thus far, which has become a *de facto* design topology for these applications. Efficiency enhancement techniques, such as supply and load modulation, are explored for both low and high-frequency applications. Additionally, a classical linearity enhancement technique, gate modulation, is explored for wideband millimeter wave communications.

While the importance of advanced architectures to achieve simultaneous linear and efficient amplification cannot be overstated, there exists a gap between conventional design and characterization capabilities and the demands of modern wideband communications. In particular, harmonic balance, the most common nonlinear microwave circuit analysis method, is highly inefficient with broadband signals, requiring a large number of harmonics to be solved. Envelope analysis can be faster and more efficient with wideband signals, but it typically employs a quasi-static solution based upon harmonic balance results. A hardware-in-the-loop analysis framework, "network emulation", is presented and is shown to effectively predict nonlinear circuit performance under modulated excitation.

In general, designing a communications power amplifier entails a large number of trade-offs and compromises. Most commercial solutions utilize bespoke application-specific solutions.

This thesis therefore demonstrates a variety of advancements to efficiency/linearity and analysis techniques to present a broad overview of the trade space available to GaN-on-SiC PAs within a range of frequency bands.

## 7.2 Thesis Contributions

A summary of chapters 2-6 is provided below:

**Chapter 2:** This chapter presents two contributions to the field of drain modulation.

- The first is a technique to maximize the realized efficient enhancement achieved under discrete supply modulation with a fixed difference between the maximum and minimum voltage levels. The device periphery can be oversized, and then the device can be run at a lower drain voltage to achieve the $P_{out}$ specification. This enables a larger relative difference between the maximum and minimum voltage levels. To demonstrate this, a trade study of different peripheries in the WIN Semiconductors process is first presented. Next, two amplifiers are designed. The first is a conventional single-stage reference amplifier with a 4x100$\mu$m device, designed to use the maximum recommended drain voltage in the process, 28 V. The single-stage PA second uses an oversized periphery of 6x100$\mu$m, and is designed to run at a lower maximum drain voltage of 22 V. The amplifiers are next characterized across power in CW with a voltage range of 10 V, corresponding to 18–28 V for the reference and 12–22 V for the oversized PA. Modulated measured results demonstrate a 10 pp efficiency enhancement. This is impacted by a large discrepancy between simulation and measurement for the reference amplifier. However, envelope simulations based on the measured CW characterization demonstrate a 5 pp efficiency enhancement at the same output power level with comparable EVM, validating the technique. This work is published in [63].

- The second contribution of this chapter is the characterization of a highly efficient discrete supply modulator architecture, designed by collaborators from the Colorado Power

Electronics Center. Using a Flying Capacitor Multi-level architecture, this discrete supply modulator achieves static efficiencies of up to $> 99\%$ and dynamic efficiencies of $> 95\%$ with a discretized 35 MHz 16-QAM signal. To evaluate the supply modulator's performance with a PA, a 10 W hybrid amplifier, using the MACOM CHG40010F discrete GaN-on-SiC device is used. After characterizing both components separately, the PA and supply modulator are integrated to evaluate the achievable efficiency enhancement. Measured results demonstrate efficiency improvements of up to 7% compared to static drain operation, corresponding to a 3.5 W reduction in dissipated power for the 10 W PA.

**Chapter 3:**

- This chapter presents an analog linearization system utilizing gate-modulation. A GaN 2-stage Ku-Band PA is designed in the WIN NP-12 process, and a GaAs MMIC is designed, which contains a 10 dB coupler to tap a small portion of the input power to be sent to a differential envelope detector. The two MMIC's are integrated with a PCB, which also contains a baseband amplifier and bias tees. Measured linearization results with 2-tone signals at a $f_c$=14 GHz demonstrate peak $IMD_3$ reduction of up to 17 at a tone spacing of 100 MHz with greater than 4 dB of suppression with tone spacings up to 1 GHz. Excessive dispersion/distortion in the baseband path limits effectiveness with more realistic multi-spectral signals. Using a 100 MHz 5G signal, ACPR improvement of 3 dB is shown with 22 dBm of $\overline{P_{out}}$. EVM with the 5G signal remains essentially unchanged across power. Despite the limited efficacy of the system with more realistic signals due to implementation limitations, this chapter demonstrates the viability of gate-modulation as a modern solution to linearization for wideband mm-wave communications and is published in [64, 65].

**Chapter 4:**

- This chapter delves into the influence of modulation on transistor performance. Specifically, it examines how the optimal impedance matching points for parameters like PAE, gain, and linearity vary as a function of the signal excitation. Additionally, the chapter explores

the feasibility of using multi-tone signals as a substitute for contemporary communication signals. This chapter is detailed in part in [61].

**Chapter 5:**

- This chapter outlines the process behind "Network Emulation", a hardware-in-the-loop circuit analysis tool. The key advantage of this technique is that the analysis process is run directly on a physical device. For applications where a device model is either unavailable or not well validated for a specific case of operation, network emulation provides an invaluable alternative that helps ensure first-pass design success. To validate the method, a PA is first designed and manufactured. The measured response of the PA is then compared against the emulated response and is shown to have relative errors below 7 % across a 30 dB power sweep. Neglecting the lower ACPR, results agree within 3 % across the power sweep. This work is currently under consideration as *Nonlinear Circuit Analysis Using Measurement-Based Emulation of Microwave Networks* in T-MTT.

**Chapter 6:**

- This chapter introduces a novel concept called "Wideband Arbitrary Load Modulation" (WALM). Building upon the network emulation concept discussed in the previous chapter, we present a method to achieve WALM on a physical device. In this approach, the load modulator is treated as a black box, providing an additional degree of freedom compared to traditional load-modulated design flows. The main stage of a Doherty is emulated, and an arbitrary load modulator generates the waveforms required for standard Doherty operation. Practical considerations such as bandwidth, dynamic range, and noise are also taken into account.

## 7.3 Future Work

This section discusses some results that are partially finished but require additional time to complete the research effort.

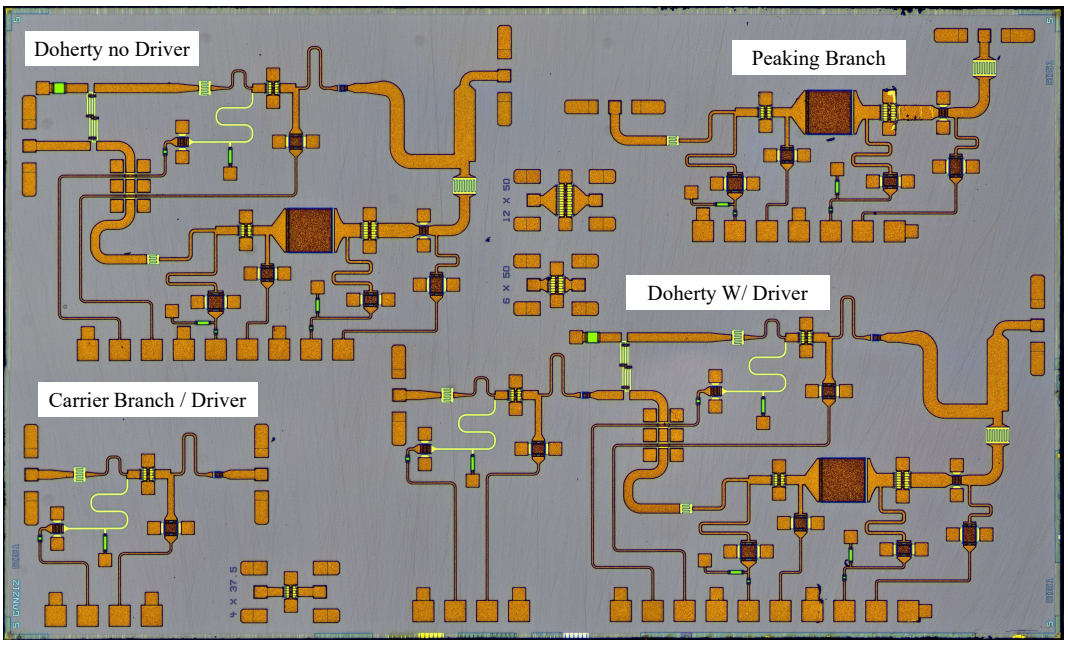



Figure 7.1: HRL T3 Doherty reticle, which includes multiple variations of the Doherty PA, including the individual branches, to more fully characterize PA performance.

### 7.3.1 *V*-Band Doherty Amplifier

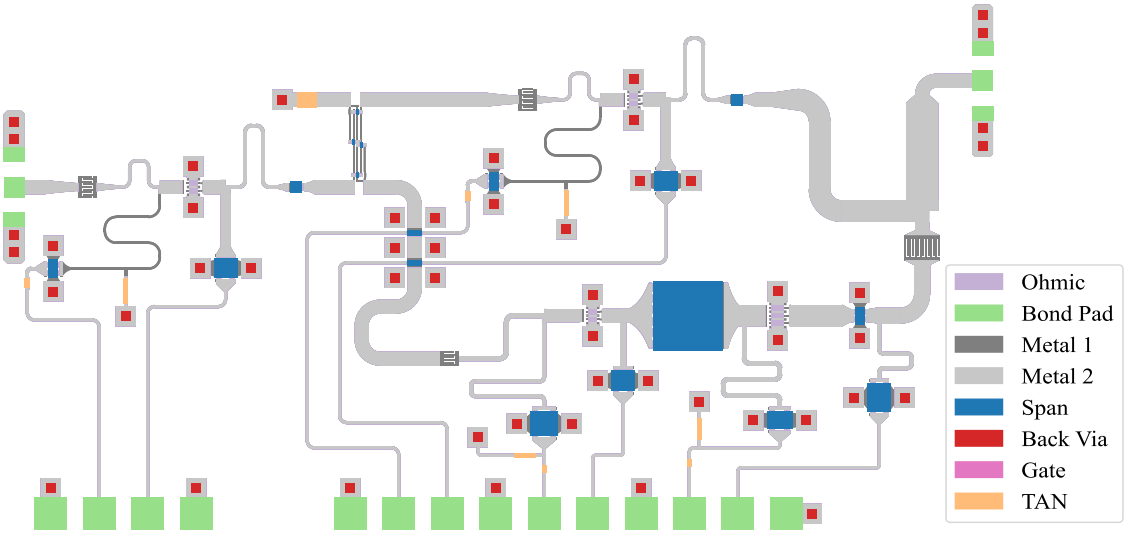
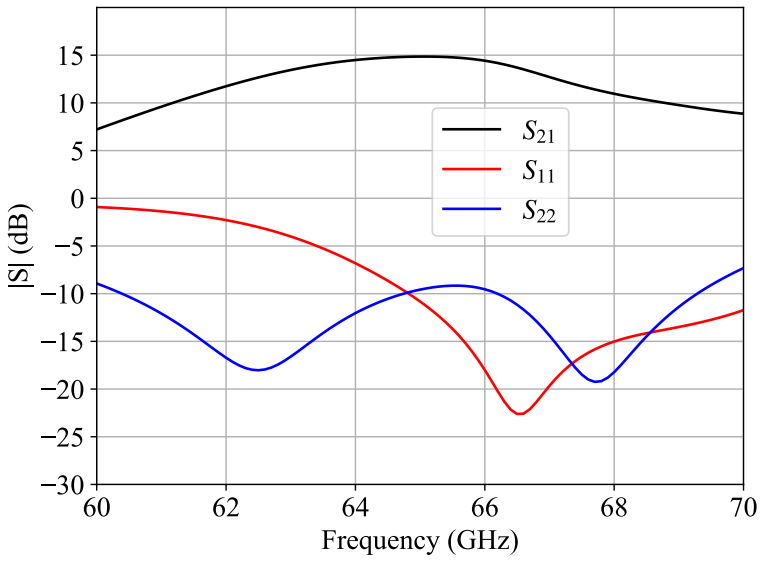
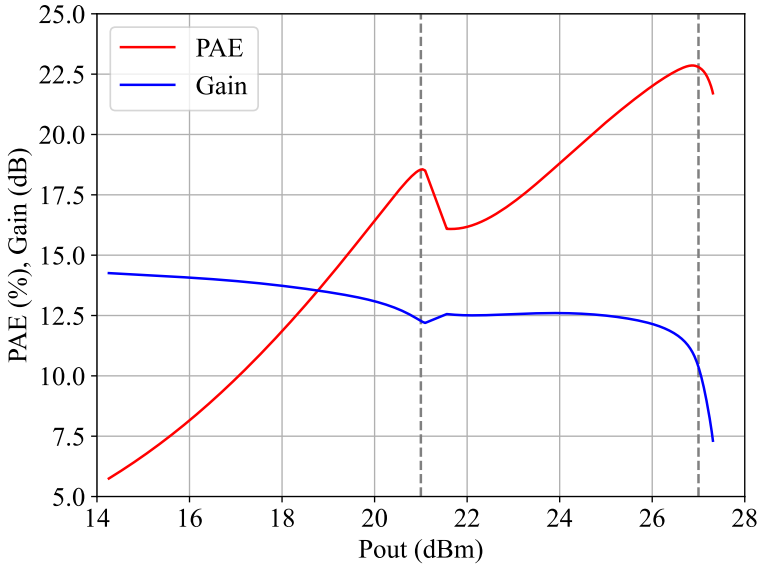



Figure 7.2: Layout of the *V*-Band Doherty including an additional driver stage.

Utilizing the HRL T3 40 nm process, a 2-stage *V*-Band (65 GHz) Doherty amplifier is de-




(a)




(b)

Figure 7.3: *V*-Band Doherty (a) small- and (b) large-signal simulated performance.

signed, shown in Fig.7.2. The Doherty consists of a single-stage AB-biased main amplifier and a 2-stage auxiliary biased into class-C for sufficient gain. The main stage is duplicated at the front of the amplifier to serve as a driver stage to increase gain. The simulated amplifier demonstrates $>$ 15 dB of small signal gain, with return loss $>$ 8 dB at both ports, as seen in Fig.7.3a. In large-signal, the amplifier has G = 12.5 dB, and a first efficiency peak where PAE=18.5 % at

Table 7.1: Summary of recent *V/E*-band GaN Doherty amplifiers.

| | $P_{sat}$ (dBm) | $PAE_{pk}$ (%) | $PAE_{BO}$ (%) | SS Gain (dB) | Freq (GHz) |
|---|---|---|---|---|---|
| T.W. | 29* | 23* | 18.5* | 15* | 65* |
| [109] | 27.8 | 28.9 | 19.8 | 16 | 60 |
| [103] | 33 | 10.0 | 9.0 | 26 | 59-71 |
| [76] | 29 | 34 | 34** | 11 | 71 |
| [21] | 35.7 | 22.5 | 16.8 | 20 | 69-76 |

* Simulated

** Auxiliary gate voltage adjusted dynamically across back off

$P_{out}$=21 dBm and a second peak where PAE = 22.5 % at $P_{out}$=27 dBm, as shown in Fig. 7.3b.

The reticle was received in August 2025, seen in Fig.7.1, but no attempts were made to measure the PA due to time constraints. The reticle contains the individual main and auxiliary amplifier branches, the Doherty without a driver stage, and the full Doherty amplifier. This decision was made to better characterize the manufactured circuit and better explain any potential discrepancies between measurement and simulation.

### 7.3.2 Emulated Doherty PA

While Ch.5 demonstrated the efficacy of the Network Emulation concept as a highly accurate hardware-in-the-loop circuit analysis method, the demonstrated methodology and results are only presented for a circuit topology with a single non-linear device. In reality, most RF nonlinear circuits, e.g., PAs, have multiple transistors. These may take the form of, e.g., sequential stages for increased gain, multiple reactively combined devices to increase $P_{out}$, or essentially isolated devices, such as those in a balanced amplifier. If network emulation is to be used as a general-purpose analysis method, it must be demonstrated to work with arbitrary multiple device architectures. Here, we demonstrate a multi-device emulation with a basic Doherty-like amplifier design. The decision to go with a Doherty demonstrator is that the devices in a load-modulated architecture must interact in a specific way to achieve efficiency enhancement. Additionally, as shown in Ch.6, the two branches generate substantially different nonlinear content which must be applied to the other device. The tightly coupled architecture and complex nonlinear interaction between the two

branches make this an excellent candidate to demonstrate general multi-device interaction.

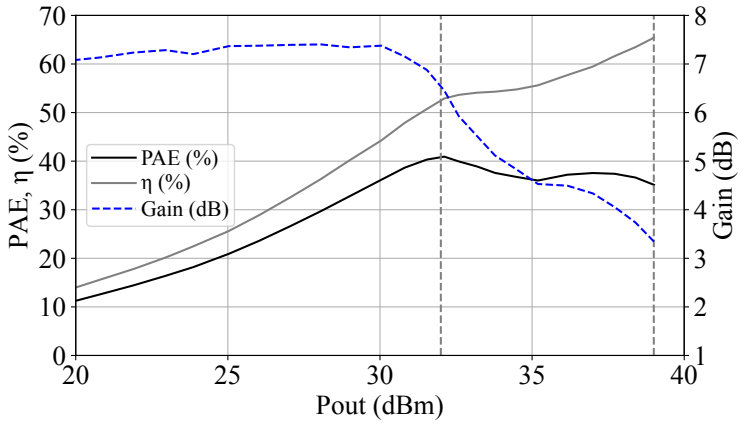



Figure 7.4: CW large-signal measured results of the emulated Doherty amplifier across $P_{out}$. The performance is not competitive with literature at the same frequency (2.25 GHz) but shows the efficacy of the network emulation method for multi-stage and load-modulated designs.

To facilitate the extension to multiple device emulation, we introduce the concept of a *virtualized device*. This is an abstraction of a physical nonlinear DUT. A virtual device has the following attributes: a bias point, specified as a drain voltage and either a desired $I_{dq}$ or a $V_{gs}$ offset from $V_{thresh}$, a set of cached $a,b$ waves at the measured terminals of the device, and a physical location. For example, in a sequential 1:1 staging ratio amplifier, the same device can be used to emulate the full 2-stage PA, where the bias conditions may either be identical or updated for each stage.

This method operates at a high level by emulating each device individually, utilizing the network equivalent source concept and the cached response of the other DUT(s) to determine the appropriate $\mathbb{S}_{eq}$ value to apply to the current DUT. This method was demonstrated for a 2-stage amplifier and was validated in small-signal against the measured $S$-parameters of the DUT [41].

Note that this raises interesting discussions regarding convergence. [41] demonstrated that the small-signal convergence criteria for a single device closely resemble the Rollet stability criterion. It is likely that this is not sufficient for multiple device emulation. This remains future work, but is likely a tractable problem due to the open-loop nature of the active load pull used herein.

One potential issue with this methodology is the scalability to architectures with physically

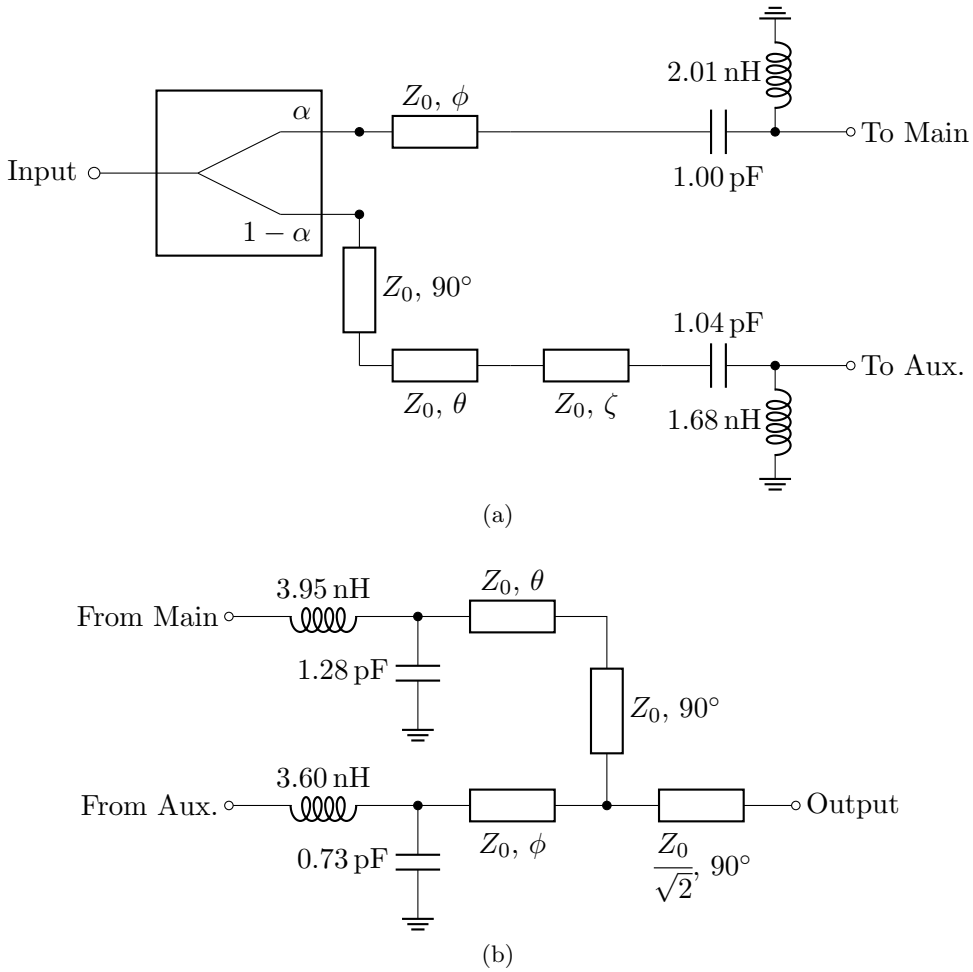



Figure 7.5: Diagram of the (a) input and (b) output matching network used for emulating a Doherty PA.

different devices. The emulation algorithm must be run iteratively with the updated excitations from the previous device(s) until convergence is achieved. If the DUTs are physically disparate and the measurement system can only support a single device at a time (e.g., a 2-port measurement system), the DUTs must be physically exchanged multiple times to obtain the circuit response. This is practically challenging in terms of time and repeatability. However, for MMIC design, an automatic probing station may alleviate this challenge because the devices can be physically exchanged with this infrastructure. This assumes that the probe station control has some interface that could be utilized by the network emulation analysis tool.

To demonstrate the viability of this virtualized device technique, we set out to design a basic

| $\theta$ | $\phi$ | $\zeta$ |
|---|---|---|
| 85° | 135° | 40° |

Table 7.2: Transmission line lengths in Doherty emulated networks.

Doherty PA using network emulation as the analysis tool. First, an architecture that can be realized using the same device in both branches is realized by reducing the $V_{ds}$ in the main branch from the nominal 28 V to 18 V. Next, the devices are load pulled under CW excitation in the system to determine the desired load impedances for maximum PAE. From this load pull analysis, the matching networks shown in Fig.7.5 are designed. The $\theta, \phi, \zeta$ values are used to compensate for non-idealities of the devices and are shown in Table.7.2. Note that $\theta, \zeta$ may be readily combined in the input branch of the auxiliary.

After designing the networks, they are combined into an isolated 6-port S-parameter file, which is loaded into the emulation system. The virtual auxiliary and main devices are assigned to their respective internal ports of the networks. Next, the circuit is iteratively solved by starting with the main branch and assuming the $a, b$ waves from the auxiliary branch are 0. This process continues until the equivalent excitations converge between iterations.

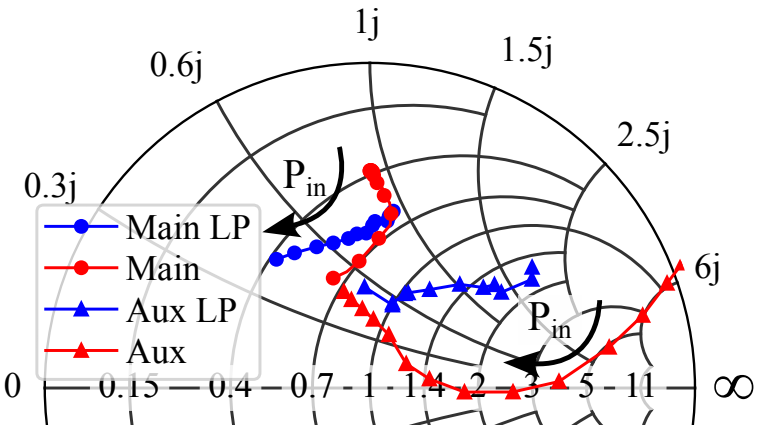



Figure 7.6: Impedance trajectory of main and auxiliary branches in emulated Doherty compared to measured load pull maximum PAE points across $P_{in}$.

The results of this PA design are seen in Fig.7.4, which demonstrates a characteristic Doherty-

like response when excited with a CW signal. The amplifier has a PAE peak of $\sim 35\,\%$ at $\sim 39\,\mathrm{dBm}$ of $P_{out}$ and a second peak of $\sim 40\,\%$ at $\sim 32\,\mathrm{dBm}$ of $P_{out}$. The gain is rather low, which limits the practicality of the designed amplifier. However, the gain could be improved slightly by refining the overall amplifier design. Additionally, the harmonic traps and bias tees placed before the matching networks complicate matching and generally lower performance. Finally, the goal of this Doherty PA design is not to demonstrate competitive performance with literature, but rather to prove that network emulation is a viable analysis method for circuit designs with multiple active devices.

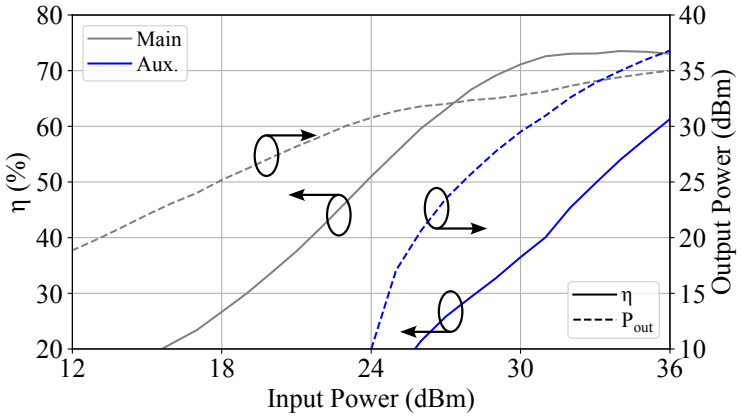



Figure 7.7: Large-signal Response of main and auxiliary branches in Emulated Doherty.

While the aggregate performance is useful to analyze and suggests a Doherty-like mode of operation, it is also useful to look at the per-branch performance of the PA. Fig.7.6 shows the CW impedance trajectories of both branches as well as the measured load pull impedance points for maximum PAE across $P_{out}$. While the measured trajectories do not match exactly with the maximum points from load pull, the trends are similar and indicate that the measured response is reasonable.

Additionally, it is of interest to look at $\eta$ and $P_{out}$ for each branch individually while operating in the Doherty-like mode. The results can be seen in Fig.7.7. The main branch $\eta$, for example, approximates the textbook response with the efficiency reaching a peak value and then remaining constant across $6\,\mathrm{dB}$ of $P_{in}$. Additionally, the auxiliary stage demonstrates a characteristic class-C

like response. From this data, it is also evident that the auxiliary is not reaching peak efficiency, and the aggregate response could be improved by having the auxiliary turn on earlier. The ability to readily analyze the individual performance of multi-device amplifier topologies is a powerful tool for circuit designers using network emulation.

## Bibliography


[1] 3GPP. 3GPP 38.820 Study on the 7 to 24 GHz frequency range for NR. https://portal.3gpp.org/desktopmodules/Specifications/SpecificationDetails.aspx?specificationId=3599, 2015.

[2] S. Alsahali, D. Gecan, A. Alt, P. Chen, S. Woodington, A. Sheikh, P. Tasker, and J. Lees. Modulated rapid load pull system for the emulation of envelope tracking power amplifiers. Electronics Letters, 56(7):325–328, 2020.

[3] Alberto Maria Angelotti, Gian Piero Gibiino, Troels S. Nielsen, Alberto Santarelli, and Jan Verspecht. Impact of broadband modulation in active load-pull on-wafer measurements of gan hemts. In 2022 99th ARFTG Microwave Measurement Conference (ARFTG), pages 1–4, 2022.

[4] V. Aparin and L.E. Larson. Modified Derivative Superposition Method for Linearizing FET Low-Noise Amplifiers. IEEE Transactions on Microwave Theory and Techniques, 53(2):571–581, 2005.

[5] Peter Asbeck and Zoya Popovic. ET Comes of Age: Envelope Tracking for Higher-Efficiency Power Amplifiers. IEEE Microwave Magazine, 17(3):16–25, 2016.

[6] Diogo R. Barros, Luís C. Nunes, Pedro M. Cabral, and José Carlos Pedro. Impact of the input baseband terminations on the efficiency of wideband power amplifiers under concurrent band operation. IEEE Trans. on Microwave Theory and Techniques, 67:5127–5138, 2019.

[7] Barros, Diogo R and Nunes, Luís C and Cabral, Pedro M and Pedro, José Carlos. Impact of the Input Baseband Terminations on the Efficiency of Wideband Power Amplifiers under Concurrent Band Operation. IEEE Transactions on Microwave Theory and Techniques, 67(12):5127–5138, 2019.

[8] Taylor Barton. Not Just a Phase: Outphasing Power Amplifiers. IEEE Microwave Magazine, 17(2):18–31, 2016.

[9] Taylor Barton. Not just a phase: Outphasing power amplifiers. IEEE Microwave Magazine, 17(2):18–31, 2016.

[10] Ahmed Ben Ayed and Slim Boumaiza. Millimeter-Wave Wideband Active Load—Pull System Using Vector Network Analyzer Frequency Extenders. IEEE Microwave and Wireless Technology Letters, pages 1–4, 2025.

[11] J. Brinkhoff and A.E. Parker. Effect of baseband impedance on fet intermodulation. IEEE Trans. on Microwave Theory and Techniques, 51(3):1045–1051, 2003.

[12] Tommaso Cappello, Gautam Jindal, Jose Nunez-Yanez, and Kevin Morris. Power Consumption and Linearization Performance of a Bit- and Frequency-Scalable AM/AM AM/PM Pre-Distortion on FPGA. In 2022 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC), pages 1–3, 2022.

[13] Tommaso Cappello, Sarmad Ozan, Laura McDonald, Andy Tucker, Peter Krier, Tudor Williams, and Kevin Morris. A Low Loss, 6 GHz Large-Signal Bandwidth Analog Pre-Distortion Linearizer for K-Band High Power Amplifiers. In 2023 53rd European Microwave Conference (EuMC), pages 368–371, 2023.

[14] Tommaso Cappello, Prathamesh Pednekar, Corrado Florian, Steve Cripps, Zoya Popovic, and Taylor W. Barton. Supply- and Load-Modulated Balanced Amplifier for Efficient Broadband 5G Base Stations. IEEE Transactions on Microwave Theory and Techniques, 67(7):3122–3133, 2019.

[15] Tommaso Cappello, Shane Verploegh, Corrado Florian, and Zoya Popovic. Single-DC-Input Multi-Level Envelope Tracking of a High-Efficiency X-band Power Amplifier. In 2019 IEEE MTT-S International Microwave Symposium (IMS), pages 464–467, 2019.

[16] Sona Carpenter, Dhecha Nopchinda, Morteza Abbasi, Zhongxia Simon He, Mingquan Bao, Thomas Eriksson, and Herbert Zirath. A *D*-Band 48-Gbit/s 64-QAM/QPSK Direct-Conversion I/Q Transceiver Chipset. IEEE Transactions on Microwave Theory and Techniques, 64(4):1285–1296, 2016.

[17] Rajan Chattamvelli and Ramalingam Shanmugam. Descriptive Statistics for Scientists and Engineers: Applications in R, chapter Kurtosis, pages 111–126. Springer Nature Switzerland, Cham, 2023.

[18] Sanket Chaudhary and Nuno Borges de Carvalho. Impact of excitation signal statistics in the selection of the optimum load for future wideband power amplifiers. IEEE Trans. on Microwave Theory and Techniques, 70(1):827–835, 2022.

[19] Audrey Cheshire, Aarranon Bharathan, and Dragan Maksimović. Flying capacitor four-level supply modulator with active balancing for rf power amplifier applications. In 2023 IEEE 24th Workshop on Control and Modeling for Power Electronics (COMPEL), pages 1–7, 2023.

[20] Audrey Cheshire, Paul Flaten, Zoya Popović, and Dragan Maksimović. High-frequency flying capacitor four-level drain supply modulator. In 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), pages 682–688, 2025.

[21] Bharath Cimbili, Mingquan Bao, Moïse Safari Mugisho, Christian Friesicke, Sandrine Wagner, and Rüdiger Quay. A High-Efficiency E-Band GaN Doherty Power Amplifier with 35.7 dBm Output Power and 22.8%/16.8% Peak/6-dB Back-Off Efficiency. In 2025 IEEE/MTT-S International Microwave Symposium - IMS 2025, pages 725–728, 2025.

[22] Robert E. Collin. Circuit Theory for Waveguiding Systems, pages 220–302. Wiley, 2001.

[23] Adam M. Conway, Yu Zhao, Peter M. Asbeck, Miroslav Micovic, and Jeong Moon. Dynamic Gate Bias Technique for Improved Linearity of GaN HFET Power Amplifiers. In IEEE MTT-S International Microwave Symposium Digest, 2005., pages 499–502, 2005.

[24] Adam Coonan. Distortion Analysis of Analog Electronic Circuits Using Modulated Signals. PhD thesis, Vrije Universiteit Brussel, 2017.

[25] D. Cox. Linear Amplification with Nonlinear Components. IEEE Transactions on Communications, 22(12):1942–1945, 1974.

[26] Steve C Cripps et al. RF power amplifiers for wireless communications, volume 250. Artech house Norwood, MA, 2006.

[27] Giovanni Crupi, Valeria Vadalà, Paolo Colantonio, Elisa Cipriani, Alina Caddemi, Giorgio Vannini, and Dominique M. M.-P. Schreurs. Empowering GaN HEMT models: The gateway for power amplifier design. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 30(1):e2125, 2017.

[28] W.R. Curtice. A MESFET Model for Use in the Design of GaAs Integrated Circuits. IEEE Transactions on Microwave Theory and Techniques, 28(5):448–456, 1980.

[29] Asmita Dani, Michael Roberg, and Zoya Popovic. PA Efficiency and Linearity Enhancement Using External Harmonic Injection. IEEE Transactions on Microwave Theory and Techniques, 60(12):4097–4106, 2012.

[30] Hailin Deng, Dewei Zhang, Dalong Lv, Dongfang Zhou, and Yi Zhang. Analog Predistortion Linearizer With Independently Tunable Gain and Phase Conversions for Ka-Band TWTA. IEEE Transactions on Electron Devices, 66(3):1533–1539, 2019.

[31] Jeff Desjardins. weforum.org. https://www.weforum.org/stories/2019/04/how-much-data-is-generated-each-day-cf4bddf29f/, 2019. [Accessed 11-01-2026].

[32] W.H. Doherty. A New High Efficiency Power Amplifier for Modulated Waves. Proceedings of the Institute of Radio Engineers, 24(9):1163–1182, 1936.

[33] Maxwell Robert Duffy, Gregor Lasser, Morten Olavsbraten, Eric Berry, and Zoya Popovic. Efficient Multisignal 2–4-GHz Power Amplifier With Power Tracking. IEEE Transactions on Microwave Theory and Techniques, 66(12):5652–5663, 2018.

[34] Maxwell Robert Duffy, Gregor Lasser, Morten Olavsbråten, Eric Berry, and Zoya Popović. Efficient multisignal 2–4-ghz power amplifier with power tracking. IEEE Transactions on Microwave Theory and Techniques, 66(12):5652–5663, 2018.

[35] Lawrence Dunleavy, Charles Baylis, Walter Curtice, and Rick Connick. Modeling GaN: powerful but challenging. IEEE Microwave Magazine, 11(6):82–96, 2010.

[36] Joel Fernandez, Lauri Anttila, Koen Buisman, Mikko Heino, Christian Fager, Thomas Eriksson, and Mikko Valkama. Over-the-Air Linearization of Phased Array Transmitters Affected by Load Modulation. IEEE Trans. Circuits Syst. I, 72(5):2366–2379, 2025.

[37] Andrea Ferrero and Marco Pirola. Harmonic load-pull techniques: An overview of modern systems. IEEE Microwave Magazine, 14(4):116–123, 2013.

[38] Andrea Ferrero and Marco Pirola. Harmonic Load-Pull Techniques: An Overview of Modern Systems. IEEE Microwave Magazine, 14(4):116–123, 2013.

[39] Ricardo Figueiredo, Sanket Chaudhary, Marc Vanden Bossche, Mohadig Rousstia, Mauro Marchetti, and Nuno Borges Carvalho. Discussion on system-level wideband active load-pull linearity measurements: How to reach broadband design techniques? In 2024 102nd ARFTG Microwave Measurement Conf. (ARFTG), pages 1–3, 2024.

[40] Ricardo Figueiredo, Sanket Chaudhary, Marc Vanden Bossche, Mohadig Rousstia, Mauro Marchetti, and Nuno Borges Carvalho. Discussion on System-Level Wideband Active Load-Pull Linearity Measurements: How to Reach Broadband Design Techniques? In 2024 102nd ARFTG Microwave Measurement Conference (ARFTG), pages 1–3, 2024.

[41] Paul Flaten. Advanced Design Approaches to High-Performance Transmitter Components. PhD thesis, University of Colorado, Boulder, 2025.

[42] Marcus Gavell, Göran Granström, Christian Fager, Sten E. Gunnarsson, Mattias Ferndahl, and Herbert Zirath. An $E$ -Band Analog Predistorter and Power Amplifier MMIC Chipset. IEEE Microwave and Wireless Components Letters, 28(1):31–33, 2018.

[43] Dragan Gecan, Karl M. Gjertsen, and Morten Olavsbråten. Novel Metric Describing Total Nonlinearity of Power Amplifier With a Corresponding Figure of Merit for Linearity Evaluation and Optimization. IEEE Microwave and Wireless Components Letters, 27(1):85–87, 2017.

[44] Dragan Gecan, Morten Olavsbråten, and Karl M. Gjertsen. Measured linearity improvement of 10 W GaN HEMT PA with dynamic gate biasing technique for flat transfer phase. In 2016 IEEE MTT-S International Microwave Symposium (IMS), pages 1–4, 2016.

[45] Lei Guan and Anding Zhu. Green Communications: Digital Predistortion for Wideband RF Power Amplifiers. IEEE Microwave Magazine, 15(7):84–99, 2014.

[46] Ramesh K. Gupta, Paul A. Goud, and Colin G. Englefield. Improvement of Intermodulation Distortion in Microwave M.E.S.F.E.T. Amplifiers using Gate-Bias Compensation. Electronics Letters, 15:741–742, 1979.

[47] William Hallberg, Dhecha Nopchinda, Christian Fager, and Koen Buisman. Emulation of Doherty Amplifiers Using Single- Amplifier Load–Pull Measurements. IEEE Microwave and Wireless Components Letters, 30(1):47–49, January 2020.

[48] John Hoversten, Michael Roberg, and Zoya Popović. Harmonic load pull of high-power microwave devices using fundamental-only load pull tuners. In 75th ARFTG Microwave Measurement Conf., pages 1–4, 2010.

[49] Li Kang, Aimin Wu, Wenhua Chen, and Xiaofan Chen. C–Ku-Band RF-Input Load Modulated Balanced Amplifier MMIC Utilizing Broadband Saturation Efficiency Enhancement Technique. IEEE Transactions on Microwave Theory and Techniques, pages 1–12, 2024.

[50] Allen Katz, John Wood, and Daniel Chokola. The Evolution of PA Linearization: From Classic Feedforward and Feedback Through Analog and Digital Predistortion. IEEE Microwave Magazine, 17(2):32–40, 2016.

[51] Göksu Kaval, Gregor Lasser, Marcus Gavell, and Christian Fager. A 100-114 GHz GaAs MMIC Power Amplifier With Fully Integrated Dynamic Gate Bias Control for Linearization and Efficiency Enhancement. In 2024 19th European Microwave Integrated Circuits Conference (EuMIC), pages 271–274, 2024.

[52] Bumman Kim, Jangheon Kim, Ildu Kim, and Jeonghyeon Cha. The doherty power amplifier. IEEE Microwave Magazine, 7(5):42–50, 2006.

[53] Myoung-Gyun Kim and Tae-Yeoul Yun. Analysis and Design of Feedforward Linearity-Improved Mixer Using Inductive Source Degeneration. IEEE Transactions on Microwave Theory and Techniques, 62(2):323–331, 2014.

[54] Justin B. King and Thomas J. Brazil. Nonlinear electrothermal gan hemt model applied to high-efficiency power amplifier design. IEEE Trans. on Microwave Theory and Techniques, 61(1):444–454, 2013.

[55] H. Kobayashi, J.M. Hinrichs, and P.M. Asbeck. Current-mode class-D power amplifiers for high-efficiency RF applications. IEEE Transactions on Microwave Theory and Techniques, 49(12):2480–2485, 2001.

[56] Gregor Lasser, Maxwell Duffy, Morten Olavsbråten, and Zoya Popović. Gate control of a two-stage GaN MMIC amplifier for amplitude and phase linearization. In 2017 IEEE 18th Wireless and Microwave Technology Conference (WAMICON), pages 1–5, 2017.

[57] Gregor Lasser, Maxwell Duffy, Jason Vance, and Zoya Popović. Discrete-level envelope tracking for broadband noise-like signals. In 2017 IEEE MTT-S International Microwave Symposium (IMS), pages 1942–1945, 2017.

[58] Gregor Lasser, Maxwell Robert Duffy, and Zoya Popović. Dynamic Dual-Gate Bias Modulation for Linearization of a High-Efficiency Multistage PA. IEEE Transactions on Microwave Theory and Techniques, 67(7):2483–2494, 2019.

[59] Gregor Lasser, Maxwell Robert Duffy, and Zoya Popović. Dynamic dual-gate bias modulation for linearization of a high-efficiency multistage pa. IEEE Transactions on Microwave Theory and Techniques, 67(7):2483–2494, 2019.

[60] Michael Litchfield. A 15–24 GHz, 15W Reactively Matched GaN MMIC Power Amplifier. In 2023 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), pages 175–178, 2023.

[61] Reyes Lucero, Mark Vanden Bossche, and Zoya Popovic. Characterization of GaN Transistors and PAs with Modulated Signals. In 2025 104th ARFTG Microwave Measurement Conference (ARFTG), pages 1–6, 2025.

[62] Reyes Lucero, Connor Nogales, and Zoya Popović. Efficiency enhancement by sizing device periphery for supply-modulated power amplifiers. In 2024 IEEE Wireless and Microwave Technology Conference (WAMICON), pages 1–4, 2024.

[63] Reyes Lucero, Connor Nogales, and Zoya Popović. Efficiency Enhancement by Sizing Device Periphery for Supply-Modulated Power Amplifiers. In 2024 IEEE Wireless and Microwave Technology Conference (WAMICON), pages 1–4, 2024.

[64] Reyes Lucero and Zoya Popovic. A Ku-Band GaN PA With GaAs Gate Modulator for Improved Linearity. IEEE Journal of Microwaves, 6(1):163–173, 2026.

[65] Reyes Lucero and Zoya Popović. A Ku-band GaN PA with GaAs Gate Modulator for Improved Linearity. In 2025 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC), pages 1–4, 2025.

[66] M. Yaqub A. Mahsud and Taylor W. Barton. MMIC Implementation of the Load Modulated Balanced Amplifier and its Variants. IEEE Journal of Microwaves, pages 1–11, 2025.

[67] Mauro Marchetti, Gustavo Avolio, Michele Squillante, and Ajay K. Doggalli. Load pull measurement techniques: architecture, accuracy, and applications. In 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), pages 1–6, 2019.

[68] Mauro Marchetti, Marco J. Pelk, Koen Buisman, W. C. Edmund Neo, Marco Spirito, and Leo C. N. de Vreede. Active harmonic load–pull with realistic wideband communications signals. IEEE Trans. on Microwave Theory and Techniques, 56(12):2979–2988, 2008.

[69] Mauro Marchetti, Marco J. Pelk, Koen Buisman, W. C. Edmund Neo, Marco Spirito, and Leo C. N. de Vreede. Active Harmonic Load–Pull With Realistic Wideband Communications Signals. IEEE Transactions on Microwave Theory and Techniques, 56(12):2979–2988, 2008.

[70] Mauro Marchetti, Marco J. Pelk, Koen Buisman, W. C. Edmund Neo, Marco Spirito, and Leo C. N. de Vreede. Active Harmonic Load–Pull With Realistic Wideband Communications Signals. IEEE Transactions on Microwave Theory and Techniques, 56(12):2979–2988, 2008.

[71] E. McCune and Q. Diduck. 4096-QAM Microwave Transmitter Providing Efficiency Exceeding 50% and EVM Below 1%. In 2019 49th European Microwave Conference (EuMC), pages 896–899, 2019.

[72] E. McCune, Q. Diduck, W. Godycki, R. Booth, and D. Kirkpatrick. A fully polar transmitter for efficient software-defined radios. In 2017 IEEE MTT-S International Microwave Symposium (IMS), pages 1946–1949, 2017.

[73] Pierre Medrel, Alaaeddine Ramadan, Jean-Michel Nebus, Philippe Bouysse, Luc Lapierre, and Jean-François Villemazet. High Efficiency Class B GaN Power Amplifier with Dynamic Gate Biasing for Improved Linearity. Electronics letters, 48(18):1136–1137, 2012.

[74] Pablo F. Miaja, Miguel Rodriguez, Alberto Rodriguez, and Javier Sebastian. A linear assisted dc/dc converter for envelope tracking and envelope elimination and restoration applications. IEEE Transactions on Power Electronics, 27(7):3302–3309, 2012.

[75] Umesh K. Mishra, Likun Shen, Thomas E. Kazior, and Yi-Feng Wu. GaN-Based RF Power Devices and Amplifiers. Proceedings of the IEEE, 96(2):287–305, 2008.

[76] Toshifumi Nakatani, Mohammad Ali Zolfaghari, Jonmei J. Yan, and Peter M. Asbeck. A 29-dBm, 34% PAE E-Band Dual-Input Doherty Power Amplifier Using 40-nm GaN Technology. In 2022 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), pages 156–159, 2022.

[77] Deltimple Nathalie, Potereau Manuel, and Ghiotto Anthony. Fully Integrated Reflector-Based Analog Predistortion for Ku-band Power Amplifiers Linearization. In ESSCIRC 2021 - IEEE 47th European Solid State Circuits Conference (ESSCIRC), pages 363–368, 2021.

[78] Connor Nogales. Broadband Supply Modulated PAs for Efficient and Linear Transmit Arrays. PhD thesis, University of Colorado, Boulder, 2024.

[79] Connor Nogales, Paul Flaten, Morten Olavsbråten, Zoya Popović, and Gregor Lasser. Deliberate Source/Load Mismatch for Linearity and Efficiency of Discrete Supply Modulated GaN PAs. IEEE Transactions on Microwave Theory and Techniques, 72(12):6833–6844, 2024.

[80] Connor Nogales, Paul Flaten, Morten Olavsbråten, Zoya Popović, and Gregor Lasser. Deliberate source/load mismatch for linearity and efficiency of discrete supply modulated gan pas. IEEE Transactions on Microwave Theory and Techniques, 72(12):6833–6844, 2024.

[81] Connor Nogales, Zoya Popović, and Gregor Lasser. A 10-w6-12ghz gan mmic supply modulated power amplifier. In 2022 52nd European Microwave Conference (EuMC), pages 436–439, 2022.

[82] Connor Nogales, Zoya Popović, and Gregor Lasser. An 800-w four-level supply modulator for efficient envelope tracking of rf transmitters. IEEE Journal of Emerging and Selected Topics in Power Electronics, 11(3):3251–3260, 2023.

[83] Dhecha Nopchinda and Koen Buisman. An active load-pull technique creating time-variant impedances to emulate coupling between power amplifiers. In 2017 IEEE MTT-S International Microwave Symposium (IMS), pages 1437–1440, Honololu, HI, USA, June 2017. IEEE.

[84] Luís Cótimos Nunes, Diogo R. Barros, Pedro M. Cabral, and José C. Pedro. Efficiency degradation analysis in wideband power amplifiers. IEEE Trans. on Microwave Theory and Techniques, 66:5640–5651, 2018.

[85] Morten Olavsbråten and Dragan Gecan. Bandwidth Reduction for Supply Modulated RF PAs Using Power Envelope Tracking. IEEE Microwave and Wireless Components Letters, 27(4):374–376, 2017.

[86] B.M. Oliver. Thermal and quantum noise. Proceedings of the IEEE, 53(5):436–454, 1965.

[87] Alex Pitt, Mark Beach, and Tommaso Cappello. An Analog Gain Inflection Predistorter for Combined Back-Off Efficiency and Linearity With Doherty Power Amplifiers. IEEE Transactions on Microwave Theory and Techniques, 73(1):167–179, 2025.

[88] Zoya Popovic. Amping Up the PA for 5G: Efficient GaN Power Amplifiers with Dynamic Supplies. IEEE Microwave Magazine, 18(3):137–149, 2017.

[89] David M. Pozar. Microwave engineering. Wiley, 4th ed edition, 2012. OCLC: ocn714728044.

[90] Roberto Quaglia, Vittorio Camarchia, Jorge Julian Moreno Rubio, Marco Pirola, and Giovanni Ghione. A 4-W Doherty Power Amplifier in GaN MMIC Technology for 15-GHz Applications. IEEE Microwave and Wireless Components Letters, 27(4):365–367, 2017.

[91] F.H. Raab. Class-F power amplifiers with maximally flat waveforms. IEEE Transactions on Microwave Theory and Techniques, 45(11):2007–2012, 1997.

[92] F.H. Raab. Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics. IEEE Transactions on Microwave Theory and Techniques, 49(8):1462–1468, 2001.

[93] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal. Power Amplifiers and Transmitters for RF and Microwave. IEEE Transactions on Microwave Theory and Techniques, 50(3):814–826, 2002.

[94] Theodore S. Rappaport, James N. Murdock, and Felix Gutierrez. State of the Art in 60-GHz Integrated Circuits and Systems for Wireless Communications. Proceedings of the IEEE, 99(8):1390–1436, 2011.

[95] Patrick Roblin. Nonlinear RF circuits and Nonlinear Vector Network analyzers: Interactive Measurement and Design Techniques. Cambridge University Press, 2011.

[96] Sheldon M. Ross. A first course in probability. Prentice Hall, 2010.

[97] Wissam Saabe, Christophe Mazière, Arnaud Delias, Sébastien Mons, and Edouard Ngoya. Rf power amplifier model extraction for accurate and fast load pull simulations with wideband signals. In 2024 103rd ARFTG Microwave Measurement Conference (ARFTG), pages 1–4. IEEE, 2024.

[98] William Sear and Taylor W. Barton. Wideband IMD3 Suppression through Negative Baseband Impedance Synthesis. IET Microwaves, Antennas & Propagation, 15(7):728–743, 2021.

[99] Alihossein Sepahvand, Parisa Momenroodaki, Yuanzhe Zhang, Zoya Popović, and Dragan Maksimović. Monolithic multilevel gan converter for envelope tracking in rf power amplifiers. In 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pages 1–7, 2016.

[100] C.E. Shannon. Communication in the presence of noise. Proceedings of the IRE, 37(1):10–21, 1949.

[101] Daniel J. Shepphard, Jeffrey Powell, and Steve C. Cripps. An Efficient Broadband Reconfigurable Power Amplifier Using Active Load Modulation. IEEE Microwave and Wireless Components Letters, 26(6):443–445, 2016.

[102] Daniel J. Shepphard, Jeffrey Powell, and Steve C. Cripps. An efficient broadband reconfigurable power amplifier using active load modulation. IEEE Microwave and Wireless Components Letters, 26(6):443–445, 2016.

[103] Giuseppe Sivverini, Andrea Meazza, Antonio Traversa, Alberto Colzani, Alessandro Fonte, Stefano Moscato, and Christian Friesicke. GaN/SiC V-band 33 dBm Power Amplifier with 10% PAE for Inter Satellite Communications. In 2023 18th European Microwave Integrated Circuits Conference (EuMIC), pages 1–4, 2023.

[104] N.O. Sokal and A.D. Sokal. Class E-A new class of high-efficiency tuned single-ended switching power amplifiers. IEEE Journal of Solid-State Circuits, 10(3):168–176, 1975.

[105] Jacques Sombrin and Pierre Medrel. Cross-correlation method measurement of error vector magnitude and application to power amplifier non-linearity performances. In 2016 88th ARFTG Microwave Measurement Conference (ARFTG), pages 1–4, 2016.

[106] Jacques B. Sombrin. On the formal identity of evm and npr measurement methods: Conditions for identity of error vector magnitude and noise power ratio. In 41st European Microwave Conf., pages 337–340, 2011.

[107] Statista. Number of smartphone users worldwide from 2014 to 2029 (in millions). https://www-statista-com.colorado.idm.oclc.org/forecasts/1143723/smartphone-users-in-the-world/, 2024. [Accessed 11-01-2026].

[108] Haiqian Tang, Songbai He, Peng Hao, Minxian Song, and Fei You. A 2.4–3.5 GHz Broadband Analog Predistorter With Independently Tunable Gain. IEEE Microwave and Wireless Technology Letters, 35(4):476–479, 2025.

[109] Jeng-Han Tsai, Yu-Hui Lin, Yi-Fan Tsao, Yuan Wang, Arpan Desai, Ping-Hsun Chiu, and Heng-Tung Hsu. A 60-GHz 27.8-dBm GaN-based Doherty Power Amplifier for V-band Applications. In 2023 Asia-Pacific Microwave Conference (APMC), pages 171–173, 2023.

[110] Amedeo Varano, Dries Peumans, and Yves Rolain. Rova: A practical, parsimonious volterra model for modulated microwave systems. IEEE Transactions on Microwave Theory and Techniques, 72(6):3701–3710, 2024.

[111] F. Verbeyst and M.V. Bossche. Real-time and optimal pa characterization speeds up pa design. In 34th European Microwave Conference, 2004., volume 1, pages 431–434, 2004.

[112] Jan Verspecht, Augustine Stav, Troels Nielsen, and Sam Kusano. The vector component analyzer: A new way to characterize distortions of modulated signals in high-frequency active devices. IEEE Microwave Magazine, 23(12):86–96, 2022.

[113] Kimon Vivien, Paolo Enrico de Falco, Olivier Venard, Geneviève Baudoin, Pascal Pierre-Charles-Félix, and Taylor Barton. Load Modulated Balanced Amplifier Design Method Based on Complex Impedance Trajectories. IEEE Journal of Microwaves, 2(1):199–213, 2022.

[114] Nikolai Wolff, Wolfgang Heinrich, and Olof Bengtsson. A novel model for digital predistortion of discrete level supply-modulated rf power amplifiers. IEEE Microwave and Wireless Components Letters, 26(2):146–148, 2016.

[115] qualcomm.com. https://www.qualcomm.com/content/dam/qcomm-martech/dm-assets/documents/qualcomm_wideband_envelope_tracker_qet7100.pdf. [Accessed 20-11-2025].

[116] iPhone 16 Chip ID — ifixit.com. https://www.ifixit.com/Guide/iPhone+16+Chip+ID/177222. [Accessed 20-11-2025].

[117] Mobile data traffic forecast. https://www.ericsson.com/en/reports-and-papers/mobility-report/dataforecasts/mobile-traffic-forecast, 2025. [Accessed 06-01-2026].

[118] Jianjun Xu, Subrata Halder, Faramarz Kharabi, John McMacken, Joseph Gering, and David E. Root. Global dynamic FET model for GaN transistors: DynaFET model validation and comparison to locally tuned models. In 83rd ARFTG Microwave Measurement Conference, pages 1–6, 2014.

[119] Han Zhou, Haojie Chang, and Christian Fager. A Ku-Band GaN MMIC Push-Pull Power Amplifier with Coupled-Line Balun and Capacitive Neutralization for 6G Applications. In 2024 IEEE European Solid-State Electronics Research Conference (ESSERC), pages 289–292, 2024.

ProQuest Number: 32448333

INFORMATION TO ALL USERS
The quality and completeness of this reproduction is dependent on the quality
and completeness of the copy made available to ProQuest.




Distributed by
ProQuest LLC a part of Clarivate ( 2026).
Copyright of the Dissertation is held by the Author unless otherwise noted.

This work is protected against unauthorized copying under Title 17,
United States Code and other applicable copyright laws.

This work may be used in accordance with the terms of the Creative Commons license
or other rights statement, as indicated in the copyright statement or in the metadata
associated with this work. Unless otherwise specified in the copyright statement
or the metadata, all rights are reserved by the copyright holder.

ProQuest LLC
789 East Eisenhower Parkway
Ann Arbor, MI 48108 USA