GaN Power Amplifiers for Multi-Objective Design and Millimeter-Wave Operation

by

Stefan Stroessner

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Committee Members

Dist. Prof. Zoya Popović

Prof. Cody Scarborough

Prof. Laila Marzall

Dr. Scott Schafer

Dr. Michael Sinanis

Dr. Andrea Arias-Purdue

Stroessner, Stefan (Ph.D., Electrical Engineering)

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Thesis directed by Dist. Prof. Zoya Popović

The electromagnetic spectrum is becoming increasingly crowded at lower frequencies, requiring power amplifier (PA) designs to address a growing number of competing objectives, including bandwidth, linearity, and efficiency. To address these challenges, this thesis focuses on GaN-on-SiC PA design, utilizing multi-objective visualization and operation at millimeter-wave frequencies.

Multi-Objective Visualization (MoV) is introduced as a design method to enable rapid trade-off analysis and improve designer intuition. Two complementary methods are developed that operate on simulated data sets, allowing designers to identify solutions that meet targeted performance goals. The methodology is validated through the design and measurement of two wideband ($> 60\,\%$ fractional bandwidth) hybrid PAs and two MMIC PAs, including a supply-modulated X-band MMIC and a multistage K-band MMIC.

Millimeter-wave GaN MMIC PAs are further investigated through designs in both developmental and advanced processes. A W-band PA in a 90 nm process is used to evaluate model accuracy and process maturity, while a reconfigurable W-band PA demonstrates the integration of tunable matching networks and highlights stability considerations and modeling discrepancies at high frequencies.

Finally, two diplexed PA architectures are presented to enable wideband operation. A quasi-MMIC approach combines GaAs diplexer filters with GaN PAs for Ku- to Ka-band coverage, while a fully integrated E-band GaN MMIC employs reflectionless filtering to achieve wide fractional bandwidth.

Together, these contributions advance both the design methodology and practical implementation of efficient, wideband, and millimeter-wave GaN power amplifiers.

Dedication

To my parents for teaching me persistence, responsibility, and integrity.

To my wife for teaching me empathy, consistency, and love.

To my son for teaching me mindfulness, curiosity, and joy.

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Chapter 1

Introduction

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1.1 Background and Motivation

Millimeter-wave frequencies (30–300 GHz), are becoming more popular for a range of applications due to the crowding of the electromagnetic spectrum at lower frequencies, as well as demands for larger bandwidths. The current allocations for a part of the millimeter-wave range are indicated in Fig. 1.1, showing that the available bandwidth increases with increasing carrier frequency. A limitation for adoption has traditionally been atmospheric attenuation, shown in Fig. 1.2. The base attenuation increases by a factor of 10 between 20 GHz and 100 GHz, with several strong peaks around 22 GHz associated with water vapor and 60 GHz associated with an oxygen molecule resonance. The so called "windows" around 30-40 GHz and 90 GHz

have lower attenuation than the peaks, but still significantly absorb electromagnetic waves compared to frequencies below 10 GHz. The high attenuation requires higher transmitted power levels in order to close communication and radar link budgets, motivating research in multi-stage, GaN power amplifiers operating into millimeter-wave frequencies, which is the topic of this thesis.

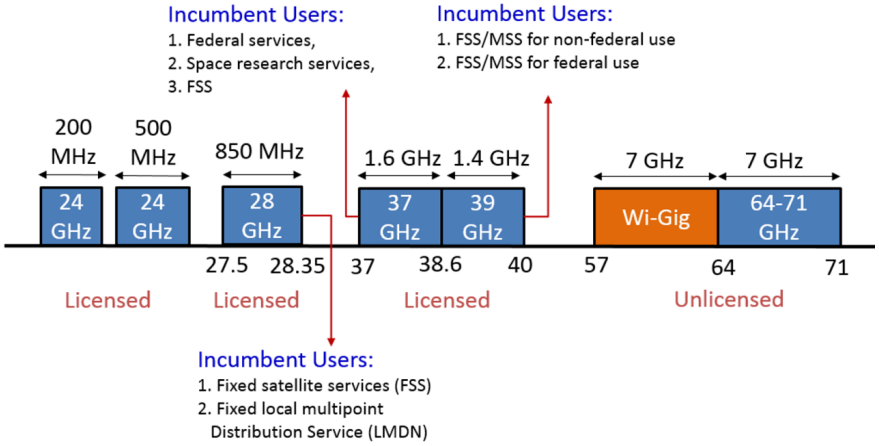


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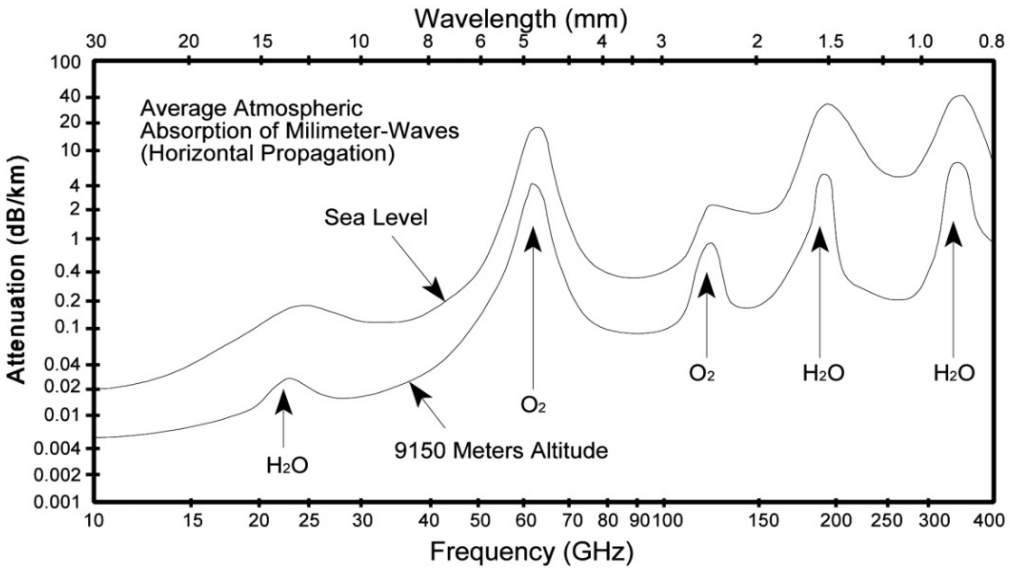


Figure 1.2: Average atmospheric attenuation vs. frequency at sea level and 9 km showing the attenuation increases with frequency with prominent windows in the 30-40 GHz range and around 90 GHz. Image from [1]

Applications at millimeter wave frequencies span commercial communications, military systems, radio astronomy, imaging, and automotive radar. These bands are particularly attractive due to the availability of large bandwidths and reduced spectral congestion compared to lower frequency allocations, which leads to lower interference for high data rate links. In particular, Federal Communications Commission (FCC) allocations in V- and W- bands include private sector point to point links from 71–76, 81–86, and 92–95,GHz [5], as well as unlicensed V-band allocations from 57–64 and 64–71,GHz [6, 7]. Leveraging these wide bandwidths, W band communication systems have demonstrated data rates of 78 Gbps, 80 Gbps, and 91.6 Gbps using 64-QAM and 16-QAM modulation schemes [8–10].

Millimeter wave communications are also of significant interest for fixed satellite services and space exploration missions [11, 12]. In addition, Ka-band low-Earth orbit (LEO) satellite constellations are increasingly deployed for both civilian [13] and military applications [14]. The close proximity of large LEO constellations to ground users increases both per user bandwidth and total system capacity due to the large number of simultaneous links and channels. The use of W-band carrier frequencies further enables a reduction in the number of transmission pathways, allowing allocated resources to be dynamically rerouted in the event of link failures.

Radar systems also benefit substantially from millimeter wave operation due to the improved spatial resolution enabled by shorter wavelengths. Automotive radar is a prominent example, with systems operating in the 76–77 GHz band [15] and the 79 GHz band, the latter offering up to 4 GHz of instantaneous bandwidth [16]. Beyond automotive sensing, advanced radar platforms include three dimensional imaging 100 GHz multiple-input multiple-output (MIMO) frequency-modulated continuous-wave (FMCW) radar [17], cloud Doppler radar arrays employing GaN MMIC power amplifiers [18], and a 93.5–94.5 GHz MIMO FMCW radar capable of simultaneous transmission [19].

Passive millimeter wave systems are widely used in radiometry and imaging applications, including security screening systems that employ compact low noise radiometric sensors [20]. Radio astronomy has similarly benefited from millimeter wave operation, where large available bandwidths allow improved sensitivity and reduced gain requirements for a given temperature resolution compared to lower frequency bands [21]. However, a key limitation of passive imaging systems is reduced spatial resolution at longer

distances. For active transmit systems, a primary challenge is achieving sufficient output power to overcome increased atmospheric attenuation at these frequencies. Significant progress has been demonstrated in this area, including solid state active denial systems operating at 92 GHz with 7-kilowatt level output power [22], as well as compact pulsed solid-state amplifiers that combine 128 GaN MMICs to achieve 100 W of output power at W band [23].

To achieve the required power levels using solid-state technology, wide bandgap compound semiconductors have been developed, with gallium nitride (GaN) on silicon carbide (SiC) being the most successful to date. Therefore, the power amplifiers demonstrated in this thesis all use GaN-on-SiC, and are shown in Fig. 1.3.

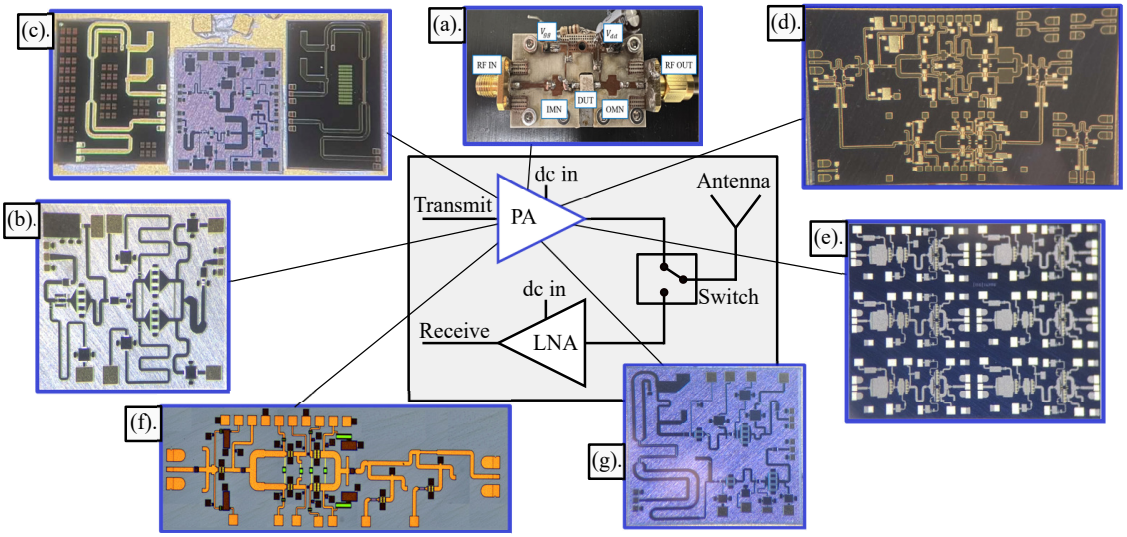


Figure 1.3: Basic transmit and receive module with the power amplifier (PA) element outlined in blue and power amplifiers (PAs) discussed in this thesis covering a range of frequencies and implemented with different device technologies. The 2-4 GHz hybrid PA with a packaged CGH40006P 6-W GaN HEMT shown in (a) and the 10-GHz GaN MMIC (b) are microwave-frequency proof-of-concept designs described in Chapters 2 and 3. The millimeter-wave PAs are described in the remaining thesis chapters: (c) a Ka-band 14-28 GHz broadband GaN MMIC PA with external GaAs passive diplexers; (d) a E-band 50-90 GHz MMIC with integrated diplexers; (e) a three-stage W-band (77 GHz) PA repeated 6 times on the die for driving and power combining experiments; (f) a W-band load-reconfigurable PA 77 GHz; and (g) a Ka-band 14-28 GHz broadband GaN MMIC PA with integrated GaN passive diplexer.

1.2 Gallium Nitride for Millimeter-Wave Power Amplifiers

Gallium Nitride (GaN) transistors were first demonstrated in the 1960s and are now widely available, especially at low microwave frequencies. GaN is a wide bandgap semiconductor belonging to the III-V compound group, with a 3.4 eV energy bandgap compared to 1.4 eV of GaAs. This results in transistors that can operate at high dc voltages and consequently high output powers. GaN does not have a native substrate that is easy to grow, so GaN layers are grown on silicon or silicon carbide (SiC) substrates. Although there are some GaN-on-Si processes available at microwave frequencies, they are generally made for power electronics, while most microwave GaN transistors use SiC as a substrate. In addition to better high-frequency operation, the SiC substrate also offers much better thermal properties with a thermal conductivity that is 3 times higher than Si and times higher than GaAs. GaN devices can operate reliably at higher temperatures compared to GaAs and Si, resulting in longer lifetimes. For example, the channel in a GaN device can operate at 500° higher temperature than GaAs for a 1-million median time to failure.

1.2.1 GaN Processes used for PA Implementations

This thesis employs four advanced GaN-on-SiC processes with gate lengths ranging from 150 nm to 40 nm, enabling PA designs from X–band through W–band. Key process parameters are summarized in Table 1.1. As gate length and bias voltage are reduced to allow for higher-frequency operation, the achievable power density (p_{out}) decreases from 4.5 W/mm to 2 W/mm, representing a necessary trade off. Substrate thickness is also reduced from 100 μm (4 mils) to 50 μm (2 mils) for higher frequencies, resulting in narrower microstrip lines and increased passive-circuit loss. The most advanced processes, QGaN09-ES and HRL T3, which operate above 50 GHz and into W-band, exhibit substantially lower P_{out} and PAE compared to lower-frequency GaN technologies. This performance reduction is primarily due to decreased breakdown voltage from scaling the gate, source, and drain dimensions to increase f_T and f_{max}. In addition, higher-frequency operation reduces skin depth and increases conductor resistance, further limiting the effective current cross-section and increasing conduction losses.

Achieving millimeter-wave performance in GaN technologies requires gate lengths scaled to tens of

Table 1.1: Comparison Table of GaN Processes

Process	Gate Length	Substrate Thickness	V_{dd}	f_T	p_{out}	PAE	Gain
NP15-00	150-nm	4-mil (100-μm)	28 V	34.5 GHz	4.5 W/mm*	55 %*	13 dB*
NP12-01	120-nm	2-mil (50-μm)	28 V	38.5 GHz	3.37 W/mm*	38.5 %*	14.5 dB*
QGaN09-ES	90-nm	2-mil (50-μm)	18 V	115 GHz	2.25 W/mm†	51 %†	6 dB$^{\#}$
HRL T3	40-nm	2-mil (50-μm)	12 V	160 GHz	2 W/mm^{+}	56 %$^{+}$	1.8 dB^{+}

* @29 GHz, $^{+}$ @94 GHz, † @35 GHz, $^{\#}$@80 GHz

nanometers and high saturation-velocity channels [2]. These requirements drive the use of complex heterostructures, which introduce greater process variability than lower-frequency GaN nodes [24].

1.3 Transistor Stackup

The performance of a power amplifier is directly related to the accuracy of the transistor models used to predict the behavior of the physical device. To understand these limitations, the complex epitaxial stackup required for high frequency GaN MMICs is first examined. An example AlGaN HEMT stackup representative of the HRL T3 process is shown in Fig. 1.4. This heterojunction device is formed by sequentially growing multiple semiconductor layers using epitaxial techniques such as molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) [2, 25].

The source and drain ohmic contacts are designed to provide low resistance access to the conducting channel. Optimization of the GaN layers enables the formation of a two dimensional electron gas (2DEG) at the AlGaN/GaN interface, created from varying Fermi energy level [26]. The 2DEG layer formed serves as a high electron mobility layer confined within a narrow space in the GaN channel layer, very close to the AlN buffer. The AlGaN barrier layer is intentionally doped to donate electrons, while the GaN channel layer is undoped. The AlN buffer layer separates the two layers and also improves electron mobility in the channel

The key outcome of this complex stackup is a significant enhancement in transconductance, enabling efficient modulation of the channel charge by the applied gate to source voltage. Amplification occurs because the power required to control the channel is much lower than the power the device is capable of

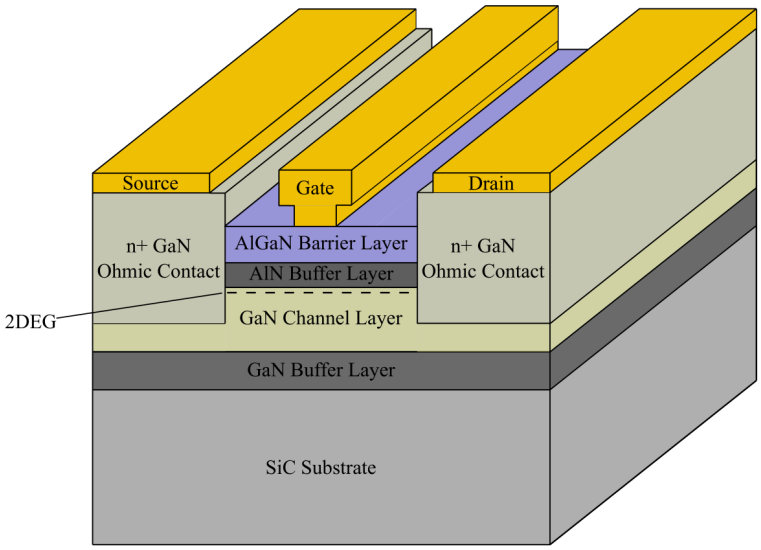


Figure 1.4: AlGaN HEMT device stackup with T-gate based on [2].

delivering to a load. To further improve high frequency performance, the gate electrode is implemented in a T-shaped geometry, which reduces the intrinsic gate to source and gate to drain capacitances, C_{gs} and C_{gd}.

These design tradeoffs are reflected in a simplified expression for the cutoff frequency f_{T}, defined as the frequency at which the device exhibits unity current gain,

$$f_{\mathrm{T}} = \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)}. \tag{1.1}$$

From this relationship, it is clear that high frequency operation is achieved by maximizing the transconductance while minimizing parasitic capacitances inherent to the device structure. Finally, the full AlGaN and GaN epitaxial stack is grown on a 50 μm SiC substrate, which provides superior thermal conductivity, low RF loss, and mechanical support for high power millimeter wave operation. It is important that this complex stackup is represented well and that the nonlinear characteristics are captured sufficiently. This is one of the major limitations in millimeter PA design using developmental processes.

1.3.1 Nonlinear Models

Accurate active device models are typically developed from measured dc characteristics and S-parameters, forming the basis for both linear and nonlinear models [27]. Linear models can be reasonably covered through equivalent circuit models that use preset analytical expressions of the model elements and values extracted from measured data over large signal conditions. Nonlinear behavior, however, requires time-frequency domain techniques implemented in computer aided design (CAD) tools, with harmonic balance (HB) simulations used for steady state large signal analysis. Nonlinear models generally fall into two categories [28]: empirical black box models [29, 30] and equivalent circuit (EC) models [31, 32]. Black box models rely on extensive measurements and look up tables, offering high accuracy but limited scalability beyond the measured device and bias conditions. EC models are more flexible, but difficult to accurately scale with device size and bias.

In GaN HEMTs, nonlinearities arise from bias dependent transconductance, voltage dependent capacitances, charge trapping effects, and self heating, all of which become more pronounced at high power and millimeter wave frequencies [33, 34]. At higher frequencies, interactions between intrinsic nonlinearities and parasitic elements complicate model extraction and validation, making large signal simulation accuracy highly dependent on how well these effects are captured across bias and frequency [35]. This challenge is exacerbated at W band, where accurate high frequency measurements are difficult to obtain [36]. Furthermore, deembedding accuracy becomes critical, as conventional short open load through (SOLT) calibration is often inadequate due to poorly defined reference planes [27]. Multi-line thru-reflect-load (mTRL) calibration is preferred since standards can be fabricated on the same substrate as the device under test (DUT) [37].

As shown in Chapter 5, variations of up to ±30 % and greater than in physical or model parameters can significantly alter the device impedance, ultimately degrading PA performance [4, 24, 38]. Consequently, successful millimeter wave PA design relies on accurate and scalable models that reliably capture bias, temperature, and geometry dependence.

1.4 Power Amplifier Design

The design of microwave power amplifiers (PAs) often requires a trade-off between a large number of input variables to achieve the best performance [39]. While the demands on carrier frequencies are increasing for the applications mentioned above, the PA efficiency remains critical, as the PA is typically the largest contributor to power consumption during transmission in communications and radar systems [40]. Since a large fraction of input dc power is dissipated as heat, efficient PA design is essential for reducing operating costs and cooling requirements, and device increasing lifetime. However, efficiency and bandwidth are often competing objectives, making it a challenge to realize both simultaneously. Multi-objective analysis provides a method for navigating these trade-offs and aiding designers at different stages of the PA development process.

This thesis investigates PA architectures and techniques that address diverse design requirements, including load reconfigurability, wideband operation, and efficiency enhancement techniques.

1.4.1 Multi-Objective Visualization for PA Design

This thesis presents an efficient method for analyzing trade-offs during various stages of a PA design. The multi-objective visualization (MoV) method is considered a preference-based interactive *a priori* visualization method that is based on other optimization black-box multi-variate problems where no analytical function exists. The method gives the designer multiple solutions that meet predefined requirements and provide a compromise among the desired objectives. The design approach takes simulation data based on a transistor nonlinear model and presents it in an interactive format referred to as "parallel coordinate plots" that significantly reduce the time needed for trade-off decision making and builds designer intuition.

An example parallel coordinate plot, discussed in detail in Chapter 3, provides an example of this form of interactive visualization. This plot is made for a $8 \times 100\,\mu$m GaN HEMT where the lines connecting the parallel axes contain information from simulated source and load-pull contours based on the device nonlinear model provided by the manufacturer. From the left, the 1^{st} through 4^{th} vertical columns are the simulated range of the desired reflection coefficients. The 5^{th} through 8^{th} columns are the minimum and maximum PAE and P_{out} values that we are trying to make a trade off between. The single red line is the solution chosen

that contains a single value from each column and represents the starting point of the PA design in this case.

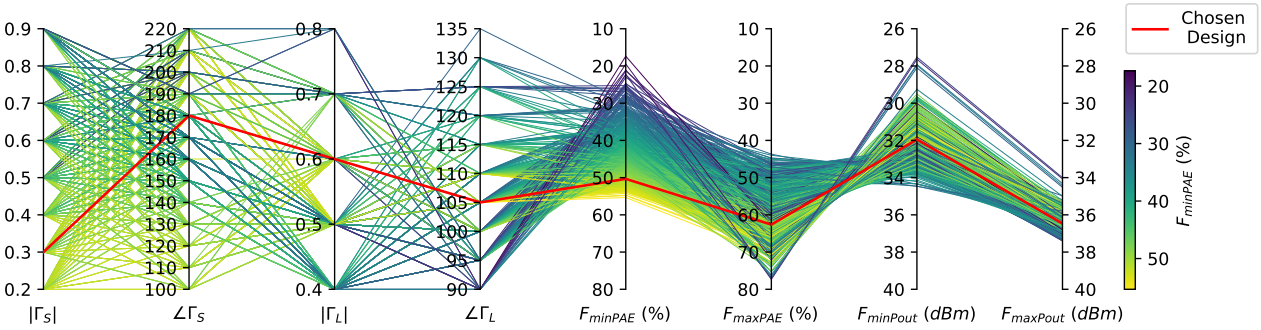


Figure 1.5: MoV plot showing the simulated source- and load-pull data for a $8 \times 100\,\mu$m GaN HEMT with varied Γs and aminimum/maximum PAE and maximum/minimum P_{out}

There is no unique optimal solution for a multi-objective problem; instead, a collection of solutions exist that represent a compromise of the desired objectives. Chapters 2 and 3 discuss how such plots are used to make choices for target impedances when designing wideband and multistage power amplifiers.

1.5 Thesis Outline

This thesis focuses on GaN-on-SiC power amplifiers, divided into two sections. Multi-objective visualization is introduced first for the basic PA design problem (Chapter 2 and Chapter 3). Here numerous examples are provided along with four different PA designs with measurements. Next, high frequency narrowband MMIC PA designs are analyzed in Chapter 4 and Chapter 5. Last two different approaches to diplexed power amplifier topologies are analyzed in Chapter 6 and Chapter 7. The thesis is concluded and future work presented in Chapter 8.

- Chapter 1 introduces motivation for millimeter-wave applications, provides background on GaN, summarizes the processes used throughout the thesis, discusses power amplifer design, and introduces multi-objective visualization for PA design.

- Chapter 2 introduces multi-objective visualization (MoV) for PA design and provides background, basic theory, and introduces the two distinct methods. The rest of the Chapter demonstrates one of

the methods, the *Load-Pull Extraction* method, and implements it on two different hybrid S-band PAs and an X-band MMIC PA designed for supply modulation.

- Chapter 3 extends the MoV method presented in Chapter 2 through the *Specific-Trade-Off* method demonstrated on an X-band MMIC design and applied to dielectric layer variation for shunt matching capacitors. Additionally, the X-band MMIC is supply modulated for a 34 and 67 MHz signal to show PAE improvement. The method is also applied to a multi-stage load-pull to capture bilateral transistor effects and aid in the two-stage Ku-band MMIC design.

- Chapter 4 presents a three stage narrowband MMIC GaN PA in the Qorvo GaN09 process in a developmental process. The PA is characterized in measurement up to 11 dBm of input power and a cascaded PA configuration is included to achieve more output power. The design shows closer agreement to simulation than previous experience with the process a few years prior. Only one nonlinear device model was permitted, limiting design architecture and performance.

- Chapter 5 presents a three stage load-reconfigurable MMIC GaN PA in the HRL T3 process. Extensive explanation of stability at W-band is presented along with the reconfigurable matching element. Additional analysis to identify simulation vs. measurement discrepancy using parameter extraction is also included.

- Chapter 6 presents a quasi-MMIC GaAs/GaN diplexed power amplifier covering Ku- to Ka-band. This demonstration of the topology utilizes the lower loss tangent of GaAs for a coupled line filter design and then higher power density of GaN for the PA. The MMICs are wire bonded together and the performance is analyzed.

- Chapter 7 presents another approach to diplexed PAs with an E-band design covering ≈45–90 GHz. This design in the HRL T3 process features two different three stage PAs and a reflectionless diplexer filter design.

- Chapter 8 provides a summary of the thesis conclusions and contributions, and discusses some avenues for future work.

Chapter 2

PA Design with Multi-Objective Visualization

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2.1 Multi-Objective Visualization

2.1.1 Motivation

The design of an RF power amplifier (PA) often involves trade-offs between a large number of input parameters such as device size, frequency range (RF bandwidth), input power range, supply voltage, and gate bias [41]. The input and output matching networks are then designed for, e.g. a specified output power (P_{out}) with maximized power-added efficiency (PAE) and saturated gain. The output impedance for highest power is

usually not the same for best efficiency, so the designer is faced with a trade-off. This is usually done by an observation of load-pull power and efficiency contours [39]. When additional input variables, such as supply voltage in efficiency-enhanced envelope tracking amplifiers [42], gate bias for linearization [43], frequency or multiple gain stages are a part of the design, the trade-off is not intuitive. The data-based selection method presented in this chapter can assist the designer and save time during the design process, as well as provide intuition about a particular or active device behavior for future design.

2.1.2 Background

Multi-objective visualization (MoV) can be used to sort the information and make the design process more time efficient. The MoV method is considered a preference-based interactive *a priori* visualization method that is based on other optimization black-box multi-variate problems where no analytical function exists. There is no unique optimal solution for a multi-objective problem; instead, a collection of Pareto solutions exist that represent a compromise of the objectives [44, 45]. Compared to single-objective methods, design goals corresponding to variables with different units can be compared and an analysis made without having to convert units.

Instead of training e.g. a neural network, the method is geared towards training the designer. The MoV method allows viewing high-dimensional datasets interactively and filtering the data accordingly. This method also addresses other issues commonly seen in parallel coordinate plots such as data clutter and fixed axes leading to implicitly defined pattern development [46]. The user can use "brushing," a technique to interactively select a subset of data, and reordering of axes to explore other patterns within the data.

2.1.3 History

Parallel coordinate plots such as the one in Fig. 2.1 have been successfully applied to a wide range of problems. The first recorded usage was in 1833 by amateur French statistician, André-Michel Guerry [3]. Guerry analyzed social issues relating crime, suicide, literacy rates, age, etc. using parallel coordinate plots. Later work was done on graphical calculation of mathematical functions in 1885 by Philbert Maurice d'Ocagne [47]. Around the same time parallel coordinate plots were used in analysis of census data in the

United States [48]. The technique was then popularized again in 1959 with Alfred Inselberg who developed applications in collision avoidance algorithms for air traffic control and data mining, both briefly covered in [49]. More recently, MoV has been applied to power systems operation analysis [50] and described as a hyper dimensional data analysis tool in [51, 52].



INFLUENCE DE L'AGE.

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2	Viol sur des adultes.	169	Assassinat.	157	Assassinat.	154	Blessures et coups.	101	Assassinat.	182	Viol sur des enfans.	165	Blessures et coups.	157
3	Meurtre.	147	Meurtre.	140	Meurtre.	132	Meurtre.	133	Blessures et coups.	122	Assassinat.	159	Meurtre.	125
4	Viol sur des enfans.	101	Rébellion.	111	Rébellion.	110	Rébellion.	100	Rébellion.	90	Blessures et coups.	135	Assassinat.	102
5	Assassinat.	101	Viol sur des adultes.	105	Viol sur des adultes.	73	Viol sur des enfans.	94	Viol sur des enfans.	85	Faux témoignage.	99	Faux témoignage.	102
6	Rébellion.	76	Infanticide.	85	Infanticide.	63	Faux témoignage.	68	Faux témoignage.	76	Rébellion.	78	Rébellion.	91
7	Infanticide.	68	Viol sur des enfans.	58	Viol sur des enfans.	59	Viol sur des adultes.	61	Viol sur des adultes.	32	Infanticide.	42	Empoisonnement.	23
8	Bless. env. accomp.	67	Bless. env. accomp.	50	Bless. env. accomp.	58	Bless. env. accomp.	44	Infanticide.	24	Empoisonnement.	36	Infanticide.	23
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10	Faux témoignage.	29	Empoisonnement.	14	Empoisonnement.	25	Empoisonnement.	28	Bless. env. accomp.	19	Associat. de malfait.	18	Associat. de malfait.	11
11	Empoisonnement.	11	Crim. env. des enf.	10	Crim. env. des enf.	16	Associat. de malfait.	19	Avortement.	15	Viol sur des adultes.	14	Voies de fait, etc.	11
12	Voies de fait, etc.	8	Associat. de malfait.	10	Associat. de malfait.	13	Bigamie.	13	Bigamie.	13	Crim. env. des enf.	11	Bless. env. accomp.	7
13	Mend. av. violence.	6	Parricide.	8	Parricide.	9	Mendicité.	8	Mendicité.	13	Bless. env. accomp.	7	Parricide.	"
14	Crim. env. des enf.	5	Voies de fait, etc.	6	Mend. av. violence.	8	Crim. env. des enf.	7	Parricide.	13	Associat. de malfait.	7	Crim. env. les enf.	"
15	Parricide.	5	Avortement.	5	Bigamie.	6	Avortement.	7	Associat. de malfait.	13	Bigamie.	7	Avortement.	"
16	Avortement.	3	Mend. av. violence.	3	Avortement.	6	Parricide.	4	Crim. env. des enf.	6	Voies de fait, etc.	7	Bigamie.	"
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Figure 2.1: A photo from first recorded usage of parallel coordinate plots by André-Michel Guerry in 1883 [3]. The plot contains different columns with data of individuals' ages and the crimes they committed with horizontal lines connecting them to identify trends over a 10-year period.

2.1.4 Solution Domination

In PA design, the two conflicting objectives that are commonly traded off are PAE and P_{out}. In the top left of Fig. 2.2 these two objectives are represented with increasing values on the x and y axes. An ideal solution is illustrated by the black dot with the highest PAE and P_{out} available from a device for a specific bias and frequency. Boundary solutions that have the highest PAE or P_{out} are represented as the green star and pink pentagon. Comparing the solutions associated with the red triangle and blue square shows that the red triangle outperforms the blue square with respect to PAE and P_{out}. One would never pick the blue solution and formally we say that the red solution *dominates* the blue solution. Similarly, the solution associated with the pink pentagon is better than the one marked by the red triangle with respect to P_{out}. Conversely, the green-star solution outperforms the red triangle with respect to PAE. Therefore the red, green, and pink solutions most effectively capture the trade-off between PAE and P_{out}. These solutions are referred to as

"non-dominated" because they perform better than or equal to all others w.r.t. at least one objective. The full set of non-dominated solutions are also known as the Pareto front, i.e. "best-of-the-best". In the left plot of Fig. 2.2, they are represented by the black dashed line curve. The right plot of Fig. 2.2 shows the same data transformed into a set of parallel coordinate plots. The two columns contain the objectives, PAE and P_{out} and the colored horizontal lines represent the solutions corresponding to those in the plot on the left.

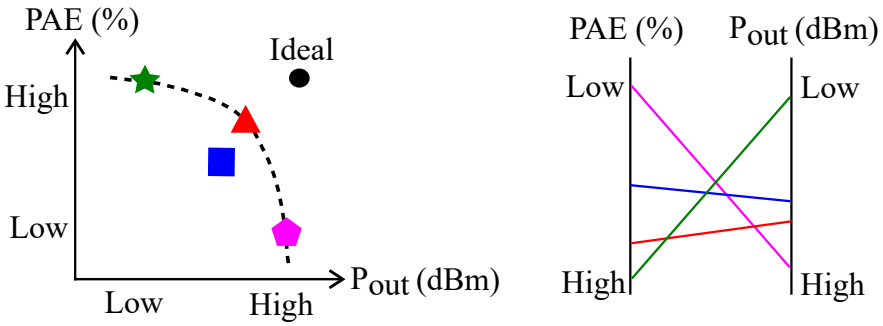


Figure 2.2: Left: illustration of possible solutions for PAE and P_{out} of a PA are represented by colored dots, with the black dotted curve representing a collection of non-dominated solutions with performance not exceeded by any other solution w.r.t. at least one objective. Right: example of the construction of the corresponding MoV parallel plot.

2.2 Multi-Objective Visualization Approach for PA Design

The discussion in this section is based on [44], where the basic multi-objective optimization problem is formulated as

$$\begin{aligned} &\max/\min \quad \{F_1(\mathrm{x}), F_2(\mathrm{x}), ..., F_k(\mathrm{x})\} \\ &\text{subject to} \quad \mathrm{x} \in S \ \text{ and } \ k \geq 2, \end{aligned} \tag{2.1}$$

and the vector of objective function is $F(\mathrm{x}) = (F_1(\mathrm{x}), F_2(\mathrm{x}), ..., F_k(\mathrm{x}))$. The decision variable vector is written as

$$\mathrm{x} = (\mathrm{x}_1, \mathrm{x}_2, ..., \mathrm{x}_n) \tag{2.2}$$

constrained within a feasible region S. Applying this formulation to the PA design example shown in Fig. 2.2, the objectives are PAE and P_{out} which are inherently conflicting as discussed briefly in Chapter 1. Thus, the

general PA design multi-objective optimization problem can be written as

$$\underset{\mathrm{x}}{\text{maximize}} \quad [F_{PAE}(\mathrm{x}), F_{P\text{out}}(\mathrm{x})] \tag{2.3}$$

The vector of decision variables (x) are parameters the designer adjusts to balance conflicting objectives simultaneously. Traditional Pareto-based optimization computes all non-dominated solutions, which can be computationally expensive and impractical for large design spaces. The MoV method requires only part of the Pareto optimal points to be generated and evaluated. The decision maker can set a predefined range of decision variables that, for example, cover only the intersecting range of objectives rather than the entire feasible solution space. As shown in Fig. 2.3, a subset of impedances—black 'x' markers—represents the overlap of PAE and P_{out} load-pull contours on the Smith chart. This illustrative chart is simulated load-pull of the CGH40006P GaN HEMT, from 2–4 GHz in 2 GHz steps. Instead of analyzing the entire Smith chart, the designer can constrain the search space to this overlap region, significantly reducing computational effort and decision-making complexity.

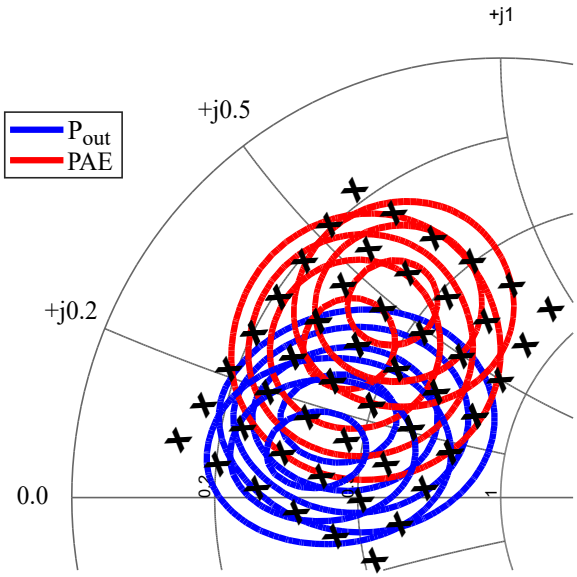
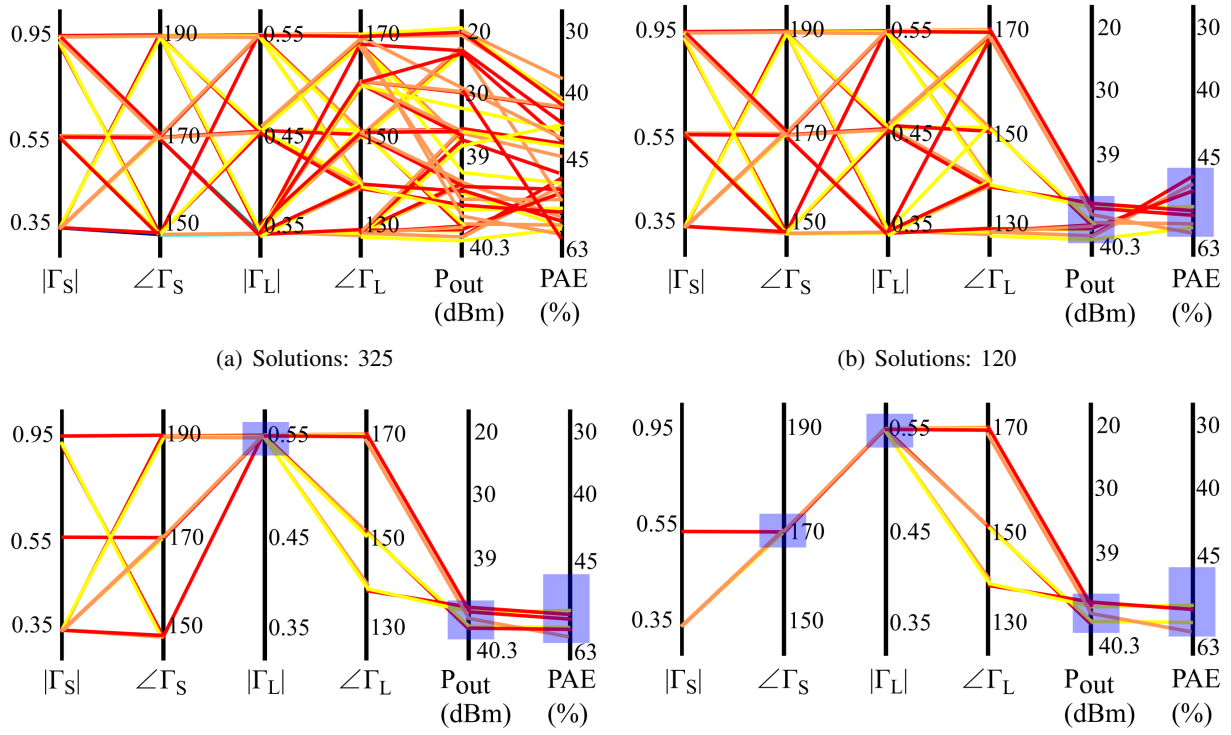


Figure 2.3: Plot of smith chart with simulated load-pull contours PAE and P_{out} in red and blue, respectively for the CGH40006P GaN HEMT, from 2–4 GHz in 2 GHz steps. Black 'x's represent the sub selected points used to create a multi-objective visualization plot. Only the intersecting regions of the maximum PAE and P_{out} contours are taken as the trade-off impedance will be somewhere in their cross section.

Once the simulated data is captured, the PA multi-objective design problem can be fully formulated.

Referring to Eq. (2.2) and (2.3), the vector of decision variables is now expanded to a 4-element vector $\mathbf{x} = (|\Gamma_S|, \angle\Gamma_S, |\Gamma_L|, \angle\Gamma_L)$, and $\mathbf{x}_1$ to $\mathbf{x}_4$ are specific values of the source and load reflection coefficients. The example MoV plot created from load- and source- pull data for a microwave power transistor is shown in Fig. 2.4. In this plot, (a) shows all of the possible simulated combinations of $|\Gamma_S|, \angle\Gamma_S, |\Gamma_L|, \angle\Gamma_L$ collected from Fig. 2.3 and a source-pull simulation (not shown here).



(a) Solutions: 325

(b) Solutions: 120

(c) Solutions: 40

(d) Solutions: 8

Figure 2.4: Interactive visualization of solution filtering for PAE and P_{out}: (a) all non dominated solutions; (b) reducing the range of acceptable PAE and P_{out}; (c) narrowing down the load reflection coefficient magnitude; and (d) further constraints on the source reflection coefficient phase. The number of solutions retained is shown below each figure.

To illustrate, four steps in the MoV process performed by the designer are outlined in Fig. 2.4, showing how data can be quickly and interactively filtered to arrive at a starting point. In Fig.2.4(b) "brushing boxes" are placed on the PAE and P_{out} columns to only show solutions that have $PAE \geq 45\,\%$ and $P_{\text{out}} \geq 40\,\text{dBm}$. This immediately narrows down the possible solution space. Note, none of the data columns are weighted and are equally relevant to selecting the solution. In (c) and (d) the designer has "brushed" the other columns to filter solutions even further and identify what combination will result in the best compromise of the

competing objectives. The number of possible solutions reduces from 325 in (a) to 8 in (d) in a matter of seconds.

As the designer interacts with the columns and filters particular solutions, they learn the trade-off behavior of the specific design problem. Additional relevant variables can be included, such as RF bandwidth (f), V_{dd}, and V_{gg}, shown in later sections. These can be classified as state variables, which are *a priori* selected conditions that the non-dominated solutions must satisfy over their entire range.

In the next two chapters we separate the multi-objective problem into two different methods. The first method discussed in more detail is referred to as the *Load-Pull Extraction* method, particularly beneficial in the early stage of PA design, providing the user with intuition on active device behavior and limitations The second method, covered in Chapter 3, is called the *Specific-Trade-Off* method and is used at various points in the design flowfor targeted analyses that are more unique like multi-stage amplifiers and component sensitivity.

2.3 Load-Pull Extraction Method

The *Load-Pull Extraction* (LPE) method is a technique within the MoV framework that uses simulated load- and source-pull data to generate parallel coordinate plots for design analysis. This method is particularly well-suited for the early stages of PA design, where it can significantly reduce the need for time-consuming iterative tuning typically required when working with conventional load- and source-pull simulations.

2.3.1 Case Study: Hybrid PA

As discussed previously, a common method for PA design involves simulating (or measuring) output parameters for a range of input and output reflection coefficients, referred to as automated source and load-pull. For example, in a single-stage PA (Fig. 2.5), the swept input variables include ($|\Gamma_L|, \angle\Gamma_L$), input power ($P_{in}$), drain bias voltage ($V_{dd}$) and frequency range ($f$), with specified targets in output power and efficiency. Load-pull simulations for many input variables result in contours that make the trade-off non-trivial. This is illustrated in Fig. 2.6, where load-pull for PAE and P_{out} contours of a Qorvo GaN bare die are shown from

2.5–5 GHz for supply voltages between 20 and 28 V. Finding the reflection coefficients that will give, for example, highest efficiency with P_{out} within 2 dB of P_{max}, is an iterative process of selecting $(|\Gamma_S|, \angle\Gamma_S)$ and $(|\Gamma_L|, \angle\Gamma_L)$ and does not guarantee the best solution. To improve the process of choosing input and output impedances for matching and bias circuit design, we evaluate a black-box analysis method.

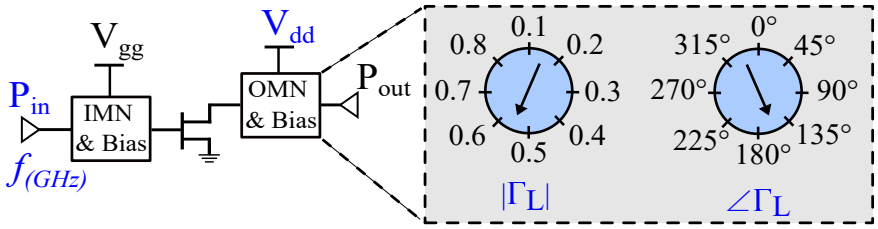


Figure 2.5: Block diagram of single-stage power amplifier where during the design process the input and output reflection coefficients are varied to achieve a good compromise in PAE and P_{out}, while the variables in blue (f, P_{in}, V_{dd}) are swept.

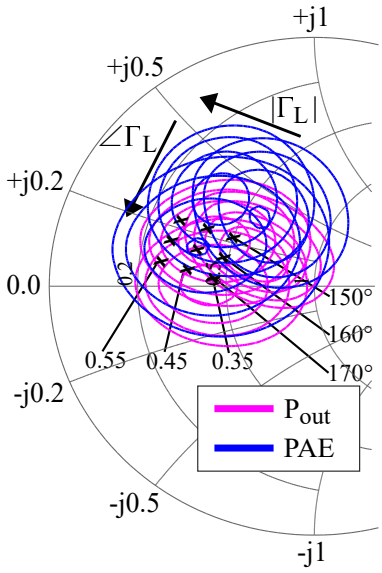


Figure 2.6: Simulated load-pull contours for the TGF2023-2-02 GaN bare die when $V_{\text{dd}} = [20, 24, 28]$, and P_{in}, f are varied from (20–30) dBm in 5 dB steps, and (2.5–5) GHz by 0.5 GHz steps. The trade-off between P_{out} and PAE is difficult to make by observing the contours.

As a case study source- and load-pull simulation sweeps are run in Cadence Microwave Office (AWR), using a foundry nonlinear model for a Qorvo TGF2023-2-02 12-W HEMT die fabricated in the 250-nm GaN-on-SiC process. Drain voltage (V_{dd}) is swept from 16–26 V in 2 V steps, frequency (f) from 2.5–5 GHz in

0.5 GHz steps, $|\Gamma_S|$ from 0.7–0.9 in 0.1 steps, $\angle\Gamma_S$ from 140°–205° in 7° steps, $|\Gamma_L|$ from 0–0.7 in 0.05 steps, and $\angle\Gamma_L$ from 125°–180° in 5° steps. The Γ_S components are swept in large step sizes as their impact on the PA's output power and PAE is less than the Γ_L components. To further examine the usefulness of this method we further constrain the input variables and fix the gate voltage (V_{gg}) to -2.8 V and the input power (P_{in}) to 28 dBm (1 dB compression point).

The entire simulation set is then imported into a graphic user interface (GUI) that processes the AWR data and makes an interactive coordinate plot. An image representation of the entire solution set is shown in Fig. 2.7. The graphical implementation contains brightly colored lines connecting the parallel axes that contain information from source and load contours, with performance metrics for a minimum PAE, maximum and minimum P_{out}. The solutions in color are all of the non-dominated solutions and the solutions in grey in the background are the dominated solutions. The connecting lines represent possible solutions. From left to right, the first four columns are the decision vectors and have no preferred vertical direction indication. The next three columns represent the objectives PAE and P_{out} broken down into more specific data types. The objective (F_{minPAE}) is the minimum PAE achieved over the entire range of drain voltages and frequencies. Note, the drain voltage range is included to allow for supply modulation of the PA in future work. This objective captures the "worst case" PAE of the amplifier. Similarly, ($F_{minPout}$) captures the "worst case" P_{out} of the amplifier. Conversely, ($F_{maxPout}$) captures the "best case" P_{out} of the amplifier.

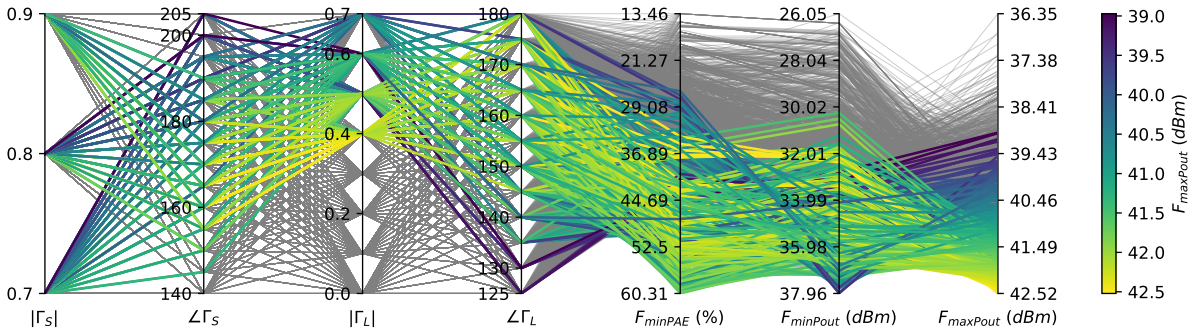


Figure 2.7: Parallel Plots to Visualize Nondominated and Dominated Solutions. Dominated solutions appear in grey while nondominated solutions are colored. Performance depicted over entire frequency range (2.5-5 GHz) and supply voltage (14-26 V).

This multi-objective visualization allows a PA designer to interactively select desired ranges within the

objective set (i.e.,"brushing") and also select a unique design which is a specification of the four decisions $(|\Gamma_S|, \angle\Gamma_S)$ $(|\Gamma_L|, \angle\Gamma_L)$ which we collect into a vector x as in Eq. (2.2) and (2.3). The multi-objective problem for this is formulated as,

$$\underset{\mathrm{x}}{\text{maximize}} \quad [F_{minPAE}(\mathrm{x}), F_{minPout}(\mathrm{x}), F_{maxPout}(\mathrm{x})] \tag{2.4}$$

The desired solution is selected from a subset of all the solutions in Fig. 2.7, a collection of just the non-dominated solutions is shown in Fig. 2.8. Brushing is used to interactively filter the non-dominated set based on designer intuition. Based on the non-dominated performance, we wish to achieve F_{minPAE} values greater than 55%, thus brushing is applied to that objective (depicted as rectangle in Fig. 2.8). Then we choose an allowed range for P_{out}, as is depicted by the brushing of the $F_{minPout}$ and $F_{maxPout}$ objectives in Fig. 2.8. This sub-selection results in the colored lines in Fig. 2.8. Among these, the selected solution is the one represented by the red line, giving $\Gamma_S = 0.7\angle 180°$ and $\Gamma_L = 0.5\angle 150°$. Once the parallel plots are created, this process requires only a few minutes to select a desired solution.

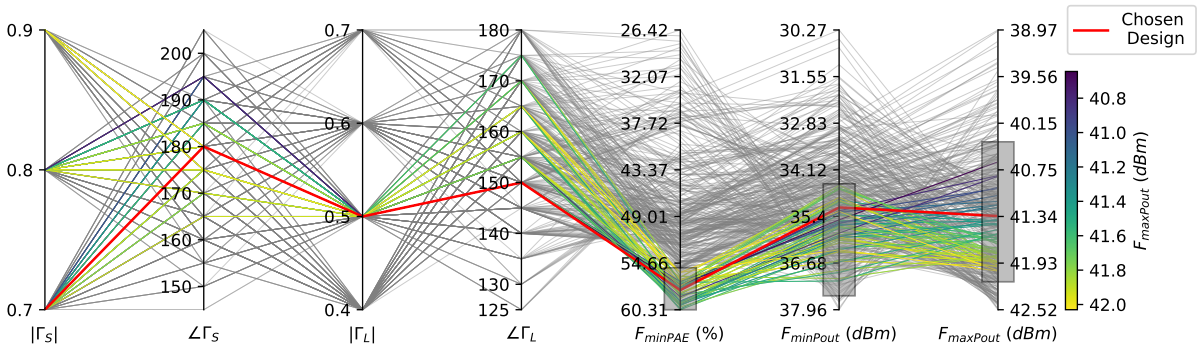


Figure 2.8: Using "Brushing" to Interactively Filter Nondominated Solutions. Filtered out solutions appear in grey while brushed solutions are shown in color. The chosen solution is depicted in red.

The PA is implemented with the Qorvo die on a 0.76-mm thick RO4350B substrate, for $Z_S = 8.82\,\Omega$ and $Z_L = 17.72 + j11.81\,\Omega$ input and output impedances. The circuit is designed using Cadence AWR MWO to minimize loss in the passive networks across 2.5–5 GHz, and incorporating biasing circuits into the single-line input matching network and a nonuniform 3-section line output matching network. To reduce coupling between the input and output matching networks, tapers are added leading to the device plane. This decreases the performance of the input and output networks independently, but improves performance of the

entire circuit when analyzed using the Axiem full-wave 2.5D simulator.

The circuit is fabricated and gold-plated for wirebonding of the die. The substrate and a stack of CuMo die carriers are silver-epoxied to a metal heat sink and the transistor is epoxied onto the carriers. The drain and gate pads are wire bonded with six and four 24.5-μm diameter gold bond wires, respectively. A parallel RC stability network is implemented with an 0402 100 Ω resistor and 1 pF capacitor in series at the gate, with additional low-frequency capacitors and resistors on the bias lines. A series inductance of 0.5 nH is added to the bond-wire inductance from the Modelithics model. This takes into account the slightly different die mounting from that shown in the Modelithics library, requiring a longer bondwire. The fabricated circuit is shown in Fig. 2.9.

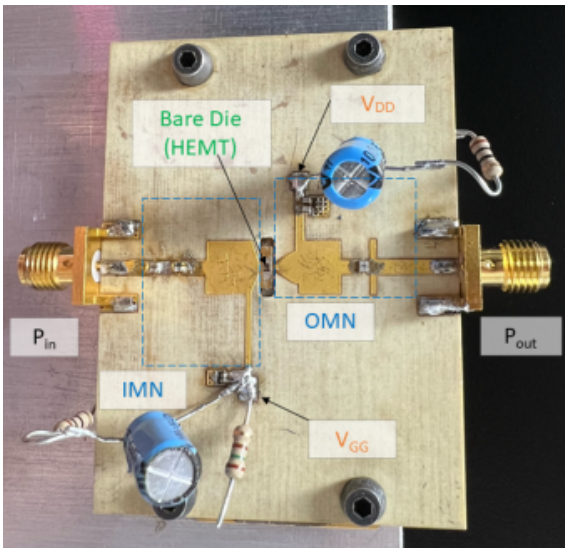


Figure 2.9: Photograph of 2.5-5GHz power amplifier designed using non-dominated Γ_S and Γ_L found from the interactive visualization method.

The measured and simulated frequency response is shown in Fig. 2.10 for three supply voltages, while the measured drive-up curves at three frequencies are shown in Fig. 2.11. The measured output power is within 3 dBm from 2.5 to 4.9 GHz. The highest PAE is 69% around 3.5 GHz at the lower supply voltages. The simulations predict the measured trends, except all measured parameters drop at 5 GHz.

In summary of this case study, a method for fast determination of input and output reflection coefficients that meet a wide range of PA performance goals is presented. The method is based on a standard load-pull simulation, and allows for interactive choice of design parameters in a matter of minutes. Validation

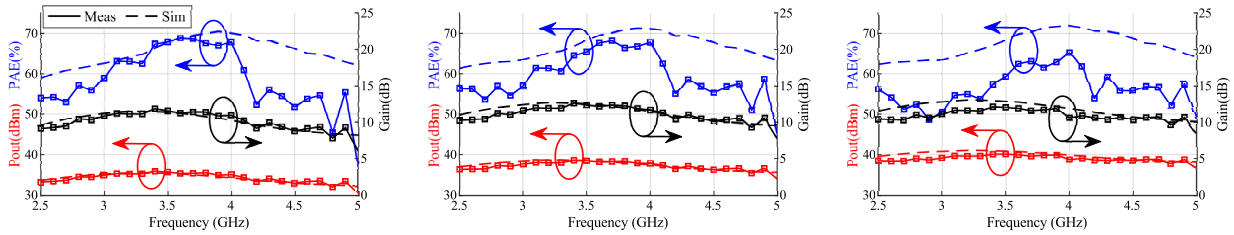


Figure 2.10: Measured (solid) and simulated (dashed) frequency performance. (a) P_{in} = 24 dBm and V_{dd} = 14 V (b) P_{in} = 26 dBm and V_{dd} = 20 V (c) P_{in} = 28 dBm and V_{dd} = 26 V.

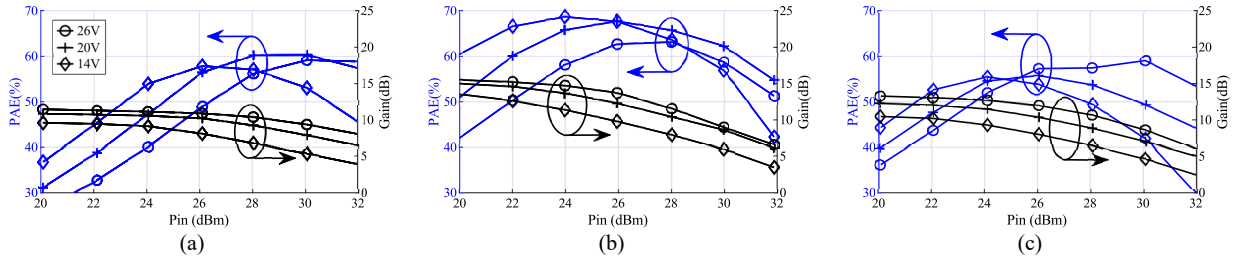


Figure 2.11: Measured PAE and Gain for V_{dd} =[14,20,26] V at (a) 2.5 GHz, (b) 3.7 GHz and (c) 4.9 GHz.

is shown on a hybrid PA covering an octave bandwidth, with a comparison to published PAs shown in Table 2.4. The first three references, [53–55], are all narrowband designs. The next two references in the table, [56,57] are more comparable in bandwidth to this work with lower peak PAE and/or less output power. Additionally, this PA is designed with specifications across a wide range of drain supply voltages, enabled by the multi-objective interactive visualization method.

Table 2.1: Amplifiers in literature using TGF2023-2-02.

Reference	PAE (%)	Frequency (GHz)	Output Power (dBm)
2010 [53]	84.9	2.15	39.14
2013 [54]	70	2.5	> 40
2011 [55]	80	3.5	38.45
2014 [56]	58	3-6.5	38.5
2019 [57]	61	1.75-2.05	41.2 ±0.5
This work	69	2.5-5	40

2.3.2 Case Study: Second Hybrid PA

This section presents the design of a wideband hybrid PA using the LPE method, where the Q factor of Γ_L and harmonic terminations guide the design. The Q factor is introduced as an additional metric, followed by the integration of harmonic terminations for PAE improvement. The design process is then outlined and validated through simulation and measurement using a packaged MACOM CGH40006P GaN transistor.

2.3.2a Quality factor

The Bode-Fano limit specifies the relationship between the loss and bandwidth of a passive matching circuit [58], [59], which can be expressed as in [60]:

$$\frac{BW}{\omega_0} \ln\left(\frac{1}{|\Gamma|_{\text{avg}}}\right) \leq \frac{\pi}{Q} \tag{2.5}$$

where Q is the quality factor, BW/ω_0 is the fractional bandwidth of the matching network and $|\Gamma|_{\text{avg}}$ is the frequency-averaged absolute value of the reflection coefficient of the matching network terminated in the system characteristic impedance. Equation (2.5) expresses the trade-off between the fractional bandwidth, the Q factor and the reflection coefficient of a matching network. In the case of a PA design, usually the Q factor of the matching network at the drain is not considered during design [61], and here we show how the LPE method can be extended to include the Q factor of the complex Γ as a decision variable for wideband matching tradeoffs.

The Q factor of the network at output (load-side) of a transistor amplifier is given by

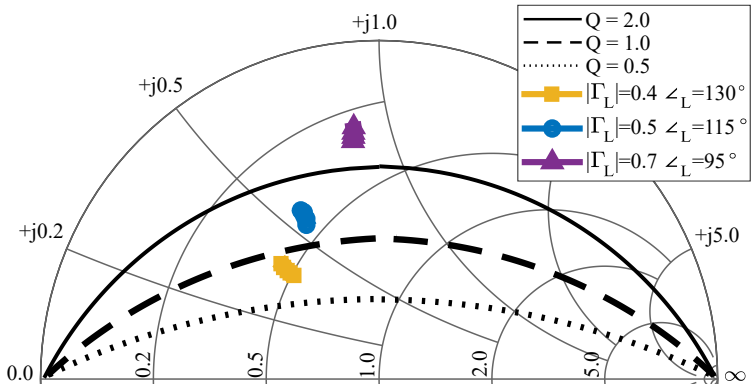
$$Q_L = \frac{|X_L|}{R_L} \tag{2.6}$$

where the impedance presented at the drain of the transistor is $Z_L = R_L + jX_L$. As a use-case example, the designer may find two similarly performing load reflection coefficients with different Q values. Choosing a load impedance with a lower valued Q factor can directly translate to a wider bandwidth of the matching network [62]. Fig. 2.12(a) illustrates constant Q-circles on a Smith chart with three example Γ_L points for the CGH40006P GaN HEMT, all simulated in 0.2 GHz steps from 1–4 GHz. Fig. 2.12 (b) presents the

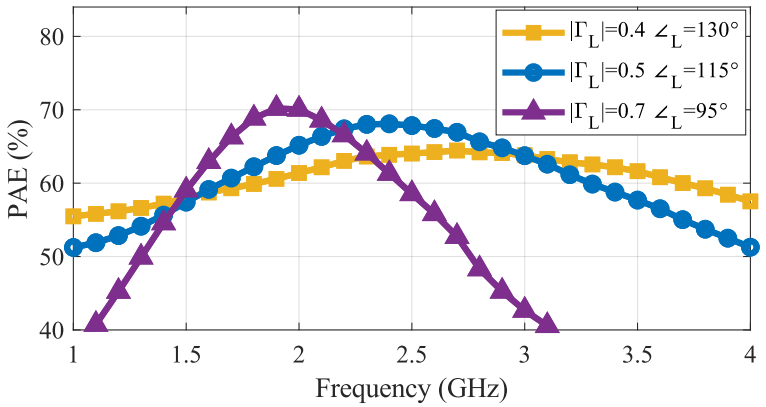
corresponding PAE frequency response for these Γ_L points. Table 2.2 summarizes the corresponding loads and calculated Q-factor values from in Fig. 2.12.

Table 2.2: Simulated Loads and Nodal Q factor Values

Load Symbols	$\lvert\Gamma_L\rvert$	$\angle\Gamma_L$	Q_L
Yellow Squares	0.4	130 °	0.7
Blue Circles	0.5	115 °	1.2
Purple Triangles	0.7	95 °	2.7



(a)



(b)

Figure 2.12: (a) Simulated CGH40006P GaN HEMT performance for Q factor trade-off at the drain, showing various loads in relation to constant Q-circles on a Smith chart. (b) The corresponding PAE vs. frequency plot for three load Q factors: higher Q loads achieve higher peak PAE but have narrower bandwidth due to increased reactive energy, while lower Q loads offer broader bandwidth at the cost of reduced peak PAE.

It is important to note that the bandwidth of a matching network is limited by the device input and output impedances, and the Q factor at the load side can be included at the start of the design process. To

demonstrate the benefit of adding this as a design parameter, we extend the MoV method to design of a wideband PA. Since our objective is also high PAE, we next consider extending the MoV method to include harmonic terminations that maximize efficiency [39].

2.3.2B Harmonic Terminations

In a PA, the nonlinearity of the device produces harmonic frequency content at both input and output. Waveform engineering refers to control of the harmonic impedances with a goal to, e.g. minimize overlap of voltage and current time-domain waveforms at the intrinsic drain, thereby reducing dissipation and increasing efficiency [63]. To observe the effects of the harmonics on efficiency, first the fundamental frequency source and load reflection coefficients are fixed to values that trade off PAE and P_{out}.

The harmonic termination reflection coefficient phase and amplitude effects on PAE and P_{out} is discussed in detail theoretically in [64]. Ideally, the harmonic impedances are high, so as the initial step, we take two harmonics into account and assume $|\Gamma(2f_0)| = |\Gamma(3f_0)| = 0.95$ although the realistic values are likely to be lower. The phases of both input and output network reflection coefficients at the harmonic frequencies are swept from 0° to 360° to identify phase values that result in high efficiency. Shown in Fig. 2.13 is a simulation of PAE as a function of 2nd harmonic termination phase for the CGH40006P GaN HEMT. At 2.5 GHz, the region between 190° and 300° (trace with orange triangle symbols) results in a drop of 10 to 20 percentage points in efficiency so the range of phases is limited to −50° to 170° to avoid the drop, while maintaining the fundamental impedance that results in high PAE and P_{out}.

In a wideband PA design, a clear "avoidance region" for harmonic impedances is difficult to identify and to avoid overlapping with fundamental frequency impedances. The MoV method can add insight to this problem by obtaining multi-harmonic load-pull data from simulations to help select harmonic terminations. In Fig. 2.13, PAE as a function of 2nd harmonic phase for several additional frequencies is shown from 2–3.5 GHz in 0.25 GHz steps. When the entire frequency range is considered, the high and low efficiency regions overlap and it is difficult to determine the best harmonic phase for a single output network. The grey shaded area from 80° to 140° represents a region $PAE \geq 53$ % across 2–3.5 GHz. This example illustrates why adding harmonic phase to the MoV design method can be beneficial.

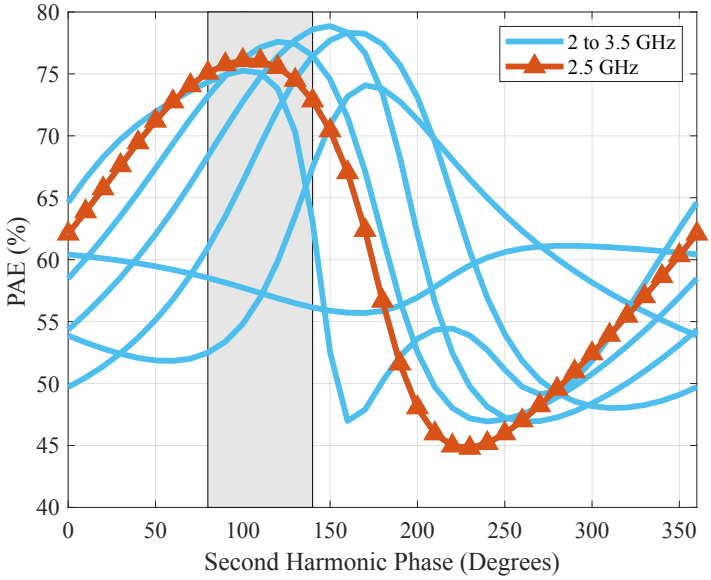


Figure 2.13: Simulated PAE as a function of 2nd harmonic termination phase for the CGH40006P GaN HEMT, assuming a $|\Gamma_L(2f_0)| = 0.95$. P_{in} = 28 dBm, V_{gg} = -2.2 V, V_{dd} = 28 V, $|\Gamma_S| = 0.6$, $\angle\Gamma_S = 210$, $|\Gamma_L| = 0.5$, $\angle\Gamma_L = 130$. The grey shared area from 80° to 140° represents a region of consistently high PAE across 2–3.5 GHz.

2.3.2c Design and Analysis of a 6W Hybrid PA

To verify the use of the Q factor and harmonic terminations using the MoV method, a wideband, high efficiency amplifier is designed. The fundamental-frequency $\Gamma_S(f_0)$ and $\Gamma_L(f_0)$ are selected using one parallel coordinate plot with Q_L as a new column to aid in selection for a wideband application. Q_L is a decision variable that the designer chooses to include to aid in the design trade-off space. For a simpler illustration, Q_S is not included as a column in this case, but is a straightforward addition. Once the desired $\Gamma_S(f_0)$ and $\Gamma_L(f_0)$ are found, they are fixed and a harmonic source and load-pull is simulated.

The Q factor MoV graphical implementation shown in Fig. 2.14 is obtained from load- and source-pull harmonic balance simulations of the CGH4006P HEMT using Cadence Microwave Office (AWR). The computational cost is dominated by the load–pull simulations rather than the visualization procedure itself. For Fig. 2.14, a total 74,880 points were simulated using AWR. The MoV analysis is performed in post–processing and adds negligible computational overhead. The horizontal lines connecting vertical axes contain the data from the simulated source- and load-pull sweeps. We fix $V_{gg} = -2.2$ V, a deep class-AB

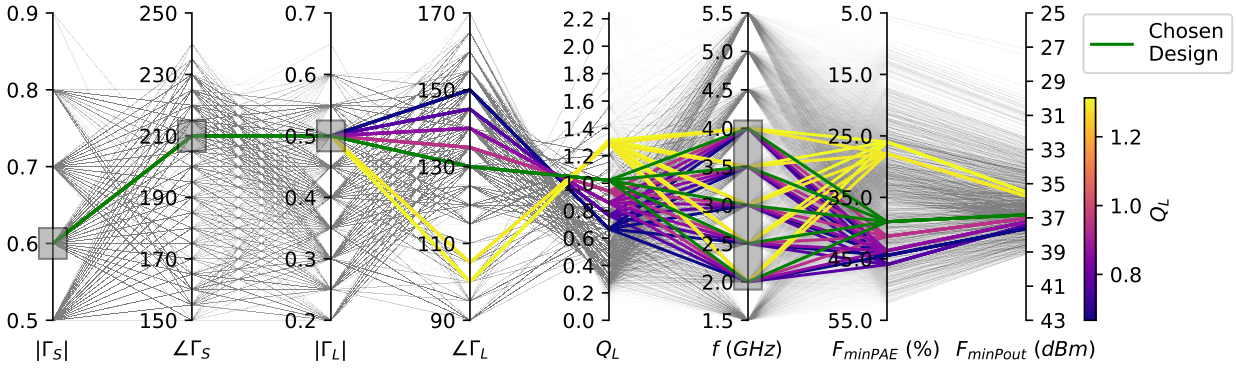


Figure 2.14: Multi-objective visualization plot of the MACOM CGH40006P 6 W GaN PA HEMT load- and source-pull data. Possible solutions are connected to the columns horizontally and solutions filtered by the brushing box are in color. The Q factor of the load, Q_L, is calculated from $|\Gamma_L|, \angle\Gamma_L$ vertical columns and used as an additional metric to aid the design in trade-off selection. The selected design at the frequency range of 2–4 GHz is shown by the unique solution highlighted in green.The frequency column is selected through simulation settings in the design software.

bias, $P_{in} = 28$ dBm (P1dB point), and $V_{dd} = 28$ V. The variable sweep ranges are given in Table 2.3. We then convert $(|\Gamma_L|, \angle\Gamma_L)$ to rectangular form and create a corresponding load Q factor, Q_L from equation (2.6). The simulation data is then imported into a Python script and filtered into columns of states, decisions, and objectives as selected by the user.

Table 2.3: Sweep Variables of Multi-Objective Q Factor Plot

Variables	$\lvert\Gamma_S\rvert$	$\angle\Gamma_S$	$\lvert\Gamma_L\rvert$	$\angle\Gamma_L$	f
Values	0.55–0.85	150–240	0.2–0.65	90–178	1.5–5.5
Steps	0.1	5 °	0.05	8 °	0.5 GHz

This implementation allows a PA designer to interactively select desired ranges within the objective set. Only solutions that are in color pass through the brushed boxes as they have been filtered interactively by the user while the greyed out solutions are not valid for the selected range. A unique design is selected which is a specification of the vector of decision variables from eq. (2.2). From left to right in Fig. 2.14, the 1st through 4th vertical columns represent the simulated reflection coefficients magnitude and angles. The 5th column is the nodal Q_L value calculated from the magnitude and angle of the load reflection coefficient. The 6th vertical column is the state variable, RF bandwidth (f) in GHz. The 7th and 8th columns are the objectives,

(F_{minPAE}) and ($F_{minPout}$), eq. (2.1). In this case, we choose the PAE minimum and maximum values to be relatively close across the bandwidth. The interactive graphical representation in Fig. 2.14 shows the set of non-dominated solutions.

The frequency is swept from 1.5 to 5.5 GHz for an octave-band PA operating from 2 to 4 GHz. We select $|\Gamma_S|$, $\angle\Gamma_S$ $|\Gamma_L|$ based on the visualized ($F_{minPout}$) column for desiring solutions with $P_{out} > 35$ dBm. The remaining selections to be made are the $\angle\Gamma_L$ and Q_L columns in Fig. 2.14. The final selected decision variables are ($|\Gamma_S| = 0.6, \angle\Gamma_S = 210\,^\circ$) and ($|\Gamma_L| = 0.5, \angle\Gamma_L = 130\,^\circ$) which is valid for a $Q_L = 1.0$ across a fundamental frequency of 2–4 GHz. This solution has $PAE_{min} = 37\%$ and $P_{\text{out,min}} = 36.9$ dBm. Note that this Q_L is chosen for a single value of $\Gamma_L = 0.5\angle 130^\circ$ for a first-pass solution. Other solutions are also good options such as $\angle 140^\circ$ or $\angle 150^\circ$. In principle, one could go back and introduce different Q_L values across different Γ_L values over the octave bandwidth.

The load reflection coefficient, columns 3 and 4 from the lefthand side of Fig. 2.14 is shown as a complex value selected from the initial load–pull data and plotted as constant across frequency. This is justified since the chosen Γ_L satisfies the corresponding F_{minPAE} and $F_{minPout}$ criteria over the frequency range of interest. Although Γ_L is frequency dependent in practice, this approximation provides a single starting point for matching network design. No specific matching network topology is assumed and is left to the designer.

The next step in designing a high-efficiency wideband PA is determining the harmonic terminations. Here, the load and source networks are treated separately, though they may also be introduced jointly to capture interactions. Load-side terminations are examined using the MoV plot in Fig. 2.15. The decision variables are the second- and third-harmonic load termination angles, $\angle\Gamma(2f_0)$ and $\angle\Gamma(3f_0)$, swept from 0 to 360°. The state variable is the fundamental frequency from 2 to 4 GHz in 0.5 GHz steps, while the objectives are defined as in eq. (2.3). The decision variables are collected into $\mathbf{x}$ for use in eq. (2.1).

The multi-objective plot represents a trade-off of harmonic phase across frequency for objectives (F_{minPAE}, F_{maxPAE}, F_{PAE}). The 4$^{\text{th}}$ column is "brushed" to set the minimum PAE to be greater than or equal to 58 %. Working backwards to the 1$^{\text{st}}$ column shows the $\angle 2f_0$ is limited to a range of 80–150 °. The 2$^{\text{nd}}$ column, $\angle 3f_0$, is less sensitive and does not have a defined range on the PAE, which aligns with the understanding of packaged devices and the impact the third harmonic may have on efficiency. This plot is

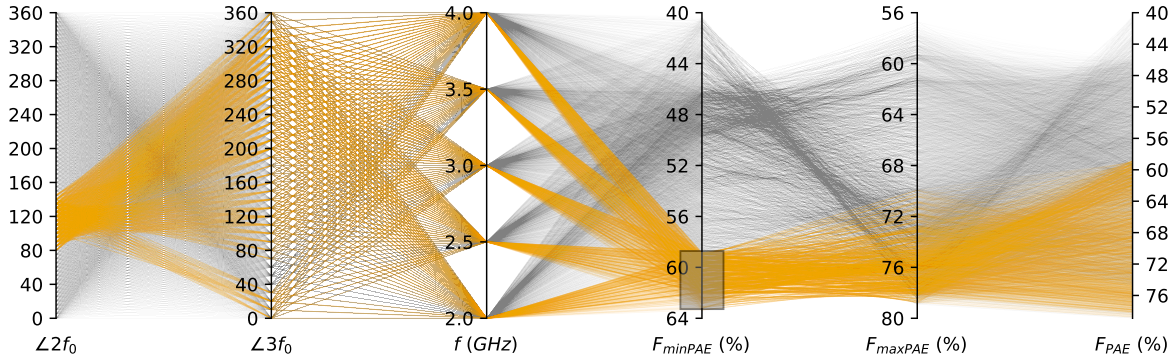


Figure 2.15: Visualization of drain terminal reflection coefficient phases of the second and third harmonics from 2 to 4 GHz swept from 0–360°. The fundamental reflection coefficient at the source and load are fixed, as well as $V_{dd} = 28$ V. The right-most column shows the range of attainable PAE. The minimum and maximum PA are separated as columns to observe subsets of the possible PAE range.

very helpful for its ability to take a lot of data, $\angle 2f_0$ and $\angle 3f_0$ across an octave of bandwidth and quickly enable the designer to identify a target range for the output matching network (OMN) phase required for high PAE across a large bandwidth.

The source-side terminations are swept after fixing the load-side and the resulting MoV plot is shown in Fig. 2.16. The column types are the same as Fig. 2.15. and the 4$^{\text{th}}$ column is "brushed" to set the minimum PAE to be greater than or equal to 58 % again. In the source harmonics case the $\angle 2f_0$ has less of an impact on the minimum PAE across fundamental frequency and the input matching networks have a wider range of termination values ranging from -40 ° to 200 °. This aligns with the understanding of the source side impact on the PAE in a power amplifier.

Now that the harmonic phase range is determined, the PA matching networks are designed to match the chosen fundamental-frequency impedances found from Fig. 2.14. The designer must also carefully control the harmonic phase of the matching networks to be within the desired ranges identified in Fig. 2.15 and Fig. 2.16. The PA matching networks are implemented with stepped-impedance microstrip structures for wideband operation. An RC stability network is added with an 0402 68 Ω resistor and two 0402 3.3 pF capacitors in series with the gate. Additional stability capacitors and resistors are added on the bias lines. The fabricated PA with soldered packaged device is shown in Fig. 2.17.

One of the challenges of this PA design is obtaining $|\Gamma_L(2f_0)|$, $|\Gamma_L(3f_0)|$, $|\Gamma_S(2f_0)|$, and $|\Gamma_S(3f_0)| = 0.95$

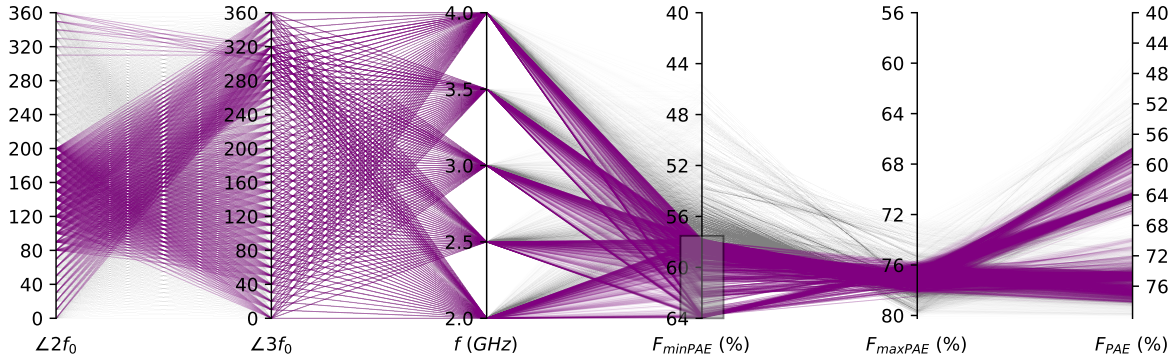


Figure 2.16: Visualization of gate terminal reflection coefficient phases of the second and third harmonics from 2 to 4 GHz swept from 0–360°. The fundamental reflection coefficient at the source and load are fixed, as well as V_{dd} = 28 V and the load harmonic impedances obtained from Fig. 2.15. The right-most column shows the range of attainable PAE. The minimum and maximum PAE values are separated as columns to observe subsets of the possible PAE range.

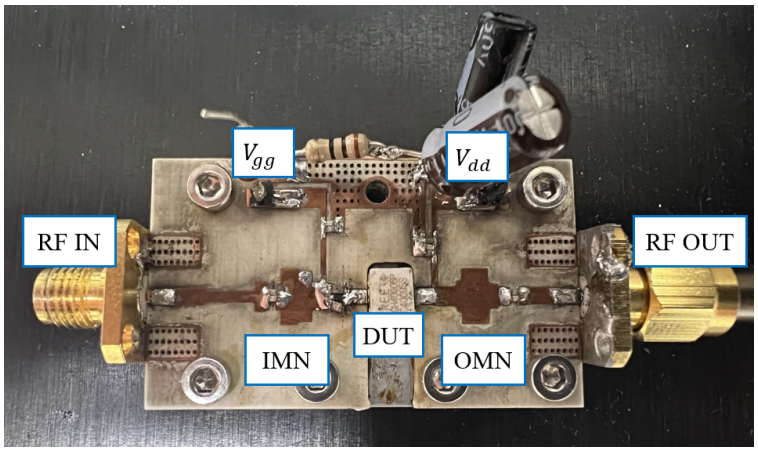


Figure 2.17: Image of the hybrid PA designed in Cadence AWR on a RO4350B substrate and uses a Macom CGH40006P 6W packaged HEMT device under test (DUT). PA input (IMN) and output matching networks (OMN) are designed with a low Q_L reflection coefficient as well as to terminate the second and third harmonics in optimal regions for improved efficiency across a wide bandwidth.

across an octave of BW. A trade-off is required in how well the harmonics are terminated and the quality of the matching networks at f_0. The simulated stepped impedance matching networks fundamental, 2nd, and 3rd harmonic phases are shown on a Smith chart in Fig. 2.18. The IMN curves are shown without symbols and the OMN are shown with symbols. The fundamental network is shown in green, the second harmonic in blue, and the third harmonic in red.

For the IMN curves, the 2nd harmonic termination varies from $0.44\angle 163°$ at 4 GHz to $0.63\angle 25°$ at 8 GHz.

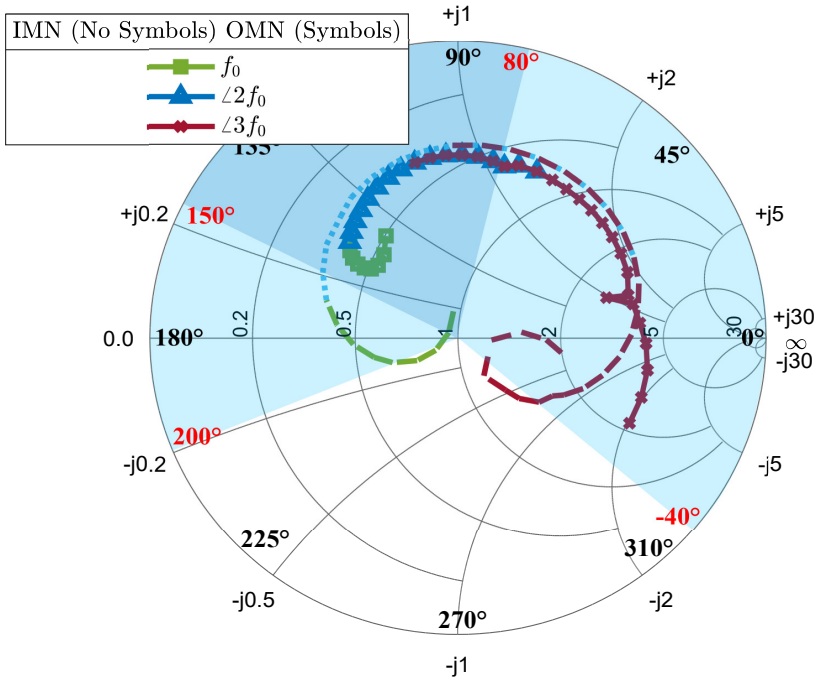


Figure 2.18: Simulated reflection coefficient phase of the stepped impedance microstrip input (IMN) and output (OMN) matching networks for the fundamental f_0 (green), second harmonic $2f_0$ (blue), and third harmonic $3f_0$ (red). IMN curves are shown without symbols, OMN curves with symbols. The second harmonic magnitude for IMN and OMN ranges from 0.44 to 0.63, different from the 0.95 termination used in simulations. Darker blue shaded arc indicates the OMN target phase range of 80°–150°, while lighter blue shading indicates the IMN target range of −40° to 200°.

The OMN 2nd harmonic termination varies from $0.48\angle 137°$ at 4 GHz to $0.61\angle 65°$ at 8 GHz. The OMN fails to achieve the desired 2nd harmonic termination range from 7.25 GHz to 8 GHz, affecting the fundamental match from 3.62 GHz to 4 GHz. Otherwise, the IMN remains within the target range of -40 ° to 200 ° Neither termination meets the ideal reflection magnitude of 0.95 with the lower magnitude around 4 GHz. Changing the $|\Gamma_L(2f_0)|$, $|\Gamma_L(3f_0)|$ from 0.95 to 0.65 lowers the maximum possible PAE to 71 % compared to 80 % originally in simulation. Fixing the same $|\Gamma_L(2f_0)|$, $|\Gamma_L(3f_0)|$ termination values from Fig. 2.15 lowers the minimum possible PAE from 2–4 GHz to 54 % compared to 58 %.

The next question to ask is how much the performance of the PA degrades from less than ideal harmonic terminations. Fig. 2.19. shows a plot of the simulated PAE variations considered during the different stages of this design. The "No Harm Term" curve represents the performance of the ideal PA without any harmonic terminations. The source and load reflection coefficients are the same as those found from Fig. 2.14. and

the second and third harmonic magnitudes and angles are left at 0. This curve represents what is obtainable without terminating the harmonics and using ideal load and source tuners with no stability network or bias lines. The "Harm Term = |0.95|" curve represents a PA with ideal maximum termination magnitudes and optimized angles from Fig. 2.15. and Fig. 2.16.

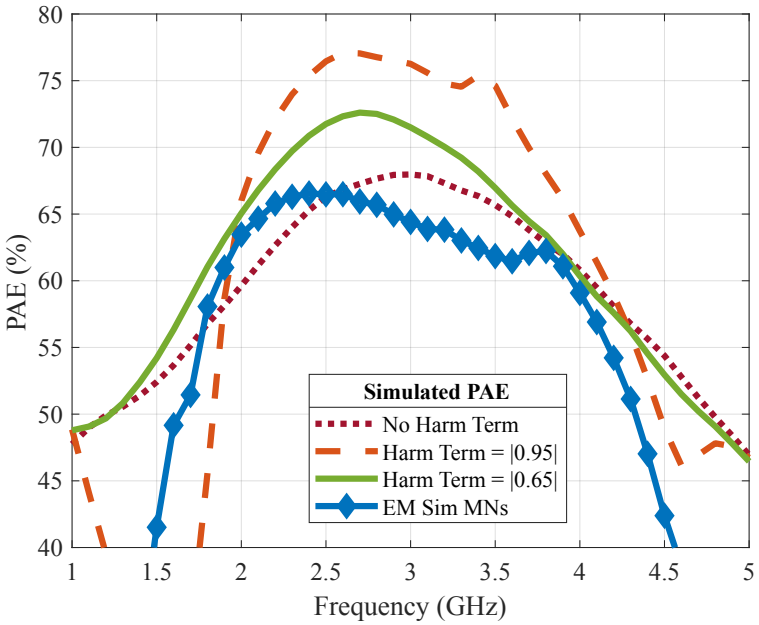


Figure 2.19: Plot of simulated PAE variations during different design points. The "No Harm Term" curve represents the performance of the ideal PA without any harmonic terminations. The "Harm Term = |0.95|" curve represents the ideal PA with said harmonic termination magnitude and the "Harm Term = |0.65|" curve represents the ideal PA with |0.65| harmonic termination magnitude. The "EM Sim MNs" curve with solid lines and diamond markers is the entire PA with full wave EM simulated matching networks, stability network, and surface mount component models.

This is the highest possible PAE performance since the tuners used for matching are perfect and are not limited in bandwidth. The "Harm Term = |0.65|" curve represents the ideal PA with an adjusted harmonic termination magnitude of |0.65| and optimized angles. This idealized simulation does not include loss of real microstrip networks or any stability considerations, it is simply observing the performance possible through more realistic harmonic termination magnitudes for this BW. The last curve, "'EM Sim MNs", with solid lines and diamond markers is the entire PA with full wave EM simulated matching networks whose phase is seen in Fig. 2.18, stability network, and surface mount component models. This is the final simulation with matching networks designed to match as well as possible to the fundamental frequency and tuning the

harmonic phase to match with the desired regions identified from the parallel plots. This performance is expected to be the lowest compared to the ideal PA circuits, but maintains reasonable performance across an octave of bandwidth for a stable, realized PA. The realized PA simulation curve predicts PAE greater than 60% across at least an octave of bandwidth.

The impact of reducing harmonic termination magnitude from an optimal |0.95| to a practical |0.65| must be considered. This reduction lowers achievable PAE, as seen in Fig. 2.19., where the ideal tuner case (orange, |0.95|) outperforms the practical realization (green, |0.65|). However, PAE still improves compared to the no harmonic termination (red). In terms of MoV plot simulation creation time, there is no difference between running a sweep with termination magnitude set at |0.95| or |0.65|.

The resulting large signal simulation (dotted) vs. measurement (solid) data is shown in Fig. 2.20. at an input power of 28.5 dBm and $V_{dd} = 23$ V. The measured output power and large signal gain matches very well with the simulation data, the PAE is not as closely matched, indicating additional dissipated dc power consumption is used than the models predict. Additionally we see a sharp drop in PAE around 3.6 GHz as the second harmonic termination is not in the desired range as predicted by Fig. 2.18. The measured PA does maintain near 50 % PAE across almost an octave of BW (61.8 %) from 1.9–3.6 GHz with a peak efficiency of 58 % at 2.5 GHz. Table 2.4 presents amplifiers using the same packaged device as the one in this work.

Table 2.4: PAs in Literature Using the CGH40006P GaN HEMT

Ref	f (GHz)	FBW (%)	G_{LS} (dB)	PAE (%)	P_{out} (dBm)
[65]	1.9–2.5	29.0	13–19	44–65	36.5
[66]	3.0–4.0	28.6	7.7–8.9	52–62	37.7–38.9
[67]	3.0–4.6	40.0	6.6–8.3	51.3–62.6	38.6–40.2
This work	**1.9–3.6**	**61.8**	**8.6–10.4**	**46–58**	**37.9–38.9**

When compared to other works in literature using the same device, the PA presented here demonstrates the widest fractional bandwidth (FBW) and has very comparable PAE. The minimum and maximum PAE from this work differ by only about 4 to 5% compared to works with about 20 to 30 % lower FBW [66], [67].

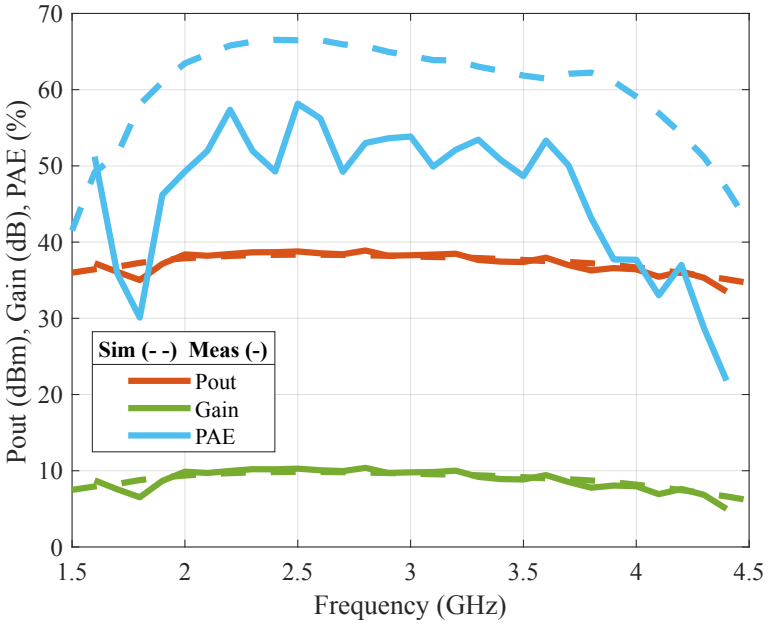


Figure 2.20: Simulated (dotted) and measured (solid) large-signal performance of the hybrid PA. The design is initialized using the load-impedance Q factor. Measurements are taken at 28.5 dBm input power with V_{dd} = 23 V and a quiescent current of 208 mA.

2.4 Conclusion and Discussion

In summary, this Chapter describes a multi-objective analysis technique for microwave power amplifiers that does not require any weighting of the vector of objectives, but quickly provides solutions that capture different compromises and provides intuition to the designer. The *Load-Pull Extraction* method is applied during early stages of a PA design to remove iterative techniques of load– and source– pull analysis and quickly arrive at a design starting point. The contents of this Chapter are reported in two conference publications [68, 69] and a journal paper [70]. As an example of an extension of the method, the Q factor of the load impedance presented to a PA is included as a decision column to aid in trade-off selection. Another extension that can aid designers in identifying optimum regions of harmonic impedance phase is included for improving PAE. To validate the techniques, a hybrid GaN 6 W wideband PA is designed, measured, and fabricated. Compared to literature using the same device, the PA shows a large fractional bandwidth (61.8 %) from 1.9–3.6 GHz and measured PAE within 4–5 % of other works that had (20 to 30) % lower fractional bandwidth. A peak

PAE of 58 %, large signal gain of 10.4 dB, and P_{out} of 38.9 dBm (7.7 W) is measured at 2.5 GHz. The PAE discrepancy between simulation and measurement, common in most PA papers with this kind of bandwidth, is most likey due to change in dc current draw compared to the nonlinear model, as well as measurement and packaging limitations.

Additional methods that can easily implemented in the MoV LPE method that use already existing load/source-pull data. For example, the source reflection coefficient Q factor ($Q_S = |X_S|/R_S$) can also be taken into account when determining the input target matching impedance. Additionally, the harmonic phase search can include other objectives, such as large-signal gain. It would be useful to test this design methodology on a bare die or MMIC PA where the harmonic terminations are not limited by the package effects.

Obvious extensions are to include the fundamental, second, and third harmonic source– and load–pull data simultaneously, as the resulting data set can be analyzed with the MoV method and narrowed down to optimal ranges for harmonics that match well with a fundamental impedance selection. Including trade-off analysis of transistor sizes available in a semiconductor process and extended passive component parameter sensitivity analysis is beneficial for MMIC design.

Furthermore, the MoV method is not intended to replace established broadband PA design techniques such as distributed amplifiers or LMBAs nor mode based techniques relying on linear or nonlinear embedding. Instead, the goal is to serve as a complementary analysis tool to visualize trade offs, assess impedance robustness, and provide insight into device operation at the current source reference planes across frequency and various operating conditions.

In summary, the MoV method is useful for managing high dimensional data sets with conflicting objectives that require trade-off selection, while building designer intuition and arriving at a target design specification in a time efficient manner. Although the degree of time savings is difficult to quantify given variations in individual design practices, the ability to view data and rapidly filter viable solutions provides clear advantages to the designer.

Chapter 3

Selective Trade-Off Method

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3.1 Introduction

This Chapter builds on the Multi-Objective Visualization method introduced in Chapter 2, which focused on the general background and two case study examples of the *Load-Pull Extraction* method (LPE). This chapter introduces an additional approach, referred to as the *Selective Trade-Off* (STO) method which enables designers to examine targeted trade-offs at various stages of a PA design. Its versatility makes it suitable for a wide range of design topics, such as analyzing component sensitivity due to process variation or simulating complex multistage load- and source-pull scenarios involving multiple transistors.

In contrast to the LPE method, which is intended primarily for early stage design, the STO method can

be applied throughout the design process, ranging from early explorations using ideal tuners to later stages involving 2.5D electromagnetic simulations of matching networks. This chapter explores the STO method and applies it to several problems such as component sensitivity analysis and multi-stage MMIC amplifier designs.

3.2 Selective Trade-off Method

As introduced in Chapter 2, the core concept of the MoV method is to organize large high dimensional datasets and enable designer insight through interactive visualization. While the LPE method relies on load- and source pull- .mdf files, the STO method operates on tabulated .txt data files generated by the designer. Although the STO method is currently validated using Cadence Microwave Office, it is not simulator specific and can be extended to other tools such as Keysight's ADS.

The STO method is intended for problems involving trade offs among multiple competing objectives in complex multivariate design spaces. The method processes raw tabulated data and requires the designer to define the decisions, states, and objectives relevant to the problem. This differs from the LPE method primarily in the flexibility of the variable definitions. In load-pull analysis, the decision variables are typically limited to the source and load reflection coefficients. In contrast, the STO method allows the decision variables to be chosen according to the design problem, such as component values, bias conditions, or geometric parameters.

As demonstrated later in this chapter, component value variation can be treated as the decision variable, while performance metrics such as PAE and P_{out} serve as the objectives across multiple operating states. Once defined, the STO framework filters and organizes the data and maps the multivariate relationships into parallel coordinate plots for visualization and analysis.

3.3 Case Study: X-band MMIC

In this section, the STO method is demonstrated through a sensitivity analysis of GaN process fabrication stackup. The analysis is performed after completion of the power amplifier design and highlights the

applicability of the STO method at an arbitrary stage of the PA design process.

3.3.1 PA Design

A similar design procedure to the power amplifier designs presented in Chapter 2 is followed. First, a MMIC fabrication process is selected. In this case the WIN Semiconductor NP15-00 150 nm gate length GaN-on-SiC process which uses a 100 mm SiC substrate. The process is capable of 28 V operation with a peak f_t of 34.5 GHz and power density of 4 W/mm at 29 GHz. Circuit design is performed in Cadence Microwave Office (AWR) using a nonlinear Angelov model for high-electron mobility transistors (HEMTs). The process offers two interconnect metal layers, high reliability metal-insulator-metal (MIM) capacitors and tantalum nitride (TaN) resistors for MMIC designs. Design specifications, are summarized in Table 3.1. P_{3dB} denotes the input power level at which gain has dropped 3 dB from the small-signal value.

Table 3.1: X–band MMIC Power Amplifier Design Specifications

Specification	Value	Unit
Frequency Range	8—14	GHz
Input Return Loss	≥ 10	dB
Small-Signal Gain	≥ 15	dB
P_{out} at P_{3dB}	≥ 38	dBm
PAE at P_{3dB}	≥ 40	%
Large-Signal Gain at P_{3dB}	≥ 15	dB
Die Size (W×H)	3×2	mm^2
Second Stage Supply Voltage Range	+10 to +28	V
HEMT Drain Current Density	100–150	mA/mm

The initial power amplifier design is performed using the LPE method presented in Chapter 2. A MoV graphical implementation, illustrated in Fig. 3.1, consists of parallel axes with values obtained from load-pull and source-pull harmonic balance simulations of a 8x100 μm HEMT in the WIN Semiconductors NP15-00 GaN-on-SiC process using Cadence Microwave Office. The lines connecting the parallel axes contain information from source and load contours that are connected with performance metrics for a minimum/maximum PAE, maximum/minimum P_{out}, with frequency varying from 8–12 GHz in 500 MHz steps, and V_{dd} varying from 14–26 V in 4 V steps. All the connecting lines are allowed solutions.

In Fig. 3.1, the 1st through 4th vertical columns are the range of the desired reflection coefficients limited by practical constraints. The 5th through 8th columns are the performance objectives that we are trying to make the best trade-off between. The state variables V_{dd} and frequency, expressed as fractional bandwidth, are embedded within the solution set shown in Fig. 3.1 but are omitted as explicit columns for clarity. The columns shown represent the non-dominated set of solutions. The selected solution, highlighted in red gives a PAE variation of 50–62%, and P_{out} from 32–36.6 dBm across the specified bandwidth and drain voltage range. The corresponding reflection coefficients are ($|\Gamma_S| = 0.3, \angle\Gamma_S = 180°$ and ($|\Gamma_L| = 0.6, \angle\Gamma_L = 105°$).

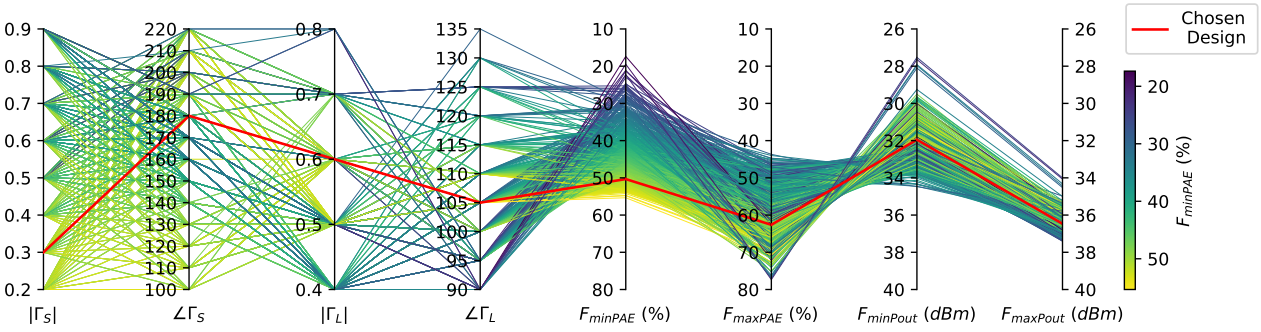


Figure 3.1: MoV showing the selected design from a set of non-dominated solutions, based on simulated load and source pull of a 8x100μm device. The performance is examined over the entire (8–14 GHz) and V_{dd} supply voltage (16–28 V) range.

The selected solution from Fig. 3.1 provides the starting point for the PA design. Once the target Γ's are determined, equivalent parallel RC networks are calculated to model load and source reflection coefficients. Then, ideal lumped elements are used to transform the parallel RC into a 50 Ω output load. This design flow is similar to that seen in [4] with ideal elements being switched out for more realistic microstrip and then finally solved with AWR's method of moments 2.5D Axiem electromagnetic solver. Based on desired gain and output power targets the PA uses two $8 \times 100\mu$m HEMTs that are reactively combined in the output stage, with a driver amplifier implemented using the same device size. The interstage matching network and the output matching network following the combiner each use two shunt capacitors connected to ground through vias, with a total capacitance of 0.22 pF. Figure 3.2 shows the final layout of the two-stage PA design. The figure shows a labeled layout with some of the key layers in color. The overall chip dimensions are 3 mm in x direction by 2 mm in the y direction. The next section presents the experimental results.

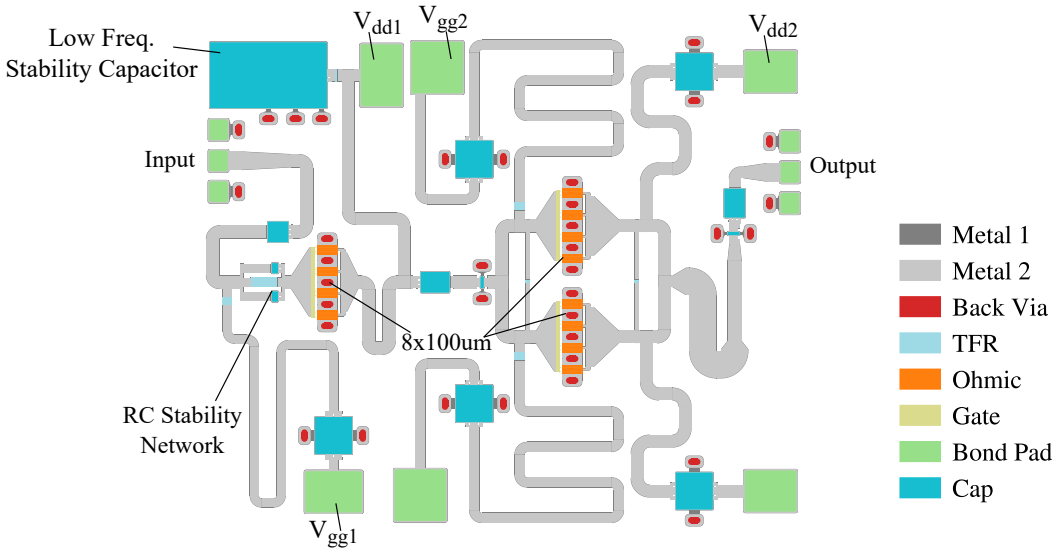


Figure 3.2: "Exploded" layout of the final PA design with some stability networks, transistors ($8 \times 100\,\mu$m HEMTs), and MMIC process layers labeled for clarity.

3.3.2 Experimental Results

This section presents the experimental results of the GaN MMIC power amplifier. The MMIC is die attached to a CuMo carrier to improve heat dissipation and to provide a mechanically robust platform for handling the chip. Additional 100 pF and 1000 pF capacitors are mounted on the CuMo carrier to enhance low frequency stability.

For small-signal characterization the PA is probed on-wafer using a probe station equipped with $150\mu m$ ground-signal-ground (GSG) probes, while the dc bias is supplied through tungsten tip probes. A 0.1–50 GHz VNA is used for small-signal measurements, although the measurement was limited to 14 GHz at the time of characterization of the chip. An image of the on-wafer probing setup is shown in Fig. 3.3 (left) and the view through the corresponding microscope lens (right).

The small-signal simulation results (dashed) vs. measured data (solid) is shown in Fig. 3.4. Although the measurements are limited to 14 GHz, they cover the majority of the operating band and show good agreement with simulation. There is slight under-estimation in $|S_{21}|$ from 13 to 14 GHz in simulation which is attributed to model inaccuracies as this process was still under development at time of design. Also of note is the poor $|S_{11}|$ which is due to intentionally designing the PA input matching network to maximize output power and

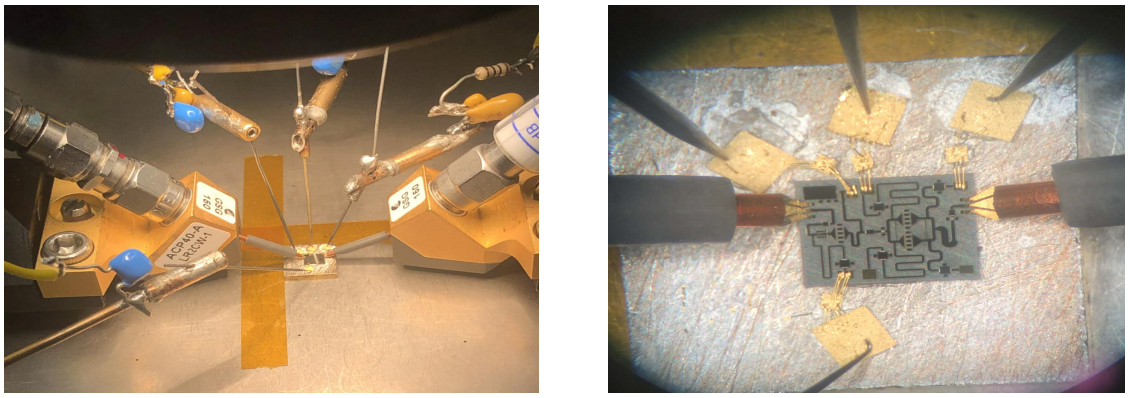


Figure 3.3: Images of on-wafer probing of MMIC PA for small- and large- signal measurements. Image on the left shows a side view of the 150μm GSG probes touching down on the chip with tungsten tip dc probes next to them. The right shows the view in the microscope of the PA attached to a CuMo carrier with all probes making contact to the single layer capacitors.

PAE in the final PA stage. Addition constraints included the drain voltage variation intended for supply modulation that impacted matching network design decisions. In addition, $|S_{22}|$ is around -10 dB matched and also aligns well with simulation.

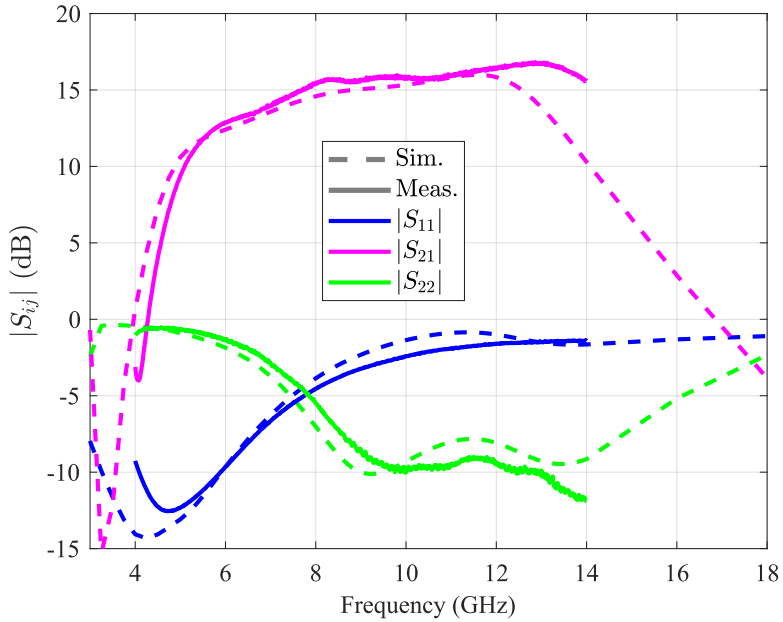


Figure 3.4: Small-signal PA simulations vs. measurements, limited to 14 GHz due to input couplers and use of a large-signal VNA for phase information capture. PA shows reasonable agreement for data captured and slight overestimation of $|S_{21}|$ from 13 to 14 GHz.

Large-signal vector measurements were performed using the same VNA as for the small signal measure-

ments with additional equipment used to safely control the output power delivered at the power meters and accurately record the input power delivered to the DUT. The VNA also enables enables phase information to be captured. A plot of the large-signal simulations (dotted) vs. measurements (solid) is shown in Fig. 3.5 from 8 to 14 GHz with drain voltage at 20 V and input power at 26 dBm.

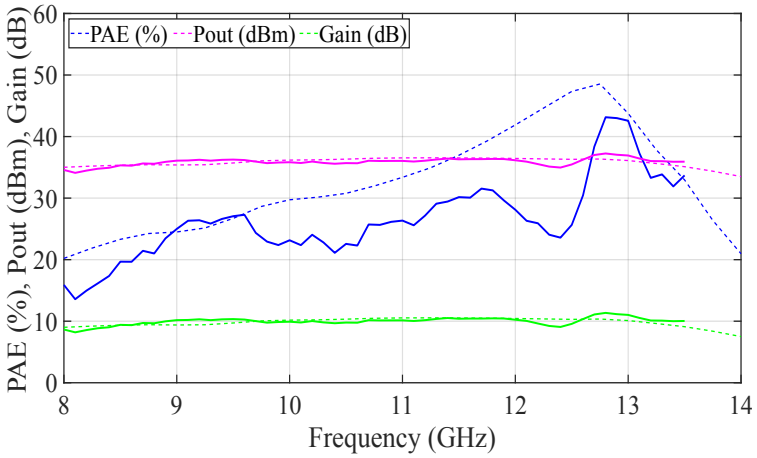


Figure 3.5: Large-signal PA simulations (dotted) versus measurements (solid), from 8 to 14 GHz.

The large-signal measurements show good agreement with simulation for the power gain and the P_{out} across frequency. The measured PAE follows the general shape of the simulation, but is noticeably different. This discrepancy may be attributed to several factors, such as model inaccuracies in predicting the dc power consumption, limitations of measurement equipment to accurately capture dc bias under large signal operation, or process variation. Investigation of these effects is the focus of the following section, which demonstrates an application of the STO method.

3.3.3 Sensitivity Analysis

As outlined, the PAE simulation vs. measurement discrepancy motivates additional analysis. One element of note in the PA design, is the small shunt capacitors used in the interstage and output matching networks. These components are outlined in red boxes in the MMIC photograph shown in Fig. 3.6.

Both capacitors are 0.22 pF at 11 GHz and formed by stacking two metal layers (metal 1 and 2) that are separated by a silicon nitride (SiN) dielectric layer in between them. The lower metal layer, metal 1 is

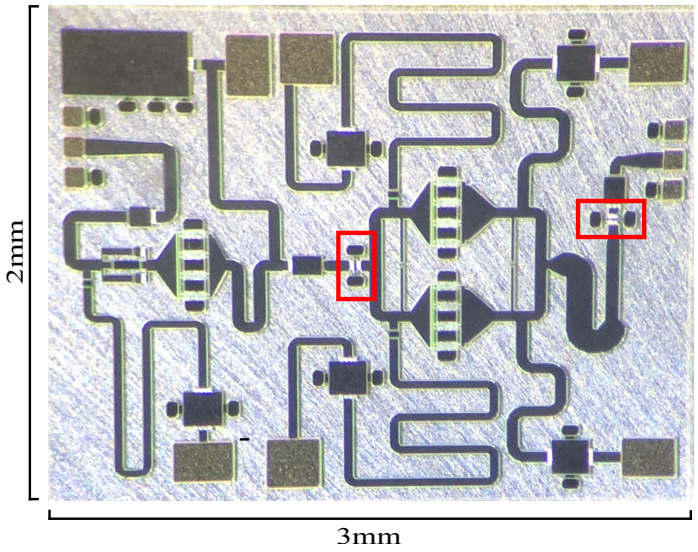


Figure 3.6: Image of MMIC PA with small shunt capacitors used in matching networks outlined in red boxes in the interstage and output matching network.

connected to the via layer which provides a ground connection through the silicon carbide (SiC) substrate to the backside metallization. The upper metal layer, metal 2, is connected on both sides through an airbridge layer and interfaces with the microstrip transmission lines at the input and output. This configuration enables the implementation of a shunt capacitor in circuit form while allowing it to be placed inline with the microstrip transmission line, giving the appearance of a series element. This saves design space and allows for functionality.

A deconstructed view of the shunt capacitor structure is shown in Fig. 3.7. The top portion of the figure illustrates a side view of the three dimensional stackup, while the bottom portion shows a top down view of the metal layers. The image labeled "Full EM" in the lower right illustrates the complete layout of the shunt capacitor element used in the design.

Variations in the silicon nitride deposition thickness during fabrication can lead to deviations in the effective capacitance value, potentially shifting the matching network away from the intended operating point. An example is illustrated in Fig. 3.8 with an LC lumped-element matching network that matches the R_pC_p equivalent output impedance of a GaN HEMT to 50 Ω at the design frequency. Starting from the load (point A on the Smith chart in Fig. 3.8), a bias inductor L_b cancels the shunt capacitance of the transistor and brings the impedance to point B. Matching inductor L_1, capacitor C_1 and inductor L_2 perform further

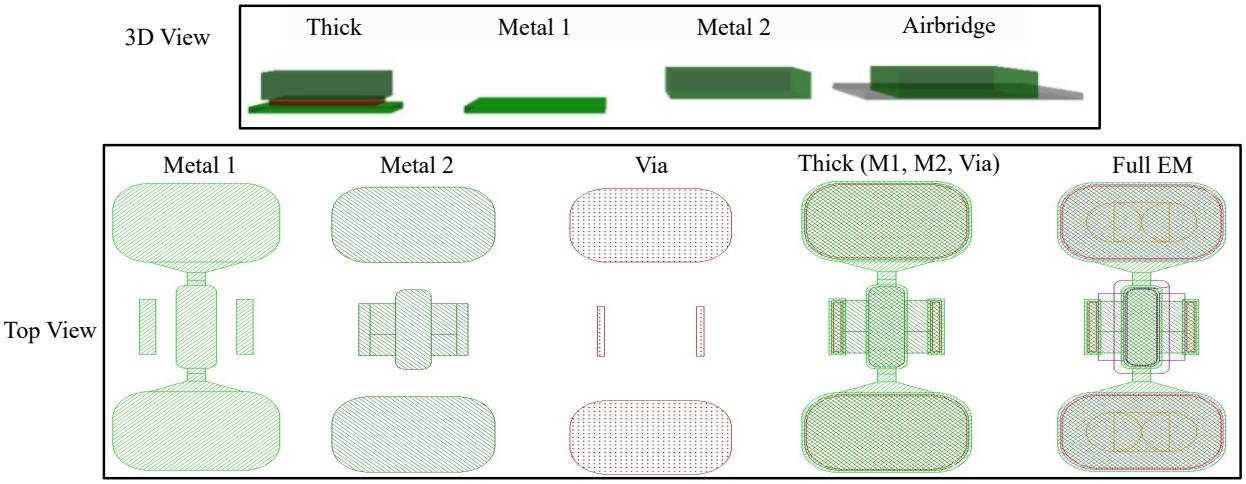


Figure 3.7: (Top) Deconstructed side 3-dimensional view of the metal layers in the process. (Bottom) top down view of the layers with final shunt matching capacitor on the far right side.

matching to points C, D and E, respectively. Finally, capacitor C_2 brings the impedance to 50 Ω. If this capacitor value varies due to the process, the match will shift to different frequencies. Performing a design sensitivity analysis w.r.t. capacitance C_2 allows a more realistic performance prediction.

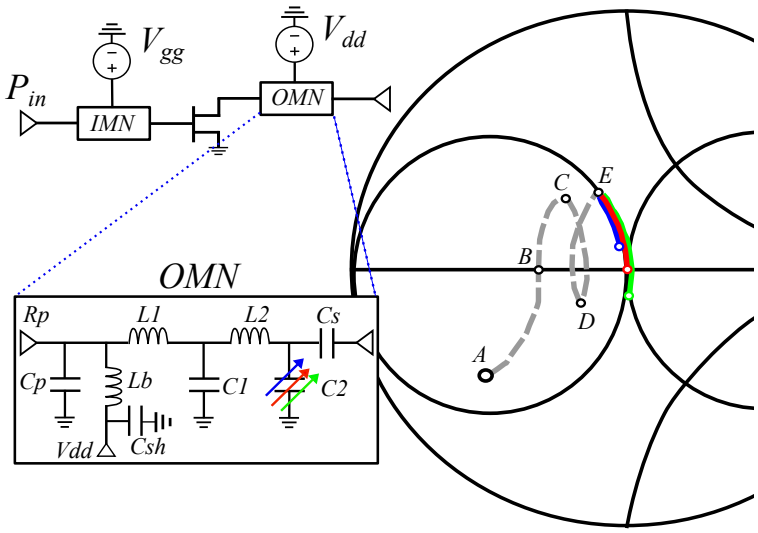


Figure 3.8: Graphic of impedances after the addition of lumped element matching network elements in the PA output matching network. The optimal load impedance of the PA is modeled as the R_pC_p network, shown with point A on the Smith chart [4]. After adding the bias inductor, the impedance moves to point B, and the Tee network $L_1 - C_1 - L_2$ moves it to point E. The shunt capacitor C_2 is designed to match the load, but the variation in its value can result in a mismatch at a given frequency.

The SiN layer used in between the shunt capacitor metal layers is called SiN layer 4, a stackup from the

PDK is shown in Fig. 3.9. Per the manufacturer data this layer is typically $0.305\mu m \pm 0.03\mu m$, so 1 10 percent variation is typically possible.

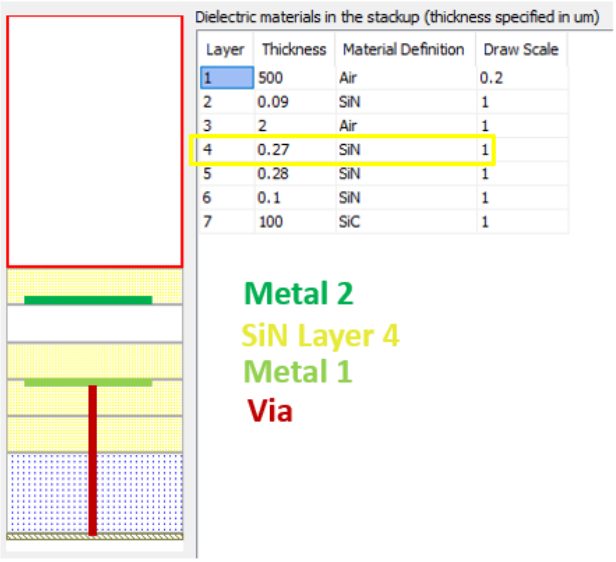


Figure 3.9: AWR EM stackup of the dielectric layers in the NP15-00 GaN process. The metal layers used in the shunt capacitor, Metal 1 and 2, along with the via to ground are also outlined as to their location in reference to the SiN layer. An air gap is created beneath Metal 2 during air bridge formation by removing a sacrificial layer, typically a photoresist or similar temporary material.

To estimate the design sensitivity using the STO method we simulate the sample output matching network first demonstrated in Fig. 3.8. We then vary the shunt matching capacitor values by $\pm 10\,\mu$m to estimate what a 20% change in capacitance value would do to our output performance in terms of PAE and P_{out}. This is equivalent to varying the SiN dielectric thickness by 20%, higher than the manufacturer's expected value but provides extra margin to demonstrate the method. The frequency is also swept from 8–14 GHz, P_{in} from 26–32 dBm, and V_{dd} from 16–28 V. This data set is simulated in AWR in a schematic and then a tabular PAE and P_{out} file are created and then exported through the GUI as a .txt file. The MoV Python code filters the data and then the swept variables are sorted. The representative parallel plot is shown in Figure. 3.10.

The columns, starting from the left, are the frequency of operation, drain voltage, input power, shunt matching capacitors (SMC), and then PAE and P_{out}, with addition label "sensitivity" just for visual. These metrics indicate how much the performance can shift depending on the selected variables V_{dd}, P_{in}, and the capacitance shift. The small red arrows show the performance variability from the ideal selected solution

across frequency and drain voltage from Fig. 3.1.

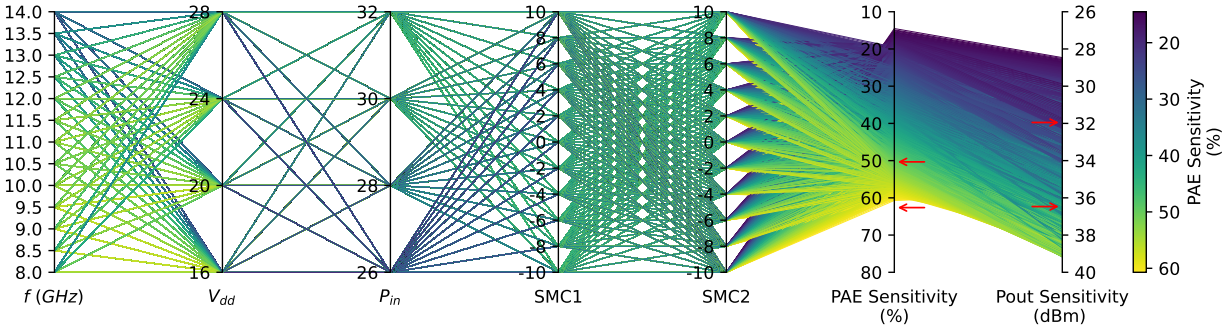


Figure 3.10: Visualization of the sensitivity of the chosen design with ±20% variation of the shunt matching capacitors (SMC). Arrows reflect the performance observed during the initial design optimization.

Fig. 3.10 shows that adding in the variance of the shunt matching capacitance, P_{in}, and V_{dd} can cause the PAE to range from 16–61% and the P_{out} from 28.2–39.1 dBm. The measured data from Fig. 3.5 shows an even further frequency shift that was not predicted by the simulations or the design sensitivity analysis. It is clear that the shunt capacitance variation is not the sole cause of the shift. Additional causes of disagreement include measurement errors, e.g. the GSG probes being slightly damaged and presenting parasitic reactances [71]. Some transistor specifications that often vary across a wafer are not considered here, but could also explain the frequency shift. For example, g_m, C_{gs}, and C_{gd} can vary by up to ±30% and can also cause additional performance shifts [24].

The final large signal PAE vs frequency plot with the +10% and -10% SiN values is shown in Fig. 3.11. This plot visualize the impact of the SiN on the PA performance and its impact on the PAE in particular. As noted, there is not significant difference and it does not seem to count for the entire PAE difference.

This section, examines the X-band MMIC PA design and analyzes the sensitivity of some of the matching components used. This was done with the STO method that processes a AWR simulation file and generated .txt data to create a parallel coordinate plot that displays the variance of the solution and gives a sensitivity idea to the designer. The designer can use this to fix certain variance and see the effect it has on performance in real time. In this case, the suspected SiN variance did not account for PAE difference, but did lead to a useful analysis of the design and demonstration of how component sensitivity can be analyzed with MoV in the future.

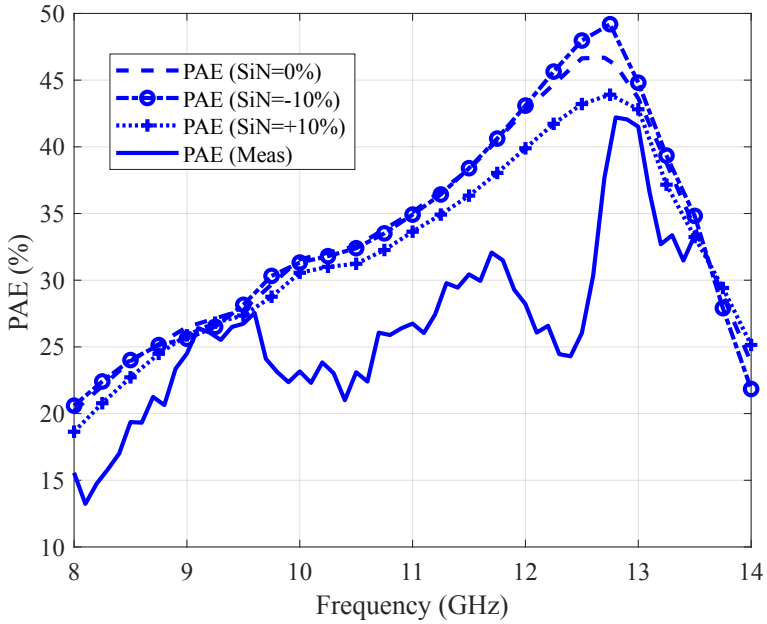


Figure 3.11: Simulated (dotted) and measured (solid) PAE when the shunt matching capacitor (SMC) values are varied by 20% at $V_{\text{dd}} = 22\,\text{V}$ and $P_{\text{in}} = 26\,\text{dBm}$.

3.3.4 Supply Modulation

One of the original specifications of the MMIC design from Table 3.1 is to design the second stage V_{dd} to cover +10 V to +28 V for use in a supply modulation setup. Supply modulation, or envelope tracking, is a microwave PA efficiency enhancement method where the drain voltage of the PA is dynamically varied according to the input signal envelope [72]. Two main challenges in this technique are: (1) design of a stable PA with a drain bias line that can support a broadband signal and has high efficiency at lower supply voltages; and (2) design of a dynamic supply (supply modulator) that can produce a range of voltages with a high slew rate with high efficiency [73]. Careful creation of shaping functions (SF) to optimize drain voltage is also important to maintain PA linearity and efficiency. The power amplifier must be designed to be stable at all load and bias conditions and have minimal stabilization capacitance on the drain bias lines to allow for rapid voltage switching [74]. The integration of the supply modulator and PA requires low inductance interconnects to minimize loading and to act as a low-pass filter [75]. Continuous supply modulators such as buck converters have been used extensively but their efficiency drops for high-bandwidth

signals [72]. Discrete supply modulation, which switches between dc voltage levels, demonstrated tracking high bandwidth signals by minimizing the number of switching instances to maintain high efficiency, with switching in the 100-MHz range [76, 77].

The discrete supply modulator (DSM) architecture used in this work is a multi-level converter with transistor switches that apply the different externally generated dc voltage levels at the output, V_{out}. The circuit is shown in the top right corner of Fig. 3.12 which shows a high-level block diagram of the supply modulation bench used in this work. It consists of an arbitrary waveform generator (AWG) that creates the baseband 34 MHz and 67 MHz 64-QAM signals fed into the vector signal generator (VSG) and bit pattern generator (BPG). An additional driver board is used to collect the IQ data from the BPG and drive the DSM. Various DC bias supplies are used to bias the DSM and PA which is connected to the DSM with a 3D printed mounting fixture. At the output of the PA, a spectrum analyzer measures the IQ data and linearity. Nonlinearities of the instrumentation are removed by a simple linearization of the input signal. A shaping function is created from the measured CW PAE, P_{out}, and gain of the PA to optimize the performance for the desired metric, which could be flat gain, maximal PAE in backoff, etc. [78].

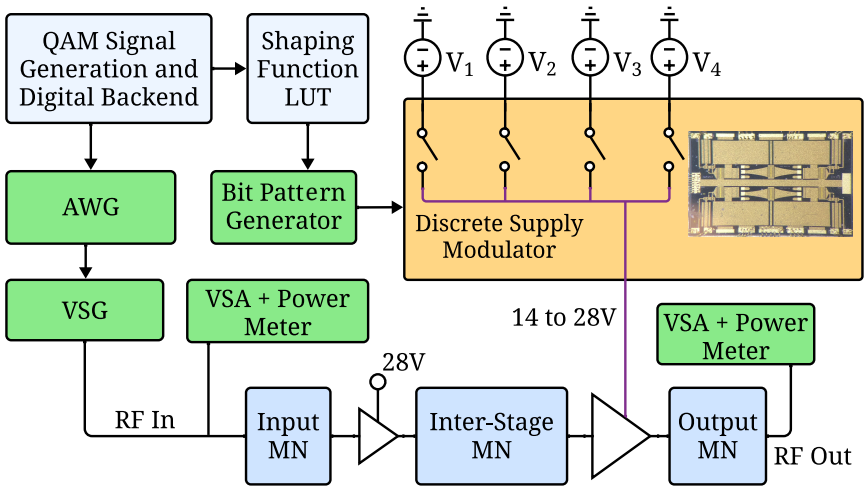


Figure 3.12: High-level block diagram of the supply modulation (envelope tracking) measurement setup used in this work.

This subsection describes the supply modulation of the previously discussed 8–14 GHz PA with a GaN MMIC multilevel supply modulator. The design description of the drain supply modulator is covered in

Paul Flaten's thesis titled "Advanced Design Approaches to High Performance Transmitter Components." A brief description of the supply modulated power amplifier characterization setup is given next, followed by the characterization of a transmitter with the two MMICs, using signals with a PAPR = 6 dB for 34 MHz and 67 MHz bandwidth 64-QAM modulated signals.

The static measured PAE and Gain vs. P_{out} curves at 12.8 GHz are shown in Fig. 3.13. The efficiency is above 40% for a 4 dB backoff, and above 35% for 6 dB backoff. The performance across frequency at V_{dd} = 20 V and input power P_{in} = 26 dBm is shown in Fig. 3.5, showing a flat output power and Gain across the frequency range.

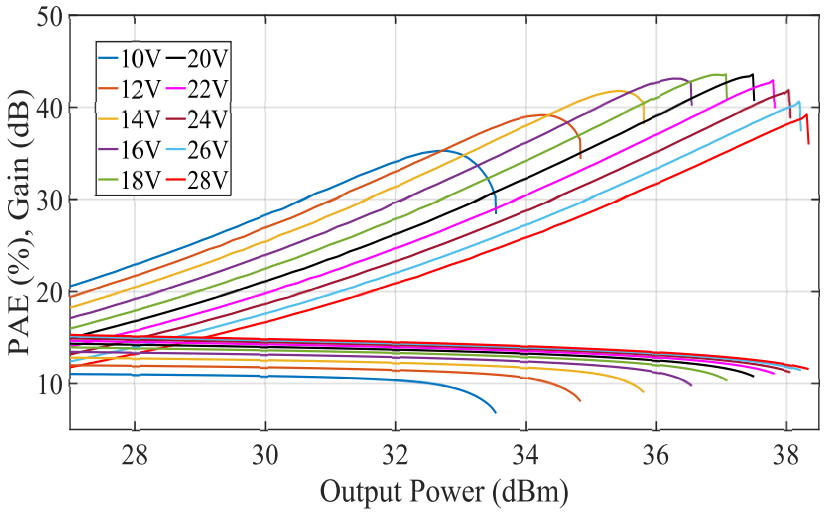


Figure 3.13: Static measured PAE and power Gain vs. output power for drain voltages ranging from 10 V to 28 V in 2 V steps at 12.8 GHz.

Figure 3.14 shows a bench top picture of the supply modulation bench used in this work. It consists of an arbitrary waveform generator (AWG) that creates the baseband 34 MHz and 67 MHz 64-QAM signals fed into the vector signal generator (VSG) and bit pattern generator (BPG). An additional driver board is used to collect the IQ data from the BPG and drive the DSM. Various DC bias supplies are used to bias the DSM and PA which is connected to the DSM with a 3D printed mounting fixture. At the output of the PA, a spectrum analyzer measures the IQ data and linearity. Nonlinearities of the instrumentation are removed by a simple linearization of the input signal. A shaping function is created from the measured CW PAE, P_{out}, and gain of the PA to optimize the performance for the desired metric, which could be flat gain, maximal

PAE in backoff, etc. [78].

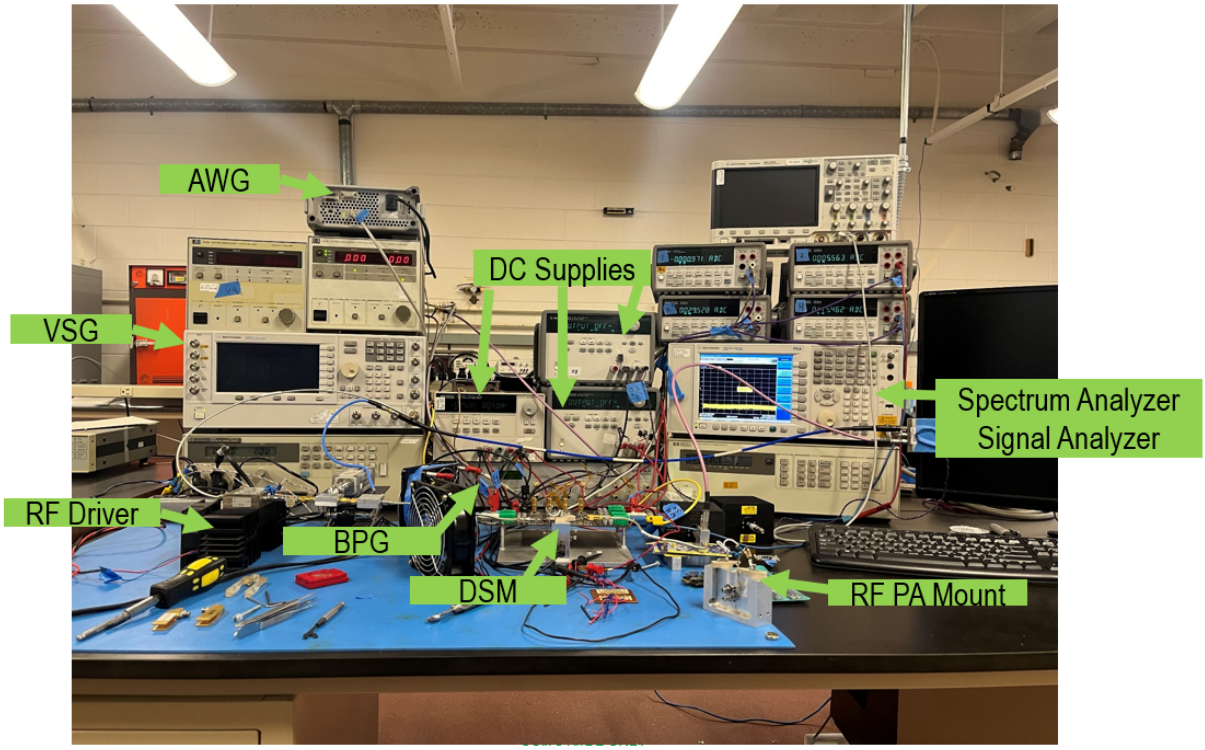


Figure 3.14: Supply modulation bench top setup in the lab for this work. Thanks to Drs. Paul Flaten and Connor Nogales for assistance in setting up the bench and design of the signals and dc supply modulator.

The supply modulation measurements of the PA combined with the DSM are performed with a 34 MHz 64-QAM signal, and with a wider-bandwidth 67 MHz signal. All measurements are performed with a shaping function for maximum PAE. The measured average PAE and composite PAE for the 34-MHz (left) and 67-MHz (right) signals at 8.8 GHz, 11 GHz, and 12.8 GHz are shown in Figs. 3.15, 3.16, 3.17 respectively. The plots also show the average gain and EVM with no DPD applied. The performance for the two signals is very similar across frequency. The dynamic measurements are compared to static supply voltage results at 28 V (dotted line). The average PAE (red solid trace) exceeds the static supply case by 5 percentage points at higher powers, and down to almost 10 dB backoff at 8.8 GHz and 11 GHz. At 12.8 GHz where the PAE of the PA peaks, the dynamic average PAE (light blue solid trace) is more than 10 percentage points higher than for the static supply case.

Although the $CPAE$ is lower than the PAE due to the added inefficiency of the supply modulator, it is in all cases at least 2 percentage points higher than the static supply. The dc supply modulator is designed

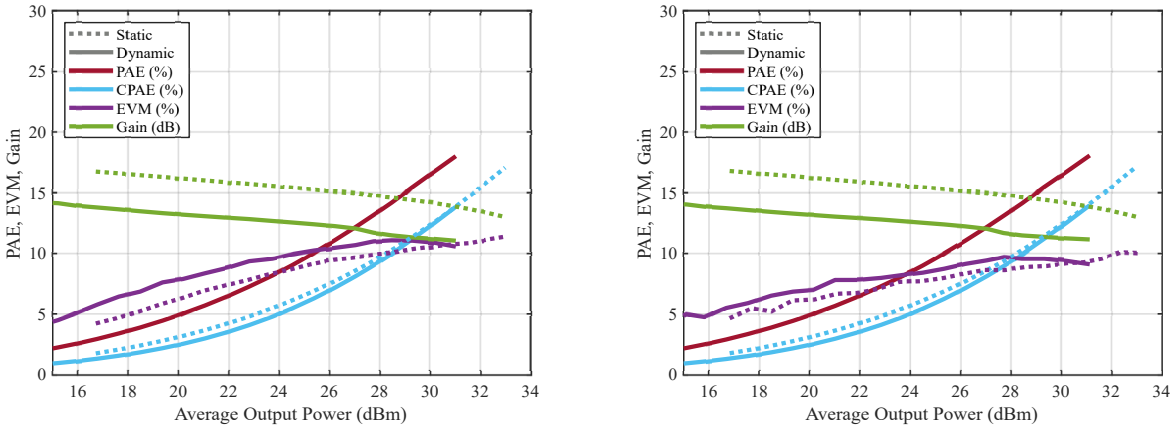


Figure 3.15: Measured static 28 V (dotted) and dynamic (solid), PA dynamic PAE, composite PAE, EVM, and gain vs. average output power for a 34 MHz (left) and a 67 MHz 64-QAM modulated signal (right) at 8.8 GHz

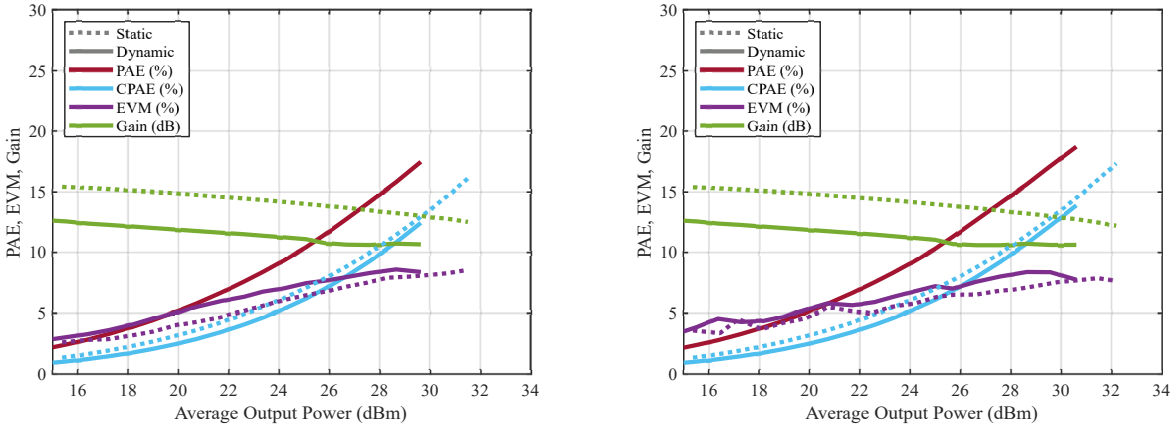


Figure 3.16: Measured static 28 V (dotted) and dynamic (solid), PA dynamic PAE, composite PAE, EVM, and gain vs. average output power for a 34 MHz (left) and a 67 MHz 64-QAM modulated signal (right) at 11 GHz

for PA's with higher output power 10 W and so the architecture utilized has higher dc power consumption in the nominal case. The PA designed in this work is a 6 W PA and is slightly undersized. Due to the increased average PAE of the PA, the RF transistors and MMIC dissipate less heat, and the heat is distributed between the PA and the DSM. This in turn means that the MMIC PA can be operated at a higher voltage.

For example, in Fig. 3.17 (left) for the 34 MHz signal, at an average output power of 30.8 dBm a comparison of the average dissipated power is compared in Table 3.2. The PA is the clear beneficiary of supply modulation in this case with 5.5 W dissipated in the static case, vs. 2.6 W in the dynamic case. While

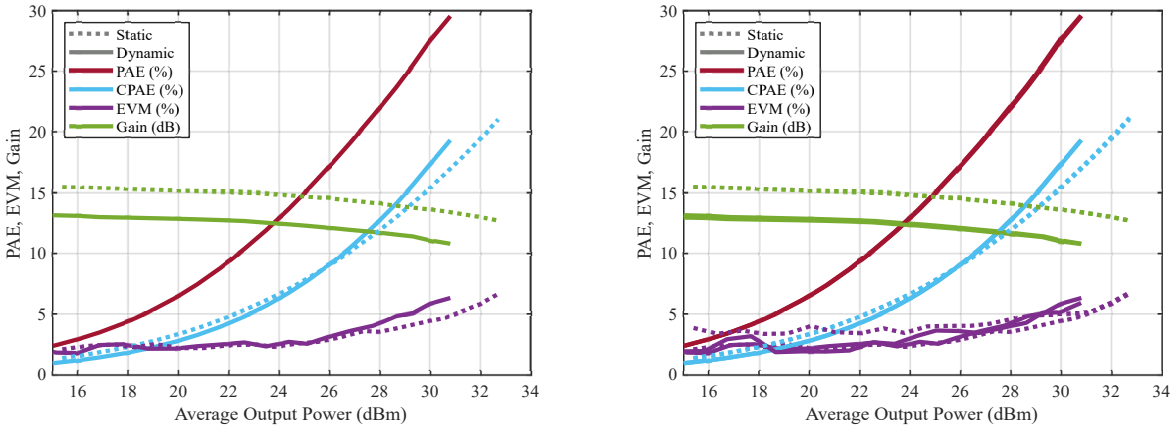


Figure 3.17: Measured static 28 V (dotted) and dynamic (solid), PA dynamic PAE, composite PAE, EVM, and gain vs. average output power for a 34 MHz (left) and a 67 MHz 64-QAM modulated signal (right) at 12.8 GHz

the system does not show as much improved power dissipation as desired, it is still better than the static case and splits up the location of the heat between the supply modulator and the PA, simplifying the heat dissipation problem.

Table 3.2: Average Power Dissipated to Heat Comparison

Avg. Pwr Dissipated. At average P_{out} of 30.8 dBm	Static V_{dd}	Dynamic V_{dd}
PA only	5.5 W	2.6 W
Entire System	5.5 W	4.5 W

Linearity can be observed through the EVM, which is measured with no DPD applied. Additionally, the measured large-signal transmission coefficient phase variation across drain voltages (10 to 28) V is shown in Fig. 3.18. Interestingly, for the lowest phase variation (at 12.8 GHz), the EVM is also lower. This indicates that a phase modulator, such as the one shown at K-band in [79], could be integrated at the PA input for analog linearization.

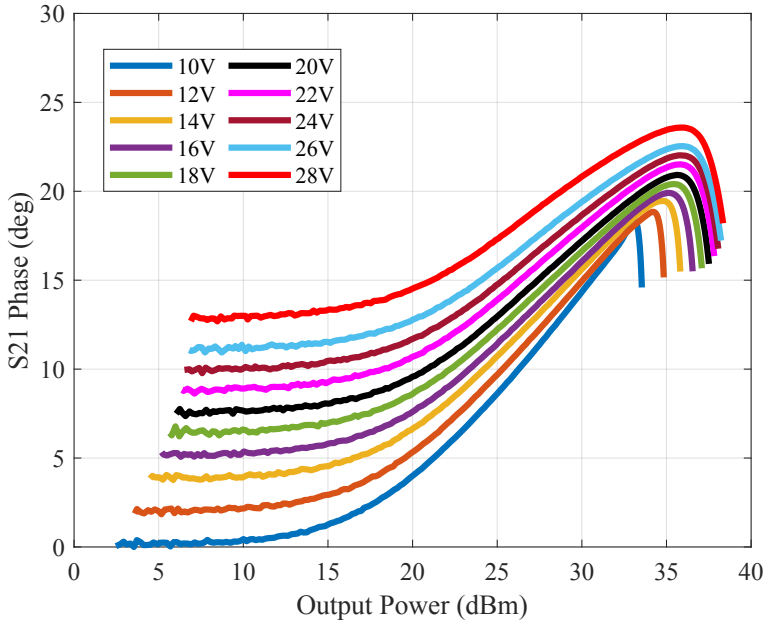


Figure 3.18: Measured transmission coefficient phase variation across drain voltages (10 to 28) V vs. CW output power at 12.8 GHz. Phase variation at 30 dBm of output power is 6.4°.

3.4 Case Study: Multistage MMIC Amplifier

In this section, the STO method is applied to a multi-stage amplifier design. A multistage Ku-band MMIC amplifier design is used as an example, starting from multiple transistor simultaneous source- and load-pull.

3.4.1 Multi-Stage PA MMIC Design Example

In a practical transmitter, multiple stages as well as on-chip combining are necessary for achieving the required output power and gain. A common design method for a multi-stage PA is to separately load- and source-pull transistors in the various stages in simulations, and then combine the individually designed stages. This only achieves an initial design which then needs to be modified to account for bilateral interactions between devices. While this is a reasonable approach, the CAD tool optimizer might find a solution that is a local extremum, resulting in e.g. a design that is difficult to practically realize, or that is sensitive to parameter values.

In current CAD tools, there is no straightforward method to perform concurrent multi-stage load- and

source- pull, which would be helpful to determine the drive levels and best impedance targets in the interstage network. The STO method can be used to run a multistage load- and source- pull sweep of a number of transistors and import the data to create a multi objective visualization plot for trade-off analysis. Fig. 3.19 shows a circuit model of the setup used in simulation software to generate the parallel plot data. The variables in blue text are varied, while the variables in black text are fixed.

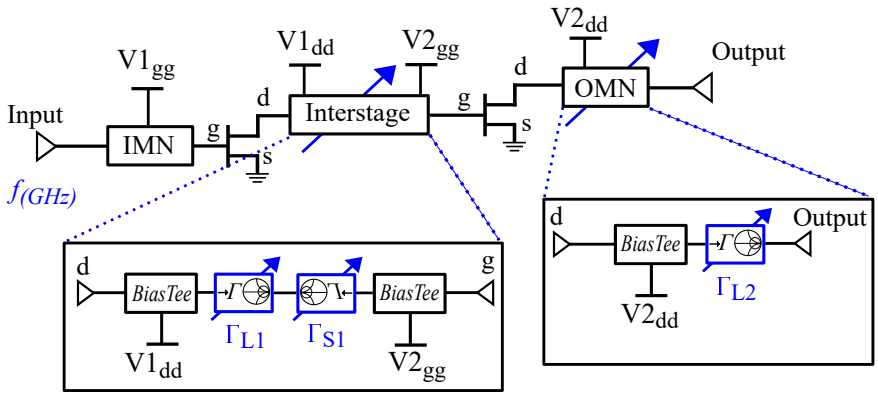


Figure 3.19: Circuit model of the multistage design setup. The IMN is fixed, while the interstage and OMN include ideal load and source pull tuners that are swept. Blue items denote swept simulation variables: $f_{(\mathrm{GHz})}$, Γ_{L1}, Γ_{S1}, and Γ_{L2}.

To validate the design methodology, a two-stage MMIC PA is designed for 20—29 GHz, aiming to maximize PAE while ensuring sufficient drive from the first-stage HEMT to drive the second-stage HEMT into compression. Following a similar approach to that in Section III.C for the 6 W hybrid PA, a "manual load-pull" schematic is created to sweep multiple transistor reflection coefficients and performance, similar to Fig. 3.19. Cadence Microwave Office and the WIN Semiconductors NP12-01 PDK (120 nm GaN, f_T > 50 GHz) are used. The staging ratio is 1:2, using a $4 \times 100\,\mu$m driver and an $8 \times 100\,\mu$m power stage, determined by the available die size and from previous device examination using the LPE method. This staging ratio ensures sufficient available drive to saturate the output stage. The input matching network is fixed from prior source-pull simulations, while the first-stage load, second-stage source, and second-stage load reflection coefficients are varied across frequency. The process for determining the interstage and final stage impedances for design of the matching networks is discussed next.

3.4.2 Interstage Matching Using the MoV STO Method

During the design using the MoV STO process, the number of variables is reduced by simulating source- and load- pull sweeps initially to confirm areas of interest for each device. The first stage $4 \times 100\,\mu$m device impedance is then fixed to $|\Gamma_{S1}| = 0.75$ and $\angle\Gamma_{S1} = 160\,^\circ$ as this has less impact on final stage PAE and P_{out}. After the individual load and source pull simulations, the combined schematic is created with sweep regions chosen by the designer. The "manual" load– and source–pull schematic is represented in Fig. 3.19. We also fix P_{in} =20 dBm, $V1_{gg} = -1.6$ V, $V1_{dd}$ =20 V, $V2_{gg} = -1.6$ V, $V2_{dd}$ =28 V. The swept variables are shown in Table 3.3.

Table 3.3: Sweep Variables of Multi-Objective Multi-Stage Plot from 20 to 29 GHz in 0.5 GHz steps

Var.	$\lvert\Gamma_{L1}\rvert$	$\angle\Gamma_{L1}$ (°)	$\lvert\Gamma_{S2}\rvert$	$\angle\Gamma_{S2}$ (°)	$\lvert\Gamma_{L2}\rvert$	$\angle\Gamma_{L2}$ (°)
Values	0.55–0.85	75–125	0.55–0.85	120–180	0.65–0.95	95–145
Steps	0.1	5	0.3	20	0.1	5

The interactive graphical representation in Fig. 3.20 is a set of non-dominated solutions. A unique design is selected which is a specification of the vector of decision variables in the form of equation (2.2). From left to right in Fig. 3.20, the 1st through 6th vertical columns represent the simulated reflection coefficients magnitude and angles. The 7th through 9th vertical columns are the objectives, (F_{minPAE}), ($F_{minPout}$), and (F_{maxPAE}) as in equation (2.1). The state column, $f_{(GHz)}$ is not included in this figure to save space.

The $|\Gamma_{S2}|$ and $\angle\Gamma_{S2}$ columns are "brushed" and found to be 0.85 and 180 ° respectively, as this has the smallest impact on the output PA performance. To obtain a feasible interstage match, $|\Gamma_{L1}| = 0.85$ and $\angle\Gamma_{L1} = 80\,^\circ$ are selected. This leaves $|\Gamma_{L2}|$ and $\angle\Gamma_{L2}$ which are chosen based on the visualized ($F_{minPout}$) column being filter for solutions with $P_{out} > 26$ dBm. The final selected solution values are ($|\Gamma_{L1}| = 0.85$, $\angle\Gamma_{L1} = 80\,^\circ$), ($|\Gamma_{S2}| = 0.85$, $\angle\Gamma_{S2} = 180\,^\circ$), and ($|\Gamma_{L2}| = 0.85$, $\angle\Gamma_{L2} = 130\,^\circ$) which is valid across $f_{(GHz)}$ = 20–29 GHz. This solution has PAE_{min} = 13.5 %, $P_{\text{out,min}}$ = 26.5 dBm, and PAE_{max} = 40.9%. These values are obtained with simulations using ideal lossless tuners and provide starting points for matching network design. The matching network implementation is chosen to use the fewest number of elements possible with

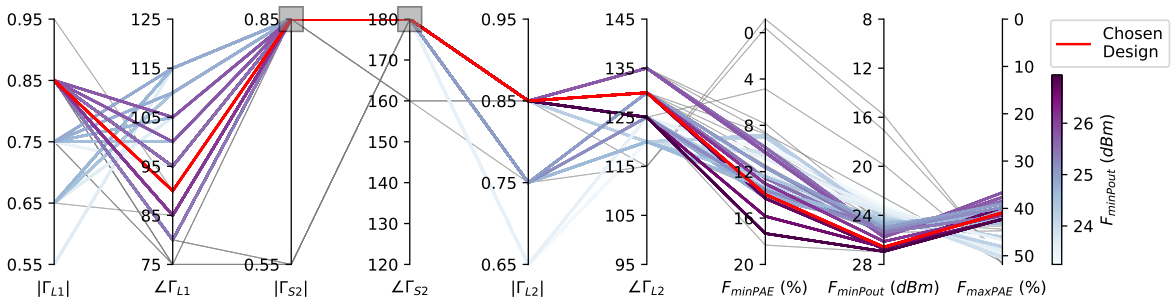


Figure 3.20: Visualization of the non-dominated solutions generated for a multistage GaN MMIC PA design with decision variable columns from left to right: $|\Gamma_{L1}|, \angle\Gamma_{L1}, |\Gamma_{S2}|, \angle\Gamma_{S2}, |\Gamma_{L2}|, \angle\Gamma_{L2}$. The next three columns represent objectives, PAE_{min}, $P_{\text{out,min}}$, and PAE_{max}. RF BW is not included in this figure as a column to save space, but was simulated and designed for 20–29 GHz.

the least loss, made possible by the relatively narrow bandwidth. The space constraint implies meandering of bias lines, as well as input and output microstrip transmission lines. This results in a final amplifier layout as shown in Fig. 3.21.

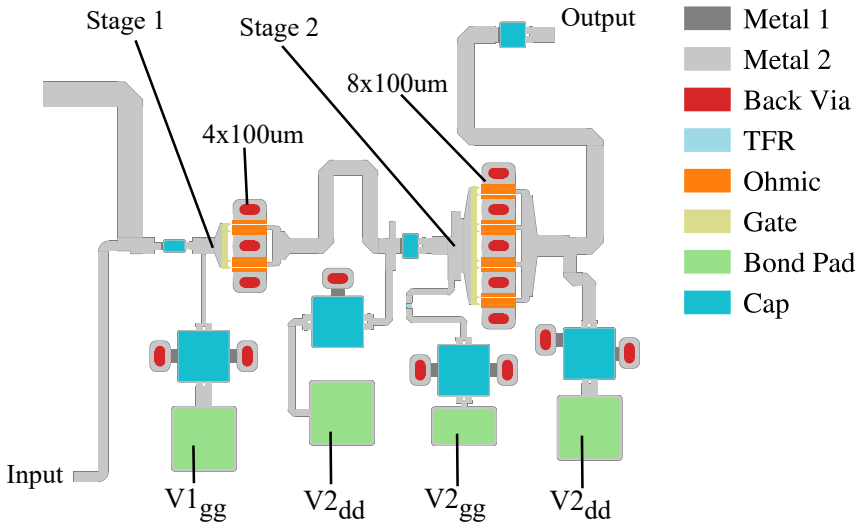


Figure 3.21: Layout of a two–stage MMIC amplifier in the WIN NP12 process.

The small-signal measurements (solid) vs. simulations (dotted), are shown in Fig. 3.22 for 18–30 GHz. The results align well with simulations, with a slight shift in $|S_{21}|$ to lower frequencies, while $|S_{11}|$ and $|S_{22}|$ show similar magnitudes and frequency shifts. This example briefly demonstrates how the MoV can be extended to additional goals, in the case multi-stage amplifier design. Other straightforward useful extensions

are discussed in the next section.

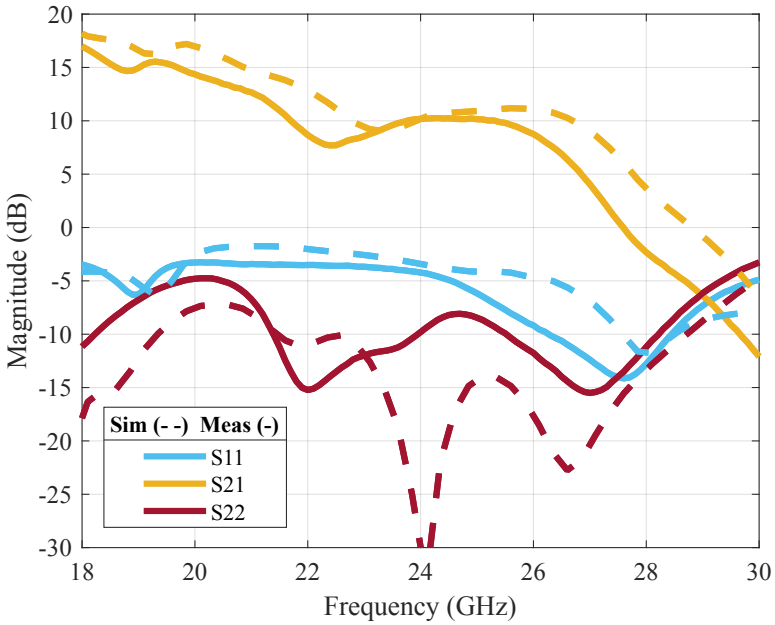


Figure 3.22: Small signal results from 18–30 GHz of a two–stage high frequency PA designed using the MoV STO method.

3.5 Conclusion and Discussion

In this Chapter, the *Selective Trade-Off* method is shown as a method extension to the LPE method and applied to the problem of interstage matching network design from bilateral source- and load-pull as well as component sensitivity analysis due to process variation. The work in this Chapter was published in two conference papers, the first is not publicly available, but titled *PA and Supply Modulator GaN MMICs for Efficient High-PAE Signals in the 8–14 GHz Band.* presented at GOMACTech 2024, the other in [69], and the rest in a Journal of Microwaves article [70].

This Chapter also builds on a previously investigated multi-objective visualization method for PA design by including a design sensitivity metric for particular matching components. The method is validated on the example of an X-band GaN-on-SiC MMIC in the WIN NP15-00 process using shunt over via matching capacitors. The potential performance shift from matching components can then be included in future designs when component variability needs to be considered.

Here we show how to obtain the starting point for a multistage PA design and demonstrate it on a two-stage MMIC PA in the WIN Semiconductors NP12-01 process. Small-signal measurements agree well with simulations from 18 to 30 GHz. A limitation of the multistage technique is that the tuner's reference impedance is not 50 Ω, so some additional optimizing must be done after MoV solution is found. The given example of the STO method, though not complete, is useful for multistage design by providing a starting place that includes the bilateral effects of the transistors.

Additionally, the X-band MMIC was designed using the MoV method to include a range of drain supply voltages intended for supply modulation. The design and characterization of the GaN MMIC heterogeneously integrated with a dc supply modulator for supply modulation. The PA is designed for a large supply voltage range (>18 V) with high efficiency in back-off for transmitting high PAPR signals. The DSM is capable of switching between four discrete states at a switching frequency of 65 MHz. When combined and characterized with 34/67 MHz 64-QAM signals with a maximum PAE shaping function, the average PA efficiency exceeds the static supply case by up to 10 percentage points, with only a small degradation in linearity with no additional digital predistortion.

Chapter 4

A Three Stage W-band MMIC PA in Qorvo's 90-nm GaN Process

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4.1 Introduction

This chapter examines a GaN-on-SiC process in development targeting W-band (75—110 GHz) performance, introduced in Chapter 1. The process is still evolving, with each run improving simulation-to-measurement agreement. In this version of the PDK, only a single nonlinear device is available and FET cell scaling is not permitted, limiting PA architecture and achievable gain.

A three-stage narrowband MMIC PA is presented with simulation and measurement results, along with a cascaded configuration to boost output power. Prior work with this process showed significant gain

degradation due to overestimation of device g_m [80]. The design objective here is to benchmark process progress and demonstrate a stable multi-stage PA design at W-band, with a possibility of straightforward external power combining of several PAs.

4.2 Unit PA Design

The single non-linear device model is first examined to determine design architecture and staging ratio. Multiple stages are required to achieve sufficient gain and output power at millimeter-wave frequencies. The only available device is a $8 \times 50\,\mu$m HEMT validated at a bias of 15 V and drain current density (J_d) of 25 mA/mm. The G_{max} of the device from 0.1 to 110 GHz is plotted in the left of Fig. 4.1. The right side of the figure shows the deconstructed layout of the device. The gain curve shows significantly higher small-signal gain at lower frequencies, which necessitates multiple stability techniques to ensure stable operation. In contrast, at 75 GHz the device G_{max} is approximately 7 dB, highlighting the need for multiple gain stages and power combining to achieve practical performance levels.

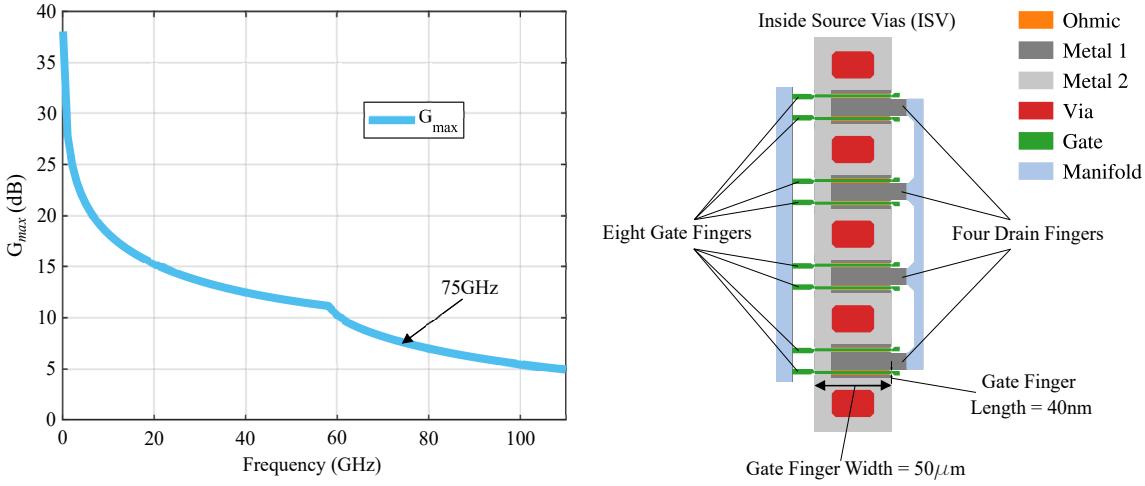


Figure 4.1: Left: G_{max} plot of the raw transducer gain of the $8 \times 50\,\mu$m HEMT. Right: Deconstructed layout of the $8 \times 50\,\mu$m HEMT with key elements pointed out.

4.2.1 Load– and Source– Pull Simulations

Since the device exhibits relatively low gain at W-band ($\leq$ 7.5 dB), multiple gain stages are required to achieve reasonable output power levels. Source– and load–pull simulations are performed in Cadence Microwave Office (AWR) using the available non-linear device model and shown in Fig. 4.2 and 4.3. At an input power of 24 dBm, the PAE and P_{out} load–pull contours nearly overlap, simplifying the trade-off decision. As expected, the source–pull contours are broad, indicating significant tolerance in source matching and its impact on output performance. Both load– and source–pull contours are plotted in roughly 10 GHz increments across W-band to illustrate expected performance and help to narrow down the target design bandwidth. At this input power, the maximum PAE drops by about 5 % every 10 GHz as frequency increases.

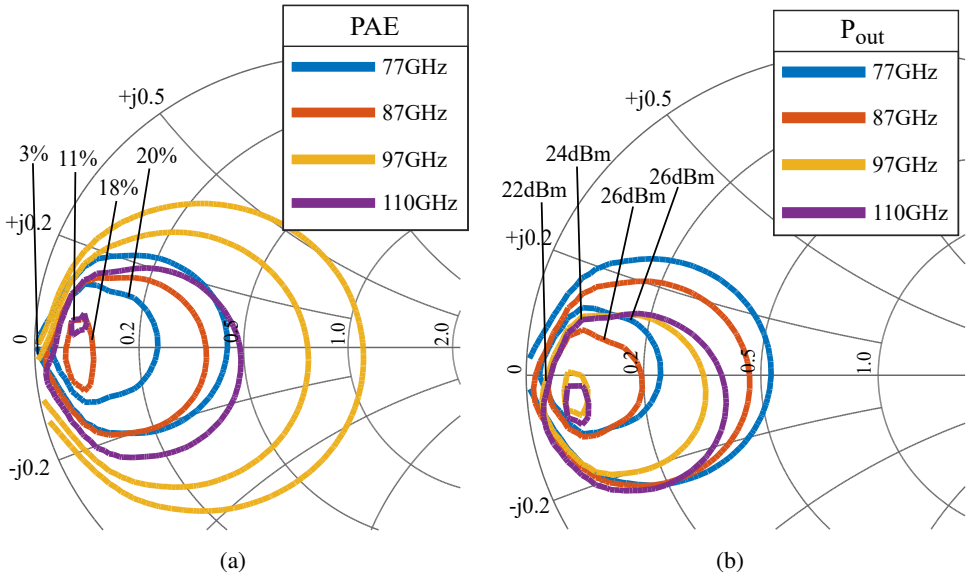


Figure 4.2: Source–pull simulations across W–band for the 8 $\times$ 50 μm HEMT, 24 dBm input. (a) PAE (b) P_{out}.

The next step is to analyze how much input power is required to reach the peak PAE for this device. The values of the Γ_S and Γ_L magnitude and angle components used in the ideal tuner simulations is listed in Table 4.1. The Γ_S values are fixed across W–band as its impact on PAE and P_{out} is minimal compared to the selection of Γ_L. The Γ_L value is varied based on the load–pull PAE contours seen in Fig. 4.3 (a). The device is biased at V_{dd} = 15 V and J_d = 25 mA/mm. The input power drive-up curves at 77, 87, 97, and 110 GHz is shown in Fig. 4.4.

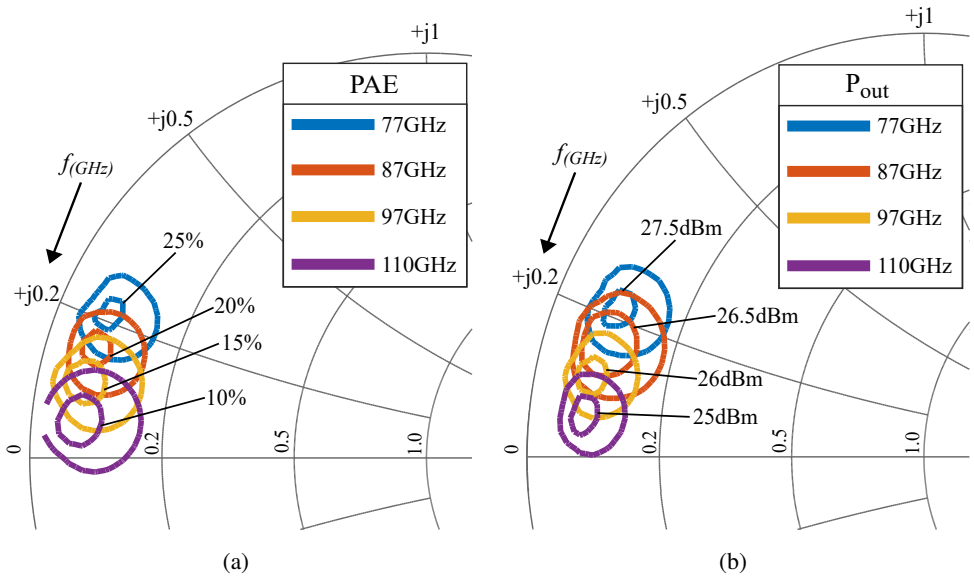


Figure 4.3: Load–pull simulations across W–band for the 8 × 50 μm HEMT, 24 dBm input. (a) PAE (b) P_{out}.

Table 4.1: Reflection Coefficients Across W-band

Frequency	$\lvert\Gamma_S\rvert$	$\angle\Gamma_S$	$\lvert\Gamma_L\rvert$	$\angle\Gamma_L$	V_{dd}	J_d
77 GHz	0.9	182°	0.85	158°	15 V	62.5 mA/mm
87 GHz	0.9	182°	0.85	162°	15 V	62.5 mA/mm
97 GHz	0.9	182°	0.83	167°	15 V	62.5 mA/mm
110 GHz	0.9	182°	0.83	175°	15 V	62.5 mA/mm

The input power drive-up curves show the peak performance of the device at W–band is the 77 GHz curve with 25 % PAE, 28 dBm of output power, and 4 dB of power Gain. As noted from the load–pull contours, at the same input power, in increasing steps of 10 GHz, the PAE drops about 5 %, output power drops about 1 dB, and power gain drops about 1 dB. To obtain reasonable levels of performance, the design is centered at 77 GHz, also an automotive radar band [15] where other PAs in literature exist for comparison. The low power gain necessitates multiple driver stages and reactive power combining to achieve watt-level output.

To achieve maximum PAE and fully compress the device, about 24 dBm of input power is required. Two devices are reactively power combined to ideally increase the output power from 28 dBm to 31 dBm. The two 8 × 50 μm devices in the output stage have a combined periphery of 800 μm. From the drive-up curves, a single interstage device can reach 24 dBm of P_{out} at an input power of 19 dBm, with a second

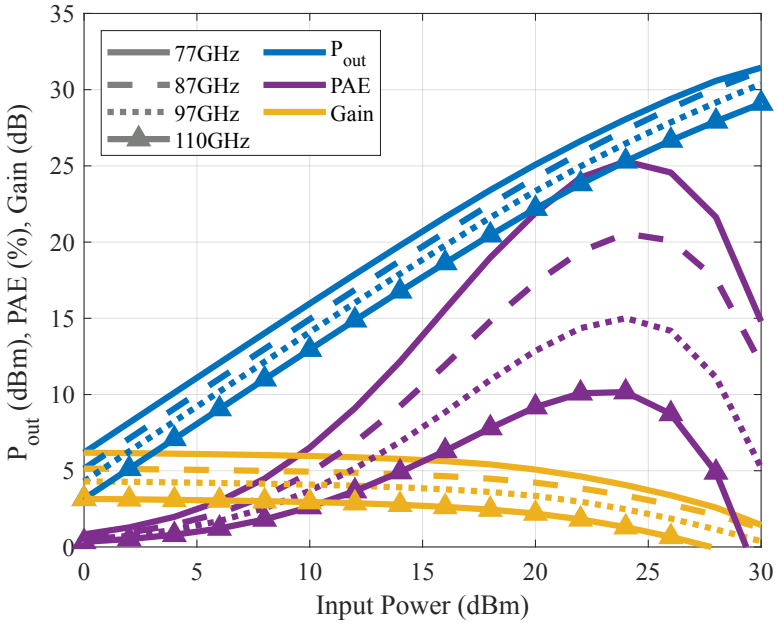


Figure 4.4: Input power drive-up curve for the $8 \times 50\,\mu$m device. Different frequency curves are represented by different line types and performance metrics represented by different colors.

stage reaching 19 dBm, of output power at 13 dBm of input power. The final staging ratio is then 1:1:2, this is less than optimal for a power amplifier due to the over sizing of staging ratio and thus adding more dc dissipation, lowering the PAE. The power budget is based on ideal targets, so an additional 1-2 dB margin should be added per stage to account for matching network loss and interstage mismatch. A figure of the circuit schematic is shown in Fig. 4.5.

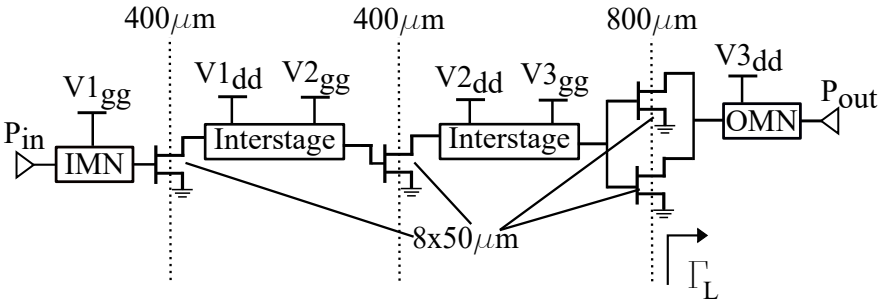


Figure 4.5: Circuit schematic for final PA design only using $8 \times 50\,\mu$m HEMTs. Device periphery and bias voltages are labeled. The direction of the Γ_L is indicated for the optimal reflection coefficient the matching network must present to the device for optimal PAE and P_{out} based on simulated load-pull data.

4.2.2 Matching Network Design

Once the architecture and frequency range are chosen, more selective source– and load–pull simulations are performed to decide on the optimal impedance to present to the transistors. The device models used rely on measured millimeter–wave load–pull data which can be limited in frequency by available equipment [25]. Since this process is developmental, the model-based simulation data may not be as accurate at lower frequencies for well characterized GaN nodes. The optimal PAE and P_{out} regions are identified from sweeps of $|\Gamma_S|$ = [0.75–0.95], $\angle\Gamma_S$ = [174–186]°, $|\Gamma_L|$ = [0.75–0.95], $\angle\Gamma_L$ = [150–176]°, and frequency is swept from 75–81 GHz. The gate bias is set at -1.6 V, drain bias at 15 V. The source– (a) and load–pull (b) plots are shown in Fig. 4.6 at the center frequency f_0 = 77 GHz and P_{in} = 24 dBm. The selected source and load reflection coefficients are outlined with a black 'x', $|\Gamma_S|$ = 0.9, $\angle\Gamma_S$ = 182°, $|\Gamma_L|$ = 0.85, $\angle\Gamma_L$ = 158°.

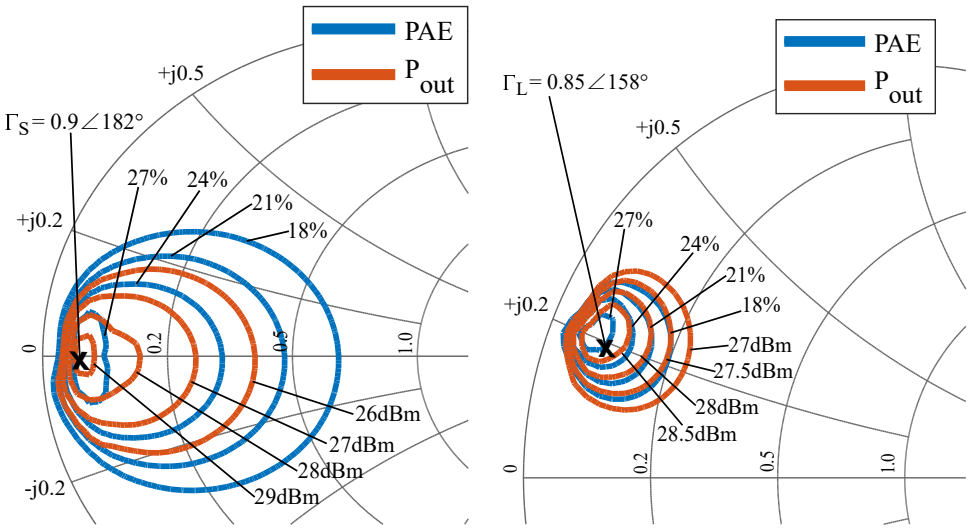


Figure 4.6: Source– (a) and load–pull (b) simulations at 77 GHz, 24 dBm P_{in} for the output stage 8 × 50 μm HEMT.

Once the desired reflection coefficient is determined, the matching network must be designed to transform the 50 Ω load termination to the ideal load termination from the load–pull simulation. The matching network design process follows [4]. The $\Gamma_L = 0.85\angle 158°$ is converted to a load impedance, Z_L, which the transistor needs to be presented at the output for PAE and P_{out} trade off.

$$\Gamma_L = \frac{Z_L - 50\Omega}{Z_L + 50\Omega} \rightarrow Z_L = 50\Omega\frac{1+\Gamma_L}{1-\Gamma_L} = 4.2 + j9.65\Omega \tag{4.1}$$

The form of eq. 4.1 assuming conjugate matching, implies the output of the transistor looks like a series RC circuit. In practicality, the frequency response of the output of the transistor acts more like a parallel RC when observing load–pull measurements [39]. To solve for parallel RC values, the conjugate of the load impedance, Z_L^*, is converted to an admittance,

$$Y_L^* = \frac{1}{Z_L^*} = \frac{1}{4.2 - j9.65} = 37.9 + 87.1\text{mS} \tag{4.2}$$

Once the conjugate of the admittance is found we can solve for the parallel resistor and capacitor values. Solving for the R_p,

$$R_p = \frac{1}{\text{Re}(Y_L^*)} = \frac{1}{0.0379} = 26.38\,\Omega \tag{4.3}$$

and the C_p,

$$C_p = \frac{\text{Im}(Y_L^*)}{2\pi f} = \frac{0.0871}{2\pi \times 77\,\text{GHz}} = 0.18\,\text{pF} \tag{4.4}$$

Once the R_p, C_p values are scaled per the number of devices, the initial ideal matching network topology is scaled accordingly. The R_p is halved and the C_p is doubled based on the number of devices scaling toward in this design. This serves as a model of the output of the transistor and can begin the matching design element. Initial output matching network design is started with ideal inductors and capacitors matching the representative R_p, C_p values to a 50 Ω load. This process follows similar outline from [4]. The ideal elements are substituted for more accurate microstrip lossy elements and bias and dc blocking capacitors substituted with three layer PDK capacitor models.

The matching networks of the amplifier are designed using varied impedance transmission lines and open stubs. This narrowband design does not have stringent restrictions on the Q–factor of the matching networks, so the smallest number of transmission-line sections are used to limit conductive losses. A deconstructed layout image of the PA is shown in Fig. 4.7.

High-frequency HEMTs have high gain at lower frequencies, so stability is critical and it is important to include a multitude of stability elements into the design. Gate bias lines include small series resistors($\approx 5\Omega$) and decoupling capacitors of multiple sizes to eliminate potential bias–line oscillations. Drain bias lines also include shunt capacitors and parallel resistor networks with a range of element values. Lastly, two small ($\approx$ 1.5Ω) resistors are placed in series in the matching networks and 50Ω odd mode stability resistors are added

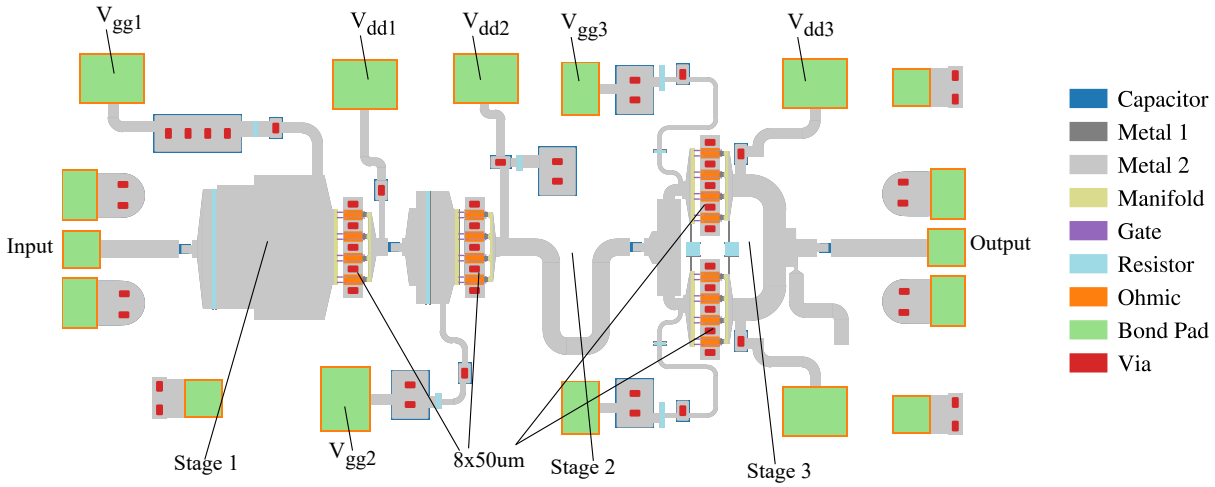


Figure 4.7: Deconstructed layout of three stage Qorvo GaN09 PA.

between the reactively power combined stage gate and drain networks. The PA stability is verified using the Nyquist criterion with the load and source termination ports of the PA varied to simulate possible instability conditions. The full PA is simulated using the Cadence Microwave Office 2.5D electromagnetic solver with a sufficiently fine mesh grid and up to 240 GHz. The Nyquist stability is calculated using gamma probes placed at the gate and drain of each transistor, and the loop gain is calculated and plotted on a polar plot.

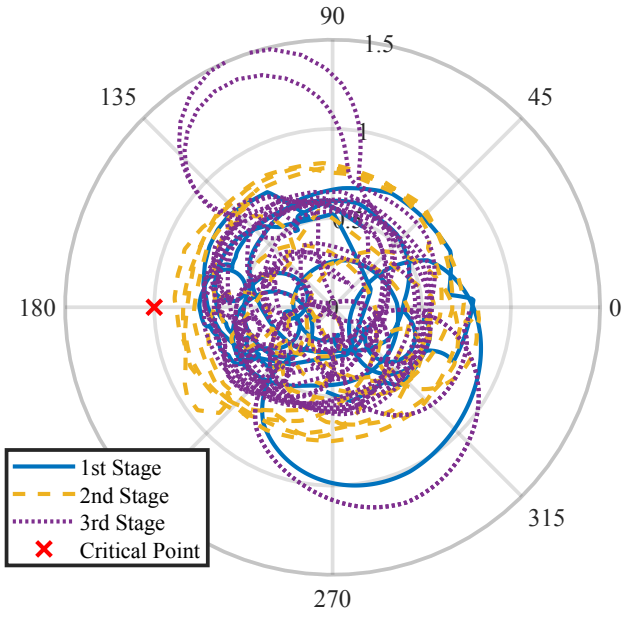


Figure 4.8: Simulated linear Nyquist plot for three stage power amplifier. Nyquist stability loops plotted to show no encirculation of the critical point (-1,0), marked by a red '×' occurs, indicating a stable PA. Simulated from 0.1 GHz to 240 GHz, the third harmonic of the PA design.

4.2.3 Unit PA Simulated Performance

The simulated performance of the PA at an input power of (6,9,12) dBm is shown in Fig. 4.9 over a frequency range 70–85 GHz. P_{out} is plotted in orange, Gain in green, and PAE in blue. Simulations at 9 dBm input power predict 23.6 dBm (229 mW) of output power, about 15 dB of gain and PAE = 6.5 %.

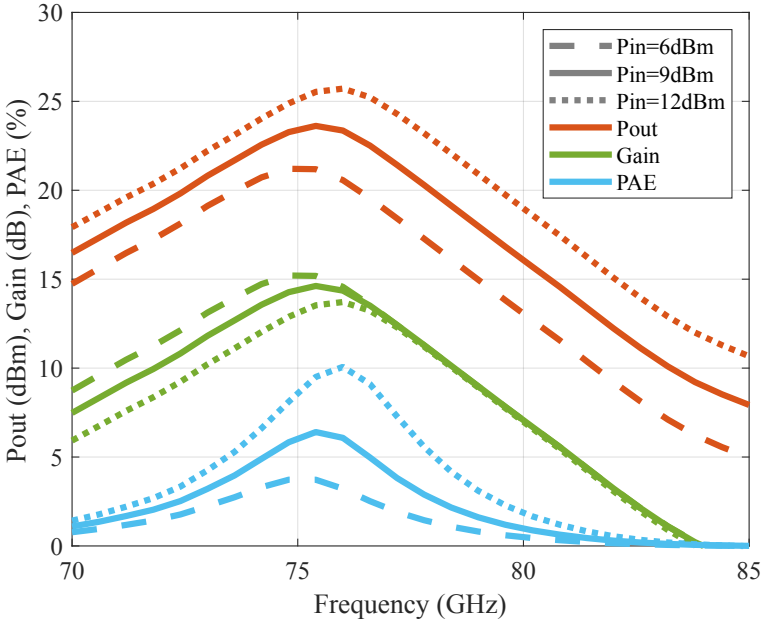


Figure 4.9: Simulated performance from 70–85 GHz of a single three-stage PA with input power curves of (6,9,12) dBm. At P_{in} = 9 dBm and 75.4 GHz, the output power is 23.6 dBm, with a G = 14.6 dB and PAE = 6.4%.

Figure 4.10 shows the simulated drive-up curves from 0–30 dBm of input power for several frequencies between 76 and 78 GHz. At P_{in} = 22 dBm at 77.2 GHz, the simulated peak PAE is 20.6 % with P_{out} = 31.1 dBm (1.28 W) and G = 9.1 dB. This result would be competitive with SOTA literature at W-band if the model was accurate, as achieving 1 W at W–band is difficult and reaching 20 % PAE would be excellent at 77 GHz.

The final PA design is then replicated six times per die to allow for power combining and additional gain to achieve higher power at W–band. The final reticle measuring 5 mm by 3.5 mm with replicated PAs is shown in Fig. 4.11 on the right. The left shows an expanded diagram of the single “unit PA”. The PAs are placed on the reticle so that the right side can be used as a driver to the left side “unit PA.”

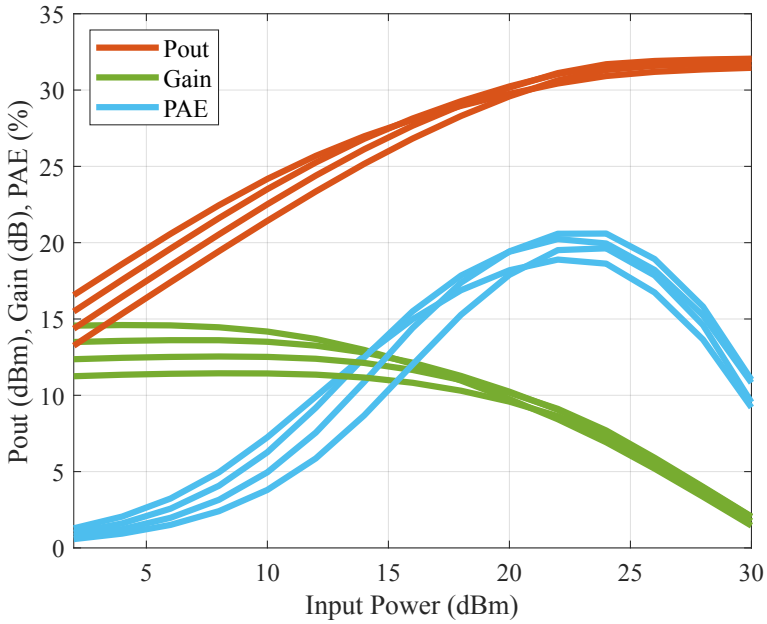


Figure 4.10: Simulated driveup curves of a single PA from 76–78 GHz for input power from 0–30 dBm. At in input power of 22 dBm and frequency of 77.2 GHz, P_{out} = 31.1 dBm, G = 9.1 dB, and PAE = 20.58 %.

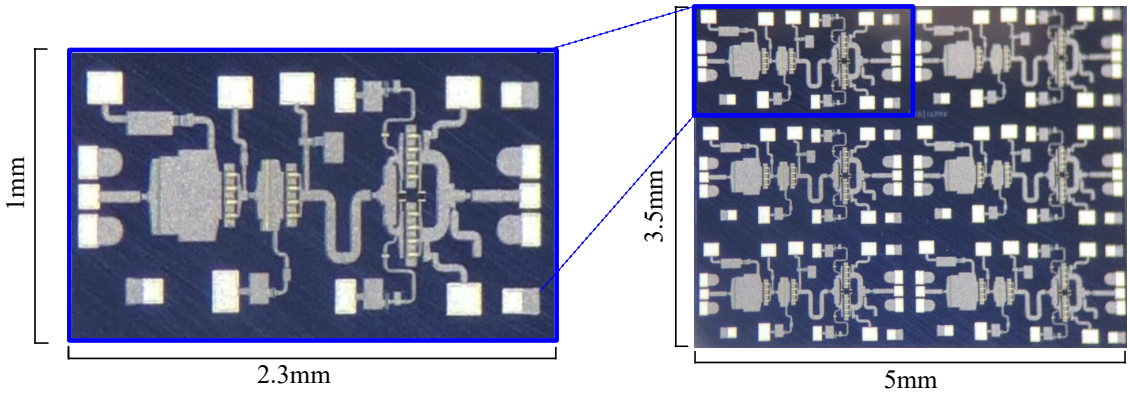


Figure 4.11: GaN09 full reticle picture showing reason for laying PAs out as such. Also conceptual power combining technique for achieving more output power at W–band.

4.3 Measurements

4.3.1 Small-Signal

The small-signal results are obtained with on-wafer probing using an HP8510C network analyzer with millimeter-wave extender heads to V-band (50–75 GHz) and W-band (75–110 GHz). The die is mounted on a copper-molybdenum (CuMo) carrier and dc probed with tungsten tips that connect to a chain of off-chip

single-layer stability capacitors (100 pF and 1000 pF). The capacitors are connected to the dc pads of the PA using 1-mil gold bondwires. The small-signal bench setup (left) and microscope image of the DUT (right) is shown in Fig. 4.12.

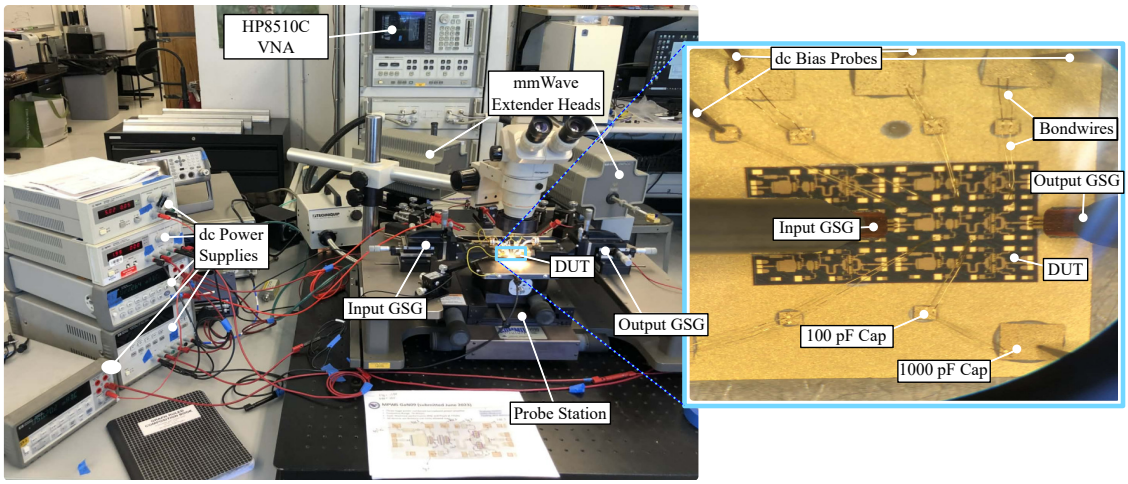


Figure 4.12: Small-Signal V- and W- band bench top setup (left) with on-wafer probing of DUT image through the microscope. (right).

Figure 4.13 plots the simulated S-parameter magnitude data in dotted lines and the measured results in solid lines. All results are shown from 55–95 GHz. Note that there is a gap in the small-signal measurements at 75 GHz due to the exchange of equipment at the frequency point. The results show simulated $|S_{21}| = 11$ dB at 74 GHz and in measurement $|S_{21}| = 7.1$ dB, a difference of about 4 dB. The $|S_{11}|$ and $|S_{22}|$ are better matched in measurement than predicted by simulations. This is especially obvious in $|S_{22}|$ where the simulated value at 74 GHz is -5 dB, while the measured value is -27.9 dB, corresponding to a magnitude of the reflection coefficient of 0.562 and 0.04, respectively. Since the amplifier is designed for a power match, a low value of the output reflection coefficient is not expected. However, the measured value corresponds to a real-valued impedance of 54 Ω, indicating that a combination of parasitics could be reducing the absolute value of the reflection coefficient. For example, there is parasitic capacitance at the input GSG pads due to the presence of the neighboring amplifier, as well as edge parasitics of the finite size substrate.

Understanding that the models differ from the simulations in this process in development, we do see an improvement compared to previous work in an earlier version of the process. In [80], the small-signal gain of a wideband W-band power amplifier was lower than predicted by about 10 dB while the shape of

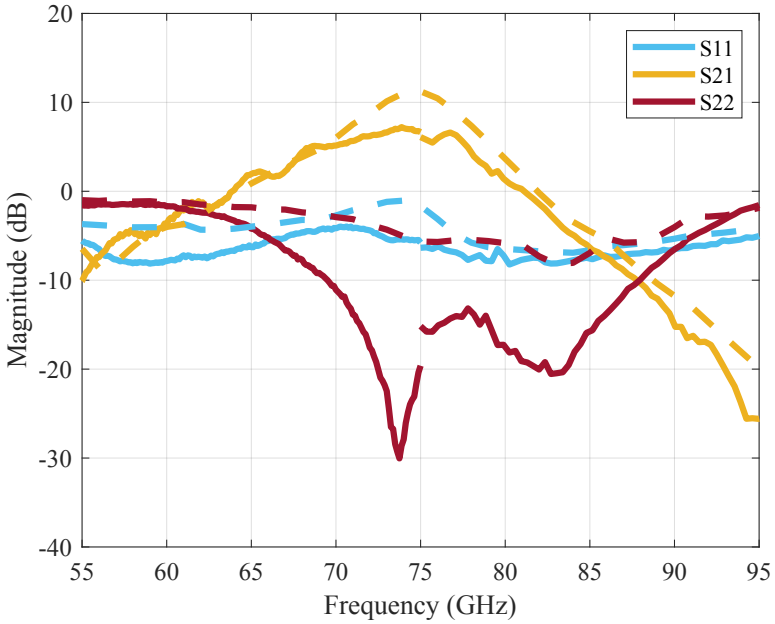


Figure 4.13: Simulated (dashed) and measured (solid) small signal results from 55–95 GHz. There is about a 4 dB gain discrepancy between simulations and measurements. Some variation is expected since this is a developmental process.

the gain was maintained. Additional analysis of the models is discussed in Chapter 5 with a different high frequency W–band GaN process. The discrepancy in small signal S-parameters can most likely be attributed to transistor model discrepancies. In this case, access to a non-linear model measured .S2p file was not available, but comparing the model conditions to the measured model intrinsic parameters would more sufficiently provide an explanation for the discrepancy seen in Fig. 4.13.

4.3.2 Large-Signal

The improvements in the 90 nm process are promising, but for this design the single three stage PA measurements suffer from the gain degradation and are limited by available driver power. As shown in Fig. 4.10, this PA requires at least 22 dBm of input power to reach the peak efficiency point and achieve 1 W of output power. Our setup for large signal measurements is limited by a Quinstar QPI-W0 1820-H4W02 W-band driver amplifier which after an isolator, coupler, and WR10 waveguide (WG) delivers a power of about 9–11 dBm at the DUT depending on the frequency. The large signal measurements of a single PA at various

input power levels vs frequency is shown in Fig. 4.14. Compared to the simulation results from Fig. 4.9 the single PA is under performing as expected based on the small-signal $|S_{21}|$ discrepancy from Fig. 4.13.

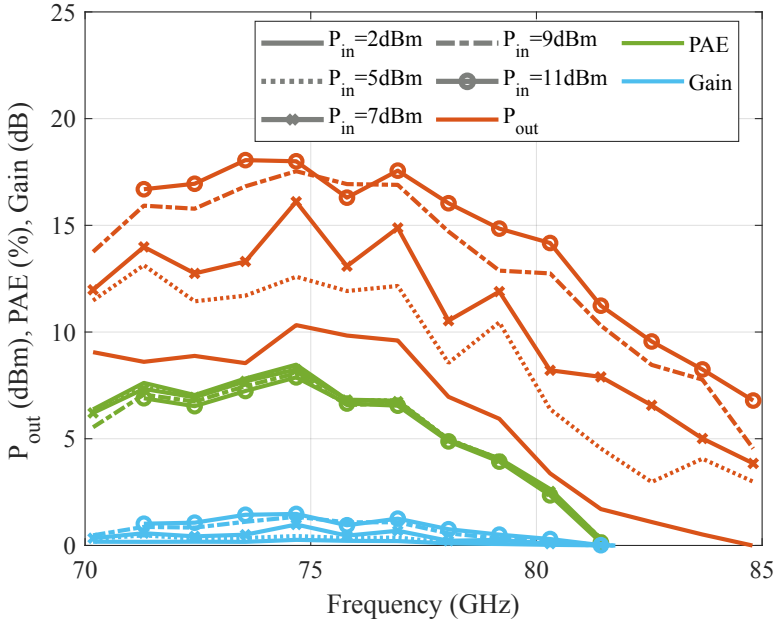


Figure 4.14: Measured performance curves vs frequency of a single PA at (2, 5, 7, 9, and 11) dBm of input power.

To overcome this limitation in obtainable instrumentation power at W-band, as well as enable external power combining, the MMIC PA is repeated 6 times on the die. This enables using one PA as a driver to the neighboring one, providing sufficient drive power up to 16 dBm at the input of the second PA. We first measured a single "unit" PA by probing on wafer, with degraded results compared to the simulations since the PA could not be driven sufficiently.

The top half of Fig. 4.15 shows a photo of a single PA probed with off-chip stability capacitors and the bottom portion (outlined in blue) shows the two cascaded PAs with the bond-wire connections. The cascaded 6-stage PA is measured using six dc probes, the maximum that can fit on the probe station for this chip. The first PA, probed by the input GSG on the right hand side of Fig. 4.15, is referred to as the "driver" and the second PA probed by the output GSG is referred to as the "output" PA. The gate and drain of the driver PA are bonded together and biased at $I_{dd} = 201$ mA, $V_{dd} = 15$ V. The three gates of the output PA are separately controlled and biased at $I_{dd1} = 30$ mA, $I_{dd2} = 60$ mA, $I_{dd3} = 128$ mA and the drains are also tied together

and set to $V_{dd} = 15\,\text{V}$. A picture of the bondwire setup for the cascaded PA for measurement is shown in Fig. 4.16.

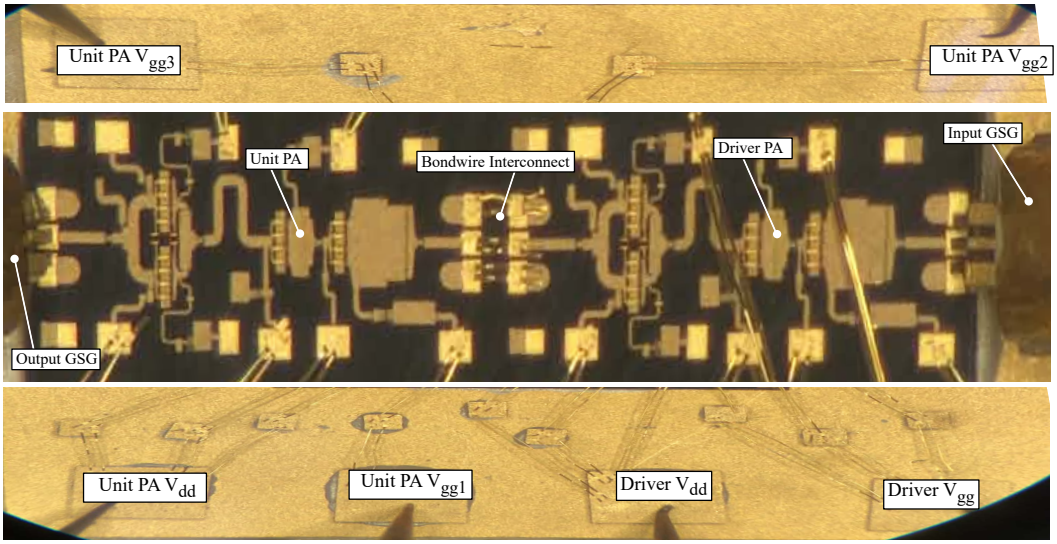


Figure 4.15: Diagram of the cascaded PA setup with corresponding biasing probe placement.

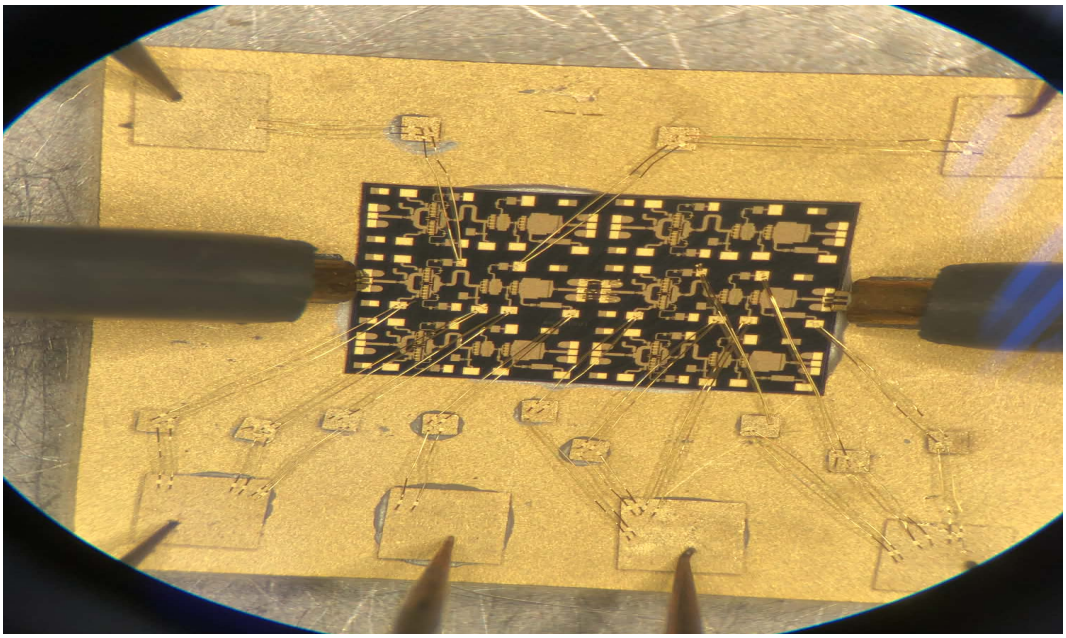


Figure 4.16: Picture showing the dc setup required for the cascaded PA setup. Required large bond wires for the dc connections.

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he measured results of the cascaded PA are shown in Fig. 4.17 with $P_{in} = 9\,\text{dBm}$. The PA achieves $P_{out} = 22.5\,\text{dBm}$ (177 mW), large signal gain of 12.15 dB, and $PAE = 2.5\%$ at 75.8 GHz. Overall, the

measured frequency response, output power, and gain show reasonable agreement with simulations. The largest discrepancy is observed in PAE, primarily due to inaccuracies in modeling the on chip "driver" PA. Because the driver is integrated on chip, it cannot be independently characterized or deembedded, and its interaction with the "unit" PA, including bondwire induced reflections, is not accurately captured in simulation. In addition, the "driver" PA is intentionally over biased, as the optimal gate bias for the final stage with two devices differs from that of the first stage. This tradeoff is acceptable, as ensuring sufficient drive power to the "Unit" PA is prioritized over optimal efficiency of the driver stage.

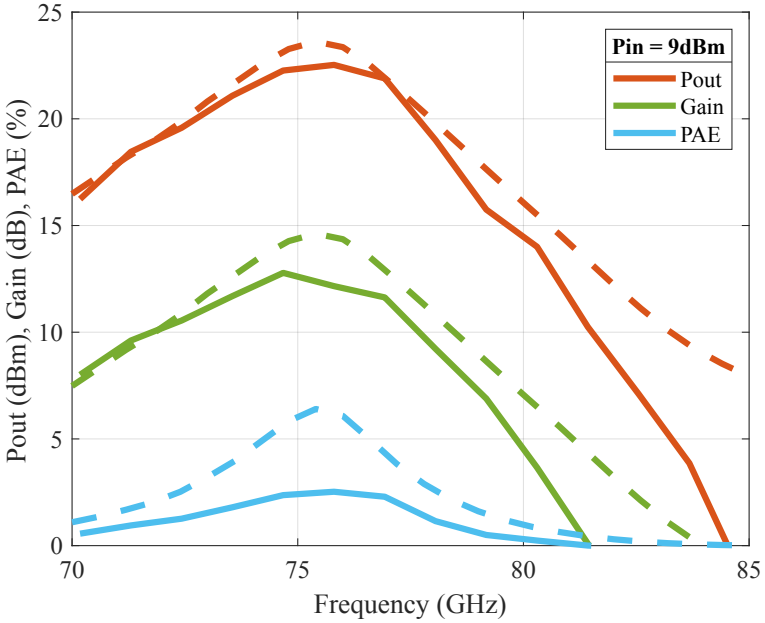


Figure 4.17: Simulated "unit" PA (dotted) vs large signal measurements of the cascaded PA (solid).

Overall, the PA is still limited in terms of the maximum performance and does not reach the peak PAE point from simulation in Fig. 4.10 of ≈20%. This still demonstrates reasonable agreement between the complex cascaded 6-stage PA and the simulation.

4.4 Conclusion and Discussion

This chapter demonstrates the design and measurement of a PA implemented in a 90 nm developmental GaN process. The process nonlinear models over-estimate the gain by about 4 dB in the 65–80 GHz range, still an

improvement from previous versions of the process compared to a previous demonstration [80]. The content in this Chapter is included in a conference publication presented at RWW 2025 [81].

Six identical PAs are placed on a single chip, enabling using one PA to drive a second one to compensate for the gain reduction and saturate the output stage. Cascading of two PAs effectively results in a 6-stage architecture with 12 dB of total gain, including the reflection from the bond-wire of the cascade. This experiment demonstrates second PA saturation and an output power similar to the predicted value of close to 200 mW of output power. Access to higher power W–band driver PA's in the future can more closely reach peak PAE and 1 W of output power at W–band. Additionally, a redesign in this process could employ more power combining per stage and include additional stages to ensure the PA can be saturated with the available W–band driver equipment. The PA in the next Chapter has the benefit of using more ideally scaled device sizes and power combining in the interstage as a demonstration of lowering the required drive power for saturation.

Chapter 5

An Impedance-Adaptive W-band GaN MMIC PA in HRL 40-nm GaN Process

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5.1 Introduction

Power amplifiers perform optimally under well-defined load conditions, but in practice, impedance often varies due to the environment or mutual coupling [82]. These variations can cause significant degradation in efficiency and output power, as demonstrated through PA simulations with antenna array scanning [83]. Several techniques have been proposed to mitigate load mismatch. Traditional solutions such as isolators or circulators decouple the PA from load variations but add loss, size, and cost, particularly at millimeter-

wave frequencies. For example, Ku-band self-biased hexaferrite circulators achieve 1.5 dB insertion loss at 13.6 GHz [84], while Ka-band commercial circulators report 0.8 dB insertion loss and 15 dB isolation [85] At higher frequencies, waveguide circulators demonstrate 0.37 dB insertion loss at 71.6 GHz with 17.8 dB isolation [86]. Transistor-based quasi-isolators have been demonstrated at W-band, e.g. in SiGe with 1.09 dB insertion loss and 28.5 dB receive-path isolation at 94 GHz [87] and in a GaN MMIC front end covering W-band with high isolation accompanied with relatively high loss [88]. Additionally, it is known that isolation of a circulator degrades when ports are mismatched, with an analysis of an active X-band MMIC circulator in a phased array environment shown in [89]. This has motivated interest in PA topologies that inherently tolerate load mismatch, either eliminating the need for additional isolation components between the PA and antenna, or improving the isolation under load mismatch.

At lower microwave frequencies, RMNs can be integrated directly into output networks, providing compact, low-power solutions using voltage-controllable reactive elements. An example that integrates an RMN and supply voltage control for recovering efficiency under load mismatch is shown in [90]. Monolithic (on-chip) RMN implementations have been demonstrated across several technologies and frequency bands, including some designed for use with PAs, though not always integrated with them [91–97]. In [93] and [94], MEMS-based tunable capacitors and high-Q inductors are used to realize integrated tuning networks for C-band and 20–50 GHz operation. A GaAs die in [91] is hybridly integrated with MEMS RMN to operate either in linear class-A or 58% efficient class-E modes at 10 GHz. A GaAs pHEMT-based varactor network offering continuous tuning at 5.8 GHz is described in [95], while [96] demonstrates a Ka-band reconfigurable PA using a discrete double-shunt stub topology with reverse-saturated SiGe switches. A self-healing CMOS PA with digital feedback for performance tuning at 28 GHz is presented in [97], and a 16-nm CMOS design with a tunable matching filter operating at 77 GHz is reported in [92].

The published demonstrations in [91–97] are at frequencies below W-band, while the higher-frequency work in [92] does not integrate the narrowband tuning network with an amplifier. The integrated tunable amplifiers are implemented in SiGe, GaAs or CMOS, and are almost exclusively single-stage, which helps maintain stability as the load is varied; the only exception is the two-stage 26.5–26.8 GHz, CMOS design with 14 dBm (0.025 W) of measured output power in [97]. The present Chapter fills the gap in published

literature by introducing a three-stage GaN power amplifier operating from 74.7—81 GHz with an integrated RMN, achieving 18.1 dB small-signal gain and 0.34 W of output power. The on-chip low-loss reconfigurable matching network is designed to recover power-added efficiency (PAE) and output power (P_{out}) in the presence of load impedance variation. The load–dependent reconfigurability is validated via comprehensive electromagnetic and large-signal simulations. The tunable elements are based on shunt FET configurations commonly used in millimeter-wave shunt switch designs, e.g. [98–104].

This chapter introduces the W-band GaN MMIC PA initial measurements with a comparison to a fixed-load PA.. Additional expansion includes a comprehensive analysis of multi-stage PA stability at W-band when the load varies, and a detailed investigation of the reconfigurable matching elements choice in terms of device sizes and characteristics. Additionally, measurements across eight chips from two wafers, test-structure validation, and extraction of intrinsic device parameters, are presented in order to explain the observed performance comparison to simulations. These results provide insights into how inherent variability in an advanced millimeter-wave 40-nm GaN process can impact the behavior of a complex tunable circuit.

5.2 PA Design in a Fixed 50 Ω Load Environment

The PA is designed in the HRL T3 40-nm GaN-on-SiC process, with f_T/f_{max} =160/360 GHz, a power density of 2 W/mm at 94 GHz, and breakdown voltage above 60 V [2]. The SiC substrate is 50-μm (2-mil) thick. Circuit design is performed in Cadence Microwave Office (AWR) using a nonlinear Angelov model for the high-electron mobility transistors (HEMTs). Passive structures such as transmission lines and air bridges are implemented with two metallization layers, while resistors use tantalum nitride and capacitors employ silicon nitride (SiN) dielectrics. Design specifications, summarized in Table 5.1, assume a 50 Ω termination impedance. $P_{3\text{dB}}$ denotes the input power level at which gain has dropped 3 dB from the small-signal value.

Specifications draw on prior research with this process and state-of-the-art W-band results [105]. Candidate devices include 2×25 μm, 4×37.5 μm, and 6×50 μm HEMTs, biased at +2, +6, and +12 V respectively, with drain current densities of 100–150 mA/mm. Available chip area limits the PA to 2–3 stages in the x-direction, constraining device choice and drive capability. The 6×50 μm HEMT is chosen for the output

Table 5.1: MMIC Power Amplifier Design Specifications

Specification	Value	Unit
Frequency Range	75–91	GHz
Input Return Loss	≥ 10	dB
Small-Signal Gain	≥ 15	dB
P_{out} at P_{3dB}	≥ 25	dBm
PAE at P_{3dB}	≥ 10	%
Large-Signal Gain at P_{3dB}	≥ 10	dB
Die Size (W×H)	4.8×1.5	mm^2
HEMT Supply Voltage	+6 to +12	V
HEMT Drain Current Density	100–150	mA/mm

stage, with additional stages needed to achieve ≥10 dB of large-signal gain. Figure 5.1 shows simulated drive-up curves for the three device options, all biased at +12 V and 150 mA/mm at the center frequency f_0 = 83 GHz.

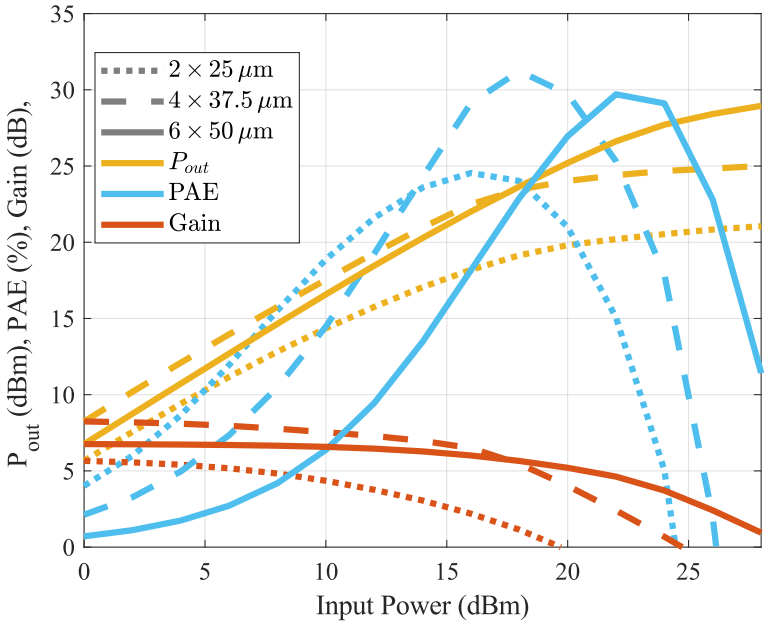


Figure 5.1: Simulated drive-up curves at 83 GHz for three devices with drain voltage of +12 V and drain current density of 150 mA/mm, terminated in maximum-PAE impedances at input and output.

The source– and load–pull simulations for the $4 \times 37.5\ \mu$m and $6 \times 50\ \mu$m devices are shown in Fig. 5.2 and Fig. 5.3, respectively. The peak value shifts counter–clockwise as frequency increases. The plots show

contours at 83 GHz, with source (Γ_S) and load (Γ_L reflection coefficient values corresponding to those used in the driveup curves in Fig. 5.1. These points provide an initial reference for designing the middle–stage device to supply sufficient output power to the $6 \times 50\,\mu$m output device. Since the $6 \times 50\,\mu$m device is larger, the associated capacitances (C_{gs}, C_{ds} and C_{gd}) increase, which reduces the reactance. The optimal matching impedance correspondingly shifts counter–clockwise compared to the smaller device. For these simulations, P_{in} = 22 dBm is selected based on the upper drive level of the $4 \times 37.5\,\mu$m device. At this drive level, the chosen load impedance $|\Gamma_L| = 0.7$, $\angle\Gamma_L = 125°$ falls within the P_{out} = 26 dBm contour. The PAE contour that intersects with the selected Γ_L is 28 %. The $PAE - P_{out}$ trade-off with this device is more significant, along with difficulty matching due to the increased capacitance of the device.

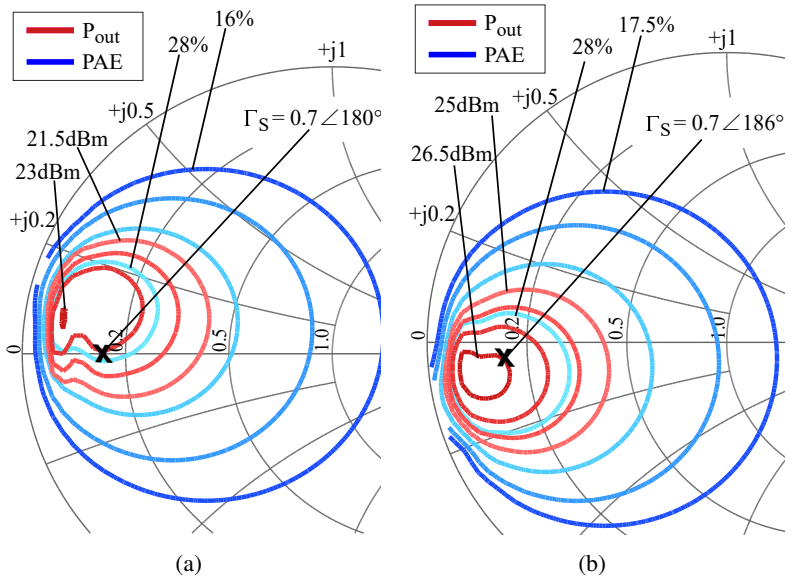


Figure 5.2: Source-pull simulations at 83 GHz of (a) a 4 × 37.5 μm HEMT at 16 dBm input power and (b) a 6 × 50 μm HEMT at 22 dBm input.

From the estimated power budget of the middle–stage device, the minimum P_{out} target is at least 20 dBm. The selected $|\Gamma_L| = 0.72$, $\angle\Gamma_L = 102°$ lies within the P_{out} = 22 dBm contour, which is broad an achievable match across frequency. The peak PAE contour also overlaps closely, simplifying the trade–off between efficiency and output power. The source–pull contours show little sensitivity to frequency, allowing the interstage match to be placed at a point that is both stable and straightforward to realize. Due to the relatively low gain of the devices at W-band, an additional driver stage is included using a single $4 \times 37.5\,\mu$m

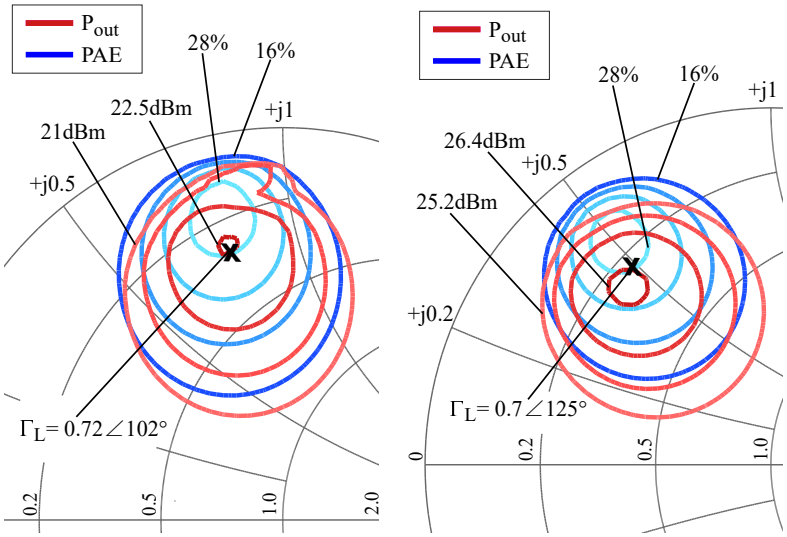


Figure 5.3: Load-pull simulations at 83 GHz for (a) a 4 × 37.5 μm HEMT at 16 dBm input and (b) a 6 × 50 μm HEMT at 22 dBm input.

device.The first stage can be driven with approximately P_{in} =12–13 dBm, producing 18–19 dBm at its output. The interstage, implemented with two $4 \times 37.5\,\mu$m devices for a combined 300 μm periphery, provides 5–6 dB of additional gain, yielding roughly 23–25 dBm to drive the final stage. The output stage, using two $6 \times 50\,\mu$m devices (600 μm periphery), requires about 22 dBm to reach compression, so the available drive ensures sufficient margin even with mismatch and interconnect losses. This staging results in a 1:2:4 ratio, chosen to balance drive capability and periphery scaling, and is expected to meet the target specifications in Table 5.1.

5.2.1 Stability Analysis

At W-band, stability is compromised by large low-frequency device gain and increased parasitic reactances. Even-mode oscillations can occur in power-combined stages since $S_{12} \neq 0$, while small asymmetries lead to odd-mode oscillations. Additionally, bias-line oscillations can occur when parallel resonance in the bias network produces negative resistance. The excess low-frequency gain must therefore be managed in the bias network to prevent feedback. This is done by using multiple capacitor values to isolate RF from the dc bias while maintaining high impedance in-band. Full-wave electromagnetic simulations are required to capture

resonance effects from bondwire inductances and external bypass capacitor parasitics. An analysis of bias line techniques is shown in Fig. 5.4.

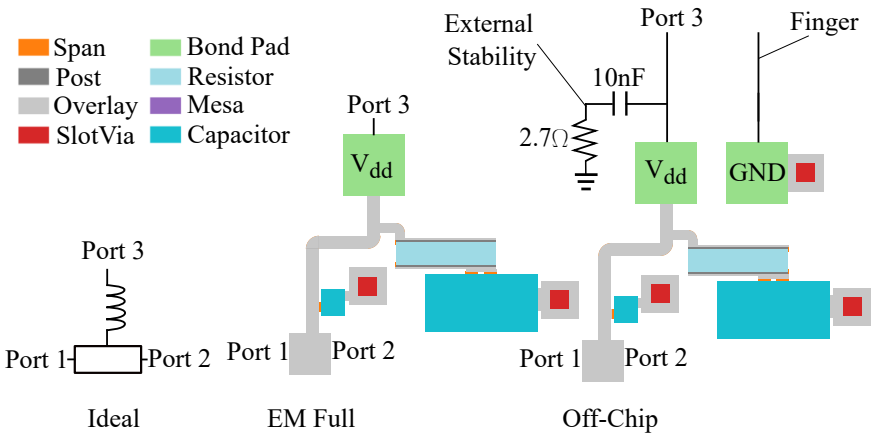


Figure 5.4: The drain bias line progresses from an ideal shunt inductor to a resonant capacitor–transmission line network, then to a full EM-simulated version with RC damping and external bypass components.

This figure illustrates the design process for stabilizing the W–band PA drain bias network. On the left, an idealized circuit is shown where a 1 nH inductor serves as the RF choke. Planar inductors are well above self-resonance at millimeter-wave frequencies, and therefore not practical. A bias line with integrated stabilization, shown in the center schematic, uses a transmission line and shunt capacitor tuned to resonate at low frequencies where the gain is high. At resonance, the shunt capacitor has a high reflection coefficient, improving stability. Such resonant capacitor–transmission line networks are effective at millimeter-wave frequencies compared to longer, narrower-band quarter-wave lines [106]. A shunt RC network is also placed near the bias pad (port 3) to damp low-frequency oscillations. The final iteration, Fig. 5.4 (right), incorporates the EM-simulated matching network with off-chip stability components: a 10 nF capacitor and 2.7 Ω series resistor to ground. These are internal to a 10-contact dc probe that is used to bias the entire PA from one side of the die, thus removing the need for bondwires in the final dc biasing structure.

The resulting simulated performance is shown in Fig. 5.5, plotting the magnitude of the S-parameters and G_{max} of a $6 \times 50\,\mu$m HEMT. Dotted, dashed, and solid traces correspond to the ideal inductor, shunt capacitor and a decoupling RC bias network, and final structure with external bypass capacitors, respectively. The solid red G_{max} curve shows the large low-frequency gain below W-band. Because gain begins to roll off

beyond 60 GHz, the bias network must suppress feedback across a very wide frequency range. For example, a small shunt capacitor is tuned to resonate at 56 GHz with some bandwidth extending into the operating band to counteract this excess gain. External bypass capacitors improve low-frequency isolation to >27 dB. In all cases, minimizing insertion loss between ports 1 and 2 in the operating band remains essential.

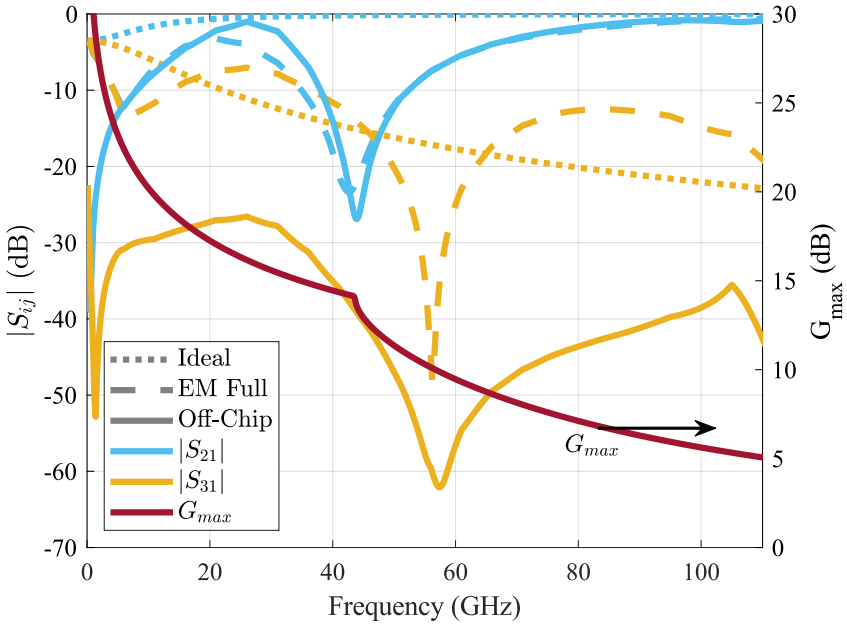


Figure 5.5: Simulated S-parameters and maximum gain of a $6 \times 50\,\mu$m HEMT at 150 mA/mm and +12 V demonstrate performance changes across the three iterations.

The PA implements reactive power combining, which assumes even-mode operation with equal voltages across transistors. Symmetry in MMIC layout helps maintain this condition [4], but device variations (I_{ds}, g_m) and passive coupling can create impedance mismatches that excite odd-mode oscillations. These are mitigated using odd-mode stability resistors (typically 10–50 Ω [26], lower on the gate side), placed symmetrically between gates and drains. When symmetry is maintained, odd-mode resistors have minimal RF impact as no current flows through them. Gate bias stability is further improved with small thin-film series resistors ($\approx 5\,\Omega$). A layout of the last-stage gate, drain, and odd-mode stabilization networks is shown in Fig. 5.6.

PA stability is analyzed using multiple techniques. While the k–factor offers a convenient first check, it is insufficient for multistage amplifiers. However, a value of $k < 1$ can strongly indicate that the PA is not

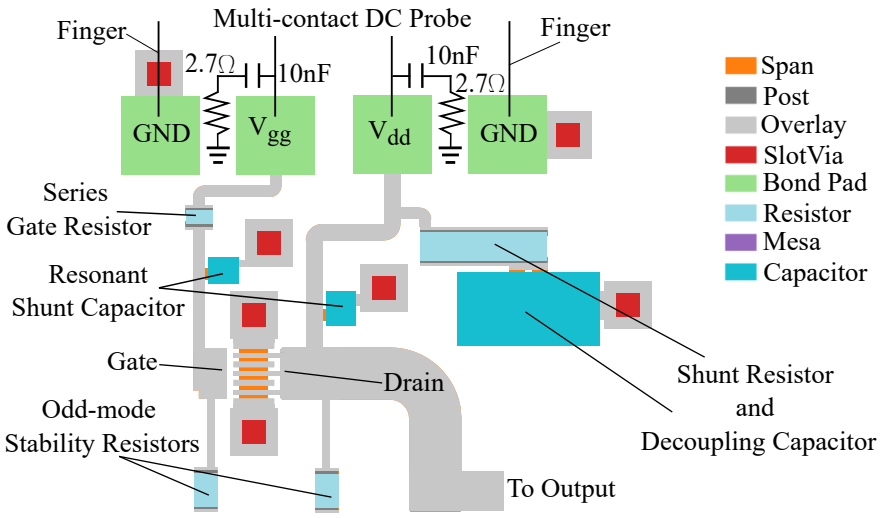


Figure 5.6: Layout of gate, drain, and odd–mode stability techniques. Odd–mode resistors are placed symmetrically between gates and drains of parallel transistors to suppress odd–mode oscillations, while small series resistors on the gate bias lines improve stability without affecting efficiency. The drain bias line includes shunt capacitor resonant structures, decoupling capacitor/resistor networks, and large off-chip bypass capacitors, to ensure operation across the band.

unconditionally stable and must be further examined. A more reliable method for multistage designs is the Nyquist stability criterion, which accounts for interstage feedback. Here, the open-loop gain function G is extracted at the gate and drain of each device and plotted on the polar plane. Stability requires that G not encircle the -1 point in the clockwise direction. In simulation, G is obtained by inserting Γ–probe devices at the gate and drain reference planes to capture internal reflection coefficients, and the closed-loop response is evaluated across frequency. A sweep up to the third harmonic (270 GHz) covers all possible instability regions. The trajectories for each stage are plotted together in Fig. 5.7, with the critical $(-1, 0)$ point marked by a red "x." Under 50 Ω terminations, the PA satisfies the small-signal Nyquist stability criterion.

To ensure robust operation, stability is further evaluated under parameter and load variations. The input and output port impedances are swept over the full reflection coefficient space ($|\Gamma|$ = 0–0.99, $\angle\Gamma$ = 0°–360°). At the device level, worst-case process variations are applied: g_m by ±30 %, C_{gs} by ∓30 %, C_{gd} by ±30 %, and SiN thickness by ±10 % [4, 24]. Nonlinear Nyquist analysis is also performed against input power, complementing the small-signal results and confirming stability across the operating range.

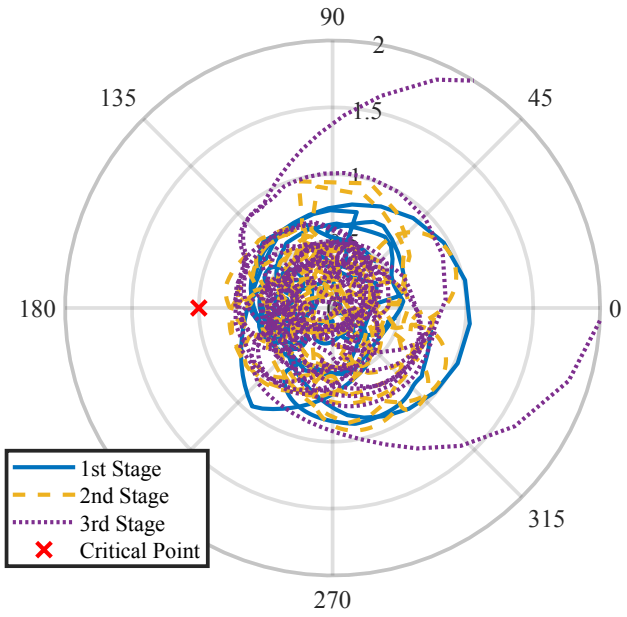


Figure 5.7: Simulated linear Nyquist plot for three stage power amplifier. Nyquist stability loops plotted to show no encirculation of the critical point (-1,0), marked by a red '×' occurs, indicating a stable PA. Simulated from 0.1 GHz to 270 GHz, the third harmonic of the PA design.

5.2.2 Simulated PA Performance

The PA layout, designed for a fixed 50 Ω system impedance, is shown in Fig. 5.8. The matching networks employ the minimum number of components to reduce conductive loss, since wideband operation is not a design objective. The input network and interstage are optimized for maximizing P_{out} and PAE, at the expense of return loss. SiN capacitors with external slot vias are used for dc blocking and bypassing.

Simulated performance for the stabilized PA for a fixed 50 Ω termination is plotted in Fig. 5.9. The P_{out}, PAE, and large signal gain are plotted for P_{in} = 12 dBm, 15 dBm, and 18 dBm. The PA demonstrates best performance at P_{in} = 18 dBm, f_0 = 83 GHz, with P_{out} = 28 dBm, PAE = 15 %, and G = 10 dB. Other input power curves are shown for completeness.

The driveup curves at 78, 83, and 86 GHz are shown in Fig. 5.10. The 3 dB gain bandwidth is from 75.7–90.6 GHz, a fractional bandwidth (FBW) of about 18 %. The P_{3dB} values for P_{out}, PAE, and gain meet the design specification design goals from Table 5.1, with the bandwidth slightly below the 20 % target.

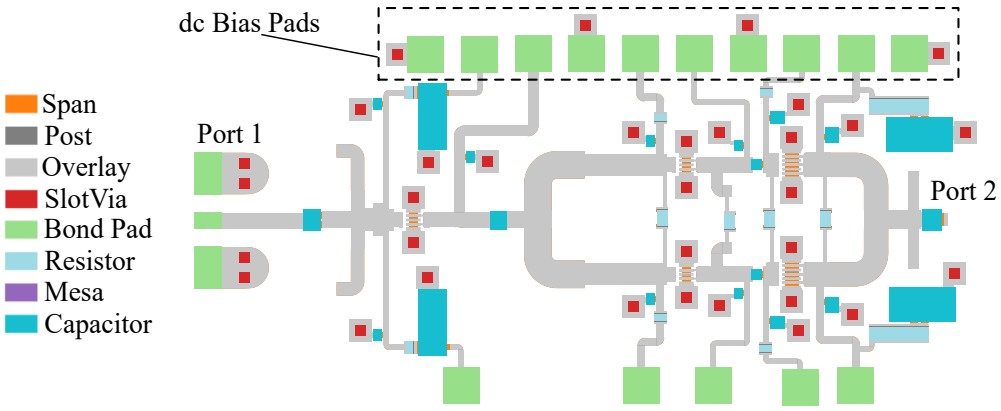


Figure 5.8: Deconstructed layout of a three-stage MMIC power amplifier designed for a fixed 50 Ω environment with some of the corresponding layers shown in legend. The dc bias pads are outlined in dashed lines. The staging ratio is 1:2:4 and the peripheries for stages 1, 2, and 3, are 150 μm, 300 μm, and 600 μm, respectively. The die area is 2.2 mm by 1.1 mm.

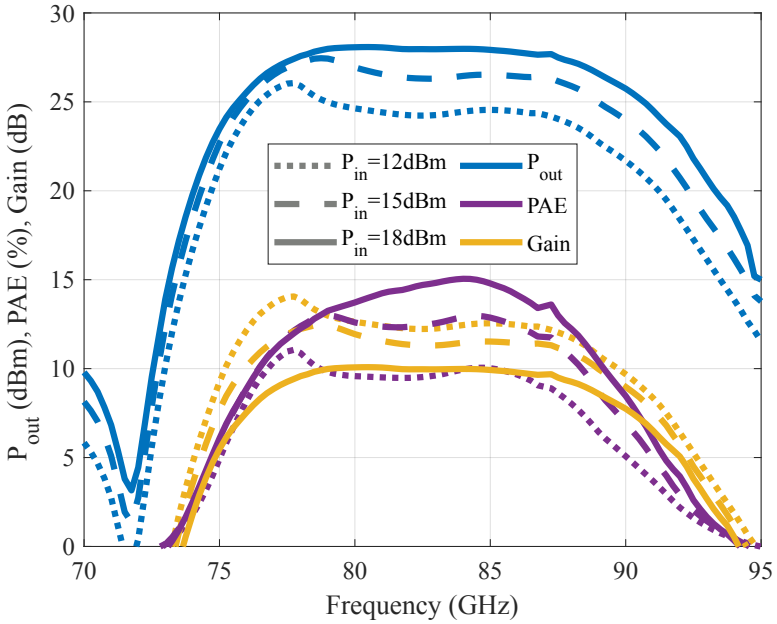


Figure 5.9: Simulated driveup curves for PA with fixed 50 Ω termination. P_{out}), PAE and large-signal gain are plotted versus input power at 78 (dotted), 83 (dashed), and 86 GHz (solid).

5.2.3 Effects of Load Variation

The PA is designed for a 50 Ω termination, but when driving an antenna array element, coupling that varies with scan angle affects this load impedance. Load variations are analyzed using a simplified model with

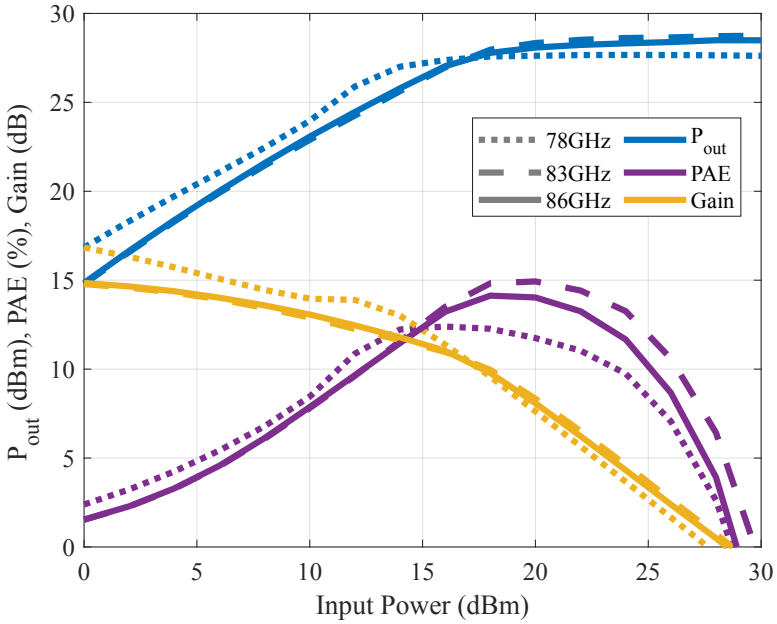


Figure 5.10: Simulated driveup curves for fixed 50 Ω PA output power (P_{out}), power–added efficiency (PAE), and large-signal gain are plotted versus input power at 78 (dotted), 83 (dashed), and 86 GHz (solid).

an ideal tuner, rather than more complex equivalent models [83, 107–109]. Simulated active reflection coefficients in prior work result in VSWR < 2.5 [110], but can also be higher [111], depending on feed and scan requirements.

The W-band PA performance boundaries are evaluated by sweeping the tuner reflection coefficient from $|\Gamma| = 0$ to 0.43 and $\angle\Gamma = 0°$–$360°$ (VSWR < 2.5). Figure 5.11 shows the resulting PAE difference at 78 GHz (left) and 86 GHz (right), with VSWR circles of 1.5, 2, and 2.5 indicated by dashed lines. The simulated results show that the PAE is lower compared to the 50 Ω case for most phases. However, a few outer-edge angles yield higher PAE because the mismatched load partially aligns with the optimum large-signal load impedance, effectively providing beneficial output-matching conditions. These instances are incidental rather than systematic. The next section investigates a reconfigurable matching network that can be integrated directly into the PA OMN to intentionally recover some performance due to load variation.

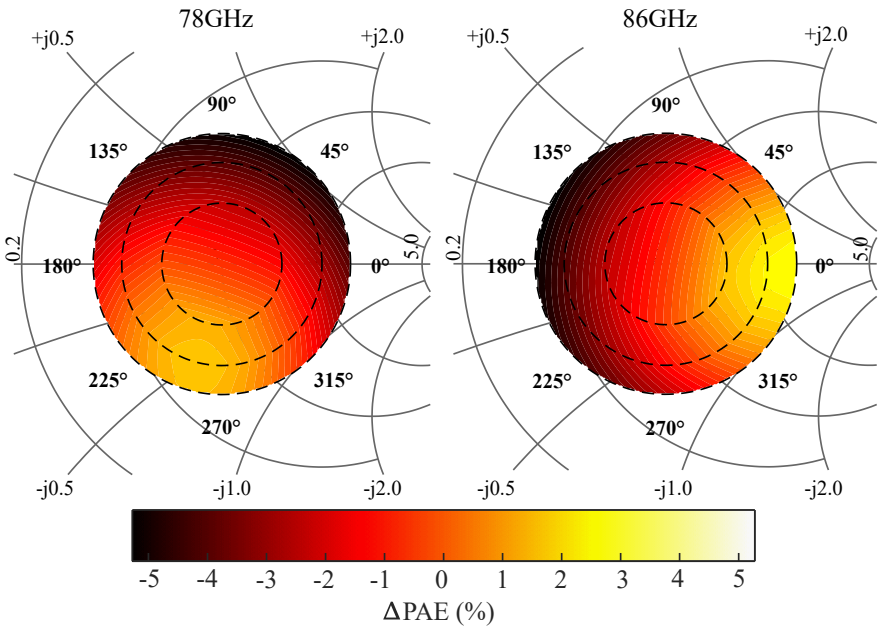


Figure 5.11: Simulated power amplifier PAE difference (ΔPAE, %) at 78 GHz (left) and 86 GHz (right) for tuner reflection coefficients swept from $|\Gamma|$ = 0 to 0.43 and $\angle\Gamma$ = 0°–360°. Both Smith charts are slightly zoomed to emphasize the regions of interest. VSWR circles of 1.5, 2, and 2.5 are indicated by dashed lines.

5.3 Reconfigurable Matching Network

The goal of the reconfigurable matching network (RMN) is to adjust the PA load matching network when the load varies. Since varactors are unavailable in the T3 process, a "cold HEMT" shunt device is used as the control element, as in the millimeter-wave switches in [98–104]. Figure 5.12 shows the shunt HEMT in relation to the main RF signal path in the top left and a small-signal equivalent circuit model with the main design parameters highlighted in blue ($C_{ds}, C_{gs}, C_{gd}, R_{ds}, L_d, L_s$).

In this topology, the un-biased drain terminal is connected to the main RF path, the source is grounded, and the gate–source dc voltage (V_c) is applied through a large, high-resistivity epitaxial resistor ($\approx$ 1 kΩ) which is used to isolate the gate bias circuitry. Depending on V_c, the device can operate in two bias states, referred to here as the "pinched–off" state and the "conduction" state to avoid confusion with the *on/off* terminology commonly used in switch literature with the same shunt HEMT topology. In the "pinched–off" state ($-6\,\text{V} \leq V_c < -0.5\,\text{V}$), the device behaves as a shunt capacitance , consisting of C_{gs} and C_{gd} which vary with V_c, combined with the relatively constant C_{ds} set largely by device geometry [100]. In this state,

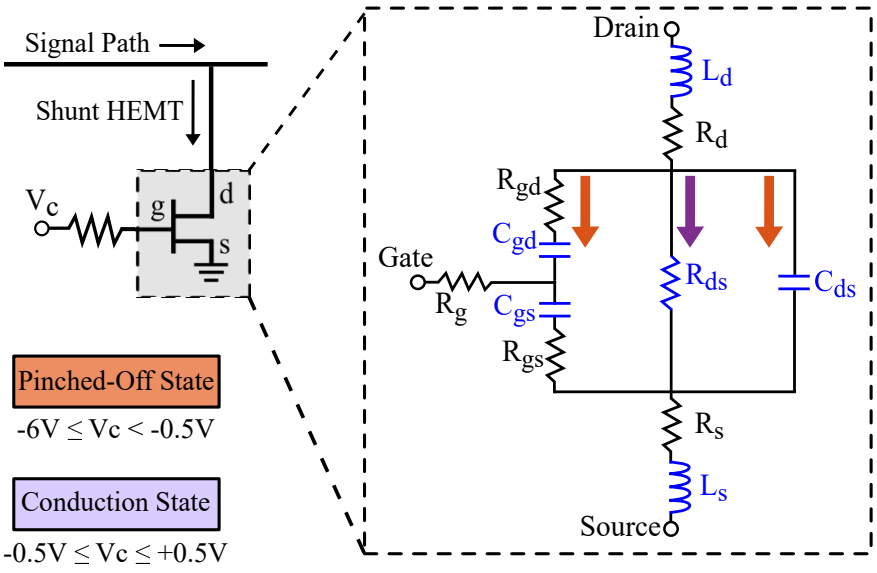


Figure 5.12: Small-signal equivalent circuit of shunt "cold HEMT" used as a variable impedance stub incorporated into the PA output matching network. The key circuit elements are outlined in blue (C_{ds}, $C_{gs}, C_{gd}, R_{ds}, L_d, L_s$).

R_{ds}, associated with the depletion region under the gate, is very large. Equivalent circuit relationships for capacitance and resistance in this state are given in [100]. The orange arrows in Fig. 5.12 illustrate the RF path for this state.

In the "conduction" state ($-0.5\,\text{V} \leq V_c \leq +0.5\,\text{V}$), the channel depletion region is partially to fully open, reducing R_{ds} dramatically. The device behaves predominantly as a resistance and inductance to ground through L_s and L_d, with the drain fingers, source contact, and via to ground dominating the impedance. The purple arrow in Fig. 5.12 shows the RF path in this state. The effects of any additional parasitics are minor.

5.3.1 Device Size Comparison

To investigate the dependence of the equivalent circuit on device size, the input impedance of four available devices ($2\times25\,\mu$m, $4\times37.5\,\mu$m, $6\times50\,\mu$m, and $12\times50\,\mu$m) is simulated. The resulting drain impedances are plotted on a Smith chart in Fig. 5.13 at 75, 83, and 90 GHz while sweeping V_c from –6 V to +0.5 V in 0.25 V steps. In deep pinch-off (V_c =-6 V), all devices are primarily capacitive, appearing at the lower edge of the Smith chart. As V_c increases, the gate–channel capacitance also increases, reducing the reactance. Near a -0.5 V bias, the channel opens, R_{ds} decreases significantly, and inductive effects from the drain/source

fingers, contacts, and vias to ground begin to dominante. Interestingly, at 0 V, the impedance crosses the real axis for all four devices.

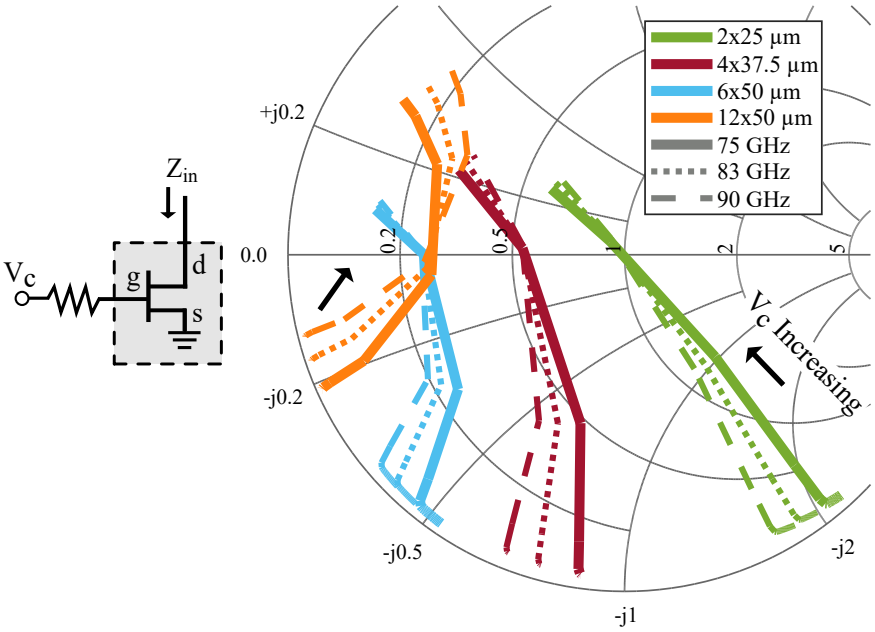


Figure 5.13: Smith chart showing the drain impedance of four HEMT device sizes as the gate bias is swept from −6 V to +0.5 V in 0.25 V steps at 75, 83, and 90 GHz.

Figure 5.14 compares the capacitance of four device sizes modeled as a parallel RC circuit. Results at 75, 83, and 90 GHz are shown for V_c from -2 to +0.5 V, since little variation occurs in pinch-off. When $V_c \geq -0.5$ V (conduction region), inductive effects begin to dominate, producing negative values for the extracted parallel capacitance.

Figure 5.15 plots the corresponding parallel resistance governed by R_{ds}, which remains large while the depletion region exists, then decreases as the channel opens, the device becomes less capacitive and inductive effects emerge for $V_c \geq -0.5$ V.

Integrating the devices into the PA output matching network requires a trade-off in tunable range and insertion loss. Devices with larger peripheries exhibit greater capacitances, while wider gates yield a smaller channel resistance [112]. The smallest device ($2 \times 25\ \mu$m) therefore has the lowest intrinsic capacitance and highest channel resistance. Figure 5.16 compares the simulated $|S_{21}|$ of the four devices. In the "pinched–off" state, the $2 \times 25\ \mu$m device exhibits the smallest $|S_{21}|$, dominated by the tunable capacitances C_{gd} and C_{gs},

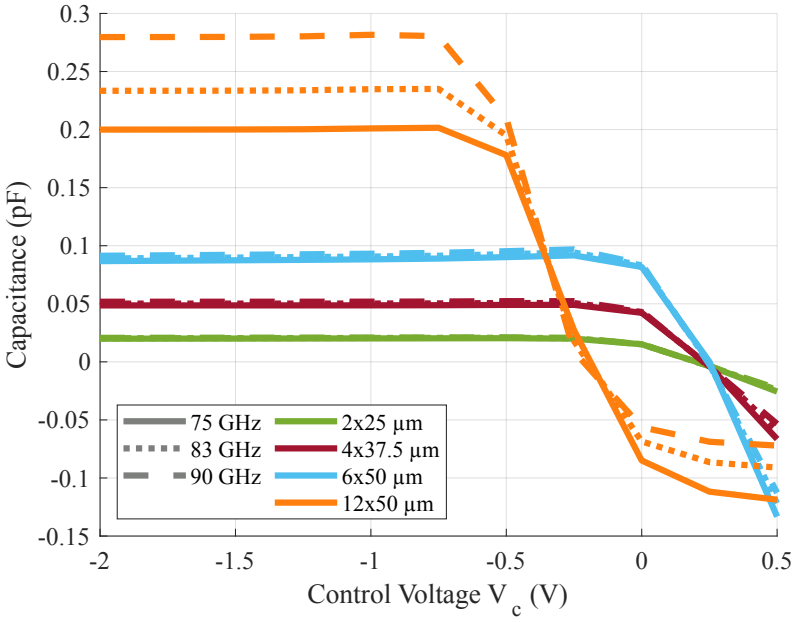


Figure 5.14: Comparison of equivalent circuit values for four device sizes looking into the drain for the capacitance extracted from a parallel-RC model. Results are shown at 83 GHz across V_c from –2 to +0.5 V, since little variation occurs between –6 and –2 V when the device is pinched off.

while its high R_{ds} makes it appear closest to an open circuit in the RF path. The largest device shows the opposite behavior, with the lowest R_{ds} and largest capacitance. In the "conduction" state, inductive effects dominate, R_{ds} decreases sharply, and more RF power is coupled, increasing insertion loss.

A practical compromise is provided by the $4 \times 37.5\ \mu$m device, which has a parallel shunt capacitance of about 0.05 pF when pinched-off and approximately 1 dB insertion loss in that region. When the tunable bias range is fully used, additional matching is required to reduce insertion loss in the "conduction" state.

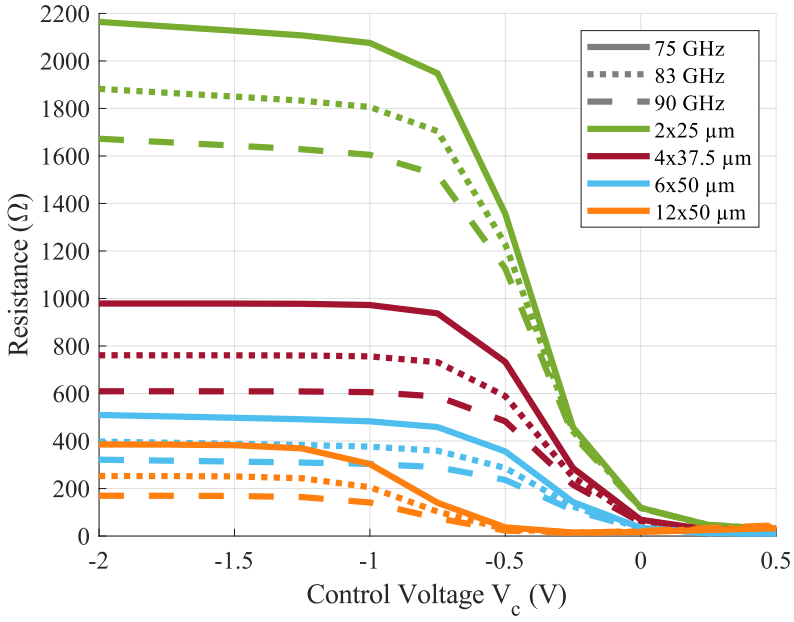


Figure 5.15: Comparison of equivalent circuit values for four device sizes looking into the drain for the resistance extracted from a parallel-RC model. Results are shown at 83 GHz across V_c from –2 to +0.5 V, since little variation occurs between –6 and –2 V when the device is pinched off.

5.3.2 Reconfigurable Matching Element

A single reconfigurable matching element (RME) employing a $4 \times 37.5\,\mu$m device with supporting transmission lines is shown in Fig. 5.17. The left side of the figure presents a circuit schematic with characteristic impedance and electrical length at 77 GHz, while the right side shows a layout identifying each section's role. Starting from the dc bias pad on the bottom, a short microstrip line connects to a 1.6 kΩ resistor that isolates the gate and dc bias circuitry from the RF path, preventing increase in loss. The resistor is directly connected to the transistor gate. On the drain side, a short microstrip segment offsets the device source vias from the main RF path, reducing undesired coupling [99]. An additional benefit of using the $4 \times 37.5\,\mu$m device in this configuration is that the drain manifold width is 44 μm, almost equal to the width of a 50 Ω microstrip line, which allows straightforward impedance matching and phase adjustment.

A shorted via near the transistor is also included, a common technique used to compensate device capacitance in millimeter-wave switches [101–103]. The focus here is to demonstrate limited reconfigurability while minimizing loss in the PA OMN. Alternative designs can be done to add more tunable range at the

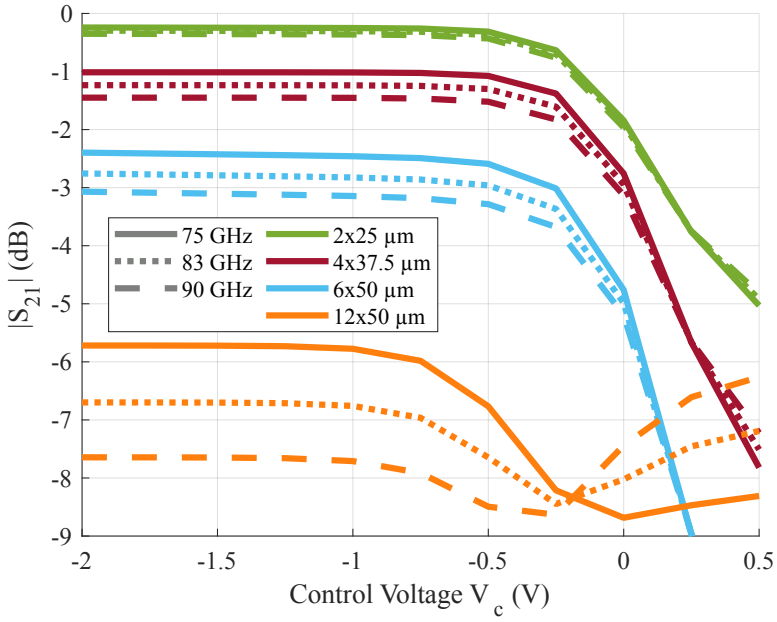


Figure 5.16: Comparison of the $|S_{21}|$ of four device sizes when the drain of the shunt HEMT is connected to the main 50-Ω signal path. Results are shown at 75, 83, and 90 GHz across gate bias V_c from -2 to 0.5 V, since little variation occurs between -6 V and -2 V when the device is pinched off.

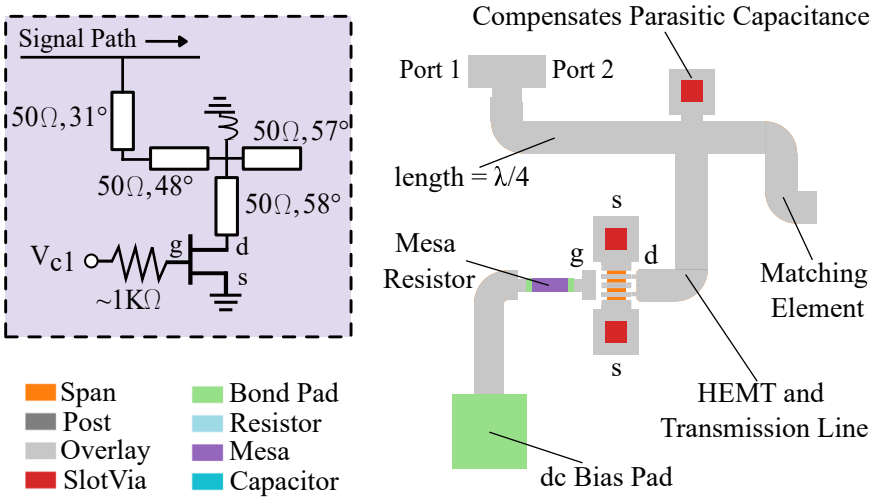


Figure 5.17: Single reconfigurable matching element (RME): circuit schematic with impedance values and electrical lengths referenced at 77 GHz (left); and physical layout, 0.49 mm × 0.58 mm in size, divided into sections corresponding to their roles in the circuit (right). A layout legend is included in the bottom left.

expense of loss. A quarter-wave line transforms the stub–transistor network to appear as an open circuit. This is an acceptable narrowband method for the presented design (≈ 18% FBW). Thus, the RME presents a low-loss open circuit to the RF path while still enabling some reconfiguration through V_c. An additional

transmission line, added in later integration with the PA OMN, widens the tuning range.

The input impedance of the RME is shown on the Smith chart in Fig. 5.18, with V_c swept from –6 to +0.5 V in 0.25 V steps and markers at –6 V, 0 V, and +0.5 V. Each color corresponds to a design stage as explained in the figure caption.

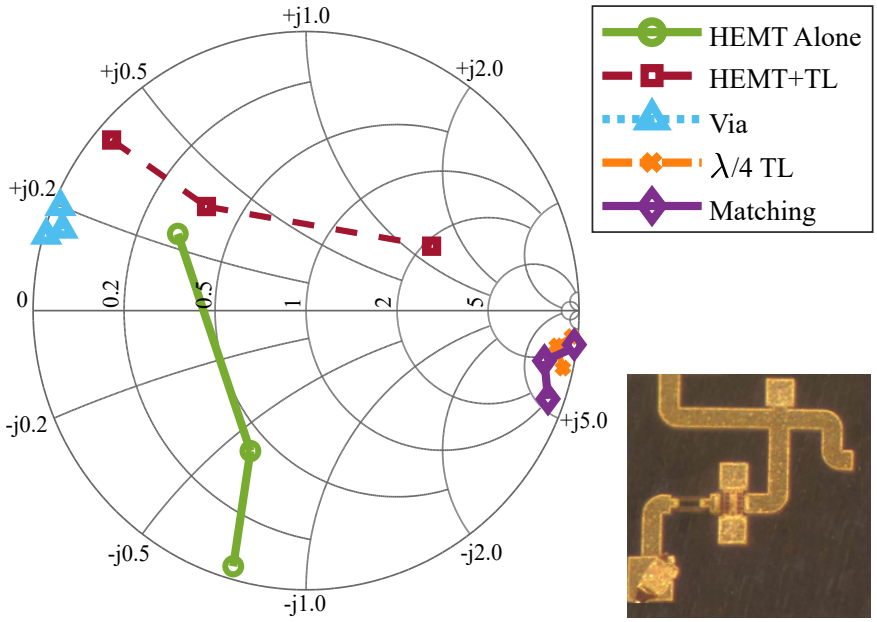


Figure 5.18: Simulated input impedance of a single RME is shown for each design stage: the solid green trace with circles shows the device and dc bias path tuning range only; the red dashed line trace with squares introduces additional phase with a microstrip transmission line; the blue dotted trace with triangles demonstrates the short-circuit response after the shorted stub via; the smallest orange trace with 'x's' shows the impedance after the quarter-wave transformation; and the purple solid trace with diamonds shows the final impedance after adding the matching line. Each curve corresponds to the impedance trajectory across the tuning range at the center frequency of 83 GHz. Markers on each curve denote bias conditions of V_c =-6 V, 0 V, and 0.5 V. The bottom right shows an image of the fabricated RME.

Figure 5.19 shows the magnitude of S-parameters from 70–95 GHz for three discrete bias states (V_c = -6, 0, +0.5 V) of the full-wave simulated RME structure. The left y-axis plots $|S_{11}|$ in blue, with solid, dashed, and dotted lines representing each bias state. The right y-axis plots $|S_{21}|$ in yellow, demonstrating minimal insertion loss (< 0.75 dB) across the fixed 50 Ω PA design band. One additional consideration is ensuring that the devices can handle the input power from the PA output. Results from [113] show that a similar switch in the same GaN process handles 1 W at the output of a large PA around 80 GHz. The HEMTs do not show signs of compression or turn-on up to the expected maximum output power of the simulated fixed

50 Ω PA, approximately 28–29 dBm.

The final reconfigurable matching network design balances insertion loss and tuning range by including two RMEs with interconnecting microstrip transmission line sections to enable a manufacturable layout, shown in Fig. 5.20. The top half presents the circuit schematic with characteristic impedances and electrical lengths at 77 GHz, while the bottom half shows the physical layout with deconstructed labels listed in the lower right corner.

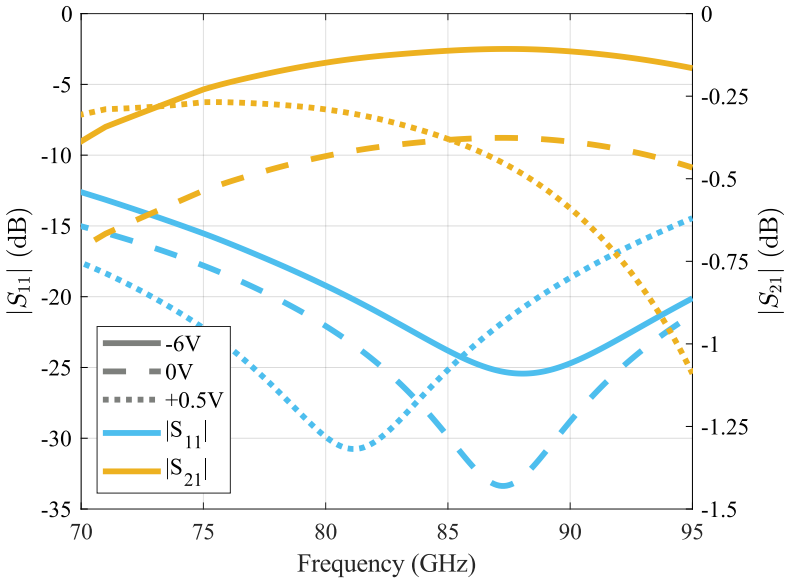


Figure 5.19: Simulated magnitude of S-parameters for reconfigurable matching element across bias states $V_c = -6\,\text{V}$, $0\,\text{V}$, and $+0.5\,\text{V}$. The left axis shows the input reflection coefficient magnitude, $|S_{11}|$, and the right axis shows $|S_{21}|$, both as a function of frequency.

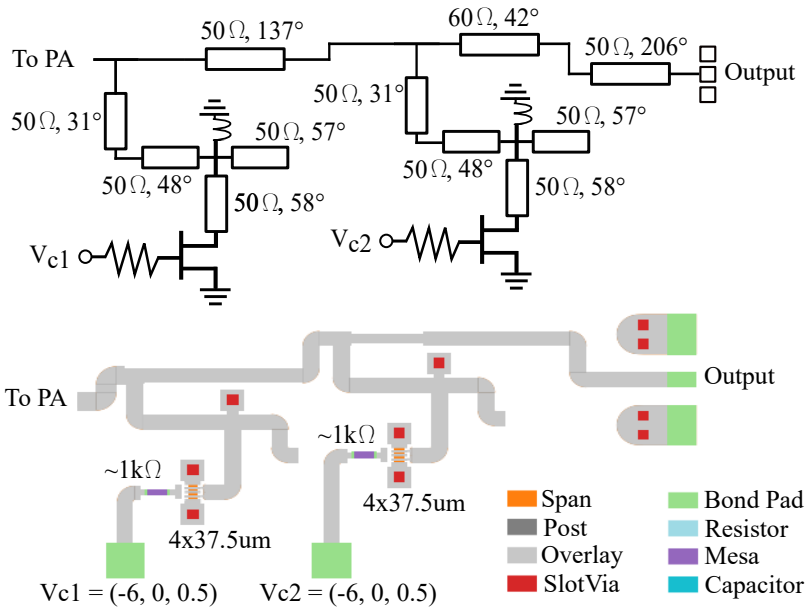


Figure 5.20: Top: Reconfigurable matching network circuit schematic with characteristic impedance and electrical lengths at 77 GHz. Bottom: MMIC layout with layers outlined in color. The capacitance of the shunt HEMTs is controlled by the bias voltages V_{c1} and V_{c2} between primarily three points, −6 V, 0 V, and +0.5 V.

5.3.3 PA with Reconfigurable Matching Network

The final PA layout with the integrated RMN is shown in Fig. **??**, with an overall die size of 3.7 mm × 1.1 mm. The matching networks employ the minimum number of components to reduce conductive loss. The input and interstage networks maximize P_{out} and PAE, at the expense of return loss. SiN capacitors with external slot vias are used for dc blocking and bypassing.

The RMN is inserted at the output of the fixed 50 Ω matching network and co-simulated with the PA to capture layout parasitics and ensure stability. Adjustments in the design are then performed to maximize PAE under mismatched load conditions. The final implementation leverages the near open-circuit impedance of the RMEs, together with additional microstrip lines, to transform the impedance back to 50 Ω at the GSG output pad. While this configuration is not intended to cover a broad range of load impedances, it provides a realizable baseline design that demonstrates the feasibility of integrating RMNs with PAs at millimeter-wave frequencies.

For comparison, the performance of the fixed OMN PA and the RMN PA stages are biased at 150 mA/mm and the drain voltage at +12 V at all stages, with an input power of 16 dBm. The output load is swept by

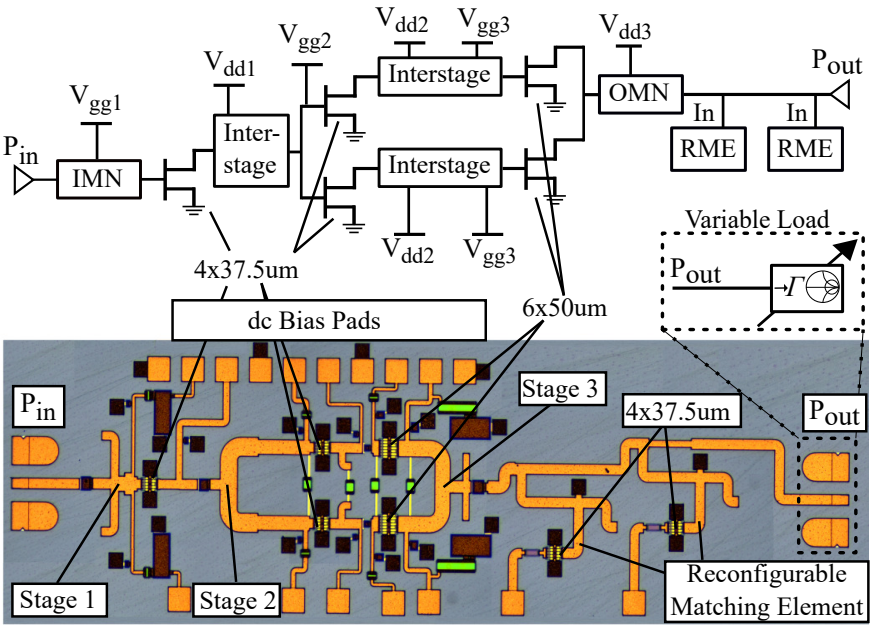


Figure 5.21: Schematic and image of a reconfigurable W-band power amplifier. The reconfigurable matching network is integrated in the output matching and combining network of the power amplifier to cover a range of output load impedances.

varying the reflection coefficient magnitude, $|\Gamma|$, from 0 to 0.8 and the phase, $\angle\Gamma$, from 0° to 360°. Figure 5.22 presents the simulated difference in PAE between the fixed 50 Ω PA and the RMN PA at 83 GHz as the load is varied on the Smith chart. The light orange-to-yellow contours indicate the positive increase in PAE achieved by the RMN PA relative to the fixed matching network PA, expressed in percentage points (pp). The black dot-and-dashed line in the center shows the 0 % contour line where there is no improvement in PAE. To generate these results, the control voltages V_{c1} and V_{c2} were swept from −6 V to +0.5 V, and the best-performing RMN configuration was compared against the fixed OMN PA at that given load.

At the nominal 50 Ω load, the fixed OMN PA achieves higher efficiency since it does not include the additional insertion loss of the RMN. However, as the load deviates from 50 Ω, the RMN PA shows improvement, particularly over selected angles. An improvement of at least 3 pp in PAE is observed for $\angle\Gamma$ spanning +80° to +200° and $|\Gamma|$ values between 0.2 and 0.7. These improvement regions are frequency-dependent and shift with operating frequency, but the trend of enhanced efficiency under mismatched loads remains consistent.

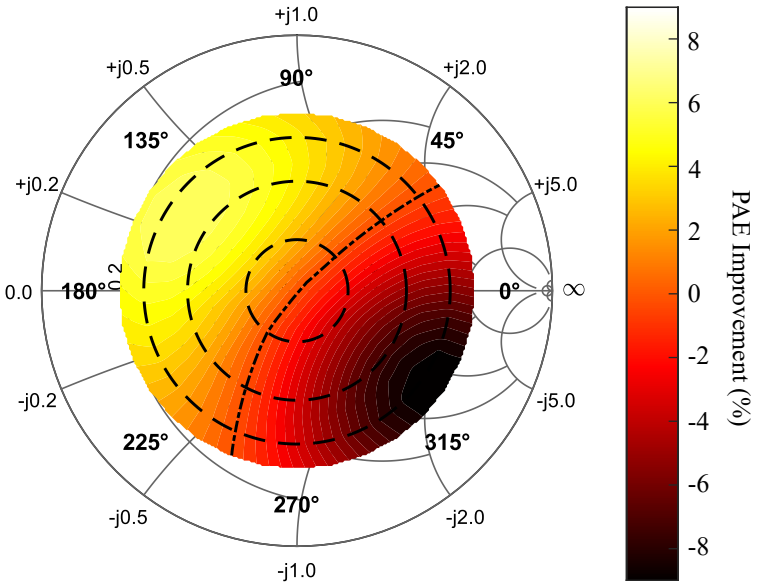


Figure 5.22: Simulated PAE difference between a fixed-load and RMN PA at 83 GHz with $P_{\text{in}} = 16$ dBm. The load reflection coefficient Γ is swept in magnitude from 0 to 0.8 and angle from 0° to 360°, with interpolation used for clarity. The color scale indicates the percentage-point PAE improvement of the RMN PA relative to the fixed-load PA. Dashed circles mark VSWR values of 1.5, 2.5, and 4. The black dot-and-dashed line shows the 0 % contour line where there is no improvement in PAE; orange to yellow corresponds to positive PAE improvement using the RMN PA.

5.4 Experimental Results

The full reconfigurable PA is characterized in small-signal operation, showing an insignificant simulation-to-measurement discrepancy. An investigation starting with characterization of a number of chips fabricated on two different wafers (Wafer 1 and Wafer 2) is performed. An analysis of a separately fabricated reconfigurable test structure, as well as transistor equivalent circuit parameter extraction are used to identify possible reasons for the discrepancy. Large-signal measurements are also performed and analyzed.

5.4.1 Small Signal

Small-signal measurements of the PA are performed on-wafer using an HP8510C network analyzer with millimeter-wave extender heads covering V-band (50–75 GHz) and W-band (75–110 GHz) separately. On-wafer short-open-load-thru (SOLT) calibration using 100 μm GSG probes on a W-band impedance standard substrate (ISS) from Cascade Microtech is done for both frequency bands. The die is mounted on a copper–molybdenum (CuMo) carrier, and the HEMTs are biased through a 10-contact dc probe (six power

and four ground). Each power contact incorporates an internal RC network to ground for stability. RMN control voltages and interstage bias are supplied via tungsten-tip dc probes, connected to off-chip 1000 pF single-layer stability capacitors. These capacitors are wire-bonded to the on-chip dc pads using 1-mil gold bondwires.

Fig. 5.23 shows a photograph of the PA during probing. Figure 5.24 plots the simulated S-parameter magnitude data in dotted lines and the measured results in solid lines from 50–95 GHz. The simulations predict $|S_{21}| \geq 10$ dB from 75 GHz–90 GHz while measurements show $|S_{21}| \geq 10$ dB from 73.25 GHz–83.25 GHz. This behavior was found by measuring an additional three chips included with this wafer, clearly a large simulation to measurement discrepancy is present and the topic of investigation next.

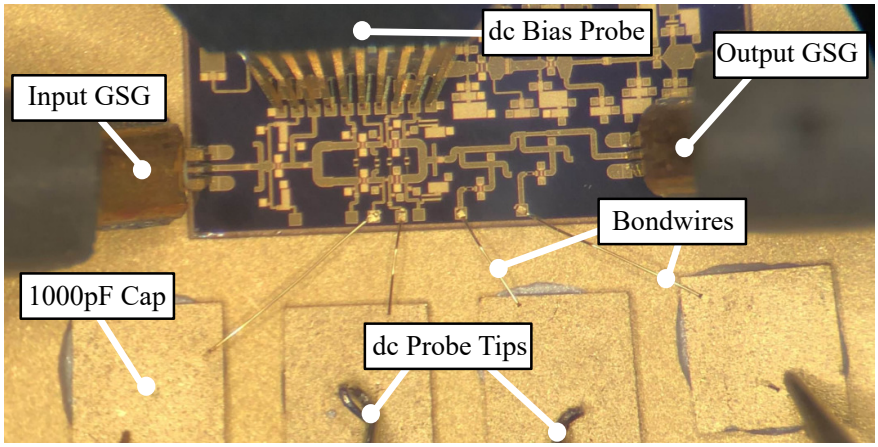


Figure 5.23: Photograph of on-chip probing of MMIC power amplifier. The dc bias probes provide drain, gate and control voltages. Off-chip single layer capacitors are bonded for additional stability.

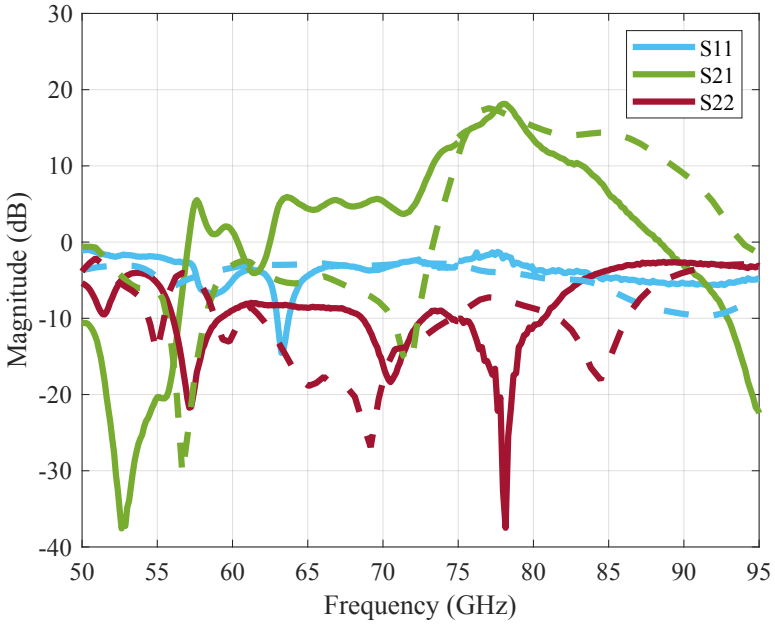


Figure 5.24: Small-signal simulated (dotted) and measured (solid) S-parameters from 50–95 GHz. The PA is designed to maximize output power and efficiency so the input match is not optimal for return loss.

5.4.2 Discrepancy Analysis

The simulated (dotted) and measured (solid for Wafer 1, dashed for Wafer 2) small-signal S-parameters are shown in Fig. 5.25 over 75–110 GHz. The PA stages are biased at 150 mA/mm with a drain voltage of +12 V. Note that the design prioritizes output performance, so the input return loss is low. To determine whether this behavior is wafer-specific, eight additional chips are characterized: four from Wafer 1 and four from Wafer 2, which show different f_t and breakdown voltages per foundry data. All eight chips are measured from 75–110 GHz. The results indicate consistent trends within each wafer. Therefore, the simulation to measurement discrepancy is systematic, rather than limited to a single die or wafer.

An initial hypothesis for the reason behind the shift in frequency between the simulated and measured data is that the "cold HEMT" element is not modeled by the nonlinear model in the process design kit (PDK). To examine the impact of the RME and device biasing, a dedicated test structure is implemented. Figure 5.26 shows the simulated (dotted) and measured (solid with triangles) two-port S-parameters from 0.1–65 GHz at V_c = -6 V, with the test-structure layout shown in the bottom left. The GSG pad orientation is rotated to fit

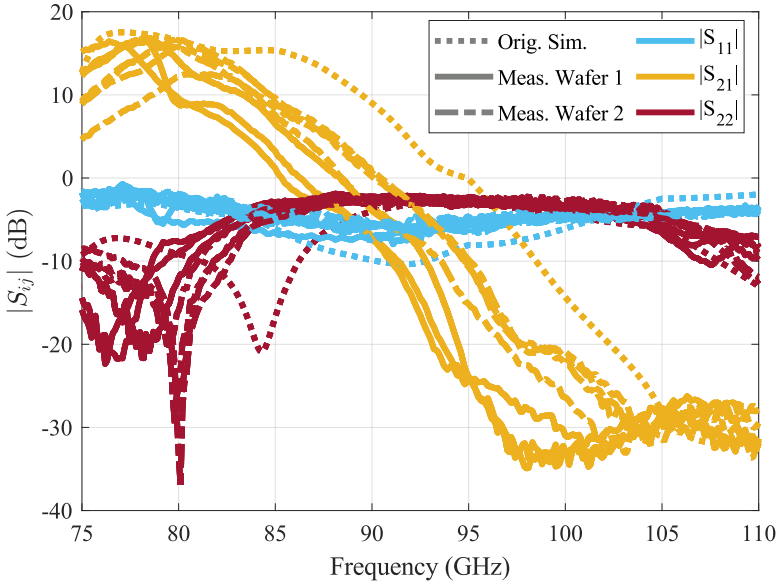


Figure 5.25: Small-signal S-parameters of the PA from 50–110 GHz: simulation (dotted), measurement (solid), and fitted simulation (solid with triangles). The fitted case is based on parameter extraction using equivalently biased HEMTs in simulation and measurement, providing a better agreement.

the reticle space, and the available 90-degree calibration substrate limits reliable two-port measurements to 65 GHz. Within this range, measured and simulated data exhibit good agreement, indicating that the RME is modeled with sufficient accuracy for this work.

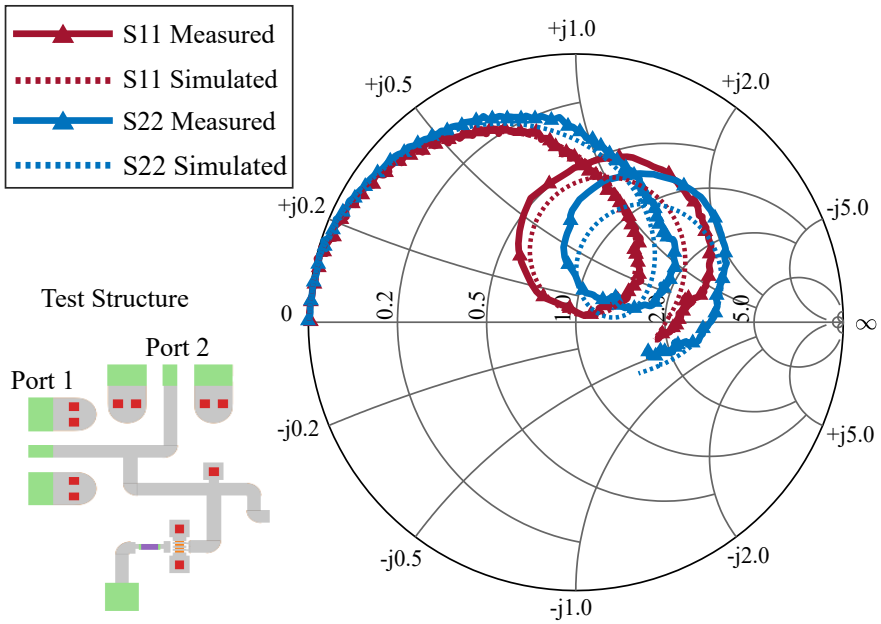


Figure 5.26: The reconfigurable matching element test structure and its simulated (dotted) versus measured (solid with triangles) S-parameters from 0.1–65 GHz. The rotated GSG layout (to fit the reticle) limits measurements to 65 GHz, and is used to verify the models accuracy up to that frequency.

5.4.3 Parameter Extraction

The next analysis step is to extract intrinsic parameters from measured HEMT S-parameters and compare them to the original simulated model. Three S-parameter sets were available for a $4 \times 37.5\,\mu$m device, measured using a multiline thru-reflect-line (mTRL) calibration algorithm [37]. The reference planes were de-embedded close to the intrinsic device plane. Measurements were taken at V_d=6, 10, and 12 V with current densities of 148, 255, and 139 mA/mm, respectively, over 0.1-–67 GHz in 0.15 GHz steps. Simulations mirroring the measurement conditions are compared on a Smith chart for S_{11} and S_{22}, as shown in Fig. 5.27. At $V_d = 12$ V and $J_d = 139$ mA/mm, S_{11} shows good agreement between simulation and measurement, while S_{22} exhibits a clear discrepancy. The bottom left of the figure shows the $4 \times 37.5\,\mu$m HEMT layout with the mTRL reference planes indicated by dashed lines.

The observed discrepancy in S_{22} suggests that some intrinsic device parameters differ from the expected values. To investigate this, the measured and simulated S-parameters are converted to Y-parameters, and intrinsic equivalent-circuit elements (C_{gd}, C_{gs}, C_{ds}, g_m) extracted using standard equations [114, 115]. A

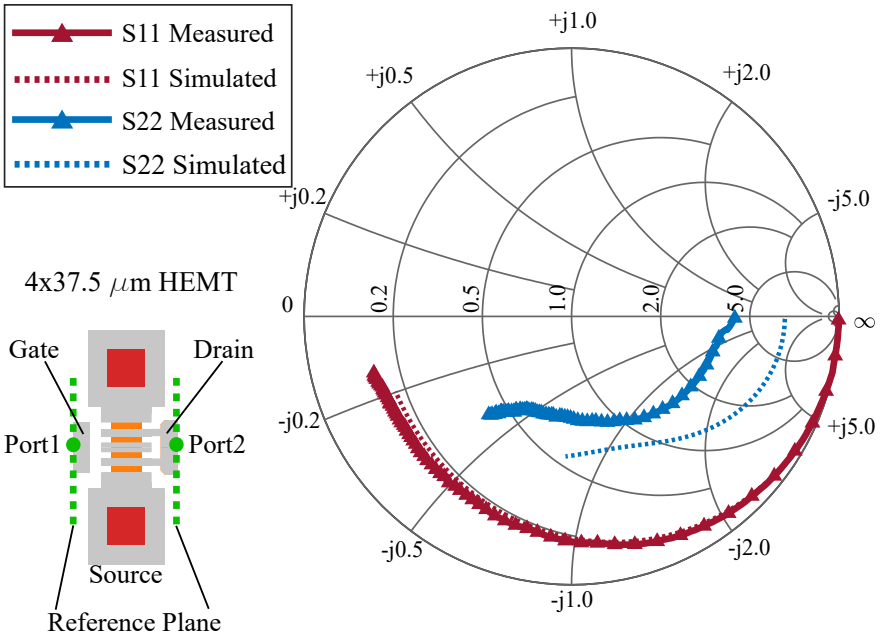


Figure 5.27: Simulated and measured S_{11} and S_{22} for a $4 \times 37.5\,\mu$m device biased at $V_d = 12$ V and $J_d = 139$ mA/mm over 0.1–67 GHz. A $4 \times 37.5\,\mu$m HEMT layout is also shown and dashed lines indicate the reference plane used for S-parameter measurements.

representative "best-fit constant value" for each parameter is computed over a selected frequency range, rather than at a single point, to reduce sensitivity to noise and measurement uncertainty.

Initially, capacitances C_{gd}, C_{gs}, C_{ds} and the g_m are extracted as functions of frequency for the $V_d = 12$ V, $J_d = 139$ mA/mm bias condition. Representative constant values are obtained by averaging across the 3.4–67 GHz band. Both the mean and a 20% trimmed mean (excluding the 10% largest and smallest values) are evaluated to mitigate outliers and account for frequency regions where the lumped model is less valid. While more advanced parameter-extraction methods incorporating comprehensive uncertainty analysis are available, e.g. [116], such techniques are beyond the scope of this work. Given the goal of identifying the key parameters contributing to the simulation–measurement discrepancy, the averaging and trimmed-mean approach described above provides a reasonable and robust first-order comparison.

The extraction results show that the measured "best-fit constant values" for C_{gd}, C_{gs}, C_{ds}, and g_m are 159.8, 902.6, 258.7 fF/mm, and 632.9 mS/mm, respectively, while the simulated values are 81.2, 746.03, 201.9 fF/mm and 539 mS/mm. This corresponds to underestimations in simulation of about 49 %, 17 %, 22 %, and 15 %. These extracted values are then applied to a tunable Angelov-based device model with

exposed parameters to assess whether the updated simulation aligns more closely with measurements. The original small-signal simulations (dotted), measurements (solid), and fitted simulations (solid with triangles), are shown in Fig. 5.28 over 50-–110 GHz.

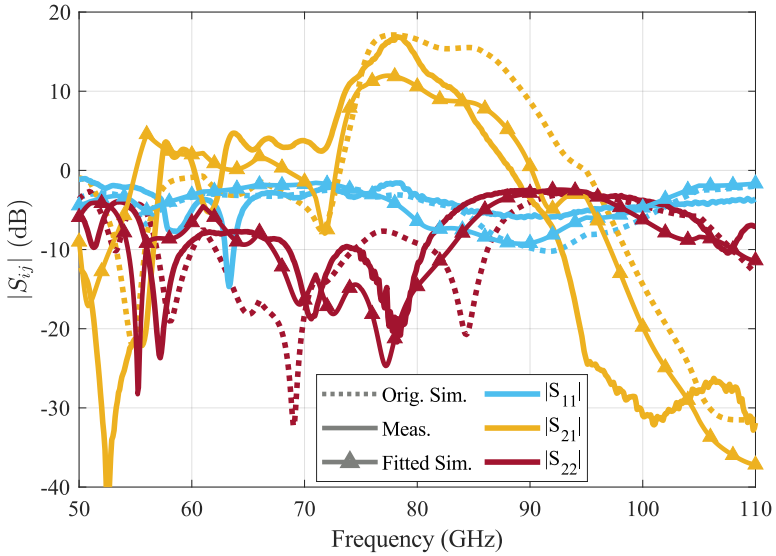


Figure 5.28: Small-signal S-parameters of the PA from 50–110 GHz: simulation (dotted), measurement (solid), and fitted simulation (solid with triangles). The fitted case is based on parameter extraction using equivalently biased HEMTs in simulation and measurement, providing a better agreement.

The updated model reproduces the sharper frequency roll-off observed in the measured $|S_{21}|$ and matches $|S_{22}|$ much closer. While this represents only a first-pass correction, it helps validate the hypothesis that the intrinsic model parameters for the fabricated devices do not match the initial Angelov model and affect the agreement between measurement and simulations used in design.

5.4.4 Large Signal Measurements

Large-signal measurements are performed using the setup shown in Fig. 5.29. An HP83650A source drives a Ka-band amplifier (QPW-18402020-J0), which in turn excites a passive frequency tripler (QPM-93003W) to generate the W-band signal. A bandpass filter (QFL-B4SW00) suppresses unwanted harmonics before the signal is amplified by a W-band driver amplifier (QPI-W01820-H4W0). An isolator is placed at the output of the amplifier for protection, and a 10 dB waveguide coupler safeguards the WR-10 power sensor

(NRP110TWG). The continuous-wave (CW) test signal is then delivered to the device under test (DUT) through several waveguide sections and a 100 μm-pitch WR-10 waveguide GSG probe.

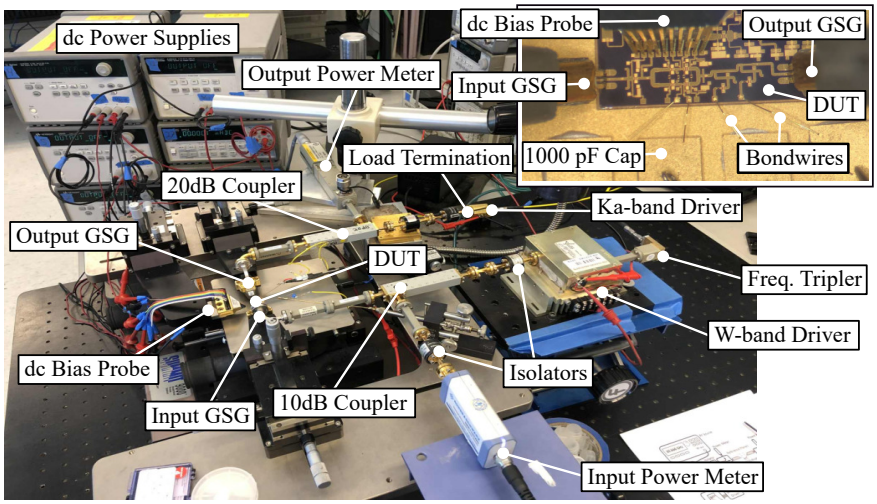


Figure 5.29: Large-signal measurement setup. The main diagram shows the labeled measurement bench, while the inset (top right) provides a close-up photograph of on-chip PA probing. The required frequency up-conversion and amplification stages to deliver a maximum of 10–11 dB input power at the DUT plane are included.

At the output, the DUT signal is coupled to a second WR-10 power sensor using a 20 dB coupler, with the through path terminated in a matched WR-10 load. Passive losses are calibrated out via a three-step power calibration procedure, de-embedding the input chain, output chain, and probe losses to reference the measurements as close as possible to the MMIC plane. The available input drive power in this setup is limited to approximately 10–11 dBm at the DUT reference plane across the frequency range.

The large-signal measurements are shown together with the fitted model simulation in Fig. 5.30. The measured data are taken from one well-performing chip, with V_{c1} and V_{c2} iterated across all combinations of -6 V, 0 V, and +0.5 V. The shaded region indicates the measured data range, while the upper bound ($V_{c1} = 0$ V, $V_{c2} = -6$ V) and lower bound ($V_{c1} = -6$ V, $V_{c2} = +0.5$ V) are highlighted with solid and dash-dotted lines, respectively. The fitted simulation ($V_{c1} = -6$ V, $V_{c2} = -6$ V), extracted from the small-signal analysis, is also included (solid with triangles) at an input power of 11 dBm. In practice, not every measured condition could reach P_{in} =11 dBm due to frequency limitations of the W-band drive chain, whereas the simulations are fixed at 11 dBm. All stages and devices are biased at +12 V with $J_d \approx 150$ mA/mm, though slight drift in the

bias during measurement introduces some variance. The fitted simulation uses the same capacitance and g_m variations identified previously, with an additional g_m curve-fit adjustment to better match the measurements. As with the small-signal case, the resulting simulation tracks the measured response more closely, capturing the overall frequency dependence, though the measured data still predict somewhat higher values. While the first-pass parameter extraction captures the overall gain trend and improves agreement in S_{22}, the extracted parameters do not fully reproduce the measured small-signal gain magnitude, as only a limited subset of tunable model parameters are available for adjustment.

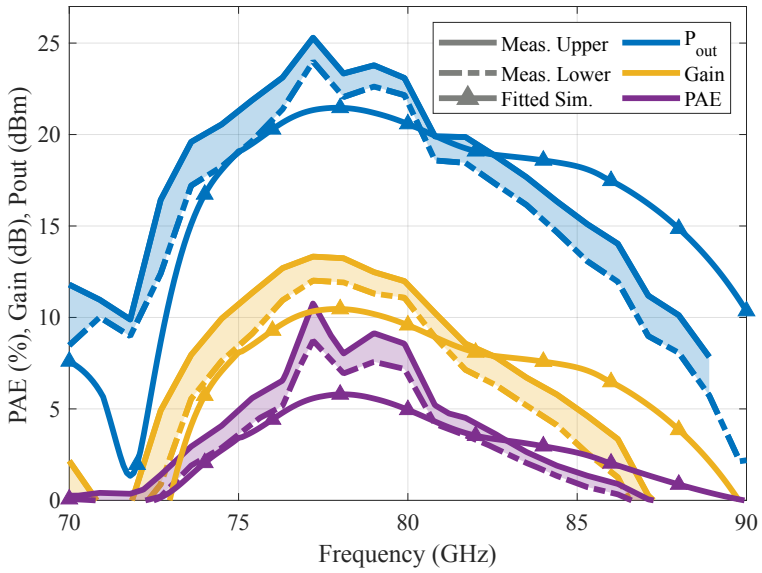


Figure 5.30: Large-signal PA performance at $P_{\text{in}} = 11\,\text{dBm}$. The shaded region shows the measured data range for V_{c1} and V_{c2} iterated over -6, 0, and +0.5 V, with the upper ($V_{c1} = 0\,\text{V}, V_{c2} = -6\,\text{V}$) (solid) and lower ($V_{c1} = -6\,\text{V}, V_{c2} = +0.5\,\text{V}$) (dot-dashed) bounds highlighted. Measurement and fitted simulation ($V_{c1} = -6\,\text{V}$, $V_{c2} = -6\,\text{V}$) (solid with triangles) use +12 V bias and $J_d \approx 150\,\text{mA/mm}$, with adjusted capacitances and optimized g_m for improved agreement over original simulation model.

The best-case biasing conditions ($V_{c1} = 0\,\text{V}, V_{c2} = -6\,\text{V}$) yield $P_{\text{out}} = 25.3\,\text{dBm}$ (0.34 W), large-signal gain of 13.3 dB, and PAE of 11 % at 77.2 GHz. The measured 3 dB gain bandwidth extends from 74.7 to 81 GHz, corresponding to an 8 % fractional bandwidth (FBW). Across this bandwidth, the measured performance spans $P_{\text{out}} = 18.5$–$25.3\,\text{dBm}$, $G = 9$–$13.3\,\text{dB}$, and $PAE = 4.2$–$11\,\%$ for the full range of V_{c1} and V_{c2} combinations, demonstrating the range of additional loss from the reconfigurable matching network

when using a 50 Ω load termination.

5.5 Conclusion and Comparison

This chapter demonstrates the feasibility of integrating a reconfigurable matching network into a W-band GaN MMIC power amplifier to compensate for modest load impedance variations. The three-stage design with reactive power combining achieves 25.3 dBm output power, 13.3 dB power gain, and $PAE = 11\,\%$ at 77.2 GHz, with an 8 % fractional bandwidth. A comparison with state-of-the-art narrow-band (≈ 20% FBW) W-band GaN PAs is provided in Table 5.2, noting that none of the other PAs contain reconfigurable matching networks.

Table 5.2: Comparison of Narrow-band W-band GaN Power Amplifiers

Ref.	Freq. (GHz)	FBW (%)	PAE (%)	P_{out} (dBm)	Pwr. Gain (dB)	Area (mm^2)
[117]	68–86	23	18.5	36.4	15.6± 2	16.25
[118]	71–85	18	15.3	36	15	15.44
[119]	90–97	7.5	18.3	37.8	10.5 ± 1*	16.72
[120]	71–86	19	10	33.5	17	10.0
[121]	77.8–89	13.4	12.3	31	12 ± 1*	3.6
[122]	86–94	8.8	8	30.6	12	4.13
[123]	71–76	6.8	27.8	34.9	11 ± 1*	1.44
[124]	71–86	19.1	9.9	31.4	17 ± 1*	10.0
[125]	88–93	5.5	14	34	15	6.65
[126]	84–95	12.3	15	28.9	10.3	-
This Work⁺	**74.7–81†**	**8**	**11**	**25.3**	**13.3**	**4.0**

* Estimated from figures

⁺ P_{in} = 11 dBm, 77.2 GHz (not at P_{sat})

† 3 dB Gain Fractional Bandwidth

A comprehensive stability analysis of the multi-stage W-band GaN PA is presented, as well as an in-depth study of the reconfigurable network device sizing. An extensive analysis is performed to explain the frequency shift between measured and simulated performance, giving insight into possible design improvements. First a test reconfigurable element is measured and analyzed. Following this, eight PA chips across two wafers

are compared. Lastly, individual devices are examined and compared using extracted model parameters, providing insight into how process variability and design choices affect reconfigurable circuits at millimeter-wave frequencies. Ideally, a W-band tuner would be used at the output to test the PA under varying load conditions, but this is not available in our lab. However, the V_c combinations are varied in measurement to illustrate the achievable performance range, and simulations show the feasibility of improvements with an integrated RMN PA at W-band. The contents of this Chapter can be found in a conference paper [38] presented at WAMICON 2025 and an IET research article titled *Analysis of an Impedance-Adaptive W-band GaN MMIC Power Amplifier* that is currently in-review.

More broadly, the work highlights both the opportunities and limitations of GaN technology at W-band. To achieve performance at millimeter-wave frequencies, GaN processes require gate lengths scaled down to tens of nanometers and high saturation velocity channels [2], necessitating complex heterostructures that introduce greater variability than lower-frequency GaN nodes [24]. These process-related variations, along with limited available drive power, constrain the maximum achievable performance in this demonstration. This work gives a first look at how reconfigurable matching can be used in W-band PAs. It provides a basis for future designs with more drive capability, tighter process control, and improved RMN circuits.

Chapter 6

A 10–29GHz GaAs/GaN Quasi-MMIC Diplexed PA

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6.1 Intro

Modern communication systems demand higher data rates, requiring both broader instantaneous bandwidths and more complex modulation schemes at higher RF carrier frequencies. This trend places increased performance requirements on power amplifiers (PAs) to operate at high efficiency while meeting linearity standards, and covering large RF bandwidth that can support multiple simultaneous signals. Traditional broadband PA architectures such as distributed or feedback-based designs can meet bandwidth requirements

[127], but often at the cost of lower power-added efficiency (PAE). Linearity and efficiency in back-off can be improved using architectures like the Doherty amplifier, e.g. [128] which is inherently bandwidth-limited, or the more complex load-modulated balanced amplifier (LMBA) topology which has been shown to cover an octave, e.g. [129].

An alternative to a single broadband PA is to use multiple narrow band PAs with a switching network as done in cell phones []. Multi-band PAs have also been shown, A number of other multi-band PAs have also been demonstrated. For example, in [130], around 15 dBm of output power is achieved at widely-separated 3.7 and 27 GHz bands from a reconfigurable CMOS PA. Some examples of dual-band GaN MMIC PAs include a 3.5/5.8 GHz [131] and a widely-separated GaN X- and K-band [132]. However, these dual-band PAs do not support signals over a wide RF bandwidth. Alternatively as opposed to using a single broad-band PA to cover a wide bandwidth is to use multiple narrowband PAs or a mu, each optimized for a specific frequency band, and combine them using a diplexer or multiplexer. This architecture not only enables continuous wideband operation, but the linearization becomes simpler for concurrent multi-band signals due to isolation between PA paths [133]. Additionally, a dual-band mode can be used by pinching-off the other PA path, enhancing PAE without the use of lossy switches or other tunable elements. Prior demonstrations include a hybrid 2–4 GHz GaN PA [133, 134], and various monolithic circuits covering C to X-band [135], X to Ku-band [136], and Ku to Ka-band [137]. The latter three PAs employ coupled-line diplexers, a technique with well-established theoretical foundations [138].

In this Chapter, we demonstrate a three-chip GaAs/GaN PA architecture shown in Fig. 6.1 capable of both wideband and individual-band operation. The demonstrated design uses a coupled-line diplexer filter to split a bandwidth (10–29) GHz into a 66 % and 33 % fractional bandwidth (FBW) sections. The diplexers are implemented on-chip in two different GaAs processes and isolate and filter the outputs of two independent, two-stage PAs. Each PA features a ~1:3 staging ratio using 6×50 μm and 8×121 μm HEMTs.

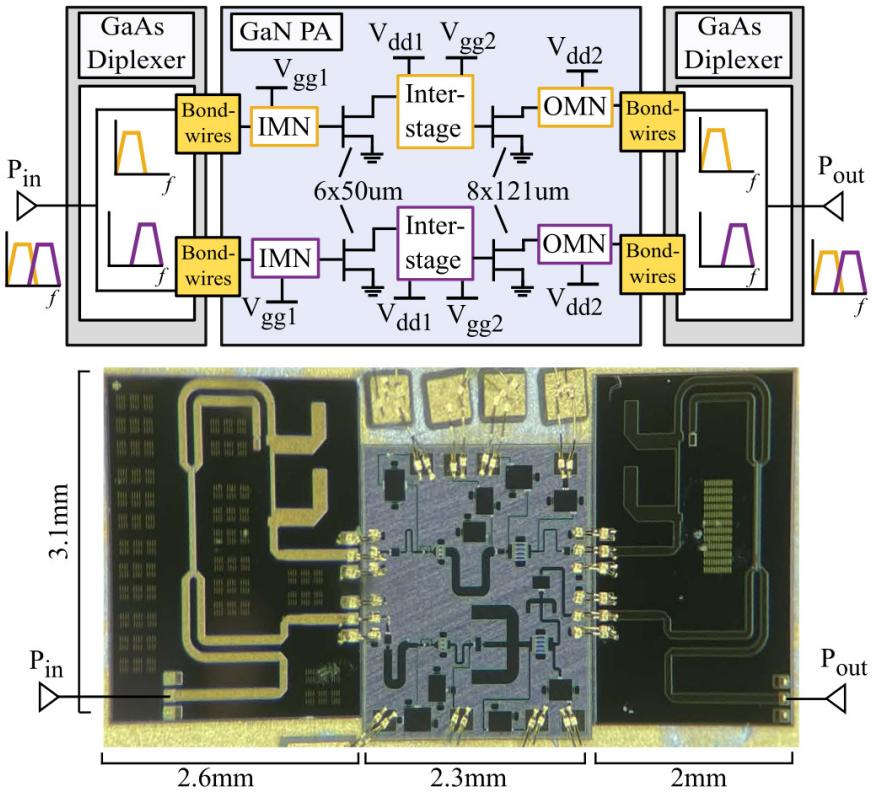
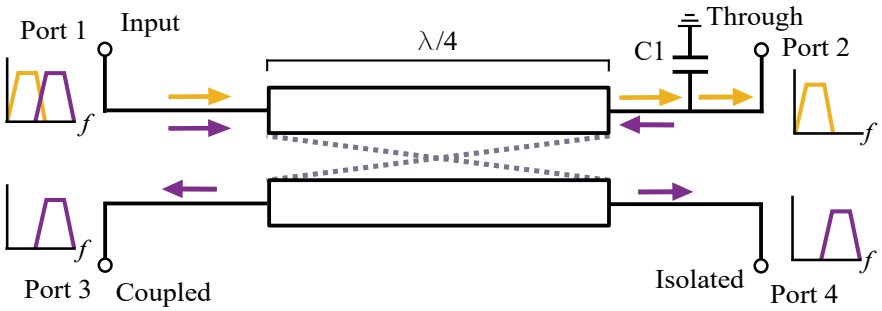


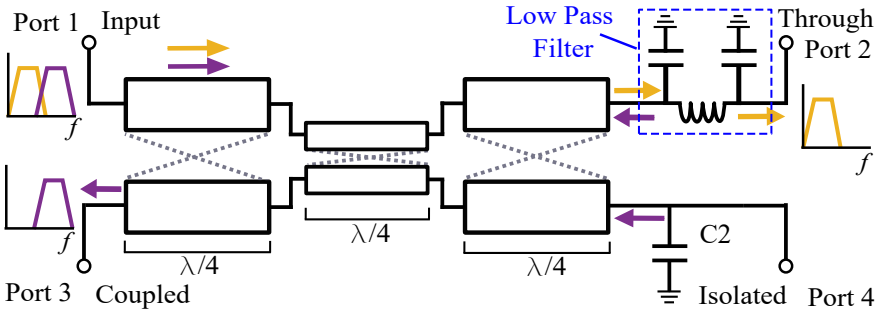
Figure 6.1: Top: Schematic of the diplexed power amplifier architecture, highlighting the GaN and GaAs chips, input/output diplexers, and two PA paths. A conceptual frequency flow plot illustrates the band-splitting behavior of the diplexers covering Ku- through Ka-band. Bottom: Photograph of the GaN and GaAs chips with labeled die dimensions (in mm). Wirebonds connecting the GaN PA output to the GaAs diplexer are visible.

6.2 GaAs Coupled-Line Diplexer

The diplexer structure in this work is based on quarter-wavelength coupled-line theory [138, 139]. As shown in Fig. 6.1, the diplexers placed at the input and output of the PAs are used to split and subsequently recombine signals across a low-frequency path shown in yellow and a high-frequency path shown in purple. The diplexer topology, depicted in Fig. 6.2(a), consists of a coupled-line transmission line section with the through port shunted by a capacitor. At low frequencies, the capacitor presents an open, while at higher frequencies starting near the crossover frequency f_{split}, the capacitor behaves as a short circuit, reflecting the high-frequency components. The reflected signal is 180° out of phase and ideally splits equally between the coupled and isolated ports.



(a)



(b)

Figure 6.2: (a) Fundamental four-port coupled-line diplexer based on quarter-wavelength coupled lines. A shunt capacitor at the through port reflects high-frequency signals by presenting a short circuit above the design cutoff. (b) Enhanced diplexer topology featuring multi-section coupled lines with varying impedances to improve bandwidth. A low-pass filter replaces the single shunt capacitor in the through path, and a shunt capacitor is added at the isolated port to redirect reflected high-frequency energy to the coupled port.

Several enhancements are introduced in this work to improve the diplexer's performance, as illustrated in Fig. 6.2(b). First, the bandwidth of each passband is extended by cascading multiple coupled-line sections, each with varying line widths and inter-line spacings. Second, the single shunt capacitor in the basic topology is replaced with a three-element low-pass filter in the through path, thereby increasing high-frequency reflection at the designed cutoff frequency. Lastly, a shorted capacitor is placed at the isolated port to redirect reflected power to the coupled port, effectively realizing a three-port diplexer with an expanded fractional bandwidth in each path.

The input and output diplexers are designed and implemented using the WIN Semiconductors GaAs PQG30C and PIH1-10 processes, receptively. The diplexers prioritize low insertion loss while selectively filtering out the other PA path. Compared to the GaN process used for the PA, the GaAs processes offer more favorable characteristics for passive structures, including a lower dielectric loss tangent (0.001 vs. 0.003 for

GaN). These features result in reduced dielectric and conductor losses compared to GaN. The two GaAs processes passive structures are almost identical, except the PQ30C's main conductor metal thickness is 2 μm thicker than the PIH1-10's, leading to marginally lower conductive losses in the input diplexer. The layout of the output GaAs diplexer is shown in Fig. 6.3 as an example.

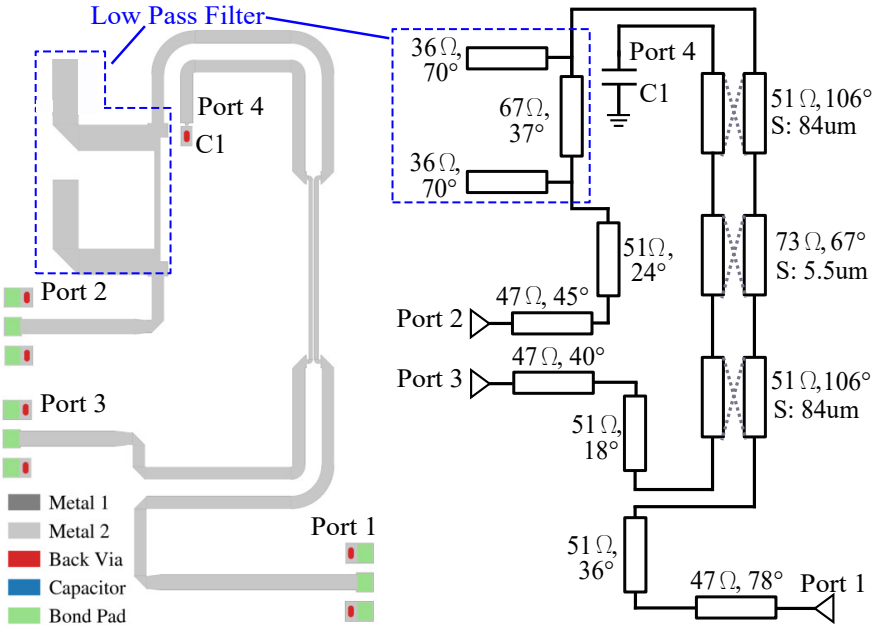


Figure 6.3: Layout and schematic of the GaAs output diplexer. Ports 2 and 3 receive the low and high frequency output from the PA branches, respectively, which are recombined at Port 1. The coupled-line sections are designed for 90° electrical length at 22 GHz, with spacing "S" denoting the microstrip line spacing.

Ports 2 and 3 serve as the inputs for the low- and high-frequency paths, respectively. The coupled-line sections are designed to be 90° at the crossover frequency of 22 GHz, with varying spacing to improve passband performance. A low-pass filter is incorporated in the through path using wide, bent transmission lines to realize capacitive elements and narrow lines for inductive sections. Port 1 serves as the output, where the two frequency paths are recombined. The input diplexer is nearly an identical design, just mirrored. Comparison of the simulated diplexers is shown in Fig. 6.4.

Due to the inability to probe all three ports simultaneously, the diplexers are characterized using three separate chips, each with alternating ports terminated with bondwires to a grounded 50 Ω surface-mount termination. This termination degrades the measured return loss most notably relative to the designed

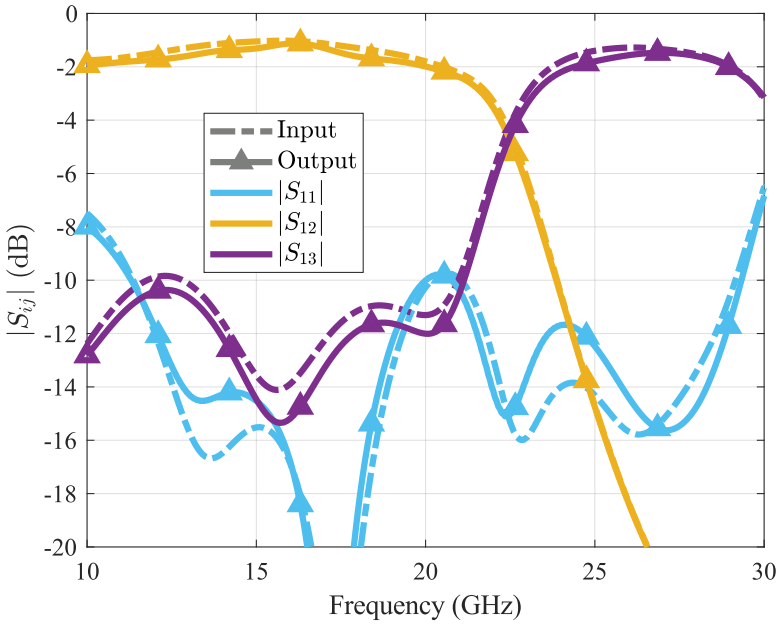


Figure 6.4: Simulated filter results for the input and output diplexers from 10–30 GHz. Processes have near identical passive structure characteristics.

diplexers performance. For fair comparison, the same termination conditions are replicated for the simulation data. Under these replicated conditions, the simulated and measured results show good agreement, validating the design approach. Small-signal simulation (dotted) and measurement (solid) for the input (top) and output (bottom) diplexers are shown in Fig. 6.5.

The filter exhibits insertion loss in both passbands of 1–2 dB, with a crossover point at 22 GHz where the measured insertion loss is around 3.3 dB. The rejection of the low frequency path is <20 dB at 25 GHz. The high frequency path has a lower rejection which varies between 8 dB (12.3 GHz) and 20 dB (19.85 GHz).

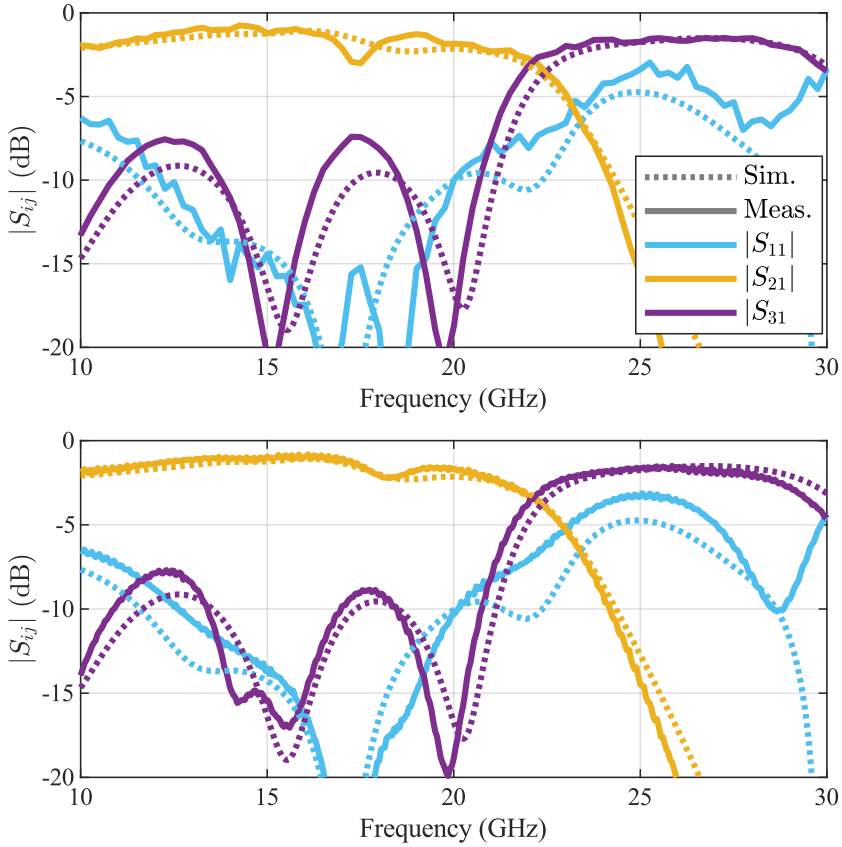


Figure 6.5: Simulated (dotted) vs. measured (solid) small-signal S-parameters of the input (top) and output (bottom) GaAs diplexers from 10–30 GHz. The return loss in simulation and measurement is worse than reality due to lack of a possible three-port measurement system for this layout.

6.3 MMIC GaN Power Amplifiers

Due to the high output power requirements of the PA, the WIN NP12-01 GaN process is selected over the GaAs process used for the diplexers. This process uses a 120-nm gate length on a 50-μm (2-mil) silicon carbide (SiC) substrate with an f_T of 38.5 GHz. The technology supports operation up to 28 V and at 29 GHz, offers a power density of 3.37 W/mm, 14.5 dB linear gain and 36.5 % PAE at P_{sat}. Passive structures such as transmission lines and air bridges are made using two interconnect metal layers. Resistors are made with tantalum nitride (TaN) and capacitor dielectric layers with silicon nitride (SiN) along with high reliability metal-insulator-metal (MIM) capacitors. Figure 6.13 shows a deconstructed layout of the

entire GaN MMIC, which includes the low-band and high-band PAs arranged for straightforward integration with the GaAs diplexers.

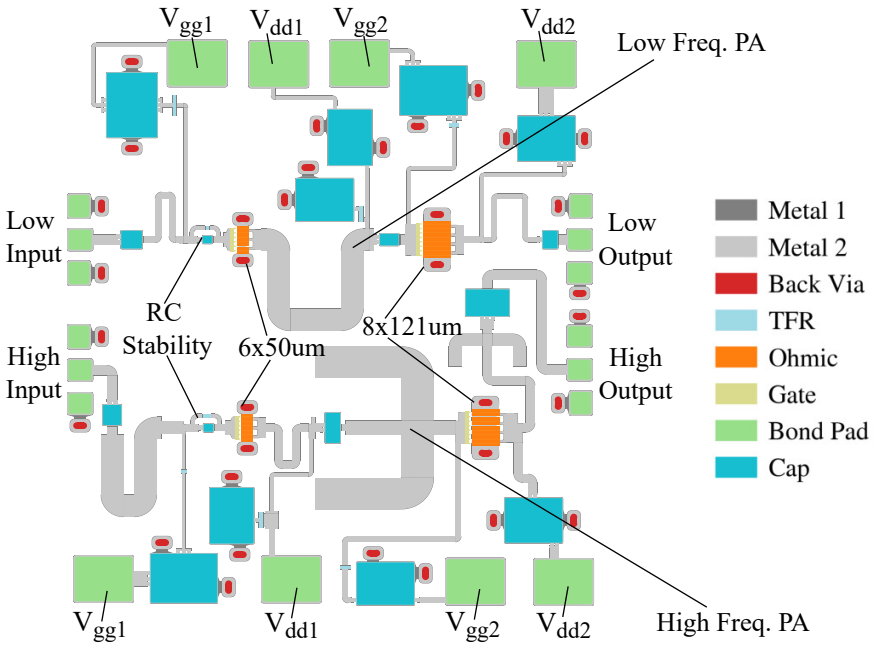


Figure 6.6: Deconstructed layout of the GaN chip implemented in the WIN NP12-01 process.

To validate the operation of the low- and high-band amplifiers before integration with diplexers, the small-signal individual measurements are performed on-wafer using a PNA with SOLT calibration. The large-signal scalar measurement setup includes a 2–29 GHz driver amplifier, a 2–40 GHz input coupler, input and output power sensors, and over 30 dB of output attenuation. Measurements are conducted on-wafer and a picture of the measurement bench with DUT picture is shown in Fig. 6.7.

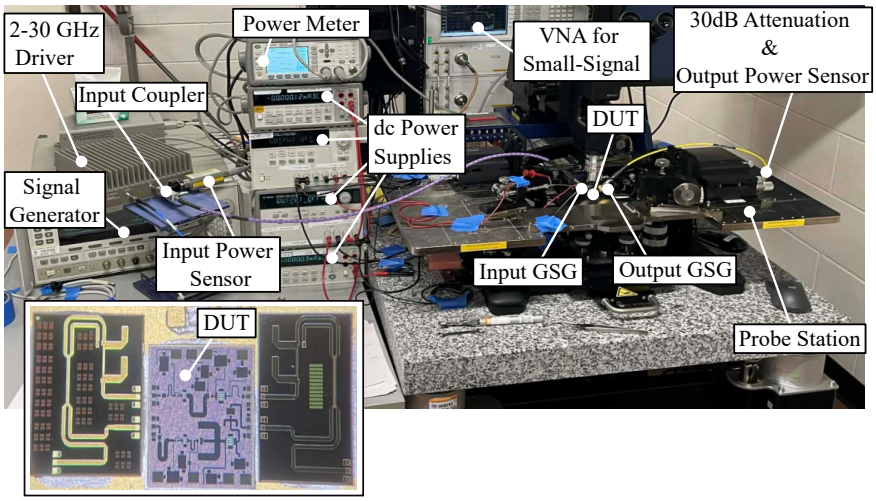


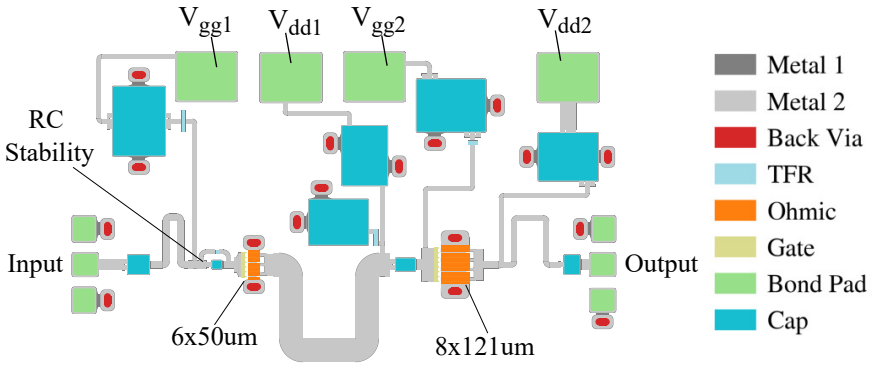
Figure 6.7: Large-signal K-band bench setup with VNA used for small-signal measurements in the background. Picture of GaN and GaAs chips is shown on the bottom left in expanded form.

6.3.1 Low-Band PA

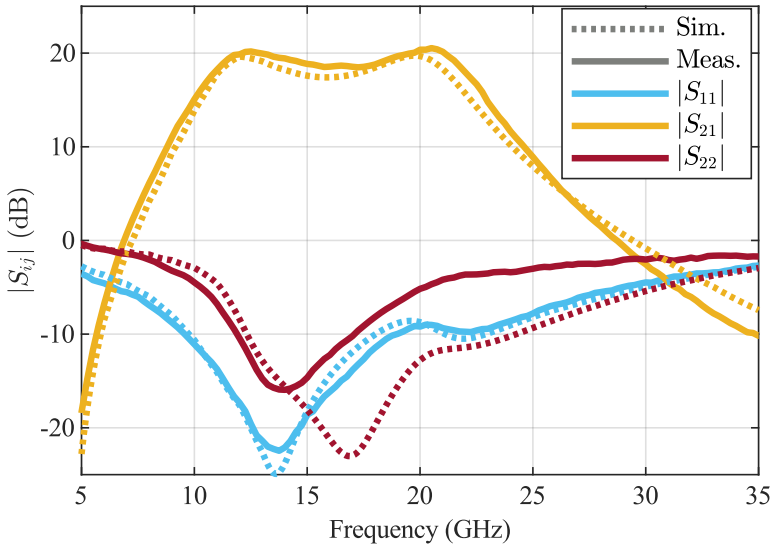
The PA is designed using Cadence Microwave Office (AWR) with the 2.5D electromagnetic solver. A $6 \times 50\,\mu$m driver is included, with an $8 \times 121\,\mu$m output HEMT for a staging ratio of approximately 1:3. The input and output matching networks (IMN and OMN) include a 0.25 nH bondwire inductance and incorporates the simulated S-parameter data of the GaAs diplexers for co–design simulation. The layout of only the low-band PA with some key layers labeled, as well as the small-signal measurements and simulations are shown in Fig. 6.8.

The first stage IMN includes a series RC stability network with a 27 Ω resistor and 0.158 pF capacitor. The gate bias lines include small ($\approx 5\,\Omega$) series resistors and shunt capacitors to terminate RF in the bias lines and prevent oscillations. The interstage matching network drain bias line also includes a decoupling resistor/capacitor network before the shunt capacitor to help with low frequency isolation. The gate and drain bias pairs are bonded off-chip to single layer 100 pF and 1000 pF capacitors to supress any low-frequency instabilities. Stability is verified through a multitude of measurements (K-factor, linear, and nonlinear Nyquist) up to the third harmonic of the center frequency (60 GHz).

The small-signal measurements in Fig. 6.8(b) are taken at $V_{dd} = 28$ V with a total bias current of 100 mA, with the gate and drain connected off chip to simplify biasing. The results show good agreement with



(a)



(b)

Figure 6.8: (a) Low-band PA layout. (b) Small-signal simulations (dotted) vs. measurements (solid) at V_{dd} = 28 V, I_{tot} = 100 mA. Gate and drain pairs are connected off-chip to simplify biasing. The low-band PA footprint size is 2.28 mm × 1.3 mm.

$|S_{21}| \geq 18$ dB from 11–22 GHz. The measured $|S_{22}|$ is in poorer agreement with simulations than $|S_{11}|$ and $|S_{21}|$ and does not predict the same simulated response at 17 GHz. The model also underestimates $|S_{21}|$ by approximately 1 dB.

The large-signal low-band PA simulations (dotted) vs. measurements (solid) are shown in Fig. 6.9 at a fixed input power of 21 dBm with the PA biased at V_{dd} = 24 V and I_{tot} = 23 mA. At 12.6 GHz, the PA achieves P_{out} = 34.47 dBm (2.79 W), Gain = 13.4 dB, and PAE = 37.5 %, with a 3 dB gain bandwidth of 11–21.8 GHz (65.8 % FBW).

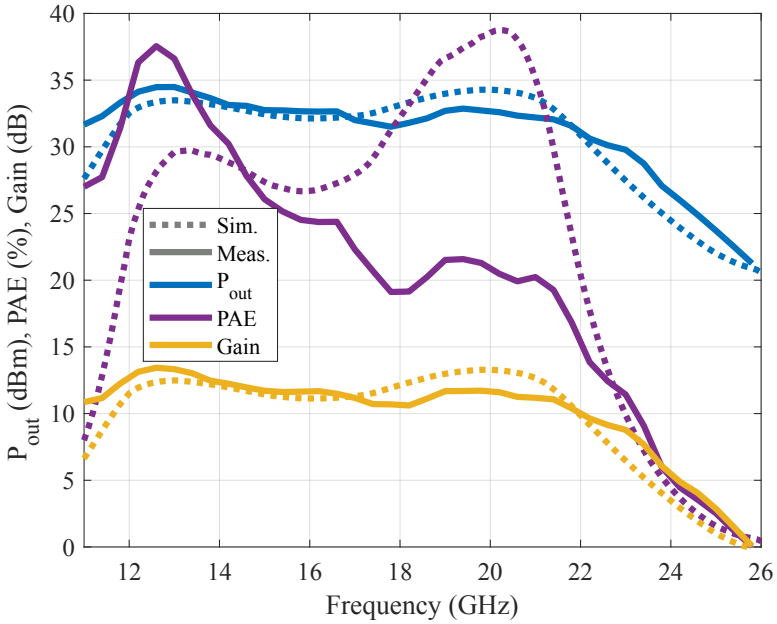


Figure 6.9: Low-band PA large-signal simulations (dotted) vs. measurements (solid) at a fixed input power of 21 dBm with the PA biased at V_{dd} = 24 V and I_{tot} = 23 mA. The 3 dB gain bandwidth is from 11–22 GHz (12.8–9.8 dB).

Measured gain and P_{out} generally agree well with simulation, although the predicted power is higher than the measured between 17–21 GHz. This over-estimate partially offsets the PAE discrepancy, however the measured PAE remains lower than predicted from 16–22 GHz, a common outcome in broadband PA designs. A comparison table for the Ku-band low-band PA is shown in Table 6.1. The PA presented shows the highest fractional 3 dB power gain bandwidth compared to other GaN MMIC PAs in the same frequency range. This work also shows the tied highest peak PAE and the works that have larger output power are larger in area and are longer gate length processes. The Ku-band PA here compares favorable to SOTA work shown.

Table 6.1: Comparison of GaN MMIC PAs at Ku-band (12-18)

Ref. (#)	Freq. (GHz)	FBW (%)	L_{gate} (nm)	Max. PAE (%)	P_{sat} (dBm)	$\|S_{21}\|$ (dB)	Area (mm^2)
[140]	17–20	16	250	32	40.0	20	15.8
[141]	10–14	33	150	38	36.1	14±1†	10.64
[142]	11–17.5	46	150	34	36.2	20±2†	6.4
[143]	15–24	46	140	31	43.0	26.7	30.06
[144]	11–18	48	120	33	34.9	26.5	5.3
T.W.	**11–22**	**66**	**120**	**38**	**35.5**	**20.5**	**3.0**

† Estimated from figure

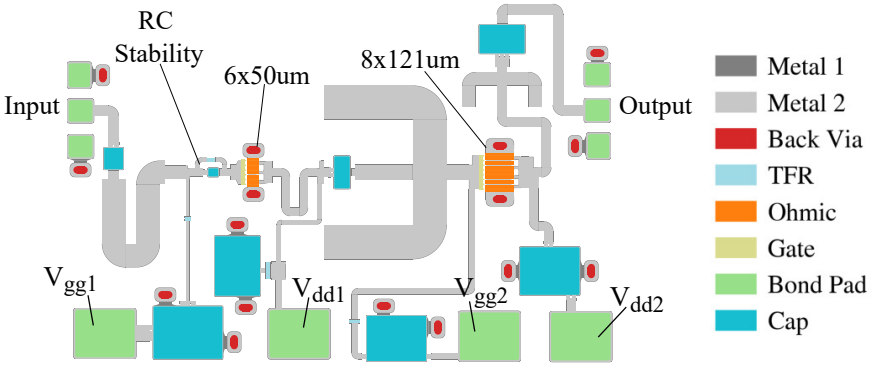
6.3.2 High-band PA

The high-band PA has the same staging ratio as the low-band PA and also uses an RC network in the IMN with a 95 Ω resistor and 0.155 pF capacitor along with the same bias line isolation techniques as the low-band PA, as allowed within the die space. The layout (a) and small-signal results (b) are shown in Fig. 6.10 at the same bias conditions as those in Fig. 6.8(b).

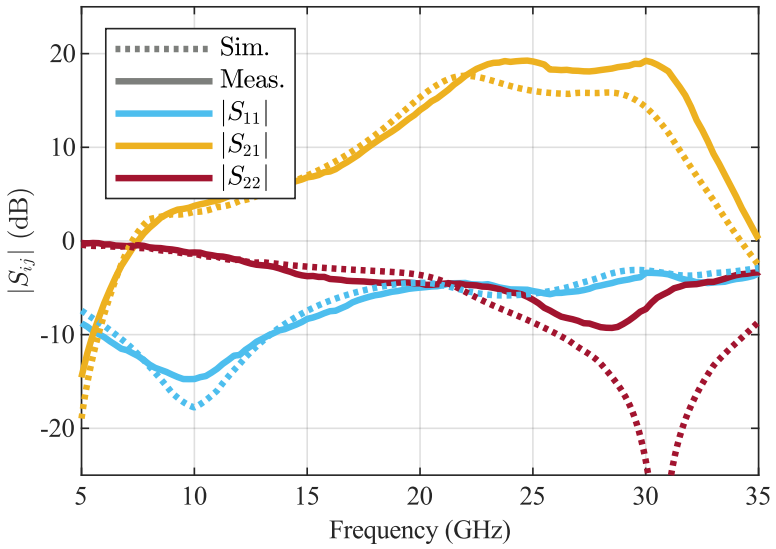
The small-signal results in Fig. 6.10(b) show the model underestimates $|S_{21}|$ starting at 23.5 GHz by approximately 3 dB and rolls off around 30 GHz compared to 32 GHz in measurement. The measured $|S_{11}|$ aligns well and $|S_{22}|$ is overestimated in the model like in the low-band PA results.

The large-signal high-band PA simulations (dotted) vs. measurements (solid) are shown in Fig. 6.11 at a fixed input power of 19 dBm with the PA biased at V_{dd} = 20 V and I_{tot} = 118 mA. At 23 GHz, the PA achieves P_{out} = 32.8 dBm (1.9 W), Gain = 13.8 dB, and PAE = 28.8 %, with a 3 dB gain bandwidth of 21–29.4 GHz (33 % FBW).

The high-band PA shows similar agreement as the low frequency path in that the measured gain and P_{out} generally agree with simulation, with some overestimation of simulation from 19–22 GHz. The PAE aligns more closely, but at the high end of the band (27.5-29 GHz) is more than 10 % lower than simulation predicts. The measured drive-up curves are shown in Fig. 6.12 for both low- and high-band PAs at 13 and 23 GHz, respectively. The low-band PA is biased at V_{dd} = 24 V, I_{tot} = 23 mA and high-band PA at V_{dd} = 28 V, I_{tot} = 82 mA.



(a)



(b)

Figure 6.10: (a) High-band PA layout (b) Small-signal simulations (dotted) vs. measurements (solid) V_{dd} = 28 V, I_{tot} = 100 mA. The high-band PA footprint size is 2.28 mm × 1.53 mm.

A comparison with PAs in the literature in a similar frequency range is shown in Table 6.2. The gain at saturation ranges from 9.4–12.4dB at 21 dBm input power from 21 to 29.4 GHz, limited by the driver used in the scalar measurements. The K-band PA presented here shows the largest FBW and has comparable output power. The few other works with larger output power are larger in size and have longer GaN gate lengths. The peak PAE is in the midrange of the table compared to other work.

A final picture taken through a microscope lens of the GaN MMIC PA is shown in Fig. 6.13. The bondwires are attached to the dc pads at dc bias lines. The entire PA is designed to integrate with the

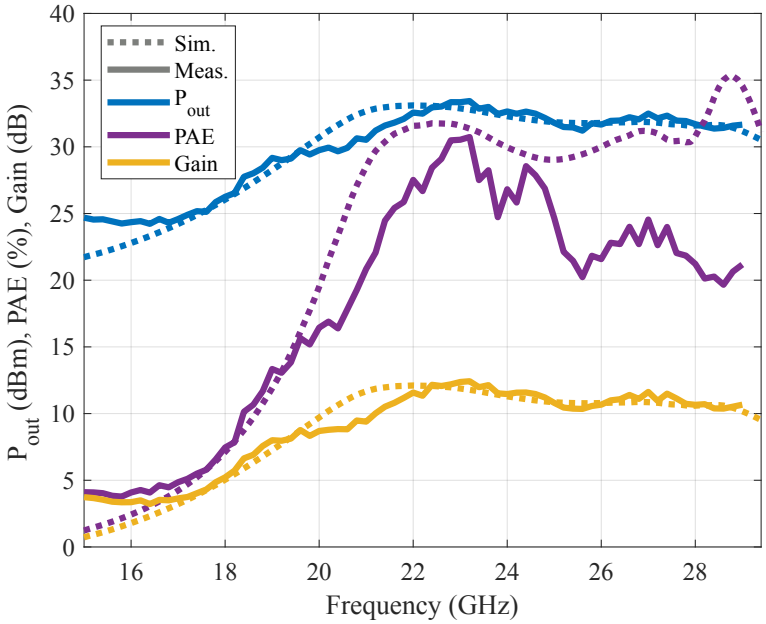


Figure 6.11: High-band PA large-signal simulations (dotted) vs. measurements (solid) at at a fixed input power of 21 dBm with the PA biased at V_{dd} = 20 V and I_{tot} = 57 mA. The 3 dB gain bandwidth is from 21–29.4 GHz (12.4–9.4 dB).

Table 6.2: Comparison of GaN MMIC PAs at K-band (18-27)

Ref. (#)	Freq. (GHz)	FBW (%)	L_{gate} (nm)	Max. PAE (%)	P_{sat} (dBm)	$\|S_{21}\|$ (dB)	Area (mm^2)
[145]	18.5–24.5	28	250	32	36.5	21	4.68
[146]	23–29.5	25	150	39.1	34.9	35	6.46
[147]	25–31	21	150	42	42.2	21	17.5
[148]	18.5–24	26	150	40	36.5	35	8.0
[149]	24–30	22	120	27.6	32.7	14.9	6.3
[150]	24–30	22	100	34.7	30.9	29	1.61
T.W.	**21–29.4**	**33**	**120**	**31**	**34.3**	**19.3**	**3.5**

previously designs GaAs coupled line diplexers.

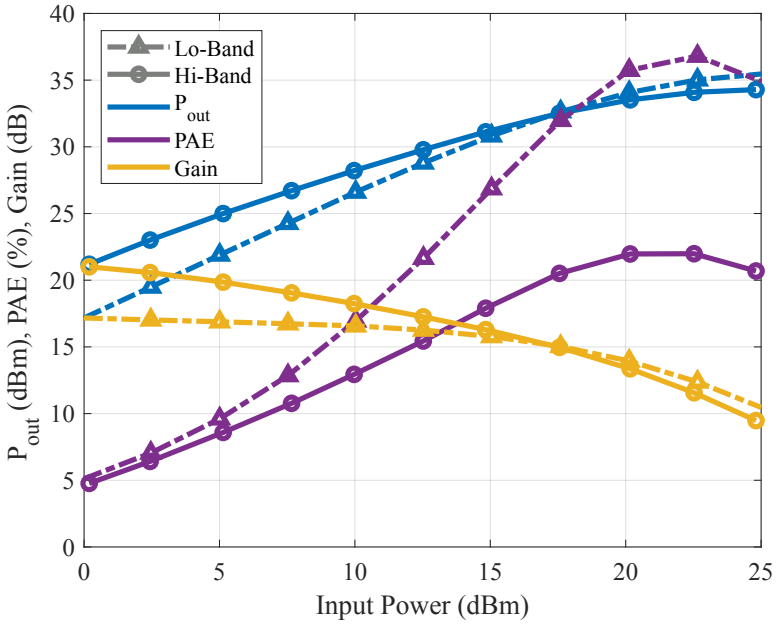


Figure 6.12: Measured drive-up curves for low- and high-band PAs at 13 and 23 GHz, respectively. The low-band PA is biased at V_{dd} = 24 V, I_{tot} = 23 mA and high-band PA at V_{dd} = 28 V, I_{tot} = 82 mA.

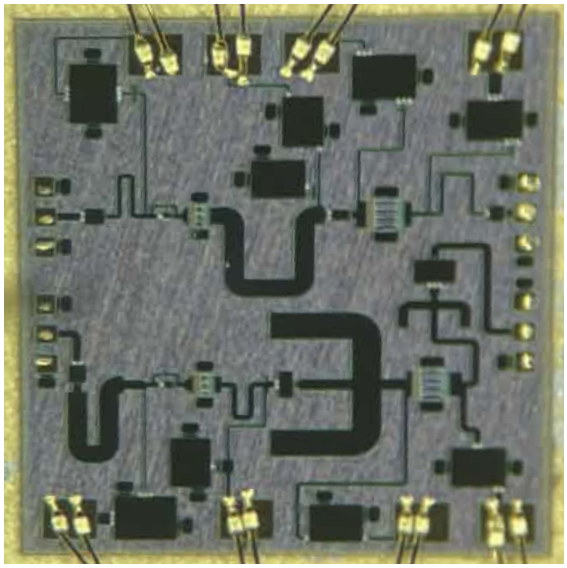


Figure 6.13: Picture of the entire GaN MMIC PA chip under a microscope lens with bondwires attached at the bias pads.

6.4 Integrated PA and Diplexers

After characterization of the GaN MMIC PAs, the GaAs diplexers are wire bonded to the PA GSG paths. The diplexer substrates are placed as close as possible to the GaN chip, estimated to be within 100 μm ±50 μm. The $100 \times 100\,\mu m^2$ GSG pads can reasonably fit two 1-mil diameter gold wire bonds. The GaAs substrate is twice as thick as the GaN-on-SiC substrate. Figure 6.14 shows a photograph of the bondwires connecting the three MMICs. The grounds of the GSGs are also connected from chip-to-chip to shorten the path to ground and minimize loop inductance.

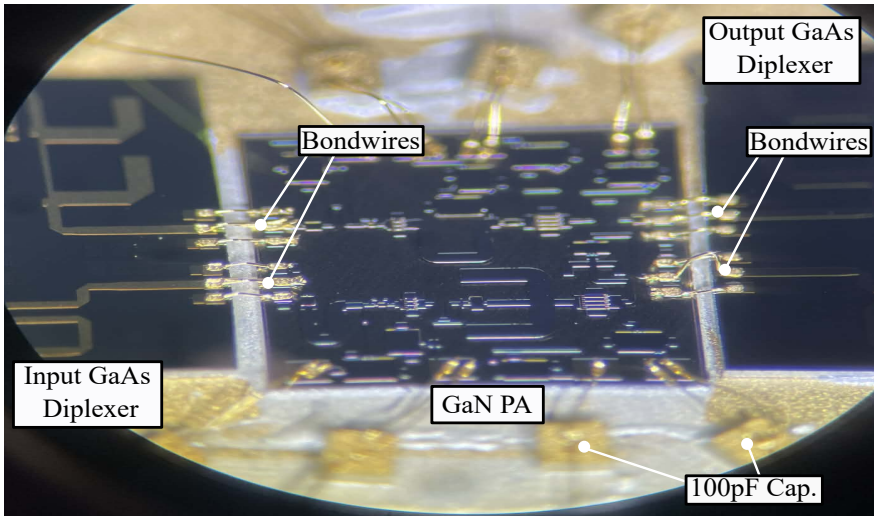


Figure 6.14: Photograph through a microscope lens showing the GaAs diplexers wirebonded to the GaN PA. The gap between MMICs is estimated to be 100 μm ±50 μm.

Once the filters are wire-bonded to the PA, the diplexer input and output are probed on-wafer and the entire quasi-MMIC is characterized with a VNA. The measured (solid) and simulated (dotted) small-signal S-parameters from 5–35 GHz for three separate diplexed PAs with both PAs biased on is shown in Fig. 6.15. Results show excellent agreement across the band, with measured $|S_{21}| \geq 10$ dB from (10.5–29.5) GHz (95% FBW). As seen in the individual PA small-signal measurements (Fig. 6.8(b), Fig. 6.10(b)), there is an model underestimation in $|S_{21}|$ from 20–29 GHz. $|S_{11}|$ aligns well with simulation and $|S_{22}|$ shows the same resonance mismatches as in the individual PA results.

One benefit of this topology is that the performance within a single PA sub-band can be improved by

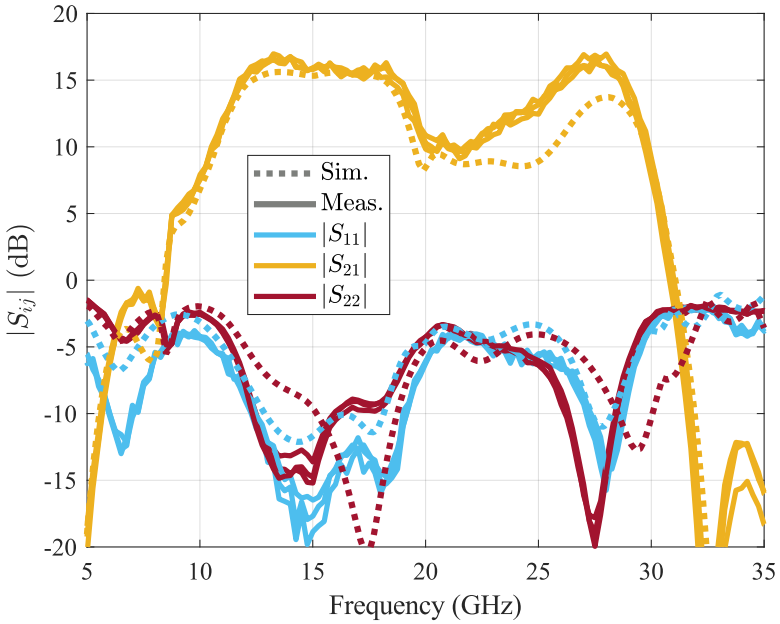


Figure 6.15: Measured (solid) and simulated (dotted) small-signal S-parameters of the full PA (5–35 GHz) with both branch PAs biased ON at V_{dd} = 28 V, I_{tot} = 140 mA in the full-band mode for three unique mounted diplexed PAs.

biasing off the other PA path. The small-signal results for the low-band PA and high-band PA is shown in Fig. 6.16 with the active PA biased at V_{dd} = 28 V and a total drain current of 83 mA.

The inactive PA in both cases is biased around V_{gg} = -1.7 V, V_{dd} = 0 V. As shown in [135] the off-state characteristics of the transistors in the inactive path affects the performance of the PA in the active path. The $|S_{21}|$ discrepancy that was seen in the solo PA small-signal measurements is also seen in the diplexed PA architecture. While this difference is not significant, the results are more pronounced in the large-signal measurements.

The large-signal measurements from the setup shown in Fig. 6.7 are first demonstrated with the PA biased in the full-band mode in Fig. 6.18. Simulated results (dotted) are at a fixed P_{in} = 21 dBm with both PAs biased at V_{dd} = 24 V and I_{tot} = 23 mA and are included to illustrate broadband performance trends. The measured results show the best achieved performance at each frequency obtained over a range of P_{in} = 20–22 dBm, V_{dd} = 24–28 V, and I_{tot} = 24–122 mA. Across the 11–29 GHz range the optimized measured results range

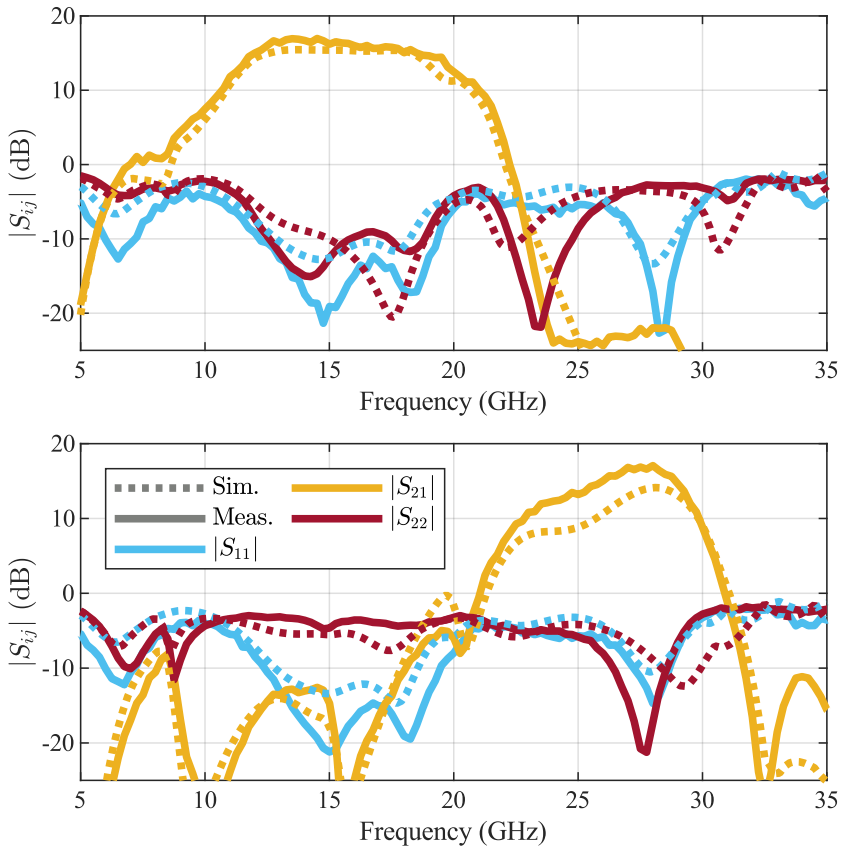


Figure 6.16: Low-band mode (top) and High-band mode (bottom) small-signal S-parameter measurement vs. simulation from 5–35 GHz.

from P_{out} = 26.3–33.6 dBm, PAE = 2.5–23 %, and power gain from 5.2–13 dB. The average values of P_{out} is 30.4 dBm (1.1 W), PAE 12 %, and gain 10 dB.

The large-signal band-enhancement mode measurements compared to a fixed input power full-band mode are shown in Fig. 6.17. The different line types illustrate the different modes and all data is taken at an input power of 21 dBm for comparison. The individual bands show slight increase in gain and output and more noticeable improvement in the PAE (5-8 %). At 13 GHz, the low-band mode achieves P_{out} = 33.03 dBm (2W), PAE = 30%, gain = 11.95 dB. At 27.4 GHz the high-band mode achieves P_{out} = 32.08 dBm (1.6W), PAE = 20.8%, G = 10.9 dB at 27.4 GHz. Changing the bias of the alternate PA path benefits the PAE the most due to the lower dc power consumption.

A comparison table of state-of-the-art wideband GaN MMIC amplifiers of similar frequency are shown

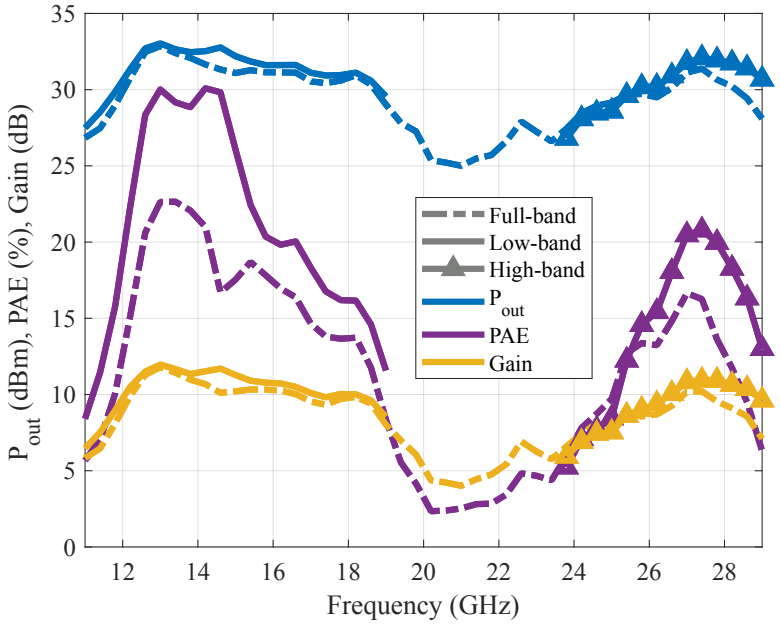


Figure 6.17: Large signal measurements from 11 to 29 GHz. Measured results all at 21dBm input power. The all-band, low-band, and high-band results are plotted together for comparison.

in Table 6.3. The bandwidth of the diplexed PA in this work is based on the small-signal gain ≥10 dB from 10.5–29.5 GHz as defined in other works, e.g. [151]. The table shows results in descending order based on the GaN process gate length (L_{gate}).

Table 6.3: Comparison of Broadband GaN MMIC Amplfiers

Ref. (#)	Topology	L_{gate} (nm)	Freq. (GHz)	FBW (%)	PAE (%)	P_{out} (dBm)	LS Gain (dB)	$\|S_{21}\|$ (dB)	Area (mm^2)
[152]	Cascode DA[1]	150	0.1–45	200	Pk. 23	29.3–33.0	–	14	2.8
[153]	Non-Uniform DA[1]	150	16–40	86	10–20	36.2–39.4	–	25	6.3
[153]	Non-Uniform DA[1]	150	16–40	86	10–19	38.5–42.0	–	24	15.6
[151]	fT-Doubler	100	28–90	105	4.4	20.6	–	19	4.5
T.W.	**Diplexed**	**120**	**10.5–29.5**	**95**	**2.5–23 Avg. 12**	**26.3–33.6 Avg. 30.4**	**5.2–13 Avg. 10**	**17**	**20.46**

[1] Distributed Amplifier

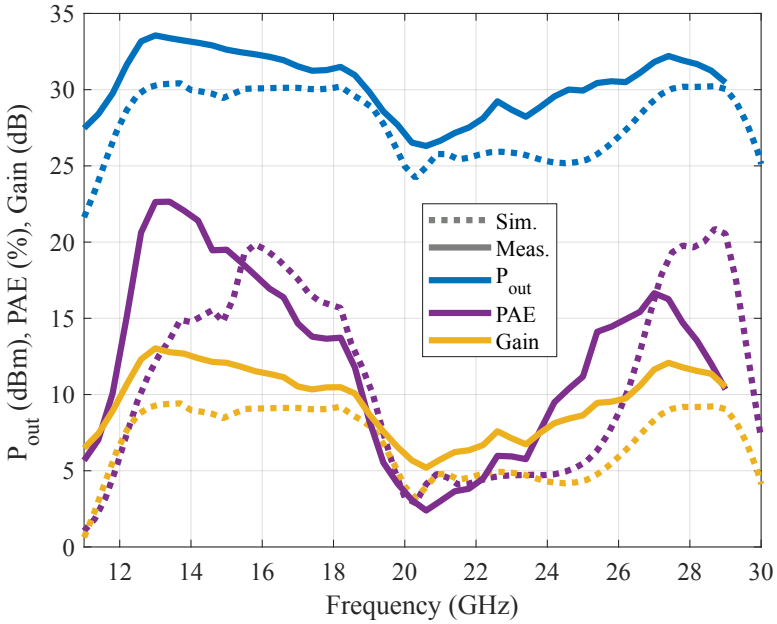


Figure 6.18: Large signal results from 11 to 29 GHz. Measured results show the best achieved performance at each frequency obtained under frequency dependent input drive and bias conditions. Simulation results are shown at a fixed input power and bias to illustrate performance trends.

6.5 Conclusion and Discussion

This chapter demonstrates a quasi-MMIC that combines two different GaAs mirrored coupled line diplexer filters with a single GaN PA MMIC for a single input and output port. The GaN PA contains two different two-stage PA designs that are optimized to work in their band of interest while maintaining some overlap in the crossover region of the diplexer filters.

Regarding high-band PA design using same staging as low-band design, in retrospect this is inopportune for this topology as the G_{max} of a 8×121 μm HEMT at V_{dd} = 28 V, I_{dd} = 40 mA, at 15 GHz is more than 4 dB greater than at 25 GHz. In future designs, larger periphery/additional stages should be added in the higher frequency path to flatten the gain response and make up for the gain difference. The performance degradation between 19–24 GHz caused by the filter's crossover can be mitigated using additional phasing lines [134] and adding more gain to compensate for the filter crossover loss. However, limited GaN reticle area prevented implementation in this work.

The quasi-MMIC presented in this Chapter shows comparable fractional bandwidth in the full-band mode to other SOTA wideband amplifiers while also having a accessible efficiency-enhancement mode for improved performance in the sub-bands. This work has one of the largest FBW, where as the few works with larger bandwidth have a lower peak P_{out} [152] and lower P_{out} and PAE [151]. The contributions from this Chapter are in preparation for the first half of a manuscript entitled *Integrated X- to W-band Diplexed Power Amplifiers*, which is currently in preparation for submission to the IEEE Transactions on Microwave Theory and Techniques.

Chapter 7

A 45–89 GHz MMIC Diplexed PA in HRL 40-nm GaN Process

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7.1 Intro

This Chapter presents a different approach to the diplexed PA architecture presented in Chapter 6 at 10.5 GHz to 29.5 GHz. The design operates in E–band, and accordingly, adds more periphery through reactive power combining along with an extra gain stage to compensate for the reduced device gain at higher frequencies. Furthermore, a reflectionless diplexer filter is employed for combining to control the stop-band impedance to improve stability. The design utilizes two distinct three-stage PAs operating at V– and W–band each with a

1:2:4 staging ratio and implemented using a combination of $4 \times 37.5\ \mu$m and $6 \times 50\ \mu$m HEMTs. The circuit schematic (top) and labeled GaN MMIC picture (bottom) is shown in Fig. 7.1.

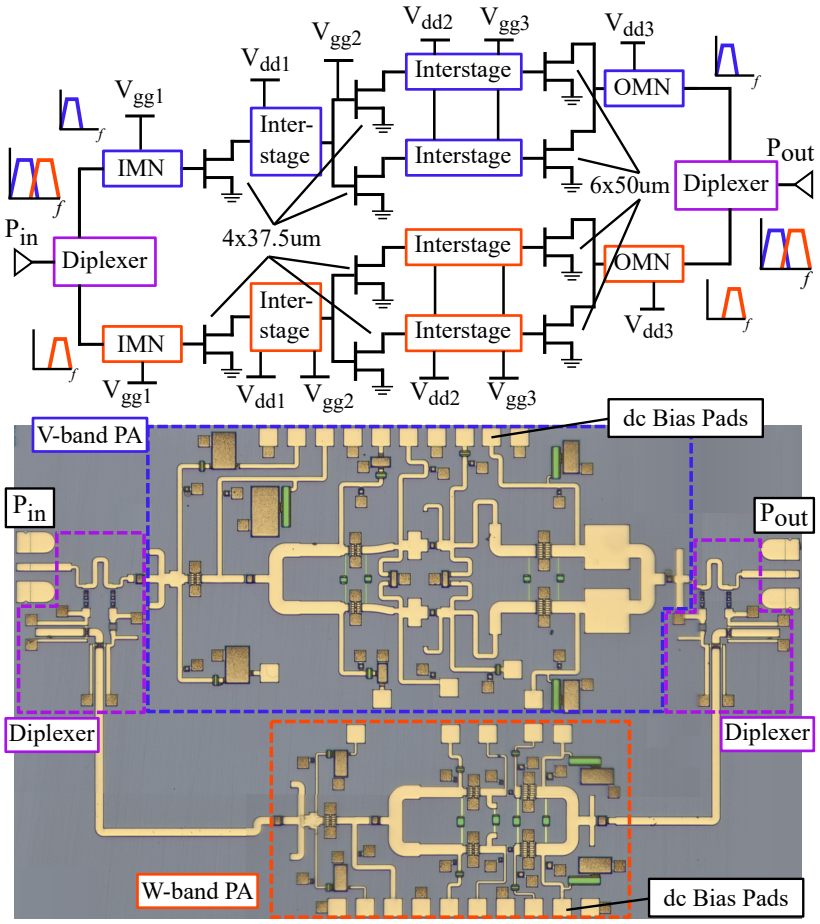


Figure 7.1: Top: System-level schematic of the diplexed power amplifier architecture, highlighting the input and output diplexers and two PA paths. A conceptual frequency flow plot illustrates the band-splitting behavior of the diplexers covering 45 through 95GHz. Bottom: Photograph of the GaN chip with labeled PAs and filters in blue, red, and purple colored dotted line boxes. Wirebonds connecting the GaN PA output to the GaAs diplexer are visible.

7.2 Reflectionless Diplexer Filter

A reflectionless filter absorbs stop-band energy rather than reflecting it back to the source. This characteristic is particularly advantageous for the diplexed PA topology, where the two isolated PAs can interact resulting in reduced overall performance. This is of additional concern when operating at millimeter-wave frequencies, where achieving sufficient low-frequency gain for isolation and stable operation is challenging.

The reflectionless filter implemented in this work is based on the topology described in [154–156], and is also discussed in [157].

The underlying theory is detailed in the cited works by M. Morgan, with additional extensions to millimeter-wave implementations using transmission lines reported in [158]. Only the essential concepts are summarized here for clarity. The ideal circuit of the reflectionless diplexer is shown on the left in Fig. 7.2, with the corresponding simulated S-parameter magnitudes shown on the right.

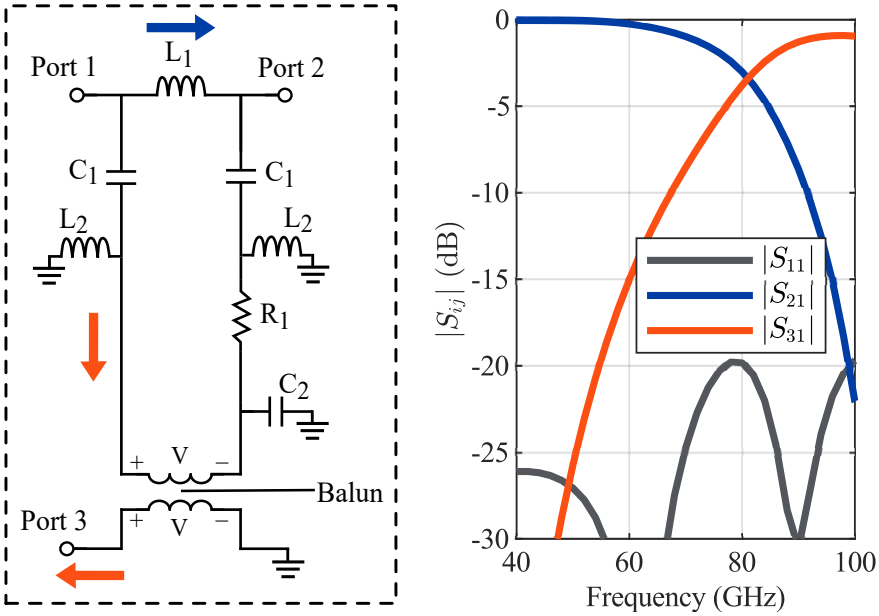


Figure 7.2: Ideal reflectionless diplexer filter circuit (left) and simulated S-parameter response (right). Low-band energy flows through low-pass circuit between ports 1 and 2, shown by blue arrow. The high-band energy flows through the high-pass path towards the ideal balun and exits out of port 3. The additional stop-band energy is terminated in the 50Ω resistor, R1.

At lower frequencies, the inductor L_1 behaves like a short, while the capacitor C_1 presents a high impedance. As a result, low-frequency signals pass directly from port 1 to port 2, as shown by the blue arrow. As described in [156], stop-band power is redirected to internal ports, so the circuit can also be viewed as a dual-directional diplexer. At higher frequencies, the capacitor C_1 behaves like a short, while the inductor L_1 presents a higher impedance. Consequently, high-frequency signals are routed toward port 3, as indicated by the orange arrow.

The high-frequency signal is first directed into an ideal balun, where it is splits 180° out of phase before

being recombined at port 3, which interfaces with the W–band PA input. The shunt capacitor C_2 acts as a frequency reflective element that reflects any high-pass signal that leaks through, while the resistor R_1 absorbs any remaining stop-band energy and reflections from port 2. The simulated S-parameters of the ideal diplexer demonstrate better than 20 dB return loss over 40–100 GHz, with a crossover loss of 3.3 dB.

A planar-Marchand balun is implemented using coupled microstrip lines and airbridges available in the foundry process similar to [159, 160]. Figure 7.3 shows the balun layout for the input diplexer with three ports labeled, ideal circuit in the upper right, and the simulated results at the bottom.

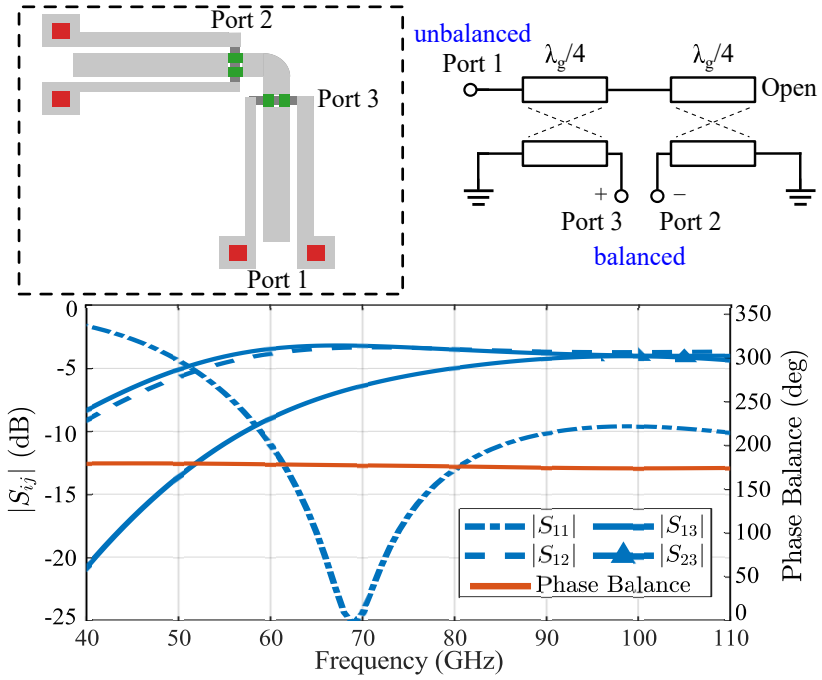


Figure 7.3: Planar Marchand balun circuit, layout and simulated response. Balun has to be bent to properly align with the filter. The balun size is 500 μm × 500 μm.

The unbalanced port (port 2) serves as the input for the high-band RF signal, which is coupled through the $\lambda_g/4$ transmission line sections and exits at ports 1 and 3 with a 180° phase difference. The S-parameters $|S_{12}|$ and $|S_{13}|$ exhibit an in-band loss of 3.3 dB at 75 GHz. The phase difference between S_{12} and S_{13}, plotted on the secondary (right) axis, is approximately 180°. The response $|S_{23}|$ indicates limited isolation between the output ports, which motivates the inclusion of a resistor between balun port 3 and filter port 2 to absorb undesired stop-band energy. The input return loss $|S_{11}|$ demonstrates good matching at the unbalanced port connected to the W–band PA. Although an ideal balun is fully symmetric, the implemented design is bent to

satisfy layout constraints imposed by the surrounding filter.

The fully EM-simulated filter and balun layout, along with the corresponding S-parameters, are shown in Fig. 7.4. Passive structures in the HRL T3 process, such as transmission lines and air bridges, are realized using two metallization layers, while resistors and capacitors are made from thin-film tantalum nitride (TaN) and silicon nitride (SiN), respectively. The ideal components from Fig. 7.2 are replaced with thin microstrip lines, MIM capacitors, TAN resistors, and shunt open stubs. The planar-marchand balun from Fig. 7.3 is incorporated and modified to meet layout constraints and design rule requirements. The overall structure is designed to maintain symmetry where possible, with the C_2 stub used to tune the filtering response.

A limitation of the design is the increased loss in the high-frequency band relative to the low-frequency band. The simulated S-parameter response, shown on the right side of Fig. 7.4, indicates a crossover magnitude of -4.3 dB at 82.3 GHz. The low-band insertion loss is 0.77 dB at 65 GHz, while the high-band insertion loss is 2 dB at 86 GHz and drops to 4 dB at 110 GHz. The input return loss $|S_{11}|$ remains better than 10 dB from 40–90 GHz.

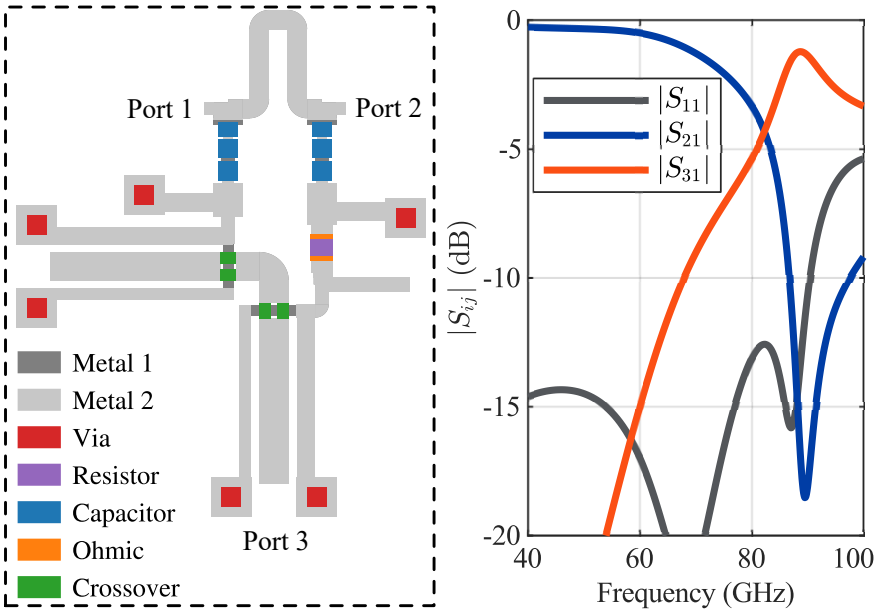


Figure 7.4: Layout of reflectionless diplexer filter circuit (left) and full–wave EM simulated S-parameter response (right). The filter size is $600\,\mu\text{m} \times 800\,\mu\text{m}$.

The measurement setup used for filter characterization consists of an HP 8510C Vector Network Analyzer with millimeter-wave extender heads covering 50–75 GHz and 75–110 GHz for small-signal measurements.

A photograph of the small-signal bench setup is shown in Fig. 7.5. Probing and measurement of the diplexer test structure are shown in the top left of Fig. 7.5. As with the coupled-line diplexer presented in Section II, simultaneous measurement of all three ports is not possible.

To take the measurement, additional microstrip lines and GSG pads are included into the filter test structure. The configuration shown in the top left of Fig. 7.5 measures S_{11} and S_{13} using a 100 μm GSG probe, while port 2 is terminated with a load connected via bond wires. The layout, small-signal simulation, and measurement results are presented in Fig. 7.6. The simulated response does not exactly represent the final design integrated filter due to the inclusion of the additional GSG pads and microstrip lines.Nevertheless, there is good agreement between simulation and measurement for the passive structure.

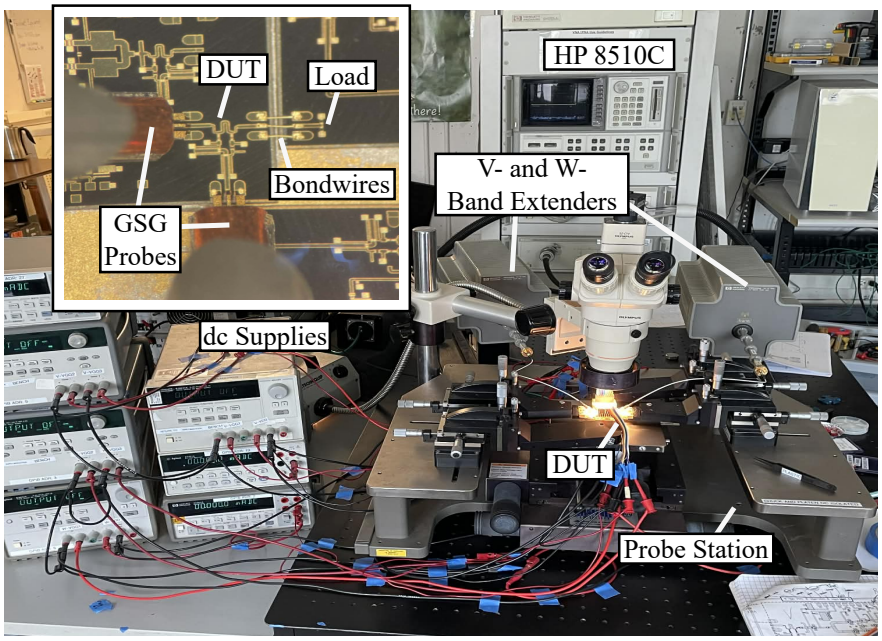


Figure 7.5: Small-signal bench and measurement setup at CU Boulder with the top left showing the filter test structure with port 2 bonded to a load termination with bondwires. Banded measurements for V– and W– are done by interchanging the millimeter-wave extender heads.

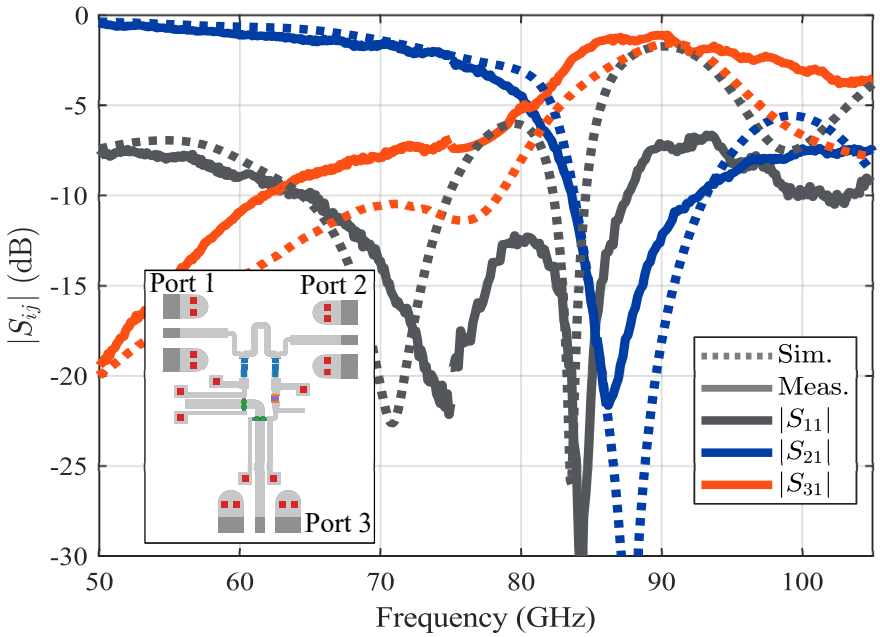


Figure 7.6: Diplexer test structure simulation vs. measurement with GSG test structure layout in the bottom left corner. The filter size is 900 μm $\times$ 1100 μm.

7.3 MMIC Power Amplifiers

The two power amplifiers are designed to cover portions of the V– and W–bands, respectively. Both amplifiers are implemented in the HRL T3 process, which features f_T/f_{max} = 160/360 GHz, a power density of 2 W/mm at 94 GHz, and a breakdown voltage exceeding 60 V [2]. The SiC substrate thickness is 50 μm (2 mil) thick. Circuit design is done in Cadence Microwave Office using a nonlinear Angelov model for the HEMTs. The design specifications are based on prior work using this process, as well as state-of-the-art V- and W-band MMIC results [105].

The PAs in this work employ three-stage topologies with reactive power combining to increase output power, resulting in a staging ratio of 1:2:4. The designs utilize a combination of 4 $\times$ 37.5 μm and 6 $\times$ 50 μm HEMTs, with the 6 $\times$ 50 μm devices used in the output stage. Additional driver stages are required to sufficiently saturate the output devices. The layout of the V–band PA is shown in Fig. 7.7. The dc bias pads are located at the top of the layout, and the bias line network includes multiple resistors and capacitors of varying sizes to provide isolation and suppress feedback between stages. A deconstructed view of the layout

is also provided, where key elements are highlighted in different colors and labeled for clarity.

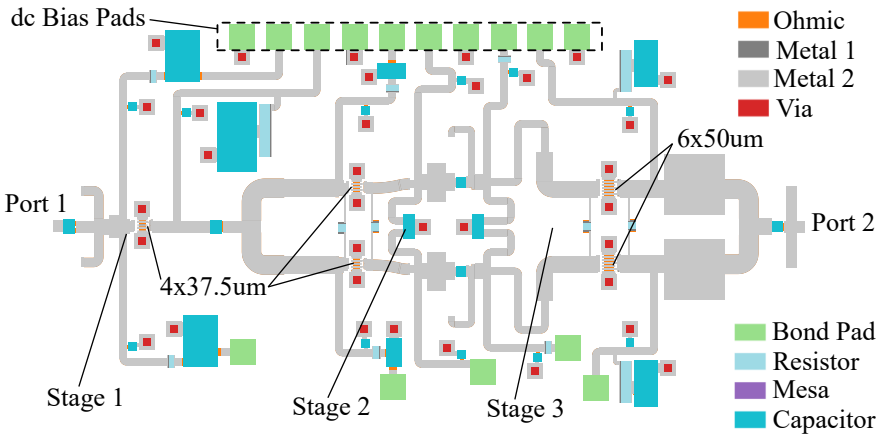


Figure 7.7: V–band PA layout. The size is 3.0 mm × 1.5 mm.

The W–band PA design is based on the core PA reported in [38], which is a three-stage PA fabricated in the same process (HRL T3) incorporating an integrated reconfigurable matching network at the output. Notably, a discrepancy between simulated and measured performance was observed in that work, attributed to shifts in intrinsic device parameters, as discussed in subsequent analysis (paper currently in review). In the present work, the simulation-to-measurement discrepancy for this PA is less pronounced, particularly in terms of bandwidth and gain magnitude, as confirmed by small-signal characterization.

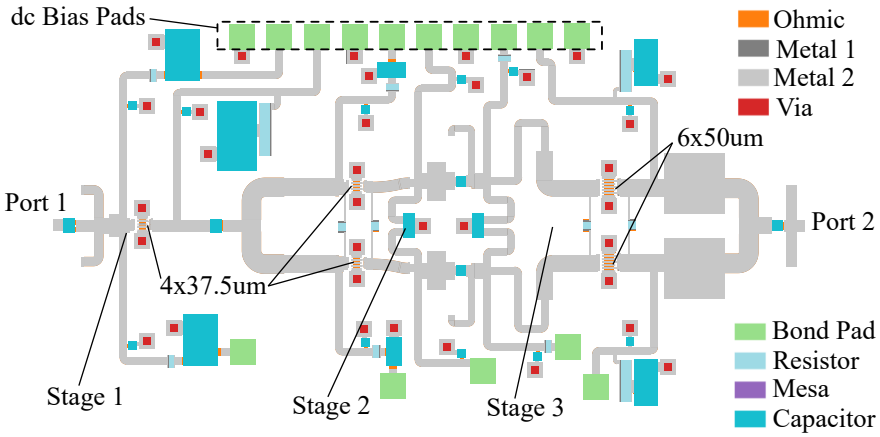


Figure 7.8: W–band PA layout. The size is 1.9 mm × 1.0 mm.

7.4 Integrated Diplexed MMIC PA

The integrated design consists of two PAs, symmetric filters, and microstrip transmission lines used to maintain in-phase operation at the crossover frequency, where constructive power combining is intended. A challenge in quasi-MMIC implementations such as the one in Chapter 6, is the interconnection of PAs and filters through bond wires, which are difficult to accurately model and can degrade performance. In contrast, the fully monolithic implementation presented in this Chapter enables more reliable integration of all components within a single process. The final layout of the integrated PAs and filters is shown at the bottom of Fig. 7.1. The lengths of the interconnecting microstrip lines are determined using the method-of-moments 2.5D AWR AXIEM solver, and are constrained by both the physical dimensions of the PAs and the required phase alignment in the crossover region.

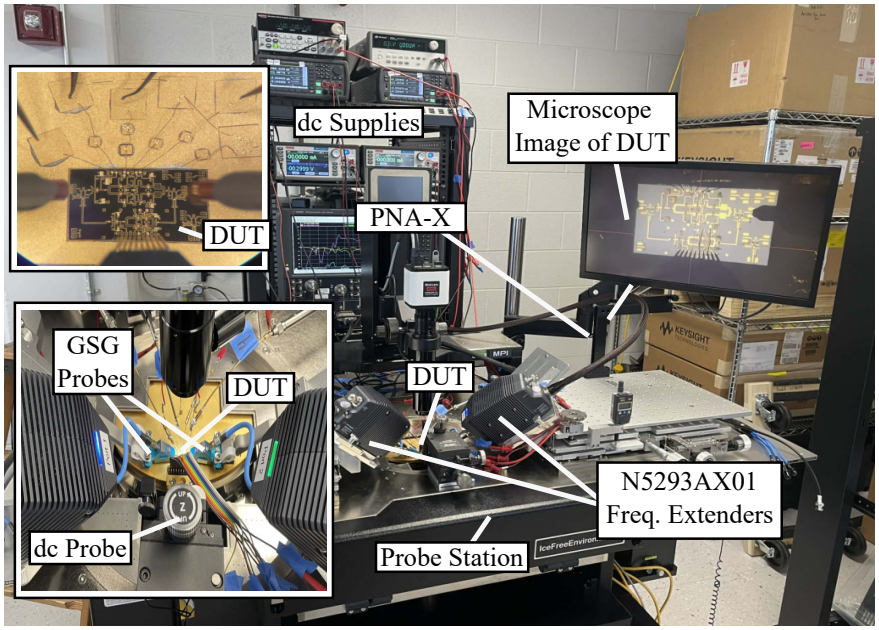


Figure 7.9: Small-signal bench and measurement setup with continuous 10 MHz to 110 GHz capability at Michigan State University (MSU) (courtesy of Prof. Nick Miller). The bottom left shows an expanded view of the DUT and GSG probes. The top left shows further expanded view of the DUT being probed on-wafer with CuMo carrier in the background.

Small-signal measurements of the integrated PA are performed using a Keysight PNA-X with N5293AX01 110 GHz frequency extenders, enabling continuous measurements from 10 MHz to 110 GHz. A photograph

of the measurement setup is shown in Fig. 7.9, with a microscope view of the DUT in the top left. The DUT is probed on-wafer with the backside ground connected to a CuMo carrier. The W–band PA is biased using a 10-element dc probe card, while the V–band PA is biased using dc probes with additional off-chip decoupling capacitors (100 pF and 1000 pF) to enhance stability.

The initial design of the V-band PA utilized a second 10-element DC probe card. However, the PA exhibited instability beyond a threshold current of 45 mA, originating from the interstage gate and drain nodes. An oscilloscope was connected to the suspected bias lines to identify potential low-frequency oscillations, but no instabilities were observed within the instrument operation frequency range. Additional off-chip RC elements, not shown, were then introduced between the DC probe connections and the DC supply; however, this approach did not resolve the issue.

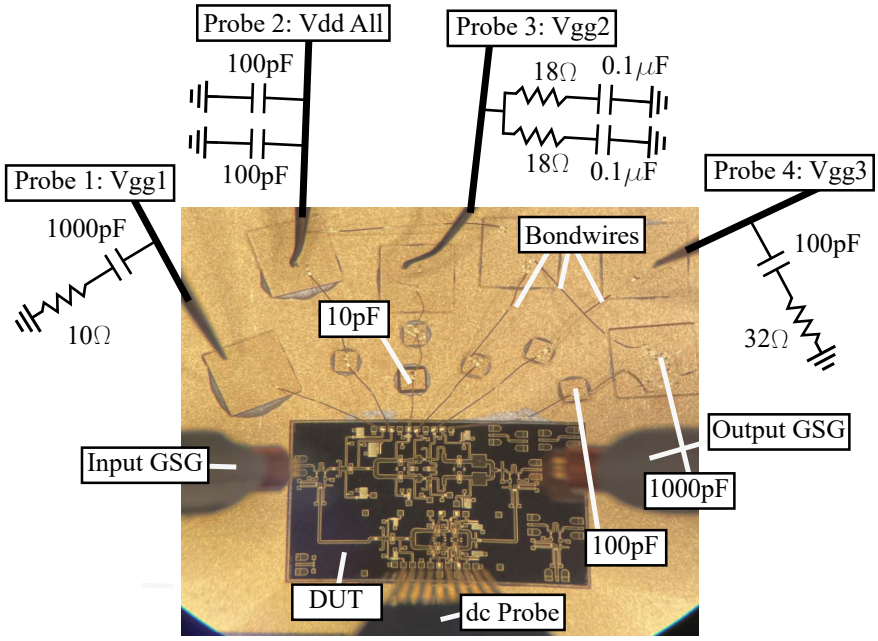


Figure 7.10: Small-signal bench and measurement setup with continuous 10 MHz to 110 GHz capability at Michigan State University (MSU) (courtesy of Prof. Nick Miller). The bottom left shows an expanded view of the DUT and GSG probes. The top left shows further expanded view of the DUT being probed on-wafer with CuMo carrier in the background.

Subsequently, single-layer capacitors were added directly to the CuMo carrier, along with DC probes incorporating additional damping components. The final configuration that stabilized the PA is shown in Fig. 7.10. This setup included DC probes with integrated RC elements, as well as bonded single-layer

capacitors of 100 pF and 1000 pF. The problematic interstage gate line was further stabilized by adding a 10 pF capacitor in addition to a parallel RC network consisting of two 18 Ω resistors and two 0.1 μF capacitors.

The simulated (dotted) and measured (solid) S-parameters are shown in Fig. 7.11 over 0.01–110 GHz. Both PAs are biased at a drain voltage of 12 V, with total drain currents of 90 mA for the V–band PA and 120 mA for the W–band PA. The amplifier shows at least 10 dB of small-signal gain from 44.5 to 88.5 GHz, corresponding to an absolute bandwidth of 44 GHz and a fractional bandwidth of 66 %. The input and output return losses, $|S_{11}|$ and $|S_{22}|$, also show good agreement, with some discrepancy observed in $|S_{22}|$ near 64 GHz. An additional resonance in $|S_{21}|$ near 44 GHz is attributed to the V–band PA interstage bias network. The PA remains stable with the external 100 pF and 1000 pF single layer decoupling capacitors added to the CuMo. Fig. 7.12 shows measured results from four chips, labeled, XII, IX, X, and VII (two from each wafer). The results show within 2-3 dB of separation across most of the band between the highest (XII) and lowest (IX) performing PAs.

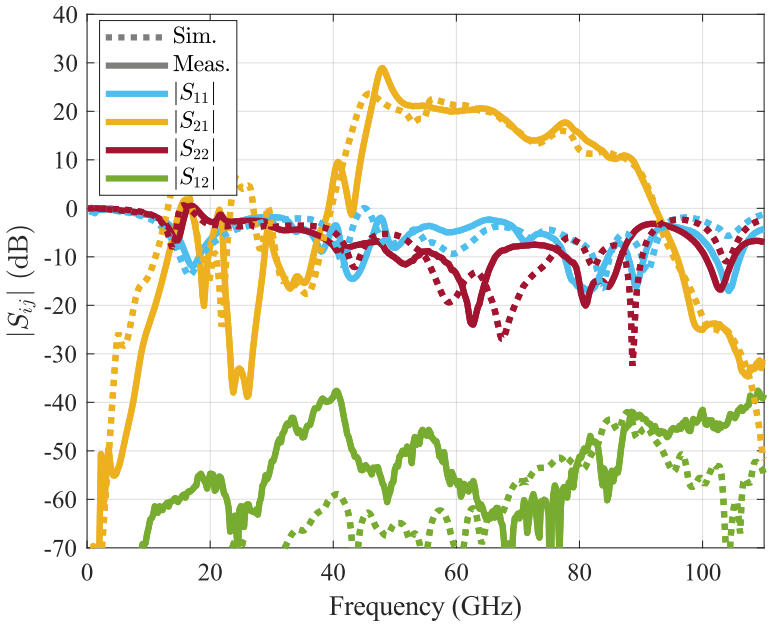


Figure 7.11: Simulated (dashed) vs measured (solid) small-signal S-parameters of a single well performing chip measured from 0.5–110 GHz. On-wafer measurements of the MMIC demonstrate small-signal gain of at least 10 dB from 44.5 to 88.5 GHz. This results in bandwidth of 44 GHz, or FBW of 66 %.

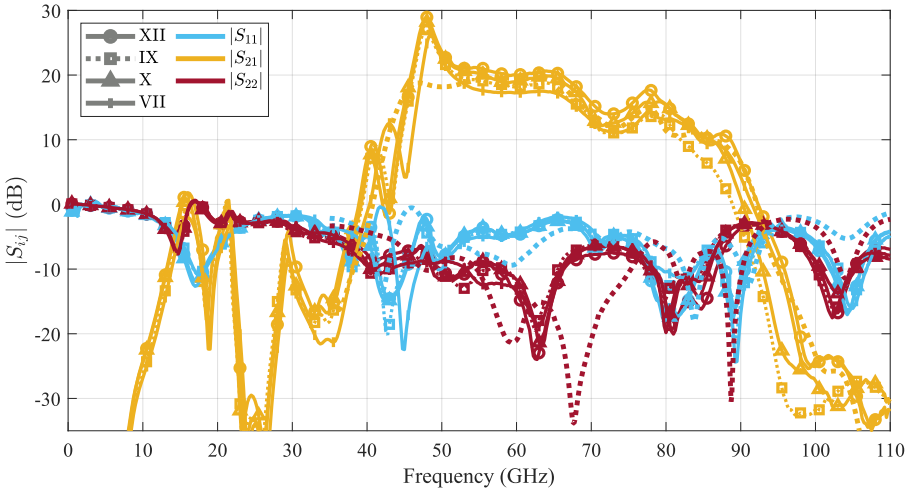


Figure 7.12: Simulated (dashed) vs. measured (solid) small-signal S-parameters from 0.1–110 GHz of four unique chips, two chips each from two different wafers.

7.4.1 Large-Signal Measurements

The large-signal measurements are performed using band-specific setups. The V–band measurements are obtained using the setup shown in Fig. 7.9, covering 50–75 GHz, with a maximum input power of 15 dBm at the DUT plane. This includes a ZVA-40703G+ driver amplifier, which is de-embedded to the DUT reference plane. A simplified block diagram for the W–band large signal measurement setup located at CU Boulder is shown in Fig. 7.13. The W–band large-signal setup is pictured in Fig. 7.14, covering 75–95 GHz, with a maximum available input power of 10–11 dBm at the DUT plane.

The corresponding full-band response, combining both measurement setups under identical bias conditions of 200 mA/mm and an input power of 11 dBm, is shown in Fig. 7.15. The PA delivers ≥20 dBm of output power from 45.5–88.2 GHz. This operating point does not correspond to saturation or peak PAE, but reflects the maximum available input drive in the W–band measurement setup. The measured performance demonstrates power gain exceeding 10 dB across a fractional bandwidth of approximately 64 %, nearly an octave.

The measured drive-up curves for both PAs, each biased at their respective optimum operating conditions,

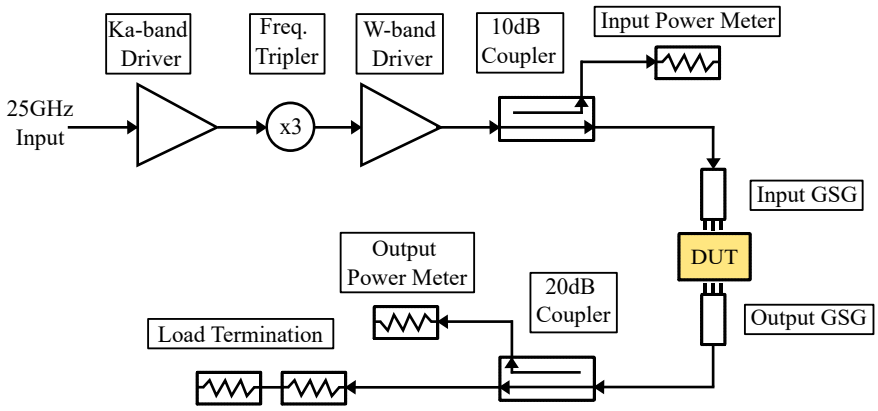


Figure 7.13: Large-signal W-band simplified block diagram. The input signal is generated by a K/Ka-band source and amplified by a Ka-band driver. It is then passed through a passive W-band frequency tripler and subsequently amplified by a W-band driver. A portion of the signal is coupled off to an input power meter, while the main signal is delivered to the DUT input. At the output of the DUT, a 20 dB coupler is used to measure the output power, and the remaining power is absorbed by a W-band termination.

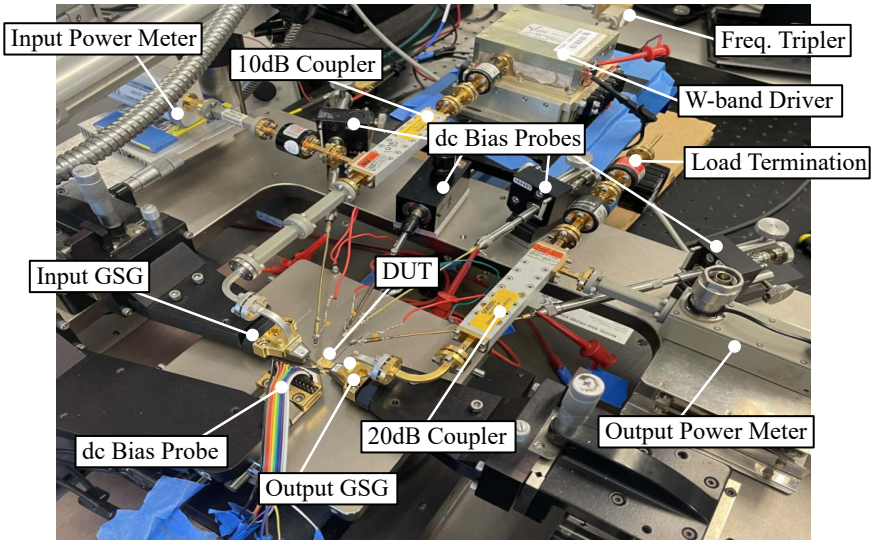


Figure 7.14: Large-signal measurement setup for 75–95 GHz. This figure shows an image of the block diagram from Fig. 7.13.

are shown in Fig. 7.16. For clarity, only the simulated curve for the W–band PA is included to illustrate model agreement and simulated saturation behavior. The V–band PA achieves a P_{sat} of 27.8 dBm (0.6 W), a PAE of 20.1 %, and a power gain of 13.5 dB at 64 GHz with an input power of 15 dBm. The W–band PA reaches peak PAE in simulation at an input power of 20 dBm.

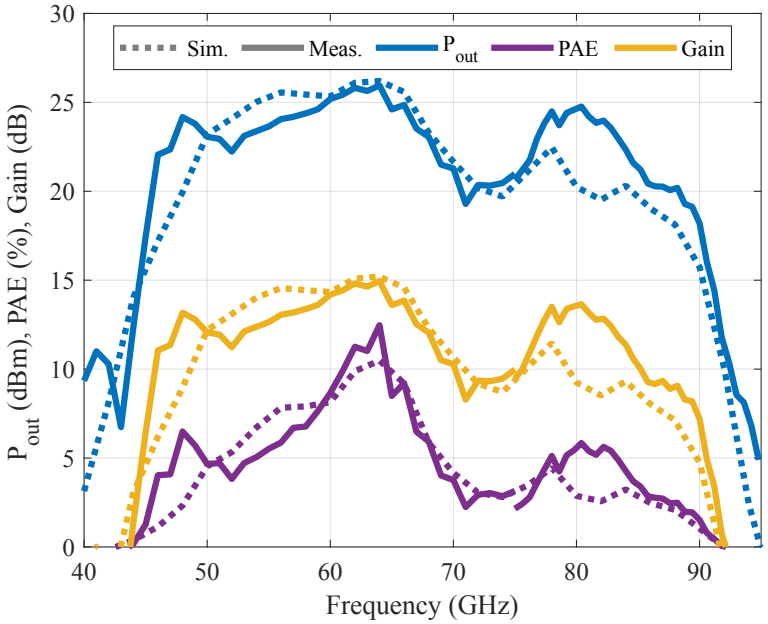


Figure 7.15: Simulated (dashed) vs. measured (solid) large-signal S-parameters for 11 dBm input power. Here the PA is operating in contiguous mode where both PA paths are biased on, in this case at 200 mA/mm per stage.

The full-frequency performance in both low– and high–band operating modes, with the respective PA paths biased ON and OFF, is shown in Fig. 7.17. The low–band mode response (left) is measured at an input power of 15 dBm and is limited by the available drive capability up to 75 GHz. This result highlights the reconfigurable operation of the PA, where performance in a given band can be optimized by deactivating the alternate signal path. The high–band mode response (right) shows good agreement between simulation and measurement and is limited by drive power to 11 dBm of input power.

A comparison with SOTA GaN power amplifiers operating in the E–band is summarized in Table 7.1. The work in [151] presents an f_T-doubler broadband amplifier and is the only example exhibiting a larger fractional bandwidth over a comparable frequency range. However, that design is not a conventional power amplifier and demonstrates lower performance in terms of PAE and P_{sat}. Several prior works [161–164] achieve higher P_{sat}, but at the expense of significantly larger chip area. Other designs [165–167] demonstrate comparable output power and slightly higher PAE, but with substantially reduced fractional bandwidth compared to this work.

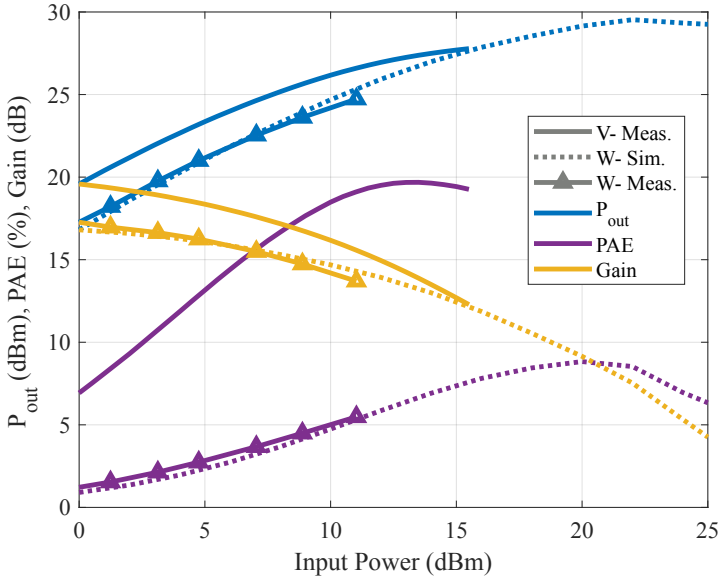


Figure 7.16: Simulated (dotted) vs. measured (solid) large-signal driveup curves with both amplifiers and all stages biased at 200 mA/mm. The V–band data is at 64 GHz and the W–band curve is at 78 GHz.

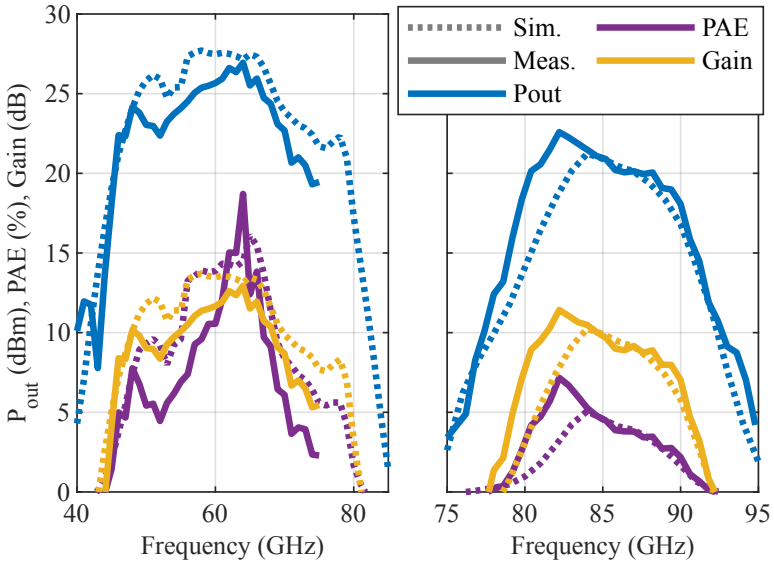


Figure 7.17: Low-band mode at an input power of 15 dBm (left) and high-band mode at an input power of 11 dBm (right).In both plots the other PA is biased OFF.

Table 7.1: Comparison of State-of-the-Art GaN Power Amplifiers at E-band

Ref. (#)	Freq. (GHz)	FBW (%)	Pk. PAE (%)	P_{sat} (dBm)	Pk. $\lvert S_{21}\rvert$ (dB)	Area (mm^2)	Tech.	Topology
[151]*	28–90	105	4.4	20.6	19	4.5	100-nm GaN	fT-Doubler
[161]	71–85	18	22	34	19.6	7.44	100-nm GaN	Class-AB
[161]	71–85	18	15.3	36	15	15.43	100-nm GaN	Balanced
[162]	71–86	19	9.5	31.8	25	–	100-nm GaN	–
[163]	68–86	23	18.5	36.4	26	16.25	100-nm GaN	Balanced
[164]	69–76	10	22.5	35.7	–	16.5	100-nm GaN	Doherty
[165]	60	–	28.9	27.8	–	2.25	100-nm GaN	Doherty
[166]	71–74.5	5	34	29	11	1.92	40-nm GaN	Doherty
[167]	79–95	18	27.8	31.1	23^{+}	–	40-nm GaN	Class-AB
T.W.	**45.5–88.5**	**64**	**20.1**	**27.8**	**29**	**6.27**	**40-nm GaN**	**Diplexed**

* Broadband Amplifier

$^{+}$ Estimated from plots in the references

7.5 Conclusion

This chapter presents an E–band diplexed MMIC GaN power amplifier that monolithically integrates two multi-stage PAs using reflectionless diplexer filters.

As discussed in Chapter 6, employing identical staging ratios for both the low-band and high-band PAs is suboptimal for this topology. Future iterations should consider increasing the periphery or the number of stages in the high-band path to better balance performance. However, this approach introduces additional design complexity, as stability considerations at these frequencies become significantly more challenging than in lower-frequency designs. This trade-off warrants further investigation in future work.

The MMIC presented in this chapter demonstrates competitive performance compared to state-of-the-art designs. In particular, it achieves one of the largest FBWs reported, while maintaining a high peak PAE relative to works with comparable chip area and output power. The contributions of this Chapter form the second half of the manuscript entitled *Integrated X- to W-band Diplexed Power Amplifiers*, which is currently in preparation for submission to the IEEE Transactions on Microwave Theory and Techniques.

Chapter 8

Conclusions and Future Work

8.1 Thesis Summary

This thesis presents the design of GaN-on-SiC power amplifiers. The demonstrated PAs span 1-95 GHz and focus on PAE, bandwidth, output power, reconfigurability, and supply modulation. This begins with multi-objective analysis techniques and progresses toward millimeter-wave implementations.

Chapter 2 introduces multi-objective visualization (MoV) for power amplifier design and presents two distinct methods. The first, the *Load-Pull Extraction* method, is applied to two hybrid S-band PAs and an X-band MMIC PA, with simulation results validated against measurements. In Chapter 3, MoV is extended to more unique trade-offs using the *Selective Trade-Off* method, including component sensitivity analysis and multi-stage PA design. The X-band MMIC from Chapter 2 is further analyzed through sensitivity studies of dielectric capacitor shunt matching elements, along with supply modulation measurements demonstrating system-level and PA PAE improvements. Additionally, the method is applied to a multistage Ku-band design using manual load-pull to capture bilateral transistor effects.

Chapter 4 shifts focus to millimeter-wave designs, presenting a narrowband W-band PA implemented in the Qorvo GaN09 90-nm process that is still underdevelopment. Despite PDK limitations restricting architectural complexity, the three-stage design achieves improved $|S_{21}|$ agreement with simulation compared

to prior work [80] in this process. Chapter 5 presents a second W-band three-stage GaN PA in the HRL T3 process, incorporating an on-chip reconfigurable matching network and a detailed W-band stability analysis. Additionally small-signal model discrepancy evaluation through parameter extraction is done in collaboration with the foundry, resulting in improved agreement between simulation and measurement.

To demonstrate broad bandwidth, a diplexed PA architecture is developed in Chapters 6 and 7. Chapter 6 introduces a quasi-MMIC GaAs/GaN diplexed PA spanning Ku-, K-, and lower Ka-band frequencies. The GaN PAs and GaAs diplexers are integrated via wire bonding, with measured results showing strong agreement with simulation. Finally, Chapter 7 presents a fully integrated GaN diplexed PA covering 45–90 GHz using a reflectionless diplexer topology to mitigate stop-band impedance interactions and improve stability. This design demonstrates state-of-the-art fractional bandwidth and PAE performance relative to comparable GaN PA works at E–band.

8.2 Future Work

The work presented in this thesis provides several paths for future work. For example, the MoV method can be applied to additional design problems and specifications. Additionally, a second tapeout in the GaN09 process, is completed and currently in fabrication. Extended measurements are also recommended for the millimeter-wave amplifiers.

8.2.1 Multi-Objective Visualization Method Extensions

The MoV method presented in this thesis establishes a general framework for PA design and demonstrates its effectiveness across a wide range of power levels, applications, and technologies. Beyond these examples, the method naturally enables a broad set of extensions. In particular, the development of a graphical user interface (GUI), shown in Fig. 8.1 is integrated with AWR and the MoV environment allows designers to rapidly explore trade-offs and significantly reduce design iteration time. The instructions and code for the GUI are located in the Appendix.

Several immediate extensions build upon the hybrid PA design introduced in Chapter 2, which incorpo-

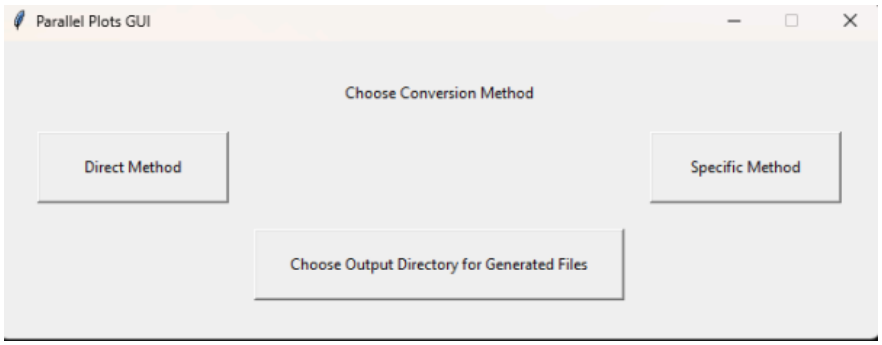


Figure 8.1: Screenshot of the graphic user interface (GUI) created to interface with AWR and speedup MoV plot creation by direct interaction with AWR. The *Load-Pull Extraction* method is called the Direct Method and the *Selective Trade-Off* method is called the Specific Method in the GUI

rates the nodal Q-factor of the load reflection coefficient. A direct extension is the inclusion of the source reflection coefficient Q-factor, enabling more informed impedance selection in the context of fundamental Bode–Fano matching limits. Further refinement could include explicit modeling of matching network component Q-factors, allowing designers to evaluate trade-offs between loss and matching network complexity.

The hybrid PA in Chapter 2 also incorporates harmonic load- and source-pull at the second and third harmonics of a packaged GaN HEMT. Extending this approach to MMIC bare-die devices in well-characterized processes would enable improved PAE by removing package-related parasitics that constrain harmonic terminations. This behavior is partially observed in the wide range of achievable third-harmonic impedance angles in that work. A natural progression is the simultaneous inclusion of fundamental and harmonic load- and source-pull data within a unified MoV framework, enabling more accurate co-analysis with improved representation of bilateral device effects.

More future work is the demonstration of MoV at the earliest stage of device selection. Key transistor parameters such as, bias conditions, gate width, and finger count could be evaluated alongside performance metrics such as efficiency and output power to guide optimal device sizing and stability trade-offs. This concept can be further extended to process-level comparisons, incorporating parameters such as gate length, wafer size, fabrication cost, timeline, f_{T}, and operating voltage. In this context, the *Selective Trade-Off* method is particularly well suited for enabling high-level, system-aware design decisions.

8.2.2 Second Qorvo GaN09 Tapeout

A second GaN09 tapeout was completed to evaluate process evolution and to further investigate the gain discrepancy previously attributed to g_m overestimation in the device models used from [80]. This tapeout was submitted in March 2025 and included updated nonlinear models, allowing for more complex PA architectures. The full reticle, shown in Fig. 8.2, takes up an area of 5 mm×5 mm. It includes a redesigned unit PA carried over from the previous tapeout, discussed in [80], which was reimplemented with minor modifications to the matching networks to account for updated model characteristics. Additional structures in this tapeout include an on-chip TRL calibration structure and several reconfigurable matching network PAs, following a similar topology to those presented in Chapter 5. These additions aim to provide further insight into model accuracy, scalability of design methodologies, and the performance of adaptable matching strategies in the updated process.

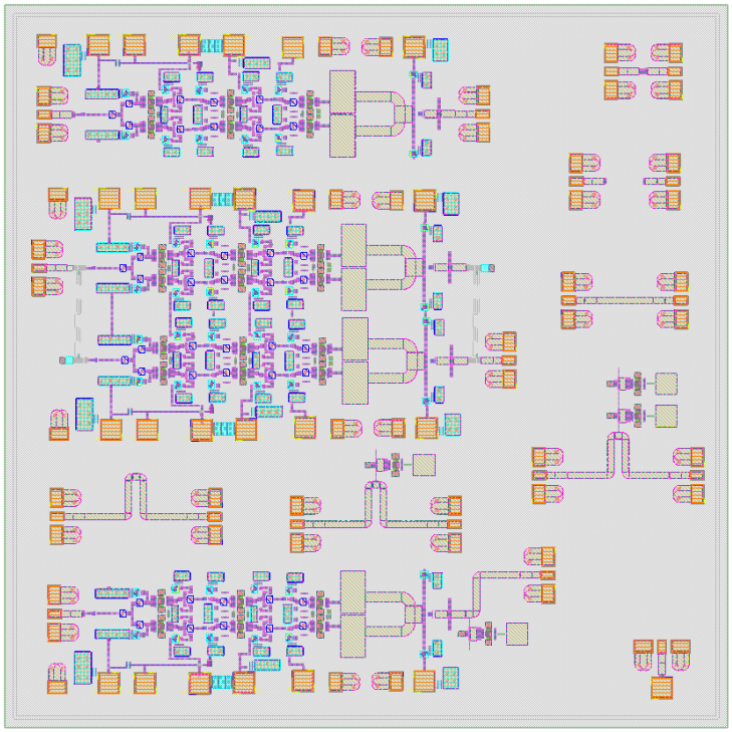


Figure 8.2: Second Qorvo GaN09 tapeout reticle (5 mm×5 mm). Several PA matching networks are re-spun and adapted for the latest $4\times40\,\mu$m and $6\times40\,\mu$m HEMTs. The reticle includes a core three-stage PA, a balanced PA, reconfigurable matching network PAs, test structures, and on-chip TRL calibration structures.

8.2.3 Measured W–Band Reconfigurable Loads

This future work builds upon the results presented in Chapter 5, which investigated a narrowband W–band GaN PA incorporating an on-chip reconfigurable matching network (RMN). Due to reticle area constraints and the lack of available W–band load-pull tuner equipment, experimental validation of reconfigurable load conditions using the RMN was not performed. A followup tapeout would allow the inclusion of several key structures to support this study. These include a 50 Ω core PA to serve as a baseline reference, a standalone RMN with GSG pads for independent characterization, and an updated RMN-integrated PA. In addition, dedicated test structures for the FETs used in the PAs should be included.

The proposed measurement procedure is as follows. First, the FETs would be characterized under small-signal conditions over a frequency range of 0.1–110 GHz and compared against simulated results to assess model accuracy. Next, the core PA would be measured to establish baseline performance under a 50 Ω load condition. With access to a W–band load-pull tuner, a range of non-50 Ω load impedances with varying phase angles could then be presented to both the core PA and the RMN-integrated PA. This approach enables direct comparison between the baseline PA performance and the performance achievable through impedance transformation using the RMN. These measurements would provide the missing information about the effectiveness of on-chip reconfigurable matching networks at W–band frequencies. Finally, future iterations could explore more complex RMN implementations using larger device peripheries to expand the achievable tuning range, with the tradeoff of added loss.

8.2.4 Extended Measurement and Scaling of Diplexed PAs

The diplexed PAs presented in Chapters 6 and 7 would benefit from measurement validation under multi-signal excitation. A key advantage of this topology for linearization is the inherent isolation between PA branches, which prevents interaction of mixing products generated by different signals. As a result, digital predistortion (DPD) can be significantly simplified compared to the case where multiple signals are amplified by a single broadband PA.

This benefit was not experimentally demonstrated in this work due to measurement limitations. However,

prior work at S–band has shown successful linearization of diplexed PA architectures under multi-signal operation [133]. Extending this validation to higher carrier frequencies is a natural next step, particularly in the E–band, where larger absolute bandwidths enable multi-channel transmission scenarios. This is especially relevant for emerging applications spanning the V– and W–band frequency ranges, where high throughput satellite communication systems are of increasing interest [168].

Beyond measurement validation, the diplexed PA architecture also lends itself to scalable extensions through the incorporation of additional multiplexed PA branches. As discussed in [133], multiple PAs can be combined using frequency-selective networks to enable simultaneous amplification across a wider aggregated bandwidth. For example, a multi-branch architecture could be designed to cover the full W–band by partitioning it into four different sub-bands, each serviced by an optimized narrowband PA.

Such an approach introduces additional design complexity in the multiplexing network and imposes tradeoffs between bandwidth, loss, and isolation. However, it offers a path toward highly efficient, wideband transmitters that retain the linearization advantages of isolated signal paths. Future work should explore these architectures in conjunction with advanced filtering and combining techniques to balance these competing requirements.

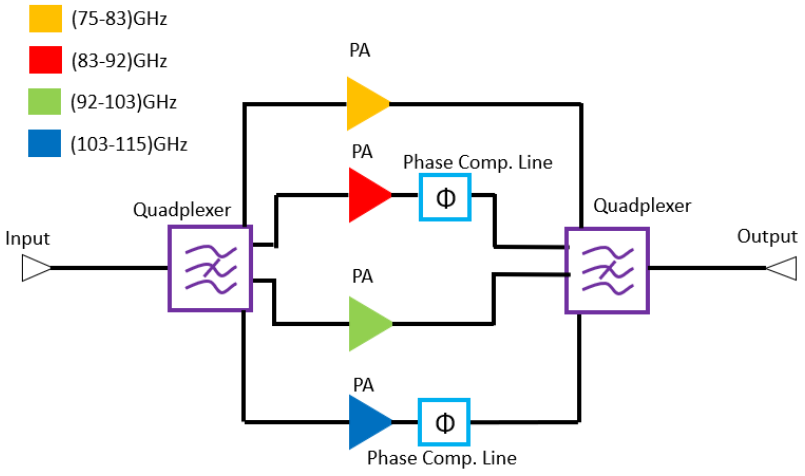


Figure 8.3: Conceptual multi-branch diplexed W–band architecture. Narrowband, high-efficiency PAs are combined using a quadplexer to enable simultaneous amplification of multiple signals across W–band, while maintaining linearity through isolated signal paths.

8.3 Summary of Contributions

This thesis has led to several contributions in the area of multi-objective power amplifier design and millimeter wave GaN PA designs. They are summarized as follows.

A multi-objective visualization (MoV) method for PA design is introduced in Chapter 2 that enables quick trade-off analysis at various stages of PA design. The *Load-Pull Extraction* method is used to determine optimal impedance regions early in the design process from simulated load- and source-pull data. Extensions including impedance Q factor and harmonic phase analysis are added. The method is validated with a 6 W wideband GaN PA achieving 58 % peak PAE over 1.9–3.6 GHz with 61.8 % fractional bandwidth. These results are reported in [68–70]. The *Selective Trade-Off* (STO) method, presented in Chapter 3, is developed as an extension of MoV for unique trade-off scenarios at various points during a PA design. Some examples demonstrated are an interstage matching design using bilateral load- and source-pull data. A component sensitivity metric is introduced to account for process variation. The method is applied to X-band and Ka-band GaN MMIC PAs, including a supply-modulated design that demonstrates improved average efficiency for high PAPR signals. These results are reported in [69, 70] and an unpublished GOMACTech 2024 conference paper entitled, *PA and Supply Modulator GaN MMICs for Efficient High-PAE Signals in the 8–14 GHz Band.*

The millimeter-wave PAs are presented next starting in Chapter 4 with a W-band GaN PA in a 90 nm process. The design goal is to demonstrate process model status and compare to previous iterations of this developmental process. The current version of the nonlinear model was shown to overestimate gain by approximately 4 dB. A cascaded six-stage architecture is implemented to achieve additional drive power, demonstrating measured output power near 200 mW. These results are reported in [81]. Another W-band GaN PA is presented in Chapter 5 that includes an integrated reconfigurable matching network (RMN) integrated into the PA OMN. The three-stage design achieves 25.3 dBm output power, 13.3 dB gain, and 11 % PAE at 77.2 GHz. A detailed analysis of RMN behavior, process variation, and model discrepancies is performed, providing insight into reconfigurable matching at millimeter-wave frequencies. These results are reported in [38] and an IET journal article currently in review entitled *Analysis of an Impedance-Adaptive*

W-band GaN MMIC Power Amplifier .

A wideband diplexed PA architecture is presented in Chapters 6 and 7. The first design is a quasi-MMIC PA demonstrated by combining GaAs diplexer filters with GaN PAs to enable wide–, low–, and high–band operation with a single RF input and output. The design achieves wide fractional bandwidth with an efficiency enhancement mode in sub-bands. Design trade-offs in staging and filter crossover are identified. Finally, an E-band diplexed GaN MMIC PA is demonstrated with monolithic integration of dual-band multi-stage PAs using reflectionless filters. The design achieves one of the largest reported fractional bandwidths while maintaining high peak PAE for comparable output power and chip area. The work included in Chapters 6 and 7 form a manuscript entitled *Integrated X- to W-Band Diplexed Power Amplifiers*. This journal paper is currently in preparation for submission to the IEEE Transactions on Microwaves Theory and Techniques.

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Appendix A

Multi-Objective Visualization: Graphic User Interface

A graphical user interface (GUI) was developed to enable rapid generation and analysis of parallel plots through direct integration with Cadence Microwave Office (AWR). The GUI is implemented in Python, with the full code provided in Appendix A.2, along with a set of tutorial videos demonstrating its use.

The underlying methodology is based on multi-objective analysis, allowing the designer to identify multiple solutions that satisfy predefined requirements while balancing competing performance objectives. Simulation data is processed and presented in an interactive format, significantly reducing the time required for trade-off evaluation and improving design intuition.

The GUI supports two primary methods. The first, the *Load-Pull Extraction* method (referred to as the *Direct Method* in the GUI), operates on simulated source- and load-pull data across a wide parameter space to identify optimal impedance regions. The second, the *Selective Trade-Off* method (referred to as the *Specific Method* in the GUI), extends this approach to targeted design scenarios, such as sensitivity analysis and multi-stage amplifier optimization.

A.1 GUI Download

Additional guidance for using the GUI is provided through a set of tutorial videos included with the download and accessible online at [169]. The six videos are intended to be viewed sequentially and cover the following topics: Multi-Objective Visualization Background, GUI Download Instructions, Direct Method, Example Project, Specific Method Sweep Interface, and Specific Method Additional Examples.

A 19-page PDF manual, entitled *Parallel Plots GUI Instruction Manual*, is also provided for further reference. The GUI, tutorial videos, and user manual are available for download on GitHub at [170].

A.2 Code

Included below is the python code used for the GUI. Special thanks to Dr. Jacob Kravits and Scott McCall for their assistance with this project.

```
#need to install pyawr

#pip install pywin32
#cd AppData\Local\Programs\Python\Python39\Lib\site-gridages\win32com\client (if using less
    than Python 3.9.5)
#python .\makepy.py
#select AWR Design Environment

#pip install pyawr

from operator import truediv
from tkinter import *
from tkinter import filedialog
from tkinter import messagebox
from tkinter import ttk
import pyawr.mwoffice as mwo
import os
import time
import ast
import pandas as pd
import numpy as np
import mopa
import threading
import multiprocessing
import webbrowser
import paxplot
import sys
import matplotlib.pyplot as plt


app = mopa.app.create_dashboard()
def run_parallel_plots():
     app.run_server()

def launch_parallel_plots():
     webbrowser.open("http://127.0.0.1:8050")

```

```
#awrde = mwo.CMWOffice(version='17.0') #may need to account if user has multiple installs

##Design Notes
#Most SAX Basic commands are Project.XXXX
#In Python, we need to use awrde variable as follows: awrde.Project.XXXXX
#can also do project = awrde.Project        #Create "project" variable as a convenience item and then do project.XXXXX similar to SAX Basic

# NumSchem = awrde.Project.Schematics.Count
# for s_idx in range(NumSchem):
#     schem = awrde.Project.Schematics[s_idx]
#     print(schem.Name)

t1 = threading.Thread(target=run_parallel_plots)
# t1 = multiprocessing.Process(target=run_parallel_plots)
t1.daemon = True
t1.start()

print("Launching GUI")
awrde = None
modify_measurement_button = None
lp_script_button = None
choose_file_button = None
export_mdf_box = None
isExampleProject = False
graph_name = ""
measurement_name = ""
frame_bg_color = "#f0f0f0"
# frame_bg_color = "#000080"
widget_pad_default = 10
frame_pad_default = 20
output_directory_path = os.getcwd() + "/"
schematic_list = []
current_schematic = ""
current_tabular = ""
check_button_correlator = []
temp_elements = []
tabular_dropdown = None
```

```
74 schematic_dropdown = None
75 graph_index = 1
76 file_creation_label = None
77 debug = True
78
79 if len(sys.argv) == 1 or sys.argv[1] != "--debug":
80      debug = False
81
82 def debug_print(msg):
83      if debug == True:
84           print(msg)
85
86 def step_1_instructions():
87      step_1_instructions_string = "Option␣1:␣Open␣\"Parallel_Plot_Example_New.emp\"␣in␣AWR."
88      step_1_instructions_string = step_1_instructions_string + "␣Enter␣values␣in␣the␣boxes␣
          below␣and␣click␣\"Run␣Load␣Pull␣Script\"␣to␣launch␣Load␣Pull␣GUI␣for␣schematic␣\"
          Load␣Pull␣Template\".\n\n"
89      step_1_instructions_string = step_1_instructions_string + "Option␣2:␣Convert␣MDF␣file␣to
          ␣.txt␣file␣containing␣tabular␣data␣for␣PAE␣or␣output␣power."
90      messagebox.showinfo(title="Step␣1␣Instructions", message=step_1_instructions_string)
91
92 def step_2_instructions():
93      step_2_instructions_string = "Enter␣values␣below␣to␣run␣manual␣sweep␣for␣schematic␣\"
          Manual␣SP␣and␣LP␣Setup\"."
94      step_2_instructions_string = step_2_instructions_string + "␣Each␣parameter␣is␣optional.␣
          Use␣the␣checkboxes␣to␣enable␣each␣different␣variable␣sweep␣in␣AWR."
95      step_2_instructions_string = step_2_instructions_string + "␣It␣is␣not␣possible␣to␣modify
          ␣just␣one␣parameter␣for␣each␣sweep.␣Make␣sure␣Start,␣Stop,␣and␣Step␣are␣all␣valid␣
          numbers␣for␣desired␣sweeps.\n\n"
96      step_2_instructions_string = step_2_instructions_string + "␣Enter␣desired␣graph␣name␣and
          ␣click␣\"Run␣Manual␣Sweep\"␣to␣generate␣tabular␣data␣for␣PAE␣and␣output␣power␣(other
          ␣measurements␣will␣be␣added␣later)."
97      step_2_instructions_string = step_2_instructions_string + "␣Once␣tabular␣data␣has␣been␣
          created,␣enter␣a␣file␣name␣to␣export␣trace␣data␣to␣a␣.TXT,␣if␣desired."
98      messagebox.showinfo(title="Step␣2␣Instructions", message=step_2_instructions_string)
99
100
101 def populate_sweep_variables(*args):
```

```
102     global check_button_correlator
103     global temp_elements
104     global cTableContainer
105
106     for element in temp_elements:
107         element.grid_forget()
108     schem = awrde.Project.Schematics(current_schematic.get())
109     swpVarNames = []
110     swpVarIDs = []
111     for element in schem.Elements:
112         debug_print(element.Name)
113         if "SWPVAR" in element.Name:
114             swpVarNames.append(element.Parameters('VarName').ValueAsString)
115             swpVarIDs.append(element.Name)
116     debug_print(swpVarNames)
117     check_button_correlator = []
118     current_row = 4
119     for value in swpVarNames:
120         toggled = IntVar()
121         swpVarToggle = Checkbutton(master = sweeps_global_frame, text = value, variable =
              toggled, justify="left", command=toggle_checkbox)
122         swpVarStart = Entry(master=sweeps_global_frame)
123         swpVarStop = Entry(master=sweeps_global_frame)
124         swpVarStep = Entry(master=sweeps_global_frame)
125         check_button_correlator.append((toggled, swpVarIDs[swpVarNames.index(value)],
              swpVarStart, swpVarStop, swpVarStep))
126         swpVarToggle.grid(row=current_row, column=0, padx=widget_pad_default, pady=
              widget_pad_default)
127         swpVarStart.grid(row=current_row, column=1, padx=widget_pad_default, pady=
              widget_pad_default)
128         swpVarStop.grid(row=current_row, column=2, padx=widget_pad_default, pady=
              widget_pad_default)
129         swpVarStep.grid(row=current_row, column=3, padx=widget_pad_default, pady=
              widget_pad_default)
130         temp_elements.append(swpVarToggle)
131         temp_elements.append(swpVarStart)
132         temp_elements.append(swpVarStop)
133         temp_elements.append(swpVarStep)
```

```
134
135           current_row=current_row+1
136       toggle_checkbox()
137       populate_tabulars()
138       cTableContainer.update_idletasks()
139       sweeps_global_frame.update()
140       cTableContainer.config(scrollregion=sweeps_global_frame.bbox())
141
142
143 def change_output_directory():
144       global output_directory_path
145       output_directory_path = filedialog.askdirectory()
146       debug_print(output_directory_path)
147       output_directory_path = output_directory_path + "/"
148
149 def export_mdf_file():
150       global root
151       popup = Toplevel(root)
152       popup.resizable(False, False)
153       popup.title("Choose␣MDF␣and␣File␣Name")
154
155       mdf_label = Label(master = popup, text="MDF␣File␣Name␣(in␣AWR)")
156       mdf_entry = Entry(master = popup)
157       destination_label = Label(master = popup, text="Destination␣File␣Name")
158       destination_entry = Entry(master = popup)
159
160       mdf_label.grid(column=0, row=0, padx=widget_pad_default, pady=widget_pad_default)
161       mdf_entry.grid(column=0, row=1, padx=widget_pad_default, pady=widget_pad_default)
162       destination_label.grid(column=2, row=0, padx=widget_pad_default, pady=widget_pad_default
              )
163       destination_entry.grid(column=2, row=1, padx=widget_pad_default, pady=widget_pad_default
              )
164
165       def export_mdf():
166
167            print("Exporting␣MDF...")
168            destination_filename = destination_entry.get()
169            if (not destination_filename.endswith(".mdf")):
```

```
170                 destination_filename = destination_filename + ".mdf"
171             awrde.Project.DataFiles(mdf_entry.get()).Export(output_directory_path +
                    destination_filename)
172             popup.destroy()
173
174         export_button = Button(master=popup, text="Export", command=export_mdf)
175         export_button.grid(row = 2, column = 1, padx=widget_pad_default, pady=widget_pad_default
                )
176
177 def convert_mdf_file():
178         global root
179         global output_directory_path
180         mdf_file_name = filedialog.askopenfilename(filetypes = [("MDF␣Files","*.mdf␣*.mdif")])
181         debug_print(mdf_file_name)
182         if mdf_file_name == "":
183             return
184         popup = Toplevel(root)
185         # popup.geometry("200x100")
186         popup.resizable(False, False)
187         popup.title("Select␣Data␣to␣Extract")
188
189
190         pout_checked = BooleanVar()
191         pae_checked = BooleanVar()
192
193
194
195         generate_plot = BooleanVar()
196         calculate_q = BooleanVar()
197         time_remaining_var = StringVar()
198         current_file_var = StringVar()
199
200         pout_check_box = Checkbutton(master = popup, text = "Pout", variable=pout_checked)
201         pout_check_box.grid(row = 1, column = 1, padx=50, pady=10)
202         pae_check_box = Checkbutton(master = popup, text = "PAE", variable=pae_checked)
203         pae_check_box.grid(row = 2, column = 1, padx=50, pady=10)
204         output_file_label = Label(text="Output␣File␣Name:␣", master = popup)
205         output_file_entry = Entry(width=50, master=popup)
```

```
206     output_file_label.grid(row=3, column = 0, padx=10)
207     output_file_entry.grid(row=3, column = 1)
208     q_check_box = Checkbutton(master=popup, text = "Calculate␣Q?", variable = calculate_q)
209     q_check_box.grid(row = 4, column = 0, pady=5)
210     plot_check_box = Checkbutton(master=popup, text = "Generate␣Plot?", variable =
            generate_plot)
211     plot_check_box.grid(row=5, column=0, pady=5)
212     conversion_progress_bar = ttk.Progressbar(master=popup)
213     conversion_progress_bar.grid(row = 6, column = 1)
214     current_file_label = Label(master=popup, textvariable=current_file_var)
215     current_file_label.grid(row=7, column=1)
216     time_remaining_label = Label(master=popup, textvariable=time_remaining_var)
217     time_remaining_label.grid(row=8, column=1)
218
219     def parse_mdf():
220
221         calculations_to_perform = []
222         if pout_checked.get():
223             calculations_to_perform.append("Output_Power")
224         if pae_checked.get():
225             calculations_to_perform.append("PAE")
226
227         for calc in calculations_to_perform:
228             current_file_var.set("Generating␣file␣for␣" + calc)
229             converted_file_name = output_file_entry.get()
230             if converted_file_name == "":
231                 converted_file_name = mdf_file_name.split('/')[-1] + "_Converted"
232             if len(calculations_to_perform) > 1:
233                 converted_file_name = converted_file_name + "_" + calc
234             if not converted_file_name.endswith(".txt"):
235                 converted_file_name = converted_file_name + ".txt"
236             debug_print(converted_file_name)
237             output_file = open(output_directory_path+converted_file_name, "a")
238
239             def file_print(message):
240                 print(message)
241                 output_file.write(message + "\n")
242
```

```
243             print("Converting...")
244
245             output_file.write(calc + "␣:␣Frequency\t")
246
247             isSourcePull = False
248             isLoadPull = False
249             df = pd.read_csv(mdf_file_name, skip_blank_lines=False, sep='^')
250             # df = pd.read_csv(mdf_file_name, skip_blank_lines=False)
251             #print (df["!Data File Info"])
252             row = 1
253             sweep_points = -1
254             z0 = -1
255             n_harm = -1
256             num_vars = 0
257             parsedToData = False
258
259             data = {}
260             # header = ""
261             startFreq = -1
262
263             #create dictionary containing list of sweep vars
264             #have list of indices that corresponds to where we are in each list
265             #increment frontmost index until it is greater than the length of
                    corresponding list -> reset back to 0 and increment next index
266             #repeat
267
268             #currently assuming order in !Sweep Info will be identical to order in VAR<>
                    section
269
270             swpVarNames = []
271             swpVarValues = []
272             swpVarIndices = []
273
274             while (not parsedToData):
275                  row_string = str(df["!Data␣File␣Info"][row])
276                  # print(row_string)
277                  if "!␣Sweep␣Variable:" in row_string:
278                       if "iGammaL1" in row_string:
```

```
279                         isLoadPull = True
280                    if "iGammaS1" in row_string:
281                         isSourcePull = True
282                    num_vars = num_vars + 1
283                    split_sweep = row_string.split('␣')
284                    swpVarNames.append(split_sweep[4])
285                    swpVarIndices.append(0)
286                    if split_sweep[-1][0] == "[" and split_sweep[-1][-1] == "]":
287                         swpVarValues.append(ast.literal_eval(split_sweep[-1]))
288                    else:
289                         numDummyVariables = int(split_sweep[5][1:-1])
290                         dummyList = []
291                         for i in range(numDummyVariables):
292                              dummyList.append(None)
293                         swpVarValues.append(dummyList)
294                    if swpVarNames[-1] == "Pwr":
295                         for i in range(len(swpVarValues[-1])):
296                              swpVarValues[-1][i] = swpVarValues[-1][i] + 30 #conversion
                                  from dBW to dBm
297               if "Total␣Sweep␣Points" in row_string:
298                    sweep_points = int(row_string.split()[-1])
299               if "Number␣of␣Recorded␣Harmonics" in row_string:
300                    n_harm = int(row_string.split()[-1])
301               if "BEGIN␣HEADER" in row_string:
302                    parameters = df["!Data␣File␣Info"][row+2].split()
303                    n_harm = int(parameters[1])
304                    z0 = float(parameters[2])
305
306               if "END<>" in row_string:
307                    parsedToData = True
308               row = row + 1
309
310          debug_print(swpVarNames)
311          debug_print(swpVarValues)
312
313          freq_position = swpVarNames.index("Freq") #should always be 0 but generalized
                 this anyways
314          if freq_position == -1:
```

```
315                     print("ERROR: No frequency information found in MDF")
316                     return
317
318                plot_labels = ["Freq (GHz)"]
319                plot_lines = []
320
321                source_string_mag = "Mag_Gamma_Source"
322                source_string_ang = "Ang_Gamma_Source"
323                load_string_mag = "Mag_Gamma_Load"
324                load_string_ang = "Ang_Gamma_Load"
325
326                if calculate_q.get():
327                     source_string_mag = source_string_mag + "_"
328                     source_string_ang = source_string_ang + "_"
329                     load_string_mag = load_string_mag + "_"
330                     load_string_ang = load_string_ang + "_"
331
332                if isSourcePull:
333                     plot_labels.append(source_string_mag)
334                     plot_labels.append(source_string_ang)
335                if isLoadPull:
336                     plot_labels.append(load_string_mag)
337                     plot_labels.append(load_string_ang)
338
339                deduction = 0
340                if "Pwr" in swpVarNames:
341                     deduction = deduction + 1
342                if "iGammaL1" in swpVarNames:
343                     deduction = deduction + 1
344                if len(swpVarValues[freq_position]) == 1:
345                     deduction = deduction + 1
346
347                start_time = time.perf_counter()
348                points_done = 0
349
350                step = 1 + n_harm + (num_vars + 2 - deduction)
351                start = row + 1 + (num_vars + 2 - deduction) #because iGammaL1 does not show
                       up in !Sweep Variable, assuming this is always the case
```

```
352                 for i in range(start, start + 1 + (sweep_points*step), step):
353                     #for j in range(n_harm):
354                     j = 0 #remove and add for loop if adding harmonics
355                     debug_print(str(df["!Data␣File␣Info"][i+j]))
356                     if str(df["!Data␣File␣Info"][i+j]) == "nan":
357                         continue
358                     if str(df["!Data␣File␣Info"][i+j])[0] == "!":
359                         break
360                     ab_waves = df["!Data␣File␣Info"][i+j].split()
361
362                     a1_real = float(ab_waves[1])
363                     # file_print("A1 real is" + str(a1_real))
364                     a1_imag = float(ab_waves[2])
365                     b1_real = float(ab_waves[3])
366                     b1_imag = float(ab_waves[4])
367                     a2_real = float(ab_waves[5])
368                     a2_imag = float(ab_waves[6])
369                     b2_real = float(ab_waves[7])
370                     b2_imag = float(ab_waves[8])
371
372                     a1 = a1_real+a1_imag*1j
373                     b1 = b1_real+b1_imag*1j
374                     a2 = a2_real+a2_imag*1j
375                     b2 = b2_real+b2_imag*1j
376
377                     if int(ab_waves[0]) == 1: #always true?
378                         vdd = float(ab_waves[11])
379                         idd = float(ab_waves[12])
380                         vgg = float(ab_waves[9])
381                         igg = float(ab_waves[10])
382
383                     mag_a1 = np.absolute(a1)
384                     mag_a2 = np.absolute(a2)
385                     mag_b1 = np.absolute(b1)
386                     mag_b2 = np.absolute(b2)
387
388                     if isSourcePull:
389                         source_gamma_real = float(ab_waves[13])
```

```
                source_gamma_imag = float(ab_waves[14])
                mag1 = np.absolute(source_gamma_real+(source_gamma_imag*1j))
                debug_print("Source Gamma Real is" + str(source_gamma_real))
                debug_print("Source Gamma Imag is" + str(source_gamma_imag))
                ang1 = np.arctan2(source_gamma_imag, source_gamma_real)
                debug_print("Arctan yields" + str(ang1))
            else:
                mag1=0
                ang1=0


            # mag1 = mag_a1/mag_b1
            mag2 = mag_a2/mag_b2

            debug_print("A/B mags")
            debug_print(mag_a1)
            debug_print(mag_b1)
            debug_print(mag_a2)
            debug_print(mag_b2)

            debug_print("Mags")
            debug_print(mag1)
            debug_print(mag2)

            # file_print("Gamma should be " + str(mag_a2/mag_b2))
            # ang1 = np.arctan(a1_imag/a1_real)-np.arctan(b1_imag/b1_real)
            # ang2 = np.arctan(a2_imag/a2_real)-np.arctan(b2_imag/b2_real)
            ang2 = np.arctan2(a2_imag, a2_real)-np.arctan2(b2_imag, b2_real)

            # file_print("Ang1 should be " + str(ang1))
            # file_print("Ang2 should be " + str(ang2))

            ang1_deg = 180*ang1/np.pi
            ang2_deg = 180*ang2/np.pi

            debug_print("Ang1 in degrees is be " + str(ang1_deg))
            debug_print("Ang2 in degrees is be " + str(ang2_deg))

```

```
428                     trans_wave = a1-b1
429                     # print(trans_wave/a1)
430                     output_wave = b2
431                     # print("Scalar gain equals:", np.absolute(output_wave/a1))
432                     # print("Logarithmic Gain equals:", 20*np.log10(np.absolute(output_wave/
                            a1)), " dB")
433                     p_out = 0.5*((mag_b2**2)-(mag_a2**2))
434                     p_in = 0.5*(mag_a1**2)
435                     # print(p_out)
436                     # print(p_in)
437
438                     plot_line = []
439
440                     frequency = str(int(swpVarValues[freq_position][swpVarIndices[
                            freq_position]]/1000000000))
441
442                     plot_line.append(int(swpVarValues[freq_position][swpVarIndices[
                            freq_position]]/1000000000))
443                     if isSourcePull:
444                          plot_line.append(round(mag1, 5))
445                          plot_line.append(round(ang1_deg, 5))
446                     if isLoadPull:
447                          plot_line.append(round(mag2, 5))
448                          plot_line.append(round(ang2_deg, 5))
449                     if data == {}:
450                          startFreq = frequency
451
452                     for swpVarIndex in range(len(swpVarNames)):
453                               if swpVarValues[swpVarIndex][swpVarIndices[swpVarIndex]] ==
                                      None or swpVarNames[swpVarIndex] == "Freq":
454                                    continue
455                               else:
456                                    if swpVarNames[swpVarIndex] not in plot_labels:
457                                         plot_labels.append(swpVarNames[swpVarIndex])
458                                    plot_line.append(round(swpVarValues[swpVarIndex][
                                           swpVarIndices[swpVarIndex]], 5))
459
460                     def ang_fix(ang):
```

```
461                     if ang < 0:
462                         return ang + 180
463                     return ang
464
465                 if frequency == startFreq:
466                     if isSourcePull:
467                         # header = header + "Source_Gamma_Mag = " + str(round(mag1, 5))
                                + " Source_Gamma_Ang = " + str(round(ang_fix(ang1_deg), 5)
                            ) + " "
468                         output_file.write(source_string_mag + "␣=␣" + str(round(mag1,
                            5)) + "␣" + source_string_ang + "␣=␣" + str(round(ang_fix(
                            ang1_deg), 5)) + "␣")
469                     if isLoadPull:
470                         # header = header + "Load_Gamma_Mag = " + str(round(mag2, 5)) +
                                " Load_Gamma_Ang = " + str(round(ang_fix(ang2_deg), 5)) +
                            " "
471                         output_file.write(load_string_mag + "␣=␣" + str(round(mag2, 5))
                                + "␣" + load_string_ang + "␣=␣" + str(round(ang_fix(
                            ang2_deg), 5)) + "␣")
472                     for swpVarIndex in range(len(swpVarNames)):
473                         if swpVarValues[swpVarIndex][swpVarIndices[swpVarIndex]] ==
                            None or swpVarNames[swpVarIndex] == "Freq":
474                             continue
475                         else:
476                             # header = header + swpVarNames[swpVarIndex] + " = " + str
                                (round(swpVarValues[swpVarIndex][swpVarIndices[
                                swpVarIndex]], 5)) + " "
477                             output_file.write(swpVarNames[swpVarIndex] + "␣=␣" + str(
                                round(swpVarValues[swpVarIndex][swpVarIndices[
                                swpVarIndex]], 5)) + "␣")
478                     # header = header + "\t"
479                     output_file.write("\t")
480                 if frequency not in data.keys():
481                     data[frequency] = ""
482
483
484                 p_delivered = 0.5*((mag_a1**2)-(mag_b1**2))
485
```

```
486                     if calc == "Output_Power":
487                          if "Output_Power" not in plot_labels:
488                               plot_labels.append("Output_Power")
489                          p_out_dbm = 10*np.log10(0.5*((mag_b2**2)-(mag_a2**2)))+30
490                          p_in_dbm = 10*np.log10(0.5*(mag_a1**2))+30 #Possibly just missing Zo
491
492                          data[frequency] = data[frequency] + "\t" + str(round(p_out_dbm, 4))
493                          plot_line.append(round(p_out_dbm, 4))
494
495                     # file_print("Freq is " + str(df["!Data File Info"][i-3]))
496                     # file_print("Output power equals:" + str(p_out_dbm) + " dBm") #Missing
                         Zo, should be (b2^2)/2Zo
497                     #For load pull, may need to do (b2^2 - a2^2)/2Zo, may not be correct,
                         need to figure out how AWR is normalizing the wave
498                     #Most important is factoring in a waves
499                     # print(np.absolute(a1))
500                     # print(0.5*(np.absolute(a1)**2))
501
502                     # file_print("Input power equals:" + str(10*np.log10(0.5*(mag_a1**2))+30)
                          + " dBm")
503                     # print("New G_trans equals:", p_out_db - p_in_db)
504
505                     elif calc == "PAE":
506                          if "PAE" not in plot_labels:
507                               plot_labels.append("PAE")
508                          pdc = (vdd * idd)#+(vgg*igg)
509                          pae = ((p_out)-(p_delivered))/pdc
510
511                          data[frequency] = data[frequency] + "\t" + str(round(pae*100, 4))
512                          plot_line.append(round(pae*100, 4))
513                          # file_print("PAE is " + str(pae*100) + "%")
514                          # print()
515
516                     for k in range(len(swpVarIndices)):
517                          if swpVarIndices[k] + 1 != len(swpVarValues[k]):
518                               swpVarIndices[k] = swpVarIndices[k] + 1
519                               break
520                          else:
```

```
521                          swpVarIndices[k] = 0
522                plot_lines.append(plot_line)
523                debug_print("Step is " +  str(100/float(sweep_points)))
524
525                points_done = points_done + 1
526                if (points_done % 100 == 0):
527                     current_time = time.perf_counter()
528                     time_remaining_estimated = round(((current_time-start_time)*(
                           sweep_points-points_done))/points_done)
529                     time_remaining_var.set("Estimated Time Remaining: " + str(
                           time_remaining_estimated) + " seconds")
530
531                conversion_progress_bar.step(100/float(sweep_points))
532                conversion_progress_bar.update_idletasks()
533
534
535           print("Parsing complete")
536           #print all data to .txt in proper format
537
538           # file_print(header[:-2]) #removing last tab and space from header
539           output_file.close()
540           output_file = open(output_directory_path+converted_file_name, "ab")
541           output_file.seek(-2, 2)
542           output_file.truncate()
543           output_file.close()
544           output_file = open(output_directory_path+converted_file_name, "a")
545           output_file.write("\n")
546           for frequency in data.keys():
547                file_print(frequency + data[frequency])
548           output_file.close()
549      popup.destroy()
550
551      if generate_plot.get():
552           debug_print("Before culling, there are " + str(len(plot_lines)) + " plot lines
                 with a length of " + str(len(plot_lines[0])) +  " and " + str(len(
                 plot_labels)) + " labels")
553           i = 0
554           while i < len(plot_lines[0]):
```

```
555                     unique_values = []
556                     for j in range(len(plot_lines)):
557                          if plot_lines[j][i] not in unique_values:
558                               unique_values.append(plot_lines[j][i])
559                     if len(unique_values) == 1:
560                          plot_labels.pop(i)
561                          for j in range(len(plot_lines)):
562                               plot_lines[j].pop(i)
563                     else:
564                          i = i + 1
565                debug_print("Plot␣labels␣are:")
566                debug_print(plot_labels)
567                paxfig = paxplot.pax_parallel(n_axes=len(plot_labels))
568                debug_print("After␣culling,␣there␣are␣" + str(len(plot_lines)) + "␣plot␣lines␣
                       with␣a␣length␣of␣" + str(len(plot_lines[0])) +  "␣and␣" + str(len(
                       plot_labels)) + "␣labels")
569                paxfig.plot(plot_lines)
570                paxfig.set_labels(plot_labels)
571                plt.show()
572
573
574      done_button = Button(master=popup, text="Convert", command=parse_mdf)
575      done_button.grid(row = 5, column = 2, padx=10)
576
577
578
579
580
581 def input_checker(entry):
582     if entry.get() == "":
583          return 0
584     try:
585          g = float(entry.get())
586          return 1
587     except:
588          print("Invalid␣parameter␣input:␣" + entry.get())
589          return -1
590
```

```
591
592 def run_load_pull_script():
593     global awrde
594     global mag1_entry
595     global mag2_entry
596     global ang1_entry
597     global ang2_entry
598     global vdd_entry
599     global vgg_entry
600
601     for routine in awrde.GlobalScripts('Load_Pull').Routines:
602         debug_print(routine)
603     # for routine in awrde.GlobalScripts('Open_Project_Directory').Routines:
604     #     print(routine)
605     # awrde.GlobalScripts('Import_Load_Pull_Files').Routines('Import_Load_Pull_Files').Run()
606     # awrde.GlobalScripts('Load_Pull').Routines('importLoadPullTemplate').RunWithArgs([False,
            True])
607     # createTemplate = True
608     # for schem in awrde.Project.Schematics:
609     #     if 'Load_Pull_Template' in schem.Name:
610     #         createTemplate = False
611     # if createTemplate:
612     #      awrde.GlobalScripts('Load_Pull').Routines('Create_Load_Pull_Template').Run()
613     #      time.sleep(5)
614
615     schem = awrde.Project.Schematics('Load_Pull_Template')
616
617     #MODIFY ELEMENT PARAMS DIRECTLY
618     # elem = schem.Elements('HBTUNER3.SourceTuner')
619
620     # elem.Parameters('Mag1').ValueAsDouble = mag1_entry.get()
621     # elem.Parameters('Mag2').ValueAsDouble = mag2_entry.get()
622     # elem.Parameters('Ang1').ValueAsDouble = ang1_entry.get()
623     # elem.Parameters('Ang2').ValueAsDouble = ang2_entry.get()
624
625     #GENERIC VERSION FOR IF WE MAKE .EMP BETTER
626     # for param in [mag1_entry, ang1_entry, mag2_entry, ang2_entry, vdd_entry, vgg_entry]:
627     #     if param.get() != "":
```

```
628     #         try:
629     #             param_val = float(param.get())
630     
631     #             schem.Equations('mag1').Expression = "mag1 = " + mag1_entry.get() + "\r\
            nang1 = " + ang1_entry.get()
632     #             schem.Equations('mag2').Expression = "mag2 = " + mag2_entry.get() + "\r\
            nang2 = " + ang2_entry.get()
633     
634     #         except:
635     #             print("Invalid parameter input:" + param)
636     #             print("Type "+ type(param.get()) " is not valid; Entered input was \"" +
            param.get() + "\"")
637     
638     #PROBLEMS:
639     #HAVE TO SET MAG AND ANG TOGETHER BECAUSE THEY ARE IN THE SAME EQUATION
640     # WOULD RESULT IN BUG IF TRYING TO CHANGE MAG1 BUT NOT ANG1 THROUGH GUI
641     
642     
643     
644     
645     
646     if (input_checker(mag1_entry) and input_checker(ang1_entry)):
647         schem.Equations('mag1').Expression = "mag1 = " + mag1_entry.get() + "\r\nang1 = " +
                ang1_entry.get()
648     if (input_checker(mag2_entry) and input_checker(ang2_entry)):
649         schem.Equations('mag2').Expression = "mag2 = " + mag2_entry.get() + "\r\nang2 = " +
                ang2_entry.get()
650     if (input_checker(vdd_entry)):
651         schem.Equations('iVd').Expression = "iVd = " + vdd_entry.get()
652     if (input_checker(vgg_entry)):
653         schem.Elements('DCVS.VGS').Parameters('V').ValueAsDouble = vgg_entry.get()
654     
655     
656     awrde.GlobalScripts('Load_Pull').Routines('Load_Pull').Run()
657     
658     # awrde.GlobalScripts('Load_Pull').Routines('doLoadPull').Run()
659     # for i in range(0, len(schem.Elements)):
660     #     print(schem.Elements[i])
```

```
661     # return
662
663 def run_manual_sweep():
664      global awrde
665      global graph_name
666      global measurement_name
667      global graph_name_entry
668      global graph_index
669
670      global modify_measurement_button
671      # print(modify_measurement_button.state)
672      modify_measurement_button.config(state = 'normal')
673      # print(modify_measurement_button.state)
674
675      schem = awrde.Project.Schematics(current_schematic.get())
676
677      #Apply sweep variables
678      for i in range(len(check_button_correlator)):
679           if (schem.Elements(check_button_correlator[i][1]).Enabled and input_checker(
                 check_button_correlator[i][2]) and input_checker(check_button_correlator[i][3])
                  and input_checker(check_button_correlator[i][4])):
680
681             schem.Elements(check_button_correlator[i][1]).Parameters('Values').ValueAsString
                    = "swpstp(" + check_button_correlator[i][2].get() + "," +
                    check_button_correlator[i][3].get() + "," + check_button_correlator[i][4].get
                    () + ")"
682      graph_name = graph_name_entry.get()
683      if graph_name == "":
684           graph_name = "Tabular␣" + str(graph_index)
685           graph_index = graph_index + 1
686      if (awrde.Project.Graphs.Exists(graph_name)):
687           #Prompt for overwrite if possible
688           awrde.Project.Graphs.Remove(graph_name)
689      awrde.Project.Graphs.Add(graph_name, 4) #I believe 4 corresponds to Tabular graph per
             AWR scripting guide, mwGT_Tabular is undefined
690      #Look at Page 389 of AWR Scripting Guide for info on how to retrieve other measurements
             (MeasurementInfos collection) (not ideal)
691      #Graph has InvokeCommand method -> see line 10065 of mwoffice.py
```

```
692     #Possible command name:? Name = GLOBAL!CE_Cookbook.copy_MWO_TB_And_Add_Graphs
            Category = Macros
693     #Name = ViewMeasurementEditor      Category = View
694
695     #Comes from Find_Command_Names global script with nothing as input
696     # awrde.Project.Graphs(graph_name).StartCommand("ViewMeasurementEditor", "awrde") #This
            is a valid command! Why won't it show the window?
697     # print("?")
698     if measurement_name == "":
699          measurement_name = current_schematic.get() + ".AP_HB:PAE(PORT_1,PORT_2)"
700     measurement_split = measurement_name.split(":")
701     awrde.Project.Graphs(graph_name).Measurements.Add(measurement_split[0],
            measurement_split[1])
702     awrde.Project.Simulator.Analyze() #Equivalent of clicking simulate in AWR
703     populate_tabulars()
704     print("Manual␣Sweep␣Complete")
705
706
707     #Potentially add CSimulator.AnalyzeOpenGraphs if we want to automate this instead of
            have the user do it
708 def modify_measurement():
709     global awrde
710     global graph_name
711     global measurement_name
712
713     for nd in awrde.Project.TreeView.Nodes("Project").Children("Graphs").Children(graph_name
            ).Children("Measurements").Children:
714          if (nd.Name == measurement_name):
715               awrde.Project.TreeView.Visible = True
716               nd.Selected = True
717               awrde.StartCommand("PropertiesObject", 0)
718               # awrde.StartCommand("ProjectAddMeasurement", 0)
719               # awrde.StartCommand("AddMeasurement", 0)
720               # awrde.StartCommand("Add Measurement", 0)
721               awrde.Project.Simulator.Analyze()
722
723     measurement_name = awrde.Project.TreeView.Nodes("Project").Children("Graphs").Children(
            graph_name).Children("Measurements").Children[0].Name
```

```
724
725
726 def create_txt_file():
727       global filename_entry
728       global awrde
729       global output_directory_path
730       global file_creation_label
731       global sweeps_global_frame
732
733       current_graph_name = current_tabular.get()
734       filename = filename_entry.get()
735       if filename == "":
736             filename = current_graph_name + "_Tabular_Data"
737       if len(filename) > 32:
738             filename = filename[0:32]
739       if (not filename.endswith(".txt")):
740          filename = filename + ".txt"
741       awrde.Project.Graphs(current_graph_name).ExportTraceData(output_directory_path+filename)
742
743       messagebox.showinfo(title="Success", message=str(filename) + "␣successfully␣created!")
744
745 def toggle_checkbox():
746       schem = awrde.Project.Schematics(current_schematic.get())
747       for pairing in check_button_correlator:
748             if pairing[0].get():
749                   schem.Elements(pairing[1]).Enabled = True
750             else:
751                   schem.Elements(pairing[1]).Enabled = False
752
753 def goto_main_menu():
754       global method_global_frame
755       global direct_method_frame
756       global specific_method_frame
757       global load_pull_tutorial_frame
758       global sweeps_global_frame
759
760       sweeps_global_frame.pack_forget()
761       cTableContainer.pack_forget()
```

```
762       direct_method_frame.pack_forget()
763       specific_method_frame.pack_forget()
764       load_pull_tutorial_frame.pack_forget()
765
766       method_global_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
767
768   def goto_direct_frame():
769       global method_global_frame
770       global direct_method_frame
771
772       method_global_frame.pack_forget()
773       direct_method_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
774
775   def goto_specific_frame():
776       global method_global_frame
777       global specific_method_frame
778
779       method_global_frame.pack_forget()
780       specific_method_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
781
782   def goto_tutorial():
783       global sweeps_global_frame
784       global load_pull_tutorial_frame
785       load_pull_tutorial_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
786       sweeps_global_frame.pack_forget()
787
788   def goto_sweeps():
789       global sweeps_global_frame
790       global load_pull_tutorial_frame
791       global sbVerticalScrollBar
792       global cTableContainer
793
794       sbVerticalScrollBar.pack(fill=Y, side=RIGHT, expand=FALSE)
795       cTableContainer.pack(fill=BOTH, side=LEFT, expand=TRUE)
796       cTableContainer.create_window(0, 0, window=sweeps_global_frame, anchor=NW)
797
798       populate_schematic_list()
799
```

```
800       if isExampleProject:
801            goto_tutorial_button.grid(row=102, column=0, padx=widget_pad_default, pady=
                   widget_pad_default)
802
803       load_pull_tutorial_frame.pack_forget()
804
805  def populate_tabulars():
806       global sweeps_global_frame
807       global current_tabular
808       global awrde
809       global tabular_dropdown
810
811       if tabular_dropdown != None:
812            tabular_dropdown.grid_forget()
813
814       tabular_list = []
815
816       for graph in awrde.Project.Graphs:
817            debug_print(graph.Name)
818            if graph.Type == 4: #Tabular
819                 tabular_list.append(graph.Name)
820
821       current_tabular = StringVar()
822       current_tabular.set(tabular_list[0])
823       tabular_dropdown = OptionMenu(
824            sweeps_global_frame,
825            current_tabular,
826            *tabular_list
827       )
828
829       tabular_dropdown.grid(row=100, column=2, padx=widget_pad_default, pady=
              widget_pad_default)
830
831  def launch_example_project():
832       global awrde
833       global root
834       global specific_method_frame
835       global load_pull_tutorial_frame
```

```
836       global isExampleProject
837       isExampleProject = True
838       awrde = mwo.CMWOffice()
839       awrde.Open(Filename=os.getcwd() + "/Parallel_Plot_Example_File.emp")
840       specific_method_frame.pack_forget()
841       load_pull_tutorial_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
842
843  def emp_file_dialog():
844       global awrde
845       global root
846       global specific_method_frame
847       global sweeps_global_frame
848       project_name = filedialog.askopenfilename(filetypes = [("AWR Project Files","*.emp")])
849       if (project_name == ""):
850            return
851       awrde = mwo.CMWOffice()
852       awrde.Open(Filename=project_name)
853       specific_method_frame.pack_forget()
854       goto_sweeps()
855
856
857  def populate_schematic_list():
858       global awrde
859       global schematic_list
860       global schematic_dropdown
861       global current_schematic
862       global schematic_list_subframe
863
864       schematic_list = []
865       for schematic in awrde.Project.Schematics:
866            debug_print(schematic.Name)
867            schematic_list.append(schematic.Name)
868
869       if schematic_dropdown != None:
870            schematic_dropdown.grid_forget()
871
872
873       current_schematic = StringVar()
```

```
874      current_schematic.set(schematic_list[0])
875      schematic_dropdown = OptionMenu(
876           schematic_list_subframe,
877           current_schematic,
878           *schematic_list
879      )
880
881      current_schematic.trace_add('write', populate_sweep_variables)
882
883      schematic_dropdown.grid(row=0, column=0)
884      populate_sweep_variables()
885
886 class Root(Tk):
887
888     def __init__(self):
889         super(Root,self).__init__()
890
891         self.title("Parallel␣Plots␣GUI")
892         #self.minsize(600,400)
893
894         ##METHOD FRAME
895
896         global method_global_frame
897         method_global_frame = Frame(bg=frame_bg_color)
898
899         method_label = Label(master=method_global_frame, text="Choose␣Conversion␣Method")
900
901         direct_method_button = Button(
902             master = method_global_frame,
903             text="Direct␣Method",
904             width=20,
905             height=3,
906             command=goto_direct_frame
907         )
908
909         specific_method_button = Button(
910             master = method_global_frame,
911             text="Specific␣Method",
```

```
912             width=20,
913             height=3,
914             command=goto_specific_frame
915         )
916 
917         output_directory_button = Button(
918              master=method_global_frame,
919              text="Choose␣Output␣Directory␣for␣Generated␣Files",
920              width=40,
921              height=3,
922              command=change_output_directory
923         )
924 
925         method_label.grid(row=0, column=1, padx=widget_pad_default, pady=widget_pad_default)
926         direct_method_button.grid(row = 1, column = 0, padx=widget_pad_default, pady=
                widget_pad_default)
927         specific_method_button.grid(row= 1, column = 2, padx=widget_pad_default, pady=
                widget_pad_default)
928         output_directory_button.grid(row=2, column=1, padx=widget_pad_default, pady=
                widget_pad_default)
929 
930         #DIRECT FRAME
931 
932         global direct_method_frame
933         direct_method_frame = Frame(bg=frame_bg_color)
934 
935         main_menu_button_1 = Button(
936             master = direct_method_frame,
937             text="Main␣Menu",
938             width=10,
939             height=1,
940             command=goto_main_menu
941         )
942 
943         convert_mdf_file_button = Button(
944             master = direct_method_frame,
945             text="Convert␣MDF␣File",
946             width=20,
```

```
947             height=3,
948             command=convert_mdf_file
949         )
950 
951         parallel_plots_button = Button(
952             master = direct_method_frame,
953             text="Open␣Parallel␣Plots",
954             width=20,
955             height=3,
956             command=launch_parallel_plots
957         )
958 
959         main_menu_button_1.grid(row = 0, column = 0, padx=widget_pad_default, pady=
                widget_pad_default)
960         convert_mdf_file_button.grid(row = 1, column = 0, padx=widget_pad_default, pady=
                widget_pad_default)
961         parallel_plots_button.grid(row= 1, column = 1, padx=widget_pad_default, pady=
                widget_pad_default)
962 
963         #SPECIFIC FRAME
964 
965         global specific_method_frame
966 
967         specific_method_frame = Frame(bg=frame_bg_color)
968 
969         main_menu_button_2 = Button(
970             master = specific_method_frame,
971             text="Main␣Menu",
972             width=10,
973             height=1,
974             command=goto_main_menu
975         )
976 
977         example_project_button = Button(
978             master = specific_method_frame,
979             text="Launch␣Example␣Project",
980             width=20,
981             height=3,
```

```
982             command=launch_example_project
983         )
984 
985         global choose_file_button
986         choose_file_button = Button(
987             master = specific_method_frame,
988             text="Choose .EMP",
989             width=20,
990             height=3,
991             command=emp_file_dialog
992         )
993 
994         main_menu_button_2.grid(row = 0, column = 0, padx=widget_pad_default, pady=
                widget_pad_default)
995         example_project_button.grid(row=1, column=0, padx=widget_pad_default, pady=
                widget_pad_default)
996         choose_file_button.grid(row=1, column=1, padx=widget_pad_default, pady=
                widget_pad_default)
997 
998         #SWEEPS FRAME
999 
1000        #CREDIT TO JOE HUTCH FOR THIS SCROLLABLE FRAME SOLUTION: https://www.joehutch.com/
                posts/tkinter-dynamic-scroll-area/
1001 
1002        global sbVerticalScrollBar
1003        global cTableContainer
1004        cTableContainer = Canvas(width=750, height=700)
1005 
1006        sbVerticalScrollBar = Scrollbar()
1007 
1008        global sweeps_global_frame
1009        sweeps_global_frame = Frame( master = cTableContainer, bg=frame_bg_color)
1010 
1011        cTableContainer.config(yscrollcommand=sbVerticalScrollBar.set, highlightthickness=0)
1012        sbVerticalScrollBar.config(orient=VERTICAL, command=cTableContainer.yview)
1013        def _on_mousewheel(event):
1014          cTableContainer.yview_scroll(int(-1*(event.delta/120)), "units")
1015 
```

```
1016        cTableContainer.bind_all("<MouseWheel>", _on_mousewheel)
1017
1018
1019
1020        global goto_tutorial_button
1021        goto_tutorial_button = Button(
1022            master = sweeps_global_frame,
1023            text="Previous",
1024            width=10,
1025            height=3,
1026            command=goto_tutorial
1027        )
1028
1029        main_menu_button_3 = Button(
1030            master = sweeps_global_frame,
1031            text="Main␣Menu",
1032            width=10,
1033            height=1,
1034            command=goto_main_menu
1035        )
1036
1037        start_sweep_label = Label(master = sweeps_global_frame, text="Start")
1038        end_sweep_label = Label(master = sweeps_global_frame, text="End")
1039        step_sweep_label = Label(master = sweeps_global_frame, text="Step")
1040
1041        parallel_plots_button_2 = Button(
1042            master = sweeps_global_frame,
1043            text="Open␣Parallel␣Plots",
1044            width=20,
1045            height=3,
1046            command=launch_parallel_plots
1047        )
1048
1049
1050        populate_sweep_variables_button = Button(
1051            master = sweeps_global_frame,
1052            text="Repopulate␣Sweep␣Variables",
1053            width=25,
```

```
1054            height=3,
1055            command=populate_sweep_variables
1056        )
1057
1058        global schematic_list_subframe
1059        global update_schematic_list_button
1060
1061        schematic_list_subframe = Frame(master=sweeps_global_frame)
1062
1063        update_schematic_list_button = Button(
1064            master = schematic_list_subframe,
1065            text=u'\u21BB',
1066            width=1,
1067            height=1,
1068            command=populate_schematic_list
1069        )
1070
1071        update_schematic_list_button.grid(row=0, column=1)
1072
1073        run_manual_sweep_button = Button(
1074            master = sweeps_global_frame,
1075            text="Run␣Manual␣Sweep",
1076            width=20,
1077            height=3,
1078            command=run_manual_sweep
1079        )
1080
1081        create_txt_file_button = Button(
1082            master = sweeps_global_frame,
1083            text="Create␣File",
1084            width=20,
1085            height=3,
1086            command=create_txt_file
1087        )
1088
1089        global modify_measurement_button
1090        modify_measurement_button = Button(
1091            master = sweeps_global_frame,
```

```
1092            text="Modify␣Measurement",
1093            width=20,
1094            height=3,
1095            state='disabled',
1096            command=modify_measurement
1097        )
1098
1099
1100
1101        global filename_entry
1102        global graph_name_entry
1103
1104        graph_name_label = Label(master = sweeps_global_frame, text="Tabular␣Graph␣Name:")
1105        graph_name_entry = Entry(master = sweeps_global_frame)
1106
1107        filename_label = Label(master = sweeps_global_frame, text="File␣Name:")
1108        filename_entry = Entry(master = sweeps_global_frame)
1109        schematic_label = Label(master=sweeps_global_frame, text="Choose␣Schematic:")
1110        tabular_label = Label(master=sweeps_global_frame, text="Tabular␣File␣to␣Export:")
1111
1112        schematic_label.grid(row=0, column=0)
1113
1114        main_menu_button_3.grid(row=0, column=3, padx=widget_pad_default, pady=
                widget_pad_default)
1115        schematic_list_subframe.grid(row=1, column = 0, padx=widget_pad_default, pady=
                widget_pad_default)
1116        parallel_plots_button_2.grid(row=1, column=3, padx=widget_pad_default, pady=
                widget_pad_default)
1117        populate_sweep_variables_button.grid(row=2, column=0, padx=widget_pad_default, pady=
                widget_pad_default)
1118
1119        start_sweep_label.grid(row=3, column=1, padx=widget_pad_default, pady=
                widget_pad_default)
1120        end_sweep_label.grid(row=3, column=2, padx=widget_pad_default, pady=
                widget_pad_default)
1121        step_sweep_label.grid(row=3, column=3, padx=widget_pad_default, pady=
                widget_pad_default)
1122
```

```
1123        #All variables start at row 4, there is room for 95 different SWPVARS
1124
1125
1126        graph_name_label.grid(row=99, column=0)
1127        graph_name_entry.grid(row=100, column=0, padx=widget_pad_default, pady=
                widget_pad_default)
1128        run_manual_sweep_button.grid(row=100, column=1, padx=widget_pad_default, pady=
                widget_pad_default)
1129        modify_measurement_button.grid(row=101, column=1, padx=widget_pad_default, pady=
                widget_pad_default)
1130        tabular_label.grid(row = 99, column=2)
1131        #dropdown box row 100 column 2
1132        filename_label.grid(row=101, column=2)
1133        filename_entry.grid(row=102, column=2)
1134        create_txt_file_button.grid(row=102, column=3, padx=widget_pad_default, pady=
                widget_pad_default)
1135
1136        #EXAMPLE PROJECT TUTORIAL FRAME
1137
1138        global load_pull_tutorial_frame
1139        load_pull_tutorial_frame = Frame(bg=frame_bg_color)
1140
1141        main_menu_button_4 = Button(
1142            master = load_pull_tutorial_frame,
1143            text="Main␣Menu",
1144            width=10,
1145            height=1,
1146            command=goto_main_menu
1147        )
1148
1149        goto_sweeps_button = Button(
1150            master = load_pull_tutorial_frame,
1151            text="Next",
1152            width=10,
1153            height=3,
1154            command=goto_sweeps
1155        )
1156
```

```
1157
1158        global lp_script_button
1159        lp_script_button = Button(
1160            master = load_pull_tutorial_frame,
1161            text="Run Load Pull Script",
1162            width=20,
1163            height=3,
1164            command=run_load_pull_script,
1165        )
1166
1167        export_mdf_file_button = Button(
1168            master = load_pull_tutorial_frame,
1169            text="Export MDF",
1170            width=20,
1171            height=3,
1172            command=export_mdf_file
1173        )
1174
1175
1176        mag1_label = Label(master = load_pull_tutorial_frame, text="Mag1")
1177        mag2_label = Label(master = load_pull_tutorial_frame, text="Mag2")
1178        ang1_label = Label(master = load_pull_tutorial_frame, text="Ang1")
1179        ang2_label = Label(master = load_pull_tutorial_frame, text="Ang2")
1180        vdd_label = Label(master = load_pull_tutorial_frame, text="Vdd")
1181        vgg_label = Label(master = load_pull_tutorial_frame, text="Vgg")
1182
1183        global mag1_entry
1184        global mag2_entry
1185        global ang1_entry
1186        global ang2_entry
1187        global vdd_entry
1188        global vgg_entry
1189        mag1_entry = Entry(master = load_pull_tutorial_frame)
1190        mag2_entry = Entry(master = load_pull_tutorial_frame)
1191        ang1_entry = Entry(master = load_pull_tutorial_frame)
1192        ang2_entry = Entry(master = load_pull_tutorial_frame)
1193        vdd_entry = Entry(master = load_pull_tutorial_frame)
1194        vgg_entry = Entry(master = load_pull_tutorial_frame)
```

```
1195
1196          main_menu_button_4.grid(row=0,column=0, padx=widget_pad_default, pady=
                  widget_pad_default)
1197          mag1_label.grid(row=1,column=0, padx=widget_pad_default, pady=widget_pad_default)
1198          mag1_entry.grid(row=2,column=0, padx=widget_pad_default, pady=widget_pad_default)
1199          mag2_label.grid(row=3,column=0, padx=widget_pad_default, pady=widget_pad_default)
1200          mag2_entry.grid(row=4,column=0, padx=widget_pad_default, pady=widget_pad_default)
1201          ang1_label.grid(row=1,column=1, padx=widget_pad_default, pady=widget_pad_default)
1202          ang1_entry.grid(row=2,column=1, padx=widget_pad_default, pady=widget_pad_default)
1203          ang2_label.grid(row=3,column=1, padx=widget_pad_default, pady=widget_pad_default)
1204          ang2_entry.grid(row=4,column=1, padx=widget_pad_default, pady=widget_pad_default)
1205          vdd_label.grid(row=1,column=2, padx=widget_pad_default, pady=widget_pad_default)
1206          vdd_entry.grid(row=2,column=2, padx=widget_pad_default, pady=widget_pad_default)
1207          vgg_label.grid(row=3,column=2, padx=widget_pad_default, pady=widget_pad_default)
1208          vgg_entry.grid(row=4,column=2, padx=widget_pad_default, pady=widget_pad_default)
1209          export_mdf_file_button.grid(row = 6, column = 0, padx=widget_pad_default, pady=
                  widget_pad_default)
1210          lp_script_button.grid(row=5, column=0, padx=widget_pad_default, pady=
                  widget_pad_default)
1211          goto_sweeps_button.grid(row=6, column=2, padx=widget_pad_default, pady=
                  widget_pad_default)
1212
1213          #### LAUNCH FIRST WINDOW
1214
1215          method_global_frame.pack(padx=frame_pad_default, pady=frame_pad_default)
1216
1217 global root
1218
1219
1220 root = Root()
1221 root.resizable(False, False)
1222 root.mainloop()
1223
1224 # t1.terminate()
1225
1226 #TODO :
1227
1228 #Fix newline issue with setting mag/ang params - would be helpful if they were all separate
```

```
        equations but they are not
```

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