Advanced Design Approaches to High-Performance Transmitter Components

by

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The demand for higher transmit data rates is driving requirements for increased transmitter linearity, efficiency, and bandwidth. To address these challenges, designers are adopting advanced architectures that significantly increase transmitter complexity, often outpacing traditional design methodologies. This thesis explores supply modulation as a means to enhance transmitter efficiency and introduces automated circuit design and hardware-in-the-loop circuit analysis techniques. The work begins with the design and testing of two monolithic multilevel supply modulators, fabricated using two distinct 150 nm Gallium Nitride (GaN) on Silicon Carbide (SiC) processes. These chips are evaluated through envelope tracking of an octave-bandwidth power amplifier under realistic signal conditions. Subsequently, the thesis reviews network synthesis concepts, presenting a novel approach to maximally flat filter design based on the electrostatic principle of equipotential volumes and the potential analog method. The simplified real frequency technique (SRFT) is then revisited and extended with a method for automated nonuniform transmission line (NTL) design. Several NTL circuits are demonstrated, including a monolithic distributed amplifier with a measured available bandwidth from DC to 40 GHz. Finally, the thesis introduces and validates a nonlinear circuit analysis technique called Network Emulation—a hardware-in-the-loop (HITL) approach designed for scenarios where traditional model-based circuit analysis is inadequate. Large-signal validation is provided by comparing the emulated and measured behavior of a nonlinear circuit with feedback.

Dedication

To Yakira and our next adventure together.

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Soli Deo Gloria

Contents

Chapter

1 Introduction **1**

1.1 Motivation: The Need for High-Performance Transmitters 1

1.2 Current Solutions to Linearity and Efficiency 4

1.3 Outline of Thesis 6

2 Introduction to RF Transmitters **9**

2.1 Communications Signals 10

2.1.1 Introduction 10

2.1.2 Digital Amplitude and Phase Modulation 13

2.1.3 Multi-Carrier Modulation 16

2.2 Amplifier Analysis 18

2.2.1 Terminology 18

2.2.2 Elements of an Amplifier 23

2.2.3 Intrinsic Model 24

2.2.4 Fundamentals of PA Behavior 25

2.2.5 Calculating the Load Line 32

2.3 Efficiency Recovery Architectures 37

2.3.1 Load Line Manipulations 38

2.3.2 Load and Supply Modulation 39

2.4 Conclusions 46

3 Supply Modulation using a Discrete Multilevel Supply Modulator **48**

3.1 Introduction . . . 48

3.2 Supply Modulator Architectures . . . 50

3.3 Supply Modulator Design in WIN 150nm GaN-on-SiC . . . 52

3.3.1 Power Switch Sizing . . . 52

3.3.2 Driver Design . . . 57

3.3.3 Simulation . . . 58

3.4 Results . . . 58

3.4.1 Static Load Measurements . . . 58

3.4.2 Envelope Tracking Measurements . . . 61

3.4.3 Supply Modulator in Qorvo's 150nm Process . . . 66

3.5 Conclusions . . . 67

4 Network Synthesis **69**

4.1 Introduction . . . 69

4.2 Background . . . 71

4.2.1 Theory . . . 72

4.2.2 Spectral Factorization . . . 80

4.3 Approximation Problems . . . 82

4.3.1 The Transfer Function . . . 83

4.3.2 The Butterworth Filter . . . 86

4.3.3 Maximally-Flat Filter Response from Square Cross-Section . . . 89

4.4 Network Realization . . . 94

4.4.1 Ladder Network Synthesis . . . 95

4.4.2 Polynomial Recovery and Numerical Correction . . . 96

4.4.3 Synthesized Filter Prototypes . . . 97

4.5 Real Frequency Techniques . . . 97

4.5.1 Approach . . . 100
4.5.2 Examples . . . 100
4.6 Summary and Conclusions . . . 103

5 Automated Design of Nonuniform Transmission Lines **105**
5.1 Introduction . . . 105
5.2 Nonuniform Transmission-Line Model . . . 107
5.2.1 SRFT Lossless Two-Port Network Description . . . 108
5.2.2 Transmission-Line Nonuniform Impedance Model . . . 109
5.2.3 Nonlinear Constraints Function . . . 111
5.3 Design Procedure for NTL Networks . . . 114
5.3.1 Initialization . . . 115
5.3.2 Optimization . . . 116
5.3.3 Growth . . . 119
5.3.4 Planar NTL Layout . . . 120
5.4 Passive NTL Examples . . . 123
5.4.1 Band-Stop Filter . . . 123
5.4.2 Single Match . . . 125
5.4.3 VCO Resonator . . . 126
5.5 Amplifier Matching Network Design . . . 129
5.5.1 Hybrid Amplifier . . . 130
5.5.2 Distributed Amplifier MMIC . . . 133
5.6 Discussion . . . 134
5.7 Conclusions . . . 135

6 Network Emulation **136**
6.1 Introduction . . . 136
6.2 The Hardware Equivalent Source . . . 140

6.2.1 The Physical Reflection Coefficient . . . 140
6.2.2 The Total Excitation . . . 141
6.3 The Tuner Equivalent Source . . . 143
6.3.1 Generalized Tuner Theory . . . 144
6.3.2 Tuner Validation . . . 147
6.4 Equivalent Source Method for 2-Port Network Emulation . . . 149
6.5 Equivalent Source Method for N-Port Network Emulation . . . 151
6.5.1 Simulation Sources and N-Port Network Definition . . . 153
6.5.2 Port Coupling . . . 154
6.5.3 Generalized Network Equivalent Source . . . 156
6.5.4 Network Emulation Procedure . . . 157
6.6 Demonstration of Network Emulation . . . 158
6.6.1 Test Bench . . . 158
6.6.2 Circuit Design . . . 160
6.6.3 Procedure . . . 161
6.6.4 Results . . . 163
6.7 Discussion and Conclusions . . . 163

7 Conclusions and Future Work **166**
7.1 Contributions . . . 166
7.2 Future Work . . . 170
7.2.1 Monolithic Integration of a Ka-Band PA and an Asymmetric, Six-Level Supply Modulator . . . 170
7.2.2 Planar Circuit Approach for Nonuniform Transmission Line Analysis . . . 172
7.2.3 Future Work In Network Emulation . . . 175
7.3 Summary . . . 177

Bibliography **179**

Appendix

A Load Line Model Source Code **192**

B Computational Network Analysis using Power Waves **217**

B.1 Power Waves 217

B.2 Network Analysis 219

B.2.1 Boundary Conditions 219

B.2.2 Network Parameters 220

B.2.3 Nodal Equations 220

B.3 Scattering Matrices of Common Elements 224

B.3.1 General Impedance 224

B.3.2 Resistor 225

B.3.3 Inductor 226

B.3.4 Capacitor 226

B.3.5 Transmission Line 226

C Generalized Tuner Convergence Criteria **228**

Tables

Table

3.1 Dynamic load line model parameters used to estimate PA efficiency recovery. 61

3.2 Comparison of efficiencies for different PAs reported in literature. 68

5.1 First Four Polynomials Relating to (5.14) 114

5.2 Settings for Band-Stop Filter Design 123

5.3 Settings for Matching Network Design 126

5.4 Settings for Hybrid Amplifier Design 131

6.1 Results of Source and Load Pull 148

6.2 Error between emulation and measurement in power sweep. 163

Figures

Figure

1.1 Technologies that rely on RF and microwave transmitters 1

1.2 Components of an RF and microwave transmitter 2

1.3 Transmitter circuits and concepts discussed in this thesis 7

2.1 A simplified block diagram of a modern wireless transmitter 9

2.2 Annotated probability density function of a 5G signal 11

2.3 Plot of a 5G signal PDF and Class AB amplifier efficiency 12

2.4 Example quadrature amplitude modulation constellations 13

2.5 Spectrum of a 16-QAM waveform 14

2.6 Time-domain IQ and amplitude representations of a 16-QAM waveform 15

2.7 A comparison of the possible PAPRs that an N-order QAM signal may take on . . . 15

2.8 Illustration of carrier aggregation using OFDM 17

2.9 Worst-case PAPRs for a uniform multi-tone modulation scheme 17

2.10 Example illustrating the importance of amplifier gain and efficiency 21

2.11 The elements of a single-stage amplifier 23

2.12 Intrinsic, equivalent-circuit model of a field-effect transistor 25

2.13 Idealized plot of a transistor's IV curves 26

2.14 Model of an amplifier with a harmonic trap. 26

2.15 Drain efficiency, delivered power, and power gain versus conduction angle 29

2.16 Power added efficiency versus conduction angle for various Class A gain levels 30
2.17 Load lines of an amplifier on the IV plane 31
2.18 Load line and corresponding waveforms of a Class AB amplifier 33
2.19 Description of how conduction angle changes in backoff 35
2.20 Drain efficiency versus output power for a given conduction angle 36
2.21 Normalized power dissipation for each amplifier class as output power is reduced. . . 36
2.22 Variation in amplifier gain versus class and output power backoff 37
2.23 Load line manipulations for different common PA enhancement architectures 38
2.24 General block diagram of a load-modulation architecture 40
2.25 General block diagram of a supply modulation architecture 43
2.26 Block diagram illustrating the three principle architectures of supply modulation . . 44

3.1 Comparison of static and modulated supply waveforms 49
3.2 A discrete four-level circuit diagram and reverse "stair-step" timing diagram 53
3.3 Multilevel supply modulator fabricated in WIN 150 nm process 54
3.4 Expected conduction and switching losses versus powers switch periphery 56
3.5 Simulated and ideal output voltage waveform of the supply modulator 57
3.6 Diagram of the measurement system used for static load testing 59
3.7 Measured and simulated supply modulator efficiency across a static load of 37.4Ω . . 60
3.8 Waveforms and static measurements used for dynamic load line simulation 60
3.9 Three frames of the dynamic load line simulation 62
3.10 Block diagram of the envelope tracking measurement system 63
3.11 Measured efficiency improvement when supply modulating an octave-bandwidth PA 64
3.12 Trajectory used for supply modulation 65
3.13 Measured PA EVM when using static and dynamic supplies 66
3.14 Layout and chip image of supply modulator fabricated in Qorvo 150 nm process . . . 66
3.15 Comparing efficiencies of supply modulators fabricated in Qorvo and WIN processes 67

4.1 A low-pass "T" network 70
4.2 Difference between linear, time-invariant circuit analysis and synthesis 72
4.3 Driving-point immittance functions of a one-port linear network 73
4.4 A two-port linear network 76
4.5 Roots of $G(p)$ on the complex plain 81
4.6 Process for maximally-flat filter design using potential analog method 83
4.7 Analog computer using the current potential analog from [1] 85
4.8 Butterworth filter transmission coefficient for various filter orders 86
4.9 Pole distribution of the Butterworth function on the unit circle 87
4.10 Faraday's Ice Pale Experiment 88
4.11 MoM solution of a square closed conductor waveguide 90
4.12 Approximated charge distribution ζ along a single edge of the conductor 90
4.13 Discrete, equally charged filament solutions for various numbers of filaments 92
4.14 Transfer function magnitude response for square cross-section filters of various orders 93
4.15 Four common canonical network forms 94
4.16 Ladder elements and their associated transmission-zero locations in frequency 95
4.17 Two realizations of a maximally-flat, low-pass filter 98
4.18 Simple 5-pole low-pass network 101
4.19 Diagram and response of a synthesized diplexer 102

5.1 Introduction to nonuniform transmission line matching networks 106
5.2 Characteristic impedance function used for NTL automated design 112
5.3 Diagram of the procedure used for automated network design 117
5.4 Manual approach to meandering a NTL 120
5.5 Constructing meandered NTLs from curved uniform line segments 121
5.6 Annotated elementary uniform curve segment of an NTL 121
5.7 Fabricated NTL band-stop filter 124

5.8 Fabricated NTL matching network . . . 127
5.9 A high-efficiency, low phase noise VCO with NTL resonator . . . 128
5.10 Fabricated amplifier with NTL matching networks . . . 130
5.11 Fabricated distributed amplifier with NTL networks . . . 132
5.12 Simulated and measured response of NTL distributed amplifier . . . 133
5.13 Simulated surface currents on a uniform and NTL microstrip line . . . 134

6.1 Network emulation of a single-stage amplifier . . . 137
6.2 Outline of the process and layers that compose network emulation . . . 139
6.3 Block diagram illustrating a single equivalent source and associate hardware . . . 141
6.4 Procedure for hardware equivalent source updates . . . 142
6.5 Introduction to the tuner equivalent source . . . 144
6.6 Relationship between hardware and tuner equivalent sources . . . 145
6.7 Procedure for tuner equivalent source . . . 147
6.8 Validation cases for the generalized tuner method . . . 148
6.9 Circuit used to demonstrate two-port network emulation . . . 149
6.10 A 2-port network and its equivalent source . . . 150
6.11 Simulated and emulated results for the example from Fig. 6.9 . . . 152
6.12 Conceptual circuits used in the network emulation process . . . 152
6.13 The coupling paths to an internal port of the emulated network . . . 155
6.14 Procedure for network equivalent source . . . 159
6.15 Photo of the measurement system used to perform network emulation . . . 160
6.16 DUT configuration for the emulation and measurement cases . . . 160
6.17 Emulated and measured circuit behavior over frequency . . . 162
6.18 Emulated and measured circuit behavior over power . . . 164

7.1 A monolithically integrated multilevel supply modulator and power amplifier . . . 170
7.2 Integrated SMPA small signal parameters . . . 171

7.3 Simulated PAE versus output power of the integrated SMPA 171

7.4 Layout of the integrated SMPA using waver-level packaging 173

7.5 2D approaches to planar circuit analysis 174

7.6 Extension of network emulation of circuits with multiple nonlinear devices 176

7.7 Emulation of a two-stage amplifier 177

B.1 The linear two-port network presented in the beginning of Chapter 4. 217

B.2 A junction of three ports. 220

B.3 Circuit schematic for finding the general S-parameters of an impedance element. . . 224

Chapter 1

Introduction

Demand for higher data-rates result in increased design constraints on transmitter linearity, efficiency, and bandwidth. To meet these requirements, designers use architectures which increase transmitter complexity at a pace that traditional design approaches have struggled to match. Investigating design methods for offsetting this growth in complexity is the primary motivation for this thesis.

1.1 Motivation: The Need for High-Performance Transmitters

RF and microwave transmitters are foundational to modern technology, enabling wireless communication, sensing, and electronic warfare across a wide range of applications. As shown in Fig. 1.1, these transmitters are integral to consumer electronics, commercial infrastructure, and

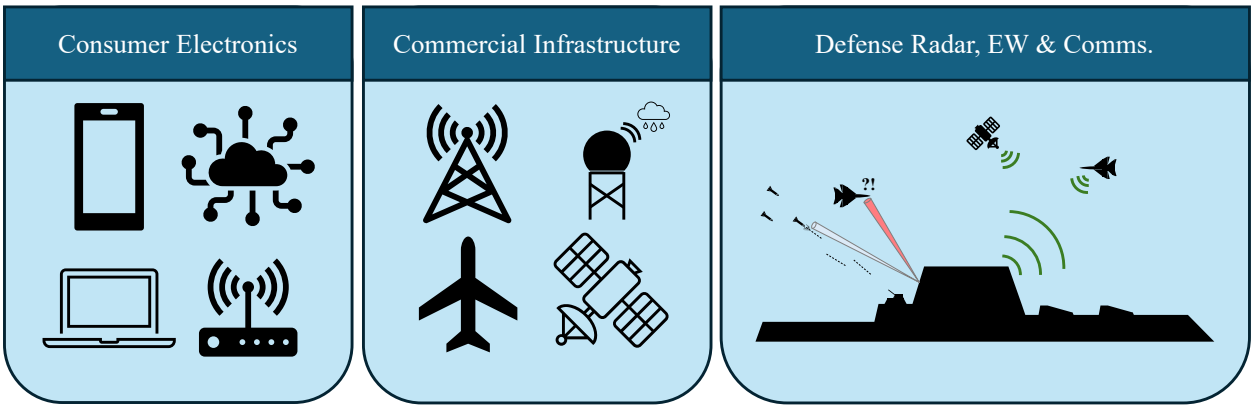


Figure 1.1: Technologies that rely on RF and microwave transmitters for communication, sensing, and electronic warfare.

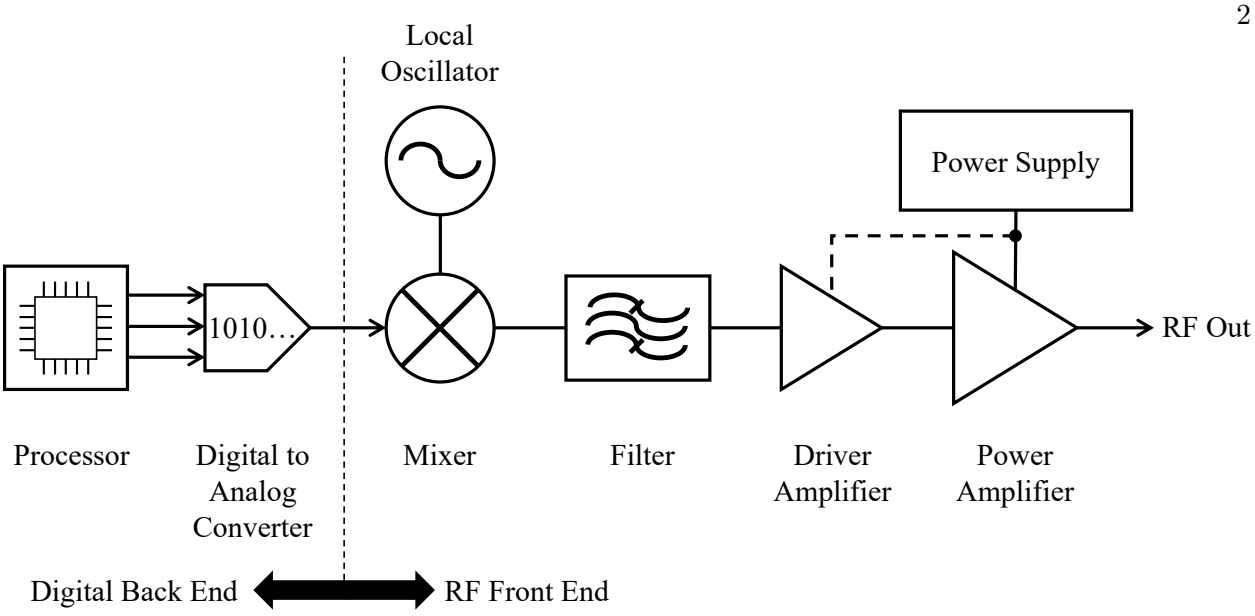


Figure 1.2: Block diagram and components of a typical RF and microwave transmitter.

defense systems. Their performance directly impacts the reliability, efficiency, and capabilities of devices and networks that underpin everyday life, industry, and national security.

Fig. 1.2 illustrates a simple diagram of an RF and microwave transmitter. Functionally speaking, the role of the RF and microwave transmitter is to source and electrically condition a signal for broadcast into a medium, e.g. free-space. Components used to source the baseband signal, i.e. information to be transmitted, make up the digital backend and consist of a processor and digital to analog converter. This baseband signal is up-converted and amplified in the RF front end of the transmitter. The RF front end up-converts this signal to the RF frequency and electrically conditions the signal for transmission. It consists of several components including a mixer, local oscillator, filter, amplifier chain, and power supply. The performance of the RF front end is the primary limiter in overall transmitter performance and is the focus of this work.

A key aspect to this conditioning is amplification–or to increasing the magnitude of the signals power for transmission. Two key metrics which describe amplification are gain and linearity where gain is essentially the quantity of amplification and linearity is the quality. More specifically, linearity refers to the property of being invariant in gain with respect to signal amplitude. Another

key design metric to amplification is efficiency–or the cost in system power. These metrics to amplification: gain, linearity, and efficiency are in direct opposition in traditional architectures–particularly linearity and efficiency.

A final consideration is the range of frequencies that a transmitter can support the required gain–also known as bandwidth. There are two types of bandwidth relevant to transmitter design–instantaneous and available bandwidth. Instantaneous bandwidth refers to the transmitter's capacity to support a signal of a given bandwidth. Available bandwidth refers to the range of frequencies that a transmitter can support. Both of these metrics are critical to modern transmitters. Wide instantaneous bandwidths are required to support high data-rate signals, while wide available bandwidths are required to support multiple radio functions, such as Wi-Fi, Bluetooth, and cellular.

An amplifier is the component within the transmitter which performs the requisite action of amplification in the transmitter. Generally, the signal supplied to the amplifier is low enough in amplitude that multiple "stages" or cascaded amplifiers are required to drive the signal amplitude to the correct power level for transmission. Earlier stages are generally smaller and are designed to maximize gain and linearity. The final stages of amplification are the largest and have the greatest impact on total amplifier efficiency. One approach to maximizing efficiency in these stages is to use high-efficiency classes such as class C, F, or E. However, this approach has several drawbacks–particularly when transmitting broadband, amplitude modulated signals. First, these classes require operating in a saturated state to achieve high operating efficiencies–meaning that they can only effectively operate at one output power. Second, they tend to use resonant networks to achieve the high-efficiency operation. Such networks are by their very nature difficult to design for large fractional bandwidths (40%) and tend to significantly restrict amplifier available bandwidth. Finally, these classes, particularily class C, are biased such that the gain changes as a function of input power–resulting in poor linearity. For these reasons, the final stages tend to be biased in a linear class such as AB or B. However, these classes are not efficient and tend to result in poor overall amplifier efficiency.

In spite of this trade-off, today's systems need transmitters with high-linearity, broad band-

width, and excellent efficiency to meet demanding commercial, industrial, and defense requirements. Growing need for higher communication data-rates is resulting in spectrum-congestion and has become an important national security consideration [2, 3]. Regardless of the government's method for overseeing and administrating spectrum allocations, transmitter linearity requirements are all but guaranteed to increase. Linearity is a key factor to maintaining signal fidelity–which relates to the maximum distance between transmitter and receiver as well as the maximum data rate the transmitter can reliably provide. Furthermore, linearity is an essential feature of spectral efficiency, i.e. how well the spectrum is used. Poor linearity results in by-products which interfere with other users–requiring guard-bands to mitigate. Higher linearity addresses this issue by relaxing these considerations and maximizing spectral efficiency.

As mentioned before, linearity is not the whole story. Efficiency is also a key consideration for many. Poor efficiency results in waste-heat which requires redress in the form of active cooling. This can have significant and detrimental implications for transmitter size, weight, and cost. Furthermore, active cooling is another system which requires power and introduces additional mechanical points of failure. A second consideration to poor efficiency is battery life and energy availability. For many mobile applications battery life is a key consideration. Energy availability is a related challenge. However, it is more concerned with the instantaneous energy demand that these systems place on a power plant or generator. This can impact transmitter linearity in the form of pulse droop and can require additional mitigation strategies–such as capacitance banks–to address. Of course these capacitor banks also require maintenance and introduce another point of failure.

1.2 Current Solutions to Linearity and Efficiency

Strategies for improving linearity and efficiency are numerous. For power amplifiers this includes techniques such as supply modulation, load modulation, and digital pre-distortion. Supply modulation is a technique that improves efficiency by dynamically adjusting the supply voltage to the power amplifier based on the instantaneous power of the input signal. This allows the amplifier

to operate more efficiently while maintaining linearity. Load modulation is a technique that adjusts the load impedance seen by the power amplifier to improve efficiency and linearity. Digital pre-distortion is a technique that compensates for nonlinearities in the power amplifier by pre-distorting the input signal before amplification.

These techniques can improve linearity and efficiency, but they also introduce additional complexity to the transmitter design. For example, supply modulation requires additional hardware, such as a supply modulator, which can increase the size and cost of the transmitter. Load modulation requires additional control circuitry to adjust the load impedance dynamically. Digital pre-distortion requires complex algorithms and digital signal processing to accurately model and compensate for the nonlinearities in the power amplifier. In all cases, increased complexity can lead to increased cost and result other design compromises that reduce overall transmitter performance.

Unfortunately, modern design techniques have not kept pace with the growing complexity of these systems. The bilateral nature of solid-state circuits and the nonlinearities of modern power amplifiers make it difficult to design and optimize these systems using traditional methods. For instance, supply modulation requires a detailed understanding of an amplifier's behavior with respect to a dynamic supply voltage. As the bias of the amplifier changes, so too does its gain and input reflection coefficient–resulting in a degraded impedance match upstream driver circuits. Both of these effects can degrade linearity of the amplifier beyond traditional design considerations, i.e. supply modulator ringing. Prior work has proposed several design techniques to address this challenge, but have not been demonstrated beyond narrow fractional bandwidths, i.e. $< 20\%$ [4, 5, 6].

In addition to growing design complexity, another challenge is the availability of accurate models and simulators for these non-linear circuits. Most models are extracted under continuous wave conditions and may not accurately represent the behavior when excited with broadband signals or pulses. This can lead to inaccurate predictions of the amplifier's performance, particularly in terms of linearity. Furthermore, traditional time-domain analog circuit simulators, such as SPICE, struggle to efficiently simulate microwave circuits due to the large difference in time constants be-

tween the RF signals and the slower dynamics of the baseband envelope. For this reason, microwave circuit designer often rely on frequency-domain, harmonic balance simulators which can efficiently simulate the steady-state behavior of these circuits. However, these simulators often struggle to accurately model the transient behavior of non-linear circuits.

In addition to these linearity and efficiency challenges, growing demand for available bandwidth and radio functions, i.e. bluetooth, Wi-Fi, and cellular, are also driving up the complexity of modern transmitters. This is particularly true for consumer electronics, where multiple radio functions must coexist in a single device, such as a smartphone. These devices often require multiple transmitters operating at different frequencies and with different modulation schemes, which can lead to increased design complexity and cost.

Together, all of these considerations are fueling growing interest in automated design techniques to offset the engineering costs and mitigate design trade-offs. Techniques such as artificial intelligence and machine learning, when coupled with modern computational power, have the potential to revolutionize circuit design by automating the design process and enabling the optimization of complex circuits. However, these methods are still in their infancy and require further development to be practical for real-world applications. To make the best use of design automation through artificial intelligence and machine learning, it is important to have a solid understanding of the underlying principles of circuit design. Particularly the principles of linear network synthesis. For this reason, part of this thesis is dedicated to the principles of linear network synthesis and its application for automated circuit design.

1.3 Outline of Thesis

This thesis focuses on design approaches for high-performance transmitter components using the techniques discussed in Fig. 1.3. The three concepts that guide this work are supply modulation, network synthesis, and network emulation. This thesis begins by discussing the design of a multilevel supply modulator. Then it transitions into using network synthesis for amplifier and passive network design. Finally it concludes with a discussion of a novel, hardware-in-the-loop circuit analysis

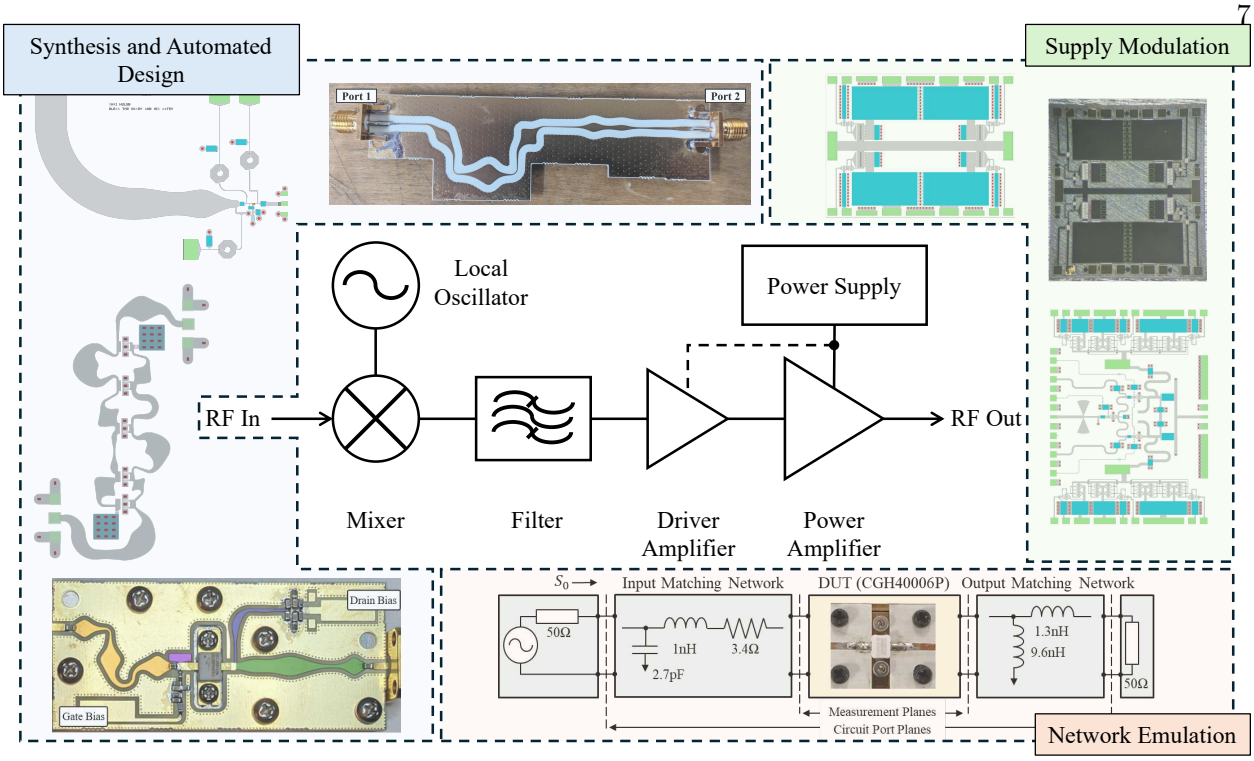


Figure 1.3: Block diagram of a transmitter along with circuits and the core concepts of this thesis.

technique called network emulation.

The chapter organization is as follows:

- Chapter 2: introduces the RF transmitter architecture and discusses why high peak-to-average power ratio signals impact power amplifier efficiency with a load-line model. Supply modulation is introduced as a solution and different supply modulator architectures are discussed.

- Chapter 3: presents the discrete, multi-level supply modulator. The design process of a discrete multilevel supply modulator fabricated in Qorvo and WIN Semiconductor's process is discussed, and test results are reported with a static load and power amplifier.

- Chapter 4: introduces network synthesis and contrasts it with automated design. This includes a brief history of network synthesis and its major contributions to circuit theory. The potential analog method is used to derive a class of "maximally-flat" and the simplified

real frequency technique (SRFT) is presented as a general method for microwave network design.

- Chapter 5: extends the SRFT framework discussed in Chapter 4 towards automated nonuniform transmission line (NTL) design. The design of several planar NTL circuits is presented, including a dc-40 GHz distributed amplifier.

- Chapter 6: presents a new, hardware in the loop, circuit analysis approach called network emulation. An equivalent source theory is introduced and developed through three abstractions into a generalized N-port emulation approach. Several demonstrations are presented: including a generalized active tuner, 2-port network emulation, and N-port network emulation of a power amplifier with electromagnetic coupling between input and output matching networks.

- Chapter 7: concludes this thesis by summarizing its contents, its contributions, and future work.

In addition, this work also contains the following appendices:

- Appendix A: lists the python code and usage of the load line model used throughout Chapters 2 and 3.

- Appendix B: details a rather straight-forward, computational approach to linear network analysis using power waves. This is a technique that the author has found invaluable throughout the course of this work–particularly in developing the network emulation and tuner algorithms of Chapter 6.

- Appendix C: contains additional details pertaining to the convergence of the tuner algorithm discussed in Chapter 6.

Chapter 2

Introduction to RF Transmitters

Fig. 2.1 shows the transmitter block diagram that introduces main concepts discussed in this chapter. A digital data source (e.g., a computer or embedded controller) supplies the information to be transmitted. This information is converted into an analog RF waveform by the waveform generator, representing the RF front-end digital to analog converter (DAC), modulation and up-converter. A power amplifier (PA) then boosts the signal power and delivers it to the load, typically an antenna. A small portion of the transmitted signal may be fed back to the waveform generator to enable corrective adjustments and improve transmission quality.

The PA in Fig. 2.1 is the primary bottleneck for transmitter front-end efficiency and linearity. This chapter summarizes the mechanisms behind PA efficiency loss and reviews methods to mitigate them, with particular emphasis on a method referred to as supply modulation. Section 2.1 examines signal characteristics that exacerbate PA inefficiency. Section 2.2 provides a concise anal-

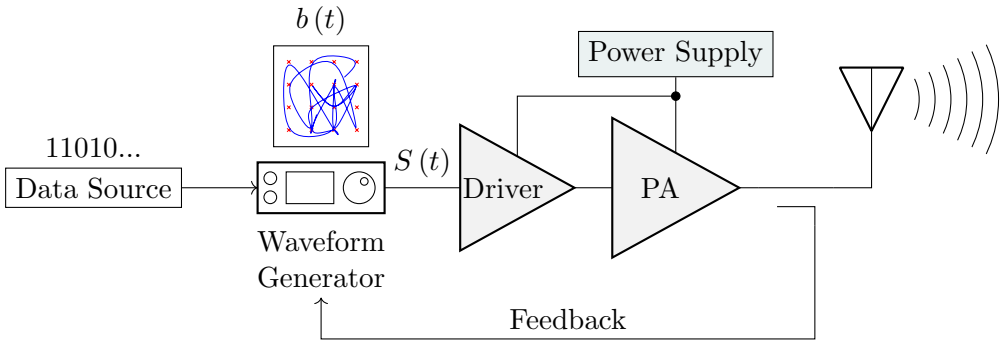


Figure 2.1: A simplified block diagram of a modern wireless transmitter.

ysis of PA behavior and explains why efficiency degrades as output power is reduced. Section 2.3 introduces techniques for recovering efficiency at reduced output power, and presents representative load-modulation and supply-modulation architectures. Section 2.4 concludes by comparing these architectures and motivating the focus on supply modulation for high-frequency PA efficiency recovery.

2.1 Communications Signals

2.1.1 Introduction

The transmitter front end is responsible for preparing a signal for transmission, which includes modulation, frequency up-conversion, and amplification. In electrical systems, a signal carries information and can be either analog (continuous) or digital (discrete). Digital signals are preferred in most applications because they offer greater noise immunity, data integrity, and reliability. The basic unit of digital information is the bit, representing a logical true or false. Communication systems transport this digital information by encoding it onto a high-frequency carrier wave that can propagate through free space. This encoding process, known as modulation, involves varying a property of the carrier in a controlled manner that reflects the original information. Mathematically, the modulated high-frequency signal can be described as:

$$S(t) = \Re\left\{b(t)\exp^{j\omega_c t}\right\} \tag{2.1}$$

where $b(t)$ is the modulating signal and ω_c is the carrier frequency. The modulating signal $b(t)$ is a complex function given by:

$$b(t) = I(t) + jQ(t), \tag{2.2}$$

where $I(t)$ and $Q(t)$ are the in-phase and quadrature components of the information signal. (2.1) describes a signal with a single carrier, however; greater amounts of data may be transmitted by combining or multiplexing multiple carriers into a single signal as:

$$S(t) = \Re\left\{b_1(t)\exp^{j\omega_{c1}t} + b_2(t)\exp^{j\omega_{c2}t} + \cdots + b_N(t)\exp^{j\omega_{cN}t}\right\} \tag{2.3}$$

where N represents the total number of signals combined into $S(t)$. In this section, common approaches to the single and multicarrier modulation schemes are reviewed. Characteristics of each approach impact the noise-immunity and data-rate achievable and are relevant properties both to the current discussion and in the broader context of wireless communications, however; this thesis is largely focused on reviewing these signals from the perspective of PA and transmitter front-end efficiency. It turns out that the instantaneous PA efficiency tends to be a strong function of the output power.[1] Therefore the particular quality which forms the context of this section is statistical distribution of the signal's instantaneous power a key metric of which is the signal's peak-to-average-power ratio or (PAPR):

$$\text{PAPR} = \frac{P_{\text{peak}}}{P_{\text{mean}}}$$

where P_{peak} is the maximum instantaneous power in the signal, and P_{mean} is the average power. The driving motivation behind this review is to quantify the required variation and formulate an understanding of what tends to drive higher PAPRs in modern signals.

PAPR is readily deduced from the statistical distribution of a signal typically represented as

[1] A review of the reasons for this is presented in Section 2.2.

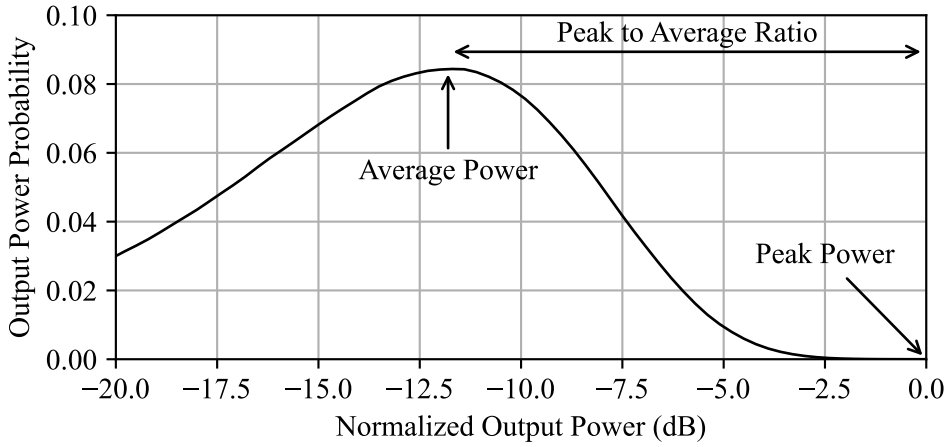


Figure 2.2: Annotated probability density function of a 5G signal. The x-axis is the ratio of the output power with respect to the peak power. The y-axis is the probability that the signal will be at the corresponding backoff power.

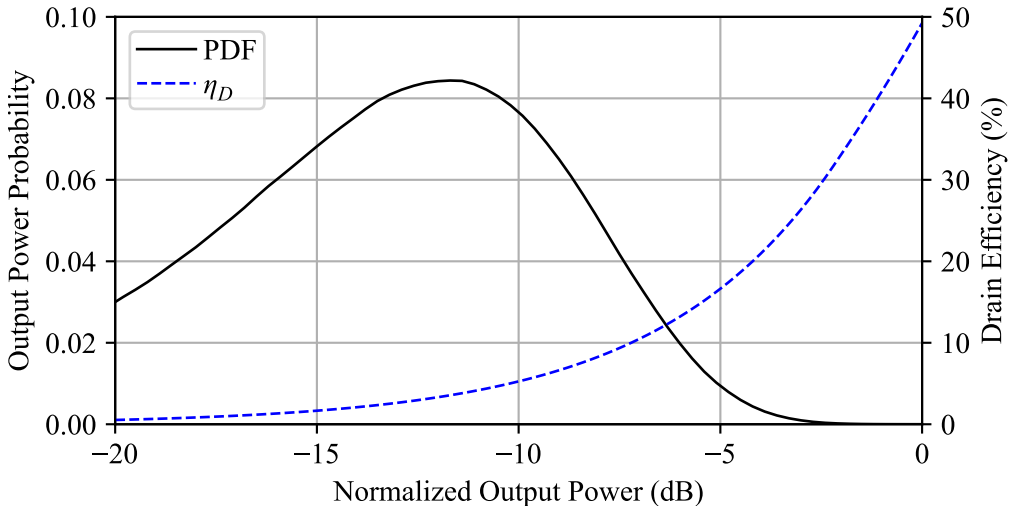


Figure 2.3: Plot of a 5G signal PDF superimposed alongside the backoff efficiency curve of a Class AB amplifier.

a probability density function (PDF) or complimentary cumulative distribution function (CCDF). Fig. 2.2 shows the PDF of a modern communications signal (i.e. 5G FR2) which exhibits a PAPR of 11.8 dB. In these plots, the x-axis represents the normalized output power to that of the peak output power in dB while the y-axis shows the probability of the signal being at each power level. The resulting distribution typically resembles a Poisson distribution, with the mean power corresponding to the mode (the peak) of the PDF. The PAPR can then be estimated graphically as the difference, in dB, between the mode and the 0 dB (peak power) point.

Fig. 2.3 illustrates the PDF of the signal illustrated in Fig. 2.2 alongside the backoff drain efficiency curve of a Class AB power amplifier with a knee voltage that is 10% of the maximum voltage. The key takeaway of this figure is that the amplifier is most efficient where the signal is highly improbable. It turns out there are several characteristics of modern signal modulation which result in high PAPR values. Two of the most common modulation schemes to date are the amplitude and phase modulation of digital data, discussed in Section 2.1.2, and multitone/multicarrier modulation schemes, which is presented in Section 2.1.3.

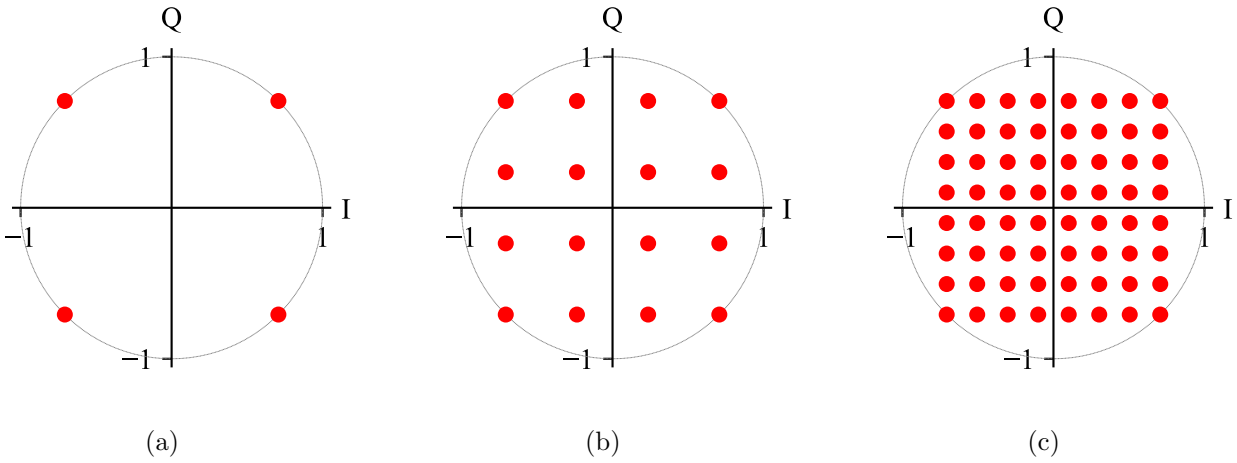


Figure 2.4: Example constellations: (a) quadrature phase-shift keying (QPSK, or 4-QAM), (b) 16-QAM, and (c) 64-QAM.

2.1.2 Digital Amplitude and Phase Modulation

Quadrature Amplitude Modulation (QAM) is a widely used digital modulation scheme in modern communication systems. Except for the special case of 4-QAM, QAM signals inherently exhibit a peak-to-average power ratio (PAPR) greater than 0 dB. In QAM, digital information is encoded as symbols, each represented by a unique point in a two-dimensional constellation diagram. These points correspond to discrete values of the signal's in-phase (I) and quadrature (Q) components, forming a grid of possible amplitude and phase combinations.

Fig. 2.4 shows example constellations for (a) QPSK (4-QAM), (b) 16-QAM, and (c) 64-QM. As the order of QAM increases, the number of constellation points grows, allowing more bits to be transmitted per symbol. The relationship between the number of bits per symbol and the QAM order N is given by:

$$\frac{\text{bits}}{\text{symbol}} = \log_2(N) \tag{2.4}$$

Since each symbol corresponds to a specific signal amplitude, calculating the PAPR of an ideal QAM signal is a straightforward statistical process (assuming no filtering or impairments). If

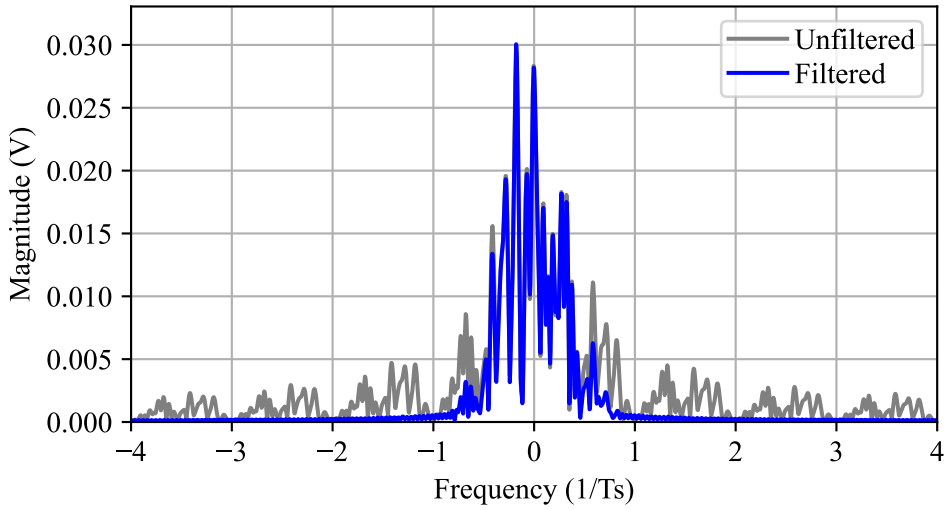


Figure 2.5: Spectrum of a 16-QAM waveform before (grey) and after (blue) low-pass filtering is applied. The unfiltered signal requires infinite frequency content to accurately re-create the time-domain waveform.

all symbols are equally likely, the average power of the QAM signal is:

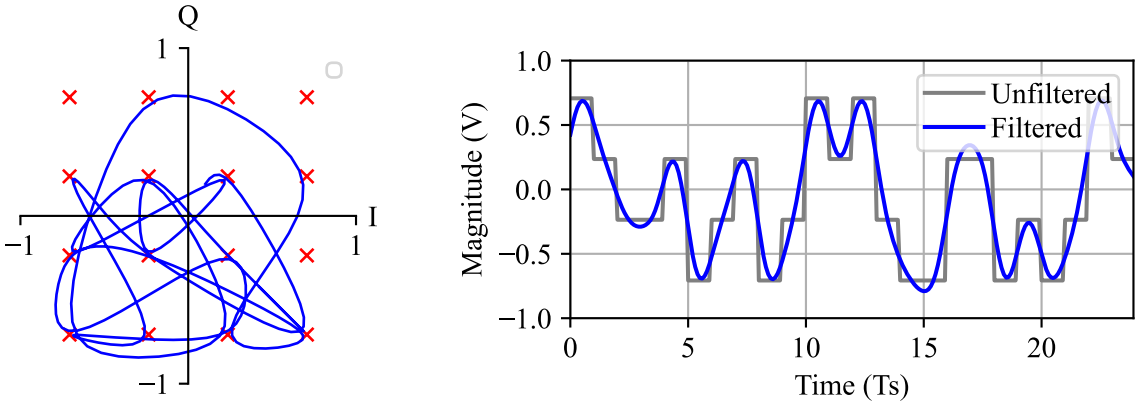
$$P_{\text{avg}} = \frac{1}{N} \sum_{k=1}^{N} |A_k|^2, \tag{2.5}$$

where N is the number of constellation points and A_k is the complex amplitude of the k-th symbol. If the constellation is normalized so that the maximum symbol power is 1 W, the PAPR for N-QAM is:

$$\text{PAPR}_{N\text{-QAM}} = \frac{1}{P_{\text{avg}}} \tag{2.6}$$

In theory, the rapid transitions between symbols in a QAM constellation would require infinite bandwidth to transmit perfectly, as abrupt changes in the signal correspond to high-frequency components. However, infinite bandwidth is not achievable in practical systems due to physical and regulatory limitations. To address this, the signal's bandwidth is limited using a low-pass filter—most commonly a root-raised cosine filter—which smooths the transitions between symbols and confines the signal within a finite frequency range. Fig. 2.5 illustrates the bandwidth of a 16-QAM waveform both before and after filtering is applied.

Fig. 2.6 illustrates the time-domain characteristics of a filtered 16-QAM signal. In Fig. 2.6a,



(a) (b)

Figure 2.6: Time-domain (a) IQ and (b) amplitude representations of a 16-QAM waveform after low-pass filtering is applied.

the signal trajectory is shown in the IQ (constellation) domain, while Fig. 2.6b displays the corresponding amplitude versus time. When the signal transitions between constellation points, the filtering process can introduce overshoot, resulting in occasional peaks that exceed the nominal symbol amplitudes. As a result, the peak-to-average power ratio (PAPR) of practical QAM signals is typically higher than that of the ideal, unfiltered case.

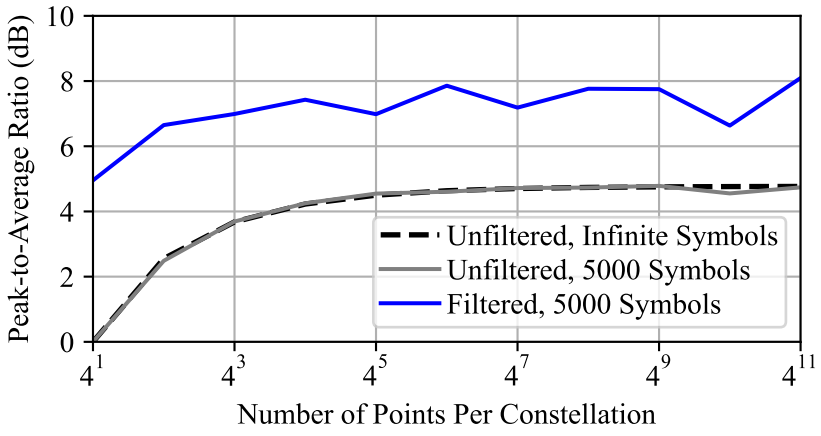


Figure 2.7: A comparison of the possible PAPRs that an N-order QAM signal may take on (a) for an unfiltered signal of infinite length and a 3000 symbol signal (a) before and (b) after filtering.

Fig. 2.7 shows how signal filtering increases the PAPR of a QAM signal. For reference the unfiltered, infinite-length signal calculated using (2.6) and (2.5) is illustrated alongside a 3000-symbol, unfiltered signal. In these "ideal" cases, 4-QAM has a PAPR of 0 dB, while higher-order QAM schemes exhibit increasing PAPR, asymptotically approaching approximately 4.8 dB for very large constellations. This trend is consistent with results reported in the literature [7]. Above these is the PAPR of the 3000-symbol signal after filtering is applied. Note that in all cases filtering increases signal PAPR–even those where the signal would normally have a PAPR of 0 dB.

While calculating the unfiltered PAPR of a QAM signal is straightforward due to its discrete constellation, estimating the PAPR after filtering is much more complex. In practical systems, filtering and other impairments make it difficult to analytically predict the PAPR and therefore the statistical distribution is analyzed numerically.

2.1.3 Multi-Carrier Modulation

Frequency Division Multiplexing (FDM) and Orthogonal Frequency Division Multiplexing (OFDM) are widely used techniques in communications for combining multiple sub-carriers, each modulated with a digital scheme. OFDM differs from FDM in that each sub-carrier—shaped like a sinc function in the frequency domain—is centered at the nulls of its neighboring sub-carriers, ensuring orthogonality and efficient spectral usage. Fig. 2.8 shows how five sub-carriers may be aggregated in the frequency domain using OFDM.

Historically, these sub-carriers have used low data-rate modulation schemes such as BPSK [8], but higher-order schemes like QAM have also been adopted [9]. Both FDM and OFDM signals are prone to high peak-to-average power ratio (PAPR). This is because the worst-case PAPR occurs when all sub-carriers are in phase, causing their amplitudes to add constructively. Mathematically, if the signal is

$$s(t) = \sum_{n=1}^{N} A_0 \cos(n\omega_0 t),$$

where A_0 is the amplitude of each individual sub-carrier, N is the total number of sub-carriers, and ω_0 is the angular frequency of the fundamental tone. This signal is assumed to be proportional

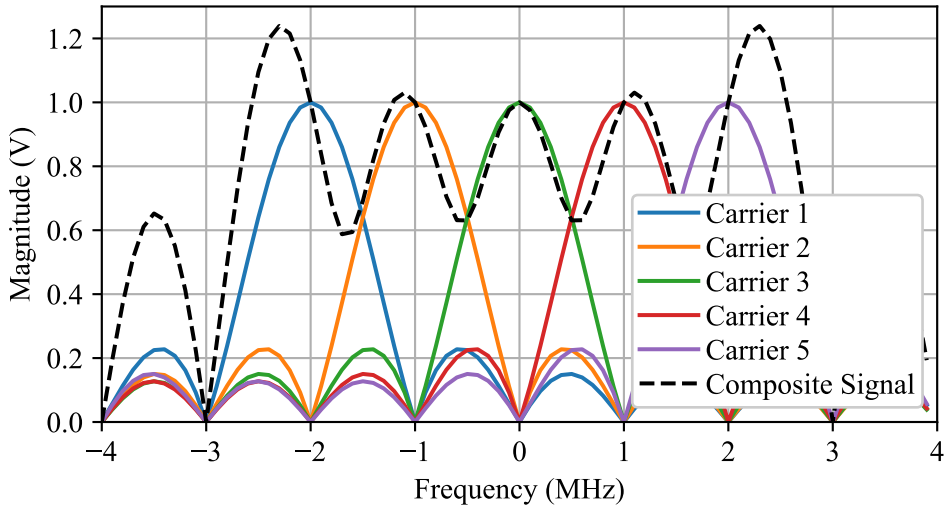


Figure 2.8: Illustration of carrier aggregation using orthogonal frequency division multiplexing. Each solid trace represents the magnitude of a sub-carrier while the dashed trace represents the magnitude of the aggregate signal. In OFDM, each sub-carrier is spaced such that there is no overlap at the corresponding carrier frequencies (e.g. -2, -1, ..., 2 MHz).

to the time-domain voltage waveform and therefore all associated powers are the square of it in

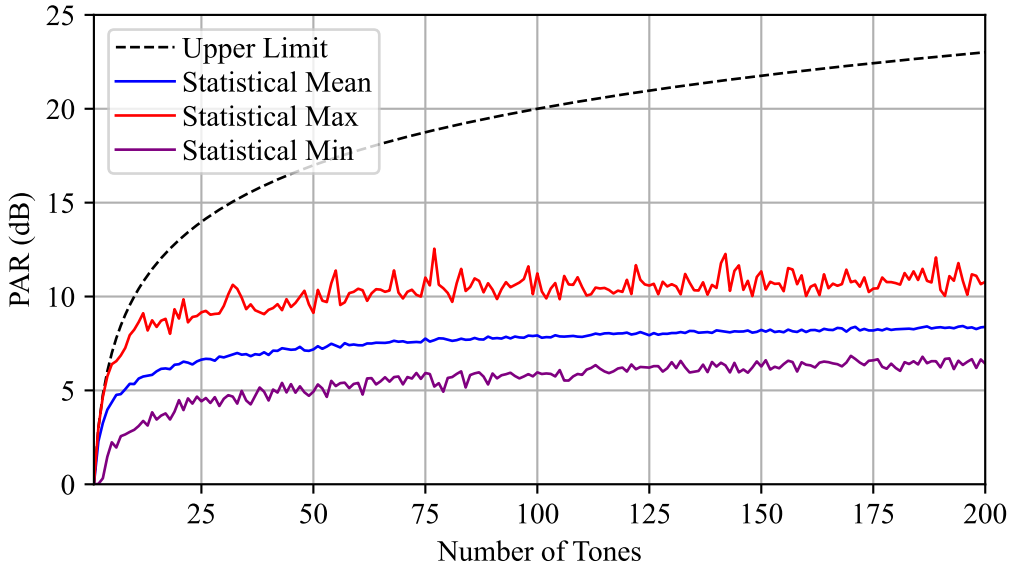


Figure 2.9: Worst-case PAPRs for a uniform multi-tone modulation scheme such as OFDM and FDM.

time. Therefore, the peak instantaneous power is:

$$P_{\text{peak}} = N^2 A_0^2,$$

and the average power is

$$P_{\text{avg}} = N A_0^2.$$

Therefore, the worst-case PAPR for an N-tone multi-carrier signal on a uniform frequency grid is

$$\text{PAPR}_{\text{max}} = 10 \log_{10} \frac{P_{\text{peak}}}{P_{\text{avg}}} = 10 \log_1 0N.$$

Fig. 2.9 shows how the worst-case PAPR increases with the number of tones in an OFDM or FDM signal. While signal processing techniques exist to reduce PAPR [10, 11], in general the growth in PAPR is also offset by the decreasing probability of encountering the particular instance where all of the sub-carriers align in phase. For this reason the PAPR of a multitone signal is usually capped to between 10 and 15 dB.

2.2 Amplifier Analysis

Next, key power amplifier (PA) terminology and theory are reviewed. This establishes the necessary background for understanding why high peak-to-average power ratio (PAPR) significantly reduces transmitter efficiency, and offers insight into how fundamental amplifier behavior can be adjusted to recover lost efficiency.

2.2.1 Terminology

2.2.1.1 Power

There are four types of power commonly used in PA design [12]:

- **Delivered power** (P_{del}): The actual power transferred from the amplifier to the load.

- **Available output power** (P_{avn}): The maximum power the amplifier can provide to the load, assuming ideal matching between the amplifier and load impedances. This represents the theoretical upper limit of P_{del}.

- **Input Power** (P_{in}): The power supplied to the amplifier's input from the signal source or generator. This is the power the amplifier receives to process and amplify.

- **Available Source Power** (P_{avs}): The maximum power the generator (signal source) can deliver to the amplifier, assuming ideal impedance matching. This is the theoretical upper limit of P_{in}.

The "available" powers (P_{avn} and P_{avs}) assume perfect matching, while "delivered" powers (P_{del} and P_{in}) reflect actual conditions, which may include losses due to imperfect matching or circuit inefficiencies. The proper choice of power metric depends on the application, but the default form of output power used in this thesis is P_{del} and the default form of input power is P_{avs}

2.2.1.2 Gain

Gain is the fundamental metric of all amplifier behavior as it quantifies the magnitude of amplification. There are three types of gain relevant to PA design:

- **Power gain** is the ratio of total power delivered to the load to the total power delivered to the input of the amplifier from a generator;

$$G_p = \frac{\mathrm{P_{del}}}{\mathrm{P_{in}}} \tag{2.7}$$

- **Transducer gain** is the ratio of total power delivered to the load to the maximum power available from the source; and

$$G_t = \frac{\mathrm{P_{del}}}{\mathrm{P_{avs}}} \tag{2.8}$$

- **Available power gain** (G_a) is the ratio of maximum power available from the amplifier to the maximum power delivered from the generator.

$$G_a = \frac{\mathrm{P_{avn}}}{\mathrm{P_{avs}}} \tag{2.9}$$

If the amplifier is conjugately matched, all three definitions for amplifier gain are equivalent. Unless otherwise specified, G_t is the default form of gain used in this thesis.

2.2.1.3 Efficiency

For PA design, efficiency quantifies the ratio of useful generated power to the total consumed power. There are three general forms of PA efficiency:

(1) **Drain Efficiency** (η_d) is the ratio of total RF power delivered to the DC power consumed;

$$\eta_d = \frac{P_{del}}{P_{dc}} \tag{2.10}$$

(2) **Total Efficiency** (η_t) the ratio of total RF power delivered to the DC power consumed;

$$\eta_t = \frac{P_{del}}{P_{avs} + P_{dc}} \tag{2.11}$$

(3) **Power Added Efficiency** (PAE) the ratio of total RF power **added** to the system to the total DC power consumed.

$$\text{PAE} = \frac{P_{del} - P_{avs}}{P_{dc}} \tag{2.12}$$

Drain efficiency, η_d, is the easiest to measure and analyze; however, it does not factor in the RF power required to drive the amplifier. On the other hand, PAE, evaluates the ratio of the net RF power added to the circuit by an amplifier divided by the total DC power consumed. PAE is related to drain efficiency through:

$$\text{PAE} = \eta_d \left(1 - \frac{1}{G_t}\right) \tag{2.13}$$

From (2.13), if G_t is large then drain efficiency converges to PAE. For instance, if G_t is 10 dB then PAE is 90% of the effective drain efficiency. For this reason, if the gain of an amplifier is >10 dB then drain efficiency will be a good predictor of overall amplifier efficiency.

If the gain of an amplifier is not large then the designer should pay closer attention to the PAE. Fig. 2.10 illustrates why–from an integration perspective–it is essential to contextualize drain efficiency with gain for power amplifiers. Fig. 2.10a illustrates a 3-stage amplifier with each

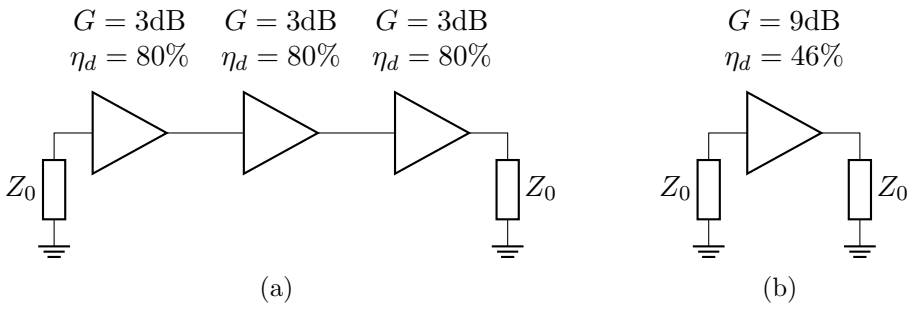


Figure 2.10: Example illustrating the importance of gain and efficiency. Compered here is a (a) a three-stage amplifier, and (b) a single-stage amplifier. Both amplifiers have the same total gain. (a) appears to have the higher overall efficiency with three high-efficiency stages, however; the total drain efficiency for both amplifiers is equivalent.

individual stage attaining an drain efficiency of 80%. Fig. 2.10b illustrates a single-stage amplifier with a quantifiably lower drain efficiency of 46%. Both cases are designed to meet a gain key performance parameter of 9 dB. At first glance it may seem that case (a) would have overall better efficiency, however; it turns out that the total drain efficiency for both is approximately 46%. For this reason, PAE is generally the preferred parameter for reporting PA efficiency as it quantifies the total RF power added by the amplifier over the total DC power consumed.

2.2.1.4 Linearity

Linearity describes how faithfully an amplifier preserves the relationship between its input and output signals. If gain quantifies the amount of amplification, linearity quantifies the quality of that amplification. In an ideal linear amplifier, the output is a scaled version of the input, following the relationship:

$$v_{out} = A_v v_{in} \tag{2.14}$$

where v_{out} is the output voltage, v_{in} is the input voltage, and A_v is the voltage gain. In RF systems, linearity is typically discussed in terms of input and output power waves.

In practice, real amplifiers deviate from this ideal in two ways:

(1) **Nonlinearity:** The output is not simply a scaled version of the input; instead, it includes

higher-order terms. This can be expressed as:

$$v_{out} = A_v v_{in} + D_2 v_{in}^2 + D_3 v_{in}^3 + \ldots + D_N v_{in}^N \tag{2.15}$$

where A_v is the linear voltage-gain of the amplifier and D_2, D_3, ..., D_N represent the coefficients of nonlinear distortion.

(2) **Memory Effects:** The output at any given time depends not only on the current input but also on past input values. These effects are typically caused by phenomena such as thermal dynamics or charge storage. While memory effects are important in amplifier behavior, they are not the focus of this thesis.

The nonlinear distortion coefficients, D_k, in (2.15) quantifies the nonlinear behavior of an amplifier as a function of an input voltage v_{in}, however; in practice PA linearity is described through the following metrics:

(1) **PA Figures of Merit:** These describe intrinsic amplifier behavior, independent of a specific signal.

- **Compression Point ($\mathbf{P_{1dB}}$, $\mathbf{P_{3dB}}$):** The output power at which the gain drops by 1 dB (or 3 dB) from its small-signal value. Indicates the onset of strong nonlinearities.
- **Third-Order Intercept Point (IIP3/OIP3):** The hypothetical input/output power where the extrapolated third-order intermodulation product equals the fundamental output. Useful for assessing weak nonlinearities.

(2) **Time-Domain Linearity Metrics:** These quantify how much a specific signal is distorted by the amplifier in time-domain.

- **Error Vector Magnitude (EVM):** Measures the root-mean-square (RMS) error between the ideal and actual received symbols in the IQ plane. Widely used for digital modulation.

- **AM/AM and AM/PM Conversion:** Quantify how the amplitude and phase of amplifier gain changes as a function of input signal amplitude, respectively.

(3) **Frequency-Domain Linearity Metrics:** These quantify how much a specific signal is distorted by the amplifier in the frequency domain.

- **Adjacent Channel Power Ratio (ACPR/ACLR):** The ratio of power leaked into adjacent frequency channels to the power in the main channel. Indicates out-of-band distortion.
- **Noise Power Ratio (NPR):** Measures in-band distortion by comparing the power in a notched frequency region to the average power elsewhere in the band. Indicates in-band distortion.

In summary, linearity metrics help designers understand both the intrinsic behavior of amplifiers and their impact on real-world signals, guiding the selection and optimization of amplifiers for specific applications.

2.2.2 Elements of an Amplifier

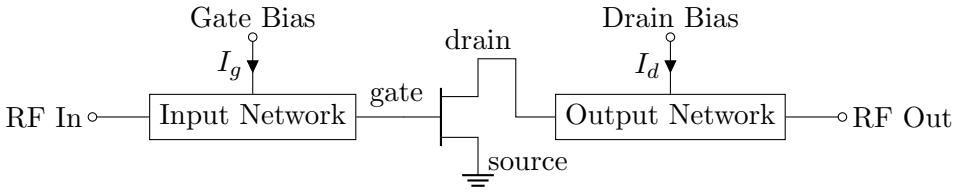


Figure 2.11: The elements of a single-stage amplifier.

Fig. 2.11 illustrates the three fundamental elements of an amplifier using a common-source transistor. The core element of any solid-state amplifier is the transistor[2] which provides the action required for amplification. Input and output networks are also required to provide the bias and RF matching to the transistor element. They are illustrated together in Fig. 2.11 because it is often prudent for bandwidth to directly integrate biasing into the matching network and therefore–in

[2] depicted here as a field-effect transistor (FET)

many practical implementations–are designed together. Later chapters in this thesis will discuss methods for input and output network design.

There are two types of transistors used in modern electronics: field effect transistors (FETs) and bipolar junction transistors (BJTs). The transistor depicted in Fig. 2.11 is a FET-type transistor. FET characteristics are broadly categorized in two ways: its mode and type of majority carrier. The mode of a FET may either be depletion (normally-on) or enhancement (normally-off).[3] The majority carrier is that which carries charge through the transistor channel and may either be n-type–where the electrons are majority carriers–or p-type–where the holes, i.e. absence of electrons, are the majority carriers. The majority carrier typically indicates the polarity of bias required to turn on/off an enhancement/depletion mode transistor, respectively.

This thesis works almost exclusively with a type of FET transistor called a high electron-mobility transistor (HEMT). In HEMTs the channel is a quantum well called a 2-dimensional electron gas–or 2DEG–which forms at the boundary between two materials with different bandgaps. The nature of the 2DEG channel means that conventional HEMTs are typically depletion-mode and n-type. This thesis uses HEMTs grown in a technology called Gallium Nitride (GaN). The high breakdown voltage and current handling of GaN technology means it can achieve higher power densities. Furthermore, this thesis uses GaN which is grown on a Silicon Carbide (SiC) substrate which is a good thermal conductor (when compared to competing technologies such as Silicon or Gallium Arsenide)–which is important for device longevity. For more information, [13] discusses specific examples where GaN is relevant to high-power, high-frequency circuits.

2.2.3 Intrinsic Model

Fig. 2.12 shows a circuit-based model of a field-effect transistor (FET), where the intrinsic device is represented by a voltage-controlled-current-source I_d in parallel with a drain-source resistance R_{ds}. This Norton equivalent circuit is useful for analyzing how the transistor sources or

[3] "Normally-on" means that the transistor conducts when $V_{GS} = 0V$ and "normally-off" means that the transistor does not conduct when $V_{GS} = 0V$

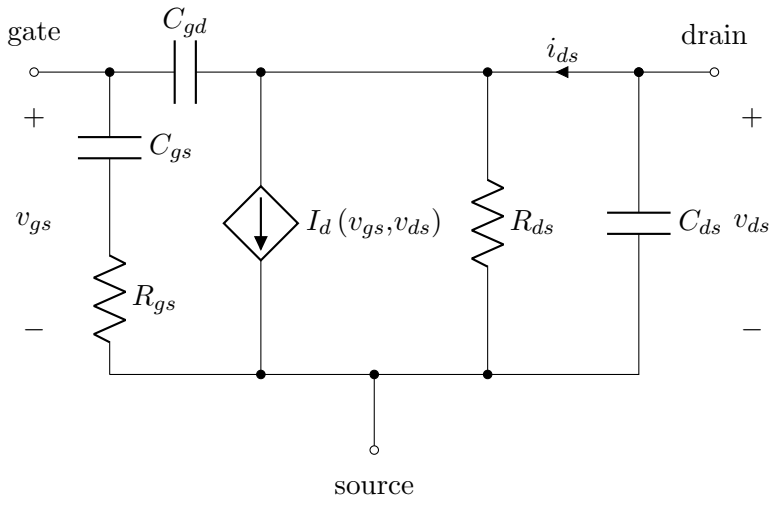


Figure 2.12: Intrinsic, equivalent-circuit model of a field-effect transistor based on the model from [14].

sinks RF power. To understand the transistor's operation, the drain current i_{ds} is plotted versus the drain-source voltage v_{ds} for different gate-source voltages v_{gs}, resulting in a set of IV curves. Fig. 2.13a presents a simplified IV curve plot for a transistor.[4] Fig. 2.13b highlights two key regions of every IV curve plot: the knee-region (or ohmic-region) and the saturation region. In the knee region, the drain-source current i_{ds} depends on both v_{gs} and v_{ds}. In the saturation region, i_{ds} depends primarily on v_{gs}. Fig. 2.13b further illustrates the instantaneous power loss at each point in the IV plane.

2.2.4 Fundamentals of PA Behavior

Fig. 2.14 illustrates a simplified transistor model for analyzing the AC behavior of a power amplifier. In this model, the resistive and capacitive elements from Fig. 2.12 are omitted for clarity. The transistor is represented as a voltage-controlled current source that operates exclusively in the saturation region of the IV curves, meaning its output current is determined only by the gate-source voltage, v_{GS}.

A bias tee is included to establish a fixed DC drain-source voltage, V_{DS}, which is essential

[4] This example assumes abrupt transitions between regions on the IV plane and that $R_{ds} \to \infty$. Effects such as self-heating and knee walkout are not considered here.

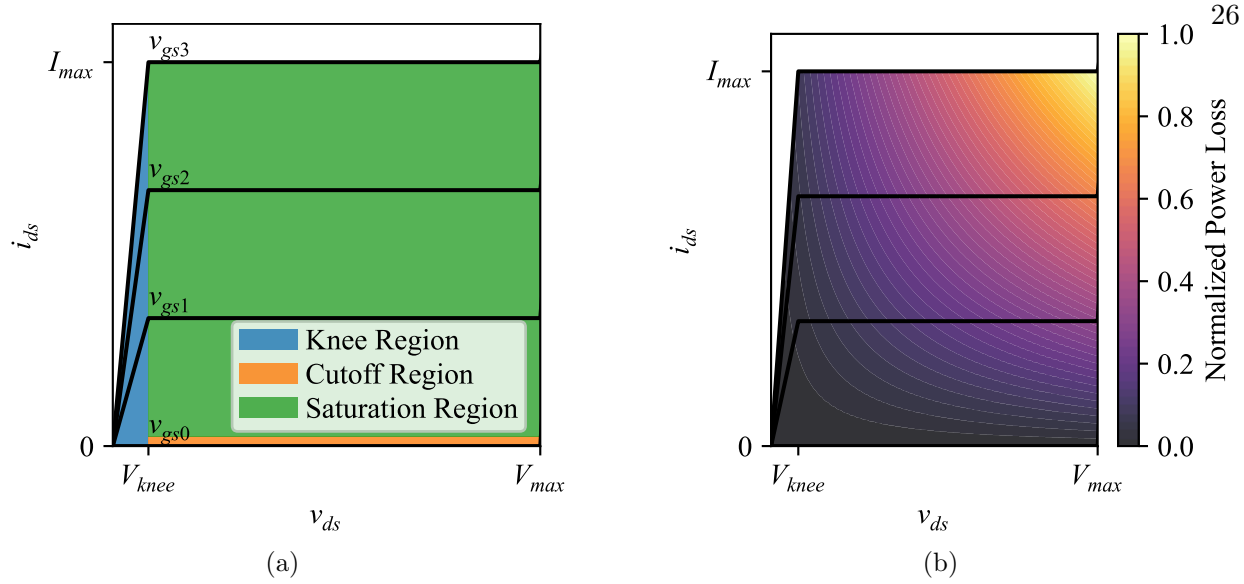


Figure 2.13: Idealized plot of a transistor's IV curves. (a) illustrates the regions of operation over the IV curves along with the v_{gs} values used to achieve them and (b) illustrates the corresponding instantaneous power loss for each point in the IV plane.

for proper PA operation. The bias tee consists of a large inductor (L_{bias}) that allows DC current to flow, and a large capacitor (C_{block}) that blocks DC from reaching the load, thereby separating the DC and AC signal paths. After the bias tee, a harmonic trap presents a short circuit to all harmonics above the fundamental frequency, ensuring that the load voltage remains sinusoidal. The load resistor (R_L) completes the output circuit.

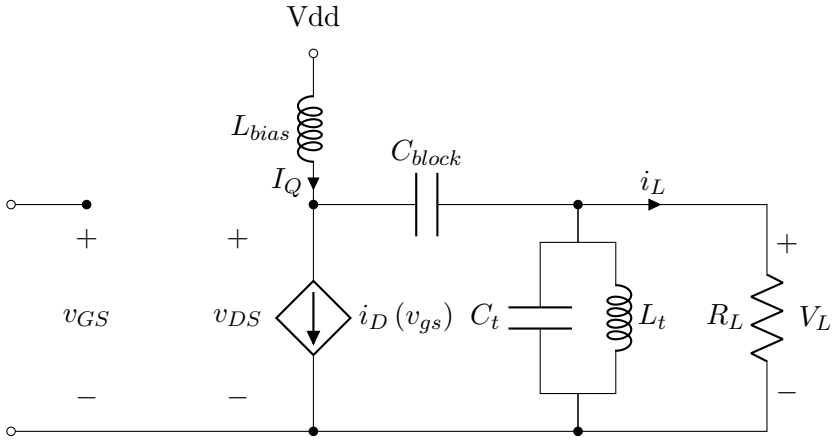


Figure 2.14: Model of an amplifier with a harmonic trap.

The bias tee is critical to the operation of the model in Fig. 2.14. As the voltage-controlled current source varies, the difference between the quiescent current (I_Q) and the instantaneous drain current (i_D) flows through the branch connected to the load. This mechanism enables the delivery of power to R_L.

From [15] drain conduction current, i_D, is only a function of carrier phase, θ:

$$i_{DS}(\theta) = \begin{cases} \frac{i_{max}}{1-\cos(\alpha/2)} \left[\cos(\theta) - \cos(\alpha/2)\right] & |\theta| < \alpha/2 \\ 0 & \text{otherwise} \end{cases}, \tag{2.16}$$

where α is the conduction angle which corresponds to the portion of the carrier cycle where the transistor is conducting. (2.16) assumes that the carrier phase has been wrapped to a value between $-\pi$ and π radians. The DC and fundamental-frequency components of (2.16) are calculated in [15] and are modified here into a piecewise form to account for an effect later referred to as "lift-off":

$$i_{DS,0} = \begin{cases} \frac{i_{max}}{2\pi} \frac{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}{1-\cos(\alpha/2)} & i_{max} - I_Q \geq I_Q \\ I_Q & \text{otherwise} \end{cases} \tag{2.17}$$

$$i_{D1} = \begin{cases} \frac{i_{max}}{2\pi} \frac{\alpha - \sin\alpha}{1-\cos(\alpha/2)} & i_{max} - I_Q \geq I_Q \\ i_{max} - I_Q & \text{otherwise} \end{cases} \tag{2.18}$$

where i_{max} is the peak value of i_{DS} and α is the conduction angle.

The harmonic trap and C_{block} ensure that only the fundamental component of v_{DS} is seen at the load. At AC, the load is effectively in parallel with voltage across the intrinsic current source, v_{DS}:

$$v_L(\theta) = v_{DS}(\theta) = -v_{DS,1}\cos(\theta) \tag{2.19}$$

Likewise, the current through the load, i_L, is equal in magnitude but opposite in phase with the fundamental, AC component of i_D. Because of C_{block}, no DC current can travel through the load and therefore, the equation for the load current must be:

$$i_L(\theta) = -i_{DS,1}(\theta) = -i_{DS,1}\cos(\theta) \tag{2.20}$$

Using the aforementioned voltage and current definitions, the fundamental power delivered to the load P_1 and DC power consumed by the transistor P_0 are related to these current components through the following:

$$P_1 = \frac{v_{DS,1} i_{DS,1}}{2} = \frac{v_{DS,1}^2}{2R_L} = \frac{i_{DS,1}^2 R_L}{2} \quad \text{and} \quad P_0 = i_{DS,0} V_{DD} \tag{2.21}$$

where

$$R_L = \frac{v_{L1}}{i_{L1}} = -\frac{v_{DS,1}}{i_{DS,1}} \tag{2.22}$$

Using (2.17) and (2.18) the drain efficiency for a given V_{DD}, V_{Knee}, and α is:

$$\begin{aligned} \eta_D(\alpha; V_{DD}, V_{Knee}) &= \frac{P_1}{P_0} \\ &= \frac{V_{DD} - V_{Knee}}{2V_{DD}} \frac{i_{DS,1}}{i_{DS,0}} \\ &= \frac{V_{DD} - V_{Knee}}{2V_{DD}} \frac{\alpha - \sin\alpha}{2\sin(\alpha/2) - \alpha\cos(\alpha/2)}, \end{aligned} \tag{2.23}$$

where V_{DD} and V_{Knee} are parameters for the function η_D. Likewise the power delivered to the load, P_{del}, is equal to:

$$P_{del}(\alpha) = \frac{1}{\pi} \frac{\alpha - \sin\alpha}{1 - \cos(\alpha/2)}, \tag{2.24}$$

normalized to unity in the case where the conduction angle is 360°.

Another important consideration of conduction angle is its impact on the gain of an amplifier. Strictly speaking, the model presented in Fig. 2.14 cannot be used to quantify gain as no power may be delivered to the input–as it is an open circuit. However, the voltage gain of the amplifier is quantifiable and therefore may be used as a reference to infer the corresponding impact on amplifier power gain. The normalized power gain for a given conduction angle is:

$$G_P(\alpha) = \left(\frac{1}{4\pi}\right)(\alpha - \sin\alpha)\left[1 - \cos(\alpha/2)\right], \tag{2.25}$$

where G_P is unity when the conduction angle is 360°.

2.2.4.1 Amplifier Classes

Amplifier operation modes, or "classes", are defined by the shapes of their current and voltage waveforms. From the model shown in Fig. 2.14, the four fundamental power amplifier classes—A,

AB, B, and C—are characterized by a sinusoidal voltage waveform and a current waveform described by (2.16). Since the shape[5] of the current waveform in (2.16) depends only on the conduction angle α, each amplifier class is uniquely specified by its conduction angle as:

- **Class A:** The transistor conducts for the entire RF cycle (2π radians);
- **Class AB:** The transistor conducts for more than half but less than the full cycle ($\pi < \alpha < 2\pi$ radians);
- **Class B:** The transistor conducts for exactly half of the cycle (π radians); and
- **Class C:** The transistor conducts for less than half of the cycle ($\alpha < \pi$ radians).

The conduction angle also impacts an amplifier's maximum achievable gain and efficiency. Fig. 2.15 shows how drain efficiency, delivered power, and power gain vary with conduction angle, calculated using (2.23) (with $V_{DD} = 1$ and $V_{Knee} = 0$), (2.24), and (2.25), respectively. This figure also highlights the regions corresponding to each amplifier class. Class A and Class B are

[5] This assumes $i_{max} \neq 0$.

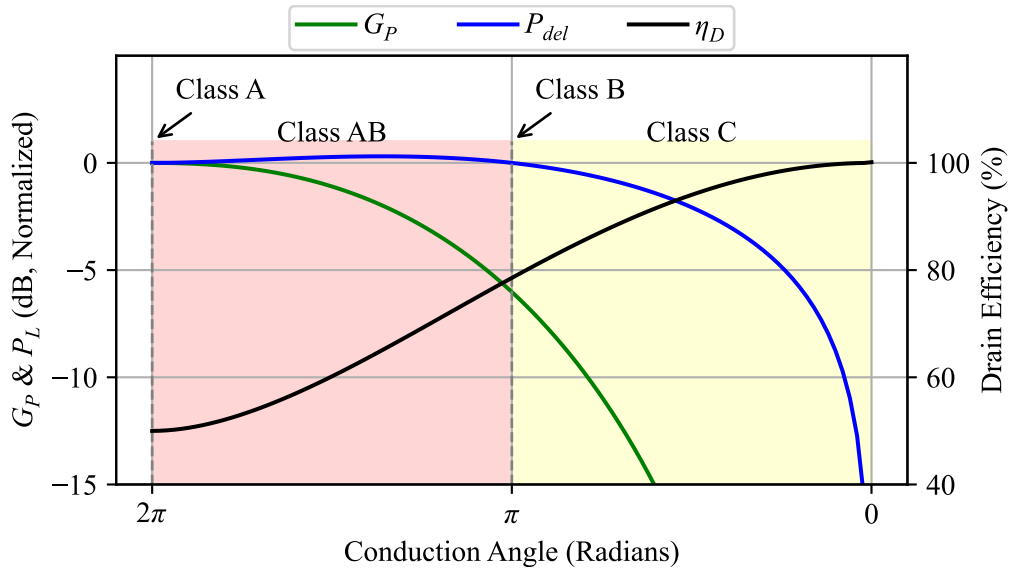


Figure 2.15: Drain efficiency (η_D), delivered power (P_{del}), and power gain (G_P) versus amplifier conduction angle (α). The delivered power and power gain are normalized to the case where the conduction angle is 2π.

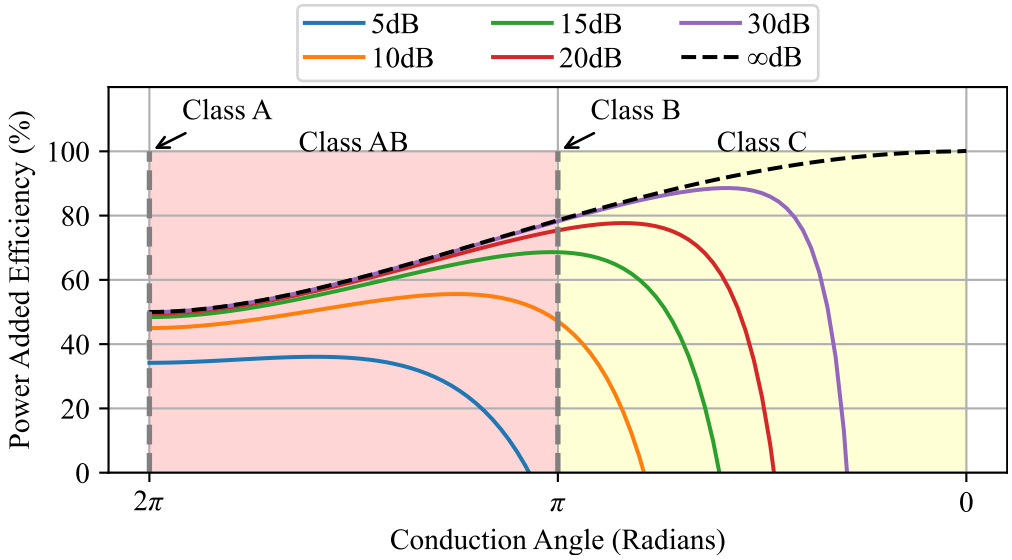


Figure 2.16: Power added efficiency (PAE) versus conduction angle for various Class A gain levels.

represented by dashed lines at their specific conduction angles, while Class AB and Class C are shown as shaded regions.

Selecting the appropriate amplifier class is a key design decision. For a given device size, deep Class AB operation is optimal for maximizing output power [15]. Class A provides the highest gain, while Class B offers the highest drain efficiency for a given output power. However, drain efficiency alone does not capture the full picture, as it does not account for amplifier gain. To address this, power added efficiency (PAE) can be expressed as a function of conduction angle by combining (2.23) and (2.25) (using (2.13)):

$$\eta_{PAE}\left(\alpha; V_{DD}, V_{Knee}, G_{P,Max}\right) = \eta_D\left(\alpha; V_{DD}, V_{Knee}\right)\left[1 - \frac{G_{P,Max}}{G_P\left(\alpha\right)}\right], \tag{2.26}$$

where $G_{P,Max}$ is the power gain at Class A. Fig. 2.16 shows how PAE depends on conduction angle and G_P in Class A (with $V_{DD} = 1\,\text{V}$ and $V_{Knee} = 0$). The optimal conduction angle for maximum PAE depends on the available gain. If the amplifier has high gain, Class C operation can achieve very high efficiency. However, for amplifiers with gain $\leq 15\,\text{dB}$, Class B or higher conduction angles are preferable. This explains why high-frequency amplifiers are rarely biased in Class C or even Class B: the available gain is often too low to justify these modes.

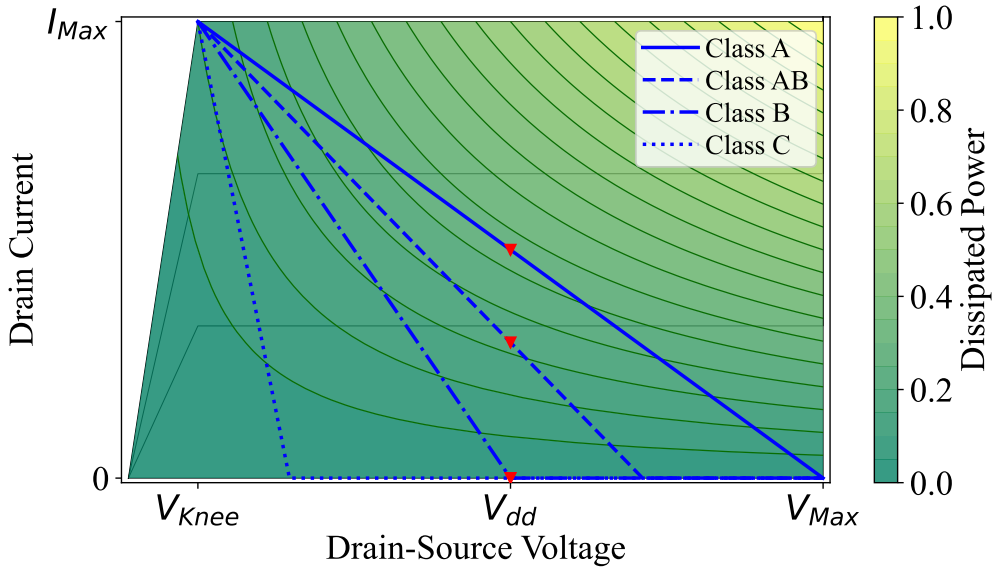


Figure 2.17: Load lines of a Class A, Class AB, Class B, and Class C amplifier plotted on the IV curve plane of a transistor. Contours of instantaneous power loss are provided to show how low-conduction angle classes improve drain efficiency by reducing overall power loss.

2.2.4.2 The Load Line Model

Another way to view the drain current and voltage waveforms is to plot their trajectory on the specific device's IV curve plot (i.e. Fig. 2.13)–which is also referred to as the IV plane. This trajectory is called the load line and is useful for gaining geometric insight into how well the device is making use of the available IV plane. Because the load line is directly derived from the current and voltage waveforms, the load line may also be considered the "finger-print" of a particular class of amplifier. Fig. 2.17 illustrates three load lines for a Class A, Class AB, Class B, Class C PA projected on top of the IV plane of the same transistor. The instantaneous power loss contours, from Fig. 2.13b are also included to provide yet another illustration of how reducing the conduction angle can enhance power amplifier efficiency. Note that as the conduction angle reduces, the load line moves out of the higher-power dissipation contours to lower ones. This strategy of moving a load line out of the higher–power regions of the IV plane forms the basis for essentially all PA drain-efficiency enhancement techniques.

2.2.5 Calculating the Load Line

Appendix A contains the code for the python script used to perform the load line calculations performed in this chapter. There are two ways of computing any load line. The first, is to take the discrete drain currents and voltages calculated over one period of the carrier waveform and then plot them with respect to one another. This is a useful technique for quickly plotting more complex functions–such as the simulated load line behavior of a nonlinear model[6] .

For the fundamental classes of amplifier, the load line is fully defined with two or three points. Two points if the load line has "lifted-off" from the base of the IV plane[7] and three points if the load line is intercepting $i_D = 0$. The analytic solution requires computing the value of i_{max} which is the instantaneous peak current of the time-domain waveform.[8] i_{max} is computed numerically by solving the bounded minimization function:

$$f(x) = \left| \sqrt{\frac{2P_1}{R_L}} - i_{DS,1}\left(i_{max} = x, \alpha = \alpha_{obo}(x)\right) \right|, \tag{2.27}$$

where

$$\alpha_{obo}(x) = 2\arccos\left(\frac{I_Q}{I_Q - \max(x, 2I_Q)}\right), \tag{2.28}$$

where $0 \leq x \leq I_{MAX}$, P_1 is the fundamental power from (2.21), R_L is the load resistance calculated from (2.22), $i_{DS,1}$ is the fundamental current from (2.18), and i_Q is the present operating quiescent current. Finally, $\max(x, y)$ is a function which returns the maximum value of x or y.

When $i_{max} < 2I_Q$ the load line is defined by two points on the IV plane with:

$$v_{DS} = [V_{DD} - v_{DS,1}, V_{DD} + v_{DS,1}] \quad \text{and} \quad i_D = [I_Q + i_{DS,1}, I_Q - i_{DS,1}]$$

Likewise when the opposite is true (i.e. $i_{max} \geq 2I_Q$) then the load line is making making contact with the base of the IV plane and must now include the zero intercept point. Therefore the load line is defined by the following three points:

$$v_{DS} = [V_{DD} - v_{DS,1}, V_{DD} - v_{DS,1}\cos(\alpha/2), V_{DD} + v_{DS,1}] \quad \text{and} \quad i_D = [I_Q + i_{DS,1}, 0, 0]$$

[6] This would be the go-to method for plotting the load line of more sophisticated classes such as Class F/F^{-1}, etc. or to plot the load line in the presence of multitone or harmonics.

[7] A specific case where this occurs is discussed in the next sub-section.

[8] Which should not be confused with I_{MAX} the peak current of the IV plane.

2.2.5.1 Load Line in Backoff

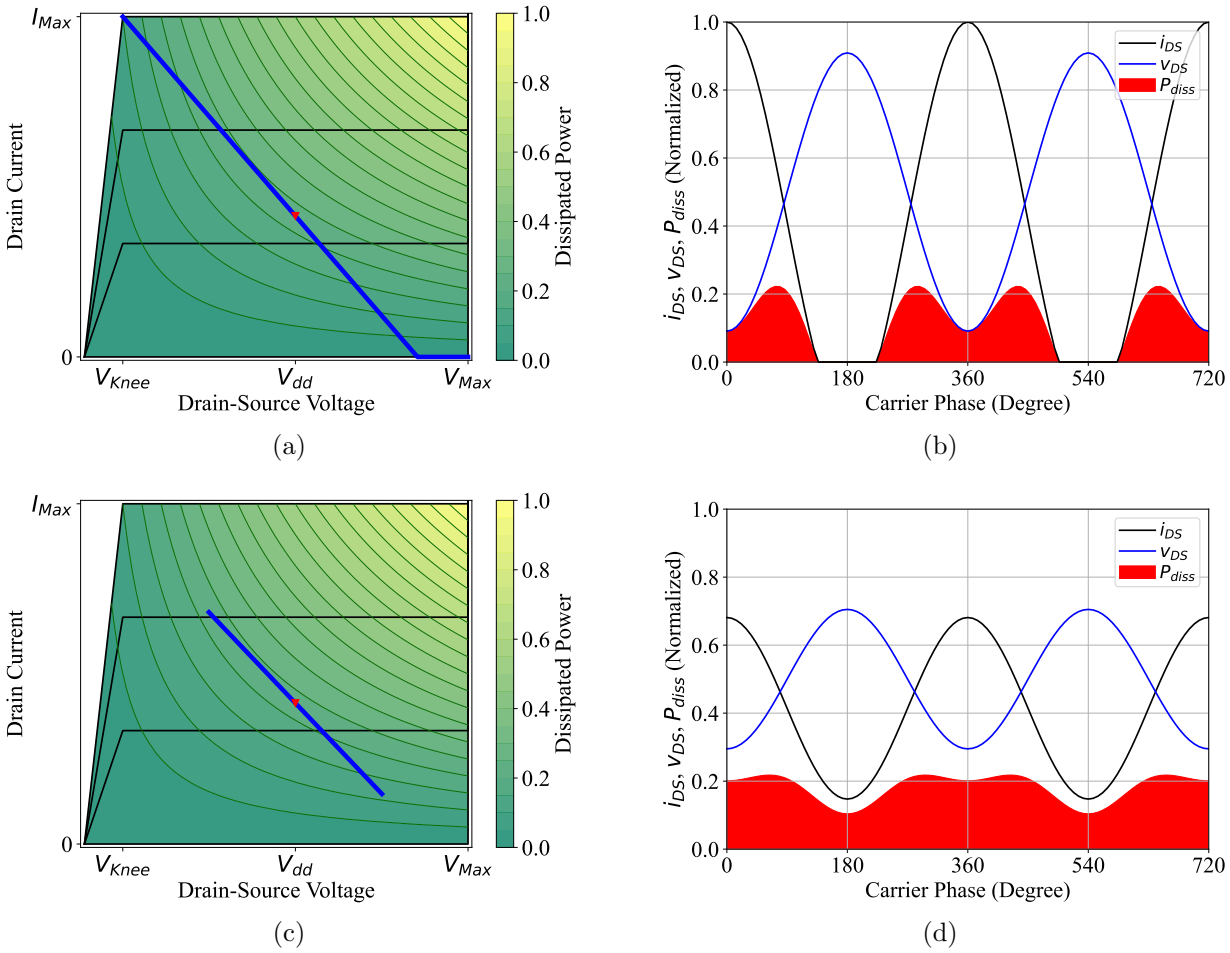


Figure 2.18: Load line and corresponding waveforms of a Class AB amplifier. (a) and (b) illustrate the case where the amplifier is operating in saturation. (c) and (d) illustrate the case where the amplifier is operating at an output power 6 dB lower than the saturated output power.

The previous sections have focused on power amplifiers (PAs) operating at their peak output power. However, it is important to understand how amplifier characteristics—such as efficiency, gain, and linearity—change as the output power is reduced from this maximum value.

Suppose the output power of the amplifier is decreased while all other boundary conditions[9] (such as supply voltage, quiescent current, load resistance, and knee voltage) remain constant. Since R_L does not change, the new fundamental voltage swing, $v_{1,obo}$, can be calculated from the

[9] Boundary conditions include V_{DD}, I_Q, V_{Max}, R_L, and V_{Knee}.

reduced output power $P_{1,obo}$ as:

$$v_{1,obo} = \sqrt{2P_{1,obo}R_L} \tag{2.29}$$

Similarly, using (2.22), the new fundamental current component is:

$$i_{1,obo} = \frac{v_{1,obo}}{R_L} \tag{2.30}$$

The updated current swing is then determined by substituting $P_{1,obo}$ for P_1 in (2.27) and (2.28). The resulting conduction angle, α_{obo}, can be found directly from $i_{max,obo}$ using (2.28).

These equations can be used to plot the behavior of the load line as the PA output power is reduced from saturation. This effect is illustrated in Fig. 2.18. Figs. 2.18a and 2.18b show the load line and drain waveforms for a saturated Class AB amplifier. Figs. 2.18c and 2.18d show the corresponding load line and waveforms when the output power is reduced by 6 dB.

Comparing Fig. 2.18a and 2.18c demonstrates that lowering the output power pulls the load line closer to the bias point (marked by a small red triangle). In this Class AB example, this results in (a) a change in conduction angle from 210° to 360°, and (b) the "lifting off" effect described previously. Examining the power dissipation contours in both load line plots reveals that the load line remains within the high-power dissipation regions even at reduced output power. In fact, the waveforms in Fig. 2.18b and 2.18d show that the amplifier spends more of the carrier cycle in these high-dissipation regions, indicating an increase in power loss.

2.2.5.2 Class Trends in Backoff

This subsection presents general trends in amplifier behavior as output power is reduced from saturation, using the load line model developed previously. In all examples, the amplifier is initially at saturation, and output power is logarithmically decreased by up to 10 dB. The IV plane parameters are set as $V_{KNEE} = 0\,\text{V}$, $V_{MAX} = 1\,\text{V}$, $I_{MAX} = 1\,\text{A}$, and the drain bias voltage $V_{DD} = 0.5\,\text{V}$.

Conduction Angle: The conduction angle is a key factor in amplifier operation. Fig. 2.19 shows contours of α_{obo}, the instantaneous conduction angle as output power is backed off. Key

observations:

- For Class A and B amplifiers, the conduction angle remains constant;
- For Class AB amplifiers, the conduction angle increases with backoff until it reaches 2π radians;
- For Class C amplifiers, the conduction angle decreases with backoff until the amplifier turns off ($\alpha = 0$).

The solid yellow region in the upper left of Fig. 2.19 indicates where a Class AB amplifier transitions to under-driven Class A operation.

Drain Efficiency and Dissipated Power: Fig. 2.20a shows how drain efficiency decreases as output power is reduced from saturation. The efficiency at saturation matches the values in Fig. 2.15, and drops as output power decreases.

To better compare how efficiency degrades across amplifier classes, Fig. 2.20b plots the ratio of backoff drain efficiency to saturated drain efficiency. Class A and AB amplifiers show a rapid decline in efficiency with backoff, while Class B and C amplifiers degrade more slowly.

Power dissipation is a critical practical aspect of PA operation as it indicates the quantity

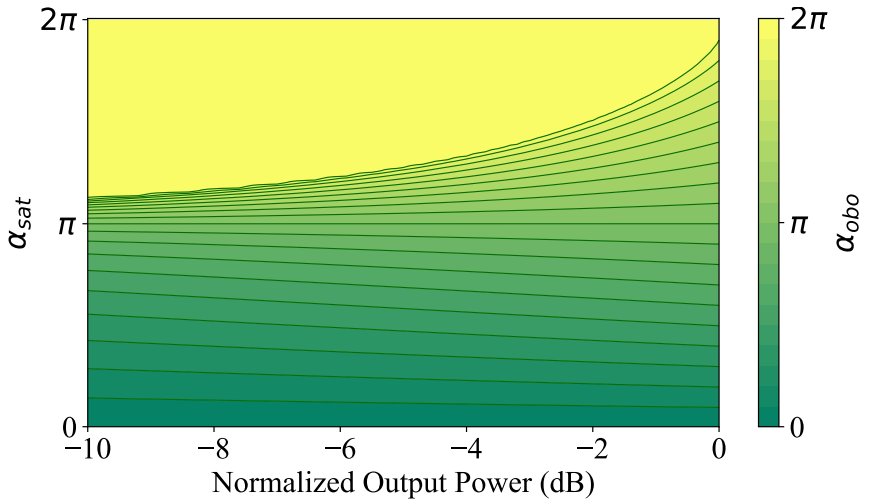
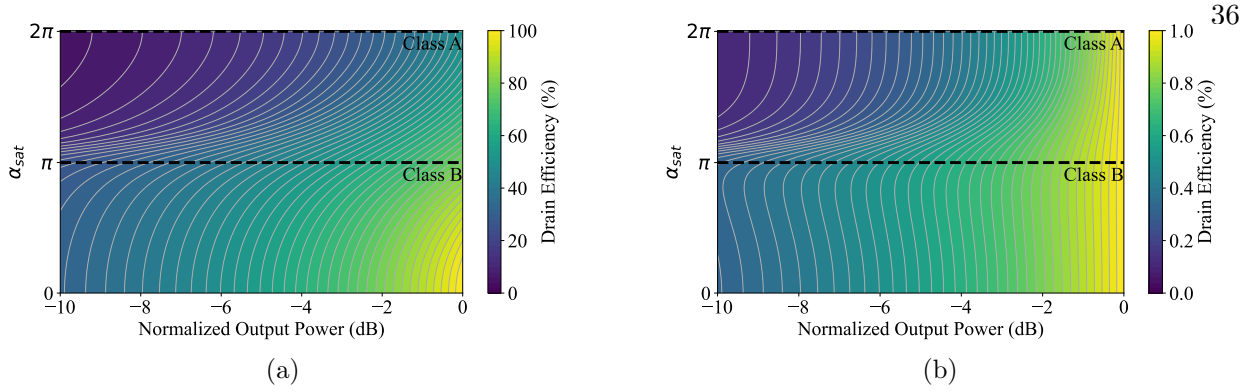


Figure 2.19: Contour plot of instantaneous conduction angle versus saturated conduction angle and output power backoff.



(a) (b)

Figure 2.20: Drain efficiency versus output power (a) value and (b) normalized to the peak value of α_{sat}.

of thermal waste generation and drives additional design considerations such as active and passive cooling. Fig. 2.21 illustrates the normalized power dissipation as output power is reduced from saturation. The plot indicates that Class A and AB amplifiers dissipate the most power among the fundamental classes. For all classes, power dissipation **increases** as output power is backed off from saturation. This highlights that efficiency loss at lower output powers is accompanied by greater waste heat, especially in linear amplifier classes.

Gain: In an ideal linear amplifier, gain does not change with input or output power. However, because conduction angle can vary with output power, gain may also change. Fig. 2.22 shows the

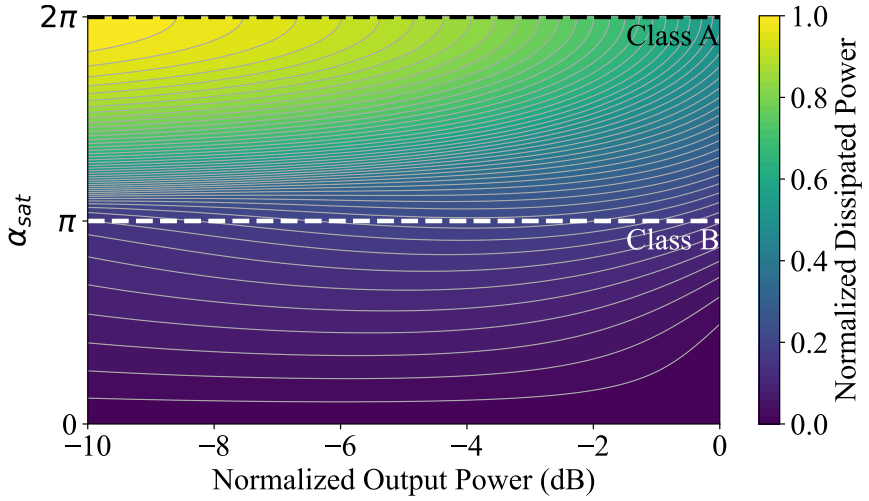


Figure 2.21: Normalized power dissipation for each amplifier class as output power is reduced.

relative change in gain from the saturated value for all conduction angles. Class A and B amplifiers maintain constant gain with output power backoff, while gain varies more rapidly in deep AB and C operation. This highlights why only Class A and B are truly linear among the fundamental PA classes.

2.3 Efficiency Recovery Architectures

Section 2.1 showed that modern, high-bandwidth communications signals tend to have high peak-to-average power ratios (PAPR) requiring amplifiers to spend **most** of their time in backoff. From Section 2.2, operating in backoff causes the PA load line to retract into regions of high power dissipation–resulting in degraded efficiency and increased levels of power dissipation, i.e. waste heat. Additionally, even though this is not the primary focus of the current discussion, gain may also change as a function of backoff. This is especially true for switch mode amplifiers which can achieve very high peak efficiencies but at the expense of very nonlinear operation.

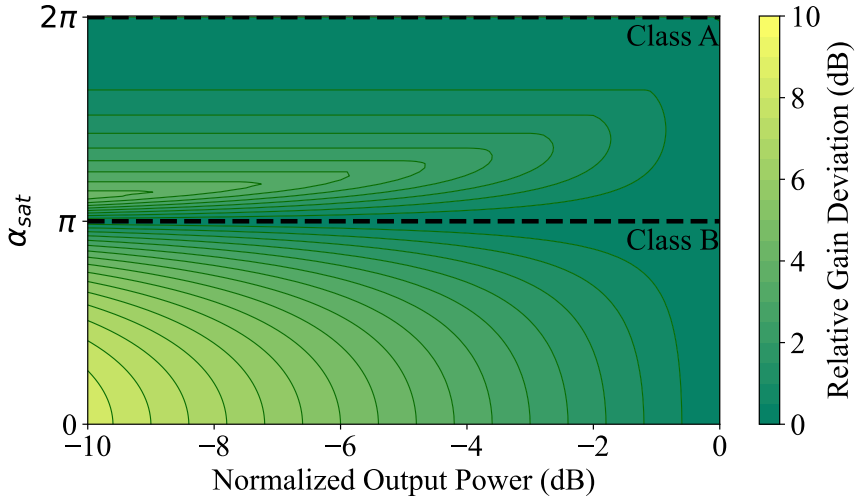


Figure 2.22: Contours showing variation in amplifier power gain versus amplifier class and output power backoff.

2.3.1 Load Line Manipulations

Fortunately, there are techniques for manipulating the load line to counterbalance the lower efficiency and increased power dissipation in backoff. There are two types of load line manipulations:

Type I Bias Manipulation: move the bias point in backoff that the load line swings around to a more optimal location in the IV plane. Geometrically, this effect is akin to shifting the bias line to a different location in the IV plane. There are two general techniques for this type of load line manipulation:

(1) **Supply Modulation**: The drain bias voltage, V_{DD}, is modulated with output power backoff. This results in a horizontal shift of the bias line throughout the IV plane, and–in the ideal load line model–does not effect the overall shape of the load line trajectory, see Fig. 2.23a.

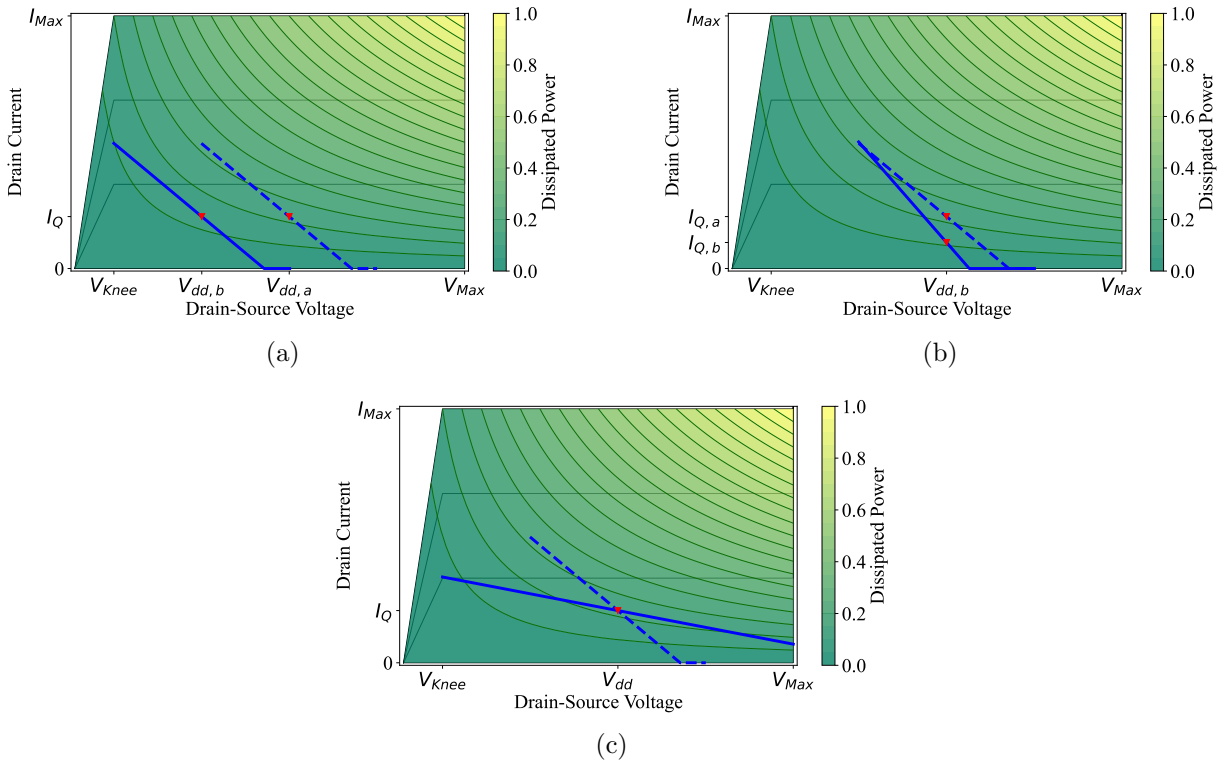


Figure 2.23: Load line manipulations for different common PA enhancement architectures (a) supply modulation, (b) gate tracking, and (c) load modulation.

(2) **Gate Tracking**: The quiescent current, I_Q, is modulated with output power backoff. This results in a vertical shift along the IV plane and may be used to adjust the backoff conduction angle, see Fig. 2.23b.

Type II Load Manipulation: change the load in backoff to alter the impedance trajectory of the load line in the IV plane. In practice this form of load line manipulation may occur at the fundamental, ω_0, or harmonics[10] , $n\omega_0$. There are three common ways load manipulation is implemented:

(1) **Reconfigurable Matching Networks**: Alter either the fundamental or harmonic value of R_L using a reconfigurable, passive matching network which typically uses switches or varactors.

(2) **Active Load Modulation**: Alter R_L at the fundamental using a second source, i.e. another amplifier. Geometrically this manifests as a flattening of the load line to recover the output voltage swing as illustrated in Fig. 2.23a.

(3) **Harmonic Injection**: Alter Z_L at a harmonic using a second source which provides power at a harmonic. Manipulations of the load line[11] harmonics geometrically manifests as altering the shape of the trajectory taken on by the load line, see [16].

2.3.2 Load and Supply Modulation

Given the critical role of load and supply modulation in enhancing power amplifier (PA) efficiency—especially under output power backoff—it is essential to review the underlying architectures for each approach. A clear understanding of these architectures not only highlights their operational principles and practical trade-offs, but also provides context for selecting the most suitable technique for a given application. By examining how each architecture manipulates the PA

[10] Harmonic load manipulations are introduced here for completeness and are not applicable to the fundamental classes of amplifier due to the harmonic trap. However, in practice a perfect harmonic trap does not exist and other classes–such as Class F–do make use of the higher harmonic content.

[11] Strictly speaking, the terminology used should be trajectory rather than line as the trajectory is not linear if the the harmonic terminations are not short circuits.

load line and integrates with modern transmitter systems, we can better appreciate their respective advantages, limitations, and the engineering challenges they address in high-efficiency RF design.

2.3.2.1 Load Modulation

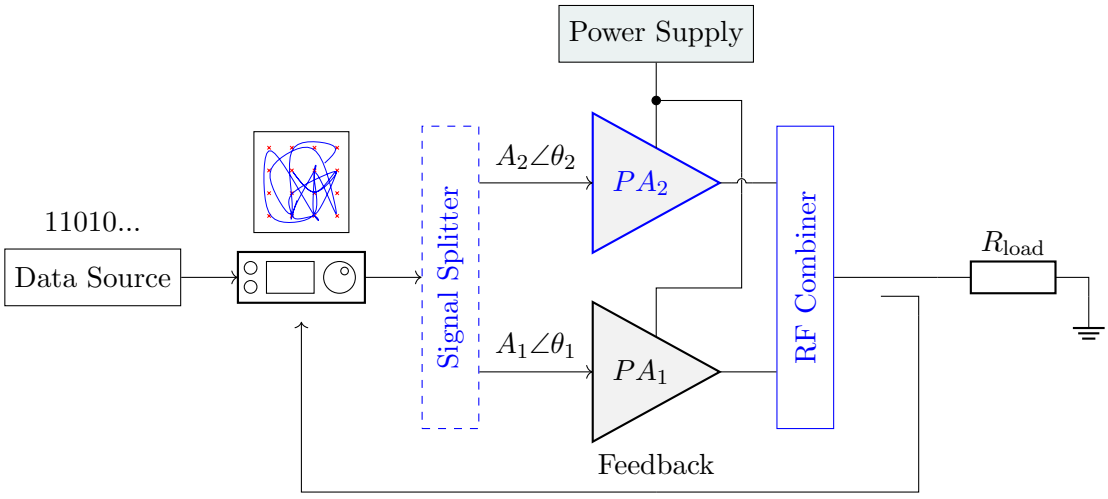


Figure 2.24: General architecture block diagram for a load-modulation transmitter.

Load modulation is a technique in which the PA load line is dynamically altered by injecting a second RF signal into the PA's RF output. While a detailed technical explanation of load modulation is not provided here, Chapter 6 provides a rigorous and general technical approach to wideband active load and source pull, which can be directly applied to understanding load modulation. Although this thesis does not focus specifically on load modulation, its widespread use for efficiency enhancement and its architectural similarities to supply modulation make it a useful point of comparison.

All load modulation architectures share common elements: a signal splitter, one or more auxiliary power amplifiers, and an RF combiner. Fig. 2.24 shows a block diagram highlighting the placement of these elements in a general load modulation system. The signal splitter distributes the RF carrier between the main and auxiliary amplifiers. Its implementation determines whether the architecture is single-drive (e.g., Doherty, using a physical splitter or coupler) or dual-drive (e.g., Outphasing, using digital signal processing). The auxiliary amplifier(s) provide additional

RF signals, typically at different amplitudes (A) and phases (θ), to modulate the main PA's load line. The RF combiner physically connects the outputs of the main and auxiliary amplifiers; in the Doherty architecture, this is typically a quarter-wavelength impedance inverter.

There are three general architectures which implement load modulation:

(1) **Doherty and Sequential Power Amplifiers:** Introduced by William Doherty in 1936 [17], the Doherty amplifier is widely used in modern telecom due to its maturity and the fact that it requires only a single RF input. In this architecture, two amplifiers—a "main"and an "auxiliary"—drive a shared quarter-wave combining network. The main amplifier is designed to reach saturation about 6 dB below the maximum output power, while the auxiliary amplifier (biased in Class C) remains off until this point. As the output power increases beyond this threshold, the auxiliary amplifier turns on and modulates the main amplifier's load line to keep it out of saturation, thereby improving efficiency in backoff. However, a key limitation of the original Doherty architecture is its use of a narrow-band quarter-wave combiner, which restricts the achievable bandwidth. Sequential amplifiers extend the Doherty concept by using three or more amplifiers to further enhance efficiency over a wider range of output power backoff.

(2) **Outphasing:** First described by Chireix in the 1930s [18], outphasing uses two generally switch-mode (highly efficient, nonlinear) amplifiers. Unlike the Doherty amplifier, the signal splitter of this architecture is typically implemented as as a dual-drive system where the signals to either amplifier has a constant envelope but modulated phase furthermore there is no distinct "main" and "auxiliary" amplifier, but rather two amplifiers which load modulate each other. The phase difference between the two amplifiers, along with the design of the reactive output combiner, enables load modulation and can–in theory–achieve greater efficiency recovery from that of the canonical Doherty approach[15, 19]. Similar to the Doherty architecture, the combiner for this approach is typically narrow-band; however, transformers may be used to achieve greater operating bandwidths [19]. Additional

modifications to this architecture include single-drive outphasing amplifiers [20], asymmetric multilevel outphasing (AMO) [21], multi-way outphasing [22, 23, 24], and mixed-mode outphasing[25]–though this is certainly not an exhaustive list. Demonstrations of Outphasing X-band amplifiers may be found [26, 27, 28]. For more information on the topic, [19, 29] present a comprehensive analysis of the history, theory, and variations of the Outphasing architecture.

(3) **Load Modulated Balanced Amplifier (LMBA):** Introduced by Shepphard et al. in 2016 [30], the LMBA is the newest of the load modulation architectures reviewed in this work. It consists of a balanced amplifier and a control amplifier that injects power into the isolation port of the output coupler. The key development in this architecture is that the output combining structure is implemented with a quadrature hybrid coupler–which can be designed for operating bandwidths in excess of an octave (i.e. such as the Lange coupler [31]). This readily enables broadband operation [32, 33, 34]. Furthermore, this architecture inherits the excellent input isolation of balanced amplifiers [15] which is excellent for system-level integration. There are some drawbacks to the LMBA architecture. First, now three amplifiers are required–two main and a "control" amplifier to perform load modulation–which can be somewhat of a disadvantage for space-constrained applications such as integrated circuit design. This challenge is addressed to some degree by a proposed variant called the Orthogonal-LMBA (O-LMBA) [35] where the control amplifier is replaced with a reactive load and the control signal is applied to the input isolation port. Another drawback drawback of the original LMBA architecture is that it was originally presented as a dual-drive scheme–which adds additional signal processing. A single-ended variant, the RF-input LMBA [32], address this by introducing a signal splitting network between the balanced amplifier and control amplifier paths. Other variants of the LMBA include the Sequential LMBA (SLMBA) [36], and double-balanced LMBA [37]. For further details, [38, 39] presents a historical and in-depth technical analysis of LMBA operation.

2.3.2.2 Supply Modulation

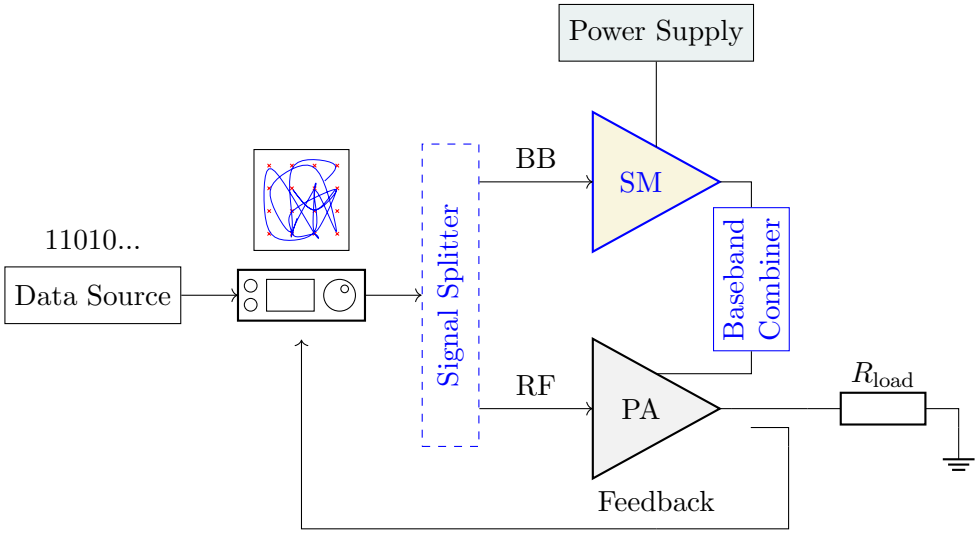


Figure 2.25: General block diagram of a supply modulation architecture. A new "amplifier" is introduced as the modulator which provides the baseband power to the envelope tracking amplifier from Fig. 2.1

Supply modulation is an alternative approach for PA efficiency enhancement. Fig. 2.25 illustrates the block diagram for a general supply modulation architecture. Like the load modulation architecture, supply modulation also has a signal splitter, secondary amplifier and a combining network. However, these elements are implemented differently. In this architecture, the secondary amplifier–or supply modulator (SM)–operates on the signal's envelope and controls the supply of the "main" PA. Because the envelope of a signal operates at baseband frequencies which are much lower than that of the carrier, the implementation of the signal splitter and output combiner is also different. The signal splitter of a supply modulator architecture now splits the desired signal into two components separated by **frequency**–with a low-frequency version of the signal–i.e. BB in Fig. 2.25–is sent to the SM for amplification and a version of the signal at the desired carrier frequency–i.e. RF in Fig. 2.25–being sent on to the PA. Likewise, the output combiner is generally implemented as a baseband interconnect–or bias network. This network is a low-pass filter which has a cutoff frequency well above the envelope frequency of the signal.

There are three principle categories of supply modulation:

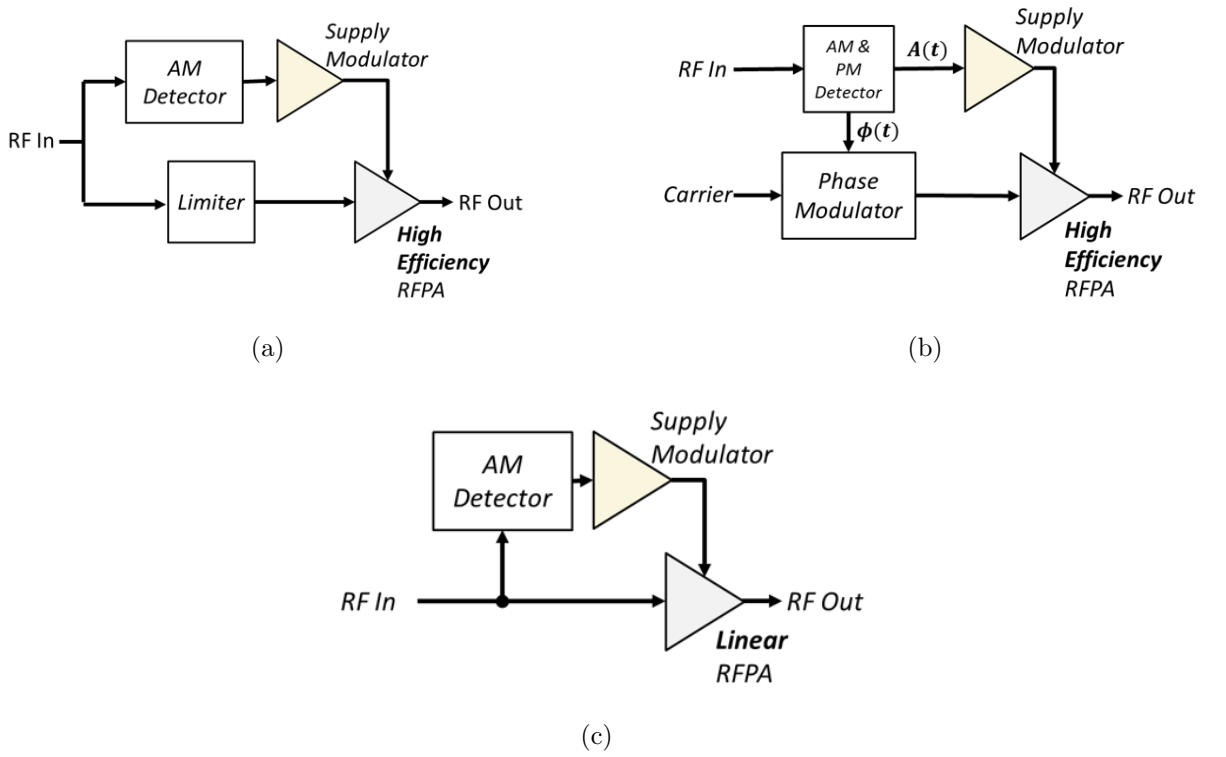


Figure 2.26: Block diagram illustrating the three principle architectures of supply modulation (a) envelope elimination and restoration, (b) polar supply modulation, and (c) envelope tracking

(1) **Envelope Elimination and Restoration (EER):** First introduced by Leonard Kahn in 1952 [40], EER is the earliest form of supply modulation. As illustrated in Fig. 2.26a, the RF amplifier operates as a high-efficiency, switch-mode amplifier held in saturation. The use of Class-E amplifiers for this architecture are discussed extensively by [41] and [42]. In the canonical form of EER the signal is split using an amplitude (AM) detector and a limiter: the AM detector extracts the envelope and sends it to the supply modulator, while the limiter removes the amplitude variations, passing only a constant-envelope, phase- and frequency-modulated signal to the PA. The original signal amplitude is then restored at the PA output by modulating the drain bias voltage. This architecture requires very precise time-alignment between the supply modulator and the PA to accurately reconstruct the signal. Alternate forms of EER–such as Hybrid EER (H-EER)–are demonstrated in [43] reporting a transmitter PAE of 40% when transmitting a 5 MHz WiMAX signal.

(2) **Polar Modulation:** This is a modern take on the original EER architecture which replaces the limiter with a phase modulator (Fig. 2.26b), improving signal reconstruction compared to the original EER approach. The approach to Polar Modulation is also slightly different from that of classical EER in that the PA is treated as a 3-port modulator rather than an amplifier [44]. Several examples of polar modulated architectures are demonstrated throughout literature. [45] reports a UHF (880 MHz) linear polar transmitter for Enhanced Data rates for GSM Evolution (EDGE) signals demonstrating an overall transmit efficiency of 56%. [46] also reports the linearity of digital polar transmitter operating at X-band with a total transmitter efficiency of 50 % for an EDGE signal. While linearity can be a challenge this architecture–due to the need for tight signal alignment–polar modulation transmission has been successfully demonstrated for high-order signals such as 4096-QAM [47] and 16,384-QAM [48] with error vector magnitudes less than 1%.

(3) **Envelope Tracking (ET):** The strict time alignment and requirement for high-efficiency, nonlinear amplifiers make EER and polar architectures challenging to implement for broadband signals. Envelope tracking addresses these challenges by allowing the full RF signal to pass through a linear PA, while the supply modulator tracks the envelope at the drain, Fig. 2.26b. This enables the use of linear amplifier classes, which are preferred for high-frequency designs due to their higher available gain. [49] reports an ET transmitter with peak PA power-added efficiencies as high as 50% when transmitting a 7.7 dB PAPR S-band W-CDMA signal. [50] also reports composite PAE improvements of 10% when modulating a 10 W PA transmitting an 18-MHz OFDM signal centered in X-band. Other examples of integrated monolithic X-band ET-chipset transmitters may be found in [51, 52]. ET may also be used to improve the efficiency of transmit arrays–as demonstrated in [53]. For more information on the topic of envelope tracking, the interested reader should refer to [52] and [54].

2.4 Conclusions

Modern high data-rate signals require power amplifiers to operate with significant output power backoff to maintain linearity. The extent of backoff needed is measured by the peak-to-average power ratio (PAPR). High PAPR in contemporary signals is primarily due to (a) bandwidth-limited digital phase and amplitude modulation schemes, and (b) the maximum achievable PAPR in multitone or multicarrier modulation schemes such as OFDM.

Traditional transmitter architectures suffer efficiency loss and increased thermal waste when handling high-PAPR signals. This efficiency degradation can be understood by examining the PA's load line and intrinsic waveforms. Many techniques for improving PA efficiency at backoff involve modifying the PA load line. Two common approaches are load modulation and supply modulation. Load modulation changes the trajectory of the PA load line, while supply modulation shifts its position on the IV plane.

Both approaches share architectural similarities, which influence their respective strengths and weaknesses. In load modulation, the signal split occurs at the carrier frequency, allowing the use of a passive network for signal splitting and enabling single-drive architectures. Dual-drive load modulation also offers greater flexibility for device optimization and in-situ tuning [30]. However, load modulation has drawbacks at higher carrier frequencies, notably the need for multiple RF amplifiers. Since linear PA efficiencies are typically low, achieving overall efficiency improvement may require nonlinear, switch-mode amplifiers or amplifiers with conduction angles at or below Class B. These strategies often involve sacrificing significant available power gain ($> 6\,\mathrm{dB}$), which is challenging at higher frequencies where gain is limited, such as in millimeter-wave applications (see Fig. 2.16). Additionally, the RF dependence of components like signal splitters, PAs, and output combiners limits their reusability across different designs. For example, a quarter-wave output combiner and auxiliary amplifier designed for an S-band (2–4 GHz) Doherty amplifier cannot be reused for an X-band (8–12 GHz) Doherty amplifier. Many of these components, except in the case of the LMBA, also have inherently narrow fractional bandwidths.

Supply modulation differs from load modulation in that its secondary amplifier (often called an envelope amplifier or supply modulator) operates at baseband and controls the drain bias of the power amplifier. Because the supply modulator does not operate at RF, its components can be reused across different designs, and its losses are largely invariant to carrier frequency. As a result, supply modulation may be better suited for efficiency recovery in high-frequency transmitters. The lower operating frequency of the supply modulator also enables the use of high-efficiency architectures common in power electronics, which are generally impractical for high-frequency amplifiers. However, supply modulation has its own challenges: the signal split design and controls are typically more complex, and the supply modulator must be capable of efficiently passing total DC power required by the amplifier in saturation, which can be substantial.

The next chapter discusses the application of supply modulation to improve the efficiency of an octave-bandwidth, X-band PA using monolithically integrated, four-level supply modulators.

Chapter 3

Supply Modulation using a Discrete Multilevel Supply Modulator

3.1 Introduction

Chapter 2 discusses why high peak-to-average power ratio (PAPR) signals degrade overall transmitter efficiency, and reviews several avenues for recovering it. Supply modulation delineates a category of techniques where a supply modulator drives the drain supply voltage of the PA–as shown in Fig. 3.1a. Envelope tracking (ET) is an approach to supply modulation where the supply modulator keeps the PA near saturation, i.e. at a high efficiency operating point, by modulating the PA's supply voltage such that it "tracks" the envelope of the PA's output signal.

Whereas the focus of the prior chapter was the PA, the focus of this chapter is the supply modulator. An ET supply modulator may track the envelope in a continuous or discrete manner. Figs. 3.1b-3.1c illustrate the PA drain waveforms for a static supply (i.e. no supply modulator), continuous-tracking supply, and a discrete-tracking supply. The type of tracking, i.e. continuous or discrete, is related to the architecture of the supply modulator which is the topic of Section 3.2 and [54]. The architecture used here is a discrete, four-level supply modulator fabricated in two RF Gallium Nitride (GaN) on Silicon Carbide (SiC) processes. GaN technologies which are optimized for RF applications have been used to develop integrated circuit (IC) supply modulators [55, 56, 57] capable of efficiently tracking large envelope bandwidths, e.g. $> 10\,\text{MHz}$, and delivering moderate powers, i.e. tens of watts, to the PA. GaN IC supply modulators may be closely integrated with the PA in the RF front end through the "chip-and-wire" approach [52] or even through monolithic integration–offer significant advantage over board-level implementations in both size and weight for

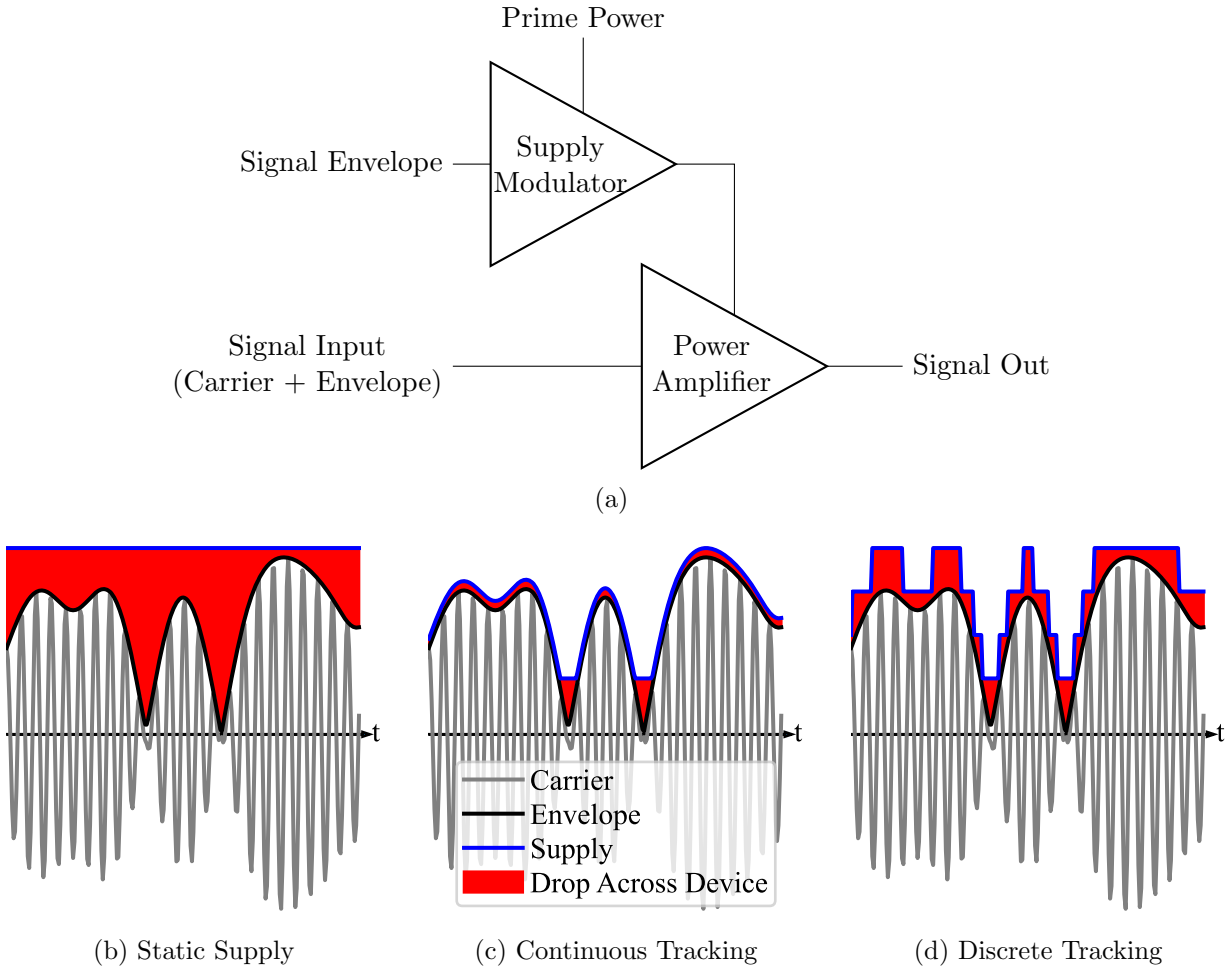


Figure 3.1: Envelope tracking is a form of supply modulation that improves power amplifier (PA) efficiency by minimizing the difference in supply voltage and the output RF envelope. Illustrated here is (a) the general block diagram of a supply modulator and PA alongside the voltage waveforms of a (b) static supply (for reference), (c) continuous-tracking supply, and (d) discrete-tracking supply.

space-constrained systems.

This chapter explores the design and test of two supply modulator chipsets intended to be used in the envelope tracking of high-frequency, moderate-power PAs. This chapter is outlined as follows: Section 3.2 provides a brief introduction to supply modulator architectures and why this work uses the discrete multilevel architecture. Section 3.3 discusses the design of a supply modulator in WIN Semiconductor's 150 nm GaN-on-SiC process. Section 3.4 reviews the simulation and measurement results of the supply modulator and compares performance with a similar design

developed in Qorvo's 150 nm GaN technology. Section 3.5 completes this chapter with a summary and some final remarks.

3.2 Supply Modulator Architectures

Supply modulators are commonly grouped into three architectures: linear, switch-mode, and multilevel. Each offers distinct trade-offs in bandwidth, efficiency, and integration complexity. A concise summary follows.

(1) **Linear supply modulators.** Implemented as analog amplifiers or open-loop linear power supplies, these provide the highest instantaneous bandwidth. Their primary drawback is low efficiency because excess energy is dissipated as heat. Linear modulators are therefore typically used in instrumentation or as a high-bandwidth complement to a lower-bandwidth, high-efficiency supply modulator [58, 59, 60].

(2) **Switch-mode supply modulators:** Implemented as a open-loop switch mode converter, this architecture is capable of achieving very high efficiencies because the transistor is operated as a switch (i.e. in the knee and cutoff regions of the IV plane, Fig. 2.13) where conduction loss is minimal. In [61], both discrete and integrated switch mode converters achieve efficiencies of 96% and 90% at switching frequencies of 10 MHz and 40 MHz, respectively. Likewise, [62] reports an integrated, synchronous Buck converter (a common type of switch mode converter) which achieves a peak efficiency of 80% when tracking a 20 MHz 4G Long Term Evolution (LTE) signal while maintaining a switching frequency of 100 MHz. Another synchronous Buck converter is also reported in [63] which attains a 64.2% total efficiency under similar operating conditions.

There are two primary challenges to this type of supply modulator. The first is that transistors have a non-zero parasitic capacitance which reduces supply modulator performance in two ways:

1. It limits how quickly the transistor can switch from an off to on state and *vice versa*– leading to unwanted, lossy conduction and "shoot-through"; and
2. Charging and discharging these capacitors results in switching loss. As the modulator switches faster, the switching loss increases.

Unfortunately, the supply modulator must track the amplitude of the modulated signal [64] which often requires the supply modulator to switch at $3x - 5x$ the signal bandwidth– making this a challenging architecture to implement for broadband signals. The second challenge is that this type of supply modulator requires a high-Q low pass filter which can be difficult to implement in planar technologies. The size of the filter can be reduced by increasing the switching frequency, but this further degrades efficiency.

(3) **Multilevel supply modulators.** These approximate the envelope with discrete voltage levels rather than continuous regulation. For a given envelope bandwidth, this type of supply modulator does not require as high of a switching frequency as a switch-mode architecture. Likewise, each level acts as a switch and therefore avoids the high conduction losses seen in linear supply modulators. Multilevel modulators are implemented with series voltage sources [65, 66] or parallel arrangements [67, 68, 57]. Series topologies can produce more voltage steps for a given number of switches but suffer higher conduction losses (current flowing through multiple switches) and increased driver complexity due to floating nodes; parallel topologies avoid floating grounds but have fewer levels and therefore cannot track the signal as closely as the series topology.

This chapter concentrates on the design and testing of monolithic multilevel supply modulators implemented in several GaN-on-SiC processes. Multilevel architectures simplify monolithic integration by avoiding the need for the high-Q filters required in by switch-mode designs. Additionally, the fast switching capability of GaN-on-SiC devices reduces switching losses and improves tracking of high-bandwidth envelope signals. The next section presents the design of a four-level supply modulator.

3.3 Supply Modulator Design in WIN 150nm GaN-on-SiC

Fig. 3.2 illustrates the circuit and timing diagrams for the the four-level, supply modulator designed in this work. The RF power amplifier is connected at the v_{out} terminal of Fig. 3.2a while the v_{dd} and v_{ss} terminals connect to static, external power supplies. The driver input signal, v_{in}, terminals connect to an external control board and bit-pattern generator. Fig. 3.2b illustrates a timing diagram for two periods of a reverse, stair-step waveform with the nominal circuit port voltages. The uppermost waveform is the supply modulator output to the PA drain, v_{out}, and the lower waveforms correspond the input signal voltages, v_{in}, corresponding to each level.

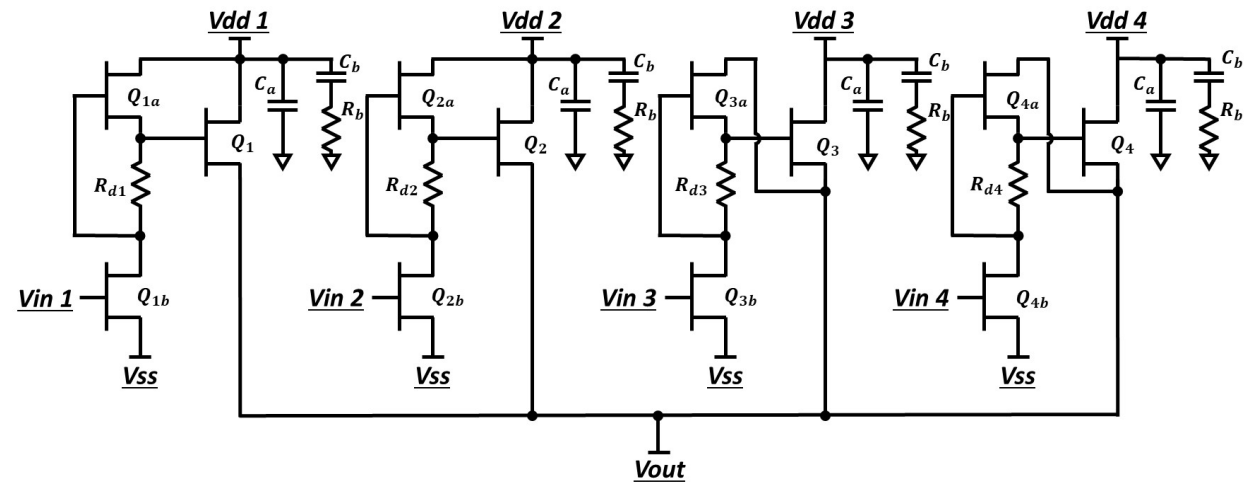
The architecture used in this work follows that of [69]. The supply modulator is made up of four distinct sections or "voltage levels", each consisting of a power switch (Q_i), a driver stage (Q_{ia}, Q_{ib} and R_{di}), and a snubber network (C_a, C_b, and R_b). At any given point of time, only one level is on with its corresponding power switch conducting. Each power switch has driver that is either an active or modified-active pull-up as discussed in [55, 69]. The lower-voltage levels, i.e. levels 1 and 2, use active pull-up drivers while the higher voltage levels, i.e. levels 3 and 4, use modified active pull-up drivers to reduce their off-state, quiescent power consumption. Each driver stage is turned on and driven independently by its corresponding input voltage v_{in}. Finally, each level has a snubber network to help lower the supply modulator's output impedance and mitigate ringing during transitions between states. The fabricated chip is illustrated in Fig. 3.3 with callouts to the corresponding terminal labels from Fig. 3.2a.

3.3.1 Power Switch Sizing

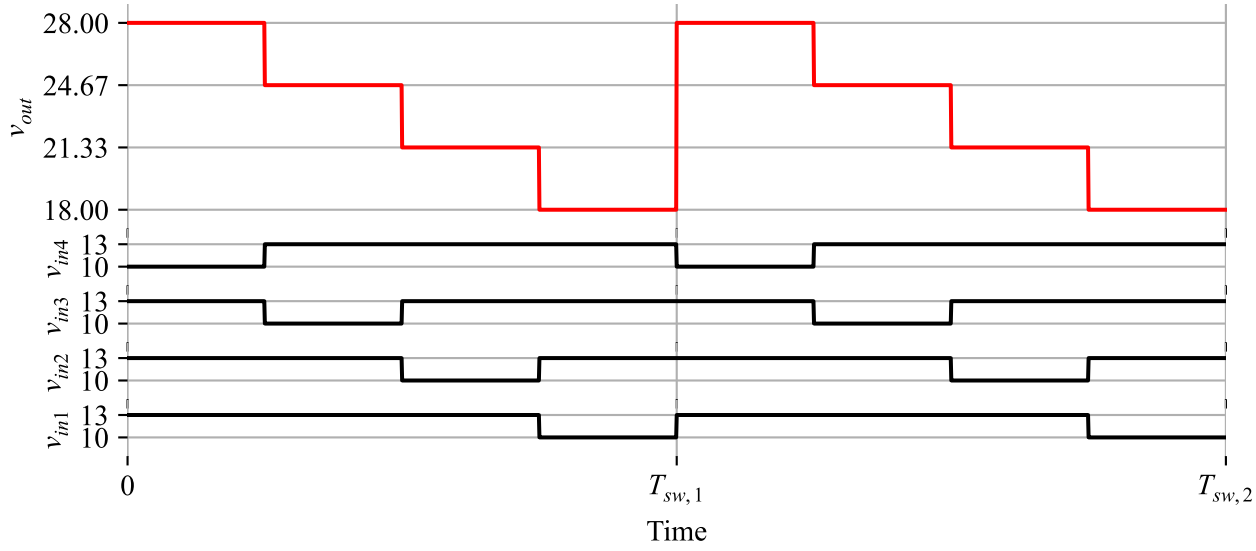
The size of each power stage is driven by three competing factors: conduction loss, switching loss, and switching speed. From [69] the conduction loss of a power stage is:

$$P_{cond} = \frac{1}{T}\int_0^{T_{sw}} R_{ds} i_{ds}\left(t\right)^2 \mathrm{d}t \tag{3.1}$$

where R_{ds} is the drain-source resistance, i_{DS} is the time-varying drain-source current, and T_{sw} is the switching period. (3.1) assumes that the on resistance of the switch is static. If within one



(a)



(b)

Figure 3.2: A discrete four-level (a) circuit diagram and (b) reverse "stair-step" timing diagram. The supply modulator is broken down into four distinct sections or "voltage levels", each consisting of a driver stage (Q_{i1} and Q_ib) and a single power switch transistor Q_i. The snubber network consisting of capacitors (C_a and C_b) and resistor (R_b) lower the output impedance and mitigate the ringing during transitions between any two voltage levels V_{ddi}. Each driver stage is turned on by an input voltage V_{in}, controlled independently. The load (RF power amplifier) is connected at the V_{out} terminal.

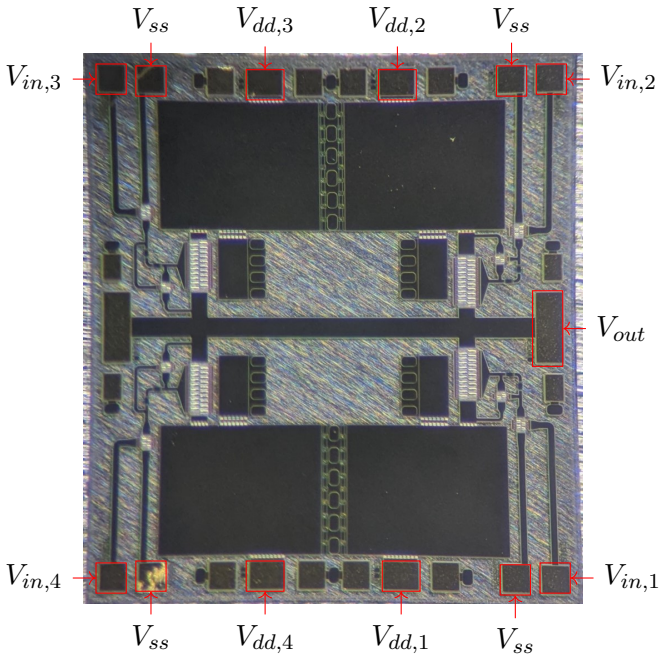


Figure 3.3: Fabricated supply modulator GaN monolithic microwave integrated circuit (MMIC) with pads annotated in accordance with Fig. 3.2a. The size of the layout is 2.68 mm×3 mm.

period of the envelope tracker waveform, $i_{ds}(t)$ is well approximated by the piecewise function

$$i_{ds}(t) = \begin{cases} I_{ds,on} & 0 \leq t \leq DT_{sw} \\ 0 & DT_{sw} < t < T_{sw} \end{cases} ,$$

where $I_{ds,on}$ is the constant on-state current of the power switch and D is the duty cycle or the fraction of the period the power switch is on–then (3.1) may be approximated as:

$$P_{cond} \approx DR_{ds}I_{ds,on}^2 \approx \frac{DR'_{ds}}{NW_g}I_{ds,on}^2 \quad , \tag{3.2}$$

where R'_{ds} is the normalized drain-source resistance of the device in Ω-mm, N is the number of fingers, and W_g is the gate width (in millimeters). Likewise, switching loss comes from charging and discharging of the power stage output capacitance during transition periods. This loss may be quantified as [55, 69]:

$$P_{switch} = \frac{1}{2}C'_{out}NW_gV_{off}^2f_{sw,avg} \quad , \tag{3.3}$$

where C'_{out} is the normalized device output capacitance in farads per millimeter, V_{off} is the electric potential across the power switch when it is not conducting, and $f_{sw,avg}$ is the average switching frequency of the power switch as defined in [69] as:

$$f_{sw,avg} = \frac{m}{T_\Delta} \ ,$$

where m is the number of switching cycles over the interval T_Δ.

Conduction loss, (3.2), decreases with device size, i.e. NW_g, while switching loss, (3.3), increases with devices size–implying an optimum device size for a given switching frequency and conduction current, $I_{ds,on}$. Also note that conduction loss depends on the current, $I_{ds,on}$, which–for a fixed V_{dd}–implies that the optimum device size is load dependant as

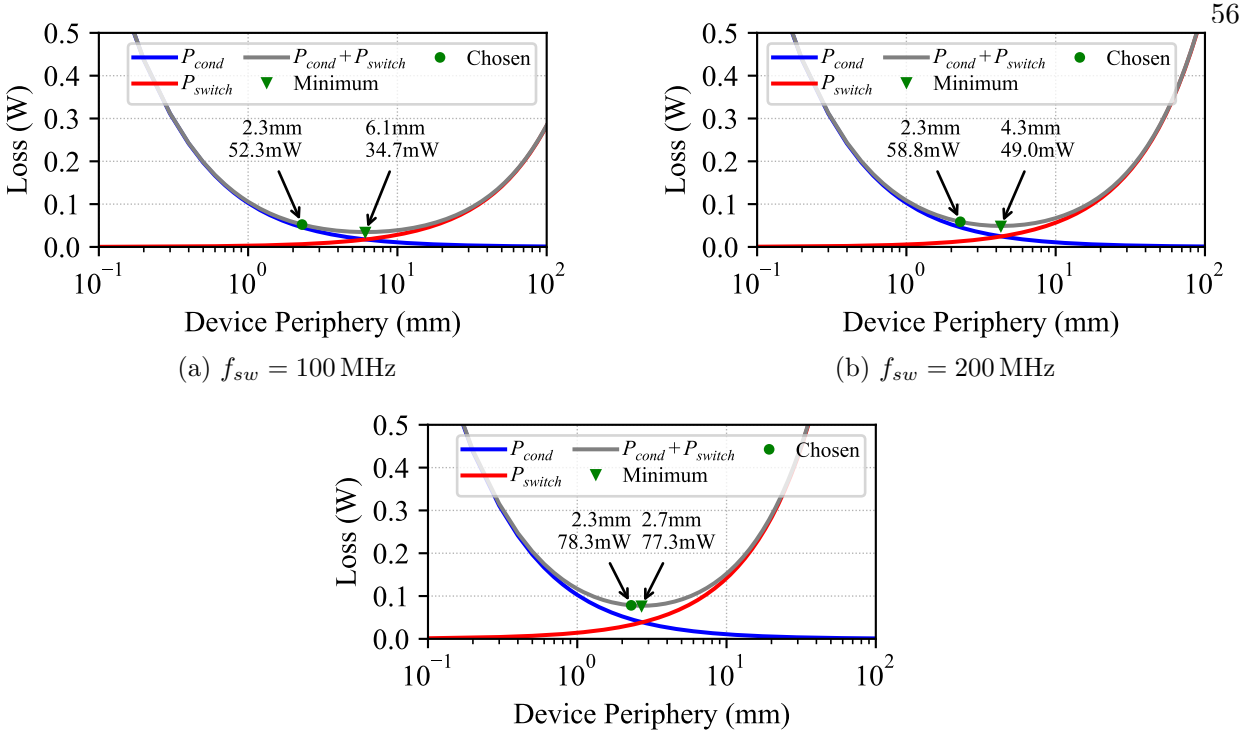
$$I_{ds,on} = \frac{V_{dd}}{R_L} \ ,$$

where R_L is the load resistance. The quiescent load characteristics of a power amplifier are readily determined if the drain voltage, output power, and drain efficiency are known (or can be approximated). The dc load of the PA can be approximated as:

$$R_{dc} = \frac{V_{dd}^2 \eta_d}{P_{out}} \ , \tag{3.4}$$

where η_d is the drain efficiency (2.10), P_{out} is the RF output power, V_{knee} and V_{dd} are the PA knee and drain voltages, respectively.

In this design, an RF switch HEMT is selected instead of a conventional common-source HEMT configuration. This choice is motivated by the interchangeable nature of the drain and source terminals in the switch, which simplifies the layout and improves resilience to gate-source breakdown. The normalized on-resistance, $R'_{ds,on}$, is measured to be $0.84\,\Omega$-mm from the default switch HEMT model by setting V_{gs} to $0\,\mathrm{V}$, applying a small DC current (e.g., $1\,\mathrm{mA}$) between drain and source, and recording the resulting voltage. The normalized output capacitance, C'_{out}, of $0.556\,\mathrm{pF/mm}$ is determined from small-signal, intrinsic model extraction. Fig. 3.4 shows the expected power loss versus gate periphery ($N \times W_g$) for a single power switch, calculated using (3.3) and (3.2). The curves in Fig. 3.4a, Fig. 3.4b, and Fig. 3.4c correspond to switching frequencies



(a) $f_{sw} = 100\,\text{MHz}$ (b) $f_{sw} = 200\,\text{MHz}$

(c) $f_{sw} = 500\,\text{MHz}$

Figure 3.4: Expected conduction and switching power loss of a single level versus the periphery of the power stage. Three switching frequencies are illustrated: (a) 100 MHz, (b) 200 MHz, and (c) 500 MHz. The device periphery is selected to be 2.3 mm, in part to allow for head room for larger tracking bandwidths.

of 100 MHz, 200 MHz, and 500 MHz, respectively. This analysis assumes a PA with $P_{del} = 10\,\text{W}$, $\eta_d = 50\%$, $V_{dd} = 10\,\text{V}$. Furthermore, the output voltage swing, V_{out} observed by the power switch is assumed to be 10 V.

For this design, a power-stage periphery of 2.3 mm is chosen for two reasons. First, it provides sufficient margin for higher switching frequencies (i.e. increased envelope bandwidth). At lower switching frequencies, as shown in Fig. 3.4a, the minimum in total power loss occurs at a gate periphery about 2.5 times larger than the selected value, but with only about 66% of the power consumption. As the switching frequency increases, the optimal device size shifts to the left, as seen in Fig. 3.4b and Fig. 3.4c. Furthermore, the minimum total loss, i.e. value of the saddle point, increases with switching frequency–indicating that a smaller device size is preferred. Sec-

ond, transient parametric simulations in Microwave Office indicate minimal–if any–improvement in modulator efficiency for switch sizes past 2.3 mm. This can be a result of increasing drive power requirements–an effect not modelled in this analysis but discussed in more detail in other works [69, 55]–or it it may be related decreasing accuracy from scaling the foundry-supplied model.

3.3.2 Driver Design

The design presented in this work uses the approach discussed in [57] featuring two different variants of driver stages. Lower levels ($V_{dd1} = 18\,\text{V}$ and $V_{dd,2} = 28\,\text{V}$) use the active-type pull-up driver, while the higher levels ($V_{dd3} = 24.67\,\text{V}$ and $V_{dd,2} = 21.3\,\text{V}$) use the modified-active pull-up configuration. The modified-active pull-up drivers use the output voltage rather than the supply voltage to reduce the voltage drop across Q_{3a} and Q_{4a}. These two driver variants are discussed in greater detail in [55].

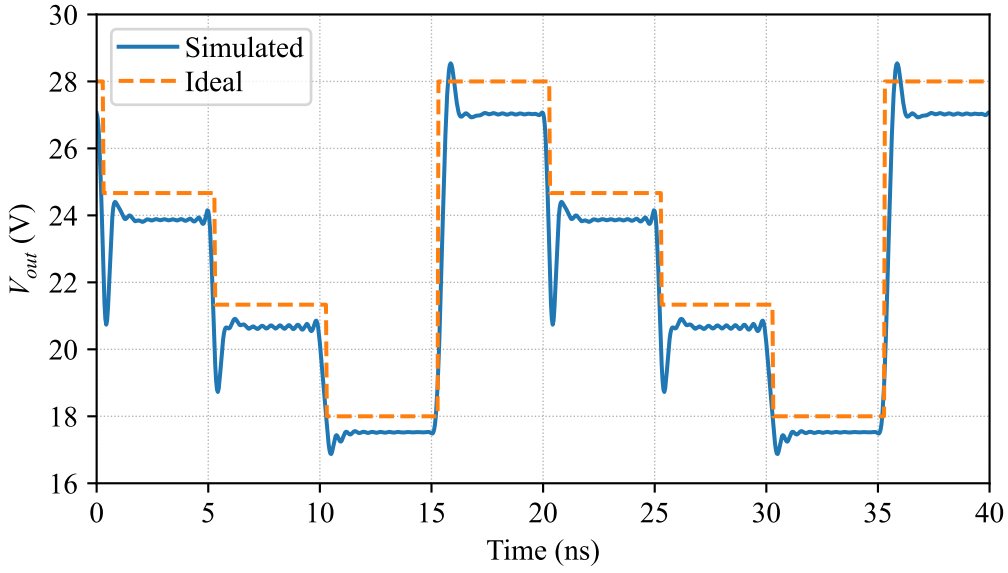


Figure 3.5: Simulated and ideal (i.e. $R_{ds,on} = 0\,\Omega$) output voltage waveform of the supply modulator.

3.3.3 Simulation

Figure 3.5 illustrates the simulated current and voltage waveforms of a 50 MHz stair-step signal for a parallel RC load at the V_{out} node. The resistance of this load is 37.4 Ω which from (3.4)–roughly corresponds to a 28-V, 10-W PA that achieves 50% drain efficiency when in saturation. The parallel capacitance is selected to be 20 pF to approximate the on-chip capacitance of a 10 W X-band PA.

The transient waveforms illustrated in Fig. 3.5 for a 1 MHz reverse stair-step pattern are simulated in the Cadence Applied Wave Research Design Environment (AWRDE) using harmonic balance analysis and nonlinear switch models from the WIN Semiconductors NP15 PDK. In this approach, AWRDE solves the steady state circuit voltages and currents in frequency up to 50 harmonics and then applies the inverse Fourier transform to approximate a steady state time-domain waveform. Time-domain, transient analysis was also attempted, but was found to have extremely poor simulation convergence.

The target levels in the simulated waveform are evenly spaced from 18 V to 28 V the simulated waveform is illustrated in Fig. 3.5 as a blue trace while the desired voltage waveform is illustrated with an orange trace. The voltage drop from the ideal waveform is a consequence of the finite on resistance of each level. Under the loading conditions above, the dc-to-dc conversion efficiency is found to be approximately 90%. This is obtained by dividing the power delivered to the load over a period by the sum total powers delivered to each input of the supply modulator (see Fig. 3.2 and Fig. 3.3).

3.4 Results

3.4.1 Static Load Measurements

Fig. 3.6 illustrates a block diagram of the measurement system used to perform static load testing of this multilevel supply modulator. This setup uses six DC power supplies. Two of these supplies deliver the V_{SS} biases to the driver board which shifts the digital TTL signal from the bit

pattern generator to the voltages necessary for each v_{IN} of the supply modulator. The lower V_{SS} is also passed directly through to the multilevel driver chip. The time domain voltage is measured with a 1 GHz Agilent 3034A digital signal oscilloscope across a known load which is a 37.4Ω resistor.

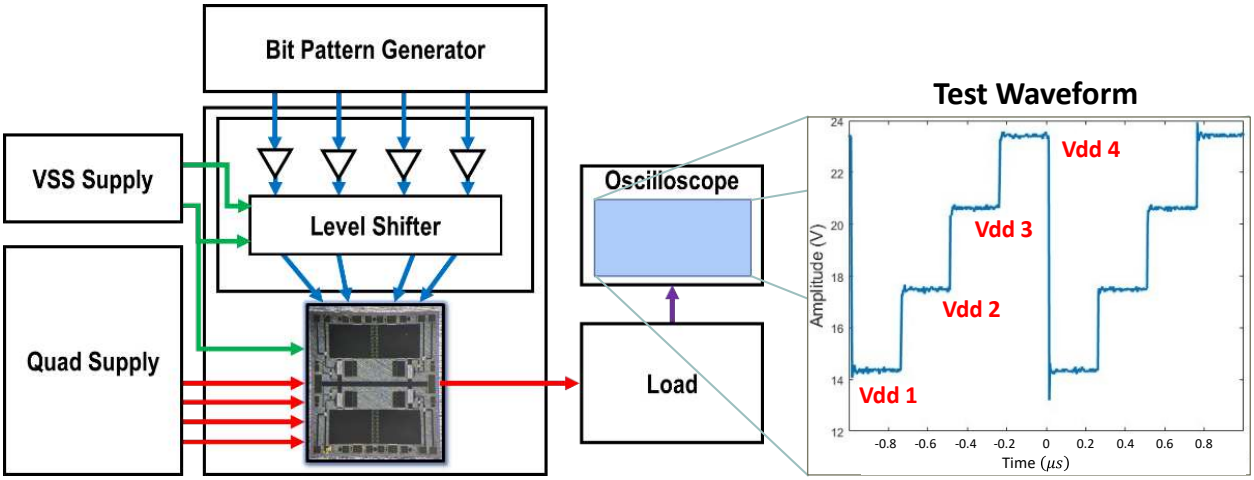


Figure 3.6: Block diagram of the measurement system used to perform measurements of the supply modulator under static loading.

Fig. 3.6 also illustrates the "stair-step" waveform used as a test signal. Static testing of the supply modulator on a 37.4Ω load is performed over three supply modulator voltage ranges while sweeping the frequency of the switched waveform from 1 MHz to 40 MHz.[1] Fig. 3.7 displays the measured and simulated efficiencies of the supply modulator. The simulated and measured efficiencies of the highest level (15-25 V) are nearly within 2pp across the frequency range at the highest level while maximum disagreement in the lower level (8-14 V) is approximately 5pp.

3.4.1.1 Dynamic Load Line Simulations

Supply modulator dynamic testing is conducted using an 35 MHz OFDM waveform with 41 carriers using 64-QAM. Fig. 3.8(a) illustrates the envelope of the waveform (blue) overlaid with the ideal voltage waveform of the supply modulator (orange). The supply modulator operates at four voltage levels 8, 12, 16, and 20 V, respectively. Fig. 3.8(b) illustrates the measured voltage across

[1] The maximum switching frequency were limited to 40 MHz due to driver board and power supplies complications during these measurements. These limitations were later resolved and are not present in the PA dynamic tests of the next Section.

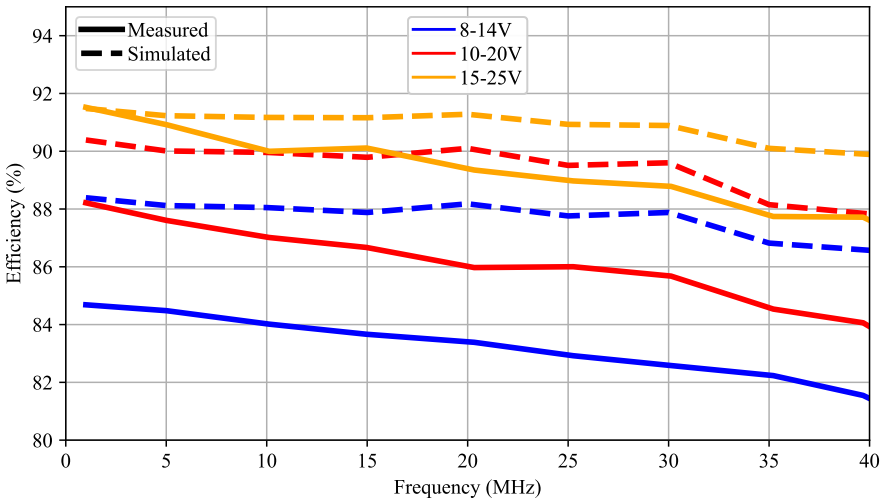


Figure 3.7: Measured and simulated supply modulator efficiency across a static load of 37.4Ω.

the 37.4Ω load with approximately a 1 V drop in output voltage at the highest level–indicating a series resistance of approximately 2Ω.

Next, the PA model from Chapter 2 is used to estimate the efficiency enhancement achieved with the supply modulator with the parameters listed in Table 3.1. The model is represents a class AB PA with a saturated output power of 5 W and a nominal drain voltage of 20 V. The parameters are specifically selected so that the saturated PA presents a 37.4 Ω load to the modulator to align

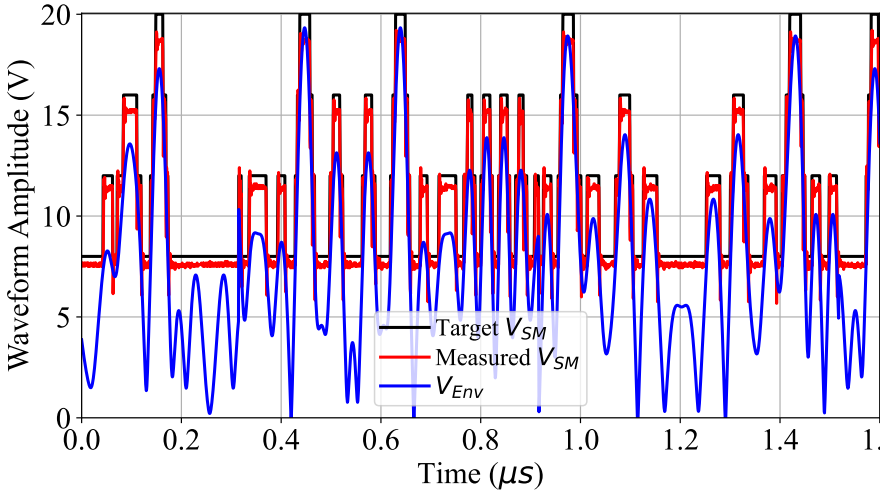


Figure 3.8: Simulated envelope, target discrete levels and measured supply modulator levels used for dynamic load line simulations.

$\eta_{d,max}$	α_{sat}	V_{Knee}	V_{dd}	I_{MAX}	$P_{del,sat}$
50%	275.5°	3 V	20 V	1.15 A	5 W

Table 3.1: Dynamic load line model parameters used to estimate PA efficiency recovery.

with the static load used in measurement.

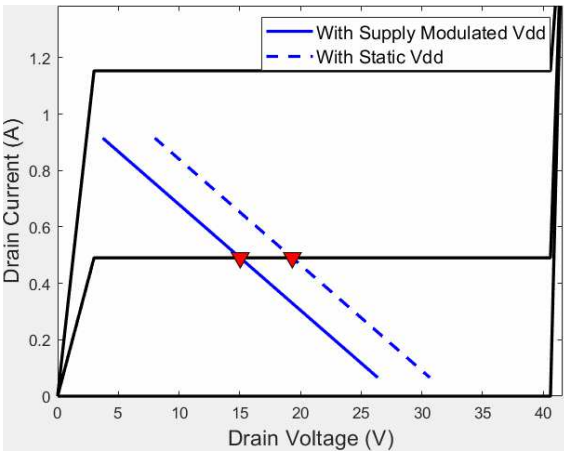
The PA model is designed to recalculate the instantaneous efficiency and load line of the amplifier at a given drain voltage and output power. Two models are instantiated–one where V_{dd} remains static at 20 V and one where V_{dd} is updated to the value measured across the supply modulator load. Fig. 3.9 illustrates a single frame of the load line simulator used to estimate the efficiency enhancement. Fig. 3.8(a) the load line that is dashed belongs to the model with a static V_{dd} and the load line that is solid belongs to the model with a dynamic V_{dd}. Without supply modulation the total drain efficiency of the PA is 17.1 %. and with supply modulation, the PA drain efficiency increases to 28.7 %. The total drain efficiency of the system, i.e. the composite drain efficiency, is found through the following relationship

$$\eta_{d,composite} = \frac{P_{del}}{P_{dc,tot}} = \frac{P_{del}}{P_{pa,dc}} \frac{P_{pa,dc}}{P_{dc,in}} = \eta_d \eta_{sm},$$

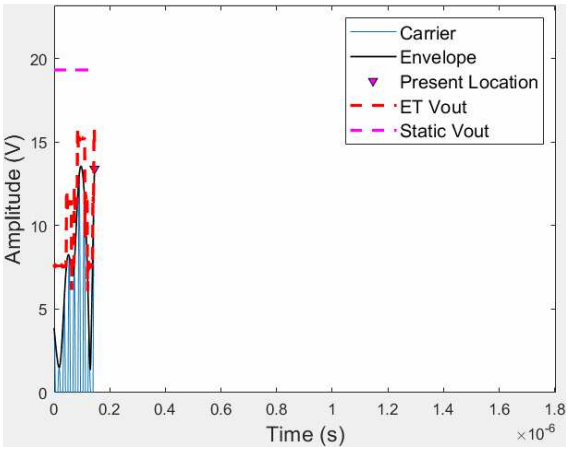
where $P_{pa,dc}$ is the DC power supplied to the PA, $P_{dc,in}$ is the DC power delivered to the supply modulator, η_d is the drain efficiency from Section 2.2, and η_{sm} is the drain efficiency of the supply modulator. The calculated composite drain efficiency of the transmitter is 23.5%.

3.4.2 Envelope Tracking Measurements

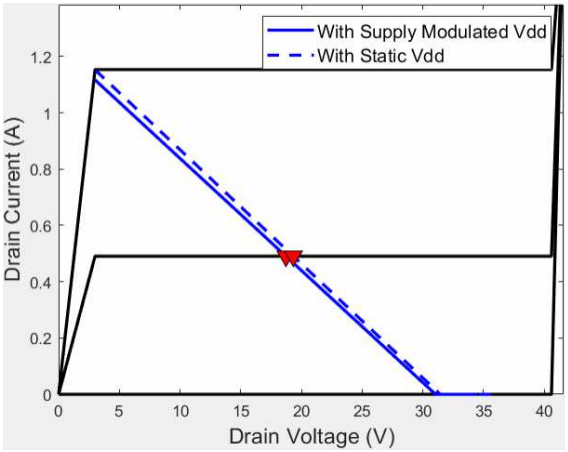
The co-simulation results from the prior subsection provide a first-order analysis of the performance improvements offered by supply modulation. However, there are many dynamic effects not captured by this analysis, and measurement of the supply modulator chip with a physical power amplifier is necessary to accurately assess the chip's capacity for efficiency enhancement. The measurements presented here involve the supply modulation of an C-X band, two-stage PA fabricated in a 28 V GaN-on-SiC process. This device is chosen because it is designed to maintain



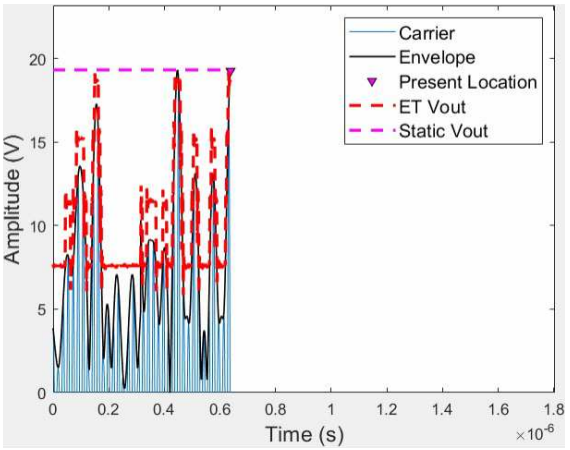
(a)



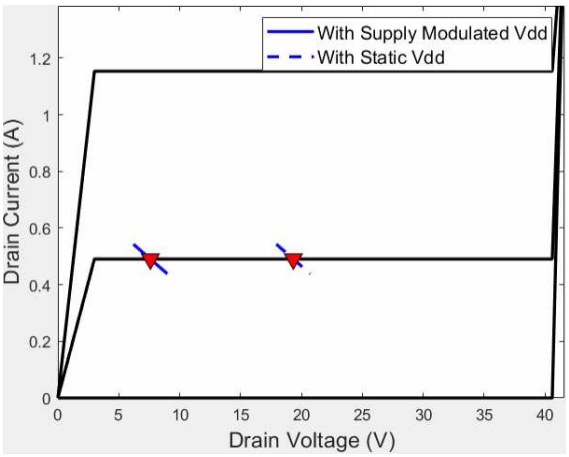
(b)



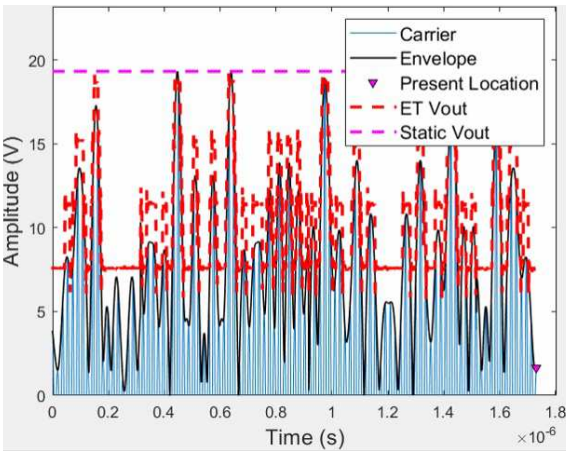
(c)



(d)



(e)



(f)

Figure 3.9: Three frames of the dynamic load line simulation. (a), (c), and (e) illustrate the dynamic load lines at several different output powers while (b), (d), and (f) illustrate the corresponding location in the time-domain waveform.

good linearity when undergoing supply modulation. The details of this design method are discussed in [70].

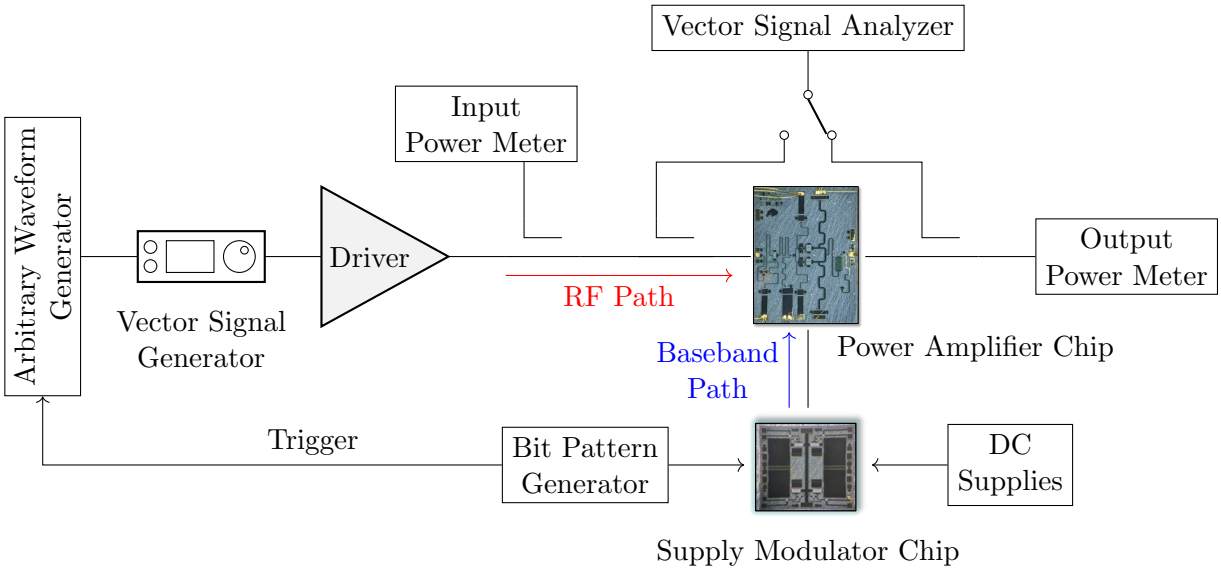


Figure 3.10: Block diagram of the envelope tracking measurement system.

Fig. 3.10 shows a block diagram of the the measurement setup for supply modulation. An arbitrary waveform generator (AWG) provides the signal in-phase and quadrature (IQ) data to a vector signal generator (VSG) which upconverts the signal to the target RF frequency. The signal is then amplified by a driver amplifier before reaching the power amplifier (PA). Directional couplers at the PA input and output allow measurement of average power and spectrum. For supply modulation, the setup includes the supply modulator chip, a four-channel bit-pattern generator (BPG) to control the modulator, and a DC power supply system to bias the circuit. The BPG, AWG, and VSG all operate on a shared a clock and trigger system to maintain alignment and synchronization.

As established in Chapter 2, supply modulation requires good time-alignment between the RF and envelope paths. To achieve this the BPG and AWG must run synchronously with one another. To achieve this, the BPG sends a trigger signal to the AWG to indicate the start of a new waveform period. The process for aligning the RF and envelope signals together is performed in

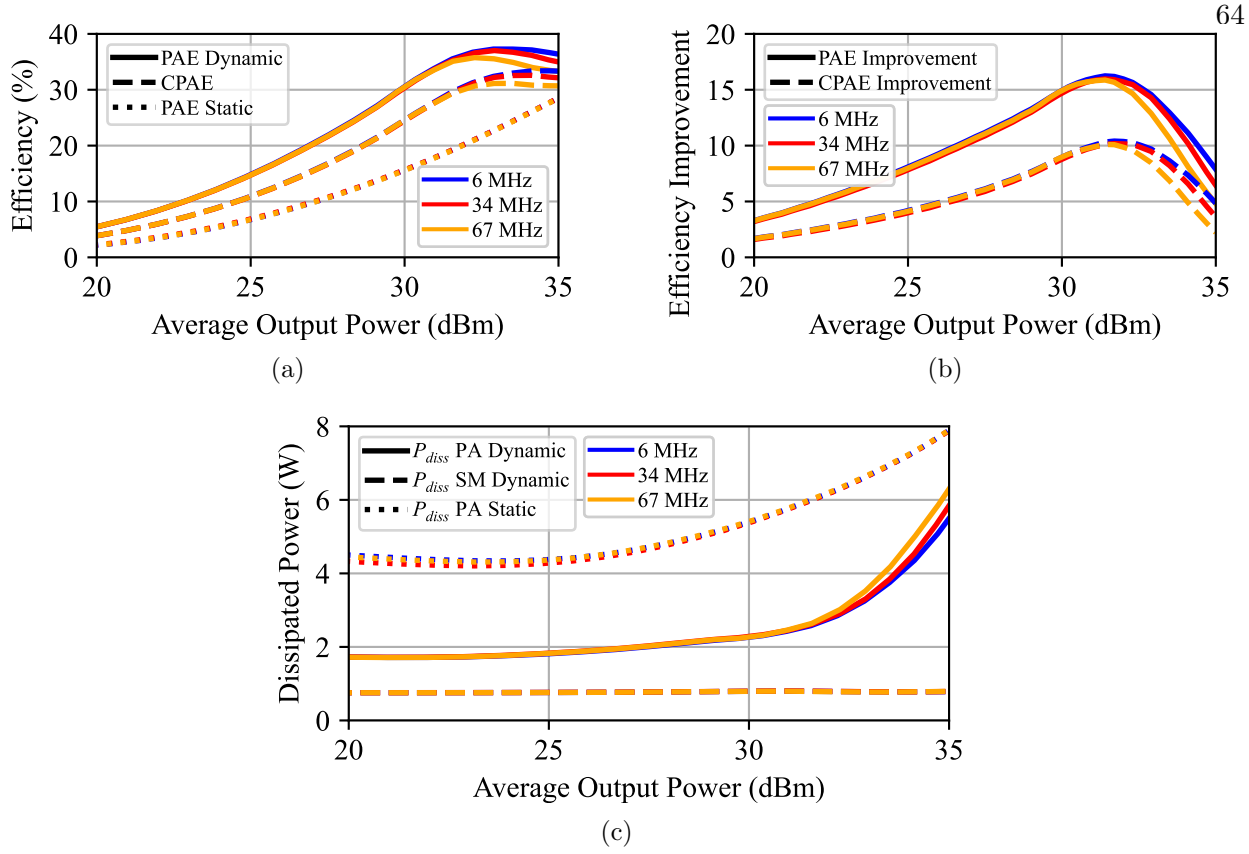


Figure 3.11: Measured efficiency improvement when supply modulating an octave-bandwidth PA. (a) Measured efficiencies with and without supply modulation. (b) The corresponding PA and total efficiency enhancements of the transmitter. (c) The powers dissipated by the PA and supply modulator when undergoing supply modulation and the power dissipated by the PA with a static bias.

two steps. First, the signal is played through the PA **with a static bias**. Then the envelope signal is applied to the PA **when under continuous-wave excitation**. After both measurements, the corresponding envelope of the signal is captured at the same reference plane. Because the envelope of the two waveforms are correlated, a cross-correlation is performed to determine the relative time offsets between the two paths which is then used to shift the RF waveform into alignment.

Figure 3.11 reports the efficiency and dissipated power in both dynamic and static testing using the setup shown in Fig. 3.10. Measurements were performed with 64-QAM signals centered at 6.5 GHz, using three bandwidths: 6 MHz, 34 MHz, and 67 MHz, each with PAPR of 7 dB. The supply modulator trajectory, illustrated in Fig. 3.12, is generated from single-tone, continuous wave

measurement of the PA and is designed to maximize the amplifier PAE.

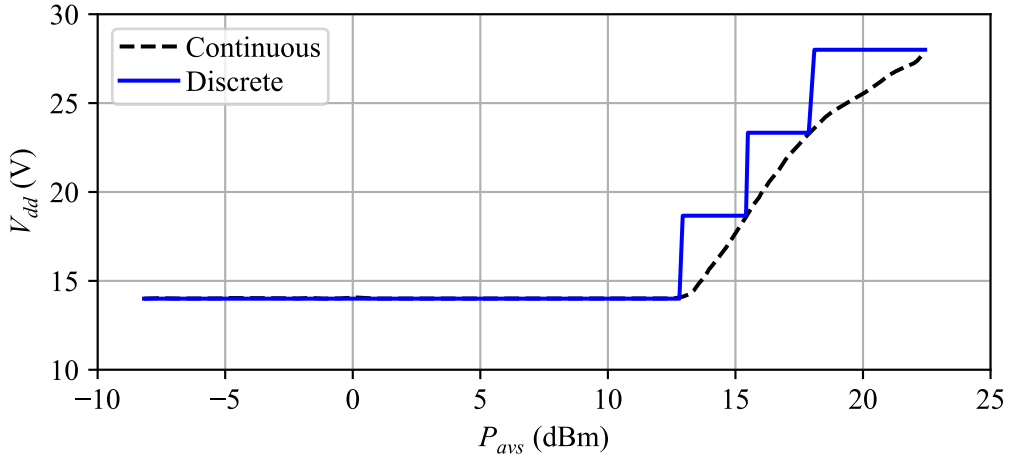


Figure 3.12: Trajectory used for supply modulation. The continuous trajectory (dashed, black) is generated from large-signal, swept, single-tone measurement of the PA and then binned into trajectory used during testing. These trajectories are generated to maximize PA efficiency.

In Fig. 3.11a, the power-added efficiency (PAE) of the octave-bandwidth PA is compared for static supply operation and for envelope tracking (ET) with supply modulation. The composite system efficiency is also shown. Fig. 3.11b presents the improvement in PAE for the PA alone and for the overall transmitter system, relative to the static supply case. The maximum observed improvement in PA PAE is 16 percentage points, while the composite system efficiency increases by up to 10 percentage points. Fig. 3.11c compares the corresponding dissipated powers in the PA with a static supply to the dissipated powers in the PA and supply modulator during dynamic testing. Note that for lower average output powers, the power dissipated by the amplifier is reduced by more than 50%. Furthermore, the power dissipated by the supply modulator remains mostly invariant with respect to PA output power.

For any efficiency recovery/enhancement technique to provide meaningful benefits to the transmitter architectures, its improvement in efficiency should not come at an excess cost in terms of linearity. Fig. 3.13 illustrates the observed error vector magnitude (EVM) of the PA with and without supply modulation. Clearly, as the amplifier goes into saturation, the EVM of the amplifier with supply modulation becomes greater than that of the case with a static supply. This is likely

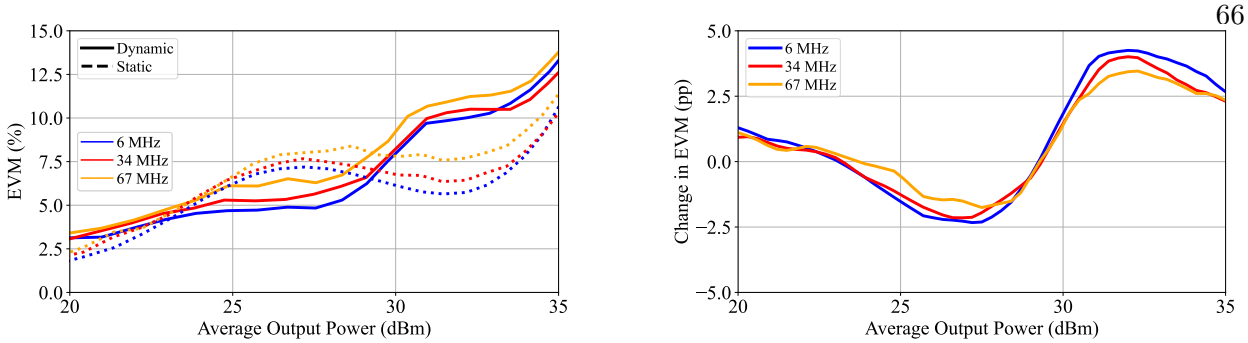
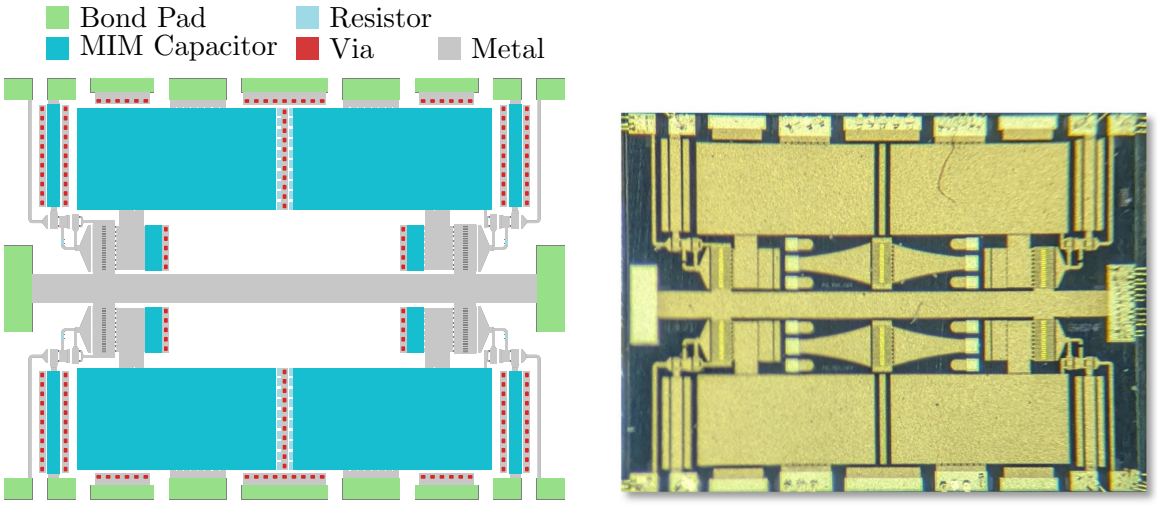


Figure 3.13: Comparison of the measured error vector magnitude (EVM) when the supply is static and when the supply is dynamic.

due to increased sensitivity in the time-alignment between the PA and the supply modulator.

3.4.3 Supply Modulator in Qorvo's 150nm Process

A second four-level supply modulator (Fig. 3.14) is also developed under this work in Qorvo's 150 nm GaN-on-SiC technology. The power switches are sized to provide an on resistance similar to that of the WIN supply modulator. Fig. 3.15 illustrates the PA PAE and composite PAE of the



(a) (b)

Figure 3.14: (a) block diagram and (b) chip image of four-level supply modulator fabricated in Qorvo 150 nm process. The layout of the chip is 3.8 mm by 2.9 mm and the arrangement of the input and output are the same as Fig. 3.3.

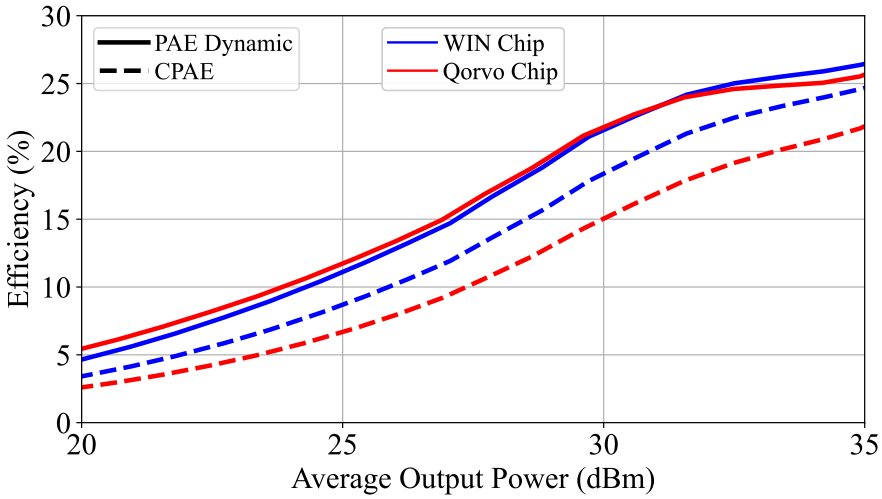


Figure 3.15: Comparison of achieved amplifier and system PAEs when using the Qorvo and WIN supply modulator.

WIN and Qorvo supply modulators together when transmitting the 67 MHz 64-QAM signal with a carrier frequency of 9 GHz. The PAE of of the amplifier in both cases is approximately equal, however; the composite efficiency for the Qorvo supply modulator is approximately 3 percentage points less than that of the WIN supply modulator. The reduction in efficiency is due to a higher driver bias currents.

3.5 Conclusions

PAs operate most efficiently near their saturated output power. Modern signals, however, have high peak-to-average power ratios (PAPR), forcing transmit amplifiers to operate with significant output-power backoff. Supply modulation is an effective strategy to recover amplifier efficiency under these conditions. Table 3.2 compares the observed efficiencies of the amplifier when transmitting a high PAPR signal with other approaches reported in literature.

The transmit architecture studied here uses a discrete multilevel supply modulator: a low-frequency amplifier that sits between the DC supply and the PA drain. This approach trades continuous tracking for high slew rates and can support broadband envelope tracking. The modulator presented was implemented in WIN Semiconductor's 150 nm process and characterized with

Table 3.2: Comparison of efficiencies for different PAs reported in literature.

Ref.	Type	Freq. (GHz)	PAPR (dB)	BW (MHz)	PAE (%)	CPAE (%)
[71]	DPA*	6.4	8.5	10	40	
[72]	DPA	5.8	8.4	10	43†	
[50]	Static	10	7.1	18	43.9	
[73]	Static	19.8	10	50	13.8	
[50]	ET	10	7.1	18	65.4	34.8
[73]	ET	19.8	10	50	13.6	21.4
[74]	ET	1.85	9.0	20	32.2	50.8
This Work	ET	6.5	7	6	37.3	33.4
				34	37	32.6
				67	35.8	31.1

* Doherty power amplifier † Drain Efficiency

static load tests and PA envelope-tracking measurements. Static tests used a "stair-step" waveform with frequency varied from 1 to 40 MHz across three supply-voltage ranges. The modulator attained efficiencies above 80% in all cases; these results contributed to [75]. In envelope-tracking experiments with a 6–12 GHz PA, the system produced an overall efficiency improvement of roughly 10 percentage points; those measurements informed [70].

Supply modulation and transmitter techniques which increase the linearity/efficiency tradespace typically come at the cost of increased design complexity. For example, in supply modulation complexity arises from the additions of the modulator and its supporting control circuitry and from the nonlinear effects imposed on a PA. Intrinsic parasitics (e.g. C_{gs}) depend on device bias, so time-varying supplies change device bias, matching, and gain during transmission. Variations in amplitude and phase introduce distortion that must be compensated. Design approaches addressing these effects are demonstrated in [76, 70], but optimizing networks over wide bandwidths remains difficult to do manually, largely because transistors are bilateral. To help manage growing transmitter-design complexity, the remainder of this thesis focuses on matching-network synthesis, automated design, and emulation.

Chapter 4

Network Synthesis

4.1 Introduction

Advanced architectures–such as supply modulation–are necessary for achieving high-performance transmitters. Naturally, these architectures always come with the cost of higher design complexity. This presents a significant challenge for cost-effective and timely high-frequency circuit design as high-frequency circuits tend to be bilateral, require complex matching and exhibit coupling. These two properties can cause elements of a circuit to interact in ways that are frequently undesirable and require iteration to directly address.

To offset this, one strategy is to liberally introduce isolation throughout a transmitter circuit with components such balanced architectures [15] and isolators. Such approaches make the process of design more tractable, but also tend to introduce additional loss while also increasing circuit size and weight.

Another approach–which this thesis explores–is to formulate better initial solutions to the design problem at hand through network synthesis and automated design. The distinction between these two techniques lies in how the network is found. In automated design, an initial network is estimated and then its components are iteratively revised through a trial-and-error process until the desired network response meets the design criteria. In network synthesis, the network is directly generated from a mathematical representation of a response that meets the design criteria.

To better understand the distinction between design and synthesis consider the simple ladder network illustrated in Fig. 4.1. Suppose a designer wants to find the element values which minimizes

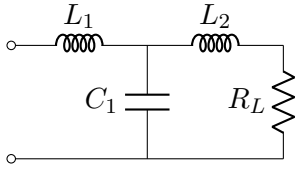


Figure 4.1: A low-pass "T" network

the input reflection coefficient, Γ_{in}, over a given bandwidth from ω_a to ω_b (with ω being the angular frequency). The function of the reflection coefficient in terms of the component values and ω is:

$$\Gamma_{in}(\omega; L_1, C_1, L_2) = \frac{-j\omega^3 L_1 C_1 L_2 - \omega^2 C_1 (Z_L L_1 - Z_0 L_2) + j\omega [(L_1 + L_2) - C_1 Z_0 Z_L] + (Z_L - Z_0)}{-j\omega^3 L_1 C_1 L_2 - \omega^2 C_1 (Z_L L_1 + Z_0 L_2) + j\omega [(L_1 + L_2) + C_1 Z_0 Z_L] + (Z_L - Z_0)} \quad (4.1)$$

Clearly, (4.1) is a rational function with the form:

$$\Gamma_{in}(\omega) = \frac{-j\omega^3 h_3 - \omega^2 h_2 + j\omega h_1 + h_0}{-j\omega^3 g_3 - \omega^2 g_2 + j\omega g_1 + g_0}, \quad (4.2)$$

where h_k and g_k are the k^{th} numerator and denominator polynomial coefficients. Referring to (4.1) the numerator and denominator polynomials of Γ_{in} in terms of the network values are polynomials of degree equal to the order of the network–making the design of high-order networks more prone to getting trapped in local minima rather than the global minima–particularly if the starting point is far from the global minima. On the other hand, the network synthesis approach is to find appropriate representation of the response in terms of the general polynomial coefficients h_k and g_k from (4.2) and then extract the network topology and element values. In this case, the degree of the function in terms of the polynomial coefficients is always equal to one–making it easier to find the global **initial** solution to the design problem.

The purpose of this chapter is to introduce some key concepts in network synthesis through presentation of two techniques: the potential analog method and the simplified real frequency technique (SRFT). The potential analog method is introduced to present a electrostatic-inspired approach to maximally-flat filter design while the SRFT is introduced as a general approach to microwave circuit design. Section 4.2 provides a summary of the relevant background pertaining to

the field of network synthesis. Section 4.3 discusses some classical approaches to the approximation problem. This section also demonstrates the "potential analog" method and how its relationship with electrostatics can be used to approximate the response of a maximally-flat filter. Section 4.4 presents an outline of some canonical network forms, classical approaches to realization problem, practical aspects of computational synthesis and concludes with the expansion of the response from the Section 4.3. Section 4.5 expands on these synthesis concepts with a brief introduction to the simplified real frequency technique with some illustrative examples. Finally, Section 4.6 concludes this chapter with a summary of the topics presented.

4.2 Background

The author would like to first point out some of the references that he has found particularly useful in his studies of the mature field of network synthesis. This by no means is meant to be an exhaustive list but is intended as a starting point for anyone interested in pursuing further study in this field. Below is a list of books:

- *Synthesis of Passive Networks* [77] by Ernst Guillemin presents an exhaustive discussion of network synthesis from the fundamental concepts of network graphs to in-depth presentation of classical realization and approximation methods for both frequency and time domain network synthesis. The only drawback to this work is that it does not directly cover more modern approaches to network analysis and synthesis such as scattering parameters. Regardless of this fact, many of the concepts are still relevant today and can be a starting point for anyone interested in the theory of passive network synthesis.

- *The Mathematics of Circuit Analysis* [78] is another work of Guillemin which is still in print today. Much of the theory of network analysis and synthesis requires background in mathematical topics in linear algebra, complex analysis, and field theory. This text is an excellent engineering resource on this subject matter as it covers the relevant topics in a thorough manner without getting bogged down in mathematical details which are not

particularly relevant to the study of circuit analysis.

- *Theory and Design of Microwave Filters* [79] by Ian Hunter is a concise (∼350 page) and modern resource on filter design. This reference has good examples and a concise presentation. The author would recommend this book to those unfamiliar with the field but looking for somewhere to start.

- *Design of Ultra Wideband Power Transfer Networks* [80] by Binboga Yarman discusses many of the key details regarding the real frequency technique (RFT) and simplified real frequency techniques (SRFT)–which are two important modern approaches to network synthesis.

- *Microwave Amplifier and Active Circuit Design using the Real Frequency Technique* [81] by Pierre Jerry and Jacques Beneat present the application of the RFT methods for broadband, multistage amplifier design.

4.2.1 Theory

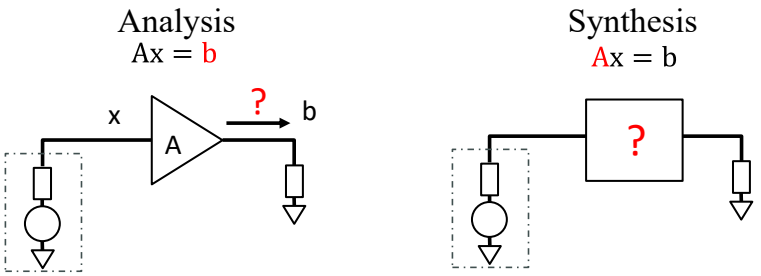


Figure 4.2: Problems of linear, time-invariant (LTI) circuit analysis and synthesis. In analysis, the system (A) is known and used to relate a known excitation to an unknown response (or vice versa). In synthesis, the goal is to find a system (A) which satisfies a given excitation (x) and response (b).

Network synthesis is the inverse problem of network analysis. Referring to Fig. 4.2, a linear network problem consists of three elements: a system (A), an excitation (x), and a response (b). In a network analysis problem,[1] the system is used along with either the excitation or response to

[1] For more details on microwave network analysis the interested reader should refer to Appendix B or to classical texts on the subject.

find the third, unknown term. The conditions by which the existence and uniqueness of a solution to this sort of problem are well-known and readily satisfied for most linear networks.

On the other hand, the network synthesis problem is the case where the excitation and response are known, and the goal is to find the system. If the system is **lossless** then the average power leaving the network should be equal to the total power entering the network. This immediately indicates that–without restraining the relationship between the excitation and response functions–there is no guarantee of a solution to the synthesis problem. Furthermore, the number of unknowns in the system is equal to the number of coefficients in the matrix, i.e. N^2, while the number of known values, i.e. the values in the excitation and response, is $2N$. Therefore the problem is underconstrained at the outset indicating that solutions are not guaranteed to be unique. These two concepts–**existence** and **uniqueness**–are critical to the problem of network synthesis and require additional systematic constraints to solve. These constraints are implemented by relating the general linear algebra problem of Fig. 4.2 to the theory of linear networks.

4.2.1.1 Driving-Point Functions of a One-Port Network

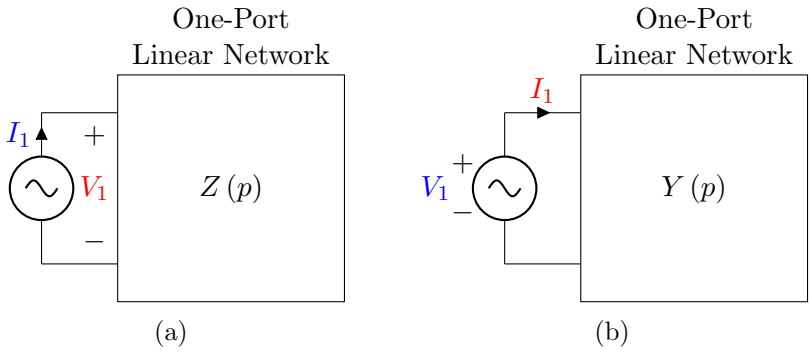


Figure 4.3: Two representations of the driving-point immittance functions of a one-port linear network: (a) represents the driving-point impedance and (b) illustrates the driving-point admittance. The blue label denotes the impressed excitation on the circuit while the red label denotes the response from the network.

Deriving the required systematic constraints begins with a discussion of the one-port network

illustrated in Fig. 4.3 where the port is formed from a two-terminal pair.[2] In this circuit, the impressed current into the port, I_1, is the excitation and the network response is the resulting voltage across the port, V_1.

In such a problem, the system is defined by the ratio of the response to the excitation– generally referred to as a driving-point immittance function, $\mathscr{F}(p)$.[3] The immittance function is used to express a general form of function which may be a driving-point impedance or admittance and is used when a property can equally apply to both. For instance, when the excitation is an impressed current, the immittance function is the driving-point impedance of the network, $Z(p)$. For lumped-element networks this driving-point impedance is expressed with the following rational polynomial:

$$Z(p) = \frac{a(p)}{b(p)} = \frac{a_N p^N + a_{N-1} p^{N-1} + \cdots + a_1 p + a_0}{b_M p^M + b_{M-1} p^{M-1} + \cdots + b_1 p + b_0} = R(p) + jX(p) \tag{4.3}$$

where the real and imaginary components are the driving point resistance ($R(p)$) and reactance ($X(p)$), respectively. Likewise, when the driven excitation is an impressed voltage the immittance function $\mathscr{F}(p)$ is the driving-point admittance, $Y(p)$, of the network. The driving point admittance is the reciprocal of the driving point impedance:

$$\begin{aligned} Y(p) &= \frac{1}{Z(p)}, \\ &= \frac{b_M p^M + b_{M-1} p^{M-1} + \cdots + b_1 p + b_0}{a_N p^N + a_{M-1} p^{M-1} + \cdots + a_1 p + a_0} = G(p) + jB(p), \end{aligned} \tag{4.4}$$

where the real and imaginary components are the driving point conductance ($G(p)$) and susceptance ($B(p)$).

A necessary and sufficient condition for the existence of a passive network as a solution to the synthesis problem[4] is that the real part of the driving point immittance function must be positive across the entire closed[5] right half of the complex plane. This is referred to as the immittance

[2] The author would like to note that terminal is sometimes referred to as a "pole" in classical literature, e.g. [82]; however, this is no longer the convention as a "pole" also refers to a root in the denominator of a rational polynomial.

[3] In this work p is used to represent the complex frequency.

[4] This was a major development in the theory of network synthesis and was proven by Otto Brune in [83]

[5] For those unfamiliar with the terminology "closed" means that the $j\omega$ axis is included in the region while "open" excludes this boundary.

function being positive-real or P.R. An immittance function is guaranteed to be P.R. if [77]:

(1) it has no poles in the open right half-plane;

(2) its real part is nonnegative on the $j\omega$ axis; and

(3) any poles or zeros on the $j\omega$ axis are simple and have positive real residues.

For a solution to exist to the network problem the immittance function **and its reciprocal** must satisfy the P.R. criteria stated above.

Condition (2) for P.R. character requires calculating the real part of a driving point immittance function along the $j\omega$ axis. Therefore a close-form expression of this solution is required. The real part of a complex function, e.g. $\mathscr{F}$, is:

$$\Re\left\{\mathscr{F}(p)\right\} = \frac{1}{2}\left[\mathscr{F}(p) + \mathscr{F}(p)^*\right], \tag{4.5}$$

where the asterisk indicates the complex conjugate. A consequence of meeting the P.R. criteria is that the numerator and denominator polynomials of the driving point immittance function must also be Hurwitz [77]. In addition to being analytic in the RHP, the coefficients of Hurwitz polynomials are always positive and real, and their roots are always symmetric about the real axis of the complex frequency plane [78]. Therefore, (4.5) reduces to the following:

$$\Re\left\{\mathscr{F}(p)\right\} = \frac{1}{2}\left[\mathscr{F}(p) + \mathscr{F}(p^*)\right], \tag{4.6}$$

where the conjugation is now only applied to the complex frequency variable, p.

If $\mathscr{F}$ is a driving point impedance function then the real part of (4.6) along the $j\omega$ axis is [77]:

$$R(j\omega) = \frac{1}{2}\left[Z(j\omega) + Z(-j\omega)\right], \tag{4.7}$$

$$= \frac{1}{2}\frac{A_0 + A_1\omega^2 + \cdots + A_K\omega^{2K}}{B_0 + B_1\omega^2 + \cdots + B_K\omega^{2K}}, \tag{4.8}$$

where K indicates indicates half the maximum order of the numerator or denominator. The minima and maxima of (4.8) are found by evaluating (4.8) at the zeros of its derivative.

In practice, working directly with $Z(p^*)$ tends to make finding (4.8) from (4.6) a tedious process. However, note that along the $j\omega$ axis $\omega^2 = -p^2$ and therefore (4.8) can be re-written in terms of p:

$$R(j\omega) = \frac{1}{2}\left[\frac{A_0 - A_1p^2 + A_2p^4 - A_3p^6 + \cdots + (-1)^K A_K p^{2K}}{B_0 - B_1p^2 + B_2p^4 - B_3p^6 + \cdots + (-1)^K B_K p^{2K}}\right]_{p=j\omega} \tag{4.9}$$

$$= \frac{1}{2}\left[Z(p) + Z(-p)\right]_{p=j\omega} \tag{4.10}$$

where $Z(-p)$ is called the paraconjugate of $Z(p)$. Equation (4.10) is the even part of the driving point impedance function. This result can be contrast with (4.6), by re-generalizing (4.10) as the even part of the driving point immittance:

$$\mathscr{F}_{even}(p) = \frac{1}{2}\left[\mathscr{F}(p) + \mathscr{F}(-p)\right] \tag{4.11}$$

4.2.1.2 Transfer Function of a Two-Port Network

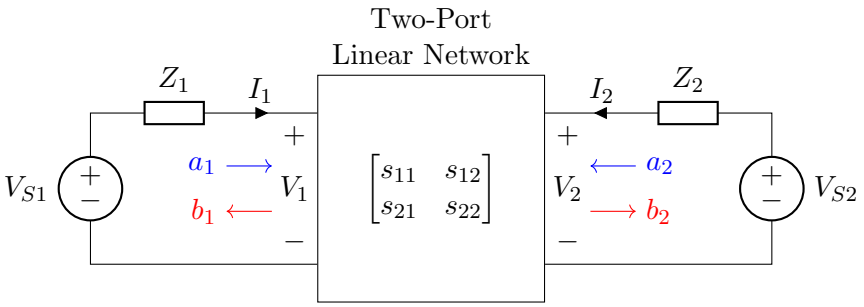


Figure 4.4: A two-port linear network.

Driving-point functions play an important role in establishing the existence of a solution, however; they do little to ensure the uniqueness of that solution. It takes little experience with network design to know that two networks with different structures can present the same driving-point immittance function. Further discussion on equivalent solutions and methods for testing for them may be found in [77]. An additional challenge with the one-port model is that most practical applications of synthesis are more concerned with the transfer function of a signal between a source and a load.

To address this, the one-port model is expanded into the two-port illustrated in Fig. 4.4. In this figure, a generator is placed at each port of the network to demonstrate that an excitation may be applied from either direction. If a load is placed at a particular port, the generator's impressed excitation is simply set to zero, e.g. $V_2 = 0$ if the generator on port two is simply a load.

Many classical texts on network synthesis and analysis are concerned with the general application of network theory and therefore present network theory solely from an immittance perspective. Therefore, the transfer function of a linear network is typically represented as an impedance or admittance matrix, i.e.:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

where z_{jk} and y_{jk} denote the corresponding entries of the impedance and admittance matrices. Determining these matrices directly from measurement is challenging at high-frequencies since the Z matrix requires presenting an open circuit and the Y matrix requires presenting a short circuit. At high frequencies, "open-circuits" have non-negligible capacitance while "short-circuits" have non-negligible inductance. Therefore, this work uses the scattering-wave formalism which is more suitable for high-frequency measurements:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, \tag{4.12}$$

where s_{kl} is a coefficient of the scattering parameter (S-parameter) matrix, a_k is the incident power-wave, and b_k is the reflected power-wave from port k.[6] The power-waves are directly related to the port voltages and currents through [84]:

$$a_k = \frac{V_k + Z_k I_k}{2\sqrt{|\Re\{Z_k\}|}} \quad \text{and} \quad b_k = \frac{V_k - Z_k^* I_k}{2\sqrt{|\Re\{Z_k\}|}},$$

where k denotes the port index and all other values are those corresponding to Fig. 4.4 with the only caveat being that the power-wave reference impedances, Z_k, do not necessarily have to be

[6] For brevity we are skipping the voltage wave definitions v_k^+ and v_k^- and are using the more flexible power-wave definition.

the **physical** port impedances as observed in [84]. For this reason, the reference impedances must be known for the power waves to be meaningful. Appendix B provides more detail regarding this subject.

The S-parameter matrix follows a derivative set of physicality conditions to that of the driving point immittance functions in that s_{kk} must be purely real if p is real and $|s_{kk}| \leq 1$ throughout the open right half plane [80]. If the S-parameters meet this criteria they are said to be bounded-real (B.R.). According to [80] the S-parameters the two-port network are B.R. if they meet the following criteria:

(1) $S(p)$ is real when p is real;

(2) $S(p)$ contains no poles or discontinuities in the closed RHP; and

(3) $S^{\dagger}(p) S(p) \leq I$

where † indicates the conjugate transpose of the system matrix and I indicates the identity matrix.

With a transfer matrix defined, the next step is to express this system in terms of polynomials. In the case of matching networks we are largely concerned with lossless networks as we wish to maximize power delivery to the load. Furthermore, the condition of reciprocity is also imposed to ensure that the elements making the network are also reciprocal, i.e. transformers, capacitors, and inductors. From [85] Belevitch shows that the scattering parameters of such a network can be expressed as:

$$S(p) = \begin{bmatrix} s_{11}(p) & s_{12}(p) \\ s_{21}(p) & s_{22}(p) \end{bmatrix} = \frac{1}{g(p)} \begin{bmatrix} h(p) & f(p) \\ f(p) & -\mu h(-p) \end{bmatrix} \tag{4.13}$$

where μ is adopted from [80, 86] as the "unimodular constant" which is expressed as:

$$\mu = \frac{f(-p)}{f(p)} = \begin{cases} +1 & f \text{ is even} \\ -1 & f \text{ is odd} \end{cases} \tag{4.14}$$

The polynomials h, f, and g have real-valued coefficients and their roots correspond with the zeros of reflection, zeros of transmission, and the poles of all S-parameters, respectively. From the

B.R. criteria stated above g must not contain a pole in the closed RHP. Furthermore, [80] shows that for a reciprocal network f cannot be a full polynomial of real coefficients but must be either even or odd.[7] Furthermore, f will have the form:

$$f = p^{N_{dc}} w(p) \tag{4.15}$$

where N_{dc} denotes the dc transmission zeros and $w(p)$ denotes conjugate pairs of **finite** transmission zeros on the $j\omega$ axis [87]. Finally, there are no specific restrictions placed on h other than the general restriction that the coefficients are real-valued.

It's common in network synthesis to normalize the coefficients of a network such that the reference impedance is 1Ω for its role as the multiplicative identity. This is an approach which is commonly attributed to Sydney Darlington's work on insertion loss theory [82, 77] and helps simplify the intermediate math during the synthesis process. Once the synthesis process is complete, impedance and frequency transforms [88, 79] are used to denormalize the network back to the desired impedance, i.e. 50Ω. Using this simplification, the driving-point immittance function network is related to s_{11} by

$$Z(p) = \frac{1 + s_{11}(p)}{1 - s_{11}(p)} \quad \text{and} \quad Y(p) = \frac{1 - s_{11}(p)}{1 + s_{11}(p)}. \tag{4.16}$$

Using (4.13) the driving point immittance can be expressed in terms of the polynomials $h(p)$ and $g(p)$ as [86, 89]:

$$Z(p) = \frac{g(p) + h(p)}{g(p) - h(p)} \quad \text{and} \quad Y(p) = \frac{g(p) - h(p)}{g(p) + h(p)} \tag{4.17}$$

Furthermore, (4.17) may be used to show that the even part of the driving-point immittance function of a lossless, reciprocal two-port is related , i.e. (4.11), is also related to f as:

$$\begin{aligned} R_{even} &= \frac{f(p) f(-p)}{b(p) b(-p)}, \quad \text{when} \quad \mathscr{F}(p) = Z(p) \\ G_{even} &= \frac{f(p) f(-p)}{a(p) a(-p)}, \quad \text{when} \quad \mathscr{F}(p) = Y(p) \end{aligned} \tag{4.18}$$

where $a(p)$ and $b(p)$ are the numerator and denominator polynomials of (4.3).[8] Using (4.15), (4.18)

[7] This is why (4.14) reduces to a constant value.

[8] Once again, this assumes the network has been terminated in a resistance of 1Ω. If the network is terminated in the resistance, R_t, then (4.18) will be multiplied by R_t^2.

may be re-written in terms of the network's transmission zeros:

$$\mathscr{F}_{even}(p) = \frac{(-1)^{N_{dc}} p^{2N_{dc}} W(p)}{d(p)\, d(-p)} \tag{4.19}$$

where $W(p) = w(p)\, w(-p)$ and $d(p)$ represents the denominator polynomial of the immittance function in accordance with (4.18).

Because (4.13) represents a lossless network, the following relation must be satisfied [90]:

$$|s_{11}(\omega)|^2 + |s_{21}(\omega)|^2 = 1 \tag{4.20}$$

However through an argument similar to the one used to derive (4.11), the S-parameters of (4.20) may be re-written in terms of the polynomials h, f, and g from (4.13) **and their paraconjugates** as:

$$\begin{aligned} g(p)\, g(-p) &= h(p)\, h(-p) + f(p)\, f(-p), \\ G(p) &= H(p) + F(p), \end{aligned} \tag{4.21}$$

where $G(p) = g(p)\, g(-p)$, $F(p) = f(p)\, f(-p)$, and $H(p) = h(p)\, h(-p)$. Equation (4.21) is sometimes referred to as the "Feldtkeller Equation" [89], and was shown by Belevitch to be a necessary condition for lossless, reciprocal, linear two-port networks [85, 91].

4.2.2 Spectral Factorization

Spectral factorization is a process by which a function is factored about the $j\omega$ axis of the complex plane. It is particularly important to network synthesis because it allows a polynomial to be recovered from its even part (4.11) or from a function times its paraconjugate, i.e. as in (4.21).

For example, consider the case where $h(p) = p^3 + 3p^2 + 2p + 1$ and $f(p) = 1$. From (4.21) the function $G(p)$ is:

$$G(p) = -16p^6 - 7p^4 + 2p^2 + 2$$

Fig. 4.5 illustrates the corresponding pole locations of G in the complex frequency plane and how they correspond to the respective functions of $g(p)$ and $g(-p)$. Spectrally factoring the roots of g

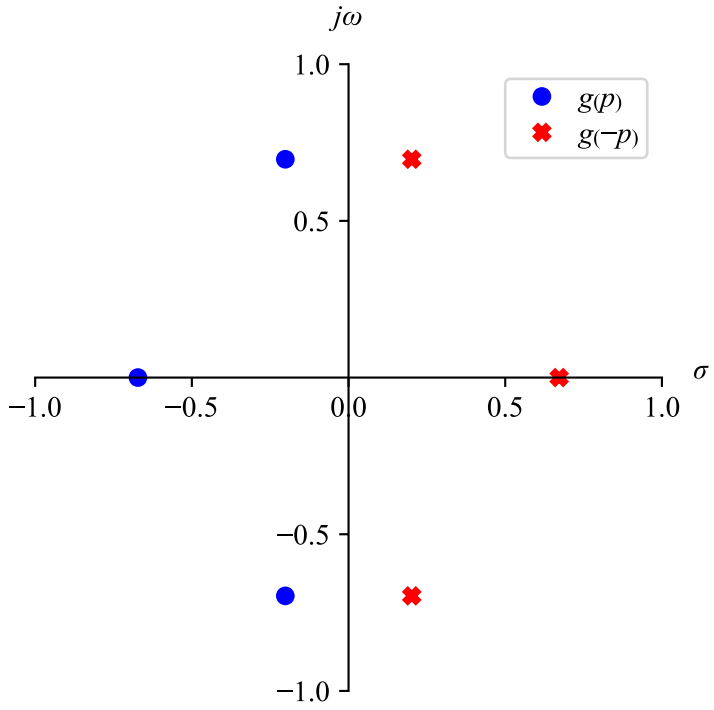


Figure 4.5: Locations of the roots of the function $G(p)$ when $h(p) = 1 + 2p + 3p^2 + 4 + p^3$ and $f(p) = 1$. The roots belonging to $g(p)$ are illustrated as blue circles while the roots belonging to $g(-p)$ are illustrated with red X's.

yields:

$$\begin{aligned} g(p) &= 4\,(p + 0.67212)\,(p + 0.20175 - j0.69665)\,(p + 0.20175 + j0.69665) \\ &= 4p^3 + 4.3p^2 + 3.19p + 1.41 \end{aligned}$$

where the coefficients of g satisfy the positive and real requirements mentioned above. The constant factor 4 in the above equation comes from taking the square root of the absolute value of the highest-order, non-zero coefficient of G, i.e. $\sqrt{|-16|}$.

Spectral factorization is also used to recover a driving point immittance function from its real part along the $j\omega$ axis by spectrally factoring the parametric form of $\mathscr{F}_{even}$. From [92] a driving point immittance function may be represented as the summation of a "Foster Function" $\mathscr{F}_F(p)$ and a minimum function $\mathscr{F}_M(p)$:

$$\mathscr{F}(p) = \mathscr{F}_F(p) + \mathscr{F}_M(p), \tag{4.22}$$

which have the following "parametric" forms found by taking the partial fraction expansion [77, 92, 93]:

$$\mathscr{F}_F(p) = \frac{k_{f,0}}{p} + k_{f,\infty}p + \sum_{n=1}^{N_f}\left[\frac{k_{f,n}p}{p^2+\omega_n^2}\right] \quad \text{and} \quad \mathscr{F}_M(p) = k_{m,0} + \sum_{n=1}^{N_m}\left[\frac{k_{m,n}}{p-p_n}\right] \tag{4.23}$$

where the residues, i.e. $k_{f,n}$, can be directly related to series impedance or parallel shunt admittance elements in accordance with [94]. Because $\mathscr{F}_M$ does not have a zero on the $j\omega$ axis it is defined by the following property [95]:

$$\min\left[\mathscr{F}(p)_M\right]_{p=j\omega} = 0. \tag{4.24}$$

When (4.22) and (4.23) are plugged into (4.11) the terms of $\mathscr{F}_F(p)$ and $\mathscr{F}_F(-p)$ cancel resulting [92, 93]:

$$\begin{aligned}\mathscr{F}_{even}(p) &= k_{m,0} + \sum_{n=1}^{N_f}\frac{k_{m,n}p_n}{p^2-p_n^2}, \\ &= \frac{1}{2}\left[\mathscr{F}_M(p) + \mathscr{F}_M(-p)\right]\end{aligned} \tag{4.25}$$

where the denominator of the in (4.25) is a paraconjugate pair, i.e. $p^2 - p_n^2 = (-p-p_n)(p-p_n)$. Therefore, recovering $\mathscr{F}$ is possible if the function is a minimum function, i.e. $\mathscr{F} = \mathscr{F}_M$. If this is true, the corresponding residues, $k_{m,n}$, and poles p_n of (4.23) are readily identified from (4.25)– which allows $\mathscr{F}$ to be completely recovered from its even part, (4.11). Finally, because $\mathscr{F}_{even}$ is equal to $\Re\{\mathscr{F}\}$ along the $j\omega$ axis **the complete immittance function may also be recovered or generated from its real part along the $j\omega$ axis so long as $\mathscr{F}$ is a minimum-real function.** This observation forms a re-occurring theme in network synthesis and is important part of methods such as the real frequency technique.

4.3 Approximation Problems

Approximation methods are employed to derive a network driving-point and/or transfer function that meets specified design criteria while adhering to the feasibility conditions established in Section 4.2. Common approximation procedures include the real frequency technique [96], simplified real frequency technique [97, 86], the method of semi-infinite slopes [98], Fourier methods [99],

and potential analogs [100, 77]. Additionally, prescribed functions such as Butterworth, Tchebycheff, and Jacobian elliptic polynomials are widely used. This chapter focuses on the potential analog approach for designing maximally-flat filters, and later provides a summary of the simplified real frequency technique (SRFT). For further details on other methods, readers are referred to the reviews by Winkler [101] and Guillemin [77].

The potential analog approach to the approximation problem is based on the property that the real and imaginary components of a complex function satisfy Laplace's equation [77, 78] in any pole-free region. In regions containing poles, the poles act as sources of the scalar field, i.e. the function, while zeros act as sinks for the scalar field. Consequently, concepts from electrostatics can be applied to functions of a complex variable, such as network driving-point or transfer functions [77]. Fig. 4.6 illustrates a high-level block diagram of the process used.

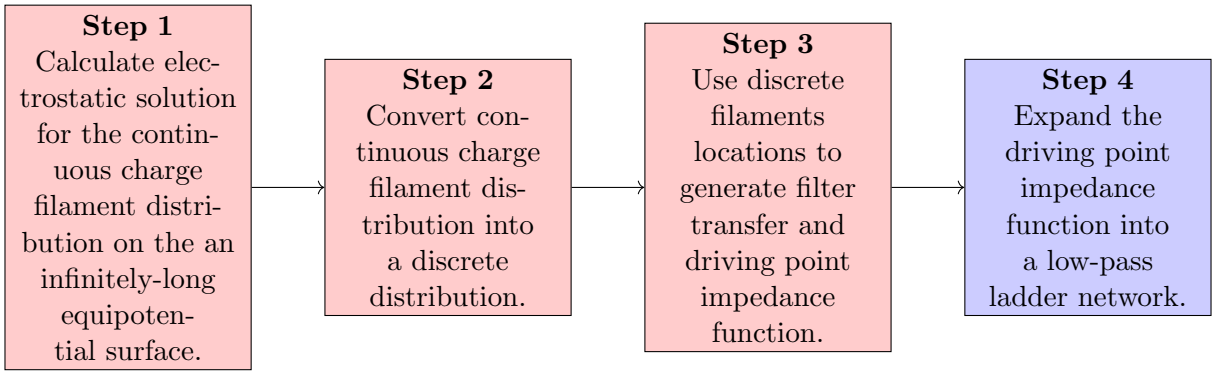


Figure 4.6: Process used to generate a maximally-flat filter using electrostatics and the potential analog. The red and blue fill indicate that the steps belong to an approximation and realization problems, respectively.

4.3.1 The Transfer Function

The initial step in network synthesis is to determine a function representing the network response. In this work, s_{21} as defined in (4.12) is used as the transfer function, although some references (e.g., [77]) use the transfer impedance z_{21}. According to Section 4.2 and Fano [102], the transfer function must satisfy:

(1) s_{21} is a real, rational polynomial of the complex frequency variable $p = \sigma + j\omega$;

(2) $|s_{21}| \leq 1$ in the closed right-half plane.

To satisfy these conditions, s_{21} must be a rational polynomial with all poles in the left half-plane. Consider the function T, representing the squared magnitude of s_{21} for $p = j\omega$:

$$T(p) = |s_{21}(p)|^2 = s_{21}(p)\, s_{21}(p)^* = s_{21}(p)\, s_{21}(-p)|_{p=j\omega} \tag{4.26}$$

Since s_{21} is rational, T is also rational and can be expressed as:

$$\begin{aligned} T(p) &= A\frac{F_N p^N + \cdots + F_2 p^2 + F_1 p + F_0}{G_M p^M + \cdots + G_2 p^2 + G_1 p + G_0}, \\ &= A\frac{\prod_{n=1}^{N}(p - z_n)}{\prod_{m=1}^{M}(p - p_m)}, \end{aligned} \tag{4.27}$$

where F_k and G_k are polynomial coefficients, N and M are the numbers of zeros and poles, and z_n and p_m are their respective locations in the complex plain. Taking the natural logarithm of (4.27) yields:

$$\ln[T(p)] = \ln|A| + \sum_{i=1}^{N} \ln|p - z_i| - \sum_{i=1}^{M} \ln|p - p_i| + j\left(\sum_{i=1}^{N} \arg(p - z_i) - \sum_{i=1}^{M} \arg(p - p_i)\right) \tag{4.28}$$

The real and imaginary parts are:

$$\alpha(p) = \ln|A| + \sum_{i=1}^{N} \ln|p - z_i| - \sum_{i=1}^{M} \ln|p - p_i|, \tag{4.29}$$

$$\Phi(p) = \sum_{i=1}^{N} \arg(p - z_i) - \sum_{i=1}^{M} \arg(p - p_i), \tag{4.30}$$

where α and Φ are analytic and related by the Cauchy-Riemann equations [78]:

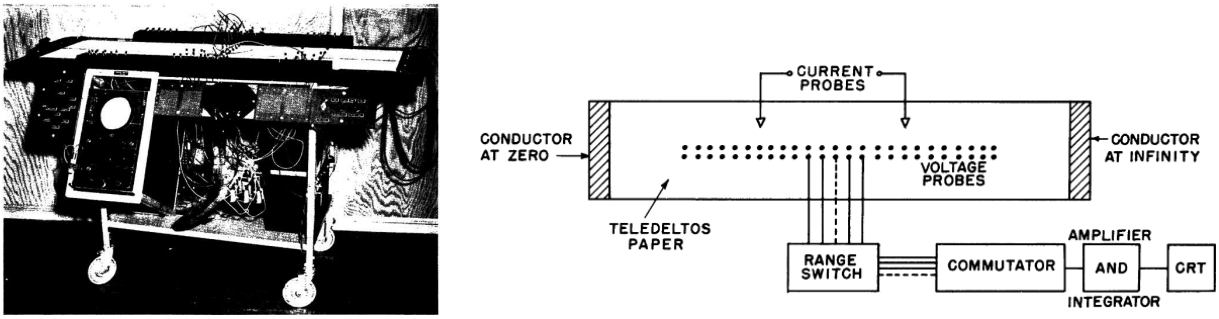
$$\frac{\partial \alpha}{\partial \sigma} = \frac{\partial \Phi}{\partial \omega}, \qquad \frac{\partial \alpha}{\partial \omega} = -\frac{\partial \Phi}{\partial \sigma} \tag{4.31}$$

with σ and ω as the real and imaginary parts of p. The phase function Φ along the frequency axis can be computed from the slope of α:

$$\Phi(\omega) = \int_0^{\omega} \frac{\partial \alpha}{\partial \sigma}\, d\omega \tag{4.32}$$

Several electrostatic problems yield field solutions analogous to the gain function $\alpha(p)$. Two examples are the electric potential from (a) current sources on a resistive plane and (b) infinitely long line charges, known as the "current" and "filament" analogs, respectively.

4.3.1.1 The Current Analog



(a) (b)

Figure 4.7: Analog computer using the current potential analog from [1] (a) photograph of the analog computer and (b) corresponding block diagram.

As described by Guillemin [77], the current potential analog can be traced back to some observations made by Maxwell in [103] and was implemented in analog computers for network synthesis [1, 104]. One such a machine, shown in Fig. 4.7, uses current probes to inject or extract DC current into a conductive sheet (e.g., Teledeltos paper), creating a nonuniform electric potential analogous to the network transfer function. The potential at a point $\vec{r}$ is:

$$V_{total}(\vec{r}) = \sum_{i=1}^{N} \frac{\rho I_i}{2\pi} \ln\left[K - |\vec{r} - \vec{r}_{x_i}|\right] \tag{4.33}$$

where I_i is the current magnitude, ρ the resistivity, K a constant, and $\vec{r}_{x_i}$ the probe location.

Rewriting (4.33) to separate positive and negative sources:

$$V_{total}(\vec{r}) = K + \frac{\rho I}{2\pi}\left[\sum_{i=1}^{N_-} \ln|\vec{r} - \vec{r}_{-i}| - \sum_{i=1}^{N_+} \ln|\vec{r} - \vec{r}_{+i}|\right] \tag{4.34}$$

where N_- and N_+ are the numbers of negative and positive sources, respectively. This form closely matches $\alpha(p)$ in (4.29), allowing the identification:

$$\frac{2\pi}{\rho I} V_{total}(\vec{r}) = \alpha(p) \tag{4.35}$$

with $p = \vec{r}$, $z_i = \vec{r}_{-i}$, $p_i = \vec{r}_{+i}$, $N_z = N_-$, $N_p = N_+$, and $\ln|A| \propto K$.

4.3.1.2 The Electric Filament Analog

Alternatively, the electric filament analog models the sources as infinitely long line charges normal to the x-y plane. The electric field and potential at $\vec{r}$ due to a line charge are [105, p. 44]:

$$\vec{E}(\vec{r}) = \frac{Q'}{2\pi\epsilon_0}\frac{\vec{r}}{|\vec{r}|^2}, \qquad (4.36)$$
$$V(\vec{r}) = \frac{Q'}{2\pi\epsilon_0}\ln\frac{r_0}{|\vec{r}|},$$

where r_0 is a reference distance and Q' is the line charge. For multiple filaments:

$$V_{total}(x,y) = K_2 + \frac{Q'}{2\pi\epsilon_0}\left[\sum_{i=1}^{N_{-Q}}\ln|\vec{r}-\vec{r}_{-i}| - \sum_{i=1}^{N_{+Q}}\ln|\vec{r}-\vec{r}_{+i}|\right]$$

This expression is analogous to (4.34) and thus to (4.29).

4.3.2 The Butterworth Filter

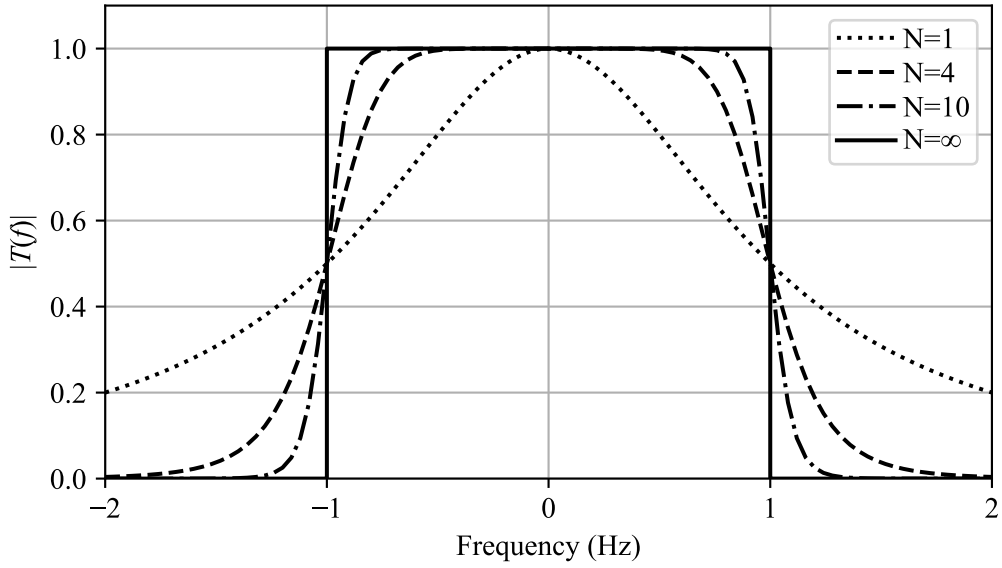
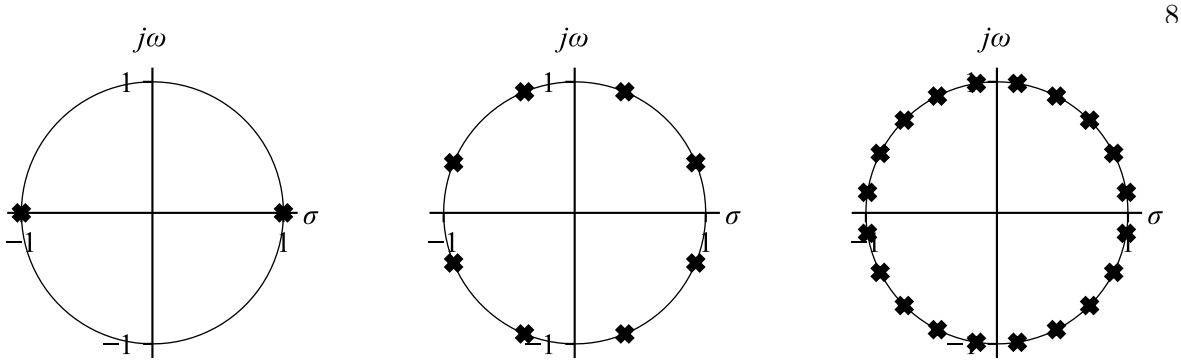


Figure 4.8: Butterworth filter transmission coefficient with a cutoff frequency of 1 Hz.

The Butterworth filter, introduced in 1930 [106], is a canonical filter type where the amplitude response is as flat as possible in the pass band. Maximally-flat filters are necessary in situations, such as signal processing, where uniform filter gain is a requirement. It is constructed to provide a maximally-flat amplitude response in the passband, achieved by ensuring that the first $2N-1$



(a) $N = 1$ (b) $N = 4$ (c) $N = 10$

Figure 4.9: Pole distribution of the Butterworth function on the unit circle.

derivatives of the amplitude response are zero at the center frequency [79]. The Butterworth transfer function is:

$$T(\omega) = \frac{1}{1 + \omega^{2N}} \tag{4.37}$$

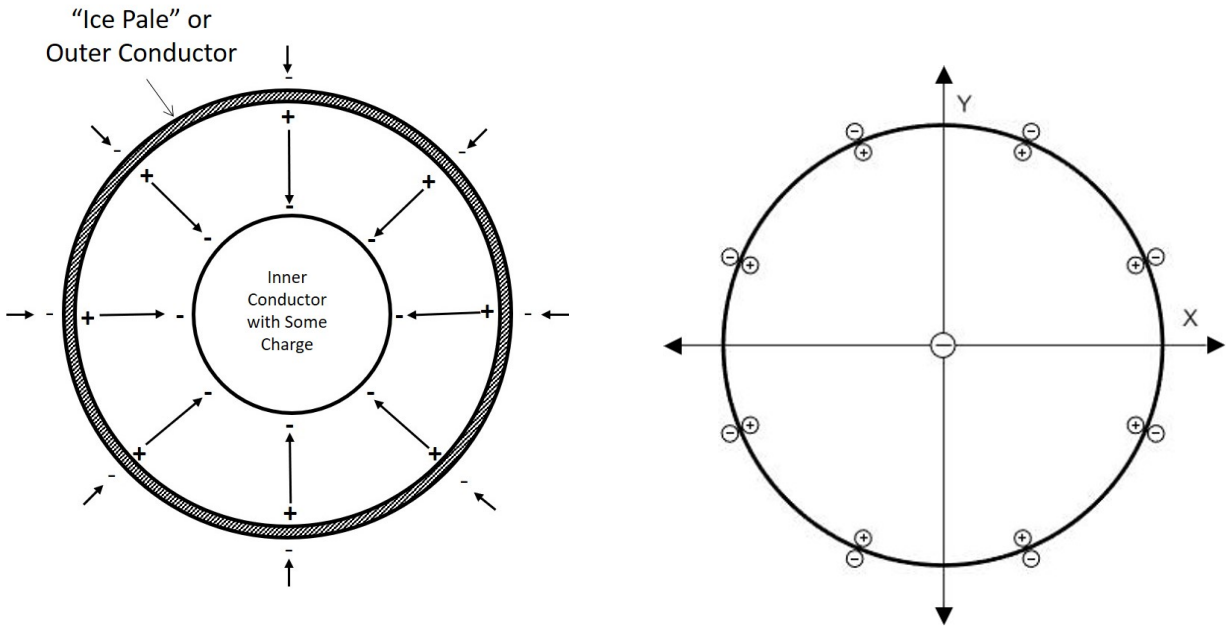
where N is the filter order. Fig. 4.8 shows the amplitude response for several orders with $\omega_c = 1$. As $N \to \infty$, the response approaches an ideal rectangular function.

The pole locations are given by [79]:

$$p_n = -\sin\left(\pi\frac{2n-1}{2N}\right) + j\cos\left(\pi\frac{2n-1}{2N}\right) \tag{4.38}$$

for $n = 1, 2, \ldots, 2N$. Fig. 4.9 illustrates the pole distribution for $N = 1$, $N = 4$, and $N = 10$. The poles lie on the unit circle, with N in each half-plane.

If the complex plane in Fig. 4.9 is viewed as the cross-section of an infinite waveguide, with poles representing line charges, the Butterworth function approaches an equipotential surface as $N \to \infty$. Guillemin [77] compared this to Faraday's "Ice Pale Experiment" [107], illustrated in Fig. 4.10a. When a charge is placed inside a closed conductor the opposite charge is induced on its inner wall such that the electric field inside is cancelled out and electrostatic equilibrium is maintained. Because the system remains in electrostatic equilibrium the potential throughout the interior of the outer conductor is constant.



(a) (b)

Figure 4.10: Faraday's Ice Pale Experiment: (a) inner conductor with negative net charge, outer conductor neutral and (b) discretized outer charge distribution discretized into eight charge filaments.

The electrostatic boundary condition for the normal electric field at the interface is:

$$\vec{n} \cdot (\vec{D}_{outside} - \vec{D}_{inside}) = \zeta \tag{4.39}$$

For a perfect conductor, $\vec{D}_{inside} = 0$, so:

$$\vec{n} \cdot \vec{D}_{outside} = \zeta \tag{4.40}$$

indicating that the external flux density determines the surface charge.

If the surface charge ζ is discretized into N_Q charges (e.g., $N_Q = 8$ in Fig. 4.10b), the resulting field approximates that of the continuous distribution, improving as $N_Q \to \infty$. Mapping the x and y axes to σ and $j\omega$, the negative charge locations correspond to the pole locations in (4.38) for $N = 4$. Thus, $N_Q = 2N$, and as $2N \to \infty$, the gain function $\alpha(p)$ becomes uniform for $|p| \leq 1$, consistent with Fig. 4.8.

While the geometry has been circular, any closed conductor preserves the equipotential prop-

erty. This implies that other shapes can also be used to derive a maximally-flat filter provided the charge distribution is symmetric in all four quadrants of the xy plane.

4.3.3 Maximally-Flat Filter Response from Square Cross-Section

The following procedure synthesizes a passive matching network using the electrostatic solution for a closed conductor with a unit square cross-section:

(1) Use the method of moments (MoM) to approximate the charge distribution around the conductor;

(2) Convert the continuous charge distribution into discrete, equally charged filaments;

(3) Determine the function T corresponding to the filament locations;

(4) Convert T into $\mathscr{F}$ using (4.21) and (4.17); and

(5) Expand $\mathscr{F}$ into an equivalent ladder network.

4.3.3.1 Electrostatic Solution

The electrostatic solution for an infinitely long square waveguide is computed using MoM with point matching. Each edge spans -1 to 1 along the x and y axes, corresponding to σ and ω in the complex frequency plane, targeting a filter prototype with cutoff at $\omega = 1$. Each edge is discretized into 100 segments. For further details on the MoM the interested reader should refer to [108, 109].

Fig. 4.11 shows the MoM solution, with electric field and potential overlaid on the conductor. As required for an PEC, equipotential volume, the potential inside is constant, and the electric field is normal to the exterior edges. Fig. 4.12 illustrates corresponding charge distribution, ζ, about the center of a single edge of the equipotential volume. The distribution is symmetric about the center, and peaks near the boundaries of the square. The piecewise discontinuities in the distribution due to the point-matching MoM formulation.

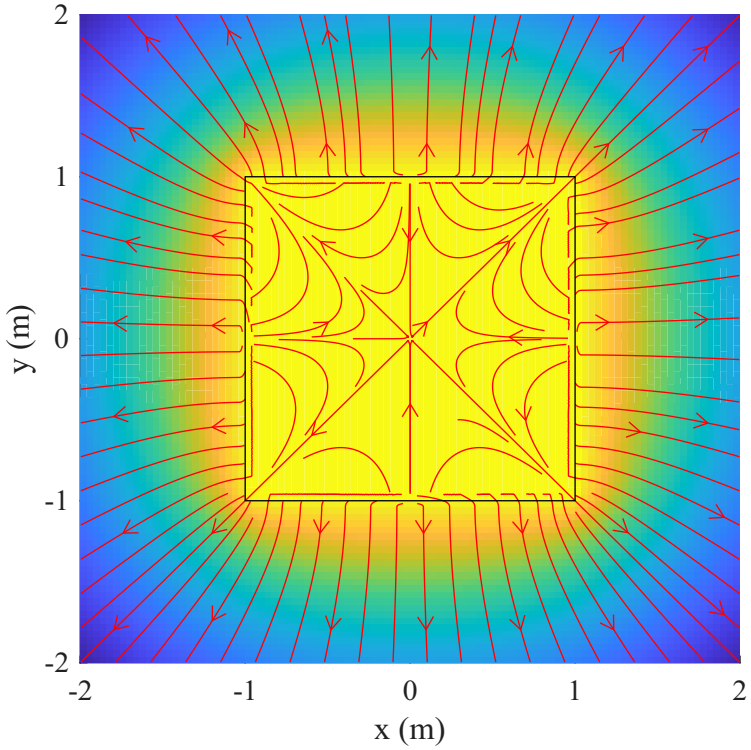


Figure 4.11: MoM solution of a square closed conductor waveguide.

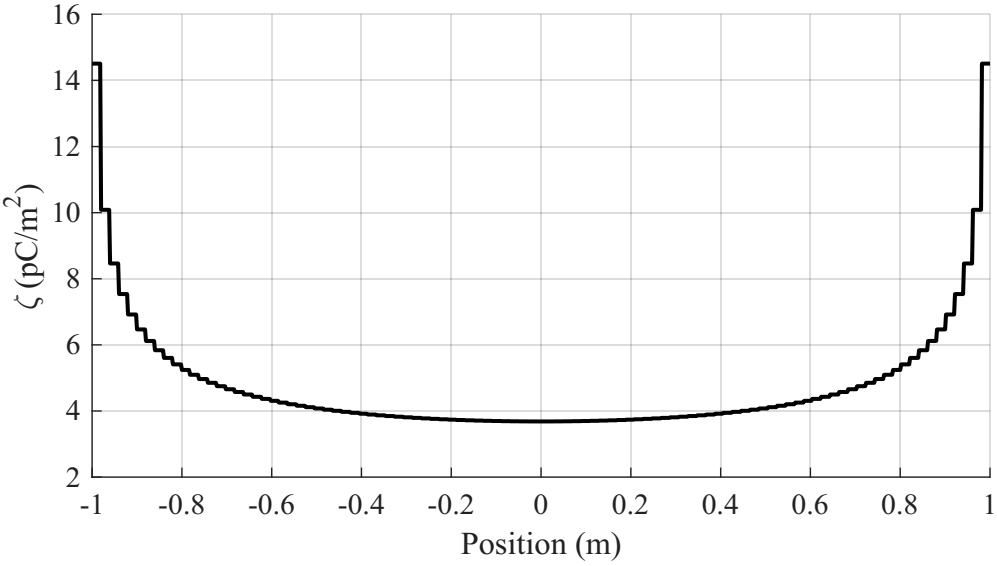


Figure 4.12: Approximated charge distribution ζ along a single edge of the conductor.

4.3.3.2 Discretizing ζ

The charge distribution is approximated by a set number of equally charged filaments placed symmetrically around the boundary, avoiding the y-axis to prevent poles on the imaginary axis. The location of each filament is determined by partitioning each edge into a given number of sub-boundaries containing the charge of one filament, Q'_Δ, and then computing the filament's position within each sub-boundary. The sub-boundaries are determined by integrating the charge distribution until the corresponding filament charge, Q'_Δ, is met:

$$Q'_\Delta = \int_0^{x_1} \zeta(x)dx = \int_{x_1}^{x_2} \zeta(x)dx = \cdots = \int_{x_{N_Q-1}}^{\ell} \zeta(x)dx,$$

where ℓ is the edge length, and $x_1, x_2, \ldots, x_{N_Q-1}$ are the sub-boundary divisions. The filament location within each sub-boundary is computed by taking the weighted mean of each location within the sub-boundary:

$$x_{Qn} = \frac{\int_{x_{n-1}}^{x_n} x\zeta(x)dx}{Q'_\Delta}.$$

Fig. 4.13 shows solutions for several filament counts. As is the case in the Butterworth filter, the approximation of the original, equipotential electrostatic solution, e.g. Fig. 4.11, improves as the filament count increases.

4.3.3.3 Extracting T from Filament Locations

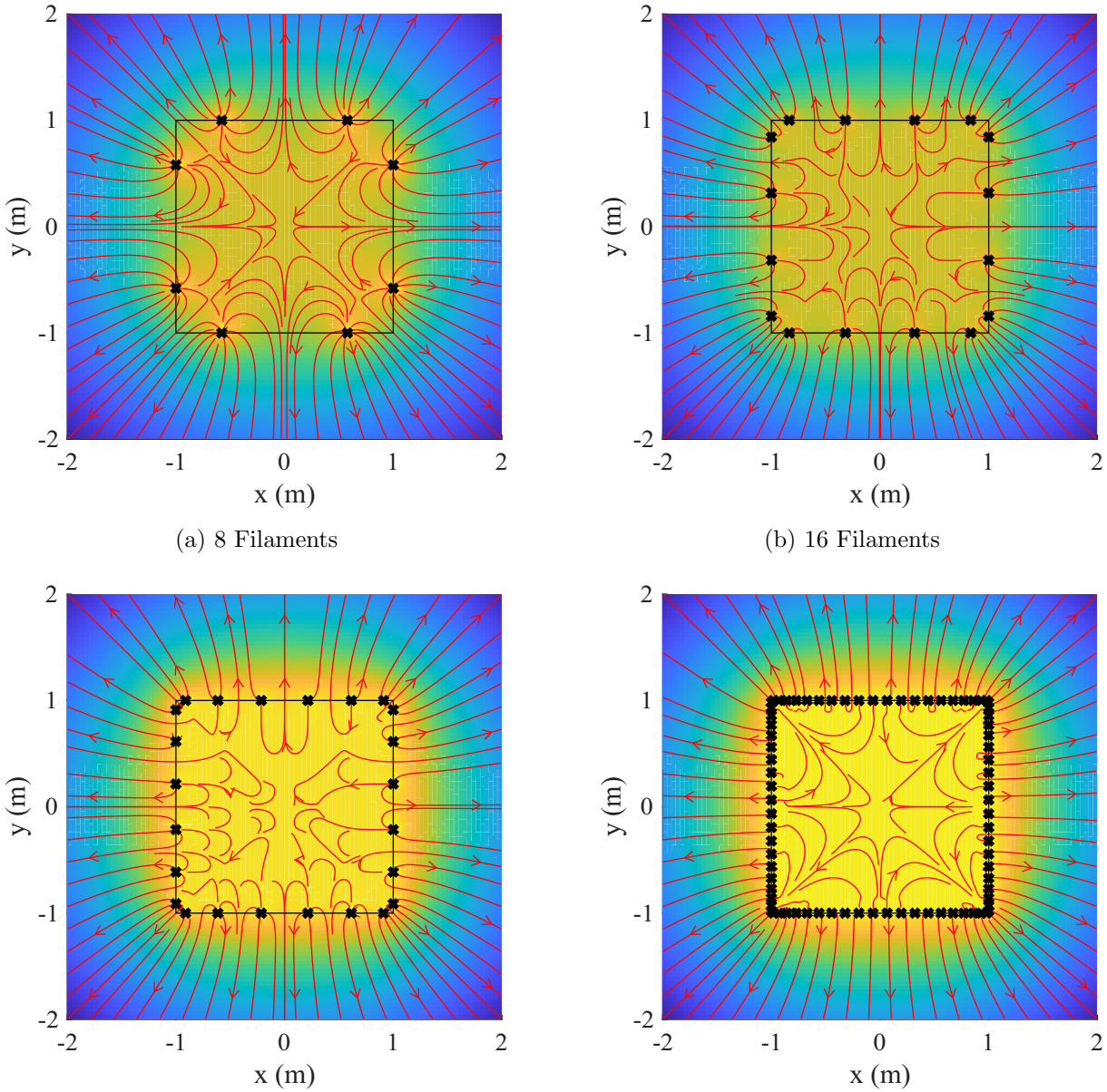
The filament locations determine the denominator polynomial $G(p)$ of T:

$$T(p) = \frac{F_0}{G(p)} \tag{4.41}$$

where F_0 is chosen so that $\max_{p=j\omega} T(p) = 1$:

$$F_0 = \min[G(p)]_{p=j\omega} \tag{4.42}$$

Fig. 4.14 shows $|T(\omega)|$ for several filter orders. The order equals the number of left-half-plane poles, i.e., half the total number of filaments. As with the Butterworth filter, the passband flattens with increasing order.



(a) 8 Filaments

(b) 16 Filaments

(c) 24 Filaments

(d) 80 Filaments

Figure 4.13: Discrete, equally charged filament solutions for various numbers of filaments. The 'x' markers indicate filament locations. The red lines indicate the path of the electric field. The electric field and potential converges to the MoM solution as the number of filaments increases.

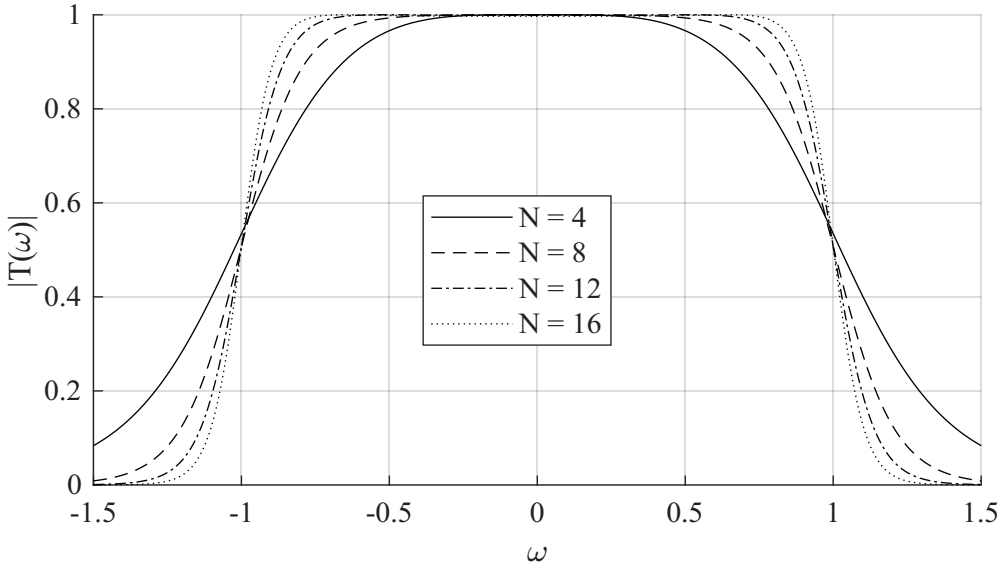


Figure 4.14: Transfer function magnitude response for square cross-section filters of various orders.

4.3.3.4 Computing the Driving-Point Impedance

With G and F determined, the driving-point impedance is computed and expanded into a ladder network. The function $H(p)$ is found from the Feldtkeller equation:

$$H(p) = F(p) - G(p) = F_0 - G(p) \tag{4.43}$$

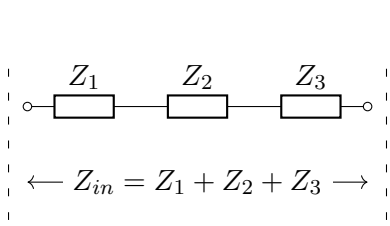
H, F, and G are then spectrally factored into Belevitch polynomials h, f, and g. The driving-point impedance is:

$$Z(p) = \frac{g(p) - h(p)}{g(p) + h(p)} \tag{4.44}$$

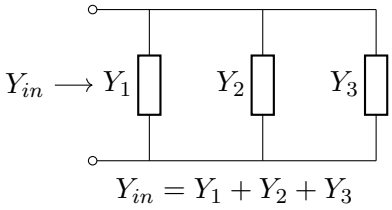
For the $N = 4$ and $N = 8$ filters in Fig. 4.14, the impedance functions are:

$$\begin{aligned} Z(p)\big|_{N=4} &= \frac{1.52p^3 + 3.63p^2 + 4.18p + 1.77}{2.0p^4 + 4.78p^3 + 6.29p^2 + 4.2p + 1.78}, \quad \text{and} \\ Z(p)\big|_{N=8} &= \frac{1.9p^7 + 10.2p^6 + 27.1p^5 + 44.5p^4 + 48.5p^3 + 35.1p^2 + 15.9p + 3.49}{2.0p^8 + 10.7p^7 + 29.6p^6 + 52.0p^5 + 64.4p^4 + 57.7p^3 + 37.3p^2 + 15.9p + 3.49}. \end{aligned} \tag{4.45}$$

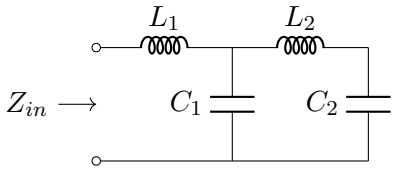
The next section discusses how these driving-point impedance functions are realized as networks and compares their ladder networks with the response of a comparable Butterworth filter.



(a) Foster Type I

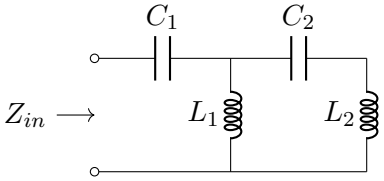


(b) Foster Type II



$$Z_{in}(p) = pL_1 + \cfrac{1}{pC_1 + \cfrac{1}{pL_2 + \cfrac{1}{pC_2}}}$$

(c) Cauer Type I



$$Z_{in}(p) = \frac{1}{pC_1} + \cfrac{1}{\frac{1}{pL_1} + \cfrac{1}{\frac{1}{pC_2} + \cfrac{1}{\frac{1}{pL_2}}}}$$

(d) Cauer Type II

Figure 4.15: Four common canonical network forms [110]. Foster canonical networks are generated from a partial fraction expansion of a driving point immittance and are named after Ronald Foster [94]. Cauer canonical networks are generated from a continued-fraction expansion of a driving-point immittance and refer to Wilhelm Cauer from [111].

4.4 Network Realization

Once a suitable driving-point or transfer function has been obtained, the next step is to convert that function into an equivalent electrical network. This conversion process is generally called network realization. Darlington provides a survey of classical realization methods in [112]. Realization methods are commonly classified by the number of ports, the element types (resistors, inductors, capacitors, etc.), the type of function realized (driving-point immittance versus transfer function), and the canonical form of the resulting network. Because this work concerns the synthesis of lossless, linear two-port networks, the discussion that follows is restricted to two-port realizations composed of inductors and capacitors, and specifically to realizations that begin from the driving-point immittance function in (4.45).

Fig. 4.15 illustrates several canonical forms of network typically encountered in microwave

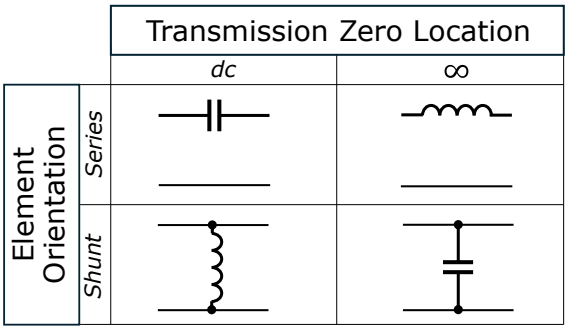


Figure 4.16: Ladder extraction elements and the associated transmission-zero locations in the complex plane. The dc transmission zeros are extracted through the process of reverse division while the transmission zeros at $\omega = \infty$ are extracted with forward division.

circuit design[110, 77]. Foster networks (Fig. 4.15a and 4.15b) are obtained by partial-fraction expansion of $\mathscr{F}(p)$: Foster type I corresponds to a series representation derived from an impedance expansion, while Foster type II is a parallel representation derived from an admittance expansion [94]. Cauer networks (Fig. 4.15c and 4.15d) are obtained from a continued-fraction expansions and produce ladder (cascade) realizations. Cauer Type I yields a low-pass ladder composed of series inductors and shunt capacitors (derived from an impedance continued-fraction), while Cauer Type II yields a high-pass ladder composed of series capacitors and shunt inductors (derived from an admittance continued-fraction) [110].

4.4.1 Ladder Network Synthesis

This work uses ladder (Cauer) networks because of their suitability for planar circuit implementations. The continued-fraction expansion is treated in detail by Matthaei in [95]. Two division strategies are used in the expansion: forward division and reverse division, and Fig. 4.16 illustrates the type of elements each form of division can extract. Forward division removes transmission zeros at $\omega = \infty$ and therefore extracts low-pass elements: applied to an impedance it yields series inductors; applied to an admittance it yields shunt capacitors. Reverse division removes transmission zeros at ω and thus extracts high-pass elements: applied to an impedance it yields series capacitors; applied to an admittance it yields shunt inductors. In summary, forward division produces low-pass

ladder elements, while reverse division produces high-pass ladder elements.

4.4.2 Polynomial Recovery and Numerical Correction

The iterative nature of continued-fraction expansion makes the process sensitive to numerical round-off, which can accumulate and corrupt coefficients of the networks and associated component values [92]. One brute-force mitigation would be to use extended-precision arithmetic, i.e. to increase the numeric precision of the numeric system beyond that of double floating-point arithmetic, but this approach becomes highly inefficient and impractical quickly. Instead, polynomial-recovery methods such as the Parametric Correction Approach (PCA) and the Feldtkeller Correction Approach (FCA) are used; these leverage a knowledge of the network's transmission zeros to recover and correct the driving-point immittance polynomial coefficients after each element is removed.

The PCA was demonstrated for low-pass ladder recovery in [92] and extended to high-pass networks in [87]. The premise of this approach is that the transmission zeros of a two-port network are reflected in the even part of the driving point immittance (4.19). As discussed in Section 4.2 this requires that $\mathscr{F}$ is a minimum function along the $j\omega$ axis (as indicated in (4.24)). Therefore, this approach is not well suited for situations where the network has transmission zeros at dc, ∞, and finite frequencies, as this necessitates the extraction of multiple transmission zeros before the even-part may be computed and the polynomial can be recovered. Once $\mathscr{F}$ is a minimum function, $\mathscr{F}_{even}$ is computed through (4.11), and its numerator is regenerated from a knowledge of the current transmission zeros as indicated in (4.19). Finally, the corrected form of $\mathscr{F}$ is found through spectral factorization of the $\mathscr{F}_{even}$.

The FCA is an alternative approach first demonstrated for low-pass ladder networks in [89]. This approach corrects numeric errors in $\mathscr{F}$ by way of correcting the coefficients of f in the Feldtkeller equation, (4.21). Unlike the PCA, where the function $\mathscr{F}$ must be minimum to be regenerable from $\mathscr{F}_{even}$, the primary requirement for using (4.21) is that the network is lossless and reciprocal. Furthermore, the use of the polynomials h, f, and g makes this approach more compatible with the simplified real frequency technique (SRFT). The polynomial h is recovered

from the driving point immittance from [89]:

$$h = \frac{1}{2}\left[a\left(p\right) - b\left(p\right)\right] \quad \text{where} \quad Z\left(p\right) = \frac{a\left(p\right)}{b\left(p\right)}$$

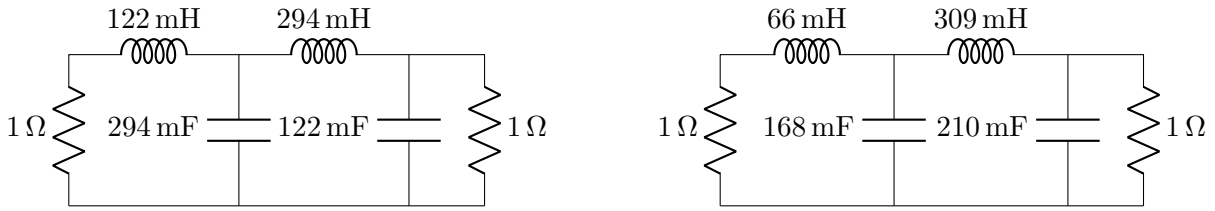
The polynomial f is directly generated from a current knowledge of the present transmission zeros as indicated in (4.15). The corrected form of g is recovered by computing and spectrally factoring G from (4.21). Finally, the corrected form of $\mathscr{F}$ is generated from the corrected h, f and g polynomials using (4.17).

4.4.3 Synthesized Filter Prototypes

Fig. 4.17 compares a 4-pole Butterworth filter, Fig. 4.17a, with a 4-pole filter designed using the potential analog method described in this work, Fig. 4.17. The values of both filters are scaled so that the cutoff frequency for both filters is approximately 1 Hz and are matched to 1Ω. Fig. 4.17c shows $|s_{21}|$ and $|s_{11}|$ for both filters. The Butterworth filter has a superior response in terms of pass-band flatness and in the sharpness in transition between the pass-band and the stop-bands. Group delay is another important filter property particularly for communications system as a non-flat group delay indicates that the filter will distort the signal. Fig. 4.17d illustrates the group delays of the Butterworth and potential analog filters. The Butterworth filter has a peak, in-band deviation of group delay of 0.3 seconds while the filter developed here illustrating a moderately better in-band deviation of 0.223 seconds.

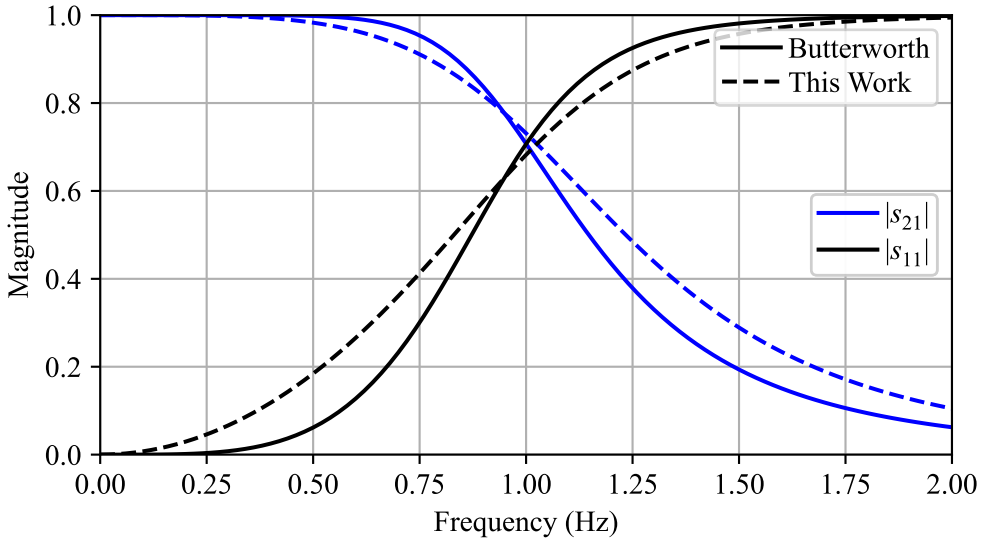
4.5 Real Frequency Techniques

Classical network synthesis methods, particularly those based on current-potential analogs, provide direct and computationally efficient solutions. However, these approaches have notable limitations when applied to practical impedance matching problems. While established techniques exist for single-ended matching (i.e., real-to-complex impedance transformations) [113], they typically rely on simplified load models, such as parallel RC networks. In reality, load impedances often exhibit behaviors that cannot be adequately captured by such elementary representations.

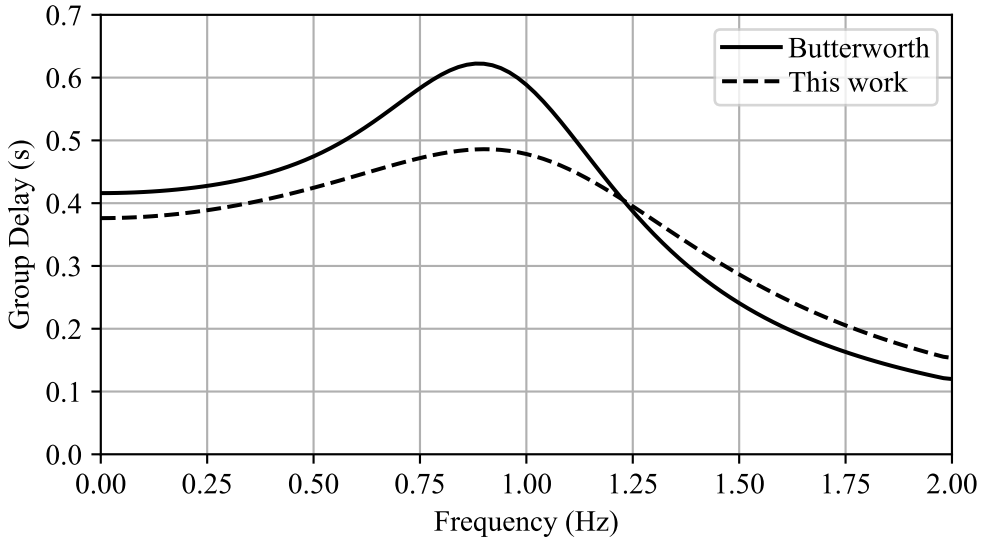


(a) Butterworth

(b) This Work



(c)



(d)

Figure 4.17: Two realizations of a maximally-flat, low-pass filter: (a) a four-pole Butterworth filter and (b) the maximally-flat filter generated from the electrostatic approximation method. (c) illustrates magnitude of the S-parameters for both filters. (d) illustrates the group delay of both filters.

Moreover, double-matching problems—where both source and load present complex impedances—are fundamental in high-frequency circuit design, especially for interstage matching between active devices (e.g., drain-to-gate configurations). Classical methods are generally inadequate for the simultaneous optimization of multiple matching networks within a system, such as input, interstage, and output networks in multi-stage amplifiers. Achieving optimal performance requires accounting for the bilateral characteristics of nonlinear devices.

Real Frequency Techniques (RFTs) address these shortcomings. The original RFT, introduced by Carlin [96], enables single-matching synthesis using direct measurement data, eliminating the need for analytical load models. Subsequent extensions to double-matching problems [114, 115] have broadened its applicability. However, the original RFT formulation lacks a complete network model, making it less suitable for co-design procedures. To overcome this, the present work employs the Simplified Real Frequency Technique (SRFT), which operates on a comprehensive representation of the network response.

The primary advantage of the SRFT is its direct use of the Belevitch polynomials h, f, and g, which, as defined in (4.13), fully characterize the network's S-parameter response. Like the RFT, the SRFT is an iterative synthesis method, where the main task is to optimize the coefficients of h to achieve a network response that meets specified design criteria. This property allows the SRFT to be integrated into existing design tools, significantly expanding the range of addressable design problems. Each synthesized network can be treated as an individual component within a larger circuit, and most design environments offer advanced optimization suites to drive the approximation process.[9] A detailed discussion of the SRFT framework used in this thesis is provided in Chapter 5, focusing on nonuniform transmission line (NTL) automated design. Additionally, Jarry and Beneat present an automated circuit design approach using the SRFT in [81]. The purpose of this section is to outline key principles of the SRFT and present design examples that demonstrate its flexibility.

[9] While the optimization process is compatible between traditional design elements and SRFT networks, the application differs. Optimizing the polynomials of an SRFT network is akin to directly optimizing a function of the network response, whereas optimizing element values is an indirect approach. For further details, see [80].

4.5.1 Approach

In the SRFT, each matching network is modeled as a component, with the primary parameters being the coefficients of the Belevitch polynomials $h(p)$ and $f(p)$. The roots of $h(p)$ correspond to the roots of reflection, while the roots of $f(p)$ correspond to the finite zeros of transmission. Since the locations of the transmission zeros define the network type, f is typically specified at the outset of the synthesis process. For a low-pass network, h and f take the forms:

$$\begin{aligned} h_{\text{low-pass}}(p) &= h_n p^n + \cdots + h_2 p^2 + h_1 p, \\ f_{\text{low-pass}}(p) &= f_0, \end{aligned} \tag{4.46}$$

where h_0 is omitted ($h_0 = 0$) to ensure transformerless synthesis, as the reflection coefficient must approach zero as $\omega \to 0$. For a high-pass network, h and f are given by:

$$\begin{aligned} h_{\text{high-pass}}(p) &= h_{n-1} p^{n-1} + \cdots + h_2 p^2 + h_1 p, \\ f_{\text{high-pass}}(p) &= f_n p^n, \end{aligned} \tag{4.47}$$

where h_n is omitted ($h_n = 0$) to ensure the reflection coefficient vanishes as $\omega \to \infty$. Transformerless band-pass and band-stop networks are typically implemented with filter frequency transforms [79] or by combining high-and-low pass networks in the appropriate cascade or shunt configurations.

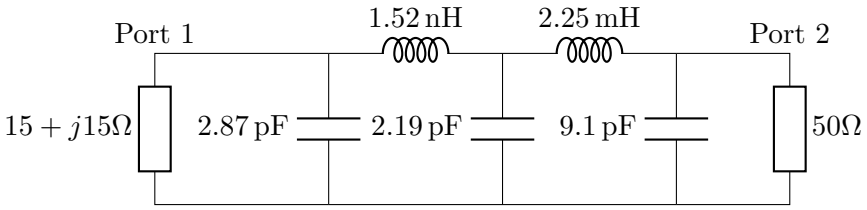
The roots of h and f may reside in either the right or left half-plane. However, since the polynomial g represents the poles of reflection and transmission, it must have roots only in the left half-plane. Consequently, g is not set directly; instead, it is derived by first determining G via the Feldtkeller Equation (4.21), and then extracting g from the left half-plane poles of G through spectral factorization.

4.5.2 Examples

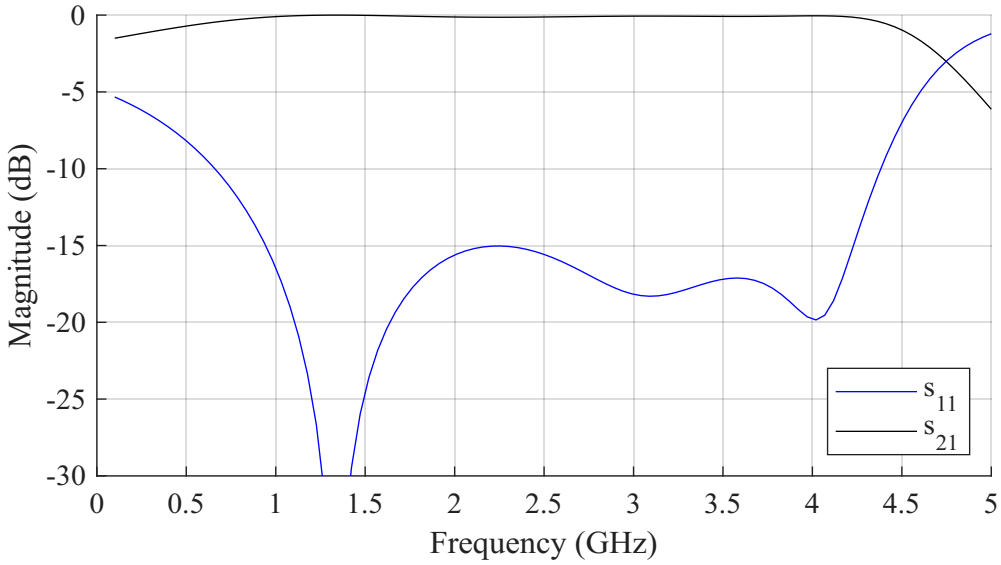
The following examples illustrate the SRFT's versatility across a range of design applications. The first example demonstrates a single low-pass matching network achieving a return loss greater than 15 dB over an octave bandwidth. The second example presents a diplexer network, highlighting the SRFT's capability for co-synthesizing high- and low-pass ladder networks.

All examples were executed in MATLAB R2025a on a MacBook Air running macOS Tahoe with an M4 chip and 24 GB of RAM. The optimizer used is MATLAB's **fmincon**, a constrained nonlinear multivariable optimizer. Reported execution times reflect the total duration from the start of optimization to final network extraction, with graphing and console output disabled to provide consistent benchmarks. No special effort was made to optimize algorithm execution time (e.g., through compiling, vectorization, or parallel processing).

4.5.2.1 Single Matching Network



(a)



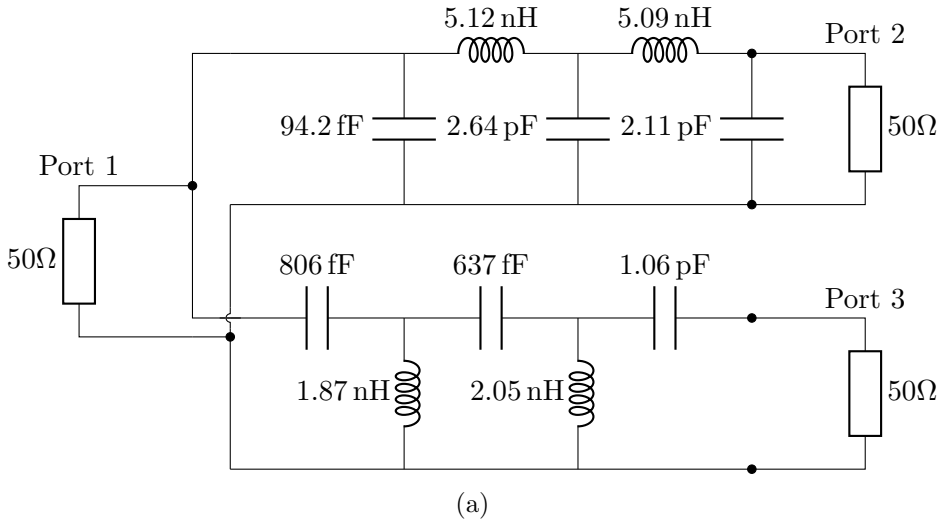
(b)

Figure 4.18: Simple 5-pole low-pass network: (a) circuit diagram and (b) response matching a complex load of $15 + j15\,\Omega$ to $50\,\Omega$. The network is synthesized to achieve a return loss greater than 15 dB from 1 to 4 GHz.

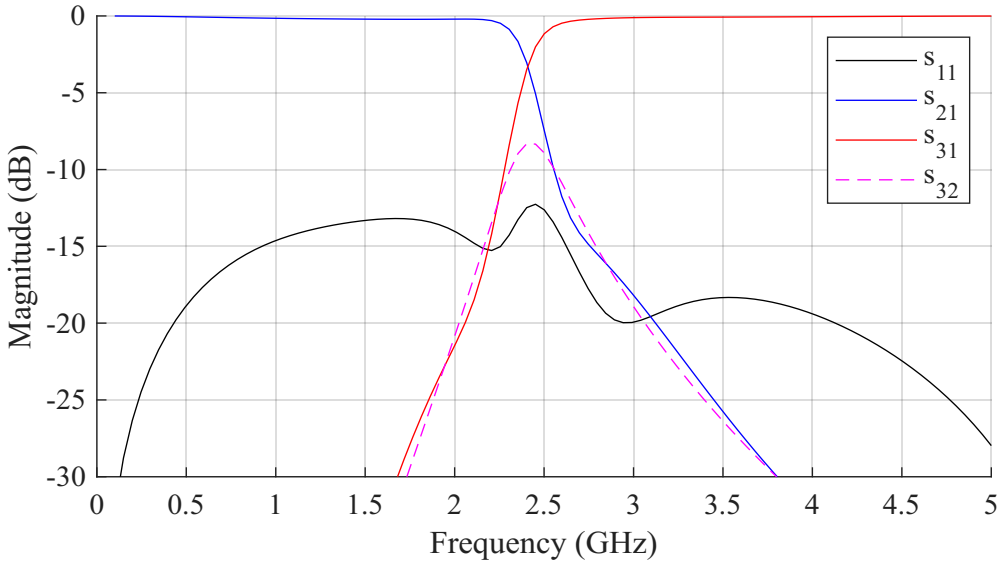
Figure 4.18 shows a 5-pole low-pass ladder network matching a $50\,\Omega$ source to a $15 + j15\,\Omega$

load, with an input return loss exceeding 15 dB over a 120% fractional bandwidth. The network was optimized to meet the return loss specification at five evenly spaced frequencies from 1 to 4 GHz. As shown in Fig. 4.18b, the optimizer converged with a total root-mean-squared (RMS) error of zero, and the total execution time from SRFT optimization to network extraction was 2.1 seconds.

4.5.2.2 Diplexer Networks



(a)



(b)

Figure 4.19: Synthesized diplexer: (a) network diagram and (b) response.

The second example demonstrates the co-synthesis of high- and low-pass networks in a diplexer. Figure 4.19a depicts a diplexer formed from 5-pole high- and low-pass networks. The synthesis objectives are: to minimize the low-pass insertion loss ($|s_{21}|$) at ten evenly spaced points from 0.1 to 2.31 GHz; to minimize the high-pass insertion loss ($|s_{31}|$) at eleven points from 2.55 to 5 GHz; and to achieve isolation between the high- and low-pass paths ($|s_{32}|$) greater than 10 dB across all frequencies. Figure 4.19b presents the final network's scattering parameter magnitudes. The synthesis completed with a final RMS error of 0.2 dB[10] and a total execution time of 8.06 seconds. The minimum isolation between the high- and low-pass paths is 8.3 dB, while the input match from port 1 exceeds 15 dB across the entire frequency range.

4.6 Summary and Conclusions

Network synthesis is the inverse of network analysis, differing from traditional design methods by generating a network directly from a desired response. The synthesis process consists of two main steps: approximation and realization. In the approximation step—using methods such as the potential analog method or the simplified real frequency technique—a network response function (typically a driving-point immittance) is found that meets both the design and feasibility criteria. In the realization step, this response function is then converted into an actual electrical network.

This work presents a novel approach to maximally-flat filter synthesis using the potential analog method. The response of a maximally flat filter is analogous to the potential along the y-axis, and the charge distribution on an equipotential, infinite waveguide surface mirrors that of a high-order maximally-flat filter, such as the Butterworth filter, whose poles are distributed on the unit circle in the complex plane. By exploiting this relationship, a maximally-flat filter is derived with poles distributed around an equipotential square infinite waveguide. The charge-filament distribution is approximated using the method of moments, and the approximate pole locations are determined by the weighted mean of the charge along each edge. These finite filament distributions are then used to construct an equivalent transfer and driving-point impedance function. The

[10] The error is measured in dB, reflecting insertion loss and isolation.

driving-point function is expanded into a four-pole, low-pass ladder network using forward division and the Feldtkeller Polynomial Approach (FCA) to mitigate numerical errors. The resulting filter is compared to a Butterworth filter of the same order. While the Butterworth filter exhibits a superior magnitude response, the derived filter demonstrates better group delay performance. This is likely because the circular waveguide's constant charge distribution is easier to approximate with fewer charges.

Although the potential approximation method is effective for filter design, modern circuit design often requires impedance matching and co-synthesis capabilities. The simplified real frequency technique (SRFT) is compatible with most modern design tools and can accommodate a wide range of design requirements. The SRFT is reviewed in this work, with illustrative examples provided to demonstrate its capabilities.

A key challenge in synthesis is its reliance on the Feldtkeller (lossless) condition. Additionally, because synthesis is based on the network response rather than the physical network itself, it is difficult to ensure that the final components are physically realizable in a given technology. Synthesis techniques also do not typically account for physical design constraints, which is a significant limitation in high-frequency design where layout is critical. To address these limitations, the next chapter expands the SRFT framework to support the automated design of nonuniform transmission lines.

Chapter 5

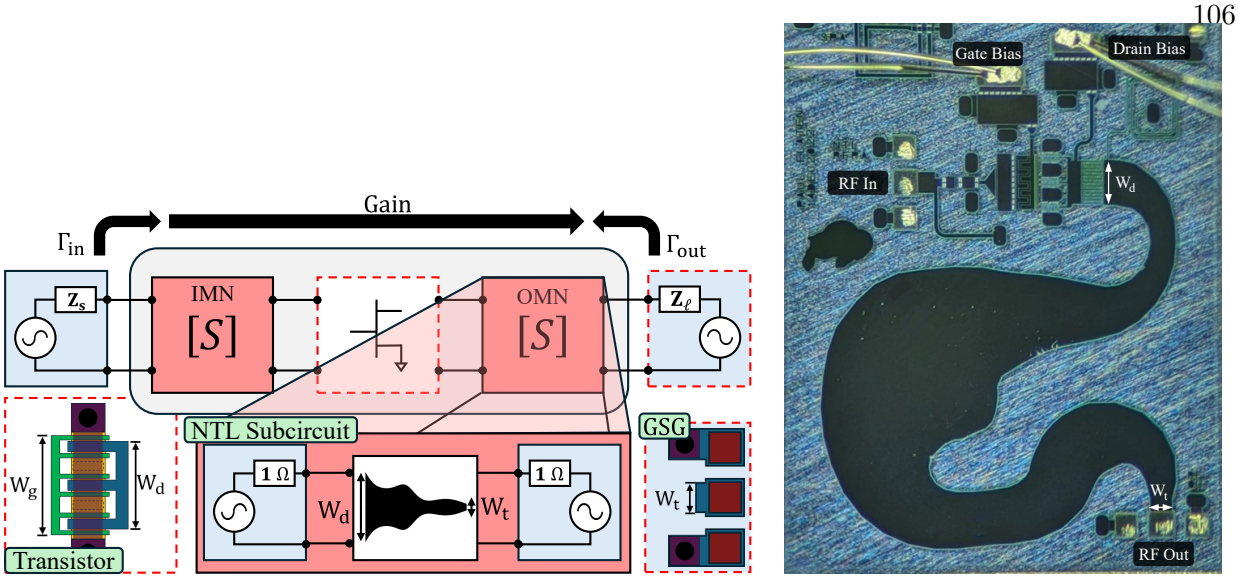
Automated Design of Nonuniform Transmission Lines

5.1 Introduction

The prior chapter discusses the synthesis of networks using predominantly lumped-element components. Lumped element networks are suitable for low-frequency network prototypes but are often not well suited for high-frequency circuit design where such elements become a significant fraction of a wavelength. For this reason the extension of synthesis and automated design to nonuniform transmission line networks is presented in this Chapter. Nonuniform transmission lines (NTLs) are used in a variety of circuits such as multi-band matching networks[116, 117, 118]; pulse/waveform shaping networks[119]; filters [120, 121, 122]; dispersion control networks [123, 124]; and amplifiers [125, 126, 127].

At first glance, these networks might appear interesting and somewhat exotic, but not immediately practical for circuit design as they are physically large and generally only match between real impedances. However, in practice NTLs are often used to provide physical transitions between layout elements of different widths. Fig.5.1a illustrates a microstrip NTL in a MMIC amplifier that provides *both* an electrical match and physical transition, i.e. W_d to W_t, between a transistor drain manifold and output-coupling structure. Fig.5.1b shows the circuit from [127] that uses an NTL output matching network in a GaN MMIC amplifier fabricated in the WIN Semiconductor 150 nm NP15-00 GaN-on-Sic process.

A variety of different NTL design approaches are available. Some close-form equations [128] and direct methods [116] exist, but are limited to applications for real-to-real impedance match-



(a) (b)

Figure 5.1: (a) Block diagram of a monolithic, single-stage amplifier design problem using a NTL output matching network (OMN) and general input matching network (IMN). The method presented in this uses these physical requirements to constrain the solution of the NTL matching network. (b) An example $2 \times 2.3\,\text{mm}$ MMIC single-stage amplifier from [127] with NTL OMN.

ing. General methods for NTL design often require optimizing a model of the electrical response or network. When the optimization is applied to a model of the NTL's response, here we refer to it as *synthesis*, while when it is applied to a model of the network it is referred to as *automated design*. NTL synthesis methods include the simplified real frequency technique (SRFT) [80]; Volterra integral equation methods [129]; and inverse Sturm-Liouville methods [130]. Methods of NTL automated design include sinusoidal modulation [131, 118]; piecewise/discrete modulation [132, 133]; and polynomial modulation [121]. Synthesis techniques can make better-posed[1] optimization problems than automated design techniques. On the other hand, automated design methods are generally more flexible as ensuring physical conformance and accounting for loss is readily incorporated into the design procedure.

Unfortunately, existing NTL design methods are presented as stand-alone applications, and the size and shape of NTLs can make them impractical for many technologies. This chapter presents

[1] That is, the measure of nonlinearity can be lower in synthesis methods than that of automated design methods [134].

a technique that adopts the interface of the simplified real frequency technique (SRFT). The proposed method is not the SRFT, but an automated design method, capable of complex impedance matching, that maintains a compatible interface and solver approach: effectively extending the capabilities of existing tools developed for the SRFT. Several hallmark properties associated with the SRFT, i.e. network co-design and leveraging commercial circuit solvers, are inherited by the proposed technique and are demonstrated with design examples. Furthermore, no methods or mechanisms for computational NTL meandering have been presented to-date. This presents a significant application barrier for integrated and compact hybrid circuit design. To address this, this chapter also introduces and demonstrates a method for computational NTL meandering.

The next section presents the transmission-line model for the design method followed up by a section on the procedure used. Section 5.3 demonstrates several applications to passive networks: a match to a parallel RC load; a band-stop filter; and the use of a loss model to predict performance in a resonator. Sections 5.4 and 5.5 present the co-design capability of this method by demonstrating its use in designing a single-stage and distributed amplifier, respectively.

5.2 Nonuniform Transmission-Line Model

This work introduces an automated design method for NTLs that enforces full-domain constraints, maintains compatibility with the SRFT, supports co-design, and enables computational meandering for compact layouts. The method relies on a model that accurately captures the guided wavelength and characteristic impedance functions of an NTL network. To ensure compatibility with the SRFT, these properties are described in a way that aligns with the SRFT interface — specifically, using the fundamental parameters optimized within the SRFT framework. In this section we present the NTL model in the following order:

- Section 5.2.1 reviews the key features of the SRFT and explains how they are adopted to encode the necessary parameters for the proposed model;
- Section 5.2.2 details the relationship between these parameters and the core properties of

the transmission line model; and

- Section 5.2.3 completes the description of the NTL model by introducing the nonlinear constraint function.

5.2.1 SRFT Lossless Two-Port Network Description

The SRFT method uses a rational polynomial model to represent a lossless two-port network. From [86] this model can be represented with three polynomials **h**, **f**, and **g** [80]:

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \frac{1}{\mathbf{g}(p)} \begin{bmatrix} \mathbf{h}(p) & \mathbf{f}(p) \\ \mathbf{f}(p) & -\mu \mathbf{h}(-p) \end{bmatrix}, \tag{5.1}$$

where **h** is a polynomial whose roots are the zeros of the reflection coefficient, **f** is a polynomial whose roots are the zeros of the transmission coefficient, **g** is a polynomial whose roots are the poles of both the reflection and transmission coefficients, μ is the ratio of **f** to its paraconjugate (i.e. $\mu = f(p)/f(-p)$), and p is the complex frequency variable. If the network is lossless, the following relationship holds:

$$\mathbf{g}(-p)\,\mathbf{g}(p) = \mathbf{h}(p)\,\mathbf{h}(-p) + \mathbf{f}(p)\,\mathbf{f}(-p) \tag{5.2}$$

The goal of SRFT algorithms is to determine the coefficients of the network polynomials in (5.1) such that the corresponding network response meets the desired design goals. The coefficients of **f** can be inferred from the type of network desired (i.e. low-pass, high-pass, band-pass). Conversely, the coefficients of **g** cannot be directly set as its roots must remain in the left half-plane. Therefore, an initial guess for the coefficients of **h** can be made and then optimized. During the process of optimization the each successive guess of **h** can be used with **f** in (5.2) to determine a valid **g**. Once **h**, **f**, and **g** are known, they can be used in (5.1) to determine the network response and an error.

While not an adaptation of the SRFT, the proposed NTL design method adopts the general naming and use of **h**, **f**, and **g**. In this method, **h** is a list of coefficients pertaining to the impedance

of the line that will undergo continuous refinement during optimization. Likewise, **f** will be a scalar variable that relates to the overall length of the designed transmission line. Finally, **g** is an array derived directly from **h** that is used to insure that the designed line remains within pre-specified physical constraints.

5.2.2 Transmission-Line Nonuniform Impedance Model

The generalized time-harmonic telegrapher's equations for any transmission line may be expressed as:

$$\begin{aligned} \frac{\partial I(z,\omega)}{\partial z} &= -Y(z,\omega)\,V(z,\omega) \\ \frac{\partial V(z,\omega)}{\partial z} &= -Z(z,\omega)\,I(z,\omega), \end{aligned} \tag{5.3}$$

where I and V are the currents and voltages at a given angular frequency, ω, and position, z, along the direction of propagation. Y and Z are the shunt admittance and series impedance per unit length, respectively. Solutions to the resulting wave-equation give the complex propagation constant, γ, and the characteristic impedance function, Z_c. These two parameters are related to Y and Z of (5.3) through:

$$\gamma(z,\omega) = \sqrt{Z(z,\omega)\,Y(z,\omega)}, \quad Z_c(z,\omega) = \sqrt{\frac{Z(z,\omega)}{Y(z,\omega)}}$$

$$Y(z,\omega) = \frac{\gamma(z,\omega)}{Z_c(z,\omega)}, \quad Z(z,\omega) = \gamma(z,\omega)\,Z_c(z,\omega)$$

Therefore, only one set of parameters, (γ, Z_c) or (Z,Y), needs to be known to have a complete model for a transmission line.

Practical considerations for transmission line length and width make the, the propagation constant, γ, and characteristic impedance, Z_c, more relevant for network design. For most planar transmission lines, the characteristic impedance is closely related to physical width. Likewise, noting that $\gamma = \alpha + j\beta$, the electrical length, θ, is related to the physical length, ℓ, through the expression $\theta = \beta\ell$. Furthermore, for lossless and non-dispersive transmission lines, the electrical length is related to frequency through:

$$\theta = 2\pi\frac{f}{f_c}, \tag{5.4}$$

where f_c is the frequency where the line is one guided wavelength long.

For lossless transmission lines, the electrical position at z and f is found by integrating $\beta\ell$:

$$\theta(z) = \int_0^z |\beta(\ell, \omega)| \, \mathrm{d}\ell \tag{5.5}$$

Dividing the electrical position, (5.5), by the total electrical length of the line, (5.4), results in the normalized electrical position variable, x, [129, 130]:

$$x(z) = \frac{f_c}{2\pi f} \int_0^z |\beta(\ell, \omega)| \, \mathrm{d}\ell \tag{5.6}$$

where x is only defined on the interval $[0, 1]$ as in [135]. x is a unitless, fractional value of the transmission line's guided wavelength. Once the line has been designed, z is recovered by integrating:

$$z = \frac{2\pi f}{f_c} \int_0^x |\beta(s, \omega)|^{-1} \, \mathrm{d}s \tag{5.7}$$

where β is a function of x, and angular frequency, ω.

(5.6) is not strictly valid for transmission lines with loss. However, the propagation constant for low-loss transmission lines is approximately the same as in the lossless case where, from [12], $RG \ll \omega^2 LC$ with $Z = R + j\omega L$ and $Y = G + j\omega C$. Therefore, the relations above may be used with minor accuracy penalties when the losses are small.

The use of normalized electrical position provides a mechanism for indirect constraint and control of the NTL's physical length through the variable $\mathbf{f}$ defined as:

$$\mathbf{f} = \frac{f_c}{f_n}, \tag{5.8}$$

where f_n is a normalization frequency constant. For most planar circuits, the approximate relation between $\mathbf{f}$ and the physical length, ℓ, is:

$$\ell \approx \frac{|v_p|}{\mathbf{f} f_n},$$

where v_p is the phase velocity of the medium and technology. Appropriate bounds on the value of $\mathbf{f}$ can be estimated from the minimum, ℓ_{min}, and maximum, ℓ_{max}, permissible line lengths for the intended application:

$$\mathbf{f_{min}} = \frac{|v_p|}{\ell_{max} f_n} \leq \mathbf{f} \leq \frac{|v_p|}{\ell_{min} f_n} = \mathbf{f_{max}}.$$

The normalized position variable, x, allows for a rather simple characteristic impedance model. The first two terms of the model form a linear impedance taper:

$$Z_c(x) = (h_2 - h_1)\, x + h_1 \tag{5.9}$$

with $h_1 = Z_c(x = 0)$ and $h_2 = Z_c(x = 1)$.

The linear impedance taper defined in (5.9) allows the designer to specify, constrain, and update the terminal impedances of the line as necessary for the problem at hand. To maintain this property while allowing for more complex intervening functions of characteristic impedance, the following sinusoidal basis functions are introduced:

$$h_3 \sin(x\pi), h_4 \sin(x2\pi), \cdots, h_{N+2} \sin(xN\pi) \tag{5.10}$$

Together (5.9) with (5.10) makes the following impedance function of the line:

$$Z_c(x) = [(h_2 - h_1)\, x + h_1] + \sum_{k=1}^{N} h_{k+2} \sin(k\pi x) \tag{5.11}$$

Therefore, the characteristic impedance profile in (5.11) is completely defined by the vector:

$$\mathbf{h} = [h_1, h_2, h_3, \cdots, h_{N+2}]$$

Fig. 5.2 visually summarizes how the hybrid bases are used. Fig. 5.2a illustrates an example stepped-impedance function and a $Z_c(x)$ from (5.11) made to approximate the example. Fig. 5.2b shows the linear (5.9) and the half-range sinusoidal bases (5.10) used to form $Z_c(x)$ in Fig. 5.2a.

5.2.3 Nonlinear Constraints Function

While it is a straight-forward process to set bounds on the values of $\mathbf{h}$, it is not as trivial to ensure that the characteristic impedances of (5.11) remain constrained over all values of x. One approach is to check at multiple points along the line when a new $\mathbf{h}$ is introduced; however this scales poorly as $\mathbf{h}$ becomes larger and may not capture large spikes in impedance. A more certain method of achieving this goal is to check Z_c at the stationary points of the harmonic function in

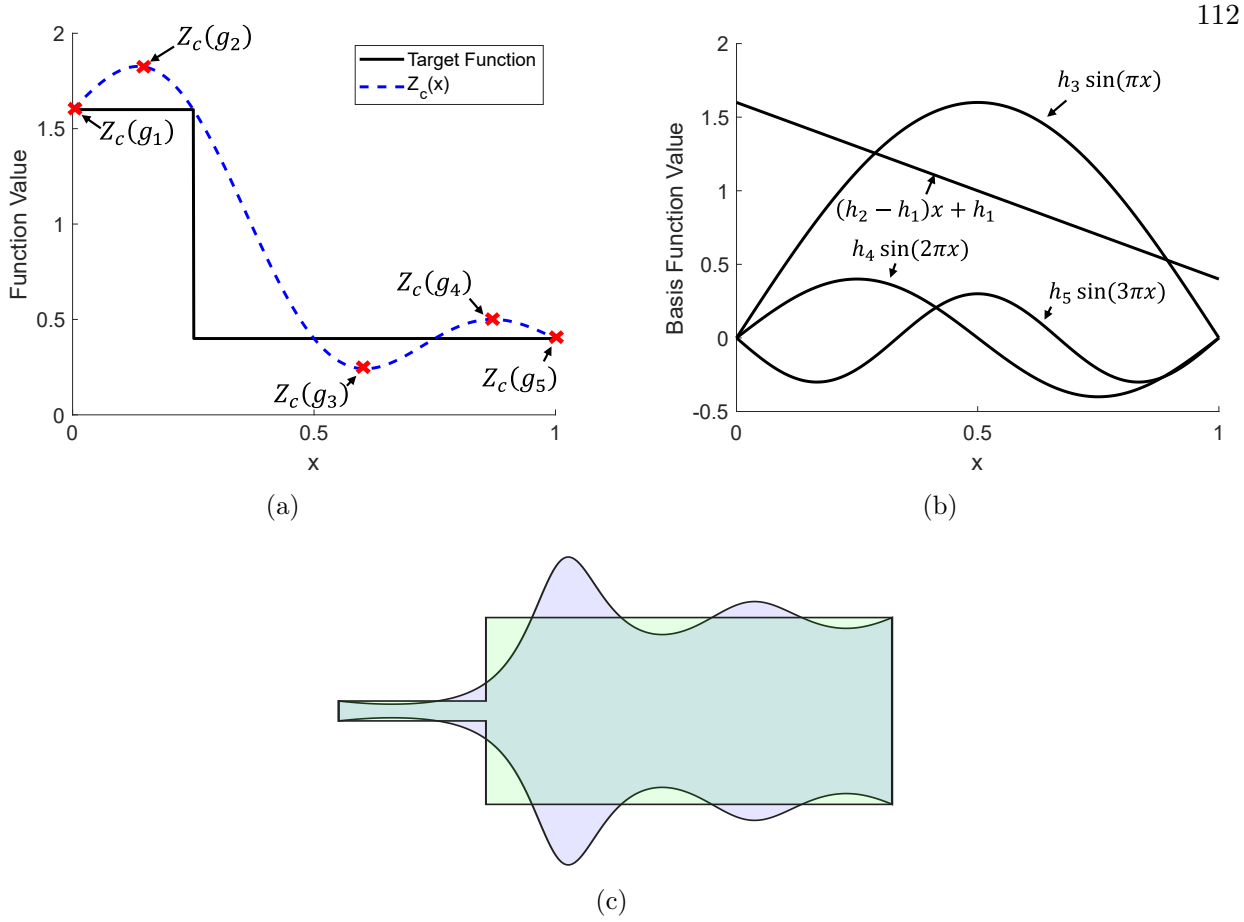


Figure 5.2: (a) Example characteristic impedance function (blue, dashed) designed to approximate a stepped impedance function (solid) over a domain of 0 to 1. The locations of Z_c for the values in the optimization vector, $\mathbf{g}$, are also called out. (b) The individual hybrid basis functions are illustrated on the bottom over the same domain with the corresponding elements of $\mathbf{h}$. The hybrid basis functions consist of a single linear function and half-range sinusoidal functions. (c) An overlay of the corresponding microstrip line silhouettes assuming a 20 mil Rogers 4350b substrate.

(5.10). This is accomplished by finding the following polynomial of the variable y:

$$f(y) = (h_2 - h_1) + \pi \sum_{k=1}^{N} h_{k+2} k T_k(y) \tag{5.12}$$

where $T_k(y)$ is the k^{th} degree Chebyshev polynomial of the first kind. Next, the stationary point locations are found by taking the arc-cosine of real zeros of (5.12) over the interval $-1 \leq y \leq 1$. This forms the final optimization vector of variable length:

$$\mathbf{g} = \begin{bmatrix} 0 & \arccos\{roots[f(y)]\} & 1 \end{bmatrix} \tag{5.13}$$

Fig. 5.2a calls out $Z_c(\mathbf{g}_n)$ for the example function. As mentioned in (5.13) the first and final values of $\mathbf{g}$ are the first and last point on the line. The intervening values of $\mathbf{g}$ are the corresponding stationary points of Z_c.

From (5.13) the non-trivial values of $\mathbf{g}$ are determined by the roots of $f(y)$ that are real and lie between -1 and 1. In order to recover $f(y)$, (5.12) may be rewritten to use a matrix $\mathbf{G}$ that will relate the values of $\mathbf{h}$ to the corresponding order of $\mathbf{y}$:

$$f(y) = (h_2 - h_1) + \pi \mathbf{h}_b \mathbf{G} \mathbf{y}^T \tag{5.14}$$

where

$$\mathbf{h}_b = \begin{bmatrix} h_3 & h_4 & \cdots & h_{N+2} \end{bmatrix} \qquad \mathbf{y} = \begin{bmatrix} y^N & \cdots & y & 1 \end{bmatrix}$$

$$\mathbf{G} = \begin{bmatrix} g_{1,1} & \cdots & g_{1,N+1} \\ \vdots & \ddots & \vdots \\ g_{N,1} & \cdots & g_{N,N+1} \end{bmatrix}$$

Table 5.1 give the symbolic expressions for the first four polynomials of (5.14). Recomputing (5.14) with every update to $\mathbf{h}$ is costly, but by computing $\mathbf{G}$ only when N is updated, the exact coefficients of (5.12) may be determined without needing to recompute the polynomial for every update to $\mathbf{h}$. $\mathbf{G}$ is a sparse matrix formed only of anti-diagonal sequences of integers with alternating signs. As an example $\mathbf{G}$ will have the form:

$$\mathbf{G} = \begin{bmatrix} 0 & 0 & 0 & 0 & a_{1,1} & 0 \\ 0 & 0 & 0 & a_{1,2} & 0 & -a_{2,1} \\ 0 & 0 & a_{1,3} & 0 & -a_{2,2} & 0 \\ 0 & a_{1,4} & 0 & -a_{2,3} & 0 & a_{3,1} \\ a_{1,5} & 0 & -a_{2,3} & 0 & a_{3,2} & 0 \end{bmatrix}, \tag{5.15}$$

where $a_{m,n}$ is entry n of sequence m. Two things are worth noting about $\mathbf{G}$. First, $\mathbf{G}_N$ is a subset of $\mathbf{G}_{N+1}$–which allows for pre-computing $\mathbf{G}$. Second, these sequences along the anti-diagonals may

Table 5.1: First Four Polynomials Relating to (5.14)

$\mathbf{h}_b\mathbf{G}\mathbf{y}^T$
$[h_3 y]$
$\left[4h_4y^2 + h_3y - 2h_4\right]$
$\left[12h_5y^3 + 4h_4y^2 + (h_3 - 9h_5)\, y - 2h_4\right]$
$\left[32h_6y^4 + 12h_5y^3 + (4h_4 - 32h_6)\, y^2 + (h_3 - 9h_5)\, y - 2h_4 + 4h_6\right]$

be determined through difference tables with the first four sequences being:

$$a_{1,n} = 2a_{1,n-1} + 2\left[2^{n-2}\right]$$

$$a_{2,n} = 4a_{2,n-1} - 4a_{2,n-2} + 4\left[2^{n-3}\right]$$

$$a_{3,n} = 6a_{3,n-1} - 12a_{3,n-2} + 8a_{3,n-3} + 12\left[2^{n-3}\right]$$

$$a_{4,n} = 8a_{4,n-1} - 24a_{4,n-2} + 32a_{4,n-3} - 16a_{4,n-4} + 32\left[2^{n-3}\right]$$

Furthermore, the first sequence is equivalent to:

$$a_{1,n} = n \cdot 2^{n-1}$$

The above outlines the formulation of the nonuniform impedance optimization vectors. The design procedure is explained next.

5.3 Design Procedure for NTL Networks

The design procedure is somewhat application dependent (i.e. a filter, amplifier, matching network, etc.) but every approach uses the building blocks described above and a combination of the following steps:

(1) Initialization – the process of defining the goals, initial conditions, boundary conditions, constraints, and network connections;

(2) Optimization – the process of systematically determining the values of the optimization vectors described above that yield a viable (or nearest viable) solution; and

(3) Growth – the process of starting with a simple solution and increasing the complexity gradually.

These concepts are discussed in the following sections in further detail, along with the process flows used in several of the later design examples.

5.3.1 Initialization

Initialization sets the initial conditions, and defines the design objectives, constraints and rate at which scaling occurs. The initial conditions play a very important role in how quickly a solution converges. For $\mathbf{h}$, the initial conditions are $h_1 = 1$, $h_2 = 1$, and $h_n = 0|_{n\neq[1,2]}$. On the other hand, if the terminal impedances of a network are already known, following (5.9) results in $h_1 = z_a$ and $h_2 = z_b$, where z_a and z_b are the known, normalized terminal impedances of the NTL element. The length of the line is initialized by setting f_c equal to the desired guided wavelength frequency, f_λ (i.e. the frequency on the target substrate corresponding with the desired initial line length). From (5.8), this is accomplished by initializing $\mathbf{f}$ to unity and choosing f_n as f_λ.

The choice of f_λ is driven by the desired bandwidth, limitations in characteristic impedance, the ratio of matching impedances, and available space. In general, a longer line (i.e. a lower f_λ) corresponds to a broader bandwidth. A lower-bound for the shortest possible line required to achieve a given match is shown in [136], where the maximum achievable bandwidth of an NTL is shown to be limited by the ratio of the minimum and maximum line impedance and the electrical length. An optimizer often attempts to use the widest range of impedance and longest lines possible. However, the minimum and maximum characteristic impedances need to be constrained to insure manufacturability, done both directly by constraining the values of $\mathbf{h}$ and indirectly by checking the impedance at each location specified by $\mathbf{g}$. Additionally, $\mathbf{f}$ should be constrained to insure that the line has a reasonable length.

The objectives include a name, weight, inequality, and target. The weighting function over frequency (sum, max, min, RMS, etc.) is also selected at this stage. This work uses the RMS weighting function.

5.3.2 Optimization

The optimizer forms the engine driving the design process, and Fig. 5.3 illustrates a the steps performed during optimization. This work uses the *fmincon* optimizer from the MATLAB optimization toolbox with the sequential quadratic programming algorithm. *fmincon* is a nonlinear, constrained optimizer that allows for direct, linear inequality, and nonlinear constraints.

While there are many methods of simulating generalized NTL networks [137, 138, 139, 140, 141, 142], this work uses 1D cascade parameters of a TEM line to simulate the line as a cascade of uniform line segments:

$$\begin{aligned}\mathbf{T}(x) &= \begin{bmatrix} A(x) & B(x) \\ C(x) & D(x) \end{bmatrix} \\ &= \begin{bmatrix} \cosh(\Theta(x,f)) & Z_c(x,f)\sinh(\Theta(x,f)) \\ \frac{\sinh(\Theta(x,f))}{Z_c(x,f)} & \cosh(\Theta(x,f)) \end{bmatrix}, \end{aligned} \tag{5.16}$$

where $Z_c(x,f)$ is the characteristic impedance of the line at the normalized position x and simulation frequency, f. Likewise, $\Theta(x,f)$ is the complex electrical length of the individual segments:

$$\begin{aligned}\Theta(x,f) &= \ell_{seg}\left[\alpha(x,f) + j\beta(x,f)\right], \\ &\approx \ell_{seg}\alpha(x,f) + j\frac{f}{\mathbf{f}f_n}\frac{2\pi}{N_{seg}}, \end{aligned} \tag{5.17}$$

where N_{seg} is the number of line segments used to model the candidate transmission line. In this work, the number of segments is chosen to be 201. The number of segments is such that the electrical length of each is electrically small, i.e. $\leq \lambda_g/10$, until a maximum frequency of $f_{max} \approx 20f_c$. One-dimensional frequency and width dependent parameters may either be estimated analytically or by applying Bloch-wave analysis to simulated ABCD parameters of the physical transmission lines.

$$\gamma = \frac{\cos^{-1}(A)}{\ell} \quad \text{and} \quad Z_c = \sqrt{\frac{B}{C}}, \tag{5.18}$$

where $\alpha = \Re\{\gamma\}$, $\beta = \Im\{\gamma\}$, and ℓ is the physical length of the simulated transmission line.

Next, the S-parameters of each individual transmission line are used to update the values of a larger network and the total S-parameters are computed. Once the network parameters for

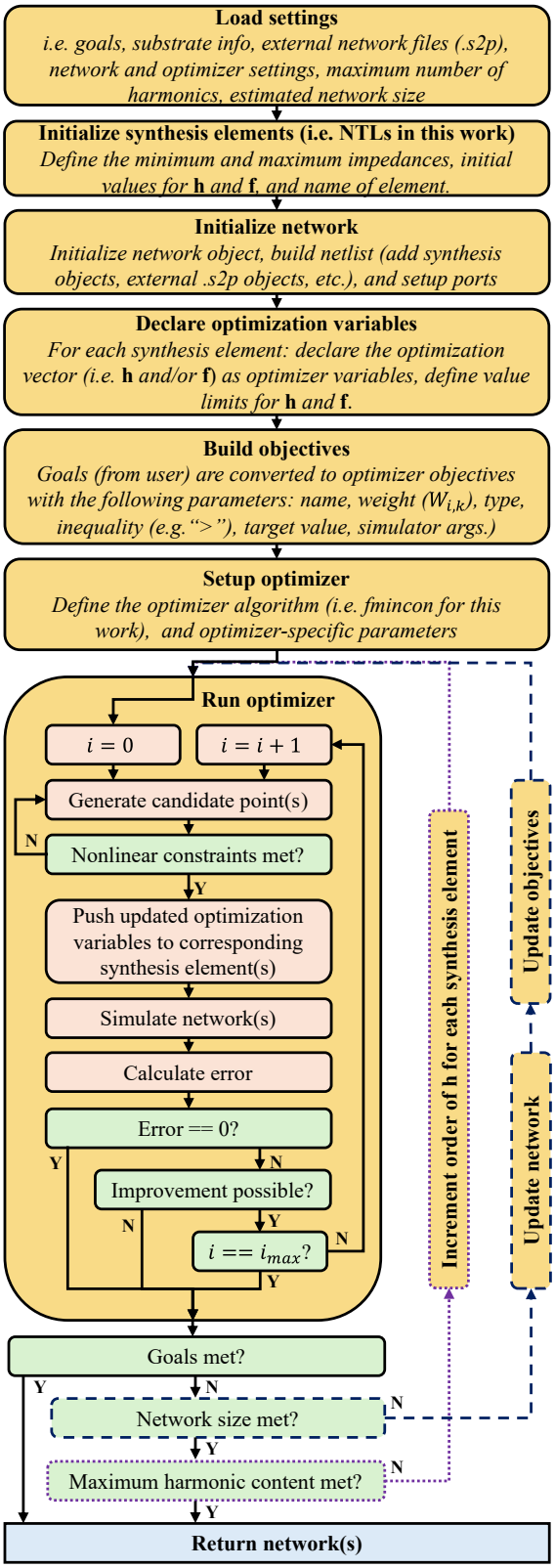


Figure 5.3: Diagram of the procedure used for automated network design. Synthesis elements such as an NTL or SRFT ladder network are combined into a complete network which is then optimized. Main tasks are denoted with a solid outline while optional growth processes, i.e. harmonic and network growth, have dashed and dotted outlines.

the entire network are determined, they may be converted to the generalized form through the following equation:

$$[S_{gen}] = [D^*]^{-1} \left([S_{norm}] - [\Gamma^*]\right) \left([U] - [\Gamma]\,[S_{norm}]\right)^{-1} [D]$$

where $[D]$ and $[\Gamma]$ are diagonal matrices with the element values:

$$D_{ii} = |1 - \Gamma_i^*|^{-1} (1 - \Gamma_i) \sqrt{1 - |\Gamma_i|^2}, \qquad \Gamma_i = \frac{Z_i - Z_0^*}{Z_i + Z_0}$$

with Z_0 being the system characteristic impedance and Z_i the load impedance at port i.

In this work, each objective function follows the pattern:

$$F_k(f_i) = \begin{cases} 0 & \text{goal met} \\ ||H_K(f_i) - G_k(f_i)|| & \text{goal not met} \end{cases},$$

where $H_k(f_i)$ is a design parameter, i.e. return loss, gain, stability, etc., and $G_k(f_i)$ is the associated goal. The objective's state, i.e. whether the corresponding goal has been met, is determined by an inequality. For an amplifier design two common goals might be the input match and gain with $\mathrm{dB}(|S_{11}|^2) \leq -10$ and $\mathrm{dB}(|S_{11}|^2) \geq 10$, respectively.

Once each objective function is defined, they are combined into a corresponding RMS error term:

$$E_k = \sqrt{\frac{1}{N+1} \sum_{i=0}^{N} \left\{ [W_{i,k} F_k(f_i)]^2 \right\}},$$

where $W_{i,k}$ is the k^{th} error weight for the i^{th} frequency f_i and $F_k()$ is the k^{th} objective function. Finally, all errors are combined into the composite error for the optimizer to minimize:

$$E_{total} = E_1 + E_2 + \cdots + E_{k-1} + E_k \tag{5.19}$$

The optimizer also uses nonlinear constraints to ensure the physical feasibility of the solution minimizing (5.19). This starts by finding the stationary values of Z_c:

$$\mathbf{Z_{stat}} = Z_c(\mathbf{g}) \ , \tag{5.20}$$

where $\mathbf{g}$ and Z_c come from (5.13) and (5.9), respectively. Next, the constraint violation with respect to the highest and lowest impedance can be found as:

$$\mathbf{Z_u} = \mathbf{Z_{stat}} - Z_{max} \quad \text{and} \quad \mathbf{Z_l} = Z_{min} - \mathbf{Z_{stat}} \ ,$$

where $\mathbf{Z_u}$ is the list of upper constraint violations and $\mathbf{Z_l}$ is the list of lower constraint violations. The maximum nonlinear constraint violation in Z_c is evaluated as:

$$Z_{const} = \max\left(\mathbf{Z_u}, \mathbf{Z_l}\right]) \ ,$$

where, from [143] where Z_{const} is c, the task of the optimizer is to ensure that $Z_{const} \leq 0$ while minimizing the objective error, E_{total}.

5.3.3 Growth

In this work, growth refers to the deliberate, systematic increase in solution complexity aimed at better fulfilling specific design objectives. We discuss two types of growth: harmonic growth and network growth. Their implementation is shown in Fig. 5.3, where they are illustrated as optional processes.

Harmonic growth refers to the iterative expansion of harmonic content, specifically by increasing the order of the vector $\mathbf{h}$. In this process, the NTL begins with an initial size, e.g. $N = 3$, and grows between design iterations, either until it reaches a maximum allowed size or until all design criteria are met.

Network growth refers to iteratively adding new networks, i.e. NTLs, to the circuit over multiple design iterations. This type of growth is frequently used for amplifier design, and often requires the use of intermediate goals with overall design criteria. For instance, the overall goal for an amplifier design might be to have 30 dB of gain with a maximum of 4 stages. To meet this overall objective, the amplifier may be designed sequentially with the target gain being increased every time a new stage is added. This approach has been documented in the synthesis of cascaded amplifiers [81, 97]. In this work, network growth is applied to the design of a distributed amplifier.

5.3.4 Planar NTL Layout

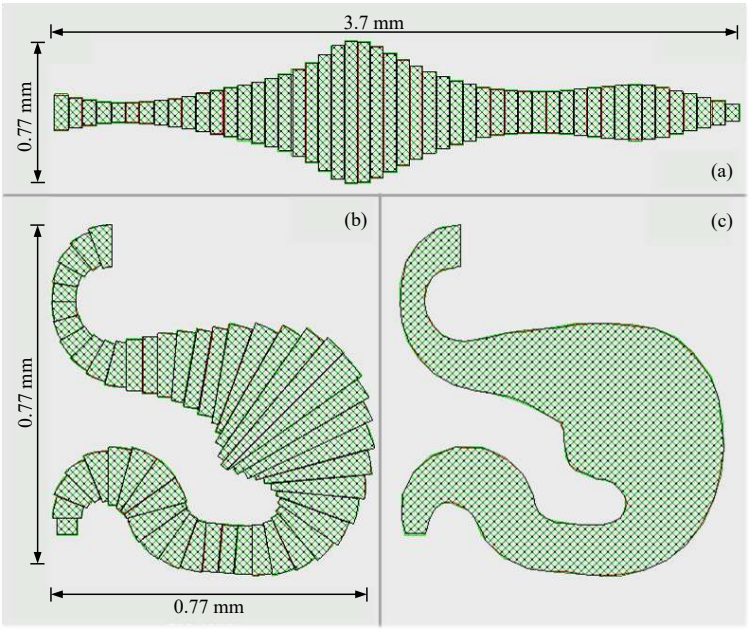


Figure 5.4: Manual approach to meandering a NTL from [127]. The transmission line (a) is imported into the design tool is manually meandered into (b) consisting of a smaller form factor and then smoothed to (c) the final network.

After the initial stages of design, meandering may be required to fit the design into the available circuit space. Fig. 5.4 illustrates the manual technique used in [127] to generate a microstrip NTL network, which is used for the layout of the amplifier of Fig. 5.1b. As mentioned in the introduction, the manual layout demonstrated in [127] is impractical due to the time and effort required and leaves little room for post-layout optimization. The following section expands this work to a method that automates the process while also observing the main electrical considerations.

Fig. 5.5 illustrates how the manual approach in Fig. 5.4 can be extended to a process for continuously meandering a NTL (e.g., Fig. 5.5a) when using N curved, uniform line segments (Fig. 5.5b). Fig. 5.6 annotates the critical parameters of these uniform line segments: the radius of curvature, R; initial direction, $\vec{d_a}$; terminal direction, $\vec{d_b}$; bend angle, θ; midline length, L; and width of the transmission line. The goal of bending or meandering a transmission line when doing circuit design is to preserve the electrical length of the transmission line at all design frequencies.

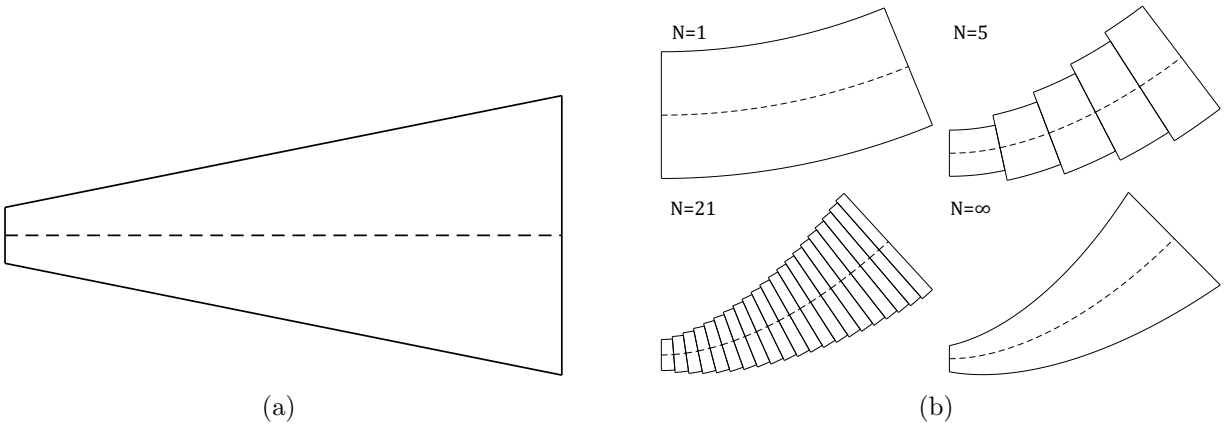


Figure 5.5: (a) The profile of a planar tapered transmission line. (b) That same transmission line meandered into a 45° bend with 1, 5, 21, and ∞ sub-segments. The curvature of the midline of the meandered taper is nonuniform and inversely proportional on the width of each sub-segment.

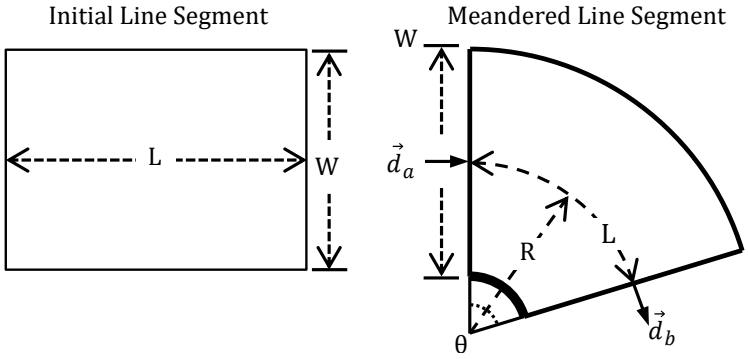


Figure 5.6: Elementary uniform curve segment of a non-uniform transmission line with annotated midline, radius of curvature, bend of segment, the initial direction ($\vec{d_a}$), and the terminal direction ($\vec{d_b}$).

Meandering planar circuits (especially microstrip circuits) introduces dispersion not present on the original line. A guideline to mitigate dispersion is suggested in [144] as:

$$R \geq 4W \tag{5.21}$$

This relation suggests introducing a new parameter that relates the width of the line to the radius of curvature:

$$\zeta = \frac{W}{2R} \tag{5.22}$$

where $-1 \leq \zeta \leq 1$ is required so that the line does not self-intersect. Combining (5.21) with (5.22)

leads to the general rule-of-thumb:

$$|\zeta| \leq \frac{1}{8} \tag{5.23}$$

In the case of a line segment of constant ζ described by a finite number of discrete midline sub-segments with a length of Δz, the total segment can be approximated as a composition of many smaller uniform microstrip bends with midline lengths of Δz. The total bend angle of the entire segment is the sum of all bend angles of each sub-segment, described as:

$$\theta = 2\zeta \sum_{i=1}^{N} \frac{\Delta z}{\max\left(W\left(i\right), W\left(i-1\right)\right)} \tag{5.24}$$

where $W\left(i\right)$ is the width at position $z\left(i\right)$ along the transmission line segment where $i \in [0, ..., N]$. Taking (5.24) and allowing $\Delta z \to 0$ the angle of the bend introduced by a segment of constant ζ may be described as:

$$\theta = \zeta \int_{z_{start}}^{z_{stop}} \frac{2}{W\left(z\right)} dz \tag{5.25}$$

where the maximum bend angle possible for a given line segment is clearly (5.24) when $|\zeta| = 1$.

After the automated a TEM solution is found the program moves to generating an equivalent microstrip network. Commensurate microstrip line segment data, i.e. widths and lengths, is generated by transforming the impedance (5.11) and electrical length (5.6) results into physical parameters using either quasi-static relations for microstrip lines, e.g. similar to the method discussed in [145], or by performing a reverse-lookup on microstrip line simulation data used to calculate Z_c and γ in (5.18). In this work, the number of line segments generated is 201. The layout is generated computationally by adding straight and curved line segments. The curved line segments are generated by meandering the midline of the microstrip line with a constant ζ from (5.24) while observing (5.23). The midline length required for a known θ and ζ can be solved from (5.24) or (5.25). Once the starting and stopping points are known, midline and width data, which is used to generate the edges, is re-interpolated over the line segment data. This work re-interpolates a bend segment to 101 sub-segments.

In the next section, we present several applications of this design method in relative order of circuit complexity, starting from passive circuits such as filters, and culminating in a GaN MMIC distributed amplifier design.

5.4 Passive NTL Examples

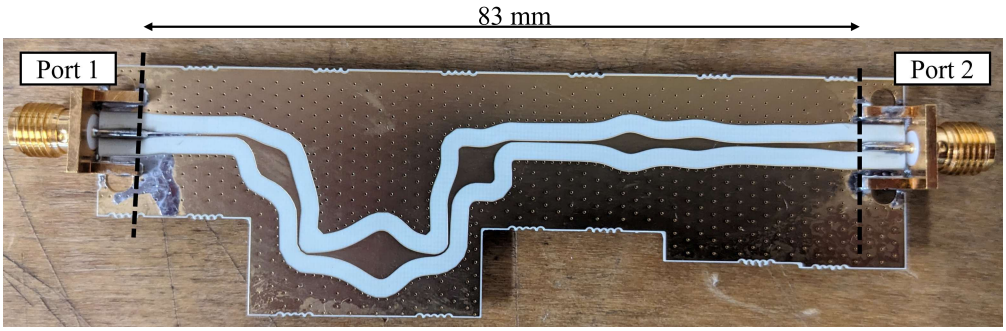
5.4.1 Band-Stop Filter

Table 5.2: Settings for Band-Stop Filter Design

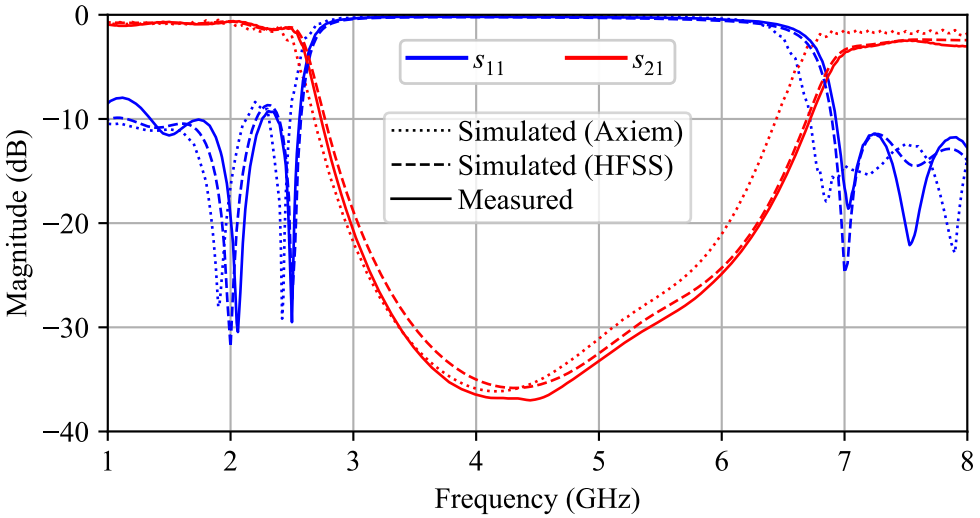
Optimization settings			
N_{segs}	201	f_n	1.8 GHz
$N_{h,start}$	24	$N_{h,stop}$	24
NTL initial state and constraints			
Parameter	Minimum	Maximum	Initial
h_1	-	-	1
h_2	-	-	1
$\mathbf{h}_n\|_{n>2}$	-1	1	0
Z_c	15Ω	100Ω	50Ω
$\mathbf{f}$	0.02	1.25	1
Objectives			
$f_{start} \rightarrow f_{stop}$ (GHz)	N_{pts}	Goal	Weight
$1 \rightarrow 2.5$	5	$\|S_{11}\|^2 \leq -10$dB	0.2
$3 \rightarrow 6$	21	$\|S_{21}\|^2 \leq -20$dB	0.05
$7 \rightarrow 8$	5	$\|S_{11}\|^2 \leq -10$dB	0.2

Simulator settings, constraints, and design goals for the band-stop filter NTL network design procedure. N_{seg} is the number of sub-segments used to compute the line parameters, $N_{h,start}$ and $N_{h,stop}$ refer to the starting and stopping number of harmonics used for this design.

To demonstrate the generality of this approach towards filter applications, a band-stop filter is designed with a target stop-band of 3-6 GHz with an insertion loss greater than 20 dB. A secondary design objective is to to maintain a return loss of greater than 10 dB in the pass-bands. Table 5.2 states the constraints and design objectives. The terminal line impedances are constrained to 50Ω, i.e. $h_1 = h_2 = 1$, so that the physical microstrip widths stay approximately the same size as the SMA connector pin diameter. The total execution time for the automated design algorithm



(a)



(b)

Figure 5.7: (a) Photograph of fabricated band-stop filter. (b) Response of the band-stop filter simulated in Axiem (2.5D method of moments), HFSS (3D finite element method), and measured.

is 28 seconds on a Dell OptiPlex 7080 with an Intel core I7-10700 CPU and 64 gigabytes of RAM and using parallel processing with 8 workers. The same computational hardware is used for all subsequent circuit designs. Referring to Fig. 5.3, the specific automated procedure used for this line is:

(1) Create NTL synthesis element with initial **h** and **f** values and Z_c nonlinear constraints from Table 5.2;

(2) Initialize a new network and add the NTL synthesis element to it between ports 1 and 2;

(3) Set the network port impedances to 50 Ω;

(4) Declare **h** as an optimization variable, terminal NTL impedances should be 50 Ω so $h_1 = h_2 = 1$;

(5) Declare **f** as an optimization variable as well and define its minimum and maximum values;

(6) Add objectives from Table 5.2 to the network;

(7) Initialize optimizer as the *fmincon* algorithm; and

(8) Optimize the network and return the results.

[120] has also demonstrates several examples of NTL networks that may be used for broadband filter applications. The fabricated NTL and the behavior over frequency is illustrated in Fig. 5.7. This network is fabricated on Rogers RO4350b and with total length of the network is 105 mm and meandering is applied to fit the NTL into the available circuit footprint. Discrepancy between the measured and simulated performance at the upper edge of the stop-band between the Axiem and measured results comes from unintended radiation losses. Simulations using a full-wave solver such as Ansys HFSS more accurately predict the impact of radiation loss on circuit performance.

5.4.2 Single Match

The methods discussed above may also be used to match resistive to complex reactive loads. Fig. 5.8a shows a fabricated NTL network that is designed to match a 50 Ω load on port 1 to a parallel RC load of 109 Ω and 0.515 pF on port 2 over a bandwidth of 2-4 GHz. Table 5.3 shows the specific settings used to generate this network. Harmonic growth is is implemented by starting with $N_{h,start} = 1$ harmonic and increasing to $N_{h,stop} = 8$ harmonics. As was the case with the band-stop filter, the terminal line impedances are constrained to 50Ω so the terminal line widths remain compatible with the SMA connectors. The total execution time for the algorithm is 1 minute and 51 seconds using the same computational hardware as in the previous example. This

Table 5.3: Settings for Matching Network Design

Optimization settings			
N_{segs}	201	f_n	4 GHz
$N_{h,start}$	1	$N_{h,stop}$	8
NTL initial state and constraints			
Parameter	Minimum	Maximum	Initial
h_1	-	-	1
h_2	-	-	1
$\mathbf{h}_n\|_{n>2}$	-5	5	0
$\mathbf{f}$	0.01	36	1
Z_c	15Ω	80Ω	50Ω
Objectives			
$f_{start} \rightarrow f_{stop}$ (GHz)	N_{pts}	Goal	Weight
$2 \rightarrow 4$	5	$\|S_{11}\|^2 \leq -15$dB	1

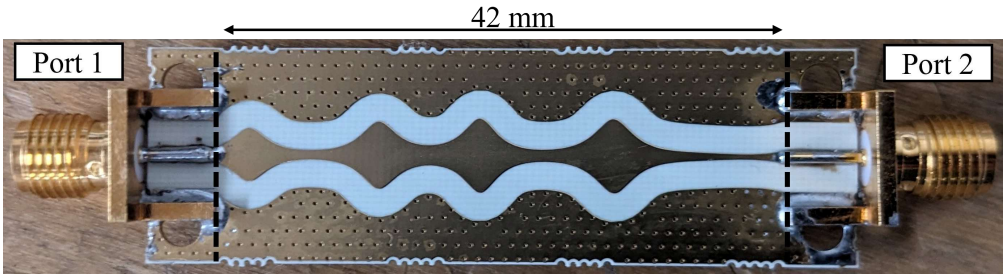
Table of settings pertaining to the design of an NTL matching network.

network is fabricated on 20 mil Rogers 4350b with a total length of 42 mm. Additionally, this circuit is designed to have terminating characteristic impedances of 50 Ω.

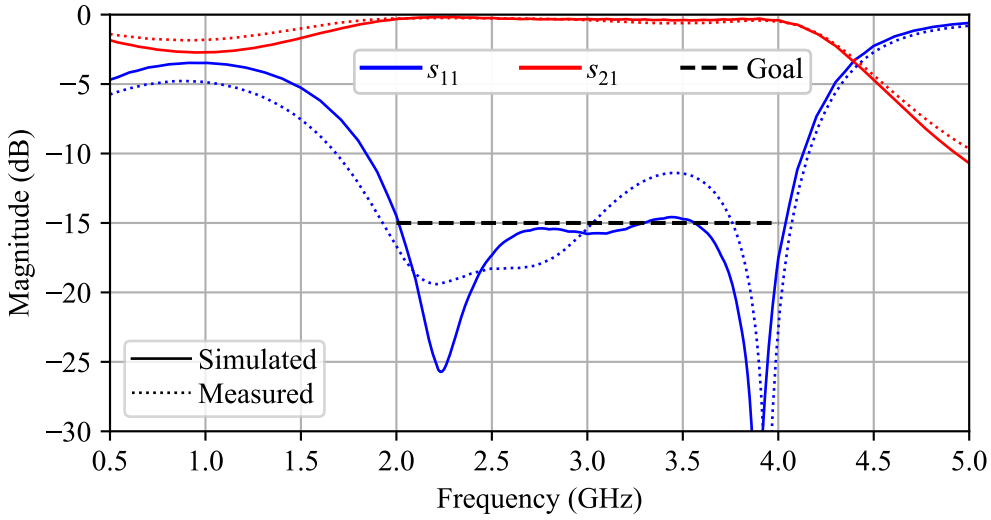
From Fig. 5.8b electromagnetic simulations of the designed network maintains a return loss greater than 15 dB across the band. The fabricated network achieve a return loss in excess of 10 dB over the same bandwidth and a return loss of greater than 15 dB from 2-3 GHz. The peak insertion loss for the fabricated network is 0.64 dB. The return loss of the fabricated network decreases to a minimum return loss of 11.4 dB at 3.45 GHz.

5.4.3 VCO Resonator

This method is applied to design a resonator for the voltage controlled oscillator (VCO) illustrated in Fig. 5.9a. Referring to Fig. 5.9b, the core and varactor elements of this VCO are designed to use a uniform shunt microstrip line resonator and the selected process is the WIN Semiconductors low-phase-noise InGaP/GaAs H01U-G3 HBT process [146]. Because resonator quality factor limits the phase noise of the VCO, a NTL resonator can improve phase noise compared



(a)



(b)

Figure 5.8: (a) Fabricated NTL matching network transforming a parallel RC load (109Ω and 0.515 pF) to a 50Ω load over an octave bandwidth. (b) Response of the matching network simulated (method of moments) and measured.

to a uniform microstrip resonator. The resonator is designed to maximize the unloaded quality factor while maintaining an input match of $1.74 + j18.4\Omega$ at 4.58 GHz. The simulated unloaded quality factor of the uniform microstrip resonator is Q_u =45.5, while the NTL resonator designed using the method shown here results in Q_u =48.

The loss and characteristic impedance versus line width is extracted from the process microstrip models using Bloch analysis. This is accomplished by performing a parameterized simulation of a microstrip line for the target process while sweeping the width, W, of that transmission line. The S-parameters are extracted at frequency f_{ex}, converted to ABCD parameters and (5.18)

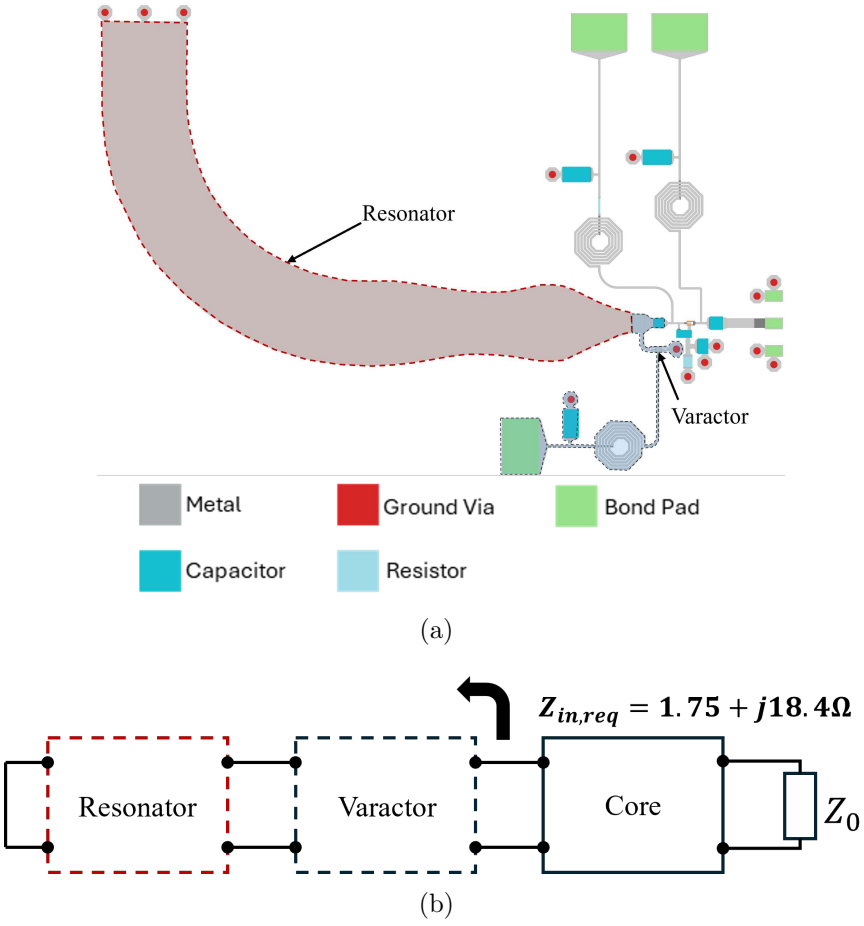


Figure 5.9: (a) Layout of a high-efficiency, low-phase-noise VCO with a total circuit size of 3.7×2.5 mm. (b) The block diagram of the VCO network.

is used to determine the corresponding complex $\gamma\,(W, f_{ex})$ and $Z_c\,(W, f_{ex})$. Note that ℓ in (5.18) is the length of the NTL used during simulation.

In (5.17), the real part of the complex electrical length depends on both ℓ and α. This presents an issue as ℓ, the physical line length, is unknown at the start of the design process. To address this, ℓ is substituted out using the following relationships:

$$\theta_{seg} = \beta \ell_{seg} \quad \text{and} \quad \ell_{seg} = \frac{\theta_{seg}}{\Im\left\{\gamma_{interp}\,(Z_c, f)\right\}}, \tag{5.26}$$

where γ_{interp} is a function of the NTL model characteristic impedance and frequency and θ_{seg} is the segment electrical length (in radians). Referring to the previous paragraph, the function for

γ_{interp} is generated from a 2D interpolation of $\gamma(W, f_{ex})$ with the corresponding $\Re\{Z_c(W, f_{ex})\}$ and f_{ex}. Using (5.11), γ_{interp} is rewritten as a function of x and f

$$\gamma_{interp}(Z_c(x), f) \rightarrow \gamma_{interp}(x, f).$$

The complex electrical length, Θ, of a uniform line segment located about x is:

$$\Theta(x, f) = \ell_{seg}\gamma_{interp}(x, f). \tag{5.27}$$

Substituting (5.26) into (5.27), removes the dependency on ℓ_{seg}:

$$\Theta(x, f) = \left(\frac{\theta_{seg}}{\Im\{\gamma_{interp}(x, f)\}}\right)\gamma_{interp}(x, f).$$

If all line segments in the NTL model are equal in electrical length, then the relationship above is rewritten as:

$$\Theta(x, f) = \frac{f}{\mathbf{f}f_n}\frac{2\pi}{N_{seg}}\frac{\gamma_{interp}(x, f)}{\Im\{\gamma_{interp}(x, f)\}}, \tag{5.28}$$

where, N_{seg}, is the number of uniform line segments used to simulate the NTL response. (5.28) is a direct replacement for (5.17) in (5.16).

The complex Z_c associated with a lossy transmission line is generated in a procedure similar to γ_{interp}. $Z_{c,interp}(Z_c(x, f))$ is derived from the 2D interpolation of $Z_c(W, f_{ex})$ with $\Re\{Z_c(W, f_{ex})\}$ and f_{ex}. Using (5.11), $Z_{c,interp}$ is rewritten as:

$$Z_{c,interp}(Z_c(x), f) \rightarrow Z_{c,interp}(x, f), \tag{5.29}$$

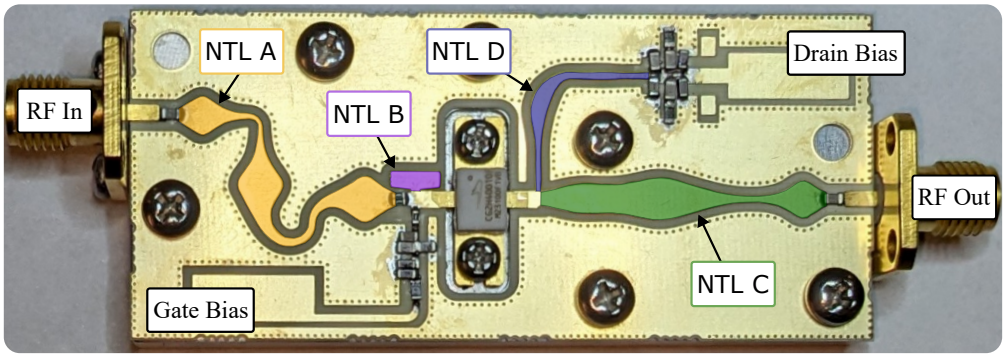
where (5.29) is substituted for $Z_c(x, f)$ in (5.16).

5.5 Amplifier Matching Network Design

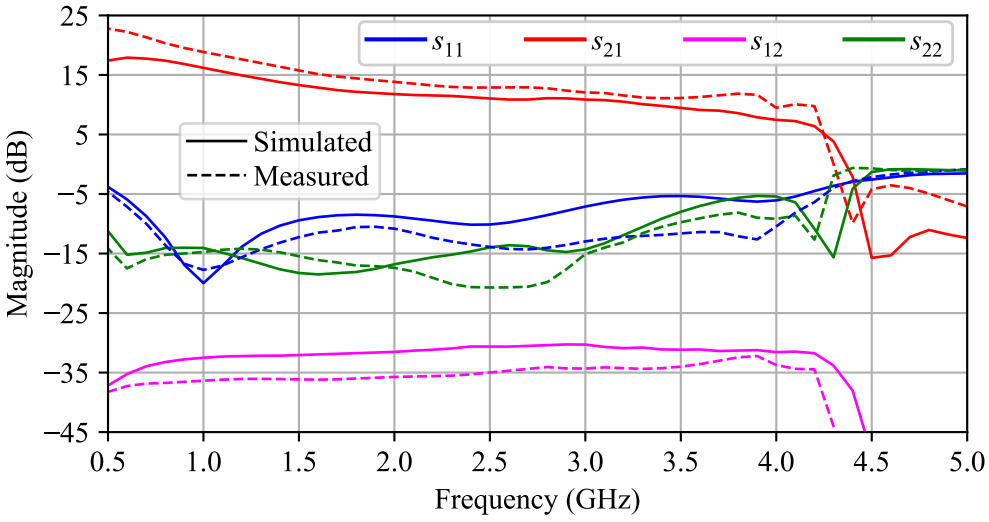
Designing amplifiers with bilateral elements is an iterative process that generally requires multiple iterations to achieve a desired behavior. The quantity of effort and time required increases dramatically when multiple stages or a large bandwidth is required–ultimately leading to longer design timelines and higher end-product costs. [97, 147] have demonstrated the application of

the simplified real frequency technique for amplifier synthesis using lumped element networks. Next, this same approach will be applied towards the design of hybrid and monolithic single-stage amplifiers.

5.5.1 Hybrid Amplifier



(a)



(b)

Figure 5.10: (a) Fabricated amplifier that uses four NTL matching networks (highlighted in orange, purple, blue, and green) and (b) the amplifier's small-signal behavior both measured and simulated.

Fig. 5.10 illustrates a driver amplifier that utilizes four co-designed NTL networks. Total execution for the design process is 5 minutes and 11 seconds. The PCB material is Rogers 4350b and the FET is a Macom CG2H40010F packaged GaN transistor. The target design goals were to

achieve a minimum return loss of 10 dB from the input and output matching networks and a gain in excess of 10 dB across a bandwidths of 1-4 GHz. The settings for this design are shown in Table 5.4. The open-circuit stub is initialized to the shortest length possible while the input matching network is initialized to the longest. The output bias line and the output matching networks are initialized to 90° and 180° at 4 GHz, respectively. Only the terminal widths of the open-circuit stub and

Table 5.4: Settings for Hybrid Amplifier Design

Optimization settings			
N_{segs}	201	f_n	4 GHz
$N_{h,start}$	1	$N_{h,stop}$	8
NTL initial state and constraints			
Parameter	Minimum	Maximum	Initial
h_1	-	-	1
h_2	-	-	1
$\mathbf{h}_n\|_{n>2}$	-5	5	0
Z_c	20Ω	110Ω	50Ω
NTL A: Input matching network[*]			
f	1	36	1
NTL B: Open-circuit stub[*]			
h_1	1.2	1.8	1.6
h_2	1.2	1.8	1.6
f	2	36	36
NTL C: Output matching network[*]			
f	1	36	2
NTL D: Output bias[*]			
h_1	1.4	1.8	1.6
h_2	1.4	1.8	1.6
f	1	36	4
Objectives			
$f_{start} \rightarrow f_{stop}$ (GHz)	N_{pts}	Goal	Weight
$1 \rightarrow 4$	11	$\|S_{11}\|^2 \leq -10$dB	1
		$\|S_{22}\|^2 \leq -10$dB	1
		$\|S_{21}\|^2 \geq 10.5$dB	10
$0.1 \rightarrow 20$	19	$\mu_1 \geq 1$	100

[*] Network-specific initial state and constraint settings. Refer to Fig. 5.10a for corresponding NTL placement.

output bias network are optimized.

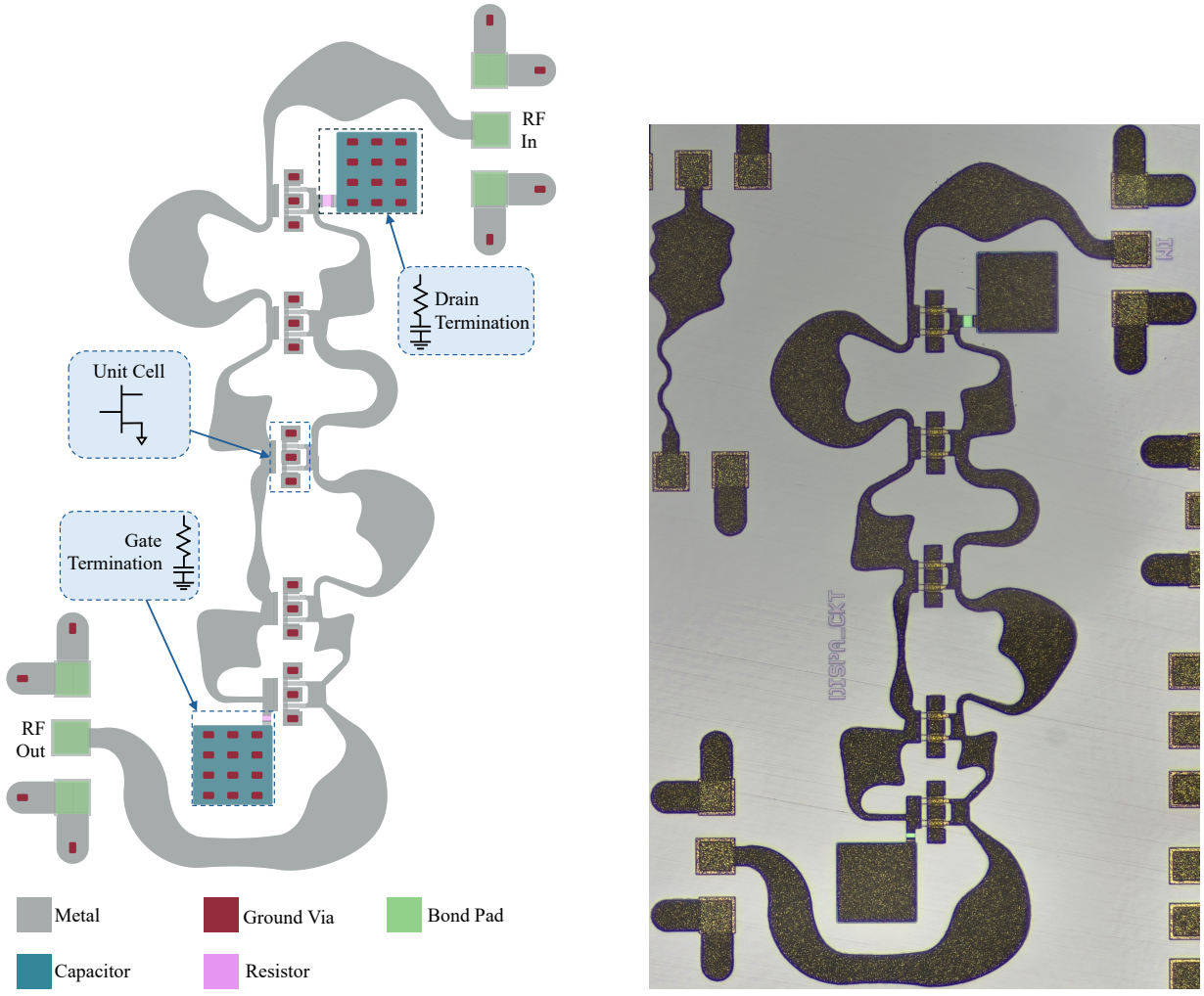


Figure 5.11: (a) Layout and (b) image of the 1.39×2.18 mm distributed amplifier using five 8x50 devices and ten meandered NTLs developed in Qorvo's 90 nm GaN on Silicon Carbide process.

Stability is always a significant consideration in amplifier design and is usually the greatest challenge at lower frequencies (i.e. where gain is greater). A parallel RC circuit in series with the gate may be used for stability but introduces a capacitor in the RF path. This would make the stability of the amplifier dependent on factors that are difficult or expensive to control–such as model accuracy, vendor reliance, and capacitor tolerance. Furthermore, because lossy elements are being introduced, it is desirable to see improvements in the match to the amplifier as well. For

these reasons a second nonuniform transmission line is added as a open-circuit stub between the series resistor and gate of the FET. The degradation in input return loss at higher frequencies is due to higher series inductance, i.e. $\approx 0.3\,\text{nH}$, in the stability resistors than was originally anticipated during the design process.

5.5.2 Distributed Amplifier MMIC

This method of design can also be applied to distributed amplifiers design. Fig. 5.11 illustrates a five-cell distributed amplifier MMIC designed in a 90-nm GaN-on-SiC process. Fig. 5.11a illustrates the layout and corresponding terminations while Fig. 5.11b shows the fabricated chip. The total execution time for the design of this network is 14 minutes and 51 seconds. The input and output transmission lines of the distributed amplifier were designed to to maintain a target transducer gain $>10\,\text{dB}$ between dc and 40 GHz and an input and output return loss $>10\,\text{dB}$ up to 50 GHz as shown in Fig. 5.12. Additionally having geometric stability factors >1 were also used as an additional design parameter for the input and output lines. Once designed, these networks are meandered using the methods discussed in this work.

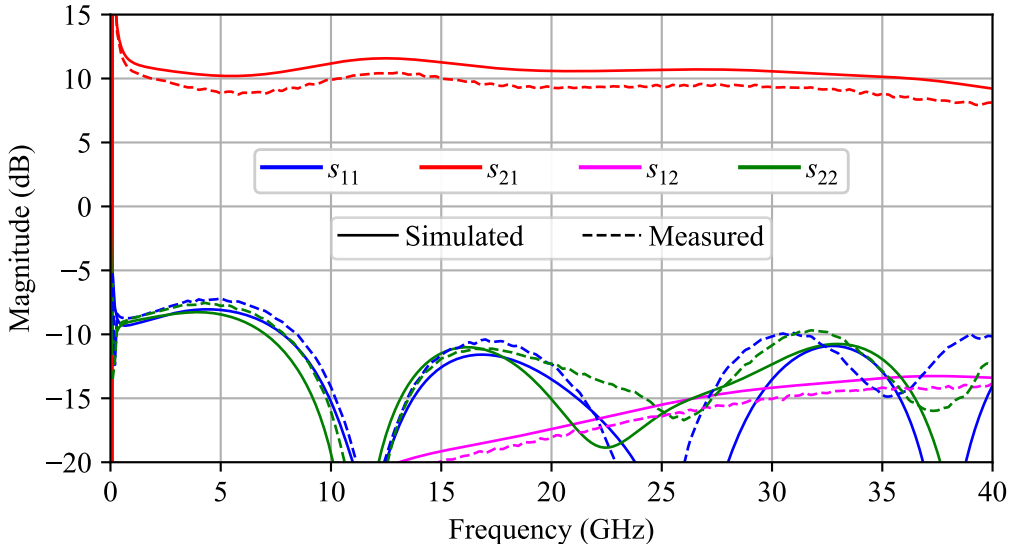
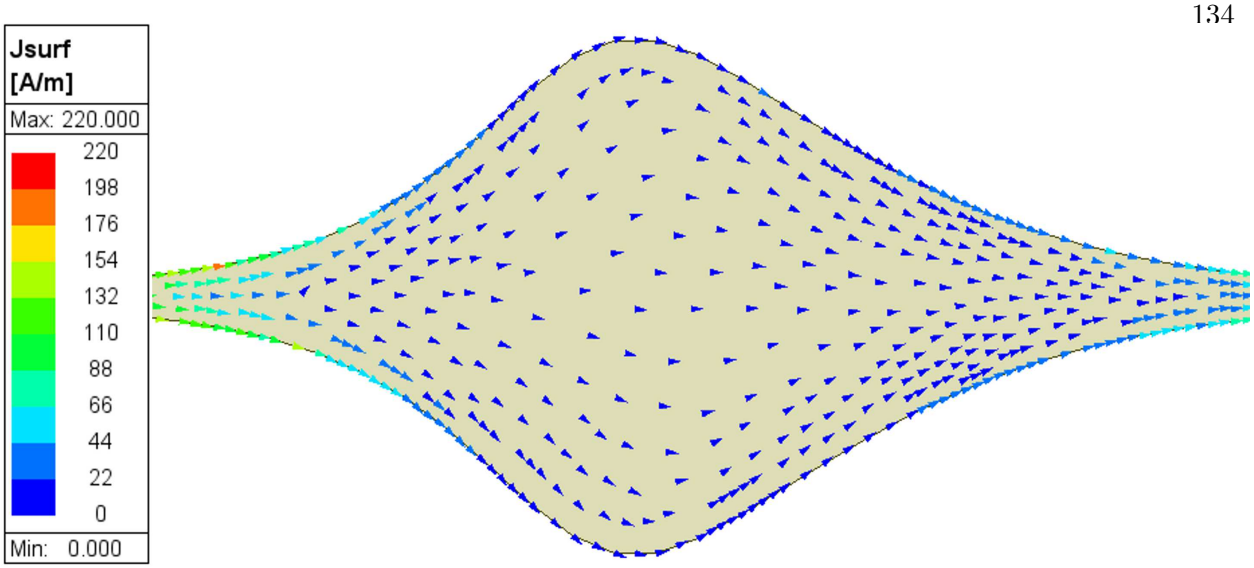
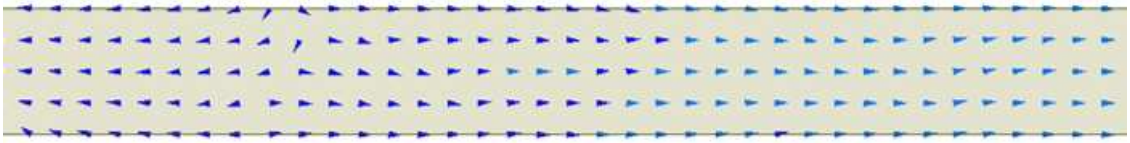


Figure 5.12: Simulated and measured scattering parameters of the distributed amplifier illustrated in Fig. 5.11. In both simulation and measurement the circuit achieves a good match from dc to 50 GHz. The simulated gain is $> 10\,\text{dB}$ from dc to 35 GHz while in measurement the gain is about 1.2 dB lower with a gain $> 8.8\,\text{dB}$ over the same range.



(a)



(b)

Figure 5.13: The direction of the surface currents on the NTL that were simulated in Ansys HFSS at 5.5 GHz for (a) a segment of the band-stop filter and (b) 50 Ω uniform microstrip line. The legend illustrated in (a) also applies to (b). The currents in an microstrip NTL tend to follow the contour of the line–exciting modes that are not TEM in behavior.

5.6 Discussion

The one-dimensional model of an NTL network is useful for computing a complete first-order approximation of the network response with minimal penalty in compute time. The drawback in this approach is that modes not supported by the transmission-line model appear when geometric properties abruptly change (e.g. line width for microstrip). In a TEM transmission line the surface currents should point in the direction of propagation. Figure 5.13 compares the vector components of the surface currents of a segment of the NTL from the band-stop filter example shown in Fig. 5.7a and a uniform microstrip line segment. Both lines are simulated at 1 GHz on the same substrate using HFSS. The surface currents in Fig. 5.13a spread out to satisfy the boundary conditions,

showing that the magnetic field vector is not quasi-TEM and has a considerable component in the propagation direction. Therefore, a stepped-impedance circuit-based model would have degraded accuracy in this case. Similarly, a microstrip radial bend also excites modes that are not quasi-TEM especially when the radius of curvature is large compared to the width of the line.

5.7 Conclusions

Here we present a method for designing nonuniform transmission lines in a manner that is readily expanded to many different types of networks. Physical size and layout considerations have traditionally presented a significant application barrier as NTLs are physically large. To manage this, a method for meandering NTL planar circuits has been presented which can be readily incorporated into modern CAD programs for further layout automation. This work is published in [127]. Likewise, the VCO resonator discussed in Section 5.4.3 is published in [148].

Chapter 6

Network Emulation

6.1 Introduction

Common nonlinear high-frequency circuit simulation methods, such as harmonic balance, rely on accurate large-signal models of nonlinear devices (e.g., high-electron mobility transistors, HEMTs) to predict key performance metrics like power, efficiency, and linearity. However, developing such nonlinear device models is a costly and time-consuming process, typically performed by the device manufacturer or a third party. As a result, models for new technologies are often underdeveloped, which can discourage early adoption. Even mature models may be inadequate for applications in extreme environments, such as those encountered in space or defense applications. While advanced, physics-based models can account for complex effects like temperature dependence [149, 150] and charge trapping [151, 152, 153], their development still requires specialized expertise. Alternatively, X-parameters [154]—an extension of S-parameters—can be measured directly by designers with the appropriate equipment and tools. However, X-parameter models can become unwieldy as the number of sweeps, ports, and parameters increases, and may not be suitable for devices with strong memory effects [155].

To address these challenges, we present network emulation—a hardware-in-the-loop (HITL) approach to circuit analysis that eliminates the need for a nonlinear device model. Network emulation is a method where electrical environment of a passive network is replicated around a physical device. Fig. 6.1 illustrates the process for a single-stage amplifier. The process begins with a circuit design, as shown in Fig. 6.1a, including sources and loads, i.e. boundary conditions, linear networks,

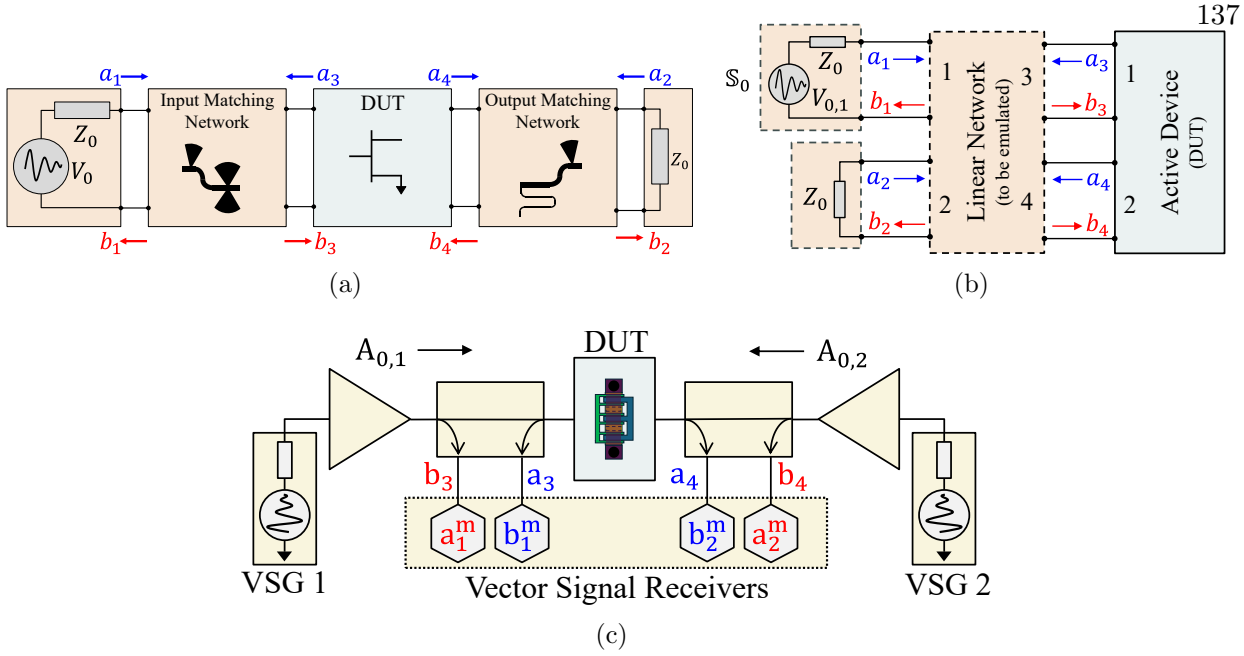


Figure 6.1: Network emulation of a single-stage amplifier. (a) Network-oriented power waves; (b) equivalent circuit diagram; (c) implementation on the active device using a vector signal transceiver measurement system. Power waves are referenced to the network, except for the measured power waves a_1^m, b_1^m, a_2^m, and b_2^m, which are referenced to the device under test.

and active devices. These elements are reorganized into the equivalent block diagram in Fig. 6.1b, which is used to determine the corresponding excitations for the active device. These excitations are then applied to the physical device via the measurement system shown in Fig. 6.1c. The measurement system records the response of the device under test (DUT) and returns it to the network model. The unknown power waves in the circuit are then determined by re-embedding the linear network, completing the analysis with the full circuit response. Although not explicitly shown in Fig. 6.1a, coupling between networks (e.g., feedback or electromagnetic coupling) is supported by this technique.

Network emulation offers novelty to the design process through its technical approach and application. Its technical approach involves determining and applying an excitation A_0. In Fig. 6.1c, $A_{0,1}$ and $A_{0,2}$ are the excitations that ensure the power waves a_3, b_3, a_4, and b_4 are equivalent to those of Fig. 6.1a. Achieving this requires several key contributions: (1) a modified and simplified

form of power-wave boundary conditions; (2) a generalized tuner model suitable for wideband active source and load-pull; and (3) a method for determining large-signal excitations through a general linear network.

It is important to note that the emulation method demonstrated herein, looks superficially like active source and load-pull and indeed the novel methodologies presented can be applied on any open-loop active source/load-pull measurement system. However the key distinction is that load/source-pull is fundamentally a *device-level* characterization tool [156]. The emulation method within allows for characterization of a physical transistor within a virtual matching network, allowing for *system-level* characterization. It may therefore be tempting to conclude that the technique presented is a simple linear embedding, however the virtual linear networks necessarily change the excitation to the non-linear device. This change in excitation leads to a different (nonlinear) device response and therefore cannot be described by a linear embedding model. As a result, it may be useful to think of this as a harmonic balance analog which uses a physical transistor, rather than a model, to determine the non-linear response of a circuit.

Microwave network emulation has been demonstrated for networks at the output of an amplifier [157, 158, 159, 160, 161], and the emulation of interstage matching networks networks is discussed in [162]. However to the best of the authors' knowledge no prior work has demonstrated coupling between the input and output networks of an amplifier stage, i.e. intentional feedback or electromagnetic coupling. This sort of coupling is an important effect in high-frequency circuits which significantly impacts performance. Additionally, the procedure followed in the aforementioned references is not entirely clear. The goal of this chapter is to provide a rigorous explanation of a general and scalable approach for microwave network emulation.

From the circuit designer's perspective, using network emulation does not change how the design process is carried out. The only change is that the nonlinear model is replaced with a physical device. The limitation is shifted from a matter of model accuracy and availability to a matter of experimental accuracy and measurement equipment availability. Fig. 6.2 illustrates the high-level process of network emulation. The process starts when the user triggers circuit analysis in the CAD

tool. The computer aided design (CAD) tool (e.g. Keysight's ADS or Cadence's MWO) Shift the phrasing to using python which can interface with all existing CAD tools. Say this later. simulates the passive network S-parameters and hands the S-parameters and desired circuit excitations over to the network emulator. The network emulator uses this information to determine the equivalent excitations for the device under test, i.e. the nonlinear device, and sends it to the test bench. The test bench applies the excitations to the DUT and returns its measured response to the network emulator. The network emulator computes the excitations at the circuit ports of interest using the network S-parameters and given excitations. Finally the CAD tool reports the overall circuit performance to the user.

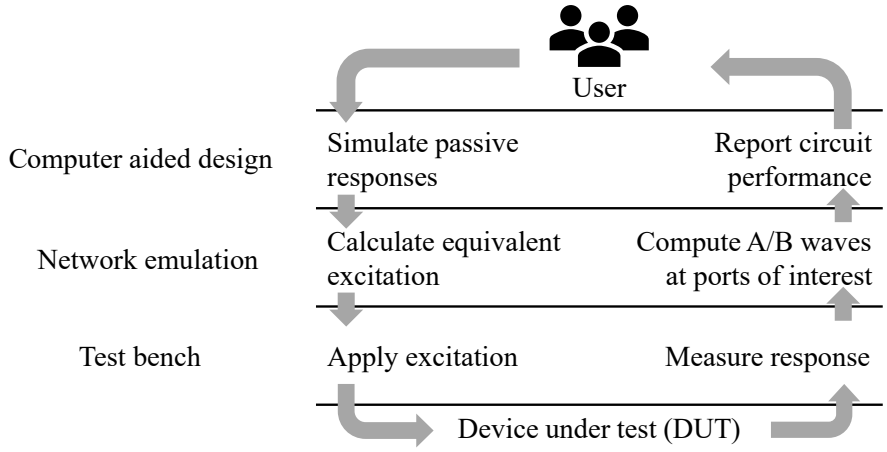


Figure 6.2: Outline of the process and layers that compose network emulation. The DUT is the only nonlinear element of this process.

The purpose of this chapter is to present a detailed accounting of the mechanisms that make network emulation possible along with working demonstrations of its viability. To that effect, this chapter is presented as follows: Section 6.2 introduces the hardware equivalent source as an abstraction of a calibrated measurement system with a vector source and receiver(s). Section 6.3 expands the equivalent source into a general, active tuner useful for load and source pull. Section 6.4 demonstrates the use of equivalent sources for emulating simple two-port networks. Section 6.5 expands two-port emulation to form a generalized N-port network emulation approach. Section 6.6 demonstrates generalized network emulation in small and large signal for a two-port amplifier.

Finally, Section 6.7 concludes this chapter with some final observations and remarks on network emulation. Measurements from the presented methods are provided in each section to illustrate their efficacy and viability.

6.2 The Hardware Equivalent Source

As a hardware-in-the-loop technique, network emulation requires a physical interface with the measurement system called the hardware equivalent source. The Thévenin and its dual, the Norton equivalent source, are commonly used in linear circuit theory to distill complex linear systems down to a pair of simple, intrinsic properties: an impedance and an excitation. The excitation can have many forms, including an RF modulated signal, which are represented in this chapter by multi-tone signals. In this chapter, we use a modified version of the Thévenin equivalent source to represent each source in the calibrated measurement system. Such a source is called a hardware equivalent source and its properties are the *total excitation*, A_0, and physical reflection coefficient, Γ_{S0}. These properties are related to the Thévenin equivalent source through the following relationships:

$$A_0 = \frac{V_S}{2\sqrt{|\Re\{Z_0\}|}} \quad \text{and} \quad \Gamma_{S0} = \frac{Z_S - Z_0^*}{Z_S + Z_0}, \tag{6.1}$$

where Z_0 is the reference impedance of the system.

These properties are some of the most important to the presentation of network emulation and will come up later in this chapter. In Section 6.2.1 we briefly discuss some of the important details surrounding Γ_{S0}, and in Section 6.2.2 we cover the role of A_0 and how it is used in the measurement system.

6.2.1 The Physical Reflection Coefficient

Γ_{S0}, is the *physical* reflection coefficient of the measurement system[1] when viewed from the measurement plane. We assume that Γ_{S0} is known at the time of network emulation. A key assumption with the hardware equivalent source is that the transceiver may be approximated as

[1] This reflection coefficient is also called the passive reflection coefficient in other work, e.g. [163].

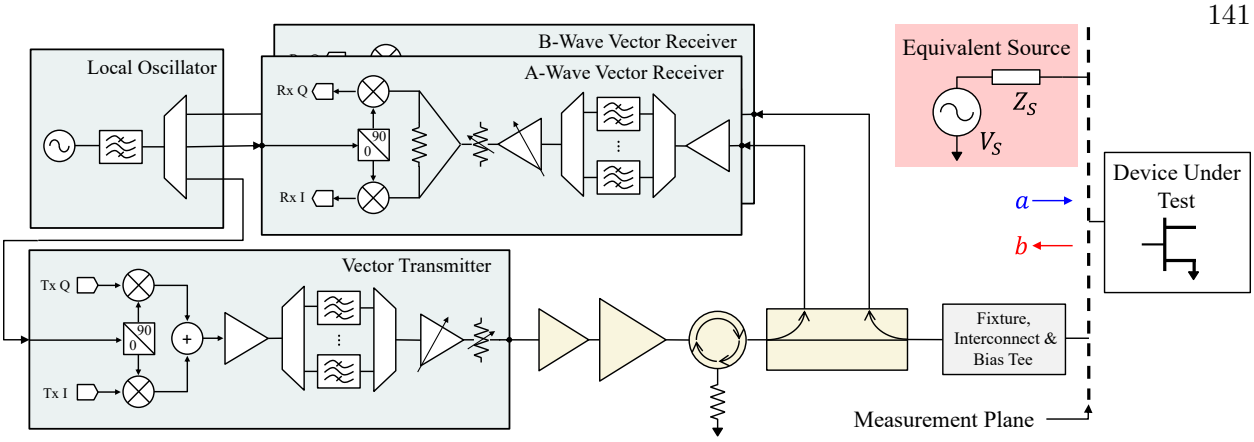


Figure 6.3: Block diagram illustrating a single equivalent source and the associated hardware used to implement it. Test bench hardware includes a vector signal transceiver (VST), driver amplifiers, isolator, couplers, and associated fixture and bias hardware. The measurement hardware is calibrated such that associated power waves are reported at the measurement plane illustrated.

a linear network. Part of this assumption is the idea that Γ_{S0} is only a function of frequency. Therefore a circulator is required to mitigate inadvertent load-modulation of the driver amplifiers, e.g. Fig. 6.3.

6.2.2 The Total Excitation

A_0 is the link between the equivalent source excitation and the transmitter excitation (Fig. 6.3). Its name comes from the observation that $A_0 = a$ when $Z_S = Z_0$ with a being the incident power wave [84]. When this condition is satisfied, the available source power $(P_{avs}) = |A_0|^2/2$. This property plays two important roles : 1) it is used to set the specific excitation required for network emulation, and 2) it is a reference that may be used for time alignment.

As suggested in Fig. 6.3, directly setting the appropriate source excitation would require thorough pre-characterization and full control of the transmit chain. Instead, this chapter uses a relative method for applying the correct excitation. To that effect, we need mechanisms for measuring the present A_0 and determining a relative correction to the transmitter's manipulable variable(s) (MV). Fig. 6.4 illustrates the process for updating A_0. In this implementation, the MVs are the transmit signal power level and the tone magnitudes and phases.

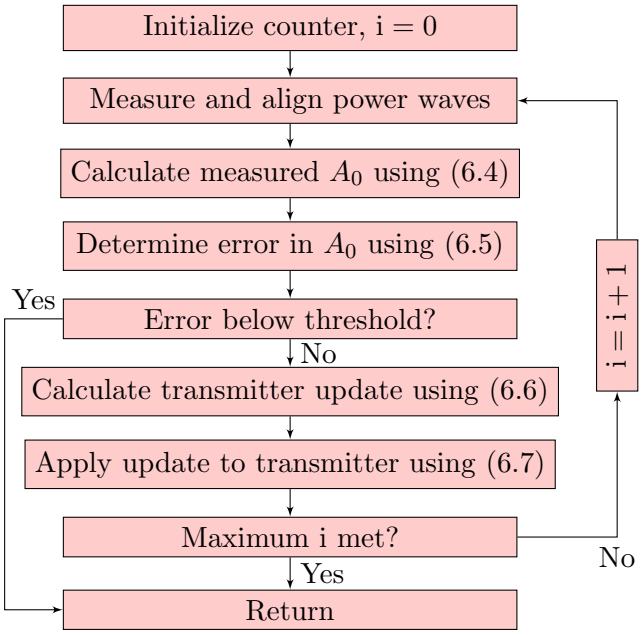


Figure 6.4: Block diagram used to update the transmitter from the hardware equivalent source model.

Measuring A_0 begins with the following boundary conditions used in S-parameter network analysis [164]:

$$a = a_s + b\Gamma_{S0}\,, \tag{6.2}$$

where a is the wave incident on the DUT from the source, wave reflected from the DUT back to the source, and a_s is the impressed a-wave from the equivalent source related to the source excitation, A_0, through the following relationship:

$$a_s = A_0\left(1 - \Gamma_{S0}\right)\,. \tag{6.3}$$

Substituting (6.3) into (6.2) and solving for A_0 yields its relationship to the *measured* a and b-waves:

$$A_0 = \frac{a - b\Gamma_{S0}}{1 - \Gamma_{S0}}\,. \tag{6.4}$$

Assuming A_0^d is the desired source excitation and A_0^m is the measured excitation the corresponding RMS error between the two is:

$$A_{0,error} = \sqrt{\frac{1}{N_{tones}}\sum_{n=1}^{N_{tones}}\left(A_0^m - A_0^d\right)^2} \tag{6.5}$$

where N_{tones} is the number of tones in the excitation. Using (6.4), the correction to the transmitter MVs in the signal's magnitude and phase is:

$$A_\Delta = \left| \frac{A_0^d}{A_0^m} \right| \quad \text{and} \quad \theta_\Delta = \arg\left(\frac{A_0^d}{A_0^m} \right), \tag{6.6}$$

where the updated values for the transmitter power are:

$$A_{n+1} = A_n A_\Delta \quad \text{and} \quad \theta_{n+1} = \theta_n + \theta_\Delta, \tag{6.7}$$

where $n+1$ designates the updated transmitter setting and n indicates the prior.

Relative updates to a transmitter's MVs also assumes that the receive waveforms are synchronous between measurements. This can be accomplished either with a common trigger between the transmitter and receiver systems, or by re-aligning the received waveforms to a common point in time between measurements [165]. The incident wave may be used as a reference for re-alignment, however; if $\Gamma_{S0} \neq 0$ then the measured incident wave is a function of the impressed, incident wave and the the reflected wave, i.e. the DUT's response. For this reason, we use A_0 as a reference for re-alignment as it is an excitation which, in a linear system, is physically independent from any of the reflected waves.

In the system described here, a specific source/transmitter is designated as the "reference" for re-alignment–meaning that the A_0 for that source is always used as the reference for waveform re-alignment. When the reference source has undergone an update since the last alignment, the measured A_0 is aligned to the source's expected A_0. When the reference source has not undergone an update, the measured A_0 is aligned to the previously measured A_0. Once the reference A_0 is aligned, the corresponding time-shift is applied to the other measured waves.

6.3 The Tuner Equivalent Source

With the interface to the hardware defined, the next question becomes exactly what A_0 to present to the DUT. This discussion begins with the reflection coefficient the network presents to the DUT. That brings us to the next level of abstraction: the tuner equivalent source.

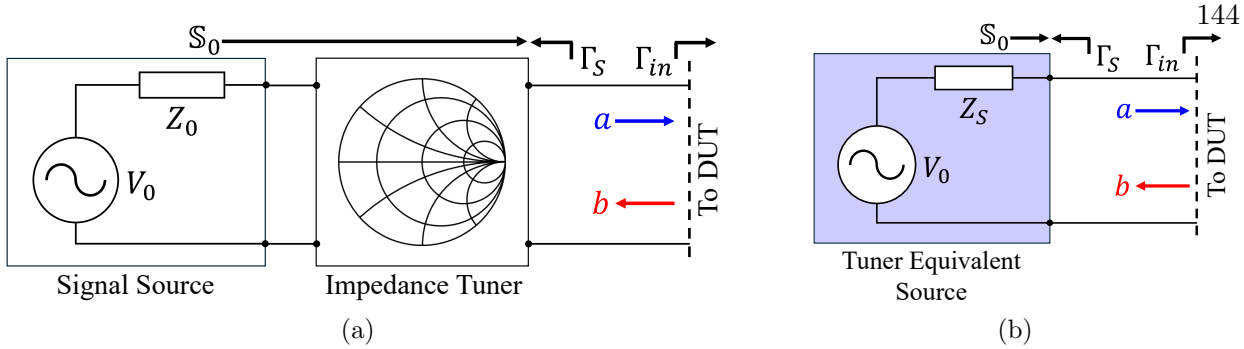


Figure 6.5: Introduction to the tuner equivalent source. We start with (a) a matched signal generator and tuner. We assert that the Thévenin equivalent (b) has the same excitation with an impedance, Z_t.

Fig. 6.5a illustrates an example of a tuner with a matched signal generator. The excitation of the system is what we call the signal excitation, $\mathbb{S}_0$. As the tuner is linear, we replace it with the tuner equivalent source illustrated in Fig. 6.5b which has an equivalent impedance Z_S that results in the same reflection coefficient as Fig. 6.5a.

This abstraction results in a new contribution to tuner theory which generalizes an approach to wide-band active load and source pull [166]. The theory is presented as follows:

- Section 6.3.1 derives generalized tuner theory by relating the tuner equivalent source to the hardware equivalent source from Section 6.2; and
- Section 6.3.2 demonstrates examples for wide-band active source and load-pull.

6.3.1 Generalized Tuner Theory

Fig. 6.6 illustrates block diagrams relating the properties of the tuner equivalent source and corresponding hardware equivalent source. The the power waves of Fig. 6.6a are related to the total excitation, A_0, through (6.4). This boundary condition may also be written in terms of Γ_{S0}:

$$\Gamma_{S0} = \frac{a - A_0}{b - A_0}, \tag{6.8}$$

which implies that Γ_{S0} is measurable even when its corresponding source is on, but only if its excitation is fully known. In its current form (6.8) is not particularly useful as Γ_{S0} is already

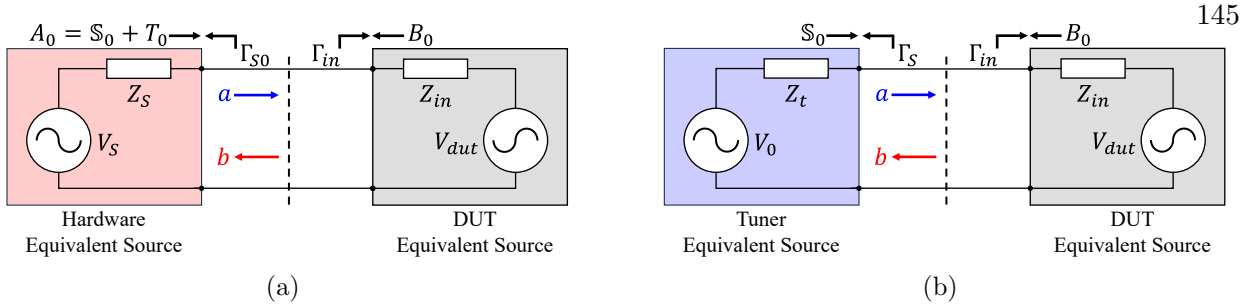


Figure 6.6: The (a) hardware equivalent source and (b) the corresponding tuner equivalent source. In both cases, the DUT is modeled as an equivalent source with an excitation B_0 and input reflection coefficient, Γ_{in}.

known. On the other hand, if we substitute the corresponding values from Fig. 6.6b into (6.8) we arrive at the following relationship between the tuner reflection coefficient and the signal excitation:

$$\Gamma_S = \frac{a - \mathbb{S}_0}{b - \mathbb{S}_0} \tag{6.9}$$

Applying (6.9) to the hardware equivalent source in Fig. 6.6a yields the effective Γ_S resulting from a tuner excitation, T_0, superimposed on the desired signal excitation, $\mathbb{S}_0$. This leads to the following definition for the total excitation:

$$A_0 = \mathbb{S}_0 + T_0 \tag{6.10}$$

At this level of abstraction, we assume that $\mathbb{S}_0$ is a *given* where:

- for source-pull: $\mathbb{S}_0$ represents the signal used to excite the DUT;
- for load-pull: $\mathbb{S}_0 = 0$; and
- for network emulation: $\mathbb{S}_0 = \mathbb{S}_{eq}$ (discussed in Sections 6.4 and 6.5).

Determining T_0 requires a complete set of boundary conditions. To do this, we utilize an equivalent source as a simple linear model for a port of the DUT, which is illustrated in Fig. 6.6. This equivalent source has an excitation, B_0, and reflection coefficient, Γ_{in} and is related to the corresponding Thévenin equivalent source through:

$$V_{\text{DUT}} = \frac{B_0}{2\sqrt{|\Re\{Z_0\}|}} \quad \text{and} \quad \Gamma_{in} = \frac{Z_{in} - Z_0^*}{Z_{in} + Z_0} \tag{6.11}$$

This source also has the following boundary condition:

$$B_0 = \frac{b - a\Gamma_{in}}{1 - \Gamma_{in}} \tag{6.12}$$

Boundary conditions (6.4) and (6.12) are used to solve the corresponding a and b-waves in Fig. 6.6a as:

$$\begin{aligned} a &= \frac{A_0\left(1 - \Gamma_{S0}\right) + B_0\Gamma_{S0}\left(1 - \Gamma_{in}\right)}{1 - \Gamma_{in}\Gamma_{S0}} \\ b &= \frac{A_0\Gamma_{in}\left(1 - \Gamma_{S0}\right) + B_0\left(1 - \Gamma_{in}\right)}{1 - \Gamma_{in}\Gamma_{S0}} \end{aligned} \tag{6.13}$$

Substituting the corresponding values from Fig. 6.6b into (6.13) yields:

$$\begin{aligned} a &= \frac{\mathbb{S}_0\left(1 - \Gamma_S\right) + B_0\Gamma_S\left(1 - \Gamma_{in}\right)}{1 - \Gamma_{in}\Gamma_S} \\ b &= \frac{\mathbb{S}_0\Gamma_{in}\left(1 - \Gamma_S\right) + B_0\left(1 - \Gamma_{in}\right)}{1 - \Gamma_{in}\Gamma_S} \end{aligned} \tag{6.14}$$

By expanding A_0 in (6.13) with (6.10) and equating the corresponding equations in (6.14) we solve for T_0:

$$T_0 = \left(B_0 - \mathbb{S}_0\right)\left(\frac{1 - \Gamma_{in}}{1 - \Gamma_S\Gamma_{in}}\right)\left(\frac{\Gamma_S - \Gamma_{S0}}{1 - \Gamma_{S0}}\right), \tag{6.15}$$

where T_0 is an *exact* solution that equates the system in Fig. 6.6a, i.e. the hardware equivalent source, to that of Fig. 6.6b, i.e. the tuner equivalent source, if all terms are precisely known. However, convergence is still achievable even if parameters like Γ_{in} are not fully known, such as when Γ_{in} is nonlinear. In such cases the iterative procedure illustrated in Fig. 6.7 with the RMS error in Γ_S defined as:

$$\Gamma_{s,error} = \sqrt{\frac{1}{N_{tones}}\sum_{n=1}^{N_{tones}}\left(\Gamma_S^m - \Gamma_S^d\right)^2}, \tag{6.16}$$

where Γ_S^m is the measured source reflection coefficient (6.9) and Γ_S^d is the desired tuner reflection coefficient. In summary, the result of the above convergent iterative algorithm is to arrive at a value of the tuner reflection coefficient that is used for network emulation. Appendix C discusses the criteria under which T_0 converges to the exact solution. Next Section 6.3.2 presents several validation cases of the generalized tuner for wide-band active load and source pull.

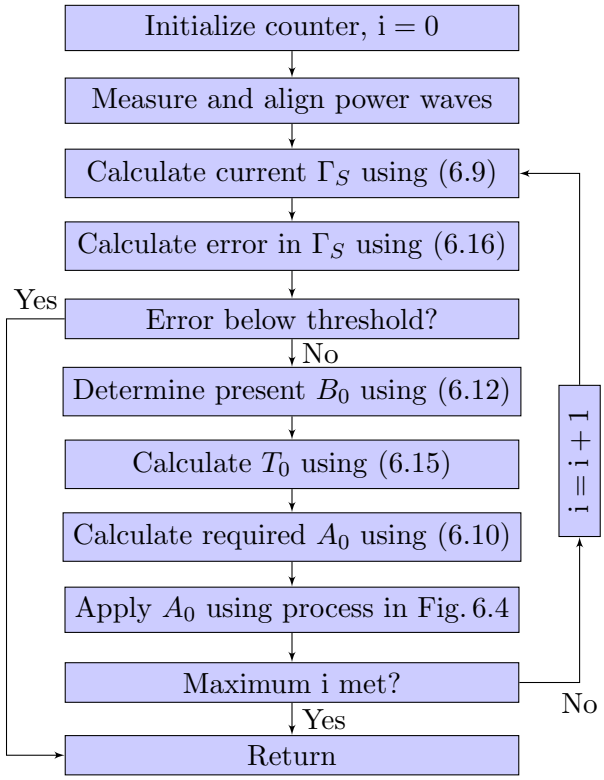


Figure 6.7: Block diagram for the generalized tuner by updating the transmitter from the tuner equivalent source model. Note that the hardware equivalent source model update procedure from Fig. 6.4 is embedded within this procedure.

6.3.2 Tuner Validation

Each validation example uses a source and load pull tuner to present impedances to a non-zero length *thru* standard. The source-pull tuner uses a 300 MHz, 300-tone signal excitation with a 6.5 dB peak to average power ratio (PAPR) and a peak available source power of 10 dBm.

6.3.2.1 Individual Load and Source Pull

The first validation case is to individually load and source pull a matched *thru*. Fig. 6.8a illustrates the constellation of reflection coefficients used by each tuner in this example. First, source pull is performed over the constellation illustrated in Fig. 6.8a while maintaining a $\Gamma_L = 0$. Next, load pull is performed over the same constellation while setting $\Gamma_S = 0$. The maximum reflection coefficient magnitude of the constellation is 0.9. Table 6.1 illustrates the maximum and

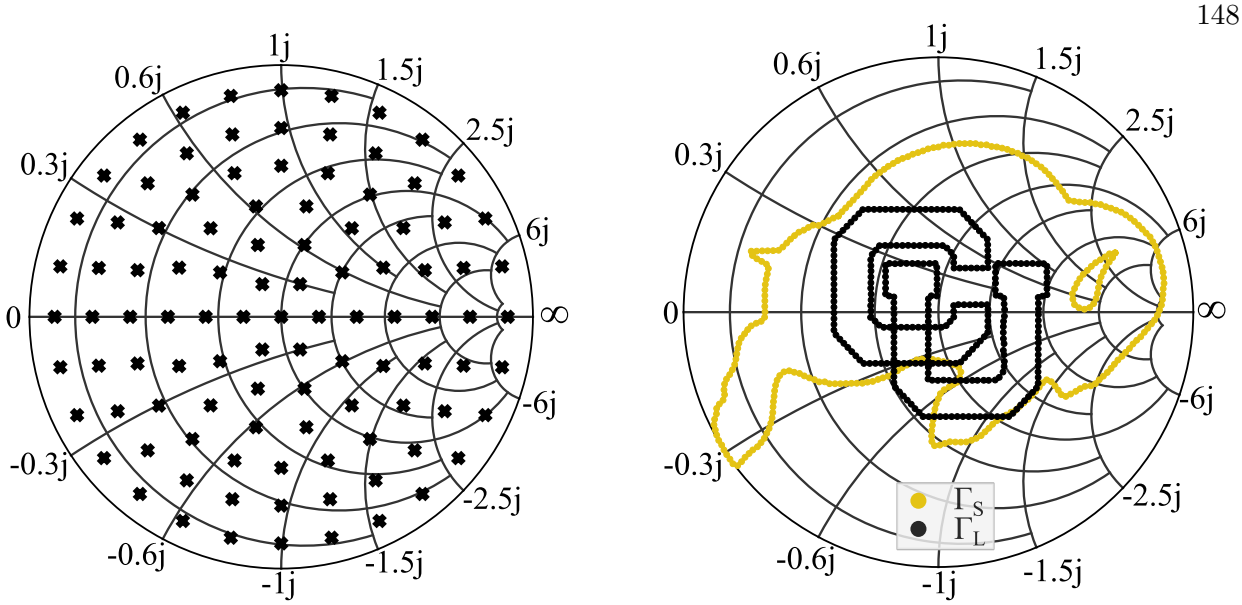


Figure 6.8: Validation cases for the generalized tuner method. (a) Single point gamma targets used for wide-band active load and source pull validation. (b) Measured simultaneous source, i.e. gold buffalo, and load pull, i.e. black "CU" logo, Γ trajectories measured on a *thru*. Each point corresponds to a single tone in a 300-tone signal.

average errors in reflection coefficient and transducer gain as defined in [90].

The measured transducer gain is calculated as:

$$\mathrm{G_{t,measured}} = \frac{P_{out}}{P_{avs}},$$

$$P_{out} = \frac{|b_2|^2 - |a_2|^2}{2Z_0} \quad \text{and} \quad P_{avs} = \frac{|\mathbb{S}_0|^2}{2}\frac{|1-\Gamma_S|^2}{1-|\Gamma_S|^2},$$

where Γ_S is measured using (6.9).

Table 6.1: Results of Source and Load Pull

	Err. Γ (dB)			Err. Gain (dB)		
	Min	Mean	Max	Min	Mean	Max
Source Pull	-30.9	-23.8	-20.4	-28.3	-24.1	-16.6
Load Pull	-34.3	-26.8	-21.7	-28.5	-24.2	-19.5

Error in reflection coefficient and transducer of the single point constellation load and source pull. The tuner convergence threshold is set to -20 dB for expediency.

6.3.2.2 Arbitrary Simultaneous Load and Source Pull

The second validation case demonstrates *simultaneous* wide-band active load and source pull validation on a *thru*. The final, measured reflection coefficients are plotted in Fig. 6.8b. The yellow buffalo trace is the source impedance trajectory and the black, "CU" logo is the final the load impedance trajectory. Each point in the trajectories presented here is a tone in the wide-band signal, and both trajectories are presented simultaneously. The final root-mean-square (RMS) error in source and load reflection coefficient are -29.9 dB and 31.2 dB, respectively. This demonstrates the efficacy of this approach to simultaneous and wideband active load and source-pull for arbitrary impedance trajectories.

6.4 Equivalent Source Method for 2-Port Network Emulation

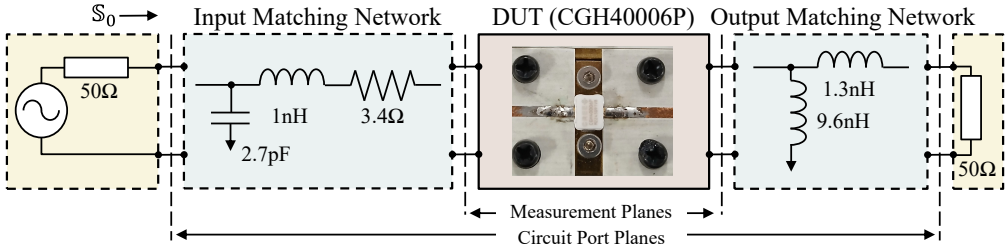


Figure 6.9: Circuit used to demonstrate small-signal two-port network emulation from 2.1–2.4 GHz with a MACOM CGH40006P packaged GaN HEMT. The lumped-element matching circuits are used to compare emulation and simulation in a straightforward manner.

We begin the discussion of network emulation with the example circuit shown in Fig. 6.9, with two sets of reference planes:

(1) **Measurement planes**, which are the *physical* locations where power waves are observed on the device under test (DUT); and

(2) **Circuit-port planes**, which are the *virtual* planes where boundary conditions—such as excitations and loads—are applied.

Modulated load-pull techniques, including the tuner equivalent source method from Sec-

tion 6.3 and other active load-pull approaches such as [167], enable the presentation of arbitrary impedance trajectories over a wide instantaneous bandwidth. In the case presented here, the trajectories include the matching networks together with possible dispersion, loss and coupling associated with these networks.

Techniques such as the one in [167] focus only on the power waves at the load measurement plane. Extending active load-pull to hardware-in-the-loop design requires that: (1) circuit performance metrics are evaluated at the circuit-port planes where they are relevant, rather than the measurement planes; and (2) excitations are transformed through the matching network to include dispersion and loss at the DUT reference plane.

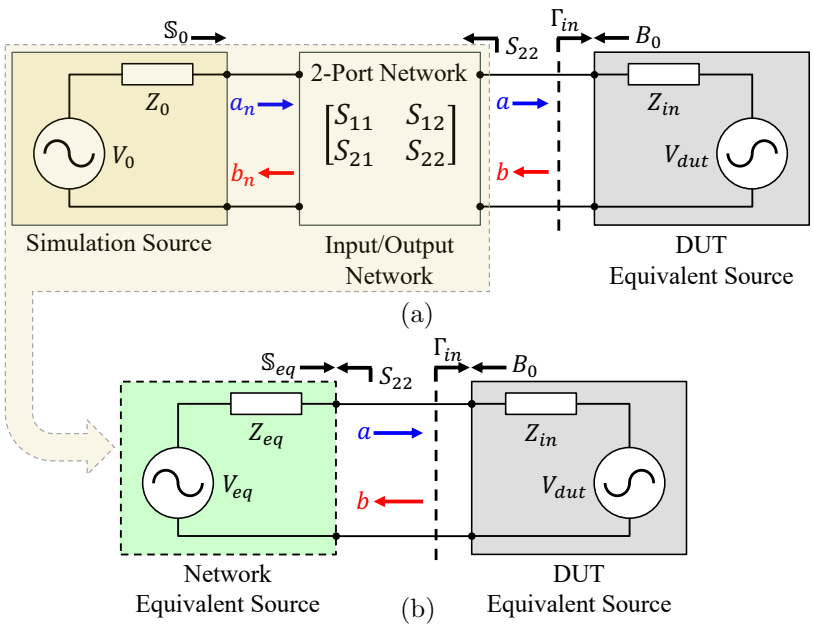


Figure 6.10: A (a) 2-port network and (b) its equivalent source.

To satisfy these requirements, the abstraction necessary for network emulation is the network equivalent source which we introduce here in the context of a 2-port network and a corresponding simulation source, e.g. Fig. 6.10a. The linear network is modeled by a S-parameter matrix with its second port connected to the DUT.[2]

[2] Note that the simulation source of Fig. 6.10a is assumed to be matched, i.e. $Z_s = Z_0$ and therefore the reflection coefficient of the network equivalent source is s_{22} of the network. The next section discusses a general approach simulation source is not matched for a general network. Alternatively, for a single two-port network, s_{22} may be

In Section 6.3 we indicated that $\mathbb{S}_0$ at the tuner abstraction level becomes $\mathbb{S}_{eq}$. From Thévenin's Theorem, $\mathbb{S}_{eq}$ is the open-circuit excitation:

$$\mathbb{S}_{eq} = \frac{\mathbb{S}_0}{1 - s_{22}}, \tag{6.17}$$

assuming that port 2 of the network is at the DUT. The corresponding total excitation becomes:

$$A_0 = \mathbb{S}_{eq} + T_0, \tag{6.18}$$

where T_0 is the tuner excitation corresponding to $\Gamma_S = s_{22}$.

Once the total excitation is set, the corresponding power waves at the circuit port plane (Fig. 6.10a), a_n and b_n are:

$$a_n = \frac{a - bs_{22}}{s_{21}} \quad \text{and} \quad b_n = \frac{as_{11} - b\Delta}{s_{21}},$$

where $\Delta = s_{11}s_{22} - s_{21}s_{12}$.

To validate this method, Fig. 6.11 compares the s_{11} and s_{21} parameters obtained from simulation and emulation for the circuit shown in Fig. 6.9. This small-signal comparison serves as a valuable demonstration that the responses of the emulated and simulated circuits are virtually identical with a peak relative error in s_{21} and s_{11} of 1.6% and 8.2%, respectively, thereby validating the effectiveness of the method in small-signal. However, this 2-port approach is incapable of handling more complicated behaviors such as feedback and coupling between networks. Section 6.5 addresses these limitations by expanding this approach to generalized N-port networks with coupling.

6.5 Equivalent Source Method for N-Port Network Emulation

Fig. 6.12 shows the two equivalent networks discussed in this section. Fig. 6.12a illustrates a block diagram of the circuit under analysis. In this figure, there are two port groups: *external* and *internal*. The external ports, $P_{e,k}|_{k\in[1,2,\ldots,N]}$, are where the signal excitation(s), $\mathbb{S}_{0,i}$, and load impedance(s), $Z_{S,i}$, are presented to the circuit. These ports define the electrical interface to the rest of the system and therefore all relevant performance metrics are evaluated at this plane. The

replaced by the output reflection coefficient, Γ_{out}, as described in [90, p.560].

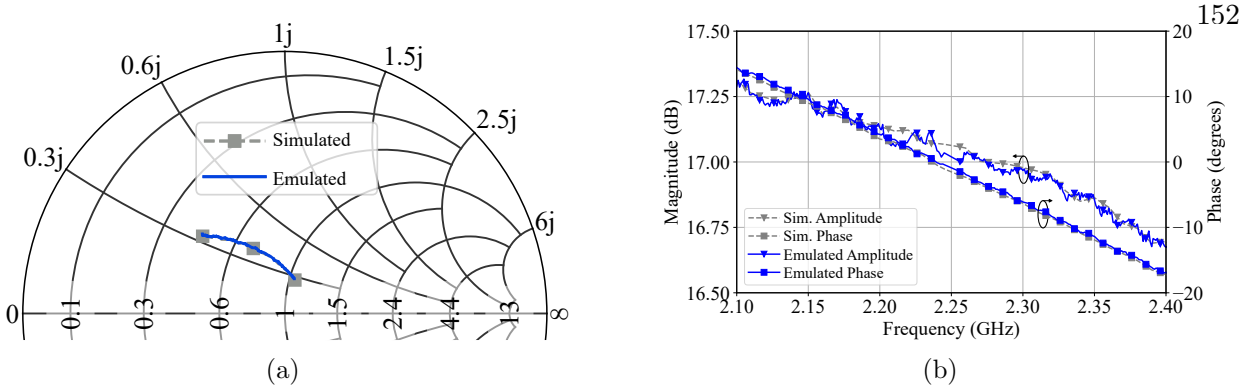


Figure 6.11: Comparison of the (a) s_{11} and (b) s_{21} simulation and emulation results of the circuit illustrated in Fig. 6.9.

active device is connected to the internal ports, $P_{i,k}|_{k\in[1,2,\ldots,M]}$, where the physical a and b waves are observed in measurement. In Fig. 6.12a the sources on the external ports and the passive network are virtual, i.e. they only exist in simulation while the active device and hardware equivalent sources on the measurement plane in Fig. 6.12b are physical.

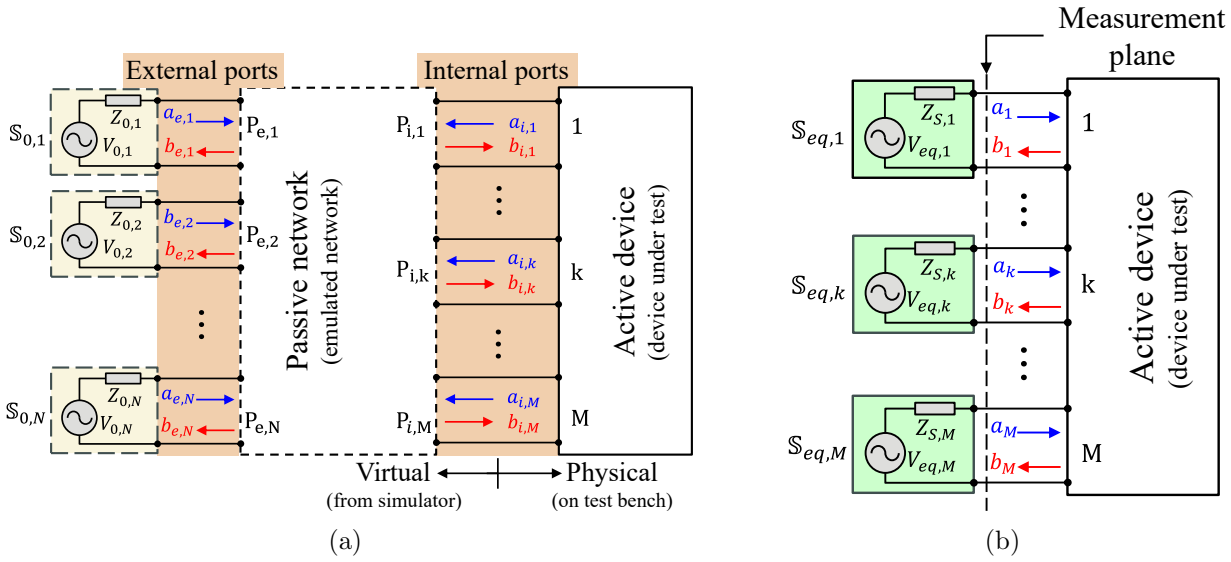


Figure 6.12: Conceptual circuits used in the network emulation process. (a) Setup of the problem with a passive network and circuit excitations where the sources and network are virtual and the active device is physical. (b) The passive networks and sources from (a) are replaced with Thévenin equivalent sources. Note that the orientation of the a and b waves are aligned to the passive networks in (a) and to the active device in (b).

Fig. 6.12b illustrates the electrical equivalent to Fig.6.12a with respect to the internal port plane. In this figure, the sources and passive network are replaced with the network equivalent sources that drive the emulation process. The derivation of these sources and their application towards network emulation is presented as follows:

- Section 6.5.1 presents the simulation sources and N-port network definition;
- Section 6.5.2 describes the three port coupling mechanisms under consideration;
- Section 6.5.3 derives the generalized network equivalent source; and
- Section 6.5.4 walks through the procedural aspects of network emulation.

6.5.1 Simulation Sources and N-Port Network Definition

The simulator sources, i.e the sources located at the external port plane of Fig. 6.12a, form the boundary conditions for the nonlinear circuit analysis problem. These sources consist of a signal excitation, $\mathbb{S}_{0,k}$, and a port impedance $Z_{S,k}$. The passive network is described with a $(N+M) \times (N+M)$ S-parameter matrix, where N and M are the numbers of *external* and *internal* ports, respectively. In this work, this scattering matrix is represented with four S-parameter sub-matrices:

$$S = \begin{bmatrix} S^{ee} & S^{ei} \\ S^{ie} & S^{ii} \end{bmatrix}, \tag{6.19}$$

where S^{ee} is a $N \times N$ matrix describing the network coupling between external ports, S^{ei} is a $N \times M$ matrix describing the network couplings from internal ports to external ports, S^{ie} is a $M \times N$ matrix describing the network coupling from external ports to internal ports, and S^{ii} is a $M \times M$ matrix describing the network coupling between internal ports. For example, a 4-port network where ports

1 and 2 are external ports and ports 3 and 4 are internal ports has the corresponding sub-matrices:

$$S^{ee} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}, \quad S^{ei} = \begin{bmatrix} s_{13} & s_{14} \\ s_{23} & s_{24} \end{bmatrix},$$
$$S^{ie} = \begin{bmatrix} s_{31} & s_{32} \\ s_{41} & s_{42} \end{bmatrix}, \quad S^{ii} = \begin{bmatrix} s_{33} & s_{34} \\ s_{43} & s_{44} \end{bmatrix}.$$

The S-parameters in (6.19) are generalized so that the reference impedances of the external ports are equal to the corresponding $Z_{S,k}$, while the reference impedance of all internal ports is equal to that of the measurement system, e.g. $50\,\Omega$. The generalized S-parameters can be found from [168], and ensure that $a_{e,k} = \mathbb{S}_{0,k}$ given $k \in [1, 2, ..., N]$ for the external ports, as discussed in the next section.

6.5.2 Port Coupling

Fig. 6.13 illustrates the primary internal-port coupling paths: (a) external to internal ports via the passive network; (b) internal to internal ports via the passive network; and (c) internal to internal ports via the active device under test. The equivalent source representation of the passive network will handle cases (a) and (b) directly. Case (c) is handled implicitly during the implementation of the tuner equivalent source, i.e. as $B_{0,k}$.

From (6.19) the b-waves of all ports are:

$$\begin{bmatrix} b_e \\ b_i \end{bmatrix} = \begin{bmatrix} S^{ee} & S^{ei} \\ S^{ie} & S^{ii} \end{bmatrix} \begin{bmatrix} a_e \\ a_i \end{bmatrix}, \tag{6.20}$$

where a_e and b_e are an N-element column vectors representing the a and b waves at the external ports. Likewise a_i and b_i are M-element column vectors of internal a and b-waves, respectively. From (6.20), the k^{th} internal port ($P_{i,k}$) power wave, $b_{i,k}$, is realized as:

$$b_{i,k} = \sum_{x=1}^{N} a_{e,x} s_{kx}^{ie} + \sum_{x=1, x\neq k}^{M} a_{i,x} s_{kx}^{ii},$$

where s^{ii}_{kk} is the k^{th} element of the passive network's internal port S-parameters, s^{ii}. Because the passive network from Fig. 6.12a is represented by generalized S-parameters this equation becomes

$$b_{i,k} = \sum_{x=1}^{N} \mathbb{S}_{0,x} s^{ie}_{kx} + \sum_{x=1, x\neq k}^{M} a_{i,x} s^{ii}_{kx} \,. \tag{6.21}$$

Equation (6.21) shows that the b-waves at each internal port depend on the a-waves at all other internal ports. This implies that an iterative approach is required to achieve the proper $\mathbb{S}_{eq}$ which satisfies (6.21). This approach is outlined in Sections 6.5.3 and 6.5.4. The error in the internal port powers is defined here as the difference between the computed ($b^{calc}_{i,k}$) (6.20) and measured ($b^{meas}_{i,k}$) waves:

$$\text{Error} = \sqrt{\frac{1}{M} \sum_{k=1}^{M} \left| b^{meas}_{i,k} - b^{calc}_{i,k} \right|^2}, \tag{6.22}$$

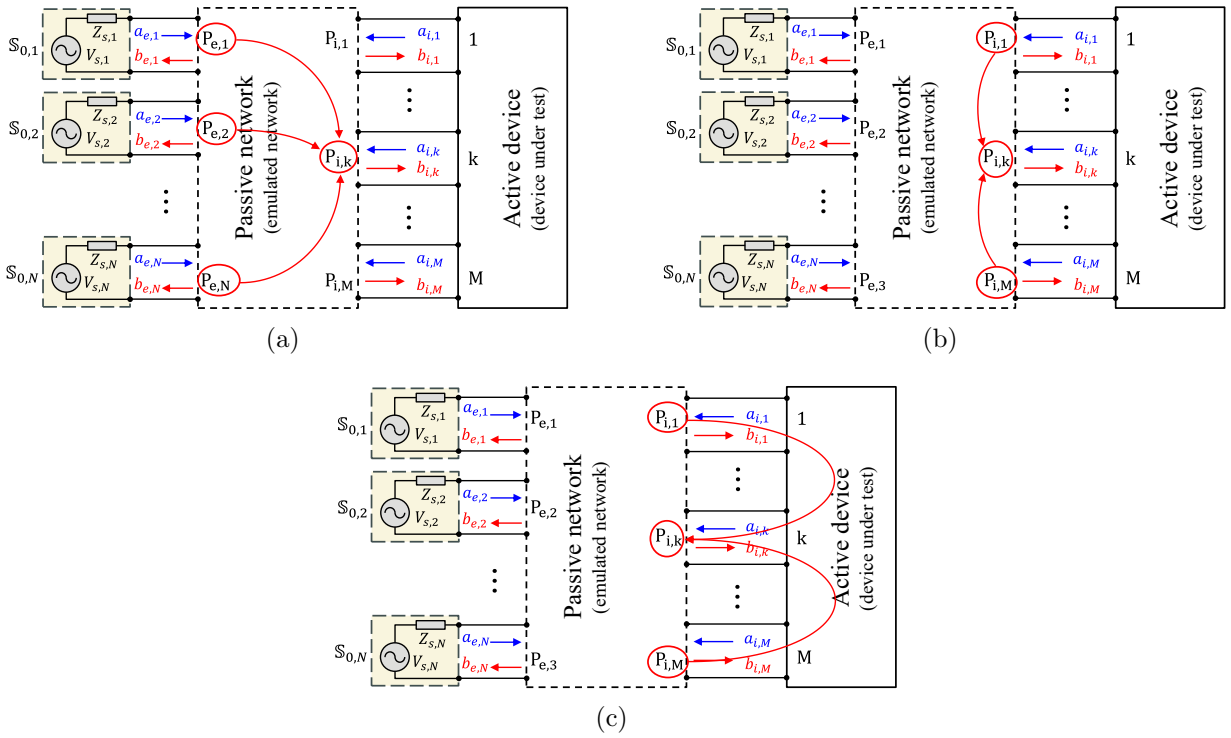


Figure 6.13: The three coupling paths to port $N + x$ of the emulated network: (a) from external ports through the network, (b) from internal ports through the network and (c) from internal ports through the DUT.

which defines the total error associated with network emulation internal port coupling[3] .

6.5.3 Generalized Network Equivalent Source

With the port coupling behavior defined, we now present the generalized network equivalent source definition. As was the case for the external port sources, each equivalent source has an equivalent excitation, $\mathbb{S}_{eq,k}$, and port impedance, $Z_{eq,k}$, where $k \in [1, 2, ..., M]$. The equivalent source impedance, $Z_{eq,k}$, is simply the open-circuit impedance:

$$Z_{eq,k} = Z_0 \frac{1 + s^{ii}_{kk}}{1 - s^{ii}_{kk}}, \tag{6.23}$$

Where each equivalent source is coupled.

Referring to the k^{th} port of Fig. 6.12b, the equivalent source excitation is:

$$\mathbb{S}_{eq,k} = \frac{b_{i,k}}{1 - s^{ii}_{kk}}$$

Substituting (6.21) for $b_{i,k}$ results in:

$$\mathbb{S}_{eq,k} = \frac{\sum_{x=1}^{N} \mathbb{S}_{0,x} s^{ie}_{kx} + \sum_{x=1,x\neq k}^{M} a_{i,x} s^{ii}_{kx}}{1 - s^{ii}_{kk}} \tag{6.24}$$

This excitation can be split between components belonging to external port excitations and internal port excitations:

$$\mathbb{S}_{eq,k} = \mathbb{S}^{e}_{eq,k} + \mathbb{S}^{i}_{eq,k}, \tag{6.25}$$

Where $\mathbb{S}^{e}_{eq,k}$ is the equivalent port excitation due to the sources at the external plane in Fig. 6.12a and $\mathbb{S}^{i}_{eq,k}$ is the equivalent port excitation due to the adjacent internal sources, i.e. feedback at adjacent internal ports from the device under test. Inferring from (6.24) these excitations are:

$$\mathbb{S}^{e}_{eq,k} = \frac{1}{1 - s^{ii}_{kk}} \sum_{x=1}^{N} \mathbb{S}_{0,x} s^{ie}_{kx} \tag{6.26}$$

$$\mathbb{S}^{i}_{eq,k} = \frac{1}{1 - s^{ii}_{kk}} \sum_{x=1,x\neq k}^{M} a_{i,x} s^{ii}_{kx} \tag{6.27}$$

[3] To keep the notation of (6.22) simple, we take the RMS of the error over each port of the network. In practice, the average should be applied over frequency as well with $M \to M \times N_{tones}$.

The reason for distinguishing (6.26) and (6.27) from (6.24) is that (6.26) only needs to be updated when the external source excitations or the passive network changes and (6.27) requires updating after each measurement. The process entailed for these updates will become clear in the next section.

6.5.4 Network Emulation Procedure

With the network equivalent sources defined, we proceed to the discussion of the network emulation procedure. Before the process can begin, the emulator requires an S-parameter definition of the network, a designation of the internal and external ports, and the simulation source configuration, i.e. signal excitation and port impedance. A tuner is assigned to each internal port.

Once initialized, the emulator begins the process outlined in Fig. 6.14. The tuners on each internal port are assigned a reflection coefficient and external excitations are generated from the provided simulation source information. The process begins by assuming all internal ports are decoupled, i.e. $\mathbb{S}^i_{eq,k} = 0$. This information is sent to the tuner, which determines the excitation T_0 required to generate the reflection coefficient at each port. Each internal port tuner is sequentially and iteratively updated until the desired reflection coefficients are obtained according to (6.16).

When complete, the port coupling error (6.22) is evaluated. If the coupling error is below the specified threshold, e.g. -20 dB, the process is assumed to be complete and the emulator returns. If the threshold is not satisfied, the excitations associated with the internal port coupling are updated, i.e. (6.27), and the total equivalent excitation is recomputed for each port. The emulator then updates the tuners again and returns to the task of iteratively updating each tuner. The process of updating $\mathbb{S}_{eq}$ and resetting the tuners to the desired Γ_S continues until either the emulator runs out of iterations or the convergence error criteria falls below the specified threshold.

Network emulation requires the existence of finite, simultaneous solutions for all $\mathbb{S}_{eq}$. This implies that in-band circuit stability is a necessary requirement emulation. A useful auxiliary test is to check if iteratively updating $\mathbb{S}_{eq,i}$ at internal port P_i converges when all other $\mathbb{S}_{eq,k}|_{k\neq i}$ remain constant. For example, if the DUT is a linear two-port, this test results in the following criteria for

convergence:

$$\left|\frac{1-s_{d,11}\Gamma_{S1}-s_{d,22}\Gamma_{S2}+\Delta_d\Gamma_{S1}\Gamma_{S2}}{s^{ii}_{12}s_{d,21}}\right|>1 \text{ and} \tag{6.28a}$$

$$\left|\frac{1-s_{d,11}\Gamma_{S1}-s_{d,22}\Gamma_{S2}+\Delta_d\Gamma_{S1}\Gamma_{S2}}{s^{ii}_{21}s_{d,12}}\right|>1\ , \tag{6.28b}$$

where (6.28a) and (6.28b) are the convergence criteria for $\mathbb{S}_{eq,1}$ and $\mathbb{S}_{eq,2}$, respectively. The S_d-parameters are those of the DUT, Δ_d is the corresponding determinant of the S_d, and S^{ii} are the internal port S-parameters (6.19) of the emulated network. Likewise Γ_{S1} and Γ_{S2} are the reflection coefficients presented to ports 1 and 2 of the DUT, respectively, and given by $\Gamma_{Sk}=s^{ii}_{kk}$ as indicated in (6.23). These criteria bear some resemblance to the Rollet condition [169], or K-factor, which further indicates the importance of circuit stability to emulation. Though (6.28) is not a completely sufficient condition for convergence, we have found it useful for predicting emulator convergence issues for many situations–even if the DUT is nonlinear two-port.

6.6 Demonstration of Network Emulation

The network emulation method is demonstrated on a Large-Signal Network Analyzer (LSNA) designed in our lab. In principle, any active load/source pull system can support this concept, provided the software can implement the algorithms described above.

6.6.1 Test Bench

The setup consists of 4 NI 5840 VSTs, which provide the 4 receivers for measuring 2-port a, b waves at the fundamental frequency. Two of the VST RF sources are used to provide the necessary excitations at P_1 and P_2 of the DUT, Fig. 6.15. The local oscillators (LOs) are daisy-chained separately for the VST sources and for the receivers, giving each group a shared LO. A pre-characterization step ensures synchronization within each group. As noted in [170], phase-locked sources are required for WALP. The sources and receivers are each synchronous, but the TX and RX LOs are independent. Therefore, A_0 is used as a fixed reference to align the measured a, b waves and enable relative source updates.

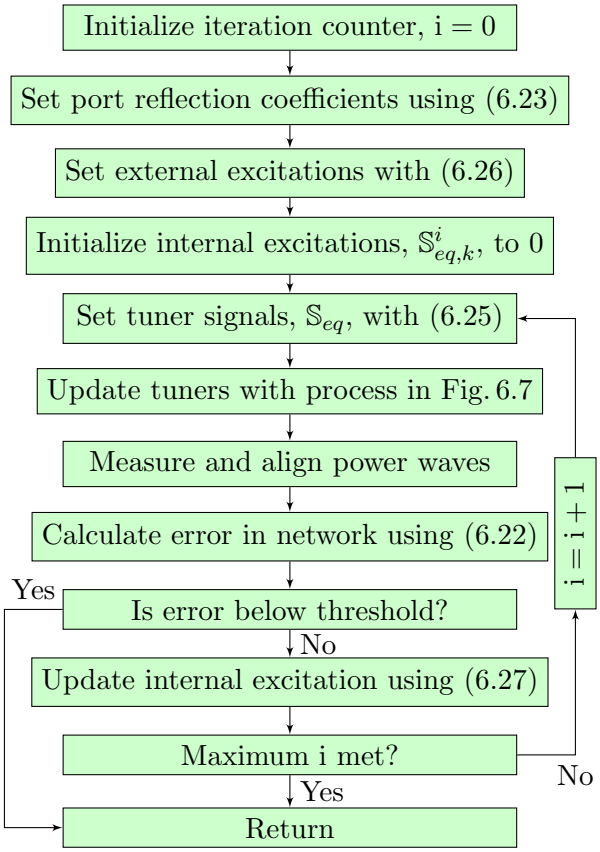


Figure 6.14: Block diagram for network emulation by updating the transmitter from with the network equivalent source model. Note that the tuner equivalent source model update procedure from Fig. 6.7 is embedded within this procedure.

AR 60S1G3 60 W amplifiers with ~ 50 dB of gain are used as drivers for P_1 and P_2. Four directional couplers sample the a, b waves, and a circulator is placed after each driver to maintain a constant Γ_{S0} and avoid inadvertently load-pulling the driver amplifiers. A spectrum analyzer is connected to the 3rd port of the P_2 circulator to provide a visual (uncalibrated) verification of the DUTs b_2 behavior. A coaxial SOLT calibration of the system is performed at $f_0 = 2.25$ GHz, over the VSTs 1 GHz instantaneous bandwidth. Additional absolute amplitude and an absolute phase calibrations are performed, using an external power meter and one of the unused VST sources outputting a 1 GHz impulse as an assumed ideal comb-generator for the respective calibrations.

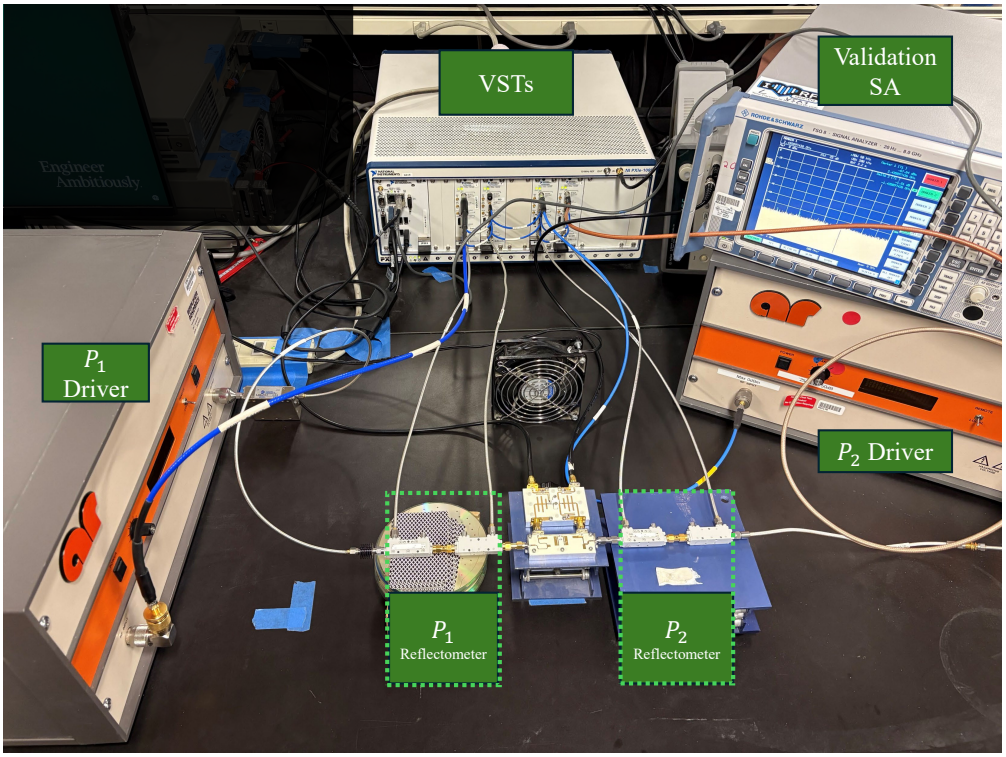


Figure 6.15: Photo of the measurement system used to perform network emulation.

6.6.2 Circuit Design

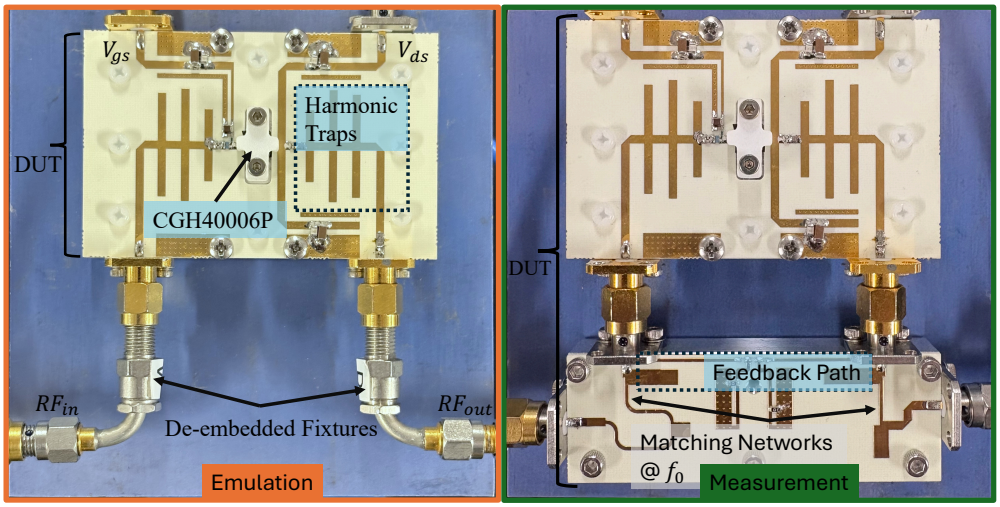


Figure 6.16: The DUT along with de-embedded fixtures (emulation case) and the physical matching network (measurement case), providing the two cases for validating the network emulation approach.

The circuit shown in Fig. 6.16 is an example device under test (DUT) designed to demonstrate large signal microwave network emulation. The DUT has a MACOM CGH40006P GAN HEMT transistor, quarter-wavelength bias network, and open-circuit trapping networks for the second and third harmonics. In large signal, nonlinear device behavior depends on the impedances presented at baseband and harmonic frequencies; however, the present system does not have enough VSTs to perform emulation at these frequencies. Therefore, bias and harmonic terminations are integrated into the DUT circuit so that both emulation and measurement test cases are impacted by the impedances and excitations provided at the fundamental frequencies. With more VSTs, the capability could be extended [171].

The network to be emulated, shown in Fig. 6.16, consists of two transmission-line matching networks with a high-pass resistive feedback path that is purposely designed to introduce between -34 to -28 dB of coupling. The rationale for including the high-pass network is to attenuate low-frequency out-of-band coupling while setting the in-band coupling as high as possible, while keeping the DUT stable. After assembly, the matching network and the 90° hardline bends are measured on a Agilent E8463C PNA with 4-port test set and phase-stable RF cables to obtain the S-parameters. A high degree of accuracy is required in these measurements, as any error will result in disagreement between the measured and emulated circuit responses. These S-parameters are used in the emulation case to obtain the results detailed below.

6.6.3 Procedure

To test the accuracy of the proposed emulation algorithm, an available source power sweep is applied to the circuit of Fig. 6.16. The signal used to excite the circuit is the 309 MHz, 300-tone signal used in the two-port circuit example of Section 6.4. The PAPR of the signal is 6.5 dB and the average available source power is swept from -6.5 to 23.5 dBm. Measurement is performed first with the physical matching network attached to the DUT. Wideband active source and load pull are used to minimize mismatch from the system and perform source leveling during measurement.

Following measurement, the physical network is removed from the DUT and the hardline

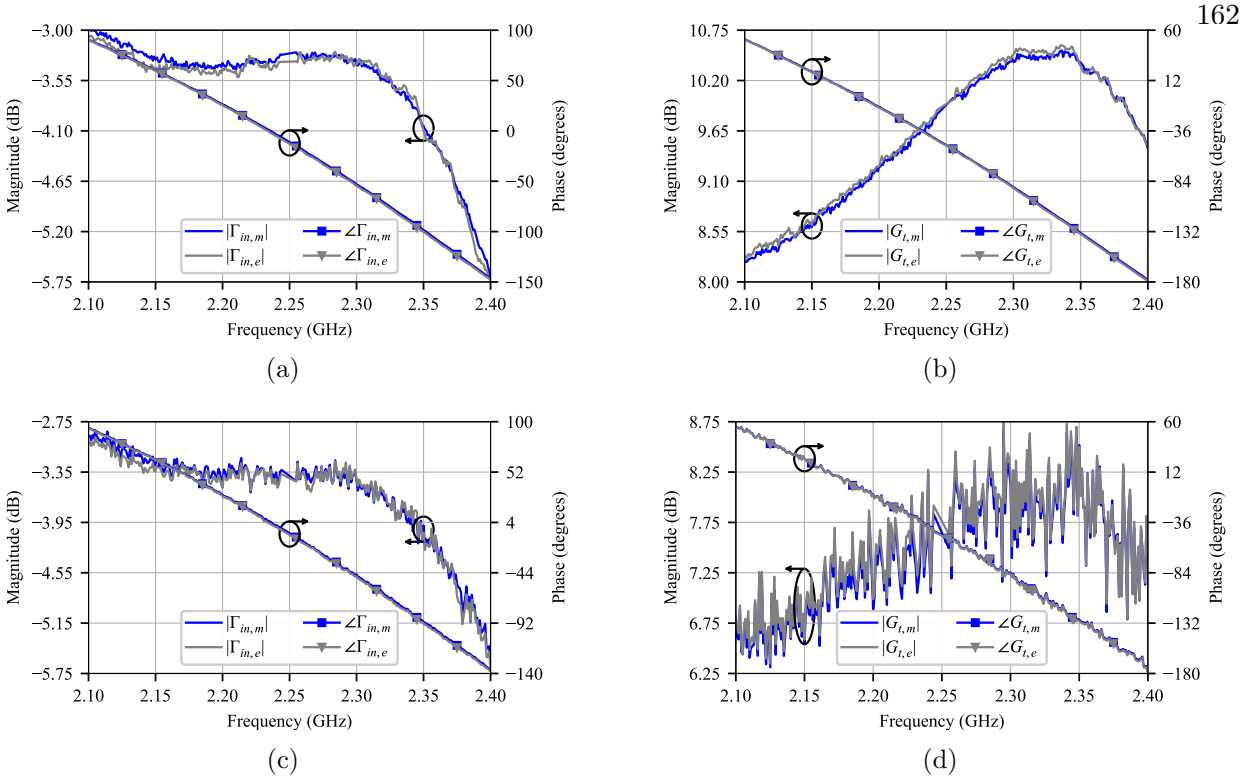


Figure 6.17: Comparison of the observed s_{11} and s_{21} versus frequency during emulation and measurement. (a) and (b) reflects the behavior in small-signal ($P_{avs} = -6.5\,\text{dBm}$) while (c) and (d) reflect the behavior of the circuit in large signal ($P_{avs} = 23.5\,\text{dBm}$).

bend fixtures are connected to the DUT. The fixture S-parameters are provided to the measurement system for in-situ de-embedding. Then the network S-parameters are loaded into the emulator and the associated external and internal port assignments are established. External ports are assigned to a network port index, signal excitation, $\mathbb{S}_0$, and impedance, Z_0. The RF input external port is loaded with the signal from the measurement test while the RF output external port is loaded with a null signal, i.e. $\mathbb{S}_0 = 0$. The internal ports are assigned to a network port index and tuner equivalent source instance. Once initialized, the network is emulated on the DUT using the procedure outlined in Fig. 6.14. Between emulations, the available source power of external port one is iteratively updated from -6.5 to 23.5 dBm.

6.6.4 Results

Fig. 6.17 compares the measured and emulated behavior of the circuit across frequency for average available source powers of -6.5 and 23.5 dBm. Figs. 6.17a and 6.17c illustrate the input reflection coefficients of the circuit with maximum relative errors of 4% and 4.2%, respectively. Likewise, Figs.6.17b and 6.17d compare the transducer gain with corresponding maximum relative errors of 3% and 2.9%, respectively. These traces correspond to the instantaneous response of the circuit over the entire signal excitation. The noisy appearance of the gain magnitude in Fig. 6.17d is due to in-band inter-modulation products.

Fig. 6.18 reports circuit performance of the emulated and measured results for the the power sweep. Table 6.2 summarizes the bounds on the relative and absolute errors between emulation and measurement. Fig. 6.18a reports the DC power consumption of the DUT during emulation and measurement. The corresponding variation in drain current is less than 1 mA at all power levels. Fig. 6.18b-6.18d report the efficiency, transducer gain, and adjacent channel power ratio (ACPR).

Table 6.2: Error between emulation and measurement in power sweep.

Measurement (unit)	Absolute (unit)		Relative (%)	
	min	max	min	max
Drain Current (mA)	0.15	0.89	0.25	0.72
DC Power (mW)	3.52	24.92	0.20	0.72
Gain (dB)	0.02	0.12	0.23	1.47
Delivered Power (dBm)	0.02	0.12[1]	0.12	1.33
PAE (%)	0.00	0.42[2]	0.11	2.84
Drain Efficiency (%)	0.00	0.40[2]	0.06	2.36
Lower ACPR (dBc)	0.07	1.70[1]	0.17	3.04
Upper ACPR (dBc)	0.30	1.93[1]	0.51	6.38

[1] dB [2] pp All entries rounded to two decimal places.

6.7 Discussion and Conclusions

This work presents an approach to emulating high-frequency networks as an alternative path to circuit analysis. The procedure for microwave network emulation used here uses three nested

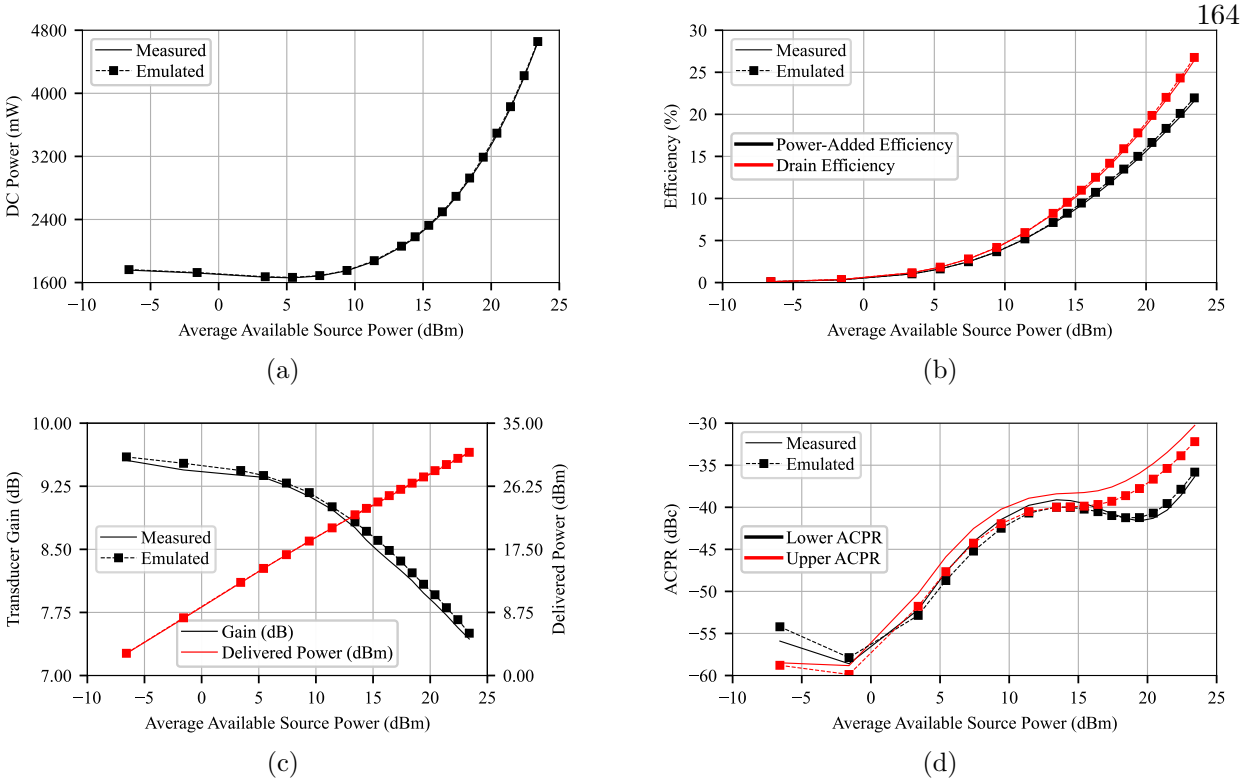


Figure 6.18: Comparison of the device under test under measurement and emulation for (a) dc power, (b) DE and PAE, (c) Gain and Delivered Power, and (d) ACPR. The results demonstrate excellent agreement backed off, at the compression corner, and in heavy compression.

equivalent source models: the hardware equivalent source, the tuner equivalent source, and the network equivalent source. The hardware equivalent source is the fundamental model used to simplify a complex measurement system into an elementary Thévenin source of two parameters, Z_S and V_s. These properties are related to Kurokawa's power waves through the total excitation, A_0, and physical reflection coefficient, Γ_{S0}. The tuner equivalent source, determines an appropriate value for A_0 which results in the same power waves as an equivalent system with excitation $\mathbb{S}_0$ and physical reflection coefficient, Γ_S. Finally, the network equivalent source determines what the excitation $\mathbb{S}_0$ should be in the tuner equivalent source if the system is replicating physical network behaviors such as coupling, loss, and dispersion.

Both small and large signal examples are provided to demonstrate the viability of the approach. First, a simple demonstration comparing emulator performance against small signal simu-

lations of a single-stage amplifier with lossy and dispersive networks over a 300 MHz instantaneous bandwidth is shown. The relative error is less than 9% for both S_{11} and S_{21} across the bandwidth of analysis.

A second, large-signal, demonstration is also presented which compares emulated results to measured results over the same 300 MHz bandwidth. To accommodate for limited test and measurement hardware, baseband and harmonic traps are used to ensure that the corresponding terminations do not change between the measurement and emulated test conditions. The emulated network is a matching network with a feedback network to demonstrate the procedure's capacity to accommodate phenomena such as electromagnetic coupling and intentional feedback. The circuit, i.e. network plus DUT, is then assessed through direct measurement and through emulation. The results of this analysis demonstrate excellent agreement in dc power consumption, efficiency, delivered power, gain, and ACPR which, except in the case of the upper ACPR, does not exceed a relative error of 3.1%.

The purpose of this work is to present a fundamental and general approach towards microwave network emulation. Ongoing and future research efforts are presently directed towards expanding the scope of this algorithm towards harmonic and baseband microwave network emulation, introducing near-band impedance control (presenting the network impedance at tones adjacent to the signal), and the virtualization of multiple devices to emulate larger systems, e.g. a multistage amplifier, load-modulation (i.e. Doherty), or array of transmitters.

Chapter 7

Conclusions and Future Work

7.1 Contributions

In summary, this thesis presents several methods regarding the design of high-performance microwave front end components with specific emphasis on efficiency enhancement, design complexity management, and hardware in the loop analysis. Specific contributions from Chapters 2-6 are summarized below with a discussion on paths for future work.

Chapter 2 reviews the power amplifier (PA), its impact on transmit module efficiency for modulated signals, and methods for recovering efficiency. The PA load-line model is reviewed and used as a platform for reviewing two common architectures for efficiency recovery: load and supply modulation. Chapter 3 continues this discussion with the design and test of a discrete four-level supply modulator. Specific contributions of these chapters include:

- Design of two discrete four-level supply modulators in WIN and Qorvo's 150 nm Gallium Nitride (GaN) on Silicon Carbide (SiC) processes. In [172], the Qorvo supply modulator is used to achieve a peak improvement of 10 percentage points the power added efficiency (PAE) of a 6 W two-stage PA using a 67 MHz, 64-QAM signal centered at 12.8 GHz.

- A simulation method is discussed which combines static-load measurements of the WIN supply modulator and the load-line model of a 10 W PA. Simulations suggest an increase in PA drain efficiency of approximately 12 percentage points and a total composite efficiency increase of 6.4 percentage points when using a 35 MHz OFDM test signal. The design of

the WIN supply modulator and static testing is published in [75].

- Demonstration of peak PA efficiency enhancement by 16 percentage points and composite efficiency enhancement of 10 percentage at an average output power of 31.4 dBm when compared to a static supply. Test signals are centered at 6.4 GHz, have a PAPR of 7 dB and have bandwidths of 6, 34, and 67 MHz. At lower output powers this corresponds to a 50% reduction in waste heat from the power amplifier. These measurements contributed to a larger work published in [70].

Chapter 4 reviews network synthesis and automated design as computational methods for managing growth in design complexity. A review of literature and material relevant to the topic of synthesis is presented covering essential concepts such how synthesis is related to analysis and design, the approximation and realization problems, criteria for realization, and important mathematical concepts such as a PR driving point function and the relationship between its even and real parts. These concepts are applied in the derivation of a non-Butterworth, maximally-flat filter using the electrostatics concepts and the potential analog method. A more general approach to lumped-element network synthesis, the Simplified Real Frequency Technique (SRFT), is also briefly presented. Specific contributions from this chapter include:

- Development of an approach to using electrostatics and the potential analog method to derive a maximally-flat filter form which is not a canonical Butterworth.

- Comparison of the four-pole behavior of the new filter form to that of a four pole Butterworth. Though these results suggest inferior performance in pass-band, magnitude flatness the new filter does have a more desirable group delay, indicating an expansion to the maximally-flat filter trade space.

- Illustrative examples of the SRFT are presented along with timed benchmarks– demonstrating the approach for general circuit automated design.

Chapter 5 expands the SRFT framework discussed in Chapter 4 for the automated design of

nonuniform transmission lines (NTLs). Like the traditional SRFT, the approach discussed here is capable of double-matching and co-design which allows for the development of more complex networks. In addition to this, this NTL automated design method is also capable of accounting for loss and physical constraints, i.e. minimum and maximum length and width. Also presented is a computational, semi-automated method for meandering planar NTLs–making the approach viable for space-constrained applications such as monolithic microwave integrated circuits (MMICs). Specific contributions from this chapter include:

- A new method for NTL automated circuit design which is published in [173]. This is designed as an extension to the traditional SRFT framework and is capable of double matching, co-design, inclusion of physical constraints and loss.
- A new computational method for meandering planar NTL networks is presented. This is an important step forward to make NTL networks practical for space-constrained circuits and technologies, e.g. integrated circuits.
- Design of several high-performance hybrid circuits using NTLs. These examples include a 1-4 GHz single stage amplifier using four co-synthesized NTL networks and an octave-bandwidth band-stop matching network.
- Design of several high-performance MMIC circuits using NTLs. These circuits include:
    * A PA developed in WIN's 150 nm GaN process which demonstrates 40% fractional bandwidth centered at 20 GHz. This PA uses an NTL output matching network designed using the method of [130, 135] and was presented at the 2024 Radio Wireless Week and is published in [127].
    * A high-efficiency, low phase-noise voltage controlled oscillator (VCO). The core circuit is designed by Alec Russell and with the transmission line resonator designed using the NTL design method discussed in [173]. This circuit is published in [146].

- A dc-40 GHz distributed amplifier designed in Qorvo's 90 nm GaN-on-SiC process. All matching networks in this circuit are implemented using NTLs.

Chapter 6 presents a method for circuit analysis which does not rely on nonlinear models. This is particularly necessary for situations where the circuit is expected to operate with signals or in environments where available nonlinear models may not be accurate. This technique is referred to in this work as Network Emulation and can be considered the logical extension of modern, state-of-the-art wideband active load and source pull. A detailed derivation of the algorithm from first principles is provided and a new approach to a generalized tuner is developed along the way. This technique has been submitted to IEEE Transactions on Microwave Theory and Techniques for publication. A summary of specific contributions include:

- A source excitation definition, A_0, derived from Kurokawa's power waves which yields a uniquely satisfying definition for a the tuner's source reflection coefficient in the presence of an excitation:

  $$\Gamma_{S0} = \frac{a - A_0}{b - A_0},$$

  where Γ_{S0} is the passive or physical reflection coefficient of the source, a is the power wave incident on the DUT from the source, b is the power wave reflected from the DUT to the source, and A_0 is the excitation of the source.

- A generalized tuner algorithm which uses the DUT input reflection coefficient at a port to directly solve for the required source excitation.

- The convergence criteria for the generalized tuner algorithm when the input reflection coefficient is not fully known. This is presented in Appendix C.

- The extension of the generalized tuner algorithm to the emulation of linear, multiport networks with loss, coupling, and dispersion.

- The general convergence criteria for simple two-port network emulation are derived and presented.

- An example of small-signal network emulation of linear networks on a MACOM CGH40006P GaN-on-SiC high electron mobility transistor (HEMT). These results are compared to simulation of the entire circuit (i.e. emulated networks with entire HEMT) with the relative error in gain and return loss being $< 1\%$.

- An example of large-signal network emulation with intentional coupling between the input and output matching networks. The total circuit response is also measured with the physical matching network. Results are reported for output power, efficiency, gain, and adjacent channel power ratio (ACPR). Aside from the upper side-band ACPR, the maximum relative error in all cases is less than 3.5%.

7.2 Future Work

7.2.1 Monolithic Integration of a Ka-Band PA and an Asymmetric, Six-Level Supply Modulator

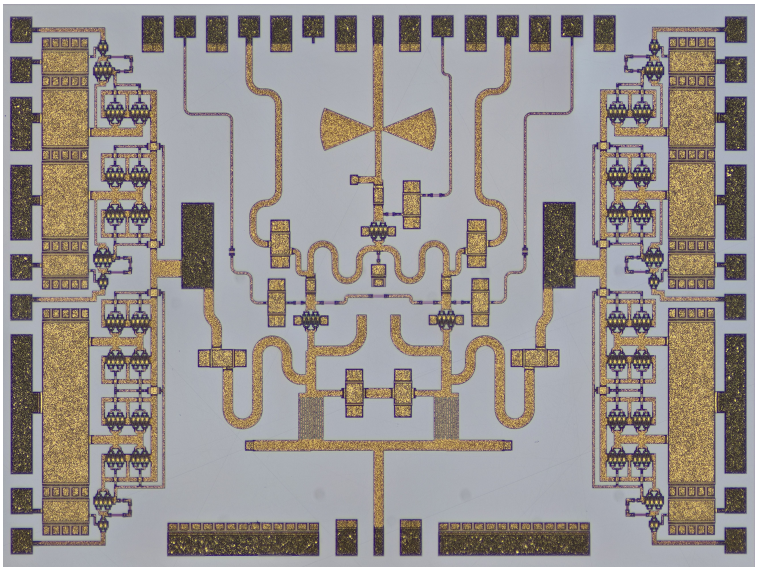


Figure 7.1: A monolithically integrated multilevel supply modulator and power amplifier. The size of the circuit is 3.5 mm by 2.6 mm.

This work also explored the monolithic integration of a multilevel supply modulator and

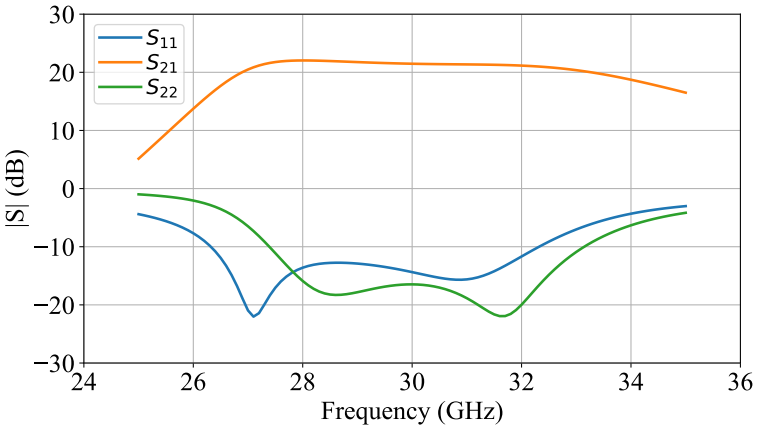


Figure 7.2: Integrated PA small signal parameters. Simulated S_{12} is less than -40 dB.

Ka-band PA designed and fabricated in Northrup Grumman's 90 nm GaN-on-SiC process. The fabricated circuit is illustrated in Fig. 7.1. The supply modulator used in this design uses a 6-level asymmetric architecture as opposed to the standard symmetric 4-level architecture. Increasing the number of levels from 4 to 6 allows the tracker to more closely track the desired envelope signal. Alternatively, if only a few levels are necessary, several of the lower power levels could be combined for reduced conduction loss and improved current handling.

The asymmetric approach stems from the observation that the conduction efficiency, (3.2), of a power switch is directly proportional to the current through the switch and its on-state current. Assuming that all current through the level is delivered to the PA drain, the on-state current is

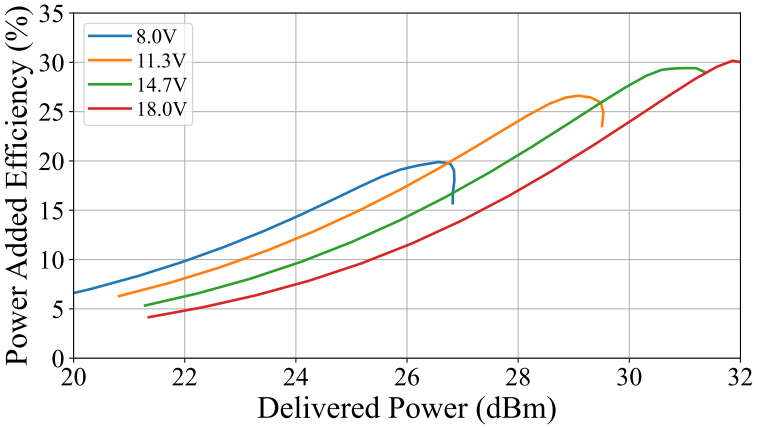


Figure 7.3: Simulated amplifier PAE versus output power.

purely a function of the level's V_{dd} bias and the drain resistance of the amplifier, i.e. (3.4). At low output powers, the drain current of the amplifier can be quite-low. This factor–along with modern signal tendency towards high PAR values–indicates that conduction losses are less important to these lower voltage levels than switching losses. For this reason the size of the power switch is tapered in this design in a 1:2:4 ratio.

Simulations of supply modulator illustrated in Fig. 7.1 indicate an efficiency of 88% when modulating a "stair-step" waveform similar to that of 3.5 with a period of 100 MHz and across a 66.5Ω load in parallel with 5 pF of capacitance. The PA shown in the center of the circuit illustrated in Fig. 7.1 is a Ka-band PA with a bandwidth centered at 30 GHz. The simulated, small-signal S-parameters of the PA are illustrated in Fig. 7.2. The anticipated small-signal gain of the final amplifier is expected to be > 20 dB. Likewise, Fig. 7.3 also illustrates the anticipated PAE of the entire PA at several different drain voltages and output powers. The saturated output power of the amplifier is expected to peak at around 1 W.

Fig. 7.4 illustrates a version of the integrated supply modulator and PA from Fig. 7.1 but in a wafer-level packaged (WLP) version of the technology. Posts–or inter-cavity interconnects–are placed throughout the circuit to suppress the formation of cavity modes. This design also includes several diodes placed throughout the space to allow for integrated temperature sensing of the circuit during test. The total size of the circuit is 5 mm-by-5 mm.

Future research will include the package and test of the integrated multilevel supply modulator and PAs illustrated in Fig. 7.1 and Fig. 7.4, respectively.

7.2.2 Planar Circuit Approach for Nonuniform Transmission Line Analysis

The nonuniform transmission line (NTL) automated design method discussed in Chapter 5 uses a one-dimensional model of a transmission line. This type of model can account for transmission line loss, but not for modes induced by interconnects, meandering, or rapid variations over position in the characteristic impedance function. Accurately incorporating these effects are essential maximizing the performance of NTL networks, and therefore further research is required to

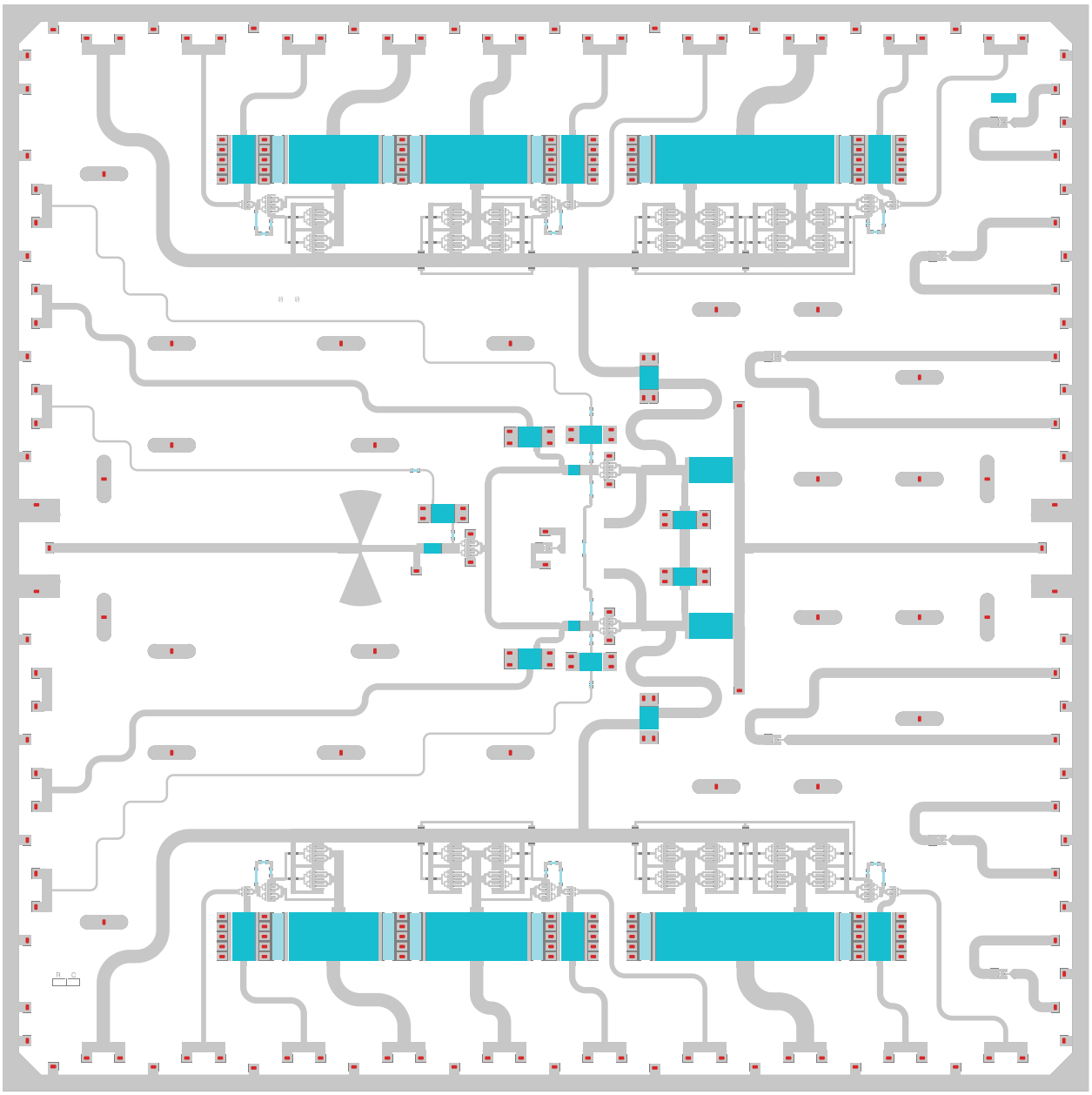
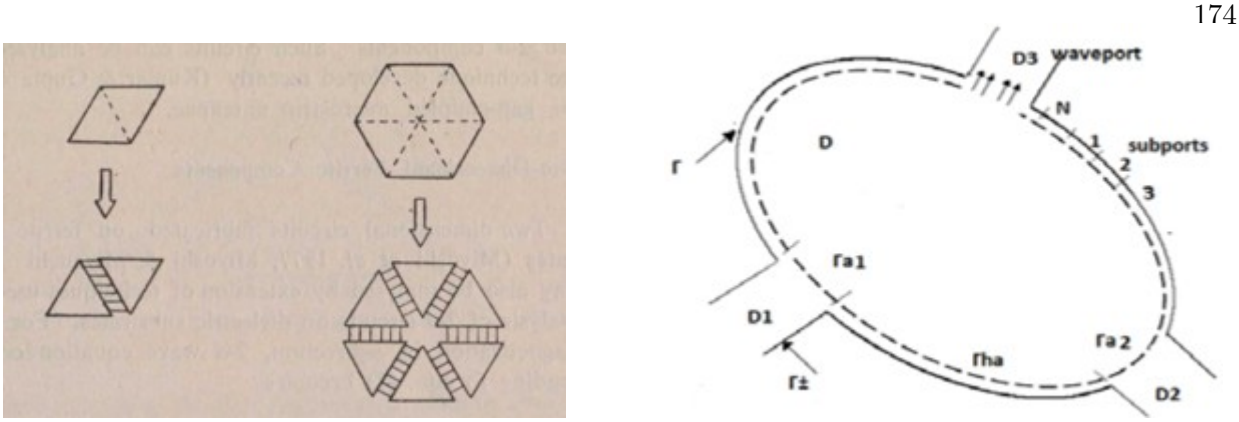


Figure 7.4: Layout of monolithically integrated supply modulator and PA using wafer-level packaging. The final size of the circuit is 5 mm by 5 mm.



(a) (b)

Figure 7.5: The planar circuit approach (a) illustration of segmentation method from [174] and (b) image of boundary integral method from [175].

expand the model.

Electromagnetic analysis can account for these effects but techniques most commonly applied to planar circuit analysis require a three-dimensional model of the network which can greatly increase the time required for analysis. The "Planar Circuit Approach" (PCA) is of interest to future research in this area as an intermediate step. The PCA is used for circuits where structures are comparable to a wavelength along the x and y axes while the circuit is much smaller than a wavelength along the z-axis. When the dielectric of planar circuit is homogenous and isotropic the problem may be reduced into a two-dimensional form along the x and y directions [176].

There are two general forms of the PCA discussed in literature the segmentation and boundary integral method approaches. In the segmentation method, Fig. 7.5a, the circuit is broken down into segments with close-form Green's functions. These segments have terminals which are connected to the terminals of adjacent segments. From this point, the impedance matrices of each segment and the connections between segments can be used to compute the planar circuit response.

The second form of PCA discussed in literature is the boundary integral method (BIM), Fig. 7.5b. The approach to the BIM is similar to a two-dimensional form of the Method of Moments (MoM). However, in the BIM the impedance matrix of the entire planar structure is found by

integrating around its boundary. This method is better-suited to NTL geometry as it does not require breaking down its geometry into pre-defined forms such as equilateral triangles.

7.2.3 Future Work In Network Emulation

This thesis presents a general approach to network emulation which can be extended in several ways.

7.2.3.1 Nearband, Harmonic and Baseband Emulation

The example presented in Chapter 6 only controls tones inside the signal bandwidth while dedicated networks are used to provide consistent harmonic and baseband terminations. For network emulation to be a valid approach to circuit analysis it must be extended to replicating the baseband, harmonic, and near-band behavior of the network. Table 6.2 and Fig. 6.18 indicates that the near-band behavior of the circuit has the highest relative disagreement between emulation and measurement. To improve this agreement, the network should be replicated in the near band as well. This is called near-band impedance control and could be accomplished without additional measurement equipment. While the theory presented is readily extended to the circuits baseband and harmonics frequencies, additional test and measurement resource are required.

7.2.3.2 Emulating Circuits with Multiple Nonlinear Devices

Another area of future research in network emulation is to extended the technique to circuits with multiple devices. One approach to addressing this would be to use multiple test benches; however, this could be undesirable as it requires duplication of hardware resources. However, if the nonlinear component of the circuit is constructed of homogenous unit elements, an alternative approach perform emulation on a single unit element but at different locations in the larger circuit– as indicated in Fig. 7.6. This is a relatively straightforward extension of the emulator algorithm which caches the DUT state at each point in the network. This concept may particularly important when extending emulation beyond circuits to systems such as transmit arrays.

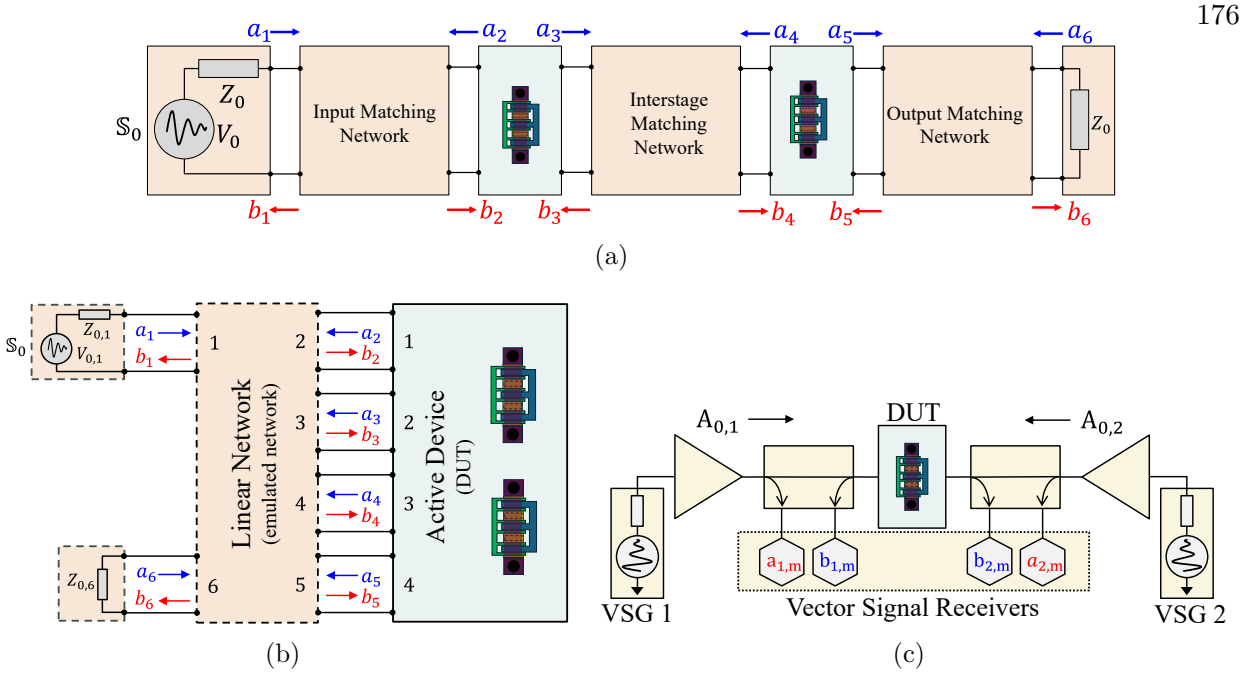


Figure 7.6: Extension of network emulation of circuits with multiple nonlinear devices. (a) a conceptual two-stage amplifier made up of repeated nonlinear elements, (b) an equivalent analysis block diagram where the elementary nonlinear device is repeated, and (c) the measurement system.

The concept of multi-device emulation is demonstrated in Fig. 7.7. Fig. 7.7a illustrates the circuit to undergo emulation. The networks to be emulated are an input matching network (IMN), interstage matching network (ISMN), and an output matching network (OMN). These networks are low-pass prototypes synthesized to maximize the two-stage amplifier gain magnitude using the SRFT discussed in Chapter 4. Likewise, "nonlinear" circuit component is the device under test (DUT) used in Chapter 6, and is used as an instance of both the first and second stage active devices.

In this example, the process of emulation is extended to multiple devices through an iterative "caching" method which wraps around the approach to emulation discussed in Chapter 6. In this approach all nonlinear devices are marked as either "activated" or "deactivated". When active, the nonlinear device is represented by the physical test hardware (DUT) in the measurement system. Upon deactivating, the current responses of the DUT are "cached" or stored. These values are then used to update the excitation of the next active device. This process continues until emulation error

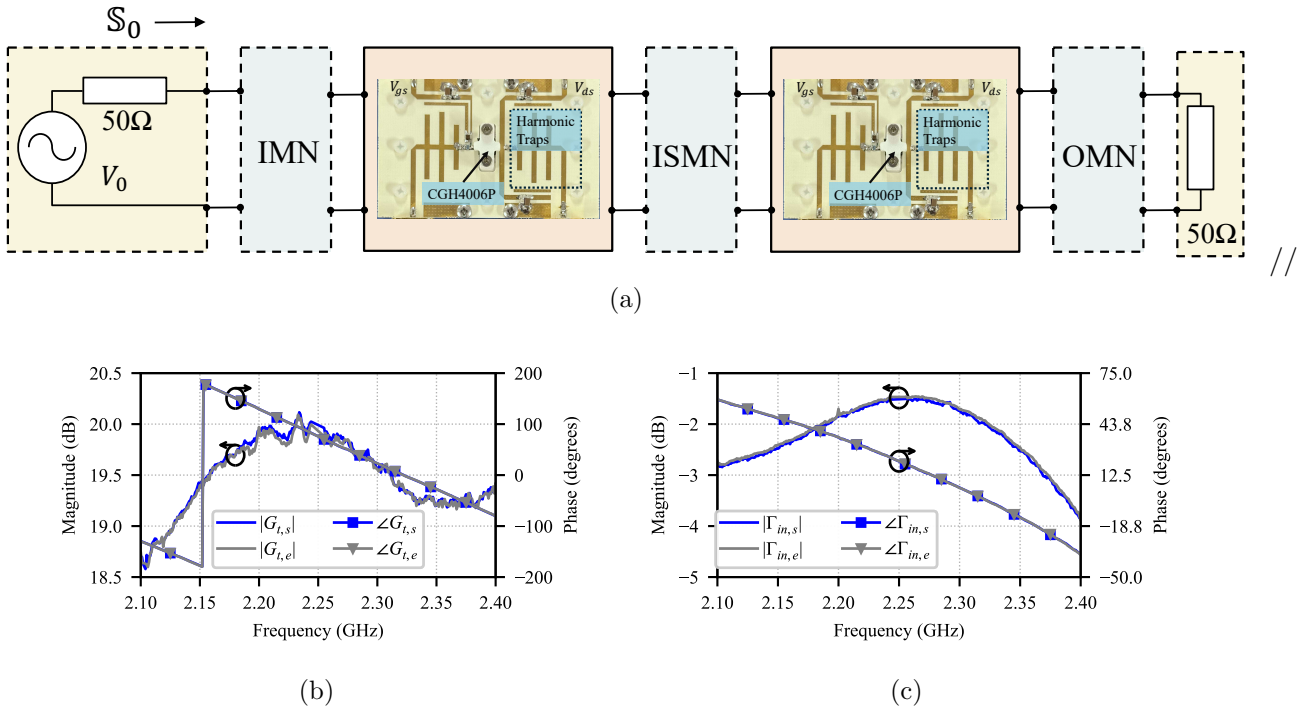


Figure 7.7: Emulation of a two-stage amplifier (a) excited with a 309 MHz bandwidth signal centered at 2.25 GHz. Shown below are are the simulated and emulated, small-signal (a) transducer gain, G_t, and (b) input reflection coefficient, Γ_{in}.

(6.22) becomes sufficiently small.

Fig 7.7b and 7.7c illustrate the emulated and simulated small-signal gain, G_t, and input reflection coefficient, Γ_{in}. The simulated values are found by simulating small-signal measurements of the DUT with the matching networks of Fig. 7.7a. For emulation, circuit available source power is set to -10 dBm to ensure that the second stage is not close to entering a saturated state. Both Fig. 7.7b and 7.7c demonstrate good agreement between simulation and emulation of the circuit. Further work is required to extend this small-signal example into a representative large-signal comparison of network emulation with an equivalent measurement.

7.3 Summary

Rising demand for higher data transmission rates is driving the need for increased transmitter linearity, efficiency, and bandwidth. To meet these challenges, designers are adopting advanced

architectures that significantly increase transmitter complexity, often surpassing the capabilities of traditional design methodologies. Supply modulation is one such approach that improves transmitter efficiency and reduces thermal waste. This is achieved by maintaining the power amplifier near saturation through modulation of its drain supply voltage using an envelope amplifier. Other methods to enhance amplifier efficiency include load modulation and harmonic injection. In all cases, the complexity of traditional amplifier architectures is increased, necessitating new tools to manage this complexity effectively. Synthesis and automated design are two such tools. Synthesis methods, such as the simplified real frequency technique (SRFT), enable complex impedance matching and address intricate design challenges. However, synthesis methods are limited in their ability to satisfy complex physical requirements. Conversely, structures like nonuniform transmission lines (NTLs) can meet these physical criteria while also achieving complex impedance matching over broad operating bandwidths.

Advanced architectures also rely on nonlinear devices (e.g., transistors and diodes) to perform functions such as amplification and mixing. Traditional design methodologies depend on the accuracy and availability of nonlinear device models to design around these elements. When these conditions cannot be met, alternative approaches must be considered, which can significantly impact design costs. Network emulation is a novel hardware-in-the-loop approach that addresses this issue by replacing the nonlinear model with a physical device. In this method, passive networks are emulated on the nonlinear device, and its response is used to inform the composite circuit behavior. Additionally, this approach allows for the controlled application of more sophisticated physical effects. While this work demonstrates the general algorithm for network emulation, further research is needed to fully explore its capabilities.

These approaches offer new opportunities for designing high-performance transmitters. Automated design and synthesis can be employed to create sophisticated matching networks, while network emulation enables the integration of nonlinear devices into the design process.

Bibliography

[1] R. E. Scott, "An Analog Device for Solving the Approximation Problem of Network Synthesis," Technical Report 137, Massachusettts Institute of Technology, Cambridge, MA, June 1950.

[2] Department of Defense, "Electromagnetic Spectrum Superiority Strategy," Oct. 2020.

[3] White House, "National Spectrum Strategy," Nov. 2023.

[4] C. Nogales, P. Flaten, M. Olavsbråten, Z. Popović, and G. Lasser, "Deliberate source/load mismatch for linearity and efficiency of discrete supply modulated gan pas," IEEE Transactions on Microwave Theory and Techniques, vol. 72, no. 12, pp. 6833–6844, 2024.

[5] A. Alt, P. Chen, S. Alsahali, G. Wang, R. Quaglia, P. J. Tasker, and J. Lees, "Impact of the input impedance on the linearity of supply modulated gan hemt power amplifiers," in 2019 49th European Microwave Conference (EuMC), pp. 706–709, IEEE, 2019.

[6] M. R. Duffy, G. Lasser, M. Olavsbråten, E. Berry, and Z. Popović, "Efficient multisignal 2–4-ghz power amplifier with power tracking," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 12, pp. 5652–5663, 2018.

[7] R. J. Baxley, B. T. Walkenhorst, and G. T. Zhou, "Signal classification using a peak-to-average power ratio statistic," in 2009 IEEE International Conference on Communications, pp. 1–5, IEEE.

[8] N. LaSorte, W. Barnes, and H. Refai, The History of Orthogonal Frequency Division Multiplexing. Pages: 3596.

[9] B. Hirosaki, "An orthogonally multiplexed QAM system using the discrete fourier transform," vol. 29, no. 7, pp. 982–989.

[10] Y. Rahmatallah and S. Mohan, "Peak-to-average power ratio reduction in OFDM systems: A survey and taxonomy," vol. 15, no. 4, pp. 1567–1592.

[11] Q. Nguyen, T. K. Nguyen, H. H. Nguyen, and B. Berscheid, "Novel PAPR reduction algorithms for OFDM signals," vol. 10, pp. 77452–77461.

[12] D. Pozar, Microwave Engineering. Wiley, 2012.

[13] C. Campbell, A. Balistreri, M.-Y. Kao, D. Dumka, and J. Hitt, "GaN Takes the Lead," IEEE Microwave Magazine, vol. 13, pp. 44–53, Sept. 2012.

[14] A. Grebennikov, RF and microwave power amplifier design. McGraw-Hill New York, NY, USA:, 2005.

[15] S. C. Cripps et al., RF power amplifiers for wireless communications, vol. 250. Artech house Norwood, MA, 2006.

[16] P. Wright, J. Lees, P. J. Tasker, J. Benedikt, and S. C. Cripps, "An efficient, linear, broadband class-j-mode PA realised using RF waveform engineering," in 2009 IEEE MTT-S International Microwave Symposium Digest, pp. 653–656, IEEE.

[17] W. Doherty, "A new high efficiency power amplifier for modulated waves," vol. 24, no. 9, pp. 1163–1182.

[18] H. Chireix, "High power outphasing modulation," vol. 23, no. 11, pp. 1370–1392.

[19] T. Barton, "Not Just a Phase: Outphasing Power Amplifiers," IEEE Microwave Magazine, vol. 17, pp. 18–31, Feb. 2016.

[20] T. W. Barton and D. J. Perreault, "Theory and Implementation of RF-Input Outphasing Power Amplification," IEEE Transactions on Microwave Theory and Techniques, vol. 63, pp. 4273–4283, Dec. 2015.

[21] S. Chung, P. A. Godoy, T. W. Barton, E. W. Huang, D. J. Perreault, and J. L. Dawson, "Asymmetric multilevel outphasing architecture for multi-standard transmitters," in 2009 IEEE Radio Frequency Integrated Circuits Symposium, (Boston, MA, USA), pp. 237–240, IEEE, June 2009.

[22] D. J. Perreault, "A New Power Combining and Outphasing Modulation System for High-Efficiency Power Amplification," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 58, pp. 1713–1726, Aug. 2011.

[23] A. S. Jurkov, L. Roslaniec, and D. J. Perreault, "Lossless Multiway Power Combining and Outphasing for High-Frequency Resonant Inverters," IEEE Transactions on Power Electronics, vol. 29, pp. 1894–1908, Apr. 2014.

[24] T. W. Barton, J. L. Dawson, and D. J. Perreault, "Experimental Validation of a Four-Way Outphasing Combiner for Microwave Power Amplification," IEEE Microwave and Wireless Components Letters, vol. 23, pp. 28–30, Jan. 2013.

[25] W. Gerhard and R. Knoechel, "Improvement of power amplifier efficiency by reactive Chireix combining, power back-off and differential phase adjustment," in 2006 IEEE MTT-S International Microwave Symposium Digest, (San Francisco, CA), pp. 1887–1890, IEEE, 2006.

[26] M. Litchfield, T. Reveyrand, and Z. Popovic, "X-Band outphasing power amplifier with internal load modulation measurements," in 2014 44th European Microwave Conference, (Rome), pp. 1428–1431, IEEE, Oct. 2014.

[27] M. Litchfield and Z. Popovic, "X-band outphasing GaN MMIC PA with power recycling," in 2015 IEEE MTT-S International Microwave Symposium, (Phoenix, AZ, USA), pp. 1–4, IEEE, May 2015.

[28] D. N. Martin, T. Cappello, M. Litchfield, and T. W. Barton, "An X-band RF-input Outphasing Power Amplifier," in 2018 IEEE/MTT-S International Microwave Symposium - IMS, (Philadelphia, PA), pp. 308–311, IEEE, June 2018.

[29] M. Litchfield and T. Cappello, "The Various Angles of Outphasing PAs: Competitiveness of Outphasing in Efficient Linear PA Applications," IEEE Microwave Magazine, vol. 20, pp. 135–145, Apr. 2019.

[30] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," vol. 26, no. 6, pp. 443–445.

[31] J. Lange, "Interdigitated Strip-Line Quadrature Hybrid," in 1969 G-MTT International Microwave Symposium, (Dallas TX, USA), pp. 10–13, IEEE, 1969.

[32] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-Input Load Modulated Balanced Amplifier With Octave Bandwidth," IEEE Transactions on Microwave Theory and Techniques, vol. 65, pp. 5181–5191, Dec. 2017.

[33] D. J. Shepphard, J. Powell, and S. C. Cripps, "A Broadband Reconfigurable Load Modulated Balanced Amplifier (LMBA)," in 2017 IEEE MTT-S International Microwave Symposium (IMS), pp. 947–949, June 2017.

[34] Y. Cao and K. Chen, "Dual-Octave-Bandwidth RF-Input Pseudo-Doherty Load Modulated Balanced Amplifier with ≥ 10-dB Power Back-off Range," in 2020 IEEE/MTT-S International Microwave Symposium (IMS), (Los Angeles, CA, USA), pp. 703–706, IEEE, Aug. 2020.

[35] D. J. Collins, R. Quaglia, J. R. Powell, and S. C. Cripps, "The orthogonal LMBA: A novel RFPA architecture with broadband reconfigurability," vol. 30, no. 9, pp. 888–891. Conference Name: IEEE Microwave and Wireless Components Letters.

[36] J. Pang, Y. Li, M. Li, Y. Zhang, X. Y. Zhou, Z. Dai, and A. Zhu, "Analysis and design of highly efficient wideband RF-input sequential load modulated balanced power amplifier," vol. 68, no. 5, pp. 1741–1753.

[37] K. Vivien, G. Baudoin, O. Venard, and P. Pierre-Charles-Felix, "A Novel Double Balanced Architecture with VSWR Immunity for High Efficiency Power Amplifier," in 2019 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), (Tel-Aviv, Israel), pp. 1–5, IEEE, Nov. 2019.

[38] R. Quaglia, J. Pang, S. C. Cripps, and A. Zhu, "Load-modulated balanced amplifier: From first invention to recent development," vol. 23, no. 12, pp. 60–70.

[39] A. Sheikhi, "Historical aspect of load-modulated balanced amplifiers," vol. 12, pp. 7974–7986.

[40] L. Kahn, "Single-sideband transmission by envelope elimination and restoration," vol. 40, no. 7, pp. 803–806.

[41] S. Pajic, N. Wang, and Z. Popovic, "Comparison of X-band MESFET and HBT class-E power amplifiers for EER transmitters," in IEEE MTT-S International Microwave Symposium Digest, 2005., (Long Beach, CA, USA), pp. 2031–2034, IEEE, 2005.

[42] Narisi Wang, Xinli Peng, V. Yousefzadeh, D. Maksimovic, S. Pajic, and Z. Popovic, "Linearity of X-band class-E power amplifiers in EER operation," IEEE Transactions on Microwave Theory and Techniques, vol. 53, pp. 1096–1102, Mar. 2005.

[43] Ildu Kim, Jungjoon Kim, Junghwan Moon, and Bumman Kim, "Optimized Envelope Shaping for Hybrid EER Transmitter of Mobile WiMAX— Optimized ET Operation," IEEE Microwave and Wireless Components Letters, vol. 19, pp. 335–337, May 2009.

[44] E. McCune, "Envelope Tracking or Polar—Which Is It? [Microwave Bytes]," IEEE Microwave Magazine, vol. 13, pp. 34–56, May 2012. Conference Name: IEEE Microwave Magazine.

[45] N. D. Lopez, X. Jiang, D. Maksimovic, and Z. Popovic, "A High-Efficiency Linear Polar Transmitter for EDGE," in 2008 IEEE Radio and Wireless Symposium, pp. 199–202. ISSN: 2164-2974.

[46] N. Wang, N. D. Lopez, V. Yousefzadeh, J. Hoversten, D. Maksimovic, and Z. Popovic, "Linearity of X-Band Class-E Power Amplifiers in a Digital Polar Transmitter," in 2007 IEEE/MTT-S International Microwave Symposium, (Honolulu, HI, USA), pp. 1083–1086, IEEE, June 2007. ISSN: 0149-645X.

[47] E. McCune and Q. Diduck, "4096-QAM Microwave Transmitter Providing Efficiency Exceeding 50% and EVM Below 1%," in 2019 49th European Microwave Conference (EuMC), pp. 896–899, Oct. 2019.

[48] E. McCune, "16,384-QAM Microwave Link With 53% Linearized-Transmitter Efficiency, 2.5 Watt Peak Power, and on-air EVM Below 1%," in 2019 IEEE MTT-S International Microwave Symposium (IMS), (Boston, MA, USA), pp. 750–753, IEEE, June 2019.

[49] D. Kimball, J. Jeong, C. Hsia, P. Draxler, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, and P. Asbeck, "High-efficiency envelope-tracking w-CDMA base-station amplifier using GaN HFETs," vol. 54, no. 11, pp. 3848–3856. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[50] A. Zai, Dongxue Li, S. Schafer, and Z. Popovic, "High-efficiency X-band MMIC GaN power amplifiers with supply modulation," in 2014 IEEE MTT-S International Microwave Symposium (IMS2014), (Tampa, FL, USA), pp. 1–4, IEEE, June 2014.

[51] T. Cappello, C. Florian, D. Niessen, R. P. Paganelli, S. Schafer, and Z. Popovic, "Efficient X-Band Transmitter With Integrated GaN Power Amplifier and Supply Modulator," IEEE Transactions on Microwave Theory and Techniques, vol. 67, pp. 1601–1614, Apr. 2019.

[52] Z. Popovic, "Amping up the PA for 5g: Efficient GaN power amplifiers with dynamic supplies," vol. 18, no. 3, pp. 137–149.

[53] C. Nogales, L. Marzall, G. Lasser, and Z. Popović, "Dynamic Supply Modulation of a 6 – 12 GHz Transmit Array," in 2023 IEEE Wireless and Microwave Technology Conference (WAMICON), (Melbourne, FL, USA), pp. 140–143, IEEE, Apr. 2023.

[54] P. Asbeck and Z. Popovic, "ET comes of age: Envelope tracking for higher-efficiency power amplifiers," IEEE Microwave Magazine, vol. 17, no. 3, pp. 16–25, 2016.

[55] Y. Zhang, M. Rodríguez, and D. Maksimović, "Very high frequency PWM buck converters using monolithic GaN half-bridge power stages with integrated gate drivers," IEEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7926–7942, 2016.

[56] T. Cappello, C. Florian, D. Niessen, R. P. Paganelli, S. Schafer, and Z. Popovic, "Efficient X-band transmitter with integrated GaN power amplifier and supply modulator," IEEE Transactions on Microwave Theory and Techniques, vol. 67, no. 4, pp. 1601–1614, 2019.

[57] A. Sepahvand, P. Momenroodaki, Y. Zhang, Z. Popović, and D. Maksimović, "Monolithic multilevel GaN converter for envelope tracking in RF power amplifiers," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1–7, 2016.

[58] D. Kimball, P. Draxler, J. Jeong, C. Hsia, S. Lanfranco, W. Nagy, K. Linthicum, L. Larson, and P. Asbeck, "50% PAE WCDMA basestation amplifier implemented with GaN HFETs," in IEEE Compound Semiconductor Integrated Circuit Symposium, 2005. CSIC '05., pp. 4 pp.–. ISSN: 2374-8443.

[59] J. Jeong, D. F. Kimball, M. Kwak, P. Draxler, C. Hsia, C. Steinbeiser, T. Landon, O. Krutko, L. E. Larson, and P. M. Asbeck, "High-Efficiency WCDMA Envelope Tracking Base-Station Amplifier Implemented With GaAs HVHBTs," IEEE Journal of Solid-State Circuits, vol. 44, pp. 2629–2639, Oct. 2009.

[60] P. Draxler, S. Lanfranco, D. Kimball, C. Hsia, J. Jeong, J. De Sluis, and P. Asbeck, "High Efficiency Envelope Tracking LDMOS Power Amplifier for W-CDMA," in 2006 IEEE MTT-S International Microwave Symposium Digest, (San Francisco, CA), pp. 1534–1537, IEEE, 2006.

[61] M. Rodriguez, Y. Zhang, and D. Maksimovic, "High-Frequency PWM Buck Converters Using GaN-on-SiC HEMTs," IEEE Transactions on Power Electronics, vol. 29, pp. 2462–2473, May 2014.

[62] Y. Zhang, M. Rodriguez, and D. Maksimovic, "100 MHz, 20 V, 90% efficient synchronous buck converter with integrated gate driver," in 2014 IEEE Energy Conversion Congress and Exposition (ECCE), (Pittsburgh, PA, USA), pp. 3664–3671, IEEE, Sept. 2014.

[63] S. Shinjo, Y.-P. Hong, H. Gheidi, D. F. Kimball, and P. M. Asbeck, "High speed, high analog bandwidth buck converter using GaN HEMTs for envelope tracking power amplifier applications," in 2013 IEEE Topical Conference on Wireless Sensors and Sensor Networks (WiSNet), (Austin, TX, USA), pp. 13–15, IEEE, Jan. 2013.

[64] J. Hoversten, Efficient and Linear Microwave Transmitters for High Peak-to-Average Ratio Signals. PhD thesis, University of Colorado, Boulder, 2010.

[65] M. Litchfield, T. Cappello, C. Florian, and Z. Popovic, "X-band GaN multi-level chireix outphasing PA with a discrete supply modulator MMIC," in 2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), pp. 1–4. ISSN: 2374-8443.

[66] A. Cheshire, P. Flaten, Z. Popović, and D. Maksimović, "High-frequency flying capacitor four-level drain supply modulator," in 2025 IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 682–688. ISSN: 2470-6647.

[67] N. Wolff, W. Heinrich, and O. Bengtsson, "Highly efficient 1.8-GHz amplifier with 120-MHz class-g supply modulation," vol. 65, no. 12, pp. 5223–5230. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[68] N. Wolff, W. Heinrich, and O. Bengtsson, "100-MHz GaN-HEMT class-G supply modulator for high-power envelope-tracking applications," IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 3, pp. 872–880, 2016.

[69] A. Sepahvand, P. Momenroodaki, Y. Zhang, Z. Popovic, and D. Maksimovic, "Monolithic multilevel GaN converter for envelope tracking in RF power amplifiers," in 2016 IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1–7, IEEE.

[70] C. Nogales, P. Flaten, M. Olavsbråten, Z. Popović, and G. Lasser, "Deliberate Source/Load Mismatch for Linearity and Efficiency of Discrete Supply Modulated GaN PAs," IEEE Transactions on Microwave Theory and Techniques, pp. 1–12, 2024. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[71] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC Modified Doherty PA With Large Bandwidth and Reconfigurable Efficiency," IEEE Transactions on Microwave Theory and Techniques, vol. 62, pp. 3006–3016, Dec. 2014.

[72] D. Gruner, K. Bathich, A. A. Tanany, and G. Boeck, "Harmonically tuned GaN-HEMT Doherty power amplifier for 6 GHz applications,"

[73] M. R. Duffy, G. Lasser, and Z. Popović, "Discrete Supply Modulation of a Three-Stage K-Band PA," in 2019 49th European Microwave Conference (EuMC), pp. 698–701, Oct. 2019.

[74] N. Wolff, W. Heinrich, M. Berroth, and O. Bengtsson, "A three-level class-G modulated 1.85 GHz RF power amplifier for LTE applications with over 50% PAE," in 2016 IEEE MTT-S International Microwave Symposium (IMS), (San Francisco, CA), pp. 1–4, IEEE, May 2016.

[75] P. Flaten, C. Nogales, and Z. Popovic, "GaN MMIC 4-Level Supply Modulator for 6-12 GHz PA," in GOMACTech, 2023.

[76] M. Olavsbråten and A. I. Hagen, "A Method for Designing a Linear, Efficient 2-Stage GaN PA for Supply Modulation," in 2024 IEEE/MTT-S International Microwave Symposium - IMS 2024, (Washington, DC, USA), pp. 551–554, IEEE, June 2024.

[77] E. A. Guillemin, Synthesis of Passive Networks : Theory and Methods Appropriate to the Realization and Approximation Problems. Robert E. Krieger Publishing Company, 1957.

[78] E. A. Guillemin, Mathematics of Circuit Analysis. M.I.T. Press, 2003.

[79] I. Hunter, Theory and Design of Microwave Filters. Institution of Engineering and Technology, Jan. 2001.

[80] B. S. Yarman, Design of Ultra Wideband Power Transfer Networks. Wiley, 1 ed.

[81] P. Jarry and J. N. Beneat, Microwave Amplifier and Active Circuit Design Using the Real Frequency Technique. Wiley, 1 ed.

[82] S. Darlington, "Synthesis of reactance 4-poles which produce prescribed insertion loss characteristics: Including special applications to filter design," vol. 18, no. 1, pp. 257–353.

[83] O. Brune, Synthesis of a Finite Two-Terminal Network Whose Driving-Point Impedance is A Prescribed Function of Frequency. Ph.D. Thesis, Massachusetts Institute of Technology, Cambridge, MA, May 1931.

[84] K. Kurokawa, "Power Waves and the Scattering Matrix," IEEE Transactions on Microwave Theory and Techniques, vol. 13, pp. 194–202, Mar. 1965.

[85] V. Belevitch, "Topics in the design of insertion loss filters," vol. 2, no. 4, pp. 337–346.

[86] R. Köprü, "FSRFT—Fast Simplified Real Frequency Technique via Selective Target Data Approach for Broadband Double Matching," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, pp. 141–145, Feb. 2017. Conference Name: IEEE Transactions on Circuits and Systems II: Express Briefs.

[87] B. S. Yarman and A. Kilinc, "High Precision LC Ladder Synthesis Part II: Immittance Synthesis With Transmission Zeros at DC and Infinity," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, pp. 2719–2729, Oct. 2013.

[88] G. Matthaei, "Tables of chebyshev impedance–transforming networks of low-pass filter form," vol. 52, no. 8, pp. 939–963.

[89] Z. Dai, S. He, J. Pang, C. Huang, J. Peng, Z. Yang, and M. Li, "Lowpass network synthesis using "feldtkeller correction approach"," vol. 7, pp. 27970–27982. Conference Name: IEEE Access.

[90] D. M. Pozar, Microwave engineering. Wiley, 4th ed ed. OCLC: ocn714728044.

[91] V. Belevitch, "Synthèse des réseaux électriques passifs an paires de bornes de matrice de répartition prédéterminée," vol. 6, no. 11. Paris: Springer-Verlag.

[92] A. Kilinc and B. S. Yarman, "High Precision LC Ladder Synthesis Part I: Lowpass Ladder Synthesis via Parametric Approach," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 60, pp. 2074–2083, Aug. 2013.

[93] A. Fettweis, "Parametric representation of brune functions," International Journal of Circuit Theory and Applications, vol. 7, pp. 113–119, Jan. 1979.

[94] R. M. Foster, "A Reactance Theorem," Bell System Technical Journal, vol. 3, pp. 259–267, Apr. 1924.

[95] G. Matthaei, "Some Techniques for Network Synthesis," Proceedings of the IRE, vol. 42, pp. 1126–1137, July 1954.

[96] H. Carlin, "A new approach to gain-bandwidth problems," IEEE Transactions on Circuits and Systems, vol. 24, pp. 170–175, Apr. 1977.

[97] B. Yarman and H. Carlin, "A Simplified "Real Frequency" Technique Appliable To Broadband Multistage Microwave Amplifiers," in 1982 IEEE MTT-S International Microwave Symposium Digest, pp. 529–531, June 1982. ISSN: 0149-645X.

[98] R. Baum, "A Contribution to the Approximation Problem," Proceedings of the IRE, vol. 36, pp. 863–869, July 1948.

[99] A. P. Brogle, "The Design of Reactive Equalizers*," Bell System Technical Journal, vol. 28, pp. 716–750, Oct. 1949.

[100] G. Matthaei, "Filter Transfer Function Synthesis," Proceedings of the IRE, vol. 41, pp. 377–382, Mar. 1953.

[101] S. Winkler, "The Approximation Problem of Network Synthesis," Transactions of the IRE Professional Group on Circuit Theory, vol. CT-1, pp. 5–20, Sept. 1954.

[102] R. Fano, "A note on the solution of certain approximation problems in network synthesis," Journal of the Franklin Institute, vol. 249, pp. 189–205, Mar. 1950.

[103] J. C. Maxwell, A treatise on electricity and magnetism, vol. 1. Clarendon press, 1873.

[104] R. Scott, "Network Synthesis by the Use of Potential Analogs," Proceedings of the IRE, vol. 40, pp. 970–973, Aug. 1952.

[105] B. M. Notaroš, Electromagnetics. Upper Saddle River, NJ: Pearson, international edition ed., 2011.

[106] S. Butterworth, "On the Theory of Filter Amplifiers," Wireless Engineer, vol. 7, no. 6, pp. 536–541, 1930.

[107] M. Faraday, "XXXII. *On Static Electrical Inductive Action*," The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science, vol. 22, pp. 200–204, Mar. 1843.

[108] J.-M. Jin, Theory and computation of electromagnetic fields. John Wiley & Sons, 2015.

[109] D. B. Davidson, Computational electromagnetics for RF and microwave engineering. Cambridge University Press, 2010.

[110] S. Darlington, "A history of network synthesis and filter theory for circuits composed of resistors, inductors, and capacitors," IEEE Transactions on Circuits and Systems, vol. 31, pp. 3–13, Jan. 1984. Conference Name: IEEE Transactions on Circuits and Systems.

[111] W. Cauer, "Die verwirklichung von wechselstromwiderständen vorgeschriebener frequenzabhängigkeit," Archiv für Elektrotechnik, vol. 17, no. 4, pp. 355–388, 1926.

[112] S. Darlington, "A survey of network realization techniques," vol. 2, no. 4, pp. 291–297. Conference Name: IRE Transactions on Circuit Theory.

[113] G. Matthaei, "Synthesis of tchebycheff impedance-matching networks, filters, and interstages," vol. 3, no. 3, pp. 163–172.

[114] A. C. Bannon and T. J. Brazil, "A new double matching real frequency technique applied to multistage amplifier design," in 29th European Microwave Conference, 1999, pp. 41–44, IEEE.

[115] B. S. Yarman and S. Kilinc, "A new real frequency line segment technique to assess the gain bandwidth limitations for the double matching problems," in 2023 International Microwave and Antenna Symposium (IMAS), pp. 111–114, IEEE.

[116] Yao-Wen Hsu and E. F. Kuester, "Direct Synthesis of Passband Impedance Matching With Nonuniform Transmission Lines," IEEE Transactions on Microwave Theory and Techniques, vol. 58, pp. 1012–1021, Apr. 2010.

[117] Y.-F. Bai, X.-H. Wang, C.-J. Gao, X.-W. Shi, and H.-J. Lin, "Compact dual-band power divider using non-uniform transmission line," Electronics Letters, vol. 47, pp. 1–2, Feb. 2011. Num Pages: 2 Place: Stevenage, United States Publisher: John Wiley & Sons, Inc.

[118] M. Khalaj-Amirhosseini, "Wideband or Multiband Complex Impedance Matching Using Microstrip Nonuniform Transmission Lines," Progress In Electromagnetics Research, vol. 66, pp. 15–25, 2006.

[119] P. Rulikowski and J. Barrett, "Ultra-Wideband Pulse Shaping Using Lossy and Dispersive Nonuniform Transmission Lines," IEEE Transactions on Microwave Theory and Techniques, vol. 59, pp. 2431–2440, Oct. 2011.

[120] A. I. Hashash, M. H. Bataineh, and A. S. Al-Zoubi, "Applications of nonuniform transmission lines in filters," in 2018 5th International Conference on Electrical and Electronic Engineering (ICEEE), (Istanbul), pp. 47–51, IEEE, May 2018.

[121] M. Le Roy, A. Perennec, S. Toutain, and L. Calvez, "The continuously varying transmission-line technique - application to filter design," IEEE Transactions on Microwave Theory and Techniques, vol. 47, pp. 1680–1687, Sept. 1999.

[122] H. Shirai, "Tapered transmission line resonators and their application to filters," in The 3rd Asia-Pacific Microwave Conference Proceedings, 1990.

[123] L. Ranzani, P. Boffi, R. Siano, S. Rondineau, Z. Popovic, and M. Martinelli, "Microwave-Domain Analog Predistortion Based on Chirped Delay Lines for Dispersion Compensation of 10-Gb/s Optical Communication Signals," Journal of Lightwave Technology, vol. 26, pp. 2641–2646, Aug. 2008.

[124] L. Ranzani, S. Rondineau, P. Boffi, M. Martinelli, and Z. Popovic, "Nonuniform transmission lines for broadband dispersion compensation," in The 40th European Microwave Conference, pp. 324–327, 2010.

[125] M. Olavsbråten, T. Mathiesen, and E. Berry, "Design of an efficient wideband (1–5ghz) 10w pa in gan technology using harmonic tuning," in 2017 IEEE 18th Wireless and Microwave Technology Conference (WAMICON), pp. 1–5, 2017.

[126] M. Fernandez, S. Ver Hoeye, C. Vazquez, L. Alonso Gonzalez, and F. Las-Heras, "On the design of broadband hybrid amplifiers using non-uniform transmission lines as impedance matching networks," IEEE Access, vol. 7, pp. 19670–19677, 2019.

[127] P. Flaten and Z. Popović, "Broadband GaN Power Amplifier MMIC with a Nonuniform Transmission Line Output Network," in 2024 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), pp. 70–73, Jan. 2024. ISSN: 2473-4640.

[128] R. W. Klopfenstein, "A Transmission Line Taper of Improved Design," Proceedings of the IRE, vol. 44, pp. 31–35, Jan. 1956. Conference Name: Proceedings of the IRE.

[129] D. Youla, "Analysis and Synthesis of Arbitrarily Terminated Lossless Nonuniform Lines," IEEE Transactions on Circuit Theory, vol. 11, no. 3, pp. 363–371, 1964.

[130] G. Xiao, K. Yashiro, and S. Ohkawa, "A new numerical method for synthesis of arbitrarily terminated lossless nonuniform transmission lines," IEEE Transactions on Microwave Theory and Techniques, vol. 49, pp. 369–376, Feb. 2001.

[131] A. Hamade, A. Kouki, and F. Ghannouchi, "Synthesis of impedance matching circuits using arbitrary nonuniform transmission lines," in 1997 IEEE MTT-S International Microwave Symposium Digest, vol. 3, (Denver, CO, USA), pp. 1619–1622, IEEE, 1997.

[132] P. Miazga, "Discrete shape optimization method of a non-uniform transmission line — advantages and drawbacks," in MIKON 2008 - 17th International Conference on Microwaves, Radar and Wireless Communications, pp. 1–4, May 2008.

[133] H. Oraizi, "Design of impedance transformers by the method of least squares," IEEE Transactions on Microwave Theory and Techniques, vol. 44, pp. 389–399, Mar. 1996.

[134] B. S. Yarman, Design of ultra wideband antenna matching networks: via simplified real frequency technique, ch. Simplified Real Frequency Technique. Signals and communication technology, New York: Springer, 2008. OCLC: ocn225437884.

[135] Gaobiao Xiao and K. Yashiro, "Impedance matching for complex loads through nonuniform transmission lines," IEEE Transactions on Microwave Theory and Techniques, vol. 50, pp. 1520–1525, June 2002.

[136] E. F. Kuester, "A lower bound for the length of nonuniform transmission line matching sections," AEU - International Journal of Electronics and Communications, vol. 66, pp. 1011–1016, Dec. 2012.

[137] M. Khalaj-Amirhosseini, "Analysis of coupled nonuniform transmission lines using Taylor's series expansion," IEEE Transactions on Electromagnetic Compatibility, vol. 48, pp. 594–600, Aug. 2006. Conference Name: IEEE Transactions on Electromagnetic Compatibility.

[138] M. Khalaj-Amirhosseini, "Analysis of coupled or single nonuniform transmission lines using the method of moments," International Journal of RF and Microwave Computer-Aided Engineering, vol. 18, pp. 376–382, July 2008.

[139] M. Khalaj-Amirhosseini, "Analysis of nonuniform transmission lines using Fourier series expansion," International Journal of RF and Microwave Computer-Aided Engineering, vol. 17, pp. 345–352, May 2007.

[140] M. Khalaj-Amirhosseini, "Closed form solutions for nonuniform transmission lines," Progress In Electromagnetics Research B, vol. 2, pp. 243–258, 2008.

[141] M. Khalaj-Amirhosseini, "Analysis of nonuniform transmission lines using the equivalent sources," Progress In Electromagnetics Research, vol. 71, pp. 95–107, 2007.

[142] K. Lu, "An efficient method for analysis of arbitrary nonuniform transmission lines," IEEE Transactions on Microwave Theory and Techniques, vol. 45, pp. 9–14, Jan. 1997. Conference Name: IEEE Transactions on Microwave Theory and Techniques.

[143] MathWorks, "Nonlinear Constraints." https://www.mathworks.com/help/optim/ug/nonlinear-constraints.html.

[144] B. C. Wadell, Transmission Line Components and Discontinuities. Artech House, 1991.

[145] Y.-W. Hsu, H.-S. Huang, S.-J. Shen, E. F. Kuester, and H.-H. Chen, "Direct Synthesis of Passband Non-uniform Transmission Lined Matching Sections with Discontinuities at the Ends and its Application in Broadband Amplifier Design," in 2019 IEEE MTT-S International Wireless Symposium (IWS), (Guangzhou, China), pp. 1–3, IEEE, May 2019.

[146] A. Russell, P. Flaten, and Z. Popović, "Low Phase Noise InGaP/GaAs HBT MMIC VCO with Nonuniform Transmission Line Resonator for a Chip-Scale Atomic Beam Clock," IEEE Microwave and Wireless Technologies Letters, 2025.

[147] R. Köprü, H. Kuntman, and B. S. Yarman, "On numerical design technique of wideband microwave amplifiers based on GaN small-signal device model," Analog Integrated Circuits and Signal Processing, vol. 81, pp. 71–87, Oct. 2014.

[148] A. Russell, P. Flaten, and Z. Popović, "Low phase noise ingap/gaas hbt mmic vco with nonuniform transmission line resonator for a chip-scale atomic beam clock," IEEE Microwave and Wireless Technology Letters, vol. 35, no. 8, pp. 1222–1225, 2025.

[149] N. C. Miller, A. Brown, M. Elliott, and R. Gilbert, "Temperature Dependent Large-Signal Modeling of GaN HEMTs at Ka-Band using the ASM-HEMT," in 2023 IEEE Wireless and Microwave Technology Conference (WAMICON), pp. 21–24, Apr. 2023.

[150] N. C. Miller, A. Brown, M. Elliott, R. Gilbert, D. T. Davis, A. E. Islam, D. Walker, G. Hughes, K. Liddy, and K. D. Chabak, "An ASM-HEMT for Large-Signal Modeling of GaN HEMTs in High-Temperature Applications," IEEE Journal of the Electron Devices Society, vol. 11, pp. 531–538, 2023.

[151] P. Beleniotis, C. Andrei, U. L. Rohde, and M. Rudolph, "Determining GaN HEMT Trap Models from MHz Load-line Measurement — Synthesis and Evaluation," in 2025 16th German Microwave Conference (GeMiC), pp. 451–454, Mar. 2025. ISSN: 2167-8022.

[152] S. A. Albahrani, D. Mahajan, J. Hodges, Y. S. Chauhan, and S. Khandelwal, "ASM GaN: Industry Standard Model for GaN RF and Power Devices—Part-II: Modeling of Charge Trapping," IEEE Transactions on Electron Devices, vol. 66, pp. 87–94, Jan. 2019.

[153] M. Pradhan, M. Alomari, M. Moser, D. Fahle, H. Hahn, M. Heuken, and J. N. Burghartz, "Physical Modeling of Charge Trapping Effects in GaN/Si Devices and Incorporation in the ASM-HEMT Model," IEEE Journal of the Electron Devices Society, vol. 9, pp. 748–755, 2021.

[154] J. Horn, D. Gunyan, L. Betts, C. Gillease, J. Verspecht, and D. E. Root, "Measurement-based large-signal simulation of active components from automated nonlinear vector network analyzer data via X-parameters," in 2008 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems, pp. 1–6, 2008.

[155] D. E. Root, J. Verspecht, J. Horn, and M. Marcu, X-Parameters: Characterization, Modeling, and Design of Nonlinear RF and Microwave Components. The Cambridge RF and Microwave Engineering Series, Cambridge University Press, 2013.

[156] A. Ferrero and M. Pirola, "Harmonic Load-Pull Techniques: An Overview of Modern Systems," IEEE Microwave Magazine, vol. 14, no. 4, pp. 116–123, 2013.

[157] J.-R. Perez-Cisneros, W. Hallberg, and K. Buisman, "An Active Load-Pull Technique to Emulate Outphasing Power Amplifiers," in 2021 IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications (PAWR), pp. 24–27, 2021.

[158] J.-R. Perez-Cisneros, H. Zhou, C. Fager, and K. Buisman, "Emulation of Non-Reciprocity applied in Load-Modulated Power Amplifier Architectures using Single Amplifier Load-Pull Measurements," in 2021 51st European Microwave Conference (EuMC), pp. 647–650, 2022.

[159] M. Mengozzi, A. M. Angelotti, A. Santarelli, P. Mezzanotte, and G. P. Gibiino, "Millimeter-Wave Implementation of Phased Array Emulation from Wideband Load-Pull Envelope Measurements," in 2025 104th ARFTG Microwave Measurement Conference (ARFTG), pp. 1–4, 2025.

[160] D. Nopchinda and K. Buisman, "An active load-pull technique creating time-variant impedances to emulate coupling between power amplifiers," in 2017 IEEE MTT-S International Microwave Symposium (IMS), (Honolulu, HI, USA), pp. 1437–1440, IEEE, June 2017.

[161] D. Nopchinda and K. Buisman, "Measurement Technique to Emulate Signal Coupling Between Power Amplifiers," IEEE Transactions on Microwave Theory and Techniques, vol. 66, no. 4, pp. 2034–2046, 2018.

[162] K. Buisman, J.-R. Perez-Cisneros, W. Hallberg, D. Nopchinda, and P. J. Zampardi, "Emulation of a Multi-Stage Differential Amplifier Using one Single-Ended Device-Under-Test," in 2021 96th ARFTG Microwave Measurement Conference (ARFTG), (San Diego, CA, USA), pp. 1–4, IEEE, Jan. 2021.

[163] M. Marchetti and M. Squillante, "Signal injection technique for measurement and control of source reflection coefficient of a device under test," 2022.

[164] J. Dobrowolski, Scattering parameters in RF and microwave circuit analysis and design. Artech House microwave library, Artech House.

[165] P. Roblin, Nonlinear RF Circuits and Nonlinear Vector Network Analyzers: Interactive Measurement and D The Cambridge RF and Microwave Engineering Series, Cambridge University Press, 2011.

[166] M. Marchetti, Mixed-Signal Instrumentation for Large-Signal Device Characterization and Modelling. PhD thesis, Delft University of Technology, 2013.

[167] A. Ben Ayed and S. Boumaiza, "Millimeter-Wave Wideband Active Load—Pull System Using Vector Network Analyzer Frequency Extenders," IEEE Microwave and Wireless Technology Letters, pp. 1–4, 2025.

[168] R. E. Collin, Circuit Theory for Waveguiding Systems, pp. 220–302. Wiley, 2001.

[169] J. Rollett, "Stability and power-gain invariants of linear twoports," vol. 9, no. 1, pp. 29–32.

[170] M. Marchetti, G. Avolio, M. Squillante, and A. K. Doggalli, "Load pull measurement techniques: architecture, accuracy, and applications," in 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), pp. 1–6, 2019.

[171] M. Marchetti, M. J. Pelk, K. Buisman, W. C. E. Neo, M. Spirito, and L. C. N. de Vreede, "Active Harmonic Load–Pull With Realistic Wideband Communications Signals," IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 12, pp. 2979–2988, 2008.

[172] "PA and Supply Modulator GaN MMICs for Efficient High-PAR Signals in the 8-14 GHz Band," in GOMACTech, Mar. 2024.

[173] P. Flaten and Z. Popović, "Automated design of nonuniform transmission lines for practical microwave circuits," IEEE Transactions on Microwave Theory and Techniques, vol. 73, no. 10, pp. 7809–7821, 2025.

[174] K. Gupta, "Two-Dimensional Analysis of Microstrip Circuits and Antennae," IETE Journal of Research, vol. 28, pp. 346–364, July 1982.

[175] M. Ourabia and R. Touhami, "Electromagnetic modeling and simulation of passive planar structures," in 2011 IEEE International Conference on Microwave Technology & Computational Electromagnetics, (Beijing, China), pp. 160–163, IEEE, May 2011.

[176] T. Itoh, ed., Numerical techniques for microwave and millimeter-wave passive structures. A Wiley-Interscience publication, New York: Wiley, 1989.

[177] R. E. Collin, Foundations for microwave engineering. John Wiley & Sons, 2007.

[178] P. Hallbjörner, "Method for calculating the scattering matrix of arbitrary microwave networks giving both internal and external scattering," vol. 38, no. 2, pp. 99–102. _eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/mop.10983.

Appendix A

Load Line Model Source Code

The following code is an output power referred load line model for a PA and has been used in Python 3.9 and 3.13. There are two methods for initializing the PA model. The first is to initialize the model for specific PA operating conditions with the following function call:

```
model = RFPA_model.at_operating_point(peak_power,
                                      drain_efficiency,
                                      drain_voltage,
                                      knee_voltage,
                                      maximum_voltage)
```

where `peak_power` is the peak power of the model in Watts, `drain_efficiency` is the drain efficiency of the amplifier as a fractional value (i.e. between 0 and 1), `drain_voltage` is the bias drain voltage of the amplifier in volts, `knee_voltage` is the knee voltage of the amplifier in volts, and `maximum_voltage` is the maximum voltage of the amplifier in volts. The second way is to initialize the model to specific model operating parameters (i.e. conduction angle) with the following function call:

```
model = RFPA_model.at_operating_point(conduction_angle,
                                      drain_voltage,
                                      knee_voltage,
                                      maximum_voltage,
```

```
maximum_current,
deg=in_degrees)
```

where the `conduction_angle` is the conduction angle of the PA at the saturated output power, `drain_voltage` is the quiescent drain voltage of the PA in volts, `knee_voltage` is the knee voltage of the PA in volts, `maximum_voltage` is the peak allowable voltage of the load line in volts, `maximum_current` is the peak current of the load line in amperes, and `in_degrees` logical value that which indicates whether `conduction_angle` should be interpreted in degrees or radians.

```
"""
Title: Load Line Model
Author: Paul Flaten
Date: 8/13/2025
"""

# Import statements
import numpy as np
from scipy.optimize import fminbound
import matplotlib.pyplot as plt

def calc_obo_power(peak_power, obo_db):
    obo_lin = 10**(obo_db/10)
    return peak_power * obo_lin

class RFPA_model:
    """
    Simple Load Line Model for RF Power Amplifiers.
    This class models the output-power referred Cripps load line, which is
        used to predict and explain fundamental power amplifier behaviors
       such as output power, efficiency, conduction angle, and load line
```

```
    resistance. It provides methods for initializing the model at a
    specific operating point or conduction angle, updating model
    parameters, and calculating key amplifier characteristics.
    Visualization methods are also included for plotting IV curves,
    dynamic load lines, and power dissipation contours."""

@classmethod
def at_operating_point(cls, Power, Efficiency, Vdd, Vknee, Vmax):
    """
    Initialize the model at a given power amplifier operating point.
    Args:
        Power (float): saturated output power of the PA in watts.
        Efficiency (float): drain efficiency (as a fractional value
            between 0 and 1) of the power amplifier at saturation.
        Vdd (float): drain bias voltage
        Vknee (float): the knee voltage of the power amplifier
        Vmax (float): maximum drain voltage of the power amplifier
    """

    #create a new rfpa object
    pa = cls()

    #set the power
    pa.P1 = Power
    pa.de = Efficiency
    pa.v1 = Vdd-Vknee
    pa.VKNEE = Vknee
    pa.Vdd = Vdd
    pa.VMAX = Vmax

```

```
44          #find the conduction angle from efficiency
45          f = lambda x: np.abs(Efficiency - (pa.v1 / (2 * pa.Vdd))*(pa.
                calcI1(imax=1,ca=x)/pa.calcI0(imax=1,ca=x)))
46          pa.CA = fminbound(f, 0, 2*np.pi)
47
48          #now find the quiescent current
49          pa.IQ = pa.IMAX*np.cos(pa.CA/2)/(np.cos(pa.CA/2)-1)
50
51          #find the value for IMAX
52          f = lambda x: np.abs(Power - pa.v1 * pa.calcI1(imax=x, ca=pa.CA) /
                2)
53          pa.IMAX = fminbound(f, 0, 1e3)
54          pa.imax = pa.IMAX
55          pa.IFAIL = 1.5*pa.IMAX
56
57          #set the loadline resistance
58          pa.RL     =   (Vdd - Vknee)**2 / (2 * Power)
59
60          #now update everything
61          pa.update()
62
63          #return the class
64          return pa
65
66      @classmethod
67      def at_conduction_angle(cls, conduction_angle, Vdd, Vknee, Vmax, Imax,
            deg:bool=True):
68          """
69          Initialize the model at a given conduction angle
70          Args:
```

```
71              conduction_angle (float): conduction angle of the amplifier (
                    interpreted as radians if deg = False and degrees if deg =
                    True)
72              Vdd (float): drain bias voltage
73              Vknee (float): the knee voltage of the power amplifier
74              Vmax (float): maximum drain voltage of the power amplifier
75              deg (bool, optional): interpret conduction angle as degrees (
                    default=True).
76          """
77
78          #Create the power amplifier
79          pa = cls()
80
81          #First make sure the conduction angle is the right value
82          if deg: conduction_angle = np.deg2rad(conduction_angle)
83          pa.CA = conduction_angle
84          pa.IQ = pa.IMAX*np.cos(pa.CA/2)/(np.cos(pa.CA/2)-1)
85
86          #Set the power amplifier maximum currents
87          pa.IMAX = Imax; pa.imax = Imax
88          pa.VMAX = Vmax; pa.VKNEE = Vknee
89          pa.Vdd  = Vdd
90
91          #Set the fundamental voltage component
92          pa.v1 = pa.Vdd - pa.VKNEE
93          pa.RL = pa.v1 / pa.calcI1()
94
95
96          #calculate the fundamental power
97          pa.P1 = (pa.v1 * pa.calcI1())/2
```

```
98
99
100         #now update everything
101         pa.update()
102
103         #return the object
104         return pa
105
106     def __init__(self):
107         """Initializes the Cripps Load Line Model with default parameters.
108         This constructor sets up the basic properties required for
               modeling the output-power referred Cripps load line, which is
               used to predict and explain fundamental power amplifier
               behaviors.
109
110         Attributes
111         ----------
112         IMAX : float
113             Maximum current (default: 1).
114         VKNEE : float
115             Knee voltage (default: 0).
116         VMAX : float or None
117             Breakdown voltage (default: None).
118         DVFAIL : float
119             Failure delta voltage (default: 1).
120         IFAIL : float
121             Failure current (default: 1e6).
122         IQ : float or None
123             Quiescent current (default: None).
124         Vdd : float or None
```

```
125             Static voltage bias point (default: None).
126         RL : float or None
127             Load resistance (default: None).
128         P1 : float or None
129             Output power (default: None).
130         CA : float or None
131             Conduction angle in radians (default: None).
132         P0 : float or None
133             DC power (default: None).
134         de : float or None
135             Drain efficiency (default: None).
136         imax : float or None
137             Maximum drain current (default: None).
138         ipeak : float or None
139             Peak current in the waveform (default: None).
140         v1 : float or None
141             Fundamental voltage component of the waveform (default: None).
142         rdc : float or None
143             DC resistance of the power amplifier (default: None).
144         N_IV_LINES : int
145             Number of IV curves to plot (default: 3)."""
146
147         #Properties which define the IV Curve Plane
148         self.IMAX    =    1
149         self.VKNEE   =    0
150         self.VMAX    =    None
151         self.DVFAIL  =    1
152         self.IFAIL   =    1e6
153
154         #Properties for the device bias
```

```
155         self.IQ      =    None
156         self.Vdd     =    None
157
158         #Static properties created here
159         self.RL      =    None
160
161         #properties that can be set
162         self.P1      =    None
163         self.CA      =    None
164
165         #properties that you poll
166         self.P0      =    None
167         self.de      =    None
168         self.imax    =    None
169         self.ipeak   =    None
170         self.v1      =    None
171         self.rdc     =    None
172
173         #plot properties
174         self.N_IV_LINES = 3     #number of fIV curves to plot
175
176     def set_op_point(self, P1=None, Vdd=None, Rl=None):
177         """
178         Sets the operating point of the load line model by updating the
               output power (P1), supply voltage (Vdd), and load resistance (
               Rl). If any of these parameters are not provided, the method
               uses the current instance values.
179         Parameters:
180             P1 (float, optional): Desired output power. Defaults to the
                   current value of self.P1.
```

```
181             Vdd (float, optional): Supply voltage. Defaults to the current
                    value of self.Vdd.
182             Rl (float, optional): Load resistance. Defaults to the current
                    value of self.RL.
183         Raises:
184             AssertionError: If the requested output power (P1) exceeds the
                    maximum allowable
185                             power for the given supply voltage (Vdd).
186         Side Effects:
187             Updates the instance variables self.Vdd, self.P1, and self.RL
                   with the new values.
188             Forces an update of all dependent values by calling self.
                   update().
189         Notes:
190             - The assertion includes a small numerical tolerance (1e-9) to
                    account for floating
191               point precision errors.
192             - This method is intended to ensure the operating point
                   remains within safe and
193               valid limits for the model.
194         """
195
196         #Use any values that haven't been explicitly set.
197         if P1 is None:
198             P1 = self.P1
199         if Vdd is None:
200             Vdd = self.Vdd
201         if Rl is None:
202             Rl = self.RL
203
```

```
204         #Check to make sure that the requested power is valid
205         assert P1 <= self.max_power(Vdd)+1e-9, "Requested output power is
                greater than the maximum at the requested operating point"
206
207         #If the assertion passes update the values
208         self.Vdd = Vdd; self.P1 = P1; self.RL = Rl
209
210         #now force an update of all other values
211         self.update()
212
213     def max_power(self, vdd_in):
214         """
215         Calculates the maximum output power for a given drain voltage (
                vdd_in).
216
217         The method computes the maximum power that can be delivered to the
                load resistor (RL) based on the supplied drain voltage and the
                knee voltage (VKNEE) of the device.
218
219         Args:
220             vdd_in (float): The input drain voltage.
221
222         Returns:
223             float: The maximum output power at the specified drain voltage
                    .
224         """
225         #reports the maximum power at a given drain voltage
226         v1_max = (vdd_in - self.VKNEE)
227         return ((v1_max)**2) / (2 * self.RL)
228
```

```
229     def calc_rl_opt(self, p1):
230         """
231         Calculate the optimum load resistance for a given power level
232 
233         This method computes the optimal load resistance for recovering
                the full voltage
234         swing of the RFPA loadline.
235 
236         Args:
237             p1 (float): Desired output power level.
238 
239         Returns:
240             float: A float reporting the optimum load resistance (in Ohms)
241         """
242         v1_max = (self.Vdd - self.VKNEE)
243         #calculate the optimum load resistance for the specified power
244         return ((v1_max)**2) / (2 * p1)
245 
246     def calc_vdd_opt(self, p1):
247         """
248         Calculate the optimum drain voltage (Vdd) for a given output power
                level.
249 
250         This method computes two possible optimum drain voltages based on
                the load resistance (RL), knee voltage (VKNEE), and the desired
                output power (p1). The calculation is derived from the load
                line analysis of a power amplifier.
251 
252         Args:
253             p1 (float): Desired output power level.
```

```
254
255         Returns:
256             tuple: A tuple containing two possible optimum drain voltages
                    (float).
257         """
258         # #Report the optimum drain voltage for a given power level
259         vk = self.VKNEE; Rl = self.RL;
260         # quantities for the quadratic formula
261         # a = 1; b = -2*vk; c = (vk**2 - 2*Rl*p1)
262         # Return the optimial drain bias voltages
263         return np.sqrt(2*Rl*p1) - vk, np.sqrt(2*Rl*p1) + vk
264
265     def calc_iq_opt(self, alpha):
266         """
267         Calculate the optimum drain current (Iq) to get the loadline back
                to a specific conduction angle
268
269         This method determines the required quiescent current required to
                achieve the specified conduction angle (alpha) whil preserving
                the fundamental voltage swing and load resistance. Together
                these in turn preserve the output power of the model.
270         Args:
271             alpha (float): Desired conduction angle (radians)
272
273         Returns:
274             float: The required quiescent current
275         """
276         # Report the quiescent current which will return the dll to the
                optimum value
277         v1 = self.v1; rl = self.RL
```

```
278         return ((2 * np.pi *v1) / (rl))*(np.cos(alpha/2) / (np.sin(alpha)
                - alpha))
279
280     def update(self):
281         """
282         Updates all key parameters of the load line model, including imax,
                conduction angle, efficiency, and related values.
283         This method performs the following steps:
284             1. Retrieves necessary input values (P1, RL).
285             2. Defines and minimizes a function to solve for the maximum
                   current (imax) that satisfies the load line condition.
286             3. Calculates the peak current (ipeak) as the difference
                   between imax and quiescent current (IQ).
287             4. Computes the conduction angle (CA) based on imax.
288             5. Calculates the DC output power (P0) using the supply
                   voltage (Vdd) and the DC current (I0).
289             6. Determines the fundamental output voltage component (v1).
290             7. Computes the drain efficiency (de) as the ratio of output
                   power (P1) to input power (P0).
291             8. Calculates the DC resistance (rdc) of the power amplifier.
292         Assumes that supporting methods such as calcI1, calcCA, and calcI0
                are implemented in the class.
293         Returns:
294             None
295         """
296         #UPDATE - updates all constituent values (CA, imax, efficiency,
                etc.)
297
298         #Grab values needed for the update
299         p1 = self.P1; rl = self.RL
```

```
300
301         #define a function to minimize for imax
302         f = lambda x: np.abs(np.sqrt((2*p1)/rl) - self.calcI1(imax=x, ca=
                self.calcCA(x)))
303
304         #now find the value of imax
305         lower_bound = np.max([0,self.IQ])
306         self.imax = fminbound(f, lower_bound, self.IMAX)
307         self.ipeak = self.imax - self.IQ
308
309         #now calculate the conduction angle
310         self.CA = self.calcCA(self.imax)
311
312         #now determine the dc power
313         self.P0 = self.Vdd * self.calcI0()
314
315         #now set the v1 component
316         self.v1 = np.sqrt(2*(self.P1)*self.RL)
317
318         #now determine the efficiency
319         self.de = self.P1 / self.P0
320
321         #determine the dc resistance of the PA
322         self.rdc = self.Vdd / self.calcI0()
323
324     def calcCA(self, imax):
325         """
326         Calculates the conduction angle for a given value of imax
327
328         Args:
```

```
329             imax (float): Peak value of Id
330         Returns:
331             float: Corresponding conduction angle in radians
332         """
333         #calculate the conduction angle from a value of imax
334         iq = self.IQ
335         #imax must be greatter than or equal to two times iq
336         imax = np.max([imax, 2*iq])
337         #calculate the new conduction angle in radians
338         return 2*np.arccos(iq / (iq - imax))
339 
340     def calcI1(self, imax=None, ca=None):
341         """
342         Calculates the fundamental current (I1) based on the specified
               peak current and conduction angle.
343         This method computes the fundamental component of the current
               waveform for a given peak current (`imax`) and conduction angle
                (`ca`). If either parameter is not provided, the method uses
               the instance's default values (`self.imax` and `self.CA`). The
               calculation accounts for the quiescent current (`self.IQ`) and
               handles the case where the peak current is less than the
               quiescent current.
344         Args:
345             imax (float, optional): Peak value of the drain current (Id).
                   If not provided, uses `self.imax`.
346             ca (float, optional): Conduction angle in radians. If not
                   provided, uses `self.CA`.
347         Returns:
348             float: The calculated fundamental current (I1) for the
                   specified conditions.
```

```
349         """
350         if imax is None:
351             imax = self.imax
352         if ca is None:
353             ca = self.CA
354 
355         #if IQ hasn't been specified yet, compute it here
356         if self.IQ is None:
357             iq = imax*np.cos(ca/2)/(np.cos(ca/2)-1)
358         else:
359             iq = self.IQ
360 
361         #calculate the specified peak current value
362         ipeak = imax - iq
363         #calculate the component of i1
364         if ipeak < iq: #if we've "lifted off"
365             return ipeak
366         else:
367             return (imax / (2*np.pi)) * ((ca - np.sin(ca))/(1-np.cos(ca/2)
                ))
368 
369     def calcI0(self,imax=None,ca=None):
370         """
371         Calculates the dc current (I0) based on the specified peak current
              and conduction angle.
372         This method computes the fundamental component of the current
            waveform for a given peak current (`imax`) and conduction angle
             (`ca`). If either parameter is not provided, the method uses
            the instance's default values (`self.imax` and `self.CA`). The
            calculation accounts for the quiescent current (`self.IQ`) and
```

```
            handles the case where the peak current is less than the
            quiescent current.
373         Args:
374             imax (float, optional): Peak value of the drain current (Id).
                    If not provided, uses `self.imax`.
375             ca (float, optional): Conduction angle in radians. If not
                    provided, uses `self.CA`.
376         Returns:
377             float: The calculated dc current (I0) for the specified
                    conditions.
378         """
379         if imax is None:
380             imax = self.imax
381         if ca is None:
382             ca = self.CA
383
384         #if Iq hasn't been specified yet, compute it directly
385         if self.IQ is None:
386             iq = imax*np.cos(ca/2)/(np.cos(ca/2)-1)
387         else:
388             iq = self.IQ
389
390         #calculate the specified peak current value
391         ipeak = imax - iq
392         #now return the DC component
393         if ipeak < iq:
394             #if we've lifted off, IQ is the dc current component
395             return iq
396         else:
397             #calculate the component of i0
```

```
398             return (imax / (2*np.pi)) * ((2*np.sin(ca / 2) - ca*np.cos(ca
                    / 2))/(1-np.cos(ca/2)))
399
400     def vd(self,theta,deg=False):
401         """
402         Calculates the drain voltage at a given conduction phase, theta.
403         Args:
404             theta (float): conduction angle in radians
405             deg (boolean, optional): interpret theta in degrees. Defaults
                    to false.
406         Returns:
407             float: The calculated drain voltage at conduction phase.
408         """
409         #convert to radians
410         if deg: theta = np.deg2rad(theta)
411         #return the drain voltage at theta
412         return self.Vdd - self.v1*np.cos(theta)
413
414     def id(self,theta,deg=False):
415         """
416         Calculates the drain current at a given conduction phase, theta.
417         Args:
418             theta (float): conduction angle in radians
419             deg (boolean, optional): interpret theta in degrees. Defaults
                    to false.
420         Returns:
421             float: The calculated drain current at conduction phase.
422         """
423         # Create a theta array
424         theta = np.array(theta)
```

```
425         id_vals = self.IQ + (self.imax - self.IQ)*np.cos(theta)
426         # Flatten the theta array
427         id_vals = id_vals.flatten()
428         # now concatenate the arrays
429         x = np.array([id_vals,np.zeros_like(id_vals)])
430         # return the results
431         return np.max(x,axis=0)
432
433     def plot_pdiss_contours(self, ax, *args,
434                             normalize_power_loss:bool = True,
435                             n_points:int=11,
436                             n_slices:int=11,
437                             cbar_label_args = None,
438                             contour_label=None,
439                             boundary_args=None,
440                             contour_ticks=None,
441                             contour_font_size=None,
442                             **kwargs):
443         """
444         Plot the dissipated power contours of the device on the IV plane.
445         Args:
446             ax (axes handle): Axes to plot the contours on.
447             *args: arguments to pass to plt.plot()
448             normalized_power_loss (bool, optional): normalize the power
                    loss to the maximum value (default=True)
449             n_points (int, optional): number of points to use for contour
                    generation(default=11)
450             n_slices (int, optional): number of slices to use for contour
                    generation (default=11)
451             cbar_label_args (optional): label arguments to pass on to cbar
```

```
            (default=None)
        contour_label (optional): labels to use for contours (default=
            None)
        boundary_args (optional): boundary arguments (default=None)
        contour_ticks (optional): ticks to use for contours (default=
            None)
        contour_font_size (optional): font size of contours (default=
            None)
        **kwargs (optional): keyword arguments to pass along to the
            plt.plot function.
    """

    # First, get the IV curves to plot
    prev_n_curves = self.N_IV_LINES
    self.N_IV_LINES = 3
    x, y = self.iv_curves
    self.N_IV_LINES = prev_n_curves

    # Next generate the starting points
    x_pts_start = np.linspace(0, self.VKNEE, n_slices)
    y_pts_start = (y[1,-1] / self.VKNEE) * x_pts_start

    # Initialize the raw data to plot
    x_pts = np.zeros((n_points,),dtype="float").repeat(n_slices)
    y_pts = np.zeros((n_points,),dtype="float").repeat(n_slices)
    z_pts = np.zeros((n_points,),dtype="float").repeat(n_slices)

    # Fill out the data
    pres_idx = 0

```

```
477         for slice_idx in np.arange(n_slices):
478             pres_vds_sweep = np.linspace(x_pts_start[slice_idx],self.VMAX,
                    n_points)
479             pres_ids_val   = y_pts_start[slice_idx]
480             for sweep_idx in np.arange(n_points):
481                 x_pts[pres_idx] = pres_vds_sweep[sweep_idx]
482                 y_pts[pres_idx] = pres_ids_val
483                 z_pts[pres_idx] = x_pts[pres_idx] * y_pts[pres_idx]
484                 pres_idx += 1
485
486         #normalize the power loss
487         if normalize_power_loss:
488             z_pts = z_pts / z_pts.max()
489
490         #now plot the contour
491         contour_plot = ax.tricontourf(x_pts, y_pts, z_pts, **kwargs)
492         cbar = plt.colorbar(contour_plot, ticks=contour_ticks)
493
494         if boundary_args is not None:
495             if "levels" in kwargs:
496                 levels = kwargs["levels"]
497             #add the boundary args and put in the levels
498             ax.tricontour(x_pts, y_pts, z_pts, levels=levels, **
                    boundary_args)
499
500         #apply the label arguments
501         if cbar_label_args is not None:
502             cbar.set_label(**cbar_label_args)
503
504     def plot_iv_curves(self, ax, ll_iv_curve:bool=True, device_iv_curves:
```

```
        bool=True, *args, **kwargs):
505     """
506     Plot the IV curves on a given axes
507     Args:
508         ax (axes handle): Axes to plot the curves on
509         ll_iv_curve (bool, optional): plot the IV curve for the
                current bias point (default=True)
510         device_iv_curves (bool, optional): plot the device load line
                iv curves. Uses the N_IV_LINES parameter to determine the
                number of curves.(default=True)
511         *args: arguments to pass along to the plt.plot function
512         **kwargs: keyword arguments to pass along to the plt.plot
                function.
513     Returns:
514         line handle: returns handle to the plotted line
515     """
516     # Plots the IV curves of the object. You can supply normal plot
            parameters
517
518     #build the points to plot
519     x = np.array([0, self.VKNEE, self.VMAX, self.VMAX+self.DVFAIL])
520
521     #logic for plotting this device's iv curves
522     N_IV_LINES = 0
523
524     #if we want to plot the current IV curve we are on
525     if ll_iv_curve:
526         N_IV_LINES += 1
527
528     #if we want to plot the device iv curves
```

```
529         if device_iv_curves:
530             N_IV_LINES += self.N_IV_LINES - 1
531 
532         #construct the container for the IV curves
533         y = np.zeros((4, N_IV_LINES), dtype="float")
534 
535         #build the curve we are travelling along
536         if ll_iv_curve:
537             y[:,0] = np.array([0, self.IQ, self.IQ, self.IFAIL], dtype="
                float")
538 
539         #now build the rest of the lines we wish to plot
540         if device_iv_curves:
541             Ivals = np.linspace(0, self.IMAX, self.N_IV_LINES-1)
542             for yi in np.arange(0, Ivals.size):
543                 y[:,yi+ll_iv_curve] = np.array([0, Ivals[yi], Ivals[yi],
                    self.IFAIL])
544 
545         #now plot the line
546         return ax.plot(x,y,*args,**kwargs)
547 
548     def plot_bias(self, ax, *args, **kwargs):
549         """
550         Plot the bias point.
551         Args:
552             ax (axes handle): handle to the axes to plot on.
553             *args: arguments to pass to the plt.plot function
554             **kwargs: keyword arguments to pass to the plt.plot function
555         Returns:
556             line handle: returns handle to the plotted line
```

```
557         """
558         #Plot the bias of the object
559 
560         #get the x and y coordinates of the bias point
561         x = self.Vdd; y = self.IQ
562 
563         #now plot the lines
564         return ax.plot(x,y,*args,**kwargs)
565 
566     def plot_dll(self, ax, *args, **kwargs):
567         """
568         Plot the dynamic load line trajectory.
569         Args:
570             ax (axes handle): handle to the axes to plot on.
571             *args: arguments to pass to the plt.plot function
572             **kwargs: keyword arguments to pass to the plt.plot function
573         Returns:
574             line handle: returns handle to the plotted line
575         """
576         #plot the dynamic load line of the object
577 
578         if self.imax < 2*self.IQ:
579             #there are two points to plot
580             x = np.array([self.Vdd - self.v1, self.Vdd+self.v1], dtype="
                float")
581             y = np.array([self.IQ+self.calcI1(), self.IQ-self.calcI1()],
                dtype="float")
582         else:
583             #there are three points to plot
584             x = np.array([(self.Vdd-self.v1), (self.Vdd - self.v1*np.cos(
```

```
                self.CA/2)), (self.Vdd + self.v1)], dtype="float")
585             y = np.array([self.imax, 0, 0], dtype="float")
586
587         #now plot the lines
588         return ax.plot(x,y,*args,**kwargs)
589
590     @property
591     def Gp(self) -> float:
592         """
593         Returns the current power gain.
594         """
595         return (1/(4*np.pi))*(self.CA - np.sin(self.CA))*(1 - np.cos(self.
                CA / 2))
596
597     @property
598     def iv_curves(self) -> tuple[np.ndarray, np.ndarray]:
599         """
600         Returns the current IV curves as a tuple of (x points, y points)
601         """
602         x = np.array([0, self.VKNEE, self.VMAX, self.VMAX+self.DVFAIL])
603         y = np.zeros((4, self.N_IV_LINES-1), dtype="float")
604
605         #calculate the IV curves
606         Ivals = np.linspace(0, self.IMAX, self.N_IV_LINES-1)
607         for yi in np.arange(0, Ivals.size):
608             y[:,yi] = np.array([0, Ivals[yi], Ivals[yi], self.IFAIL])
609
610         # return the results
611         return x, y
```

Appendix B

Computational Network Analysis using Power Waves

This appendix presents the approach to microwave network analysis used in this work.

B.1 Power Waves

From [84] the reflected and incident power waves are:

$$a_k = \frac{V_k + Z_k I_k}{2\sqrt{|\Re\{Z_k\}|}} \quad \text{and} \quad b_k = \frac{V_k - Z_k^* I_k}{2\sqrt{|\Re\{Z_k\}|}} \tag{B.1}$$

where k denotes the port index, V_k is the voltage between the port terminals, I_k is the current into the port, and Z_k is the reference impedance for the port. Scattering parameters (S-parameters) are the coefficients for a set of linear equations which relate the incident, a, and reflected, b power waves at each port of a network. The reference impedance Z_k must be known for the power waves and S-parameters to be meaningful. Typically the reference impedance is chosen to be 50Ω; however, other values such as 1Ω are also used for computational simplicity. Additionally, it can be useful to make the power aves equal to the corresponding source impedances presented at each port,

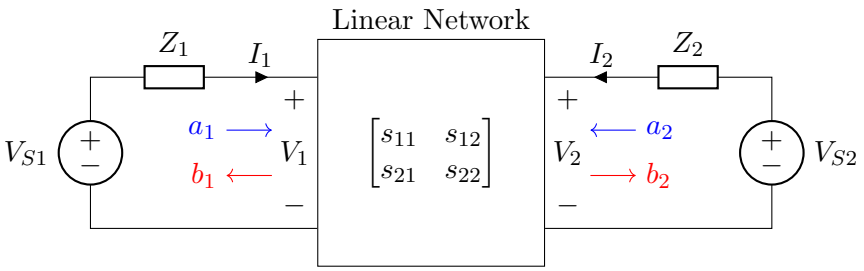


Figure B.1: The linear two-port network presented in the beginning of Chapter 4.

i.e. $Z_k = Z_{S,k}$. When this condition is satisfied we say that the circuit is "matched" and the S-parameters become equal to the input reflection coefficients and transmission coefficients from each port.

A method for changing the reference impedance of S-parameters is presented in [177] and may be found in Chapter 5. However, sometimes it is more useful to directly transform a given set of power waves from one reference impedance to another. The derivation of the close-form solution suitable for this is as follows.

(B.1) is re-written to solve for the port voltage and current [84]:

$$V_k = K_k \left(Z_k^* a_k + Z_k b_k \right) \tag{B.2}$$

$$I_k = K_k \left(a_k - b_k \right) \tag{B.3}$$

where

$$K_k = \frac{\operatorname{sign}\left(\Re\left\{ Z_k \right\} \right)}{\sqrt{\left| \Re\left\{ Z_k \right\} \right|}} \tag{B.4}$$

The corresponding matrix equation for (B.2) and (B.3) is

$$\begin{bmatrix} Z_k^* & Z_k \\ 1 & -1 \end{bmatrix} \begin{bmatrix} a_k \\ b_k \end{bmatrix} = \begin{bmatrix} V_k \frac{1}{K_k} \\ I_k \frac{1}{K_k} \end{bmatrix} \tag{B.5}$$

Asserting that (B.5) corresponds to the system with the power waves at the **desired** reference impedance, $Z_{k,2}$, (B.2) and (B.3) may be used to substitute V_k and I_k with the power waves and parameters belonging to the **initial** reference impedance, $Z_{k,1}$. This results in the corresponding matrix equation:

$$\begin{bmatrix} Z_{k,2}^* & Z_{k,2} \\ 1 & -1 \end{bmatrix} \begin{bmatrix} a_{k,2} \\ b_{k,2} \end{bmatrix} = \begin{bmatrix} \frac{K_{k,1}}{K_{k,2}} \left(Z_{k,1}^* a_{k,1} + Z_{k,1} b_{k,1} \right) \\ \frac{K_{k,1}}{K_{k,2}} \left(a_{k,1} - b_{k,1} \right) \end{bmatrix} \tag{B.6}$$

This is sufficient to directly compute the power waves with the updated reference impedance, however; the close-form solution is readily found as:

$$\begin{aligned} a_{k,2} &= \frac{K_{k,1}}{K_{k,2}} \frac{a_{k,1} \left(Z_{k,1}^* + Z_{k,2} \right) + b_{k,1} \left(Z_{k,1} - Z_{k,2} \right)}{2 \Re\left\{ Z_{k,2} \right\}} \\ b_{k,2} &= \frac{K_{k,1}}{K_{k,2}} \frac{a_{k,1} \left(Z_{k,1}^* - Z_{k,2} \right) + b_{k,1} \left(Z_{k,1} + Z_{k,2}^* \right)}{2 \Re\left\{ Z_{k,2} \right\}} \end{aligned} \tag{B.7}$$

B.2 Network Analysis

This section presents a straightforward approach to network analysis which draws from common circuit theory principles such as power-waves and Kirchoff's Current Law (KCL). The approach discussed here directly solves the power waves at each element of a system and presents a relatively straightforward approach to power-wave network analysis and is useful for studying network behavior and analyzing power waves throughout a circuit. The primary advantage of this approach is its relative simplicity. For more advanced and computationally efficient methods the reader might be interested in an approach such as that discussed in [178].

B.2.1 Boundary Conditions

Each source applied to excite and/or load the circuit being analyzed provides a single equation to the system. The boundary conditions presented here are discussed in greater detail in Chapter 6. In general, this boundary condition is:

$$b_n - a_n\Gamma_{S0,n} = A_{0,n}(1 - \Gamma_{S0,n}) \tag{B.8}$$

Where n is the source index, $\Gamma_{S0,n}$ is the reflection coefficient of the source, $A_{0,n}$ is the source excitation.[1] If only an impedance is presented at a port, i.e. an excitation is not present, than $A_{0,n} = 0$ and (B.8) simply reduces to:

$$b_n - a_n\Gamma_{S0,n} = 0 \tag{B.9}$$

Likewise, if the source is matched, i.e. $\Gamma_{S0,n} = 0$, then (B.8) reduces to

$$b_n = A_{0,n} \tag{B.10}$$

Finally, if the source is both matched and does not have an excitation (B.8) simply reduces to

$$b_n = 0 \tag{B.11}$$

[1] Note that the power-waves of (B.8) b_n and a_n are **source referred**, i.e. a_n is the power wave incident on the source. This should not be confused with (6.4) of Chapter 6 where the power waves are **network referred**, i.e. a_n is incident on the network.

B.2.2 Network Parameters

Each network used in circuit analysis provides a number of equations equal to the number of ports. For instance, the network of Fig. B.1 provides exactly two equations because it has two ports. The equation for port k of a linear N-port network is:

$$\sum_{i=1}^{N} a_i s_{k,i} - b_k = 0 \tag{B.12}$$

The general matrix form of (B.12) for a N-port network is:

$$\begin{bmatrix} s_{11} & s_{12} & s_{13} & \cdots & s_{1N} & -1 & 0 & 0 & \vdots & 0 \\ s_{21} & s_{22} & s_{23} & \cdots & s_{2N} & 0 & -1 & 0 & \vdots & 0 \\ s_{31} & s_{32} & s_{33} & \cdots & s_{3N} & 0 & 0 & -1 & \vdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ s_{N1} & s_{N2} & s_{N3} & \cdots & s_{NN} & 0 & 0 & 0 & \vdots & -1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \vdots \\ b_{N-1} \\ b_N \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 0 \end{bmatrix} \tag{B.13}$$

B.2.3 Nodal Equations

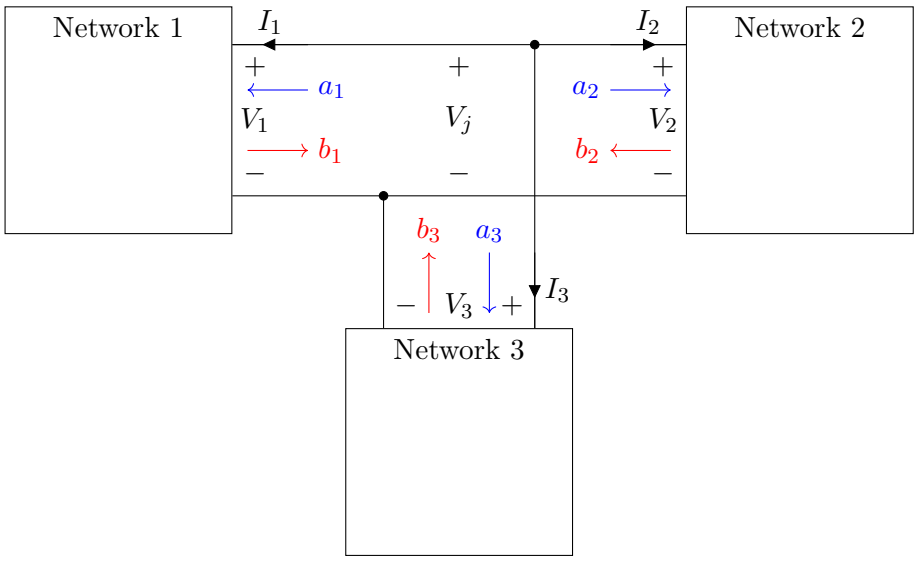


Figure B.2: A junction of three ports.

The connection point of two or more networks also results in a contribution to the linear system of equations. The nodal equations are those which satisfy the nodes voltage and current

equations. Each node will yield a number of linearly independent equations equal to the number of ports connected to it.

The relevant equations relating the currents and voltages at each port are:

$$\sum_{k=1}^{N} I_k = 0 \tag{B.14}$$

$$V_k = V_j|_{j \neq k} \tag{B.15}$$

Where, (B.14) states that the sum of all currents leaving a node must equal 0, and (B.15) states that the voltages across each port, V_k, must be equal. (B.14) yields **one** linearly independent equation while (B.15) yields $N-1$ linearly independent equations (with N being the number of ports connected to the node). Referring to Fig. B.2, the current equation will be:

$$I_1 + I_2 + I_3 = 0, \tag{B.16}$$

and the two voltage relations resulting from the junction are

$$V_1 = V_2 \quad \text{and} \quad V_1 = V_3. \tag{B.17}$$

Using (B.14) to substitute for each current in (B.14) results in the power wave equivalent:

$$\left[\sum_{k=1}^{N} a_k - \sum_{k=1}^{N} b_k\right] = 0, \tag{B.18}$$

which for the junction of Fig. B.2 becomes:

$$a_1 + a_2 + a_3 - b_1 - b_2 - b_3 = 0 \tag{B.19}$$

Likewise, using (B.15) to substitute out each voltage in (B.15) gives:

$$\left(Z_k^* a_k - Z_j^* a_j\right) + \left(Z_k b_k - Z_k b_j\right)|_{k \neq j} = 0.$$

If the reference impedance for all equations are equal and real then this relation reduces to:

$$(a_k - a_j) + (b_k - b_j)|_{k \neq j} = 0, \tag{B.20}$$

which will yield the following two linearly independent equations for the junction of Fig. B.2:

$$\begin{aligned}(a_1 - a_2) + (b_1 - b_2) = 0 \\ (a_1 - a_3) + (b_1 - b_3) = 0\end{aligned} \tag{B.21}$$

Altogether, the general matrix form of a junction with N ports connected to it is:

$$\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 & -1 & -1 & -1 & \cdots & -1 \\ 1 & -1 & 0 & \cdots & 0 & 1 & -1 & 0 & \cdots & 0 \\ 1 & 0 & -1 & \cdots & 0 & 1 & 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 1 & 0 & 0 & \cdots & -1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ \vdots \\ a_N \\ b_1 \\ b_2 \\ b_3 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{B.22}$$

For the three-port network illustrated in Fig. B.2, (B.22) becomes:

$$\begin{bmatrix} 1 & 1 & 1 & -1 & -1 & -1 \\ 1 & -1 & 0 & 1 & -1 & 0 \\ 1 & 0 & -1 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{B.23}$$

Elements that have a grounded or short-circuit port may be handled in a manner similar to that of the general junction node. However as elements may have internally grounded nodes which are not accounted for explicitly in the nodal formulation, Kirchoff's current no longer applies. Fortunately, another conditions–namely that the junction voltage is $0V$ may be applied in its place. In other words, consider the junction as illustrated in Fig. B.2 but now this junction represents a

part of the global ground node. In this case, $V_j = 0V$ and therefore (B.15) becomes:

$$V_k = V_j|_{j \neq k} = 0V \tag{B.24}$$

This condition can be enforced by replacing the current equation (B.19) with the power-wave equivalent to $V_1 = 0V$. This results in the following power wave equation:

$$a_1 + b_1 = 0 \tag{B.25}$$

and therefore the general form of the nodal matrix may be re-written as:

$$\begin{bmatrix} 1 & 0 & 0 & \cdots & 0 & 1 & 0 & 0 & \cdots & 0 \\ 1 & -1 & 0 & \cdots & 0 & 1 & -1 & 0 & \cdots & 0 \\ 1 & 0 & -1 & \cdots & 0 & 1 & 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & -1 & 1 & 0 & 0 & \cdots & -1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ \vdots \\ a_N \\ b_1 \\ b_2 \\ b_3 \\ \vdots \\ b_N \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \tag{B.26}$$

If the three-port junction represents the ground node for the circuit it may be re-written as:

$$\begin{bmatrix} 1 & 0 & 0 & 1 & 0 & 0 \\ 1 & -1 & 0 & 1 & -1 & 0 \\ 1 & 0 & -1 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \tag{B.27}$$

Once the **local** nodal matrix is generated, it may be converted to the global circuit matrix by multiplying against a mapping matrix, T. If the local junction matrix is of size $n \times n$ and the

global system matrix has N columns, T will be of size $n \times N$ and the resulting addition to the global system matrix will be $n \times N$. In general, T is a $n \times N$ sparse matrix with $T[x, y] = 1$ where x is a list of indices corresponding to the local nodal index and y is a list of indices of the corresponding global indices.

B.3 Scattering Matrices of Common Elements

Here we review the derivation of the S-parameters common two-port elements used in circuit analysis. These are the parameters. Here we assume that the S-parameters for each element are extracted with sources of port impedance Z_0 which may be a complex value to avoid loss of generality.

B.3.1 General Impedance

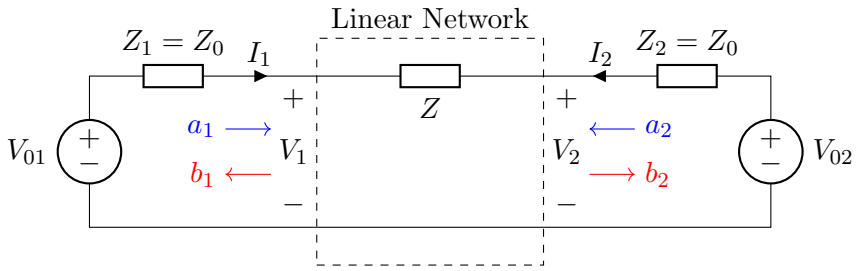


Figure B.3: Circuit schematic for finding the general S-parameters of an impedance element.

The general impedance element is the simplest form of two-port circuit element and will be converted to a capacitor and inductor element in the following sub-section. Assuming $V_{02} = 0$, the voltages and currents around the network are

$$\begin{aligned} V_1 &= V_{01}\frac{Z + Z_0}{Z + 2Z_0}, \quad V_2 = V_{01}\frac{Z_0}{Z + 2Z_0}, \\ I_1 &= V_{01}\frac{1}{Z + 2Z_0}, \quad I_2 = -I_1 = -V_{01}\frac{1}{Z + 2Z_0} \end{aligned} \tag{B.28}$$

where Z_0 is the reference impedance for all S-parameters and Z is the value of the impedance

element. Using (B.1) the incident power power wave on port 1, a_1, is:

$$\begin{aligned} b_1|_{V_{02}=0} &= K(V_{01}\frac{Z+Z_0}{Z+2Z_0} + Z_0\frac{1}{Z+2Z_0}) \\ &= KV_{01}\frac{Z+2Z_0}{Z+2Z_0} = KV_{01}, \end{aligned} \tag{B.29}$$

where

$$K = \frac{1}{2\sqrt{|\Re\{Z_0\}|}}$$

Likewise the scattered wave at port 1, b_1, is:

$$\begin{aligned} b_1|_{V_{02}=0} &= K\left(V_{01}\frac{Z+Z_0}{Z+2Z_0} - V_{01}\frac{Z_0^*}{Z+2Z_0}\right) \\ &= KV_{01}\frac{Z+Z_0-Z_0^*}{Z+2Z_0} = KV_{01}\frac{Z+2\Im\{Z_0\}}{Z+2Z_0} \end{aligned} \tag{B.30}$$

Finally, the scattered wave at port 2, b_2, is:

$$\begin{aligned} b_2|_{V_{02}=0} &= K\left(V_{01}\frac{Z_0}{Z+2Z_0} + V_{01}\frac{Z_0^*}{Z+2Z_0}\right) \\ &= KV_{01}\frac{Z+Z_0+Z_0^*}{Z+2Z_0} = KV_{01}\frac{Z+2\Re\{Z_0\}}{Z+2Z_0} \end{aligned} \tag{B.31}$$

The scattering parameters s_{11} and s_{21} are computed from (B.29), (B.30) and (B.31) as:

$$s_{11} = \left.\frac{b_1}{a_1}\right|_{V_{02}=0} = \frac{Z+2\Im\{Z_0\}}{Z+2Z_0} \quad \text{and} \quad s_{21} = \left.\frac{b_2}{a_1}\right|_{V_{02}=0} = \frac{2\Re\{Z_0\}}{Z+2Z_0}. \tag{B.32}$$

Because the impedance element of Fig. B.3 is a reciprocal and symmetric network $s_{11} = s_{22}$ and $s_{21} = s_{12}$. Therefore the S-parameter matrix of the impedance element is expressed as:

$$S_{\text{impedance}} = \frac{1}{Z+2Z_0}\begin{bmatrix} Z+2\Im\{Z_0\} & 2\Re\{Z_0\} \\ 2\Re\{Z_0\} & Z+2\Im\{Z_0\} \end{bmatrix} \tag{B.33}$$

B.3.2 Resistor

The impedance function of a resistor of value R is simply:

$$Z_R = R \tag{B.34}$$

which, when substituted for Z in (B.32) results in the S-parameters for a resistor:

$$S_{\text{resistor}} = \frac{1}{R+2Z_0}\begin{bmatrix} R+2\Im\{Z_0\} & 2\Re\{Z_0\} \\ 2\Re\{Z_0\} & R+2\Im\{Z_0\} \end{bmatrix} \tag{B.35}$$

B.3.3 Inductor

The impedance of an inductor is:

$$Z_{inductor}(p) = pL \tag{B.36}$$

where p is the complex frequency variable and L is the inductance in Henries. Now $Z_{inductor}$ may be substituted for Z in (B.33) leading to the following S-parameter matrix:

$$S_{\text{inductor}} = \frac{1}{pL + 2Z_0}\begin{bmatrix} pL + 2\Im\{Z_0\} & 2\Re\{Z_0\} \\ 2\Re\{Z_0\} & pL + 2\Im\{Z_0\} \end{bmatrix} \tag{B.37}$$

B.3.4 Capacitor

The impedance of an inductor is:

$$Z_{\text{capacitor}}(p) = \frac{1}{pC} \tag{B.38}$$

where p is the complex frequency variable and C is the capacitance in Farads. Now $Z_{capacitor}$ may be substituted for Z in (B.33) leading to the following S-parameter matrix:

$$S_{\text{capacitor}} = \frac{1}{\frac{1}{pC} + 2Z_0}\begin{bmatrix} \frac{1}{pC} + 2\Im\{Z_0\} & 2\Re\{Z_0\} \\ 2\Re\{Z_0\} & \frac{1}{pC} + 2\Im\{Z_0\} \end{bmatrix}$$

which has a pole in the response at dc. This pole is removed by multiplying all equations by $\frac{pC}{pC}$ leading to the following form:

$$S_{\text{capacitor}} = \frac{1}{1 + 2CZ_0 p}\begin{bmatrix} 1 + 2C\Im\{Z_0\}p & 2C\Re\{Z_0\}p \\ 2C\Re\{Z_0\}p & 1 + 2C\Im\{Z_0\}p \end{bmatrix} \tag{B.39}$$

B.3.5 Transmission Line

From [164] the S-parameters of a transmission line are:

$$S_{\text{transmission line}} = \frac{1}{2Z_cZ_0 + \left(Z_c^2 + Z_0^2\right)\tanh(\gamma\ell)} \begin{bmatrix} j2Z_c\Im\{Z_0\} + \left(Z_c^2 - |Z_0|^2\right)\tanh(\gamma\ell) & (2\Re\{Z_0\}Z_c)/(\cosh\gamma\ell) \\ (2\Re\{Z_0\}Z_c)/(\cosh\gamma\ell) & j2Z_c\Im\{Z_0\} + \left(Z_c^2 - |Z_0|^2\right)\tanh(\gamma\ell) \end{bmatrix},$$

where Z_c is the characteristic impedance, Z_0 is the reference impedance, ℓ is the physical length of the transmission line, and γ is the propagation constant of the transmission line. If the transmission line is lossless $\gamma\ell$ may be written as:

$$\gamma\ell|_{\alpha\to 0} = j\beta\ell = j\theta,$$

where θ is the the electrical length of the transmission line in radians.

Appendix C

Generalized Tuner Convergence Criteria

The problem illustrated in Fig. 6.6 is a linear system where Γ_{in} is a constant. For nonlinear DUTs, Γ_{in} is a function of several variables such as bias, power, and temperature. For such cases, we start with an *estimated* value, Γ'_{in}, which is used in (6.12) to find an estimate of B_0. Then an estimate T_{0_1} is found from (6.15) and after n iterations we arrive at

$$T_{0_n} = T_{0_1} \left(C_1 \Delta_{\Gamma_{in}}\right)^{n-1} + C_1 C_2 \sum_{k=0}^{n-2} \left(C_1 \Delta_{\Gamma_{in}}\right)^k , \tag{C.1}$$

where $n \geq 2$ and T_{0_1} is the first guess of T_0. The coefficients C_1, C_2 and $\Delta_{\Gamma_{in}}$ are:

$$C_1 = \frac{\Gamma_S - \Gamma_{S0}}{\left(1 - \Gamma_{S0}\Gamma_{in}\right)\left(1 - \Gamma_S \Gamma'_{in}\right)}, \quad C_2 = \frac{\left(B_0 - \mathbb{S}_0\right)\left(1 - \Gamma_{in}\right)\left(1 - \Gamma_{S0}\Gamma'_{in}\right)}{1 - \Gamma_{S0}}, \quad \text{and} \tag{C.2}$$

$$\Delta_{\Gamma_{in}} = \Gamma_{in} - \Gamma'_{in}.$$

Fig. 6.7 outlines the iterative procedure where the approximate solution for T_0 tends to converge to the exact solution. Here we are assuming that the DUT is linear but Γ_{in} is not well known, since it could depend in reality on power, bias, etc. Evaluating (C.1) as $n \to \infty$ yields:

$$\lim_{n\to\infty} T_{0_n} = C_1 C_2 \sum_{k=0}^{\infty} \left(C_1 \Delta_{\Gamma_{in}}\right)^k = T_0$$

when

$$\left|C_1 \Delta_{\Gamma_{in}}\right| < 1 \ . \tag{C.3}$$

Equation C.3 may be used to establish an upper bound on the acceptable error magnitude in Γ_{in} by rewriting it in the following form:

$$\left|\frac{\Delta_{\Gamma_{in}}}{1 - \Gamma_{S0}\Gamma_{in}}\right| < \left|\frac{1 - \Gamma_S \Gamma'_{in}}{\Gamma_S - \Gamma_{S0}}\right|, \tag{C.4}$$

where $\Delta_{\Gamma_{in}}$ can be interpreted as the magnitude of the error in Γ_{in}. If the source is matched, i.e. $\Gamma_{S0} \to 0$, (C.4) becomes:

$$|\Delta_{\Gamma_{in}}| < \left| \frac{1}{\Gamma_S} - \Gamma'_{in} \right|, \tag{C.5}$$

where the maximum error magnitude in Γ_{in} is bounded by the desired reflection coefficient, Γ_S, and the estimated input reflection coefficient, Γ'_{in}. Another way to interpret (C.5) is as a sensitivity to large-signal variation in Γ_{in} for a given small signal Γ'_{in} and desired reflection coefficient Γ_S.

Equation C.3 also defines a circular boundary of convergence for Γ'_{in} and Γ_s. The boundary of convergence for Γ'_{in} with center $C_{\Gamma'_{in}}$, and radius, $R_{\Gamma'_{in}}$ is:

$$C_{\Gamma'_{in}} = \frac{\Gamma_{in} - |\gamma_a|^2 \Gamma_S^*}{1 - |\gamma_a \Gamma_S|^2} \quad \text{and} \quad R_{\Gamma'_{in}} = \frac{\sqrt{|\Gamma_{in}|^2 + |\gamma_a|^2 \left(1 - 2\Re\left\{\Gamma_S \Gamma_{in}\right\}\right)}}{\left|1 - |\gamma_a \Gamma_S|^2\right|},$$

where:

$$\gamma_a = \frac{1 - \Gamma_{S0}\Gamma_{in}}{\Gamma_S - \Gamma_{S0}} \ .$$

Whether or not the region of convergence is interior or exterior to the boundary is determined by evaluating the following condition:

$$|C_1 \Delta_{\Gamma_{in}}| < 1 \,|_{\Gamma'_{in} = C_{\Gamma'_{in}}}$$

If true, then the interior to the boundary is the convergent region. If false, then the exterior of the boundary is the convergent region.

Likewise, the boundary of convergence for Γ_S is:

$$C_{\Gamma_S} = \frac{\Gamma_{S0} - |\gamma_b|^2 \Gamma'^*_{in}}{1 - |\gamma_b \Gamma'_{in}|^2} \quad \text{and} \quad R_{\Gamma_S} = |\gamma_b| \frac{\sqrt{1 + |\Gamma'_{in}\Gamma_{S0}|^2 - 2\Re\left\{\Gamma'_{in}\Gamma_{S0}\right\}}}{\left|1 - |\gamma_b \Gamma'_{in}|^2\right|}, \tag{C.6}$$

where:

$$\gamma_b = \frac{1 - \Gamma_{S0}\Gamma_{in}}{\Gamma_{in} - \Gamma'_{in}}.$$

The corresponding region of convergence is determined in a manner similar to the Γ'_{in} boundary except the following condition is evaluated:

$$|C_1 \Delta_{\Gamma_{in}}| < 1 \,|_{\Gamma_S = C_{\Gamma_S}}$$

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