GaN MMICs for In-Band Full-Duplex Phased Arrays

by

Seth Johannes

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Committee Members:

Zoya Popović, Chair

Dejan Filipović

Cody Scarborough

Scott Schafer

Jeffrey Herd

Johannes, Seth (Ph.D., Electrical Engineering)

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With the ever-increasing wireless data usage, methods to increase spectrum efficiency have been a point of interest. In the ideal case, in-band full-duplex or simultaneous transmit and receive (STAR) doubles the spectrum efficiency of a communications system, allows for integrated sensing and communications (ISAC), and several other applications. Due to high self-interference during full-duplex operation, the RF front-end has a significant impact on system performance, especially on the allowable transmit and receive power. This thesis investigates high-power GaN components and front-ends, and antenna arrays for in-band full-duplex phased arrays. Designed and measured GaN single-pole double-throw switches (SPDT) and a variable attenuator is presented. Two front-end GaN MMICs for analog-assisted digital self-interference cancellation in an aperture-level in-band full-duplex system are demonstrated at S-band and X-band. A linear antipodal Vivaldi array is designed and measured, in addition to a throughput comparison between half-duplex and full-duplex when there is added noise during full-duplex operation. Considering element-level in-band full-duplex operation, an integrated full-duplex front-end with a novel quasi-circulator is demonstrated.

Dedication

To my parents and siblings, especially my mom, who told me "it's okay if you are a business major".

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Chapter 1

Introduction

1.1 Motivation

With increasing wireless data usage [1], network providers are continuously trying to increase the amount of wireless data they can support. Fig. 1.1 shows the increase in wireless data from 2008 to 2016, with more than a tripling of wireless traffic from 2014 to 2016. One way for wireless network providers to support the data increase is by purchasing wider frequency bands, but this comes at a significant in addition to the limited available spectrum from the FCC [11]. Therefore, the spectrum

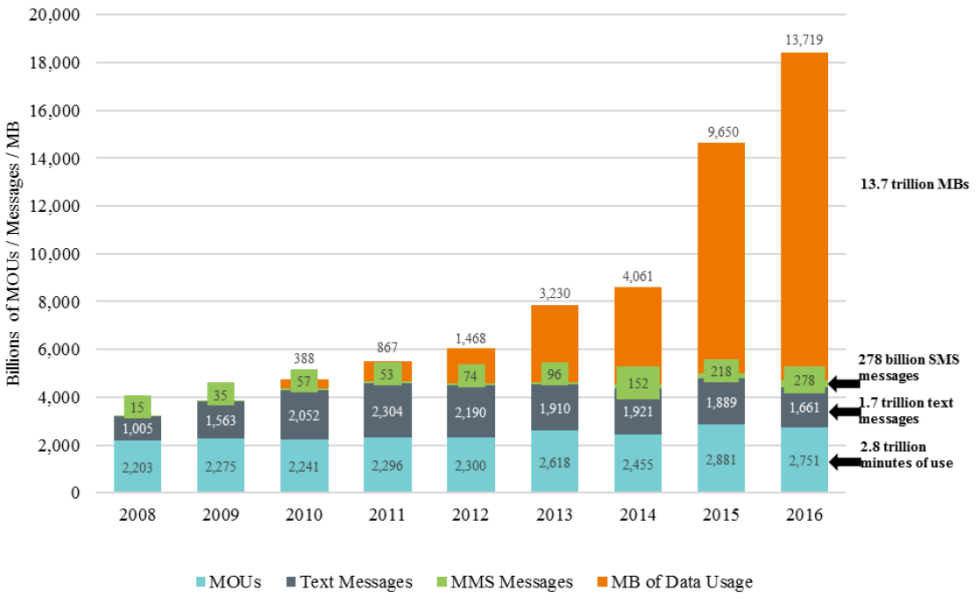


Figure 1.1: Annual minutes, messages, and megabytes of wireless traffic from 2008 to 2016 [1]. From 2014 to 2016 wireless traffic more than tripled, motivating increased wireless spectrum efficiency.

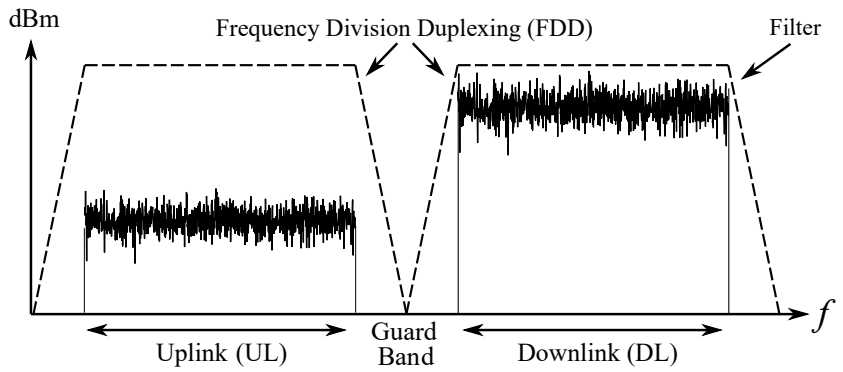


Figure 1.2: Frequency division duplexing spectrum used to mitigate "self-interference" between uplink (UL) and downlink (DL). LTE band 7 (IMT-E) from 2.50 GHz to 2.69 GHz, uses FDD with UL from $2.50 - 2.57$ GHz, DL from $2.62 - 2.69$ GHz, and a guard band from $2.57 - 2.62$ GHz.

efficiency (bits/s/Hz), which quantifies the amount of data in a 1 GHz, bandwidth of a network of a network has become a key metric. A common technique for increasing spectrum efficiency is redesigning more complex signal modulation schemes, such as orthogonal frequency division multiplexing (OFDM) and code division multiple access (CDMA) [12]. In a cellular system, e.g. LTE band 7 (IMT-E) using frequency division duplexing (FDD) as shown in Fig. 1.2, the uplink (UL) ranges from $2.50 - 2.57$ GHz and the downlink (DL) ranges from $2.62 - 2.69$ GHz, requiring expensive high-Q filters to prevent leakage between the bands also referred to as "self-interference". A possible approach for increased spectrum efficiency is the implementation of in-band full-duplex (IBFD) or simultaneous transmit and receive (STAR), allowing for concurrent transmit and receive signals in a single frequency band, ideally doubling spectrum efficiency, however it has been shown in difficult to achieve in practice [5].

1.2 In-Band Full-Duplex

To avoid self-interference between transmit and receive, time division duplexing (TDD) can also be used such as in LTE band 42 (CBRS) from $3.4{-}3.6$ GHz. These duplexing schemes are shown Fig. 1.3a and Fig. 1.3a. Systems with TDD can also be refereed to as half-duplex (HD), with non simultaneous transmit and receive signals. For IBFD operation as shown in Fig. 1.3c, there

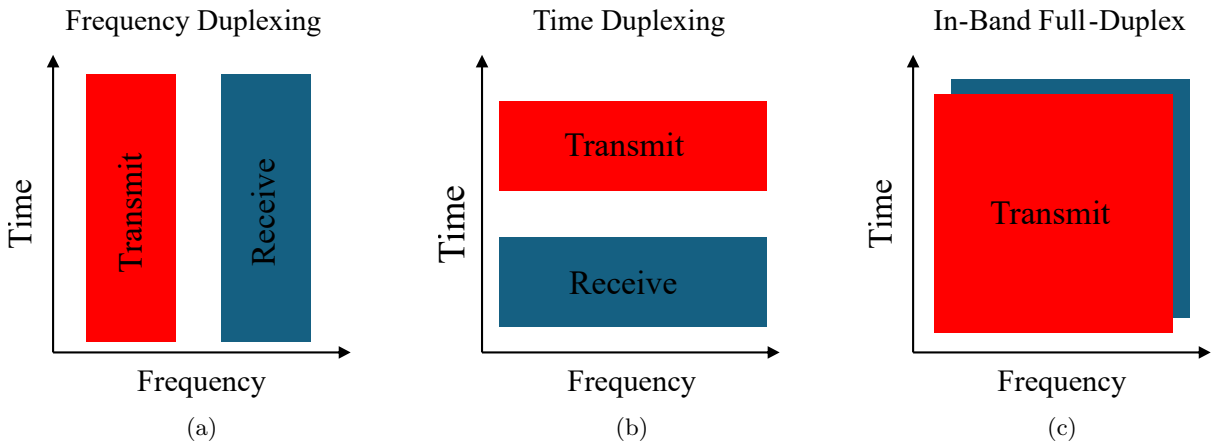


Figure 1.3: Wireless system with (a) frequency division duplexing and (b) time division duplexing for self-interference mitigation with equal spectrum efficiency. (c) In-band full-duplex operation, with overlapping transmit and receive signals, ideally doubles the spectrum efficiency of a wireless network.

is no time or frequency division between signals, instead transmit and receive occupy the same frequency and time. An acoustic analogy is a conversation between two people where both are continuously talking and understand each other perfectly.

As expected, IBFD operation leads to high self-interference from transmit to receive, masking the received signal of interest, which can be mitigated by self-interference cancellation (SIC). This can be done in the propagation, analog, and digital domains as shown in Fig. 1.4. For SIC to be applied, the receive chain should remain linear, with the received signal being a summation of self-interference and the received signal of interest. In a given IBFD system, the required level of ideal SIC is a receiver noise floor that matches that of half-duplex operation with no transmit signal. Applying this to e.g., WiFi as shown in [5], with a transmit power of 20 dBm and a receiver noise floor of -90 dBm, the ideal SIC level is 110 dB. To reach this level, typically cancellation techniques in all three domains are required.

When implemented in a practical environment, an IBFD system has multiple coupling paths, as shown in Fig. 1.5a. Paths 1 and 2 are direct and fixed object refection paths, where Path 1 is independent of the environment, and both paths are time invariant. Path 3 is a moving object

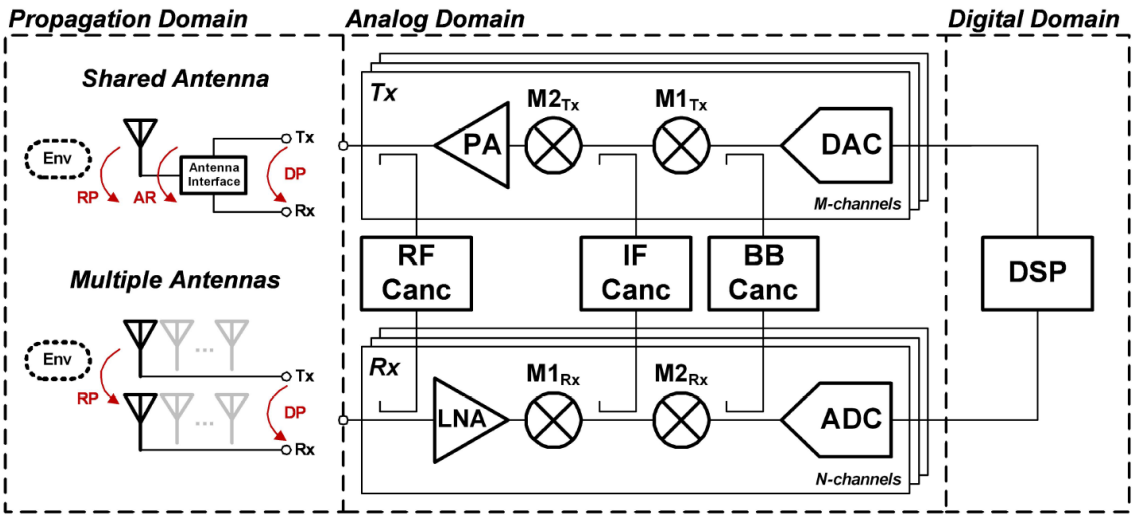
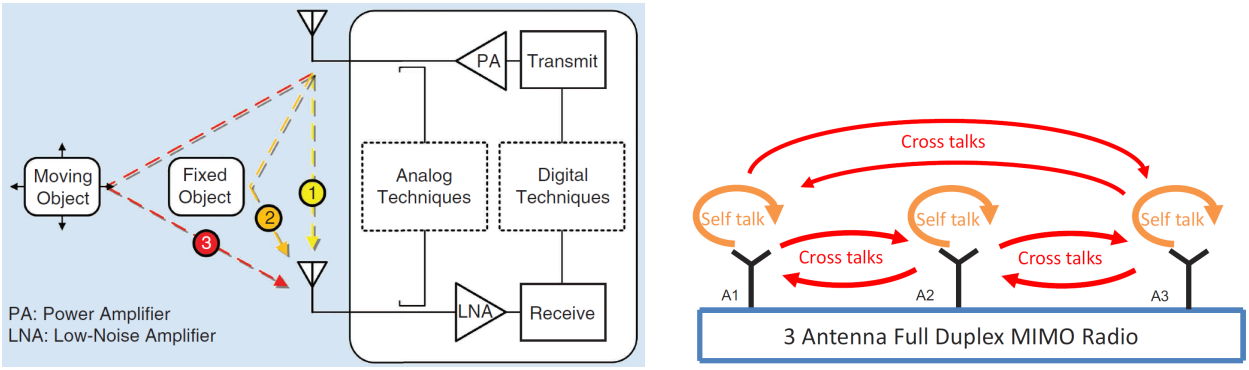


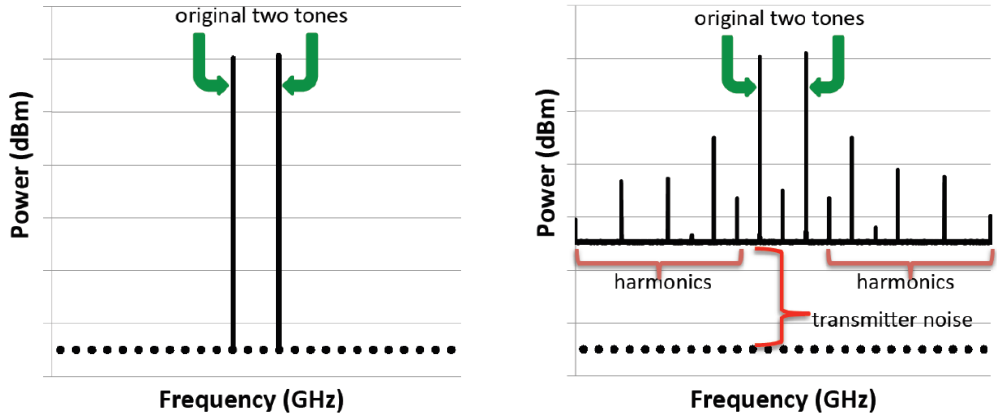
Figure 1.4: General self-interference cancellation (SIC) techniques for in-band full-duplex transceivers [2]. SIC can be applied in the propagation, analog, and digital domain. For an ideal IBFD system the receive noise floor after SIC is identical to half-duplex operation with no transmit signal.

refection path, which varies with time, requiring a time-dependent SIC function. In Fig. 1.5a, only two antenna elements are shown. As the system is scaled to more antenna elements, the number of interference paths grows with the number of elements. For a three-element IBFD array, the direct coupling paths are shown in Fig. 1.5b from [4], demonstrating the difficulty of array scaling



(a) (b)

Figure 1.5: (a) Two antenna IBFD system with multiple self-interference paths from [3]. Self-interference from 1) direct path, 2) fixed object refection, and 3) moving object refection. (b) Three element IBFD system depicting the increasing number of direct path interference from [4].



(a) (b)

Figure 1.6: An (a) ideal two tone transmit signal and a (b) actual transmit two tone signal with added noise and nonlinearities from the transmit chain [5]. Due to the randomness of the added noise, the transmit signal needs to be sampled after the transmit chain for accurate signal representation.

for IBFD arrays.

For a practical IBFD system using SIC, the final transmitted signal should be used during cancellation. The transmit chain, especially the front-end power amplifier, adds noise and nonlinearities to the ideal transmit signal. An example of this for a two-tone signal is shown in Fig. 1.6, with an ideal signal in Fig. 1.6a and a practical signal with added noise and nonlinearities in Fig. 1.6b. Due to the added noise and nonlinearities of the transmit signal contributing to the coupled self-interference signal, sufficient SIC can not be done with the ideal transmit signal. Some approaches, such as [13], make a duplicate transmit chain for SIC, but in part due to the randomness of noise, the duplicated transmit chain doesn't fully cancel the self-interference to the half-duplex noise floor. Even with the increased noise floor due to full-duplex operation, [13] shows performance improvements from half-duplex operation compared to full-duplex operation.

In-band full-duplex phased arrays can be implemented in three different ways, as shown in Fig. 1.7 from [6]. The simplest approach is shown in Fig. 1.7(a) with a multi-aperture array having a separate transmit and receive array separated by a fixed difference. Combining the separate array, Fig. 1.7(b) shows an aperture-level IBFD array, with a single array subdivided into transmit

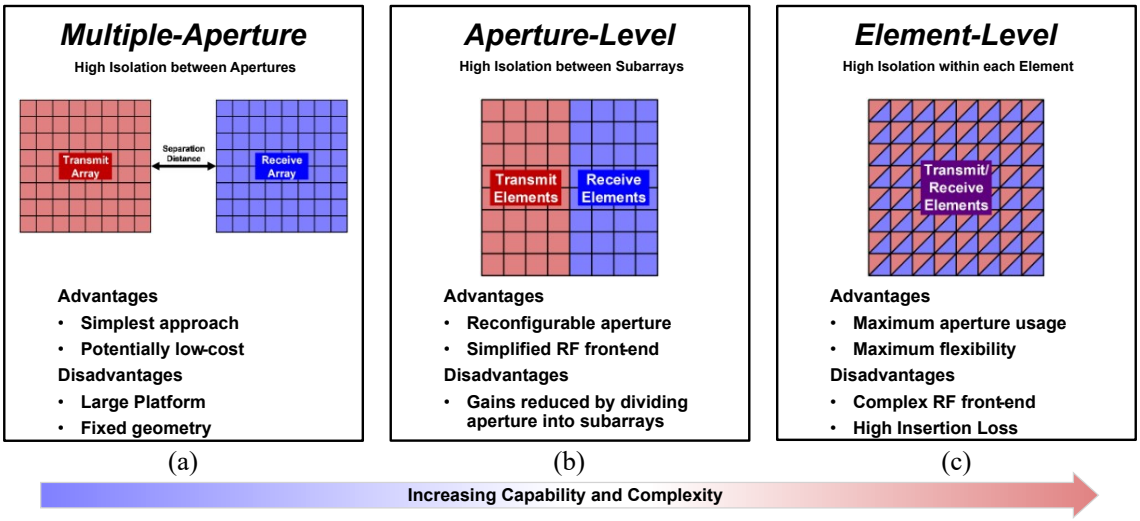


Figure 1.7: In-band full-duplex array architectures from [6]. (a) Multi-aperture is the simplest implementation with two distinct transmit and receive arrays. (b) Aperture-level sub divides the array into transmit and receive array, lowering antenna gain for transmit and receive. (c) Element-level transmits and receives at each element for maximum aperture usage but requires a complex front-end for each element.

and receive. This configuration still allows for a simple front-end but reduces the transmit and receive gain due to subdividing the array. For transmission and reception done at the element level, Fig. 1.7(c) shows an element-level IBFD array with maximum aperture usage. Element-level IBFD can also be realized with a single antenna with a T/R module containing a circulator, causing a high level of insertion loss in transmit and receive.

1.3 Applications and Implementation of In-Band Full-Duplex

In addition to increased spectrum efficiency for wireless communication, in-band full-duplex has been applied to several applications, as shown in Fig. 1.8. For the previously mentioned application of communications, Fig. 1.8a shows a cellular relay node using IBFD operation, which is demonstrated in [7]. Another common application of IBFD is integrated sensing and communications (ISAC), shown in Fig. 1.8b from [8], with the ability to detect objects while simultaneously communicating. In addition, electronic warfare (EW) has applied IBFD technology to a variety of applications discussed in [9]. One of the discussed applications, shown in Fig. 1.8c, demonstrates a

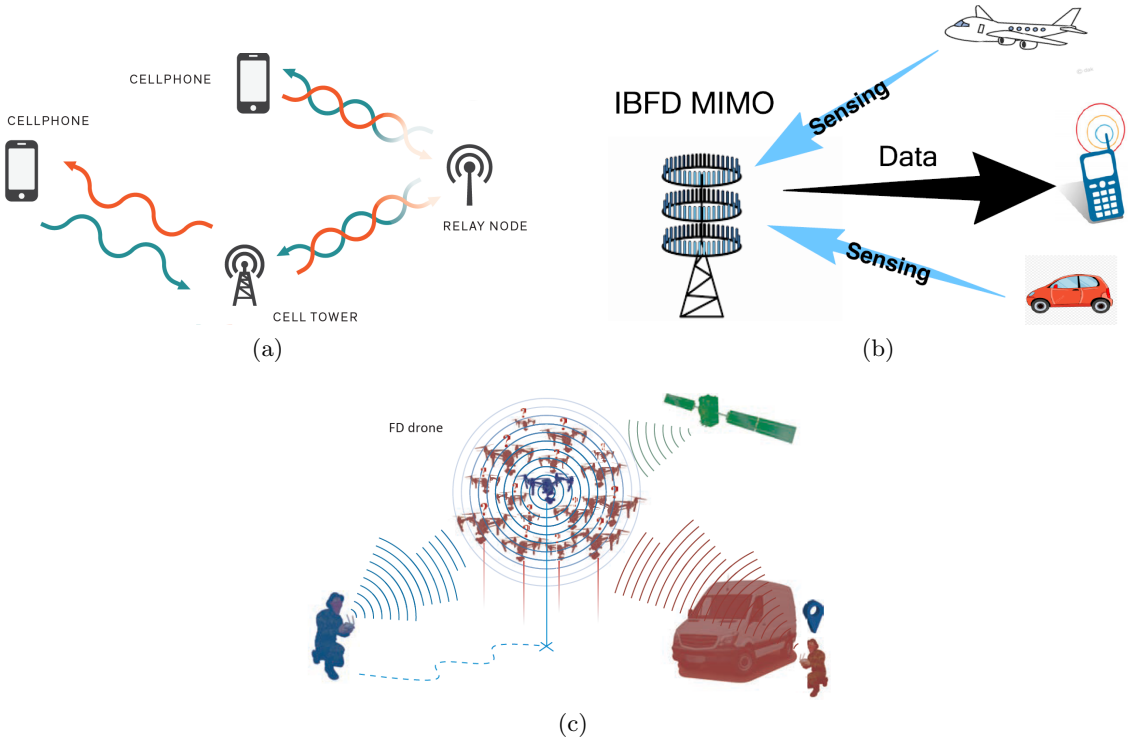
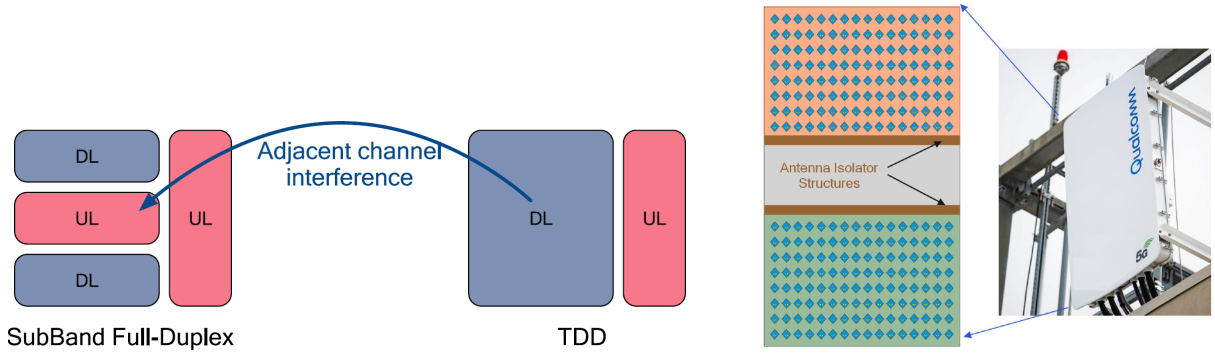


Figure 1.8: Application of in-band full-duplex. (a) A cellular network relay increasing spectrum efficiency of the network, shown in [7]. (b) Integrated sensing and communications (ISAC), allowing communications and radar simultaneously, shown in [8] (c) Electronic warfare (EW) IBFD drone performing simultaneous jamming and communications, shown in [9]

drone simultaneously jamming and communicating using IBFD technology. Similar to EW, IBFD has been applied to wireless encryption demonstrated in [14], showing improved encryption from HD to IBFD. A comprehensive overview of IBFD application and design aspects are discussed in [8] and [15].

Communications systems using IBFD technology for improved spectrum efficiency have been demonstrated in [5, 16, 4]. Using a single antenna element, [5] demonstrates a IBFD WiFi system for standard WiFi 802.11ac PHYs at 2.4 GHz with an $1.87x$ improvement in throughput, utilizing all three SIC domains to achieve an overall SIC of 110 dB. Both [16] and [4], show element-level in-band full-duplex phased arrays at 0.8 GHz and 2.45 GHz. Using beamforming and impedance tuners at each antenna element, [16] shows improved self-interference suppression with 3 dB of degradation in transmit and receive array gain. With a IBFD three-element array for WiFi, [4]



(a) (b)

Figure 1.9: Qualcomm's proposed subband full-duplex communication network shown in [10]. (a) Legacy TDD downlink (DL) and uplink (UL) communication and proposed subband full-duplex UL and DL. (b) Multi-aperture subband full-duplex antenna array.

demonstrates and compared the designed system with HD operation and a single antenna IBFD system shown an almost doubling of throughput with an $1.95x$ improvement. With a

For commercial implementation IBFD has been proposed for a 5G-advanced and a 6G system [17] [18] that will allow system with higher flexibility, lower latency, and ISAC. Shown in [10] Qualcomm introduces the first step toward cellular IBFD with subband full-duplex reducing latency and improving flexibility. The proposed subband full-duplex operation compared to legacy TDD operation is shown in Fig. 1.9a. Subband full-duplex enables uplink (UL) and downlink (DL) in adjacent sub bands simultaneously, with self-interference created from adjacent channel leakage between UL and DL, instead of direct channel overlap with IBFD. Using a multi-aperture approach as shown in Fig. 1.9b, a spatial isolator greater than 80 dB from 3.2 to 3.6 GHz between transmit and receive is achieved. For addition isolation, digital cancellation and beam forming are implemented for a 17 dB increase.

In this thesis, elements of the RF front-ends required for aperture-level and element-level IBFD arrays are demonstrated, as shown in Fig. 1.10. The shaded MMIC pictures at the bottom of the figure show designed and tested MMICs, with their components referred to in the system diagram in the figure with matching color. The Isolation section, blue in the diagram, shows a multi-

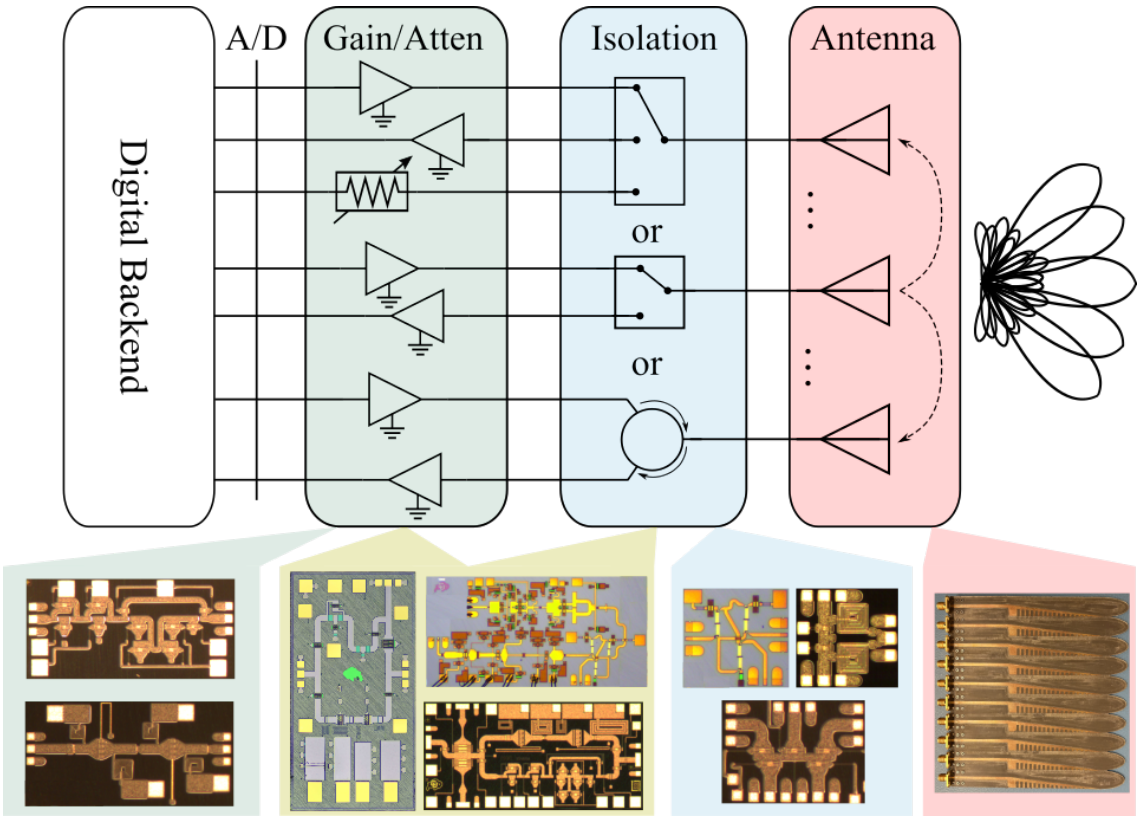


Figure 1.10: RF front-ends for aperture-level in-band full-duplex and element-level in-band full-duplex arrays. The designed and tested MMICs are illustrated in gray with each co-designed component outlined with a dashed box. A designed and measured antipodal Vivaldi array (AVA) is highlighted in yellow for aperture-level in-band full-duplex.

port switch, a single-pole double-throw (SPDT) switch, and a circulator. System Gain/Atten, highlighted in green, shows a PA, LNA, and variable attenuator (VA). The co-deigned MMICs, with components from Isolation and Gain/Atten, are highlighted in yellow. Highlighted in red is an antenna array, with a picture of the designed and fabricated array below.

Table 1.1: GaN-on-SiC Processes

Company	Process	Gate Length (μm)	Max Freq. (GHz)	Nom. Drain Voltage (V)	Power Density (W/mm)
Qrovo	QGaN25	0.25	25	40	8
WIN	NP15-00	0.15	35	28	3
HRL	T3	0.04	140	12	1.5

The GaN-on-SiC processes used for the front-end MMIC designs are listed in Table 1.1, showing gate length, max frequency, and power density for each process [19]. Using the desired operational frequency of each front-end a different process is chosen: Qorvo's QGaN25 process for S-band operation, WIN Semiconductors' NP15-00 process for X-band operation, and HRL's T3 process for W-band operation.

1.4 Thesis Contents

The thesis is organized in 8 chapters following Fig. 1.10.

Chapter 2 presents three reflective-type, single-pole double-throw (SPDT) switch topologies intended for a switch feedback network in a full-duplex phased array module. The MMIC switches are implemented in a 250 nm GaN on SiC process, with a design frequency range of 2.5 to 3.5 GHz. Due to the relatively low design frequency, lumped elements are used for the passive networks, and the design procedure is described. The reported switch topologies demonstrate an insertion loss below 2 dB across the desired bandwidth with varying isolation based on the topology. Measured performance is compared with simulations using foundry transistor models.

Chapter3 presents a 3.5-bit variable attenuator (VA) MMIC that operates from 1 to 5 GHz. The MMIC is implemented in the Qorvo 250 nm BCB2 GaN-on-SiC process. An attenuation range of 55 dB in steps of 5 dB is achieved with resistive T networks and HEMT switch devices. The bit values are implemented with 5 dB, 10 dB, and 20/40 dB networks. The 20 dB and 40 dB resistive networks are combined into a single network, with the attenuation level determined by a switchable shunt resistance, resulting in an additional half bit. For the desired 10 Ω and 1 Ω shunt resistance values of the 20 and 40 dB T networks, the R_{on} of the shunt switch devices are used, balancing the R_{on} and C_{off} of the device. The VA demonstrates all 11 attenuation states with a return loss better then 10 dB across all states within a 5:1 frequency range and a minimum input P1dB of 34 dBm.

Chapter4 presents an 8-element linear antipodal Vivaldi antenna array from 8 to 18 GHz designed for aperture-level in-band full-duplex operation. The array is designed to be manufactured from a single substrate, with separate feed lines at each element to allow for a completely

reconfigurable system. At 10 GHz the antenna element has a width of $\lambda/2$, corresponding to the spacing between elements, allowing for scanning up to 20°. For $|S_{11}| < -10$ dB or better with a width below λ for the antenna element, corrugations are added. With all 8 elements, the simulated array demonstrates a gain of 15 dB to 18 dB, and a front-to-back ratio of 16.5 dB or better.

Chapter4 presents an analysis showing increased channel capacity of an aperture-level in-band full-duplex array and a designed antenna array for full-duplex operation. The system analysis of the aperture-level in-band full-duplex array is based on the maximum capacity of a digital communications channel in the presence of uncorrelated additive Gaussian noise introduced by Shannon [20] for unidirectional communications. The analysis shows an increase in channel capacity up to a certain level of SNR degradation during full-duplex operation compared to half-duplex operation. To enable aperture-level in-band full-duplex an 8-element linear antipodal Vivaldi antenna array from 8 to 18 GHz designed for aperture-level in-band full-duplex operation, is presented. The array is designed to be manufactured from a single substrate, with separate feed lines at each element to allow for a completely reconfigurable system. At 10 GHz the antenna element has a width of $\lambda/2$, corresponding to the spacing between elements, allowing for scanning up to 20°. For $|S_{11}| < -10$ dB or better with a width below λ for the antenna element, corrugations are added. With all 8 elements, the simulated array demonstrates a gain of 15 dB to 18 dB, and a front-to-back ratio of 16.5 dB or better.

Chapter5 presents a front-end MMIC that samples the transmit signal to improve digital self-interference cancellation (SIC) in aperture-level in-band full-duplex (IBFD) phased arrays. The circuit is a co-designed low-noise amplifier (LNA), variable attenuator (VA), and front-end RF network for transmit (Tx) and receive (Rx) operation. When the array element is in Tx mode, the MMIC couples a portion of the transmitted signal through the capacitance of an OFF switch. This is subsequently fed through a variable attenuator, downconverted, and sampled as a "transmit observation" signal for digital SIC. The MMIC is implemented in a 150-nm GaN on SiC process for operation from 8–12 GHz. In transmit mode, the switch insertion loss is less than 1 dB, return loss greater than 10 dB, and a simulated power handling greater than 40 dBm. During reception,

the co-designed LNA using complex-to-complex impedance matching has a peak gain of 16 dB and a minimum noise figure of 2 dB.

Chapter6 presents a front-end MMIC designed for integration into an aperture-level in-band full-duplex system operating from 2.7 GHz to 3.5 GHz. The system utilized analog assisted digital SIC, allowing for a scalable IBFD array while still accounting for added noise and nonlinearities in the transmit chain. The designed MMIC consist of a co-deigned front-end 50 W 5-port switch, high-power LNA, variable attenuator, and back-end single-pole-double throw switch. The MMIC enables transmit observation for analog assisted digital SIC, through sampling of the transmit signal through the off capacitance (C_{off}) of an OFF switch. This transmit observation signal is then feed through the variable attenuator to condition the signal for direct digitization. The MMIC is implemented in Qorvo 0.25μm GaN on SiC process with a power density of 6 W/mm at 10 GHz. The transmit path demonstrates an insertion loss less than 1 dB and power handling greater than 50 W at 3 GHz. The packaged MMIC shows a receive path gain greater then 20 dB from 2.5 to 4.5 GHz and an input P1dB of 10 dBm at 3 GHz.

Chapter7 presents a fully integrated 75-100 GHz element-level in-band full-duplex (IBFD) front-end MMIC. The MMIC is implemented in a 40-nm HEMT GaN-on-SiC process and consists of a tunable passive quasi-circulator (PQC), power amplifier (PA), and low noise amplifier (LNA). The tunable passive circulator, consisting of three Lange couplers, uses self-interference cancellation for circulator like performance. With tunable loads at the isolated ports in two of the couplers, this passive quasi-circulator demonstrates an isolation of 30 dB from transmit to receive dependent on tunable load biasing, in addition to a return loss better than 10 dB across the band for all bias levels. The passive circulator is then integrated on chip with a three-stage PA and a three-stage LNA, with a measured system transmit gain of 13.6 dB and a receive gain of 17 dB. The fully integrated front-end demonstrates a transmit output power of 22 dBm and a receive noise figure of 5 dB.

Chapter 8 A summary of contributions of the work described in this thesis is given, with some avenues for future work.

Chapter 2

RF Switches for Analog Front-Ends

2.1 Introduction

Referring to Fig. 1.10, RF switch design and measurements are described with GaN MMICs at 3 GHz. When transmitting in half duplex, as done in pulsed radar systems, a switch is used to route the signal from the final stage power amplifier (PA) to the antenna, reducing the available receive-mode time [21]. Full duplex, or simultaneous transmit and receive arrays, usually require circulators, which are bulky, lossy and limited in bandwidth. Additionally, circulators have limited isolation which can be degraded when the impedance of the antenna changes during scanning [22]. Another approach, considered in this chapter and illustrated in Fig. 2.1 is to use switches in each TR module, but use a fraction of the array elements for transmitting, while the remaining elements receive [23]. This digitally-scanned array architecture is reconfigurable in terms of number of T and R elements.

Figure 2.1 shows a SIC technique similar to those demonstrated in [24] and [25]. Both propagation and digital domain SIC is incorporated, for a reconfigurable in-band full-duplex phased array with $\lambda_0/2$ spacing at the center frequency, as discussed in [23]. In this architecture, each element-level TR module is either in transmit or receive mode, determined by the switch. In the transmitting elements (shown in red in the figure), the feedback network samples a portion of the transmitted signal and routes it to the transmit-element receiver (shown in blue). After down-conversion, the sampled feedback signal is compared in the digital domain with the received (green) down-converted and sampled signal. The feedback network can have several architectures,

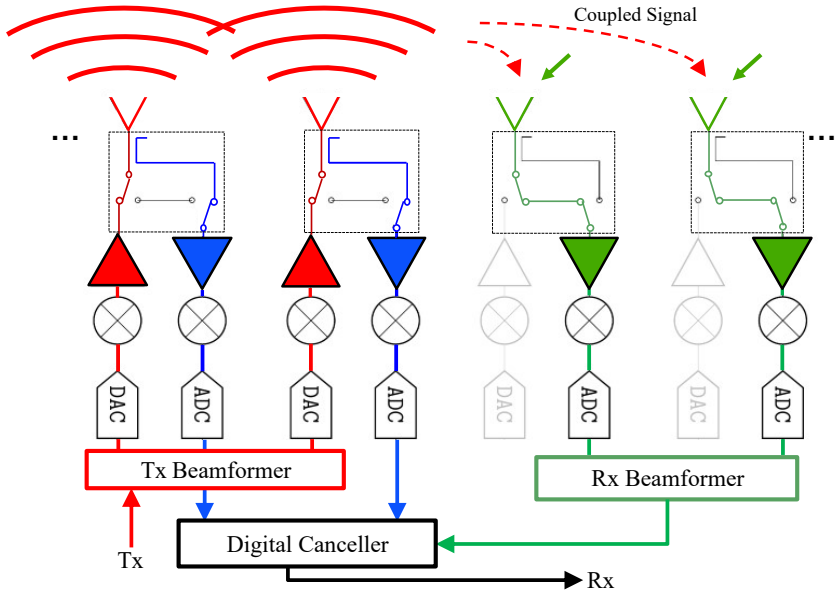


Figure 2.1: In-band full duplex digitally-scanned phased array block diagram, where transmitting elements in the front end are shown in red, while the receiving ones are shown in green. The receive path of the transmitting elements, shown in blue, couples a part of the transmitted signal and provides information on self-interference coupling to the digital cancellation circuit.

all requiring high-quality switches that can be easily integrated into the front end elements.

Some examples of published work on RF switches include devices demonstrated in [26] and [27], which show multiple topologies and performance focused on low insertion and high isolation. In this chapter, we focus on similar switch topologies, but with performance parameters tailored to the feedback network application. This requires low insertion loss and a specific level of isolation and compression that depend on TR module parameters, e.g. the output power of the transmit PA. Several switches are designed for the purpose of comparison, and then implemented in a 250-nm Qorvo GaN on SiC MMIC process using foundry models.

2.2 SWITCH TOPOLOGIES AND DESIGN

For the front-end feedback circuit from Fig. 2.1, the switches need to meet three key performance metrics. First, the isolation between T and R ports needs to be high to protect the receiver chain while transmitting, but sufficiently low to allow transmit signal sampling for digital cancellation. The switch insertion loss from the antenna port to either R or T ports needs to be

low to maintain low noise figure of the receiver. Finally, the switch footprint should be as small as possible to be integrated into the front-end TR module.

The design and fabrication of several switch topologies is performed in Qorvo's 250-nm GaN on SiC process, which has good performance around the deign frequency of 3 GHz. A 3×75 μm switch device, with gate control voltages of 0 V and -30 V for a shorted and open device, respectively, is used to compare the three topologies. Fig. 2.2 shows the simulated complex impedance between the drain and source for the two states of the RF-grounded gate switch HEMT, obtained from the foundry transistor linear model.

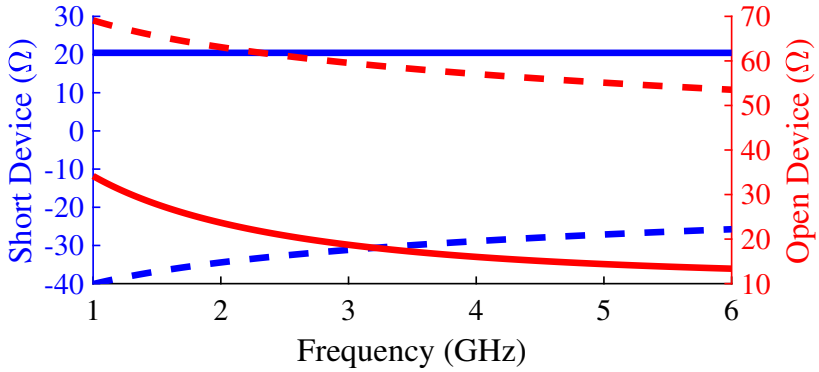


Figure 2.2: Impedance of a 3×75 μm switch HEMT in the Qorvo GaN25 process for the shorted device biased at 0 V (blue) and open device biased at -30 V (red). The real part is shown in solid line, and the imaginary in dashed line.

A simple reflective switch using a shunt transistor, shown in Fig. 2.3(a), requires an impedance transformer, usually implemented with a quarter-wavelength microstrip line. At 3 GHz, this is prohibitively large, so a lumped-element Π network with shunt capacitors and a series inductor is designed, with element values given by [28] and [29]:

$$C_{shunt} = \frac{1}{2\pi f_0 Z_0} \quad \text{and} \quad L_{series} = \frac{Z_0}{2\pi f_0}. \tag{2.1}$$

These expressions are used to determine values of an inverter that transforms 42+j1.8 Ω to 60-j2.5 Ω and 27-j2.5 Ω to 94-j2 Ω for the ON an OFF states at 3 GHz, respectively. This results in $C_{shunt} = 1.1$ pF and $L_{series} = 2.7$ nH. The input impedance $Z_{in} = Z_0^2/Z_L$ is found for the ON and

OFF states. For the ON case, looking into the tee network while transmitting, the inverter is loaded with 50 Ω in parallel with an open circuit from the receive path, resulting in Z_L= 42+j1.8 Ω, found from full-wave simulations. For the OFF case, the receive path is shorted, resulting in Z_L=27-j0.5 Ω. The two values of Z_{in} are then found to be 60-j2.5 Ωs and 94-j2 Ω, respectively. Full-wave simulated Z_{in} for both load impedances is shown in Fig. 2.4.

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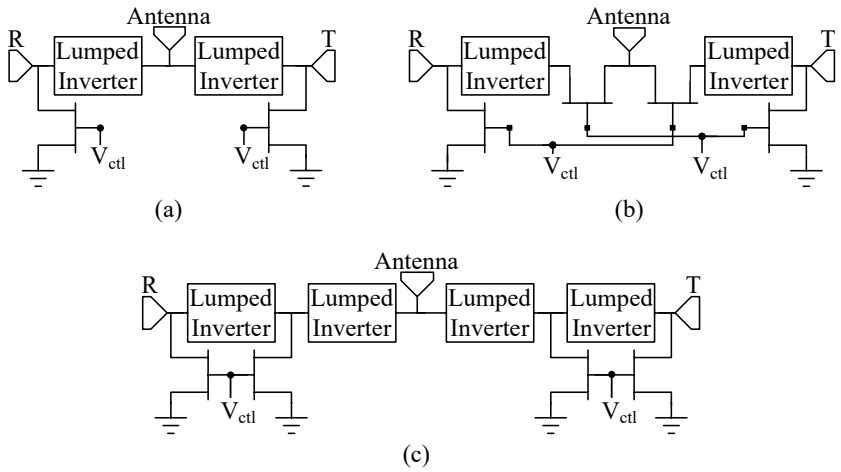


Figure 2.3: Circuit schematics of the three switch topologies: (a) simple reflective switch; (b) series-shunt HEMT switch; and (c) dual-shunt HEMT switch.

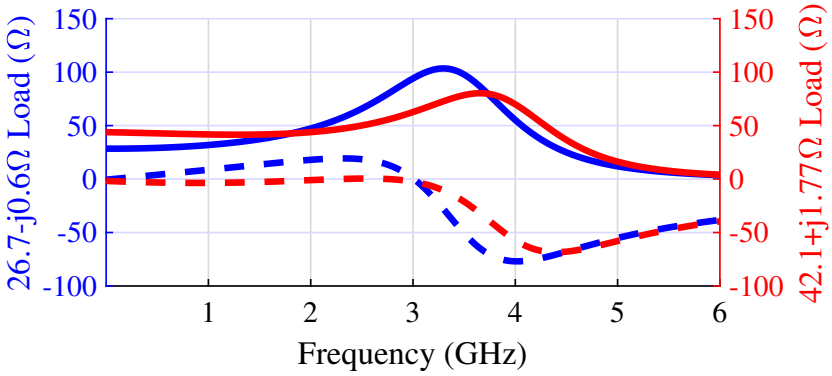


Figure 2.4: Lumped-element inverter impedance with C_{shunt} = 1.1 pF and L_{series} = 2.7 nH, showing a zero imaginary part at the design frequency of 3 GHz. These results are obtained with full-wave electromagnetic simulations of the inverter layout.

Three switch designs are compared using the above impedance transformer, and shown in

Fig. 2.3. In addition to the simple reflective switch consisting of a symmetric single shunt HEMT with an added lumped-element impedance inverter, Fig. 2.3(a), a symmetric reflective dual-shunt device switch shown in Fig. 2.3(b) is designed using the same lumped-element inverters. The third design shown in Fig. 2.3(c) consists of a symmetric single series and single shunt HEMT, with inverters between the series and shunt device. This topology allows testing of a series and shunt device combination, as well as the biasing networks required for a series and shunt configuration.

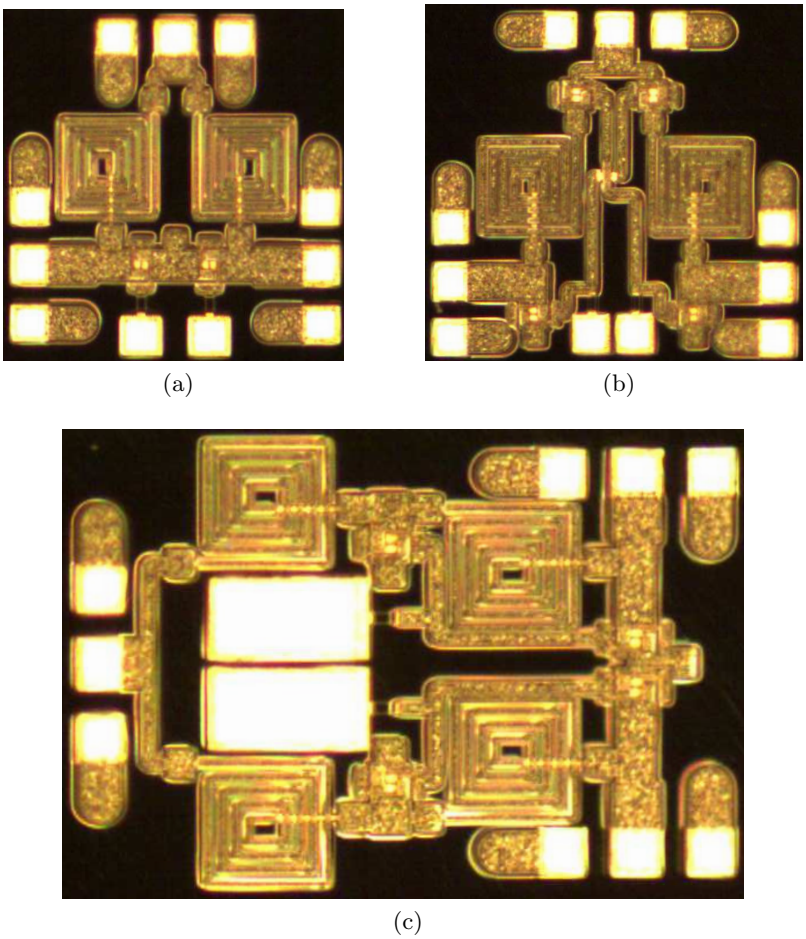
The three circuits are then designed in the MMIC process to obtain the smallest footprint, as shown in Fig. 2.5. The simple shunt switch requires the smallest area ($0.9\times0.9\,\mathrm{mm}^2$), while the shunt-series switch is the largest ($1.4\times0.9\,\mathrm{mm}^2$). The series inductor is the limiting component for reducing the size of the die, resulting in the lumped-element impedance inverter of $0.4\times0.3\,\mathrm{mm}^2$ in size. Due to the tight layout, full-wave electromagnetic simulations are essential and are performed using the 2.5D Cadence AWR Axiem tool. Layouts of the switch and GSG pads take ease of probing into account. For example, no two GSG pads can be on the same side of the die for probing. The grounds of the GSG pads are rotated to decrease the die area. For both circuits in Fig. 2.5(b) and Fig. 2.5(c) four DC bias pads are required, and for easier probe measurements the drain biases are tied together. The circuit in Fig. 2.5(b) consists of a series-shunt configuration, and a bridge and underpass are required for the drain terminals to be connected together.

2.2.1 Measured Performance

The MMICs are measured on-wafer using a network analyzer calibrated with Alumina SOLT 2-port standards, with ports aligned and across from each other, while the third port is terminated in a 50Ω load. The measurements are performed from 1 to 6 GHz to check the broadband performance around the 2.5 to 3.5 GHz operating frequency range. Fig. 2.6 displays the measured S-parameters compared to the simulated ones. The plotted data shows key performance metrics for the switch feedback network application in the full-duplex array from Fig. 2.1. Red traces display the insertion loss of the ON path from the transmitter power amplifier to the antenna feed. Blue traces display the isolation between T and R while transmitting, giving a sample of the transmitted signal used

as the feedback for self-interference cancellation. Green traces show the isolation of the OFF path from the antenna feed to the transmitter during receiving. Finally, the black curves show the return loss at the antenna feed port in receiving mode of operation.

The measured and simulated performance of the simple shunt switch is shown in 2.6(b), showing good agreement overall, with only the measured isolation about 5 dB lower than predicted. 2.6(c) shows performance of the series-shunt switch MMIC, which displays the best match between simulated and measured performance. A low insertion loss, ranging from 1.2 dB to 1.3 dB across the desired bandwidth is measured, along with a return loss better than 10 dB. With an isolation



(a) (b)

(c)

Figure 2.5: Photographs of the three fabricated SPDT switch MMICs corresponding to the topologies in Fig. 2.3: (a) simple reflective switch with an area of $0.9\times0.9\,\mathrm{mm}^2$; (b) shunt-series switch with an area of $1\times1\,\mathrm{mm}^2$; and (c) dual-shunt switch $1.4\times0.9\,\mathrm{mm}^2$ in size.

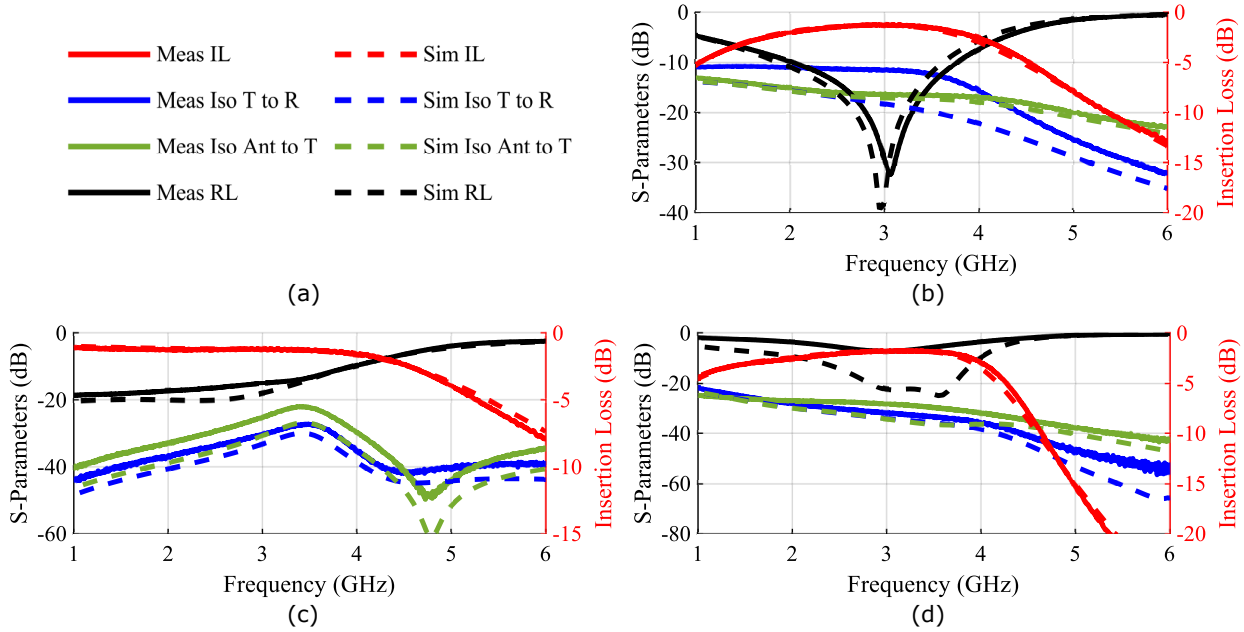


Figure 2.6: (a) Key parameters for switch performance. Measured (solid lines) and simulated (dashed lines) performance of the single shunt switch (b), series-shunt switch (c) and dual-shunt switch (d).

better than 20 dB in the frequency range of operation (2.5 to 3.5 GHz), this configuration allows measurement of a sample of the transmitted signal which is required for the switch feedback network. The improved isolation can be thought of as a filter that only allows the desired signal to be sampled. Finally, Fig. 2.6(d) shows performance of the dual-shunt configuration. Measured insertion loss and isolation matches the simulations, however the return loss deviates considerably. A possible cause for this is a poor probe contact on the third port, which was terminated with a 50 Ω loaded GSG probe.

2.3 Chapter Summary

In summary, this chapter presents three reflective-type, single-pole double-throw (SPDT) MMIC switches designed for operation from 2.5 to 3.5 GHz and intended for a switch feedback network in a phased array module. Due to the relatively low design frequency, lumped elements are used for the passive networks, resulting in compact MMIC designs. The reported switch topolo-

gies demonstrate an insertion loss below 2 dB across the desired bandwidth with varying isolation based on the topology. Measured performance is compared with simulations, validating foundry transistor and passives models. Depending on the input power sampled from the transmit path, and compression level of the receiver chain, a switch can be designed for desired feedback network performance, with a desired level of isolation. These contributions are published in [30]. Results from this investigation are applied to the S-band T/R front-end described in Chapter 6.

Chapter 3

Variable Attenuator

3.1 Introduction

In this chapter, variable attenuator MMIC design and measurements from Fig. 1.10 are detailed. Aperture-level in-band full-duplex (IBFD) phased arrays described in Chapter 2, use vector modulators for analog self-interference cancellation (SIC) to recover the sensitivity of the receiver [31] [32] [33] [34]. This is done by sampling the high-power transmit signal, attenuating it to prevent damage to the receiver, then comparing it with the receive signal for self-interference cancellation. In addition to simple biasing, zero power consumption and a small footprint required for ease of integration into the phased array, a VA with large dynamic range is needed to account for high transmit power levels. The application for the 3-GHz design in this chapter is sampling for direct digitization.

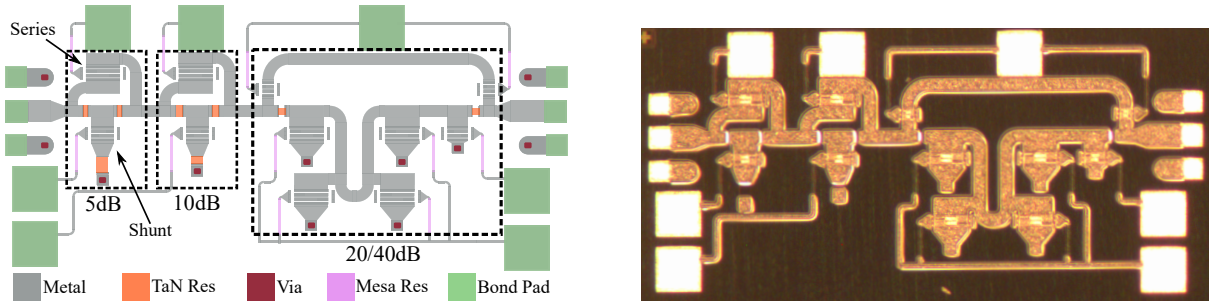


Figure 3.1: (a) Layout of variable attenuator with labeled attenuation bits. (b) Photograph of the GaN MMIC in the Qorvo GaN25 BCB2 process. The die has an active area of 2 mm × 0.8 mm.

Variable attenuator architectures are usually made in the form of Π or T networks, and can be continuous or discrete. Analog attenuators use the variable resistance of diodes or transistors with adjustable bias, e.g. [35] [36] [37] [38] [39]. Discrete attenuators with switched networks allow more precise attenuation levels across frequency. To enable more than just one attenuation level, multiple resistive networks, referred to as bits, are stacked allowing for a range of attenuation levels. The most common implementation has 6 bits (0.5, 1, 2, 4, 8 and 16 dB), resulting in a range of 31.5 dB in steps of 0.5 dB [40] [41] [42] [43] [44]. Different numbers of bits and attenuation ranges have been demonstrated, from 4 to 6 bits and 15.5 to 70 dB range, in [45] [46] [47] [48] [49]. Generally the largest attenuation bit is 16 dB, limited by the required shunt resistance and series switch isolation necessary for implementing the higher attenuation bits. Instead, to achieve high attenuation values, multiple bits are cascaded leading to increased size and loss. For high power handling and large dynamic range, when the real-estate is limited such as in phased arrays, a VA with a reduced number of bits and a large attenuation range is desired. This letter presents a 3.5-bit stepped attenuator with 55 dB of range, using a combined 20/40 dB attenuation bit to reduce the overall number of bits. The VA is implemented in a GaN MMIC, shown in Fig. 3.1, demonstrating a minimum P1dB of 34 dBm and a compact active area of $2\,\text{mm} \times 0.8\,\text{mm}$.

3.2 Variable Attenuator Design

Switchable resistive T networks shown in Fig. 3.2 are cascaded to form a 3.5-bit design. The switches are biased at the gate with $-40\,\text{V}$ and $0\,\text{A}$, consuming zero power.

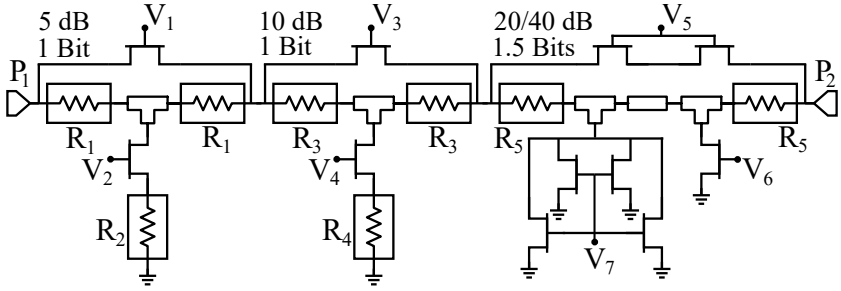


Figure 3.2: Schematic of implemented 3.5 bit variable attenuator. Due to asymmetry, it does not have bi-directional power handling.

Traditional single-bit attenuators are demonstrated for 5 dB and 10 dB as seen in Fig. 3.2, where the values of R_1, R_3 and R_2, R_4 determine the attenuation level and impedance match. These are implemented with TaN resistors and switch HEMT devices for a 50 Ω match, as indicated in the layout of Fig. 3.1a. The ideal values for the 5 and 10 dB attenuators are $R_1 = 14\,\Omega$, $R_2 = 82\,\Omega$ and $R_3 = 26\,\Omega$, $R_4 = 35\,\Omega$. A bypass series switch device with a periphery of $3 \times 150\,\mu$m is chosen for minimal loss of the reference state, determined by the R_{on} of the device. The shunt switch device size of $3 \times 100\,\mu$m is chosen for minimal C_{off} to allow flat attenuation response across frequency and reduce leakage. Due to the added resistance from the R_{on} of the shunt switch devices and the reference attenuation level of the series switch, the TaN resistance values are adjusted to realize the desired 5 dB and 10 dB attenuation matched to 50 Ω.

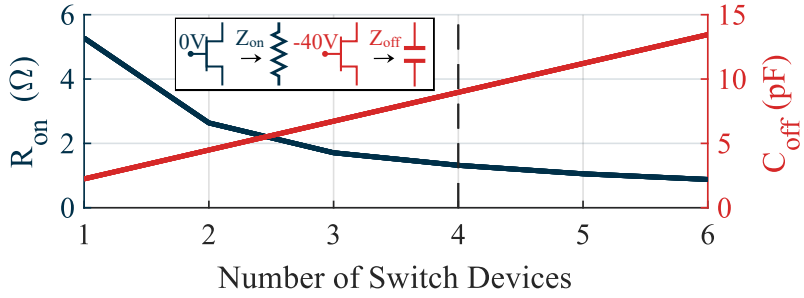


Figure 3.3: Simulated R_{on} and C_{off} for differing numbers of $3 \times 150\,\mu$m devices. The dashed line indicates the number of devices chosen for a 1-Ω resistance.

The 1.5 attenuation bit is implemented combining a 20 dB and 40 dB resistive T, denoted as 20/40 dB in Fig. 3.2, which adds a switchable shunt resistance to the 1-bit network, prohibiting the two levels from coexisting. This topology reduces the footprint, reference level loss, and biasing of the switching devices. Since the series resistance R_5 is the same for both attenuation states, the two different attenuation levels require similar series resistance values. The ideal series resitance values for 20 dB and 40 dB attenuation are 41 Ω and 49 Ω respectively, and an implemented series resistance of 45 Ω, which is the average of the two, realizes the 1.5 bit. Additionally, the isolation of the series bypass switch used for this bit needs to be greater than the maximum attenuation level. For a series switch isolation greater than 40 dB, two series $3 \times 50\,\mu$m switch devices are used.

For 20 dB attenuation, the desired shunt resistance of 10 Ω is realized with the R_{on} of a single shunt $3 \times 90\,\mu$m switch device, allowing for a reduced area. Additionally, the 40 dB attenuation requires a 1 Ω shunt resistance, however the R_{on} of a single shunt $3 \times 150\,\mu$m device exceeds this value. Increasing the number of shunt devices reduces R_{on} with the trade-off of increased C_{off}. This is shown in Fig.3.3, which plots the shunt R_{on} (left) and C_{off} (right) for different numbers of $3 \times 150\,\mu$m switch devices. For a 1.3 Ω shunt resistance, four shunt $3 \times 150\,\mu$m devices are used to realize 40 dB attenuation. The single $3 \times 90\,\mu$m and four $3 \times 150\,\mu$m shunt switch devices, enabling the 1.5 bit, can be seen on the right of Fig. 3.1a.

Table 3.1: Attenuation steps of 3.5 bit variable attenuator

5 dB	10 dB	20 dB	40 dB	Atten
				0 dB (3.5 dB)
X				5 dB
	X			10 dB
X	X			15 dB
		X		20 dB
X		X		25 dB
	X	X		30 dB
X	X	X		35 dB
			X	40 dB
X			X	45 dB
	X		X	50 dB
X	X		X	55 dB

The 3.5 bit VA with 5 dB, 10 dB, and 20/40 dB attenuation values is implemented in the 250-nm Qorvo GaN on SiC BCB2 process, suitable to 18 GHz with a maximum operating voltage of 40 V. The manufactured 2.5 mm × 1.2 mm MMIC is shown in Fig. 3.1b, with the input of the VA on the left (P_1) and output (P_2) on the right. For the 3.5-bit implementation, Table 3.1 displays all 11 realizable attenuation levels from the digital step attenuator, referenced to the simulated reference level loss of 3.5 dB at 3 GHz.

3.3 Measurements

The VA is mounted on a CuMo carrier, the dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors. The MMIC is measured on a Summit 9000 probe station with 150-μm pitch GSG probes and characterized in small-signal operation from 1 GHz to 5 GHz using a N5241B Keysight Nework Analyzer with on-wafer calibration, using a Cascade Microtech Impedance Standard Substrate 101-190 C. The measured small-signal performance is shown in Fig. 3.4 from 1 to 5 GHz for the 11 attenuation steps and bypass state. The bypass state is shown in black with a 4.5 dB loss at 3 GHz, which is 1 dB larger than simulated. Despite this difference, the VA reaches a normalized attenuation range of 55 dB. Fig. 3.5 show the measured $|S_{11}|$ and $|S_{22}|$, which are below 10 dB across the band for all states, in agreement with simulations.

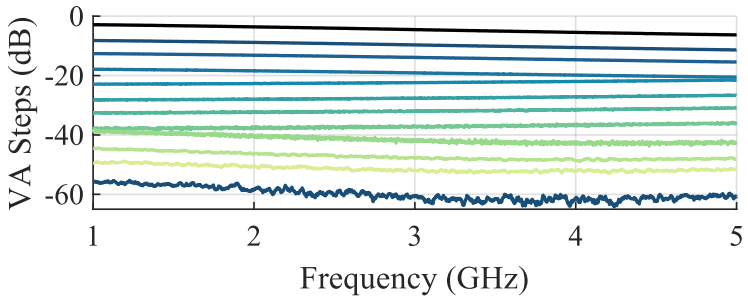


Figure 3.4: Measured 11 steps of VA, including bypass state attenuation. The maximum attenuation state has increased noise compared to other attenuation levels as it approaches the noise floor of the network analyzer. This can be improved by an increase in the single power level of the network analyzer.

Performance comparison of the typical 1 bit attenuators and 1.5 bit attenuator, Fig. 3.6 (left)

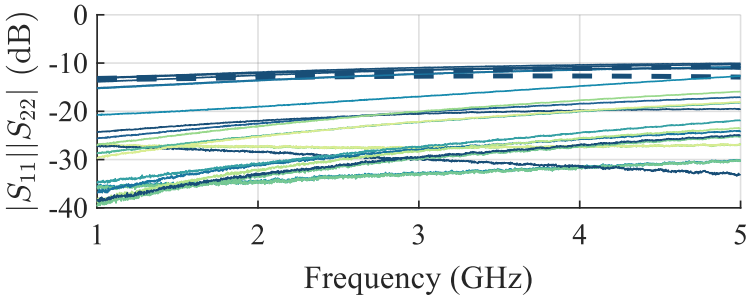


Figure 3.5: Measured $|S_{11}|$ and $|S_{22}|$ across all VA states (solid) and simulated bypass state (dashed). Trace colors correspond to VA steps shown in Fig. 3.4.

displays the measured and simulated attenuation levels which only use the individual attenuation bits of 5, 10, 20 and 40 dB. Each state is normilized to the bypass state. The single bit attenuation levels of 5 and 10 dB align well with desired levels and show good agreement with simulations. For the 1.5 bit attenuation levels of 20 and 40 dB, there is some deviation from simulation due to using the R_{on} of switch devices, which varies more than the TaN resistors, especially for the 20 dB level which deviates about 1 dB across the band. Namely, the single shunt $3 \times 90\,\mu$m device in the 20 dB attenuation bit has an additional $R_{on} = 1\,\Omega$ of resistance in measurement compared to simulation.

Four shunt switch devices are used for the 40-dB attenuator, while the 20 and 40-dB attenuators are combined into a single 20/40 dB attenuator as seen in Fig. 3.2. For 20 dB of attenuation, V_5 biases both series switches *off* and V_6 biases the single shunt switch *on*, and the signal path is loaded with the shunt device capacitance, introducing a frequency dependence (yellow trace in Fig. 3.6. For 40 dB attenuation, the signal path remains the same, but the shunt switch devices are shorted to ground with V_7. When neither the 20 dB or 40 dB attenuation levels are used, the signal bypasses the 20/40 dB attenuator through the two series switches, seeing little effect of C_{off} of the shunt devices. The RMSE of the VA levels is calculated across frequency for all 11 attenuation steps, shown in Fig. 3.6 (right), with a minimum of 1.5 dB. The RMSE level is a result of using transistor R_{on} of the switch devices, which vary with frequency and do not have an adequate model.

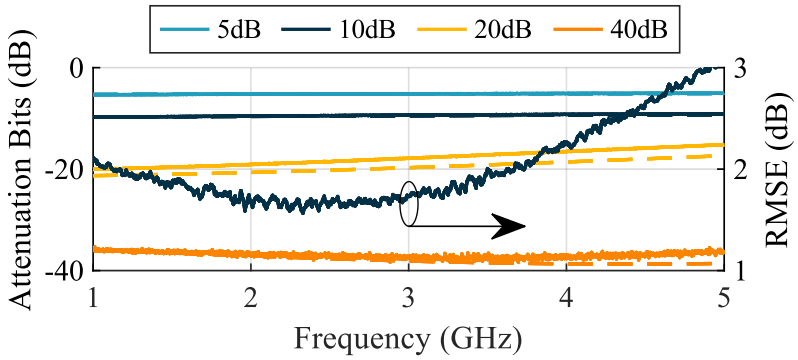


Figure 3.6: Measured and simulated attenuation levels of normalized individual bits (left), and RMSE of all 11 state (right).

The large-signal compression of the VA is measured in the bypass and 5 dB states, with results shown in Fig. 3.7. Measurements show an increase in $P_{0.1dB}$ by about 5 dB from the bypass

state to the 5 dB state. A switch nonlinear model, such as the one in [?] is not available in the foundry PDK, not permitting large signal simulations. With the VA compression based on the switch devices, the 0.1 dB compression point of the switch devices in the *off* and *on* states can be calculated as follows [50] [51] [52]:

$$P_{\text{off}} = \min\left[\frac{2(V_{BD} - V_g)^2}{Z_0}, \frac{2(V_g - V_p)^2}{Z_0}\right] \tag{3.1}$$

$$P_{\text{on}} = Z_0 I_{0.1\text{dB}}^2/2 \tag{3.2}$$

where the breakdown and pinch-off are $V_{BD} = -80\,V$, $V_p = -5\,V$, $I_{0.1\text{dB}}$ is the device current at the 0.1-dB compression point. P_{off} is found from (1) to be 46 dBm with $V_g = -40\,V$ and is unrelated to device size. Equation (2), for the *on* state 0.1 dB point (related to the device size), is limited by the smallest device of $3 \times 50\,\mu$m, required for 40 dB of isolation. Instead of a single small device, using two larger devices in series which together have 40 dB of isolation gives a higher $I_{0.1\text{dB}}$. The last bit uses the loss from the previous bits to increase power handling. A 0.1-dB compression point of 25 dBm is calculated from the process current of 750 mA/mm to be $I_{0.1\text{dB}} = 112.5$ mA (750 mA/mm $\cdot$ $3 \times 50\,\mu$m).

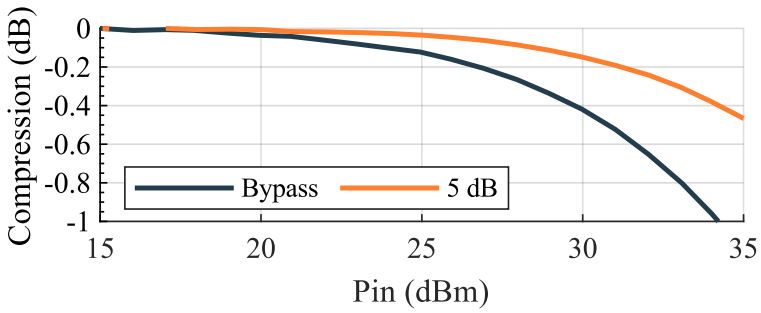


Figure 3.7: Measured compression of lowest attenuation state at 3 GHz.

3.4 Conclusion

In summary, this chapter presents a 3.5-bit VA with a range of 55 dB in steps of 5 dB, operating from 1 to 5 GHz. Although resistive Tee networks are a common approach for variable

Table 3.2: Variable Attenuator Comparison Table

Ref.	Freq. (GHz)	Range/Step (dB)	IL (dB)	P1dB (dBm)	Area (mm^2)
[41]	0 - 67	31.5/0.5	7.8	-	1.2
[42]	1 - 6	31.5/0.5	2.3	22.5	2.0
[45]	0 - 40	23.0/1.0	6.0	-	4.5
[46]	1 - 50	70.0/2.0	4.0	-	5.9
[53]	11 - 14	15.5/0.5	6.5	17.0	9.0
[49]	24 - 49	21.5/0.5	6.5	-	0.5
This Work	1 - 5	55.0/5.0	4.5	34.0	1.6

attenuators, they typically demonstrate a dynamic range of 31.5 dB using 7 attenuation bits. Table 3.2 compares this work to previous publications. We demonstrate unique attenuation bits for a much larger dynamic range, and with fewer bits, in addition to a new method of combining the bits. The implemented 1.5-bit combines a 20 dB and 40 dB bit into a single network. The R_{on} of shunt switch devices is used for the desired shunt resistance of the 20 dB and 40 dB attenuation levels, allowing a shunt resistance of 10 Ω and 1.3 Ω, accompanied by an increase in C_{off}. The 1.5-bit series bypass switch has an isolation greater than 40 dB, and all 11 attenuation steps demonstrate a measured range of 55 dB with only 3.5 bits and a minimum P1dB of 34 dBm, as reported in [54]. Results from this investigation are applied to the S-band T/R front-end described in Chapter 6, having a large dynamic range and compact size for transmit observation and integration in an aperture-level in-band full-duplex phased array.

Chapter 4

Aperture-Level In-Band Full-Duplex

4.1 Introduction

In-band full-duplex systems have been mentioned as ideally doubling the throughput of a digital communications system compared to a half-duplex system, due to the two directions of transmission and reception [15]. Realistically, due to a higher noise floor in a full-duplex system, the throughput is not fully doubled [5]. With an antenna array, allowing for aperture-level in-band full-duplex, SIC becomes much more feasible compared to a single antenna element full-duplex system. For an aperture-level in-band full-duplex array that samples the transmit signal at the antenna level, a theoretical analysis of channel capacity is presented along with a designed antipodal Vivaldi antenna array for aperture-level full-duplex operation.

4.2 Capacity of Aperture-Level In-Band Full-Duplex

With the ability to accurately sample the transmitted signal, we next consider how this can be used to cancel self-interference in an aperture-level IBFD array and which affects channel capacity and therefore spectrum efficiency. The maximum capacity of a digital communications channel in the presence of uncorrelated additive Gaussian noise was introduced by Shannon [20] for unidirectional communications. The maximum capacity of a channel with noise is:

$$C = Wlog_2(1 + SNR), \tag{4.1}$$

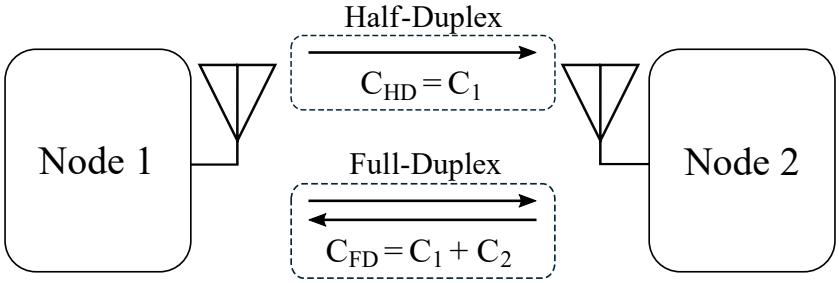


Figure 4.1: Channel capacitance between node 1 and node 2 for full-duplex and half-duplex operation. If there is no degradation in SNR the channel capacitance doubles from half-duplex to full-duplex operation.

for a given bandwidth (W) and signal-to-noise ratio (SNR). With a signal-to-noise ratio for half-duplex (SNR_{HD}) and full-duplex (SNR_{FD}), the channel capacity for each operation is

$$C_{HD} = W \log_2(1 + SNR_{HD}). \tag{4.2}$$

and

$$C_{FD} = 2\Big[W \log_2(1 + SNR_{FD})\Big]. \tag{4.3}$$

The factor of 2 comes from bidirectional communication as shown in Fig. 4.1. In the ideal case, the noise floor is not degraded during full-duplex operation ($SNR_{HD} = SNR_{FD}$), doubling the maximum channel capacity with full-duplex operation. Additionally, during full-duplex operation, the SNR at each node can be different in practice, but is assumed to be equal at both nodes. In a practical full-duplex system, the SNR degrades compared to half-duplex operation, not fully double the channel capacity.

4.2.1 Aperture-level Self-Interference

A diagram of a linear aperture-level IBFD system with uncorrelated added white Gaussian noise power (n) following the PA, is shown in Fig. 4.2, with ideal signal processing similar to the demonstrated work in [33]. The transmitted and received signals of interest are denoted as x and y. The transmit antennas are labeled 1 through K on the left, and the receive antennas are labeled 1 through J on the right. The coupling matrix between transmit and receive elements ($\mathbf{C}^{KJ}$) and

transmit to transmit elements ($\mathbf{C}^{KK}$) are shown with dashed arrows at the top of the figure. The receive path gain is denoted with g, and the transmit observation path coupling and attenuation with p.

The summed transmit and vectorized transmit signals are,

$$a = \sum_{k=1}^{K} x_k + n_k^x \tag{4.4}$$

and

$$\mathbf{A}^K = [x_1 + n_1^x, x_2 + n_2^x, \ldots, x_K + n_K^x]. \tag{4.5}$$

The vector of transmit signals allows for a dot product with the coupling matrices to determine the coupling between transmit and receive, along with transmitting elements. Incorporating the transmit-to-receive coupling, the total summed receive signals (b) are

$$b = g \sum_{j=1}^{J} y_j + n_j^y + \mathbf{C}_j^{KJ} \cdot \mathbf{A}^K, \tag{4.6}$$

amplified by the receiver gain (g).

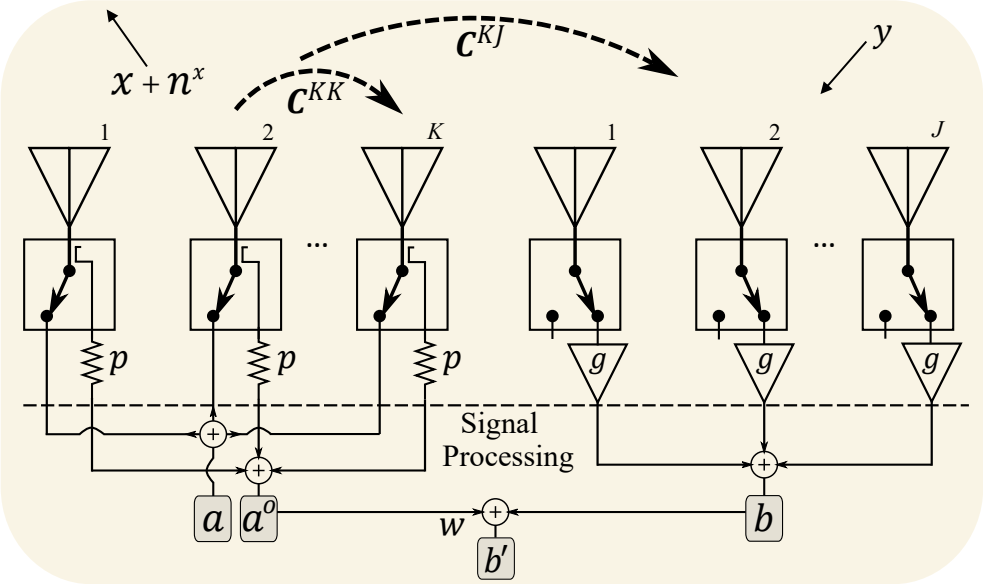


Figure 4.2: Diagram of aperture-level in-band full-duplex with transmit observation with SIC. Coupling between transmit and receive ($\mathbf{C}^{KJ}$) and transmit to transmit ($\mathbf{C}^{KK}$) is shown with dashed arrows. The SIC operation is shown with a summation of the received signals (b) and the weighted (w) transmit observation signals (a^o).

For the transmit observation signals, assuming an ideal match at each element, the summed signals are

$$a^o = (a \cdot p) + p\sum_{k=1}^{K} n_k^o + \mathbf{C}_k^{KK} \cdot \mathbf{A}^K, \tag{4.7}$$

accurately representing the transmit signals for SIC to recover the received signal of interest (y). Due to non-idealities, the transmit observation signal also includes transmit-to-transmit coupling and added noise, degrading SIC.

4.2.2 Self-interference Cancellation

Not considering the digital domain, with ideal signal processing, SIC is applied as

$$b' = w[a^o] + b, \tag{4.8}$$

summing the received signal (b) and the weighted (w) transmit observation signal (a^o). For alignment of the amplitude and phase during cancellation, w is a complex number.

Replacing the variables with their summations, rearranging terms, and separating them into the brackets, the summed received signal and weighted transmit observation signals are

$$b' = \left[g\sum_{j=1}^{J} y_j + n_j^y\right] + \left[g\sum_{j=1}^{J}(\mathbf{C}_j^{KJ} \cdot \mathbf{A}^K) + w(a \cdot p)\right] + \left[w\sum_{k=1}^{K} p(n_k^o + \mathbf{C}_k^{KK} \cdot \mathbf{A}^K)\right]. \tag{4.9}$$

The bracketed terms show the received signals, the summed signals for SIC, and the residual noise from full-duplex operation. To determine the value of transmit observation signal weight (w), the summed transmit to receive interference and weighted transmit observation signals are set to zero,

$$\left[g\sum_{j=1}^{J}(\mathbf{C}_{(j)}^{KJ} \cdot \mathbf{A}^K) + w(a \cdot p)\right] = 0 \quad \rightarrow \quad w = \frac{-g}{(a \cdot p)}\sum_{j=1}^{J}(\mathbf{C}_{(j)}^{KJ} \cdot \mathbf{A}^K) \tag{4.10}$$

completely canceling the transmit-to-receive interference.

After SIC, the received signal is

$$b' = \left[g\sum_{j=1}^{J} y_{(j)} + n_{(j)}^y\right] + \left[w\sum_{k=1}^{K} p(n_{(k)}^o + \mathbf{C}_{(k)}^{KK} \cdot \mathbf{A}^K)\right], \tag{4.11}$$

which includes added noise from transmit to transmit interference and added transmit observation noise. This shows that even with ideal SIC, the added self-interference from full-duplex operation

isn't fully removed, due to the transmit-to-transmit coupling and added noise in the transmit observation signal. This residual noise degrades the SNR during full-duplex operation compared to half-duplex operation. Depending on the coupling between transmitting elements and the method for sampling the transmit observations, the residual transmit-to-transmit interference can be reduced.

4.2.3 Channel Capacity with Reduced SNR

To determine the SNR for half-duplex (SNR_{HD}) and full-duplex (SNR_{FD}) operation that have the same maximum channel capacity, C_{FD} and C_{HD} can be equated as

$$Wlog_2(1 + SNR_{HD}) = 2\Big[Wlog_2(1 + SNR_{FD})\Big]. \tag{4.12}$$

Assuming the same operational bandwidth (W) for half-duplex and full-duplex operation, the reduced SNR during full-duplex operation (SNR_{FD}), which matches the maximum channel capacity of half-duplex operation, is

$$SNR_{FD} = \big(1 + SNR_{HD}\big)^{\frac{1}{2}} - 1. \tag{4.13}$$

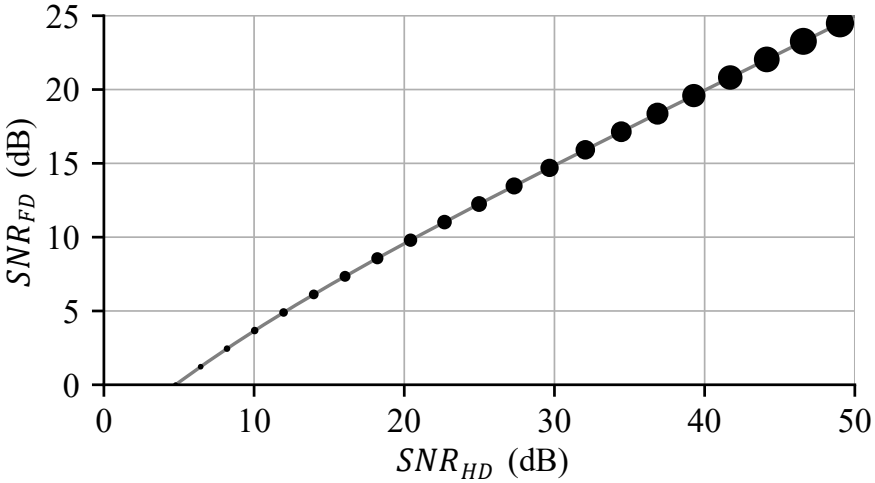


Figure 4.3: Equating maximum channel capacity for SNR level for half-duplex (SNR_{HD}) and full-duplex (SNR_{FD}) operation. The increasing marker size on the trace shows an increasing channel capacity as SNR increases. The trace shows for a given SNR_{HD} what SNR_{FD} values give identical channel capacity.

where SNR_{HD} is the signal-to-noise ratio of a half-duplex link. From Eq.4.13, the allowable reduction in SNR for full-duplex operation compared to half-duplex operation can be determined. This is shown in Fig. 4.3, with the trace showing the required SNR_{HD} and SNR_{FD} for the same channel capacity. The increasing marker size along the trace shows the increased channel capacity with increasing SNR. With a lower SNR_{FD} than SNR_{HD}, the same channel capacity can be achieved, e.g., a half-duplex system with an SNR_{HD} equal to 30 dB and a full-duplex system with an SNR_{FD} equal to 15 dB, both have a maximum channel capacity of 10 bits per second/Hz. This is shown in Fig. 4.3, where the trace intersects at SNR_{HD} equal to 30 dB and SNR_{FD} equal to 15 dB. The area above the trace corresponds to a higher throughput during full-duplex operation, while the area below the trace corresponds to a higher throughput during half-duplex operation.

4.3 Antipodal Vivaldi Antenna Array

To further investigate aperture-level in-band full duplex operation, a linear $8-12$ GHz 8-element array is designed and characterized. For a broadband antenna array that covers X-band with a simple feed and substrate integration, an antipodally-fed Vivaldi antenna array can be designed. Such an element was first demonstrated in [55]. The antipodal Vivaldi antenna is an

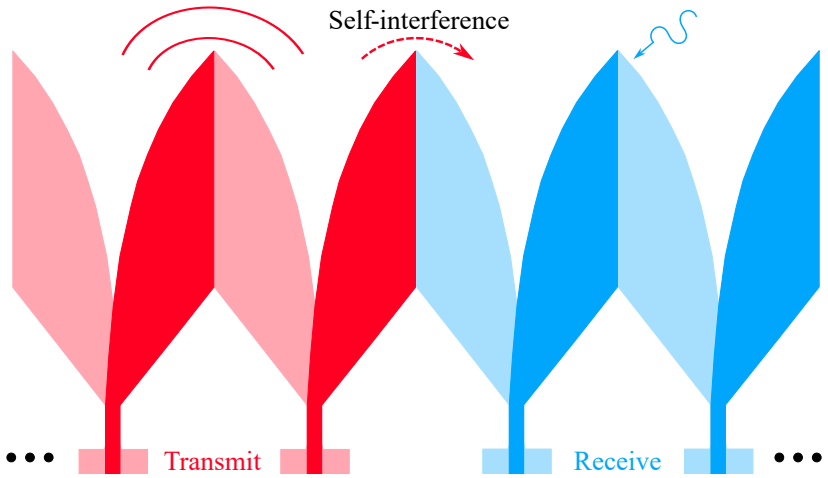


Figure 4.4: In-band full-duplex array block diagram, with transmitting (T) elements of the front end shown in red, while the receiving (R) elements are shown in blue. The coupled transmit signal is shown in the dashed red line.

end-fire traveling-wave antenna. Depending on the frequency, different parts of the antenna radiate, with the size of the radiating part based on the wavelength. The limitation in bandwidth is due to the finite dimensions of the antenna, with the maximal and minimal widths determining the lowest and highest frequencies of operation. In a more standard Vivaldi antenna, the limitation in bandwidth is also limited by the feed line, e.g. microstrip-to-slot transition [56]. An example of a linear 4-element IBFD antipodal Vivaldi array is shown in Fig. 4.4, with the element in red transmitting and the elements in blue receiving. The darker and lighter red and blue shading illustrates the top and bottom conducting strips of the antipodal antennas.

For wide-angle scanning with no grating lobes, the individual element size is $\lambda_0/2$. This tight element spacing is difficult to achieve with antipodal Vivaldi antennas due to antenna width, and the close proximity can lead to resonances between elements [57]. One method of avoiding resonances is direct electrical connection [57], [58], allowing the elements to load each other. The drawback to this high coupling is a degradation in noise performance [56], [59], especially in an in-band full-duplex system in which there is an attempt to minimize coupling between the transmit and receive elements.

Many versions of antipodal Vivaldi antennas have been published with a survey of different designs in [60], demonstrating various performance enhancement techniques. Other demonstrations of antipodal Vivaldi arrays are shown in [61] [62] [63] [64] [65]. Ideally, the antennas are horizontally polarized, eliminating lost power to vertical polarization, also known as cross-polarization. For an antipodal configuration, with conductors on opposite sides of the substrate in the vertical direction, the antennas can suffer from high cross-polarization due to the vertical component between conductors. One way to mitigate this for thick substrates is with a balanced configuration, as shown in [61]. If the substrate thickness is not determined, choosing a thin substrate will also improve the polarization, due to reducing the vertical component between the two conductors. Shown in [63], with the addition of dielectric rods at each element, the gain and isolation between elements are improved.

4.4 Antipodal Vivaldi Antenna

As mentioned previously, due to the conductors being on opposite sides of the substrate, the antipodally-fed Vivaldi antenna can suffer from high cross-polarization levels, which is related to the thickness of the dielectric. With a thick dielectric, more of the E-field is in the vertical direction, compared to a thin substrate [60]. To reduce cross-polarization levels, a thin dielectric of 31 mils is chosen using the Rogers 5880 with a permittivity of 2.2. Using a lower permittivity substrate can increase fringing fields, leading to higher antenna gain.

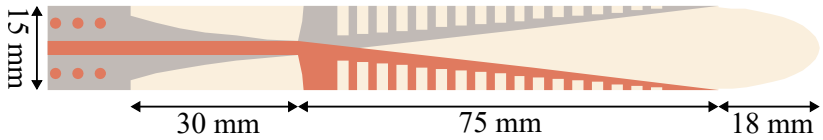


Figure 4.5: Single element antipodally-fed Vivaldi antenna designed for operation across X-band.

As mentioned previously, the desired spacing between elements is $\lambda/2$, determining the maximum width of an antenna element. The designed single-element antipodal Vivaldi antenna is shown in Fig. 4.5, with its dimensions labeled. The top side conductor is shown in orange, while the bottom side conductor is shown in gray. The antenna is fed by a 50 Ω microstrip trace with three vias on each side, seen on the left of the figure.

With a width of 15 mm ($\lambda/2$ at 10 GHz), the antenna element allows for $\lambda/2$ spacing of

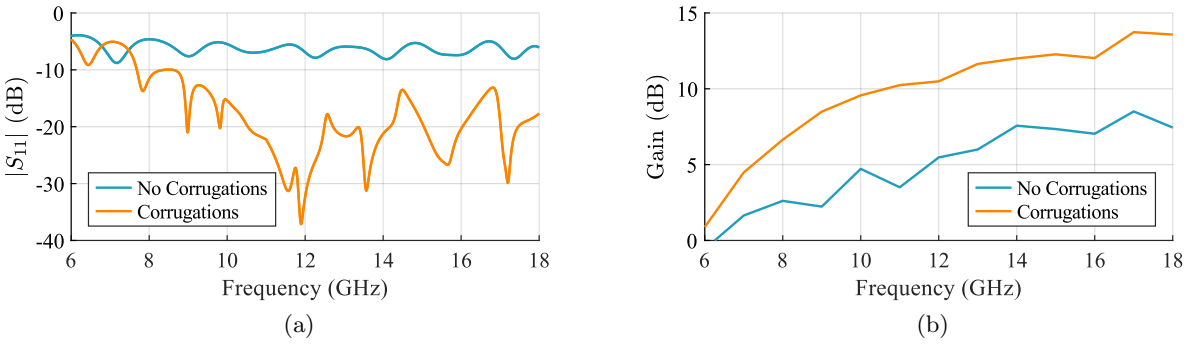


Figure 4.6: Simulated single antipodal Vivaldi antenna performance comparison with and without corrugations. (a) $|S_{11}|$ referenced to the input microstrip trace and (b) total gain comparison.

antenna elements at 10 GHz. Across the frequency range of 8 – 12 GHz, the antenna has a size of 0.4λ at 8 GHz to 0.6λ at 12 GHz. Due to the fixed width of the antenna for array spacing, the length and taper rate of the antenna were designed for the desired performance, along with corrugations.

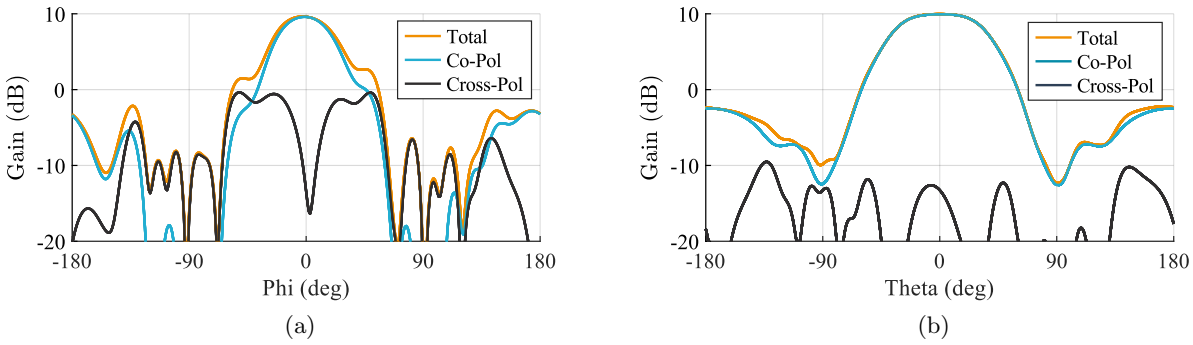


Figure 4.7: Simulated radiation pattern in the (a) E-plane and (b) H-plane, with cross-pol of both planes shown in black.

To achieve an $|S_{11}| < 10$ dB, referenced to the input microstrip trace, for an element width of 15 mm, corrugations are added to the antenna. The corrugations can be seen in Fig. 4.5, with rectangular cutouts from the top and bottom conductors. A parametric study is conducted to determine the optimal number and size of corrugations for achieving the desired performance. Comparison of $|S_{11}|$ and total gain, with and without corrugations, for the antenna is shown in Fig. 4.6a and Fig. 4.6b. With the added corrugations, $|S_{11}|$ is improved to better than 10 dB at 8 GHz and above, in addition to a 5 dB improvement in total gain from 8 to 12 GHz. The total radiation pattern along with the co- and cross-pol for the E- and H-planes at 10 GHz of the designed antenna are shown in Fig. 4.7a and Fig. 4.7b, showing good co-pol and cross-pol.

4.5 Antenna Array

Using the antipodal Vivaldi antenna element discussed in the previous section, an 8-element linear array with terminated elements on both sides is designed, comprising a total of 10 elements. This can be seen in Fig. 4.8 showing tight element spacing to allow array scanning and substrate integration with end-launch SMA connectors at each element. Additionally, vias are included at

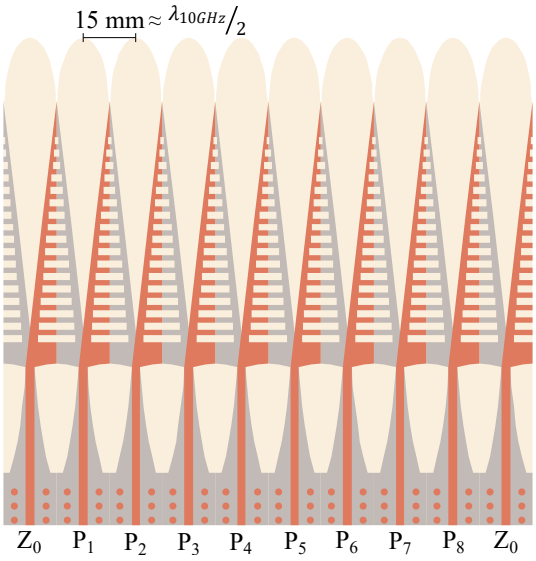


Figure 4.8: Aperture level in-band full-duplex antipodal Vivaldi linear 8-element array. Additional terminated elements are added on each side of the array to reduce edge effects. There is a 15 mm element spacing which is half a wavelength in free space at 10 GHz.

the end launch SMA point and show spacing between connectors.

Figure 4.9a and Fig. 4.9b show the input match from 6 to 18 GHz ($|S_{44}|$) for the fourth element from the left in the array, with little to no difference between elements across the array. An input match of 10 dB from 8 to 18 GHz is obtained, except for a slight increase at 9.5 GHz from 10 dB to

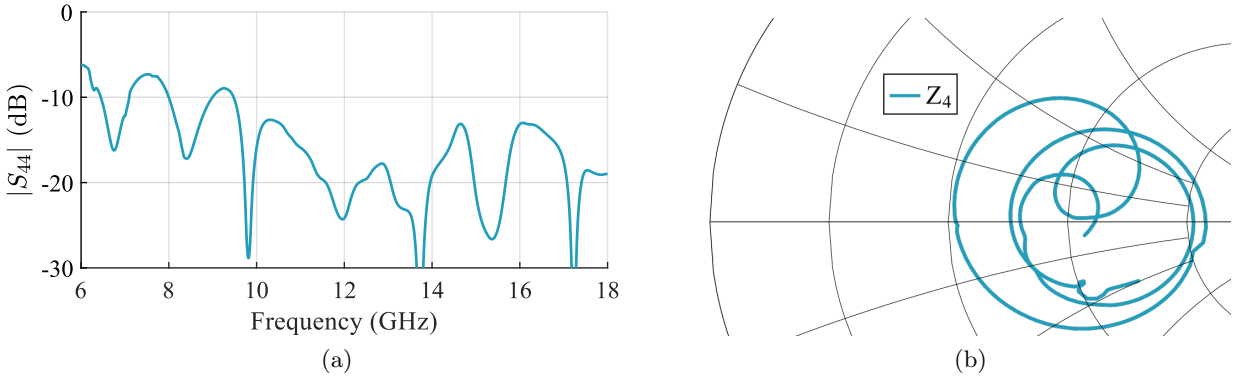


Figure 4.9: Simulated (a) $|S_{44}|$ from 6 to 18 GHz and (b) impedance of the fourth antenna from 8 to 12 GHz with little to no difference across the array. Across X-band $|S_{44}|$ remains below 10 dB besides a slight increases from 9.2 dB at 9.5 GHz. At 10 GHz the array shows a very good match, showing $|S_{44}|$ better than 20 dB.

9.2 dB. Normalized array scanning of 10° at 10 GHz can be seen in Fig. 4.10. This is done with all 8 elements in the array, where the array is in half-duplex operation, for either transmit or receive.

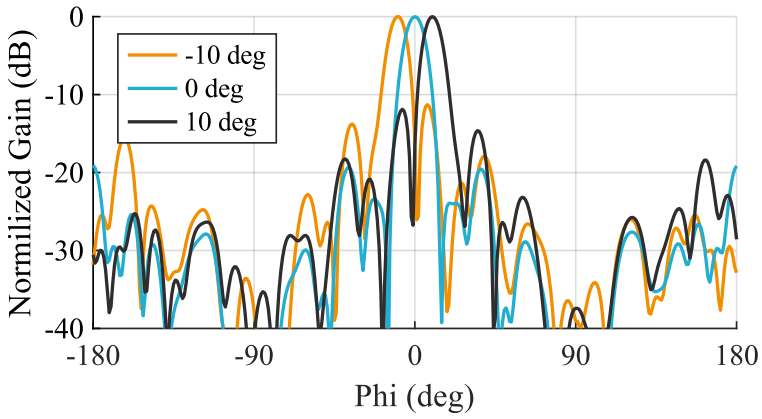


Figure 4.10: Normalized array scanning of 10° at 10 GHz using all 8 elements for either transmit or receive operation. The progressive phase shift at each port is 40 °.

For full-duplex operation, the coupling between elements is a concern. Fig. 4.11 shows the coupling between antenna elements in the array for neighboring elements, spaced by one element, and spaced by two elements. As expected, the coupling is reduced for elements further from each other. This is true from 6 to 11 GHz, but at 12 GHz and above, the coupling between elements does not change significantly as the spacing between elements increases.

Based on the front-end circuitry, the array can operate in full-duplex or half-duplex. For half-

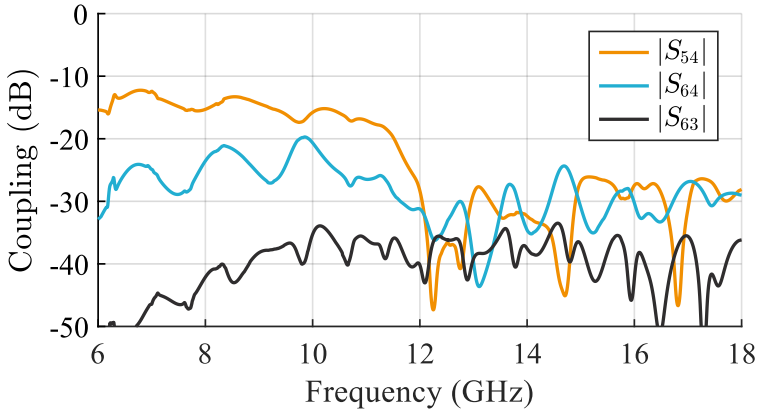


Figure 4.11: Coupling of antenna elements for neighboring elements, elements spaced one element apart, and elements spaced two units apart.

duplex operation, all 8 elements can either be in transmit or receive. For full-duplex operation, the array can be divided in half, 4 elements in transmit and 4 in receive. Additionally, the array can be unevenly divided for full-duplex operation, with 5 elements in transmit and 3 elements in receive. This would be useful in a scenario where you need higher gain in transmit than in receive. Such as a relay node that is close to the origins of the received signal of interest and far from the desired destination of the transmit signal. Depending on the allowable elements coupling, the middle elements can be turned off with only 3 elements for transmit and 3 elements for receive, resulting in an isolation better than 35 dB. The radiation pattern in the E-plane for 8-elements, 4-elements, and 3-elements is shown in Fig. 4.12, with all 8-elements achieving a total gain of 16.5 dB at 10 GHz.

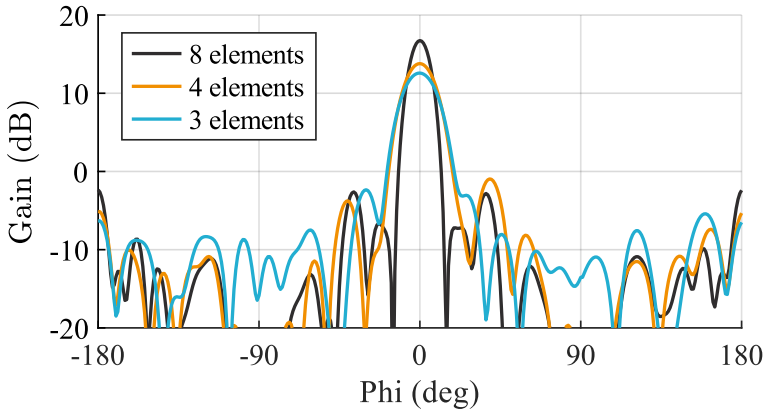


Figure 4.12: Gain of array with 8, 4, and 3 elements, showing reconfigurable gain when array is sub-divided into transmit and receive arrays for full-duplex operation.

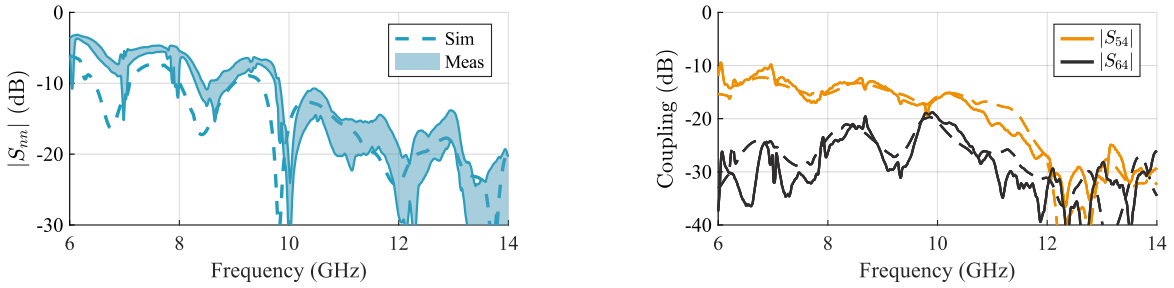
The designed antenna array was then fabricated on a milling machine and connectorized for measurement. Originally, end-launch SMA connectors were to be used for connectorizing of the array, but due to the loose fitting of the connectors, screw-in connectors were used. For use of screw-in connectors, an aluminum mount was designed to attach to the ground plane of the array. The top and bottom of the fabricated antenna array, mounted and connectorized can be seen in Fig. 4.13a and Fig. 4.13b. The rectangular aluminum block is attached to the bottom side ground plane with attachment screws that also act as vias on the top side, as seen in Fig. 4.13a.



(a) (b)

Figure 4.13: Fabricated Antipodal Vivaldi antenna array (a) top and (b) bottom. The bottom shows the aluminum mount used for SMA connection.

Scattering parameters of the array are measured focusing on return loss at each antenna element, with the measured range shown as shaded, and coupling between the middle elements as seen in Fig. 4.14a and Fig. 4.14b. Measurements were taken with an Agilent Technologies PNA Network Analyser E8364C using an SOLT calibration reference to the connector plane. Both plots



(a) (b)

Figure 4.14: Measured (solid) and simulated (dashed) (a) return loss at each antenna element and (b) coupling between elements at the center of the array. Coupling between elements in the center of the array is focused on based on how the array would be split for full-duplex operation.

show measured (solid) and simulated (dashed) data for comparison. Due to fabrication variations across the array, Fig. 4.14a shows the measured range in match across antenna elements with a solid filled trace from 6 to 14 GHz. Measured data compared to simulated data shows a slight frequency shift and degraded match below 10 GHz, while at 10 GHz the measured match for all elements is better than 20 dB. For element coupling, Fig. 4.14b shows the two adjacent center elements ($|S_{54}|$) coupling in orange and coupling between two antennas separated by one element ($|S_{64}|$) in black. Both simulated and measured data have good agreement across the band.

4.6 Conclusion

In summary, this chapter presents an aperture-level in-band full-duplex array, and a system analysis is presented, showing residual noise in the received signals after SIC. As shown in the analysis, a comparison of maximum channel capacity based on SNR for full-duplex and half-duplex operation is presented due to residual noise during full-duplex operation. From the comparison, an allowable reduction in SNR during full-duplex compared to half-duplex operation is quantified for communication systems. For other applications such as integrated sensing and communications (ISAC), CW radar, and simultaneous jamming and communications, the residual noise during full-duplex operation reduces the sensitivity of the system but enables continuous monitoring and increased capabilities.

The linear 8-element antipodal Vivaldi array is designed for simple substrate integration with separate feeds for each antenna element. To allow for compact spacing, the width of the antenna element is reduced with corrugation added to maintain performance. With the reconfigurable array, all 8 elements can be used for transmit or receive in a half-duplex operation, along with an aperture-level full-duplex operation with the array subdivided into transmit and receive arrays. These contributions are published in [66]. The fabricated and connectorized array is shown with mounting screws, acting as vias for secure SMA connection. Measured antenna match and coupling are shown matching simulations, with small differences due to fabrication tolerances.

Chapter 5

X-Band Transmit Observation GaN MMIC for Analog Assisted Digital Self-Interference Cancellation

5.1 Introduction

As discussed in Chapter 1, in-band full-duplex (IBFD), or simultaneous transmit and receive (STAR), refers to wireless systems that can transmit (Tx) and receive (Rx) simultaneously at the same carrier frequency, thus improving spectral efficiency. An early implementation of full-duplex was in CW radar [67], and this remains of interest to e.g. vehicular radar [68]. More recent applications include communications with improved spectral efficiency [7], integrated sensing and communications (ISAC) [69], electronic warfare with simultaneous communications and jamming [9], as well as multiple-input multiple-output (MIMO) systems [70, 7].

Phased arrays can implement IBFD at the element or aperture level. For such a phased array, a limiting factor is the isolation between the Tx and Rx paths. Low isolation leads to high self-interference from Tx to Rx, which can mask the received signal. As introduced in Chapter 1, to recover the signal of interest, self-interference cancellation (SIC) is applied [2] and can be done in the propagation [71] [72], analog [73] [73], and/or digital domains [74]. Multiple SIC techniques are required to achieve sufficient cancellation between Tx and Rx for most applications. Element-level arrays, or mono-static IBFD, are accomplished with ferrite circulators, active circulators [22], quasi-circulators [75], or analog self-interference cancellation (SIC) networks [68] in each antenna element. This leads to reduced Tx output power and increased Rx noise figure (NF) [76], typically reducing bandwidth and power handling. Aperture-level IBFD arrays operate by electronically dividing the

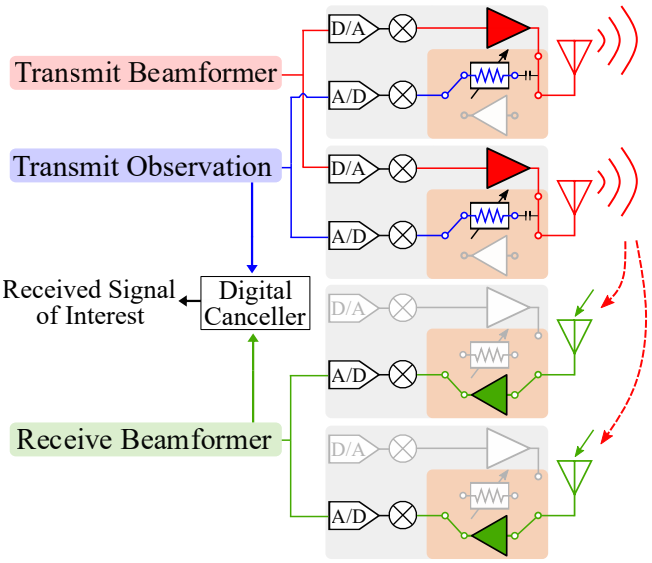


Figure 5.1: Aperture-level in-band full-duplex phased array block diagram, with transmitting (Tx) elements of the front end shown in red, while the receiving (Rx) elements are shown in green. The transmit observation path, shown in blue, samples the transmit signal, providing information for digital self-interference cancellation. The coupled transmit signal is shown in the dashed red line. This paper details the co-designed LNA, VA, and switch network MMICs indicated by the dashed-line boxes at the antenna feeds. Only two Tx and Rx elements are shown for clarity.

array into subarrays, with a fraction of the elements in Tx and the remaining elements in Rx [24], as illustrated in Fig. 5.1. This is done by a front-end switch at the antenna port, enabling each element to be either in Tx or Rx. With this architecture, a reconfigurable fraction of the elements can be transmitting while the remainder are receiving. Additionally, this multi-function approach can operate in standard half-duplex mode with all elements.

Provided the LNA and the analog-to-digital converter (ADC) in the downconversion path are not saturated, digital SIC techniques can be used to recover the sensitivity of the receiver. An array architecture with analog-assisted digital SIC, Fig. 5.1, incorporates propagation and digital domain SIC as discussed in [23]. In the transmitting elements (shown in red), the signal is coupled through the capacitance of the OFF switch,C_{off}, and fed through the variable attenuator (VA), for transmit signal observation (shown in blue). After digitization of the transmit observation signal and the received signal (shown in green), digital cancellation is used to recover the signal of interest. The front-end chip shown in dashed boxes in Fig. 5.1 implements a T/R switching network, LNA,

and VA for transmit signal observation. This approach requires a high-power handling robust LNA to avoid compression due to high coupled transmit signal levels. This can be enabled by GaN technology [50, 77], which not only eliminates the need for a limiter at the input of the LNA but also preserves the dynamic range of the signal. Additionally, GaN LNAs are more linear than their GaAs and Si counterparts, which is relevant when using SIC for recovery of the received signal of interest. GaN LNAs with competitive NF at X-band show little change in performance with as much as 2 W of input power [78, 79].

Typical front-end GaN RF switches use a single-pole double-throw configuration, e.g. [26], and have power handling compatible with the robust LNAs. For half-duplex operation, both series and shunt switch devices, symmetric relative to the common antenna port, can be used with tradeoffs in R_{on}, C_{off}, and power handling made possible through device sizing. Due to the limited chip overall size, individual series switch devices are used for the switching network in this work. To enable transmit signal observation of the high-power transmit signal, a variable attenuator (VA) conditions the power level. Digital implementation of variable attenuators, using switchable resistive pi or tee networks, allow for fix attenuation values to be applied or bypassed. A range of precise attenuation levels can be achieved with multiple resistive π or T cascaded networks, each with a different attenuation level, as shown in e.g. [45, 48, 41, 44, 40, 46, 49]. For precise attenuation levels across frequency, the transmit signal observation path in this work incorporates a simplified digital variable attenuator.

5.2 Switching Network for Transmit Observation

The TXO MMIC schematic is shown in Fig. 5.2a, depicting the co-designed LNA, VA, and RF switching network. For different switch positions, high power is transmitted from Port 1 to Port 2, low power is received from Port 2 to Port 3, and the sampled TXO signal is transmitted through an OFF switch between Ports 1 and 3. The red, green, and blue arrows show the transmit, receive, and transmit observation paths, corresponding to Fig. 5.1. The circuit is designed in the WIN Semiconductors' NP15 GaN-on-SiC 28 V process. The layout of the the 3.2 mm × 1.8 mm

MMIC is shown in Fig. 5.2b, again with the variable attenuator highlighted in blue and the low noise amplifier in green. This process has an $f_T > 35\,\text{GHz}$, with three scalable depletion mode HEMT models. The nonlinear models include thermal behavior, while a linear ungrounded source device model includes noise figure, and a symmetric nonlinear switch device model is also available with a gate bias up to $-40\,\text{V}$. Through-wafer metalized vias, three metal layers, and two types of capacitors, inductors, and resistors are included in the process design kit.

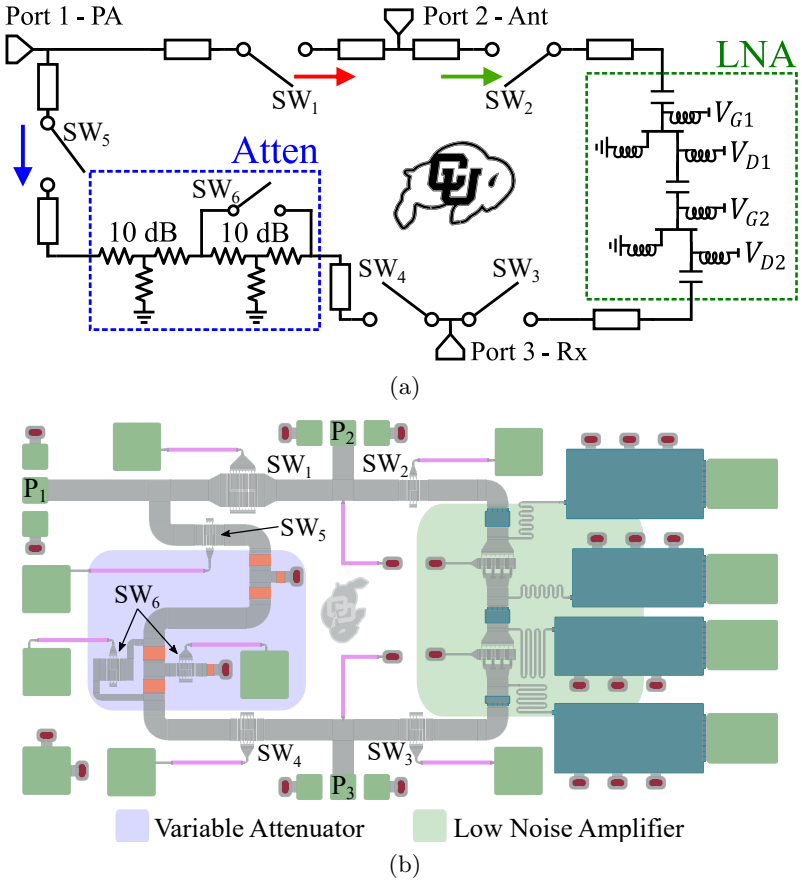


Figure 5.2: (a) Schematic of the circuit showing the 4 T/R switches, two-stage LNA, and variable attenuator. The red, blue, and green arrows indicated the Tx, TXO and Rx paths, respectively. (b) Layout of the $3.2\,\text{mm} \times 1.8\,\text{mm}$ GaN MMIC in the WIN Semiconductors' NP15-00 process.

During transmit operation (Tx), SW_1 is a short and the signal is fed from Port 1 to Port 2. Both SW_2 and SW_3 are biased open along with $0\,\text{V}$ on the gate and drain of the LNA. For transmit signal observation (TXO), the signal is sampled from Port 1 to Port 3 with SW_5 biased OFF and

SW_4 biased ON. Coupling through C_{off} of SW_5 implies that the insertion loss of the transmit signal is not degraded and the sampled signal is at a controlled reduced power level compared to the transmit signal. Depending on the Tx power level and the desired TXO level, SW_6 allows for an additional 10 dB of attenuation to the signal.

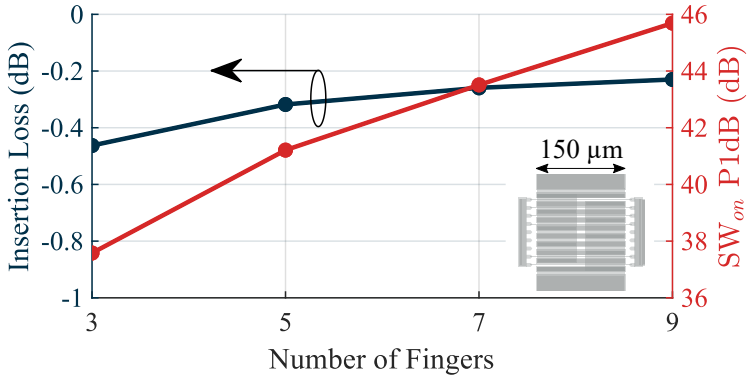


Figure 5.3: Simulated insertion loss and $P1dB_{on}$ of a 150 μm wide switch device as a function of the number of gate fingers. For a $P1dB_{on}$ greater than 45 dBm a $9 \times 150\,\mu$m device is chosen for SW_1.

The performance of the transmit operation is largely determined by SW_1, with a desired low insertion loss and high $P1dB_{on}$ in the ON state. The power handling of an ON switch device is determined by the maximum allowable current through the device, which increases with device size, while the OFF power handling is determined by the breakdown voltage, bias voltage, and pinch-off voltage [50, 51]. Due to process voltages and the maximum V_{bias} of -40 V, SW_5 has a maximum $P1dB_{off}$ of 45.5 dBm. Due to the power handling limited by the $P1dB_{off}$ of SW_5, the desired $P1dB_{on}$ of SW_1 is greater than 45 dBm. Figure 5.3 shows the simulated insertion loss and the $P1dB_{on}$ point of a 150 μm wide switch device with varying number of gate fingers. A $9 \times 150\,\mu$m device is chosen for the desired power handling greater than 45 dBm with an insertion loss better than 0.25 dB. For low C_{off} coupling of the transmit signal, a $3 \times 95\,\mu$m switch device is chosen for SW_5 while a slightly large $5 \times 100\,\mu$m switch is chosen for SW_4.

For Rx operation, the signal is fed through the LNA from Port 2 to Port 3, with both SW_2 and SW_3 biased ON and all other switches biased OFF. With SW_2 at the input and output of

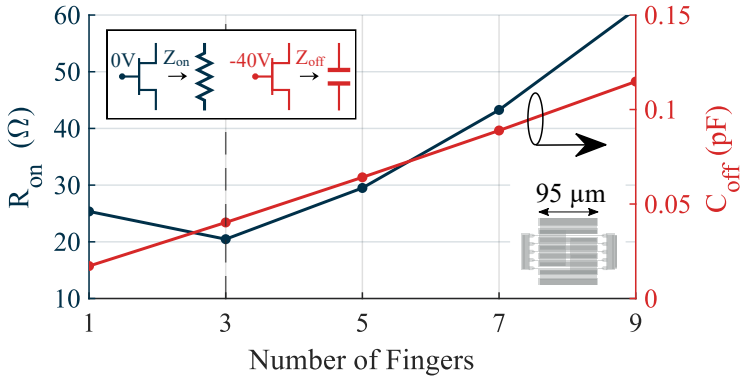


Figure 5.4: R_{on} and C_{off} of a 95 μm wide switch device as a function the number of gate fingers. For the desired trade-off, a $3 \times 95\,\mu$m switch device is chosen for SW_2 at the input to the LNA.

the LNA, the R_{on} of the switch devices can have a major impact on receiver performance, while C_{off} needs to be minimized to avoid leakage to the transmit path. Since a 50 Ω trace is 95 μm wide in the NP15 process, the device width of SW_2 is chosen to be 95 μm, minimizing the required number of tapers. Figure 5.4 show the R_{on} and C_{off} of a 95 μm wide switch device for different gate finger numbers. For a trade-off in R_{on} and C_{off} a $3 \times 95\,\mu$m switch device size is chosen for SW_2 indicated by a vertically dashed line in Fig. 5.4. With a simulated initial compression point $P0.1dB_{on}$ of 25 dBm, the chosen $3 \times 95\,\mu$m switch has sufficient power handling for the LNA input P1dB point. With the same trade-off in R_{on} and C_{off}, but a necessary increase in power due to the LNA gain (28 dBm maximum output power), a $5 \times 100\,\mu$m switch device with a $P_{0.1}dB_{on}$ of 30 dBm is chosen for SW_3.

5.3 MMIC Operation

We next describe how the switching network described above is included in Tx and Rx modes of operation, with more detail given for the variable attenuator and LNA.

5.3.1 Trasnmit Operation

A detailed layout and schematic of the transmit and transmit observation paths is shown in Fig. 5.5a and Fig. 5.5b. The transmit path is again depicted with a red arrow over the $9 \times 150\,\mu$m

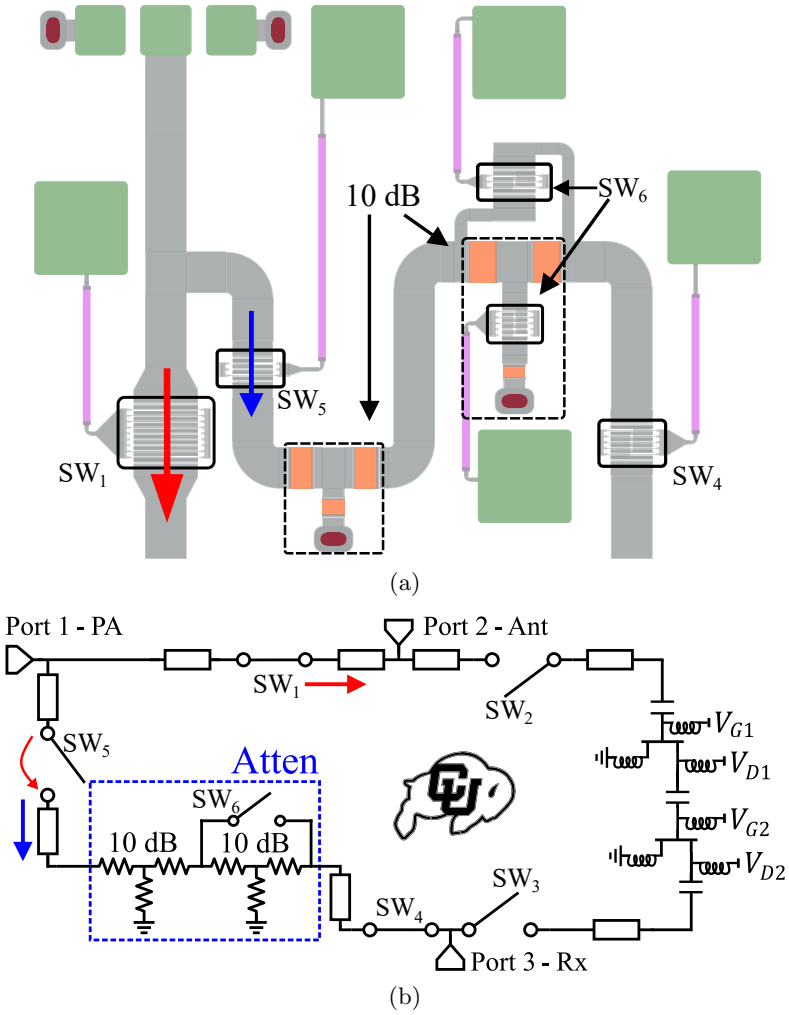


Figure 5.5: (a) Layout of MMIC Tx and TXO paths, denoted with red and blue arrows, respectively. SW_1 uses a $9 \times 150\,\mu$m switch transistor for high power and low insertion loss of the transmit signal. SW_5 uses a $3 \times 95\,\mu$m device for low C_{off} capacitance for sampling low power levels of transmit signal. (b) Schematic of transmit operation.

switch device (SW_1) and the transmit observation path over a $3 \times 95\,\mu$m switch device (SW_5) with a blue arrow. Each switch is biased with a high-resistance mesa resistor. The variable attenuator in the transmit observation path is made of one fixed 10 dB attenuator and switchable resistive T networks, enabling a variation in attenuation of up to 10 dB in the transmit observation power level.

The two resistive T networks are made using precise TaN resistors, seen in Fig. 5.5a. The TaN resistance values are chosen for 10 dB of attenuation and a 50 Ω match, giving a series resistance

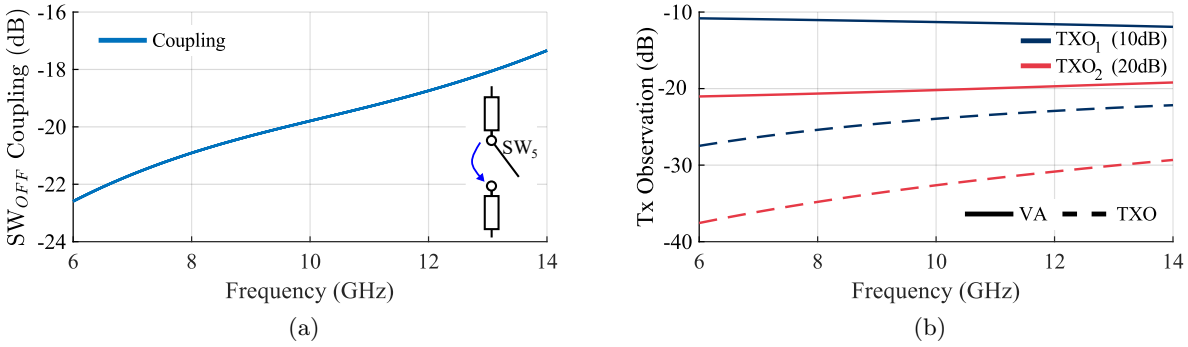


Figure 5.6: (a) Simulated SW_5 C_{off} coupling. (b) Simulated attenuation levels of variable attenuator (VA) in solid and the complete (coupling and VA) transmit observation (TXO) signal path in dashed. The 10 dB attenuation level is shown in blue and the 20 dB attenuation level is shown in red. The dashed transmit observation (TXO) path shows the difference in power level of the transmit (TX) and transmit observation (TXO) signals for the two attenuation levels.

of 26 Ω and shunt resistance of 35 Ω. The switchable attenuation is enabled by SW_6, made with a series $3 \times 100\,\mu$m and shunt $5 \times 60\,\mu$m switch device. The series switch allows for the signal to bypass the attenuator while the shunt switch avoids the signal splitting between the bypass and the attenuator. The R_{on} of the shunt $5 \times 60\,\mu$m switch is taken into account when determining the shunt resistance value to keep the desired match and attenuation. The series switch of $3 \times 100\,\mu$m is chosen for low insertion loss during bypass with isolation better than the desired attenuation level of 10 dB. With the chosen $3 \times 100\,\mu$m, the minimum 11 dB isolation across the band is below the desired attenuation level, with an insertion loss of 0.6 dB.

The transmit signal is sampled through C_{off} of SW_5, which is simulated across frequency and shown in Fig. 5.6a. The performance of the stand-alone variable attenuator is plotted with solid traces in Fig. 5.6b, showing the fixed 10 dB (blue) and switchable combined 20 dB (red) attenuation levels. Figure 5.6b also show the complete TXO path, with dashed traces, through SW_5 C_{off} coupling and the variable attenuator. The plotted transmit observation depicts the difference of the transmit and transmit observation signal levels.

5.3.2 Receive Operation

The Rx circuit layout is shown in Fig. 5.7a. A two stage LNA, SW_2 at the input, and SW_3 at the output form the Rx signal path (green arrow in Fig. 5.7b). The two stage LNA uses two $8 \times 50\,\mu$m linear devices with ungrounded sources that enable inductive source degeneration, chosen as a compromise between based on the NF and power handling. Power handling of the LNA is an

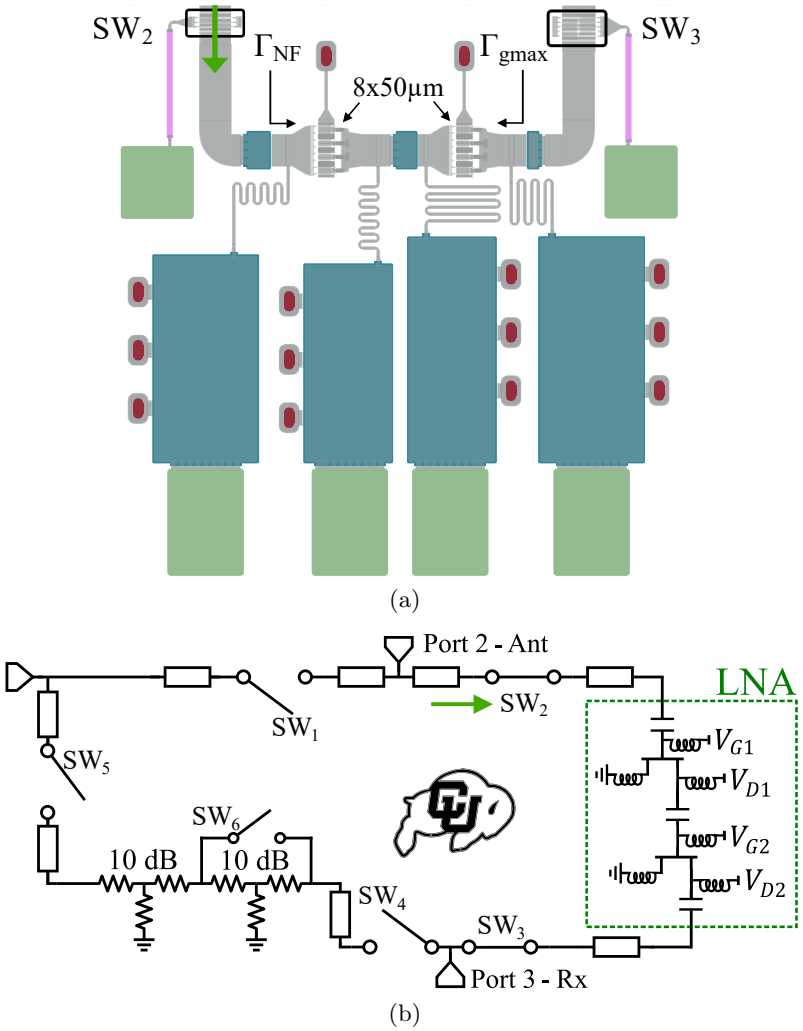


Figure 5.7: (a) Layout of MMIC receive path, denoted with green arrow, co-deigned LNA and switch network. Input of LNA is matched for minimum NF and output is matched for maximum gain, with SW_2 and SW_3 respectively. The choice of fairly large $8 \times 50\,\mu$m devices of the LNA is justified since increasing the number of fingers increases power handling but not NF. (b) Schematic of receive operation.

important consideration for IBFD systems using SIC, which requires the receive signal to remain linear for cancellation. A high power LNA avoids compression due to undesired coupling of the high-power transmit signal, and therefore enables a linear receive signal. For low NF and high power handling, the number of fingers in the device can be increased without greatly affecting the NF, while increasing the power handling. The devices that include noise have only linear models, so the nonlinear behavior of the $8 \times 50\,\mu$m devices is extrapolated from the nonlinear device model at an input P1dB of 17 dBm.

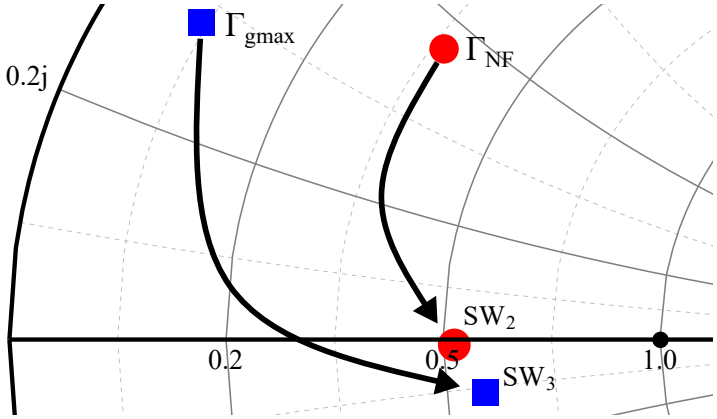


Figure 5.8: Co-designed complex impedance matching of LNA and switch network. Z_{out} of SW_2 is matched to LNA input of Γ_{NF} for lowest NF, shown is red. Z_{input} of SW_3 is matched to LNA out of Γ_{gmax} for highest gain, shown in blue.

During receive mode shown in Fig. 5.7b, SW_2 at the input and SW_3 at the output are co-designed using complex-to-complex impedance impedance matching with the two-stage LNA. This allows for a single matching network at the input and out of the LNA, instead of multiple $50\,\Omega$ matching networks, reducing the loss and complexity. Source degeneration of a $8 \times 50\,\mu$m device is also used to help bring the desired matching impedances closer together for simpler matching. The complex-to-complex impedance matching at the input and output of the LNA can be seen on the Smith chart in Fig. 5.8. The input impedance match is shown with red circles, denoting the optimum match for minimum NF and the output impedance of SW_2. The complex impedance at output of SW_2 is $Z_{\text{sw}} = 26 + j0.5\,\Omega$. This is matched to $Z_{\text{NF}} = 17.5 + j25\,\Omega$, for $\Gamma_{\text{NF}} = 0.56\angle 126°$, giving the minimum NF of the LNA at 10 GHz. The output impedance match is shown with blue

squares, denoting the optimum match for maximum gain (g_{max}) and the input impedance of SW_3. The complex impedance at the output of the LNA for $gmax$ is $Z_{\text{gmax}} = 2.2 + j16\,\Omega$. This is directly matched to the input impedance of SW_3, $Z_{\text{sw}} = 28 + j5\,\Omega$ at 10 GHz.

5.4 Measurement Results

The MMIC is mounted on a gold-plated copper molybdenum (CuMo) carrier, and the dc pads are wire-bonded to off-chip capacitors for stability and ease of probing, shown in Fig. 7.1b. On-wafer measurements are performed with an Agilent Technologies PNA Network Analyser E8364C using a Summit 9000 Probe Station. A 2-port and 3-port calibration is done for small-signal Tx and RX modes, respectively, with on-wafer calibration using a Cascade Microtech Impedance Standard Substrate. Additionally, on-wafer Rx path NF and OIP3 were done with an Agilent Technologies PSA Series Spectrum Analyzer E4448A. On-wafer Rx large signal was done with a Keysight PNA-X Nework Analyzer N5241B. Finally, on-wafer Tx power handling was done with an Agilent N1914A EPM Series Power Meter.

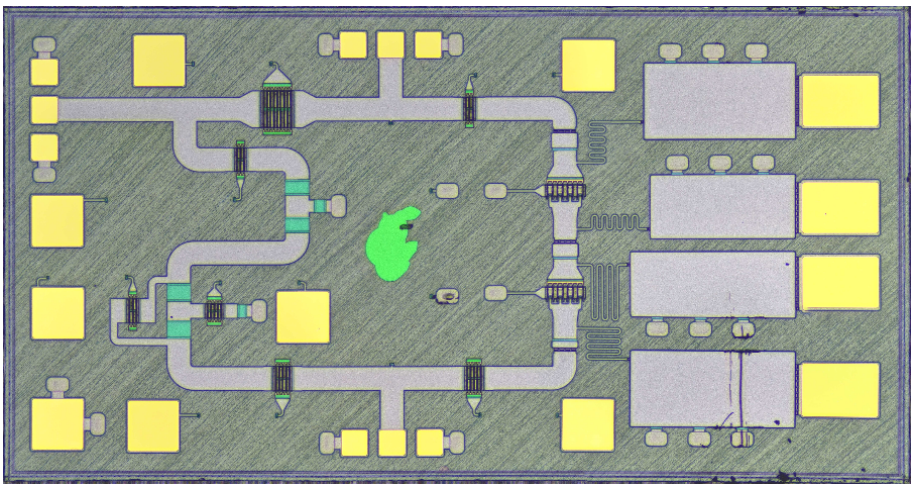


Figure 5.9: Photograph of the fabricated GaN MMIC in the WIN 150 nm NP15 process. The die size is 3.2 mm × 1.8 mm.

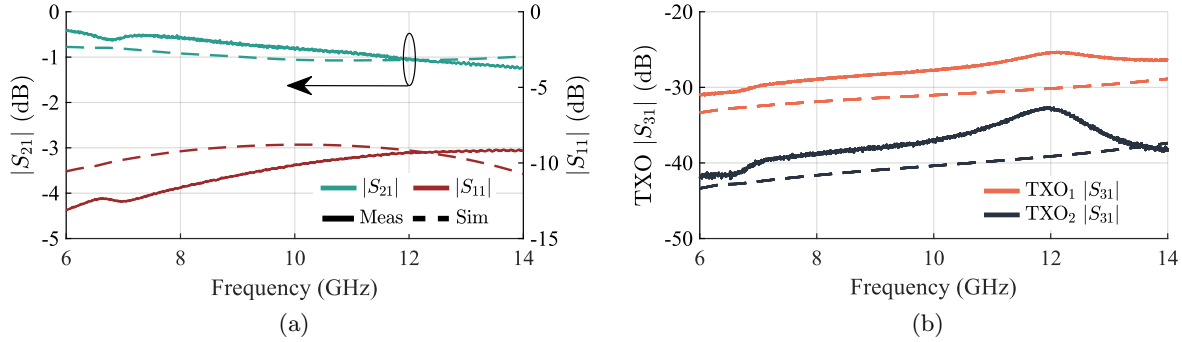


Figure 5.10: Measured (solid) and simulated (dashed) transmit (TX) performance (a) insertion loss and return loss (b) transmit observation (TXO) performance.

5.4.1 Tx and TXO Path Measurements

The 3-port calibration is required to capture transmit and transmit observation performance, shown in Fig. 5.10. For transmit operation switch devices are biased OFF with $V_g = -40\,V$ and ON with $V_g = 0\,V$, while the LNA is grounded for a 0 V bias on both the gate and drain. Fig. 5.10a shows the measured (solid) and simulated (dashed) transmit insertion loss in green and return loss in red. From $8 - 12\,GHz$ the insertion loss is better than 1 dB while the return loss is better than 9 dB. Measurements show similar trends to simulation but are slightly shifted up in frequency.

Figure 5.10b shows the simulated (dashed) and measured (solid) transmit observation path

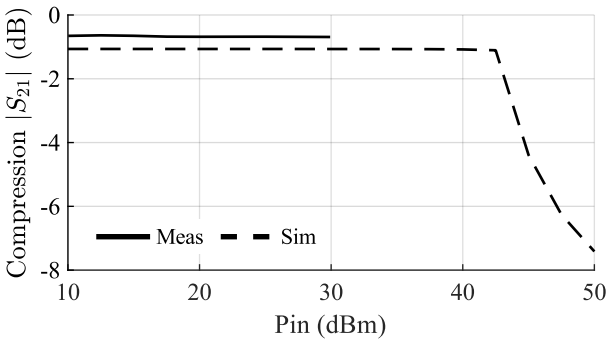


Figure 5.11: Measured (solid) and simulated (dashed) transmit path at 10 GHz with an ON switch bias of $V_g = 0\,V$ and OFF switch bias of $V_g = -40\,V$. On-wafer power measurements could only be performed up to 30 dBm of input power.

for both the 10 dB attenuation level in orange and 20 dB attenuation level in black. Both simulated and measured transmit observation traces show an increase with frequency, as to be expected from the C_{off} coupling of SW_5, but differ in level and variation across frequency. This difference is attributed to numerical convergence issues at low power levels. Additionally, device models that include the noise exist for specific bias levels that do not include 0 V bias. Instead, a separate nonlinear device model, with identical periphery and unspecified device bias levels is used for transmit and transmit observation simulations. This allows for a simulated 0 V bias (off) LNA, but as expected deviates from the measured performance of TXO. To confirm the LNA's impact on the transmit observation path, the LNA is also measured with a gate bias of $V_g = -1$ V and 2 V, which degrades the transmit observation level for both the 10 dB and 20 dB levels.

The measured (solid) and simulated (dashed) power handling of the transmit path at 10 GHz is shown in Fig. 5.11. The measurements were done with an ON switch bias of $V_g = 0$ V and OFF switch bias of $V_g = -40$ V. Due to input driver power limitation, the measurements were done up to 30 dBm of input power which is not sufficient to demonstrate switch compression. The simulated performance shows a sharp compression point at an input power of 42.5 dBm.

5.4.2 Receive Path Measurements

For small signal receive measurements of the co-designed LNA a 2-port calibration was done with the third RF port of the MMIC terminated in 50Ω during measurements. Comparison between measured and simulated receive performance is shown in Fig. 5.12 with good agreement across the band. An LNA drain bias of $V_D = 10$ V and $I_D = 40$ mA for both stages is used, with 0.4 W per stage. The LNA demonstrates a peak gain of 16 dB at 10 GHz and a minimum in-band gain of 12.6 dB at 8 GHz shown in Fig. 5.12a. The receive path measured (solid) and simulated (dashed) NF from 8 to 12 GHz is shown in Fig. 7.26. The measurements show an NF below 2.9 dB across the band and a minimum measured NF of 2 dB at 10.5 GHz.

Additionally, large-signal measurements are done across frequency and power to show compression of the LNA. This is shown in Fig. 5.13 where the receive path has an input P1dB point of

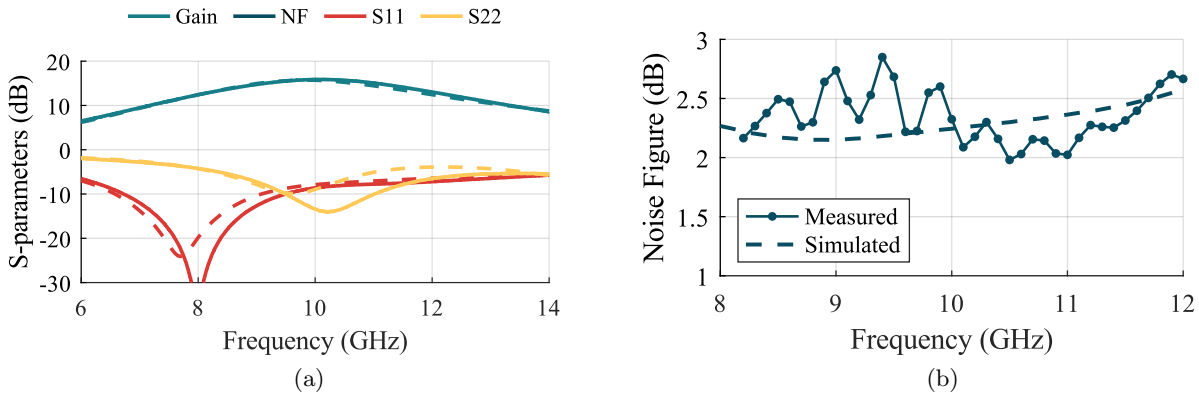


Figure 5.12: Measured (solid) vs. simulated (dashed) small signal Rx performance. (a) Both measurement and simulation are done at a bias of $V_D = 10\,\text{V}$ and $I_D = 40\,\text{mA}$, showing a peak gain of 15.9 dB at 10 GHz, showing good agreement. (b) noise figure performance, showing a measured noise figure of 2.7 dB or lower across the band. Both measurement and simulation are done at a bias of $V_D = 10\,\text{V}$ and $I_D = 40\,\text{mA}$.

5 dBm at 8 GHz and minimal compression at 0 dBm of input power. From the measured compression of the LNA, the max allowable input power to the LNA must remain below 0 dBm for in-band full-duplex operation, in which SIC can be applied to recover the sensitivity of the receiver.

Along with compression of the receive chain, linearity is a key factor for SIC during in-band full-duplex operation. The nonlinearities of the receive path degrade the received signal, reducing

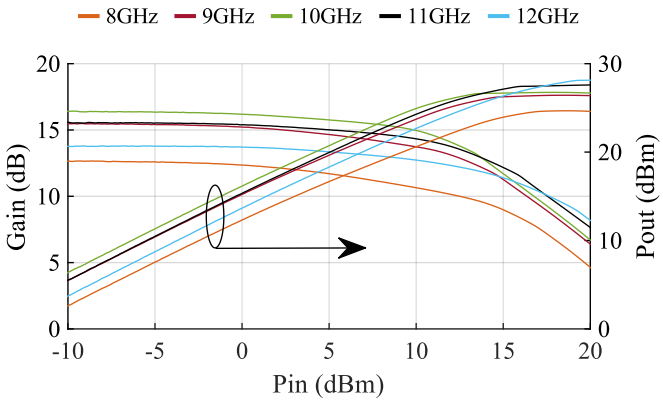


Figure 5.13: Measured compression of the LNA during reception at several frequencies in X band. The large signal measurement demonstrates the saturation level of the LNA during in-band full-duplex operation where SIC techniques can be used to recover receiver sensitivity.

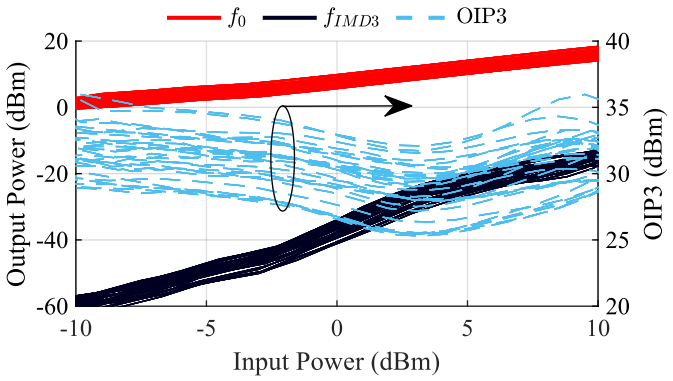


Figure 5.14: Measured receive path IMD3 (solid black) and OIP3 (dashed blue) across frequency. The measurements demonstrate an OIP3 from 25 dBm to 35 dBm across frequncy and power. The fundamental tones power levels are shown with solid red traces, IMD3 in solid back traces, and OIP3 in solid blue traces.

the ability to recover the signal of interest with SIC. The measured OIP3 and IMD3 products of the receive path across frequency and power are shown in Fig. 5.14, again with no simulated comparison due to linear models. The fundamental tones are shown in solid red traces, IMD3 products in solid black traces, and OIP3 in dashed blue traces. Depending on the allowable receive IMD3 products a max coupled receiver input power level can be decided.

5.5 Full-duplex Array Considerations

With the TXO chip fully characterized, and assuming that each transmit-receive element in an array has an analog front end that consists of a PA, and a TXO chip (with an LNA), we next consider self-interference cancellation at the array level.

To determine the TXO sampling, a power amplifier MMIC demonstrated in [80] is connected to the TXO MMIC in a hybrid circuit shown in Fig. 5.15. The MMICs are connected with bond wires to a 50 Ω alumina trace, and dc biased through single-layer capacitors. An on-wafer 3-port calibration is performed to characterize all three ports across frequency. The measurements are done by probing the power amplifier input, antenna, and transmit observation port directly on-wafer. The measured S-parameters of the integrated MMICs and individually measured PAs is plotted in Fig. 5.16. The Tx path in black is compared to the PA in red, showing a very similar

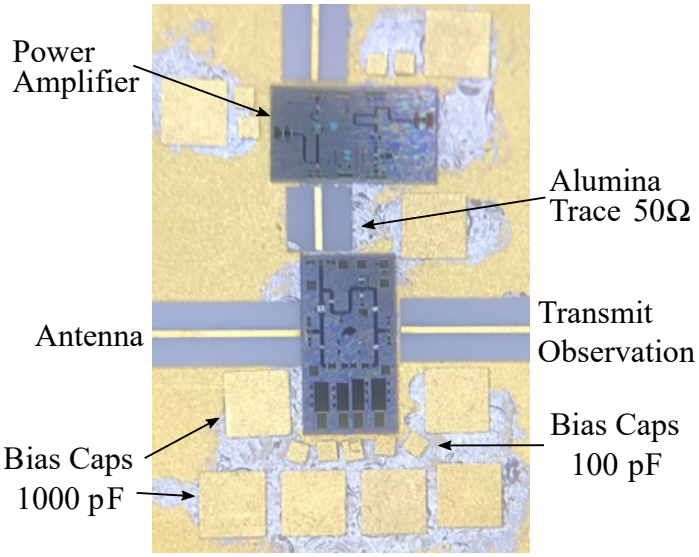


Figure 5.15: Integrated power amplifier and transmit observation MMICs on a (CuMo) carrier. The bias lines of both MMICs are bonded to capacitors for biasing and are RF connected with a 50 Ω alumina trace.

level of gain across frequency. The transmit observation (TXO) signal shown in blue demonstrates an accurate representation of the Tx across frequency and about 25 dB down the output Tx signal. These measurements are performed with the fixed 10 dB of attenuation in the TXO path with SW_6 ON. The match at each port of the integrated MMICs is shown with dashed black traces, with the

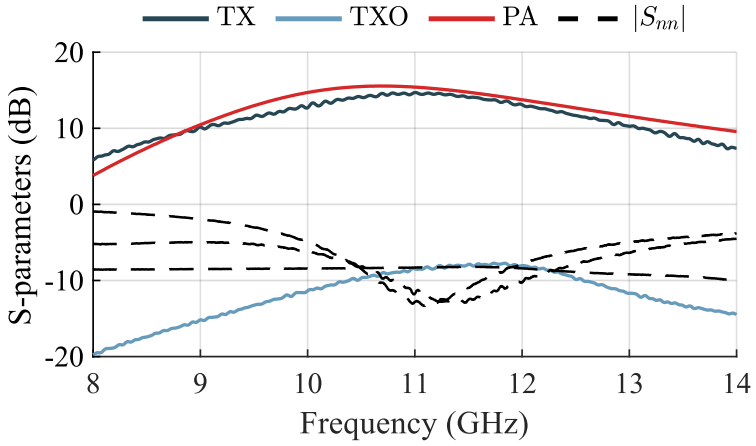


Figure 5.16: Measured integrated power amplifier and transmit observation integrated MMICs demonstrating very minimal performance change in power amplifier (PA) gain and an accurate transmit (TX) signal with transmit observation (TXO).

PA input and antenna port having a match better than 10 dB at 11 GHz. The TXO port shows an almost flat return loss greater than 8 dB from $8 - 14$ GHz.

5.6 Discussion & Conclusions

This chapter presents a co-designed LNA, variable attenuator, and front-end T/R switching network GaN MMIC enabling aperture-level in-band full-duplex operation. The front-end MMIC allows for transmit signal observation at the antenna port, providing an accurate signal representation for enhanced digital self-interference cancellation. The transmit-mode switch insertion loss is less than 1 dB, with a return loss greater than 10 dB across X-band, and a simulated power handling greater than 40 dBm.

The transmit observation path uses a variable attenuator for power level adjustments for differing transmit power levels. The LNA is co-designed with the T/R switching network and exhibits a minimum NF below 2 dB and a max gain of 16 dB. The LNA compression and linearity are measured to determine the max allowable receive input power and the allowable added receive nonlinearity. Additionally, the MMIC is integrated with an X-band power amplifier to demonstrate the observation of the transmit signal. The measurement of the integrated MMICs shows an accurate observation of the transmit signal with about 25 dB reduction in signal level compared to the transmit signal. The transmit signal of the integrated MMICs through the transmit observation is also compared to the stand-alone power amplifier, which shows very comparable gain across frequency.

The demonstrated MMIC is designed for insertion into an aperture-level full-duplex antenna system with downconversion and digital self-interference cancellation enabled for reconfigurable T/R array elements. Sampling of the transmit signal at the antenna level the nonlinearities and noise that is generated in the transmit path can be accurately represented during digital SIC. Implementing direct analog cancellation between each element in an array becomes increasingly difficult as the number of elements increases, resiting the array size. By relying on the digital domain for cancellation, the array size can be increased without a large increase in complexity.

Chapter 6

T/R Module for Advanced Phased Array Systems (TAPAS)

In a completely ideal case, with an ideal noiseless linear transmit chain that is fully characterized, the transmit signal can be easily reproduced in the digital domain for cancellation. In a practical nonlinear noisy system, the transmit signal cannot be easily reproduced for cancellation, lowering the isolation between transmit and receive. To increase the SIC, previous work shows the cancellation signal replicated in the analog domain with a duplicated transmit chain [13], increasing the hardware complexity of the system. The noise amplified through the transmit chain cannot be appropriately characterized by a duplicate transmit chain, lowering the cancellation level.

For more accurate transmit signal representation, the signal can be sampled at the antenna port after the signal has passed through the transmit chain. This is referred to as the "transmit signal observation (TXO)". Knowledge of the transmit signal enables the signal used for self-inference cancellation to account for noise and nonlinearity that have been added to the transmit signal [33]. Furthermore, the sampling hardware can be integrated at the front-end of the system, utilizing the receive path, reducing the overall complexity and required hardware. Finally, to enable scaling of the full-duplex phased array without added complexity, no cancellation is done in the analog domain, instead, cancellation is only done in the digital domain with direct digitization RFSoC ([81]) using the TXO signal.

This architecture is shown in Fig. 6.1, with only four elements for simplicity. Each element is operating in either transmit (Tx) or receive (Rx) mode, determined by the front-end switch. In the transmitting elements (shown in red), the signal is coupled through the capacitance of the

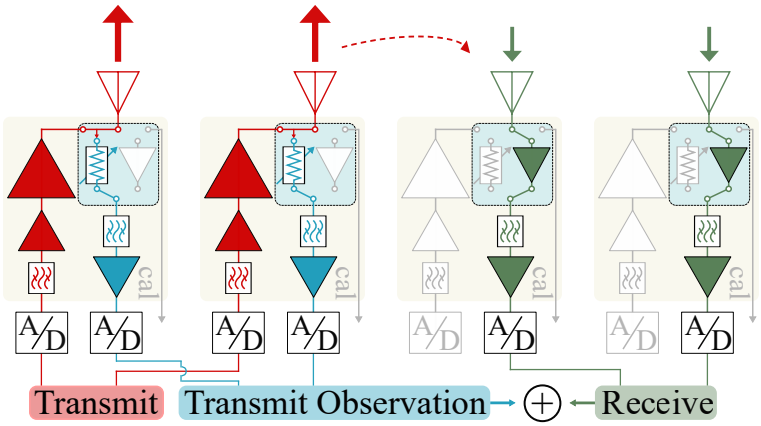


Figure 6.1: Lincoln Laboratory aperture-level in-band full-duplex phased array block diagram, with transmitting (TX) elements of the front end shown in red, while the receiving (RX) elements are shown in green. The transmit observation (TXO) path, shown in blue, demonstrates the transmit signal, which provides information for digital self-interference cancellation. The coupled transmit signal is shown in the dashed red line. The front-end TR module is shaded in tan, with the blue shaded GaN MMIC in the front-end TR module. Only two TX and RX elements are shown for clarity.

off switch and fed through the variable attenuator (VA), for transmit signal observation (TXO), shown in blue. For the elements in the receive operation, shown in green, the signal is fed through a high-power low-noise amplifier (LNA) to avoid damage from the high-power self-interference. After digitization of the transmit observation signal and the received signal, digital cancellation is used to recover the received signal of interest. With the system designed to operate from 2.7 GHz to 3.5 GHz allowing for direct analog to digital conversion. Before transmission and reception, the system is calibrated (cal), shown in gray, for a reduction in digital computation [6]. This is enabled by the high power and high linearity gallium nitride (GaN) co-designed MMIC [50, 82] at the front end of each element, as seen in the dashed box shaded in blue. The GaN MMIC is packaged and then mounted on a PCB T/R module, shaded with a tan box.

The designed T/R module schematic, operating from 2.7 to 3.5 GHz, is shown in Fig. 6.2. The module incorporates a commercially available GaN high power amplifier (HPA) from Qorvo [83], with an output power of 46 dBm. The output of the HPA is then connected to the designed transmit observation MMIC, shown in a dashed box within the T/R module schematic. The top

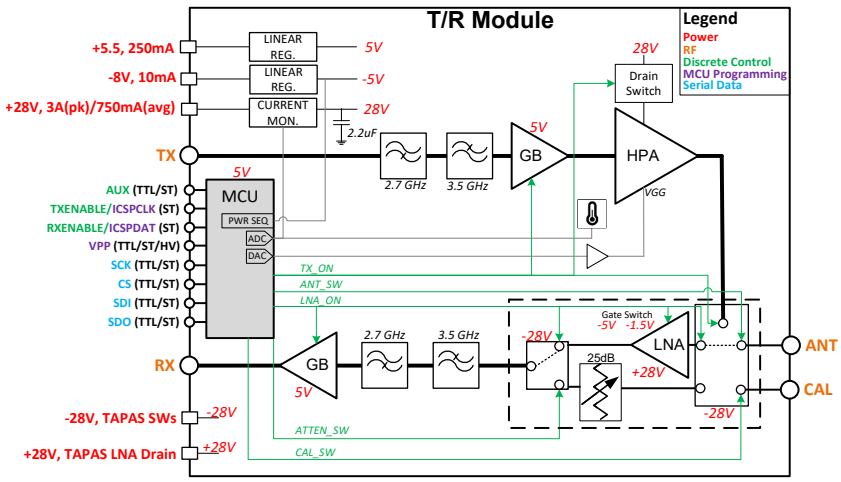


Figure 6.2: Schematic of T/R module incorporating designed MMIC in the dashed black box.

side of the fabricated 1.2 in × 0.6 in PCB T/R Module, intended for phased array packaging, is shown in Fig. 6.3. For the incorporation of the transmit observation MMIC in the PCB, the chip is packaged in a 30-pin QFN package. The packaged MMIC, with the second largest footprint on the board, can be seen on the right side of Fig. 6.3. For thermal management of the PCB board, a cold plate is connected to the back of the board centered around the HPA and TXO MMIC.

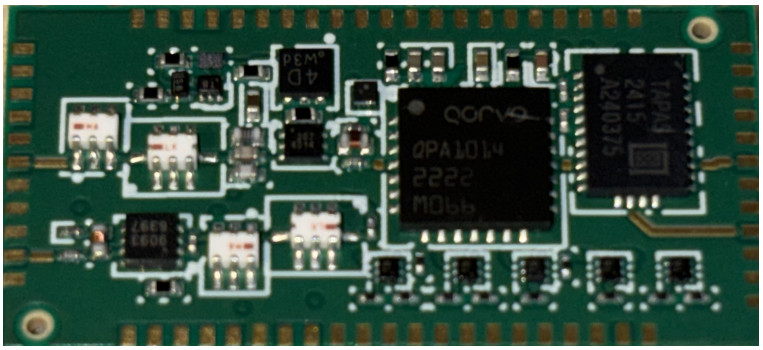


Figure 6.3: Fabricated 1.2 in × 0.6 in PCB TR module with packaged MMIC on far right of the board.

The remainder of this chapter will focus on the designed GaN-on-SiC MMIC to allow for the presented aperture-level in-band full-duplex architecture. The remainder of this chapter is organized as follows. Section 6.2 details the design and measurements of the T/R switching network for a

reconfigurable array. Section 6.3 shows the designed and measured high-power LNA for receive during full-duplex operation. Section 6.4 discusses the designed and measured variable attenuator and transmit observation sampling for accurate digital SIC.

6.1 MMIC For Full-Duplex Transmit Observation

A block diagram of the designed MMIC is shown in Fig. 6.4, with ports Tx, Rx, TXO, cal, and the antenna. The LNA and the variable attenuator are highlighted in blue and green, respectively, corresponding to receive and transmit observation signal in Fig. 6.1. The T/R switching network of the MMIC is broken up into a 5-port switch at the front-end of the MMIC (LNA and variable attenuator input) and a single-pole double-throw (SPDT) switch at the back of the MMIC (LNA and variable attenuator output). The front-end switch allows for the system to switch between transmit, receive, and transmit observation or calibration. The back-end switch allows for the receive and transmit observation signals to use a single output port for the same back-end hardware chain, reducing complexity and overall hardware of the system.

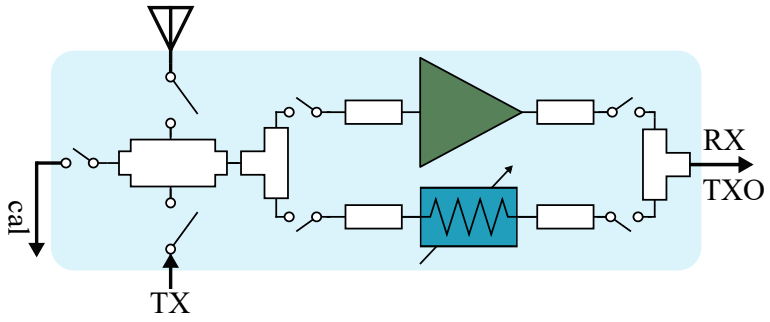
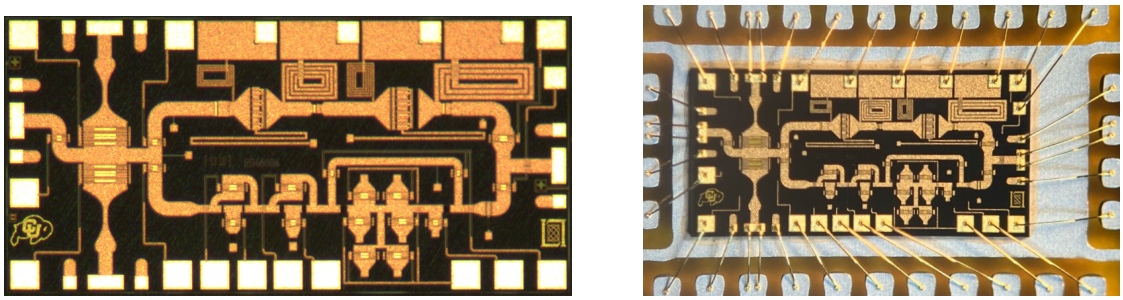


Figure 6.4: Block diagram of GaN MMIC for transmit observation, consisting of a T/R switching network, low-noise amplifier (LNA), and variable attenuator (VA).

The fabricated MMIC, as seen in Fig. 6.5a, is designed in Qorvo's GaN-on-SiC QGaN25 process, featuring 250 nm GaN transistors fabricated on a 100 μm thick SiC substrate. The process has a maximum operating frequency of 18 GHz and a power density of 8 W/mm, providing state-of-the-art power density at S-band frequencies [61]. Additionally, the process has a breakdown voltage greater than 100 V and an operational voltage of 40 V, allowing for high off switch power handling



(a) (b)

Figure 6.5: (a) QGaN25 GaN-on-SiC 4 mm × 2 mm MMIC and (b) QFN packaged MMIC with two bond wires on each signal GSG bond pad.

[50]. The process design kit (PDK) consists of GaN HEMT nonlinear models, linear noise models, and linear switch devices with a max gate width of 300 μm. The PDK also includes passives with three metalization layers, TaN and Mesa Resistors, through-wafer vias, and capacitors. The MMIC is also packaged in a 30-pin QFN, as seen in Fig. 6.5b, for PCB integration. Due to a high-power transmit signal, the transmit path requires two bond wires for current handling. To increase the size of the signal bond pad, allowing for multiple bond-wires, a 250 μm pitch GSGs is used at each RF port.

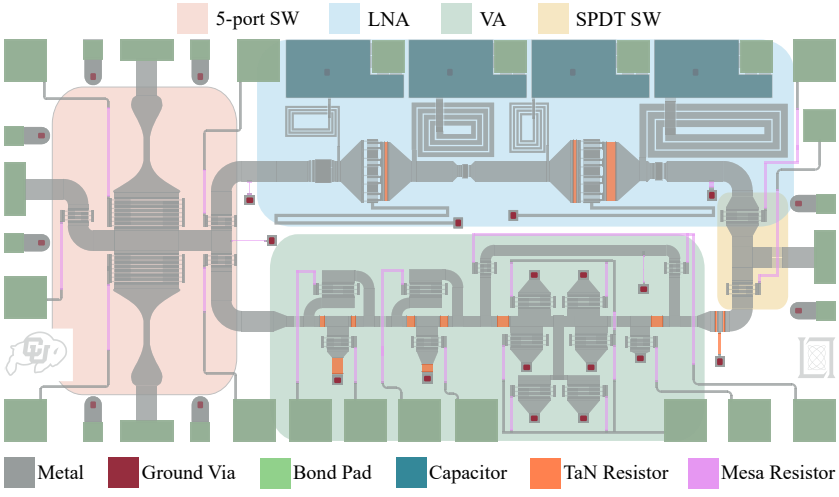
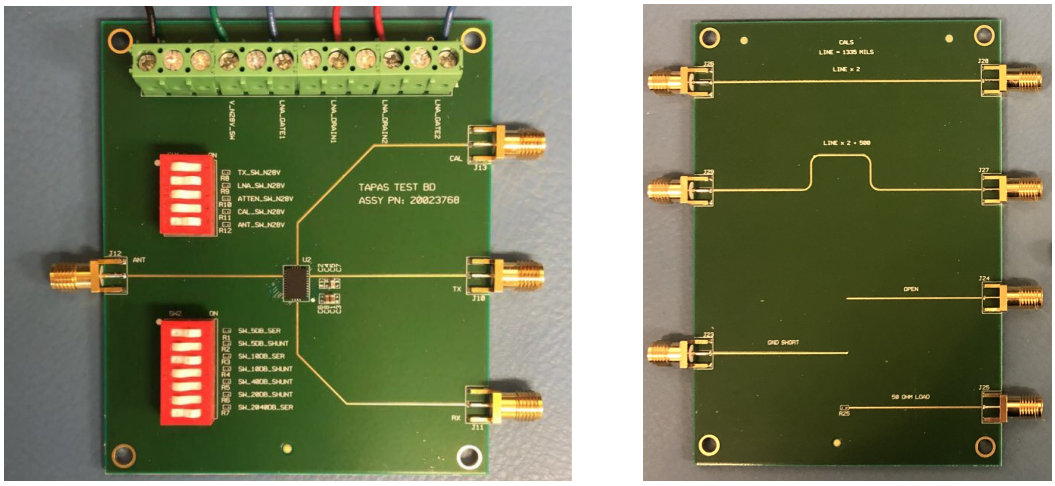


Figure 6.6: Layout of 4 mm × 2 mm GaN MMIC.

The layout of the 4 mm × 2 mm GaN MMIC is shown in Fig. 6.6, with specific coloring for different components. The metal traces are colored in gray, bond pads are shown in green, grounded vias in red, and capacitors in teal. For thicker traces, both metal layers are used, connected by a continuous via, for high current handling lines. To allow for bias routing air bridges are used, only using the top metal, which is seen in light gray. The design also uses both TaN and Mesa resistors, depending on the desired resistance value. The TaN resistors, seen in orange, with lower Ω/sq and a tighter tolerance, are used for variable attenuator resistive tees and increased stability of the LNA. For biasing that does not draw current, and a high resistance value is desired, Mesa resistors are used, seen in pink.



(a) (b)

Figure 6.7: (a) MMIC test board (b) calibration board for MMIC testing.

For testing of the packaged MMIC, an evaluation board with switches for switch device biasing is used. The evaluation board can be seen in Fig. 6.7a, with the black QFN in the center of the board and the switches on the left of the board in red. Additionally, to the right of the chip are surface mount capacitors on the bias lines of the LNA for stability. With the evaluation board, high power measurements, above on-wafer probe limitations, are possible for the transmit path, along with each variable attenuation state of the transmit observation path. To calibrate

the package plane, a calibration board consisting of a short, open, load, thru, and line is used as seen in Fig. 6.7b. For direct comparison to the simulation and evaluation of the chip, on-wafer measurements are performed in addition to measurements at the package plane with the test board.

6.2 T/R Switching Network

The T/R switching network of the MMIC (5-port and SPDT switch) is highlighted in Fig. 6.8. As mentioned previously, the 5-port switch at the front-end of the MMIC is on the left of the figure, and the back-end SPDT switch is on the right of the MMIC. All of the switch devices are biased at the gate through a high-resistance MESA resistor, drawing no current. With a small-signal design trade-off of R_{on} and C_{off} for each switch device, the large-signal power handling is also a consideration. The P_{off} and P_{on} switch power handling, as shown in chap. 3 (equations 3.1 and 3.2), determine the allowable transmit power level. Power handing for P_{off} and P_{on} are dependent on the impedance presented with P_{off} directly proportional and P_{on} being inversely proportional. For the presented design, we are using the standard impedance of 50Ω. The P_{off} determined by voltage can be increased by stacking switch devices, while P_{on} determined by the maximum allowable current through the device can be increased with device size.

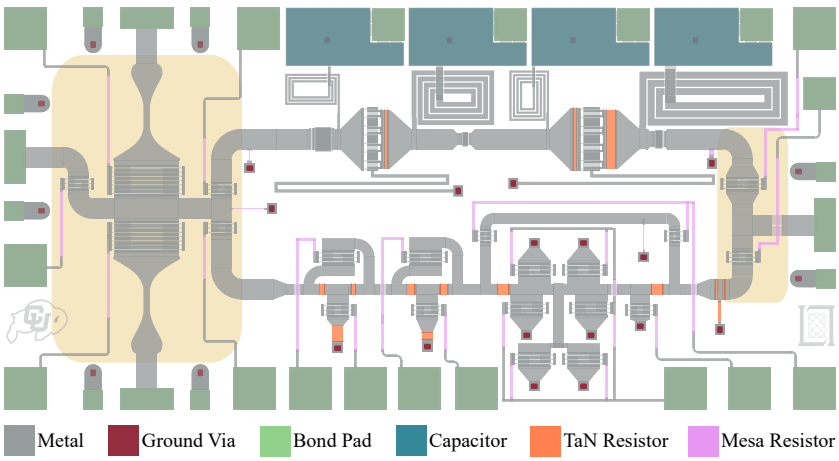


Figure 6.8: Layout of MMIC with highlighted switching networks. The front-end 5-port switching network is on the left and the back-end single-pole double-throw switching network is on the right.

6.2.1 Front-End 5-port Switch

The front-end 5-port switch, through which the high power 46 dBm transmit signal passes, requires a switch device with a P_{on} greater than the transmit signal. Due to P_{off} having a power handling of 47 dBm (50 W), with a -40 V gate bias, in a 50Ω environment, the desired P_{on} of the transmit switch device is greater than or equal to 47 dBm (50 W). Fig. 6.9 plots current vs. Pin for a 50Ω load with the largest available switch device in the PDK of $5 \times 300\,\mu$m, using to extrapolate the current for a $7 \times 300\,\mu$m switch device. The desired 50 W switch input power (PA output power) is labeled with a solid vertical line showing a device current just below 1500 mA. Additionally, the maximum allowable current of a $5 \times 300\,\mu$m and $7 \times 300\,\mu$m switch device is shown with dashed horizontal lines, indicating the maximum input power where the dashed lines intersect the blue trace. Due to the $5 \times 300\,\mu$m device having a maximum current below the 50 W vertical line and the $7 \times 300\,\mu$m device having a maximum current above the vertical line, a $7 \times 300\,\mu$m switch device size is chosen for the transmit path. Due to a fixed number of fingers in the largest PDK switch device of 5 fingers and maximum width of 300 μm, a $7 \times 300\,\mu$m was drawn from the $5 \times 300\,\mu$m device and simulated with two $5 \times 210\,\mu$m in parallel to match device periphery. For the receive operation of the front-end switch, the maximum input power will be limited by the LNA input

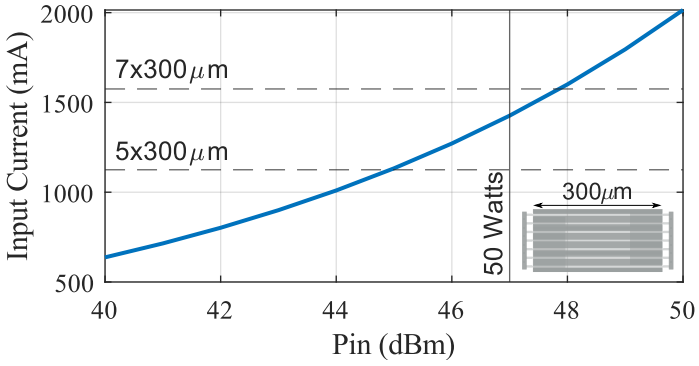


Figure 6.9: Current through ON switch device across input power. The solid vertical lines show the current through the device with a 50 W (47 dBm) input power. The maximum allowable current of a $5 \times 300\,\mu$m and $7 \times 300\,\mu$m switch device is shown with a horizontal dashed lines. The $7 \times 300\,\mu$m device is implemented in the transmit path for a P_{on} greater then 50 W.

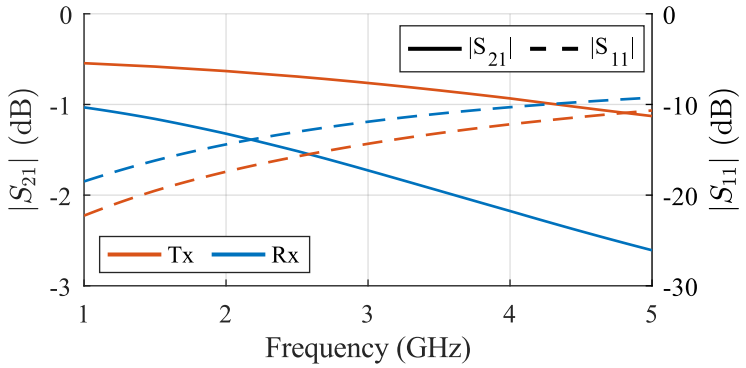


Figure 6.10: Simulated transmit and receive path of the front-end switch. The $|S_{21}|$ for each path is in solid and the $|S_{11}|$ of each path is shown in dashed.

power of less than 10 dBm for linear operation. Using a $3 \times 95\,\mu$m switch device, which matches the 50 Ω trace width, the receive path has a P_{on} of 30 dBm for sufficient receive power handling.

With the device size mentioned above, Fig. 6.10 shows the simulated small signal transmit and receive path through the front-end 5-port switch. The loss for each path is shown with solid traces and the match at the input for each path is shown with dashed traces. The transmit path shown in orange shows less than 1 dB of path loss and a match better than 10 dB below 4 GHz. The receive path shown in blue has a slightly degraded performance compared to transmit, as expected with the smaller $3 \times 95\,\mu$m device having a larger R_{on} and the larger C_{off} from the $7 \times 300\,\mu$m

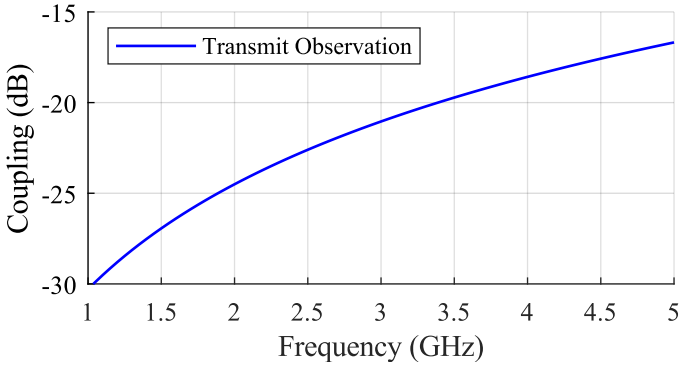


Figure 6.11: Simulated C_{off} coupling of the transmit observation path through off $3 \times 95\,\mu$m switch device.

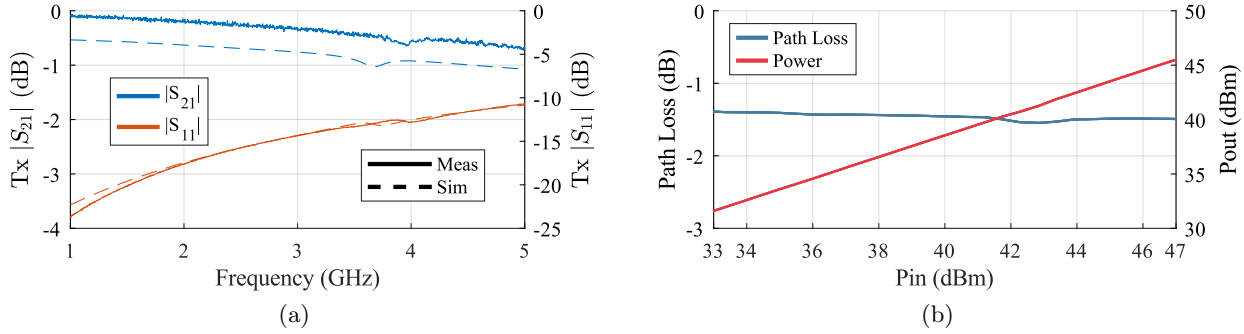


Figure 6.12: Measured (solid) and simulated (dashed) (a) on wafer small signal and (b) test board large signal transmit path.

device.

Similar to the receive path, the transmit observation path uses a $3 \times 95\,\mu$m switch device but is instead biased OFF, using the C_{off} coupling of the device to sample the transmit signal. This allows for a large reduction in power level from the transmit signal as well as minimal loss to the transmit signal power. Fig. 6.11 shows the reduction in power level from the transmit signal to the transmit observation signal through the C_{off} coupling across frequency. From 2.5 to 3.5 GHz the coupling ranges from 23 to 20 dB, which will be further reduced in power level to the desired level using the implemented variable attenuator.

Measurements of the transmit path are shown in Fig. 6.12, with on-wafer small-signal in Fig. 6.12a and breakout board large-signal in Fig. 6.12b. Due to a shorted layout of the $7 \times 300\,\mu$m device in the transmit path, the devices are shorted and can not be biased off. This increases the loss before the LNA during the receive operation, lowering the overall receive gain. From the two $7 \times 300\,\mu$m devices being shorted the loss during transmit, shown in blue, is reduced compared to simulation as shown in Fig. 6.12a. Large signal measurements of the transmit path are done with the breakout board for an available input power of 47 dBm at 3 GHz. This is calibrated to the QFN package having a total path loss of about 1.5 dB and no compression up to 47 dBm of input power as shown in Fig. 6.12b.

6.2.2 Back-End SPDT Switch

The back-end single-pole double-throw switch uses a single output for either the LNA during receive or the variable attenuator for transmit observation during transmit operation. The maximum input power seen by the SPDT switch is the maximum output power of 35 dBm from the LNA, which is above P_{on} of the $3 \times 95\,\mu$m switch device, while the output power of the variable attenuator will remain below 0 dBm. Fig. 6.13 shows the device current across input power with a vertical line showing the max LNA output power at 35 dBm. Using a $5 \times 150\,\mu$m device, shown with a horizontal dashed line, a current handling sufficient for greater than 35 dBm of input power is achieved.

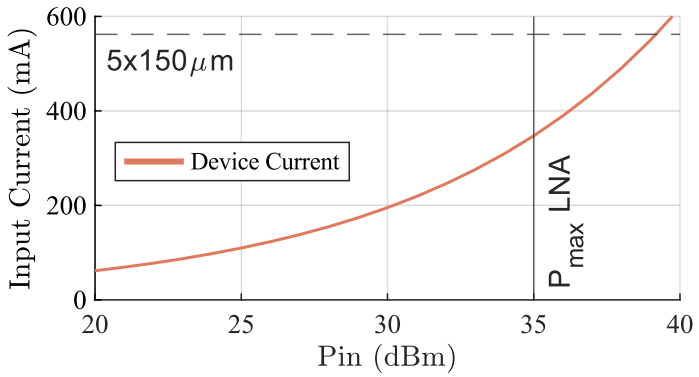


Figure 6.13: Current through the ON switch device across the input power of the back-end SPDT switch, power handling of LNA output power. The solid vertical line shows the maximum output power of the LNA and the resulting current through the device. The horizontal dashed line shows the chosen $5 \times 150\,\mu$m device current handling and the resulting P_{on} of the device being sufficiently above the LNA output power.

Implementing a $5 \times 150\,\mu$m device on receive path (LNA output) and a $3 \times 95\,\mu$m on the transmit observation path (variable attenuator output) the simulated small signal SPDT switch is shown in Fig. 6.14. The path loss ($|S_{21}|$) for receive and transmit observation are shown in solid traces while the input match ($|S_{11}|$) is shown with dashed traces. The receive path, shown in orange, shows a slightly reduced path loss compared to the transmit observation due to a reduced R_{on} in the receive path from the larger $5 \times 150\,\mu$m switch device.

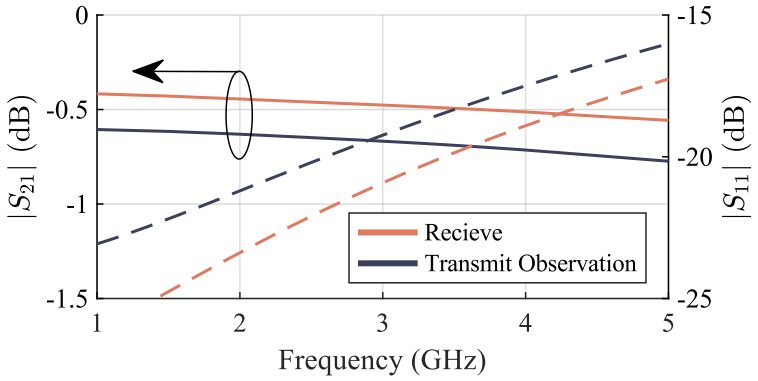


Figure 6.14: Simulated small-signal receive and transmit observation path of the back-end SPDT switch. The $|S_{21}|$ for each path is in solid and the $|S_{11}|$ of each path is shown in dashed.

6.3 Receive - Low Noise Amplifier

The receive path 2-stage low noise amplifier of the GaN MMIC is highlighted in Fig. 6.15, showing a compact 2.4 mm × 0.9 mm design to allow for MMIC integration. For aperture-level in-band full-duplex, which has a high power receive signal from the coupled transmit signal, the LNA needs to be robust to avoid damage in addition to keeping the receive signal linear for SIC. The implementation of the LNA in GaN provides a high power robust LNA compared to gallium

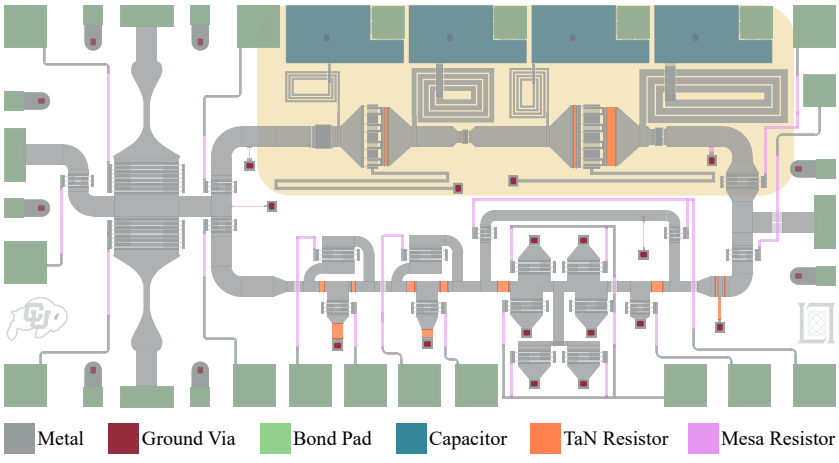


Figure 6.15: Layout of MMIC with highlighted receive path LNA. The LNA has an area of 2.4 mm × 0.9 mm.

arsenide (GaAs) and indium phosphide (InP) [77] [84], removing the need for a limiter, keeping the receive signal linear, and a competitive noise figure [79].

6.3.1 Design

For increased LNA power handling the device size can be increased with a trade-off of higher noise figure and increased drain current. For overall system specifications, the maximum combined drain current is 100 mA. Fig. 6.16a shows the nonlinear device model extrapolated to the linear noise model periphery gain compression for multiple device sizes at 3 GHz. As expected, with increasing device size the power handling increases with the smallest device ($8 \times 25\,\mu$m) having an input P1dB of 0 dBm. Using the same device peripheries Fig. 6.16b shows the minimum NF and drain current at 3 GHz for each linear noise device model. For a desired P1dB greater than 0 dBm and comparable noise figure, the next largest device of $8 \times 50\,\mu$m, having a drain current of 40 mA, is chosen for the first stage. To increase power handling, a larger device is chosen for the second stage to avoid the first stage gain compressing the second stage prematurely. With the maximum allowable drain current of 100 mA an $8 \times 75\,\mu$m device, with a drain current 60 mA, is chosen for increased power handling while keeping the total drain current within 100 mA. Although the $8 \times 75\,\mu$m device has a larger noise figure do to being implemented at the second stage, the

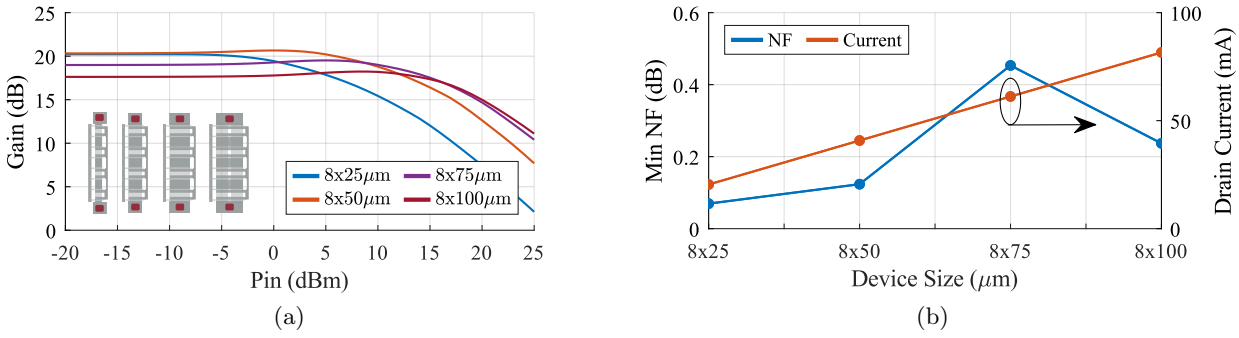


Figure 6.16: (a) Simulated nonlinear device model's power handling extrapolated to linear noise device model periphery at 3 GHz. (b) Simulated linear noise device model noise figure and drain current across device size at 3 GHz.

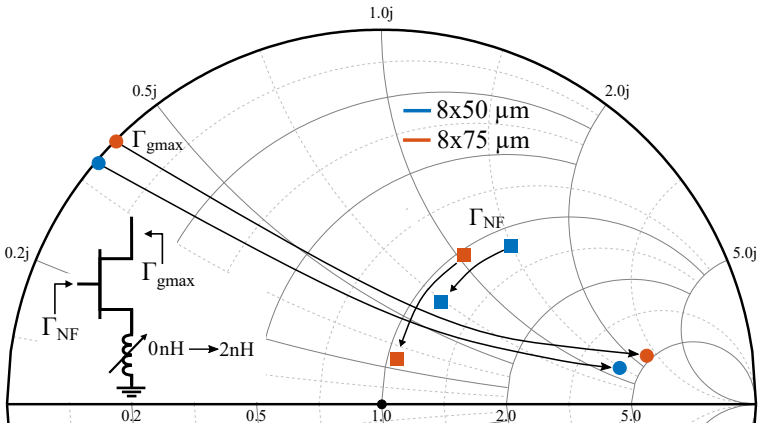
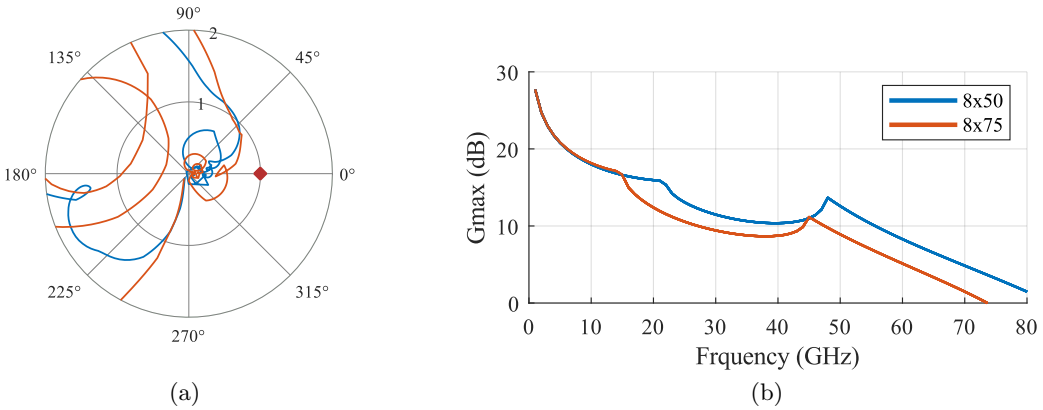


Figure 6.17: Ideal matching impedance of the gate (Γ_{NF}) and drain (Γ_{gmax}) as source inductance is increased.

impact on noise figure is reduced from the gain of the first stage.

The chosen device sizes for the first and second stages of the LNA source degeneration at each stage were used for simultaneous noise figure and gain match. The matching network of the LNA was designed for a minimum noise figure at the input (gate) and maximum gain at the output (drain) of each device. Fig. 6.17 show the optimum impedance match for noise figure (Γ_{NF}) at the input of each device and gain (Γ_{gmax}) at the output of each devise as a function of ideal inductance on the source at 3 GHz from 0 nH to 2 nH. Using the source inductance, both Γ_{NF} and Γ_{gain} can



(a) (b)

Figure 6.18: (a) Loop gain stability analysis of stage 1 $8 \times 50\,\mu$m device (blue) and stage 2 $8 \times 75\,\mu$m device (blue). (b) Gmax of $8 \times 50\,\mu$m and $8 \times 75\,\mu$m devices.

be shifted towards 50 Ω with a reduction in the Q of the optimal matching impedance.

For a compact LNA, the matching network size needs to be simple for minimal area. Using long thin shunt traces for source degeneration, the optimal gate and drain impedance are shifted for ease of matching. Each gate and drain is matched with a specific bias line inductance, to a resonant short 3 GHz capacitor for biasing, taking up minimal area. The inductors on the drain for each device use wide traces for current handling, while the gate inductors, not requiring current handling, use thin traces.

To ensure LNA stability, loop gain analysis [85] shown in Fig. 6.18a is used for both stages, seen in blue and orange. Due to possible out of band oscillations, the analysis was done from 1 MHz to $G_{max} = 0$, as shown in Fig. 6.18b. The LNA shows stable operation with the +1 and 0 ° point not being encircled, as shown with a red square in Fig. 6.18a.

6.3.2 Receive Measurement

The measured receive path small signal parameters with the evaluation board in solid traces are shown in Fig. 6.19 along with the simulated noise figure with a dashed trace, for a drain voltage of 30 V and current of 100 mA. Using the designed board, an SOLT calibration was used

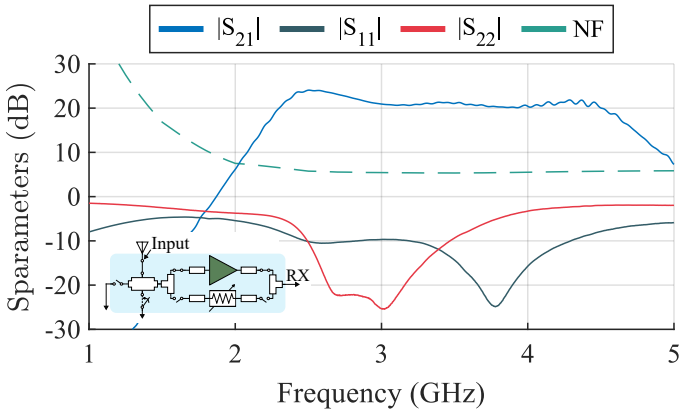


Figure 6.19: Measured receive path on board packaged Sparameters and simulated wafer level NF with a drain voltage of 30 V and current of 100 mA. The packaged MMIC demonstrates a receive path gain greater than 20 dB from 2.5 GHz to 4.5 GHz. A diagram of the T/R switch configuration is shown in the bottom left of the figure, with the switch loss as part of the measurement.

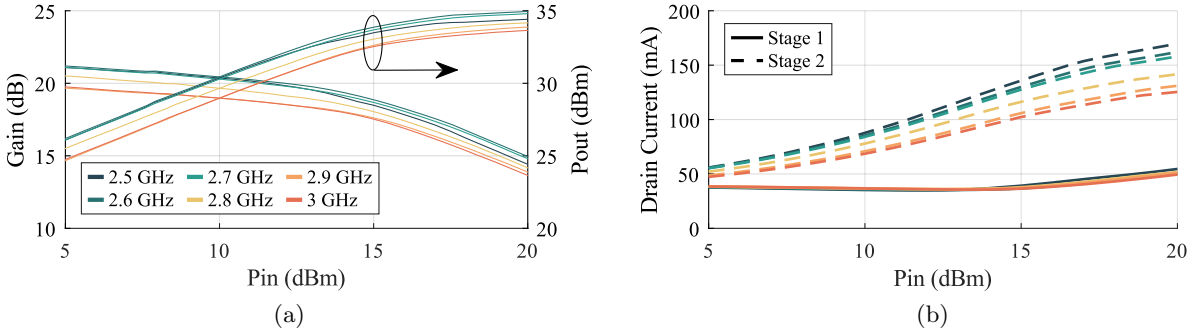


Figure 6.20: (a) Large signal measurement of receive path using the evaluation board calibrated to the package plane. (b) Associated LNA stage 1 (solid) and stage 2 (dashed) drain current across input power.

for calibration to the package plane, removing board loss. Due to the QFN package not being simulated, the measured small signal parameters do not have a direct simulated comparison. The receive path demonstrates a gain greater than 20 dB from 2 to 4.5 GHz along with an $|S_{11}|$ and $|S_{22}|$ better then 10 dB from 2.5 to 3.5 GHz. The simulated noise figure, which is done at the wafer level, stays below 5.5 dB from 2.5 to 4.5 GHz.

Large signal measurement of the receive path LNA is shown in Fig. 6.20a from 2.5 to 3 GHz in 0.1 GHz steps. The associated drain current across input power for each stage is shown Fig. 6.20b,

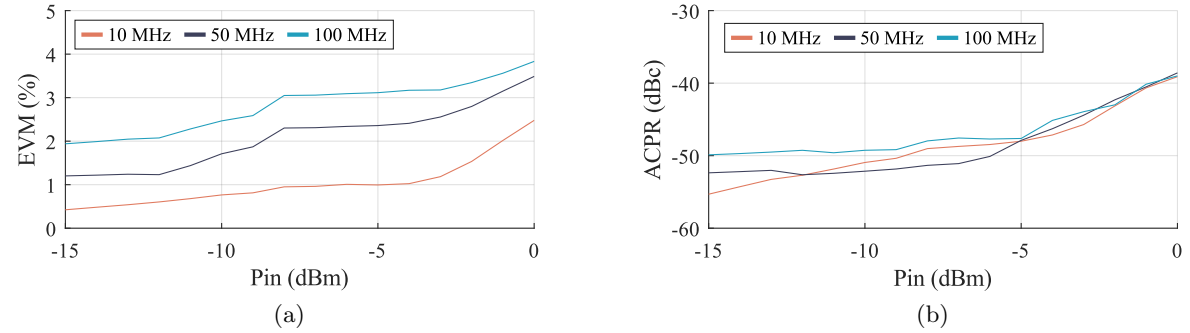


Figure 6.21: Receive path (a) EVM and (b) ACPR measurements across input power with varying signal bandwidths centered at 3 GHz. With an input power below −5 dBm, both EVM and ACPR show high receive path linearity.

highlighting the input power effect on drain current. The measurement on done with the PCB evaluation board, calibrated to the package plane with higher frequency range measurements limited to the available driver frequency range. No simulated traces are shown due to the previously mentioned linear noise figure device models that do not simulate compression. At 3 GHz the receive path shows an input P1dB point of 10 dBm and the ability to handle more than 20 dBm of input power without damage.

Receive path EVM and ACPR linearity measurements across input power are shown in Fig. 6.21a and Fig. 6.21b using a Rohde & Schwarz FSW signal and spectrum analyzer. The measurements are done with a signal bandwidth of 10 MHz, 50 MHz and 100 MHz. EVM shows a max of 3 % with a 100 MHz signal bandwidth for an input power of −5 dBm or lower. The ACPr for all three signal bandwidths hovers right around −50 dBc with an input power below −5 dBm. Shown from the linearity measurements with an input power of −5 dBm or lower, the receive path remains linear for SIC to allow for aperture-level in-band full-duplex operation. The measured ACPR frequency spectrum of the receive path with a 100 MHz signal across input power is shown in Fig. 6.22. As shown previously, ACPR shows a significant increase from an input power of −10 dBm to 0 dBm of input power.

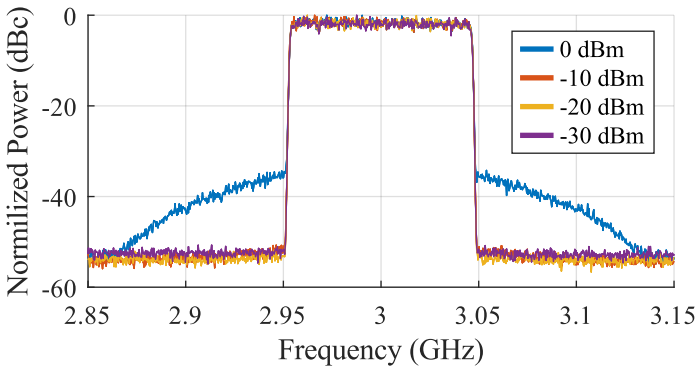


Figure 6.22: Measured ACPR frequency spectrum of receive path 100 MHz signal.

6.4 Transmit Observation - Variable Attenuator

For power level conditioning, the transmit observation path incorporates an updated version of the variable attenuator presented in Chapter. 3 and [66]. Fig. 6.23 shows the variable attenuator highlighted at the bottom of the MMIC layout. Using the same attenuation bits of 5 dB, 10 dB, and 20/40 dB, the transmit observation power level can be adjusted in 5 dB steps. The updated variable attenuator uses an additional 2 shunt $3 \times 150\,\mu$m devices for the 40 dB of attenuation while maintaining an area of 2 mm $\times$ 0.8 mm. For ease of bonding and packaging, air-bridges are used to bring bias pads to the edge of the MMIC.

With a desired transmit observation power level of 0 dBm or less the variable attenuator is used to reduce the sampled power to the desired level. With an input power of 46 dBm Fig. 6.24 shows the simulated transmit output power (P_{TX}) in red and the transmit observation (P_{TXO}) in blue. The block diagram in the figure depicts the T/R switching network bias for transmit and transmit observation operations. As discussed previously, the loss in the transmit path is less than 1 dB shown with the red trace just above 45 dBm of output power. Using the C_{off} coupling, discussed previously, the sample transmit power level is reduced by more than 20 dB before the

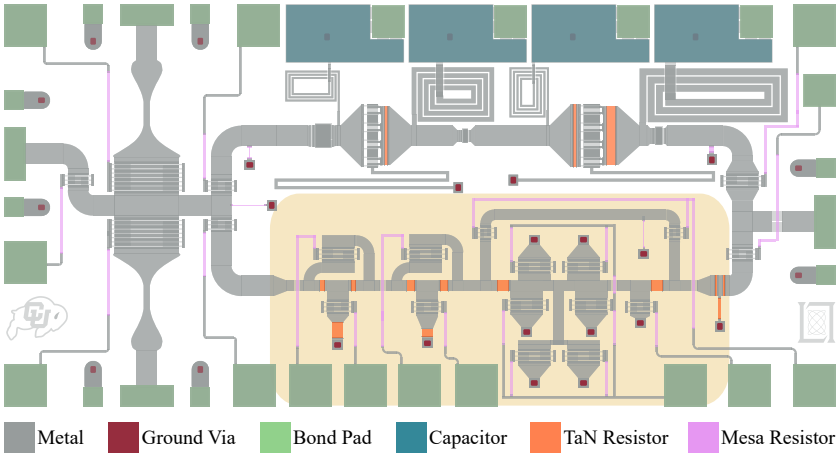


Figure 6.23: Layout of MMIC with highlighted transmit observation path variable attenuator. The variable attenuator is an updated version of the variable attenuator presented in chap. 3 with the same attenuation bit level.

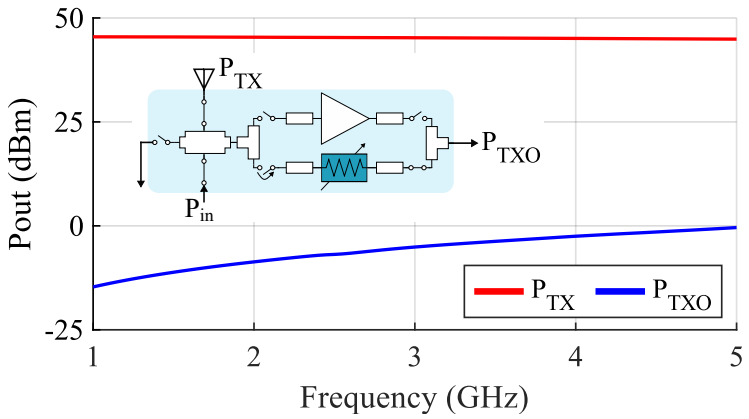


Figure 6.24: Simulated transmit and transmit observation path with an input transmit signal of 46 dBm. The variable attenuator is set to 20 dB of attenuation for a desired transmit observation power level of 0 dbm. The transmit and transmit observation operation of the MMIC is shown in the block diagram.

variable attenuator. To reduce the transmit observation power level to the desired 0 dBm or lower level, the variable attenuator is set to 20 dB of attenuation. With this configuration simulated transmit observation power level remains below 0 dBm.

The measured transmit observation path for each attenuation state using the evaluation board is shown in Fig. 6.25. Due to the LNA in a parallel path to the variable attenuator, the leakage through the OFF LNA limits the max attenuation of the variable attenuator. During transmission, the LNA is biased OFF, which can be done with 0 V on both the gate and drain or with the drain current pinched off using −5 V on the gate while the drain voltage remains at 30 V. Fig. 6.25a shows each step with an LNA bias of 0 V on the gate and drain, while Fig. 6.25b shows the steps with a gate bias of −5 V and a drain voltage of 30 V. Seen with both LNA OFF biases, the transmit observation level is limited to about -60 dB between 4 and 5 GHz. Below −60 dB the transmit observation signal begins the have higher variation across frequency due to the leakage through the LNA, which changes based on bias. For a desired transmit observation power level of 0 dBm and a transmit signal greater than 0 dB, the transmit observation signal needs to be able to match its reduction with the transmit power level. The transmit power reduction can be matched up to a

transmit signal power level of 55dBm seen in Fig. 6.25.

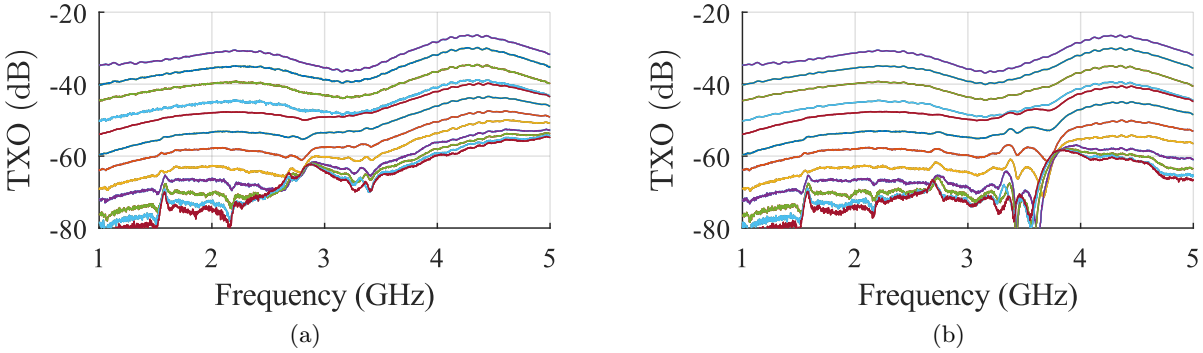


Figure 6.25: Measured transmit observation path with an OFF LNA bias of (a) $V_g = V_d = 0\,V$ and (b) V_g = -5 V and $V_d = 30\,V$. Showing the bottom attenuation levels is limited by the leakage through the LNA path.

6.5 Chapter Summary

This chapter presents a GaN MMIC packaged and PCB level integrated for an aperture-level in-band full-duplex system utilizing digital self-interference cancellation enabled by transmit signal observation. Enabling sampling of the transmit signal at the antenna level allows for the noise and nonlinearities generated in the transmit chain to be accurately represented during digital self-interference cancellation.

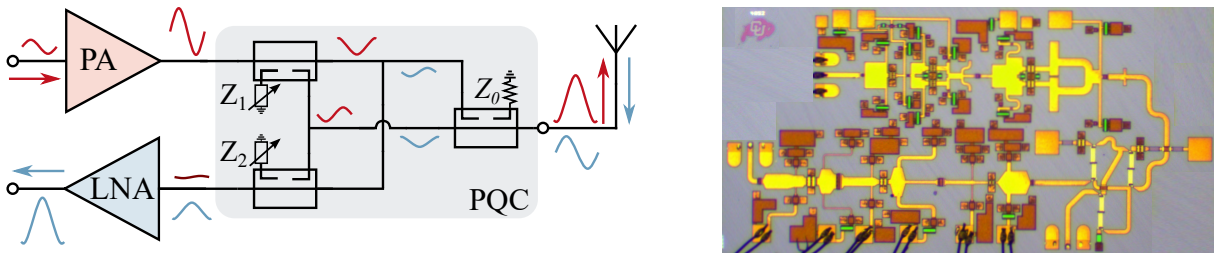
The designed MMIC demonstrates a co-designed low noise amplifier, variable attenuator, and T/R switching network. The MMIC enables re-configurable transmit and receive antenna elements in addition to a completely transmit or receive half-duplex array. The high power LNA allows for a robust receive path to handle the coupled transmit signal during full-duplex operation, while the variable attenuator, published in [54], allows for power level conditioning of the transmit observation signal.

Chapter 7

Element-Level Full-Duplex Front-End

7.1 Introduction

As frequency increases, the size of a unit element of an active antenna array decreases faster than the circuit size, and interconnects become increasingly lossy. Using a single chip integrated front-end as shown in [86] [87] at 6 and 34 GHz, and [88] [89] [90] [91] above 70 GHz, instead of multiple chips, helps with overall array integration. This is especially the case for monostatic in-band full-duplex (IBFD) systems, in which the power amplifier (PA) and low noise amplifier (LNA) share a single antenna. Integrating a passive quasi-circulator (PQC) in the front-end, as shown in Fig. 7.1a, further improves functionality without adding substantial volume to the unit element. A photo of the integrated front-end MMIC can be seen in Fig. 7.1b. In this approach, the output of the power amplifier is transmitted through the passive quasi-circulator, with some associated loss,



(a) (b)

Figure 7.1: (a) Block diagram of IBFD 3-port front-end. The passive quasi-circulator (PQC) network suppresses leakage from the PA to the LNA by more than 30 dB. All three components are integrated on the same GaN MMIC covering 75–100 GHz for an isolation better than 30 dB and return loss better than 10 dB. (b) Photo of the 4 × 2 mm^2 GaN MMIC die.

but isolated from the receive path low noise amplifier. The isolation is accomplished by appropriate phasing in the Tx and Rx paths.

Other approaches for in-band full-duplex front-end modules with a shared antenna element requiring Tx-Rx isolation include commonly use ferrite circulators [92] [93] [94] [95], which require bulky external magnets and are not monolithically integrated. Alternatively, active circulators [96] [96] [22] and quasi-circulators [97] [75] can be implemented on chip, using non-reciprocity of transistors to enable circulation and isolation with gain, e.g. 2.4 dB in [22]. Integrated switch-based circulators, using switched gyrator networks, have been demonstrated in [98] and [99]. These networks can be integrated on chip, using time-controlled transistor switch devices in the signal path, enabling circulator-like performance limited by switch insertion loss, isolation and response time. Another approach for IBFD isolation are balanced duplexers demonstrated in [100] [101] [102], which incorporate a single coupler with one tunable load. For more precise impedance tuning, [102] incorporates an electromechanical impedance tuner for measurements on the balanced duplexer, demonstrating an isolation greater than 40 dB at 1.9 GHz. The approach from Fig. 7.1a, taken here, incorporates multiple couplers with two tunable loads, enabling more control over a wider bandwidth.

The quasi-circulator demonstrated in this chapter is a passive device amenable to monolithic integration over a wide bandwidth. We show that the TX path does not have power limitations if active tunable devices are implemented at the isolated port of the Lange couplers and not in the signal path. The device does not consume dc power and is tunable. To demonstrate this functionality, the passive quasi-circulator (PQC) is integrated in a single MMIC with a PA and LNA for an in-band full-duplex front-end. The results in this chapter expand on the research presented at the IEEE International Microwave Symposium 2024, Washington DC [66]. The extension includes additional simulations and explanation of tunability, tunable load power handling capabilities, and small-signal measurements expanded to 50 GHz on the lower end of the band for the PQC and integrated front-end. Additionally, large-signal measurements are performed with the separate passive quasi-circulator to validate that compression in the transmit path is not an

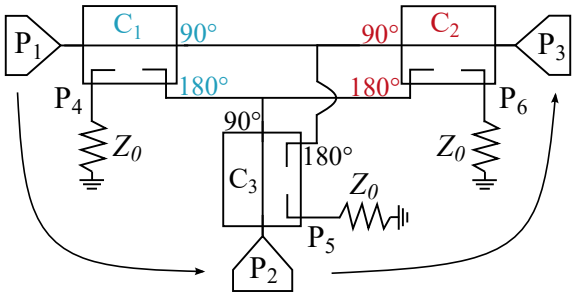


Figure 7.2: Passive Quasi Circulator (PQC) schematic showing the direction of circulation. The phases of the coupler outputs are indicated to show how they produce isolation.

issue. Furthermore, measurements of the noise figure in the receive path are performed from 75 to 110 GHz and large-signal transmit/receive integrated front-end characterization is presented.

The chapter is organized as follows. Section II, details design and characterization of the tunable passive quasi-circulator is shown, with a comparison to previous published work. Section III briefly discusses PA and LNA design for completeness, while Section IV gives final results of the transmit and receive behavior of the integrated front-end MMIC.

7.2 Passive Quasi-Circulator

The components and full Tx/Rx chip are designed in the HRL T3 process, featuring 40 nm GaN transistors fabricated on a 50 μm thick SiC substrate. The HEMTs have a f_T/f_{max} = 200/400 GHz, a breakdown voltage greater than 50 V, and a power density of 1.5 W/mm [103] [104]. Transmission lines and air bridges use three metallization layers, with SiN capacitors and TaN or MESA resistors. The design of the PQC is presented next, followed by the experimental characterization of the fabricated MMIC. We note that the HRL T3 process has recently been expanded into T3L and T3.5 with improved power density and PAE at W-band [105].

7.2.1 Passive Quasi-Circulator Design

A schematic of the passive quasi-circulator (PQC) consisting of three 90° hybrids is shown in Fig. 7.2. The ideal phase of the *through* and *coupled* paths, referenced to the import port, are shown for each coupler in blue, black, and red, respectively. The coupler connections create a 6-port

network, and assuming lossless couplers and 50 Ω transmission-line connections between them, the scattering matrix is given by

$$[S]_{6\times6} = j\frac{2}{3}\begin{bmatrix} 0 & 1 & 0 & -\frac{1}{2} & 0 & 1 \\ 1 & 0 & 1 & 0 & -\frac{1}{2} & 0 \\ 0 & 1 & 0 & 1 & 0 & -\frac{1}{2} \\ -\frac{1}{2} & 0 & 1 & 0 & 1 & 0 \\ 0 & -\frac{1}{2} & 0 & 1 & 0 & 1 \\ 1 & 0 & -\frac{1}{2} & 0 & 1 & 0 \end{bmatrix} \tag{7.1}$$

An input signal at P_1 is split evenly by coupler C_1, with a 90° phase between the *through* and *coupled* ports. Each signal is then split again at a T-junction, and recombined independently by couplers C_2 and C_3. Assuming 50 Ω lines, the 3-port T-junctions are not ideally matched to the couplers, and this results in waves reflected back to the isolated coupler ports. The *through* and *coupled* ports from coupler C_1 connect to the same ports of C_2. They combine destructively at P_3 and constructively at P_2. Due to signal splitting, a 3 dB loss occurs from P_1 to P_2. There is also constructive combining at P_6, which can be terminated. The network operates similarly when a signal is incident at P_2, thus a 3 dB loss is also experienced from P_2 to P_3.

Figure 7.1a illustrates the signals when this network is used in a transmit-receive front end, with relative amplitudes shown. For in-band full-duplex operation, only three of the ports are used for Tx, Ant, and Rx, respectively, while the remaining ports are terminated. With P_1, P_2 and P_3 corresponding to Tx, Ant, and Rx, and with remaining ports terminated, a 3-port PQC scattering matrix results:

$$[S_{PQC}] = j\frac{2}{3}\begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix} \tag{7.2}$$

having $|S_{31}| = 0$, infinite isolation from Tx to Rx. and insertion loss in transmit and receive paths $|S_{21}| = |S_{32}| = 2/3$ or -3.5 dB.

The PQC is implemented using Lange couplers with the layout and simulated performance

across V and W bands shown in Fig. 7.3, with the isolated port terminated in Z_0. The amplitude and phase imbalance is 2.5 dB and 5° from 50–110 GHz, while the isolation and match are better than 25 dB across the frequency range. The aspect ratio of the layout is convenient for placement in a MMIC, however the transmission-line and cross-over connections required for the PQC layout add loss and phase, changing the behavior relative to the ideal case.

Waves on the lines connecting the couplers cannot experience the same phase and amplitude differences without additional meandering of the transmission lines at the nodes between couplers. This is a challenge at W-band, where a 300 μm transmission line is approximately $\lambda/4$ long at 90 GHz in the T3 process. Fig. 7.4 shows the difference in amplitude and phase of the transmission lines connecting C_1 to C_2, indicated in the layout in Fig. 7.5a. For ideal cancellation, the difference in amplitude and phase would be zero. However, in the layout the transmission lines connecting the couplers differ in length. To accommodate for proper phasing with unequal routing distances, the length between C_1 and C_3 is approximately twice as long as the connections between C_2 and C_3, as displayed in Fig. 7.5a. The receive path connects to C_2 with a shorter path length, minimizing the impact on noise figure due to loss, while the transmit path connects to C_3. The bandwidth of the network is defined for the reflection coefficient at all ports lower than −10 dB and the Tx–Rx tunable isolation range greater than 30 dB. Fig. 7.5b shows the simulated small-signal performance with ideal Z_0 terminations on all isolated ports of the couplers, with the maximum simulated

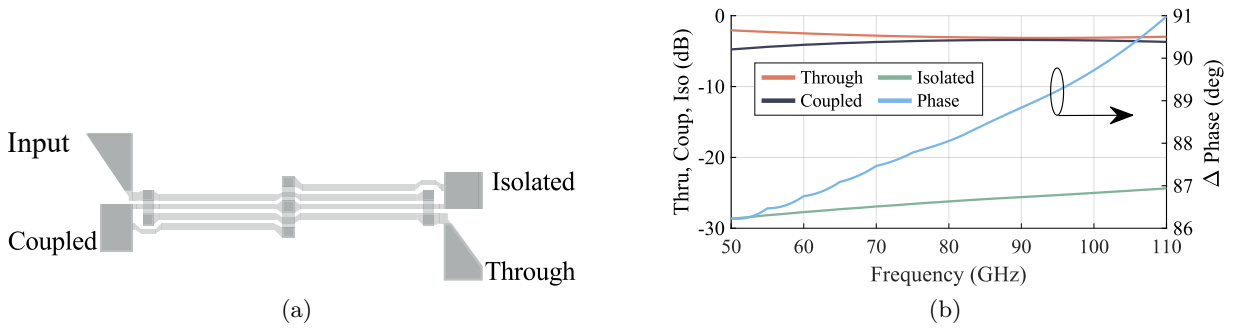


Figure 7.3: (a) Layout of 375 × 140 μm^2 Lange coupler. (b) Simulated performance of Lange coupler across frequency with a Z_0 termiantion at the coupled port.

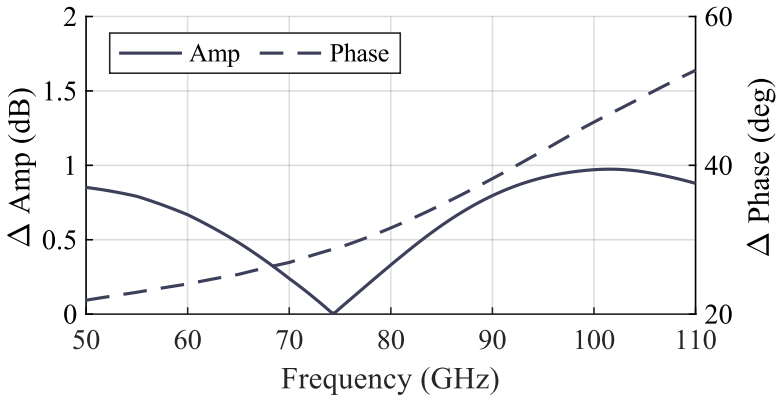


Figure 7.4: Simulated difference in amplitude (solid) and phase (dashed) of transmission lines connecting C_1 and C_2 in Fig. 7.5a.

isolation of 22 dB. For the simulated case with 50-Ω terminations, the isolation never reaches the desired level of 30 dB, motivating tunable loads added to the isolated ports of the couplers to compensate degradation in isolation.

Tunable impedance loads in the T3 process can be realized using nonlinear HEMT devices provided by the foundry. The device models are not extracted for these specific configurations at 0 V drain bias, but are useful for predicting trends in performance. Since the tunable impedances are connected to the isolated ports of the Lange couplers, the loss of the loads is not a significant consideration. Using source-grounded HEMT devices, Fig. 7.6 shows three possible configurations

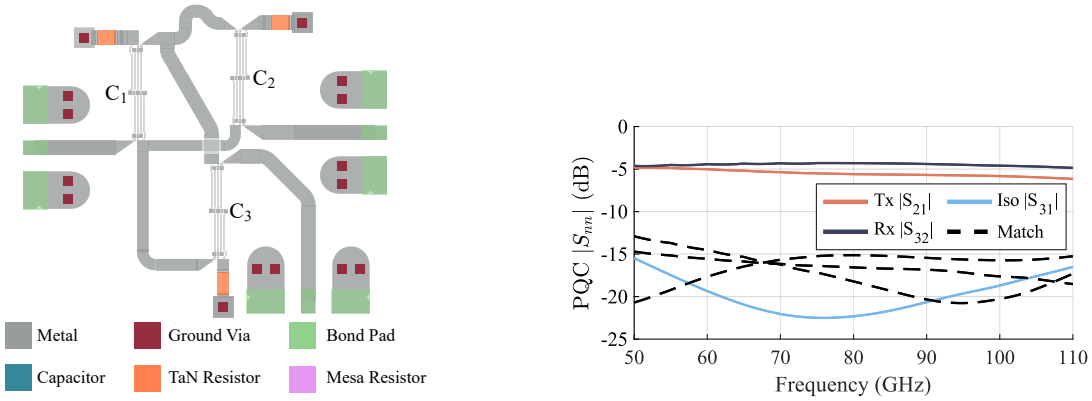


Figure 7.5: (a) Layout of 1.1 × 1 mm^2 Z_0 terminated PQC. (b) Simulated circulator performance of Z_0 terminated PQC.

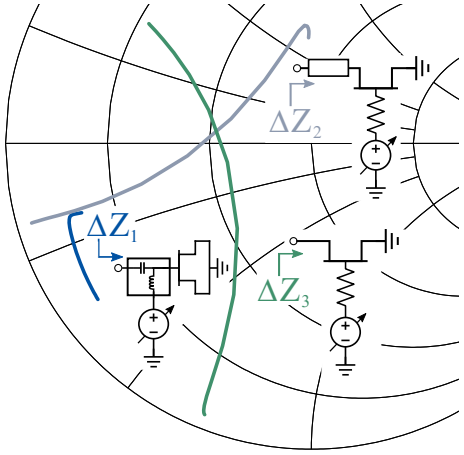


Figure 7.6: Simulated impedance for different HEMT tunable load configurations. It is seen that the ΔZ_3 configuration (green) has the largest tuning range in phase combined with the simplest implementation.

for implementing a tunable load, with port impedances ΔZ_1 (blue), ΔZ_2 (gray), and ΔZ_3 (green). The tunable impedance of each configuration is plotted for -1 V to 1 V bias sweep at 90 GHz, showing the total impedance range. Looking into the gate of the configuration ΔZ_1, simulated with an ideal bias tee, we observe the smallest impedance and the most complicated biasing structure. Both ΔZ_2 and ΔZ_3 are connected at the drain with a 100 μm transmission line added before the device in ΔZ_2, showing how the impedance of the device can be shifted. Both ΔZ_2 and ΔZ_3 have a much

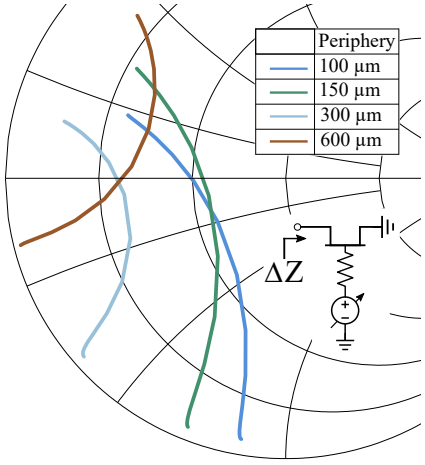


Figure 7.7: Simulated impedance range of tunable load for 100 μm, 150 μm, 300 μm and 600 μm device periphery for a -1 V to 1 V bias sweep. For the largest tuning range and nearest 50 Ω real impedance crossing, a 150 μm device size is chosen.

wider impedance range than ΔZ_1 along with a simpler biasing structure.

Comparing ΔZ_2 and ΔZ_3, and focusing on size and complexity in addition to impedance range, we note that both impedance traces cross the real axis, ΔZ_2 at $\approx 25\,\Omega$ and ΔZ_3 at $\approx 30\,\Omega$. Taking the bias extremes at $\pm 1\,V$, the impedance ranges become $\Delta Z_2 = 35+j39\,\Omega$ and $\Delta Z_3 = 12+j50\,\Omega$, with ΔZ_2 showing a larger amplitude difference and ΔZ_3 a larger phase difference. ΔZ_3 configuration is chosen for the tunable load for its smaller footprint and larger phase change. The variable load impedance is plotted for different device peripheries across bias in Fig. 7.7. The 150 μm periphery, realized with a $4 \times 37.5\,\mu$m device, is chosen for the tunable load because it has the largest impedance range.

For large input signals, the nonlinear device impedance changes, degrading the performance of the tunable load. Setting a threshold impedance change of 5Ω, the maximum power is determined. For the $4 \times 37.5\,\mu$m device, Fig. 7.8 shows the real and imaginary parts of the impedance at V_g = -1 V, 0 V, 0.2 V, and 1 V bias across input power. Shown with a light blue trace, the impedance at 0 V shows the lowest tolerance to input power: at 7 dBm the real part of the impedance changes by $5\,\Omega$. This bias point is the most sensitive, since the next $5\,\Omega$ change happens at 18 dBm (more than 10 times the power).

To compensate for degradation in isolation due to interconnecting line lengths and other non-idealities, the isolated ports of two of the couplers (C_1 and C_2) are terminated with tunable loads,

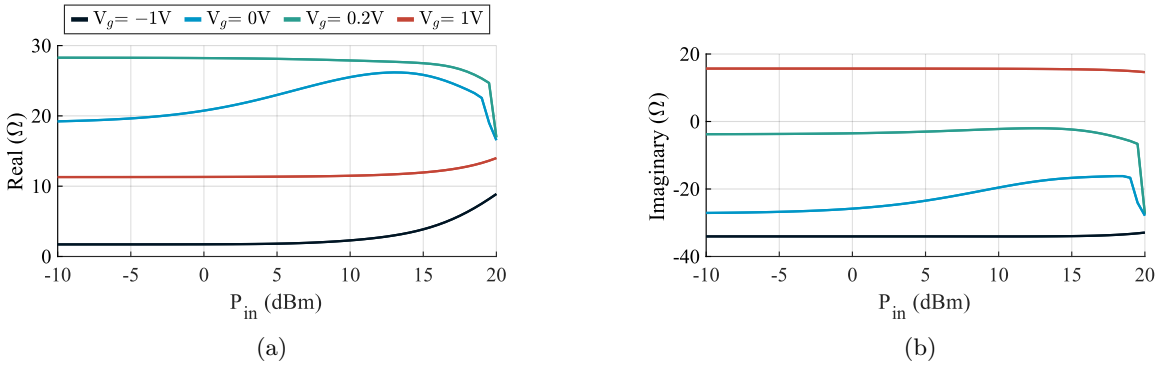


Figure 7.8: Simulated (a) real and (b) imaginary parts of the tunable load impedance of a $4 \times 37.5\,\mu$m (150 μm periphery) device across input power with V_g = -1 V, 0 V, 0.2 V, and 1 V.

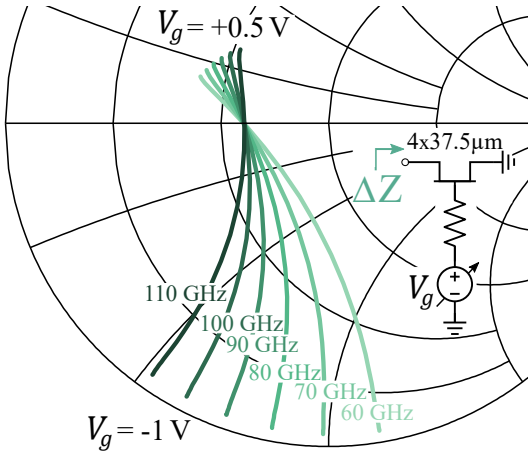


Figure 7.9: Simulated impedance variation across gate bias from −1 V to +0.5 V looking into the drain of a $4 \times 37.5\,\mu$m device from 60 to 110 GHz.

while the third coupler (C_3) isolated port is terminated in a 50 Ω resistor. This enables recovering isolation across frequency based on the tunable-load bias. A plot of the simulated tunable range from 60 to 110 GHz is displayed in Fig. 7.9. When the HEMT is pinched off, it appears purely capacitive. With the gate voltage at approximately +0.2 V, the impedance is purely real across frequency. At this bias point, the impedance is ≈ 30 Ω and is reasonably well matched to the 50 Ω coupler. Beyond this voltage, the HEMTs appear inductive.

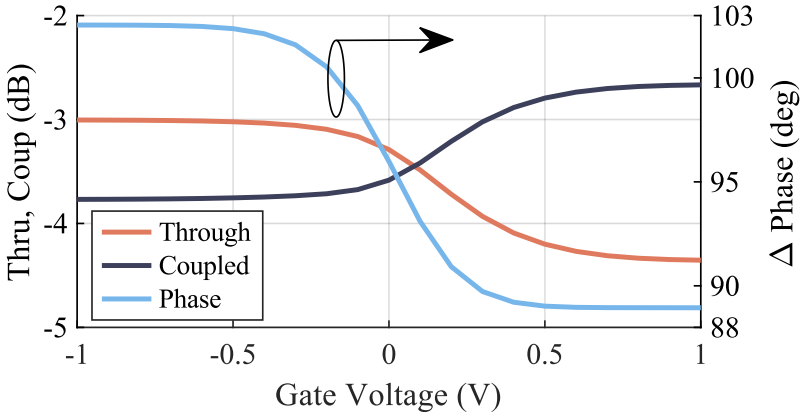


Figure 7.10: Simulated performance of Lange coupler with tunable impedance connected at the isolated port at 91.5 GHz vs. bias voltage of tunable load. The *through* and *coupled* traces show the transmission coefficient. The phase trace is the relative phase difference between the two ports. Note the significant change of all parameters for a control voltage of −0.5 V and +0.5 V.

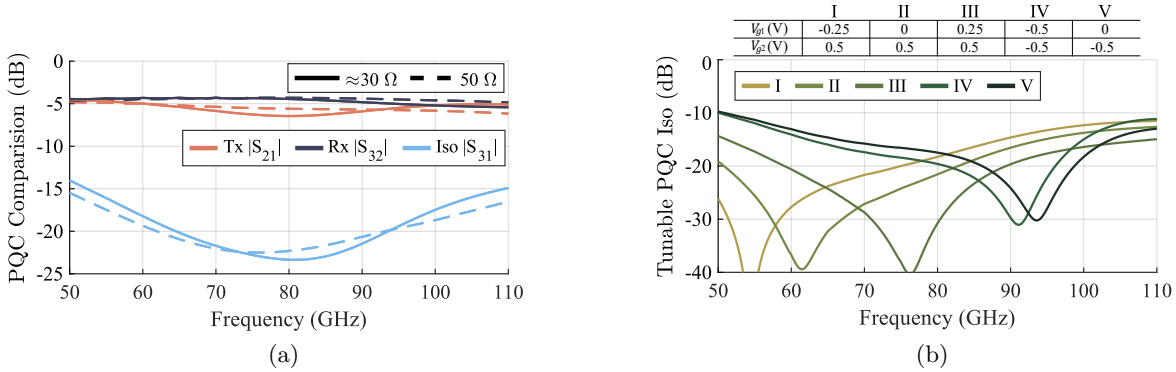


Figure 7.11: (a) Simulated performance comparison of passive quasi-circulator with implemented tunable loads (solid) and 50-Ω terminated (dashed) passive quasi-circulator. The tunable loads are biased at 0.2 V for ≈30 Ω impedance presentation. (b) Simulated passive quasi-circulator isolation using the implemented tunable loads.

With tunable loads added to the isolated port of the couplers, the coupling coefficent and the phase differences vary across bias. This can be seen in Fig. 7.10, which shows the simulated performance of the coupler at 91.5 GHz while the bias of the tunable load is varied form -1 V to +1 V. The amplitude for both the through and coupled path vary more than 1 dB while there is 13.5 ° change in phase. The most significant change in amplitude and phase happen from -0.5 V to +0.5 V, which is used as the bias range during measurement.

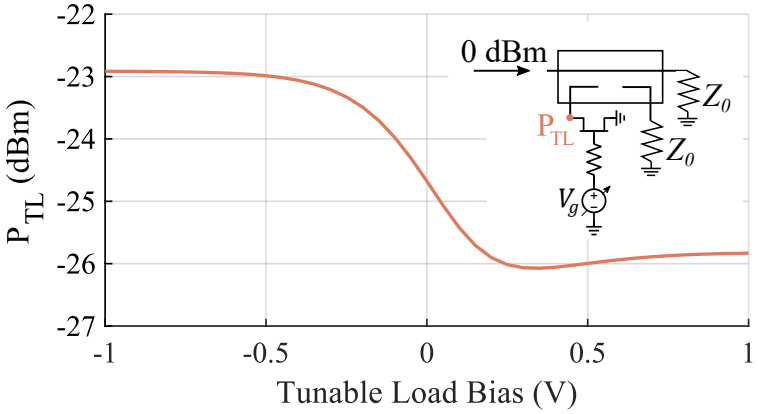


Figure 7.12: Simulated power through the Lange coupler to the isolated port at the tunable load input (P_{TL}) across bias with a 0 dBm input power at 90 GHz. The tunable load power handling requirement is reduced with increased isolation of the Lange coupler.

Figure 7.11a shows a comparison between the 50-Ω terminated PQC from Fig. 7.5 (dashed lines) and the PQC with tunable load terminations (solid lines) from 50 to 110 GHz. The plot shows a slight degradation in both Tx and Rx with an improvement in isolation around 80 GHz. Using the implemented tunable loads, Fig. 7.11b demonstrates multiple PQC isolation levels greater then 30 dB across frequency, a significant improvement over the 50-Ω case. Consistent with Fig. 7.10, the tunable load bias ranges from -0.5 V to +0.5 V, where the most significant tunability occurs.

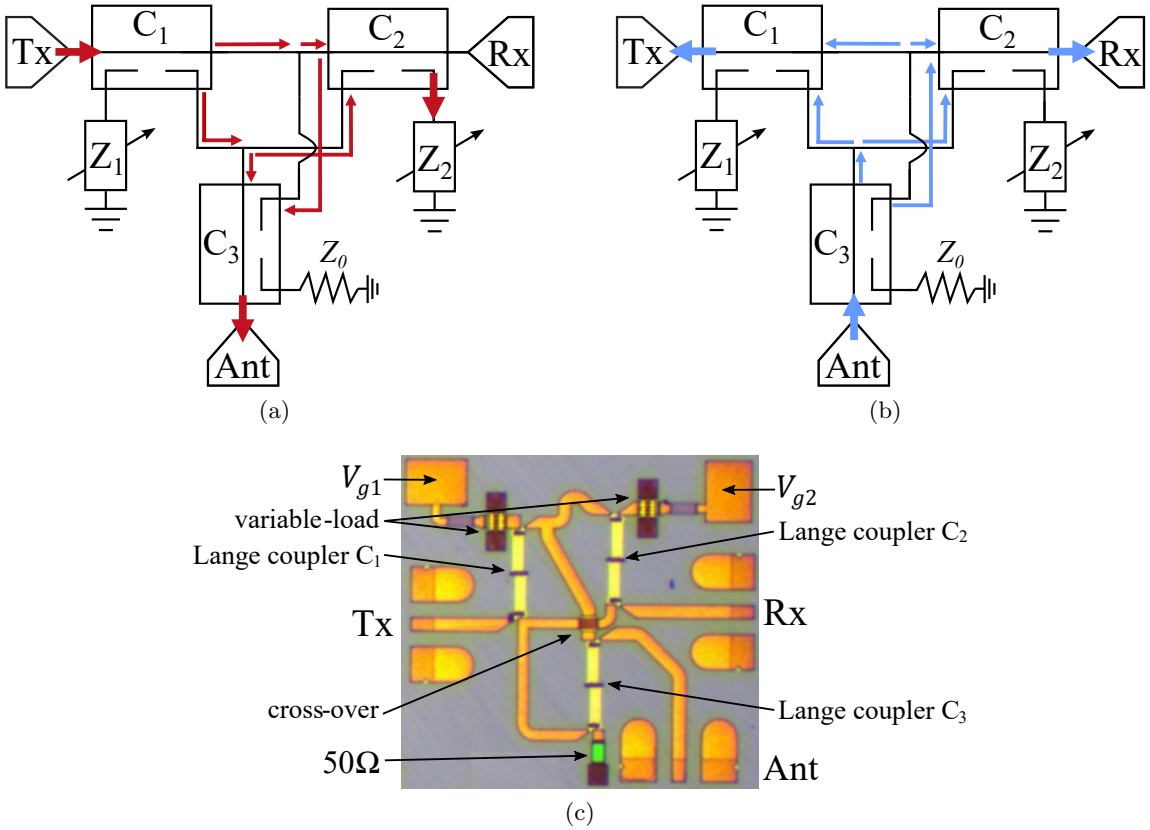


Figure 7.13: Tunable passive quasi-circulator (PQC) schematic for (a) Tx and (b) Rx signal paths, with inherent 3 dB loss in both paths. (c) Photograph of GaN MMIC PQC with a size of 1.1 × 1.1 mm^2, including RF and dc pads. The GSG pads at the RF ports have a 100 μm pitch.

For large input signals, the power at the tunable loads compared to the input signal is reduced as the Lange coupler isolation is increased. Fig. 7.12 shows the power seen by the tunable load through the Lange coupler to the isolated port (P_{TL}) across bias at 90 GHz. From Fig. 7.8 and Fig. 7.12 the simulated maximum allowable input power of the PQC can be determined. Using

a 0 V tunable load bias, which has the lowest power handling (Fig. 7.8), the input power to the device should remain below 7 dBm. From Fig. 7.12, with a 0 V tunable load bias the device sees about 25 dB less power than the input signal to the Lange coupler, implying that the PQC has a simulated maximum input power of 32 dBm.

The implemented tunable passive quasi-circulator schematic with the Tx (red) and Rx (blue) signal paths are shown in Fig. 7.13a and Fig. 7.13b, respectively. The two active devices in the network are only used for impedance tuning and are not in the signal path, they are in reverse bias and do not draw current, therefore we consider this network to be passive. The labeled layout of the tunable passive quasi-circulator MMIC is shown in Fig. 7.13c with a size of $1.1 \times 1.1\,\mathrm{mm}^2$.

7.2.2 Passive Quasi-Circulator Measurements

The measured small-signal isolation of the PQC is shown in Fig. 7.14 for a range of control voltages given in Table 7.1. The simulated performance of the PQC network is plotted for the voltages on both tunable load device gates of 0 V, shown with a dashed red trace. This simulation is comparable to the measured trace IV, shown with a solid red line. Simulation and measurement show a similar trend but clearly differ in isolation level, a result of the foundry HEMT devices lacking a validated 0 V drain bias model. From Fig. 7.14, it is seen that a notch below -30 dB is tunable within the operating frequency of the front-end for all measured control voltages. The interference cancellation is below 12.5 dB for the rest of the band. Gate voltages between 0 and 0.5 V are applied to move the notch within the frequency range. The notch center frequencies and bandwidths for each control voltage combination are given in Table 7.1, demonstrating the upper and lower frequency range of tunable isolation with the implemented tunable loads.

The transmission between Tx-Ant and Ant-Rx ports is plotted in Fig. 7.15, where Tx-Ant is shown in gray and Ant-Tx shown in orange. The shaded regions represent the range across bias when the voltages applied to the two gate pads are varied ± 0.5 V to give the extremes of coupler tunability (Fig. 7.10). To demonstrate the range of $|S_{21}|$, Fig. 7.15 plots the maximum and minimum transmission coefficient magnitude for any bias at a given frequency point. Simulation

Table 7.1: Tunable load bias for an isolation notch $< 30\,\mathbf{dB}$

Trace	I	II	III	IV	V
V_{g1} (V)	0.25	0.5	0.5	0	0.4
V_{g2} (V)	0.5	0.25	0.15	0	0
Notch (GHz)	72 - 74	78 - 80	84 - 88	89 - 93	95 - 100

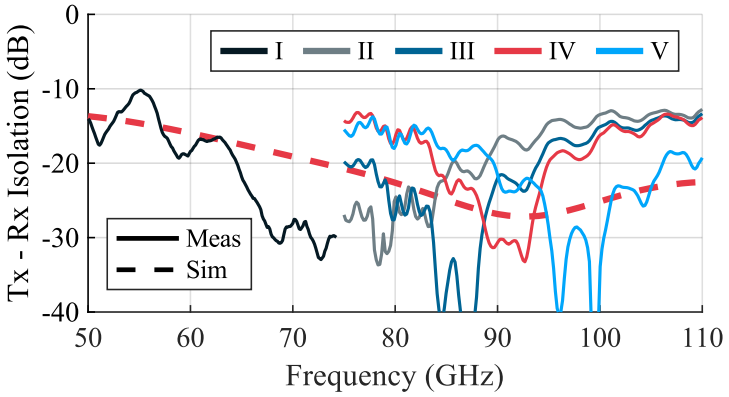


Figure 7.14: Measured (solid) and simulated (dashed) Tx-Rx isolation notch of tunable PQC. In the simulation, the control voltage is held at 0 V. For the measurements, cases I–V correspond to control voltages from Table 7.1.

of $|S_{21}|$, shown with dashed traces, are done with a 0 V bias on both tunable loads. As predicted by simulation, the transmit path experiences the largest loss. A maximum insertion loss difference is measured between the two paths at 86 GHz, while they cross at 63 GHz when $|S_{21}| = -4.4$ dB. Simulations agree well with measurements above 90 GHz. Below this frequency, the simulated and measured transmission coefficients differ by as much as 3 dB, although the trends are predicted. Again, we attribute the differences between simulations and measurements to the HEMT model which does not accurately represent the tunable loads.

The return loss at the antenna (Ant) port is plotted in Fig. 7.16. For in-band full-duplex systems, return loss at the antenna can have a significant impact on performance. Namely, the transmit (Tx) signal can be reflected at the antenna port and then fed into the receive (Rx) chain, lowering Tx-Rx isolation. Since refections internal to the chip cannot be measured, the antenna port match can be quantified from the refection coefficient at Port 3 when a 50 Ω antenna is attached

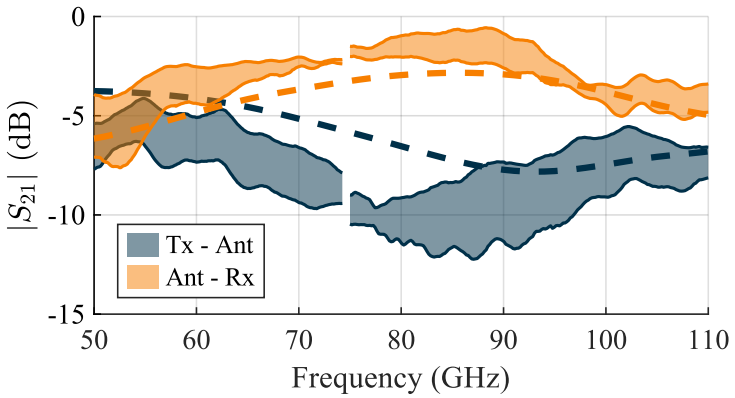


Figure 7.15: Measured (solid) and simulated (dashed) characterization of PQC network. $|S_{21}|$ between Tx-Ant and Ant-Rx. The shaded region shows measurements when the gate control voltage is varied from ±0.5 V for both paths, showing the extreme values in solid line. In the simulations, the control voltage is held at 0 V.

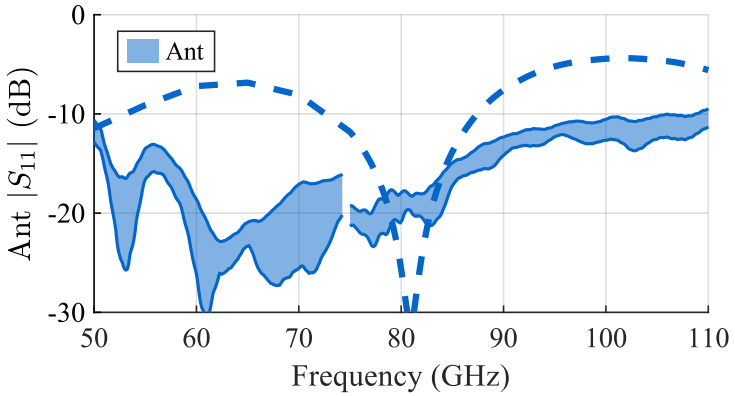


Figure 7.16: Measured (solid) and simulated (dashed) match of tunable passive quasi-circulator at the antenna (ANT) port. The shaded region shows the measurement over a range of control voltages.

to the port. Again, the measurement is done with the tunable load bias swept ±0.5 V for the most significant performance variation. The measurements show a return loss better than 10 dB at the antenna from 50 to 100 GHz across tunable load bias, which is shown as the shaded region in blue. Simulated performance with 0 V bias on both tunable loads is shown with a dashed line, having a narrowband return loss better than 25 dB at 80 GHz.

The reflection coefficients at the Tx and Rx ports are shown in Fig. 7.17, with the same tunable load bias sweep as in previous measurements. From 75 to 100 GHz, the return loss is better

than 10 dB for all tunable load impedances, defining the bandwidth of the passive quasi-circulator. This is seen by the shaded region in gray (Tx) and orange (Rx). As expected, the return loss for both of these ports varies more with tunable load bias, due to the mismatched isolated port of the couplers.

For demonstration of the passive quasi-circulator power handling, the transmitted power between the Tx and Ant ports is measured with an input power swept from 14 to 24 dBm at the Tx port, with the upper end limited by our driver amplifiers in W band. For on-wafer measurements, the tunable loads are wire-bonded to ground for a bias of 0 V, reducing the number of required probes in the on-wafer measurements. The tunable loads are the only active devices in the PQC, potentially limiting the power handling, and a 0 V bias presents the most conservative condition. Measurements are done in 1 GHz steps from 92 to 96 GHz, with results shown in Fig. 7.18 along with the simulated power handling of the PQC at 94 GHz. The measurements show no compression of the passive quasi-circulator up to the available input power of 24 dBm while simulations show compression slightly bellow 24 dBm.

The frequency of operation for the PQC, 75 to 100 GHz, is defined by a tunable SIC better than 30 dB and a return loss better than 10 dB at all ports. Across the frequency of operation, the insertion loss is averaged for both Tx and Rx to determine the loss of the PQC. Table 7.2

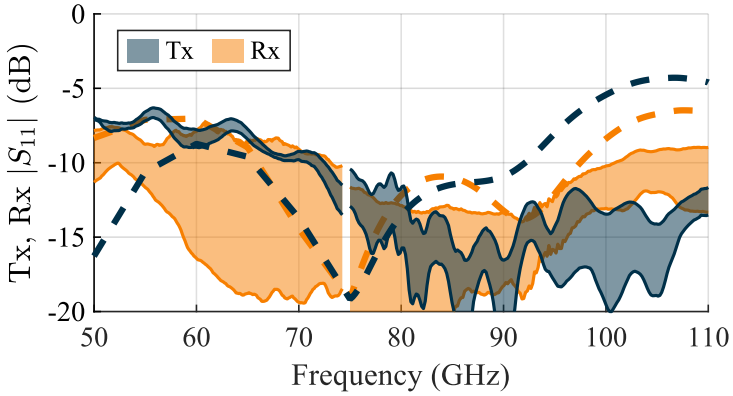


Figure 7.17: Measured (solid) and simulated (dashed) match of tunable passive quasi-circulator at the transmit (Tx) and recieve (Rx) ports. The shaded region shows the measurement over a range of control voltages.

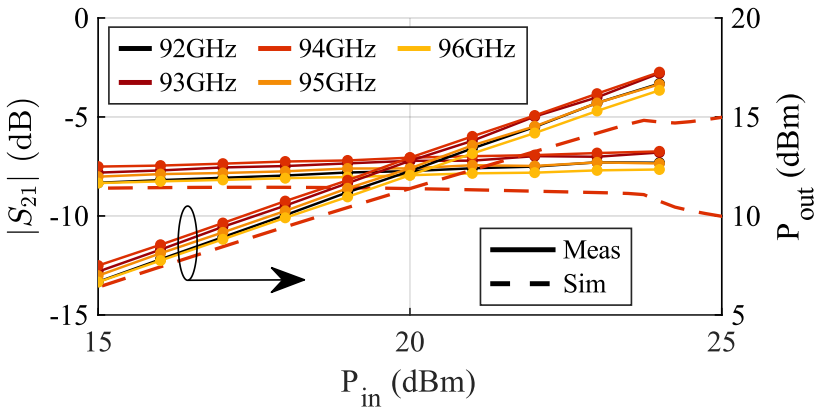


Figure 7.18: Measured (solid) and simulated (dashed) large signal power sweep of passive quasi-circulator transmit path across frequency, with 0 V on tunable load bias. The Rx port is terminated in a matched load.

Table 7.2: Tunable Passive Quasi-Circulator Comparison Table

Reference	Technology	Frequency (GHz)	Insertion Loss (dB)	Isolation (dB)	DC Power (W)	P1dB (dBm)	Area (mm^2)
[93]	Ferrite	55 - 66	1	15	0	54	11
[106]	GaN	50 - 100	6.3	20	1.5	16	4.5
[97]	GaAs	10 - 12	4.5	35	0	35	8
[75]	SiGe	76 - 80	1	16	0.06	1	0.07
[98]	CMOS	0.9 - 1	2.5	30	0.17	30.5	16
[100]	PCB	2.5 - 2.8	3/4	25	0	-	-
This Work	GaN	75-100	9.5 Tx / 2.5 Rx	> 30	0	> 24	1.1

compares the performance of the passive quasi-circulator to other circulator-like networks, showing high frequency of operation, no dc power consumption and high isolation, at the expense of insertion loss in Tx.

7.3 Integrated Full-Duplex Front-End

The passive quasi-circulator is combined into a single-chip transceiver MMIC as a proof of concept integrated analog front-end. A three-stage power amplifier (PA) is integrated with a three-stage low noise amplifier (LNA) and a tunable PQC that enables shared antenna in-band full-duplex operation. The layout of the full, $4 \times 2\,mm^2$ chip, is given in Fig. 7.19. The three-stage PA is at the top, with the input denoted by Tx, and was separately characterized with results given in [47].

This reactively-combined PA has over 12 dB of simulated gain from 75 to 110 GHz, and 27 dBm of output power at an input power of 15 dBm. The PA output is fed to the PQC network, shown at the bottom right. The second port of the PQC is connected to the antenna GSG probe (Ant). The third port of the PQC network is connected to a three-stage LNA with a 50-Ω microstrip line. A photograph of the fabricated MMIC is shown in Fig. 7.1b. A 50-Ω load GSG resistor is included in the layout close to the Tx and Rx GSG pads and bonded when needed so that the ports can be terminated without an additional probe. The resistors are not shown in the MMIC photograph (Fig. 7.1b) or layout (Fig. 7.19) for clarity.

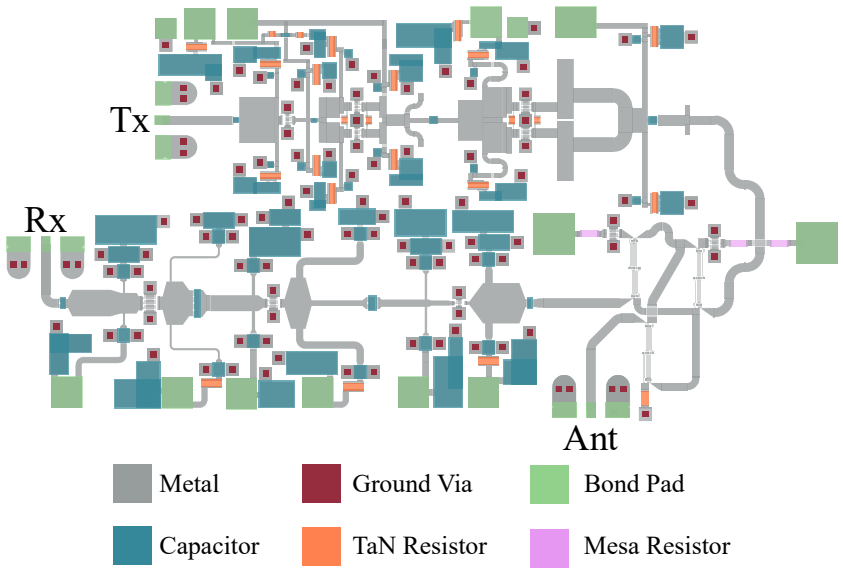


Figure 7.19: Layout of the $4 \times 2\,\mathrm{mm}^2$ integrated full-duplex front-end GaN MMIC. A three-stage PA is on the top, while the LNA is on the bottom and the PQC network is between the output of the PA and the antenna port, with the third port connected to the LNA input.

Due to the full-duplex implementation, the peak PA output power and minimum isolation are of concern when considering linearity of the LNA. Compression of the LNA degrades the linearity and limits effectiveness of additional self-interference cancellation later in the receive chain. A high compression level is a benefit of GaN LNAs [107], further making full Tx-Rx integration advantageous.

The 75-100 GHz LNA has three-stages for sufficient receiver gain when the approximately 3 dB

loss of the PQC network is included. While the decrease in gain can be overcome by additional gain stages, the noise figure (NF) suffers. Placing an emphasis on NF, the smallest device with a validated model of $2 \times 25\,\mu$m, giving the lowest NF of 2.1 to 2.7 dB from 75 to 100 GHz, is chosen for the first LNA stage. In stages two and three, the next largest validated devices of $4 \times 37.5\,\mu$m and $6 \times 50\,\mu$m are used, with a NF of 2.5 and 2.7 dB at 90 GHz. For stability, large shunt capacitors on the bias line in addition to low a resistance are added, reducing gain at lower frequencies. Bias lines of each stage are separated for individual control of drain current for each stage if desired. The LNA has a simulated gain of 15.5 dB to 16.5 dB, a noise figure ranging from 3.5 dB to 3.9 dB from 75 to 100 GHz, and a P1dB of 1 dBm at 91 GHz.

7.4 Measured Full-Duplex Front-End

The front end is mounted on a gold-plated copper molybdenum (CuMo) carrier, and the dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for stability. The circuit is measured on a Summit 9000 probe station with 100-μm pitch GSG probes and characterized in small-signal operation from 50 GHz to 75 GHz, then 75 GHz to 110 GHz using an HP8510C Vector Network Analyzer with V- and W-band extender heads, respectively. Network calibration for V- and W-band were done separately with on wafer SOLT calibrations. The integrated front end is next measured in transmit and receive modes with the unused path unbiased and terminated with an on-chip load. A resistor is included in the layout close to the GSG pad and bonded when needed to the microstrip. The resistors are not shown in the layout for clarity. The bias on both tunable loads of the passive quasi-circulator is set to 0 V for both transmit and receive measurements. The operational bandwidth of the full-duplex front-end is determined by the a return loss better than 5 dB and a 3 dB drop from the maximum gain.

7.4.1 Transmit Path Performance

The small-signal measured (solid) and simulated (dashed) transmit path parameters are displayed in Fig. 7.20. The measurements are carried out with the gate and drain bias of the PA tied

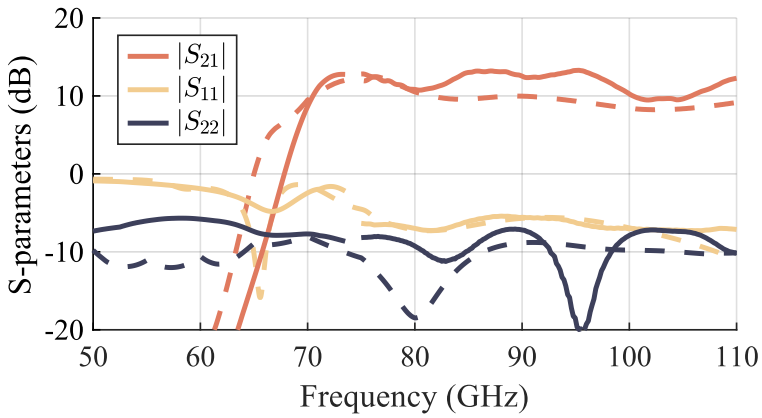


Figure 7.20: Measured (solid) and simulated (dashed) small-signal characterization of front-end transmit path. Port 1 is the input of the PA (Tx), and port 2 is at the antenna port (Ant) or output of the PQC. Measurements and simulations are shown for 0 V bias on both tunable loads.

together using off-chip capacitors, at a drain voltage of 12 V and a total drain current of 100 mA. The measured small-signal gain from 70 to 100 GHz ranges from 10.5 to 13.5 dB, which is up to 5 dB higher than simulation at 95 GHz. Note that we observe an increase in gain at the higher end of the band at 110 GHz. The measured return loss is better than 5 dB above 75 GHz.

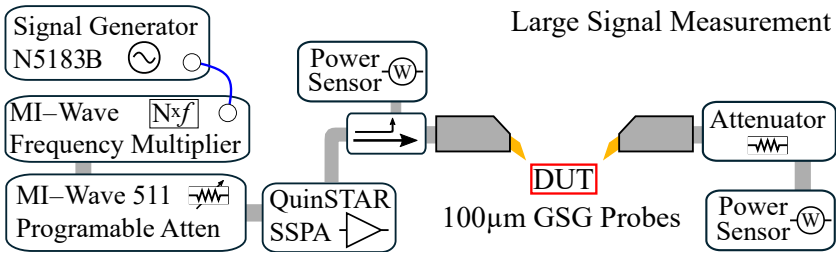


Figure 7.21: Block diagram of the large-signal measurement setup.

The 92-96 GHz large-signal setup is shown in Fig. 7.21. The measurements are conducted using a Keysight N5183B signal generator with a MI-Wave frequency multiplier and a MI-Wave 511 programmable attenuator, amplified by a QuinSTAR SSPA. The output of the SSPA is connected to a WR-10 waveguide bidirectional coupler that measures the incident wave with a WR-10 power sensor. Following this are WR-10 waveguide GGB GSG RF probes connected to the device under test (DUT). The output signal is then fed into an attenuator and a WR-10 power sensor.

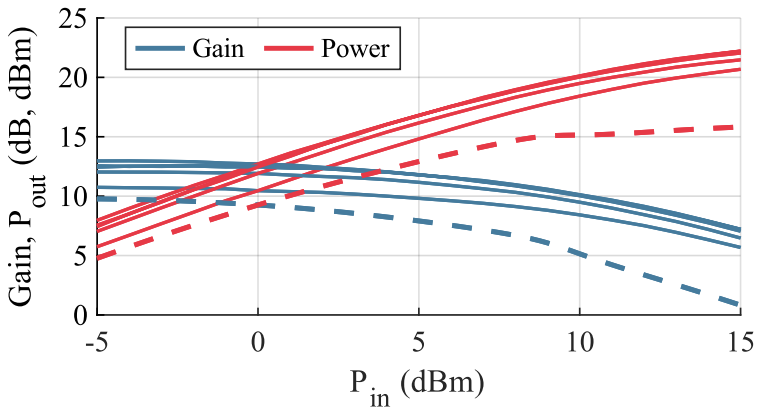


Figure 7.22: Measured (solid) and simulated (dashed) large signal characterization of transmit path. Measurements are shown from 92 to 96 GHz in 1 GHz steps and simulations are shown for 94 GHz. The measurements and simulations correspond to 0 V bias on both tunable loads.

Large signal measurements and simulations of the transmit path are shown in Fig. 7.22. The measurement is performed with an input power of −5 to +15 dBm across 92 to 96 GHz in steps of 1 GHz, shown in solid line, while simulations are done at 94 GHz (dashed). The measured gain and output power are higher than simulation, as expected from small-signal measurements in Fig. 7.20 which are larger than simulated ones from 92 to 96 GHz. With an input power of 15 dBm the transmit path demonstrates an output power of 22 dBm and a gain of 7 dB at 96 GHz.

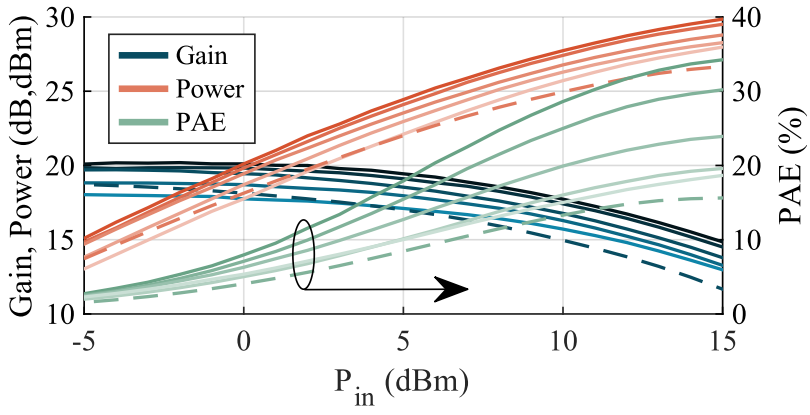


Figure 7.23: Measured (solid) de-embedded PA from 92 to 96 GHz in 1 GHz steps from light to dark coloring and simulated (dashed) PA at 94 GHz. The PA is de-embedded with the large signal $|S_{21}|$ measured data in Fig. 7.18.

Taking into account the PQC loss in the transmit path (Fig. 7.18), the de-embedded measured (solid) large signal performance of the PA is shown in Fig. 7.23. The PA demonstrates a maximum output power of 30 dBm, remaining below the allowable input power to the PQC, and a peak PAE of 35 % at 96 GHz. We note that the simulated standalone PA performance, shown at 94 GHz in dashed line, is consistently lower across frequency than the measured performance. The small-signal measurements were done at two independent facilities with excellent agreement. We attribute the improved measured performance to process improvements [105].

7.4.2 Receive Path Performance

The measured performance in receive mode is seen in Fig. 7.24. Both simulations and measurements are performed with gate and drain biases tied together, at a drain voltage of 12 V and a combined drain current of 95 mA. The measurements show a small-signal receive gain of 17 to 14 dB and input and output return losses better than 5 dB from 75 to 100 GHz. Based on the transmit and receive small signal measurements, the full-duplex single-chip analog front-end demonstrates a 25 GHz or 28.6% bandwidth from 75 to 100 GHz.

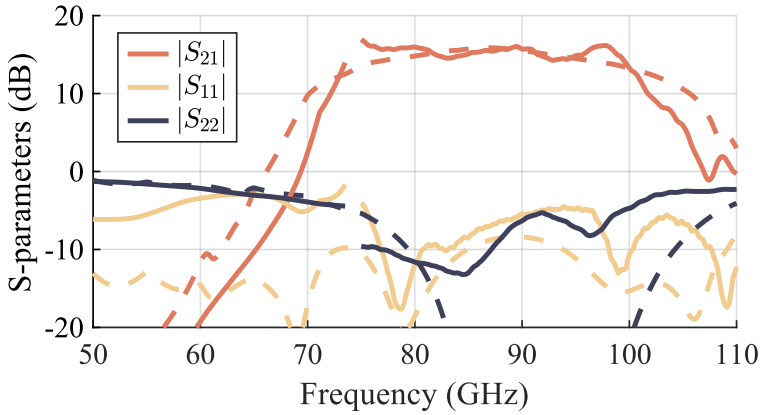


Figure 7.24: Measured (solid) and simulated (dashed) small-signal characterization of receive path. Port 1 is at the antenna port (Ant) or input of the PQC, and port 2 is at the output of the LNA (Rx). The measurements and simulations are shown for 0 V bias on both tunable loads.

A diagram of the W-band noise figure measurement setup is shown in Fig. 7.25. The measure-

ments are conducted using a Quinstar QNS-FB15LW WR-10 waveguide noise source feeding a WR-10 waveguide-to-GSG RF probe adaptor connected to the DUT. A Maury Microwave LNA/mixer combination is used for downconversion, with the LO varied for a constant IF frequency, measured with an Agilent E4448A Spectrum Analyzer noise figure personality option. This measures the raw noise figure, and the S-parameters of all of the components are characterized for post-processing and correction.

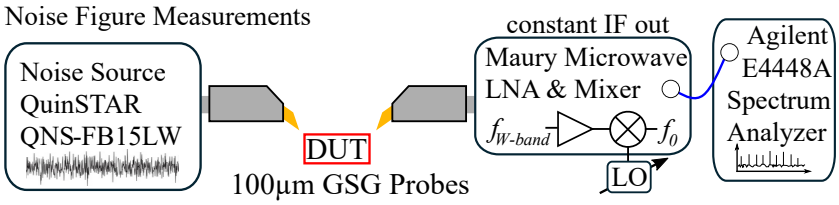


Figure 7.25: Block diagram of on-wafer noise figure measurement setup using a fixed-IF topology with a QuinSTAR noise source and Maury Microwave LNA and mixer.

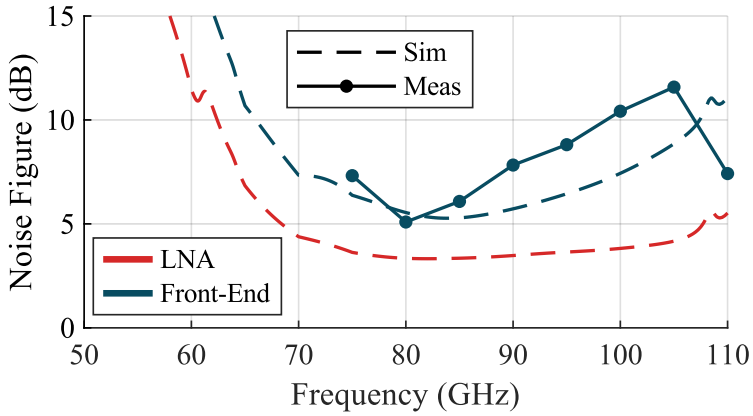


Figure 7.26: Measured (solid) and simulated (dashed) noise figure of receive path with 0 V bias on both tunable loads. The simulated noise figure of the LNA alone is shown in red.

The noise figure of the receive path is measured from 75 to 110 GHz, in 5 GHz steps, as seen in Fig. 7.26. The simulated performance of the receive path (blue) and LNA (red) are also plotted for comparison. The receive path has a measured minimum noise figure of 5 dB at 80 GHz, which aligns well with the simulated receive path noise figure of 5.5 dB at 80 GHz. The measured noise figure follows a similar trend to the simulated receive path noise figure across frequency, with a

deviation at 110 GHz.

Receive path large-signal measurements and simulations are shown in Fig. 7.27. Measurements are performed with an input power from -10 to 10 dBm across 92 to 96 GHz in steps of 1 GHz, shown in solid line. Simulations are done at 94 GHz, shown in dashed line. The measured and simulated data are in good agreement, having and input P1dB of 1 dBm with similar gain and output power. This is expected as the receive path small signal data in Fig. 7.24, line up well from 92 to 96 GHz. This high power LNA, integrated in the full-duplex front-end, will protect the receive chain from damage and remain linear while the high-power PA is transmitting.

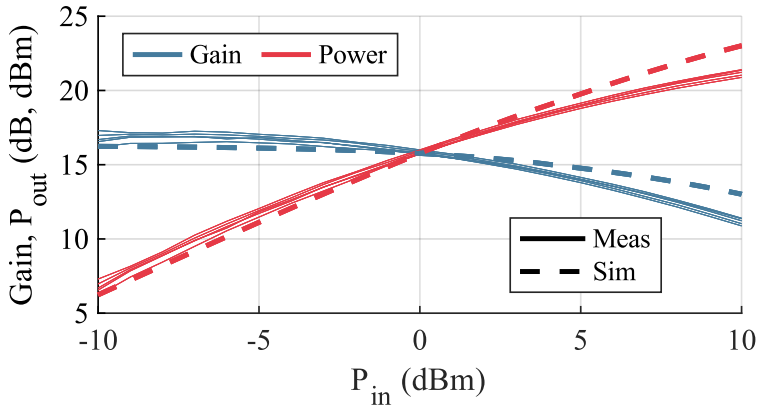


Figure 7.27: Measured (solid) and simulated (dashed) large-signal characterization of receive path. Measurements are shown from 92 to 96 GHz in 1 GHz steps and simulations are shown for 94 GHz for 0 V bias on both tunable loads.

The large signal measurements of the Tx and Rx path shown in Fig. 7.22 and Fig. 7.27 differ in deep compression. This is due to the PA and LNA having different staging ratios of 1:2:3 for the PA and 1:3:6 for the LNA. The PA staging ratio is motivated by a high PAE which requires the pervious stages to have enough gain and power handling to saturate the final stage for peak PAE. For the LNA the staging ratio is 1:3:6, motivated by high power handling and the diminishing affect the cascaded stages have on NF. Additionally, each stage of the LNA uses a validated device while the first two stages of the PA use a device scaled from a validated model.

7.5 Discussion and Conclusions

In summary, this chapter presents a tunable passive quasi-circulator (PQC) which is then integrated on chip for a in-band full-duplex analog front-end GaN MMIC from 75 to 100 GHz. The PQC network is made of three Lange couplers with tunable loads, using $4 \times 37.5\,\mu$m HEMT devices at the isolated ports of two of the couplers. This tunability allows for greater than 30 dB of isolation from transmit to receive across the band, achieved by varying the bias of tunable HEMT loads. The PQC demonstrates a return loss better than 10 dB across the band and does not show any indications of compression up to 24 dBm of input power. Therefore, the self-interference cancellation level remains constant up to the same input power level. Furthermore, in a non-ideal environment, with varying antenna impedance, simulations show the tunable loads can be used to compensate for antenna mismatch. For the designed network the average path loss in band for Tx and Rx differ, with an Rx loss of 2.5 dB and Tx loss of 9.5 dB. The high loss of the Tx path is a result of different signal path lengths between Lange couplers, resulting in a phase change which degrades signal recombination. Additionally, the required crossover of the connecting transmission lines contributes about 2 dB of loss.

Table 7.3: Comparison of W-Band Integrated Font-End GaN MMICs

Ref.	Freq. (GHz)	Duplex (Full/Half)	P_{out} (dBm)	NF (dB)	Area (mm^2)
This Work	75-100	Full	22	5-11	8
[88]	71-77	Half	30.6-31.5	4.7-5.5	10.75
[89]	75-110	Half	29	5.2-7.8	15
[90]	100-110	Half	30	6-6.4	19
[91]	75-86	Half	> 27	4.5	6.375

Due to the compact size, ease of integration, large bandwidth, high isolation and high linearity, the PQC is an attractive component for integrated transmit-receive in-band full-duplex front-ends. Additionally, it is frequency-scalable and does not require any dynamic biasing or dc power. The main drawback is relatively high Tx insertion loss, which could be improved if the phase difference in the transmission lines connecting coupler is reduced. For the implemented PQC

at W-band, phase compensation was done with tunable load on the isolated ports of the couplers. In future designs, the tunable loads can be used for compensating for mismatch in applications such as phased array, where the antenna impedance changes with scanning.

Using the PQC integrated with a 3-stage PA and LNA, to the authors knowledge, the first W-band in-band full-duplex front-end GaN MMIC is demonstrated. The transmit path shows a small signal gain ranging from 10.5 to 13.5 dB across the band, with a peak output power of 22 dBm. For receive, the front-end demonstrates a minimum noise figure of 5 dB and a gain ranging from 17 to 14 dB across the band. Additionally, the receive path shows a measured input P1dB of 1 dBm, allowing full-duplex operation without damage or compression of the receive chain. The passive quasi-circulator that enables full-duplex operation comes at the cost of additional loss, and therefore the output power of the presented front-end is lower than the compared half-duplex front-end MMICs. A comparison of W-band integrated switchable front-end T/R GaN MMICs is shown in Table 7.3, for the closest comparison to the presented front-end MMIC. The table shows competitive performance to switched front-end modules in the frequency range of 75–100 GHz with a total area of 8 mm^2. These contributions are published in [108].

Chapter 8

Contributions & Future Work

8.1 Summary and Contributions

This thesis focuses on circuits for aperture and element-level for in-band full-duplex phased arrays. Chapter 2 details the design and characterization of a MMIC front for aperture-level IBFD at X-band with transmit observation for self-interference cancellation. Chapter 4 explores the improved throughput of full-duplex compared to half-duplex operation, in addition to an antipodal Vivaldi array designed for full-duplex operation at the aperture. Chapter 5 presents an X-band GaN MMIC for an aperture-level IBFD receiver front-end and a linear 8-element antipodal Vivaldi array. Chapter 6 outlines a designed S-band MMIC for integration into a MIT Lincoln Laboratory aperture-level IBFD system operating at S-band. Finally, an element-level W-band full-duplex front-end is presented in Chapter 7, incorporating a tunable passive quasi-circulator. The chapters are summarized as follows.

- Chapter 2: This chapter presents three reflective-type, single-pole double-throw (SPDT) MMIC switch designs in Qorvo's QGaN25 250-nm GaN-on-SiC process, using a $3\times75\,\mu$m switch device size, for operation from 2.5 to 3.5 GHz. Due to the relatively low design frequency, lumped element Π network inverters are used in place of transmission lines, resulting in compact switch designs of $0.9\times0.9\,\text{mm}^2$, $1\times1\,\text{mm}^2$, and $1.4\times0.9\,\text{mm}^2$. The reported switch topologies demonstrate an insertion loss below 2 dB across the desired bandwidth with varying isolation based on the topology. Measured performance is compared with simulations, validating foundry transistor and designed lumped element Π network inverters.

These contributions are published in [30].

- Chapter 3: This chapter presents a 3.5-bit variable attenuator with a range of 55 dB in steps of 5 dB, operating from 1 to 5 GHz. Although resistive Tee networks are a common approach for variable attenuators, they typically demonstrate a dynamic range of 31.5 dB using 7 attenuation bits. We demonstrate unique attenuation bits for a much larger dynamic range, and with fewer bits, in addition to a new method of combining the bits. The implemented 1.5-bit combines a 20 dB and 40 dB bit into a single network. The R_{on} of shunt switch devices is used for the desired shunt resistance of the 20 dB and 40 dB attenuation levels, allowing a shunt resistance of 10 Ω and 1.3 Ω, accompanied by an increase in C_{off}. The calculated and measured power handling of the variable attenuator show good agreement, with a minimum 0.1 dB compression point of an input power of 25 dBm. These contributions are published in [54].
- Chapter 4: This chapter presents a system analysis of the aperture-level in-band full-duplex array, showing increased channel capacity up to a certain level of SNR degradation during full-duplex operation and an antenna array for full-duplex operation. The antenna array is a reconfigurable aperture-level in-band full-duplex made of antipodally-fed Vivaldi antennas. The linear 8-element antipodal Vivaldi array is designed for simple substrate integration with separate feeds for each antenna element. To allow for compact spacing, the width of the antenna element is reduced with corrugation added to maintain performance. These contributions are published in [66]. The fabricated and measured array is compared with simulations, showing good agreement, with some differences due to fabrication tolerance.
- Chapter 5: This chapter presents an X-band co-designed LNA, variable attenuator, and front-end T/R switching network GaN MMIC enabling aperture-level in-band full-duplex operation fabricated in the WIN Semiconductors' NP15 150-nm GaN-on-SiC process. The front-end MMIC allows for transmit signal observation at the antenna port, providing an accurate signal representation for enhanced digital self-interference cancellation. The transmit observation path uses a variable attenuator for power level conditioning for digitization.

The LNA compression and linearity are measured to determine the max allowable receive input power and the allowable added receive nonlinearity. Initial chip measurements are published in [66]. The MMIC is integrated with an X-band power amplifier to demonstrate the observation of the transmit signal. The measurement of the integrated MMICs shows an accurate observation of the transmit signal with about 25 dB reduction in signal level compared to the transmit signal. The transmit signal of the integrated MMICs through the transmit observation is also compared to the stand-alone power amplifier, which shows comparable gain across frequency.

- Chapter 6: This chapter presents a designed GaN MMIC, designed in Qorvo's QGaN25 250-nm GaN-on-SiC process, packaged for PCB level integration for a re-configurable aperture-level in-band full-duplex system. Enabling sampling of the transmit signal at the antenna level for the noise and nonlinearities generated in the transmit chain to be accurately represented during digital self-interference cancellation. The deigned MMIC demonstrates a co-designed low noise amplifier, variable attenuator, and T/R switching network. The high-power LNA allows for a robust receive path, while the variable attenuator allows for power level conditioning of the transmit observation signal.
- Chapter 7: This chapter extends the frequency range to millimeter waves at W-band and presents a tunable passive quasi-circulator (PQC) which is then integrated on chip for an in-band full-duplex analog front-end GaN MMIC from 75 to 100 GHz. The tunable PQC allows for greater than 30 dB of isolation from transmit to receive across the band and does not show any compression up to 24 dBm of input power. Due splitting of the signals through the network and termination in a load, there is an inherent loss for both Tx and Rx. Due to the compact size, ease of integration, large bandwidth, high isolation, high linearity, and frequency-scalability, the PQC is an attractive component for integrated transmit-receive in-band full-duplex front-ends. Using the PQC integrated with a 3-stage PA and LNA, to the authors' knowledge, the first W-band in-band full-duplex front-end GaN MMIC is demonstrated. With a peak transmit output power of 22 dBm at 96 GHz and a receiver

gain across W-band from 17 to 14 dB. These contributions are published in [109] and [108].

8.2 Future Work

Several related topics are pursued as a part of this thesis as avenues for future work. The next section describes the design and initial characterization of a GaN W-band LNA that can provide improved resilience to high-power interference signals. Section 8.2.2 discusses further integration of the C-band chip into an array, performed at the MIT Lincoln Laboratory and including the MMICs designed in this thesis. Section 8.2.3 considered system-level integration of the designed X-band in-band full-duplex array, considering its limited spacing and front-end MMICs at each element. Additionally, the effects of array scanning are discussed, and its effects on element coupling and impedance over scan angle and frequency. These initial results provide a starting point for an IBFD array with self-interference cancellation at the aperture, analog, and digital levels.

8.2.1 W-band HRL T3 LNA

The designed in-band full-duplex front-end presented in Chapter 7 incorporates a high-power W-band LNA. On a later run, this LNA was taped out for individual testing. The layout of the 3-stage LNA is shown in Fig. 8.1, has a total area of $3\times1\,\mathrm{mm}^2$. As discussed previously, for high-power, the LNA uses increasing device sizes.

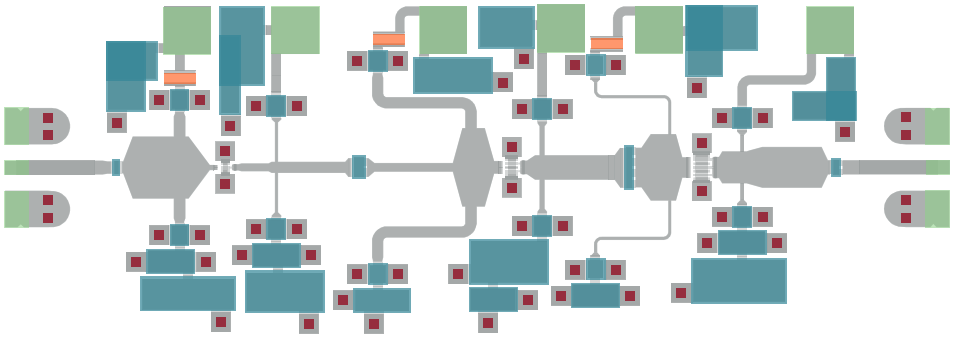


Figure 8.1: Layout of high-power W-band LNA previously incorporated in integrated full-duplex front-end MMIC.

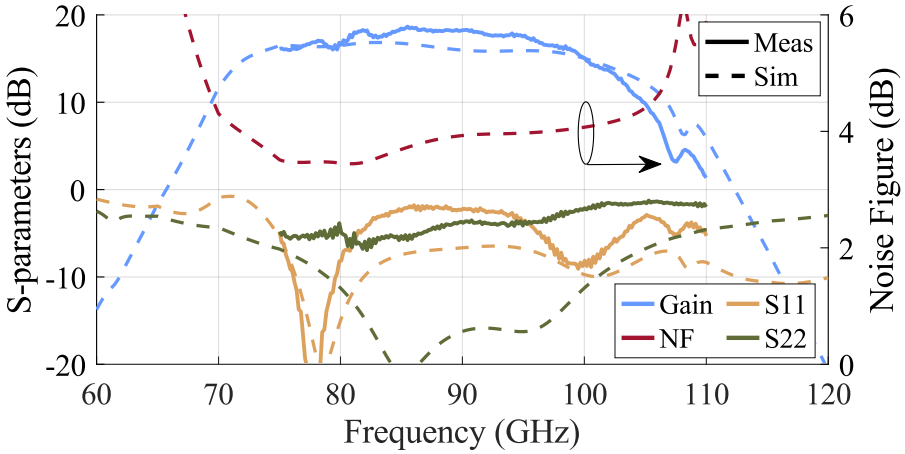


Figure 8.2: Measured (solid) and simulated (dashed) S-parameters and NF of the designed LNA. Measured gain shows good agreement with simulation, while measured $|S_{11}|$ and $|S_{22}|$ degrade compared to simulation. Simulated NF is below 4 dB across W-band.

Small-signal measurements (solid) and simulation (dashed) are shown in Fig. 8.2. The LNA is biased with V_d= 12 V and I_d = 100 mA, with all the gate and drain biases tied together off chip, for a DC power of 1200 mW. The measured and simulated gain align well with a faster roll off in measured gain at higher frequencies and a higher measured peak gain at 90 GHz. The input and output match $|S_{11}|$ and $|S_{22}|$ degraded in measurement compared to simulation, possibly due gate

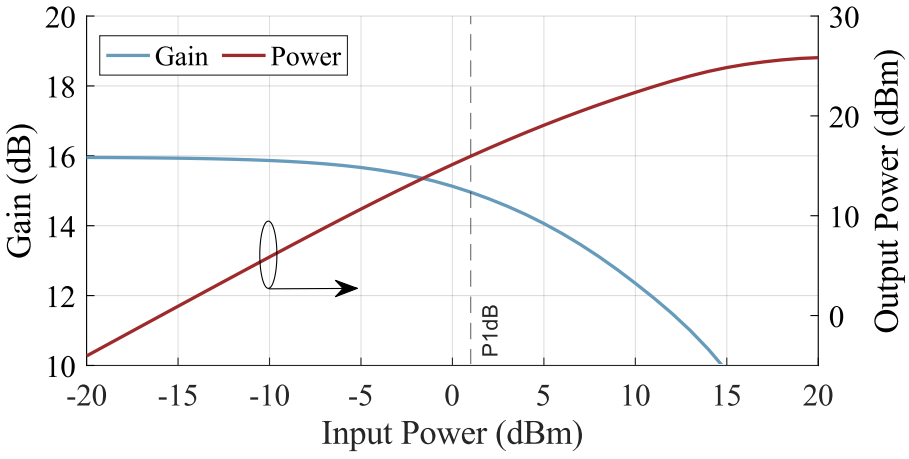


Figure 8.3: Simulated large-signal gain and power of W-band LNA at 91 GHz. The simulations show an input P1dB point of 1 dBm.

and drain bias being tied. To ensure the designed device current at each stage, each LNA stage can be biased separately during measurement. The simulated NF is shown on the right of the figure, remaining below 4 dB across W-band. For further investigation of the measured and simulated performance, the LNA NF can be measured.

With the application of in-band full-duplex, the LNA was designed to have an input P1dB point greater than -4 dBm. The simulated large signal gain and power at 91 GHz is shown in Fig. 8.3, with an input P1dB point of 1 dBm. Measurement of large signal gain and power to demonstrate power handling, and further compare simulation to measurements, can be performed along with the comparison of simulated and measured drain current, and is left to future work [110].

A comparison of the published W-band GaN-on-SiC MMIC LNA with the designed LNA is shown in Table 8.1. The performance metrics for the presented LNA, shown in the table, are taken from the full-wave simulated LNA. The 3 dB gain bandwidth of the designed LNA is the second highest with a competitive gain. For the designed high power handling, the simulated LNA shows the highest P1dB with one of the lowest NF ranges. This is a result of increasing device sizes for each stage of the LNA. The first stage has the largest impact on cascaded NF uses the smallest device for the most gain and lowest NF, while the last stage has the largest impact on P1dB uses the largest device. High-power LNA can also apply to a half-duplex system, which allows the removal of a limiter at the input.

Table 8.1: W-band GaN-on-SiC MMIC LNA Comparison Table

Ref.	Gate Length (nm)	Frequency (GHz)	Gain (dB)	$P1dB_{input}$ (dBm)	DC Power (mW)	NF (dB)
[111]	70	63-101	21-24	-10	307	2.8-3.3
[112]	90	75-83/91-96	15.5-16/18-19	n/a	200	3.85/3.55
[113]	100	91-96	>20	n/a	128	2.9-5
[114]	120	80	20.4	n/a	n/a	3.8
[115]	100	78.5-89	14.5-17	-7	109	4.5-5.2
[116]	100	84	25	-6.7	800	5.6
[117]	100	106.5-113.5	28.4-31.4	-13	2400	7.6
This Work*	40	71-102	13.5-16.5	1	1200	3.4-4

8.2.2 System Integration for 64-Element In-Band Full-duplex Array

As mentioned in Chapter 6, the demonstrated MMIC is designed and packaged into a T/R module for implementation into an aperture-level in-band full-duplex array at MIT Lincoln Laboratory [6]. A schematic for an individual array element is shown in Fig. 8.4, separating the aperture, T/R Module, and backplane. For the 64-element array, each antenna element is dual-polarized, requiring a minimum of 128 T/R Modules. Testing of T/R modules has been carried out at Lincoln Laboratory, with 133 boards passing evaluation tests.

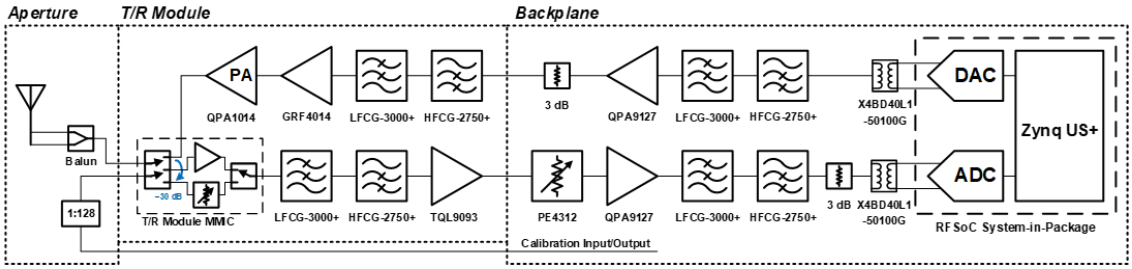


Figure 8.4: Schematic for each antenna element aperture, T/R module, and backplane. Each element is dual-polarized with two T/R modules per element.

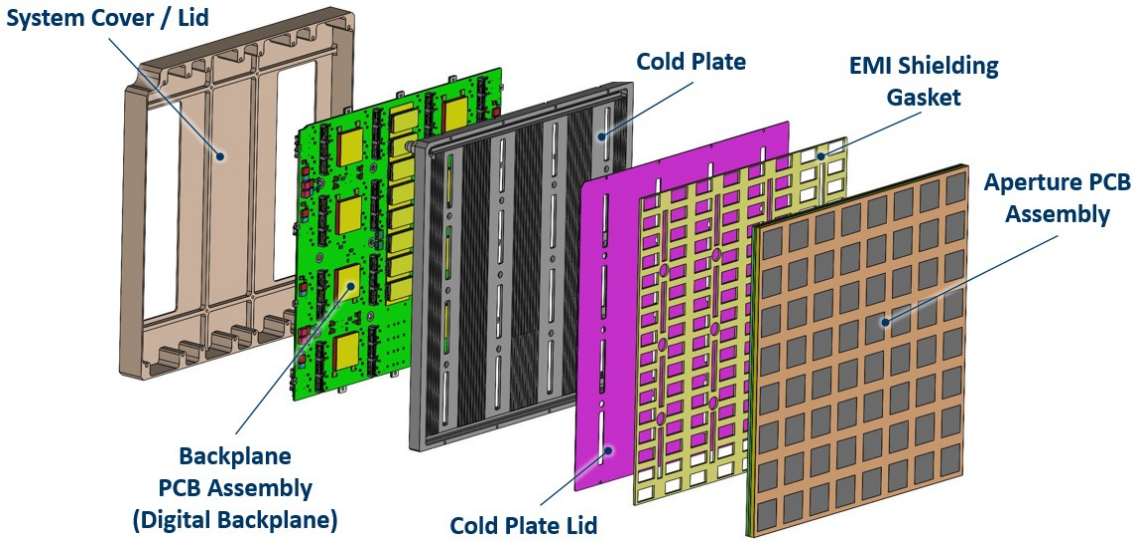


Figure 8.5: Aperture-level in-band full-duplex phased array integrating with the chip discussed in Chapter 6. With the increased components for IBFD operation, the 64-element requires compact integration.

A diagram of the complete array sections is shown in Fig. 8.5. Implementation of a 128 T/R module in the confined spacing of the array requires compact integration. To remove the generated heat from the T/R modules and digital backplane electronics, a cold plate is used, which can be seen in the figure.

8.2.3 Linear 8-Element X-band Antenna Array for IBFD Integration

For an aperture-level in-band full-duplex phased array at X-band, the MMIC discussed in Chapter 5 and the linear 8-element array in Chapter 4 could be used as part of the system. To complete the system, a digital backend is required for SIC, with an algorithm similar to that presented in [6]. Additionally, the analog signals will need to be digitized for SIC, focusing on minimizing added noise. For SIC, each transmitting element will require an analog Tx and TXO signal trace, which can all be digitized separately or split/combined in the analog domain. If the Tx and TXO signals are split/combined in the analog domain, the Tx and TXO traces will have to cross each other, requiring a multilayer board.

Integration with a half wavelength (15 mm) spacing array at 10 GHz, as the one presented

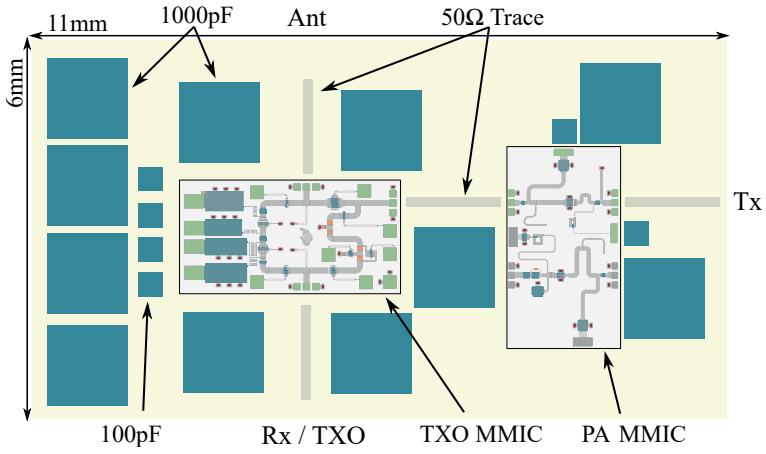


Figure 8.6: Layout of integrated X-band transmit observation MMIC with PA MMIC discussed in Chapter 5 with reduced mounting size of 11 mm by 6 mm. Operating at 10 GHz with a 15 mm half wavelength, implementation into a 10 GHz half wavelength element spacing antenna, similar to that presented array in Chapter 4, requires compact integration.

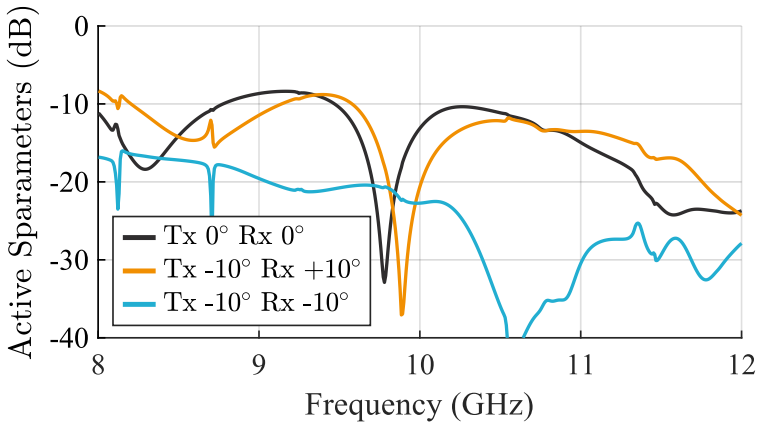


Figure 8.7: Simulated array coupling using "Active Sparameters" across scan angle at port 4 of the previously proposed aperture-level in-band full-duplex antipodal Vivaldi array in Chapter 4. Coupling between elements for aperture-level IBFD can be reduced based on the scan angle of transmit and receive, improving overall SIC.

in Chapter 4, electronics require condensed integration. Fig. 8.6 shows the layout of a condensed aperture-level IBFD front-end, compared to that in Chapter 4, having an area of 11 mm × 6 mm. With the front-end oriented for antenna alignment, the space separating each front-end, which will handle bias and analog signal routing, is 4 mm.

Coupling between elements and return loss for each element is a key factor for IBFD, which changes based on steering angle. Fig. 8.7 shows the active S parameters (coupling between array elements) at port 4 of the antenna array presented in Chapter 4, for different steering angles at 10 GHz of the transmit and receive subarrays. The steering angle can be used to reduce coupling between elements, increasing the overall SIC of the system and relaxing the required receive path power handling.

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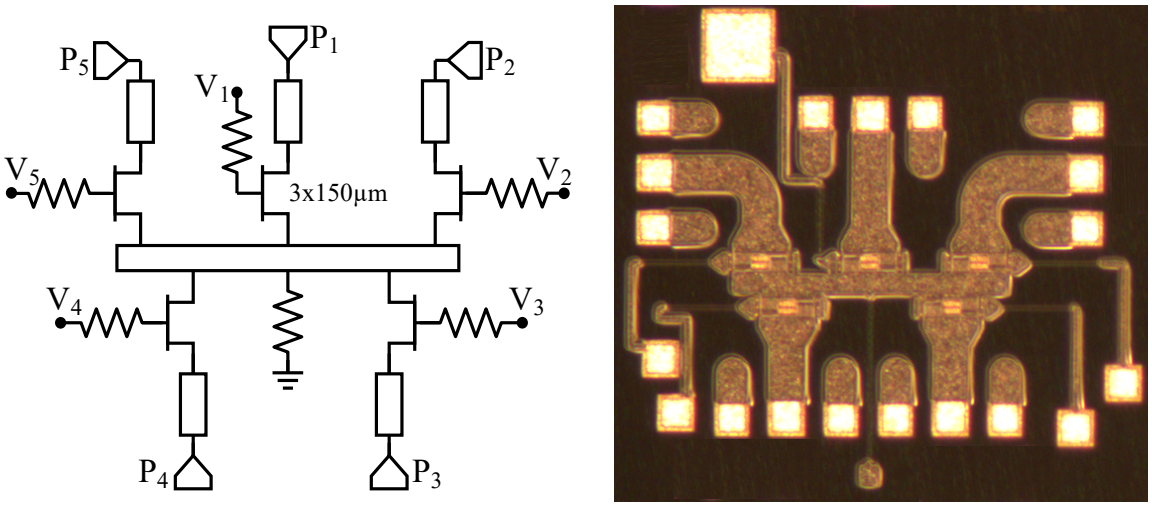
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Appendix A

Symmetric 5-port switch

For the proposed multi-function aperture-level in-band full-duplex array in Chap.6, the front-end 5-port switching network is a key component. An initial design of a symmetric 5-port switch is presented. This was done in Qorvo's QGaN25 process, on the same run as the initially validated variable attenuator in Chap.3. Due to the limited area on the run, the switch has a compact size of $1.4 \times 1.3\,mm^2$ using $3 \times 150\,\mu$m switch devices. A schematic of the 5-port switch is shown in Fig. A.1a, with the 5 ports labeled P_1 through P_5, their corresponding gate bias, and a grounded resistor for DC biasing. The fabricated MMIC is shown in Fig. A.1b.



(a) (b)

Figure A.1: (a) Schematic of symmetric 5-port switch using $3 \times 150\,\mu$m switch devices. (b) Compact layout of 5-port $1.4 \times 1.3\,mm^2$ GaN MMIC in Qorvo's QGaN25 process.

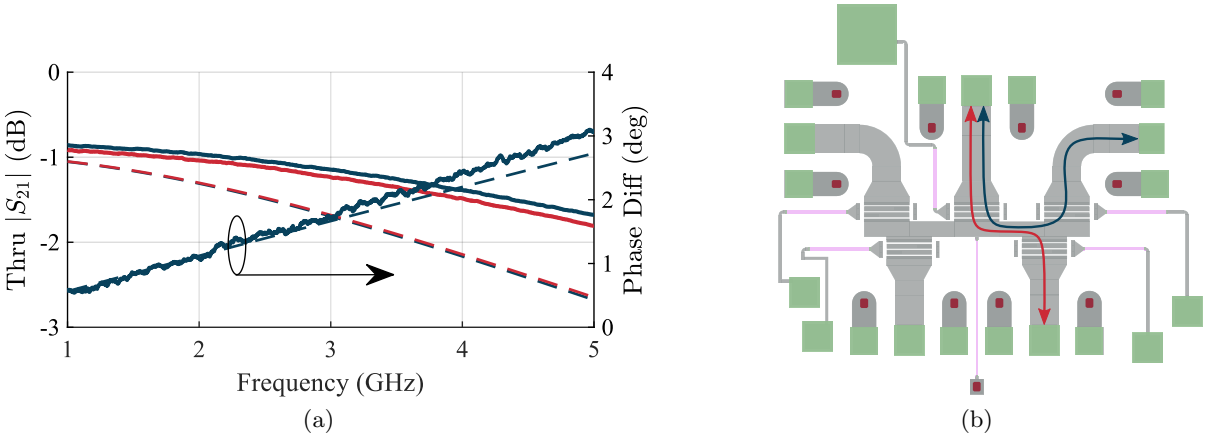


Figure A.2: (a) Measured (solid) and simulated (dashed) insertion loss from P_1 to P_2 and P_1 to P_3 and the phase difference between the tow paths. (b) Layout of switch with depicted signal paths from P_1 to P_2 and P_1 to P_3.

Small single measurements of the switch with one input port and one output port, P_1 to P_2 and P_1 to P_3, are shown in Fig. A.2a with measured in solid and simulated in dashed. The measurements use a $-40\,\mathrm{V}$ bias at the gate of the off devices and a $0\,\mathrm{V}$ bias at the gate of the on devices. The plot shows the insertion loss of the two different paths along with the difference in phase of the two paths. Shown with the layout of the switch in Fig. A.2b, arrows of the different signal paths are shown for clarity. The colors of the traces in Fig. A.2a match the color of the arrows in Fig. A.2b, showing the signal path.

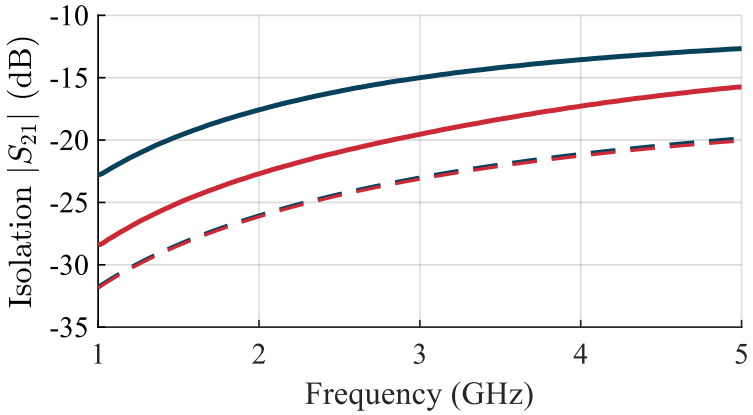


Figure A.3: Measured (solid) and simulated (dashed) isolation from P_1 to P_3 when P_1 to P_2 is a through in blue and P_1 to P_2 when P_1 to P_3 is a though.

Isolation of the different signal paths is shown in Fig. A.3 with measured in solid and simulated in dashed. The color of the different traces corresponds to which path is a through path. The blue trace shows the isolation from P_1 to P_3 when P_1 to P_2 is a through and red shows the isolation from P_1 to P_2 when P_1 to P_3 is a though. As seen in the plot, the blue and red traces differ in isolation due to different signal paths, with the same device sizes and biasing for the signal paths. The simulated isolation shown with a dashed line overlap for the different signal paths and has a higher isolation than measured.

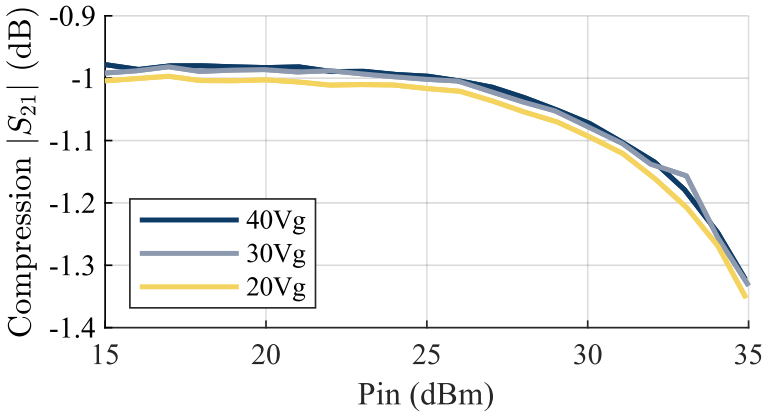


Figure A.4: Measured large signal of the through path from P_1 to P_2 with multiple off switch bias level at 3 GHz. With no difference in compression for different off switch bias voltages, the compression of the switch is based on the on switch power handling.

The large signal of the through path from P_1 to P_2 is measured at 3 GHz shown in Fig. A.4 with multiple bias levels for the off switch devices. The switch devices provided by the PDK are linear, so there is no simulated data to compare to the measured data. With different trace colors, the compression for different off switch bias levels is shown with no difference in compression. Due to the off switch bias voltage, the compression on the switch is based on the on devices and not the off devices. The power handling of the on devices can be increased with device size to allow more current through the device before compression. The power handling of the off switch devices does not scale with device sizes and is related to the voltages across the device.

With each port having a corresponding switch device, many different through-path configurations can be realized. This includes having one input and four outputs or one input and two

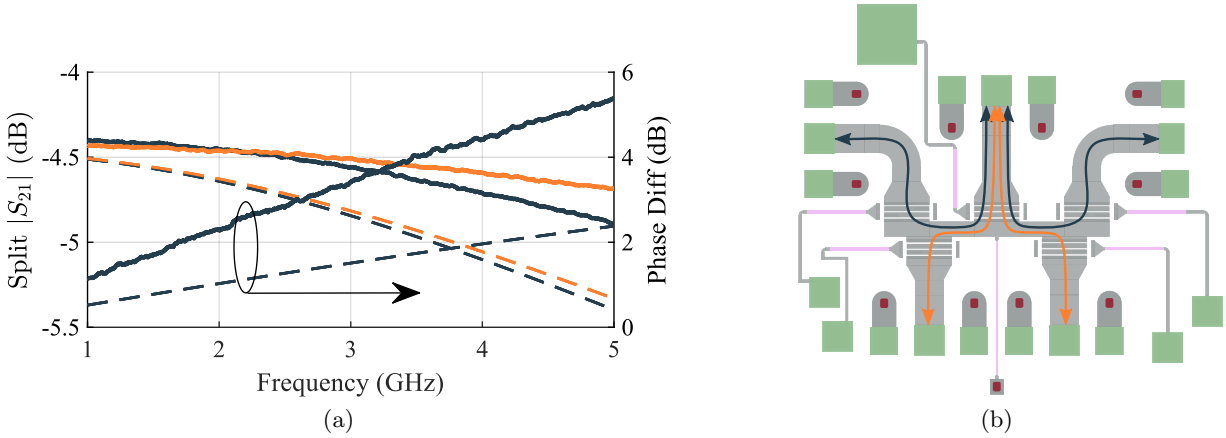


Figure A.5: (a) Measured (solid) and simulated (dashed) for a single input and two output configurations of the switch. (b) The layout of the switch with one input and two output configurations is shown with orange and black arrows over the layout. The measured and simulated data show the insertion loss for one signal path while the other through path is terminated in a 50Ω load. The phase difference of the two configurations is also plotted on the right.

outputs. Fig. A.5a shows the measured (solid) and simulated (dashed) small signal data for one of the signal paths when the switch is configured with one input and two outputs. The specific switch configuration that is measured and simulated is shown with arrows over the layout in Fig. A.5b. The color of the arrows matches the plotted measured and simulated data. As expected from the

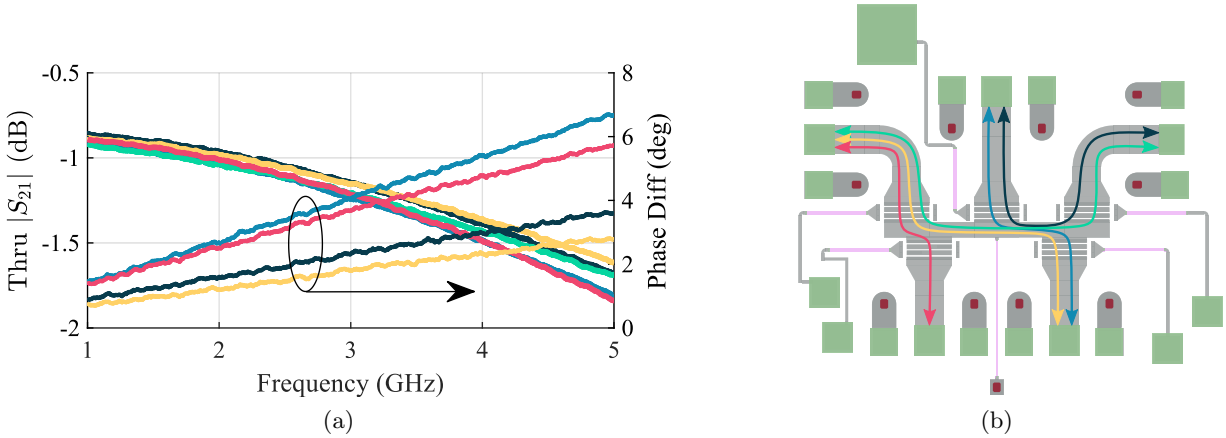


Figure A.6: (a) Measured insertion loss and phase difference of the one-input-one-output signal path combinations. (b) Layout of the switch with arrows of the measured one-input-one-output signal paths colored to match the plotted data.

splitting of the signal power, the measured and simulated data show an increase in insertion loss of about 3 dB compared to a one-input-one-output configuration. This flexibility in switch configuration allows for a reconfigurable front-end, such as those in an aperture-level in-band full-duplex system.

With a completely reconfigurable switch, there are many combinations for one input and one output configuration. The measured small signal data of these different combinations is shown in Fig. A.6a with the colors corresponding to the arrows over the layout in Fig. A.6b. This demonstrates minimal difference in insertion loss for the different signal paths, allowing the switch to be an arbitrary 5-port switch with any input and output port connection.

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