Broadband Multi-Beam Front-Ends with Interference Suppression

by

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Microwave and millimeter-wave frequencies in the electromagnetic spectrum are increasingly crowded leading to difficulties in creating high-performance systems in a spectrally congested environment. This thesis addresses challenges of broadband analog front-ends by introducing new components to work in broadband phased arrays. The broadband performance allows the same system to operate at different frequencies, avoiding spectral interference, while the phased array architecture facilitates better use of the spatial dimension, either directing radiated power or received power. First, two MMIC components are introduced operating over 6–12 GHz, a GaAs phase shifters and a 2-W GaN power amplifier. Compatible with these components is a 6–12 GHz metal double-ridged horn antenna array, which is characterized for both electromagnetic and thermal performance. This validated 4×1 array is expanded to a 4×4 array in simulations. Beamforming feed networks for this array are implemented on novel processes that enable heterogeneous integration: HRL's MECA process and 3D Glass Solutions' Apex glass. The Butler matrix beamformer is then scaled to operate at 44 GHz, a millimeter-wave frequency useful for future communication systems, as an on-chip GaAs implementation. Although this compact design has a smaller bandwidth compared to previous examples, this limitation is addressed by introducing a novel frequency-tunable beamformer. A reflective phase shifter is integrated into the GaAs Butler matrix, allowing frequency tuning from 40 to 44 GHz, resulting in reduced phase error and a broader bandwidth. Finally, the thesis addresses the receive operation of broadband front-ends, focusing on in-band external interference, which is a significant issue for these systems. To prevent ADC saturation, an on-chip MMIC interference suppression circuit is proposed, first presenting the theory of operation and then introducing a 6—12 GHz proof-of-concept design. The thesis concludes with suggestions for future work that builds on the components developed in this research.

Dedication

To my husband, family, friends, and all those who have supported me.

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Chapter 1

Introduction

This thesis explores various analog components essential to front-end systems for wireless communications. The main motivation is the crowding of the spectrum by commercial and military radio sources. For various applications to coexist and share the spectrum, active antenna arrays are often employed. These active arrays require a number of components at the carrier frequency, e.g. beamforming networks, power amplifiers, low noise amplifiers, filters, and antennas.

1.1 Electromagnetic Spectrum, Spectrum Congestion and Interference

The focus of this thesis is on the microwave segment of the electromagnetic spectrum, typically defined as frequencies from 3 GHz to 300 GHz, corresponding to free-space wavelengths between 10 cm and 1 mm. Within this range, millimeter waves, with wavelengths on the order of millimeters (generally above 30 GHz), represent a particularly interesting subset. The Federal Communications Commission (FCC) regulates the radio spectrum from 3 kHz to 300 GHz, as shown in their frequency allocation chart [1]. These frequencies support a wide variety of wireless applications, including cellular communications [2], satellite communications [3], radar [4], sensing [5], internet-of-things [6], industrial processing [7], and medical and biological applications [8]. These applications use a modulated carrier frequency to encode the data to be transmitted. The specific allocation of these frequencies is shown in Fig. 1.1. If two systems have carrier

frequencies that are close, they can interfere, thus degrading operation for either and/or both applications. Quantification of what "close" means depends on the specific application, which will be further examined in subsequent sections. In addition to overlapping in frequency, wireless applications can also interfere spatially, as discussed more in Section 1.3.

The regulation of spectrum in the United States began with the creation of the FCC through the Communications Act of 1934. The FCC oversees spectrum management for various commercial, state, and local government interests. Additionally, the National Telecommunications and Information Administration (NTIA), established in 1978, provides spectrum management and legislative advisory services. Fig. 1.1 highlights the complexity of spectrum management with various application-specific allocations.

For example, the bright yellow boxes in Fig. 1.1 are allocations for radioastronomy, which involves the detection of very weak signals from space. The allocation is from 608–614 MHz, between two television broadcasting allocations (blue boxes), which are high power transmitters. If the television broadcast signals leak over in frequency or the radioastronomy components work in a larger bandwidth than their allocation, the quality of the data for radioastronomy received will be degraded. Similarly, an Industrial, Scientific, and Medical (ISM) band allocation at 2.450 GHz, which can be used for medical application. These systems could be impacted by adjacent mobile allocations.

The growing number of users and increasing data demand, as depicted in Fig. 1.2 by Ericsson for fixed wireless access (FWA), mobile data, 5G, and previous generations (2G/3G/4G) [10], underscores the escalating demand for spectrum, in just one of the many uses for microwaves and millimeter-waves. This trend highlights the increasing demands on the spectrum to accommodate rising data rates.

Systems generally have a limited fractional bandwidth around their carrier frequency. For instance for a 10% bandwidth, a system operating at 10 GHz would have a bandwidth of 1 GHz, whereas a system at 30 GHz would have a bandwidth of 3 GHz. This increased bandwidth supports greater data throughput, motivating interest in utilizing higher frequency bands, particularly in the millimeter wave range. Additionally, while it does not appear obvious in Fig. 1.1, there are fewer users already at these higher frequencies, above 30 GHz where the bottom row. The x-axis for frequency is a log scale so there are many more frequencies covered in this row than previous rows.

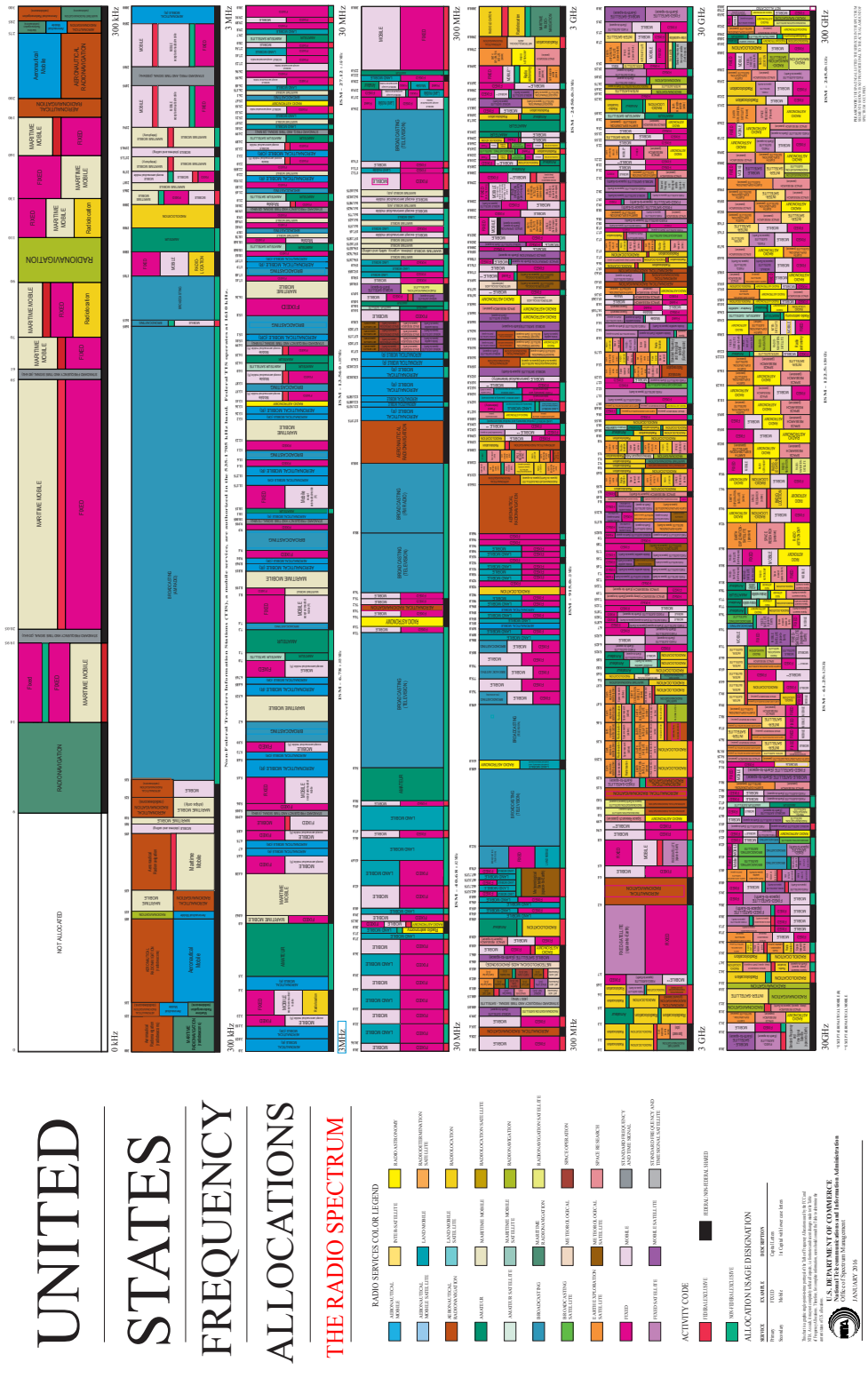


Figure 1.1: United States spectrum allocation as of 2016 [1].

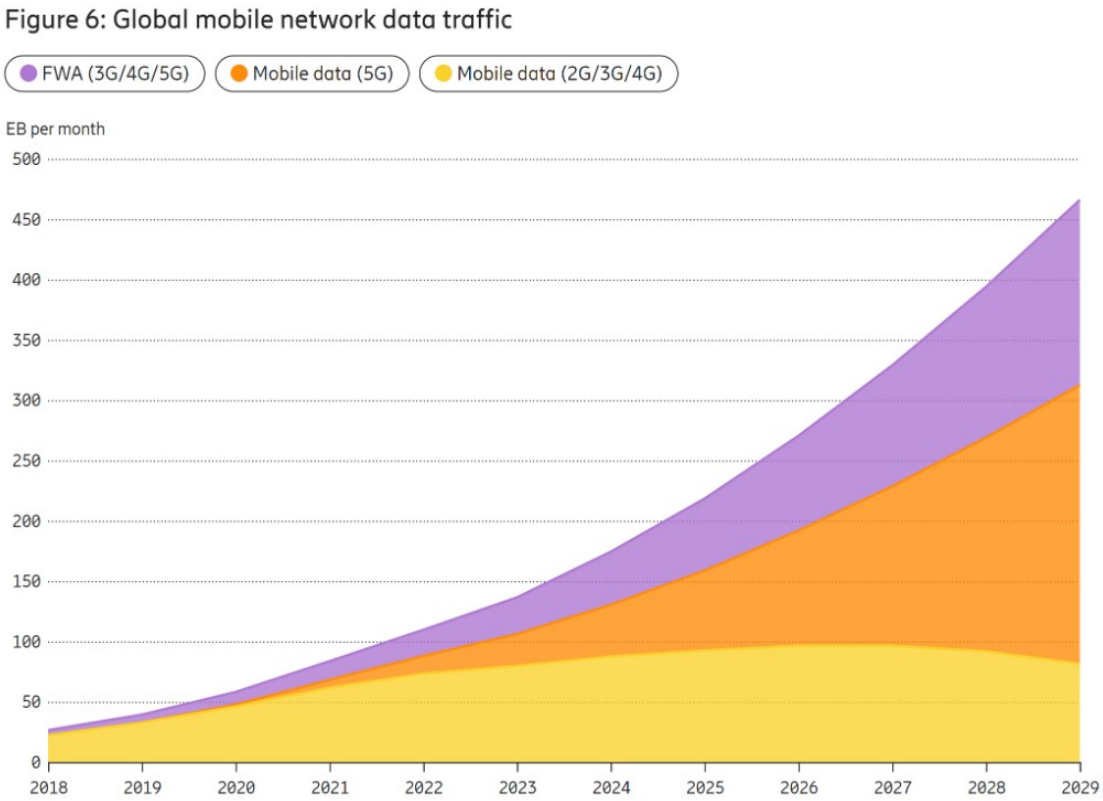


Figure 1.2: Projected growth (in terms of data) of mobile traffic through 2029 from [9]. Total usage is projected to triple in the next 5 years with mobile network data requirements more than doubling by 2029.

Another solution considered is reallocating and sharing spectrum bands. Potential bands for reallocation include 5.030-5.091 GHz, 7.125-8.400 GHz, 12.2-12.7 GHz, 12.7-13.25 GHz, 37.0-37.6 GHz, 42.0-42.5 GHz as discussed in the 2023 National Spectrum Strategy [10]. A notable example of spectrum sharing is the introduction of the Citizen Broadband Radio Service (CBRS) [11], which has enabled shared and coordinated usage between federal and non-federal entities since 2015. Future spectrum reallocation will necessitate advanced spectrum sharing strategies, imposing stricter requirements on radio hardware to minimize interference from transmitters and suppress interference in receivers. Additionally, developing technology for millimeter waves is crucial to leveraging less crowded spectrum areas, despite challenges such as increased propagation loss, high costs of new technologies, and atmospheric effects [12].

There are different figures of merit used to describe interference from signals with similar carrier frequencies. One common metric, especially in communication standards, is the Adjacent Channel Power Ratio (ACPR). ACPR measures the amount of power in an adjacent channel relative to the power in the

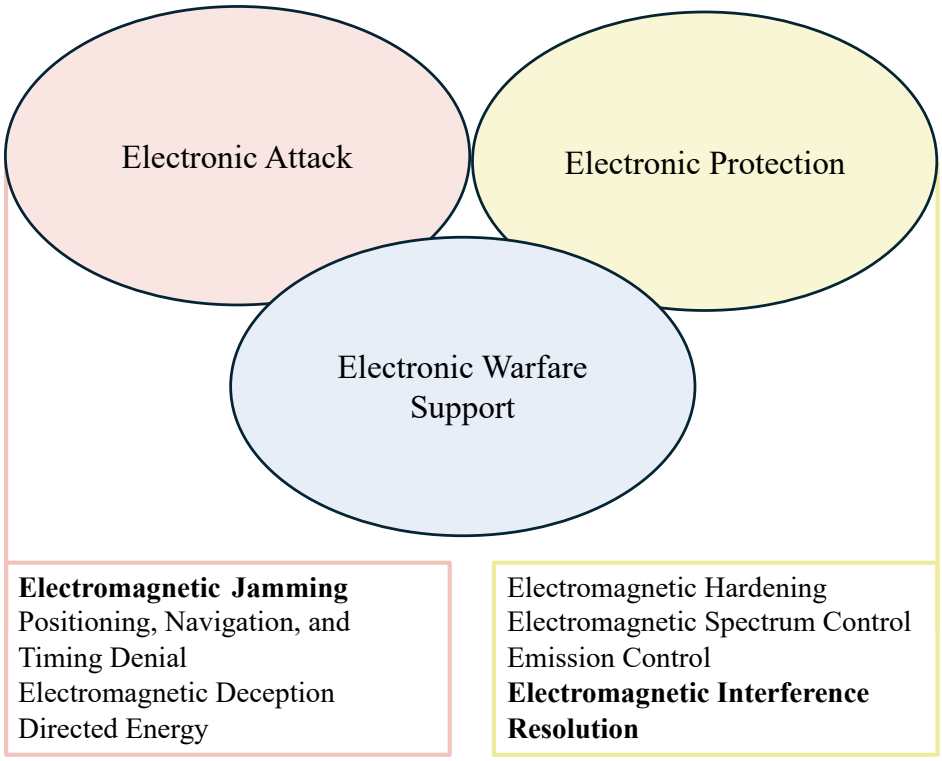


Figure 1.3: The three primary divisions of electronic warfare in the United States with some specific activities listed related to EA and EP. Motivation for the work in this thesis falls under both EA and EP, electromagnetic jamming and electromagnetic interference resolution, shown in bold text.

intended channel for a modulated signal [13]. A lower ACPR indicates less leakage into adjacent channels, reducing potential interference.

1.2 Electronic Warfare

While the above discussion focuses on commercial use of the spectrum in the United States, the U.S. government also has broad usage, e.g. Departments of Commerce and Defense. One example is the large topic of electronic warfare (EW), which refers to "military activities that use electromagnetic energy to control the electromagnetic spectrum ('the spectrum') and attack an enemy" [14]. This has three primary divisions:(1) electronic protection (EP); (2) electronic attack (EA); and (3) electronic warfare support (ES) [15]. An overview of EW is shown in Fig. 1.3.

EP is defined as the "division of electronic warfare involving actions taken to protect personnel, facilities,

and equipment from any effects of friendly or enemy use of the electromagnetic spectrum that degrade, neutralize, or destroy friendly combat capability" [14]. EA is defined as the "division of electronic warfare involving the use of electromagnetic energy, directed energy, or antiradiation weapons to attack personnel, facilities, or equipment with the intent of degrading, neutralizing, or destroying enemy combat capability and is considered a form of fires" [14]. ES is defined as the "division of electronic warfare involving actions tasked by, or under direct control of, an operational commander to search for, intercept, identify, and locate or localize sources of intentional and unintentional radiated electromagnetic energy for the purpose of immediate threat recognition, targeting, planning and conduct of future operations" [14].

There are a wide range of EW activities, [16] lists 24 individual primary activities, some specific examples listed under EA and EP are included in Fig 1.3, including in bold font two that motivate the work in this thesis. Some varied examples include electromagnetic deception, electromagnetic hardening, electromagnetic intrusion, electromagnetic pulse, electronic security, electronic reconnaissance, precise geolocation, and low-observability/stealth [16]. One specific example, electromagnetic jamming, motivates the work done for transmit elements shown in this thesis. Electromagnetic jamming falls under the umbrella of EA [16]. It is defined as "the deliberate radiation, reradiation, or reflection of electromagnetic energy for the purpose of preventing or reducing an enemy's effective use of the electromagnetic spectrum, and with the intent of degrading or neutralizing the enemy's combat capability" [14]. In short, the goal of jamming is to radiation large enough amounts of power to interfere with advisories' systems, so requires high enough power systems that can radiate enough directed power, one such solution which will be introduced next are phased arrays. While high directed power is often the primary objective for a jamming system, other requirements may include efficiency, temperature limitations, and bandwidth requirements. Under EP, electromagnetic interference resolution motivates the work in this thesis on the receive side. Interference mitigation for friendly forces in congested environments is an important tasks and can be vital for successful operation.

Broad bandwidth systems offer the advantage of flexibility for continuous usage if there are intentional or unintentional congestion at the initial frequency of operation. They also have an advantage that it can be used at different frequencies so a single set of hardware can be utilized for multiple systems, therefore reducing the overall size, weight, and power (SWaP).

On the topic of bandwidth, it is important to note in this context, bandwidth refers to overall bandwidth of the RF carrier. This means at what frequencies the system can operate. This is compared to instantaneous bandwidth which refers to the real-time bandwidth used by a specific signal, or the bandwidth at which the a system is transmitting/receiving at the same time. For example, in this thesis, many components (Chapters 2, 3, 4, 7) have an RF or carrier bandwidth of approximately 6–12 GHz. The instantaneous or signal bandwidth is on the order of 10 MHz or 100 MHz. The focus of this thesis is broad RF bandwidth, covering up to an octave.

1.3 Phased Arrays

In wireless systems, the spatial aspect of performance is also considered, both for overall system performance and to mitigate interference. For example, for a radar system, the beam needs to be focused on the target to get meaningful data. Or in communication systems, power (and cost) are a concern, so it is advantageous to have a beam focused directly on the user. Similarly, in jamming, focused beams mean that excess power is not wasted and the target is the one affected.

Phased arrays allow for directed and steered beams, and are a concept that is discussed and studied extensively since first introduced in the middle of the 20th century. A more complete overview can be found in several books focused specifically on phased arrays, e.g [17–20]. Briefly, the general theory of operation will be presented here.

A simple diagram for operation of an uniformly spaced phased array is shown in Fig. 1.4. For an n element array, each path has its own phase shift, $\Phi_1, \Phi_2, ..., \Phi_n$ before the antenna, either directly from the digital controls or through analog power dividers and/or variable gain of the amplification element in each path, there is an associated magnitude $A_1, A_2, ..., A_n$. Often, the phase difference between adjacent paths to held constant, known as the progressive phase shift (PPS), so $\Phi_2 - \Phi_1 = \Phi_3 - \Phi_2 = \Phi_n - \Phi_{n-1}$.

The geometry of the array, frequency of operation, and amplitude and phase of each path result in what is known as the array factor (AF). The AF is the generalized sum of the electric field vector from the position of each of the antenna elements. Full derivation of AF can be found in most antenna or phased array textbooks

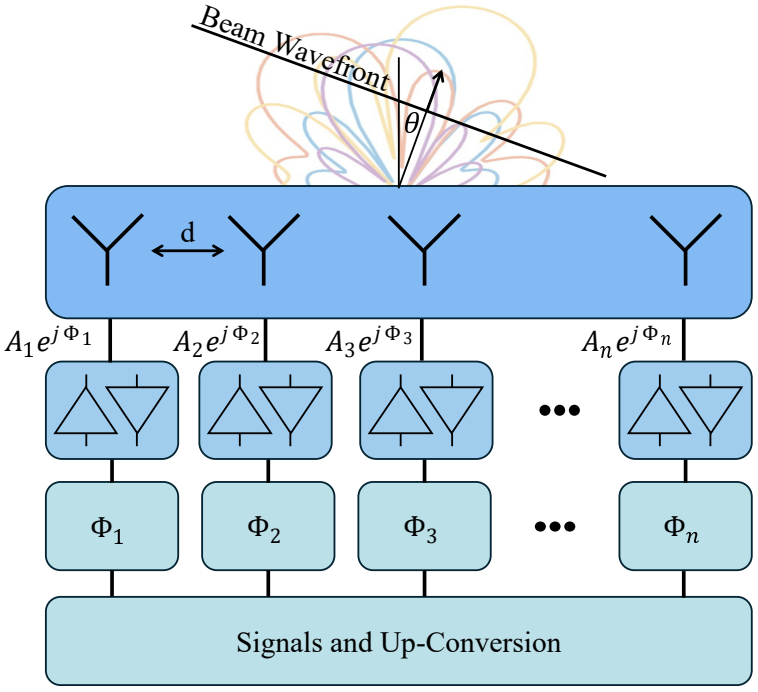


Figure 1.4: Diagram of phased array operation of an n element array with element spacing of d. The array factor at angle θ can be found by the geometry of the array. Each path under goes a phase shift Φ_i and amplification at the antenna array the value for each path can be found as $\underline{A}_i = A_i e^{j\Phi_i}$.

so a final result for an uniformly spaced array is:

$$AF = \sum_{i=1}^{n} A_i e^{j(kd\cos\theta + \Phi_i)} \tag{1.1}$$

where n is the total number of elements, k is $2\pi/\lambda$, λ is wavelength of frequency of operation in the medium of operation, d is the distance between elements, θ is the beamsteering angle, A_i is the amplitude at the ith element, and Φ_i is the phase shift at the ith element.

This can be rearranged to find the PPS needed for a desired beamsteering angle. This is found as

$$PPS = \frac{2\pi d \sin\theta}{\lambda} \tag{1.2}$$

where d is spacing between elements, θ is the desired beamsteering angle, and λ is wavelength at frequency of operation. This array factor theory can and has been extended for circular arrays, 2-D arrays, and other specific cases and derivations can be found in many antenna books, e.g. [21], [17].

The total excitation of an array is found by multiplying the beam pattern for a single element by the

calculated array factor [21]. The AF gives the direction and general pattern, but the element pattern is also integral to understanding the overall operation of an array system. One limiting factor for array design is the appearance of grating lobes, or additional maxima in the AF. At broadside, grating lobes appear once the element spacing goes beyond one-half wavelength, so geometric design of antenna arrays is limited to prevent radiation in unwanted directions.

Beamsteering for phased arrays can be done in the digital or in the analog domain. In digital beamsteering, the phase and amplitude for each element is defined in baseband at the digital back-end and up-converted to feed each antenna element. Since each path is fed with its own amplitude and phase, there is greater tunability and reconfigurability available. Each path requires its own DAC/ADC and up-/down-converter raising the overall cost and complexity.

Analog beamsteering for phased arrays, with an example block diagram shown in Fig. 1.5, is done using analog components. This means there is a single baseband signal from the digital backend and the power division and phase shift is done using analog components. This method allows for less complexity on the digital side and fewer components like DACs/ADCs, but it is more limited in reconfigurability. This can especially be true for amplitude reconfigurability which is straightforward when done digitally but requires additional design in the analog domain [22, 23].

One area of interest showing intriguing promise in the use of hybrid beamforming, having both digital and analog beamforming to get the advantages of both methods while minimizing the drawbacks. For this method, the array is split into smaller sub-arrays. Each sub-array has its own digital input, utilizing digital beamsteering methods, and within each sub-array, analog beamsteering is used. Hybrid beamforming has been shown to be an energy and cost efficient method [24–27]. In this method, different technologies can be selected to trade-off between cost of fabrication, cost of operation (dc energy requirements), heat generation, and power output. While hybrid beamforming techniques are not included in this thesis, the four-element linear array and beamforming networks would work as a sub-array to be used within a hybrid beamforming network.

The work in this thesis is focused on a 4×1 antenna array and associated front-end components. A block diagram of the parts of a phased array is shown in Fig. 1.5. As explained above, this specific solution has two

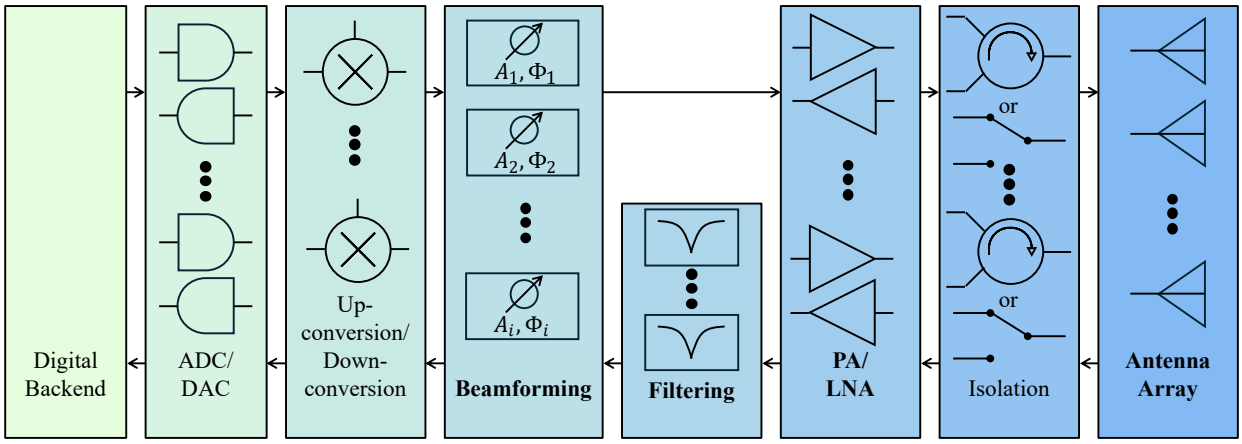


Figure 1.5: An overview of the components of a phased array system front-end for transmit (Tx) and/or receive (Rx). This includes the digital components, the digital-to-analog converter (DAC) and/or analog-to-digital converter (ADC), up- and/or down-conversion, beamforming network including power division for amplitude (A_i) and phase or delay elements (Φ_i), potential filtering on Rx path, amplification as either a power amplifier (PA) or low noise amplifier (LNA), isolation elements if used as a transceiver, and radiating elements in an antenna array. Components presented in this thesis are in bold font.

main advantages over a single antenna system. First, having multiple antenna elements, the darkest blue block on the ride side in Fig. 1.5, i.e the array part of phased array, allows for a higher directivity beam compared to using just one (same sized) element. The phased part of the phased array means that there is a way to adjust the delay or phase of the signal that goes to each element, which allows for beamsteering or adjusting the direction of the beam, done by the teal fourth section from the left section labelled beamforming.

Phased arrays can be used in both transmit and/or receive operation. The transmit (Tx) path can be followed in Fig. 1.5. First, the signal comes from the digital backend before going through a digital-to-analog converter (DAC). It goes through a beamforming network before amplification. If the system can both transmit and receive, next there are an isolation elements on each path before finally going to the antenna array and radiating into space. Similarly the receive (Rx) path can be followed. The signal comes from the right side as the radiated power is received at the antenna array before passing through the previously mentioned isolation elements. Then the signal is amplified by a low noise amplifier before passing through filtering. The received signal passes through a beamforming network before an analog-to-digital converter (ADC) and into the digital backend.

The higher directivity and beamsteering are advantageous in a congested spectrum environment by the

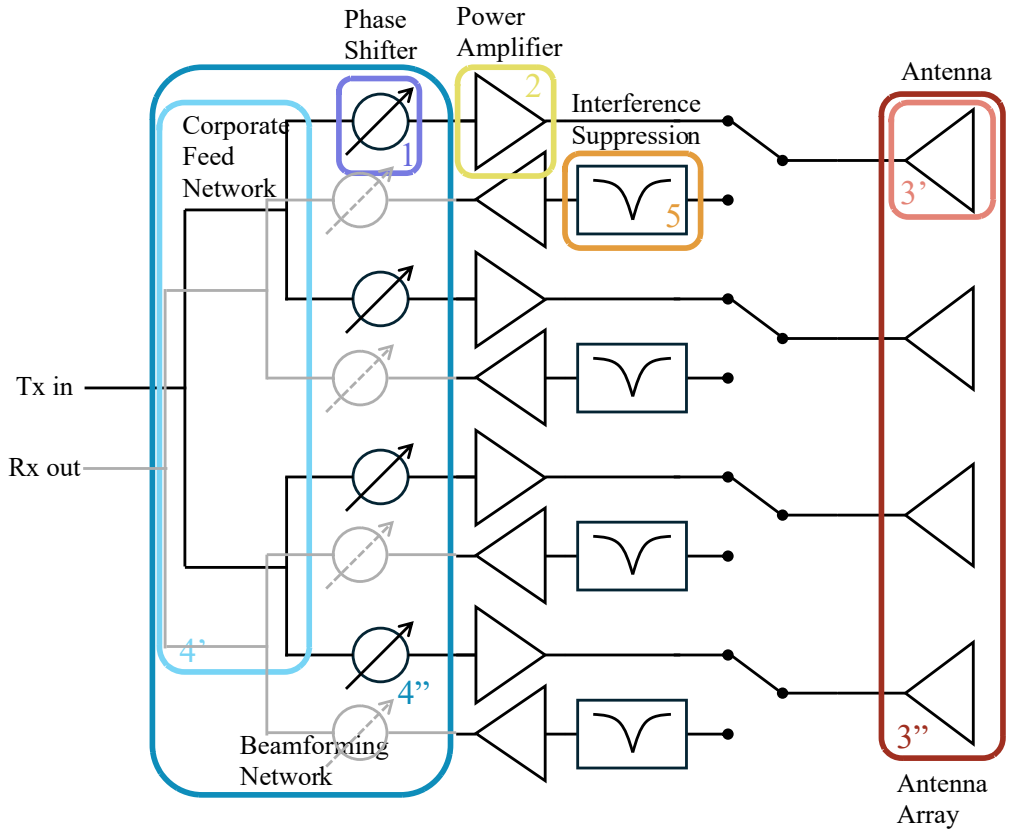


Figure 1.6: A block diagram of an analog front-end for a phased array. Components presented in this thesis include analog phase shifter (1), power amplifier (2), antenna element (3'), antenna array (3"), corporate feed network (4'), beamforming network (4"), and interference suppression circuit (5). The grey path shows the receive path that is identical to the beamforming network for the transmit path.

use of more directed energy transfer which limits interference with other systems by controlling the direction in which the radiated power is transmitted or received. Beamsteering, in addition to frequency tuning, can allow a system to quickly change operation if there are intentional or unintentional interferers or to be reused by different systems to reduce overall SWaP. For jamming applications, phased array architectures mean more power is radiated in the desired direction, a more efficient use of power, and that the desired direction can be changed, increased reconfigurability.

Components that are specifically discussed in this thesis are in bold font in Fig. 1.5. A 4×1 analog front-end is shown in Fig. 1.6. The colored blocks are the components demonstrated in this thesis. These are an analog phase shifter (1), power amplifier (2), antenna element (3'), antenna array (3"), corporate feed network (4'), beamforming network (4"), and active interference suppression circuit (5).

1.4 Outline of Thesis

This thesis focuses on the design and implementation of broadband components for phased arrays, in both transmit and receive. The components presented as a part of this thesis are outlined and numbered in Fig. 1.6.

The chapter organization is as follows:

- Chapter 2: presents a brief introduction to MMIC processes and some processes used in this thesis is included. Next, a broadband GaAs phase shifter is presented including the design, small signal simulations and measurements, and large signal performance compared to a similarly designed GaN phase shifter. Phase shifters, labelled 1 in Fig. 1.6, are an important component in overall beamformers, labelled 4", when combined with corporate feeds, labelled 4'. Another individual MMIC component is also described, a broadband GaN 2 W power amplifier, labelled 2 in Fig. 1.6. The GaN power amplifier is two stages with reactively matched matching networks made of multiple discrete inductors and capacitors for over 33 dBm output power and 35% from 6.5–12.0 GHz.

- Chapter 3: introduces the antenna element and the antenna array, 3' and 3" in Fig. 1.6, respectively. The metal double-ridged 4×1 antenna array is designed for good electromagnetic and thermal performance. Simulations and measurements are both completed. The initial array is also extended in simulation to a 2-D 4×4 version for increased power output.

- Chapter 4: presents two broadband beamforming networks, labelled 4" in Fig. 1.6, that are done in different fabrication processes. Both are 4×4 Butler matrices, a type of multi-beam feed. The first presented is fabricated in HRL's metal embedded chip assembly (MECA) and operates from 6–12 GHz. The second, designed in 3D Glass Solution's Apex glass, operates over 9–13 GHz, is still in fabrication.

- Chapter 5: introduces an on-chip implementation of a Butler matrix beamforming network, again 4" in Fig. 1.6. This GaAs chip operates from 43–45 GHz, a frequency scaling from the previously presented beamformers.

- Chapter 6: continues to focus on beamforming networks, 4" in Fig. 1.6, describing the theory of single

frequency Butler matrix operation before introducing bandwidth considerations. Next, by using the developed theory, a tunable beamformer operating from 40–44 GHz is presented. This includes a broadband GaAs phase shifter separately characterized before implemented with the traditional Butler matrix design.

- Chapter 7: focuses on the effects of interference on the receive side path and the introduction of a interference suppression analog circuit. The theory is presented for this interference suppression chip, labelled 5 in Fig. 1.6, before a 6–12 GHz integrated on-chip GaAs example is detailed.

- Chapter 8: summarizes the thesis and its contributions and highlights future work that can be continued from what is included in this thesis.

Chapter 2

Examples of Front-End MMICs

As introduced in Chapter 1 Fig. 1.5 and Fig. 1.6, an RF front-end is composed of many components. This chapter presents two specific components of the front end implemented as microwave monolithically integrated circuits (MMICs). The first component is part of a beamforming network, an analog phase shifter, number 1 in Fig. 1.6. This would be used with a power divider network to create the entire beamforming network, number 4". The second component is a power amplifier (PA), number 2 in the same figure.

Various technologies are used in front-ends, these two examples are implemented as MMICs. Additional MMICs are shown in later chapters as well as designs done in other technologies. Table 2.1 shows the MMIC processes used in this thesis and some of their properties. These processes include both gallium arsenide (GaAs) and gallium nitride (GaN), which are III-V semiconductors. An important property of a process is the gate length of the transistor, which is inversely proportional to the maximum operating frequency. Shorter gate lengths allow the process to work at higher frequencies, as indicated by f_T, the frequency at which the short circuit current gain goes to 1. The thickness refers to the thickness of the semiconductor substrate. The two modes of operation are depletion mode (D-mode) and enhancement mode (E-mode). Traditional operation is D-mode, where the gate has a negative bias while the drain has a positive bias. Newer processes include some that are E-mode, allowing for single-polarity dc biases, which can simplify setup and integration in a full system. The only process in this thesis that is E-mode is the WIN Semiconductors

	Name	Type	Mode	Thickness	Gate Length	V_d	f_T	ε_r
1	WIN PIH1-10	GaAs	E-mode	4-mil	150nm	4 V	100 GHz	12.9
2	WIN NP15-00	GaN-on-SiC	D-mode	4-mil	150nm	28 V*	34.5 GHz	9.7
3	WIN PP10-20	GaAs	D-mode	2-mil	100nm	4 V	160 GHz	12.9
4	HRL T3	GaN-on-SiC	D-mode	2-mil	40nm	12 V	200 GHz	9.8

Table 2.1: Table of properties of MMIC technologies used for designs in this thesis. *Previous versions of this process had V_d of 20 V.

PIH1-10, process 1. The nominal drain voltages for these processes are listed; this is the highest voltage at which the devices have been verified and modeled. The breakdown voltage is higher than what is listed. Finally, the relative permittivities are listed, with GaAs processes having slightly higher permittivities than GaN processes. The other commonly quoted electric property of substrates, the loss tangent, tanδ, is not listed as it is very small and similar for all cases, between 0.001 and 0.003.

All these processes listed have two available metal layers that can be overlaid to create a single thick metal layer for design purposes. They also feature a backside metal that serves as a ground, with vias to connect the metal layers to the ground layer. Additionally, these processes include materials for building capacitors and resistors. While different active devices may be available depending on the process, the examples in this thesis focus on using pHEMT transistors. An example cross-section from WIN Semiconductors' PIH110 E-mode GaAs process is shown in Fig.,2.1. This cross-section displays three active devices: a PIN diode, a Schottky barrier diode (SBD), and a pHEMT, as well as the cross-sections of a resistor and capacitor. The example illustrates the various layers that make up a MMIC chip, with each color representing a different layer. Notable layers include the metal layers shown in purple and dark green, and the yellow TFR of the resistor and light purple MIM SiN in the capacitor, which are primarily manipulated in the design. The internal features of the pHEMT active components are fixed in terms of transistor finger width and the number of fingers in any of the processes used in this thesis.

Both GaAs and GaN MMIC designs have demonstrated high performance for various applications over the past decades. GaAs is the more mature process of the two. Interest in GaN has increased, as evidenced by federal funding programs such as STARRY NITE and the CHIPS and Science Act [29, 30]. GaAs has many attractive properties, including relatively high power density (compared to silicon), low noise figure,

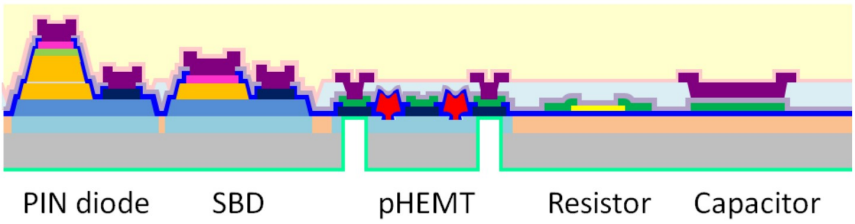


Figure 2.1: Cross section from WIN Semiconductors' PIH1-10 process [28] for various devices and components including the pHEMTs, resistors, and capacitors used in the phase shifter design in this chapter. Different colors represent the layers in this process. The process also has PIN diodes and schottky barrier diodes (SBD) but neither are used in designs in this thesis.

high relative permittivity, low loss, and established models with numerous high-frequency demonstrations, including millimeter-wave applications. GaN also exhibits a low noise figure, high relative permittivity (though lower than GaAs), and low loss. It can outperform GaAs in terms of power density and linearity, but the less mature process means fewer developed models and devices, and less availability [31]. GaN has a bandgap energy of 3.4 eV compared to 1.4 eV for GaAs and 1.1 eV for Si, which allows GaN fto achieve a much higher breakdown voltage compared to other semiconductors. Both listed GaN processes are GaN-on-SiC, which utilizes high thermal conductivity—over six times higher than GaAs—combined with GaN's high bandgap energy. This allows for power densities over five times greater than GaAs and over ten times greater than silicon [31]. This capability enables smaller chips to deliver the same amount of power, as illustrated in Fig. 2.2 taken from [32]. The figure shows a 6 W PA at 30 GHz for both GaAs and GaN: the GaN amplifier is 3.24 mm by 1.74 mm using four-way combining, while the GaAs amplifier is 5.71 mm by 3.86 mm using 32-way combining. This highlights GaN's advantage for high-power applications, such as the power amplifier in this chapter which uses process 2, WIN NP15-10. GaAs remains a high-performing semiconductor substrate, suitable for receive-side applications or circuits preceding PAs in the transmit path, such as the phase shifter in this chapter which is built using process 1, WIN PIH1-10.

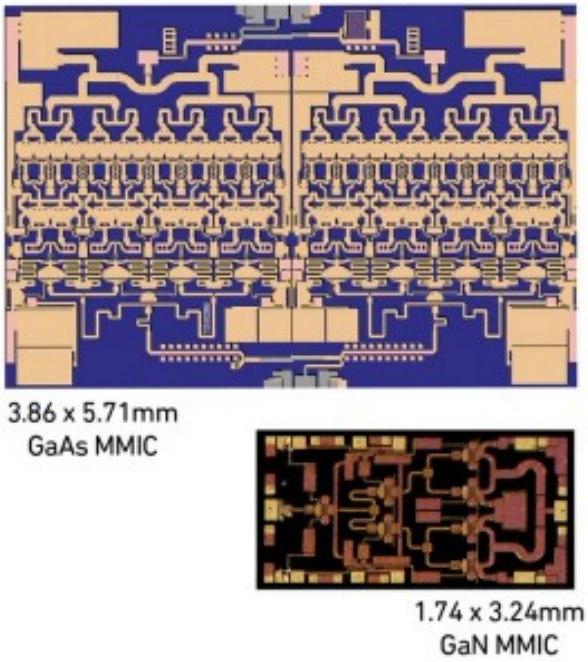


Figure 2.2: Size and complexity comparison of a GaAs and GaN 6 W PA at 30 GHz taken from [32]

2.1 Broadband Phase Shifter

2.1.1 Phase Shifter Introduction

Phase shifters are common components in analog beamformers for phased array antennas, as well as in instrumentation applications such as reflectometers, frequency translators, and phase-noise discriminators [33–37]. Additionally, phase shifters are used in linaerization of amplifiers [38]. Numerous phase shifter architectures have been demonstrated, both digital and continuous, with various bandwidths [39, 40]. Common RF phase shifter topologies are illustrated in Fig. 2.3.

In Fig. 2.3(a), a reflective type phase shifter is depicted. This configuration includes a hybrid coupler with the through and coupled ports terminated by highly reflective loads. These loads can be discrete, as in the top example, where the loads are switched, or continuous, as in the bottom example, where a single tunable load is used. Broadband examples around X-band have been implemented using MEMS [41] and varactors [42, 43]. Other on-chip examples, such as [44] and the phase shifter used in a Butler matrix feed network later in this thesis, also fall into this category. Although these are not true time delay elements, they

can offer broad bandwidth depending on the hybrid coupler's bandwidth. To achieve a greater phase shift, multiple phase shifters can be cascaded, as demonstrated in [43–46].

In Fig. 2.3(b), a loaded line phase shifter topology is shown. This type approximates the transmission line model, typically using series inductors and shunt capacitors. This configuration can be implemented with discrete states, using switched loads, or continuously. Published examples around X-band have employed varactors [47], MEMS [48], and ferroelectrics [49, 50]. Unlike the reflective type, loaded line phase shifters are true time delay elements. Their bandwidth is limited not by phase performance but by matching performance. As the delay changes with reactive elements, the impedance also changes, so perfect matching occurs only at one tuning point. Though with the addition of more tunable elements, the match can also be improved [51].

Finally, Fig. 2.3(c) illustrates switched line phase shifters. These are inherently discrete and feature n bits, leading to 2^n states. The example shown uses physical lengths of transmission lines to achieve true time delay, although reactive elements can also be used to create a constant phase shift across the bandwidth. Bandwidth depends on both the switches used and the delay elements. Published X-band examples include MEMS [52] and MMIC implementations [53–56].

This section presents a broadband GaAs continuous MMIC phase shifter, with its topology shown in Fig. 2.4. It combines the features of the topologies in (a) and (b), leveraging the broadband matching of the hybrid topology and the true time delay performance of the loaded line topology. This GaAs implementation is fabricated using the WIN Semiconductors PIH1-10 process, process 1 from Table 2.1. The following sections will briefly describe the design, followed by simulated and measured results for both small and large signals. Finally, the high power performance will be compared to a similarly designed GaN chip [57].

2.1.2 Phase Shifter Circuit Design

The phase shifters are designed using traditional design methods for both reflective and loaded line topologies, outlined in [58]. A reflective phase shifter's performance is found by analyzing the voltages at each port of the coupler as follows: The incoming and outgoing voltages at each port of a 90° hybrid coupler are

$$V_1^+ = V_0 \tag{2.1a}$$

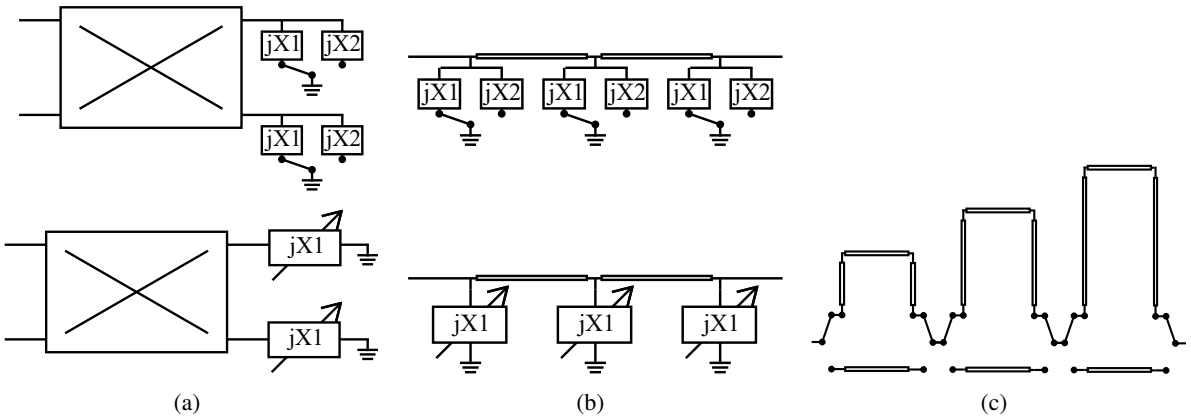


Figure 2.3: Examples of some of the main types of phase shifters that can be implemented on chip using transistors or diodes. (a) Reflective phase shifters can have switched loads (top) or tunable loads (bottom). (b) Loaded line phase shifters also can have discrete (top) or tunable (bottom) components. (c) Switched phase shifters have individual bits that can be switched in or out, often these sections are different length transmission lines as shown but can also be reactive type elements.

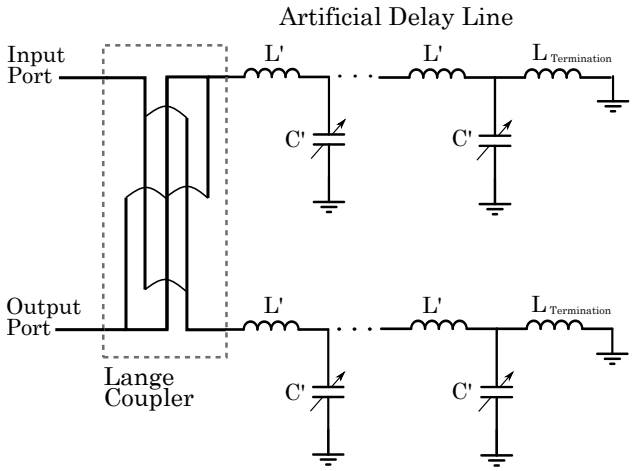


Figure 2.4: Topology of reflective loaded-line continuous broadband phase shifter. The coupled and through ports of the Lange coupler are variable reactances, as in a reflective phase shifter. The variable reactances are implemented with tunable artificial transmission lines that use diode-connected transistors as variable capacitors. The reactive loads are implemented with lumped inductors and a shorted termination.

$$V_2^+ = \Gamma_2 V_2^- \tag{2.1b}$$

$$V_3^+ = \Gamma_3 V_3^- \tag{2.1c}$$

$$V_4^+ = 0 \tag{2.1d}$$

$$V_1^- = \frac{-j}{\sqrt{2}} V_2^+ + \frac{-1}{\sqrt{2}} V_3^+ \tag{2.2a}$$

$$V_2^- = \frac{-j}{\sqrt{2}} \Gamma_2 V_1^+ \tag{2.2b}$$

$$V_3^- = \frac{-j}{\sqrt{2}} \Gamma_3 V_1^+ \tag{2.2c}$$

$$V_4^- = \frac{-1}{\sqrt{2}} V_2^+ + \frac{-j}{\sqrt{2}} V_3^+ \tag{2.2d}$$

Letting the two loads be equal so $Z_{L2} = Z_{L3}$ so $\Gamma_2 = \Gamma_3 = \Gamma$,

$$V_2^- = \frac{-j}{\sqrt{2}} V_0 \tag{2.3a}$$

$$V_2^+ = \Gamma \frac{-j}{\sqrt{2}} V_0 \tag{2.3b}$$

And similarly

$$V_3^- = \frac{-1}{\sqrt{2}} V_0 \tag{2.4a}$$

$$V_3^+ = \Gamma \frac{-1}{\sqrt{2}} V_0 \tag{2.4b}$$

Therefore

$$V_4^- = j\Gamma V_1^+ = |\Gamma| e^{-j\phi} \tag{2.5}$$

In this circuit, the loads are the loaded transmission lines which approximate the lossy transmission line model. For a lossy transmission line, the propagation constant γ is

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.6}$$

and the characteristic impedance is

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.7}$$

The input impedance of lossy transmission line with length l is given as

$$Z_{in}(l) = Z_0 \frac{Z_L + Z_0 \tanh \gamma l}{Z_0 + Z_L \tanh \gamma l} \tag{2.8}$$

For a loaded transmission line, l is the number of sections and R, L, G, C are the values per unit of through inductor and shunt capacitor. In this GaAs implementation, the line is terminated in a short so the impedance at each line becomes

$$Z_{in} = Z_0' \tanh \gamma l \tag{2.9}$$

Therefore, the reflection of each load at the two ports of the coupler is

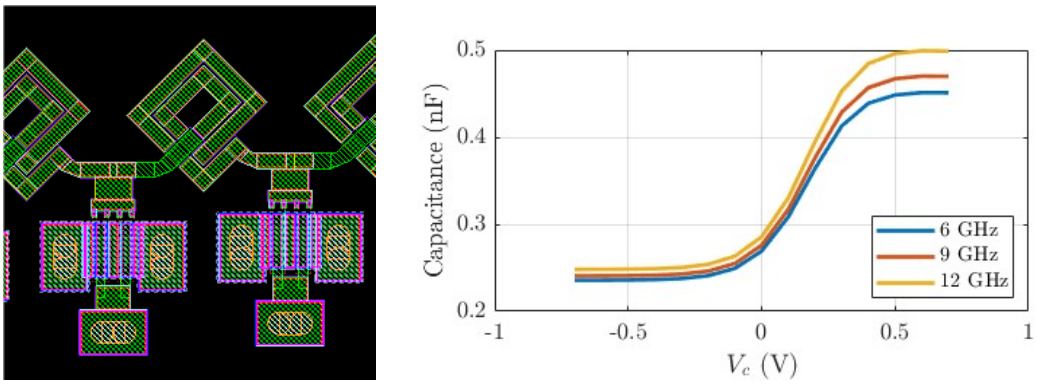
$$\Gamma = \frac{Z_0 - Z_0' \tanh \gamma l}{Z_0 + Z_0' \tanh \gamma l} \tag{2.10}$$

where Z_0 is the impedance of the system and Z_0' is the impedance of the loaded transmission line. Both Z_0' and γ are functions of the inductance and capacitance. In this case, the capacitance is variable and controlled by control voltage V_c so these are a function of f and V_c. If an input of V_0 is placed at port 1, the output at port 4 is given as

$$\tau = j\Gamma V_0 = |\Gamma| e^{-j\Phi} \tag{2.11}$$

which is a scaling and phase shift of the original signal by the loaded line reflection coefficient given in (2.10). The amount of phase shift can be found by analyzing the phase variation in (2.10) as the V_c varies.

With this understanding of how this combined topology operates, the first step is to understand the capacitance and capacitance variation available in the transistor of this process. The WIN Semiconductors PIH1-10 process is a high-frequency process featuring 150μm gate enhancement mode pHEMT transistors. The process includes two metal layers, built-in MEM capacitors, MESA resistors, and vias to ground. In this design, the transistors are used as varactors with a diode connection setup with the source and drain are grounded. The the size and width of the fingers of the transistor are varied and simulated using nonlinear models in Cadence's AWR Microwave Office. Larger peripheries have larger capacitance and capacitance variation but are bulkier and take up more room. Additionally, while the line impedance is not as crucial as in traditional loaded line designs, it is still designed to be around 50 Ω to match the coupler. To keep a characteristic impedance of 50 Ω, as the value of C increases, the value of L must increase. The value



(a) (b)

Figure 2.5: (a) Layout of the 4×75 μm source-drain grounded transistor acting as a varactor and 0.4 nH spiral square inductors that make up the loaded line the GaAs phase shifter. (b) Simulated capacitance over control voltage of the 4×75 μm transistor source-drain grounded transistor at 6, 9, and 12 GHz.

of available inductance is limited by the self resonance of the spiral inductors in the process. Larger spiral inductors, besides being large in size and more difficult to integrate into the circuit, have more capacitance which causes the self resonance to be lower in frequency. At X-band, self resonance limits the inductance to less than about 1.5 nH in this process. Therefore, 4×75 μm transistors are chosen. A section of loaded line including the spiral inductors and the 4×75 μm transistors and the simulated capacitance of a single transistor are shown in Fig. 2.5. The capacitance range varies from 0.241-0.470 pF at 9 GHz for gate bias variations from −0.2 to 0.6 V. The inductors are designed using full-wave simulation to capture the parasitic effects. The final square spiral inductors have inductance values of approximately 0.4 nH. The number of units is varied and the final design is a trade-off in available phase shift, size fitting into the chip area, and resonance within the line structure.

Fig. 2.6 shows a photograph of the fabricated chip, with dc bias, RF input, and RF output labeled. The GaAs phase shifter uses three lumped 0.4-nH inductors and four transistors with the end of the line shorted to ground. The Lange coupler is folded to decrease the length in one direction so it can fit into the chip area. The bends in the Lange coupler increase phase imbalance but this is compensated by the feed and bridge placements. A simple bias tee is added on each loaded line using a large blocking capacitor at the ports of the Lange coupler and a large spiral inductor connected to a single dc bias bad for the control voltage.

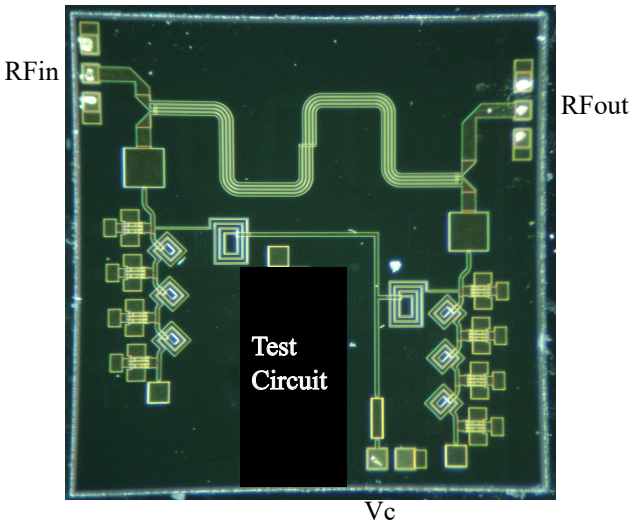
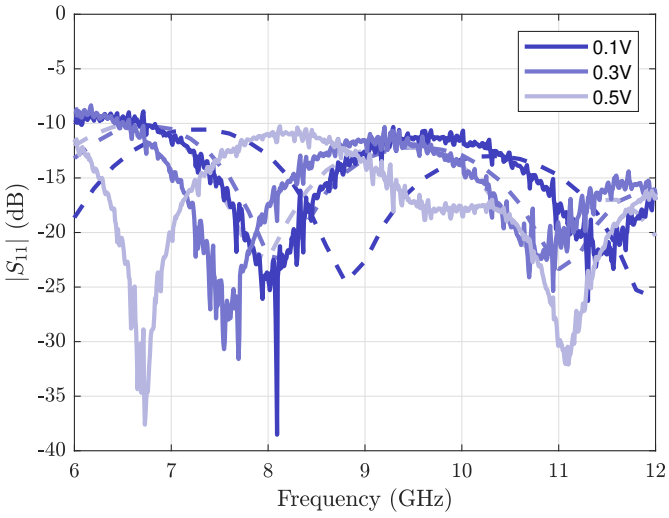


Figure 2.6: Photographs of 2.5 mm×2.5 mm GaAs MMIC chip. The Lange coupler is the hybrid used for the reflective phase shift topology. The loads uses are loaded transmission lines with discrete square inductors and source-drain grounded transistors acting as varactors. A single bias is used for both lines. The effects of bends in the Lange couplers are compensated with electrical length and bridge placement.

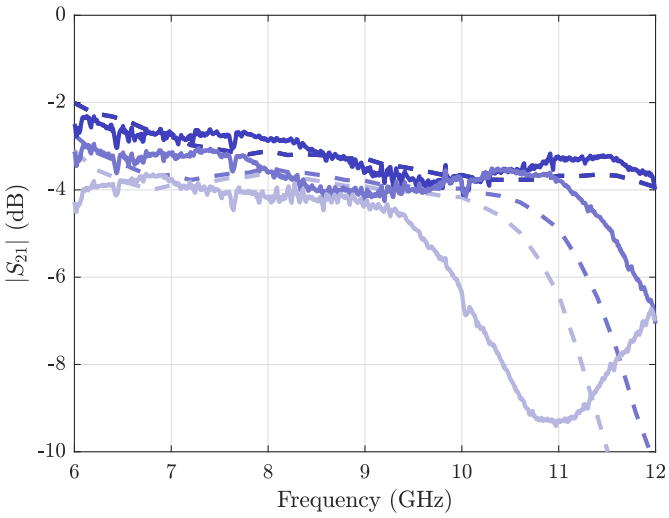
2.1.3 Phase Shifter Small Signal Performance

The fabricated MMIC is measured using a probe station, 150 μm probes, and PNA network analyzer with SOLT calibration standards. The simulated and measured performance of $|S_{11}|$ and $|S_{21}|$ across 6-12 GHz are shown in Fig. 2.7(a) and (b) respectively, for three different control voltages at the edges and middle of the bias range. The match is better than 10 dB due to the Lange coupler. Loss increases slightly with frequency, but the most significant variation occurs with bias voltage. At higher bias voltages, such as 0.5 V, the loss is higher. Near 12 GHz, the loss starts to increase rapidly, which we attribute to a resonance in the electric length of the loaded transmission line, causing frequency-dependent changes for different bias points. The measured and simulated results begin to deviate more closely to this point, but overall behavior is still predicted well.

The phase shift performance, both simulated (dashed) and measured (solid), is shown is Fig. 2.8 as a function of bias voltage and frequency. Overall, the phase shift increases with frequency and bias voltage. The measured performance generally matches simulations, indicating that the nonlinear models accurately predict the capacitance change. However, there is a slight shift down in frequency, and the model begins to deviate from measurements more at higher bias voltages as the transistor starts to turn on. The GaAs circuit

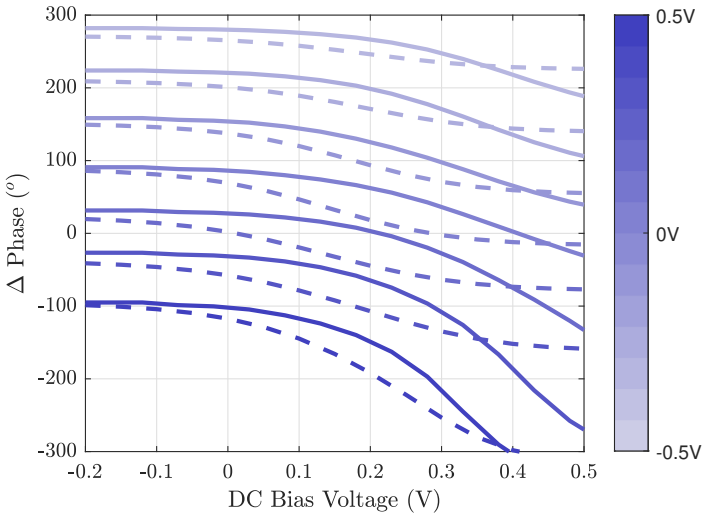


(a)

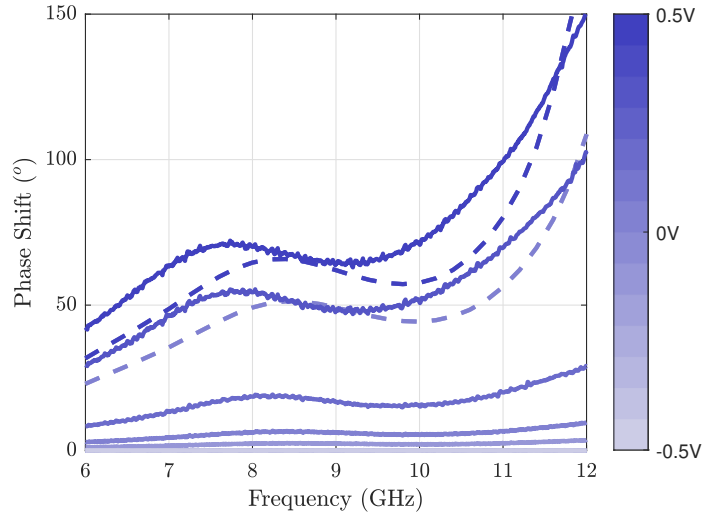


(b)

Figure 2.7: Measured (solid) and simulated (dashed) performance of (a) $|S_{11}|$ and (b) $|S_{21}|$ of the MMIC phase shifter over frequency with various biases.



(a)



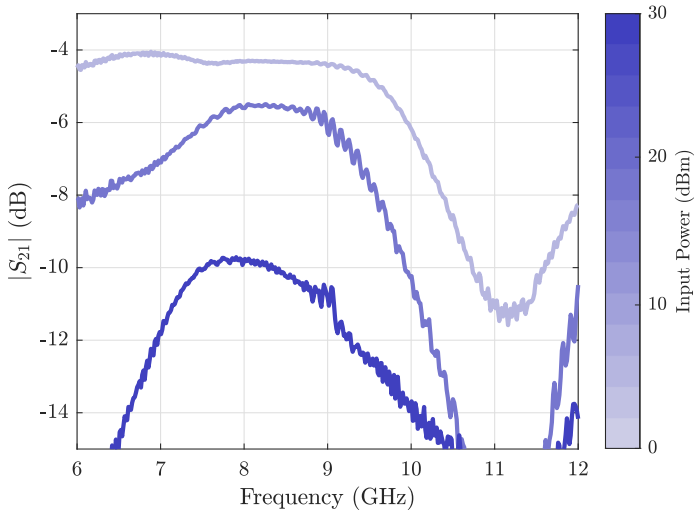
(b)

Figure 2.8: Measured (solid) and simulated (dashed) performance of the phase variation over dc bias voltage at various frequencies and (b) phase shift over frequency for various dc biases.

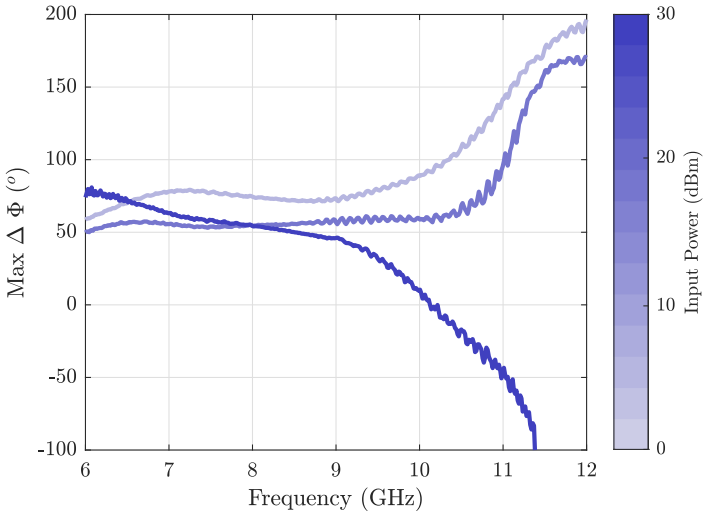
provides 40°-150° of phase variation available depending on the frequency.

2.1.4 Phase Shifter Large Signal Performance

Large signal measurements are also performed using the same probe station and PNA, calibrated with a linear amplifier at the input for increased power. Fig. 2.9(a) shows how the amplitude of $|S_{21}|$ changes as input power increases, and (b) shows how the maximum available phase shift changes with input power. The



(a)



(b)

Figure 2.9: (a) $|S_{21}|$ and (b) maximum available phase shift of the GaAs phase shifter at various RF input power levels. As power increases, loss increases and the available phase shift begins to change from expected performance from small signal measurements.

variations are frequency-dependent, but the general trend indicates increasing loss and a reduction followed by significant variation in the maximum available phase shift at high input power levels. Loss increases to above 15 dB over 10 dBm of input power, and available phase shift drops by about 20°. At very high input powers, performance stabilizes as the first varactor turns fully on and behaves as a lossy short to ground.

Harmonics are quantified and compared to a similarly designed GaN phase shifter [57]. This measurement

uses a CW signal from a signal generator, passes through a linear amplifier before the phase shifter, and is measured on a spectrum analyzer. A coupler and power meter at the chip input enable calibrated power measurements. The results, shown in Fig. 2.10, are for 9 GHz, with each circuit measured at the edges and middle of the bias range. The GaN phase shifter generates similar harmonic levels to the GaAs phase shifter but at about 20 dB higher input power, demonstrating higher power handling. Thus, for transmit arrays with large power requirements, a GaN device may be more appropriate. However, since phase shifters are typically placed before power amplifiers and are inherently lossy, the GaAs phase shifter, with power handling still above 0 dBm, may be sufficient for many applications. Harmonic generation is frequency- and bias-dependent for both MMICs, with the GaN phase shifter generating the same harmonic level at 20 dB higher input power than the GaAs circuit, as expected.

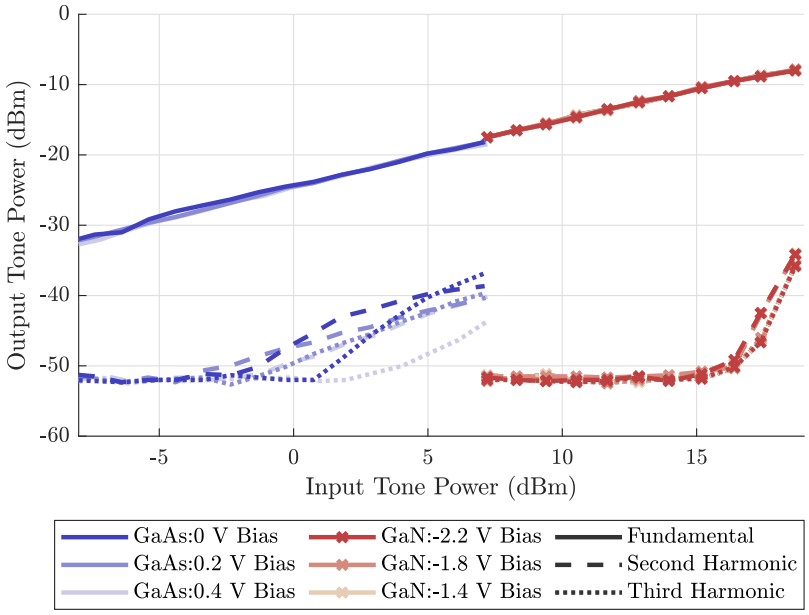


Figure 2.10: Harmonic generation as a function of input power for the GaAs (blue) and GaN (red) phase shifters at 9 GHz from [57]. The power handling of the GaN is about 20 dBm higher than the GaAs when comparing similar levels of harmonic generation.

Table 2.2: Summary of Broadband Phase Shifters at X-band

Ref.	**f_c, GHz**	**FBW, %**	**ΔΦ**	**IL, dB**	**Topology**
[59]	10.2	43	105	3	Reflective
[60]	12	100	120	4	Reflective
[45]	10.25	114	98	9	Reflective dual
[46]	9.75	67	90	3.65	Reflective dual
[50]	10	40	285	11	Loaded Line
[61]	11.5	113	400	8	N/A
[57]	10	40	167	7.4	Reflective
This	**8**	**50**	**71**	**6**	**Reflective**

2.1.5 Phase Shifter Conclusion

A GaAs broadband phase shifter is presented that combines a reflective phase shift topology with a loaded transmission line topology. The phase shift and loss performance are comparable to other published reflective and loaded line phase shifters, as well as to the best commercially available phase shifters, as shown in Table 2.2. Both large and small signal results are presented, showing good agreement between simulations and measurements. As expected, the GaAs phase shifter has lower power handling compared to a similarly designed GaN phase shifter, by about 20 dBm. This circuit can be integrated with a power dividing network for X-band operation, serving as a feed network for a phased array, as shown in 4" of Fig. 1.6 from Chapter 1. To achieve increased phase shift, this phase shifter could be cascaded; it is well-matched, so this should not pose issues. The next active component following a phase shifter in a transmit array is a power amplifier, with an example of one in this frequency range presented next.

2.2 Octave-band 2W MMIC Power Amplifier

Power amplifiers (PAs) are important for any transmit RF front-end. There are many books and journals width in-depth study and discussion on the design and operation of PAs for those interested, i.e. [62], [63]. This section briefly describes a reactively matched, 2-stage PA biased in class-AB. While more complex architectures exist, this example offers broadband operation with competitive efficiency levels.

The fundamental components of a PA include matching networks, bias tees, and the transistors themselves. Initially, the transistors are load-pulled to determine the optimal impedances for output power and efficiency.

Device selection is based on meeting the required specifications. Bias tees are then added to allow dc power to reach the transistors while preventing it from interfering with the RF input or output. They also ensure that the RF signal only travels between the transistor and the RF input or output. These bias tees are often designed and incorporated into the matching networks.

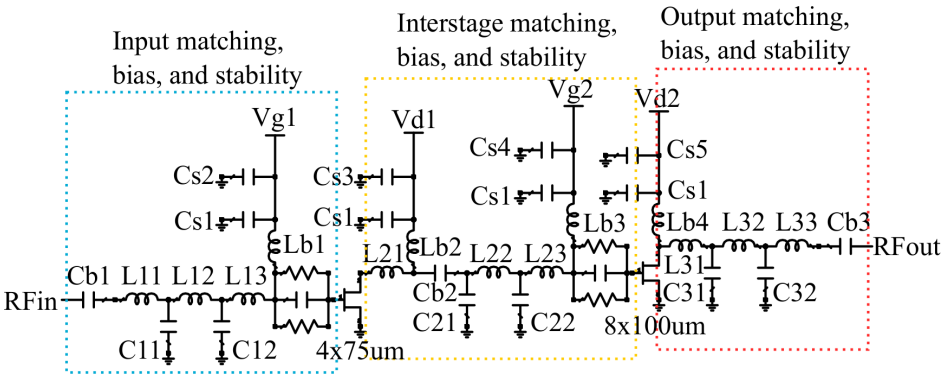
Each transistor requires a matching network to convert its impedance to desired system impedance, usually 50 Ω. The matching network between a transistor and the RF probes transforms the impedance found in load pull to the system impedance. An interstage matching network, which connects multiple transistors, converts complex impedance to complex impedance as determined from load pull. To achieve broadband performance, multi-stage matching networks are employed. Adding additional sections of reactive elements in a pi configuration helps to widen the bandwidth of the matching network [63].

The layout and photo of the fabricated 3.1 mm by 2.4 mm MMIC are shown in Fig. 2.11(a) and (b), respectively. The following sections will cover the design, small signal performance, and simulated and measured large signal performance over the 6—12 GHz octave.

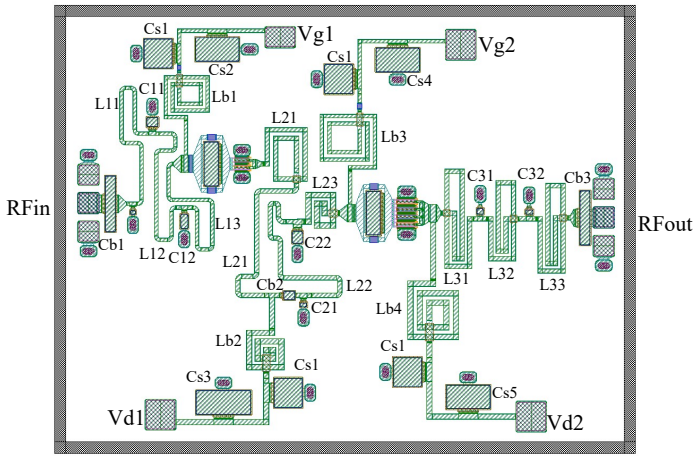
2.2.1 Power Amplifier Design

The PA design and simulation are performed using Cadence AWR Microwave Office and its harmonic balance simulator for nonlinear simulations, with nonlinear models provided by the foundry. The NP15 GaN-on-SiC process, process 2 from Table 2.1 has nominal drain voltage of V_d=28 V. Earlier versions of the process, used during the design phase, had a nominal voltage of V_d=20 V, so this design also operates at V_d=20 V. The process includes two interconnect metal layers, high-reliability MIM capacitors, precision TaN resistors, and through-substrate vias for low inductance ground connections.

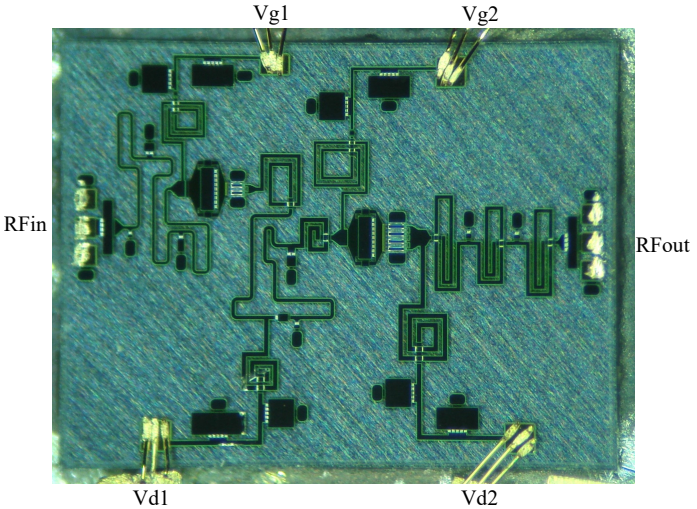
The first step is device selection. The power density of this process is 4 W/mm at 29 GHz. An 8x100 μm device is chosen for the second stage to achieve required output power level of 2 W. The first stage uses a 4x75 μm device which provides sufficient output power and gain to drive the second stage device into compression. Both transistors are biased at 20 V. The I_{ds} in small single operation for the 4×75 μm transistor in stage 1 and the 8×100 μm transistor in stage 2 are set at 23 mA and 61 mA, respectively, class AB bias points, with $V_{g1} = V_{g2} = V_g$=-1.6 V.



(a)



(b)



(c)

Figure 2.11: (a) Circuit diagram, (b) layout, and (c) photograph of the WIN NP15 two stage power amplifier. The chip is 3.1 mm by 2.4 mm.

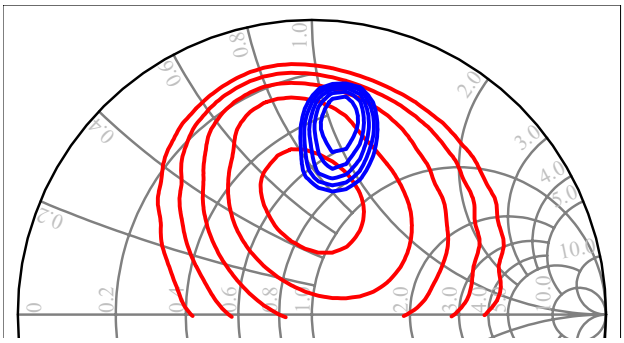


Figure 2.12: Load pull at 9 GHz for the 8×100 μm transistor used for stage 2 for PAE (blue) and P_L (red). PAE contours plotted are from 60-64% and P_L contours plotted are from 32-36 dBm.

The next step is load pull to find the impedance points. The design goal is to maximize PAE across frequency so both maximum PAE points and maximum power is considered. Contours are shown in Fig. 2.12 for the 8×100 μm device which is shown for the second stage where maximum PAE is 64% and maximum P_L is 36 dBm with contours of 1% and 1 dBm are plotted. The PAE contours (blue) are closer together meaning moving away from the PAE impedance point results in PAE dropping off quicker than moving away from the P_L impedance point. This is also done across frequency from 6-12 GHz, Fig. 2.13 shows the maximum PAE and maximum P_L points for both the 4×75 μm device for stage 1 and the 8×100 μm device for stage 2. The maximum PAE and maximum P_L impedance points move counterclockwise around the Smith chart, while passive elements move clockwise. This is one of the challenges of broadband PA design. The maximum delivered power of the transistors for stage 1 and stage 2 is 31.5 dBm and 36.0 dBm, above what is needed for 2 W or 33 dBm output, the design impedances chosen are close to the maximum PAE points (solid lines). The maximum values for PAE are 64% and 66% for the transistors for stage 1 and stage 2 respectively. With real components, there is loss so these values will not be achieved at a single frequency let alone across an octave of bandwidth.

Biasing and stabilization are crucial aspects of PA design. Bias tees are designed to stabilize the circuit and provide dc bias. Large capacitors are placed near the RF input and output ports for dc blocking. These capacitors do not significantly impact in-band impedances and are tuned out during optimization. A capacitor in series is built into the interstage matching network as a dc block. Large inductors are added to each bias line, as shown in Fig 2.14(a), followed by two capacitors to ground. The size and placement of

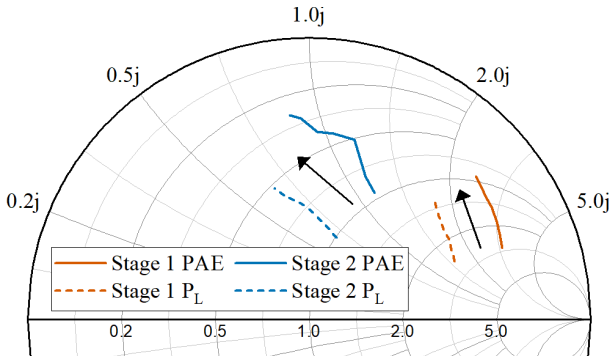
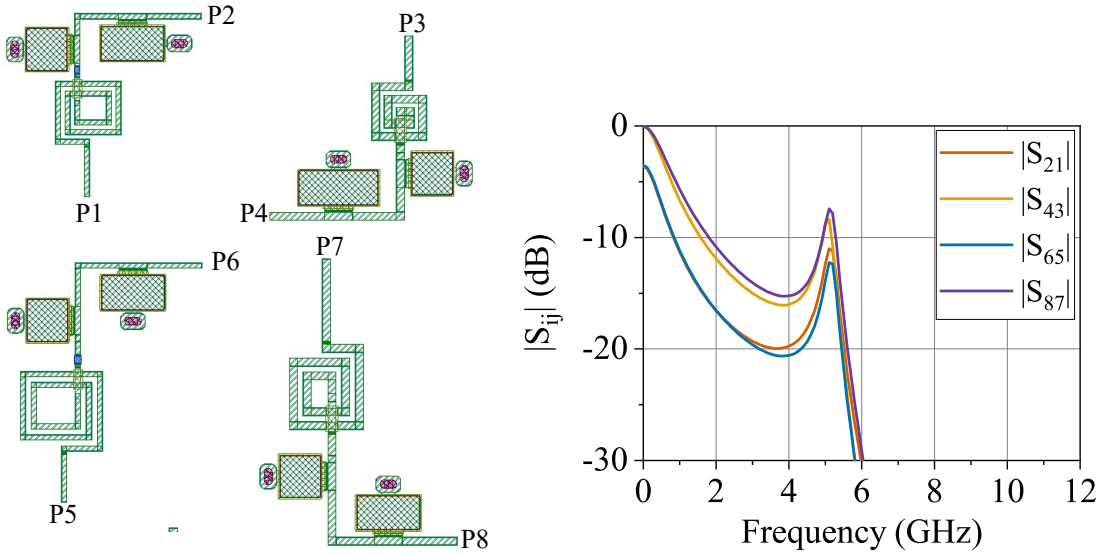


Figure 2.13: Load pull is done on multiple devices across the 6-12 GHz. The desired impedances for maximum PAE (solid) and maximum delivered power, P_L (dashed) are shown for the 4×75 μm device used in stage 1 (red) and the 8×100 μm used in stage 2 of the final design. The arrows denote the direction across frequency, counterclockwise.

these inductors are varied as they are part of the impedance matching networks, which required full-wave simulations to capture coupling effects accurately. The first capacitors after the inductors are identical in size and designed to RF-short to ground as part of the matching network. The second capacitor slightly varies in each line, which helps ensure all RF frequencies are shorted to ground and avoids unexpected resonances. On the gate bias lines (P1/P2 and P5/P6), a 50 Ω resistor is added in series to further stabilize the circuit. These resistors are placed on the gate side to reduce loss and heat generation compared to placing them on the drain side. The S-parameter response from dc through the band is shown in Fig. 2.14(b). At dc, good transmission is observed, while in-band (above 6 GHz), there is minimal transmission, indicating effective bias tee performance.

To further stabilize the devices, an RC network is added at the input of both transistors. This network introduces a small amount of loss in-band, as the capacitor behaves like a short. At lower frequencies, where the capacitor behaves more like an open, additional loss is introduced through the resistive path, helping stabilize the circuit. Resistors are placed on both sides of the capacitor for symmetry, ensuring even current distribution across the transistor's fingers. Nyquist stability analysis is performed in Cadence AWR Microwave Office from dc to 60 GHz on the input and output of each transistor, as shown in Fig. 2.15. The analysis confirms that -1 is not encircled, indicating that the circuit meets stabilization criteria.

Reactive matching with discrete elements is used to achieve octave bandwidth. Each matching network incorporates multiple inductors and capacitors in a pi configuration. For the output matching network, ideal



(a) (b)

Figure 2.14: (a) Layout with ports labelled on all four bias tees used in the design. (b) S-parameter performance across frequency for all four bias tees showing good transmission at dc and little transmission at higher frequencies. Bias tees 1 and 3 have more loss at dc due to the resister in series on the gate bias lines.

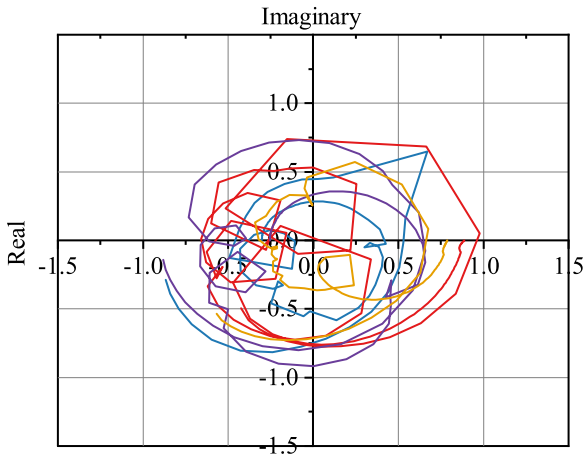


Figure 2.15: Sweep of Nyquist stability at the input and output of each device sweep using Cadence AWR Microwave Office from dc to 60 GHz. At no point is -1 encircled, showing stability.

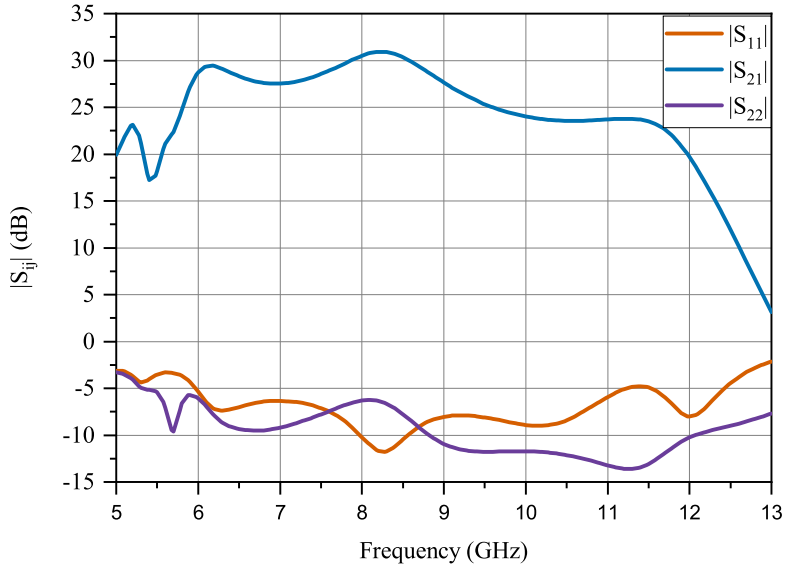


Figure 2.16: Simulated small signal performance of the 2 W PA for V_d=20 V and V_g=-1.6 V.

elements are first used to match the 50 Ω RF output port to the desired impedance found from load pull for the 8x100 μm transistors. Once ideal values are determined of the three series inductors, one shunt inductor, and two shunt capacitors, these are converted to real components. The spiral square inductors' values are found using full-wave simulations to ensure their self-resonance is well above the operating band, limiting the size of available inductance. Capacitors and connecting transmission lines are initially modeled using PDK elements. These are then one by one added to full-wave simulations. As each element is added, component values are tuned to match the performance of ideal elements closely. This process is repeated for the interstage and input matching networks. For these networks, smaller inductor values are achieved using thin lines as inductors, as shown in Fig. 2.11(b) and (c). Again, the inductance is found using full-wave simulation. These lines also help fit the final design into the 3.1 mm by 2.4 mm chip size and minimize unused space.

Simulated small signal performance is shown in Fig. 2.16 for a bias of V_d=20 V and V_g=-1.6 V which corresponds to I_{ds1}=23 mA and I_{ds2}=61 mA. Across 6-12 GHz, $|S_{21}|$ reamins above 20 dB with both $|S_{11}|$ and $|S_{22}$ below -6 dB. Small signal gain peaks around 8.5 GHz at 30 dB.

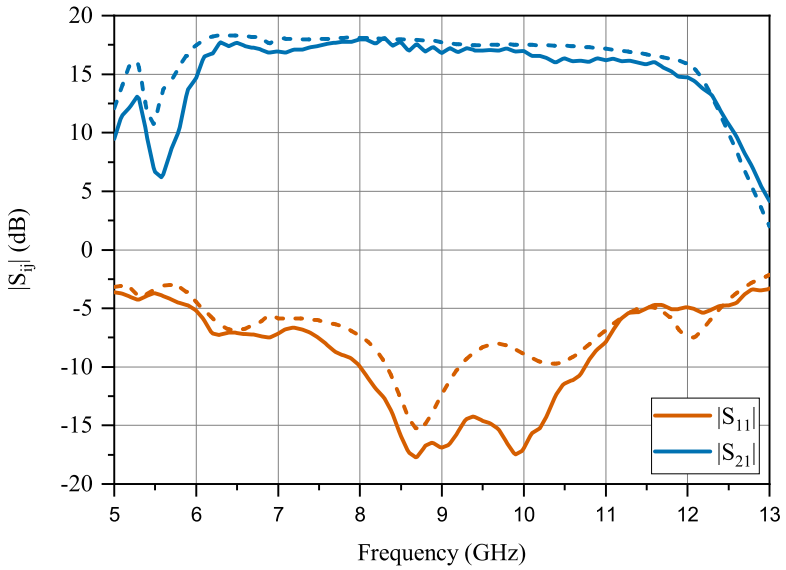


Figure 2.17: Simulated (dashed) and measured (solid) large signal S parameters of the 2 W PA with P_{in}=16 dBm biased at V_d=20 V and V_g=-1.6 V.

2.2.2 Measured Large Signal Results

The PA is mounted on a copper-molybdenum (CuMo) substrate, with additional single-layer capacitors bonded to the dc pads for low-frequency stabilization. Measurements are conducted on-chip, starting with a spectrum analyzer to verify chip stability, followed by using an Agilent PNA for both small signal and large signal measurements. The measurements are performed on a probe station using Cascade ACP50 150 μm probes, with calibration done using on-wafer SOLT (Short-Open-Load-Thru) standards.

Large signal measurements are taken across frequency and power levels. The large signal S-parameter measurements, shown in Fig. 2.17, reveal a slight frequency shift compared to simulations, although the shapes of the measured and simulated results are closely aligned. The measured $|S_{21}|$ has an approximately a 1 dB decrease, remaining above 16 dB from 6.5 to 11.5 GHz and above 14.7 dB from 6 to 12 GHz. Additionally, $|S_{11}|$ is below -4.8 dB from 6-12 GHz, showing slight degradation from simulations.

PAE and output power, P_{out} are also measured. Fig. 2.18 presents the simulated (dashed) and measured (solid) performance at various frequencies from 6 GHz to 12 GHz against output power for PAE (blue

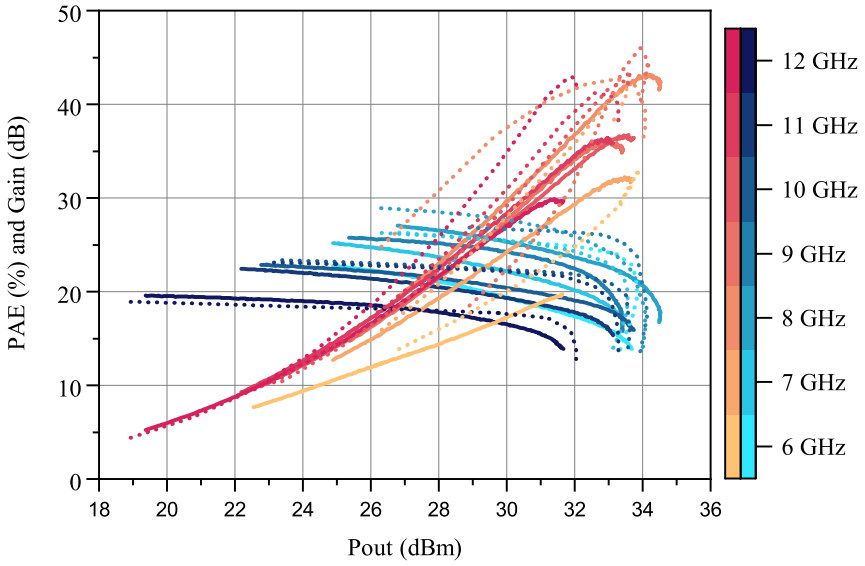


Figure 2.18: Simulated (dashed) and measured (solid) drive up curves for PAE (blue gradient) and gain (red gradient) for 6-12 GHz with V_d=20 V and V_g=-1.6 V.

gradient) and P_{out} (red gradient). Generally, the measured PAE is lower than the simulated values, and the gain decreases, particularly at lower frequencies. This discrepancy is partly attributed to the frequency shift observed in the large signal S-parameter measurements.

Fig. 2.19 compares the simulated and measured performance across frequencies at an input power of 16 dBm, with a bias point set at V_d=20 V and V_g=-1.6 V. The measured data show that the gain, P_{out}, and PAE shapes across frequency closely match the simulated results. However, the measured PAE decreases from around 40% to approximately 35% compared to simulations. The PA performance peaks just above 6 GHz and extends beyond 12 GHz. The measured PAE peaks at 41% around 8 GHz, , across 6.5-12 GHz, PAE varies from 30-41%. For above 6.5 GHz, the measured gain varies from 14.0-16.7 dB and the measured P_{out} exceeds 33 dBm.

Table 2.3 lists similar PAs, including the commercially available TGA2598 from Qorvo. While this PA compares favorably in frequency range and power level, it has slightly lower power and PAE compared to some alternatives but offers broader bandwidth. Given its stable performance at these frequencies, off-chip combining is a viable option for creating a higher power PA with good PAE and broadband performance.

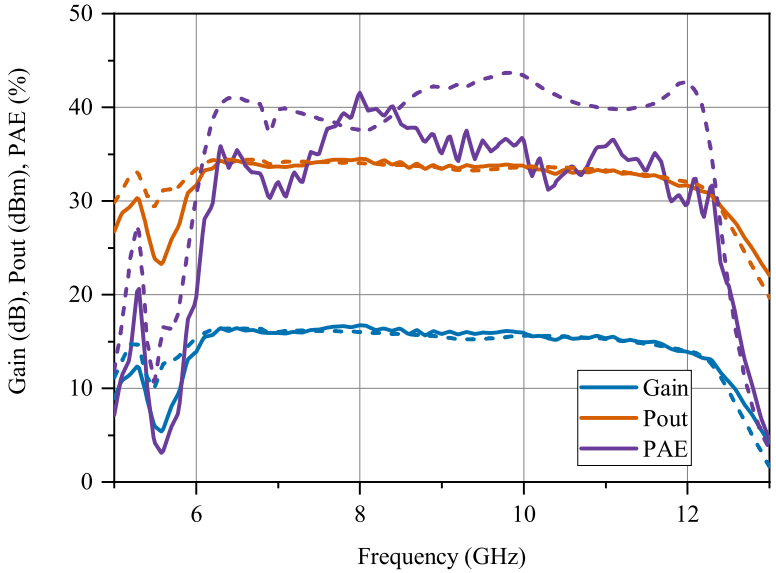


Figure 2.19: Simulated (dashed) and measured (solid) gain (blue), P_{out} (red), and PAE (purple) with input power P_{in}=16 dBm. Gain and P_{out} closely match while there is a drop in measured PAE.

Additionally, this PA could serve effectively as a driver PA for higher power PAs in a transmit system.

Ref.	Technology	Frequency (GHz)	$\|S_{11}\|$ (dB)	PAE (%)	P_{out} (dBm)
[64]	AlGaAs	8.5–11.5	<-13	45	35
[65]	GaAs	7.5–11.2	<-6	44	36.5
[66]	GaN	8–12	<-10	45	40
[67]	GaN	6–12	<-9	31	33
This	**GaN**	**6.5–12.0**	**<-5**	**30–41**	**33**

Table 2.3: Comparison of this PA to other published or commercially available MMIC PAs with similar power levels and frequency range.

2.3 Conclusions

This chapter presents two examples of MMICs suitable for use in an RF front-end, both designed for broadband operation around the X-band. The next chapter will focus on an X-band broadband antenna array specifically designed for transmission. This array design will enable the integration of active components, such as the ones discussed here, with thermal results provided for a 2 W PA similar to the device discussed

in this chapter. The phase shifter is published in [57].

Chapter 3

Broadband Ridged Horn Antenna Array

3.1 Introduction

The previous chapter introduced two components that can be used in a front-end: phase shifters and power amplifiers (PAs). These components can be combined with others into a front-end system. In addition to these active components, antennas and antenna arrays, parts 3' and 3" in Fig. 1.6, are crucial for the system's performance, especially when aiming for broadband operation. The focus of this chapter is on the design and implementation of a broadband antenna array, specifically one that operates across 6–12 GHz.

To achieve effective broadband performance, both the active components and the antenna array must be designed to handle a wide frequency range. For antenna arrays covering octave bandwidths, considerations include element spacing at the highest frequency and managing inter-element coupling at lower frequencies [68]. This chapter examines these trade-offs using the example of a 6-12 GHz array composed of small ridged waveguide horns with dielectric lenses, as depicted in Fig. 3.1. The array is intended to work with 2–20 W GaN MMIC power amplifiers (PAs) for spatial power combining in the far field, and is designed to provide effective thermal dissipation.

Broadband arrays have been constructed with various types of antennas. Tapered slot antennas, for instance, are designed for bands such as 3–12 GHz and 8–20 GHz [69], 2-18 GHz [70], and 5–10 GHz [71].

These printed dielectric antennas, while effective, often lack the capability to accommodate heat-dissipating elements like power amplifiers. An all-metal thinned Vivaldi antenna array, offering improved thermal properties and beam steering capabilities, operates from 10-35 GHz [72]. Other examples include metal waveguide and horn-based arrays, such as open-ended waveguide antennas covering 3.5-6.5 GHz [73], horn antennas spanning 8–12 GHz [74] and 4–8 GHz [71]. Demonstrated double-ridged waveguide horn arrays include a 6-18 GHz array [75], as well as Rotman lens fed arrays, e.g. a 6-12 GHz array [76], and a 3D printed array with up to up to 30° beam steering [77].

Active transmit antenna arrays are often thermally limited. Different methods to manage the heat dissipated by the power amplifiers have been explored, limited to narrowband radiators. These include placing heat sinks in the antenna [78], and different cooling systems [79], [80], [81]. Integrating a heat sink into the antenna design is shown in a 25-31 GHz dipole array feeding aluminum horn reflectors [82]. Narrowband antennas in the 2 GHz range shaped as heat sinks are demonstrated in [83] and [84], showing improvement in antenna efficiency. An interesting fractal shaped antenna which increases the surface area for radiative heat dissipation is discussed in [85].

This chapter presents a broadband antenna array with effective thermal properties, as illustrated in Fig. 3.1. The input SMA connector feeds a 3-section microstrip Wilkinson divider corporate network which can incorporate broadband MMIC phase shifters the phase shifter from the previous chapter [86] and power amplifiers, e.g. [67] or the PA from the previous chapter. The array acts as a heat sink for power amplifiers, with the possibility of additional cooling, e.g. with liquid-filled channels. The heat-sinking properties are demonstrated through thermal simulations and measurements. Octave-band microstrip-to-ridge waveguide transitions [87] connect to linearly-polarized horn antenna elements. Each waveguide flares in the E-field direction with a tapered ridge to form a square aperture horn. The horn elements are tightly packed with 1 λ_0 spacing from center to center at the upper edge of the band (12 GHz). To increase the gain and improve the match at the lower end of the band, dielectric lenses with tapered matching sections are inserted in the horn elements as in [88]. The perforations in the dielectric lens control the average relative permittivity and do not affect thermal dissipation significantly. The chapter is organized as follows: Section 3.2 describes the antenna element, feed and array design; Section 3.3 contains the measured performance of the linear array,

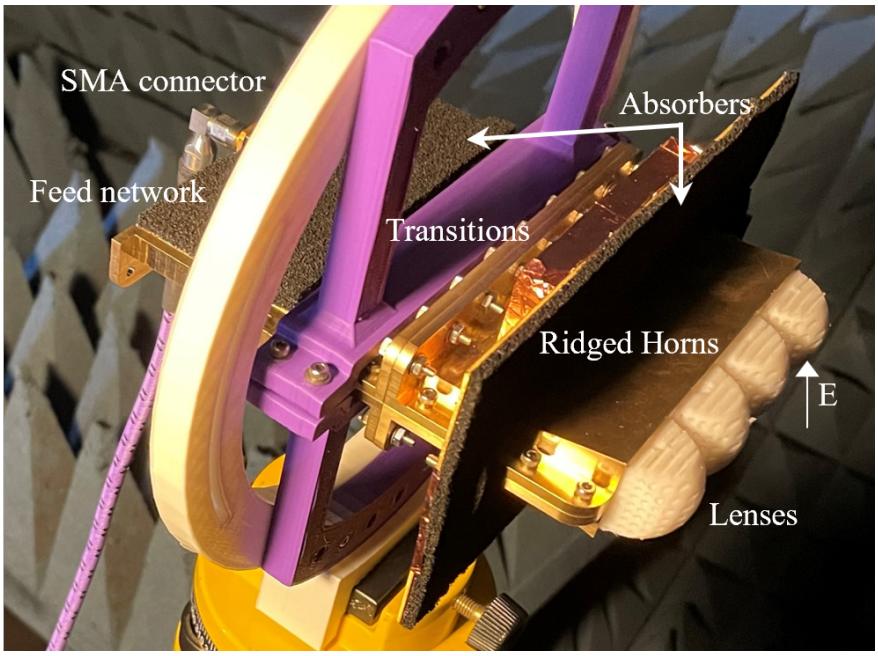


Figure 3.1: Double-ridge horn antenna array with waveguide-to-microstrip transitions from a broadband Wilkinson divider feed. The absorber on the reflector and microstrip-to-waveguide transitions limits back radiation. Each of the 4 ridged horn antennas are filled with a perforated dielectric lens.

including element coupling and radiation patterns; and Section 3.4 discusses thermal performance of the array assuming MMIC power amplifier heat sources; and Section 3.5 explores extending the 1-D array into a 2-D array.

3.2 Feed Network and Array Performance

The antenna element, labeled 3' in Fig. 1.6, is the same as the one described in [88] but with a different lens made of PTFE machined with holes to lower the dielectric constant. The aperture is a square with sides of 21.27 mm. The corporate feed network, component 4' in Fig. 1.6, is implemented with 3 two-way Wilkinson dividers fabricated on Rogers TMM6 substrate and designed to operate over 6-12 GHz [89]. The measured performance using a coaxial calibration is shown in Fig. 3.2, showing an insertion loss that ranges from 0.5-3 dB over the octave bandwidth. The return loss and isolation are better than 13 and 15 dB, respectively.

The antenna is fabricated from brass using split-block machining and in several modules connected with flanges, shown in Fig. 3.1. The measured and simulated reflection coefficients of the four elements when the

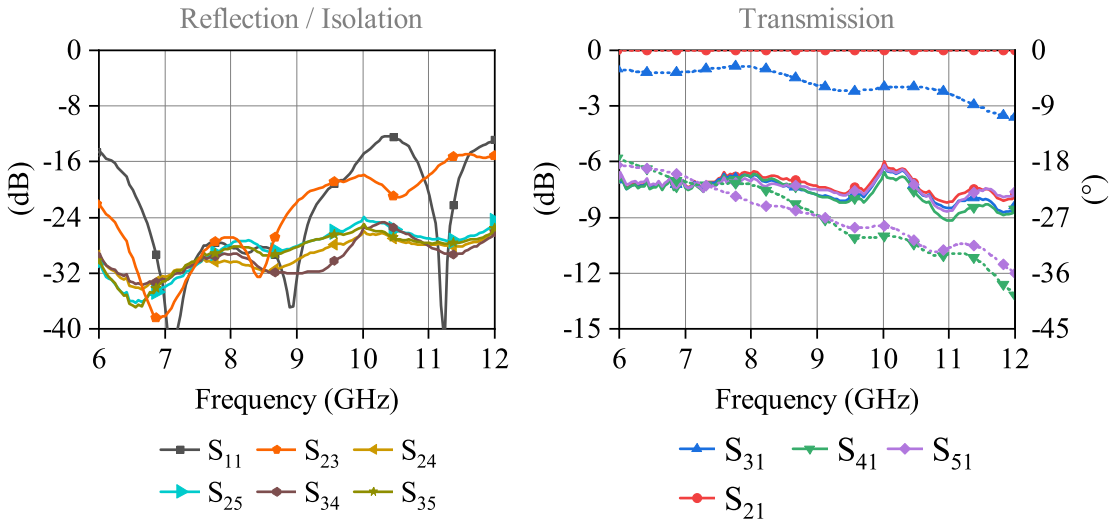


Figure 3.2: Measured S parameters of the 6-12 GHz Wilkinson divider feed network with four 50Ω microstrip output ports. The outer element ports are 2 and 5. Left: magnitudes of reflection and isolation parameters. Right: magnitude and phase of the transmission.

others are matched are shown in Fig. 3.3 and are below 8 dB across the octave bandwidth.

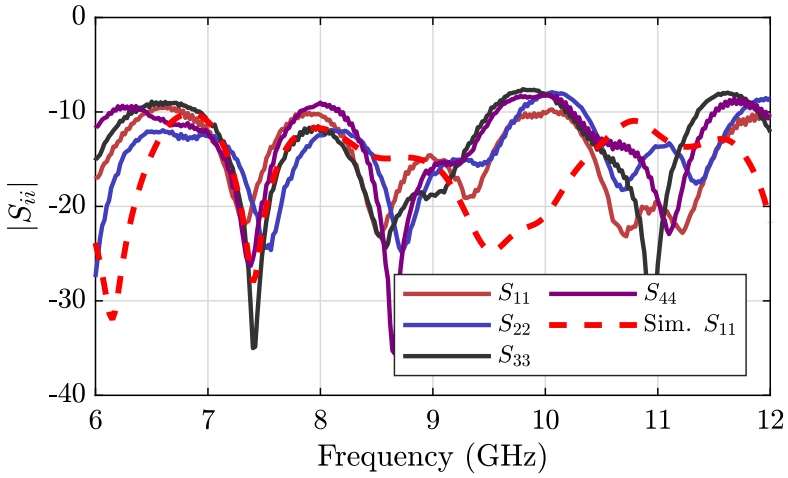


Figure 3.3: Measured and simulated reflection coefficient at the microstrip input of each antenna array element feed, with the other ports terminated.

The Wilkinson feed network is connected to an array of four microstrip-to-waveguide transitions and horns. The measured and simulated reflection coefficient magnitude at the input port of the feed network is shown in Fig. 3.4. While the feed network and antennas are individually well matched, we notice some degradation around 10 GHz. At this frequency, the simulated impedance at the horn feed port is 69.5+j8.5 Ω,

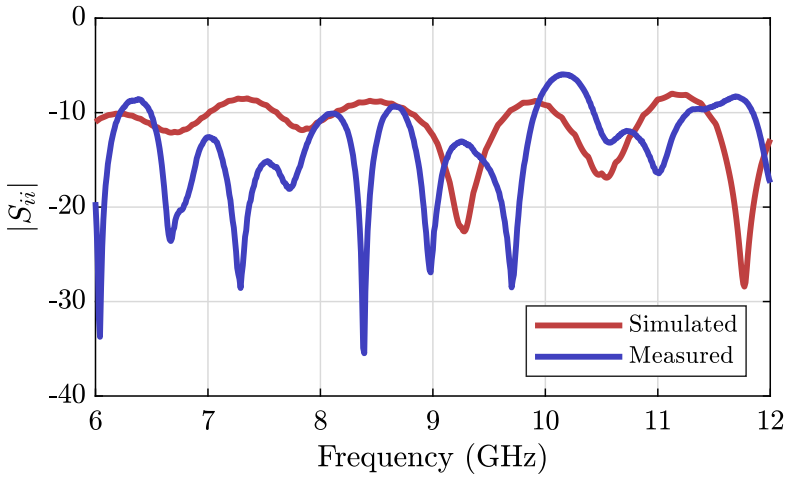
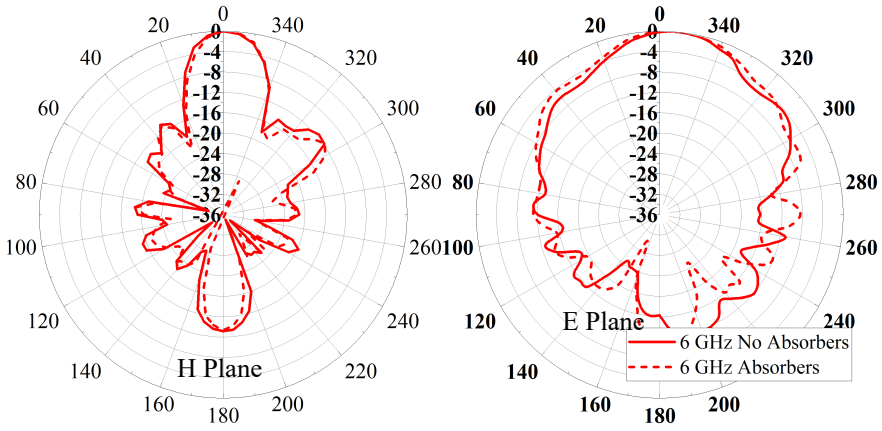


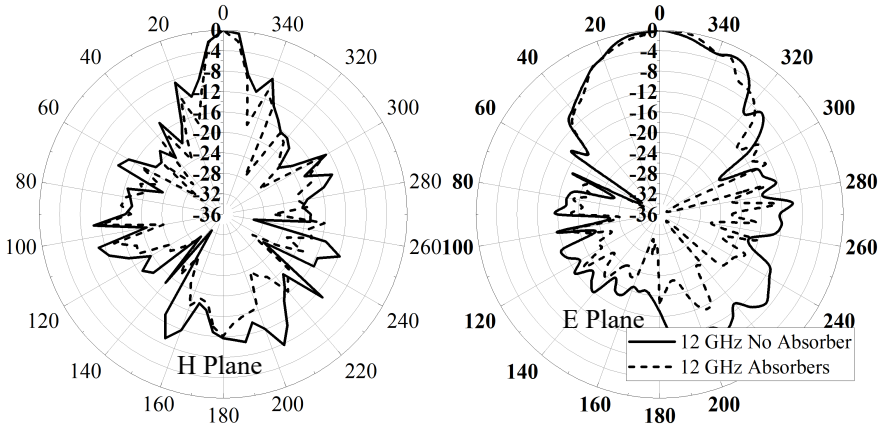
Figure 3.4: Measured and simulated $|S_{11}|$. The match is degraded around 10 GHz due to interaction between the Wilkinson divider and the antenna. Individually, each antenna port and all the Wilkinson ports are well matched.

while the measured impedance is 26.5+10 Ω most likely due to fabrication imperfections of the dielectric insert used for matching. Since the impedance at the output of the feed network is 43+j4 Ω, a mismatch of approximately $|S_{11}| = -6.1$ dB occurs and can be corrected with improved fabrication.

The transition between the microstrip and the double ridged waveguide in [87] is well matched and broadband, with reported radiation at the waveguide opening ranging from 5-25% of the total power across the 6-12 GHz bandwidth. This contributes to back radiation in the array which is mitigated by adding absorbers behind the transition area and the reflector plane. Absorbers do affect the radiation pattern in the comparison at the edges of the band, shown in Fig. 3.5. Notice that the main beam is narrowed and the back radiation reduced, especially at the lower frequencies. The remaining back radiation is due to the cable feed. black. The radiation efficiency before and after placing the absorbers is simulated in HFSS. Across the band, a 10-29 percentage point drop in overall radiation is observed, with a general increase as frequency increased. This radiation efficiency compared incident power to radiated power around the entire antenna so took into account matching and material losses as well as back radiation. As shown in Fig. 3.5(b), there is noticeable reduction in back radiation which contributes to this larger drop in total radiation efficiency. The simulated and measured gain are shown in Fig. 3.6, showing a variation of 6.1 dBi to 12.9 dBi, with a general increase across the band.



(a)



(b)

Figure 3.5: Measured array radiation pattern without absorbers (solid) and with absorbers (dashed) H- and E-plane at (a) 6 GHz and (b) 12 GHz. Absorbers narrowed the main beam in the E plane.

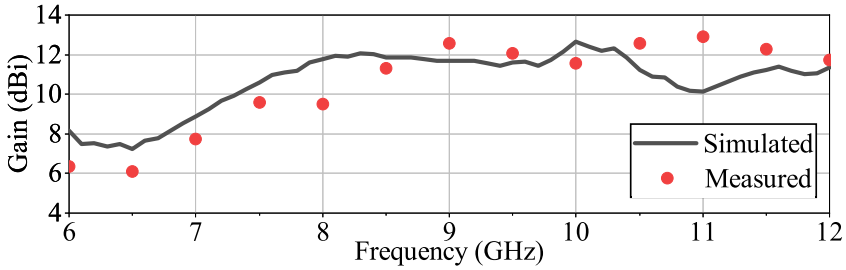


Figure 3.6: Simulated and measured array gain across the band. The measurement is performed in an anechoic chamber and calibrated using the three-antenna method [90].

Measured and simulated radiation patterns at broadside with absorbers are shown in Fig. 3.7 for three frequencies: 6, 9 and 12 GHz. Overall, there is good agreement between simulated and measured perfor-

Table 3.1: Ideally excited array main performance parameters

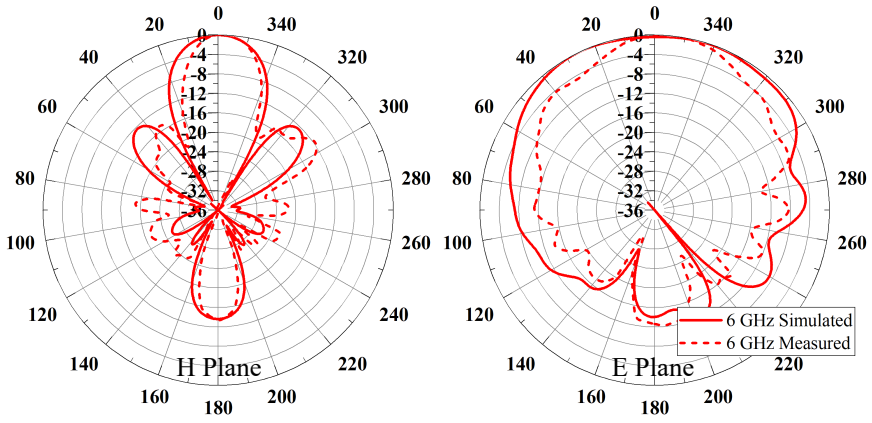
Frequency	6 GHz		9 GHz		12 GHz	
PPS (°)	0	−60	0	−60	0	−60
HPBW (°)	26	26	17	16	13	13
SLL (dB)	−14.2	−12.6	−15.5	−11.2	−12.9	−9
F/B (dB)	10	10	14.6	15.5	18	18.7

mance. (Note that the dashed line in Fig. 3.7c corresponds to that in Fig. 3.5b.) There are some differences in the back radiation due to the cable feed. The H-plane radiation patterns are nearly symmetric as expected, with some minor discrepancies attributed to manufacturing differences in the brass structure and the lenses. The asymmetry in the E-plane patterns is due to the microstrip-to-waveguide transition.

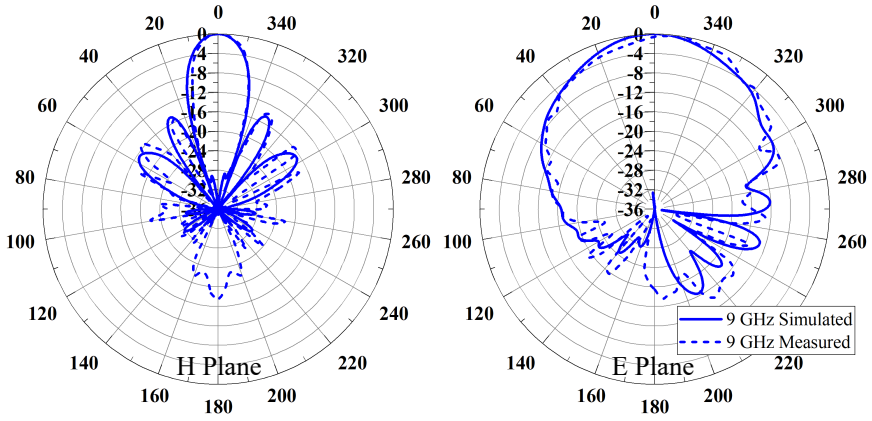
Simulations of this passive array if used as a phased array in 1 GHz steps across the 6-12 GHz band are shown in Fig. 3.8. The simulations are done by exciting microstrip ports at each antenna input in the full-wave model. The steering angle as a function of progressive phase shift and the corresponding gain at that steering angle shows less steering at higher frequencies, with increased gain, as expected. Table 3.1 shows the progressive phase shift (PPS), half-power beamwidth (HPBW), sidelobe level (SLL) and front-to-back (F/B) ratio with the array excited uniformly at 6, 9 and 12 GHz.

3.3 Thermal Performance

The brass ridged horn antenna approach in this paper is specifically chosen to provide thermal dissipation. The performance of the antenna structure as a heat sink is explored using Ansys Icepak. The steady state thermal solution is found by placing a thermal source the size of a Qorvo TGA2598 2-W GaN MMIC amplifier [67] between the Wilkinson divider and the transition to waveguide, Fig. 3.9. This PA is similar in power and bandwidth as the PA presented in Chapter 2. The TGA2598 is on Qorvo's 0.25 μm GaN-on-SiC process, QGaN25. It covers the octave 6-12 GHz with 33 dB of output power and over 31% PAE at a drain voltage of 25 V. This model is chosen as Qorvo provided X-parameters which allowed for in-depth simulations for various power levels using Cadence's AWR Microwave Office so that over-the-air measurements could be compared to simulations as done in [91].



(a)



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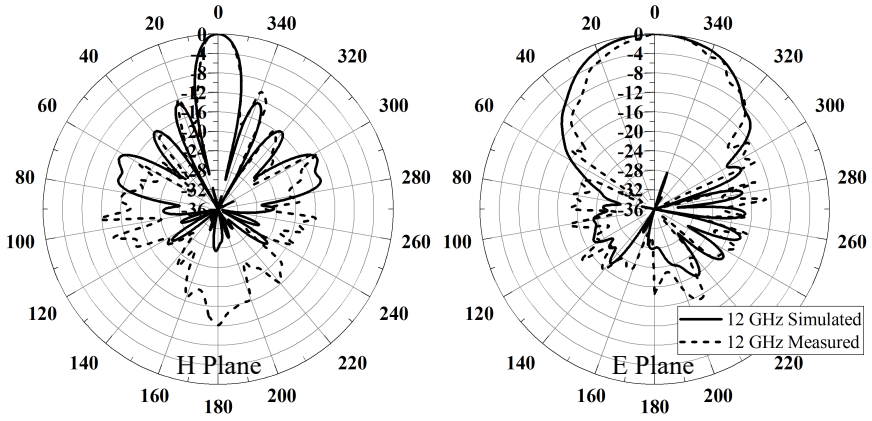


(c)

Figure 3.7: Simulated (solid) and measured (dashed) H- and E-plane array radiation patterns at (a) 6 GHz, (b) 9 GHz, and (c) 12 GHz, with absorber. The back radiation varied from simulations due to the feed.

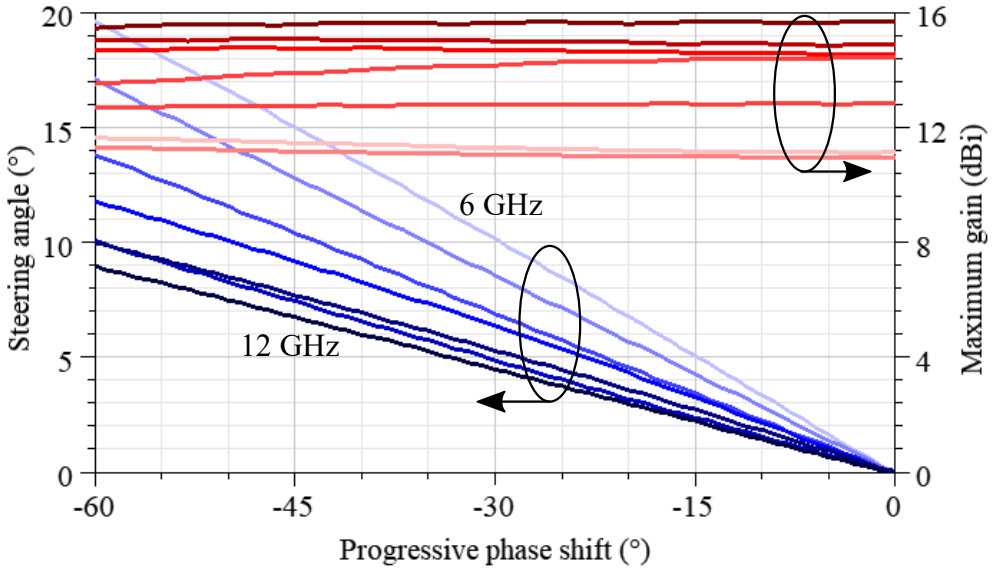


Figure 3.8: Steering angle (blue) and associated maximum gain (red) for progressive phase shift applied to the ports of the array. Frequencies shown for 6 to 12 GHz from lighter to darker colors. More beam steering is achieved at lower frequencies while there is more gain at higher frequencies.

Brass pedestals are added to level the MMIC surface with the TMM6 substrate of the feed network for low-inductance bond wires from the MMIC pads. A set thermal power is used as the excitation at the four MMIC PA positions, corresponding to expected dissipation by the active devices. For example, a 50% efficient 2 W amplifier dissipates 2 W of thermal power. In all plots, the thermal power is listed per source, so in the above example, the total thermal load in the simulation is 8 W. The brass structure allows for direct integration of cooling channels, also shown in Fig. 3.9. The cooling channels extend through the first two brass blocks, allowing a closed flow that can be created externally to the antenna structure. The absorbers are not included in the thermal simulations, both for simplicity of initial tests and because their thermal properties are not well quantified by their manufacturer. The brass is a yellow brass with thermal conductivity of 111 W/m K. The fabricated model did not include the cooling channels, but such a design would allow for easy integration in the future when a new array is fabricated. To explore their effects, the cooling channels are added in simulations. For simplification of simulations, the channels are set to a constant temperature and not given material properties. Simulations are done for two cases of channel temperatures, set to 20° C and 40° C. Ideally, a system would be implemented that could successfully circuit a cooling medium to keep the temperature near to room temperature, but even in the worse case scenario of 40° C, there is significant

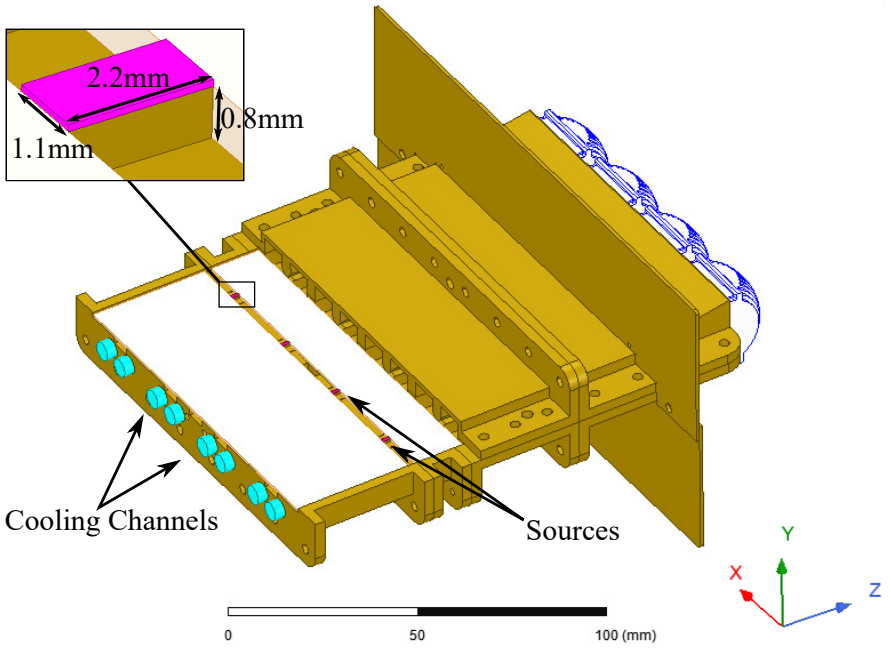


Figure 3.9: Geometry used for thermal simulations. The cooling channels are placed longitudinally, and the four power amplifiers are modelled as uniform heat sources shown in the inset. The cooling channels extend through the first two modular brass blocks (feed network and MMICs).

improvements in thermal behavior which is shown in the subsequent results.

Fig. 3.10 shows the heat distributions of the array when 2 m/s of airflow is forced from the back of the array to the front. The temperature across two cross-sections is shown: a cut perpendicular to the flow of the signals through the source (xy plane); and a cut through the base of each pedestal for a top view of the entire array (xz plane). The temperature is highest at the sources, as expected, and the heat conduction is clearly observed, with an increase of 15°C at the horn antennas.

This behavior is quantified in Fig. 3.11 which shows the temperature profile in the y direction, starting directly above the MMIC source, through the source, and to the bottom of the brass structure. A measurement with a dc-biased GaN MMIC at (25 V, 70 mA) gives a temperature of 45° at the bottom of the brass structure ($y = -15.9$ mm), showing good agreement with thermal simulations. The top of the source is marked by the blue line and the bottom of the brass structure is marked by the red line, while measured data point is indicated with a black cross. Adding cooling with forced air flow or liquid at a constant 20°C results in a significant drop in temperature. Additionally, widening the MMIC pedestals from 1.1 mm to 3.3 mm

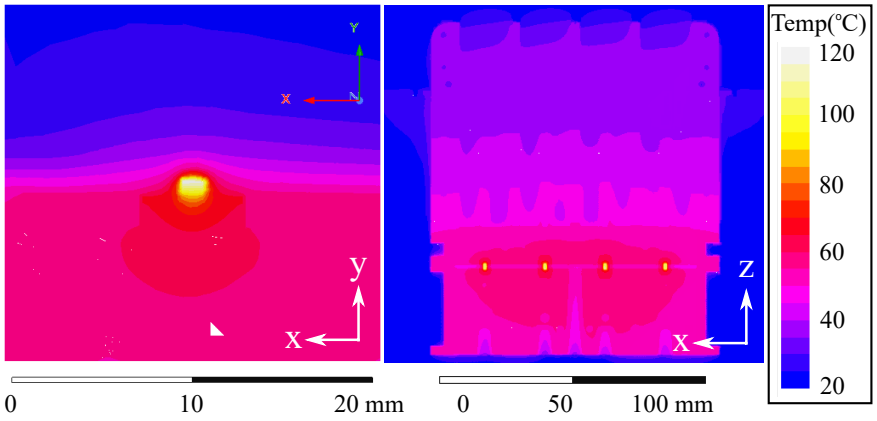


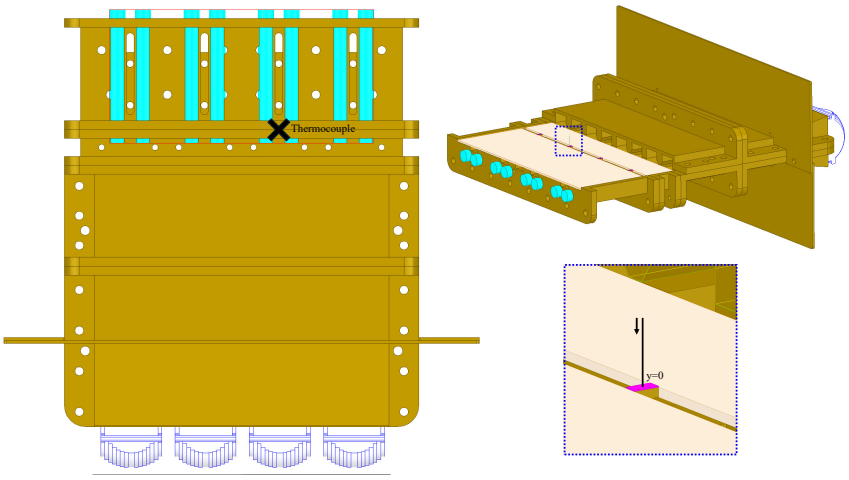
Figure 3.10: Steady state temperature distribution when 10 W of thermal power is applied at each source and with forced air flow with a 2 m/s velocity. Left: a cut through the MMIC source perpendicular to the direction of propagation. Right: a cut looking down at the antenna array with the horns at the top.

decreases temperature without any additionally cooling mechanisms. For example, right below the source ($y = -0.1$ mm) with 5 W of dissipated power, and with no additional cooling, the temperature is 117°C, while wider pedestals lower the temperature to 94°C. With 2 m/s forced air flow, the temperature drops to 62°C, and with the channels fixed at 20°C an additional drop to 46°C is observed.

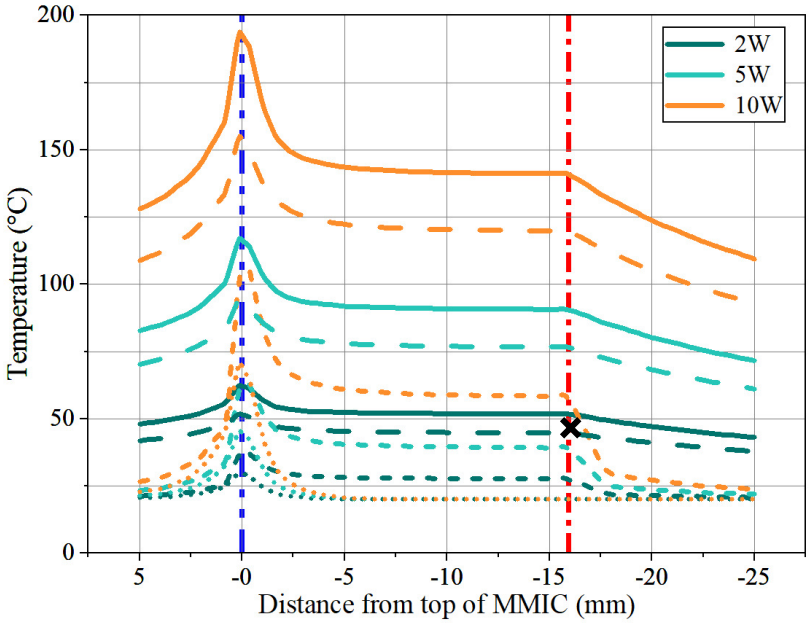
The behavior is also quantified over power as shown in Fig. 3.12 for the center of the pedestal directly below the source. Adding forced air lowers the temperature dramatically, by over 100°C for 10 W or higher per source. The addition of pipes for cooling also greatly lowers the temperatures, even when set to a relatively high 40°C, performing better than air cooling for 5 W or greater of thermal power.

3.4 Scaling to 2-D Array

The initial presented 4×1 array provides a good starting point for further work and analysis to larger configurations. Having four elements is one of the smallest sizes that still allows for beam steering and amplitude tapering. Work in the upcoming chapters focus on beamforming networks with four outputs that could feed an array like this ridged horn antenna array. For scaling, a second dimension could be added with repeated feed networks stacked on top of each other, either the Wilkinson feed in this chapter or a feed similar to one of the next chapters. The inputs to each of these feeds can be fed simultaneously, allowing beamsteering in one direction or by an analog or digital feed network that can adjust phase between feed



(a)



(b)

Figure 3.11: (a) Simulation set up showing the placement of the thermocouple marked with a black cross and the line that the simulated temperature is plotted along in (b). (b) Simulated temperature as distance from the top of the source in the y direction, for different applied powers per amplifier. Results shown for no air flow (solid), increased pedestal size (long dash), 2 m/s air flow (short dash), and addition of pipes for cooling set to 20° C (dotted). The vertical blue line shows where the top of the MMIC source is and the vertical red line shows where the brass structure ends. The symbol (black cross) shows measured steady-state temperature under a MMIC biased at 25 V and 70 mA with no RF input, producing 1.75 W of heat.

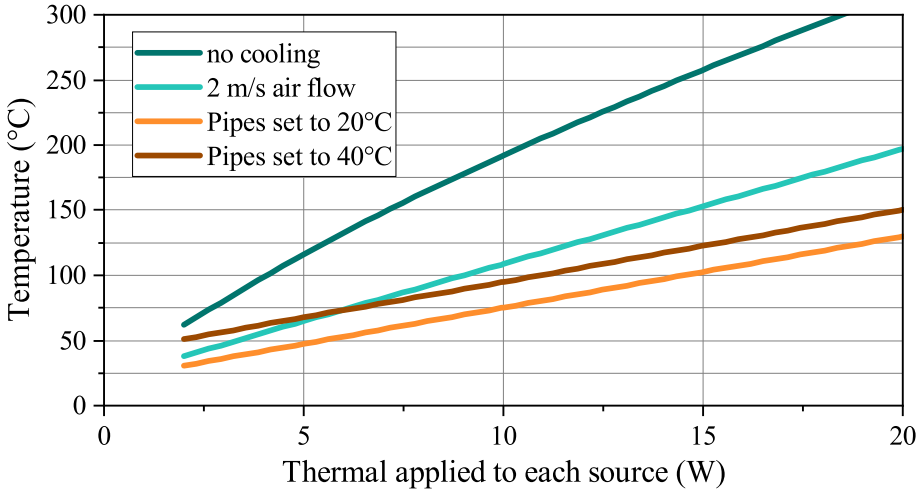


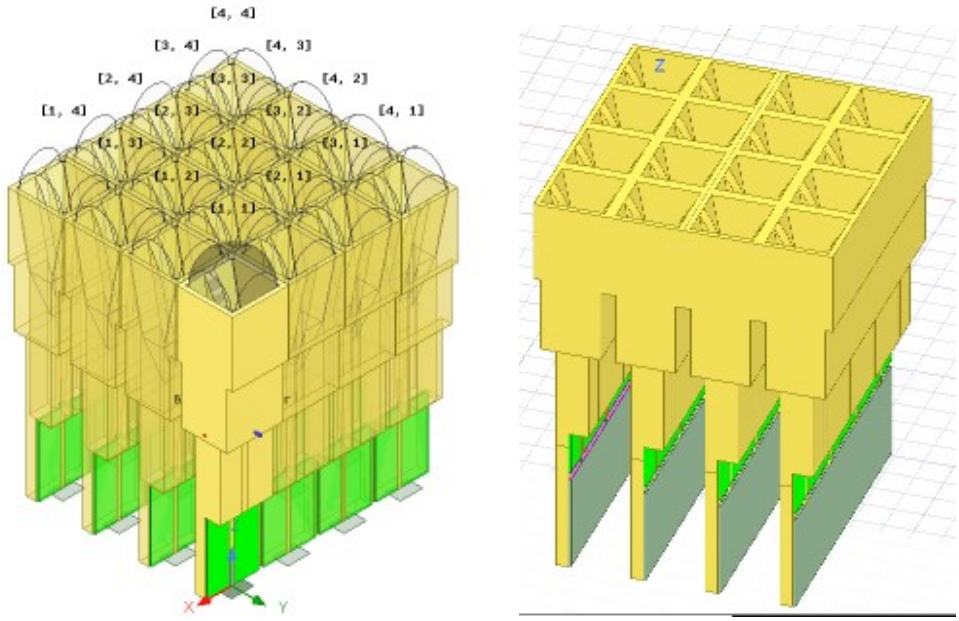
Figure 3.12: Temperature from directly under the source as applied thermal power is increased for no air flow, forced 2 m/s airflow, wider pedestals, and addition of channels for cooling set to two different temperatures.

networks allowing for 2-D beam scanning.

To further explore scaling, a brief study is done to add elements to create a 2-D 4×4 array, the simulated model shown in Fig. 3.13(a). The 4×1 array is repeated four times with the center of the elements of subsequent arrays spaced 25 mm.

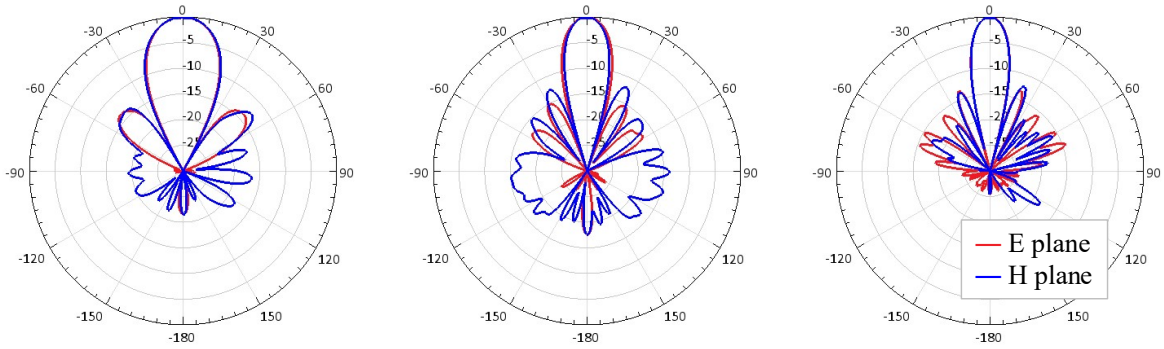
Simulations conducted using ANSYS HFSS assess the performance of this expanded array. The simulated radiation patterns at 6 GHz, 9 GHz, and 12 GHz, shown in Fig. 3.14, reveal that the antenna gain for the 4×4 array increases to between 16 dB and 22 dB across the frequency range. There now is near symmetry in the E- and H-planes due to having equal number of elements in both directions.

To evaluate the impact of this scaling on performance, the equivalent isotropic radiated power (EIRP) is calculated. EIRP considers both the power input to all antenna elements and the overall antenna gain, capturing the combined effect of power amplifiers (PAs) and any associated losses in the beamforming network and connections. For a 2 W PA, similar to those discussed earlier, the EIRP is calculated based on the assumption that each of the 16 PAs outputs 2 W (33 dBm). At 9 GHz, with a simulated maximum gain of 20.1 dBi, the EIRP reaches 65.2 dBm, equating to over 3.3 kW. If each PA instead outputs 5 W (37 dBm), the EIRP increases to 69.1 dBm, or over 8.1 kW. This demonstrates the substantial benefits of scaling up the array in terms of both gain and power handling capacity.



(a) (b)

Figure 3.13: The simulation model used in Ansys (a) HFSS for electromagnetic simulation and (b) Icepak for thermal simulation of the 4×4 antenna array. Elements are spaced 25 mm apart in both dimension. For thermal simulations, the lenses are removed to reduce computation complexity and cooling pipes (shown on right) are added.



(a) (b) (c)

Figure 3.14: Simulated E (red) and H (blue) plane normalized radiation patterns for the 4×4 antenna array at (a) 6 GHz, (b) 9 GHz, and (c) 12 GHz.

Thermal simulations for the 2-D array are performed using ANSYS HFSS, with the model shown in Fig. 3.13(b). To simplify the analysis, dielectric lenses are omitted. The thermal results indicate that without additional cooling systems, the temperature at the base of a thermal source reaches 92°C with 2 W of thermal power and rises to 255°C with 10 W of thermal power. These findings underscore the thermal challenges associated with high-power operation and the need for effective thermal management strategies.

3.5 Conclusion

This chapter details the design and implementation of a 4×1 octave-bandwidth antenna array operating over the 6—12 GHz range, intended for integration with high-power MMIC amplifiers. Thermal simulations provided insights into temperature distribution across the array for thermal powers ranging from 2 to 20 W per amplifier, with results aligning well with a thermal measurement. Coupling between horn elements is maintained within a VSWR of 2 across the octave and the antennas stay relatively well matched. The increase in mismatch will degrade PA performance causing more heat dissipation, but the metal design can handle heat dissipation. Analysis of PA performance under scanning in an array can be found in detail in [91]. The scaling to a 2-D 4×4 array demonstrates enhanced performance, including increased gain and EIRP.

The array's design supports integration with various beamforming networks, including those utilizing phase shifters or discrete beamforming networks. The work presented is adaptable to different frequency ranges and components, showcasing the design's versatility and scalability. Further details can be found in the publications referenced in [88] and [92].

Chapter 4

Passive Butler Matrix Implementations

In the previous chapter, an array is introduced that is fed by a corporate feed network made up of a Wilkinson power divider. Feed networks, denoted as 4' in Fig. 1.6, are crucial for beamforming networks, labeled as 4". While corporate feed networks are commonly used, other feed networks exist, such as series feeds, lenses, and matrices [18, 20]. These examples not only act as feed networks that power-divide the incoming signal but also serve as beamforming networks since they can steer the beam. For a corporate network like the Wilkinson divider, phase shifters, similar to the ones discussed in Chapter 2, are placed after the network to complete the beamforming network.

This chapter focuses on a different beamforming network: a 4-input, 4-output Butler matrix operating from around X-band, which could be used to feed the array discussed in the previous chapter.

4.1 Butler Matrix Basics

Beamforming is briefly introduced in Chapter 1, highlighting the three types of beamforming systems: digital, analog, and hybrid. This thesis only focuses on analog beamforming. Traditionally, analog beamforming uses a corporate power divider followed by phase shifters on each path. Alternative analog beamforming networks include lenses and matrices [93], which can produce multiple orthogonal beams simultaneously. In a lens, an incident plane wave is focused to a point on a focal surface that depends on the incident angle [94].

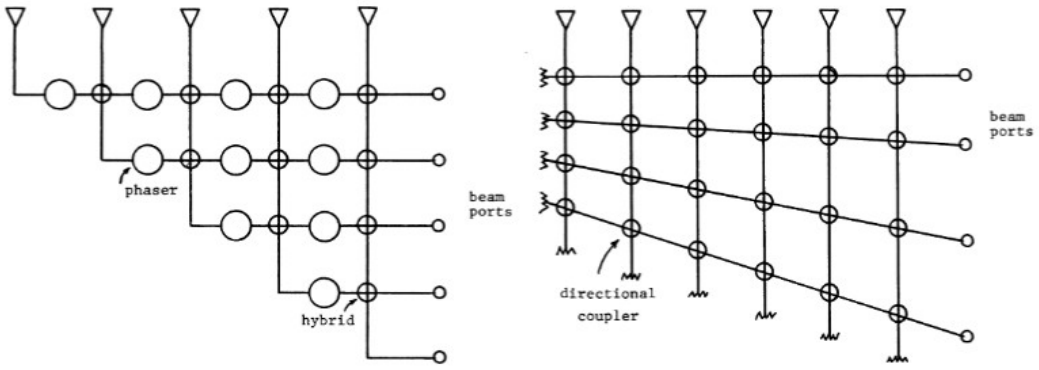


Figure 4.1: General 4-input, 4-output structures of a Nolen matrix (left) and Blass matrix (right) from [18].

Lenses are true-time delay components and therefore inherently broadband. In addition to dielectric lenses such as those of Lunberg type [95], bootlace lenses can be implemented with coaxial lines [96] and parallel plates [97], and Rotman lenses have been demonstrated at RF and millimeter-wave frequencies using micro-coaxial technology [98], stripline [99–101]. In microstrip-based constrained Rotman lenses, also referred to as discrete lens arrays, active components have been directly integrated to provide additional functionality, e.g. amplification [102, 103] and optical control [104].

Types of beamforming network matrices include Nolan, Blass, and Butler matrices [105–107]. Fig. 4.1 illustrates their general structures for 4-input examples of Nolen and Blass matrices with an example of a Butler matrix in Fig. 4.2.

Nolan matrices are a generalized form of beamforming matrix. Its derivation comes from that fact that having orthogonal output beams requires a unitary coupling matrix. This coupling matrix can be built using a unit that consists of a coupler and a phase shift. These units are combined to create the general Nolan matrix structure. The Blass and Butler matrix are both types of Nolan matrices. Blass matrices use a set of transmission lines going to the antenna elements that intersect with a set of transmission lines for the input feeds. At each intersection there is a directional coupler and one set of ports on both set of lines are terminated in matched loads. The lengths of lines between the intersections vary for each feed so the phase at the antenna elements vary depending on which feed is excited. The phase shifts from the generalized Nolan matrix are implemented as the transmission lines of various lengths.

Butler matrices have couplers and constant phase shift networks connected to create specific phase

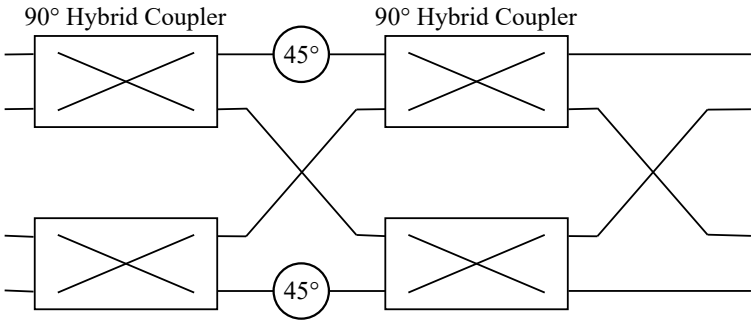


Figure 4.2: Block diagram of a 4×4 Butler matrix composed of 90° hybrid couplers and 45° constant phase shifts.

progressions at the 2^n outputs depending on which of the 2^n inputs is excited. The specific values calculated by Butler are what distinguish the Butler matrix from the general Nolan matrix. For 4×4 matrices, the output phase progressions when using 90° hybrid couplers and 45° phase shifters are ±45°, ±135°. The bandwidth of these matrices is limited by the bandwidth of the couplers, crossovers, phase shifters, and connections used in their construction, shown in the block diagram in Fig. 4.2.

Common types of couplers that are inherently broadband include Lange couplers and multi-section branchline couplers [108]. Branchline couplers use $\lambda/4$ lengths of lines connected to create equal power division and a 90° phase difference at the through and coupled ports. Since this depends on wavelength, they are inherently narrowband, but cascading multiple sections can increase bandwidth up to [109, 110]. Lange couplers use interdigitated coupled lines. Although coupled lines by themselves are broadband, process limitations make it difficult to achieve tight coupling for high coupling coefficients, so multiple more loosely coupled lines are used in Lange couplers [111]. The even and odd mode impedances have been calculated for the coupling coefficients needed to create the desired output response [112, 113]. Early examples of branchline and Lange couplers are shown in Fig. 4.3 with their calculated design parameters for various frequency responses.

Another broadband coupler topology is tandem coupled lines. The tandem coupler approach, introduced in [114], uses two 8.34 dB coupled lines connected in tandem to achieve a total 3 dB coupling with a 90° phase difference at the through and coupled ports. A simple analysis of this can be done through use of signal flow graphs, shown in Fig. 4.4 [115].

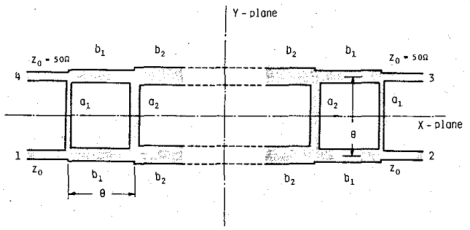


Fig. 1. A 3-dB directional branch coupler with two-fold symmetry about the x and y planes.

TABLE III
CHARACTERISTICS OF FOUR-BRANCH COUPLERS**
(4-1: Butterworth Coupler; 4-2: Chebysev Coupler)

	D	b_1 [Ω]	b_2 [Ω]	a_1 [Ω]	a_2 [Ω]	$BW_{8.1}$ [%]	BW_C [%]	S_{min} [dB]	S_{max} [dB]	K_0 [dB]
4-1	—	39.97	30.33	263.85	52.82	43	32	∞	—	0
4-2	—	36.83	28.77	170.53	57.44	60	34	∞	22.14	0
4-3	16	44.34	39.40	152.95	90.96	63	44	36.02	20.51	0.28
4-4	20	44.14	39.15	162.39	85.32	60	40	36.23	22.73	0.19
4-5	24	45.03	41.99	157.52	91.12	58	38	29.03	23.02	0.14
4-6	16	39.40	30.66	*166.67	67.03	62	44	31.89	20.47	0.29
4-7	16	42.99	36.84	*156.25	83.91	63	44	47.30	20.45	0.28
4-8	16	47.16	44.76	*147.06	106.32	61	43	28.90	20.46	0.28
4-9	16	51.96	54.85	*138.89	136.09	57	43	23.47	20.39	0.26
4-10	16	57.37	67.39	*131.58	174.95	50	43	22.06	20.15	0.25
4-11	14	53.68	56.51	*142.86	*142.86	57	45	25.24	20.20	0.40
4-12	16	53.94	58.31	*142.86	*142.86	55	43	24.17	21.41	0.29
4-13	16	52.50	55.92	*138.89	*138.89	56	43	23.30	20.52	0.27
4-14	18	52.62	57.14	*138.89	*138.89	54	41	24.16	21.01	0.21
4-15	20	52.69	58.06	*138.89	*138.89	52	40	25.66	21.23	0.17
4-16	20	51.28	55.34	*135.14	*135.14	53	40	26.33	20.04	0.16
4-17	22	51.32	56.41	*135.14	*135.14	52	39	27.75	20.08	0.13

**The impedances of 166.67, 156.25, 147.06, 138.89, 135.14, and 131.58 correspond to the normalized admittances of 0.30, 0.32, 0.34, 0.36, 0.37, and 0.38, respectively.

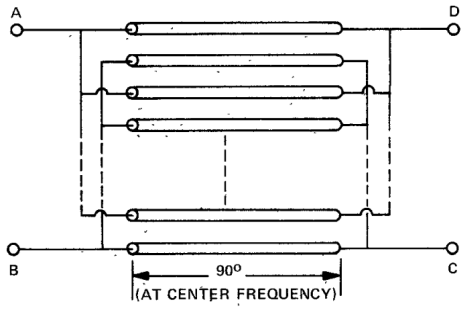


Fig. 2. Interdigitated directional coupler.

TABLE I

No. of Lines k	Power Coupling Ratio (dB)	Y_{oo} (℧)	Z_{oo} (Ω)	Y_{oe} (℧)	Z_{oe} (Ω)
2	3 dB	0.0483	20.71	0.00828	120.7
	6 dB	0.0346	28.87	0.0115	86.60
	10 dB	0.0277	36.04	0.0144	69.37
4	3 dB	0.0190	52.61	0.00568	176.2
	6 dB	0.0147	67.96	0.00702	142.5
	10 dB	0.0131	76.30	0.00845	118.3
6	3 dB	0.0121	82.55	0.00411	243.1
	6 dB	0.00951	105.1	0.00490	204.3
	10 dB	0.00819	122.1	0.00552	181.1

Figure 4.3: The design of a multi-stage branchline coupler and its calculated design parameters for various frequency responses from [110] (left).The design of a Lange coupler and calculated design parameters for various frequency responses from [112] (right).

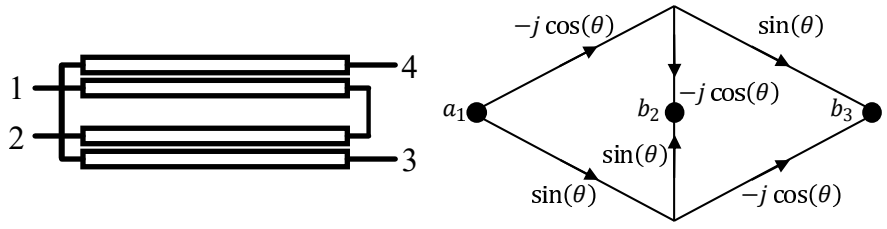


Figure 4.4: The circuit diagram of a two-section tandem coupled line coupler (left) and the signal flow graph from input port 1 to output ports 2 and 3 (right)

The two sections of equal coupled lines are shown on the left and the corresponding signal flow graph on the right and use of the S-parameter values of reciprocal, lossless, and symmetric coupled lines. The through path is $\sin\theta$ and the coupled path is $-j\cos\theta$. Using the signal flow graph the paths to port 2 and 3 are found to be:

$$S_{21} = \sin^2(\theta) - \cos^2(\theta) = \cos(2\theta) \tag{4.1}$$

$$S_{31} = -j2\sin(\theta)\cos(\theta) = -j\sin(2\theta) \tag{4.2}$$

Since the overall coupling is 3-dB, these values can be set to $1/\sqrt{(}2)$ so

$$\cos(2\theta) = 1/\sqrt{(}2) \rightarrow \theta = 22.5^\circ \tag{4.3}$$

Then the coupling coefficient can be found from the coupled line equations to be

$$\sin(22.5^\circ) = 0.383 = 8.34\,dB \tag{4.4}$$

So each line should have 8.34 dB coupling for the single frequncy analysis of a 3-dB tandem coupler. The overall frequency response can be achieved for various ripple levels, numbers of sections, and bandwidths [116]. This design requires crossovers and has been implemented in microstrip with wire-bonding [117,118], multilayer microstrip [119], and coplanar waveguide (CPW) [120, 121]. Some designs use more than two sections to get specific responses in the desired aspect ratio [118]. Fig. 5.2 includes some published examples of tandem couplers.

For narrowband implementations, the phase shift element used in Butler matrices can be implemented as a transmission line. For broadband operation, the most common phase shift element used is a Schiffman phase shifter [122]. The Schiffman phase shifter uses a shorted pair of closely coupled lines to control the even and odd mode impedances, creating a nearly constant phase shift compared to a reference length of transmission line. Various studies have explored improving the performance and bandwidth of this phase shifter [123–126]. Schiffman phase shifters are particularly attractive for feed network implementations because they are single-layer and planar, making them easy to integrate into most technologies such as microstrip or stripline.

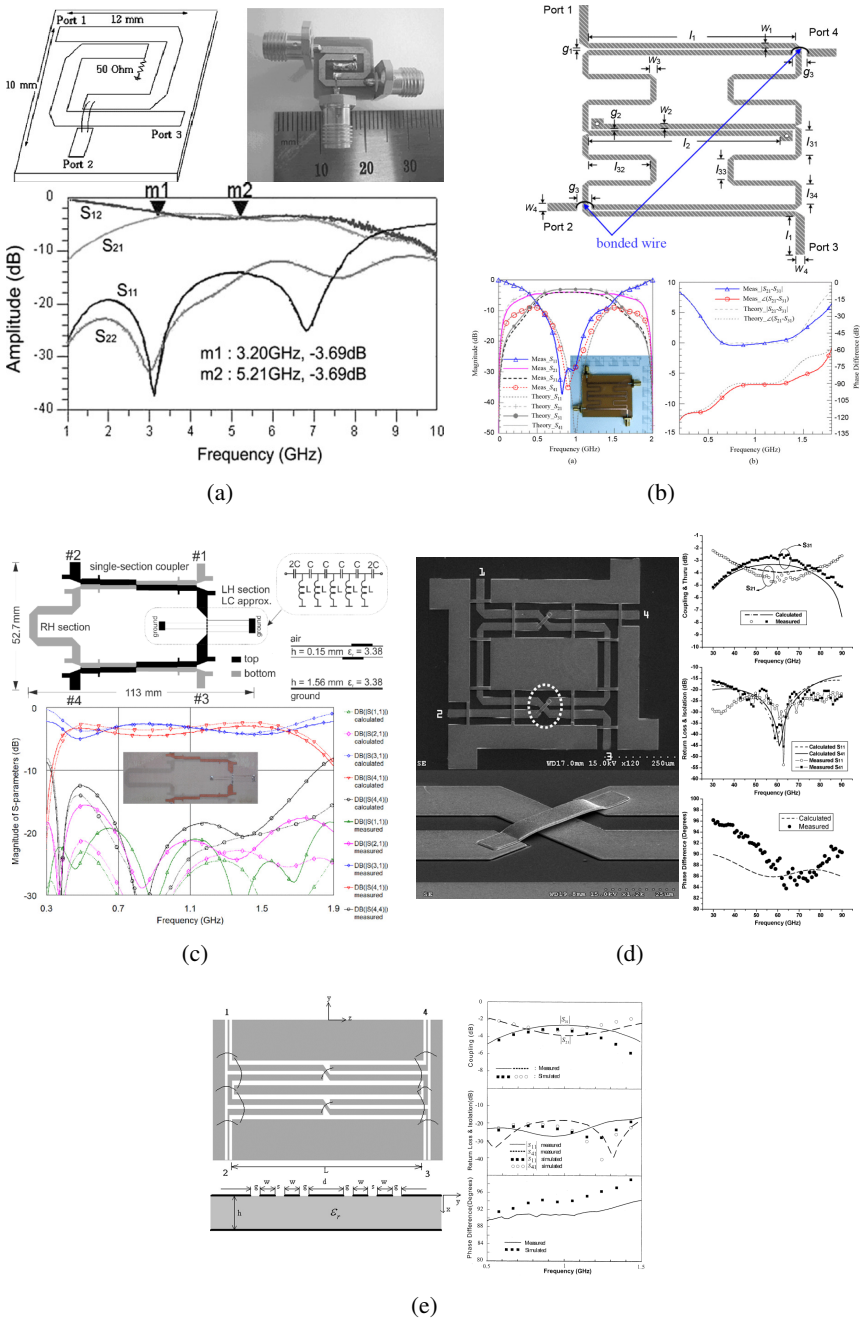


Figure 4.5: Examples of broadband tandem couplers. (a) A microstrip 3.6-5.5 GHz two-section tandem coupler using bondwires and with the isolated port terminated [117]. (b) A 0.6-1.4 GHz three-section microstrip tandem coupler using bondwires [118]. (c) A 0.4-1.7 GHz two-section tandem coupler made on multi-layer microstrip with right-hand and left-hand lines connecting the sections [119]. (d) A 30-90 GHz two-section CPW tandem coupler on a single layer PCB process with dedicated air-bridge structures [121]. (e) A 0.4-1.5 GHz two-section CPW tandem coupler using bondwires [120].

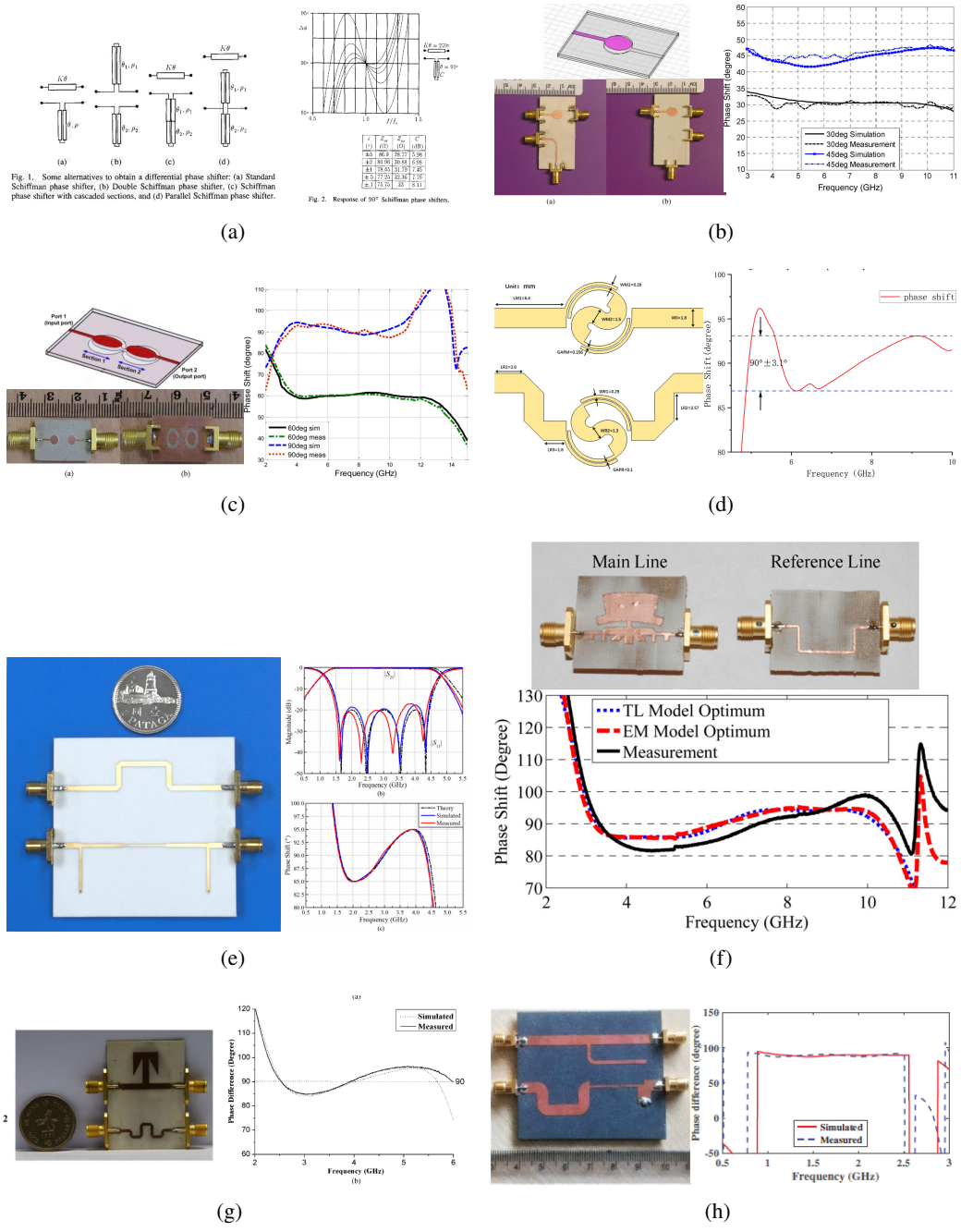


Figure 4.6: Examples of broadband constant phase shift elements. (a) Various versions of Schiffman phase shifters and the calcuated performance for various design parameters [127]. (b) A front- and back-side coupled resonator based phase shift [128]. (c) A front- and back-side coupled resonator based phase shift with extend phase shift range [129]. (d) A multi-mode resonator based phase shift [130]. (e) A $\lambda/4$ stubs and resonator based phase shift [131]. (f) A loaded line based resonator [132]. (g) A single stub loaded line based resonator [133]. (h) A stub loaded line based resonator [134].

Other examples of broadband of planar constant phase shifters include utilizing coupling between front- and backside metal structures [128, 129], resonant structures [130, 131, 135], and lines loaded with stubs [132–134, 136, 137]. Some of these constant phase shifts are highlighted in Fig. 4.6.

Similarly, planar designs for crossovers are attractive for easy implementation, but they are challenging to design for broadband matching and isolation between ports. An overview of planar crossovers is presented in [138]. Most of the crossovers surveyed are narrowband, though some, including multiple-stage branchline couplers and cascaded branchline couplers, demonstrated broader bandwidths [139–141]. Some designs require patterning on both front- and back-side metals. When multiple metal layers are available, RF crossovers can be designed by routing crossing lines over each other in different layers. Coupling remains a consideration, so minimizing the overlap of lines is beneficial. An example of some published crossovers are shown in Fig. 4.7

Butler matrices have been demonstrated at many frequencies, with most work at lower microwave frequencies. A higher frequency millimeter-wave example is introduced in the next chapter. Most published Butler matrices are narrowband, though numerous 4×4 broadband designs have been published, with a majority implemented in stripline, as in [142]- [143]. Other examples are designed using corrugated slots [144] and substrate-integrated waveguides (SIW) [145]. There have also been larger Butler matrices published including 8×8 examples [146] and [147] both which are in stripline with bandwidths of 8-12 GHz and 2-18 GHz respectively. In general, for broadband performance, the limiting factor is the phase imbalance.

4.2 Heterogeneously Integrated 6-12 GHz Butler Matrix

The Butler matrix presented here uses a heterogeneous integration process from HRL called metal embedded chip assembly (MECA). This process aligns the tops of multiple chips and back fills with copper to create a dc, RF, and thermal ground within the mechanical structure. It includes a photolithographically-defined interconnect layer that allows the chips to be connected and structures added on top of the chip without the use of bondwires [148]. An example of a cross section of a MECA design is shown in Fig. 4.8. Here, the front alignment of the chips made of various processes is clear as well as their connections using the gold

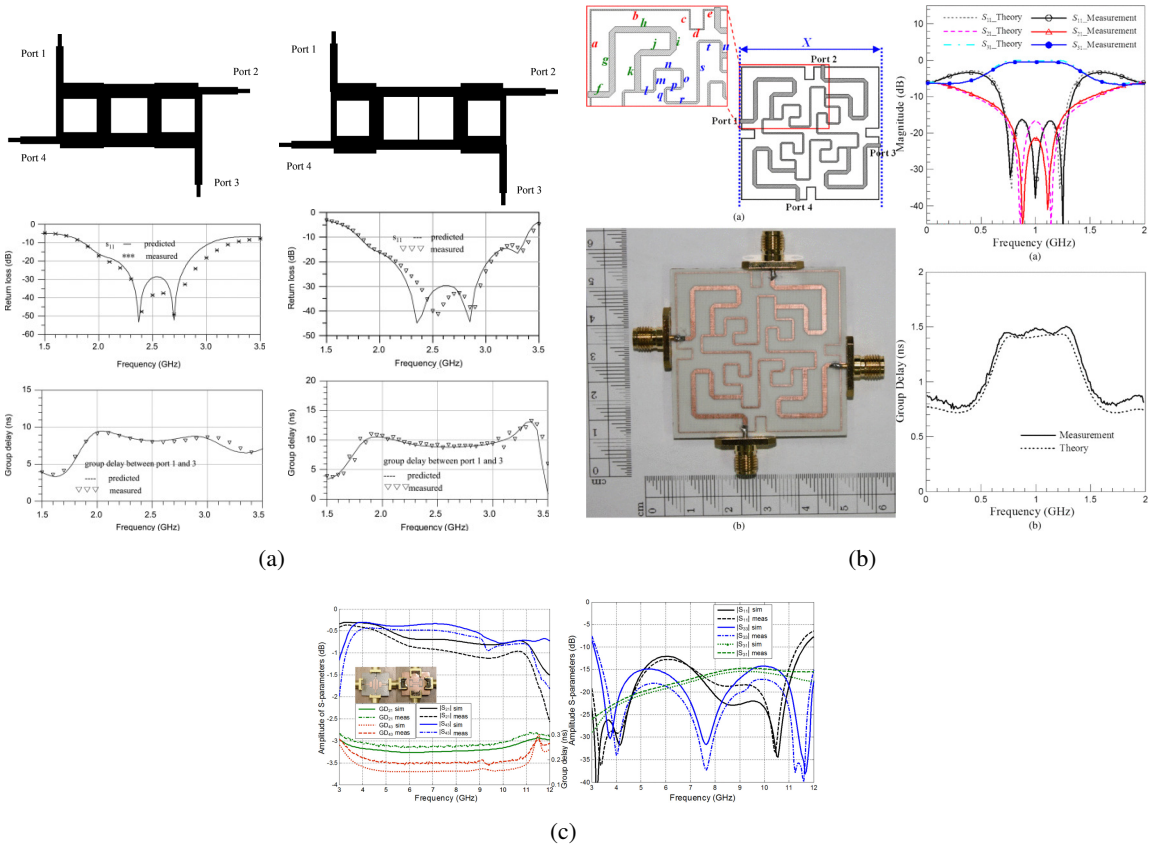


Figure 4.7: Examples of broadband planar crossovers. (a) Three-section and four-section 0-dB branchline couplers for planar crossovers [139]. (b) A folded branchline-type 0-dB coupler used as a planar crossover [140]. (c) A microstrip-to-CPW based broadband planar crossover [141].

interconnect layer. A close up of the interconnect is shown on the bottom of the figure. The interconnect layer allows for well defined RF paths between chips as well as design on the chip itself. Examples of using this layer for implementing various passive components including couplers are shown in [149].

4.2.1 Design of MECA Butler Matrix

The Butler matrix is comprised of three alumina pieces, with a photograph of the manufactured network shown at the top in Fig. 4.9. The total design is compact, 10.7 mm by 5.5 mm in area. The input and output are two identical pieces containing two folded Lange couplers. The middle section includes two Shiffman phase shifters with appropriate line offsets including the necessary RF crossover as shown in the bottom left of Fig. 4.9. The interconnect layer is used for the crossover as well as the bridges of the Lange couplers

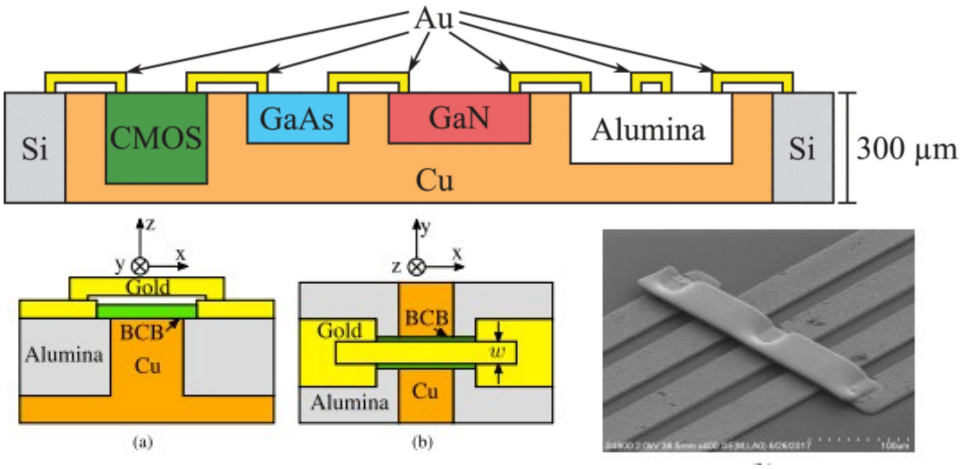


Figure 4.8: A cross section of an example metal embedded chip assembly (MECA) chip that includes chips of various processes (top). These subcircuits are connected with an interconnect layer. Two views of this intereconnect layer as well as a photograph are also shown (bottom).

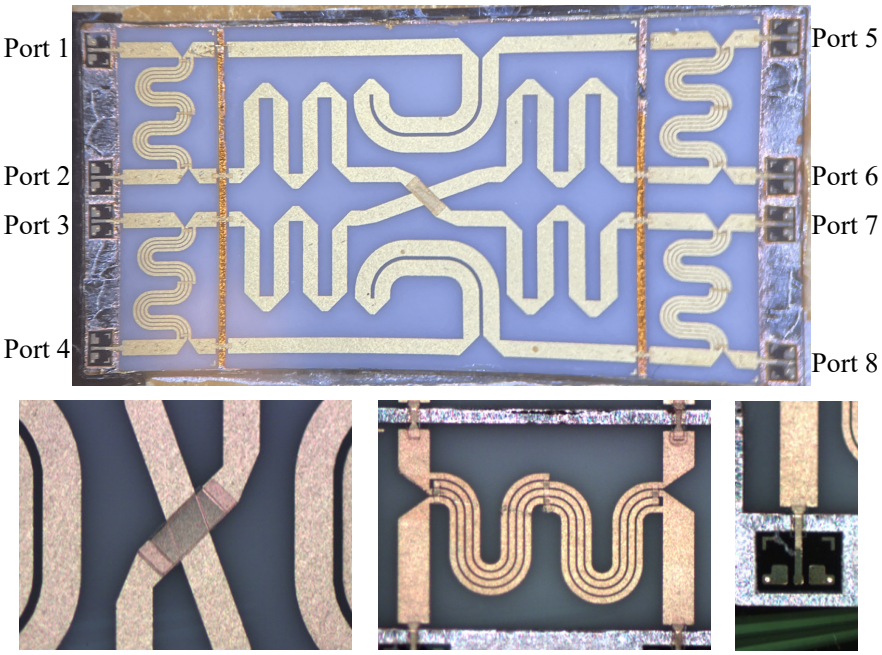


Figure 4.9: Photograph of manufactured MECA Butler matrix (top). Bottom row photographs show details of center crossover (left), Lange coupler (center), and launcher with interconnect (right).

and the connections between the alumina pieces and the launchers which can be seen in the bottom right of Fig. 4.9.

The Lange couplers (bottom center of Fig. 4.9) are meandered for a desirable aspect ratio. The Schiffman phase shifters are modified from the traditional 90° to the needed 45° by scaling the length of the coupled

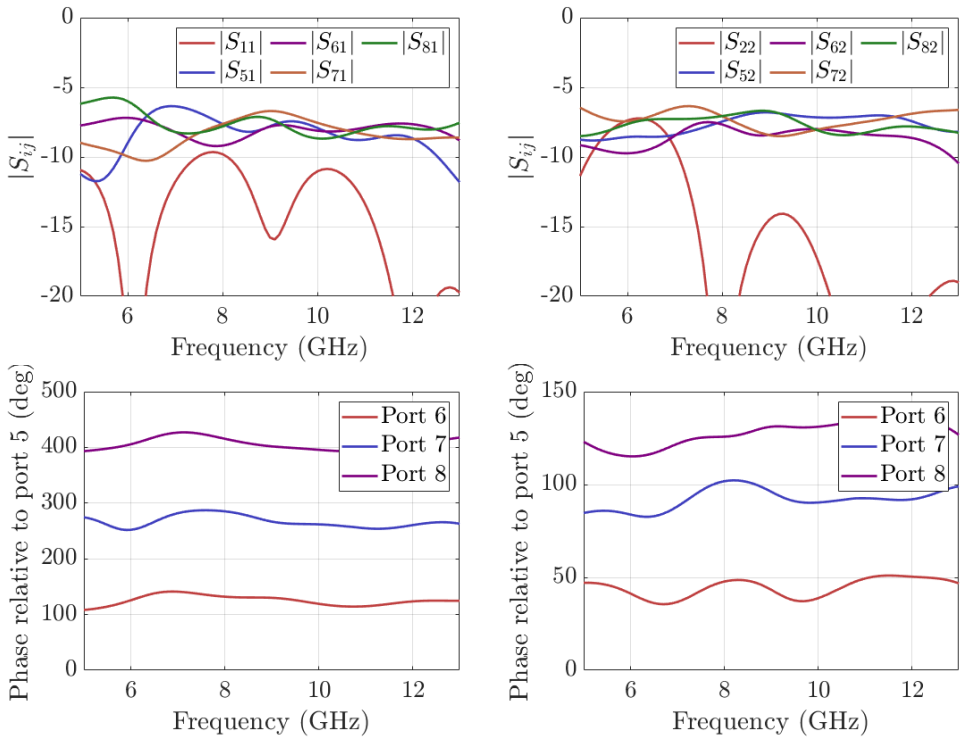


Figure 4.10: Simulated magnitude (top) and phase relative to port 5 (bottom) for when port 1 (left) and 2 (right) are excited of the Butler matrix.

section and reference line [122]. The reference and coupled lines are meandered and bent, which required tuning of the lengths from ideal values, but did not overall affect bandwidth performance.

4.2.2 Simulated Results of MECA Butler Matrix

Fig. 4.10 shows the simulated magnitude and phase response for ports 1 (left) and 2 (right), using Ansys HFSS. Similar behavior is exhibited when exciting ports 3 and 4 as when exciting ports 2 and 1 respectively except the phase progression is reversed. The magnitude responses are shown in the top plots. All ports are matched to better than 7 dB across 6-12 GHz and better than 10 dB from 7-12 GHz. From port 1, the output magnitudes are -7.8±1.5 dB and from port 2, they are -7.5±0.7 dB. The phase progressions are shown on the bottom of Fig. 4.10 where the 135° and 45° phase progressions are seen from port 1 and 2 respectively with phase imbalance of 21°.

The Butler matrix is designed to fit with a previously designed 4×1 antenna array. The array is comprised of 4 double ridged horns loaded with dielectric lenses with a microstrip to waveguide transition. Full details

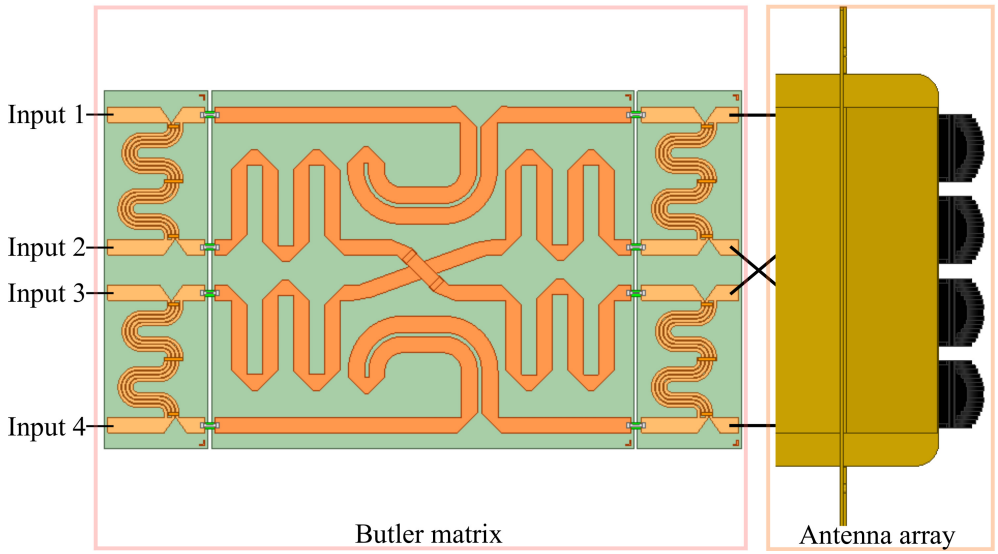
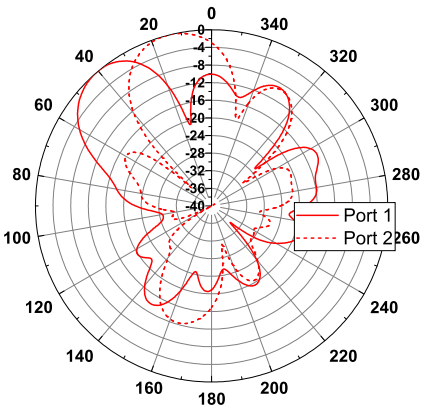


Figure 4.11: Sketch of 10.7 mm×5.5 mm MECA Butler matrix connected to 4-element small-aperture ridged horn antenna array from [92], not to scale.

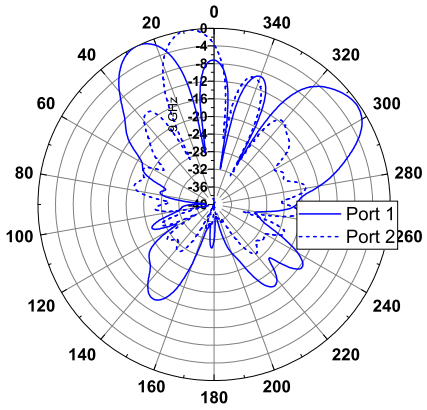
are given in [92]. The spacing of the array elements is 25 mm so an additional microstrip feed board is required to connect the MECA structure to the antenna ports, the Butler matrix and array are shown in Fig. 4.11. The expected performance when connecting the Butler matrix to the antenna array is shown in Fig. 4.12 at 6, 9, and 12 GHz. The output phases and angles when port 1 (solid) and port 2 (dashed) are used as inputs for the antenna array for the plotted radiation patterns.

With port 1 excited, which has phase progression of approximately 135°, at 6 GHz the beam steers 40°, and at 9 and 12 GHz the steering is 26° and 21°, respectively. With the phase progression from port 2 of approximately 45°, at 6 GHz the beam steers by 14°, while at 9 GHz and 12 GHz a steering of 9° and 7° is obtained. Similar results are exhibited when ports 3 and 4 are excited except reflected across the center axis with the opposite phase progressions.

The Butler matrix is fabricated by HRL and dc testing revealed some interconnects are damaged from the fabrication and shipping. The entire circuit is attached to a backing metal and the discontinuous sections are wire-bonded. This successfully held the chip together and all expected paths had dc continuity. Unfortunately, the backing prevents easy integration to the microstrip feed network designed for testing and to connect to the 25 mm spaced horn antennas for full array operation. Future runs need to more carefully consider connections to outside components and for testing with structures that have many ports, such as this 8-port



(a)



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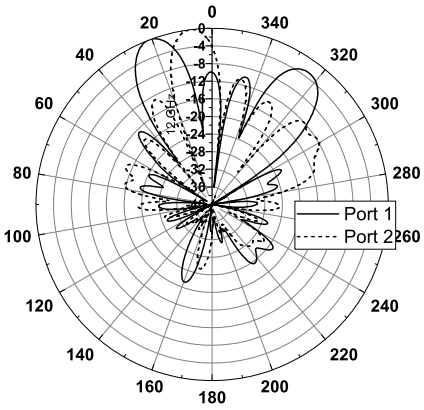


(c)

Figure 4.12: Radiation patterns with the simulated Butler matrix fed at port 1 (solid) and port 2 (dashed) when connected to the measured 4-element linear array from [92] at (a) 6 GHz (b) 9 GHz and (c) 12 GHz.

feed network.

4.3 9-13 GHz Butler Matrix on Low Loss Glass

4.3.1 Apex Glass Substrate and Process

Another novel process capable of heterogeneous integration of feed networks uses a glass substrate developed by 3D Glass Solutions. This process includes the design of an X-band 9-–13 GHz 4××4 Butler matrix, similar to the MECA Butler matrix. The technology is based on their patented APEX glass substrate, an alumino-silicate glass known for its low loss at millimeter-wave frequencies. Key properties of this substrate are

Thermal Conductivity	Coefficient of Thermal Expansion	Electrical Resistivity	Loss Tangent	Relative Permittivity
1.5 W/mK	10 ppm/K	1012 Ω-cm	0.0102	6.4

Table 4.1: Select Properties of 3D Glass Solution's APEX Glass Substrate

detailed in able. 4.1 from [150].

The manufacturing process involves placing a photomask on a wafer, exposing it to UV light, baking it to convert the exposed regions into ceramic, and then etching away the ceramic with acid. This method enables the creation of various etched features, including through-glass vias, cavities, channels, and wells, with sub-micron accuracy [151]. This approach facilitates the production of low-cost, high-volume circuits with integrated 3D structures, such as high-Q resonators with air coil inductors, filters, matching networks, and packaging [152]. Although glass is typically known for its thermal insulating properties, thermal management solutions have been developed to accommodate active components that generate heat [153]. 3D Glass Solutions offers two Process Design Kits (PDKs) for use with commercial RF design software Cadence AWR: "LC-IPD" for sub-6 GHz applications featuring high-Q lumped elements, and "SIW" for millimeter-wave applications in the W- and D-bands based on SIW distributed elements [154, 155]. For custom designs, as in this design, full-wave simulations are done using ANSYS HFSS to create unique three-dimension designs.

Various stack-ups are available, including the stack-up used in this design and shown in Fig. 4.13, which consists of one backside metal layer, a glass substrate, and two top-side metal layers separated by a polymer layer. The glass is 300 μm thick, with copper metal layers each 10 μm thick. The polymer layer is approximately 20 μm thick, providing a 10 μm separation between the two metal layers. The polymer layer covers all exposed glass and metal layers directly on the glass. There are two types of vias: thru-glass vias (TGVs), which connect the bottom metal layer to the top metal layer directly on the glass, and μVias, which connect the two metal layers through the polymer. Vias cannot be directly stacked. While vias of different sizes can be manufactured, for easy of manufacturing all vias are the same size with 60 mum diameter TGV and 40 μm diameter μVias. Metal lines can extend over cavities and cavities can be custom sized.

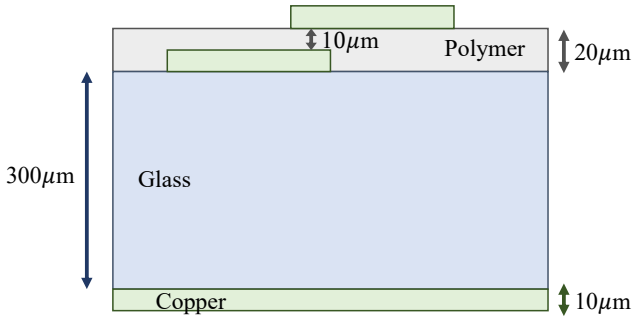


Figure 4.13: A cross section of the stack up for the design of the Butler matrix done in 3D Glass Solution's Apex glass substrate. Not pictured is the solder mask on the top side metals that extend 10 μm above the top-most metal layer. Thru-Glass vias (TGV) extend through the glass substrate and have a diameter of 60 μm. μVias go through the polymer layer between the two upper metal layers and have a diameter of 40 μm.

4.3.2 Glass Butler Matrix Design

The glass wafer is divided into 10 cm by 10 cm design areas. A broadband Butler matrix is designed, as shown in Fig. 4.14. The frequency range is adjusted higher than the MECA version to accommodate Lange couplers within the chip space. The light purple traces represent the metal layer directly on the glass, the darker traces denote the topmost metal layer, and the light blue features indicate cavities in the glass substrate. The bottom metal layer is unpatterned except for release holes under the cavities, necessary for the fabrication process.

Similar to the MECA Butler matrix, the design includes a hybrid coupler, a constant phase shift, and a crossover. Various Lange coupler designs are tested, including configurations with interdigitated fingers on one or both top metal layers. Placing all fingers on one metal layer versus the other showed no significant difference. When using both layers, the width is reduced, but the polymer layer between the metal layers made it difficult to achieve the desired levels of coupling so a single layer design is chosen. Cavities are introduced under the fingers, reducing losses, but also coupling so the spacing is re-tuned. Due to manufacturing constraints, the fingers are placed on the metal layer directly on the glass, with the Lange coupler's connecting bridges on the topmost metal layer. Glass rails are added under the bridges to accommodate both metal layers. The Schiffman coupler is placed on the metal layer directly on the glass.

The crossover is specifically designed to limit coupling between the two metal layers, similar to the

approach in [141]. A microstrip line is converted into a CPW mode by introducing ground planes between perpendicular lines. These ground planes are placed on both metal layers, with TGVs connecting them to the backside metal and μVias connecting them to each other. This CPW mode reduced metal overlap and coupling by shrinking the line width.

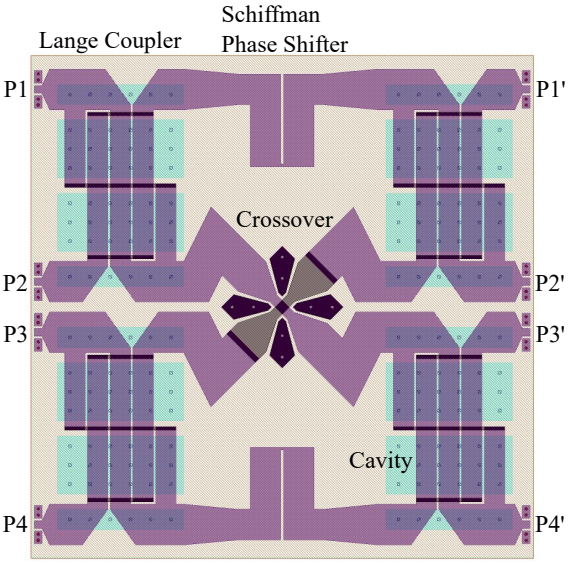
RF inputs and outputs are terminated in 250 μm GSG probe pads, suitable for X-band applications while avoiding process constraints. These pads are on the metal layer directly on the glass, without a polymer layer on top for probing.

Simulated performance for the glass-based Butler matrix is shown in Fig. 4.15 and Fig. 4.16 for magnitude and progressive phase shift, respectively. When P_1 is excited, the match is better than 12.2 dB with transmission losses ranging from 6.3 dB to 9.9 dB across 9-13 GHz. Progressive phase shifts vary from 33.5° to 62.9°. When P_2 is excited, the return loss remains better than 9.6 dB with transmission losses between 6.8 dB to 10.1 dB. The progressive phase shift ranges from 126° to 146.1°.

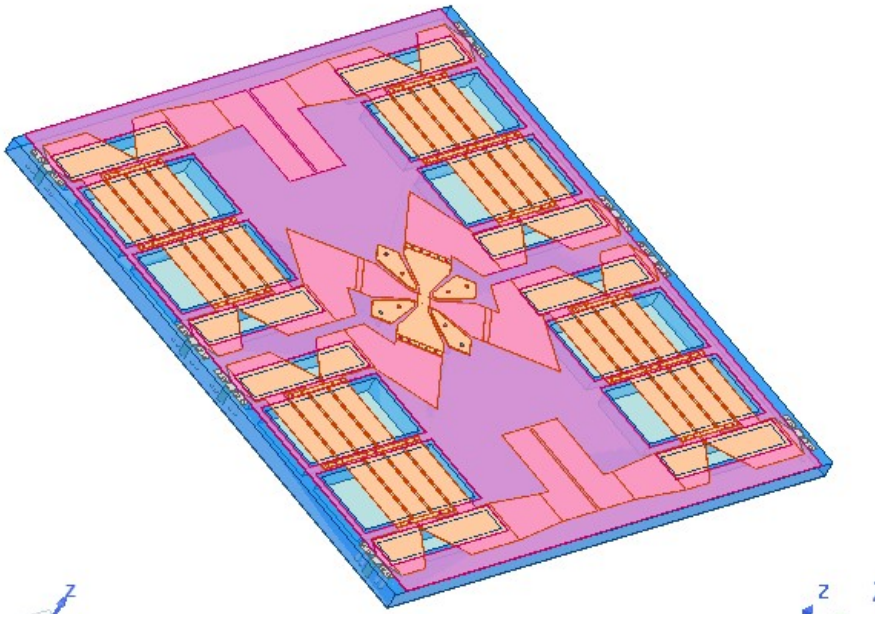
Breakout structures of the Schiffman phase shifter, Lange coupler, crossover, and transmission lines are included on an addition 10 cm by 10 cm chip, along with resonator designs as shown in Fig. 4.17. A TRL kid is also designed for the 250 μm probe pads used in the Butler matrix design.

4.4 Conclusion

This section introduced Butler matrices, a type of multi-beam beamforming network, an important component in phased array front-ends. Two broadband 4×4 Butler matrix designs are developed using processes from HRL and 3D Glass Solutions. These processes are notable for their potential in heterogeneous integration, though the presented designs are entirely passive with no integrated active components. A broadband 6-12 GHz Butler matrix is presented using the MECA heterogeneous integration process for integration with a 4×1 double ridged horn array. This is one of the largest demonstrations of a single MECA process chip at the time of fabrication and is unique for broadband Butler matrix multibeam feed networks implementation as is done in microstrip. The Butler matrix is a fully passive system so additional nonlinearites are not added, in contrast to beamformers that use active components such as phase shifters. This property, as well

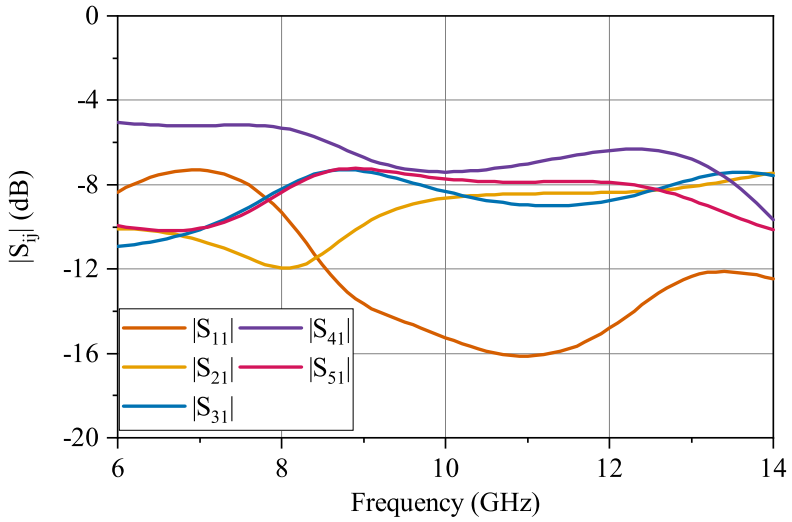


(a)



(b)

Figure 4.14: (a) Submitted layout of 10 cm by 10 cm Butler matrix for fabrication by 3D Glass Solutions. (b) 3-D rendering of submitted Butler matrix design. The glass is in blue. The metal layers are orange. The polymer layer is shown in pink. The cavities under the couplers can be seen with just the grey back-side metal showing.



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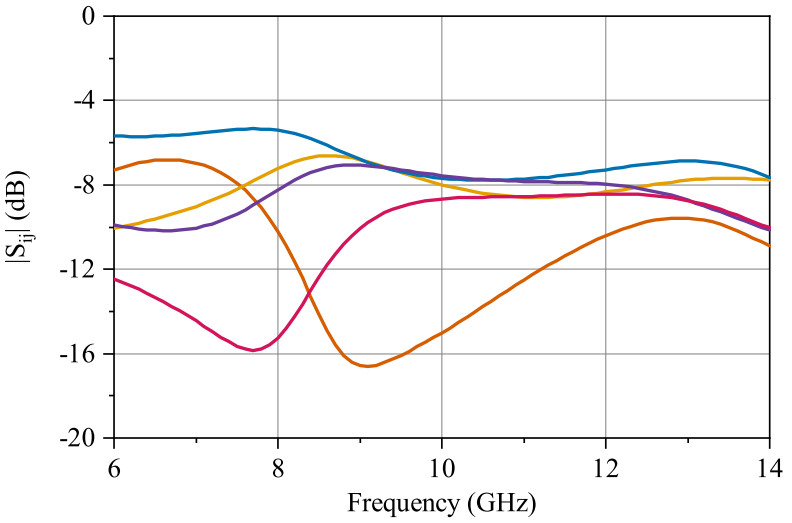
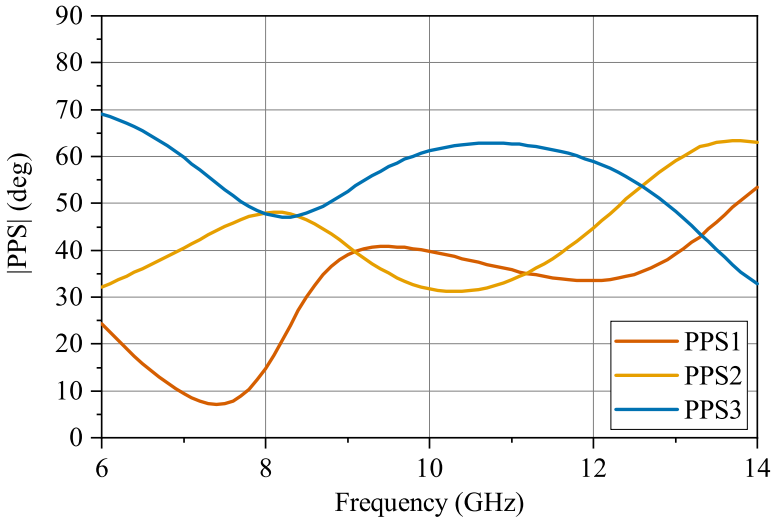
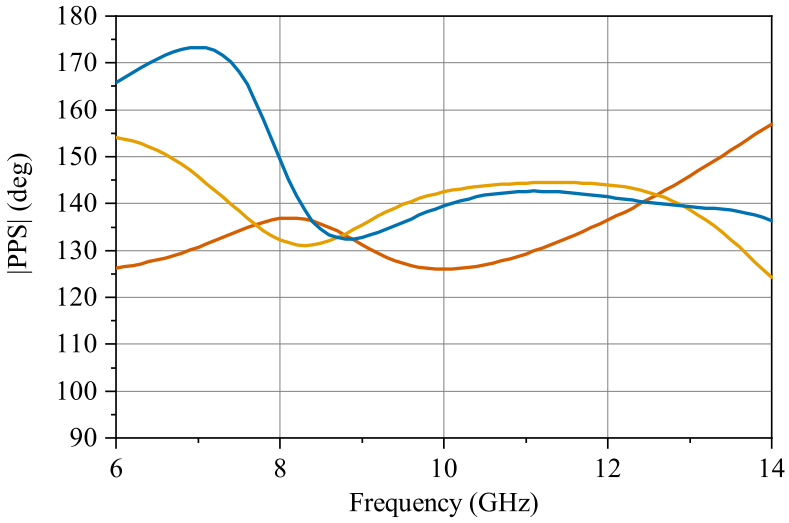


(b)

Figure 4.15: Simulated S-parameters for exciting input port (a) P_1 and (B) P_2 of the 3D Glass Solutions' Butler matrix.



(a)



(b)

Figure 4.16: Simulated progressive phase shift from exciting input port (a) P_1 and (b) P_2 of the 3D Glass Solutions' Butler matrix.

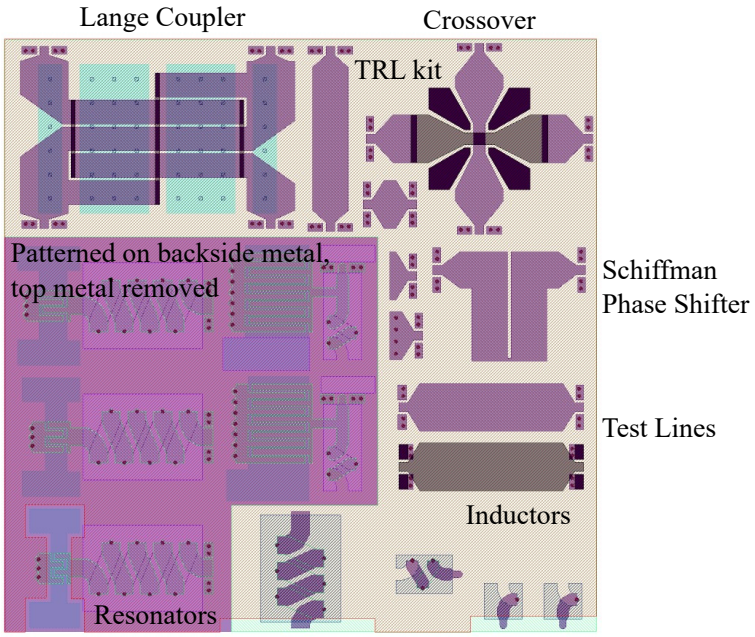


Figure 4.17: Submitted layout of 10 cm by 10 cm chip that contains test structures from the Butler matrix along with resonator structures.

as the broadband nature of the design, will be useful as further work continues on multiple beam antenna array systems. Table 4.2 compares this beamformer to other Butler matrices reported in literature. While not as broadband as some examples, specifically those in stripline, this has broadband performance as well as the potential to be integrated directly with active components using the MECA heterogeneous integration process. The second implementation is done in a low loss glass process by 3D Glass Solutions. This 9-13 GHz example is also detailed in Table 4.2 and utilizes the processes multiple metal layers and air cavities to create a low loss broadband beamforming network.

The next chapter will explore the design of similar feed networks with integrated active components to enhance performance.

The MECA Butler matrix portion of this chapter is published in [57]. These glass chips are currently in fabrication by 3D Glass Solutions.

Table 4.2: Summary of Broadband Butler Matrices

Ref.	$\mathbf{f_l}$ (GHz)	$\mathbf{f_h}$ (GHz)	**Technology**	**Size**	$\Delta\theta$ (°)	ΔA (dB)
[142]	3	10	Stripline	4x4	14	Not given
[144]	3.1	10.6	Corrugated Slot	4x4	4.5	1.2
[156]	1.8	12	Stripline	4x4	15	2
[145]	8.5	10.6	SIW	4x4	5	0.6
[143]	2	3	Stripline	4x4	3	Not given
[146]	8	12	Stripline	8x8	15	1
[147]	2	18	Stripline	8x8	15	1.5
This work	6	12	MECA	4x4	21	1.5
This work	9	13	Glass	4x4	19	1.7

Chapter 5

Millimeter-Wave On-Chip Butler Matrix

In the previous chapter, two implementations of beamforming networks, the component labelled 4" in Fig. 1.6, are introduced, both around X-band. These examples demonstrate broadband performance and their design processes show promise for easy integration with active components through heterogeneous integration. Another possibility for active component integration is to do the beamforming design directly on-chip in a process that contains active devices. This becomes more plausible at higher frequencies as the components decrease in size with frequency. This chapter presents an implementation of an on-chip beamforming network, specifically in WIN Semiconductors' PP10-20 GaAs process (process 3 from Table 2.1). This example operates at 44 GHz with 2 GHz of bandwidth. This implementation shows an example of frequency scaling from previous designs, resulting into a more compact final chip. As discussed in Chapter 1, there is increasing interest in millimeter wave spectrum. The frequencies around 40 GHz are useful for future communication, e.g. 5G bands N259 (39.5-43.5 GHz) and N260 (37.0-40 GHz), and satellite communications, e.g. MILSTAR government satellites with carrier frequencies at 20 and 44 GHz [157].

5.1 Introduction of Millimeter-Wave Butler Matrices

As introduced in the previous chapter, Butler matrices are first described in [107] and are composed of a series of connected couplers and constant phase shift networks create specific phase progressions at the

2^n outputs depending on which of the 2^n inputs is excited. For 4×4 matrices ($n = 2$), the output phase progressions when using 90° hybrid couplers and 45° phase shift networks are ±45°, ±135°. These allow for the production four separate beams, two on each side of broadside. The generated AF for these ideal progressive phase shift produce beams at ±14.5°, ±48.5° off broadside.

As discussed in the previous chapter, hybrid implementations, from 4×4 to 16×16, have been demonstrated, e.g., in microstrip and stripline with a 4×4 Butler matrix operating as low as 0.9 GHz [158, 159]. At millimeter-wave frequencies, including V and W bands, implementation using hollow waveguides [160], substrate integrated waveguides (SIW) [161, 162], liquid crystal polymer circuits [163], and gap waveguides [164] have been demonstrated. Most implementations are narrowband, limited by the bandwidth of the couplers and phase shift networks.

On-chip demonstrations include examples in GaAs at 2.4 GHz [165], 15 GHz [166] and 24 GHz [167]. The 24 GHz GaAs example contains an integrated switch and reported an overall insertion loss of 5.6±0.95 dB and phase error of 6°. Also at 24 GHz, a CMOS design demonstrated an insertion loss of 2.2±0.6 dB, and a phase error of 6° [168]. Some examples have been published around 60 GHz in CMOS [169, 170]. The CMOS chip in [170] showed insertion loss of 2.77±0.6 dB and phase error of 5° at 63 GHz. Another CMOS Butler matrix in [169], which includes an integrated switch, reported a total insertion loss of 7.5 dB and a phase error of 16°. Higher order examples include a V-band 8×8 CMOS implementation operating from 56-66 GHz [171]. Many of these on-chip examples directly integrate switches as part of the beamforming network to select one of the inputs e.g., [165, 167, 169]. Switches can be included on the input side so there is only one RF input path. This simplifies measurement and integration but with a SP4T switch, only one input port can be excited at a time so the beamformer no longer works as a multi-beam feed. These integrated demonstrations show for on-chip implementations can be directly integrated with the beamforming network.

In this chapter, a 44-GHz 4×4 Butler matrix in an GaAs millimeter-wave process is demonstrated. A block diagram with input ports labeled P1 States 1, 2, 3, and 4 and output ports P2, P3, P4, and P5 is shown in Fig. 5.1. The architecture integrated on-chip allows straightforward extensions to more beams, as well as integration with amplifiers and other active components.

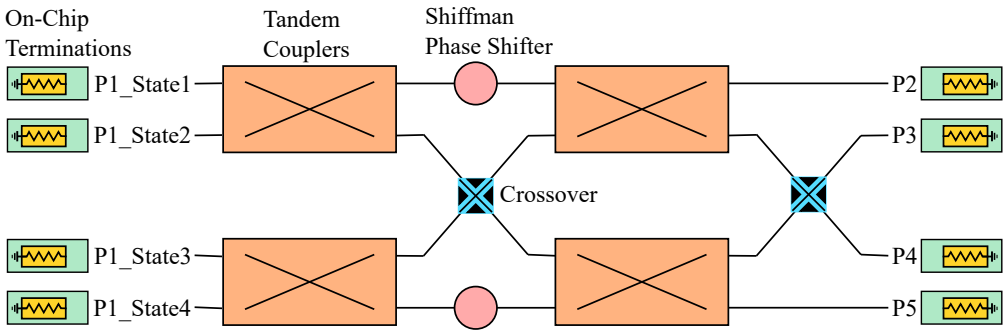


Figure 5.1: Block diagram of the 44 GHz on-chip Butler matrix beamforming network.

5.2 Integrated Butler Matrix Design

The beamformer is designed with several specific goals, including the possibility of extensive testing using a two-port network analyzer. To enable terminating the 6 ports when measuring S-parameters of any two ports, 50-Ω on-chip terminations are co-designed with the ground-signal-ground (GSG) pads. Key components of a Butler matrix at millimeter-wave frequencies are the couplers, necessary cross-over, and phase shifters. The component design and final layout are described below and highlighted in Fig. 5.1. The Butler matrix is designed for fabrication on 150 mm GaAs wafers using the WIN Semiconductors PP10-20 pHEMT platform. The core of this technology is a 160 GHz f_t, 0.1 μm-gate D-mode transistor and is qualified for 4 V operation. This platform offers two interconnect metals with air bridge crossovers, monolithic PIN diodes for on-chip ESD protection, precision thin film resistors with 50Ω/□ resistance, MIM capacitors, through-wafer vias for low-inductance ground connections and can be manufactured with through-chip RF transitions.

The 3-dB tandem coupler is designed from two 8.34 dB couplers with a ground plane between them to correct the phase and amplitude imbalance between Port 2 and Port 3, as shown in the layout of Fig. 5.2. A short open stub is added in the interconnecting transmission lines to compensate for airbridges reactance and improve matching/isolation. The full-wave simulated coupler performance is given in Fig. 5.3. Across 39-49 GHz, the minimum and maximum phase differences between the *through* and *coupled* ports are 88.7° and 89.4°, respectively. At 44 GHz, all ports are matched better than -30 dB. Across the 39-49 GHz range, the match stays below -27 dB at all ports. The amplitude imbalance at 44 GHz is 0.35 dB, while across 39-49 GHz it is below 0.9 dB. The insertion loss at 44 GHz is simulated to be 0.35 dB.

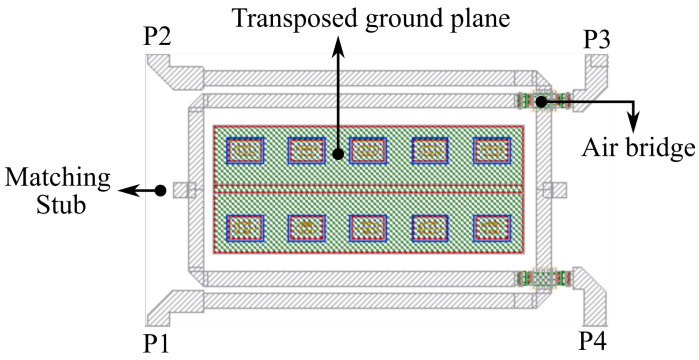


Figure 5.2: Layout of the 3-dB tandem coupler consisting of two 8.7-dB coupled-line couplers connected with an air-bridge. The ground plane and matching elements are used to ensure amplitude and phase balance at the *through* and *coupled* ports.

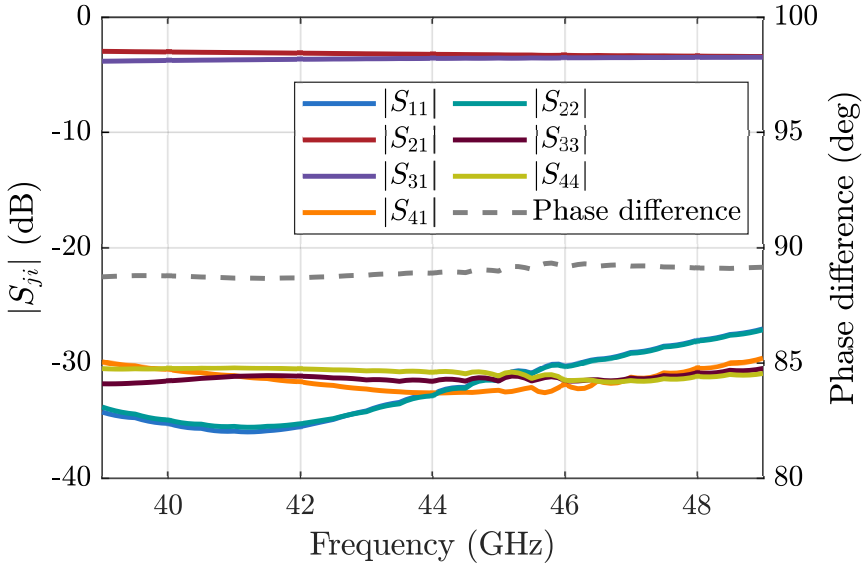


Figure 5.3: Simulated S-parameter amplitudes (solid) of the 3-dB tandem coupler and phase difference between the *through* and *coupled* ports (dashed).

In a 4×4 Butler matrix, the connection of input and output ports through hybrid couplers requires two cross-overs. At 44 GHz, it is not straightforward to design this element with low coupling and a good match. Fig. 5.4 shows the cross-over layout, where ground pads are included between the lines to improve isolation and match by turning the microstrip mode into a CPW mode lowering coupling by over 8 dB. The simulated performance of the cross-over element is shown in Fig. 5.5, showing an isolation of better than 30 dB between all ports from 35 to 55 GHz and all return loss values greater than 20 dB.

For probe-station characterization of the beamformer chip, all 8 ports need to be matched and terminated.

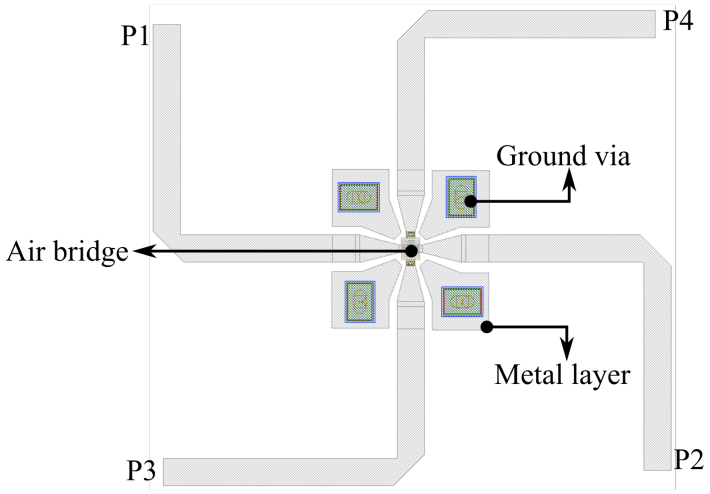


Figure 5.4: Layout of the crossover required in the beamformer design. Pads with vias to the ground are added to improve the match and reduce coupling. Ports 1 and 2 are directly connected to the metal layer, while Ports 3 and 4 are connected with an air bridge.

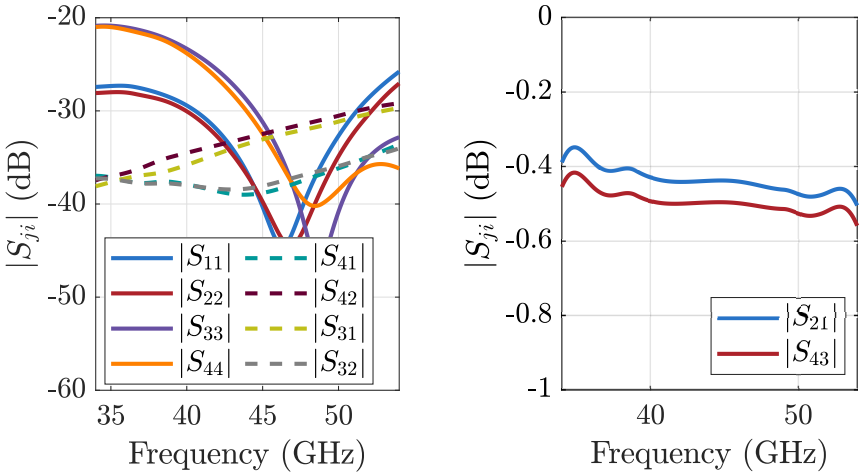


Figure 5.5: Simulated crossover performance. (a) Reflection coefficients (solid) and isolation (dashed). (b) Transmission magnitude (solid) of both paths.

Since most network analyzers are 2-port instruments (or at most 4-port), a solution adopted in this work is to include on-chip resistive terminations close to the ground-signal-ground (GSG) RF in/out pads. The terminations can then be wire-bonded to the signal microstrip lines at the ports that are not connected to the network analyzer ports. The layout of the final beamformer network in Fig. 5.6 shows the compensated terminations on all 8 ports. Assuming each bondwire has an inductance of 0.7-1 nH, the size of the resistor is enlarged to increase the parasitic capacitance that tunes out the bondwire inductance, while maintaining 50 Ω

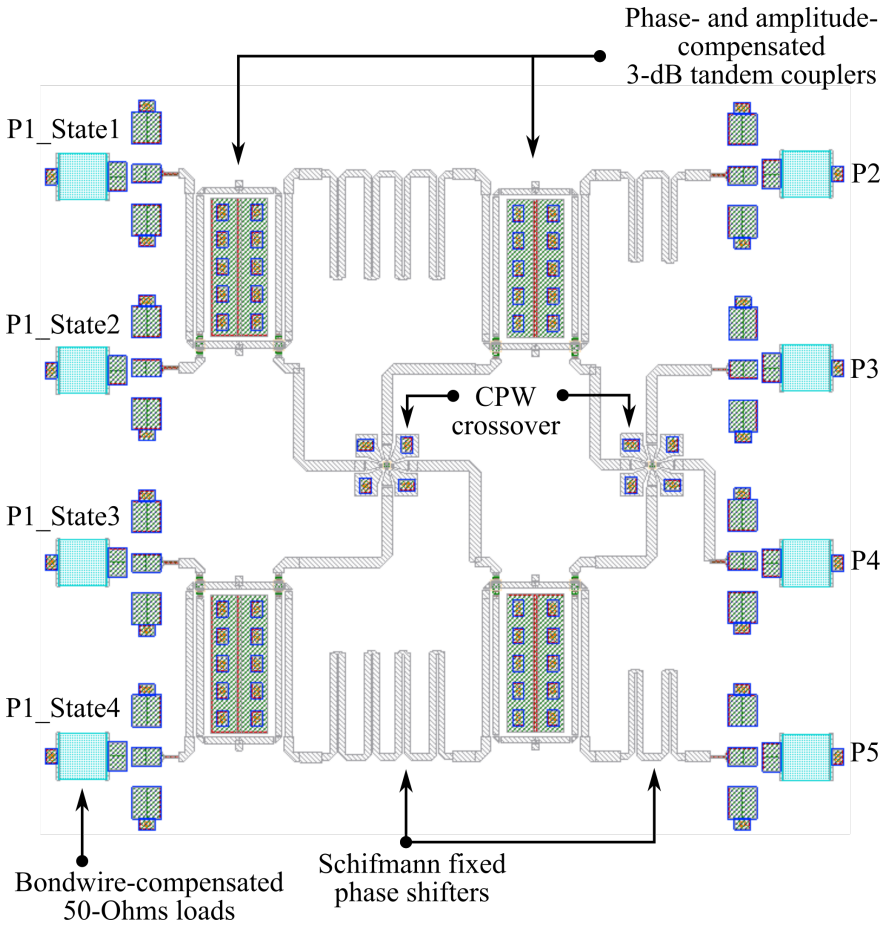


Figure 5.6: Layout of the 4×4 Butler matrix showing the important elements: 3-dB hybrid couplers, crossover, compensated loads and Shiffman fixed phase shifters (not discussed here in detail). The chip size is 2.5 mm by 2.5 mm.

impedance. The final resistor size is 150μm × 150μm. Additional compensation for the GSG pads is done with the thin inductive microstrip line between the pads and the couplers to compensate for the capacitance of the probe pads.

5.3 On-chip Butler Matrix Measurement Results

Two 150-μm pitch probes connected to two ports of a vector network analyzer are used for characterization. One probe is connected to one of 4 inputs (Port 1 States 1, 2, 3, or 4) and the other to one of the outputs (Port 2, 3, 4, or 5) as seen on the left and right sides respectively in Fig. 5.6 and the fabricated 2.5 mm by 2.5 mm GaAs chip in Fig. 5.7. The other 6 GSG pads are wire-bonded to their local on-chip terminations previously

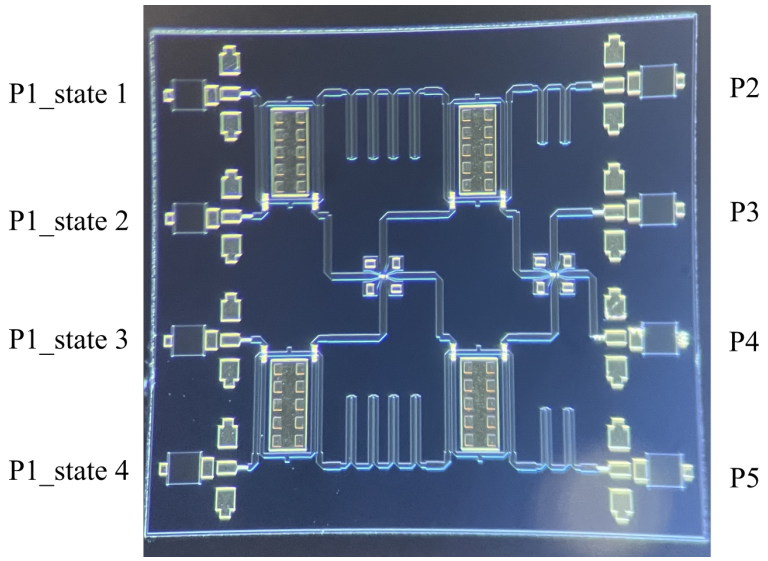
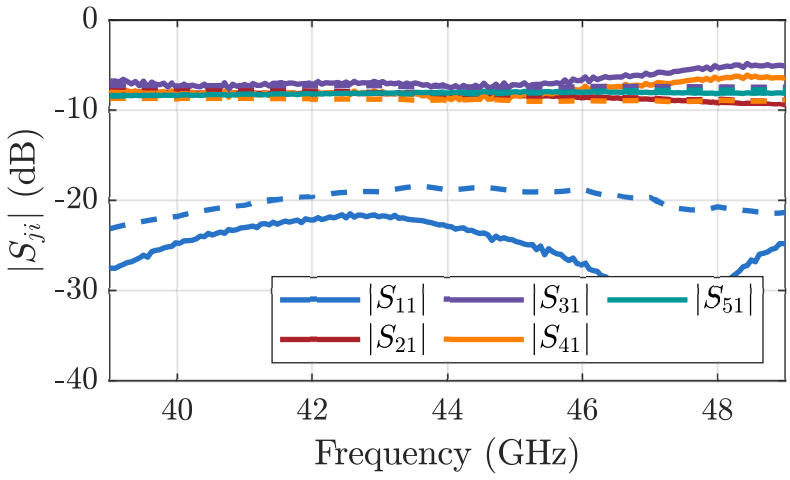


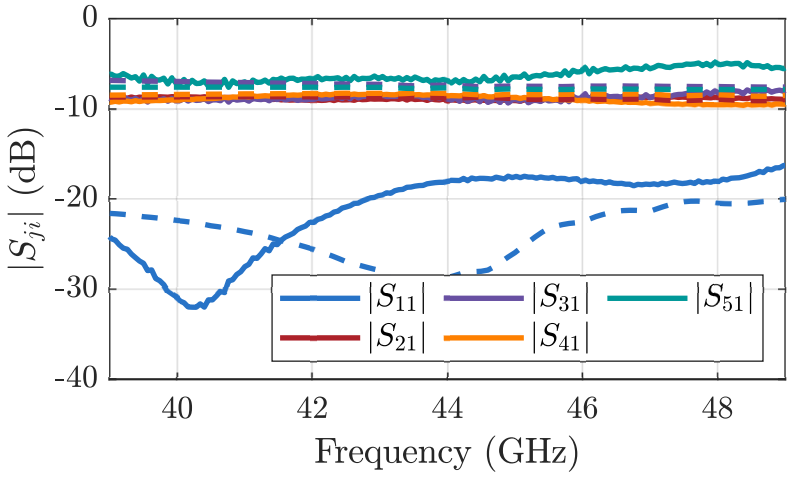
Figure 5.7: Photo of the fabricated GaAs 4×4 Butler matrix. The chip size is 2.5 mm by 2.5 mm. The input ports (P1) are on the left with the 4 output ports (P2-P5) on the right. There are four possible states depending on which input is excited. For each state, all four output ports have approximately the same magnitude signal with a different phase progression, i.e. ±45°,±135°.

described. The measured versus simulated performance when exciting the outside port P1 State 1, are shown in Fig. 5.8(a) for magnitude and Fig. 5.9(a) for progressive phase shift (PPS), while the performance for port P1 State 2 excited is shown in Fig. 5.8(b) and Fig. 5.9(b).

In State 1, the simulated match is better than -18.3 dB, and the measured match is better than -21 dB, with both simulated and measured insertion loss of 2.1 dB. In this state, the simulated amplitude imbalance is less than 0.8 dB, while the measured value is less than 0.7 dB. The progressive phase error for both simulations and measurements in this state is 10°. In State 2, the simulated match is better than -20 dB, while the measured match degrades slightly (below -16.5 dB). In this state, the insertion loss increases in measurement to 2.4 dB. We believe this is partly due to the mounting and uneven bondwire lengths to the loads. In State 2, the amplitude imbalance increases between simulation and measurements from less than 0.8 dB to less than 1.5 dB, while the maximum progressive phase error increases from 3.8° to 6.3°. Taking a 2 GHz bandwidth from 43-45 GHz, the return loss is greater than 18 dB, the insertion loss is less than 2.4 dB, the progressive phase error is less than 19° and the amplitude imbalance is less than 1.6 dB.



(a)



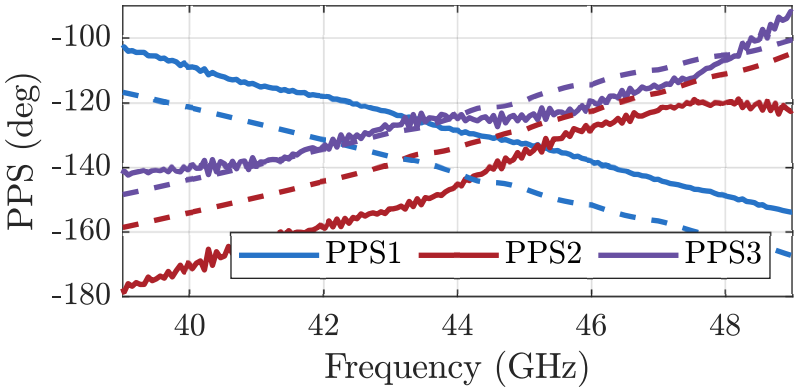
(b)

Figure 5.8: Magnitude of S-parameter performance for States 1 (a) and 2 (b). Simulated performance is shown in dashes, and measured performance is shown in solids.

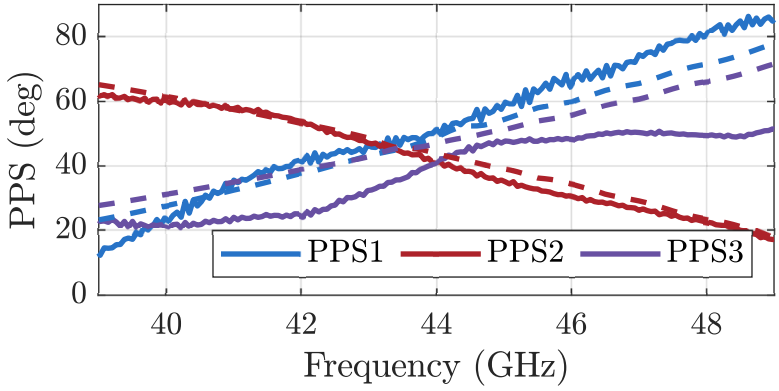
5.4 Beamforming for a Patch Antenna Array

Butler matrices are beamforming networks so their behavior in an antenna array is an important consideration. First, an antenna array factor (AF) is calculated from measurement outputs for the two excited ports (solid) and compared to the calculated AFs using the simulated outputs (dashed), shown in Fig. 5.10. The beam steering error between simulation and measurements is less than 0.5° at 44 GHz. The sidelobe levels are higher for the measured values of P_1 and the nulls are not as deep for either port.

To see how this works with a real antenna array, an example 4×1 patch antenna array is designed centered

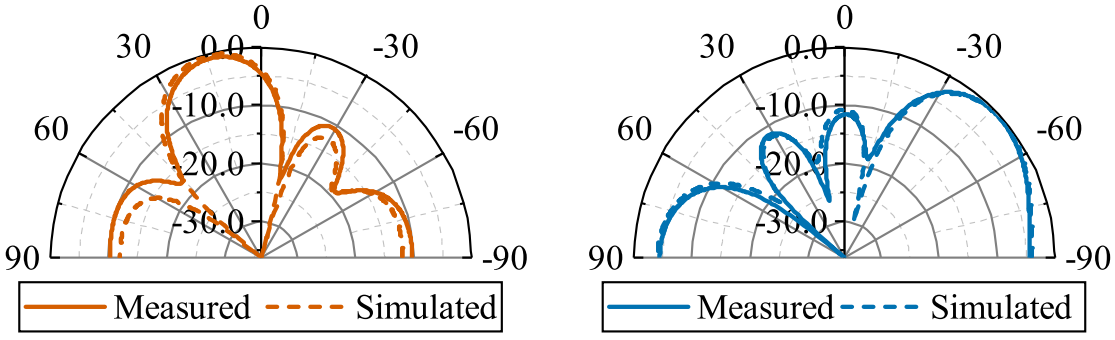


(a)



(b)

Figure 5.9: Simulated (dashed) and measured (solid) progressive phase shift (PPS) when exciting States 1 (a) and 2 (b). The -135° PPS and 45° are seen from States 1 and 2 as expected.



(a) (b)

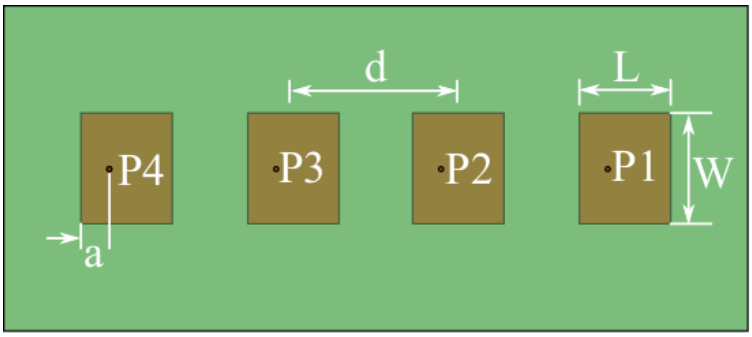
Figure 5.10: Generated normalized array factor from simulated (dashed) and measured (solid) results of the passive Butler matrix when (a) State 1 and (b) State 2 are excited. All AFs are normalized to the maximum value for the case when P_1 is excited.

Table 5.1: Active Impedances Presented at Each Port for Phase Progression Φ

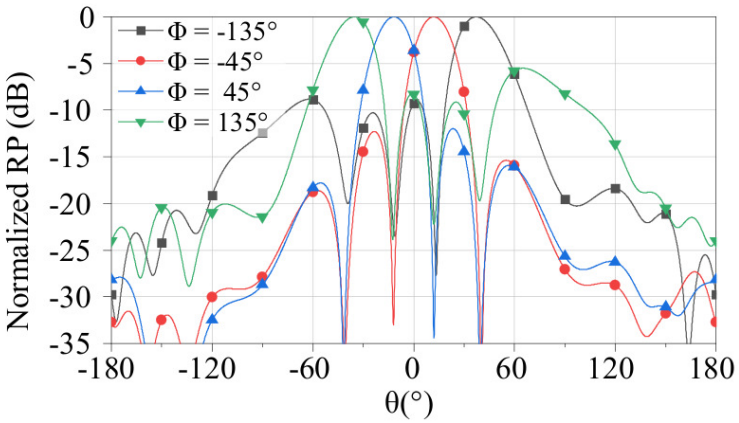
Φ	P1	P2	P3	P4
$-135°$	48-j12	41-j7	41-j1	45+j8
$-45°$	63	68+j11	70+j1	58+j8
$45°$	58+j8	69+j1	69+j12	63-j1
$135°$	46+j9	40	40-j7	48-j14

at 44 GHz in Ansys HFSS, as illustrated in Fig. 5.11(a). The array is designed on a Rogers RT/Duriod 5880 substrate of thickness 0.3 mm and a 0.5 mm thick aluminum reflector backing with four identical probe-fed antennas with dimensions $L = 2.03$ mm long and $W = 2.49$ mm wide, spaced $d = 3.88$ mm apart and with a off-center feed at $a = 0.5$ mm. Rogers RT/Duriod 5880 is a low-loss PTFE composite microwave substrate with a relative permittivity of 2.2 that has used into the millimeter-wave frequencies for antenna fabrication, e.g. [172–174]. The resulting radiation patterns at each of the ideal PPS is shown in Fig. 5.11(b). For each PPS, the corresponding active impedances at all four ports, shown in Table 5.1, and the Butler matrix beamformer scattering parameters are used as an excitation of the array elements, resulting in radiation patterns that take into account mutual coupling as a function of scan angle, Fig. 5.12. For States 1-4, beam steering and realized gain have values of (37°, 14.4 dB), (-13°, 21.4 dB), (13°, 20.0 dB) and (-34°, 14.4 dB), respectively.

Butler matrices are multi-beam beamforming networks. To demonstrate this capability, a simulation in Cadence Microwave Office is performed where State 1 is excited at 44 GHz with 30 dBm power and then States 2, 3, or 4 are also excited at 45 GHz with 30 dBm power. The leakage between the paths and output at each of the four output ports are simulated. This is then used to excite the four patch antennas of the array and generate the radiation patterns shown in Fig. 5.13 for when States 1 and 2 (left), 1 and 3 (middle), and States 1 and 4 (left) are simultaneously excited. While there is some variation due to the non-ideal leakage compared to the ideal excitations at a single frequency, two distinct beams are formed, one at 44 GHz and one at 45 GHz as expected from a multi-beam network.



(a)



(b)

Figure 5.11: Simulated 4 × 1 patch antenna array designed on Rogers RT/Duroid 5880. (a) Layout. (b) Radiation patterns simulated for ideal phase progression.

5.5 Conclusion

In summary, this chapter demonstrates a 44-GHz MMIC 4-beam on-chip InGaAs Butler matrix beamforming network that is integratable with active elements such as amplifiers and phase shifters. A typical beamforming network at this frequency would require a phase shifter as well as a power divider. A comparison with published on-chip phase shifters around 40 GHz is given in Table 5.2. Compared to these phase shifters, while having a larger phase imbalance, this circuit has lower insertion loss with and a larger available phase shift, though fewer available phase shift settings. The values in the table are just for the phase shifters and do not include a power divider which would increase and insertion losses and could also affect the listed phase and amplitude imbalances. Additionally, this circuit can handle more power than silicon implementations.

For a design in two metal layers in GaAs, a compensated crossover is designed that keeps the coupling

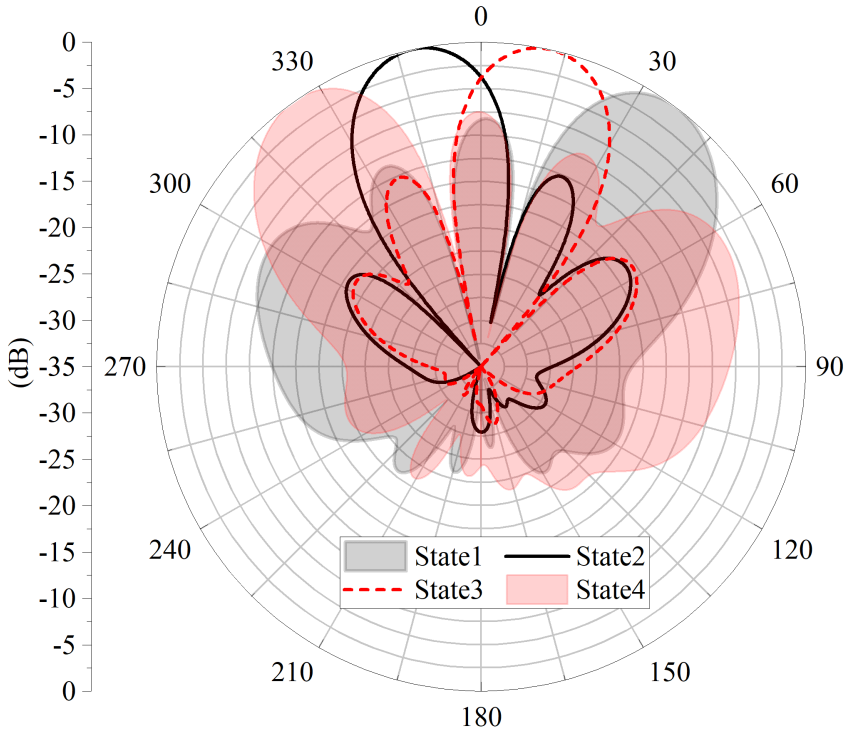


Figure 5.12: Simulated normalized radiation patterns for each of the 4 states of the full Butler matrix with the patch antenna array. Beam steering of 37°, -13°, 13°, -34° is achieved for States 1-4 respectively.

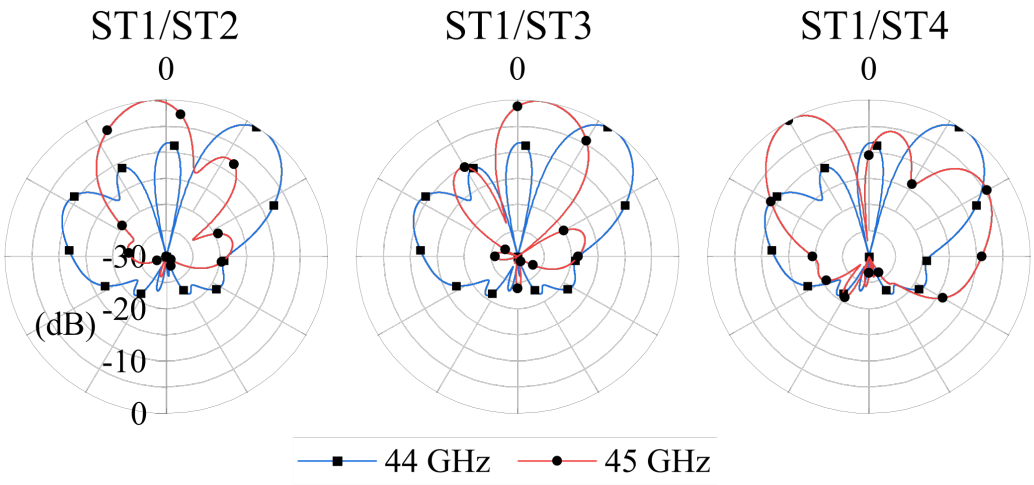


Figure 5.13: Simulated radiation patterns when State 1 is excited at 44 GHz and State 2 (ST1/ST2), 3 (ST1/ST3), and 4 (ST1/ST4) are excited at 45 GHz. Two distinct beams are successfully created while leakage exists between the paths, affecting performance.

below −30 dB and match better than −28 dB, respectively. The phase shifts are implemented with multiple coupled-line sections and tandem couplers. On-wafer measurements on a 2.5 mm by 2.5 mm chip show an insertion loss of 2.4 dB and match better than 16.5 dB with amplitude imbalance and phase error of 1.5 dB

Table 5.2: Performance of discrete millimeter-wave phase shifters.

Ref.	Process	Freq. (GHz)	Phase Shift	IL (dB)	$\Delta°$	ΔA (dB)
[175]	CMOS	36–40	360	20.2	2.6*	2.6*
[176]	CMOS	37–40	360	9.3	8*	0.6*
[177]	CMOS	37–40	202	11	4.1*	0.3*
[178]	InGaAs	31–40	360	8.8	4.7*	0.6*
This'	InGaAs	43–45	405	2.4	19	1.6

*root mean square error, 'includes power divider

and 10.8°. A narrowband patch antenna array is designed on Rogers RT/Duroid 5880 to show the measured beamformer performance effect on simulated radiation patterns. Steering of 37°, -13°, 13°, -34° is achieved for exciting States 1-4 respectively. When two States are simultaneously excited, the distinct beams are still present. This passive beamformer can be integrated with HEMTs in the same process to provide switching, amplification and mismatch compensation.

Compared to the two Butler matrices from the previous chapter, this chip takes into consideration the measurement problem of an 8-port circuit with the on-chip terminations making for more straightforward measurements after wire-bonding. Even more so than the heterogeneous integration process, active integration is a logical next step as active components can be designed in this MMIC process. But, while this chip is much smaller than the previous examples, the bandwidth is much narrower. A possible solution to this bandwidth problem is introduced in the next chapter.

The work in this chapter is published in [179].

Chapter 6

Frequency Tunable MMIC Butler Matrix

The last two chapters have introduced a variety of implementations of Butler matrices. The on-chip implementation in Chapter 5 has significantly smaller bandwidth than the previous examples. This chapter introduces a novel approach to increase bandwidth by introducing an active element integrated directly into the beamformer so that the circuit has frequency tunability. This tunability decreases the phase error and thus the beamsteering error of the array. This is implemented on a GaAs substrate, process 3 from Table 2.1.

6.1 Active Butler Matrix Introduction

As introduced in the previous chapters, there have been many examples of Butler matrices at various frequencies, including on-chip examples. Many of these on-chip circuits directly integrate switches as part of the beamforming network to select one of the inputs, e.g. [165, 167, 169]. Active components integrated in the Butler matrix can improve performance as demonstrated in [180], where an original phase error of 22° is corrected by using phase shifters at each output. A different approach is shown in [181], where a tunable power dividing network at the inputs is used to excite multiple inputs simultaneously, and the total output is a weighted sum of the inputs which allows beamsteering. A similar approach is shown in [182] which also introduces phase shifters in addition to a reconfigurable power dividing network for continuous beam steering. Other examples of modified active Butler matrices with continuous beamsteering are seen

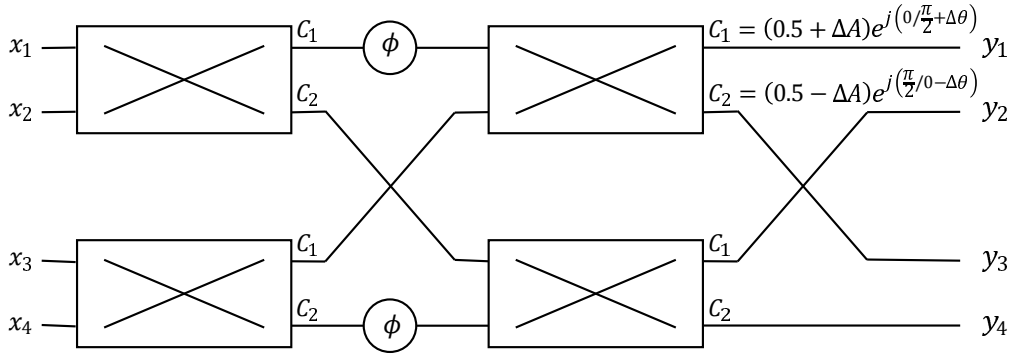


Figure 6.1: Block diagram of 4×4 Butler matrix. Input are x_1, x_2, x_3, and x_4 with outputs y_1, y_2, y_3, and y_4. The transfer function for the couplers' through path is $C_1 = (0.5 + \Delta A)e^{j\Delta\theta}$ and the coupled path is $C_2 = (0.5 - \Delta A)e^{j(\pi/2-\Delta\theta)}$. The phase shift behavior is given by Φ.

in [183–185], where phase shifters are introduced on each output, and in [186], where phase shifters are also embedded within the Butler matrix as well as at the outputs.

Active components can also be used to increase the numbers of beams. In [187], the couplers are reconfigurable to have different phase differences so that the possible number of output beams is three times greater than in a traditional Butler matrix. Another example uses switched phase shifters in the middle and at the output ports to make a 4×4 Butler matrix have an option for 8 beams, normally requiring a larger 8×8 Butler matrix [188]. Similarly, in [189], there are four possible sets of four output beams that can be chosen using phase shifters at the outputs of a static 4×4 Butler matrix.

This chapter focuses on an integrated circuit beamformer that, instead of steering tunability, has frequency tunability from a phase shifter inserted into the middle of the Butler matrix and first introduced in [190]. Frequency tuning allows for lower phase imbalance across frequency, reducing beam steering error. This can be compared to the example from the previous chapter operating at 44 GHz.

6.2 Single-Frequency Butler Matrix Operation

First, the general operation of a Butler matrix at a single frequency is presented. Referring to Fig. 6.1, a 4×4 Butler matrix can be analyzed in transmit mode as follows. The output values of $\underline{y}_i$ can be found by tracing the paths from each of the inputs x_1, x_2, x_3, and x_4:

$$y_1 = C_1 e^{j\Phi} C_1 x_1 + C_2 e^{j\Phi} C_1 x_2 + C_1 C_2 x_3 + C_2 C_2 x_4 \tag{6.1}$$

$$y_2 = C_2C_1x_1 + C_1C_1x_2 + C_2e^{j\Phi}C_2x_3 + C_1e^{j\Phi}C_2x_4 \tag{6.2}$$

$$y_3 = C_1e^{j\Phi}C_2x_1 + C_2e^{j\Phi}C_2x_2 + C_1C_1x_3 + C_2C_1x_4 \tag{6.3}$$

$$y_4 = C_2C_2x_1 + C_1C_2x_2 + C_1e^{j\Phi}C_2x_3 + C_1e^{j\Phi}C_1x_4 \tag{6.4}$$

where C_i are complex constants that depend on frequency and x_i and y_i are also in general complex. The phase shift, Φ, does not have magnitude. Note the symmetry between (1) and (4) as well as between (2) and (3) where the coefficients are flipped between the input elements. The 3-dB couplers' behavior includes an amplitude imbalance, ΔA and a phase imbalance $\Delta\theta$.

In receive mode operation, assuming no imbalances in the coupler (ΔA=0,$\Delta\theta$=0) and a phase shift $\Phi = 45°$, the input values can be found from

$$\begin{pmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{pmatrix} = \begin{pmatrix} e^{j\pi/4} & e^{j\pi/2} & e^{j3\pi/4} & e^{j\pi} \\ e^{j3\pi/4} & e^{j0} & e^{j5\pi/4} & e^{j\pi/2} \\ e^{j\pi/2} & e^{j5\pi/4} & e^{j0} & e^{j3\pi/4} \\ e^{j\pi} & e^{j3\pi/4} & e^{j\pi/2} & e^{j\pi/4} \end{pmatrix} \begin{pmatrix} y_1 \\ y_2 \\ y_3 \\ y_4 \end{pmatrix} \tag{6.5}$$

If we apply the values to y_i for an expected output phase progression, i.e. ±45°, ±135°, we find that only a single input port has a non-zero value, as expected. For example, let $y_1 = e^{j0}$, $y_2 = e^{-j\pi/4}$, $y_3 = e^{-j\pi/2}$, and $y_4 = e^{-j3\pi/4}$, for a phase progression of 45°. Substituting these into the above equations gives

$$x_1 = \frac{1}{4}(e^{j\frac{\pi}{4}} + e^{j\frac{\pi}{4}} + e^{j\frac{\pi}{4}} + e^{j\frac{\pi}{4}}) = 1 \tag{6.6}$$

$$x_2 = \frac{1}{4}(e^{j\frac{3\pi}{4}} + e^{-j\frac{\pi}{4}} + e^{j\frac{3\pi}{4}} + e^{j\frac{\pi}{4}}) = 0 \tag{6.7}$$

$$x_3 = \frac{1}{4}(e^{j\frac{\pi}{2}} + e^{j\pi} + e^{-j\frac{\pi}{2}} + e^{j0}) = 0 \tag{6.8}$$

$$x_4 = \frac{1}{4}(e^{j\pi} + e^{j\pi} + e^{j0} + e^{j0}) = 0 \tag{6.9}$$

Similar analysis can be done for the other three expected phase progressions to excite input ports 2-4.

These equations can be written in the summation form as

$$x_n = \frac{1}{N}\sum_{k=1}^{N} e^{j\frac{\pi}{N}(2k-1)n}y_k \tag{6.10}$$

The Butler matrix is compared to the Discrete Fourier Transform (DFT), specifically the Fast Fourier Transform (FFT) with a modified butterfly diagram as shown [191] and first noted in [192]. Transforms are mathematical techniques used to solve problems indirectly by translating them into a different domain. The Laplace transform, which transforms a problem into the "s" domain, is commonly the first introduced to engineers and mathematicians. The Fourier transform, $\mathcal{F}(t)$, converts a continuous signal from the time domain to the frequency domain, utilizing the fact that all signals can be decomposed into a sum of sinusoids.

The Discrete Fourier Transform (DFT) transforms a discrete-time signal into discrete frequency signals (unlike the Discrete Time Fourier Transform, which converts a discrete, sampled time signal into a sum of continuous frequency signals). The definition of the DFT is

$$A_k = \sum_{n=0}^{N-1} e^{-j\frac{2\pi}{N}kn} a_n \tag{6.11}$$

where A_k is the output in the discrete frequency domain, n is the index of the discrete time domain signal, N is the number of time domain samples, k is the discrete frequency domain index, and a_n is the time domain value at index n.

Similarly, the inverse discrete Fourier transform (IDFT) is defined as:

$$a_n = \frac{1}{4} \sum_{k=0}^{N-1} e^{j\frac{2\pi}{N}kn} A_k \tag{6.12}$$

Note, these definitions are nearly identical, except for the scaling factor when transforming back to the time domain and the change in polarity on the exponential.

To solve, the value in the summation can be calculated for all indexes k and n, commonly this part is notated

$$W_N^{kn} = e^{-j\frac{2\pi}{N}kn} \tag{6.13}$$

For a four-point DFT, the solution becomes,

$$W_4^{k*1} = e^{-j\frac{\pi k}{2}} \tag{6.14}$$

$$W_4^{k*2} = e^{-j\pi k} \tag{6.15}$$

$$W_4^{k*3} = e^{-j\frac{\pi 3n}{2}} \tag{6.16}$$

$$W_4^{k*4} = e^{-j2\pi n} \tag{6.17}$$

Using these equations, the outputs for all indices k can be found, note for $k = 0$, all values become $e^0 = 1$.

$$A_0 = e^0 a_0 + e^0 a_1 + e^0 a_2 + e^0 a_3 \tag{6.18}$$

$$A_1 = e^0 a_0 + e^{-j\pi/2} a_1 + e^{-j\pi} a_2 + e^{-j3\pi/2} a_3 \tag{6.19}$$

$$A_2 = e^0 a_0 + e^{-j\pi} a_1 + e^{-j2\pi} a_2 + e^{-j3\pi} a_3 \tag{6.20}$$

$$A_3 = e^0 a_0 + e^{-j3\pi/2} a_1 + e^{-j3\pi} a_2 + e^{-j9\pi/2} a_3 \tag{6.21}$$

Note, these outputs are sums of the inputs with an applied phase shift, just like a Butler matrix. When looking at the coefficients for each of the outputs, we can find the phase progression. For A_0 it is 0, for A_1 it is $-\pi/2$, for A_2 it is $-\pi$, and for A_3 it is $-3\pi/2$. A similar pattern is observed if the Inverse Discrete Fourier Transform (IDFT) is used to derive time-domain components from the frequency-domain summations.

Comparing the summation notation for the inputs of the Butler matrix, (6.12), to the IDFT definition, (6.14), reveals similar forms. Thus, the Butler matrix operates as a mapping similar to the Discrete Fourier Transform (DFT). Note that the indices differ due to the absence of an equivalent "dc" path in the Butler matrix, so the index starts at 1.

This analysis of the circuit in Fig. 6.1 is valid for a single frequency. In a practical implementation, the amplitude and phase imbalance vary over frequency and affect the progressive phase shift at the output.

Using the definitions for the through and coupled ports, and assuming all couplers have the same magnitude imbalance ΔA and phase imbalance $\Delta\theta$ as shown in Fig. 6.1, the first two output equations become

$$\begin{aligned} y_1 =& (0.5 + \Delta A)^2 e^{j2(\Delta\theta+\Phi)} x_1 + (0.5^2 - \Delta A^2) e^{j(\pi/2+\Phi)} x_2 \\ &+ (0.5^2 - \Delta A^2) e^{j\pi/2} x_3 + (0.5 - \Delta A)^2 e^{j(\pi-2\Delta\theta)} x_4 \end{aligned} \tag{6.22}$$

$$
\begin{aligned}
y_2 =&(0.5^2 - \Delta A^2)e^{j\pi/2}x_1 + (0.5 + \Delta A)^2 e^{j2\Delta\theta}x_2 \\
&+ (0.5 - \Delta A)^2 e^{j(\Phi + pi - 2\Delta\theta)}x_3 \\
&+ (0.5^2 - \Delta A^2)e^{j(\pi/2+\Phi)}x_4
\end{aligned}
\tag{6.23}
$$

These equations give the expected complex values at the output ports when any one or a combination of input ports is excited. Since this is a linear system, the output of multiple excitations is the sum of the individual excitations.

The on-chip GaAs example from the last chapter demonstrates the frequency limitations for Butler matrices as the phase error quickly increases away from the center frequency of 44 GHz. The bandwidth limitation of the Butler matrix is the phase imbalance. Referring to (6.22) and (6.23), the phase imbalance introduced by the couplers is multiplied by two, while the amplitude imbalance, a number smaller than 1, is squared, so the frequency dependent behavior of the couplers phase impacts the overall performance more quickly than amplitude. For example, for an operating bandwidth of 2 GHz, from 43-45 GHz or 4.5% fractional bandwidth, the return loss values are greater than 15 dBm, the insertion loss is less than 2.4 dB, the phase error is 19°, and the amplitude imbalance is less than 1.6 dB.

6.3 Bandwidth Considerations

To evaluate beamforming performance over frequency, a Butler matrix is simulated using the frequency-dependent amplitude and phase imbalance of an ideal branchline coupler and phase dependence of an ideal Schiffman phase shifter. For 30% bandwidth, the output port values are shown in Fig. 6.2 when input ports P_1 and P_2 are excited. Variations in phase and magnitude are observed for each output port, resulting in increasing magnitude imbalance and changes in the progressive phase shift. The values of the outputs are used to excite array elements, and the generated array factors for $0.85f_0$, f_0, and $1.15f_0$ are shown in Fig. 6.3 for input ports P_1 and P_2 excited. At the edges of the band, phase and magnitude imbalances decrease null depth, increase sidelobe levels, and cause beamsteering angle errors up to 2°.

Real implementations also have non-ideal connections between elements, that is there are lengths of

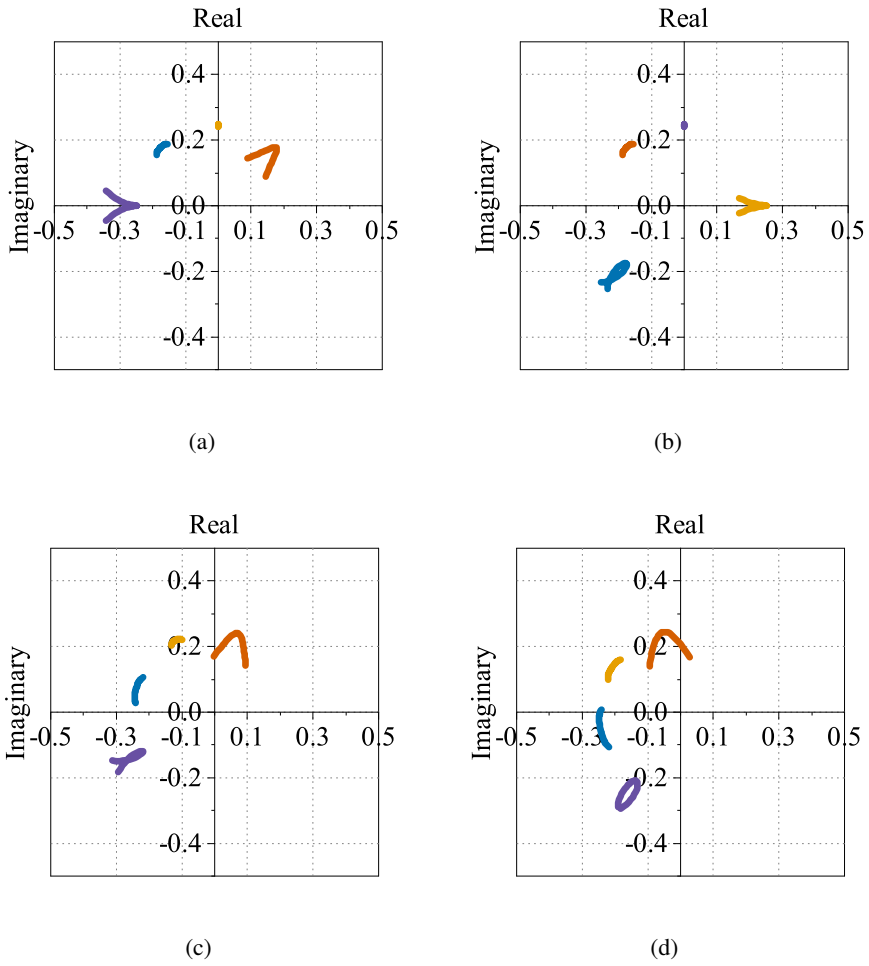


Figure 6.2: The output values over 30% bandwidth when (a) P_1 and (b) P_2 and when P_1 is excited adding (c) 0.5λ lines and (d) 1.0λ lines along each path.

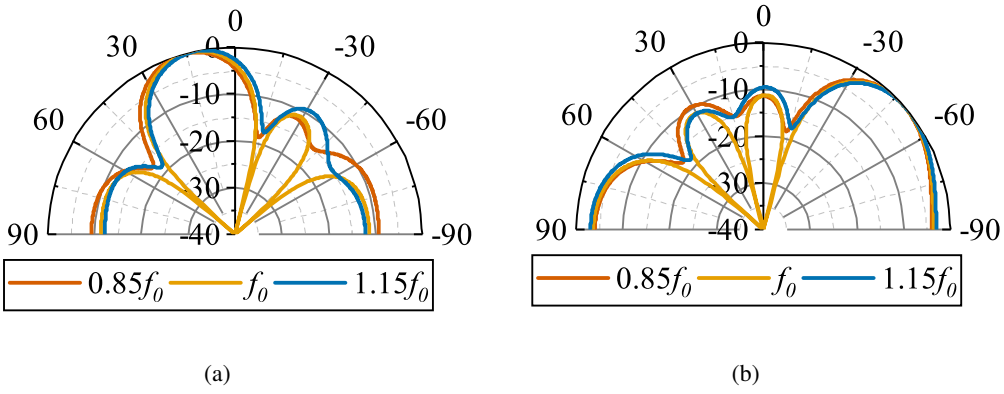


Figure 6.3: The generated array factors when (a) P_1 and (b) P_2 are excited individually for a Butler matrix using ideally simulated hybrid couplers and Schiffman phase shifters at the normalized frequency of operation, f_0, $0.85f_0$, and $1.15f_0$.

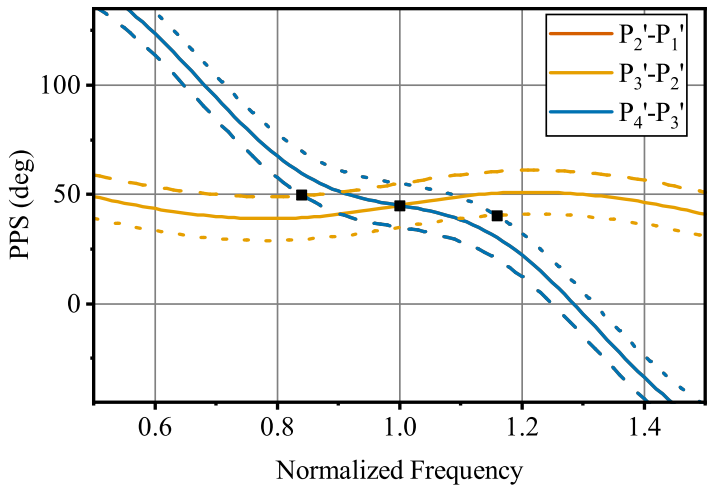


Figure 6.4: The progressive phase shift at the output ports P_1'-P_4' when exciting input port P_1 while changing the value of phase shift, Φ with extra line length 0.5λ on each path. The base case, when Φ=45° is shown in solid, with Φ=35° in dotted line and Φ=55° in dashed line.

transmission line. Adding these additional transmission line lengths also introduces frequency-dependent phase behavior. This can be observed in the output values in Fig. 6.2(c) and (d), shown over a 30% bandwidth, where line lengths of 0.5λ and 1.0λ are added to represent the connections. The added transmission lines cause a rotation around the origin and increasing changes in amplitude and phase for all four output ports. At the center of the band, the phase shift and amplitude remain the same.

The ideal transmission lines behave as true time delay elements. To compensate for the phase change, the phase shift Φ in the middle of the Butler matrix can be purposefully adjusted. By varying Φ from 35° to 55°, the overlap point of the progressive phase shift can vary from $0.85f_0$ to $1.15f_0$ as shown in Fig. 6.4. The corresponding PPS value varies from the ideal 45° to about 49° and 41° as Φ changes. This additional controllable phase shift can correct for phase error and therefore beam pointing error.

6.4 Reflective Phase Shifter

To utilize this phase control compatibility, a phase shifter that operates around 40 GHz is designed. The phase shifter must be broadband enough and provide sufficient phase shift to tune across the desired frequency range. Phase shifters are important components in many RF and millimeter-wave systems, not

just for beamsteering. Their applications include use in reflectometers, frequency translator, and amplifier linearization [33, 35–38, 40]. Common topologies for RF and millimeter-wave phase shifters include loaded lines, switched types, and reflective types. Loaded line phase shifters use series inductors and shunt capacitors to approximate the transmission line model. One of these elements, usually the shunt capacitor, is tunable and is used to change the effective length of the line. Switched type phase shifters consist of one or more bits, each with a reference path and an additional path that introduces the desired phase shift or delay. This additional path can be a simple length of transmission line or a combination of reactive elements. Reflective type phase shifters, the topology used in this design, employ a hybrid coupler with the through and coupled ports terminated in reflective loads, either switched or continuously tunable. Phase shifters can be discrete, also known as digital, with a set number of states, or continuous, also known as analog, with tunable components can be set to any value within the tuning range. Switched type phase shifters are always discrete, while loaded line and reflective types can be either discrete or continuous. Another type of phase shifter used in on-chip implementations is the active sum or vector modulator, demonstrated in millimeter-wave CMOS in [40].

Continuous phase shifters demonstrated at millimeter wave frequencies include a loaded-line CMOS phase shifter at 60 GHz [193] and a 20-40 GHz BiCMOS implementation [194]. Reflective phase shifters have been demonstrated in CMOS [195–198] and BiCMOS [199, 200], as well as in GaN MMIC [44] and MEMs [201] technologies. A summary of continuous phase shifters, specifically near 40 GHz, is given in Table 6.1. In general, there is a tradeoff between bandwidth, phase shift, and insertion loss (IL). A phase shifter cannot simultaneously achieve large bandwidth, large phase shift, and small insertion loss with minimal variation.

To increase available phase shift for increased beam steering, two reflective phase shifters can be cascaded [44, 201]. Another approach to increase phase shift is to combine digital bits with smaller continuous phase shifters as done in [203, 205]. This results in increased phase shift but also larger chip sizes and increased bias complexity. In phased arrays, phase shifters are typically placed before power amplifiers, however linearity remains an important metric. Reported power handling linearity of CMOS continuous phase shifters includes examples that with P1dB ranging from -9 to 0 dBm [197] and one with P1dB above

Table 6.1: Performance of continuous millimeter-wave phase shifters.

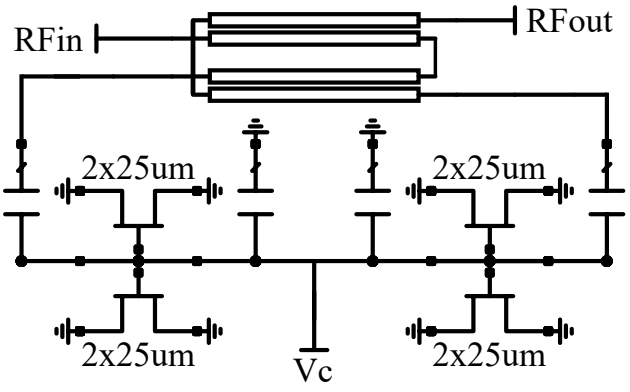
Ref.	Process	Freq. (GHz)	Phase Shift	IL (dB)
[202]	CMOS	40–75	360°	18±2
[196]	CMOS	25–43	180°	9.1±2.5
[197]	CMOS	38	161°	1.45±0.35
[198]	CMOS	39	410°	10.3±8.5
[200]	BiCMOS	30–50	60°	5±1
[203]	BiCMOS	14–54	180°	9.1±3.1
[201]	MEMs	15–45	123°	3.6
[204]	GaAs	37–42	360°	12.8
[44]	GaN	50–110	149°	10±4
This	GaAs	38–46	80°	3.8±1.5

4 dBm [195]. A GaN example demonstrated much higher linearity with P1dB as high as 24 dBm at W band [206].

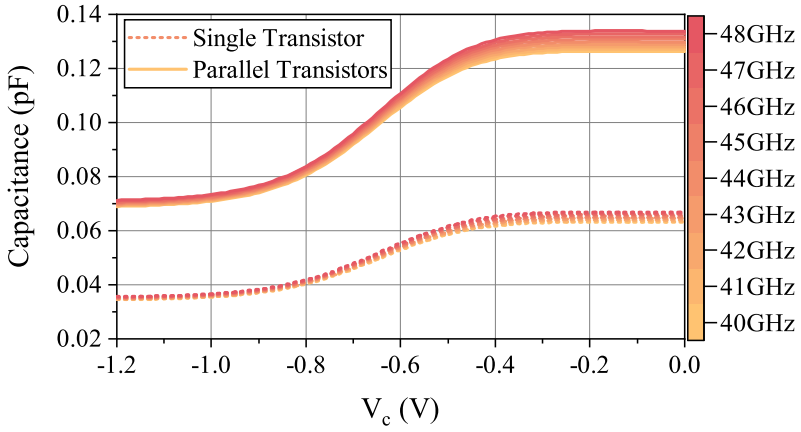
A continuous reflective type phase shifter is designed for use in a frequency-tunable GaAs MMIC Butler matrix feed network. The circuit diagram is shown in Fig. 6.5(a), where coupled lines are connected in tandem for the hybrid coupler and two shunt 2×25 μm transistors are used for the reflective loads on each port. The amount of phase shift is proportional to the change in the reflective load. The capacitance of available transistors in the process is simulated using foundry models with the drains and sources grounded. While transistors with larger periphery have a larger capacitance value as well as more capacitance variation, their size makes them difficult to integrate. Therefore, two smaller transistors are connected in parallel. The resulting capacitance for a single HEMT and two parallel HEMTs across gate control voltage V_c is shown in Fig. 6.5(b). Using two transistors increases the total capacitance as expected and, more importantly, increases the capacitance variation across V_c which translates to more phase shift.

The final layout and a photo of the manufactured GaAs phase shifter are given in Fig. 6.6. The tandem coupler has the coupled line sections separated by a ground and short stubs on the connections to increase isolation and improve match. The shunt transistors are on the through and coupled ports connected to a single dc bias pad. Additional capacitors are used for RF and dc blocking.

The fabricated chip is measured on wafer using 150 μm probes, a probe station, and a PNA vector network analyzer calibrated with a Cascade Microtech alumina SOLT standard. The results from small-signal measurements (solid) and simulation results (dashed) are shown in Fig. 6.7 as V_c varies from −1.2 V to



(a)



(b)

Figure 6.5: (a) Circuit diagram of the reflective phase shifter where the through and coupled ports' load is two 2×25 μm source-drain grounded transistors in parallel. (b) Extracted capacitance from the foundry model for a single 2×25 μm transistor (dashed) and two 2×25 μm transistors in parallel (solid) varying V_c from −1.2 V to 0 V from 40-48 GHz.

0 V. From 38-46 GHz, the measured $|S_{11}|$ stays below -19 dB and the measured $|S_{21}|$ varies between -5.3 dB and -2.3 dB. The relative phase shift is compared to one edge of the control voltage band, V_c=0 V. The maximum relative phase shift peaks at 130° at 39 GHz and is the lowest at 75° at 46 GHz. Between 40 GHz and 44 GHz, where this phase shifter is used in the Butler matrix, the maximum relative phase shift varies from 126° to 93°. The simulations predict the trend in the measurements. The measured match improves compared to simulations, while the transmission coefficient variation slightly increases across the frequency range. The phase shift behavior shows a slight downward frequency shift; where simulations predict the maximum phase shift at 40 GHz, measurements show maximum phase shift at 39 GHz.

The behavior across input power is also measured using 150 µm probes, a probe station, a ZNA R&S

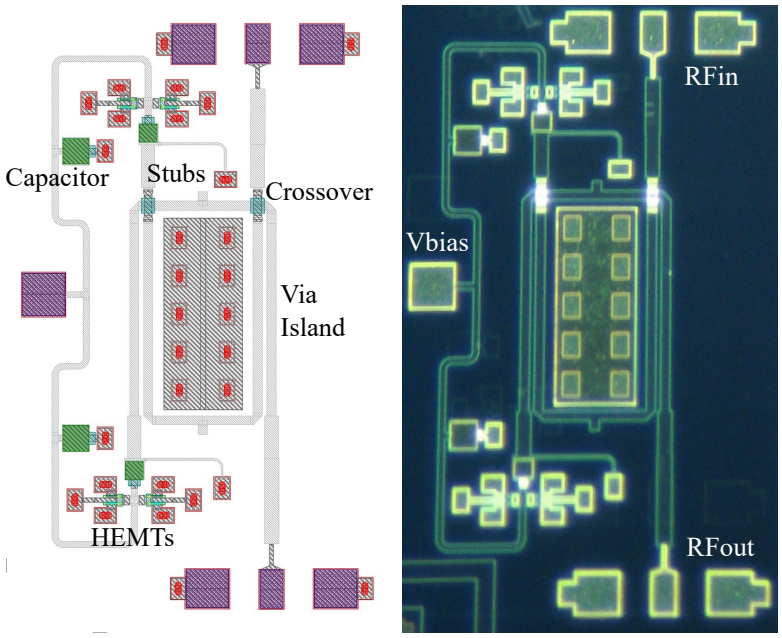
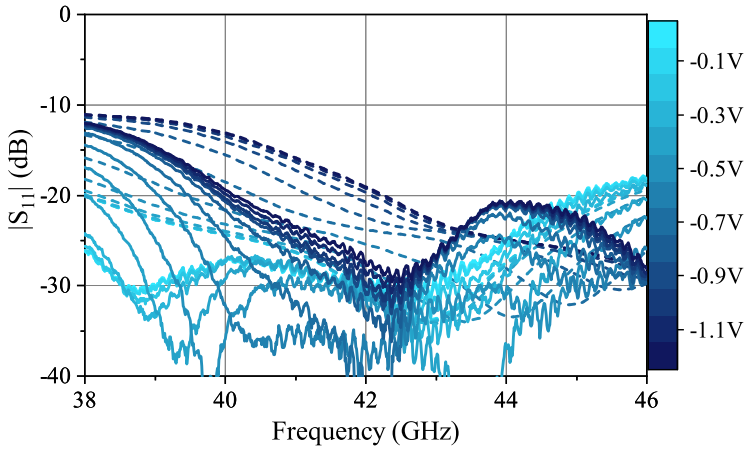


Figure 6.6: (a) Layout and (b) photograph of the 0.8 mm by 1.5 mm reflective phase shifter.

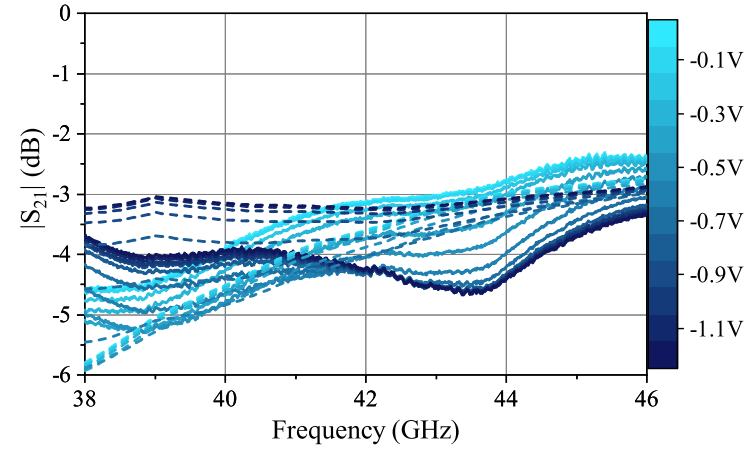
vector network analyzer, and a Mini-Circuits ZVA-24443G1 amplifier as the driver amplifier. Input power to the phase shifter chip is varied from -10 dBm to 10 dBm. Fig. 6.8 shows the simulated and measured relative phase shift at 40, 42, and 44 GHz while varying V_c and P_{in}, compared to the phase shift at the lowest input power setting, P_{in}=-10 dBm. As power increases, the variation also increases as expected. The phase shift variation is also greater at the edges of the range of V_c, though it swings in opposite directions at either edge. This indicates that, when considering absolute phase shift rather than relative phase shift, the phase shift becomes more linear across the control voltage. This behavior is due to the transistor becoming more resistive for higher input power. Similar plots can be generated for other frequencies in the 40 to 44 GHz range. Fig. 6.9 shows this behavior across frequency for maximum phase shift at 40 GHz, 42 GHz, and 44 GHz . As input power increases, the available phase shift decreases at all frequencies from 125°, 105°, and 88° to as low as 84°, 63°, and 55° for 40 GHz, 42 GHz, and 44 GHz, respectively.

As mentioned earlier, cascading reflective phase shifters can increase the available phase shift. A version with two cascaded phase shifters is also manufactured, as shown in Fig. 6.10. The base unit is identical to the one previously described, but now features two bias pads for dc bias.

The chip is measured for small signal performance, with relative phase shift behavior plotted in Fig. 6.11



(a)



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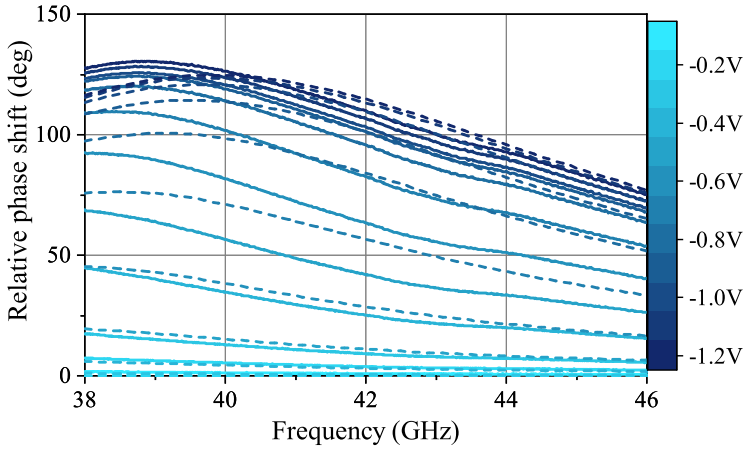


(c)

Figure 6.7: Measured and simulated S-parameter performance of the reflective phase shifter across frequency with various V_c settings (color bar) for (a) $|S_{11}|$, (b) $|S_{21}|$ and (c) phase shift relative to the phase shift at V_c=0 V.

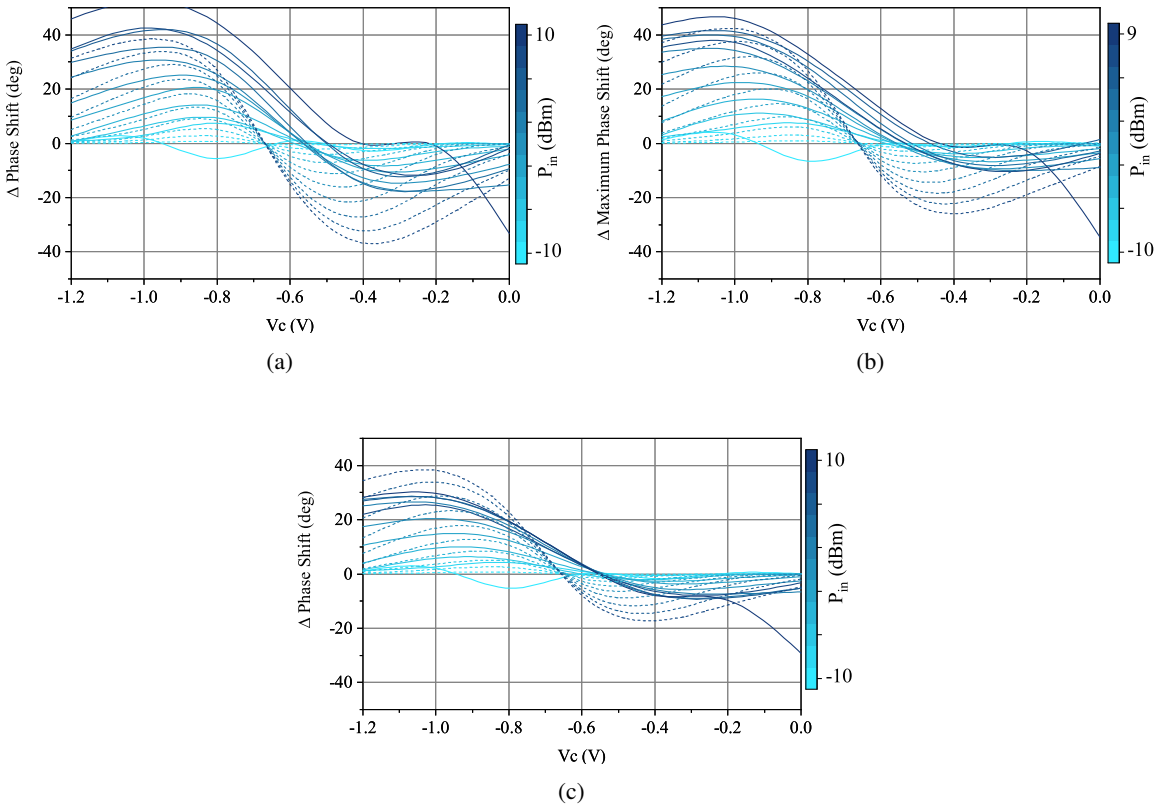


Figure 6.8: Measured (solid) and simulated (dash) change in phase shift across control voltage compared to the lowest input power (-10 dBm) at (a) 40 GHz, (b) 42 GHz, and (c) 44 GHz. Increasing input power increases the deviation from small signal operation.

for both biases set to the same control voltage V_c. The peak available phase shift increases from 130° in the single version to 249° in the cascaded version. Again, there is a slight shift down in frequency in the measured behavior, with an increase in the available phase shift. The match behavior is similar to that of the single version, dominated by the couplers, showing better than 12 dB across the measured bandwidth. Losses do increase and vary from -9.8 dB to -4.7 dB across frequency and bias.

6.5 Tunable Butler Matrix

To increase the frequency range while minimizing phase error as described in earlier, the phase shifter is integrated into a Butler matrix, with the final chip shown in Fig. 6.13 and a block diagram shown in Fig. 6.12. The individual components of this beamformer circuit design are the same as those used in the fixed version

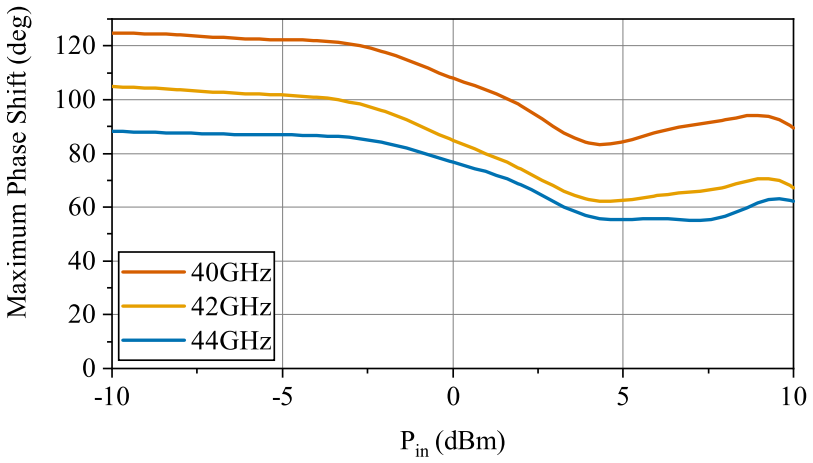


Figure 6.9: Maximum available phase shift at 40 GHz, 42 GHz, and 44 GHz over input power.

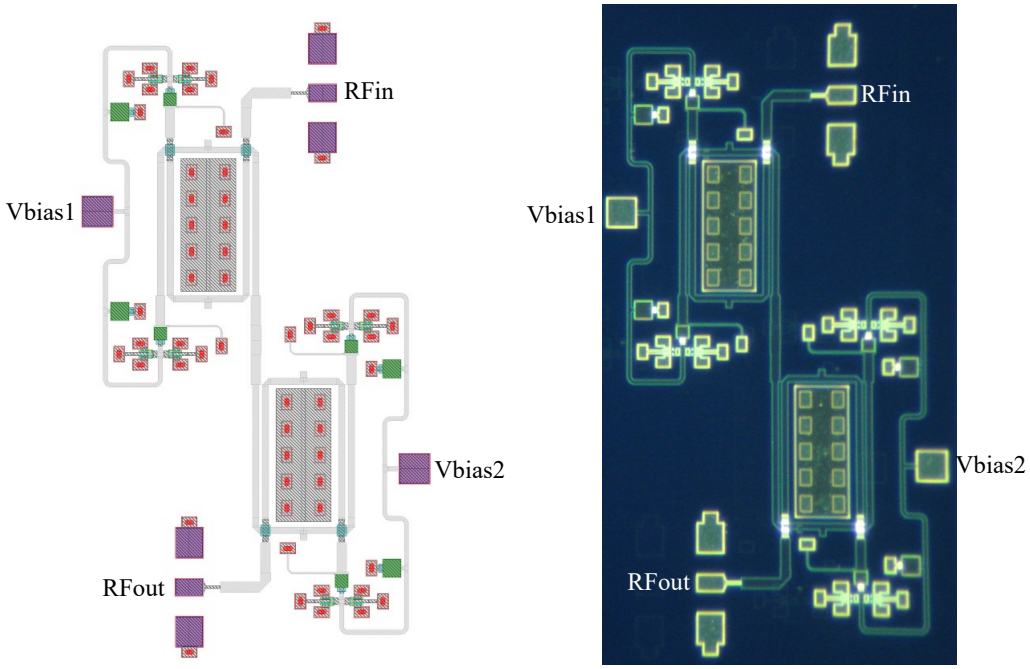


Figure 6.10: (a) Layout and (b) photograph of the manufactured cascaded reflective phase shifter.

presented in the previous chapter, with the addition of the already described phase shifter and attenuators in the crossed paths. The attenuator is fixed, with a value that compensates approximately the average loss of the phase shifter to help with amplitude balance. This tunable Butler matrix is first characterized in small-signal operation. If used in transmit mode, the power dependence is relevant and is examined in simulations.

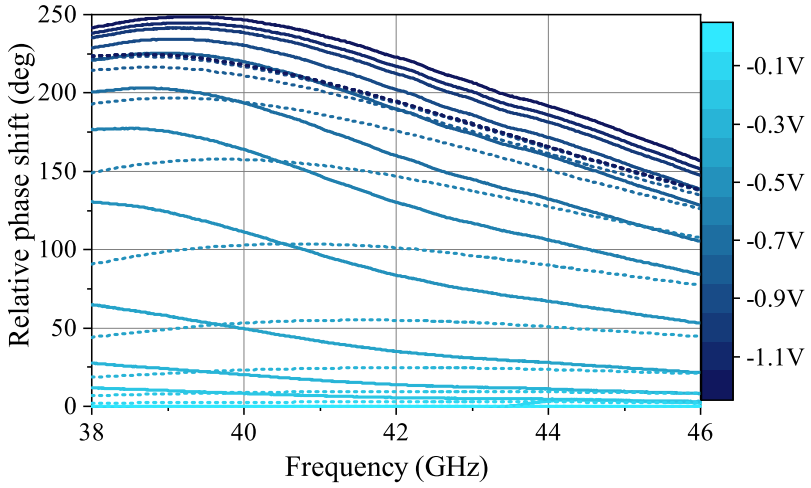


Figure 6.11: Simulated (dashed) and measured (solid) phase shift for the cascaded phase shifter relative to V_c=0 V.

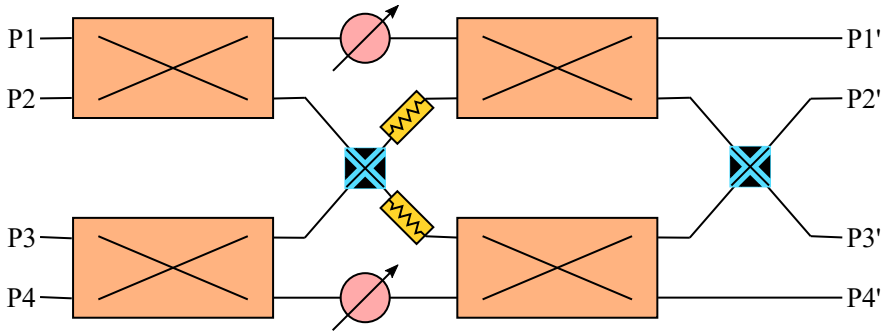
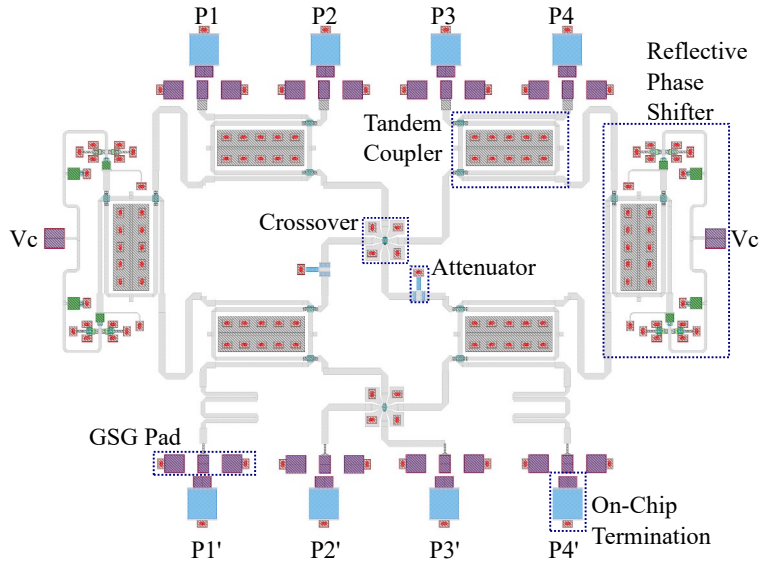


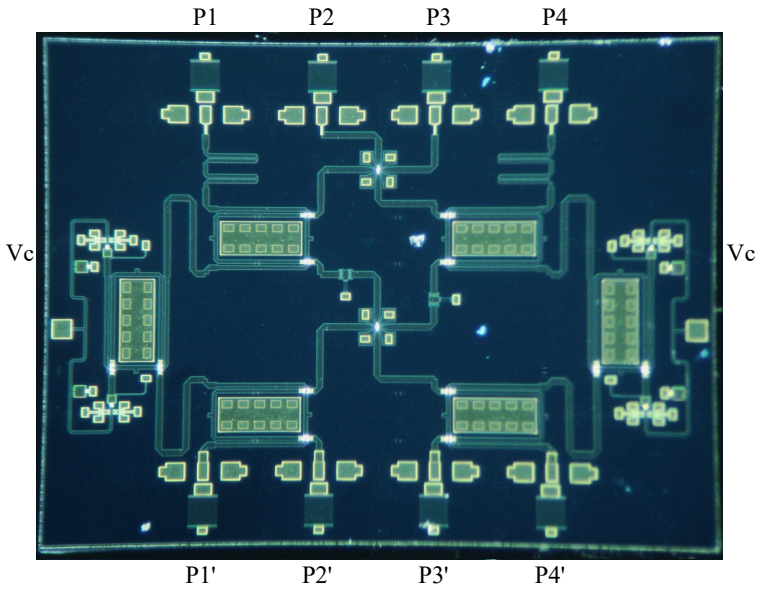
Figure 6.12: A block diagram of the 4×4 frequency-tunable Butler matrix beamforming network with input ports P_1-P_4 and output ports P_1'-P_4' with the individual components highlighted in different colors including the tandem hybrid couplers, the tunable phase shifters, the crossovers, and the attenuators.

6.5.1 Small-Signal Characterization

During two-port measurements of the tunable Butler matrix, the unused ports are wire-bonded to the on-chip 50 Ω terminations (refer to Fig. 6.13). Simulated and measured progressive phase shift (PPS) performance is presented in Fig. 6.14 for (a) $V_c = -0.2$ V and (b) $V_c = -1.0$ V when input port P_2 is excited, showing that simulations and measurements align for these control voltages. Ideally, the phase lines for each control voltage intersect at one frequency, and this frequency tunes with control voltage from 40 to 44 GHz. The circles in Fig. 6.14 indicate these cross-over regions for both simulated and measured PPS, showing that the tuning across frequency indeed happens. Table 6.2 shows simulated and measured frequency where the



(a)

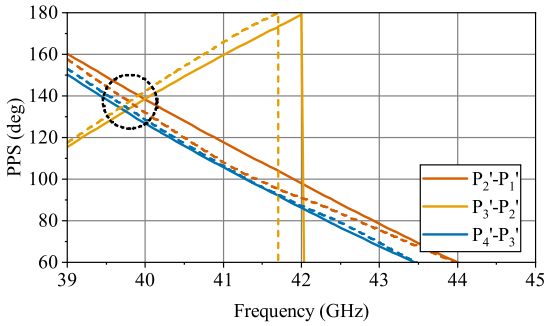


(b)

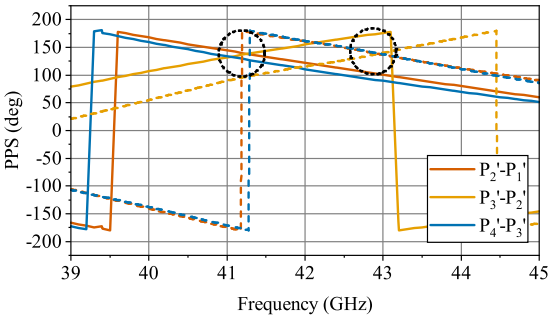
Figure 6.13: (a) Block diagram and (b) labeled photograph of the fabricated 2.68 mm by 3.6 mm tunable Butler matrix MMIC. The four inputs are labelled P_1, P_2, P_3, and P_4 with the outputs labelled P_1', P_2', P_3', and P_4'. Each output excites a different phase progression at the four output ports.

difference between the three phases between two outputs is minimized for several other control voltages. The values in the table, together with Fig. 6.14, show that the control voltage tunes the frequency of operation.

The reflection coefficient for the input port P_2, referred to as $|S_{11}|$, and the *thru* coefficients to the output ports P_1'-P_4', referred to as $|S_{j1}|$, are shown in Fig. 6.15 across frequency for different V_c values. There are more measured values of $|S_{11}|$ than simulated because all measurements are done as two-port



(a)



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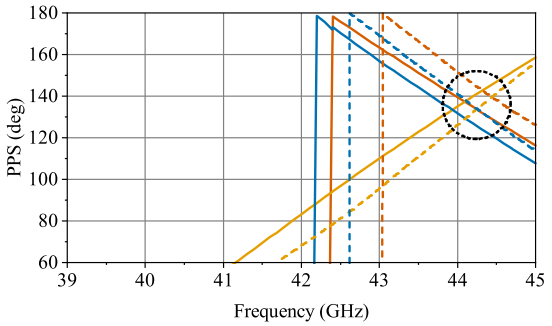


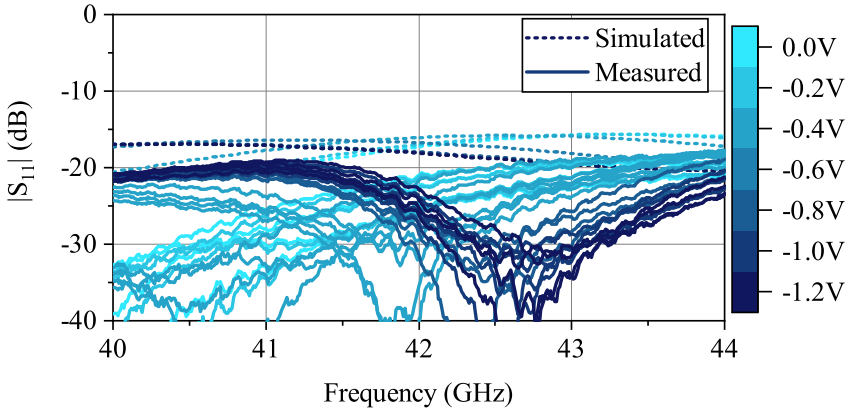
(c)

Figure 6.14: Simulated (dashed) and measured (solid) phase progression of the Butler matrix at (a) $V_c = -0.2$ V and (b) $V_c = -1.0$ V when P_2 is excited. The circles indicate the frequency region where all phase plots intersect, indicating the frequency of operation for the beamforming.

measurements, requiring multiple sets of measurements for each output port. In contrast, a single five-port simulation is performed. The measurements for all output ports and V_c settings remain below -18 dB, and are equal to or better than simulated values. For $|S_{j1}|$, there are the same number of simulated and measured values, one for each output port at each V_c setting. Measurements show an increase in loss at the lower V_c settings, compared to simulations, which increases the transmission loss variation. Measured $|S_{j1}|$ varies

Table 6.2: Frequency of operation and PPS for different V_c.

$\mathbf{V_c}$(V)	−1	−0.8	−0.6	−0.4	−0.2
Simulated f_0 (GHz)	44	43.1	41.2	40	39.8
Simulated PPS	135°	135°	134°	135°	137°
Measured f_0 (GHz)	44.3	43.9	43	40.4	39.7
Measured PPS	139°	134°	138°	136°	136°



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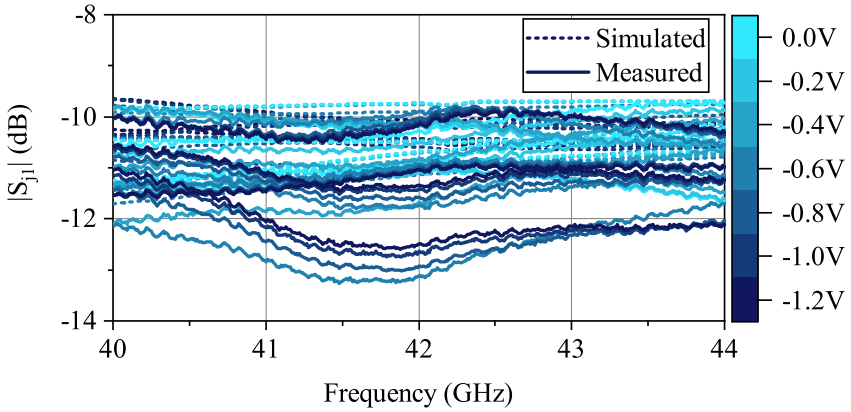


(b)

Figure 6.15: Simulated (dashed) and measured (solid) (a) $|S_{11}|$ and (b) $|S_{j1}|$ when exciting input port P_2. Voltage settings are shown in the same shade of blue. More values of $|S_{11}|$ are measured than simulated as there is a single five-port simulation for each voltage setting, while the measurements are done as separate two-port measurements.

from -13.3 dB to -9.4 dB, including the 6 dB splitting loss, so the transmission loss ranges from 7.3 dB to 3.4 dB, compared to simulation values ranging from 5.9 dB to 3.4 dB.

The output values from simulations and measurements are used to generate array factors in Fig. 6.16 for (a) $V_c = -0.2$ V at 40 GHz, (b) $V_c = -0.6$ V at 42 GHz, and (a) $V_c = -1.0$ V at 44 GHz. These patterns are

normalized to the maximum value generated in the simulated AF at 44 GHz. At 40 GHz, the beam steering angle error is under 0.5° for both measured and simulated values. At 44 GHz, the simulated value is under 0.5° while the measurement value under 1.5° as compared to the ideal excitation AF. The measured values show shallower first nulls due to increased amplitude imbalance. A larger discrepancy between simulation and measured AF values is observed at 42 GHz, as expected from the phase variation seen in Table 6.2. The beam steering angles vary by 5.5° from each other. The simulated and measured beam steering angles deviate from the ideal by −1° and 4.5°, respectively.

6.5.2 Power Dependence of Tunable Butler Matrix

The insertion loss characterized above in small-signal operation is relevant to receive-mode beamforming as it will affect the noise figure. In transmit mode, however, because of the active tuning element, we expect some dependence on input power. The nonlinear tunable phase shifter behavior with increased power is quantified in Section V and the simulations predict measured trends. Therefore, the foundry models are used to simulate the behavior of the entire Butler matrix across power, shown in Fig. 6.17. Three effects are quantified: (1) change in progressive phase shift with increased input power on the corresponding port; (2) leakage from the excited port in the three terminated (not excited) input ports; and (3) harmonic content at the output as input power increases from 0 to 20 dBm.

The change in magnitude and progressive phase shift (PPS) at the output ports while exciting input ports (a) P_1 and (b) P_2 is presented for three different V_c settings in Fig. 6.17. The input power variation from 0 and 20 dBm, is approximately equivalent to the -10 dBm to 10 dBm sweep used for characterizing the phase shifters, since the input signal passes through the 3 dB hybrid coupler before reaching the phase shifter. The magnitude at the output is affected by the tunable phase shifter only for the two ports whose paths include this nonlinear element, while the other two outputs show no significant change. At $V_c = -1.0$ V, the most pinched-off and therefore most nonlinear setting, the amplitude changes for lower input power levels but remains relatively constant as input power increases (around 16 dBm). In comparison, for $V_c = -0.2$ V, the magnitude changes significantly around 12 dBm. Fig. 6.17 also shows the change in progressive phase shift, which would affect the beam direction in an antenna array. The PPS is clearly affected by input power even

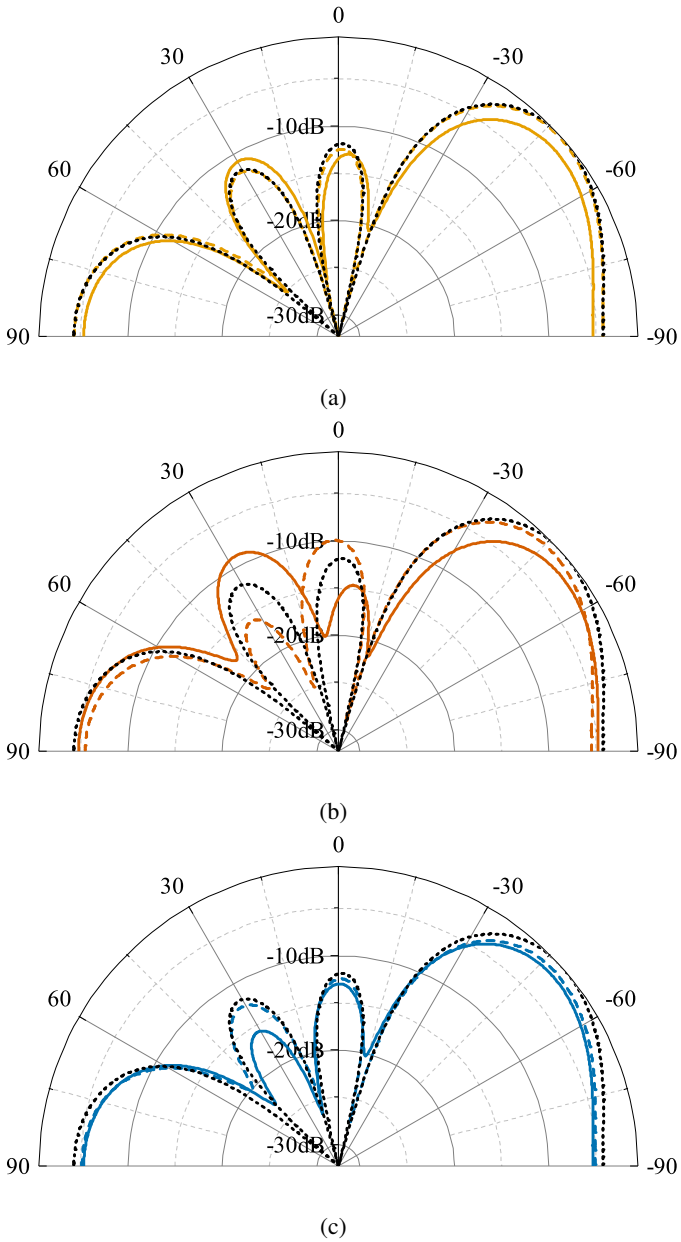


Figure 6.16: Simulated array factors using simulated (dashed) and measured (solid) S-parameters for (a) $V_c = -0.2$ V, (b) $V_c = -0.6$ V, and (c) $V_c = -1.0$ V at 40 GHz, 42 GHz, and 44 GHz respectively compared to AF for ideal excitation (black dotted).

for low power levels. For $V_c = -1.0$ V, the most variation in phase occurs at the lower input powers, in contrast to amplitude changes at this control voltage. More generally, for all settings, phase variation occurs at much lower power levels than magnitude variation. As expected, the changes with input power are almost the same when Port 2 is excited, except that different ports are affected. For example, when P_1 is excited with 20 dBm, the largest PPS variation occurs for the phase difference between P_2' and P_1'. When P_2 is

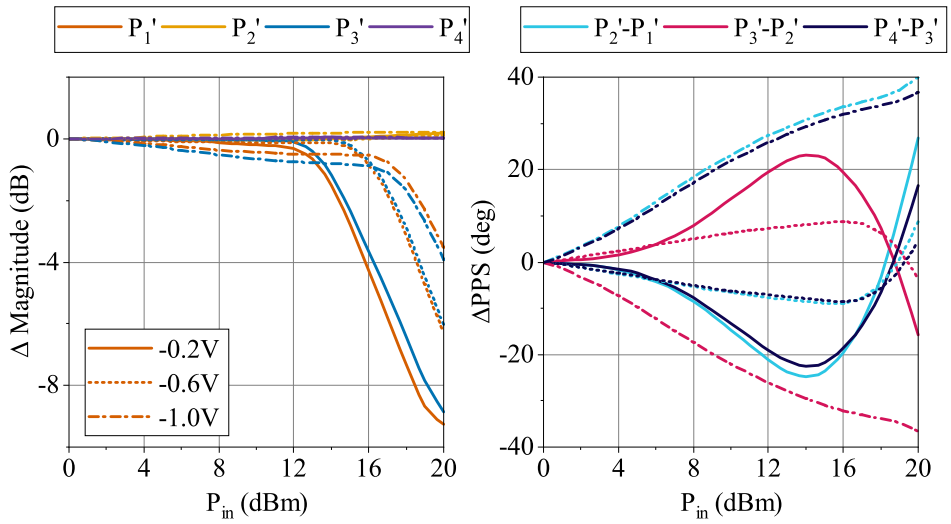
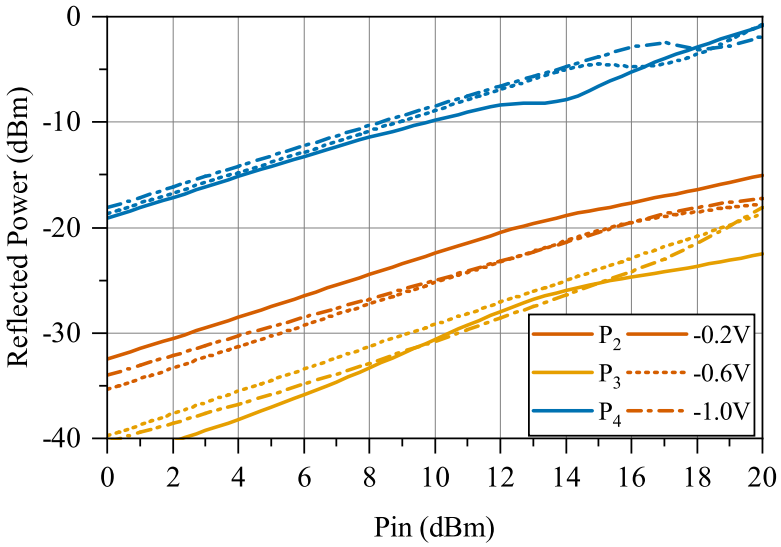


Figure 6.17: The change in magnitude (left) and PPS (right) at the outputs when input power varies from 0 dBm to 20 dBm at P_1 at 40 GHz/V_c = −0.2 V (solid), 42 GHz/V_c = −0.6 V (dotted), AND 44 GHz/V_c = −1.0 V (dash-dot).

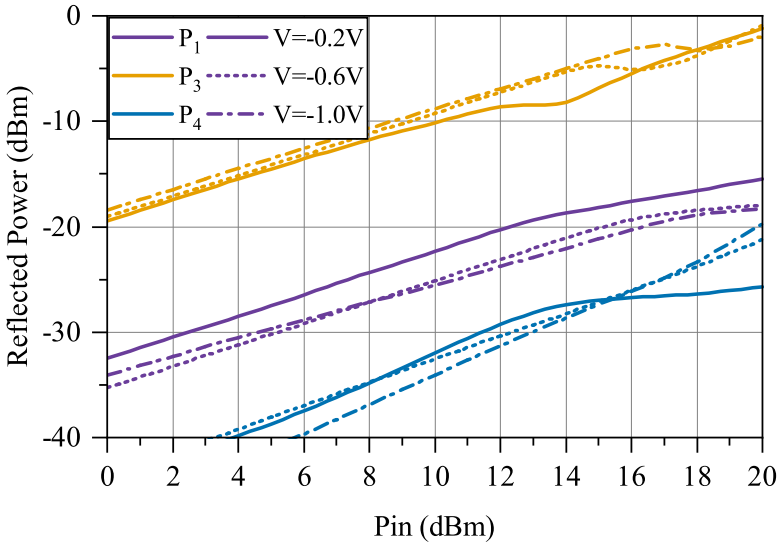
excited with 20 dBm, this behavior translates to the phase difference between P_3' and P_2'.

An ideal Butler matrix has isolated input ports; however, real implementations exhibit coupling, meaning some power leaks into the non-excited input ports. The leakage levels due to the presence of the nonlinear element are explored over input power in Fig. 6.18. The powers at [P_2, P_3, P_4] are plotted when P_1 is excited and at [P_1, P_3, P_4] when P_2 is excited. Without nonlinearities, these lines increase linearly with the same slope. As power increases, the effects of the nonlinearities become apparent, causing deviations from straight lines. Further, the different control voltage settings result in different responses over power.

Ideally, the outputs of a Butler matrix are orthogonal at a given frequency, and exciting multiple inputs should yield outputs that can be found by linear superposition of outputs from separately excited inputs. The introduction of an active element results in harmonic generation as input power increases, and intermodulation products generated if the beams are at different frequencies. For the same phase shifter setting, the Butler matrix can be operated simultaneously at frequencies that are 0.5 GHz apart. Figure 6.19 shows the IMD3 and IMD5 content generated when simultaneously exciting two input ports, P_1 at 40 GHz and P_2 at 40.5 GHz. This example is for V_c = −0.2 V at 40 GHz. The power at P_2 is set to 0 dBm, 10 dBm, and 20 dBm, while the power at P_1 is swept from 0 dBm to 20 dBm. As the power increases at either port, the amount of power at the intermodulation frequencies increases, but remains below -39 dBm.



(a)



(b)

Figure 6.18: Simulated leakage at each of the other three input ports when (a) P_1 and (b) P_2 are excited for $V_c = -0.2$ V/40 GHz, $V_c = -0.6$ V/42 GHz, and $V_c = -1.0$ V/44 GHz.

6.6 Conclusion

This chapter presents a frequency tunable beamforming network that operates from 40-44 GHz. The Butler matrix is fully integrated on a GaAs chip with four inputs and four outputs, with the passive components comparable to the static 44-GHz Butler matrix presented last chapter as a benchmark. The design and

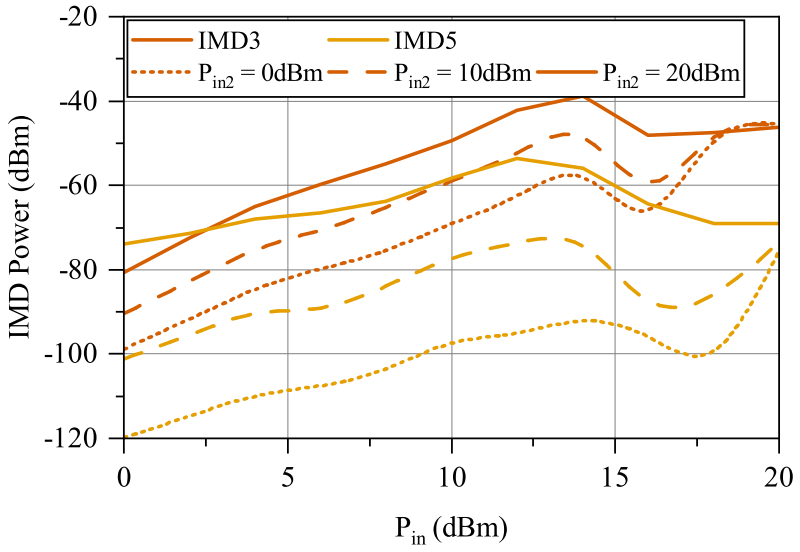


Figure 6.19: Intermodulation products, IMD3 (red) and IMD5(yellow), at output port P_1' when input port P_1 is excited at 40 GHz with various power levels with P_2 being excited at 40.5 GHz at 0 dBm (dotted), 10 dBm (dashed), and 20 dBm (solid) with $V_c = -0.2$ V.

performance analysis of a continuous reflective type phase shifter is then introduced, and combined with the passive Butler matrix to create the tunable beamformer. By adjusting the control voltage V_c from -1.0 V to -0.2 V, the point of minimum variation in the output progressive phase shift (PPS) can be tuned from 40 GHz to 44 GHz achieving phase error of less than 6° while maintaining a good match. Although the introduction of the phase shifter increases the transmission loss, it reduces the phase error and has minimal impact on amplitude imbalance compared to the static version. The performance of this GaAs chip is compared to other millimeter-wave on-chip Butler matrices in Table 6.3. The only other GaAs Butler matrix operates at a lower frequency of 24 GHz and results are reported at a single frequency.

This work demonstrates how integrating an active component into a Butler matrix can enhance performance. The frequency tunability distinguishes it from other published tunable Butler matrices. Although the addition of an active component affects the inherent linearity of the on-chip Butler matrix, the reduction in phase error across a broader frequency range makes this approach both novel and attractive for millimeter-wave beamforming. The integrated GaAs implementation also supports further integration with switches or amplifiers, and can be extended to a GaN implementation with improved linearity.

Table 6.3: Comparison of Millimeter-Wave Integrated Butler Matrices

Ref.	**Freq. (GHz)**	**Process**	**Size (mm^2)**	**IL (dB)**	**ΔA (dB)**	**$\Delta\theta$ (°)**
[167]	24	GaAs	2x2	5.2	0.95	6
[168]	23–25	CMOS	0.9x0.46	2.2	0.6	6
[169]	57–63	CMOS	0.33x1.4	3	1	16
[170]	59–69	CMOS	0.33x0.22	2.8	1.5	N/A
[179]	43–45	GaAs	2.5x2.5	2.4	1.6	19
This work	40–44	GaAs	3.6x2.7	5.2	1.7	6

These beamforming networks presented in the last chapters make up an important part of a broadband front-end. The on-chip examples are well-suited for further integration with the other components that have been introduced so far. The beamformers play an important role in both the transmit and receive paths of an array. The next chapter focuses specifically on the receive path and a component that would be placed directly before the beamformer, an active analog interference suppression circuit.

The work in this chapter is published in [190, 207].

Chapter 7

Interference Suppression MMIC Circuit

The previous chapters show circuitry that is used in both the transmit and receive paths of a front-end system. While the antenna array presented in Chapter 3 focuses on its operation in transmit mode, by reciprocity, any of its characteristics are the same in receive mode. This chapter focuses on the receive side of operation, specifically the filtering function, denoted as 5 in Fig. 1.6.

With broadband systems, the receive side is subject to many signals across a variety of frequencies besides the signal at the frequency of interest. These unwanted interferers can degrade the system performance. In this chapter, the theory of operation behind a circuit used for external interference suppression is introduced, and a GaAs prototype is presented. The general operation is shown in Fig. 7.1. Two different interferers are present, I_1 and I_2 with the signal of interest S_1. Let the frequencies of these interfers and signals are at 6 GHz, 8 GHz, and 12,GHz. The first interference suppression notch filter is applied, the dashed curve, resulting in suppression of I_1 and amplification of S_2, shown in the middle of the figure. The second notch, the dash-dot, can also be applied resulting in the output on the right with suppression of I_2 and even greater amplification of S_1 due to the increase in spacing between the interferer and the signal.

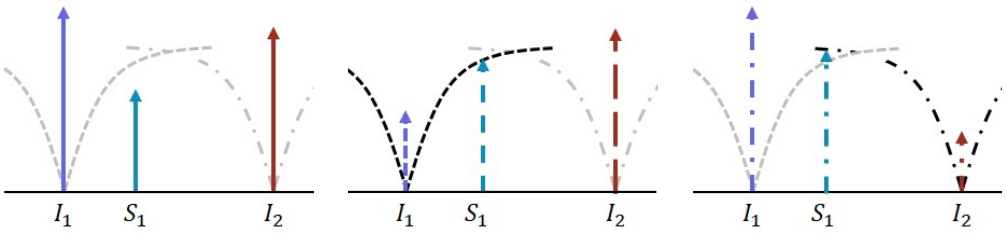


Figure 7.1: An illustration showing the general goal of the interference suppression circuit introduced in this chapter with the left figure showing before the notch is applied and the center and right the output after two different notch filters are applied. The signal of interest, S_1, is at 8 GHz and shown in blue. There are two interferers of different amplitude, I_1 at 6 GHz and I_2 at 12 GHz in purple and red, respectively. Placing the notch filter at S_1, the dashed notch, results in the dashed results in the center, suppressing I_1 while amplifying S_1 and ideally having no effect on I_2. Alternatively, the other notch, the dash-dot, can be placed at I_2. Now the output, shown on the right, suppresses I_2 while amplifying S_1.

7.1 Interference in Broadband Systems

As discussed in Chapter 1, there is increasing demand for the RF and millimeter-wave spectrum. With this increase, there is a greater chance of interferers, either intentional or unintentional, degrading the performance of the system. This is an even bigger problem for broadband systems as the broad bandwidth operation captures signals from potential interferers at more frequencies. Nearly all systems are expected to have some amount of interference and degradation to the received signal. This can usually be handled through digital cancellation, but if the interferer power is large enough, this can saturate the receiver so digital cancellation is no longer possible.

There are two main types of interference: self-interference and external interference. Self-interference happens when a system both transmits and receives, and some of the transmit signal couples into the receive path. External interference can come from other systems operating at nearby frequencies or intentional jammers. These interferers can be at the same carrier frequency or other frequencies within the RF bandwidth of the system. For both external and internal interference, interference suppression and cancellation can be done in the digital domain, analog domain, or spatial domain (i.e., antennas) [208].

This work focuses on analog interference suppression in the RF domain. The different interference suppression methods can be used in parallel with other interference suppression techniques. This layered approach is a common practice already used in systems needing high levels of interference suppression

[208], such as in-band full-duplex systems needing 100 dB. Self and external interference in broadband analog receivers can overload the analog-to-digital converter (ADC) [209]. A further discussion of ADCs is provided next. Interference is a topic that has been extensively investigated in full-duplex systems (simultaneous transmit and receive), where a system transmits and receives at the same frequency and at the same time. Overviews of self-interference in full-duplex front-ends and possible solutions are provided in [208,210,211]. Another area of research on interference suppression is in ultra-wideband (UWB) systems. The FCC released spectrum from 3.1 to 10.6 GHz for unlicensed use, but the power density must be below -41.3 dBm/MHz [212]. These small power levels make it important to be able to distinguish the power coming from interferers so that the intended signal can be demodulated. Multiple examples of UWB systems have emerged, including some with integrated interference mitigation techniques [213, 214].

An overview of current interference suppression techniques is given in Table. 7.1, including the technique used for the circuit introduced in this chapter. For out-of-band fixed-frequency interfering signal suppression, static filters are often used, while a possible solution for variable unwanted signals is electronically-tunable passive filters, with overviews in [215, 216] and examples of bandpass or bandstop filters in e.g., [217–221]. Bandstop filters are spectral notches that can be placed where the unwanted signal is. Bandpass filters tune to only allow the wanted signal frequencies through while attenuating all other signals. These tunable filters, however, can be lossy at higher frequencies and bulky at lower microwave frequencies [222].

Another approach uses a feedback path, in either the analog or digital domains, such as those in [223,224]. The transmit signal is appended, adjusted, and recombined with the received signal. The need for adaptive circuits is an area of growing interest for full-duplex systems, e.g., [209], [225].An example of analog adaptation is shown in [226]. This feedback technique is also used in RFIDs [227]. Multiple taps or delay lines, akin to FIR filters, are explored in [209, 225, 228], using 2, 3, and 16 taps, respectively. Since this method also requires directly tapping the outgoing signal, it is suited only for self-interference cancellation.

A circuit architecture that can be used for cancelling external interference is shown in [229], as it does not directly tap the outgoing signal. Rather, feed-forward auxiliary paths filter out the pre-determined desired signal and then amplify and time-delay the interfering signal before combining it with the main path, thus suppressing the unwanted signal. This demonstration is tunable but only over a narrow range from 874.1 to

Technique	Pros	Cons
Filters	High Q factor and high rejection (with increased loss)	Only can address out-of-band signals, cannot move across spectrum
Tunable Filters	Can suppress a dynamic interferer, currently an area of interest	Often quite large, bulky, and lossy
Tapped feedback in duplex systems or RFID	Established technique to add 40-60 dB of isolation for RF full duplex (STAR) or RFID systems.	Limited to self-interference
Feedforward cancellation	Can be used for self or external interferers	Requires use of down conversion and many filters, can have signal bandwidth limitations
FIR filters in optical systems	Can be adjusted to account for changing environment	Demonstrated at optical frequencies not RF and microwave frequencies
MMIC Interferometer (This work)	Can be used for any interference, adjustable over a broad bandwidth, small size, integratable with other components, has gain	Limited selectivity, limited number of interferers

Table 7.1: Summary of some current techniques used for interference cancellation and suppression including the technique introduced in this chapter.

884.4 MHz with a 2-MHz wide 20 dB deep notch.

The approach introduced in this chapter is an interferometer design suited for interferers not at the same frequency as the intended signal. The input signal is split into two paths, each of which is amplified and delayed before recombining. The operation is described in more detail in the coming sections.

7.2 Receivers and Analog-to-Digital Converters

Before further exploring this interference suppression circuit, the operation and limitations of ADCs are briefly discussed to provide context for why interference suppression is important in the analog domain. For a receive system, the signal or signals first reach the antenna before passing through an isolation element. Typically, a bandpass filter is then applied to remove out-of-band interference. Next, the signal is amplified, usually by a low-noise amplifier (LNA), before down-converted and sampled before going to digital processing. The received signals are often very small, making it crucial to avoid adding noise in the various components so that the ADC can properly quantize the data and the digital backend can demodulate the signal.

A driving factor for this work is to limit the demands on the downstream hardware, specifically the analog-to-digital converter (ADC). Shown in Fig. 1.5, the ADC serves as the interface between analog amplification and radiation and the digital backend, which includes data processing. Digital converters are a broad field of study on their own; an overview of the basics of ADCs/DACs can be found in [230]. While this handbook does not include current state-of-the-art examples, it provides a general overview of the basics of conversion, digital and analog data, and some basic architectures used in converters. A more modern overview is given in [231], which discusses some of the common topologies used in ADCs and compares their general performance on important metrics such as sampling rate, resolution, power consumption, size, and accuracy.

The two metrics of most interest here are the sampling rate and the resolution. The fastest ADCs have sampling rates up to tens of giga-samples per second (GS/s) [231]. This relates to the maximum frequency at which the system can sample. According to Nyquist sampling limitations, to avoid aliasing, the sampling rate must be at least twice the frequency of the signal. For practical implementations, the sampling rate should be five to ten times the maximum signal frequency [232]. For example, with a 500 MS/s ADC, the highest frequency sampled should be 100 MHz. Note that this is much smaller than the frequencies of the analog systems in this thesis because this refers to the signal frequency, not the RF carrier frequency, hence the up- and down-converters in Fig. 1.5.

The other critical metric for data conversion is the resolution. The data is quantized, so for an N-bit, an ADC has 2^N possible outputs. The resolution resolves how separated the different output states are. This can be expressed in various ways, including least significant bit (LSB), parts per million of full-scale (ppm FS), or absolute values such as volts or millivolts [233]. For example, for a 10 V range, a 2-bit ADC has four states, LSB of 2.5 V, 250,000 ppm FS or 25%. For the same range, a 10-bit ADC has 1024 states, 10 mV LSB, 1000 ppm FS or 0.1%. Thus, a 10-bit system can denote much smaller differences than a 2-bit system. Furthermore, if the operation range doubles to 20 V, the 10-bit resolution still is 1024 states, but now the other resolution metrics become 20 mV LSB, 2000 ppm FS or 0.2%. There have been demonstrations of ADCs with up to 24 bits [231]. For millimeter wave systems, since the wide available bandwidth is the goal often up to 1 GHz, the sample rates must be multiple giga-samples per second. Even for lower frequencies

currently in use, data rates of GS/s are considered. The IEEE 802.15.3c standard for WPAN enhancements could require as many as 8 bits at speeds of 2.5 GS/s [234].

It is also important to note that power consumption is another limiting metric for data conversion performance. There is a continuous pursuit of lower power circuitry. This is especially important in array environments, especially those using digital or hybrid beamforming, as multiple ADCs are needed. If the power consumption for each is high, the overall power consumption of the system increases rapidly.

ADCs quantize the signal at their input, which is the sum of all signals within its bandwidth of operation, including both the desired signal and interferers. Interferers can negatively impact performance in several ways. First, they make the changes at the signal frequency of interest less distinct due to the increased signal content at each point in time. For small levels, digital processing can still discern the signal of interest. However, this becomes more problematic if the interferers are large enough, causing the total signal to remain at the upper end of the measurement range. In this case, the ADC operates inefficiently, with an 8-bit unit effectively using only 5 or 6 bits, behaving like an ADC with less resolution, wasting power. Using all the bits efficiently is also important as bandwidth increases, as currently most higher-frequency ADCs have fewer bits for similar cost and power consumption compared to smaller bandwidth implementations. Similarly, if the interferers become large enough, the ADC can become saturated, outputting only the highest levels and failing to capture changes in the signal at the frequency of interest. The goal of the circuit in this chapter is to prevent this saturation by providing a spectral notch at the frequency of an unwanted interferer while providing gain to the signal at the frequency of interest.

7.3 General Theory of Operation

This chapter focuses on the topology given in the last entry of Table 7.1. A general block diagram of the interference suppression circuit is shown in Fig. 7.2.

The analysis of the interference suppression circuit refers to the notation in Fig. 7.2. The input is on the left side where the input signals are $\underline{s}_{1,2} = A_{1,2}\cos(\omega_{1,2}t + \phi_{1,2})$. The signal passes through a coupler with through path $\underline{c}$ and coupled path $\underline{\bar{c}}$ to be split into two paths. The paths have an amplifier with gain

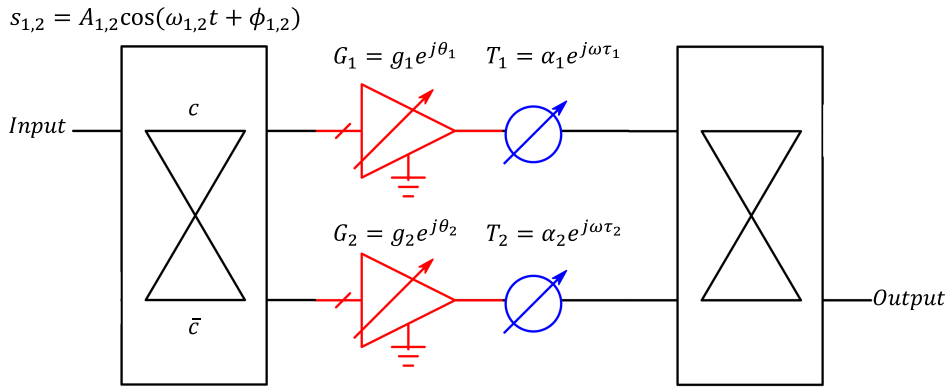


Figure 7.2: The general architecture of the interference suppression circuit.

$\underline{G}_{1,2} = g_{1,2}e^{j\theta_{1,2}}$ followed by a variable delay $\underline{T}_{1,2} = \alpha_{1,2}e^{j\omega\tau_{1,2}}$. These are then recombined with the same coupler with through path $\underline{c}$ and coupled path $\underline{\bar{c}}$ to produce the output. The gain of each amplifier has a magnitude g_i that can be set with a gate voltage (V_{gi}) as well as a phase, θ_i. The delay lines have an attenuation α_i and an electric length τ_i, which are selected with a control voltage V_i.

The output is the sum of the values from path 1 and path 2 so the output, $\underline{y}$ is

$$\underline{y} = (\underline{s}_1 + \underline{s}_2)\underline{c} \cdot g_1(V_{g1})e^{j\theta_1}\alpha_1 e^{j\omega\tau_1(V_1)}\underline{\bar{c}} + (\underline{s}_1 + \underline{s}_2)\underline{\bar{c}} \cdot g_2(V_{g2})e^{j\theta_2}\alpha_2 e^{j\omega\tau_2(V_2)}\underline{c} \tag{7.1}$$

First, let the couplers be lossless and perfectly isolated, and both the amplifiers and delays be linear and matched. The couplers split the signal in half and in-phase so $\underline{c} = \underline{\bar{c}}$. The gain magnitude, g_i, and the delay path electric length, τ_i, are functions of control voltages. With real implementations, the selection of the control voltages also affects the gain phase, θ_i, and the delay path attenuation, $alpha_i$.

If $\underline{s}_1$ is the intended signal and $\underline{s}_2$ is the interferer, the first solution is to find the state such that $|\underline{s}_2|$=0. If the $\underline{c} = \underline{\bar{c}}$, $g_1 = g_2$, $\theta_1 = \theta_2$, and $a_1 = a_2$, this occurs when $\omega_1\tau_1 + \omega_2\tau_2 = (2n+1)\pi$, where $n = 0, 1, 2, \ldots$. A theory for this case is developed in [235]. There are multiple solutions. When increasing the number of multiples of π, the width of the notch decreases increasing suppression at closer spacing.

A more interesting solution set appears when instead of just minimizing the interferer, we solve a different problem: maximizing suppression, or maximizing $|\underline{s}_1(\omega_1)|$ while minimizing $|\underline{s}_2(\omega_2)|$. This is done in Matlab using their constrained optimizer, $fminmax$.

This is used to solve for suppression as the spacing varied between the signal at f_0 and the interferer

as seen in Fig. 7.3 where the amount of suppression is determined while varying the offset from -0.6 to 1.1 compared to the normalized frequency of the signal of interest f_0. The suppression values are a linear value showing how much the interferer is suppressed compared to the intended signal. The different curves show the solutions when the possible delays in both paths are limited by different amounts. For the 2π curve, the delay in both paths is limited between 0 and 2π while for the 8π curve, the delays in both paths are limited between 0 and 8π. By allowing larger delays, there is more suppression near the normalized signal frequency f_0 and the suppression stays higher at all frequencies. The plotted suppression values are not continuous in the plot as a new optimization problem was solved for each frequency offset. The jagged effects are an artifact of solving these discrete problems and could be artificially smoothed. The difference in the effect of the delays settings is also shown in Fig. 7.4. All the outputs are plotted for the solutions used to calculate suppression values in Fig. 7.3 for the 2π curve and 4π curve where the increase in sharpness of the notch and the wider variation in the delays settings is apparent in the 4π limited solutions compared to the 2π limited solutions.

Even more interesting behavior is apparent as this model becomes more realistic. First, let the gain and attenuation vary over frequency. Therefore, the output values at the frequency of the signal and of the interferer are going to have different values. A simplified example is explored in Fig. 7.5 where the gain is set to -4 and +4 linearly across frequency. When setting the null at the center of the band, the slope on either side varies so the suppression is different. The solution can be optimized, as before, for maximizing the suppression so simultaneously maximizing the signal value and minimizing the interferer. Fig. 7.6 shows the optimized suppression results for various gain slopes. The slope affects the overall suppression available.

For example, let the frequency of the signal be 8 GHz and there be interferers at 6 GHz and 12 GHz, so normalized offsets of -0.25 and +0.5. If the settings are limited to 2π, Fig. 7.6(a), and the slope is -4, when the notch is placed at 6 GHz, the suppression level is 0.4, compared to 0.35 when the slope is +4. If the notch is placed at the 12 GHz interference, the suppression increases to 0.55 and 0.8 for -4 and +4, respectively, for the 8 GHz signal of interest. This shows how more suppression is achieved when the interferers are further away and how the frequency-dependent gain impacts the suppression performance.

To meet suppression specifications, the lesser value of suppression (above or below) should be used. The

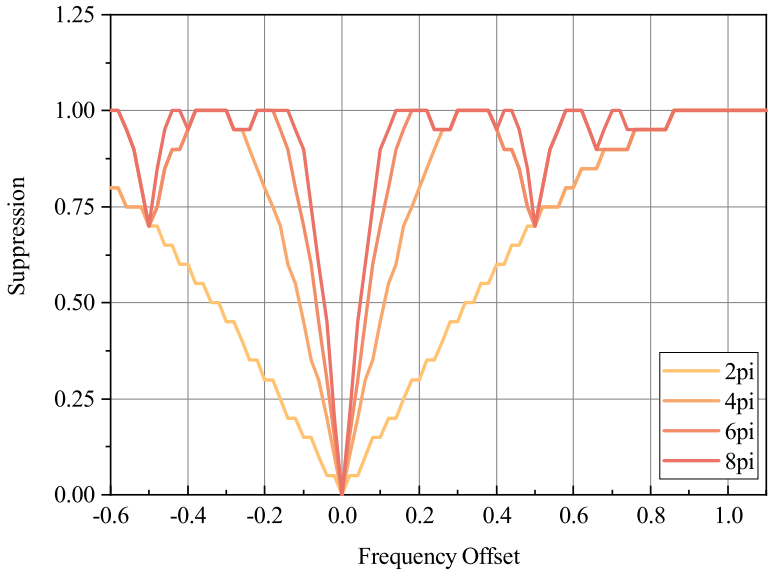


Figure 7.3: The suppression between the interferer at different offsets from the normalized signal frequency f_0 (-0.6 to +1.1) while varying the limits of the delay setting solution. The different curves represent how much the solutions are allowed to vary, so the 2π curves means the delays in both paths are between 0 and 2π while the 8π curve could have the delays in both paths be anything between 0 and 8π. The jagged lines are due to each offset frequency point being a discrete solution to an optimization problem.

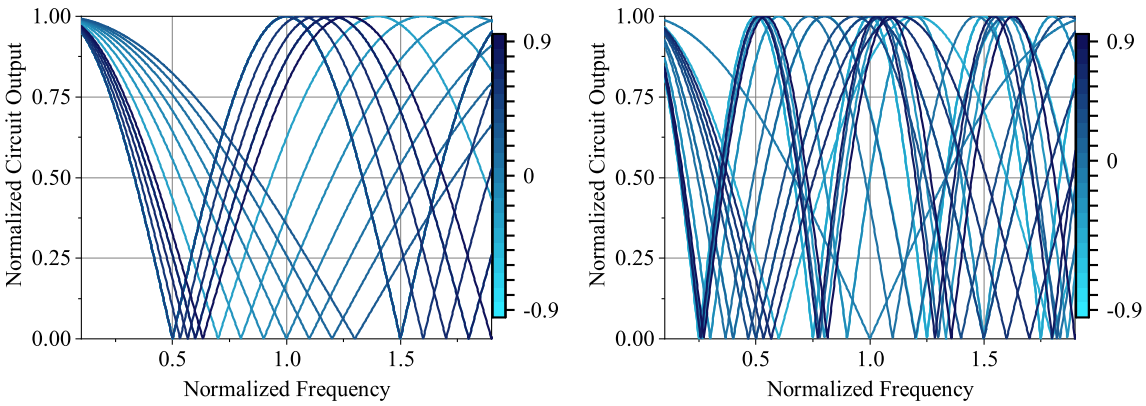


Figure 7.4: The frequency response for the total output at the solved settings from Fig. 7.3 for the interferer frequency ranging from $0.4f_0$ to $2.1f_0$ (offsets of -0.4 to 1.1) for when the delay solutions are limited to (a) less than 2π and (b) less than 4π. Note some of the solutions overlap in (a) so not all offset curves are visible. The addition of extra nulls can be seen in (b) as the delay solutions are allowed to reach higher values.

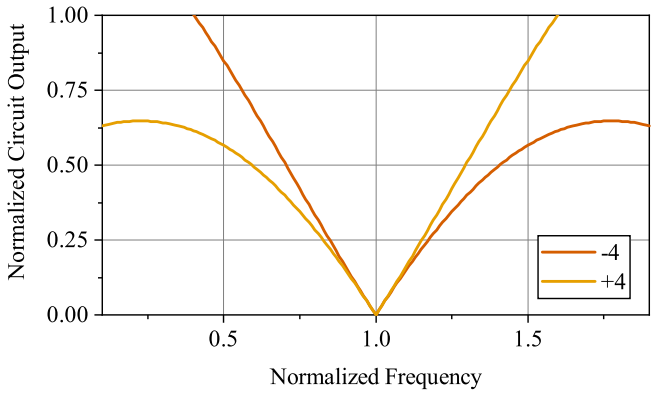


Figure 7.5: The circuit output when the gain is -4 and +4 over frequency. The slope of the gain affects the frequency response so at the same frequency point, there are different amounts of suppression depending on the loss of the system. The amount of suppression is plotted in Fig. 7.6.

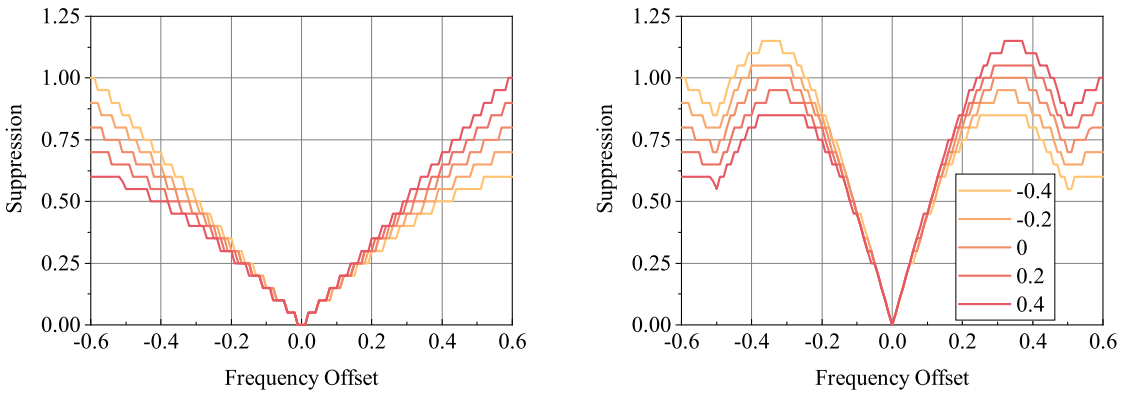
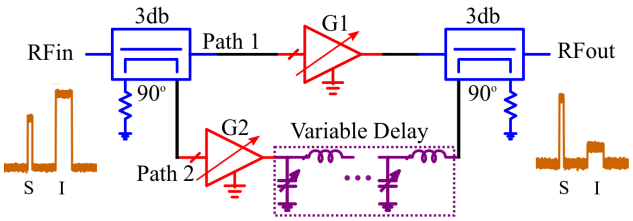
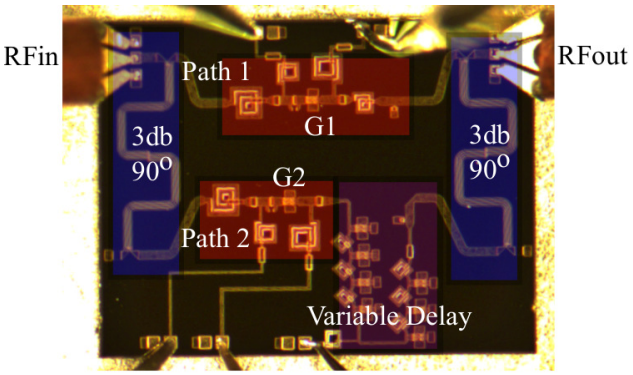


Figure 7.6: The amount of suppression achievable when the path have different gain slopes for various interferer frequency offsets from f_0 when the delay setting solutions are limited to under (a) 2π and (b) 4π. The negative and positive slopes cause the suppression to be different whether the interferer is above or below f_0 in frequency. The jagged lines are due to each offset frequency point being a discrete solution to an optimization problem.



(a)



(b)

Figure 7.7: (a) The block diagram of the interferometer designed to provide a tunable spectral notch. (b) Photograph of the final GaAs MMIC chip with corresponding areas to the block diagram colored. The total chip area is 3.8 mm × 2.9 mm.

general frequency dependence of amplifiers and the delays lines cause a decrease in gain across frequency. This model can be used with more realistic amplifier and tunable lines models, expanding from the simplified models in the previous example to directly taking the performance data from simulations or measurements. This can be used to quantify the amount of suppression available and over what frequency range to see if it meets specifications before fabrication of the circuit. Additionally, the gain of the amplifier can be changed and the setting-dependent gain phase and delay attenuation can be used to extend this theory.

7.4 GaAs Interferometer for Broadband Interference Suppression

Next, an analog broadband interference suppression GaAs MMIC based on the active interferometer architecture is presented. The block diagram and photograph of the MMIC are shown in Fig. 7.7. This architecture applies to a general signal, and covers a wide RF bandwidth, in this case 8-12 GHz, creating a spectral notch at the unwanted signal carrier frequency. The notch is tunable with a small range of control voltage. A

similar design is presented in [235], but is not fully integrated, at a lower frequency, and does not have gain. The circuit can be placed after an LNA in a receiver without degrading the noise figure while contributing gain. As discussed earlier, suppression of an interfering signal can help optimize the useful dynamic range of the ADC, and therefore improve digital cancellation. Therefore, including variable gain in both paths of the circuit in Fig. 7.7 can assist digital signal cancellation over a wide RF bandwidth, providing improvements in dynamic range.

7.4.1 Tunable Active Notch Circuit Design

The tunable active notch is designed using WIN Semiconductors' GaAs enhancement (E) mode single-polarity supply PIH10 process (process 1 from Table 2.1), with a final size of 3.8 mm by 2.9 mm. The circuit is an interferometer in which the input signal is split into two paths that are recombined after analog processing. Path 1 in Fig. 7.7 is a variable gain stage, while Path 2 consists of a variable gain stage followed by a variable delay line implemented with discrete inductors and diode-connected pHEMTs with drain and source terminals grounded. When the signals in the two paths are 180° out of phase, destructive interference results in a transmission null. The final MMIC implementation is shown in Fig. 7.7(a) with each area is highlighted in the same color as in the block diagram of Fig. 7.7b. This front-end circuit is intended to be placed after the LNA and before down-conversion.

Folded Lange couplers with isolated ports terminated in 50Ω are used as the splitter and combiner. For a small footprint and operation over the 6-12 GHz octave, the Lange couplers are folded as shown in the layout of Fig. 7.7(b). When folding the coupled-line sections, a phase unbalance occurs, which is compensated by varying the length of the coupled lines close to the ports. Fig. 7.8 shows the simulated performance before and after compensation.

Both gain stages are conjugately matched in small-signal operation and use 4x75 μm transistors which are chosen as their output impedance is well matched to the variable delay line over bandwidth and over control voltage. The drain supply voltage is 2 V. The gate bias voltages are set to obtain a gain value that compensates for the additional loss of the tunable variable delay line. In both simulation and measurements, the gate voltage of Path 1 is 0.8 V and that of Path 2 is 1 V. The variable delay line in Path 2 (purple in

Fig. 7.7), consists of seven 4x75 μm transistors, and 6 spiral 0.4-nH inductors. The transistors are chosen for their large variation in capacitance with a small footprint, while the inductor size is determined by the 50Ω desired line impedance. Additional lines and capacitors help match the output of the gain stage and achieve the desired phase difference between the two paths.

7.4.2 Simulated and Measured Performance

A separate Path 2 circuit, which includes gain stage G2 and the variable delay line, is fabricated and characterized first to assess how the nonlinear model predicts diode-connected transistor behavior. With a gate voltage of 1 V and drain voltage of 2 V, the delay line control voltage is varied from $V_c = -0.7$ to +0.7 V. The measured S parameters are shown in Fig. 7.9, plotted with control voltage varied in $\Delta V_c = 0.2$ V steps. The input and output match of the line stays well matched with $|S_{11}| < -9.8$ dB and $|S_{22}| < -8.0$ dB across the entire 8-12 GHz range. The transmission gain is above 5 dB for most control voltages and drops above $V_c = 0.3$ V when the transistors approach turn-on, shunting a part of the RF signal to ground. The measured $\angle S_{21}$ is plotted in Fig. 7.9(b) and increases with control voltage, allowing for adjustment of phasing between Paths 1 and 2, thereby tuning the frequency of the notch.

It is interesting to compare the simulated performance, since the nonlinear transistor model is not extracted for varactor simulations. Fig. 7.10 shows the agreement between simulations and measurements of

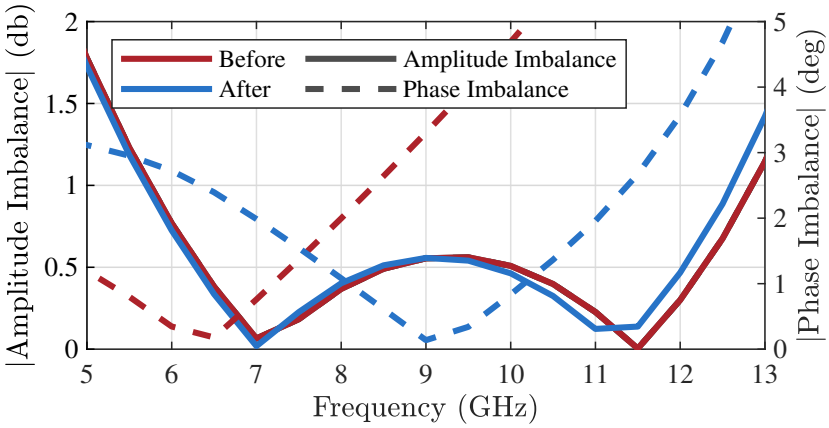
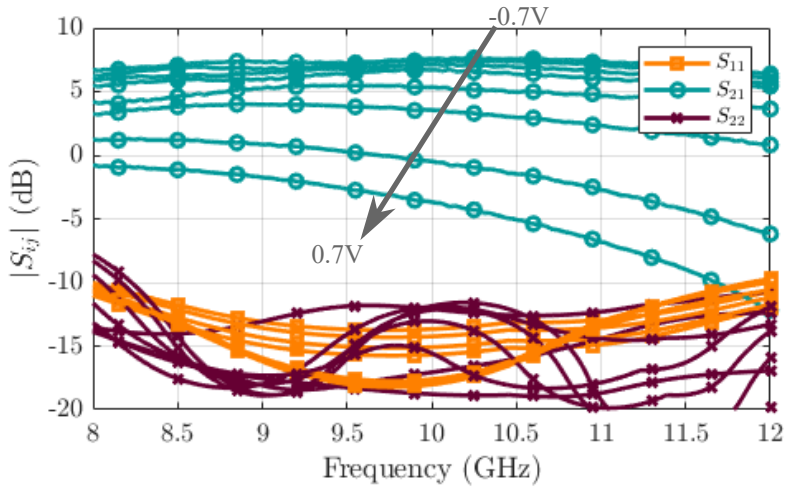
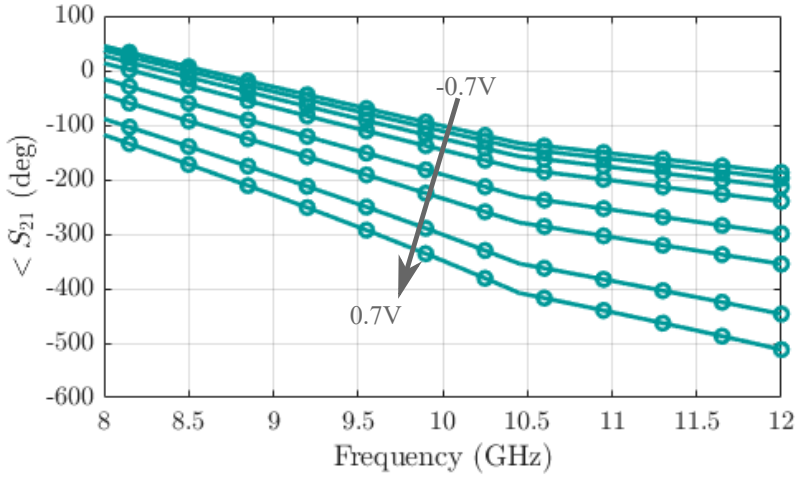


Figure 7.8: Simulated folded Lange coupler amplitude (solid) and phase (dashed) imbalance before (red) and after compensation to account for folding (blue).



(a)



(b)

Figure 7.9: (a) Measured magnitude of S parameters and (b) angle of S_{21} of Path 2. The control voltage V_c is increased from -0.7 to 0.7 V (in the direction shown by the arrow) with the gate voltage at 1 V and the drain voltage at 2 V.

the transmission coefficient magnitude and phase for the two extreme control voltages. Note that the trend is well predicted, but the absolute values differ and show more phase variation in measurements, as well as increased gain variation. The simulated return loss remains below 8 dB and is slightly higher than in measurements in the center of the band.

The results of full interferometer circuit simulations and measurements are shown in Fig. 7.11(a) and (b). For both cases, the drain voltage is set to 2 V, and the Path 1 and Path 2 amplifier gate bias voltages are 0.8 V

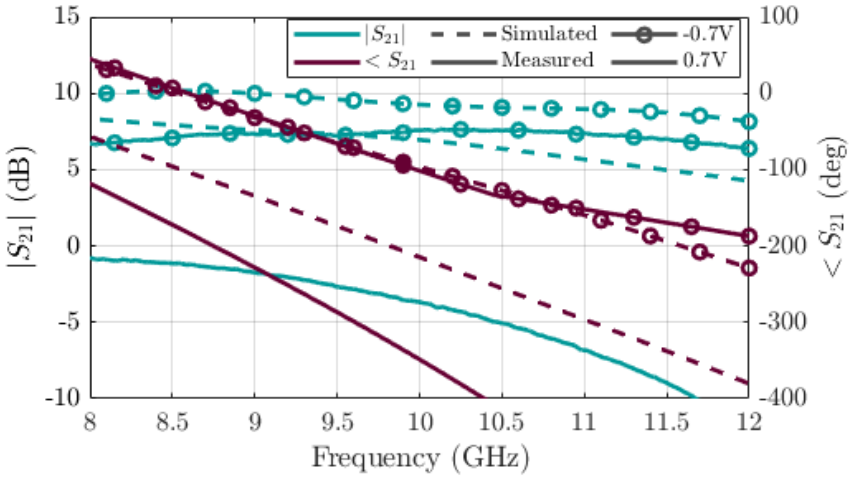
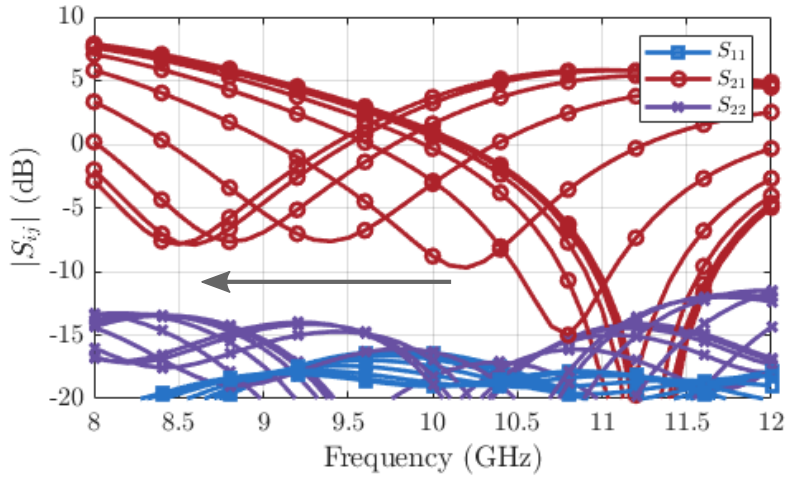


Figure 7.10: Simulated (dashed) and measured (solid) transmission coefficient range for the extreme values of the control voltage.

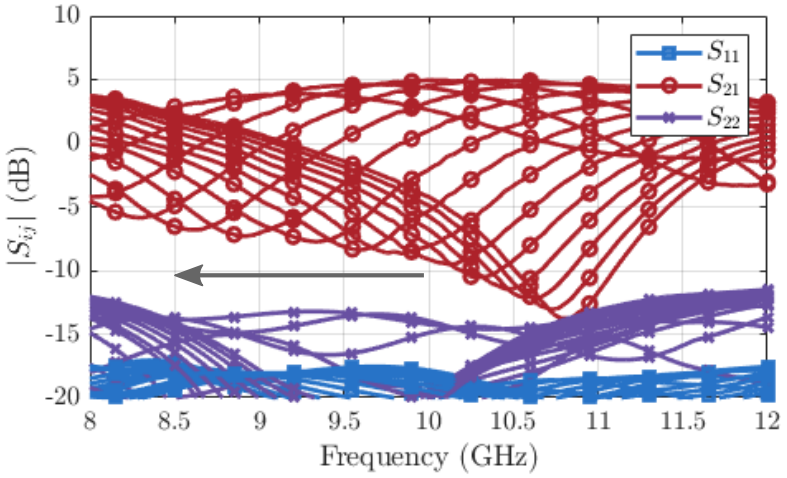
and 1 V, respectively. The input and output match closely agree between simulations and measurements and remain below −16 dB and −12 dB across the 6-12 GHz octave due to the Lange couplers, however the notch tuning is somewhat narrower and covers X band. The 6-8 GHz range is not plotted to better present the notch data over frequency. There is a shift of about −0.4 GHz in the measured vs. simulated notch tuning with control voltage, namely 10.8-8.2 GHz vs. 11.3-8.5 GHz. The depth of the notch is shallower in the measured case when the same control voltage is used as in the simulations. Simulations show that changing the gate bias voltage can improve the depth of notch in the lower part of the frequency band.

7.4.3 Two-Signal Suppression Tests

Two CW tones at different frequencies and different spacings are used to demonstrate the performance of the interference suppression circuit. In the experiment, two generators with equal output powers are combined with a broadband coupler before the chip input, while the output of the MMIC is measured with a spectrum analyzer, Fig. 7.12(a). First, the output with two tones at a Δf=2 GHz spacing is measured as a function of control voltage on the variable delay line, with the results for 8.5 GHz and 10.5 GHz shown in Fig. 7.12(b) in blue and red. Next, tones at 6.5 and 9.5 GHz with a Δf=3 GHz spacing are applied and the output powers as a function of control voltage are shown in yellow and purple. The higher frequencies are more attenuated



(a)

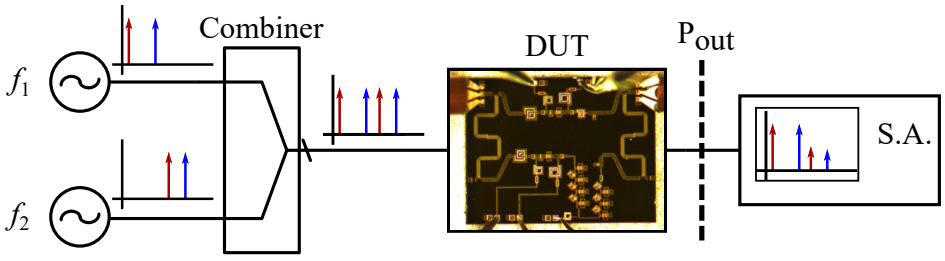


(b)

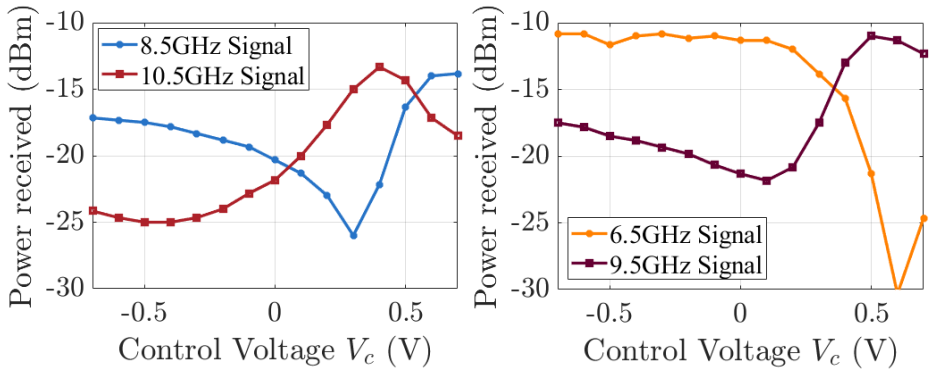
Figure 7.11: (a) Simulated and (b) measured S parameters of the interferometer chip. The control voltage for the artificial line is varied from $V_c = -0.7$ V to 0.7 V. As the control voltage, increased, the notch placement goes down in frequency as shown by the arrow. The drain voltage is set at 2 V. The gate voltages on Paths 1 and 2 are 0.8 and 1.0 V, respectively.

for negative control voltages, while lower-frequency signals undergo more attenuation at higher voltages. Fig. 7.13 displays the difference in power levels between the two sets of signals.

The behavior over frequency is shown in Fig. 7.14 when measuring four cases of frequency spacing and control voltage comparing to the previously measured $|S_{21}|$. Four conditions are shown: (a) Δf=2 GHz, V_c=−0.4 V (red); (b), Δf=2 GHz, V_c=+0.4 V (blue); (c) Δf=3 GHz, V_c=0 V (yellow); and (d) Δf=3 GHz, V_c= 0.6 V (purple). The $|S_{21}|$ shows the expected trends. The difference in power level is normalized to a



(a)



(b)

Figure 7.12: (a) Block diagram of two simultaneous signal measurement setup. The power is calibrated to the reference plane labeled P_{out} using a "thru" and a power meter. (b) The measured output power for 8.5 and 10.5 GHz (left) and 6.5 and 9.5 GHz CW input signals (right), measured on a spectrum analyzer as the control voltage is varied. The input signal powers are -10 dBm.

"thru" line transmission.

For condition (a), the 8.5 GHz signal has about 1 dB of gain while the 10.5 GHz is about 8 dB lower, while for condition (b), there is gain of nearly 5 dB for the 10.5 GHz signal while the 8.5 GHz signal is about 9 dB lower. For condition (c), the 6.5 GHz signal has 5 dB of gain and the 9.5 GHz signal is 10 dB lower, while for condition (d) the 9.5 GHz signal is at 6 dB of gain and the 6.5 GHz signal is attenuated 19 dB for a value of -13 dB. For a larger Δf, the suppression is larger, as expected. The signal suppression predicted from small-signal measurements differs from the one observed in large signal measurements, especially for condition (d) where the varactor diodes are forward biased close to conduction, although the spurs as measured on the spectrum analyzer are 30 dB lower.

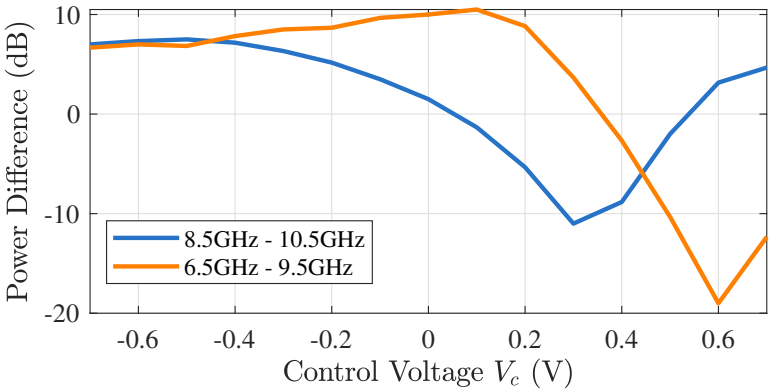


Figure 7.13: The difference in output power between 8.5 and 10.5 GHz (blue) and 6.5 and 9.5 GHz CW input signals (yellow), measured on a spectrum analyzer as the control voltage is varied. The input signal powers are -10 dBm.

7.5 Conclusion

This chapter presents the background on interference in broadband systems and introduces a circuit topology for analog interference suppression. The theory is explained including what occurs when there is frequency dependence in the path gain. An active, tunable notch filter for suppressing interfering signal power is implemented using a single-polarity GaAs E-mode HEMT process for operation between 8 and 12 GHz. This circuit effectively reduces the power of an interfering signal that is 2 or 3 GHz away from the desired signal by 9 and 19 dB, respectively, while amplifying the desired signal by up to 6 dB. It is straightforward to bias and offers tunability within a small control voltage range.

This architecture applies to a general signal and covers a wide RF bandwidth. Suppression of an interfering signal can help optimize the useful dynamic range of the ADC and improve digital cancellation, over a wide RF bandwidth. This base topology demonstrates a proof of concept of a fully integrated interferometer MMIC circuit for receive side operation. Some possible extensions for this work will be discusses in the future works section in the following chapter. The GaAs interference suppression chip is published in [236].

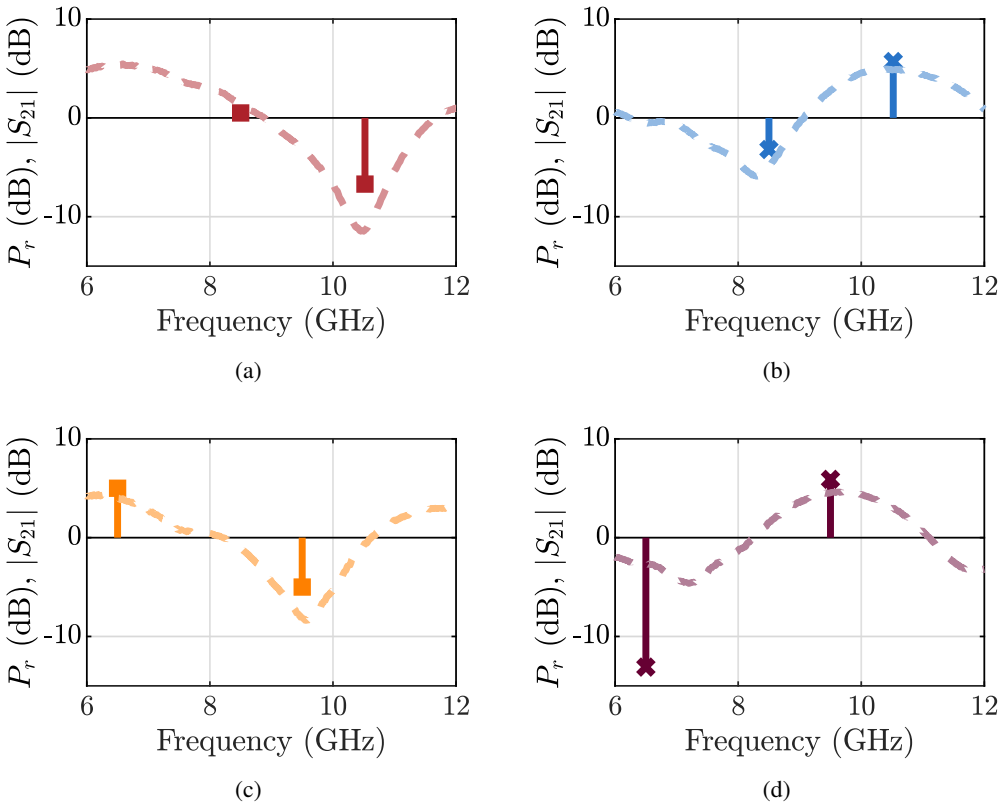


Figure 7.14: Measured two-signal power normalized to a "thru" line transmission (vertical bars). Measured $|S_{21}|$ (dashed) plotted for comparison. For $\Delta f = 2$ GHz, two control settings are measured, (a) $V_c = -0.4$ V and (b) 0.4 V. For $\Delta f = 3$ GHz, the control voltages are (c) $V_c = 0$ V and (d) 0.6 V.

Chapter 8

Conclusions and Future Work

8.1 Thesis Summary

This thesis is focused on broadband front-end components for phased arrays, covering both transmit and receive operations. The primary focus is on the 6-12 GHz octave frequency range. Chapter 2 introduces MMIC processes and two examples of MMICs: a broadband GaAs phase shifter and a broadband 2 W GaN power amplifier. The chapter details the design process for these MMICs and presents both small and large signal results. These MMICs can be integrated to create a front-end system, with the GaN PA playing a crucial role in transmit performance and the phase shifter designed to be integrated with a corporate feed network as part of a beamformer usable in both transmit and receive modes. Chapter 3 covers the design of a 4×1 double-ridge horn antenna array operating at 6-12 GHz. The electrical and thermal performance are simulated using Ansys HFSS and Icepak, respectively. This metal design demonstrates effective thermal management, making it well-suited for a transmit phased array. Additionally, the array is extended to a 2-D 4×4 version, showing high EIRP suitable for intended EW operations. Chapter 4 focuses on beamforming, essential for both transmit and receive operations, specifically discussing a multi-beam beamformer known as a Butler matrix. Two four-input, four-output examples are presented: one using HRL's heterogeneous integration process MECA and one using 3D Glass Solutions' Apex glass substrate.

Both designs are centered around the X-band (8-12 GHz) and are compared with other published broadband Butler matrices. The MECA example faced fabrication issues that prevented complete integration into the previously mentioned array, while the 3D Glass example is still in fabrication. Chapter 5 demonstrates frequency scaling through the design and measurement of a narrowband 44 GHz GaAs Butler matrix. The component designs for this on-chip example include considerations for measurement with the inclusion of on-chip terminations. This beamforming network is miniaturized compared to previous examples but has a narrower bandwidth. Chapter 6 includes the theory behind Butler matrices, specifically at a single frequency, and then introduces bandwidth considerations, leading to a frequency-tunable 40-44 GHz GaAs on-chip beamformer is presented. The inclusion of a broadband continuous reflective phase shifter enables frequency tuning with reduced phase error compared to static implementations. Finally, Chapter 7, shifts focus to the receive side, specifically addressing interference suppression. It discusses interference in broadband systems and its effects on performance, particularly ADC performance, before introducing an interference suppression circuit. The operation of this circuit is described, followed by details of a 6-12 GHz GaAs prototype which can be integrated with components discussed in Chapters 2, 3, and 4.

8.2 Future Work

8.2.1 Beamformers and Integration

Chapter 4 introduced two Butler matrix beamformers, both employing advanced processes for RF and millimeter-wave frequencies. The next step after characterizing these beamforming networks is to connect them to an antenna array and conduct over-the-air measurements. Initial feed network boards for the MECA implementation are fabricated, as shown in Fig. 8.1. These boards are designed with lines of equal electrical length, and the outputs are spaced 25 mm apart to feed the array described in Chapter 3. This design also allows for simultaneous measurement of multiple inputs and outputs using SMA connectors, enabling further characterization of the multi-beam behavior of the beamforming network.

However, as noted in Chapter 4, the additional metal backing on the entire chip and extra copper left around the edges of the GSG launchers due to the dicing process causes the bondwires to be excessively long,

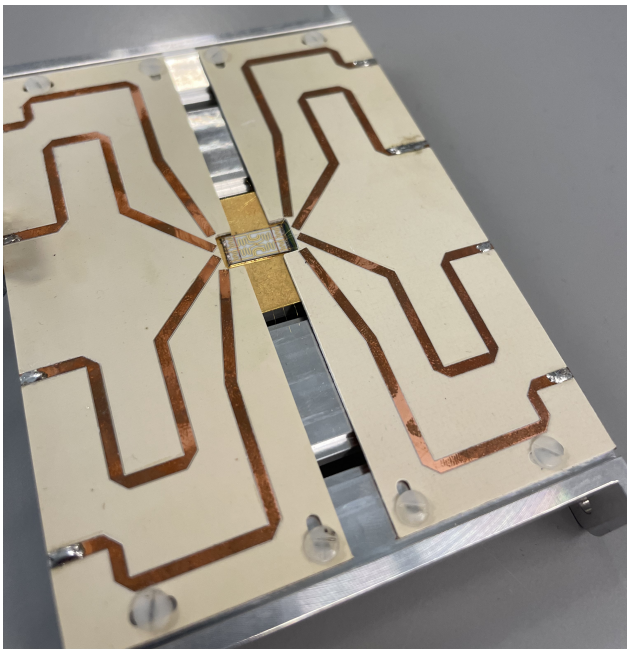


Figure 8.1: The fabricated microstrip feed lines designed to connect the MECA Butler matrix to the 25 mm spaced double ridged horn antenna. The backing added to the MECA chip creates a large height difference between the feed lines and the MECA chip that cannot be compensated for. The long, varied length bondwires prevents this from being used to feed the fabricated antenna array.

adding over 1 nH of inductance, which negatively impacts performance. Consequently, this structure is not suitable for array implementation. Future designs should consider the impact of antenna array interconnects on performance.

Both processes that are used for the Butler matrices in Chapter 4 facilitate direct integration of active components and thermal management [148, 153]. Future research could explore integrating these beamformers or similar components into a complete front-end system that includes a power amplifier (PA) for transmission (as described in Chapter 2), low-noise amplifiers (LNAs) for reception, and/or isolation circuitry for transceiver operations.

Moreover, the tunability introduced in Chapter 6 could be applied to the static versions of beamformers discussed in this thesis. The passive components can be combined with broadband phase shifters, such as the one presented in Chapter 2, to create frequency-tunable beamforming networks. As highlighted in some tunable Butler matrix examples from Chapter 6, continuous tunability could be achieved if phase shifters are placed at each output. However, for effective integration, the added parasitics must be carefully considered,

making this a complex process.

8.2.2 Advanced Heterogeneous Integration

This thesis explores two advanced processes used for X-band beamformers. However, other innovative processes for broadband integrated beamforming networks are also worth considering. These include various emerging heterogeneous integration techniques, e.g. [237–241]. A comprehensive comparison of these processes could advance the field by examining differences in performance metrics such as integration of different chip types, thermal performance, size constraints, limitations, and interconnect properties.

Another rapidly developing technology for RF and millimeter-wave designs is 3D printing, or additive manufacturing [242–244]. While most current published examples of 3D printed components focus on waveguides, there is potential to apply this technology to metal coaxial lines, particularly rectangular coaxial lines with air dielectric. Air-filled coaxial lines are attractive due to their low loss and high power handling capabilities, and they have been explored by various researchers [245–248].

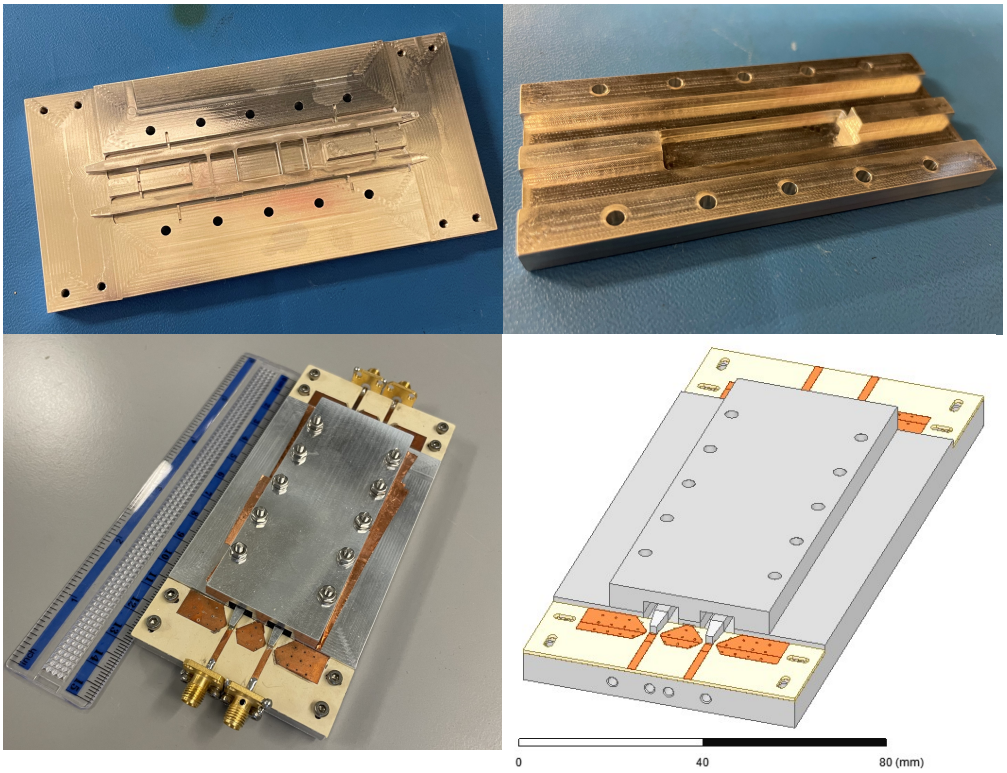
Initial studies are completed to assess the feasibility and behavior of all-metal rectangular coaxial lines with integrated metal supports. These are promising candidates for additive manufacturing since they are entirely metallic. Recent work suggests using angled elements to enable vertical printing of more complex structures [249], which could facilitate printed metal supports for these two-conductor transmission lines. The idea is to integrate the performance of the metal supports—primarily inductive at high frequencies—into the overall circuit design.

For the initial proof of concept, the design is fabricated using CNC milling rather than additive manufacturing. The initial designs resemble miniaturized coaxial lines created using the PolyStrata process [250]. CNC milling and additive manufacturing offer more design flexibility compared to this earlier method, allowing continuous control over the height and width of both the inner and outer conductors. Various simulations are conducted to characterize the impedances and bandwidths while adjusting the widths and heights of the conductors. Once the impedances are known, a multi-section branchline coupler is designed. The perpendicular branches are all placed in a single cavity, where inner conductor widths are tuned for optimal performance. Metal supports are added, two per feed. No mechanical analysis has been conducted;

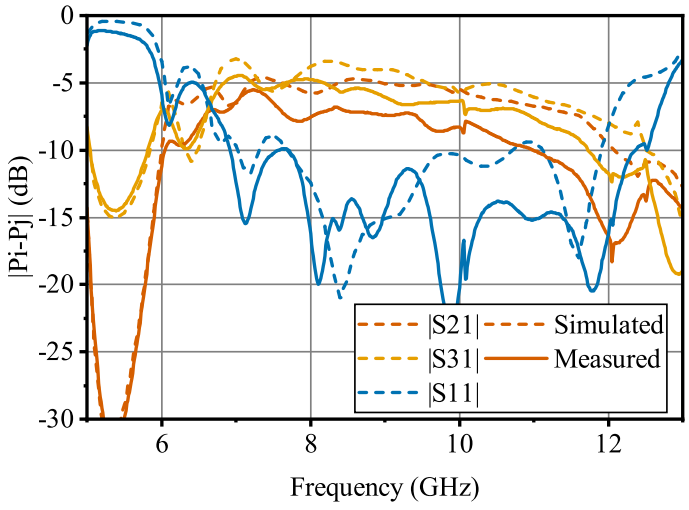
such analysis could be a useful avenue for future research to determine the minimum number of supports needed. Simulations are performed to evaluate the size and placement of the supports and their effect on performance. As expected, smaller supports (relative to the size of the inner and outer conductors) generally shift the passband to higher frequencies. A microstrip-to-coax transition is developed by extending the inner conductors beyond the outer conductor walls to connect to microstrip lines on a PCB. SMA connectors are attached to the microstrip lines for measurement.

For CNC milling used in this initial prototype, the branchline coupler is fabricated in three parts: the bottom half outer conductor, the upper half outer conductor, and the inner conductor, shown is Fig. 8.2(a) on the top. The two halves of the outer conductor are joined with metal screws. The supports for the inner conductor are placed flush with the bottom of the inner conductor, and notches are milled into the outer conductor wall for these supports to rest in. The fabricated branchline coupler is shown in Fig. 8.2(a) on the bottom. The performance of the fabricated branchline coupler is measured using a two-port PNA calbirated with 3.5 mm coaxial calibration SOLT standards. During measurements, the other couple ports are terminated in 50Ω SMA loads. The simulated and measured performance for the through and coupled ports are shown in Fig. 8.2(b). Although the shape matched well, the measured performance exhibits increased loss across the band. This is partly due to leakage between the outer conductor halves. Placing a broadband horn on the sides and edges of the coupler and measuring the output with a spectrum analyzer shows that adding copper tape along the seam reduced leakage, though power levels measured along the sides of the coupler are still about 20 dBm lower than at the open ends near the transition. Adding copper tape further reduced these levels by an additional 10 dBm. Surface roughness, due to the lack of post-processing to smooth the surface after milling, is another likely factor contributing to the increased loss. Surface roughness can significantly impact losses [242], and more specialized post-processing could potentially reduce these losses. Additionally, the losses observed are relatively high in both simulations and measurements, primarily due to radiation losses in the microstrip-to-coaxial transition where up to 17% of the total power is lost to radiation. Future design work should include an improved transition to minimize radiation effects.

This passive component is just one part of a beamforming network. This proof of concept can be expanded to other components to develop a Butler matrix or other feed networks. Further work is needed



(a)



(b)

Figure 8.2: (a) Photographs of the lower half of the outer conductor and inner conductors (top left), upper outer conductor (top right), and combined branchline coupler including PCB feeds (bottom). (b) Simulated (dashed) and measured (solid) S-parameter performance for the through and coupled ports.

to design constant phase shifts and crossovers, which may require additional axes for milling or adaptation for additive manufacturing. As with the MECA and Apex glass implementations, the next step would be to integrate additional passive and active components, as demonstrated in coaxial line examples provided in PolyStrata references [251, 252].

8.2.3 GaN Extensions of Interference Suppression Circuits

The work presented for interference suppression focuses on a GaAs protoype [236]. While GaAs has traditionally been used in receive circuitry [253], newer GaN processes have noise figures that are competitive with GaAs processes noise figures [254,255]. The large power handling, robustness, and high linearity makes GaN an attractive process in the presence of jammars or unwanted interferers [256–260] leading to increased interest in integrated transceivers on a single GaN chip at a variety of frequencies through W-band having both PAs, isolation circuitry, and LNAs [261–265].

Two chips are briefly introduced here, showing design and simulations, both fabricated in WIN Semiconductors' NP15-00 process (process 2 from Table 2.1). The first is a two-stage amplifier followed by a variable delay loaded line with varacators made of transistors in a cold-FET topology. The second is an fully integrated interference suppression circuit with both paths, including a two-stage LNA followed by a variable delay loaded line with source-drain grounded transistors acting as the varactors.

The first GaN chip, designed with a cold-FET variable delay line, demonstrates the possibility of increased frequency capabilities with increased variation in available delays. This design is for a single path, an amplification stage and a variable delay line, that would then be combined externally into an interferometer. Additionally, this iteration looks at an alternate set-up for the varactor, a cold-FET configuration. The two-stage amplifier uses source degeneration. Unfortunately, the models available at the time of this design for CPW mode, needed for source degeneration, are still being developed. Subsequent PDK releases greatly changed the model so the noise simulations of this design not longer are valid when using the newer PDK.

The cold-FET configuration, as opposed to the source-drain grounded transistor setup used previously, allows for improved control over the delay line, as used in [235]. The circuit model and layout of the 8×65 μm cold FET transistor are shown in Fig. 8.4(a). A static bias, V_{bias}, is set to -20 V on the gate side, which also

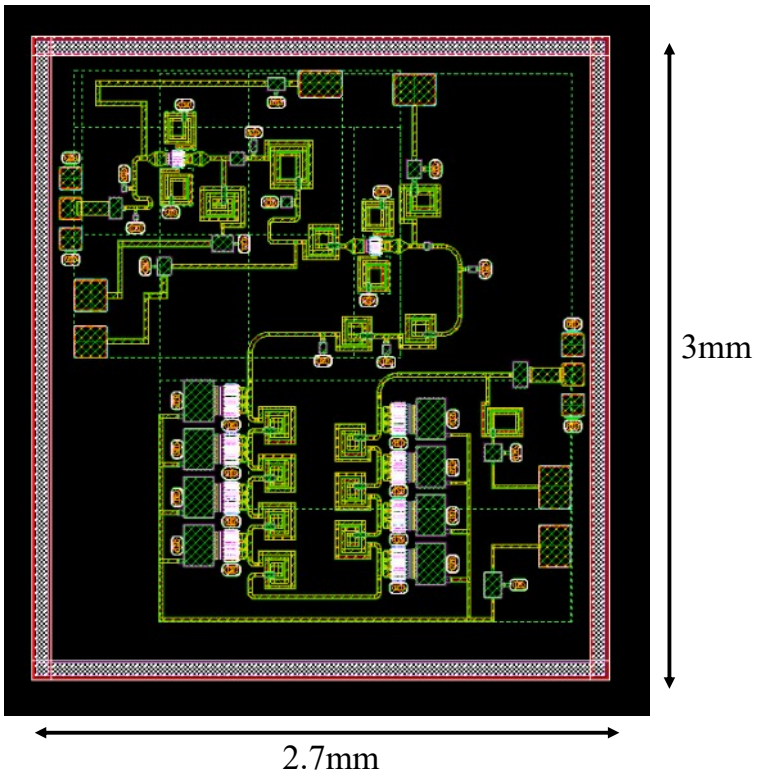
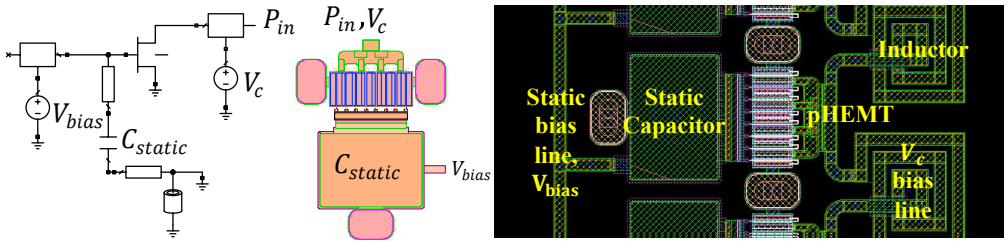


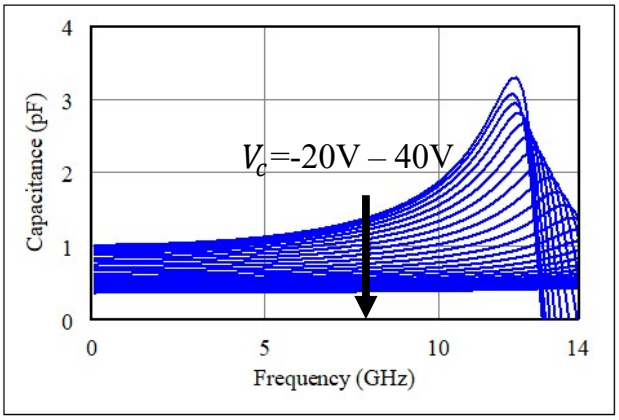
Figure 8.3: Layout of the GaN LNA with variable loaded line using cold-FET transistors

includes an additional static capacitor. The control bias, V_c, is varied from -20 V to 40 V, on the drain side, which is connected to the inductors of the loaded line. The capacitance over frequency at various control voltages is shown in Fig. 8.4(b). Compared to the similar set up at 2-4 GHz in [235], the size of the transistor and static capacitor are reduced to move the point where the capacitance collapses (seen in Fig. 8.4(b)) above the frequency band. The control voltage is much larger now, for the integrated circuit, varying from 0 V to 40 V, compared to just -3 V to -1 V using the source-drain grounded configuration. This allows for better control of the delay. The cold-FET transistors are connected with 0.5 nH square inductors to create the delay line with 8 transistors and 7 inductors as shown in the final chip, Fig. 8.3.

The input, interstage, and output networks are designed similarly to the PA in Chapter 2, first matching with ideal elements to the desired impedances before moving to circuit elements and full-wave simulations. Both stages use 4×75 μm transistors biased at V_d=16 V, I_{ds}=20 mA. The results of the final 2.7 mm by 3 mm chip with various V_c is shown for magnitude and phase in Fig. 8.5. There are two gate biases, two drain biases, V_c, and V_{bias}. The simulated gain stays above 8.5 dB across all frequencies and V_c. The phase



(a)

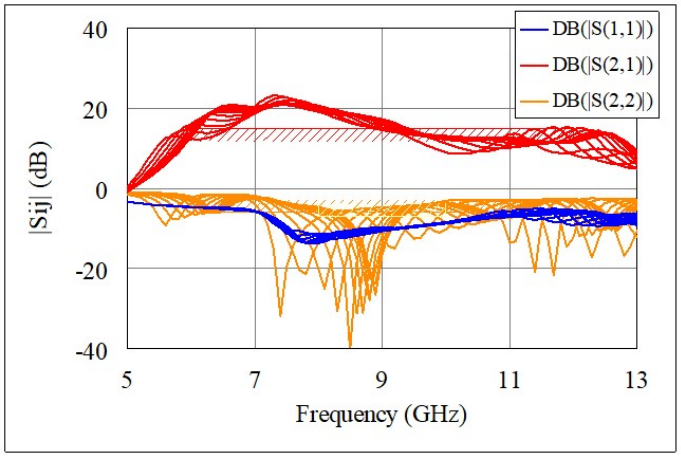


(b)

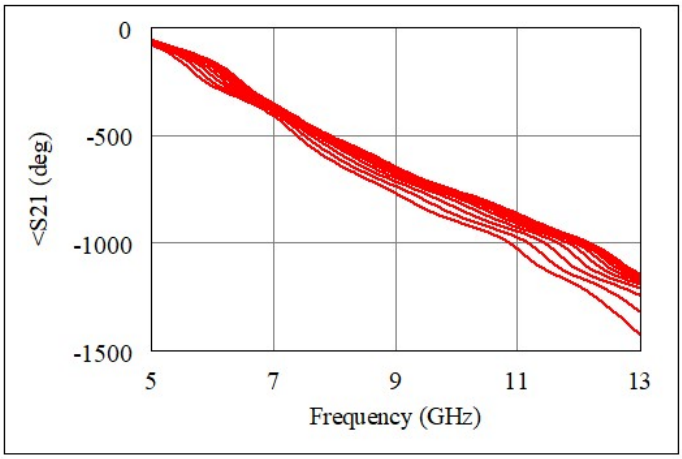
Figure 8.4: (a) The circuit diagram and layout of a cold FET transistor used in this GaN design and (b) the simulated capacitance over V_c and frequency.

difference varies up to 120° at 6 GHz and 225° at 12 GHz. The input RL is above 6 dB.

To create the interference suppression circuit, this would be combined off chip. To demonstrate how the total system would behave, simulations of ideally connected chips are shown in Fig. 8.6. First, in (a), the control voltage of one line, V_{c1}, is set to 0 V while the other control voltage, V_{c2} is varied from 0 V to 40 V. This places the notch somewhere below the center of the band, 9 GHz. Second, in (b), V_{c1} is set to the top of the tuning range at 40 V while V_{c2} again varies. Now, the spectral notches are in the upper half of the frequency range. The deepest notches occur at the center of the band when the two control voltages are similar, therefore gain and losses are similar. To increase the notch depth elsewhere in frequency, the gain can be changed by changing the gate voltage of one or both paths, adjusting one or both magnitudes. This improvement is shown in Fig. 8.6(c) where the gate voltages of the different paths are varied by 0.2 V. Now the notch has less depth at 9 GHz and more depth around 10-11 GHz. Further work can be done varying the gate voltages, of both stages and both paths to try and get more specific behavior. A specifically designed



(a)

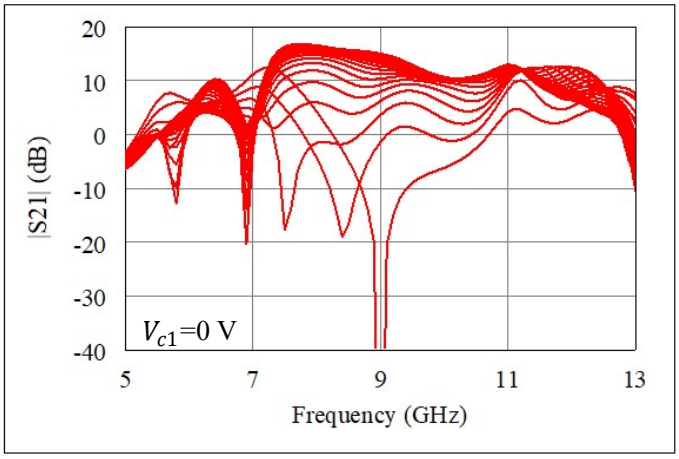


(b)

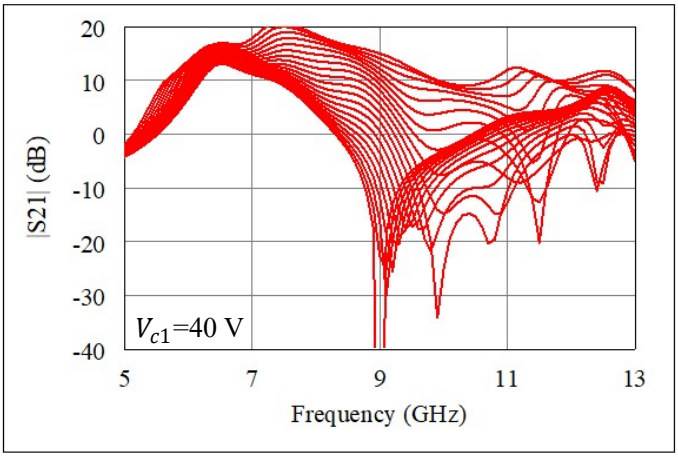
Figure 8.5: Simulated (a) S-parameter magnitude and (b) phase of the transfer coefficients for the GaN LNA followed by variable loaded line circuit.

variable gain amplifier also would allow increased control.

While the previous GaN circuit showed impressive tunability in terms of delay, the size limits the on-chip integration into a complete interference suppression system. The second GaN design reverts back to using the original drain-source grounded configuration but includes delay lines in both paths to create enough delay variation to cover the entire octave in a single 3 mm by 3.5 mm integrated chip, shown in Fig, 8.7. This design has the amplifiers specifically matched for noise so that this can be one of the first elements in the receive chain. While this LNA design is not as low noise as some X-band state-of-the-art demonstrations, such a set-up decreases the number of components in the front-end. Additionally, this configuration increases the



(a)



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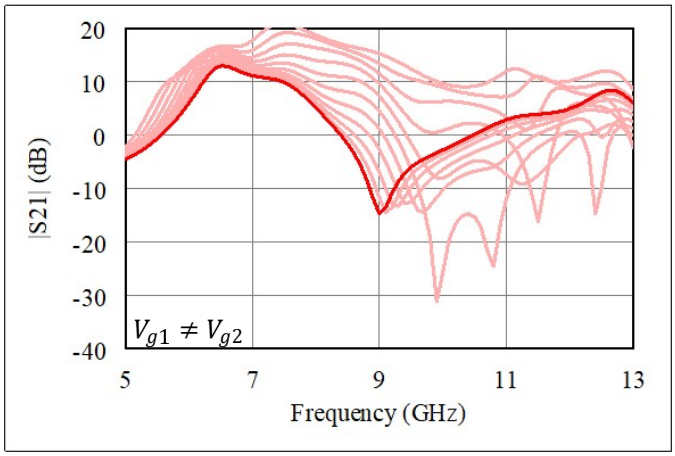


(c)

Figure 8.6: Simulated performance when ideally combining two of the GaN amplifier followed by variable loaded lines when varying V_{c2} while (a) V_{c1}=0 V, (b) V_{c1}=40 V, and (c) V_{c1}=40 V and $V_{g1} \neq V_{g2}$ so the gains of the two paths are different.

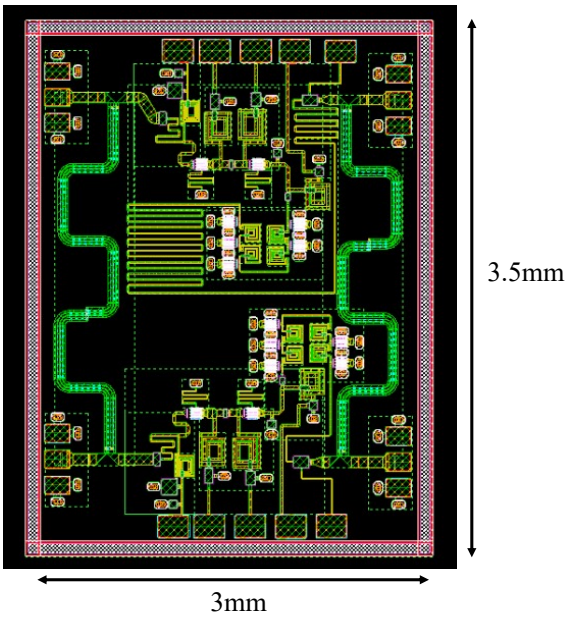
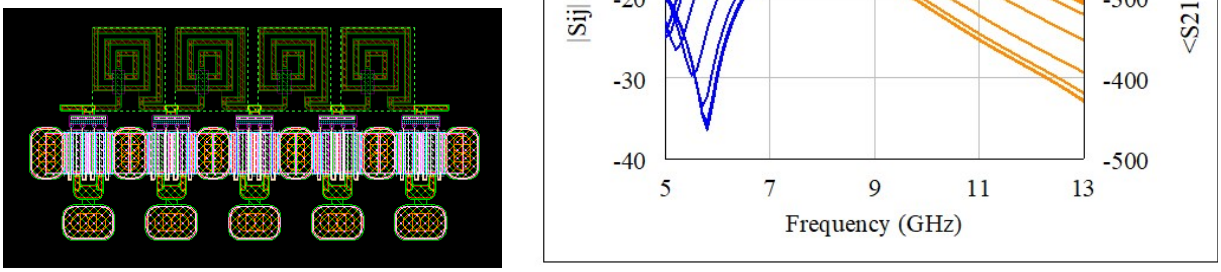


Figure 8.7: Layout of the GaN integrated interference suppression circuit where each delay path has a two-stage LNA followed by a delay line with source-drain grounded transistors.

IP3 by 3 dB due to the splitting of the signal while only decreasing the NF by the loss in the splitter.

First, the delay line is designed. This is very similar to the delay line used in the earlier GaAs implementation with 4×75 μm transistor connected with 0.5 nH inductors. The final line used five transistors and four square spiral inductors. In the final version, the delay line is split into two sections. This adds some additional inductance between the third and fourth transistor and therefore slightly alters behavior from the layout and simulated performance shown in the straight version in Fig. 8.8. The control voltage, V_c, applied to the gate varies from -3 V to -1 V. The phase difference varies from 50° at 6 GHz to 115° at 12 GHz. Note this is less than half the variation demonstrated in the previous GaN chip which included more transistors and the cold FET topology.

The two-stage LNA is also separately designed, shown in Fig. 8.9, with a similar processes as previously mentioned. Source degeneration is used on both stages with 4×75 μm transistors. The updated PDK version had better noise models for the CPW transistor so the input stage and interstage are matched for noise. These updated models are only at certain bias points, set V_d and I_{ds} so both stages are biased at V_d=10 V and I_{ds}=75 mA. The noise modelled transistors had much lower than nominal drain voltages. The output is conjugate matched for gain. Compared to the PA and previous GaN amplifier, fewer elements are used



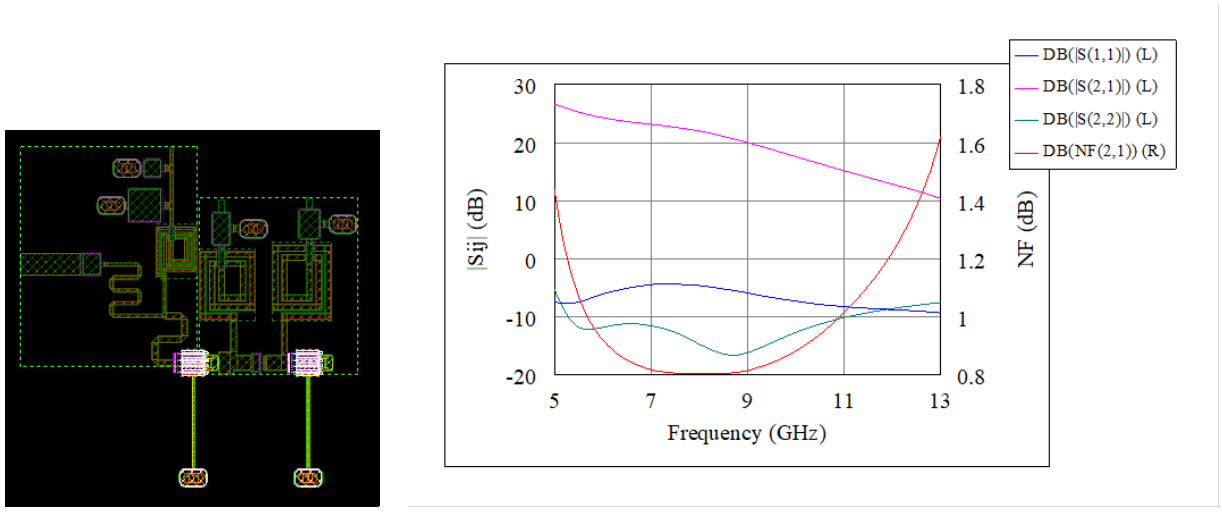
(a) (b)

Figure 8.8: (a) The layout of the delay line with discrete inductors and source-drain grounded transistors and (b) the simulated performance over frequency and V_c.

for the matching network. This decreased the broadband performance, Fig. 8.9(b), which can be noted in the change in performance of gain across frequency, but saved on size. The overall performance is still acceptable across bandwidth. The shown performance is when V_c is set to the middle of its range for the approximately "average" impedance presented. The gain stays above 13 dB from 6-12 GHz with input match better than -5 dB and output match better than -9 dB. Noise figure stays better than 1.2 dB and is as low as 0.8 dB around 8 GHz.

The two lines are connected using meandered Lange couplers for broadband performance and acceptable aspect ratio. The final simulated results are shown in Fig. 8.10 for when (a) V_{c1}=-3 V and (b) V_{c1}=-1 V while varying V_{c2} from -3 V to -1 V. This either places the notch below 9 GHz, the center of the band, or above 9 GHz as demonstrated in the previous design. The notch placement covers more than the entire 6 GHz, unlike the GaAs version that varied across 8-12 GHz. The match is excellent due to the couplers, below -19 dB. Notch depth varies whether looking above or below the notch frequency. This is due to the variation in gain from the LNA discussed earlier. There is still a distinct spectral notch, but the non-flat gain has an impact. For future work, limitations on the gain variation, at the expense of size, NF, or other metrics, would improve the overall performance in terms of notch depth.

As above, but not shown, the depth of the notch could also be changed by adjusting the gain of each path



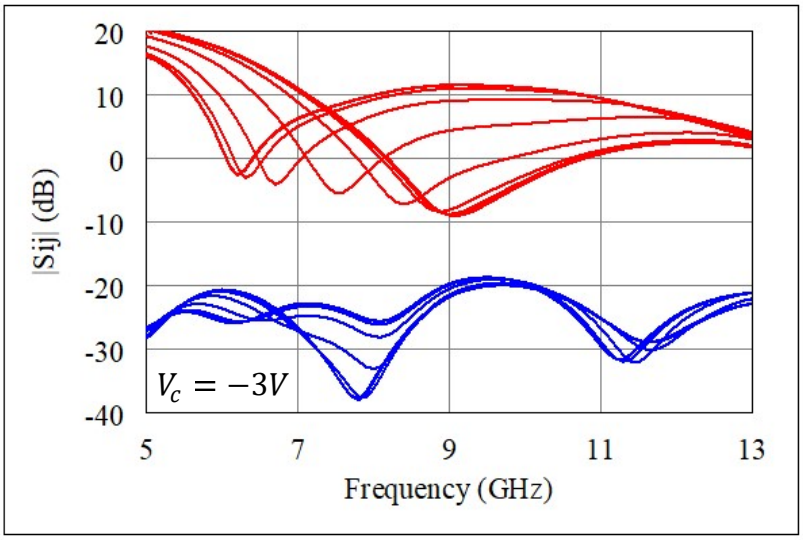
(a) (b)

Figure 8.9: (a) The layout of the two stage GaN LNA and (b) simulated performance at with the average value of the impedance of the variable laoded line.

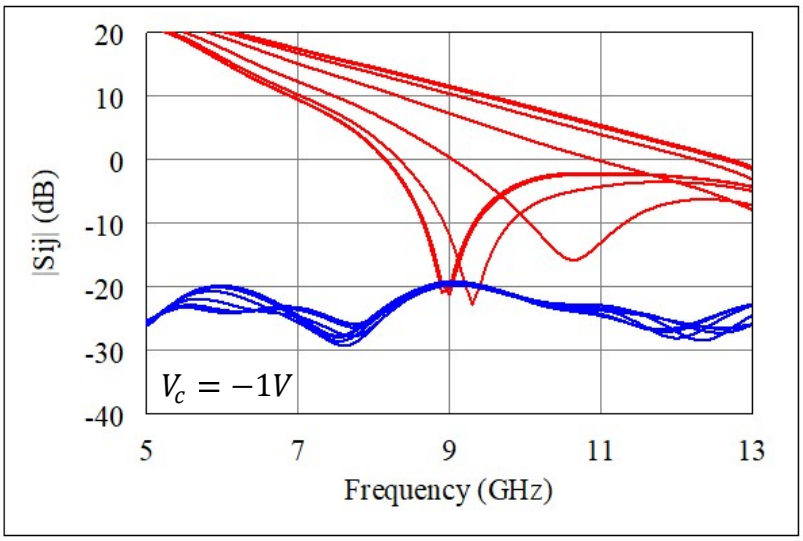
through the gate voltages.

This version has four ports available for measurement, the input and isolated ports on both Lange couplers. Simulation results found that tuning the loads on the unused ports not used for RF input and output, also adjusts the placement of the notch, but it de-tunes the performance of the amplifiers as it changes the impedances at the other Lange ports. Additionally, both output ports can be used with the notch centered at different frequencies due to the 90° phase shift inherent to the Lange coupler. The issue with this is that the difference in frequency is large and the circuit does not work nearly as well outside of the design bandwidth of 6-12 GHz. In future iterations, if even broader band amplifier are designed, this could be utilized for further frequency tuning.

Both chips are received back after fabrication by WIN Semiconductors. Unfortunately, both chips are unstable when measured using 150 μm GSG probes, despite the addition of off-chip capacitors. This could be due to the uncertainty in models for the transistors acting as varactors. Future designs are in work to create GaN interference suppression circuitry with integrated LNAs that either have a single stage to decrease the bias complexity and/or with more stabilization at the cost of NF to compensate uncertainty in the HEMT models. These GaN implementations and their simulation performance are presented in [266].



(a)



(b)

Figure 8.10: The simulated performance of the complete interference suppression GaN chip when V_{c1}=-3 V and (a) V_{c2}=-3 V and (b) V_{c2}=-1 V.

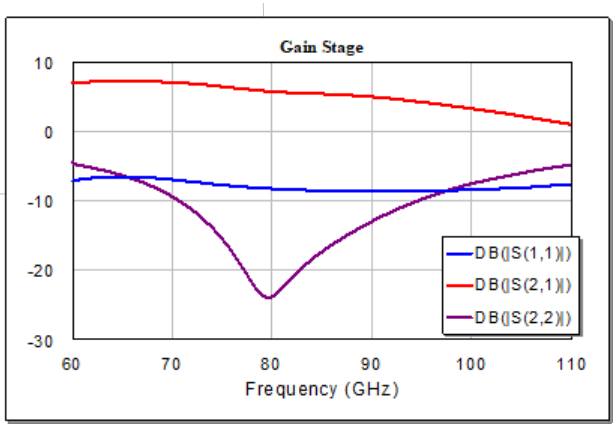


Figure 8.11: The simulated S-parameter response of the two-stage gain block across W-band designed for an interference suppression circuit in HRL's T3 GaN process.

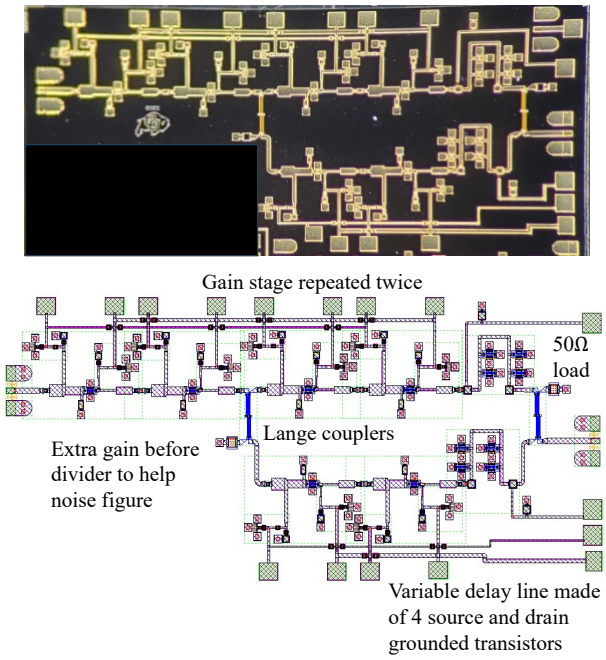
8.2.4 Frequency Extensions of Interference Suppression Circuits

The work presented in this thesis primarily focuses on the 6-12 GHz range with one example of frequency scaling to 40 GHz for the beamforming network. The topology of the interference suppression circuit discussed can also be scaled for different frequency ranges. While implementations at lower frequencies (e.g., 2–4 GHz) have been demonstrated [235], there is increasing interest in millimeter-wave frequencies. This includes the development of new MMIC processes such as HRL's T3 GaN process (process 4 in Table 2.1). This GaN process features a gate length of 40 nm and an f_t above 300 GHz, making it suitable for designs up to W-band.

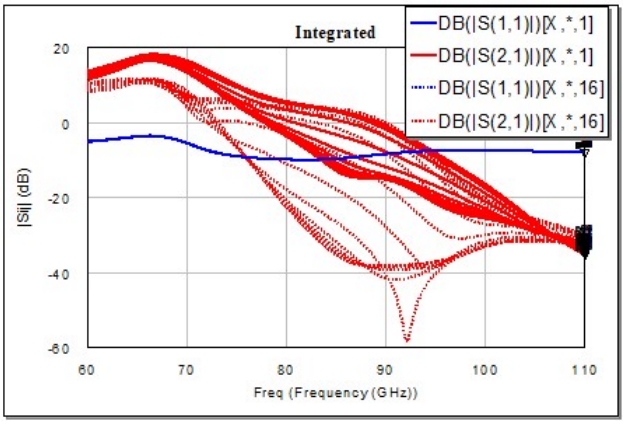
A scaled version of the GaAs design from Chapter 7 is developed using the T3 process. First, a gain block is designed. Due to higher losses and significantly lower gain per transistor at these frequencies, the gain block is designed as a two-stage amplifier. The layout and simulated response of this gain block are shown in Fig. 8.11.

This gain block is combined with a variable delay loaded line, constructed using source-drain grounded resistors. The final fabricated circuit is depicted in Fig. 8.12, along with its simulated performance. The increased loss and reduced gain across frequency has degraded notch behavior compared to lower frequency implementations. This degradation aligns with the theory discussed in Chapter 7.

For future work involving higher frequency implementations, special attention must be paid to optimizing



(a)



(b)

Figure 8.12: (a) Layout of the interference suppression W-band circuit. (b) Simulated S-parameter response of the W-band interference suppression circuit. The decrease in gain and increase in loss across frequency degrade the notch behavior.

the frequency response and minimizing losses. Additionally, further studies to determine the fewest number of components needed for effective frequency tuning would be beneficial for millimeter-wave designs.

8.2.5 Additional Work on Interference Suppression Circuits

In addition to more designs in different processes and with low noise amplifiers, another avenue of research is exploring multiple notches. Early work using 2-4 GHz GaN delay lines, and combined off-chip is done in [267]. This work can be extended to on-chip versions and with different numbers of paths. Additionally, cascading the chips could allow for multiple notches and varying notch behavior.

Additional support circuitry could enhance the interference suppression circuit previously presented. One potential development is a frequency sensing circuit, which would enable real-time system monitoring and precise placement of the spectral notch. Integrating this sensing circuit on the same process as the interference suppression circuit would facilitate further integration. While spectrum sensing algorithms are well established for wide-band radio, there is limited research on MMIC circuit-based implementations [268, 269]. Key design considerations include the accuracy of the sensing, the number of frequency settings to sense, and the method for sampling the signal. Once designed, it will be crucial to evaluate the overall behavior and speed of the sensing circuitry, as these factors are important for real-time systems. The speed of the interference suppression circuit will be limited primarily by the switching time required to apply new control voltages.

Moreover, the interference suppression circuit presented in this thesis can be combined with other interference suppression techniques to address both internal and external interferers. As long as the circuit does not introduce significant non-linearities, reducing unwanted signals should benefit various digital signal processing approaches.

8.3 Thesis Contributions

This thesis addresses challenges of broadband analog front-ends by introducing new components to work in broadband phased arrays. The broadband performance allows the same system to operate at different frequencies, avoiding spectral interference, while the phased array architecture facilitates better use of the spatial dimension, either directing radiated power or received power. First, two MMIC components are introduced operating over 6-12 GHz, a GaAs phase shifter and a 2 W GaN power amplifier. Compatible with

these components is a 6-12 GHz metal double-ridged horn antenna array, which is characterized for both electromagnetic and thermal performance. This validated 4×1 array is expanded to a 4×4 array in simulations. Beamforming feed networks for this array are implemented on novel processes that enable heterogeneous integration: HRL's MECA process and 3D Glass Solutions' Apex glass. The Butler matrix beamformer is then scaled to operate at 44 GHz, a millimeter-wave frequency useful for future communication systems, as an on-chip GaAs implementation. Although this compact design has a smaller bandwidth compared to previous examples, this limitation is addressed by introducing a novel frequency-tunable beamformer. A reflective phase shifter is integrated into the GaAs Butler matrix, allowing frequency tuning from 40 to 44 GHz, resulting in reduced phase error and a broader bandwidth. Finally, the thesis addresses the receive operation of broadband front-ends, focusing on in-band external interference, which is a significant issue for these systems. To prevent ADC saturation, an on-chip MMIC interference suppression circuit is proposed, first presenting the theory of operation and then introducing a 6—12 GHz proof-of-concept design. The thesis concludes with suggestions for future work that builds on the components developed in this research.

Contributions in the area of broadband components and phased array beamforming are summarized as follows:

- Chapter 2: A phase shifter that combines reflective and loaded line topologies is presented. This broadband phase shifter, and a similar designed GaN phase shifter, show competitive performance with published and commercial phase shifters around X-band with an unique topology combining more commonly used topologies. Small signal and large signal behavior is reported. The phase shifter's performance is published in [57].

- Chapter 3: An all metal double-ridged horn antenna array is presented that performs well across an entire octave. While some individual antennas have explored thermal performance, this analysis looks at thermal performance for an entire array, including validation of the Ansys Icepak simulations with a thermal measurement. The initial linear array is extended into a 2-D array for both electrical and thermal performance. The individual antenna element is published in [88]. The entire array is published in [92].

- Chapter 4: Two broadband beamforming networks are presented, both in processes that have not published Butler matrix examples before. The MECA Butler matrix fabricated by HRL is the largest MECA chip at the time of fabrication, pushing the fabrication process. The 3DGlass Solution's Apex glass implementation utilized the air cavities to lower losses under the couplers which also has not be explored previously. Both designs use the multiple metal layers to create the crossovers and couplers. The MECA Butler matrix is published in [270] while the 3D Glass Apex glass implementation is still in fabrication.

- Chapter 5: A GaAs on-chip Butler matrix's design and performance are detailed. This is the highest frequency GaAs Butler matrix published so far and is competitive compared to published V-band CMOS examples. Each component of the Butler matrix is carefully designed to keep phase and amplitude imbalance low. The chip is designed for ease of measurement including on-chip 50Ω terminations. The 44 GHz GaAs Butler matrix is reported in [179].

- Chapter 6: A new type of tunable Butler matrix is introduced, starting with the theory of operation. The 40-44 GHz tunable beamformer is the first published Butler matrix to demonstrate frequency tunability. The phase shifter used as the tunable element is separately characterized, including over input power, to validate the model. Non-linear simulations are also done on the full Butler matrix to further characterize performance showing the effects of adding an active element into a traditionally passive structure. The tunable Butler matrix is reported in [190, 207].

- Chapter 7: An analog interference suppression circuit that can be used for interferers at a different frequency is explored. First, the theory is presented for when both paths have gain and a delay line, which can vary across frequency. An initial design in GaAs operating across 6-12 GHz is characterized showing over 9 dB of suppression at 2 GHz spacing and 19 dB suppression at 3 GHz spacing in measurements. The GaAs interference suppression circuit is published in [236]. Some of these components are also featured in [271].

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