Monolithic Integration of Millimeter Wave Circuits in Advanced GaN Processes

by

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Millimeter-wave applications allow for high-speed data transfer due to the wide bandwidths available in comparison to the overcrowded spectrum at lower frequencies. Unfortunately, atmospheric attenuation also increases generally with frequency, demanding higher output powers and/or multi-element arrays to transmit signals over the air. New gallium nitride (GaN) semiconductor processes operate with high power densities on the order of several watts per millimeter, and cutoff frequencies well beyond 1 GHz. In this thesis, several GaN integrated circuits are designed at frequencies from Ka through W-band (26.5–110 GHz). Both commercially available and developing GaN technologies are employed, with 150 nm, 120 nm, 90 nm, and 40 nm process nodes. The thesis begins with monolithic microwave integrated circuits (MMICs) at the component level, by exploring the optimal biasing networks on chip for various active circuits. Several Ka-band amplifiers are then designed, measured, and analyzed. Comparisons between nonlinear foundry and scalable physics-based HEMT models are performed. The next three chapters focus on various control circuits, i.e. phase shifters, switches, and isolators. These circuits are generally very wideband, covering all or most of V and W-bands (50–110 GHz) and demonstrate high linearity. The level of integration increases in Chapters 7 and 8 with integrated systems designed on a single MMIC, containing both amplifiers and control circuits. First, two active circulators are presented, operating over V and W-bands with measured isolation comparable to commercial products. Finally, two W-band integrated transceiver front ends are described. The first is the most wideband GaN front end published to date. The second is the only full-duplex GaN front end published to date. Every circuit presented is characterized in measurement and simulation, with small signal, large signal, and noise measurements describing their performance.

Dedication

To Luca Anthony Romano, my newborn son.

Acknowledgements

First and foremost I would like to acknowledge my family for their support throughout my lives. My grandfather, to whom I was his namesake, has always been an inspiration to me as the only other electrical engineer in my family. Thank you to my parents for encouraging me to work hard, and for my siblings and extended family for keeping me company along the way. Last but not least, I would like to acknowledge my wife for being by my side during my pursuit of graduate degrees for six years.

Professor Zoya Popovic has been a great advisor and I thank her for giving me the opportunity to learn all that I can from her, as well as pursue my own research interests. Her dedication to her students inspires me to be a mentor to those who come after me.

I would like to thank all of the current and former members of the Microwave and RF Research Group who I have had the privilege of working alongside with. Designing and measuring MMICs with Dr. Tim Sonnenberg has been as fun and entertaining as it has been technically productive. It has also been an honor to sit between Seth Johannes and Jack Molles during my four years at CU Boulder.

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Contents

Chapter

Tables

Table

Figures

Figure

Chapter 1

Introduction

1.1 Semiconductor Manufacturing in the United States

Since entering the 2020 decade, the lack of semiconductor manufacturing in the United States has become a concern for everyday Americans and public officials. Chip shortages have resulted in supply chain issues in many industries, such as auto manufacturing [6]. They have also caused slowdowns in the 5G roll-out and shortages of consumer electronics. To many government officials, the reliance on Asia for semiconductor manufacturing is considered a threat to national security [7]. These concerns led the US federal government to pass the CHIPS and Science Act, which was signed into law on August 9th, 2022. This bill authorizes almost $280 billion to be spent over the next ten years to boost the country's semiconductor manufacturing capabilities and workforce. A breakdown of the funds, displayed in Fig. 1.1, includes $200 billion for commercialization and scientific R&D, almost $53 billion for semiconductor manufacturing, and $24 billion in tax credits to boost production, among many other initiatives [1].

In summary, the bill aims to leverage the depth of talented scientists and engineers across the United States to draw supply chains and semiconductor manufacturing back onto our shores, while training the next generation of skilled workers. New investments in development along with current capabilities are displayed graphically in Fig.1.2. Companies that currently perform foundry services or integrated device manufacturing (IDM), along with university R&D partners including the University of Colorado at Boulder, are indicated on a map of the US in Fig. 1.2a. New and expansion projects for semiconductor manufacturing by companies as of January 2024 are displayed in Fig. 1.2b. These new projects are largely due to the CHIPS and Science Act.

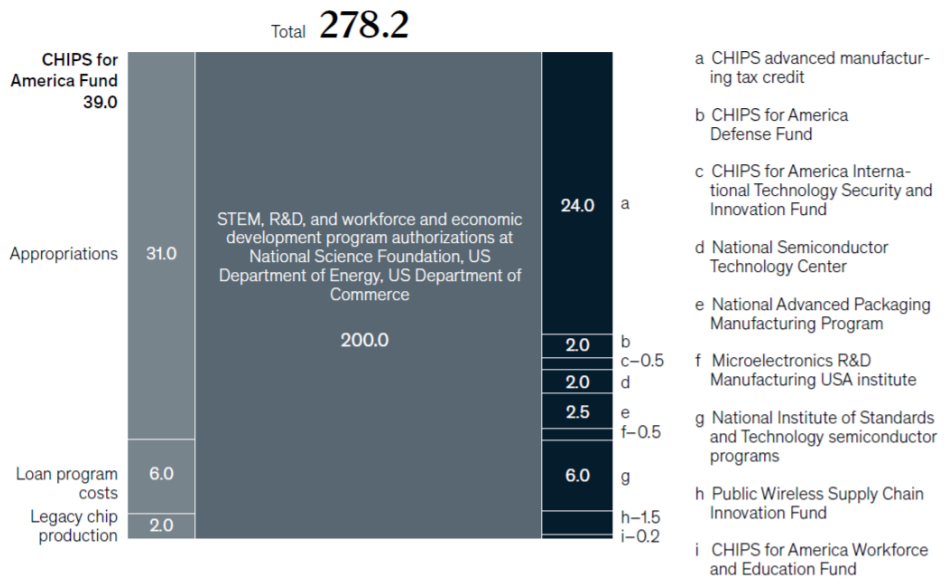
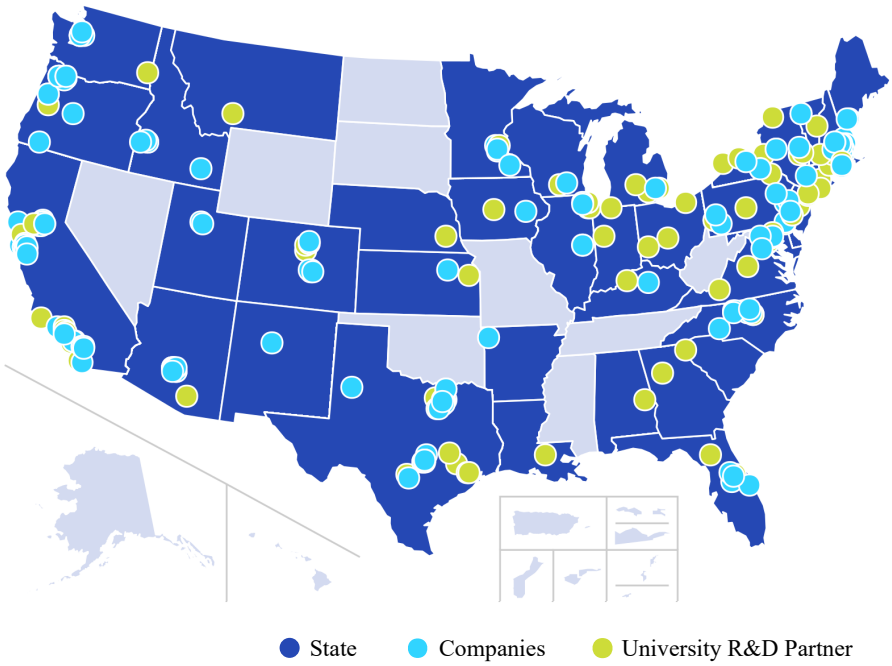


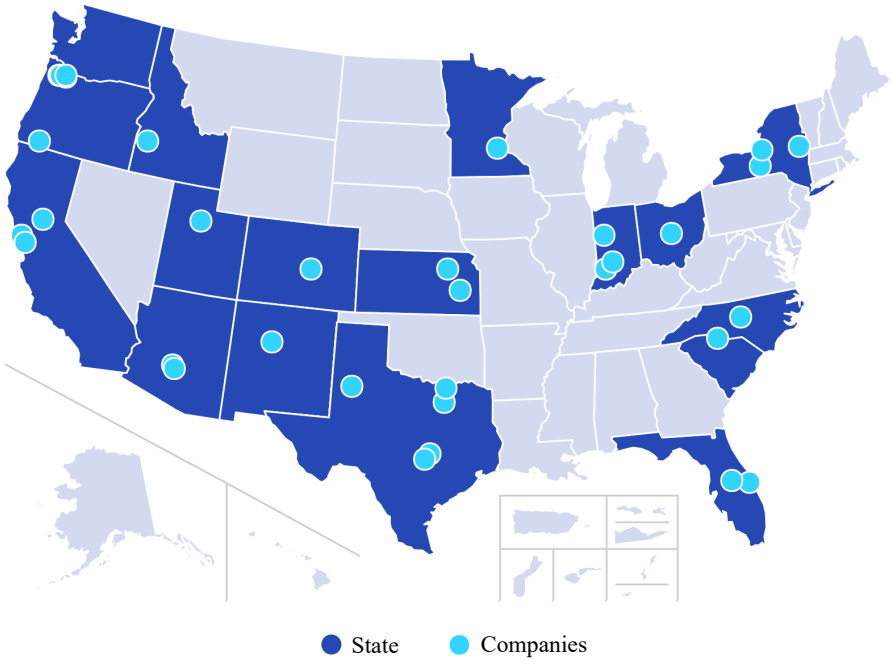
Figure 1.1: CHIPS and Science Act funding between 2022-2026 [1]. Amounts listed in billions.

Along with the ramp-up of manufacturing capabilities for corporations is the designation of "tech hubs" across the country [8], including the creation of eight Microelectronics Commons Hubs by the Department of Defense (DoD) to accelerate prototyping of advanced microchips [9]. These hubs focus R&D and manufacturing in select areas but are located in different regions across the country to draw talent from a wide population. They are located in southern and northern California, Arizona, Massachusetts, New York, North Carolina, Ohio, and Indiana [9]. This will lead to more opportunities for universities such as CU Boulder, which is a partner in the Southwest (SWAP) hub led by Arizona State University, to perform research into new integrated circuit technology and designs.

Developing gallium nitride (GaN) for monolithic microwave integrated circuits (MMIC) stands out as one of the primary areas to pursue R&D. This is evident as some of the first grants from the CHIPS and Science Act are awarded to BAE Systems to modernize their microelectronics center which fabricates six-inch GaN high electron mobility transistor (HEMT) wafers [10], as well as revitalizing a Global Foundries plant in Vermont to fabricate GaN on silicon semiconductors [11]. Prior to the CHIPS Act, the ongoing STARRY NITE program funded by the Naval Surface Warfare Center and the DoD was created to advance domestic GaN technologies for mm-wave applications. This program provides competitive multi-project wafer space in state-of-the-art foundries HRL, Northrop Grumman, and Qorvo from 2022-2026 [12].



(a)



(b)

Figure 1.2: Map of United States displaying (a) Existing foundries, IDMs, and University R&D partners, and (b) announced expansion and new projects as of January 2024 [2].

1.2 Gallium Nitride for Millimeter-Wave Applications

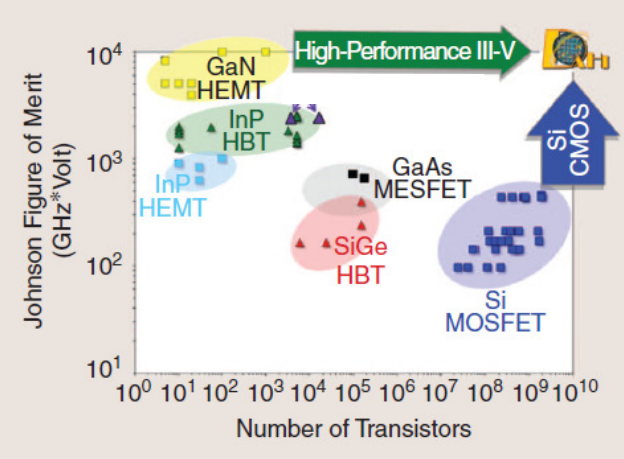


Figure 1.3: Plot of Johnson Figure of Merit vs integration complexity for several device processes using integrated transceivers as data points from [3].

The advancement of GaN semiconductor processes provides many opportunities for millimeter-wave applications. These include radar [13], imaging [14], telecommunications [15, 16], satellite and deep space communications [17–19], implantable devices [20–22], and many others [23]. Compared to other commonly used semiconductors, GaN holds many advantages. Its inherent bandgap of 3.4 eV is more than three times that of either Si or InP, and more than twice that of GaAs, yielding much higher output powers [3]. GaN devices have maximum oscillation frequencies comparable or greater than Si or GaAs and operate with wide bandwidths [12]. The Johnson Figure of Merit (FoM), transistor cutoff frequency multiplied by breakdown voltage, is used to compare these two metrics between processes. This metric is plotted against integration complexity for many different device technologies using several integrated front end circuits as data points from [3] in Fig. 1.3. GaN offers the highest Johnson FoM with front-end integration complexities similar to InP. However, digital and mixed-signal integrated circuits can be implemented more readily in GaAs and Si technologies. The high gain and high power characteristics that make GaN superior for RF front-end design lead to instabilities and excessive power consumption in these circuits. For low power applications, CMOS technologies are often employed [24]. Heterogeneously integrating multiple dies to maximize the benefits of many processes has been aggressively pursued, with programs such as the Diverse Accessible Hetero-

geneous Integration (DAHI) by DARPA to find solutions to this challenge [3, 25]. For example, the metal embedded chiplet assembly for microwave integrated circuits (MECAMIC) platform integrates individual chiplets into 2.5D and 3D multi-chip modules [26, 27]. The chiplets are mechanically embedded into an interposer wafer using backside metallization processes and interconnected with gold plated transmission lines [27].

Table 1.1: State-of-the-art millimeter-wave wideband GaN PAs up to W-band

Ref.	Tech. Node (nm)	Freq. (GHz)	BW (%)	$P_{DC,q}$ (W)	$\|S_{21}\|$ (dB)	P_{out} (dBm)	PAE (%)	Area (mm^2)
[28]	140	75−100	28.6	11.7	12−16	34±1	12	14.85
[29]	40	75−110	37.8	1.8	15−20	26.7	14.8	7.77
[30]	40	75−110	37.8	-	23	27	3	-
[31]	140	70−105	40	2.16	16.3−20.2	24.5	5.8−10.3	-
[32]	100	71−110	43.3	2.25	>15	24.2±1	8	11.7
[33]	100	70−110	44.4	5.88	>13	25.6	6.1	12.75
[34]	100	49−83	51.5	3.96	26.3	29.3	13.5	-
[35]	70	80−122	41.6	1.84	>24	22.8−24.3	9.6−13.4	3.5

High performance GaN processes are under constant development to push performance limits. In the STARRY NITE program, multi-user fabrication runs in the HRL 40 nm T3, Northrop Grumman 90 nm, Qorvo 90 nm, and Qorvo 150 nm processes are available [12]. The circuits presented in this thesis are fabricated in a number of GaN processes. Ka-band designs are fabricated in the Qorvo GaN15 150 nm GaN-on-SiC, WIN NP1500 150 nm GaN-on-SiC, and WIN NP1200 120 nm GaN-on-SiC processes. Each process has an f_T of 33 GHz, 34.5 GHz, and 36 GHz respectively, with more information on these processes documented in [41, 42]. The HRL T3 40 nm GaN-on-SiC process is used extensively for V and W-band circuits. This process has an f_T of 200 GHz and is detailed in many published works, e.g. [43–45]. Finally, the Qorvo 90 nm GaN-on-SiC process detailed in [46,47] with an f_T of 140 GHz is used for W-band design.

Other cutting edge GaN foundries were not available for designs in this thesis, including MACOM, IAF, BAE, Samsung, SONY, etc. A comparison of several state-of-the-art wideband millimeter-wave GaN power amplifiers (PA) is displayed in Table 1.1 which includes amplifiers designed into these processes as well as those included in this thesis, such as T3. At W-band, GaN PAs typically produce output powers on the order of hundreds of milliwatts, aside from the traveling-wave power combined PA in [28], which

Table 1.2: State-of-the-art millimeter-wave wideband GaN LNAs up to W-band

Ref.	Tech. Node (nm)	Freq. (GHz)	BW (%)	$P_{DC,q}$ (W)	$\|S_{21}\|$ (dB)	P_{out} (dBm)	NF (dB)	Area (mm^2)
[35]	70	80−122	41.6	1.84	>24	22.8−24.3	3.5−5.5	3.5
[36]	90	70−110	44.4	0.2	15.5−19.1	-	3.3−4.2	3.12
[37]	70	63−101	46.3	0.31	21−24	-	2.8−3.3	2
[38]	40	65−110	51.4	0.42	>25	16	2.3−3.2*	-
[39]	40	60−105	54.6	-	>23	24	<4	6.63
[40]	40	2−85	190.8	0.396	9.8	25	4	-
[40]	40	2−91	191.4	0.402	9.5	24	4	-
[40]	40	5−125	184.6	0.448	7.3	19	6	-

* Simulated

outputs over 2 Watts across the band. Power added efficiency (PAE) tends to drop with increasing frequency due to Ohmic losses, among other factors, with none of the listed PAE for these amplifiers exceeding 15%. GaN is also suitable for low noise operation, with most or all of the wideband LNAs compared in Table 1.2 having noise figures below 5 dB. A wideband amplifier referenced in [48] also operates as an isolator and will be discussed in depth in Chapter 5. The circuits presented in this thesis were designed with the goal of forming monolithic analog front ends. A block diagram of such a system is displayed in Fig. 1.4. All of the components in this hypothetical system will be presented in subsequent chapters with increasing degrees of integration as individual circuits are combined. Control circuits such as phase shifters and isolators are discussed, as well as duplexers, e.g. switches, active circulators, and a passive cancellation network. Additionally, several amplifier topologies will be presented, concluding with two integrated transceivers.

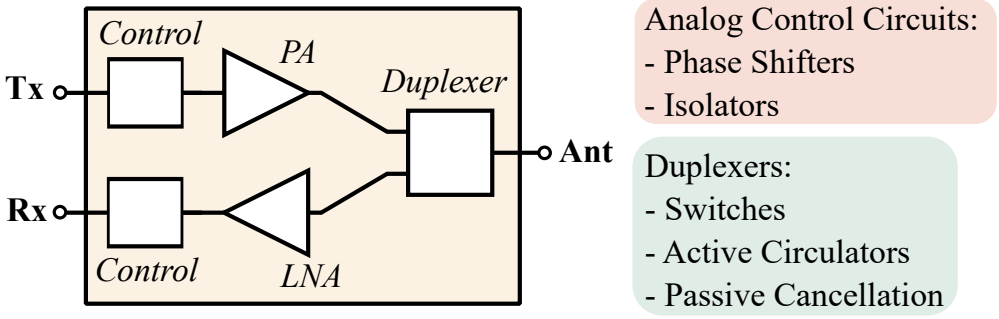


Figure 1.4: Block diagram of hypothetical front end MMIC using components presented in this thesis.

1.3 Thesis Outline

The work presented in this thesis explores designs of various mm-wave circuits in cutting-edge GaN on SiC processes. Many of the circuits attempt to scale conventional techniques up to higher frequencies and compare the results to state-of-the-art designs. The thesis is structured by discussing component level designs with greater levels of integration as the chapters progress. The operation frequency of each design also increase generally with each chapter, starting with Ka-band and working up to W-band designs. The content of each chapter is as follows:

Chapter 2: Bias lines are a necessary part of every active circuit, but there is little information on their design in textbooks [49] or publications. In this chapter, a study on bias lines for millimeter wave GaN MMICs is performed with a focus on integration of bias lines with matching and stability networks. Several bias line structures are fabricated separately in GaN and tested, comparing different techniques. The study is extended to practical design for a single-stage amplifier.

Chapter 3: Various Ka-band power amplifiers topologies are explored. A study of second harmonic termination for narrowband power amplifiers at 32 GHz with increased efficiency is presented. Two amplifiers are designed in different GaN processes and the results are compared. Next, Amplifier design with a physics-based HEMT model is explored in comparison to foundry models at Ka-band. First, three single-stage test amplifiers are designed for each model with variable gate pitches. A four-stage balanced power amplifier is then designed and measurements are compared to the simulation of both models.

Chapter 4: As a validation of the 40 nm technology, continuous reflective phase shifters are designed, covering all of V and W-band. Both 90° and 180° phase shifter MMICs are fabricated, measured, and analyzed.

Chapter 5: This chapter discusses building blocks for integrated duplexers. In the first section, several switch designs are discussed in two GaN processes, which are integrated into a transceiver design in subsequent chapters. The second section discusses an active isolator which is integrated into an active circulator in Chapter 6.

Chapter 6: Two active circulator MMICs in the V and W-bands are discussed. The circulators are

composed of three amplifiers cascaded with Lange couplers. One active circulator topology contains distributed amplifiers and uniform Lange couplers, while the second contains cascode amplifiers and nonuniform Lange couplers.

Chapter 7: Two W-band integrated front ends are presented, designed in part with new circuit blocks and in part with existing components. First a switched half-duplex front end is presented. Second, an in-band full-duplex front end is discussed.

Chapter 8: A summary of contributions of the work described in this thesis is given, with some avenues for future work.

Chapter 2

Millimeter-Wave Bias Lines

Bias lines are essential components for microwave amplifiers and other circuits, requiring careful design to ensure stability, appropriate supply current handling, and good matching. Techniques used at lower microwave frequencies, such as described in e.g. [49, 50], cannot be directly scaled to millimeter-wave frequencies due to parastic reactances resulting in, e.g., self-resonance of inductors. It is often advantageous to co-design the bias, matching, and stability networks, especially for broadband circuits. Additional functions that can be performed with bias lines include linearity enhancement [51,52], supply modulation [53], rectification [54], and adaptive bias control using power detectors [55]. In technologies such as CMOS and GaAs, current mirrors are often used for biasing [56, 57]. Self-biasing techniques have also been implemented in GaN [58], however, temperature and process variations negatively impact the ability to maintain a constant bias [59,60]. This chapter focuses on passive element bias techniques for millimeter wave MMIC amplifiers in GaN technologies.

Several millimeter-wave bias line test structures are fabricated in the WIN NP12 GaN process and displayed in Fig. 2.1. This process includes 120 nm GaN HEMT devices fabricated on a 2 mil SiC substrate, although no active devices are included with these test structures. The test structures, which will be discussed in depth in subsequent sections, are (a) parallel resonant bias, (b) inductor bias, (c) quarter wave transmission line bias at Ka-band, (d) quarter wave transmission line bias at W-band, (e) coupled low pass filter bias, and (f) line for loss de-embedding. Each test structure is a three port network to enable measurement of both the isolation between RF and dc, and the insertion loss between the two RF paths.

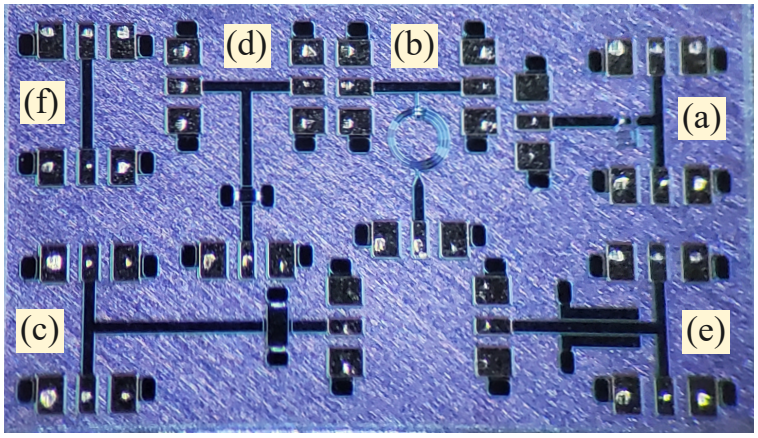


Figure 2.1: Bias-line test structures fabricated in the WIN NP12 process: (a) parallel resonant bias; (b) inductor bias; (c) quarter wave transmission line bias at Ka-band; (d) quarter wave transmission line bias at W-band; (e) coupled low pass filter bias; and (f) line for loss de-embedding.

2.1 Bias-Line Design Techniques

In conventional amplifier design, dc bias lines should present a high impedance to the rest of the circuit in the band of operation, with the goal of reflecting in-band signals while keeping a steady bias point. Considering a bias circuit as a three-port network, where ports 1 and 2 are the RF inputs, and port 3 is the dc input, the circuit element should be well matched at the RF ports with low insertion loss from P1 to P2. The transmission from P1 to P3, and P2 to P3 should also be minimized with a low $|S_{31}|$ and $|S_{32}|$. An ideal dc bias line has the following scattering matrix in the operating RF band:

$$S = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \tag{2.1}$$

This can be approximately implemented with lumped elements, transmission lines, coupled-line filters and any combination of these elements. At dc, the network should present the bias points applied from the supply without any voltage drop. In subsequent sections, simulations of various bias line techniques in Cadence AWR Microwave Office Software and AWR AXIEM 3D Planar EM Analysis are compared with measurements.

2.1.1 Lumped Element Bias Lines

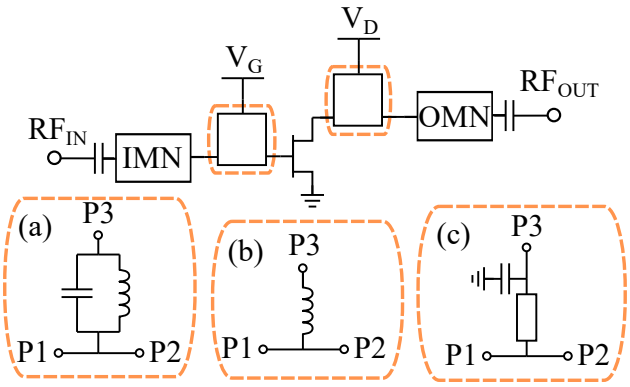


Figure 2.2: General RF amplifier schematic with some common bias-line topologies highlighted in (a)-(d).

Bias lines realized with lumped elements are commonly used in circuits. At low frequencies, resistors and bypass capacitors provide biasing [56, 61], but are not preferable due to RF loss and dc voltage drop between the supply and transistor drain. A simple schematic of a common-source RF amplifier is displayed in Fig. 2.2. The circuit is a two-port network with one device and separate drain and gate biases. Matching networks transform the impedance at the device plane to the port impedance, and blocking capacitors prevent dc current from flowing to the ports. The bias lines are highlighted in orange, with three common RF biasing techniques shown. Topology (a) is a parallel LC network, which presents an open circuit at its resonant frequency, $\omega_c = 1/\sqrt{LC}$, and is inherently narrowband. Topology (b) is an inductor, or RF choke, where the impedance $Z = j\omega L$ theoretically increases with frequency for an ideal element. In practice, planar inductors take up significant chip area in an IC and have a self-resonance frequency when the capacitance between windings starts dominating over the inductance. Additionally, current handling is reduced by the airbridge connecting to the inner winding of the inductor.

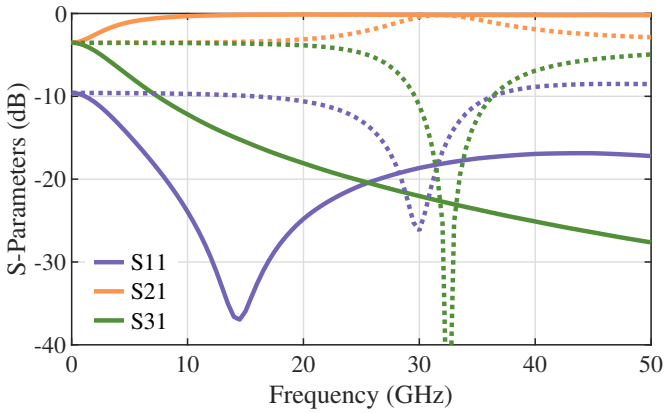


Figure 2.3: Simulation of ideal 1-nH inductor RF choke bias line (solid) and parallel LC bias line with L=0.25 nH and C=0.1 pF (dotted). Ports 1 and 2 are RF ports, port 3 is the dc connection.

Simulated millimeter-wave bias lines composed of an ideal LC tank with L=0.25 nH and C=0.1 pF, and a purely inductive bias with a 1 nH inductor are plotted in Fig. 2.3. These values can reasonably be implemented on a MMIC. The LC bias provides near infinite isolation between ports 1 and 3 at its resonance and close to zero insertion loss between the two RF ports. In contrast, the inductor provides comparable isolation and insertion loss over a much broader bandwidth. By observation, an RF choke bias is necessary for broadband design. However, a much smaller inductor is required to achieve resonance at RF, so the LC tank may be preferable for narrowband design due to the smaller footprint. This ideal simulation is provided for comparison with realistic fabricated on-chip networks.

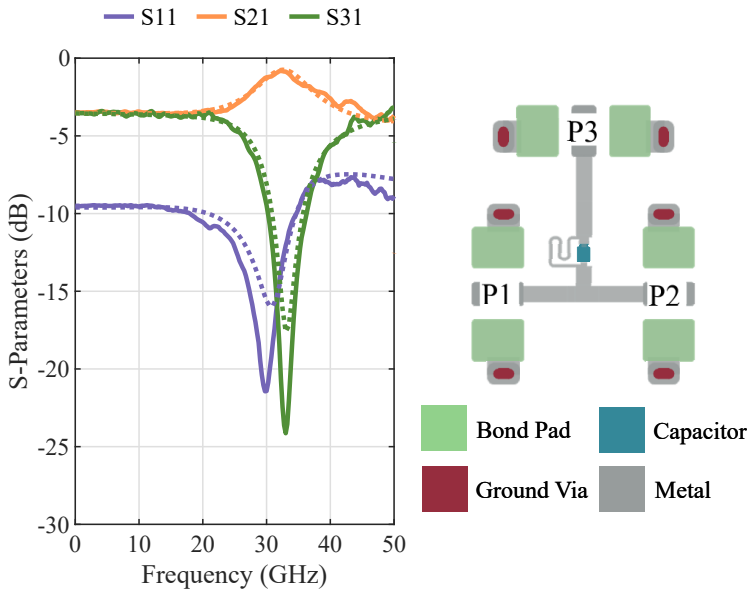


Figure 2.4: Measured (solid) and ideal (dashed) small-signal performance of parallel resonance bias line. The layout in the WIN Semiconductors NP12 GaN process is shown on the right, with 100-μm and 46-μm wide 50-Ω lines.

To further explore these topologies, a parallel LC resonant network and RF choke were designed for Ka-band (27-40 GHz), structures (a) and (b) respectively in Fig. 2.1. A layout depiction of the parallel LC network is displayed in Fig. 2.4. In practice, these structures are difficult to realize at Ka-band as the required values of the inductor and capacitor become very small. Thus, a meandered line is used for the inductive element in parallel with a lumped capacitor. The capacitor is also close to its minimum dimensions where process variations can significantly impact its value. The simulated and measured S-parameters of this test structure are also plotted in Fig. 2.4. A maximum $|S_{21}|$ of –0.76 dB is measured at 32.5 GHz with a 1 dB bandwidth of 7 GHz. An $|S_{11}|$ ranging from –22.3 dB to –9.3 dB, and an $|S_{31}|$ from –25.8 dB to –6.8 dB are measured throughout this range.

A layout and plot of S-Parameters of the RF choke is displayed in Fig. 2.5. The fabricated inductor is made of windings that are only 10 μm thick, limiting the current to around 60 mA at the center tap where only the lower metal layer is exposed. This topology would not be suitable for a high-power amplifier with a significant current draw at the drain, but may be useful for a gate bias line. The measured inductor has a

maximum measured $|S_{21}| = -0.22$ dB with a 1 dB bandwidth ranging from 7.5 GHz to 32.4 GHz. Isolation ranges from –18.9 dB to –7.4 dB and the RF ports are well matched with $|S_{11}| < -10$ dB. The inductor is more broadband than the resonant network, as expected. Both designs are of practical use up to 30 GHz, but the loss becomes significant beyond this frequency, degrading overall circuit performance.

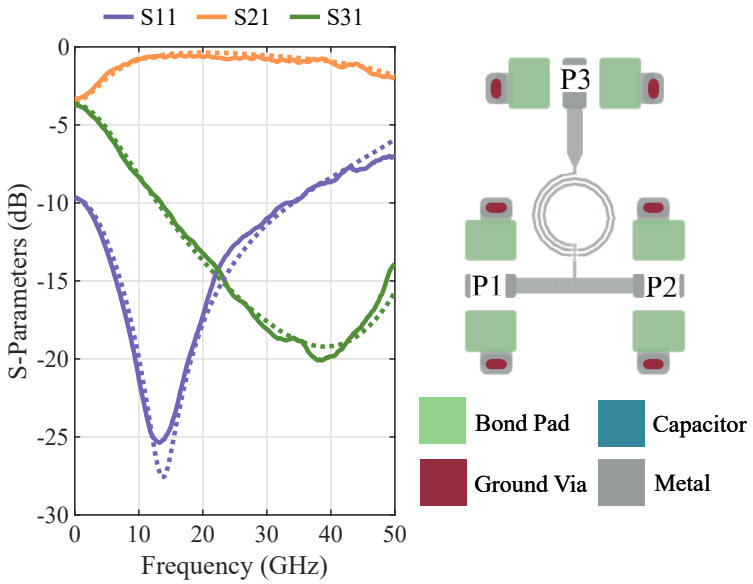


Figure 2.5: Measured (solid) and ideal (dashed) small-signal performance of inductor bias line. The layout in the WIN Semiconductors NP12 GaN process is shown on the right, with 100-μm and 46-μm wide 50-Ω lines.

2.1.2 Transmission Line Bias Lines

2.1.2.1 RF Termination

Transmission lines are frequently used in the microwave regime to present a high impedance to the circuit. Topology (c) in Fig. 2.2 is a transmission line connected to a shunt capacitor. Conventionally, a large bypass capacitor is connected at the node where the transmission line meets the supply voltage line. As capacitance and frequency vary inversely with impedance, the capacitor presents a short, making the transmission line a shorted stub. A shorted quarter-wave line then presents an open circuit to its other terminal. When designing MMICs however, space is often limited and large capacitors occupy substantial

area on the reticle. In the WIN NP12 process for example, 5 pF, 10 pF, and 20 pF capacitors occupy spaces of $151 \times 151\,\mu\text{m}^2$, $215 \times 215\,\mu\text{m}^2$, and $304 \times 304\,\mu\text{m}^2$, respectively. These three capacitors are terminated with a via and simulated over frequency, as displayed in Fig. 2.6. Each capacitor reflects waves at Ka-band frequencies, as desired, with $|S_{11}|$ greater than –0.5 dB. Phase varies greatly across frequency and across capacitor sizes, far from the desired 180° for a perfect short.

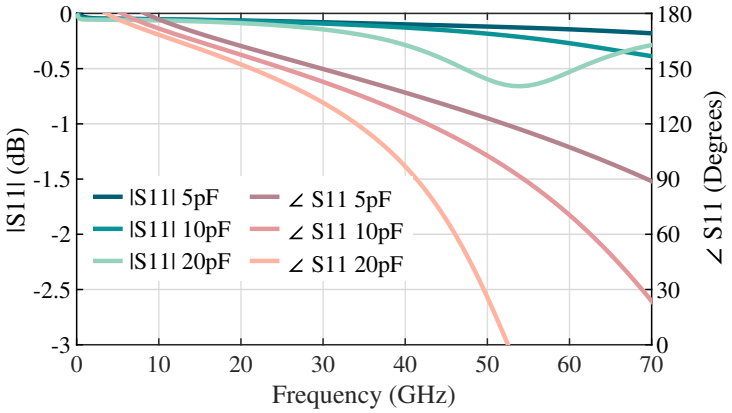


Figure 2.6: Magnitude and phase of S_{11} from full-wave electromagnetic simulations of three large bypass capacitors.

A more compact and effective way to terminate a transmission line with a short is to use a shunt capacitor at its resonant frequency. This design must be developed directly with full-wave EM simulations, as schematic elements do not accurately predict the resonance effects. Three example capacitors designed to resonate at approximately 32 GHz are displayed in Fig. 2.7. Capacitor (a) is centered over the transmission line, which is drawn on the top layer metal, with the lower metal layer connecting to a via on each side. Capacitor (b) is the same topology but with only one via, and capacitor (c) has a single via and is placed off to the side with minimum spacing to the transmission line. Their sizes vary to achieve resonance at the same frequency based on the number of vias and parasitic from the transmission line. The respective capacitor areas are $148 \times 80\,\mu\text{m}^2$, $78 \times 67\,\mu\text{m}^2$, and $52 \times 57\,\mu\text{m}^2$, all significantly smaller than the large capacitors simulated in Fig. 2.6. Each capacitor is connected to a short length of 50 Ω line.

A capacitor operating at its resonant frequency can be modeled by the circuit displayed in Fig. 2.8. The via(s) are represented by series inductor L_3 and R_3 in parallel with capacitor C_3. The impedance of the

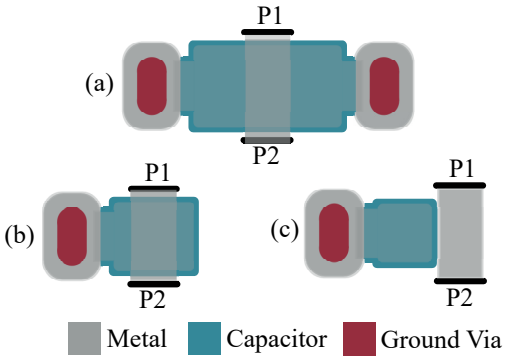


Figure 2.7: Resonant capacitor layouts, with areas of (a) $148 \times 80\,\mu\text{m}^2$, (b) $78 \times 67\,\mu\text{m}^2$, and (c) $52 \times 57\,\mu\text{m}^2$. Each capacitor is connected to a short length of $50\,\Omega$ line at the P1 and P2 ports.

via is described by:

$$Z_{via} = \frac{R_3 + j\omega(L_3 - L_3^2 C_3 - C_3 R_3^2)}{(1-\omega^2 L_3 C_3)^2 + (\omega C_3 R_3)^2} \tag{2.2}$$

The capacitor resembles the Modified Buttorworth Van-Dyke (MBVD) circuit whose impedance, Z_{cap} has been described in [62], with elements R_1 and C_1 in parallel with L_2, R_2, and C_2. Additional inductance from the transmission lines is captured by L_1 between the ports and shunt device. The overall impedance of the resonant structure, where Port 2 is terminated by the bias impedance, Z_{bias} becomes:

$$Z_{in} = j\omega L_1 + \frac{(Z_{cap} + Z_{via})(j\omega L_1 + Z_{bias})}{Z_{cap} + Z_{via} + j\omega L_1 + Z_{bias}} \tag{2.3}$$

At its resonant frequency, the shunt capacitor should reflect any incoming RF signal and operate independently of Z_{bias}. The three resonant capacitors in Fig. 2.7 are designed for approximately 32 GHz and terminated with $50\,\Omega$ port impedances. The S-parameters of these three structures are displayed in Fig. 2.9 with solid lines. The elements of the circuit model represented in Fig. 2.8 are fitted to match each of the three structures and matches up almost perfectly from dc to 70 GHz in both magnitude and phase of the S-parameters. Figure 2.9a shows how resonant capacitor (a) has the highest degree of reflection over the broadest bandwidth of the three structures, followed by (b) then (c). Centering the capacitor directly over the transmission line, as well as using multiple vias reduces the amount of parasitic inductance and resistance, allowing the resonant structure to operate over a broader bandwidth. A slightly larger capacitor size also makes it robust against frequency shifts due to process variations. At W-band for example, resonant capacitor sizes may approach the minimum width allowed by process design rules. In most cases, capacitor

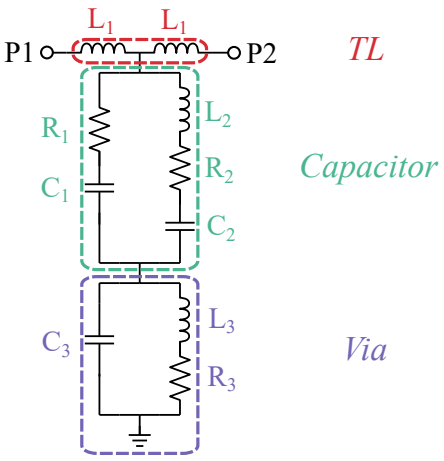
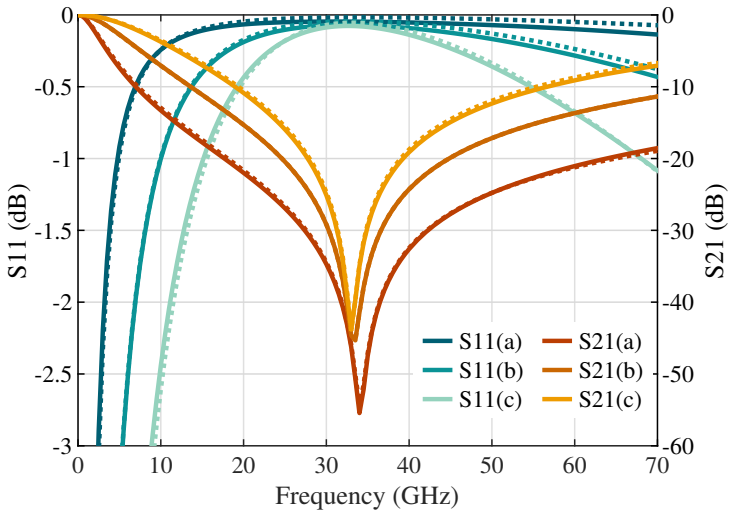
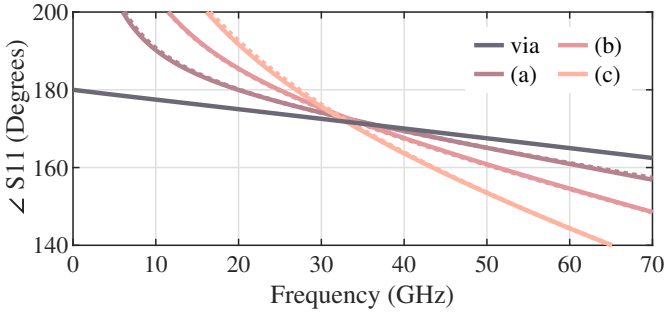


Figure 2.8: Circuit model of resonant shunt capacitor.

(a) is the preferable design choice, with the exception of bias lines with a large current draw, such as the output drain stage of a power amplifier, where capacitor (c) is preferable so that more metal layers can be used in the dc path. The phase of S_{11} is displayed in Fig. 2.9b, where the resonant structures are predictably close to 180°. A transmission line connecting to the structure can then be designed for approximately a quarter wavelength to present an open circuit to the matching network. An EM simulation of a metallized via is also plotted in Fig. 2.9b for comparison.



(a)



(b)

Figure 2.9: Simulated S-parameters of RF short EM structures (solid) and circuit models (dashed). (a) Magnitude and (b) phase of reflection and transmission coefficients for three RF short topologies, compared to a metallized via.

The resonant capacitors plotted in Fig. 2.9 perform better than arbitrarily large bypass capacitors in Fig. 2.6 at millimeter wave frequencies, in terms of their reflection in band and predictable phase. Resonant capacitors reflect over a wide bandwidth, while a quarter wave line presents an open at only a single frequency point. For wideband applications, the line length of the shorted stub should be built directly into the matching network [63]. The small resonant capacitor also allows low frequencies to pass through, which can be advantageous for applications such as supply modulation [53], but can also lead to instability. For gate biasing where there is little or no current draw, a small resistor can be placed after the resonant capacitor to

attenuate low-frequency signals. Larger capacitors can also be placed where space allows on the reticle or off chip to short low-frequency signals and prevent oscillations, as in [18].

An alternative method to shunt capacitors is terminating the bias transmission line with radial stubs. Several types of radial stubs have been explored in [64] on a Rogers substrate. These topologies perform well over a broad bandwidth and are suitable if fabrication allows. However, radial stub biases on integrated circuits consume a large area and are used only at very high frequencies, such as W-band and above [33]. Below this frequency, they are typically only used in hybrid circuit designs.

2.1.2.2 Bias-Circuit Test Structures

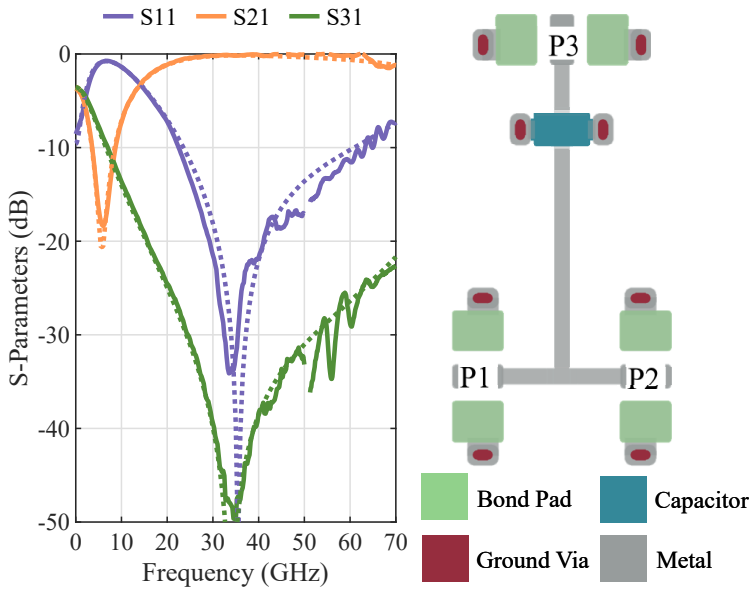


Figure 2.10: Measured (solid) and ideal (dashed) small-signal performance of Ka/U-band $\lambda/4$ bias line.

Two bias-line test structures with a resonant capacitor are fabricated in the WIN NP12 process. First, a Ka/U-band bias is designed using capacitor (c) from above, displayed in Fig. 2.10. The measured $|S_{21}|$ is above –0.5 dB for over an octave of bandwidth from 22.6 to 63.9 GHz, while $|S_{11}| < -10$ dB and $|S_{31}| < -25$ dB within this range. This design is repeated at V/W-band in Fig. 2.11. The resonant capacitor in this test structure has a size of $68 \times 46\,\mu\text{m}^2$. Simulated $|S_{21}|$ is above –0.5 dB from 43 to 102 GHz for this bias line, covering all of V and most of W-band. Simulated $|S_{11}|$ and $|S_{31}|$ are below –12 dB and –

20 dB respectively within this range. Measured results follow the trend in simulation with some additional measurement limitations due to the reduced dynamic range of test equipment in W-band.

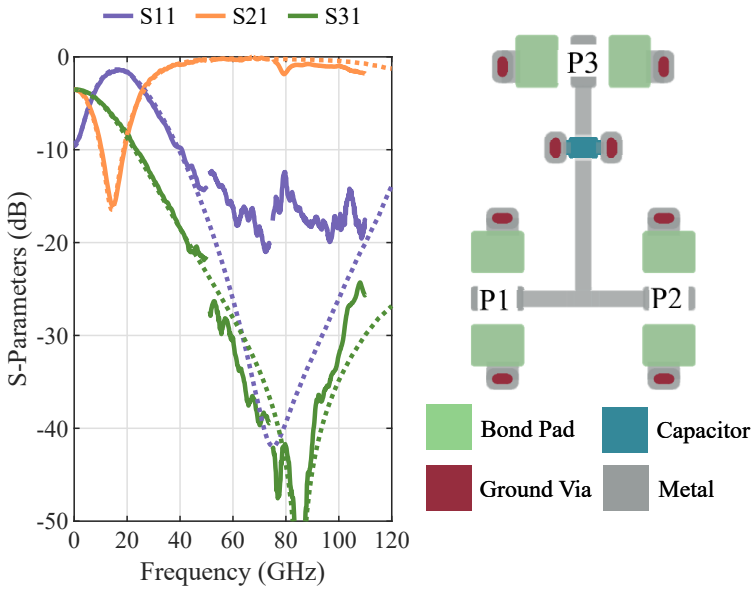


Figure 2.11: Measured (solid) and ideal (dashed) small-signal performance of V/W-band $\lambda/4$ bias line.

2.1.3 Coupler-Line Filter Bias Lines

Above 100 GHz, lumped resonant capacitors begin to reach minimum allowable dimensions in MMIC processes. An alternative way to isolate the RF from the dc current is with coupled lines [65]. One technique is to implement coupled short stubs, as displayed in Fig. 2.12a. A shorted stub on either side of the main transmission line acts as a band stop filter centered around the frequency where the stub is $\lambda/4$. Simulated S-parameters of this filter are shown in Fig. 2.12b with one, two, and three coupled sections, where adding more sections sharpens the roll-off and decreases the return loss, as expected. This approach operates over a moderate bandwidth, such as 80–100 GHz and adding multiple sections of coupled stubs also significantly increase the size of the bias line. The benefit, however, is the potential for a very sharp roll-off and high RF rejection while allowing large dc current handling. The coupled-line structure can also be curved to fit in a more compact space [66].

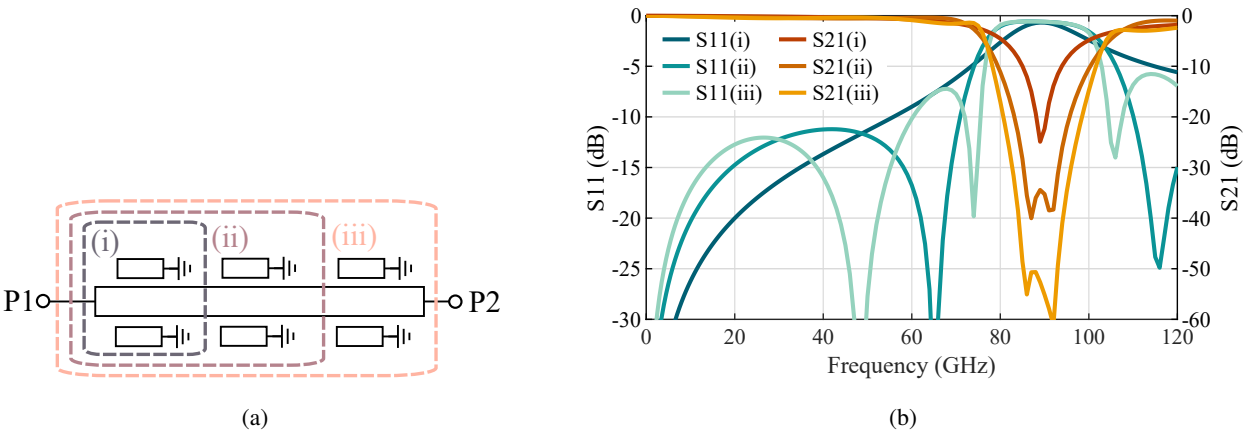


Figure 2.12: (a) Circuit schematic of coupled-line bias line with one (i), two (ii), and three (iii) coupled sections. (b) Simulated S-parameters of the three coupled-line filters.

A bias line using a single coupled-line short stub section at 90 GHz is designed and displayed in Fig.2.13. The simulated structure operates over a narrower bandwidth with insertion loss less than 0.5 dB from 87 to 92 GHz. Simulated $|S_{11}|$ and $|S_{31}|$ are both below –20 dB within this range. Measured results follow the simulation trends.

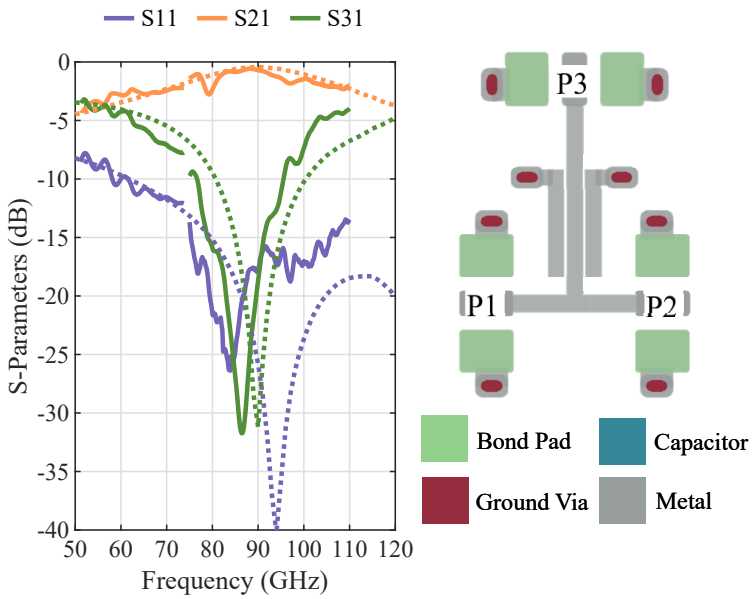


Figure 2.13: Measured (solid) and ideal (dashed) small-signal performance of W-band coupled-line bias line. The discontinuity around 75 GHz is due to the waveguide-band extenders of the network analyser.

Table 2.1: Comparison of Bias Line Test Structures

Topology	Center Frequency (GHz)	Fractional Bandwidth (%)*	Average $\lvert S_{21}\rvert$ (dB)	Average $\lvert S_{31}\rvert$ (dB)	Average $\lvert S_{11}\rvert$ (dB)
Parallel LC	33	6.2	-1.29	-14.13	-14.28
Inductor	26	37.4	-0.82	-15.04	-14.41
K-band $\lambda/4$ TL	44	97.0	-0.15	-33.36	-16.35
W-band $\lambda/4$ TL^{+}	77	107.2	-0.42	-32.50	-25.87
Coupled Filter^{+}	90	28.3	-0.80	-15.06	-23.64

* Referenced to 1 dB bandwidth of minimum $\lvert S_{21}\rvert$
+ Simulated Values

A comparison of the five different bias line test structures is displayed in Table 2.1. For the two W-band test structures, the simulated performance is listed due to the reduced dynamic range of the network analyzer when frequency extenders are added. Of the five topologies, the transmission lines terminated in a resonant capacitor have by far the greatest fractional bandwidth and greater isolation than the other structures. The parallel *LC* resonant network and inductor are designed at their upper frequency limit as the forward loss surpasses 1 dB above 30 GHz. The coupled-line bias line performs similarly to the inductor and is best suited for frequencies at W-band or above as its footprint decreases and multiple coupled sections can be added to take advantage of the high RF rejection and high dc current handling. As mentioned previously, the quarter-wave line can be used above W-band by replacing the resonant capacitor with a resonant radial stub to achieve similar performance.

2.2 Example Circuits with Discussion of Bias Lines

Some of the described techniques are implemented in a narrowband power amplifier at Ka-band, a W-band amplifier with approximately 30 % bandwidth and a 46–102 GHz wideband cascode amplifier. The bias line design in each case is discussed.

2.2.1 Ka-band Power Amplifier

A Ka-band amplifier is designed in the Qorvo QGaN15 process, featuring 150 nm gate length GaN HEMTs and a number of passive components on a 100 μm SiC substrate. A two-stage amplifier, Fig. 2.14,

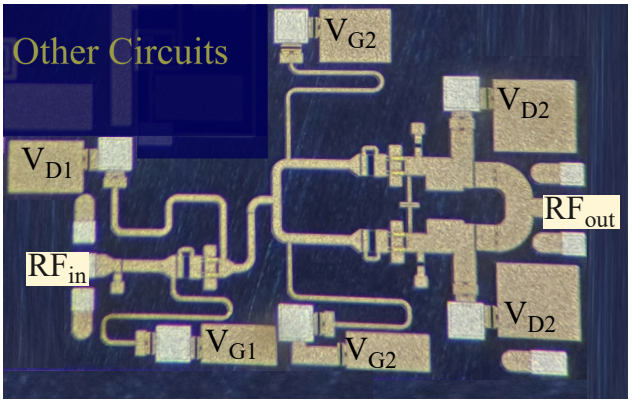


Figure 2.14: Photograph of narrowband 32 GHz harmonically terminated power amplifier. The MMIC implemented in the Qorvo 150-nm GaN process has a 2.2 mm by 1.6 mm footprint.

is designed with a 1:2 staging ratio and a harmonically-terminated reactively power combined output stage, discussed in depth in Chapter 3. The circuit is narrowband by design, centered around a target frequency of 32 GHz. Simulated and measured S-parameters of the amplifier are displayed in Fig. 2.15, with a measured maximum $|S_{21}|$ of 19.7 dB and a 6.8 % fractional 3 dB bandwidth.

The amplifier contains four separate bias lines: two gate lines and two drain lines. The two bias lines of the second stage are mirrored on either side of the amplifier for symmetry to ensure an identical impedance presentation to the matching network. Due to the narrowband nature of this circuit, the bias lines are designed independently of the matching networks to present an open circuit at the frequency of interest, with the exception of the output stage which uses a quarter-wave line terminated in a resonant capacitor. First, the resonant capacitor is designed. This element has a size of $44 \times 104\,\mu\text{m}^2$ and allows the dc current to pass over the top layer. One major difference between this capacitor model and those used for test structures in Section 2.1.2, is that the QGaN15 process allows capacitors to be fabricated directly over vias. Bias lines V_{G1}, V_{D1}, and V_{G2} are all composed of a quarter-wave transmission line terminated by the resonant capacitor. These present an open circuit to the matching network at 32 GHz, allowing it to be designed independently. In the gate lines, a small resistor is placed directly between the resonant capacitor and dc pad for stability. The output drain biases V_{D2} also contain a transmission line terminated by the resonant capacitor, but the line is much shorter and wider than in the previous three bias lines. In this case, the bias line impedance is designed into the output combiner and used for matching. All four bias networks

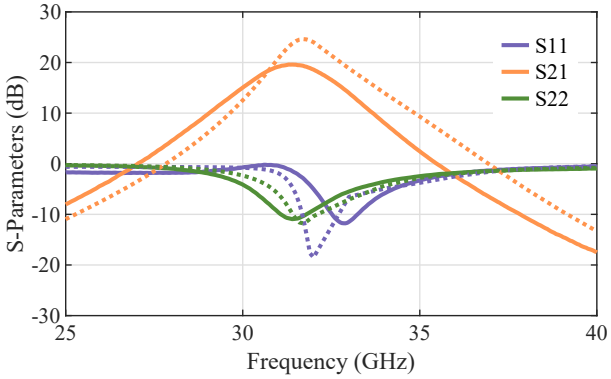


Figure 2.15: Measured (solid) and simulated (dashed) S-parameters of harmonically tuned PA. Circuit is biased with $V_D = 28\,V$, $I_{D1} = 5\,mA$, $I_{D2} = 7\,mA$.

contain a much larger shunt capacitor at the bias pad with a small decoupling resistor. These capacitors are drawn arbitrarily large to fit into the remaining space on the die, and help attenuate low frequency signals.

Each bias line is simulated with Port 1 at the junction to the matching network and Port 2 at the dc pad. The four unique bias lines are plotted in Fig. 2.16. Their resonances are centered close to 32 GHz due to the identical resonant capacitor used in all cases, but the responses are not at exactly the same frequency due to the interaction with other elements in the networks. The bypass capacitor also lowers $|S_{21}|$ below the design frequency, as seen in Fig. 2.16 where the $|S_{21}|$ plots flatten around 10 dB between 15 GHz to below 1 GHz. In comparison, isolation of the circuit in Fig. 2.10 decreases below 10 dB at around 8 GHz without a large bypass capacitor. This attenuation at low frequencies out of band is critical for maintaining stability.

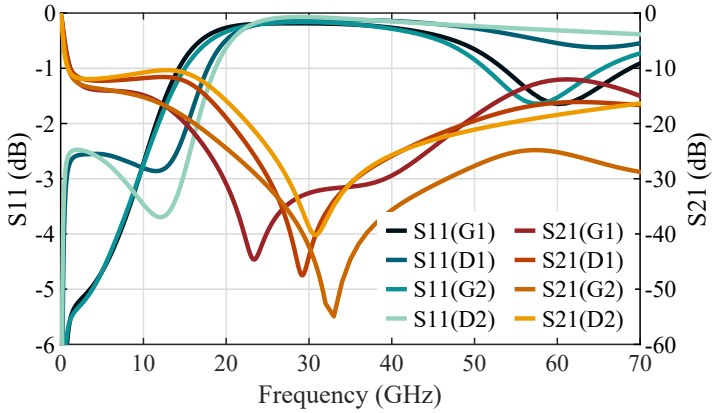


Figure 2.16: Simulated S-parameters of bias lines implemented in the two-stage 32 GHz GaN MMIC amplifier from Fig. 2.14.

2.2.2 W-band Amplifier

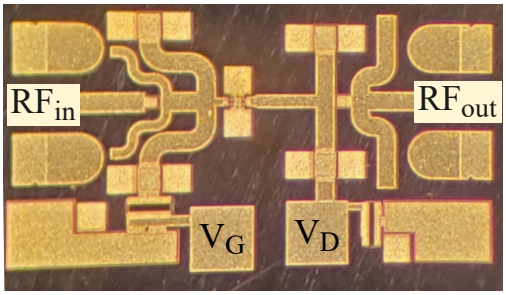


Figure 2.17: Photograph of a single-stage broadband W-band MMIC amplifier fabricated in the HRL T3 40-nm GaN process, 1.2 mm by 0.6 mm in area.

The single-stage W-band MMIC amplifier shown in Fig. 2.17 uses one $2 \times 25\,\mu$m device. The amplifier is designed in the HRL T3 process, featuring 40 nm GaN HEMTs and fabricated on a 50 μm SiC substrate [45]. Simulated and measured S-parameters of the amplifier are displayed in Fig. 2.18. The amplifier has a maximum gain of 10.3 dB at 84 GHz with a measured 28.8% 3 dB fractional bandwidth. Similar to the 32-GHz amplifier, the bias lines in this circuit are designed as a transmission line terminated with a resonant capacitor. However, both the gate and drain biasing networks are designed into the matching networks, allowing broadband operation.

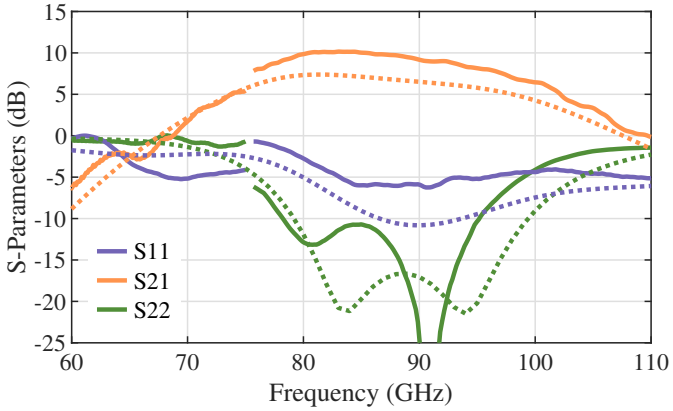


Figure 2.18: Measured (solid) and simulated (dashed) S-parameters of the W-band amplifier MMIC from Fig. 2.17. Separate upconverson setups are used to capture S-parameters in V and W bands, accounting for the discontinuity in measurements. Circuit is biased with $V_D = 12\,V$, $I_D = 13\,mA$.

The bias lines of the single-stage W-band amplifier are simulated separately with results given in Fig. 2.19. The bias lines present a high reflection to RF with $|S_{11}|$ greater than -0.25 dB from 40 GHz to at least 200 GHz. The $|S_{21}|$ is below –20 dB throughout this range.

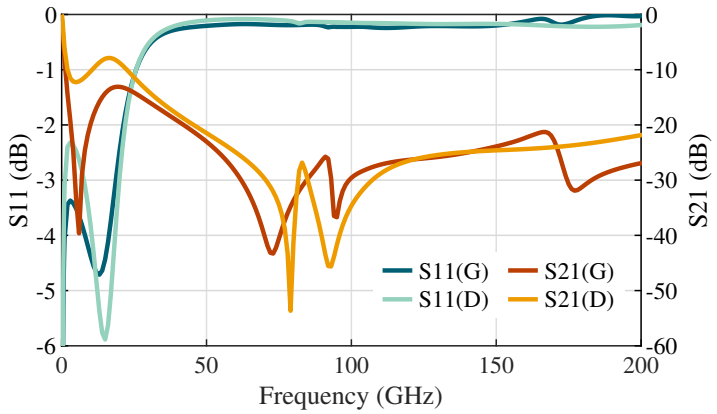


Figure 2.19: Simulated S-parameters of the bias lines in the W-band amplifier from Fig. 2.17.

In contrast to the separate stability networks in the 32-GHz amplifier RF path, the stability networks for the single-stage W-band amplifier are completely integrated into the bias line design. As mentioned previously, larger bypass capacitors with small "de-Q-ing" resistors are placed directly at the bias pad, but after the in-band resonant capacitors, as can be seen in Fig. 2.17. These arbitrarily large capacitors, typically

made as large as space allows on the die, are not seen by the in-band signal, but attenuate lower frequencies that may propagate on the bias lines. To further emphasize this point, K-factor is plotted for the single stage amp with and without the bypass capacitors in Fig. 2.20. The trace without bypass capacitors clearly crosses into the conditionally unstable zone ($K < 1$) several times between 5-7 GHz whereas the trace with bypass capacitors does not. Conditional instability indicates that the device may oscillate under some impedance conditions at the ports. Generally, conditional instability is acceptable in-band, provided that the impedance presented to the device is carefully controlled. However, it is essential to guarantee unconditional stability outside of the band of operation where the port impedances are not known, commonly done by including large bypass capacitors.

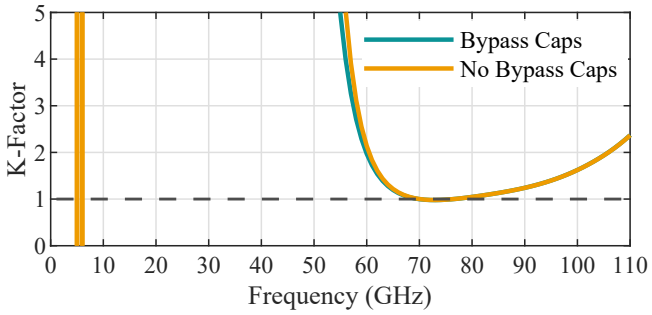


Figure 2.20: Simulated K-factor of the single-stage W-band amplifier.

2.2.3 Wideband Cascode Amplifier

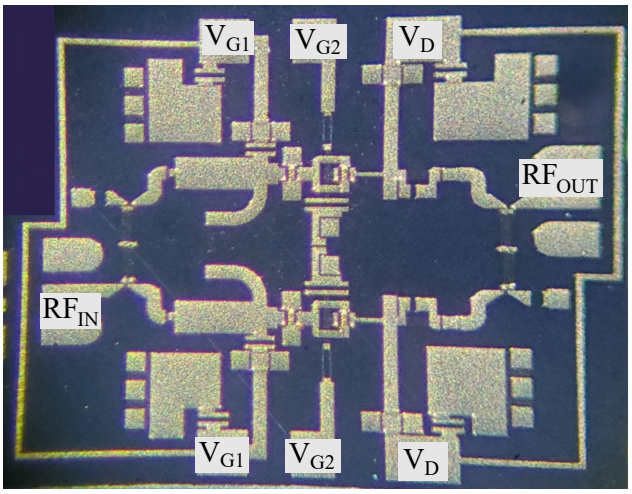


Figure 2.21: Photograph of broadband 50–110 GHz MMIC amplifier fabricated in the HRL T3 40-nm GaN process, 2.1 mm by 1.6 mm in area.

A wideband cascode amplifier, Fig. 2.21, also designed in the HRL T3 process consists of two single-stage cascode amplifiers connected in a balanced configuration, with all HEMTs $2 \times 25\mu m$ in size. The design of this circuit is discussed in depth in Chapter 5. A photograph of the MMIC is displayed in Fig. 2.21. Simulated and measured S-parameters of the amplifier are given in Fig. 2.22. A flat gain of 7 dB is measured with a 3 dB bandwidth of 46–102 GHz. The broadband performance is due to the cascode architecture as well as its balanced configuration for matching. Nonetheless, the bias lines are essential for operating over the entire frequency range and maintaining stability. Separate setups are used to measure S-parameters in K, V, and W-bands, accounting for the discontinuities in measurements.

Some of the bias lines in this broadband circuit are designed to present small amounts loss due to stability considerations. S-parameters of the three bias lines are plotted in Fig. 2.23. The drain of the cascode cell uses the same technique as the first W-band amplifier presented: a microstrip line terminated in a resonant shunt capacitor with a larger shunt capacitor placed off of the bias pad. The performance is also very similar, with a high degree of reflection across the entire bandwidth and high insertion loss above 20 dB beyond 40 GHz. The gate bias on the first transistor applies the same technique with one difference; a small

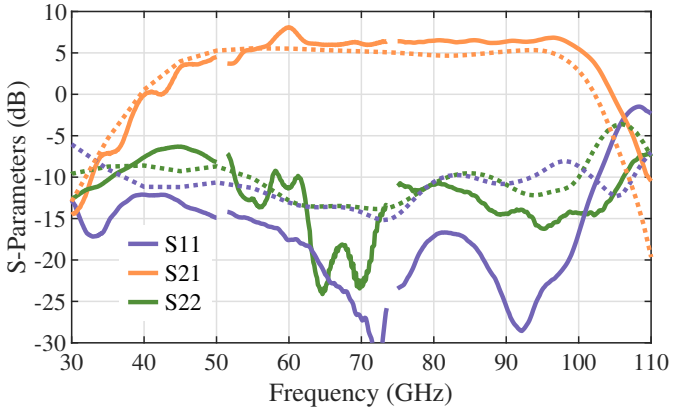


Figure 2.22: Measured (solid) and simulated (dashed) S-parameters of the cascode MMIC amplifier from Fig. 2.21. Circuit is biased with $V_D = 12\,V$, $I_D = 38\,mA$.

resistor is placed between the capacitor and transistor, as opposed to after the resonant capacitor before the bias pad. This is done intentionally to add loss, rather than including a parallel *RC* stability network. The insertion loss is comparable to that of the drain bias network, while a return loss between 2 and 3 dB is simulated above 5 GHz, corresponding to the small amount of resistance included in the network design. Finally, the second gate bias is implemented using a mesa resistor. Simulations of the mesa-resistor bias indicate a minimum insertion loss of 27 dB at dc, while the return loss ranges from 0.7 to 2.3 dB within the band of operation. The gate of the second device is not directly in the signal path, however, so it does not add loss to the circuit.

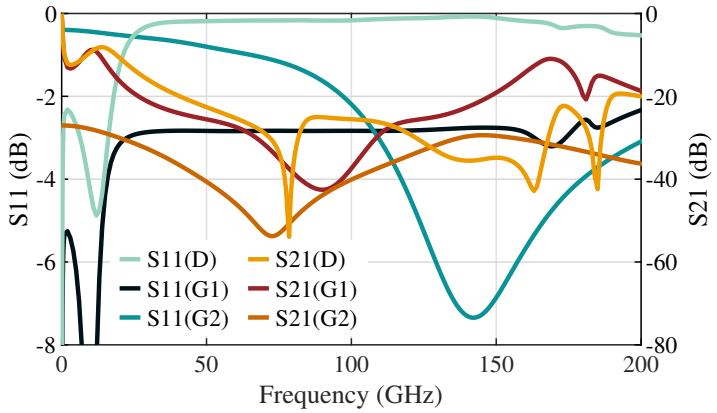


Figure 2.23: Simulated S-parameters of bias lines for the cascode MMIC amplifier of Fig. 2.21.

2.3 Conclusion

This chapter explores the design of different bias networks and their applications to millimeter wave MMIC amplifiers. Low-frequency techniques such as RF chokes, parallel resonant structures, and bypass capacitors are analyzed in both measurement and simulation. It is determined that the scaling of these techniques beyond 30 GHz results in performance degradation. We show that RF signals can be more effectively reflected using microstrip lines with resonant structures such as small shunt capacitors, coupled filters, and radial stubs, while still allowing a path for dc current. Bias lines can also help amplifier stability by isolating the RF path from interference at other frequencies. This is achieved by adding large bypassing capacitors with some attenuation on the die or off chip. Three GaN MMICs are presented with a detailed discussion of their bias networks: a single-stage W-band amplifier; a two-stage Ka-band amplifier, and a power-combined cascode V/W-band amplifier. The techniques discussed in this chapter apply to conventional MMIC amplifiers and the results are given in [67]. Interesting topics for further research related to bias line design include, e.g., supply-modulated power amplifiers and dc collection lines for rectifiers.

Chapter 3

Ka-Band Power Amplifiers

3.1 Harmonically Terminated Power Amplifiers

Millimeter-wave communication allows for increased data rates compared to lower frequencies. For NASA, improving Ka-band communication capabilities is essential to increasing uplink and downlink data rates between ground and satellites. This advancement also has applications in improving navigation use for deep space missions and autonomous operations, such as rovers and helicopters. The potential of GaN power amplifiers in the millimeter-wave regime for these applications has placed it on the list of NASA Jet Propulsion Laboratories' strategic technologies [19]. For communication over vast distances, e.g. interplanetary ones, kilowatts of transmitted power are required. Currently, vacuum tube amplifiers can output hundreds of watts at these frequencies while operating with efficiencies up to 50% or more [68, 69]. However, they often add significant weight and require large power supplies to operate, while their operating lifetime is limited compared to solid state amplifiers. GaN is investigated as a potential candidate to replace tube amplifiers. Current state-of-the-art Ka-band solid state amplifiers can output a few watts of power with up to 40% efficiency, but can improve one of these two metrics while sacrificing the other [17, 18, 70–73]. To compete with tube amplifiers, several power amplifier MMICs can be spatially combined. This has been demonstrated at millimeter waves with beyond 90% combining efficiency [74–77]. While these assemblies do not yet surpass tube amplifiers in terms of output power or efficiency, new GaN technologies are quickly closing in on their performance. In this chapter, the design of a high efficiency narrowband 32 GHz power amplifier in two GaN technologies is discussed to test the current peak performance limits.

3.1.1 Process Selection

Several process design kits are evaluated as potential candidates to design this power amplifier. Among the factors are cost, operating frequency, reliability, and simulated characteristics based on load pull, such as efficiency and output power. Only GaN foundries are considered, as the design requires a high power density: at least 1 W of output power with two stages. The WIN NP1500 is first selected. This process features 0.15 μm depletion mode HEMTs with a 28 V operation and an f_T of 34.5 GHz. Two metal layers provide the ability to design low loss transmission lines, while lumped MIM capacitors, TaN resistors, and inductor pcells are included. The circuits are fabricated on a 4 mil substrate with through substrate vias providing ground connections. Furthermore, WIN Semiconductors has been a generous partner with the University of Colorado Boulder, providing free runs of this advanced process.

To test the validity of this process at Ka-band, JPL tested several WIN devices and performed load pull along with large signal measurements. This data was provided to us for analysis before continuing with the design [4]. Drive-up curves at 32.05 GHz are plotted in Fig. 3.1. Displayed is output power, gain, drain efficiency, power added efficiency, and drain current vs. input power. The curves are representative of a $4 \times 50\,\mu$m device with a 24 V drain voltage and a 20 mA quiescent drain current. However, this analysis is performed on both $4 \times 50\,\mu$m and $8 \times 50\,\mu$m devices at drain voltages ranging from 20 – 28 V and quiescent currents from 1 – 40 mA, all at the same frequency.

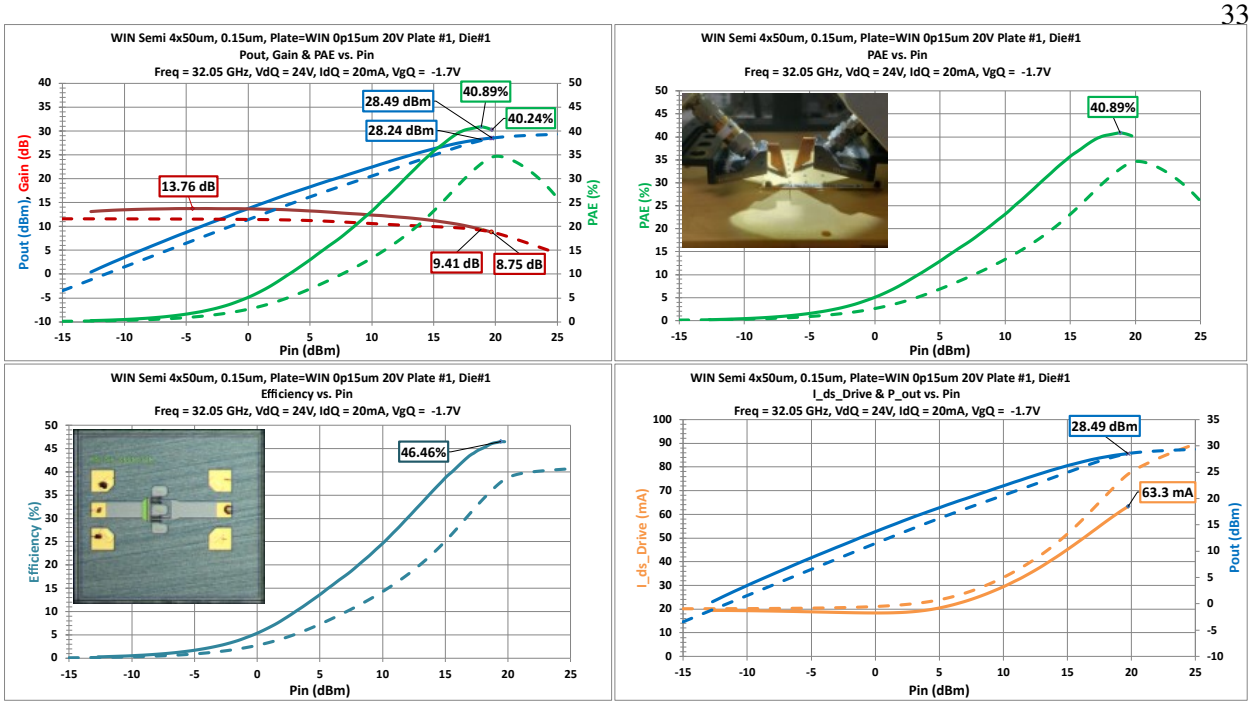


Figure 3.1: Comparison of measured (solid) and simulated (dashed) characteristics of a $4 \times 50\,\mu$m device in WIN NP1500 process. Measured data was performed and provided by NASA Jet Propulsion Laboratory [4].

The curves displayed in Fig. 3.1 are closest to the design conditions of the output stage in terms of periphery and bias, discussed in Section 3.1. While the accuracy between measurement and models varies in the drive-up curves for each measurement condition, of great significance is that the measured results in Fig. 3.1 tend to perform better than in simulation, i.e. higher measured efficiency and comparable output power. These results are encouraging and had a significant impact on the decision to select this process for the first design. The amplifier is then repeated in the QGaN15 process for comparison. Qorvo has also been a valuable partner with CU Boulder as Qorvo's Tier 1 university, and several MMICs have been designed in their foundry with excellent results, e.g. [78]. The QGaN15 process employed for this design is also a 28 V process with $0.15\,\mu$m depletion mode HEMTs fabricated on a 4 mil substrate. Pcells for MIM capacitors, TaN resistors, and lumped inductors are also included. Additionally, this PDK allows shunt capacitors over vias which reduce parasitic losses.

3.1.2 Power Amplifier Design

The WIN NP1500 and QGaN15 processes are selected for the power amplifier design due to their availability and demonstration to reach the desired specifications. Load pull simulations are performed on several devices to determine the output periphery and staging ratio. Simulations on a 2 $\times$ 50 μm device, a 4 $\times$ 50 μm device, and an 8 $\times$ 50 μm device, all biased in deep AB region are performed in the WIN PDK. Power added efficiency (PAE) contours generated from load pull for the 4 $\times$ 50 μm device are displayed in Fig. 3.2. A peak efficiency of 57% is displayed with an input power of 19 dBm. A maximum output power of 29.7 dBm is also measured under these same conditions. Load pull of a 4 $\times$ 50 μm Qorvo device presents a peak PAE of 44.2% and output power of 29.3 dBm. Two of these devices are chosen for the output stage of the PA, utilizing a power combining output matching network to boost the delivered power by approximately 3 dB. The first stage is similarly determined from load pull, with the requirement to compress the output stage for maximum efficiency ($\approx$ 22 dBm output to drive two 4 $\times$ 50 μm devices), while still operating efficiently. A 2 $\times$ 50 μm device is selected for the first stage, yielding a 1:4 ratio for the entire two stage amplifier.

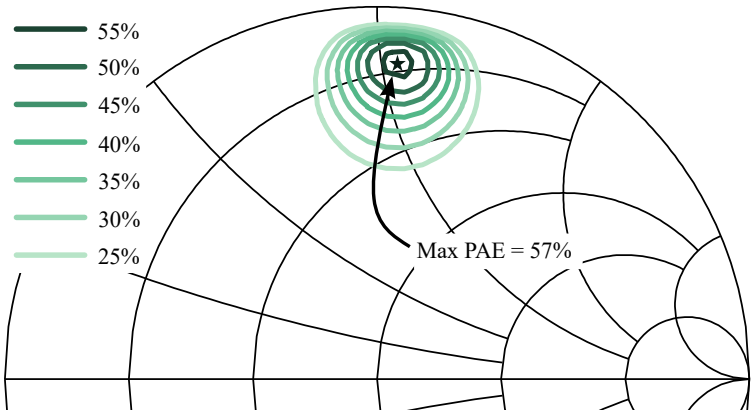


Figure 3.2: Fundamental load pull contours at 32 GHz of 4 $\times$ 50 μm device in WIN NP1500 process. Device is biased with 28 V drain voltage and 100 mA/mm drain current.

3.1.2.1 Second Harmonic Termination Output Combiner

The narrow frequency requirements of this amplifier allow the use of efficiency enhancement techniques that do not necessarily translate to wideband design. Waveform shaping is investigated to boost PAE at 32 GHz. In particular, properly terminating the second harmonic at 64 GHz decreases the overlap between voltage and current by [49]. This effectively reduces power dissipation in the device and increases efficiency.

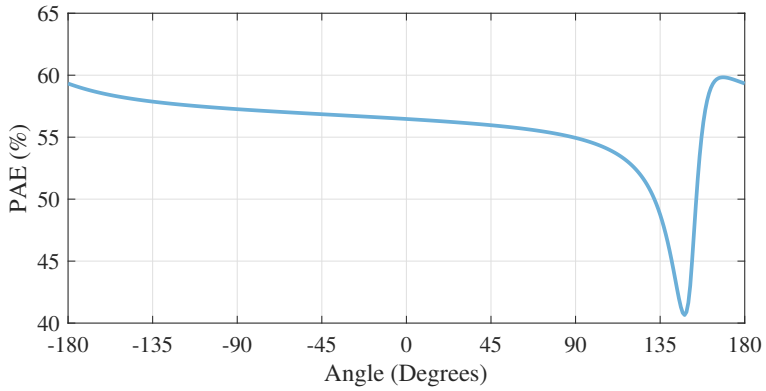


Figure 3.3: Second harmonic angle sweep of $4x50\,\mu$m device in WIN NP1500 process. The fundamental load impedance is matched for maximum PAE at 32 GHz with the second harmonic magnitude confined to the edge of the Smith Chart.

The application of this technique is investigated at the device level. From the initial load pull results, the output device is terminated using ideal tuners for maximum efficiency at the output. The input is conjugate matched. The second harmonic is then confined close to the edge of the Smith Chart, $0.9 < \Gamma < 1$, on the ideal tuner, as the angle is swept around the circumference, -180° to $+180^\circ$. Fluctuations in PAE are then observed as the angle is swept, as plotted in Fig. 3.3. PAE peaks 59.8% when the second harmonic is reflected at an angle of 169°. On the other hand, a 16% dip relative to the peak fundamental PAE is observed when the angle is 148°.

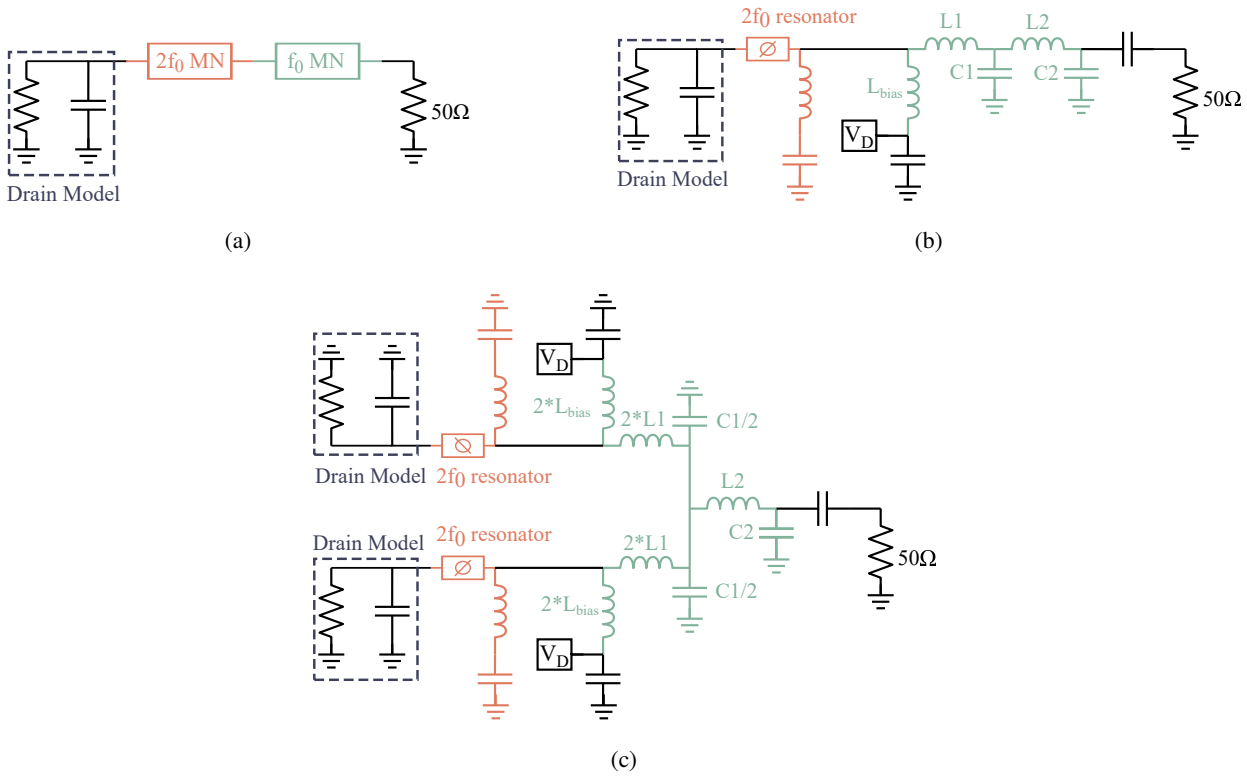


Figure 3.4: Equivalent circuit of output network (a) blocks, and (b) lumped element implementation of matching networks, and (c) even-mode lumped element two-way combiner.

Harmonically tuned combiners have previously been demonstrated in SiGe [79] at X-band, and have shown to increase efficiency and output power in GaN at Ka-band [80, 81]. A proper 64 GHz termination is incorporated into the output combiner matching network in a number of steps, as illustrated in Fig. 3.4. A general block diagram is displayed in Fig. 3.4a. The network is designed using only passive elements for increased simulation speed. The drain impedance is modeled using a parallel *RC* whose values are derived from the maximum PAE point on the fundamental load pull sweep. The second harmonic network is then placed directly after the drain to reflect the second harmonic immediately at the output of the HEMT, followed by the fundamental matching network which incorporates the first network impedance into the design. The output is terminated in 50 Ω. This is expanded to a single-ended schematic lumped element network in Fig. 3.4b. The second harmonic is reflected using a series *LC* resonant short with an additional phase element to tune PAE along the simulated plot in Fig. 3.3. The fundamental matching network is

realized with a series bias inductor and two sets of *LC* low pass networks. These elements can then be separated into a combiner by doubling the value of the inductors and halving the value of the capacitors [63]. This is performed on the first three elements. To translate this topology to a layout, the lumped inductors are converted to microstrip lines, while shunt capacitors are available in the selected PDKs. DC biasing is performed with a microstrip line connected to a resonant shunt capacitor, as discussed in Chapter 2.

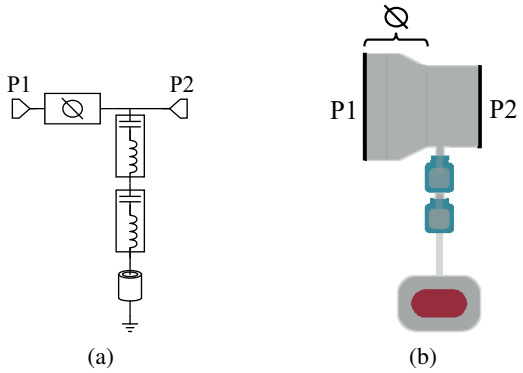
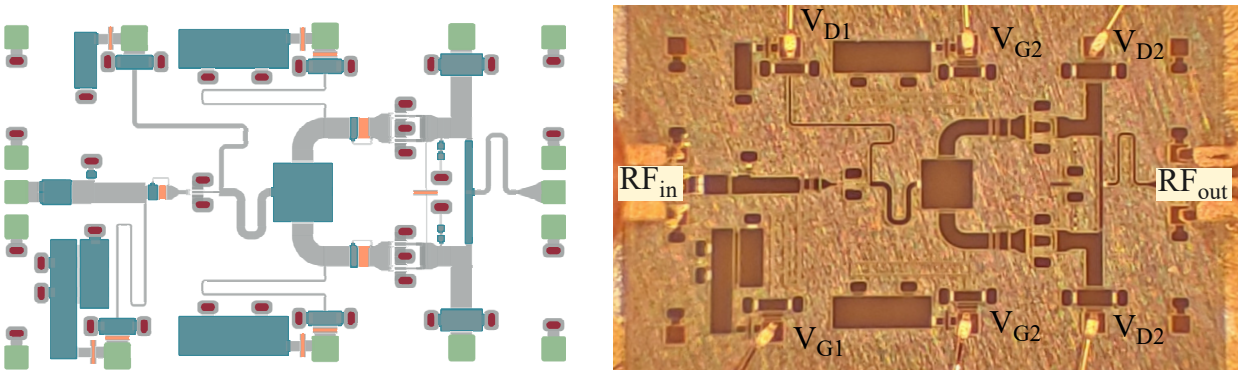


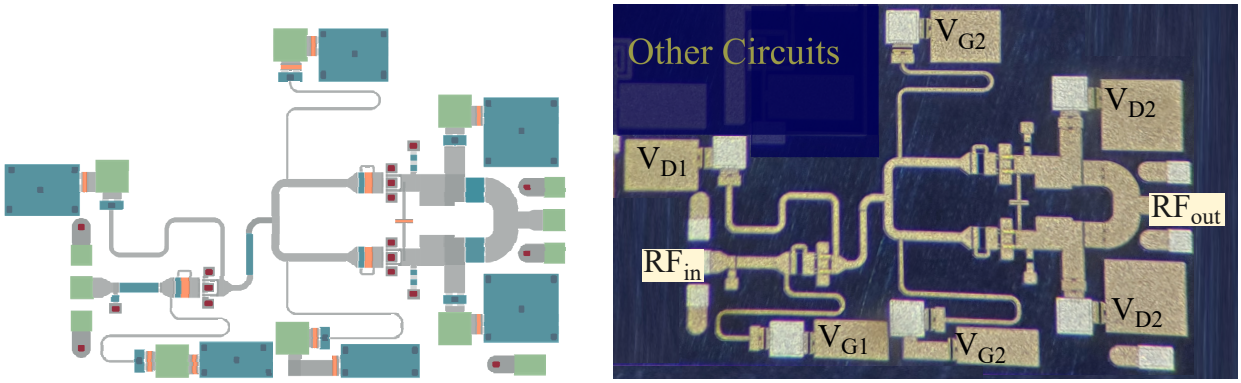
Figure 3.5: Second harmonic termination (a) schematic and (b) layout. Capacitors are $18\,\mu$m $\times$ $18\,\mu$m (0.075 pF).

The second harmonic termination is first designed as a series *LC* resonator with some added phase at the input. The impedance of an ideal series *LC* circuit is $Z_{in}(\omega) = j\omega L + 1/(j\omega C)$. This impedance is 0 when $\omega = 1/\sqrt{LC}$. Above this resonant frequency, the inductive term dominates the equation, while the opposite is true below the design frequency. Therefore, the network adds additional capacitance at the fundamental frequency which is incorporated into the matching network. Due to the minimum size constraints in the process, two small capacitors are placed in series along with a thin inductive line to generate a series resonance at 64 GHz. Via parasitics are also taken into account in simulation. A schematic and layout depiction of this network is displayed in Fig. 3.5. From these figures, Port 1 is connected to the drain of the HEMT, while Port 2 is connected to the fundamental matching network. The additional phase is inserted with a short transmission line whose width is the same as the HEMT manifold, and a taper reducing the width to match $50\,\Omega$.



(a) (b)

Figure 3.6: (a) Layout and (b) photograph of WIN NP1500 harmonically terminated 32 GHz power amplifier with a footprint of 2.4 mm $\times$ 1.5 mm.



(a) (b)

Figure 3.7: (a) Layout and (b) picture of QGaN15 harmonically terminated 32 GHz power amplifier with a footprint of 2.2 mm $\times$ 1.6 mm.

The remainder of the combiner is performed by converting the lumped element ideal network to transmission lines. The power amplifier is designed initially in the WIN NP1500 process and repeated in the Qorvo GaN15 process using identical topologies, staging ratios, and techniques for a fair comparison. The layouts and picture of each amplifier are displayed in Figures 3.6 and 3.7, respectively. For each amplifier, the bias lines (aside from the second stage drain at the combiner) are realized using a quarter wave transformer connected to an RF short at the dc port, presenting an open to the matching network. The interstage matching network presents the impedance to maximize efficiency of the first stage drain from load

pull, while splitting the power to conjugate match the second stage gate. Meanwhile, the first stage gate is conjugate matched from 50 Ω. DC blocking capacitors are built into the matching networks.

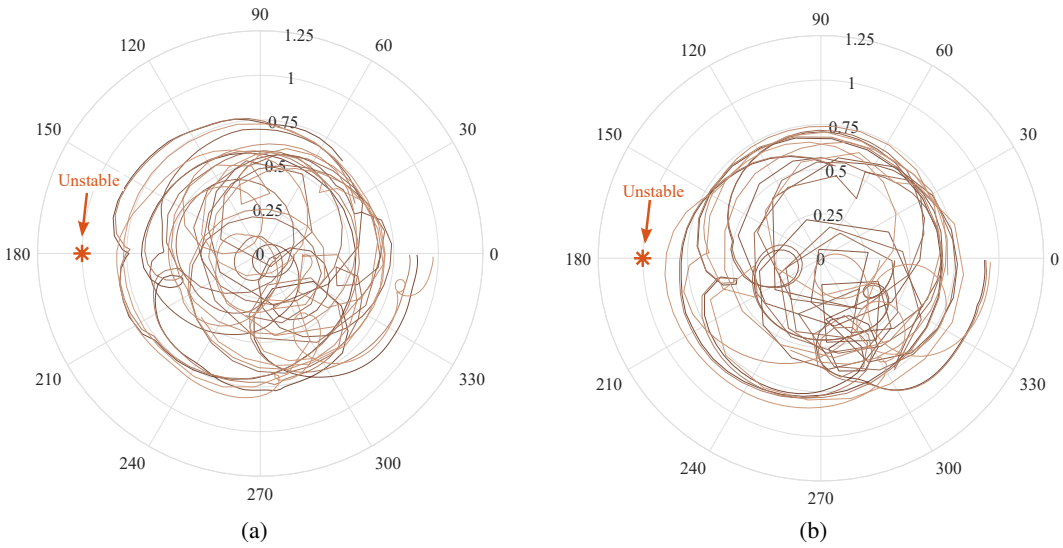


Figure 3.8: Nyquist sweep of (a) WIN and (b) QGaN15 32 GHz harmonically terminated amplifiers.

Amplifier stability is guaranteed by incorporating a number of different networks into the layout. First, capacitor ladders are added to the dc bias paths as space allowed on the reticle. Small series resistors help to "de-Q" any capacitor self resonance and attenuate low frequency signals. Second, odd mode stability resistors are connected to the two inputs of the combiner. Third, a series *LC* network is connected to the gate of each device with its resonant frequency tuned to 32 GHz. A small resistor is connected in parallel to attenuate out-of-band signals while those in band do not experience loss. Simulated Nyquist stability plots of the two amplifiers are displayed in Fig. 3.8, with a 32 GHz input source, analyzing amplifier stability from 100 MHz to 100 GHz. Probes are placed at the gates and drains of each HEMT to generate these curves. The simulation is repeated at a number of input frequencies and source/load/bias impedances to ensure stability over all possible test conditions. The (-1, 0) point is not encircled, indicating the amplifier is unconditionally stable.

3.1.3 Measured Results

The power amplifiers under test are displayed in Figs. 3.6b and 3.7b. The die is mounted onto a CuMo carrier and bonded to off-chip capacitors. The MMICs are probed on a Summit 9000 probe station with 150-μm pitch probes from 15-40 GHz. An E8364C PNA Network Analyzer is used to capture small signal S-parameters. SOLT calibration is performed on a Cascade Microtech impedance standard substrate using coefficients from the probe manufacturer.

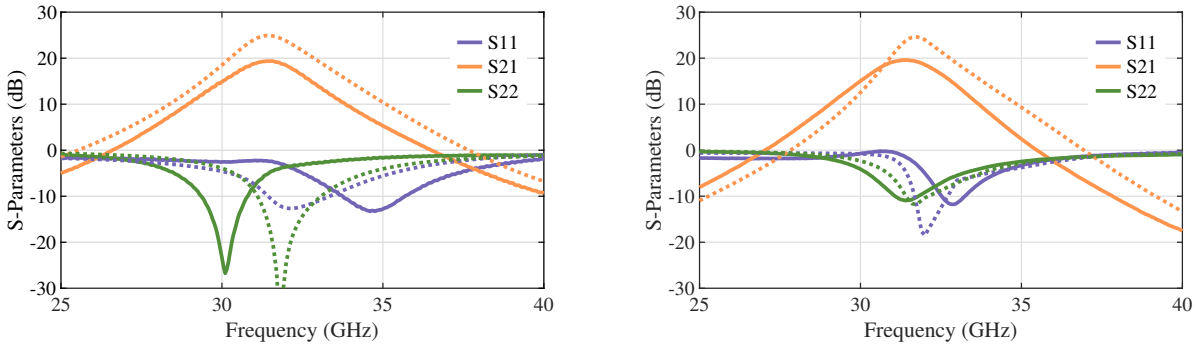


Figure 3.9: Simulated (dashed) and measured (solid) S-parameters of 32 GHz harmonically terminated amplifiers fabricated in the WIN Semiconductors NP1500 (a) and Qorvo QGaN15 (b) processes.

Measured and simulated S-parameters of both power amplifiers are displayed in Fig. 3.9. Both designs have a very similar simulated and measured maximum gain within 200 MHz of 31.5 GHz. The simulated curves display a maximum $|S_{21}|$ of 24.9 and 24.6 dB for the WIN and Qorvo designs, respectively, while measured gain is approximately 5 dB lower for both, at 19.6 and 19.4 dB. The WIN design is well matched in simulation at the target frequency, but in measurement $|S_{11}|$ is shifted up in frequency and $|S_{22}|$ is shifted down about 2 GHz, causing unwanted reflections. The Qorvo design matching follows the simulated trend more closely, although the dip in return loss is not as pronounced. Although the peak $|S_{21}|$ are within 300 MHz for the measured and simulated traces, the measured curve is shifted slightly down in frequency.

Large signal measurements are next performed on the two amplifiers to analyze efficiency and output power. To perform these measurements, a Ka-band signal is generated with an HP 83650A synthesized sweeper and first amplified with a Ka-band driver. The input signal is coupled off and measured with a

Keysight 8487A power sensor. The output signal is also measured in this manner after some attenuation. A calibration is first performed with the power meters to measure the loss through passive elements.

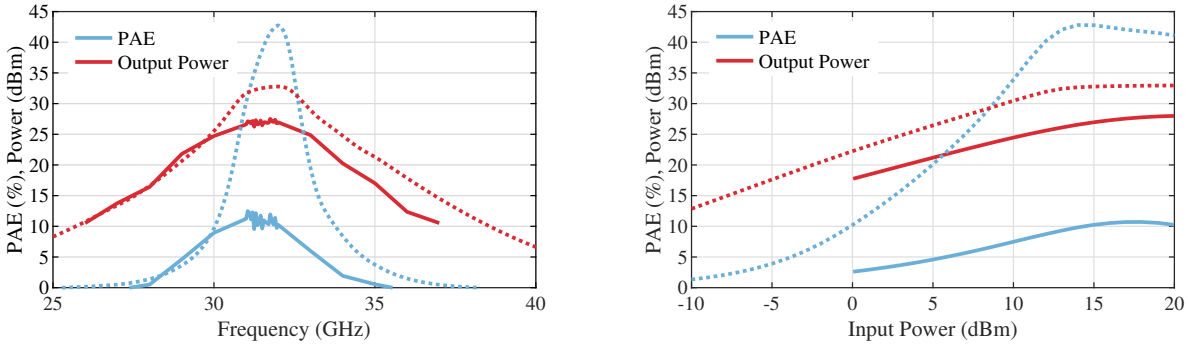


Figure 3.10: Simulated (dashed) and measured (solid) PAE and output power of WIN 32 GHz harmonically terminated amplifier. (a) Parameters plotted vs. frequency with $P_{in} = 15$ dBm. (b) Parameters plotted vs input power at 32 GHz.

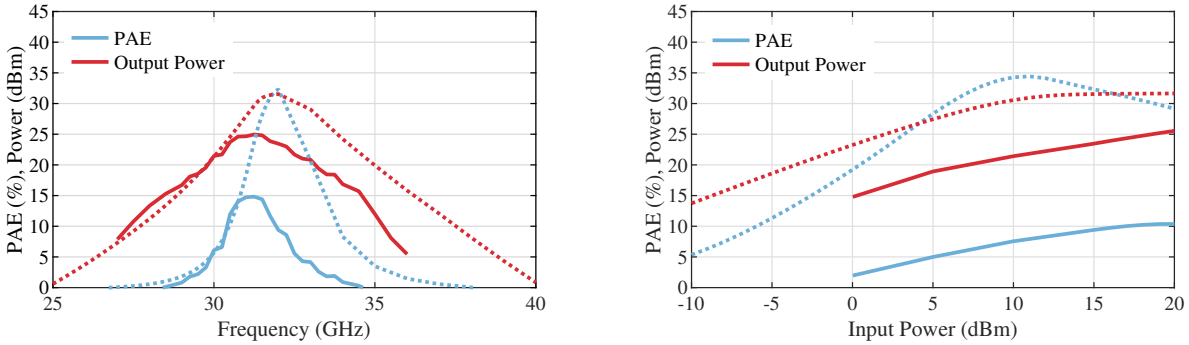


Figure 3.11: Simulated (dashed) and measured (solid) PAE and output power of Qorvo 32 GHz harmonically terminated amplifier. (a) Parameters plotted vs. frequency with $P_{in} = 15$ dBm. (b) Parameters plotted vs input power at 32 GHz.

The large signal characterization is first displayed for the WIN PA in Fig. 3.10. Output power and PAE are plotted against frequency with a 15 dBm input in Fig. 3.10a. Simulated results display a very high efficiency of 42.8% at 32 GHz with an output power exceeding 2 W. Measured results are significantly

lower in both metrics, with PAE reaching a maximum of 12.5% and output power at 27.5 dBm with this input power. The drive-up curves in Fig. 3.10b show a similar trend. However, PAE peaks at 14 dBm input for the simulated PA while measured PAE peaks at 18 dBm input.

These measurements are next performed on the Qorvo PA using the same setup. Simulated and measured large signal results are displayed in Fig. 3.11. With a 15 dBm input power, the simulated PA demonstrates a PAE and output power of 32.3% and 31.5 dBm at 32 GHz respectively. The measured performance is much lower, consistent with the WIN design, and is shifted down in frequency compared to simulation, with the maximum PAE and output power of 14.8% and 25.0 dBm occurring 750 MHz lower. Drive-up curves are consistent with the plots vs frequency.

3.1.4 Discussion

The second harmonic termination applied to this power amplifier topology boosted efficiency in simulation, but this technique unfortunately did not translate to measurement for these two processes. Neither design kit is rated for operation above 40 GHz, which could indicate why this technique was not successful. The second harmonic at 64 GHz may not generate enough power to justify the use of a separate termination network, which inadvertently adds loss to the fundamental signal. Furthermore, phase of the second harmonic may not be predicted properly by simulation. Repeating this design with a design kit rated for higher frequencies, e.g. a 90 nm gate process, may result in improved performance of this technique compared to matching only with fundamental load pull results. The operating frequency of the amplifiers in subsequent sections are backed down to 27-31 GHz where process models may be better fitted to measurements.

3.2 FEP Model

The Foundational Engineering Problem (FEP) model framework developed by Modelithics and Qorvo adds advanced capabilities to GaN MMIC design with its physics-based PDK. These capabilities feature foundry scaling, distributed thermal modeling, reliability modules, and layout modules [82]. The foundry scaling parameters displayed in Fig. 3.12 include seven geometry parameters and one material parameter. They include aluminum content (Alx), gate/channel length (L6), barrier thickness (L5B), trunk nitride thick-

ness (L7), gate-source spacing (L8A), gate-drain spacing (L8B), GFP-drain side (L2B), and SFP-drain side (L10B).

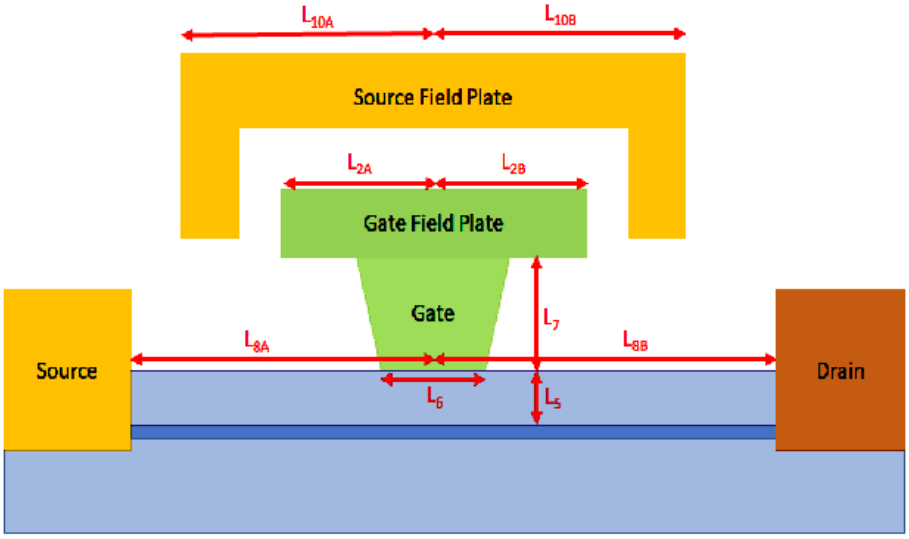


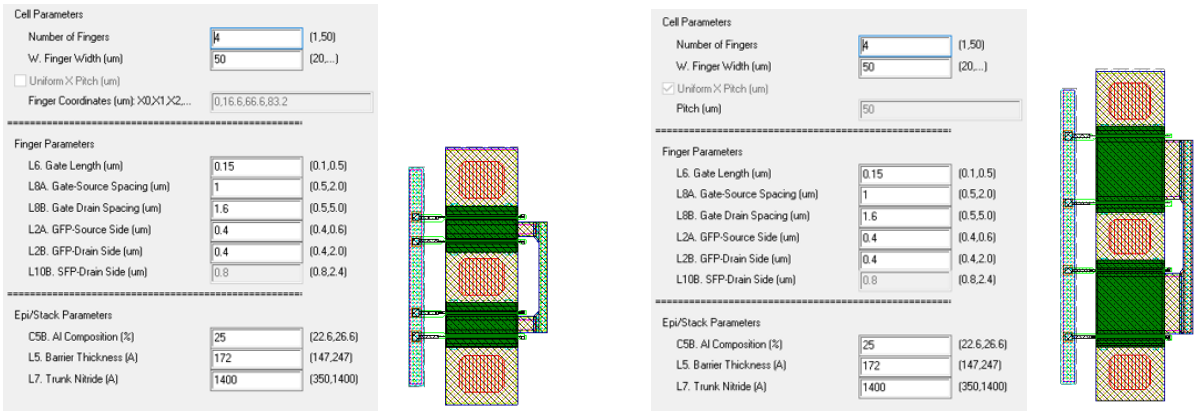
Figure 3.12: Tunable cell parameters of FEP model

The advanced distributed thermal model allows for temperature tracking at the finger level, including coupling. Similarly, the electrical model allows for I/V characterization at the finger level. The degradation module allows the user to monitor long-term stress effects, although it is not fitted to the Qorvo PDK in the version used for this design. However, reliability is assessed with the advanced thermal model and Qorvo's standard published reliability curves.

3.3 Single Stage Test Amplifiers

3.3.1 Test Amplifier Design

Three single-stage amplifiers are designed to test the validity of the FEP model at Ka-band. For each amplifier, a $4\times50\,\mu$m HEMT is employed with different finger pitches. All other parameters are left unchanged to limit the variables under test. The three transistors contain individual source vias (ISV). The first amplifier is designed using a QGan15 device with 15 μm spacing between fingers without source vias and 52 μm spacing between fingers with source vias. This standard foundry device is the only nonlinear



(a) (b) (c) (d)

Figure 3.13: (a) Cell parameters and (b) layout of first FEP device. (c) Cell parameters and (d) layout of second FEP device.

$4\times50\,\mu$m HEMT available in the PDK and its finger spacing is fixed. The second amplifier includes a HEMT of the same dimensions but is matched to the FEP model impedance. The cell parameters used to generate this device along with its layout are displayed in Figs. 3.13a and 3.13b respectively. The HEMT layout used for amplifier 1 is the same as in Fig. 3.13b with slight differences in the manifold. The third amplifier features the HEMT whose parameters and layout are displayed in Figures 3.13c and 3.13d, respectively. The pitch between all four fingers is adjusted to $50\,\mu$m. Although it has a uniform gate spacing, this device is non-standard and could not be replicated in the QGaN15 PDK for comparison.

Load pull simulations are performed on the three devices at 24–30 GHz. For each device, a 28 V drain voltage is applied with a 100 mA/mm drain current. The source is conjugate matched and input power is swept from 6–23 dBm. A comparison of the three load pulls is displayed in Fig. 3.14 at 26 GHz with an 18 dBm input power. Gain circles are plotted in red in 1 dB steps with 6 dB as the outermost circle, while PAE circles are plotted in blue in 5% steps with 15% as the outermost circle. As previously stated, the HEMTs with load pull shown in Fig. 3.14(a) and (b) are identical, with (a) displaying the foundry model simulation and (b) displaying the FEP model simulation. Fig. 3.14(c) displays load pull for the FEP model with a wider, uniform finger spacing.

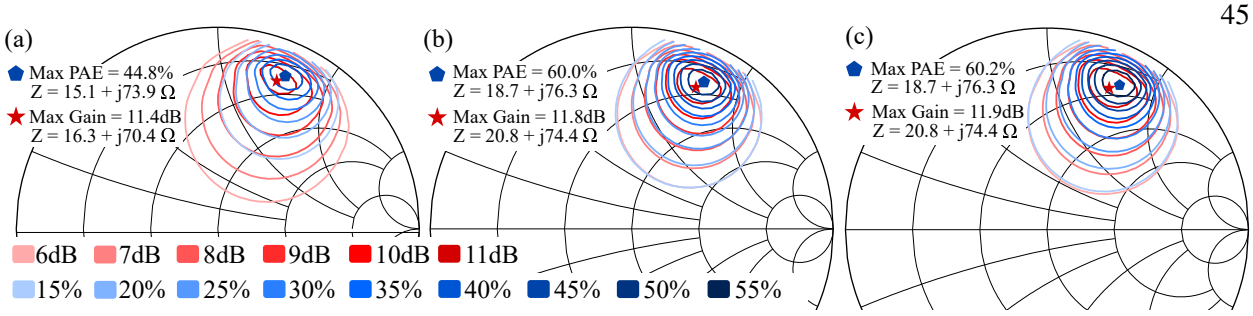


Figure 3.14: Simulated load pull contours of (a) foundry device used in first test amplifier, (b) FEP model device used in second test amplifier, and (c) FEP model device used in third test amplifier. All contours are generated at 26 GHz with 28 V drain bias, 100 mA/mm drain current, and 18 dBm input power.

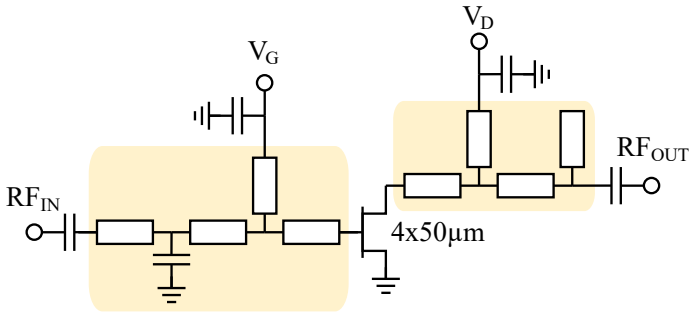


Figure 3.15: Simplified schematic of single stage amplifier designed for FEP models. Highlighted elements are tuned to match to each of the three $4\times50\,\mu$m device models.

The gain contours of the foundry device are more expansive as compared to the FEP contours, while the opposite is true for PAE contours. The maximum gain and PAE for the two FEP models are almost identical, differing only 0.1 dB and 0.2%, respectively. Conversely, the foundry model has a maximum gain approximately 0.5 dB lower, and a maximum PAE more than 15% lower in comparison. The impedance of the maximum points also differ slightly compared to those of the two FEP models which are identical.

The general schematic adapted for the three device models is displayed in Fig. 3.15. Each amplifier is constructed with the $4\times50\,\mu$m device in a common source configuration. Biasing is performed through microstrip lines with shunt bypass capacitors at the dc connection. The input and output matching networks, composed of transmission lines and lumped capacitors, are highlighted in yellow in Fig. 3.15. These elements are tuned to match to the maximum PAE impedances from Fig. 3.14 for each of the three devices.

A photograph of the die which includes the three test amplifiers is displayed in Fig. 3.16. The ports

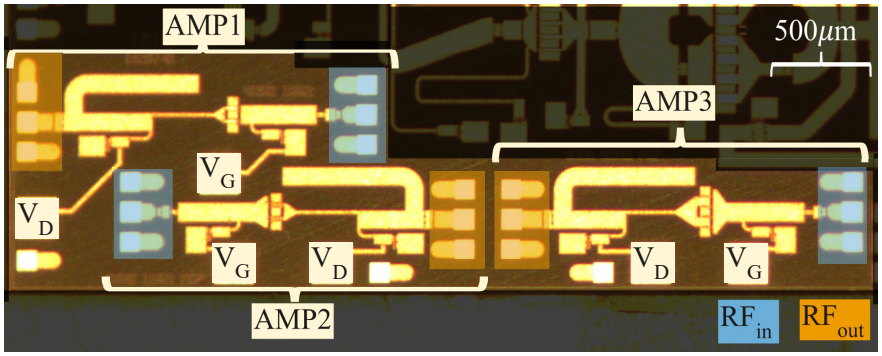


Figure 3.16: Photograph of three-single stage 26 GHZ amplifiers fabricated in QGaN15 on 4 mil.

and pads of the three amplifiers are labeled. The die is mounted on a gold-plated copper molybdenum (CuMo) carrier. The dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for stability and ease of probing.

3.3.2 Test Amplifier Measurements

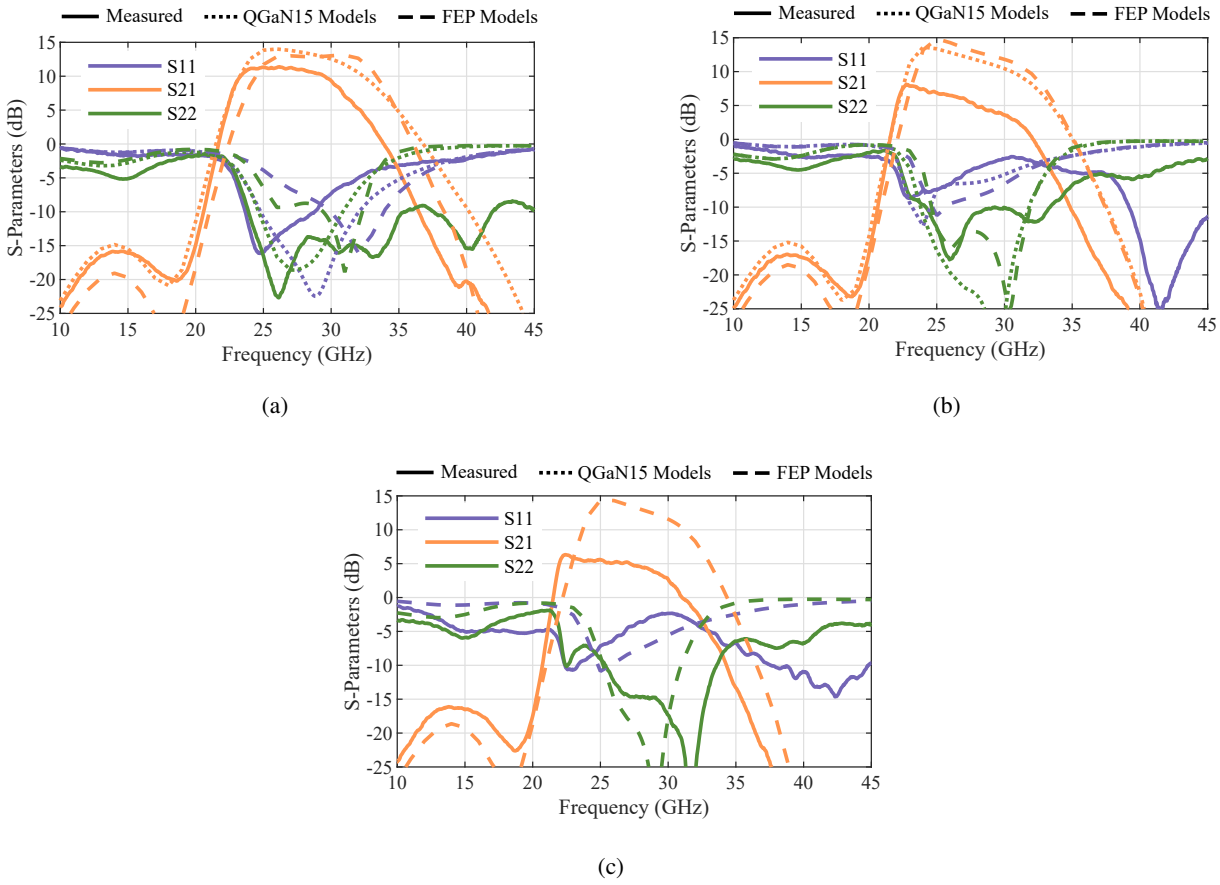


Figure 3.17: Measured and simulated small signal S-parameters of (a) amplifier 1, (b) amplifier 2, and (c) amplifier 3.

Small signal characterization of the three amplifiers is performed with an Agilent E8364C PNA Network Analyzer calibrated with an SOLT impedance standard substrate. The S-parameters for amplifiers 1, 2, and 3 are captured and displayed in Fig. 3.17(a), (b), and (c) respectively. Each plot displays measured results in solid lines, foundry model simulations in dotted lines, and FEP models simulations in dashed lines. In comparing the performance of the three circuits, amplifier 1 has the highest measured gain, about 3 and 5 dB higher than amplifiers 2 and 3, respectively, although it has the lowest simulated gain with both models. Return loss is also the lowest for amplifier 1 designed with the foundry model. Interestingly, all

three amplifiers have lower measured gain than both simulated models above 23 GHz by several dB, but follow the foundry model simulations closely below this frequency. The FEP model simulations are also shifted up in frequency, almost 1 GHz across the board.

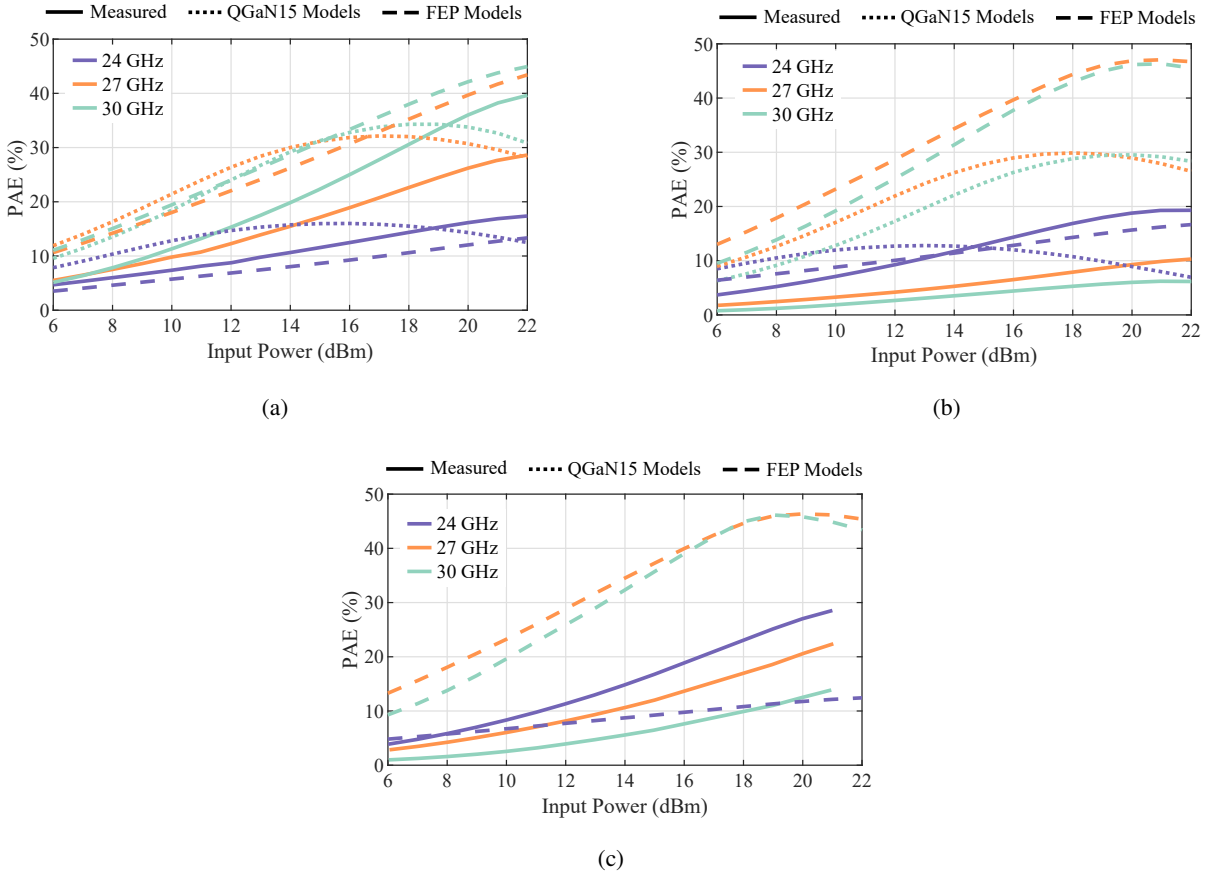


Figure 3.18: Measured and simulated power added efficiency vs. input power of (a) amplifier 1, (b) amplifier 2, and (c) amplifier 3.

Large signal measurements are next performed on the three amplifiers to analyze efficiency and output power delivery. To perform these measurements, a Ka-band signal is generated with an HP 83650A synthesized sweeper and first amplified with a Ka-band driver. The input signal is coupled off and measured with a Keysight 8487A power sensor. The output signal is also measured in this manner after some attenuation. A calibration is first performed with the power meters to measure the loss through passive elements.

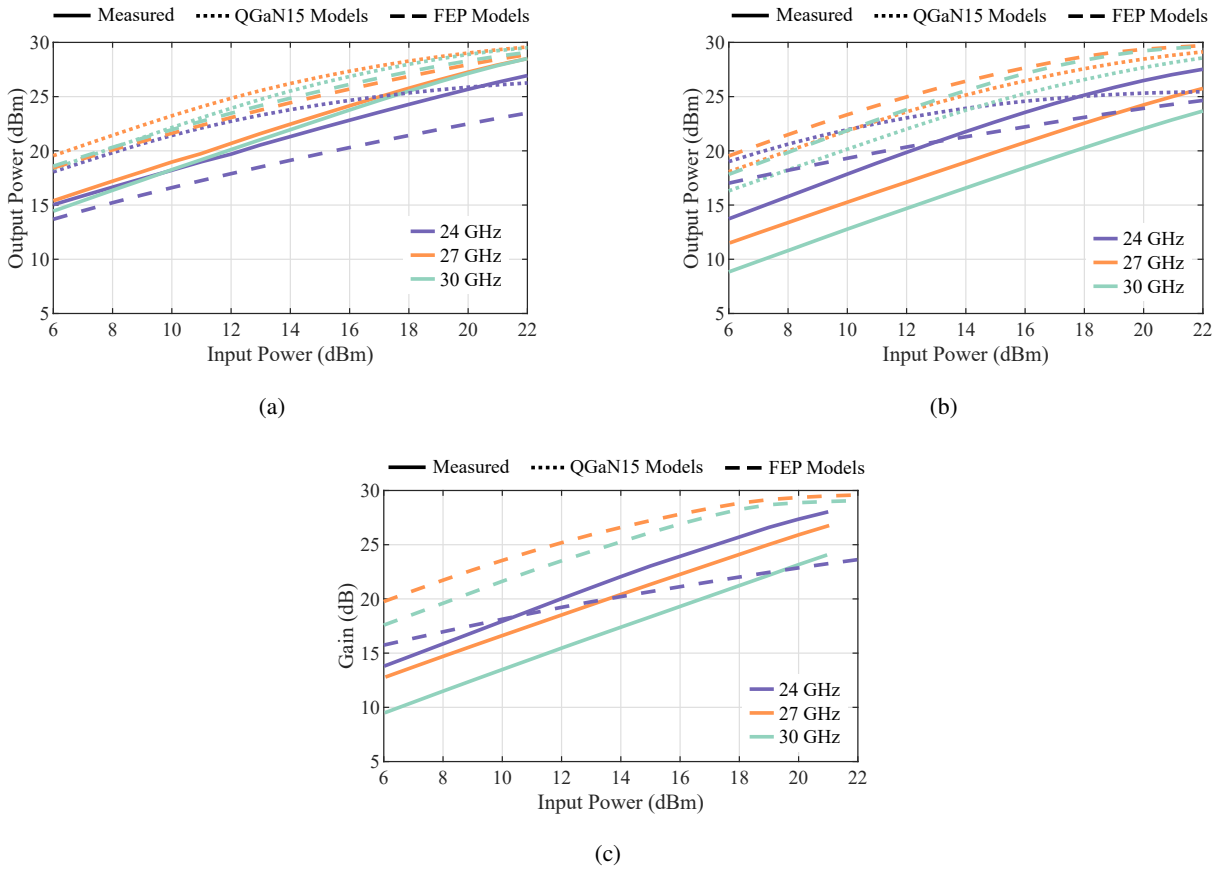


Figure 3.19: Measured and simulated output power vs. input power of (a) amplifier 1, (b) amplifier 2, and (c) amplifier 3.

Power added efficiency and output power are plotted vs. input power in Figs. 3.18 and 3.19, respectively, at 24, 27, and 30 GHz. Measured results are displayed in solid lines, foundry models in dotted lines, and FEP models in dashed lines. For amplifier 1 in Fig. 3.18a, the peak measured PAE is 39.6% at 30 GHz with 22 dBm input power. This is higher than the simulated 34.3% at 18 dBm input with the foundry models but lower than the 45.4% with FEP models at 23 dBm input. Efficiency is much lower at the other frequencies however, indicating that it is more limited in bandwidth. Amplifier 2 operates with much lower efficiency as displayed in Fig. 3.18b. It is also shifted down in frequency, with the maximum PAE measured at 24 GHz. Amplifier 3 performed similarly to amplifier 2 but with slightly higher efficiency. In all three cases, the FEP model significantly overestimates efficiency. However, it more accurate in predicting the input power level at which saturation occurs.

Amplifier 1 delivers the highest saturated output power in Fig. 3.19a as compared to amplifiers 2 and 3. This is expected on account of its higher gain measured in small signal. The expected output power matches more closely, within 1 dBm, at most frequencies between the two models.

3.3.3 Discussion

Three single-stage amplifiers have been designed to test the robustness of the FEP model with finger pitch scaling and comparison to foundry models. In both small and large signal, the FEP model appears over-optimistic in terms of gain and efficiency, as is evident from S-parameters and large signal characterization. A shift in the target impedance from load pull compared to foundry models is the suspected reason for the shift in frequency in measurement.

3.4 Dual mode power combined Ka-Band PA Design

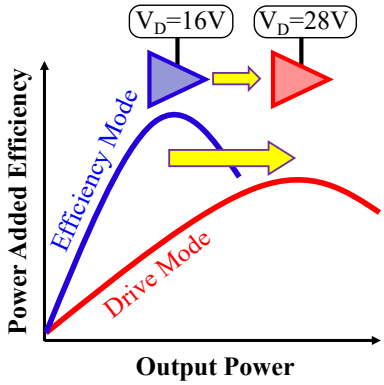


Figure 3.20: Plot of PAE vs. output power for static dual mode amplification concept. Amplifier operates in two modes: efficiency mode with 16 V drain voltage, and drive mode with 28 V drain voltage.

A larger power amplifier is designed into the same process as the three test amplifiers. Given the limited availability of validated FEP models, the amplifier is designed with foundry models and compared to simulations with the FEP device as in amplifier 1 from Section 3.3.1. Specifications for frequency, efficiency, and output power are given for a limited input drive. The amplifier is to operate from 27–31 GHz with input power not exceeding 20 dBm. The amplifier must operate in two modes. First, a high efficiency mode with a power added efficiency greater than 30% and at least 4 W output power. To achieve these

specifications, a drain voltage below the nominal value is used, as illustrated by the blue curve in Fig. 3.20 with $V_D = 16V$. Second, the drain supply is increased to the nominal voltage or above to achieve a target output power of 12 W while still maximizing PAE. This is illustrated by the red curve in Fig. 3.20 with $V_D = 28V$.

3.4.1 Power Amplifier Design

To reach the maximum output power of 12 W (40.8 dBm) with a maximum input drive of 20 dBm, a gain of at least 20.8 dB is required in large signal. A similar design process as discussed in Chapter 3 is applied for this circuit, starting with load pull simulations to determine the final stage device size. A load pull analysis is performed on five nonlinear HEMT models available in the PDK. They include a $4 \times 50\,\mu$m device, an $8 \times 50\,\mu$m device, and three $8 \times 100\,\mu$m devices with increasing standard finger pitches. Simulations of an $8 \times 100\,\mu$m device with the second of three increasing finger pitches at 29 GHz present a maximum output power of 36.6 dBm and a power added efficiency of 34.0% when the HEMT is biased in class AB with $V_D = 28$ V and $P_{in} = 31$ dBm. Combining four of these devices at the simulated bias point boosts the output power by 6 dB in an ideal circuit. For a realistic design, approximately 1 dB of loss will result from the output matching network and combiner, degrading the output power by the same amount and the PAE by at least 5%. With these approximations in mind, four $8 \times 100\,\mu$m devices can be combined to produce the desired specifications in drive mode. The efficiency mode specifications are met with the drain supply and input power reduced to 16 V and 24 dBm respectively. The PAE and output power for a single device are 43.9% and 31.2 dBm under these conditions.

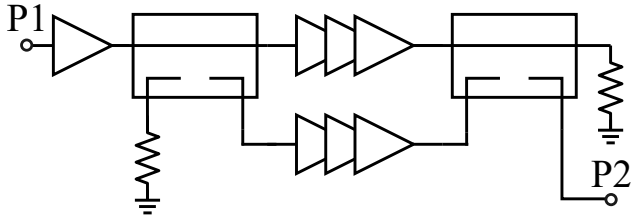


Figure 3.21: Block diagram of power amplifier used for both designs. One drive stage feeds a three-stage balanced configuration.

The output power and efficiency characteristics from load pull occur at approximately 4 dB and 2 dB

gain compression of the output stage transistor for drive and efficiency mode, respectively. A four stage power amplifier is designed to deliver the appropriate amount of gain at a maximum 20 dBm input power. A block diagram of the amplifier is displayed in Fig. 3.21. A single drive stage is followed by a three stage balanced topology. The balanced amplifier provides twice the periphery and good matching over the frequency range. Using the simulated load pull results and working backwards from the output stage, a 1:2:8:16 ratio is selected as the total periphery of each stage to achieve the desired efficiency and output power characteristics.

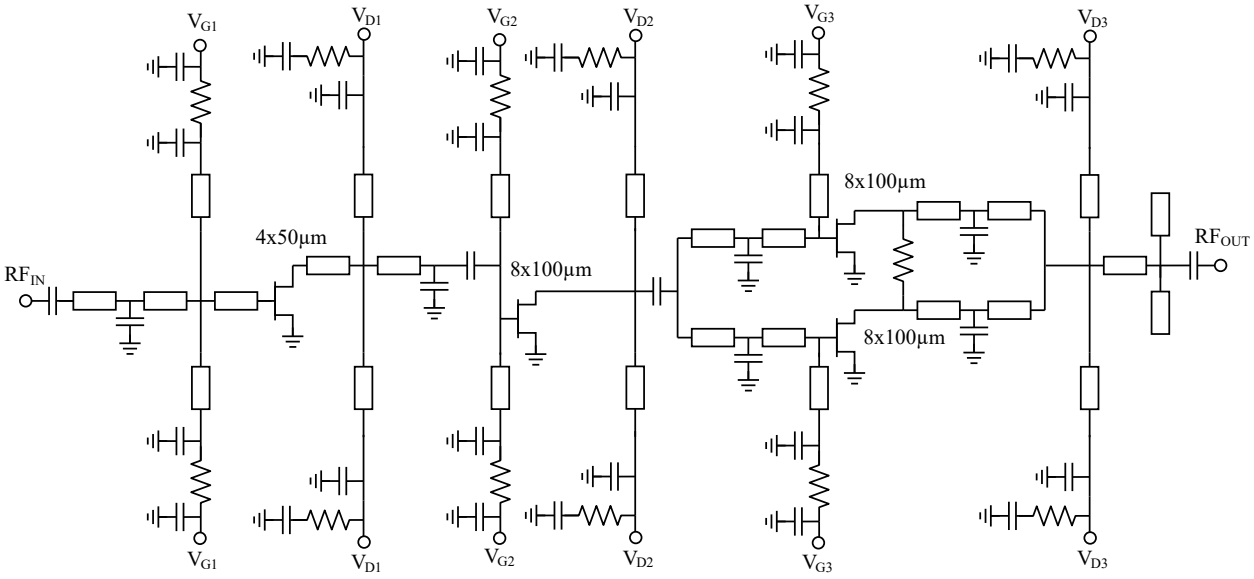


Figure 3.22: Schematic of single-ended unit amplifier.

The balanced portion of the power amplifier contains two unit amplifiers. A schematic of one single-ended three stage amplifier is displayed in Fig. 3.22. The first stage uses one $4 \times 50\,\mu$m device, the second stage uses one $8 \times 100\,\mu$m device with the smallest finger pitch, and the third stage employs two $8 \times 100\,\mu$m devices with a wider finger pitch for improved thermal dissipation. Matching is achieved with microstrip lines and lumped capacitors. The QGaN15 process features shunt capacitors directly over vias, reducing parasitic losses and increasing the quality factor of these elements and their corresponding matching networks. The bias lines are designed into the matching network using the microstrip matching techniques discussed in Chapter 2. Stability networks are included in the bias lines with capacitor ladders and series

resistance in the gate lines, as well as an odd mode resistor in the output power combined stage.

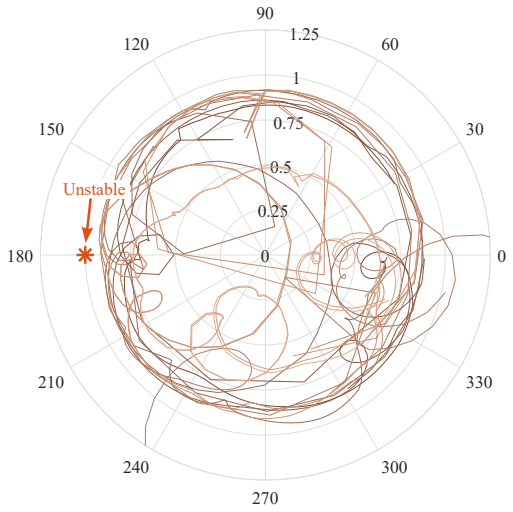


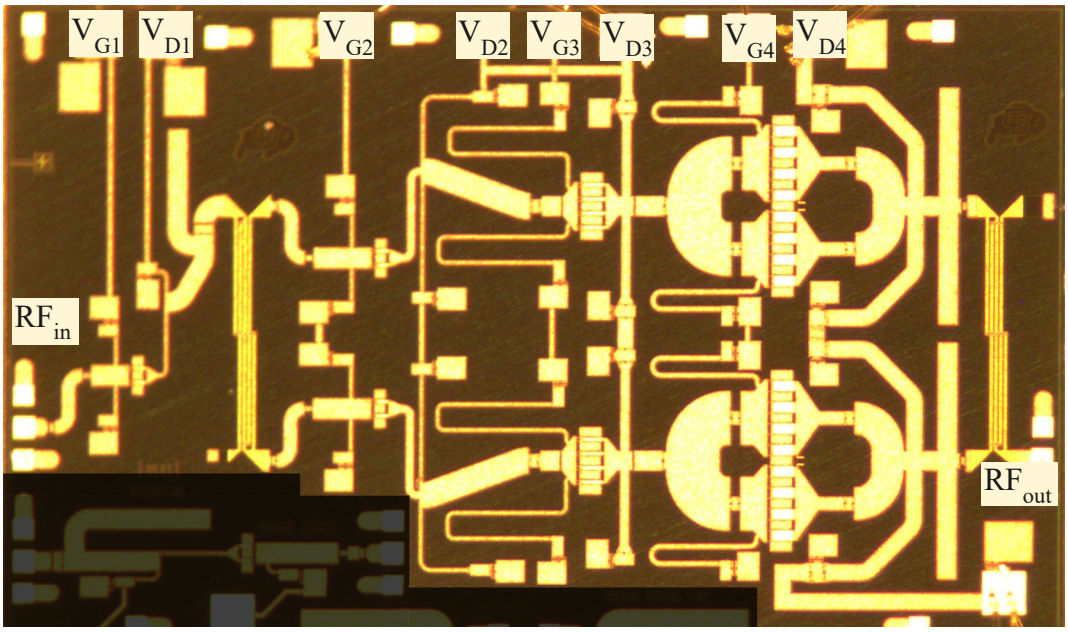
Figure 3.23: Nyquist plot of single-ended power amplifier under drive bias conditions.

A simulated Nyquist stability plot of the unit amplifier is displayed in Fig. 3.23. This simulation displays curves with a 29 GHz input source, analyzing amplifier stability due to feedback from 100 MHz to 100 GHz. Probes are placed at the gate and drain of each HEMT to generate these curves. The simulation is repeated at a number of input frequencies and source/load/bias impedances to ensure stability over all possible test conditions.

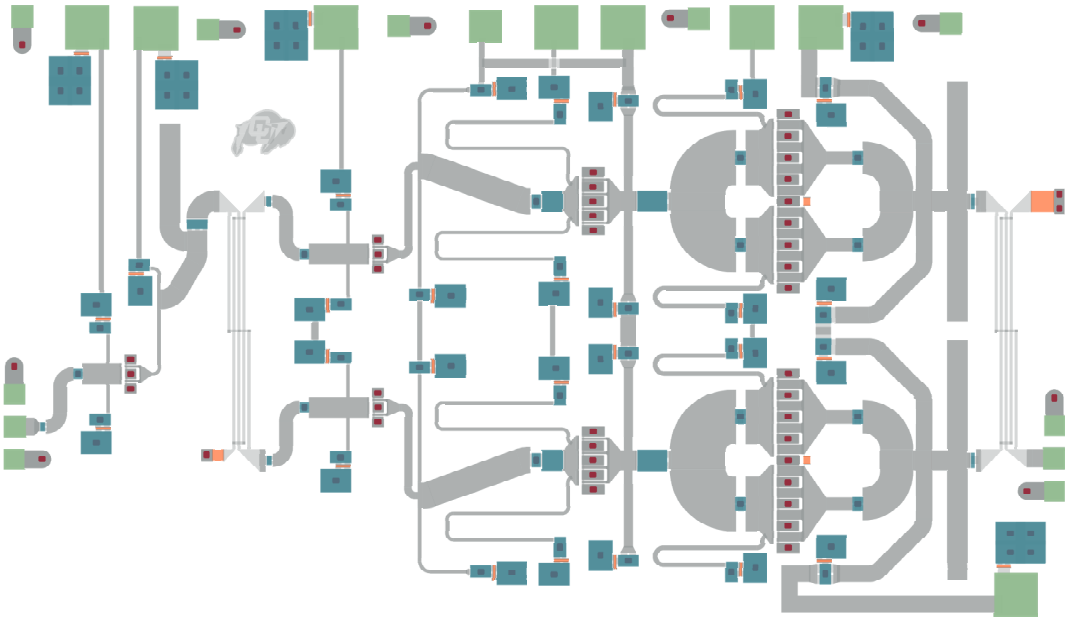
A complete layout and picture of the die are displayed in Fig. 3.24. Symmetry in the layout of the unit amplifier allows for easy dc connectivity to the top and bottom branches, and is biased from one side only. The second and third stage drains are dc connected on chip, while the other stages are tied using bond wires off chip. However, the output power combined stage is biased from both sides due to the large current draw and limited electromigration characteristics of airbridges connecting to the shunt capacitors. The first stage driver is designed independently to match to 50 Ω at the input and output to match to the Lange Coupler.

3.4.2 Power Amplifier Measurements

The power amplifier is displayed in Fig. 3.24. The die is mounted onto a CuMo carrier and bonded to off-chip capacitors. The MMIC is probed on a Summit 9000 probe station with 150-μm pitch probes from 15-40 GHz. An E8364C PNA Network Analyzer is used to capture small signal S-parameters.



(a)



(b)

Figure 3.24: (a) Photograph and (b) layout picture of four-stage Ka-band Amplifier, 5 mm $\times$ 2.8 mm.

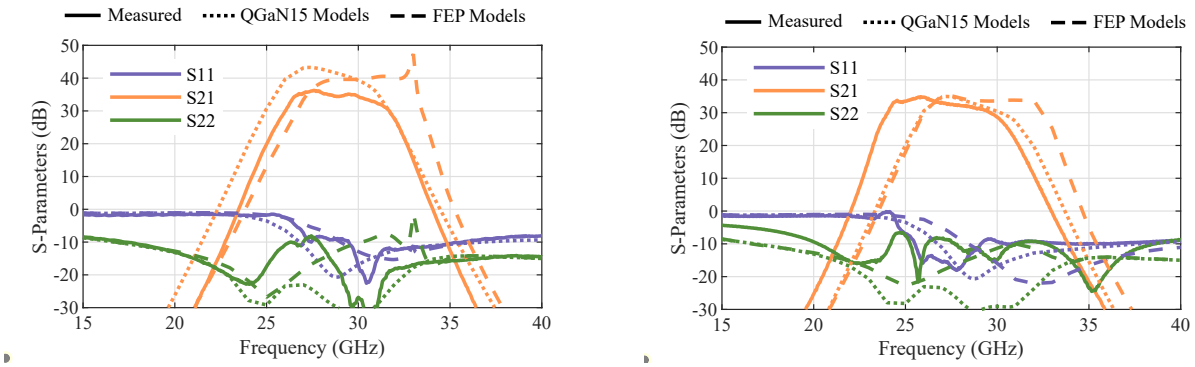


Figure 3.25: S-parameters of Design Challenge III PA in (a) drive mode with Vd = 28 V and (b) efficiency mode with Vd = 16 V.

S-parameters of the power amplifier in drive mode and efficiency mode are displayed in Fig. 3.25. Measured results are plotted with solid lines, foundry model simulations with dotted lines, and FEP model simulations with dashed lines. Drive mode in Fig. 3.25a is performed with a drain voltage of 28 V. A maximum $|S_{21}|$ of 36.3 dB is measured at 27.6 GHz with a 3 dB bandwidth from 26.4–30.6 GHz. Simulations with foundry models display a higher gain of 42.3 at 27.3 GHz and a 3 dB bandwidth of 26.5–29.5 GHz. The frequency response of S-parameter simulations using foundry models match with measurements well in simulation, while the gain is exceedingly high by up to 6 dB. This is consistent with the single-stage test amplifier measurements in Section 3.3.1. Meanwhile, simulations using the FEP model are shifted up in frequency, with $|S_{21}| > 39$ dB from 28.2–33.2 GHz. In efficiency mode with Vd=16 V, measured gain is slightly reduced by approximately 1.4 dB, while the 3 dB bandwidth is significantly shifted down in frequency by about 2 GHz. Both foundry and FEP models also display an $|S_{21}|$ around the same magnitude as measured, although the reduction in gain from drive mode is much greater. Simulations also do not predict the frequency shift observed in measurement.

Large signal measurements are next performed on the amplifiers using the same setup from Section 3.3.2. Power added efficiency and output power are plotted vs frequency with an input drive of 18 dBm in drive mode in Fig. 3.26a. A maximum output power of 35.9 dBm is measured at 28.5 GHz, about 4.2 dB lower than foundry simulations. This is likely due to the reduction in measured gain. Simulations with FEP

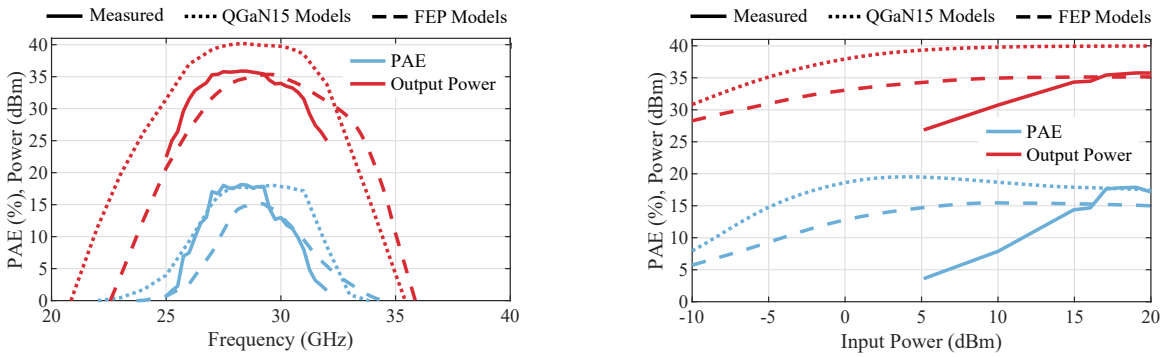


Figure 3.26: Measured and simulated large signal sweep of PA in drive mode with Vd = 28 V (a) vs. frequency at 18 dBm input drive and (b) vs. input power at 29 GHz.

models on the other hand display a much similar output power with an upward shift in frequency response by approximately 1 GHz, consistent with small signal measurements. Efficiency curves match up well between measurements and foundry models with less than 1% difference from 26.3–29.3 GHz, although the dropoff occurs at a lower frequency in measurement. The drive-up curves at 29 GHz in Fig. 3.26b, also indicate that the peak efficiency and compression occur at a significantly lower drive, by 14 dB for foundry models and 10 dB for FEP models.

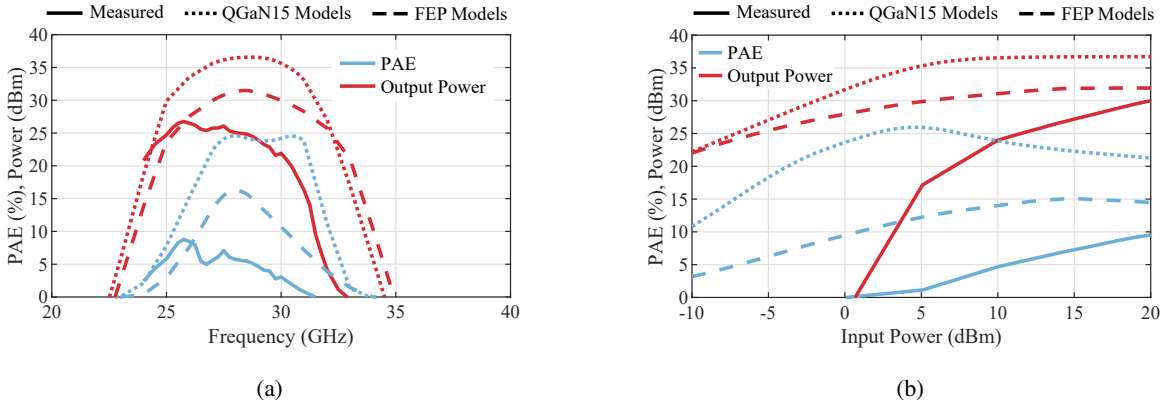


Figure 3.27: Measured and simulated large signal sweep of PA in drive mode with Vd = 16 V (a) vs. frequency at 10 dBm input drive and (b) vs. input power at 29 GHz.

In efficiency mode in Fig. 3.27, simulations indicate a boost in PAE by about 5% with foundry models,

while peak output power drops by only 3 dB. Unfortunately this trend was not observed in measurements, where measured PAE dropped 10% from its peak in drive mode. Output power is also 4 dB lower. The discrepancy between measurement and simulation is attributed to the lack of device modeling at this lower bias voltage where the device impedance differs, consistent with the downward shift measured in small signal.

3.5 Conclusion

This chapter describes the design of several Ka-band amplifiers. The first section uses foundry models to design two harmonically terminated power amplifiers. The second and third section compare measurements to both foundry and FEP model simulations. In every case, gain and efficiency are overestimated by simulation. Although these amplifiers do not reach all of their target specifications, the information presented in this chapter provides useful feedback to both the foundries and designers. The first set of amplifiers from Section 3.1 were designed very close to the f_T of the process where the device characteristics may be extrapolated from measurements at lower frequencies, particularly at the second harmonic. To improve this design, a more advanced process node could be used with a higher f_T. Alternatively, the design could be repeated in the same process at a lower frequency. With little to no gain produced at the second harmonic (64 GHz), the designated matching network most likely adds loss and reduces efficiency rather than boosts it. The bias lines were also designed as quarter-wave lines in the first stage to present a high impedance due to the narrowband nature of this circuit, as discussed in Chapter 2. An analysis comparing the measured S-parameters of the individual matching networks and harmonic terminations with electromagnetically simulated results could provide more clarity on their impact to overall circuit performance. Such a study could be performed as future work by breaking out several passive networks or performing iterations on the amplifier for comparison.

The four-stage power amplifier from Section 3.4 was designed for two different bias voltages. This presented an added challenge, especially without specific information on what bias conditions the models are validated at. In simulation, the amplifier was able to meet most desired specifications within the frequency range, aside from PAE in efficiency mode, which was about 5% lower than the target efficiency.

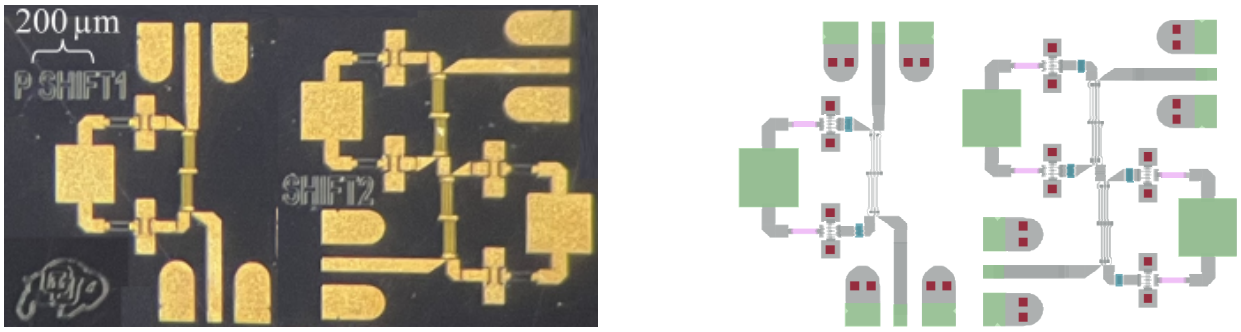
Unfortunately, the drain voltage used in efficiency mode is not validated in the transistor models, as is evident in small signal with an unexpected frequency shift and large signal with very low measured efficiency. This design could be improved by tuning the matching networks to operate only at the bias conditions under which the active models are validated. Additonally, the FEP model may provide future opportunities to improve amplifier performance. While the FEP models include tuning knobs for device geometry and material parameters to optimize MMIC design, additional modeling is needed to ensure its maturation and usefulness.

Chapter 4

50-110 GHz Continuous Reflective Phase Shifters

Monolithically integrated transceivers often require analog control circuits for various applications. The front end MMIC in Fig. 1.4 contains a "Control" block to represent one of these circuits. In this chapter, the focus shifts from amplifiers to control circuits by discussing wideband millimeter-wave phase shifters. Phased array antennas commonly use phase shifters in feed networks for beam forming and steering [83]. They are also necessary for instrumentation applications, such as in frequency translators and reflectometers [84–86]. At higher millimeter-wave frequencies, loss and availability of devices presents a challenge for achieving a large phase shift across a wide bandwidth. In this chapter, continuous GaN MMIC phase shifters that cover the entire 50–110 GHz V- and W-bands are presented. A photograph of the circuits are shown in Fig. 4.1a, along with a rendering of the layout in Fig. 4.1b. Additionally, compression of the phase shifters is measured to assess linearity. The continuous phase shifter circuit is a reflective topology with broadband hybrids and gate-bias controlled diode-connected HEMTs as variable reactances. A theoretical expression for the reflection and transmission coefficients shows how the transmission phase is related to the variable reactance. When two 90° phase shifters are cascaded to form a 180° phase shifter, lower overall insertion loss can be obtained by proper choice of control voltages.

One of the motivations for implementing GaN shifters is integration with other components that have demonstrated superior performance compared to other semiconductor technologies, such as power amplifiers with watt-level outputs at W-band [28], LNAs and switches with high IP3 [30, 39], quasi-circulators for full-duplex operation [87], etc. Another application for these phase shifters is broadband analog linearization of power amplifiers, shown at low frequencies in e.g. [88, 89]. At W-band, it is difficult to get



(a) (b)

Figure 4.1: (a) Photograph of single-stage 90° reflective phase shifter (left) and two-stage 180° reflective phase shifter. (b) Layout of single-stage 90° reflective phase shifter (left) and two-stage 180° reflective phase shifter.

high power and reasonable efficiency from PAs [29] without saturating them, so linearization is important. Further, the high absolute bandwidth for a modest fractional bandwidth at millimeter-wave carrier frequencies allows amplification of wideband signals, which makes digital pre-distortion (DPD) difficult and new analog linearization techniques are of interest [90]. Therefore, continuous phase shifters that handle higher power levels can be useful.

Phase shifter circuit architectures demonstrated at W-band include digitally switched-delay lines, reactively-loaded lines, and reflective phase shifters [91]. They can be implemented using MEMS [92–95], liquid crystals [96], and various integrated semiconductor technologies. Examples in CMOS include [97–102], and while these are highly integrated and compact circuits, they suffer from loss due to the substrate, low power handling, and nonlinearity. GaAs phase shifters have also been demonstrated at W-band, e.g. [103, 104]. In transmit phased arrays where higher power levels are required, GaN phase shifters have shown better linearity than GaAs across X-band [105]. At W-band, GaN phase shifters are demonstrated in [38] from 78–89 GHz with 2 bits giving 4 phase states from 22.5° to 67.5° and with 2.9 dB minimum insertion loss. Single-bit 90° and 180° cells are also demonstrated in [38] from 70-78 GHz with less than 10° phase error and insertion loss between 1.8 and 2.8 dB and 2.1 and 4.6 dB, respectively. In this chapter, the design and characterization of continuous reflective GaN MMIC phase shifters covering the entire V- and W-bands, from 50 to 110 GHz implemented in the HRL 40 nm GaN-on-SiC HEMT process is described.

4.1 Design of Reflective Phase Shifters

Reflective phase shifters allow continuous tuning of phase through reflections from variable reactive loads on two ports of a 90° hybrid coupler, with an ideal circuit schematic shown in Fig. 4.2a. The 3 dB coupler splits the incoming signal power evenly between the "thru" and "coupled" ports. $1/\sqrt{2}$ of the signal arrives at the "thru" port with a $-90°$ phase shift, while the remaining part at the coupled port is shifted by $-180°$. The reactances at the "thru" and "coupled" ports reflect the signal with a tunable phase shift. The two signals then combine constructively at the isolated port with a $-270°$ shift added to the tunable phase. The reflected signals cancel at the input.

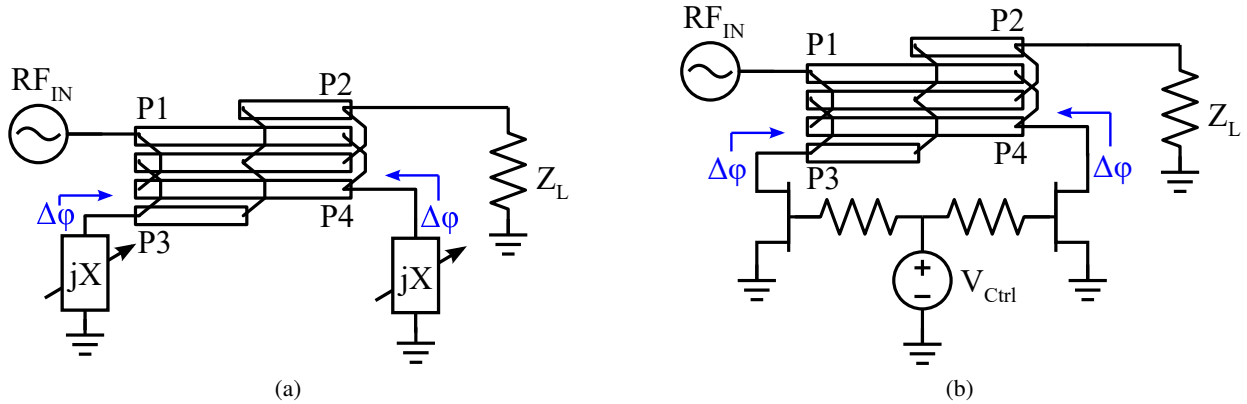


Figure 4.2: (a) Schematic of an ideal reflective 90° phase shifter with lossless identical tunable loads jX connected at ports 3 and 4, controlled simultaneously. (b) Schematic of broadband 90° reflective phase shifter implemented with a Lange coupler and gate-bias controlled HEMT loads.

A block diagram of this four port system with reflections Γ_3 and Γ_4 at ports 3 and 4, respectively, is displayed in Fig. 4.3. This is translated to signal flow graphs to calculate the reflection coefficient, $\rho = b_1/a_1$, in Fig. 4.4a, and transmission coefficient, $\tau = b_2/a_1$, in Fig. 4.4b of the four port system. The 4-port coupler is analyzed under the conditions of matched terminations at ports 1 and 2, and perfectly reflective tunable loads at ports 3 and 4. In Fig. 4.4a, the four forward path gains from a_1 to b_1 are:

$$G_1 = S_{11} \tag{1}$$

$$G_2 = S_{31}\Gamma_3 S_{43}\Gamma_4 S_{14} \tag{2}$$

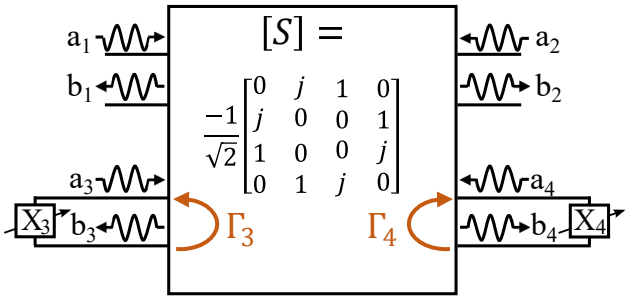


Figure 4.3: Block diagram of a two-port network with ideal lossless reactive loads at ports 3 and 4 of an ideal Lange coupler.

$$G_3 = S_{31}\Gamma_3 S_{13} \tag{3}$$

$$G_4 = S_{41}\Gamma_4 S_{14} \tag{4}$$

Three loops are also observed in this signal flow graph with loop gains equal to:

$$L_1 = S_{33}\Gamma_3 \tag{5}$$

$$L_2 = S_{44}\Gamma_4 \tag{6}$$

$$L_3 = \Gamma_3 S_{43}\Gamma_4 S_{34} \tag{7}$$

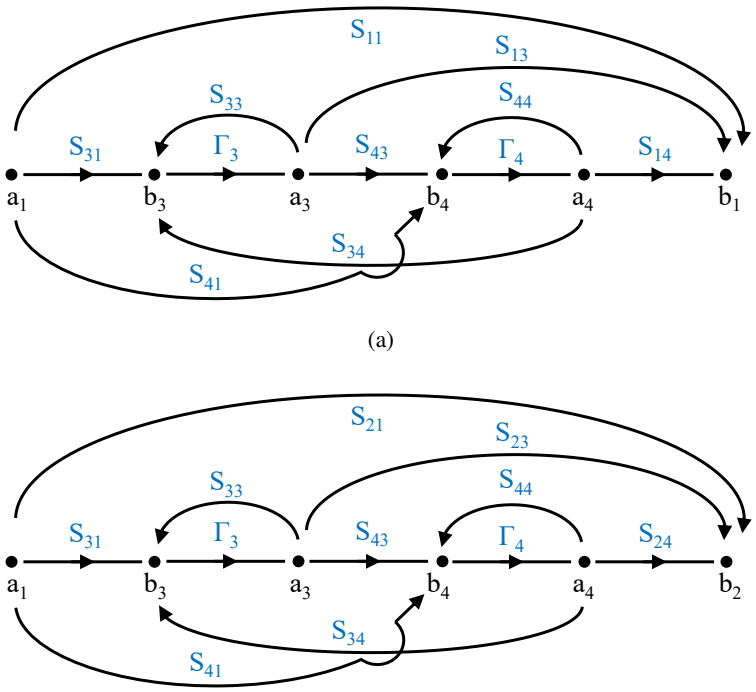


Figure 4.4: Simplified signal flow graphs for the reflective phase shifter topology for (a) reflection and (b) transmission assuming a perfectly reactive load.

For an ideal hybrid coupler, which is perfectly matched and isolated between ports 1 and 4, and ports 2 and 3, the gains G_1, G_2, G_4, L_1, and L_2 become zero. A similar analysis is performed to obtain the forward gain paths and loop gains for the transmission signal flow graph. Applying Mason's rule results in the following expressions for the reflection coefficient at port 1, and the transmission from port 1 to port 2:

$$\rho = \frac{b_1}{a_1} = \frac{\Gamma_3 S_{31} S_{13}}{1 - \Gamma_3 \Gamma_4 S_{34} S_{43}} \tag{8}$$

$$\tau = \frac{b_2}{a_1} = \frac{S_{21} - \Gamma_3 \Gamma_4 S_{21} S_{43} S_{34} + \Gamma_3 \Gamma_4 S_{31} S_{43} S_{24}}{1 - \Gamma_3 \Gamma_4 S_{43} S_{34}} \tag{9}$$

By inserting the values for an ideal Lange coupler into (8) and (9) and assuming the reflected loads are identical, $\Gamma_3 = \Gamma_4 = \Gamma$, the reflection and transmission coefficients simplify to:

$$\rho = \frac{b_1}{a_1} = \frac{\Gamma}{2+\Gamma^2} \tag{10}$$

$$\tau = \frac{b_2}{a_1} = \frac{-j\frac{2}{\sqrt{2}}(1+\Gamma^2)}{2+\Gamma^2} \tag{11}$$

With $\Gamma = x + jy$, the real and imaginary parts of the transmission coefficient (11) can be expressed as:

$$\Re\mathrm{e}(\tau) = \frac{\frac{4}{\sqrt{2}}xy}{x^4+y^4+2x^2y^2+4x^2-4y^2+4} \tag{12}$$

$$\Im\mathrm{m}(\tau) = \frac{\frac{-2}{\sqrt{2}}(x^4+y^4+2x^2y^2+3x^2-3y^2+2)}{x^4+y^4+2x^2y^2+4x^2-4y^2+4} \tag{13}$$

The transmission coefficient $\tau = \mathrm{T}\angle\phi$ acquires a phase shift $\phi(X)$, calculated from (12) and (13) as:

$$\begin{aligned}\phi(X) &= \tan^{-1}\left[\frac{\Re\mathrm{e}(\tau)}{\Im\mathrm{m}(\tau)}\right] \\ &= \tan^{-1}\left[\frac{-(x^4+y^4+2x^2y^2+3x^2-3y^2+2)}{2xy}\right]\end{aligned} \tag{14}$$

It is seen from these expressions that the signal from port 1 to port 2 receives a negative phase shift as a function of the two tunable loads, jX_3 and jX_4. The circuit is also well matched, with $|\rho|$ ranging from 0 to $1/3$.

4.1.1 Varactor HEMT Variable Load

The phase shifter design presented here is implemented in the HRL T3 40 nm GaN process on a 50 μm SiC substrate, well documented in [106]. The current T3 process achieves an $f_T/f_{\max}$ of 200/400 GHz with a breakdown voltage greater than 40 V. Three metallization layers are used to form transmission lines and airbridges, while capacitors and resistors are formed with silicon nitride (SiN) and tantalum nitride (TaN), respectively.

Tunable loads at W-band on a MMIC can be realized by connecting HEMTs as varactors, illustrated in Fig. 4.2b. In this case, the varactor reactance is controlled through the gate bias voltage of the HEMT.

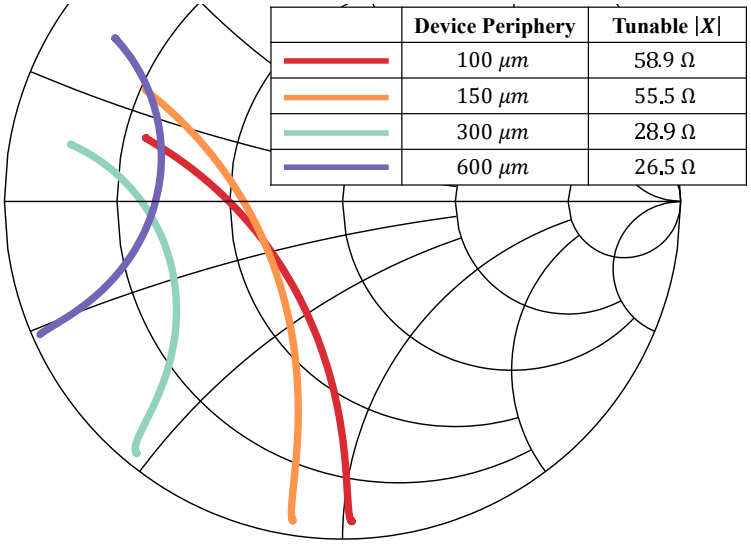


Figure 4.5: Impedance range at 75 GHz looking into the drain of a diode-connected HEMT device for different device peripheries. The traces show variation with control voltage, with the capacitive reactances corresponding to negative gate voltages (devices off).

The foundry nonlinear device models are not extracted for this HEMT configuration with no drain bias, but we assume that they can show trends. An analysis to optimize phase tuning is first performed in order to select the proper HEMT device size. The T3 GaN PDK offers transistors of four standard total peripheries: 50 μm, 150 μm, 300 μm, and 600 μm. Looking into the drain of these source-grounded devices, the largest tunable reactance range is found by sweeping the gate voltage from -1 V to $+1$ V. The variable impedance range of these devices is plotted on the Smith Chart in Fig. 4.5. The real and imaginary parts of the HEMT reactive load for the 100 μm device are plotted in Fig. 4.6. The reactance dependence on control voltage can be expressed by a sigmoid function [107]:

$$X(V_c) = X_0(1-\Delta_X/2) + \frac{X_0\Delta_X}{1+e^{-(V_c-\bar{V})/\sigma_V}}, \tag{15}$$

where there are three fitting parameters: Δ_X is the normalized range in the value of reactance; $\bar{V}$ is the voltage at which the average value of capacitance occurs; and σ_V describes the rate of how reactance varies with voltage. X_0 is the reactance at the inflection point, $-22.2\ \Omega$. A curve fitting tool gives values of 2.625, 0.01873, and 0.09282 for Δ_X, $\bar{V}$, and σ_V, respectively. The goodness of fit for the sigmoid function is described by an R-squared value of 0.9998. This expression can be inserted in (14) to obtain the dependence

of transmission phase on control voltage. The real part of the impedance follows the derivative of $X(V_c)$ with some added constants and contributes to phase shifter loss. It is seen that the loss is the highest in the region where the reactance exhibits the most change.

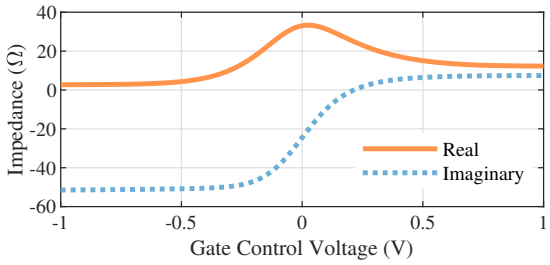


Figure 4.6: Real and imaginary parts of tunable impedance for a 100 μm device at 75 GHz, corresponding to the red curve in Fig. 4.5.

4.1.2 Lange Coupler

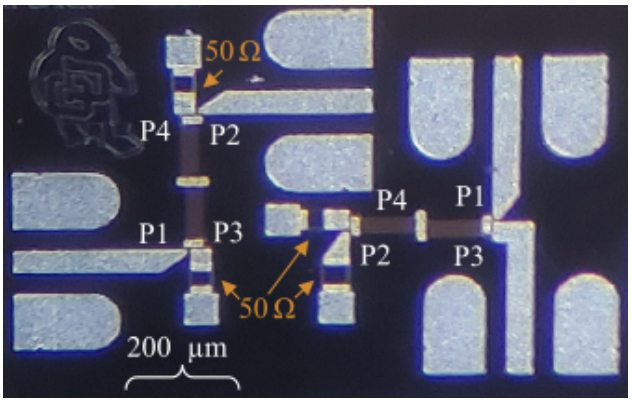
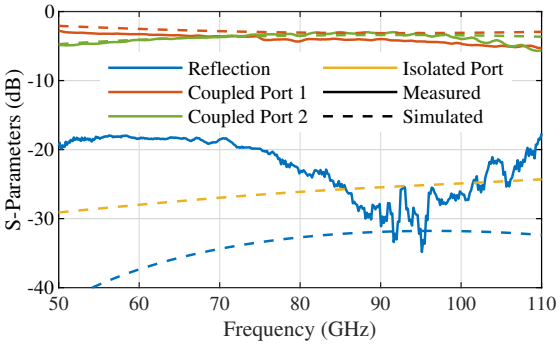


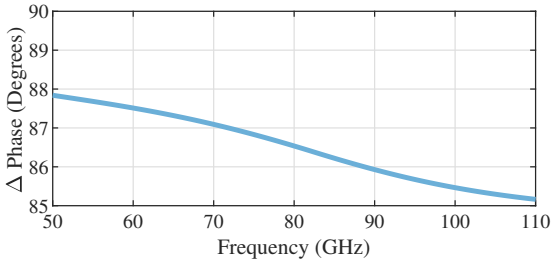
Figure 4.7: Photograph of the Lange coupler test structures on the MMIC, used to evaluate the phase and amplitude balance from 50 to 110 GHz. The isolated ports are terminated with 50 Ω on-chip resistors.

The coupler is a major component of a reflective phase shifter topology. Lange couplers are advantageous for this application due to their small footprint, low reflection, and wide bandwidth. A MMIC process with at least two metal layers to create airbridges and the ability to place metal traces with narrow spacing for the proper coupling factor are the key requirements for implementing a Lange coupler at millimeter wave

frequencies on chip. To characterize the couplers independently from the phase shifter, two test structures are fabricated on chip to compare the two coupled paths, Fig. 4.7. These structures are measured and compared to their simulated characteristics in Fig. 4.8a, from where it can be observed that the coupled ports have an increased loss of about 1-2 dB at the higher end of the band (>90 GHz) as compared to simulation. This negatively impacts the insertion loss. The simulated and measured amplitude imbalance from 50–110 GHz can be seen in the plot, while the simulated phase balance stays within 5° of the the ideal 90° relative transmission angle between the ”thru” and ”coupled” ports, as seen in Fig. 4.8b. The measurement of the phase balance involves two separate probe landings on two different test Lange couplers, making phase difference difficult to calibrate, but nevertheless the measured phase between the two coupled ports ranges from 70° to 85° across the octave bandwidth. The two types of port orientations give slightly different coupling across frequency, as presented in Fig. 4.8 and analyzed in [30].



(a)



(b)

Figure 4.8: (a) Comparison of measured and simulated Lange coupler test structure performance. (b) Simulated transmission phase difference between through and coupled ports.

4.1.3 MMIC Reflective Phase Shifter Simulations

Fig. 4.9 shows how the phase varies with control voltage in the range of most variation and as a function of control voltage for three device sizes and three frequencies in the band. The $4 \times 25\,\mu$m ($100\,\mu$m periphery) and $4 \times 37.5\,\mu$m ($150\,\mu$m) devices display a similar phase shift at 75 GHz, but the $4 \times 25\,\mu$m device performs better at the low end of the band at 60 GHz and below. The $6 \times 50\,\mu$m ($300\,\mu$m) sized device has a much lower simulated phase shift, as is the trend as the device size increases. The $100\,\mu$m device is selected for the design, as it provides the greatest phase shift across V- and W-bands.

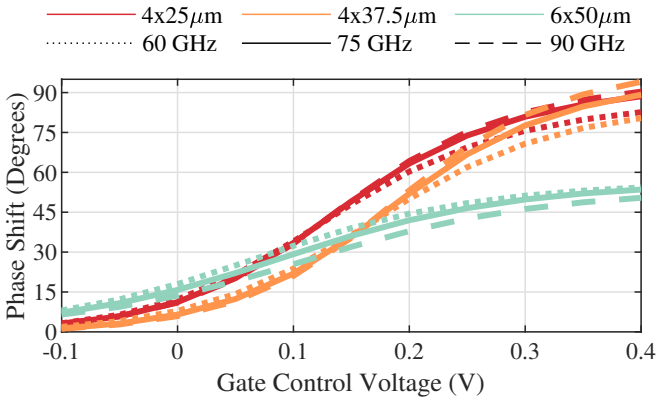


Figure 4.9: Plot of output phase of the reflective phase shifter from Fig. 4.2b for three device sizes at 60 GHz, 75 GHz and 90 GHz.

4.2 90° Phase Shifter Characterization

The phase shifter is characterized in small-signal operation as a function of control voltage and over frequency using a VNA with extenders, as well as in a scalar setup for compression and power handling.

4.2.1 Small-Signal Measurements

The fabricated circuits are tested with a calibrated HP 8510C network analyzer with V- and W-band extenders for small-signal characterization from 50–110 GHz in two separate bands, indicated by the dashed grey line. The waveguide outputs from the extenders transition to 1 mm coaxes connected to GSG $100\,\mu$m pitch probes, and the calibration for each band is done on-wafer with SOLT standards. Phase, return loss,

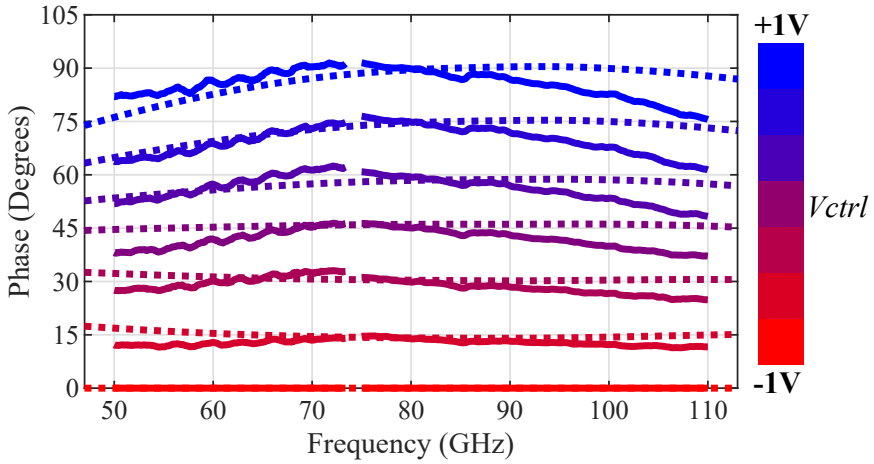


Figure 4.10: Simulated (dashed) and measured (solid) phase states of a single-bit reflective phase shifter in approximately 15° steps over frequency. Control voltage ranges from -1 V (red) to +1 V (blue) for 15° steps in phase.

and insertion loss are tuned continuously by adjusting the gate bias. To demonstrate the full tuning range, these parameters are captured for each 15° increment in phase. The phase states of the single-stage phase shifter are plotted in Fig. 4.10, displaying a tunable phase shift ranging from 76° to 90° over the entire bandwidth. $|S_{11}|$ and $|S_{21}|$ for each state are displayed in Fig. 4.11. Overall, the return loss ranges from 30 to 10 dB, indicating that the device is well matched over the bandwidth. The insertion loss is flat within 2 dB across the full 50–110 GHz tuning range for each individual phase state, but ranges from 2 to 12 dB across control voltage levels, comparable to other demonstrated phase shifters in this frequency range, as discussed in Section 4.4.

Continuous tuning of phase allows us to normalize the relative phase shift for the calculation of phase error at a given frequency and voltage point applied to the gate bias. Therefore, phase difference is calculated across frequency relative to the phase at 75 GHz at each gate bias. The phase differences for all measured bias points are then averaged to calculate the mean phase error across frequency. The average measured and simulated phase errors are plotted in Fig. 4.12. Across the frequency band, the measured phase error for the 90° phase shifter shown in blue is less than 11°, within -10° to +1°, with the trend well predicted by simulations. Negative phase error corresponds to a reduction in the phase tuning of this circuit. While a phase shift of 90° is measured at 75 GHz, the maximum tuning range is 82° at 50 GHz and 76° at 110 GHz.

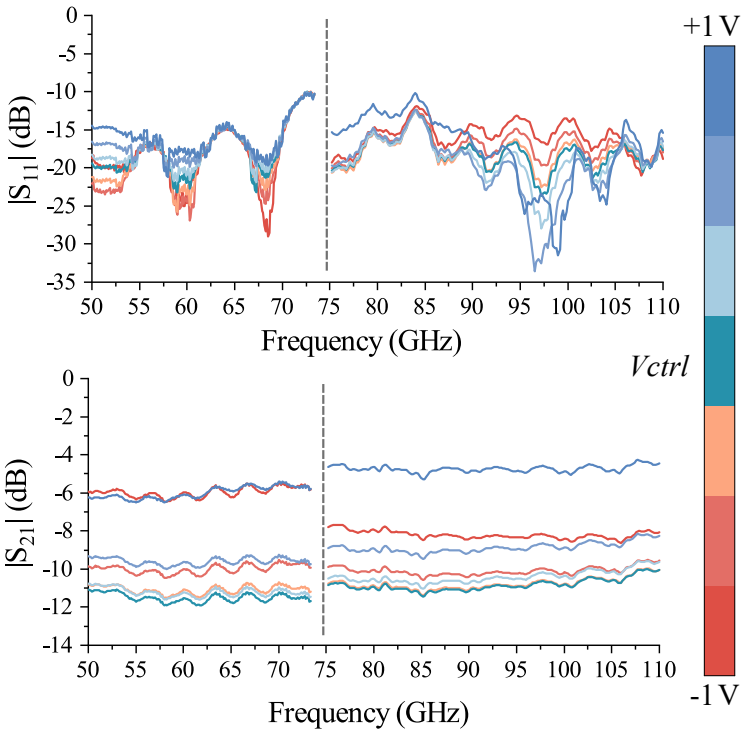


Figure 4.11: Measured insertion and return loss of single bit phase shifter for seven phase states. Dashed line indicates break where separate measurement setups were used for V- and W-band.

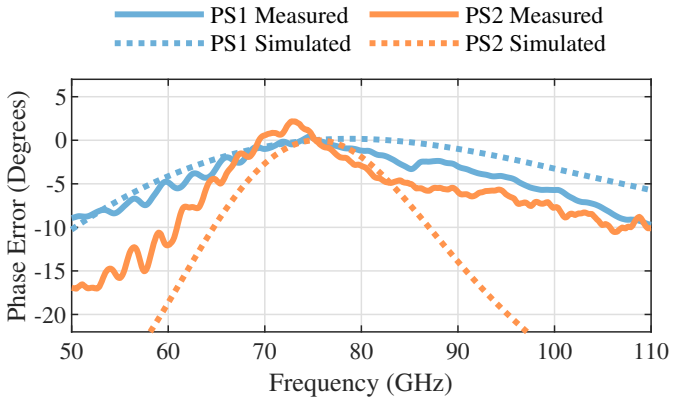


Figure 4.12: Simulated and measured phase error of the 90° and the 180° reflective phase shifters shown over frequency.

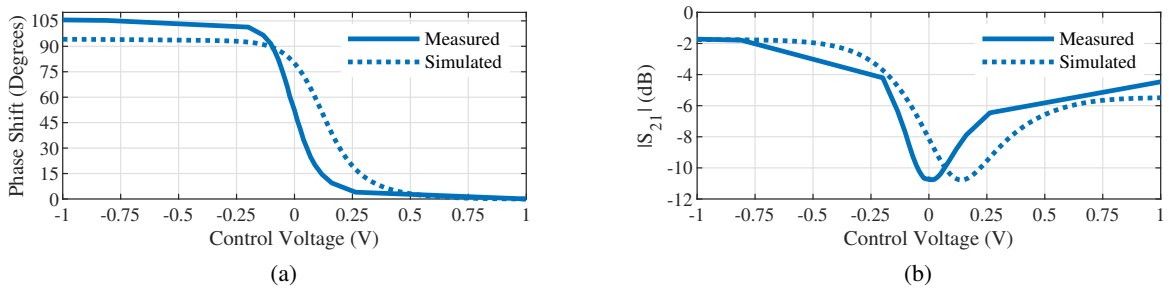


Figure 4.13: Measured (solid) and simulated (dashed) (a) phase shift and (b) $|S_{21}|$ versus control voltage at 75 GHz for single bit phase shifter.

The phase shift vs. control voltage is plotted at 75 GHz to compare the measured and simulated results in Fig. 4.13a, with practically the same results at other frequencies across the band [108]. Additionally, the simulations show a phase shift of up to 90°, while the measured phase shift can reach up to 105° tunability at 75 GHz. A comparison for $|S_{21}|$ as a function of control voltage is plotted at 75 GHz and is shown in Fig. 4.13b. When the HEMT impedance is closest to 50 Ω, insertion loss is maximized as the devices absorb some of the power. The insertion loss correlates well between measured and simulated results, although the minimum point is shifted by approximately $+0.1$ V in the measured data.

4.2.2 Large-Signal Characterization

The phase shifters are measured in a large signal setup as displayed in Fig. 4.14, to quantify compression and power handling. A 30.67 GHz RF source feeds a Ka-band driver, and the output of the driver is then upconverted with a frequency tripler and band-pass filtered. The W-band signal is then amplified with a driver and a high power amplifier stage. Measurements are taken with W-band power meters before and after the reference planes. The passive components connecting to the DUT are de-embedded to produce an output vs. input power dependence, displayed in Fig. 4.15. The curve displays the 0° state of the signal bit phase shifter at 95 GHz. A 1 dB compression point is measured at approximately 19 dBm input drive at the DUT and is not predicted by the nonlinear model.

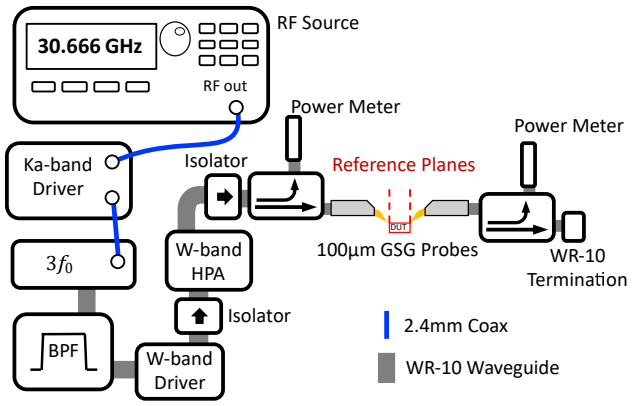


Figure 4.14: Simplified block diagram of large signal setup for measuring power handling of phase shifters.

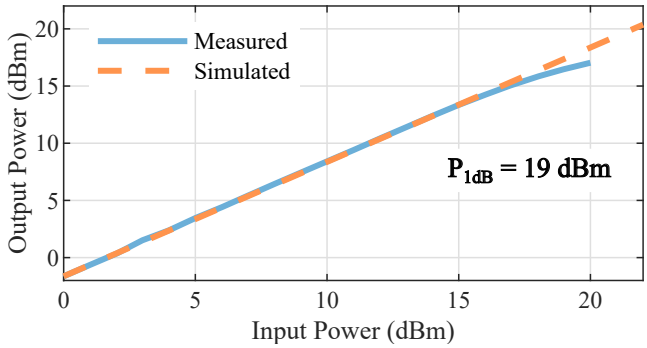


Figure 4.15: Measured and simulated power handling characterization at 95 GHz of single bit phase shifter. The 1 dB compression point is measured at approximately 19 dBm input power.

4.3 180° Phase Shifter Measurements

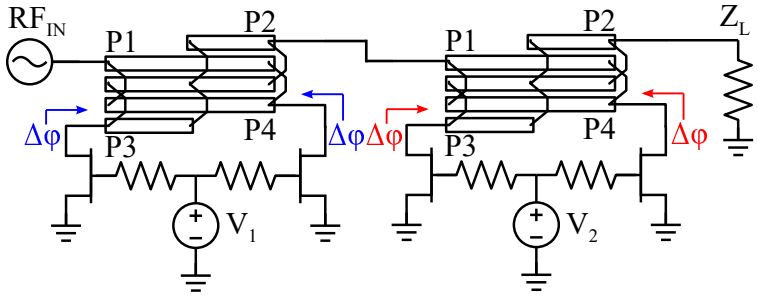


Figure 4.16: Schematic of reflective 180° phase shifter topology which consists of a cascade of two 90° phase shifters.

For increased phase shift, a 180° phase shifter is realized by cascading two 90° phase shifters, Fig. 4.16. This effectively doubles the range of phase tuning over frequency. The total simulated and measured phase shift from 50–110 GHz is displayed in 15° increments referenced to 75 GHz in Fig. 4.17. In contrast to the upper-band results for the 90° phase shifter shown in Fig. 4.10, each phase state appears flatter at the edges of the band in measurement as compared to simulation. At the high edge of the band, the phase states appear to compress; the lower states increase in phase shift while the higher states decrease. The range of phase shift varies over the frequency range, as is predicted in simulation. The maximum range of 195° is recorded at 73 GHz. The range decreases with increasing frequency at W-band, but remains operational with 149° of phase shift at 110 GHz. Phase error averaged for all states of the 180° phase shifter is plotted in orange in Fig. 4.12. Measured phase error ranges from -17° to +2° as compared to -32° to 0° in simulation.

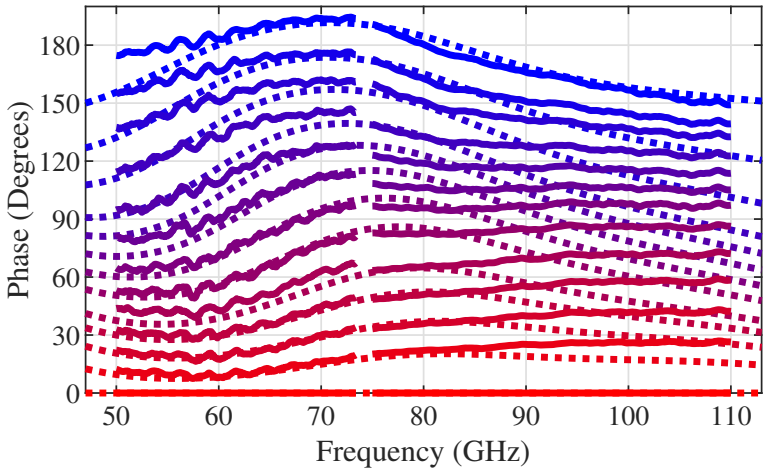


Figure 4.17: Measured (solid) and simulated (dashed) phase states of two bit reflective phase shifter in 15° steps over frequency. Control voltage ranges from -1 V (red) to +1 V (blue) for 15° steps in phase.

While phase is increased, the insertion loss for each state is expected to approximately double compared to the values in Fig. 4.11 when cascading two sections. This leads to more insertion loss variation across states, as the dip in $|S_{21}|$ from Fig. 4.13b becomes more pronounced. However, the addition of two stages to control phase also gives the ability to control insertion loss. After initial characterization of the

90° phase shifter, a lookup table can be constructed with phase shift and corresponding gate voltages, along with the resulting insertion loss for each state. Then, an appropriate combination of the two control voltages is chosen to maintain the same overall phase shift by allowing each stage to contribute different amounts of phase shift at a reduced overall insertion loss. In addition to reducing the loss, the goal is to flatten the insertion loss curve across phase.

Table 4.1: Voltages Applied to each gate for loss compensation at 75 GHz

Phase Shift	22°	54°	81°	113°	144°	175°
V_{g1} (V)	-0.28	-0.17	-0.05	-0.05	-0.05	0.00
V_{g2} (V)	-1.00	-1.00	-0.50	-0.35	-0.26	-0.17

This concept is demonstrated in Fig. 4.18 at 60 GHz, 75 GHz, and 100 GHz. Compared to the case when the gate control voltages are connected and varied simultaneously, controlling the gates independently reduces insertion loss by up 15 dB at 60 GHz while achieving the same total phase shift. Additionally, insertion loss variation is reduced from around 20 dB to less than 5 dB between 22° and 175° for the recorded states. The gate voltages corresponding to the control voltage distribution for improved insertion loss at 75 GHz are tabulated in Table I. This measurement is performed at three frequencies at the middle and edges of the band, but can be applied at any frequency within the range to give similar results; while the insertion loss still varies over the control voltage, it is mostly flat across frequency, as seen in Fig. 4.11.

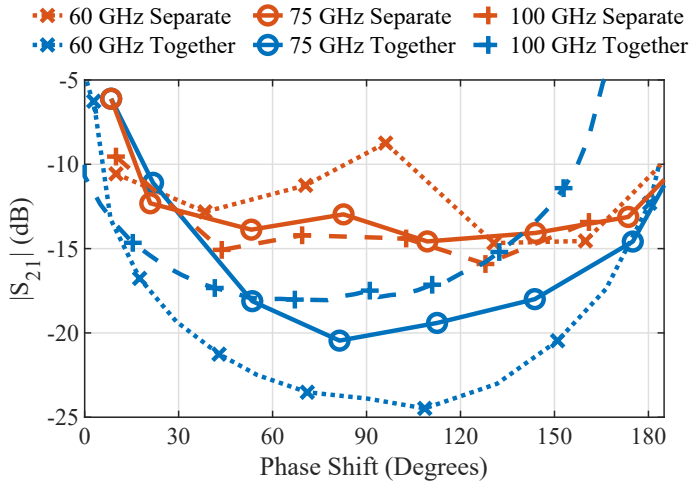


Figure 4.18: Comparison of insertion loss for two bit phase shifter with HEMT control voltages toggled independently and together at 60 GHz, 75 GHz, and 100 GHz.

4.4 Conclusion

In summary, this chapter presents design, simulation, and measurements of continuous 90° and 180° phase shifters implemented in a 40 nm GaN-on-SiC process in a reflective topology. Measured results show greater than 90° phase shift across 50–110 GHz with less than 10 dB average loss over a control voltage range of –1 V to +1 V, and a measured 1 dB compression point of 19 dBm at 95 GHz. Cascading two 90° phase shifters results in a 180° phase shifter in which toggling each set of tunable devices independently is shown to improve insertion loss by as much as 15 dB while providing the same phase change. Simulations with foundry models match measurements well for phase tuning and S-parameters over bandwidth, but cannot predict the power compression characteristic in this topology.

Table II shows a comparison of V- and W-band monolithic phase shifters, including vector modulators (VM) integrated in BiCMOS [99], CMOS SOI [102, 109] and GaAs [103]. Two GaN phase shifters are presented in [38] using the same technology and a digital phase shifter topology. While these designs display excellent performance, including phase errors $<5°$ and $<10°$ for circuits 1 and 2 respectively, they operate over a narrower bandwidth from 78–89 GHz and achieve 67.5° phase shift for the variable phase shifter. Additionally, 90 and 180° fixed phase bits are shown with 10° phase error for a narrow frequency

range from 70–78 GHz. In contrast, the GaN phase shifters presented here show the largest bandwidth with maintained phase variation up to 180° and with comparable insertion loss and area. The power handling is greater than 22 dBm, limited by our measurement capability, and the phase shifters do not consume any dc power. In a future design, the insertion loss can be flattened by incorporating variable gain amplifiers with low phase variation as in [110]. The contributions of this chapter are published in [30, 108, 111].

Table 4.2: Comparison of Millimeter Wave Phase Shifters

Source	Technology	Topology	Frequency (GHz)	Phase Shift (°)	S21 (dB)	P1dB (dBm)	Core Area (mm^2)
[99]	130 nm BiCMOS	Reflective	58-64	360	-3.7 to -10.3	13.8	0.16
[102]	45 nm CMOS	VM	57.7-84.2	360	-4 to -12	5	0.11
[109]	28 nm CMOS	VM	80.2-96.8	360	+0.83	-6	0.06
[103]	100 nm GaAs	Reflective	91.5-96.5	181-190	6.9	-	1.3
[38]	40 nm GaN	Reflective	78-89	67.5	2.9	>+24	0.85
[38]	40 nm GaN	Refelctive	70-78	180	2.1 to 4.6	>+24	1.7
This Work	40 nm GaN	Reflective	50-110	76-91	-4 to -12	+19	0.19
This Work	40 nm GaN	Reflective	50-110	149-195	-6 to -14	+22*	0.38

* Estimated, RF source limited to 20 dBm at 92 GHz

Chapter 5

Building Blocks for Integrated Duplexers

Duplexers allow for bi-directional communication over a single antenna, as displayed in the RF front end of Fig. 1.4. Half-duplex requires switching between the two paths, while full duplex allows for transmit and receive concurrently. Duplexers are highly scalable in terms of operating frequency and bandwidth, and can be monolithically integrated with other circuits, provided they have the power handling capability that exceeds the maximum power amplifier output power. This chapter presents several V and W-band (50–110 GHz) GaN HEMT switches in both the HRL T3 40 nm the Qorvo 90 nm GaN processes. The switches are characterized in terms of match, isolation, loss and power handling. A wideband active isolator is then introduced, which is later configured into an active circulator for full-duplex operation in Chapter 6.

5.1 Millimeter Wave Switches

Integrated millimeter-wave switches have been realized in several different semiconductor technologies: CMOS [112, 113], SiGe [14, 114], GaAs [115], and graphene [116]. W-band switches implemented in a 180nm CMOS process have a measured 1-dB compression point of 11 dBm [112]. A $P_{1dB} = 24$ dBm is achieved in SiGe BiCMOS with a PIN diode [117], and $P_{1dB} = 22$ dBm with SiGe HBT technology in [114]. High 1-dB compression points have been shown up to 300 GHz with $P_{1dB} = 14$ and 19 dBm for two and one 160-μm periphery transistors in a metamorphic 50 nm GaAs process [118]. Published GaN HEMT switch results show $P_{1dB} > 24$ dBm demonstrated for an HRL 40-nm GaN SPDT switch [38], and $P_{1dB} > 25$ dBm for an IAF 100-nm GaN HEMT switch with 160 μm periphery [119]. Table 5.1 gives a comparison of W-band GaN switches published to date, all using a shunt HEMT topology.

Table 5.1: Comparison of V- and W-band GaN Switches

Freq (GHz)	Type	IL (dB)	ISO (dB)	P_{1dB} (dBm)	Year Ref.
66-134$^{\triangle}$	SPDT*	1.2–2.2	16.8–20	>25	2018 [119]
68-134$^{\triangle}$	SPDT*	1.1–2.1	17.6–21.5	>25	2018 [119]
60-110†	SPST	0.9-1.4	>9	>24	2014 [38]
80-100†	SPDT*	1.3–1.7	>9	>24	2014 [38]
60-100†	SPST	**0.9-2.2**	**25-30**	**>20^{+}**	**2023 [120]**
65-105†	SPDT*	**1-1.5**	**15-20**	**>20^{+}**	**2023 [120]**
60-105†	SPDT$^{\blacksquare}$	**1.8-6**	**30-40**	**>20^{+}**	**2023 [120]**

$^{\triangle}$ 100 nm, † 40 nm, * SPDT single-HEMT, $^{\blacksquare}$ SPDT double-HEMT
$^{+}$ Peak large-signal values @ P_{IN} = 20 dBm and 92 GHz

5.1.1 40 nm GaN HEMT Switch Design

Three switches are demonstrated in this section in the HRL T3 40 nm GaN process. The switch design is described along with small signal measurements. An in-depth discussion of device size selection and large signal measurements of the switches can be found in [120].

5.1.1.1 MMIC Switch Operation

A common topology of millimeter-wave switches is the quarter-wave shunt topology. Series switch topologies are not useful at high frequencies because of the capacitance in the off-state and the added loss in the on-state of the switch [113]. Schematic depictions of the SPST and SPDT form of this circuit are displayed in Fig. 5.1. A positively biased shunt HEMT in the OFF-state presents a short to the signal. This is transformed through a quarter wave transmission line to appear as on open. In the ON-state, the shunt HEMT is pinched off and acts as a grounded capacitor loading the line. This capacitance resonates with a short inductive stub and is not seen by the signal, as it presents a parallel resonance to ground. The shorted stub also provides a dc ground at the HEMT drain, negating charge buildup.

Bandwidth limitations primarily result from the parallel resonant *LC* circuit and electrical length of the $\lambda/4$ section [119]. Terminating the quarter wave line with a perfect short is not easily accomplished at millimeter-wave frequencies where ohmic losses and parasitic reactances increase. Using more than

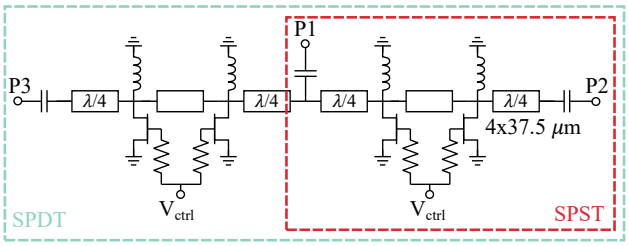


Figure 5.1: Circuit schematic of double-shunt HEMT SPDT and SPST switches.

one shunt source-grounded HEMT to improve isolation and power handling was demonstrated by InGaAs metamorphic HEMTs, at the cost of insertion loss [115].

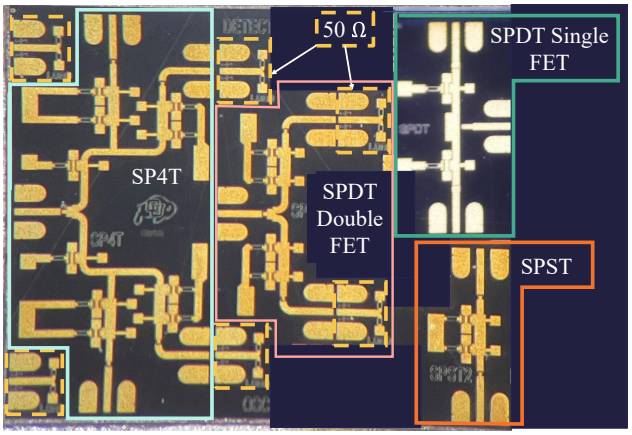
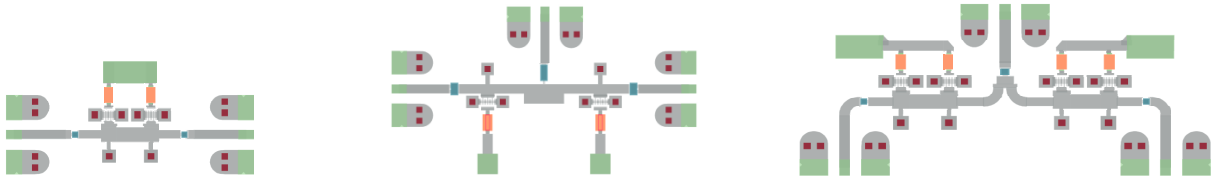


Figure 5.3: Photograph of HEMT switch MMICs in the HRL T3 40-nm GaN-on-SiC process, showing a SPST, two SPDTs and a SP4T switch with a total area of approximately 4 mm × 3 mm.

Fig. 5.2 shows the MMIC layouts of the double-HEMT SPDT and SPST switches, along with an SPDT with a single sunt HEMT in each branch. Each switch uses $4 \times 37.5\,\mu$m devices and compensating inductive shorted stubs. The switches are operated with a control voltage of -10 V for the ON state and +3 V for the OFF state through a 1.6 kΩ resistor to the gate of the HEMT. The switches are terminated in 100 μm pitch GSG pads which were optimized for operation across V- and W- band for on-wafer measurement. A picture of the reticle containing the switches along with terminations is displayed in Fig. 5.3. An SP4T is also displayed, whose design and performance is described further in [120].



(a) (b) (c)

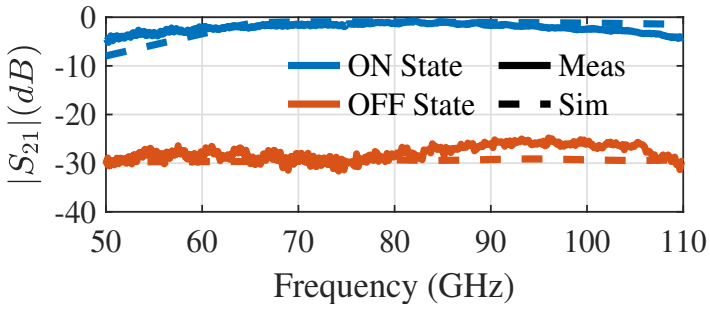
Figure 5.2: Layout of (a) the SPST switch, (b) the SPDT switch with a single shunt HEMT and (c) the SPDT switch with 2 shunt HEMTs.

5.1.1.2 Measured Results

On-wafer small-signal measurements are conducted with an HP8510C VNA with WR-15 and WR-10 frequency extender heads for V- and W-band S-parameter characterization, respectively. On-wafer SOLT calibration using 100 μm GSG probes on a W-band impedance standard substrate (ISS) from Cascade Microtech, was done for both bands of interest.

A summary of measured results from 50 to 110 GHz in small-signal operation and compared with simulated data is shown in Fig. 5.4 for the SPST and SPDT switches. The SPDT switch with a single shunted HEMT in Fig. 5.4b achieves an isolation of 15–20 dB and an insertion loss of 1–1.5 dB, while that in Fig. 5.4c achieves an isolation of 30–40 dB and an insertion loss of 1.2–6 dB. A dip in $|S_{21}|$ in Fig. 5.4c above 85 GHz compared to simulation is believed to result from imperfect loading at the OFF port from bondwires connecting to the termination. Nonetheless, a trade-off between isolation and insertion loss is observed by including one or two shunt HEMTs.

Power sweeps from 0 to 20 dBm at the DUT are performed for each presented HEMT switch at 92 GHz. The switches do not display any signs of compression up to the available input power of 24 dBm, as shown in [120]. Simulations also do not show any compression up until the simulators fail to converge around 10 W.



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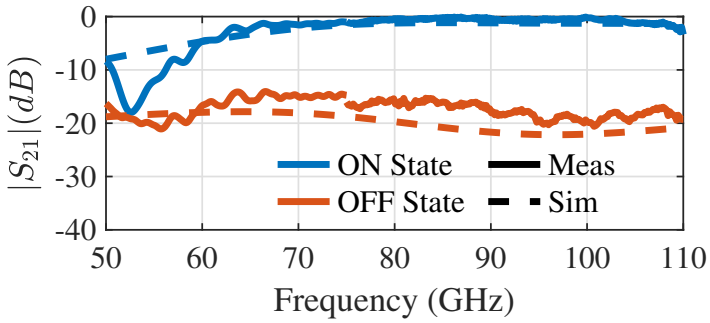

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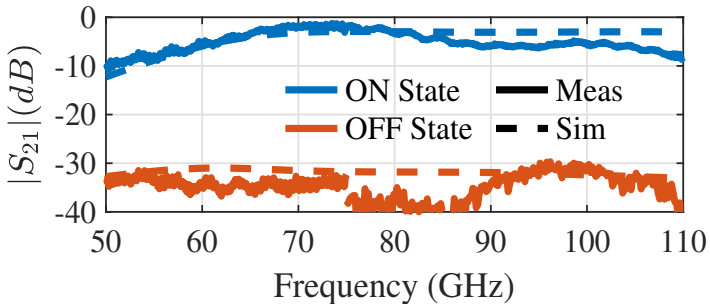


(c)

Figure 5.4: Measured and simulated small signal operation of (a) the SPST switch, (b) the SPDT switch with a single shunt HEMT and (c) the SPDT switch with 2 shunt HEMTs.

5.1.2 90 nm GaN HEMT Switch Design

An SPDT is also designed in Qorvo's 90 nm GaN T-gate process. This 15 V process is fabricated on a 50 μm SiC substrate and has an f_T/f_{max} of 115/250 GHz. It demonstrates PAE above 50 % at W-band with a maximum power density of 2.25 W/mm [46]. The QGaN09 process has been employed to design

high performing LNAs and PAs [36,47]. The switch is designed to integrate with the power amplifier whose design is thoroughly discussed in [121]. The topology selected for the SPDT is displayed in 5.5a. The switch is very similar to the single-shunt HEMT design from Section 5.1.1 with some slight differences. First, the shunt HEMTs used in this topology have a periphery of $3\times40\,\mu$m. The input matching is also slightly altered, with one shorted stub at the input replacing the input matching and two shorted stubs in Fig. 5.2b.

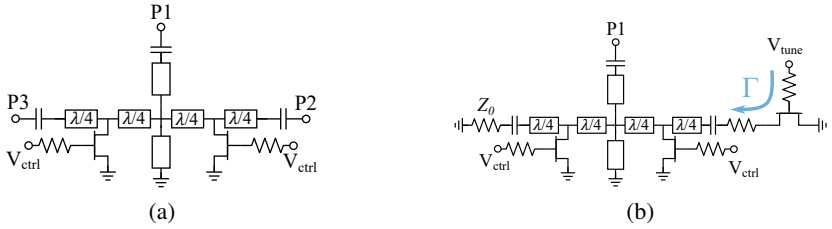


Figure 5.5: Schematic of SPDT with (a) three ports and (b) terminated output ports.

Simulated S-Parameters of the SPDT are displayed in Fig. 5.6. The switch has a minimum insertion loss of 1.5 dB in the ON path. The switch is not designed to cover such a wide bandwidth as compared to those in Section 5.1.1 due to the bandwidth of the PA. Thus, the 1 dB insertion loss bandwidth ranges from 72-102 GHz. Isolation to the OFF path is above 8 dB throughout this frequency range, while the return loss is above 9 dB through all of W-band.

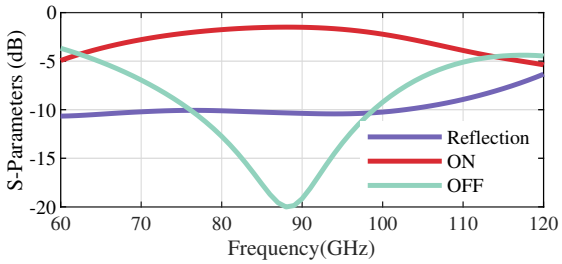
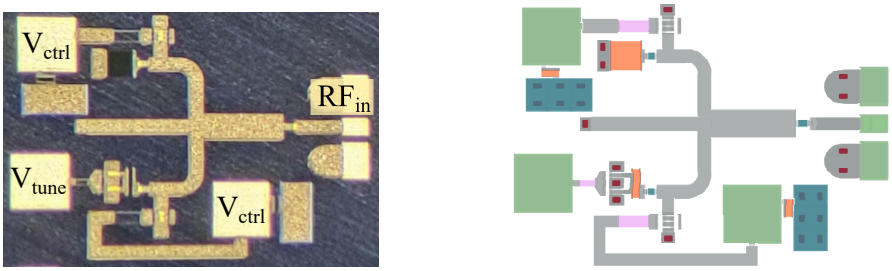


Figure 5.6: Simulated S-Parameters of SPDT Switch.

The switch is terminated at both output ports to integrate with the PA, as displayed in Fig. 5.5b. At one output, a matched termination is placed at the port. On the other, the port connects to the drain of a source grounded HEMT. The gate voltage has an additional dc pad to tune its impedance. This structure is

placed on the reticle as a breakout structure for individual characterization, displayed in Fig. 5.7.



(a) (b)

Figure 5.7: (a) Photograph and (b) layout of the terminated SPDT MMIC in QGaN09 with a total size of 0.8 mm × 0.9 mm excluding pads.

The one-port terminated SPDT is characterized in the two modes: matched termination and tunable impedance mode. Simulated and measured $|S_{11}|$ in the matched state are displayed in Fig. 5.8. A range of values are plotted in the shaded region showing the minimum and maximum bounds as the HEMT gate voltage is tuned. For the simulated plots, return loss ranges from as high as 2.4 dB at 100 GHz, to as low as 21.7 dB at 68 GHz. The measured values display lower return loss overall, as little as 21.8 dB at 86 GHz and as high as 4.4 dB at 110 GHz. A slight discontinuity is observed at 75 GHz where the W-band and V-band setups meet.

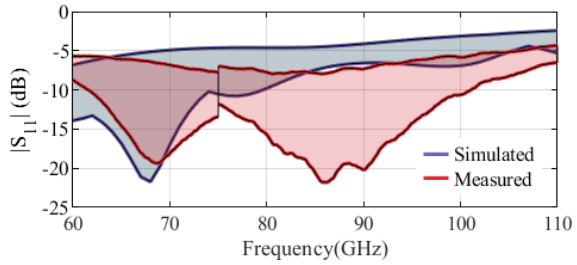


Figure 5.8: Range of $|S_{11}|$ as V_{tune} is swept from -5 to 1 V.

Simulations and measurements of the S_{11} in tunable impedance mode are displayed in Fig. 5.9 on a Smith Chart. In each plot, S_{11} is plotted as the gate voltage is tuned from -5 V to 0 V. Traces from 60 GHz to 110 GHz are displayed in 10 GHz steps. From the simulated plots, a wide tuning range at each frequency

is observed, with almost a full 360° rotation around various impedances. Measured results however do not display a wide tuning range. The start and end points based on the voltage tuning range are indicated, with an arrow pointing along the direction of the impedance path.

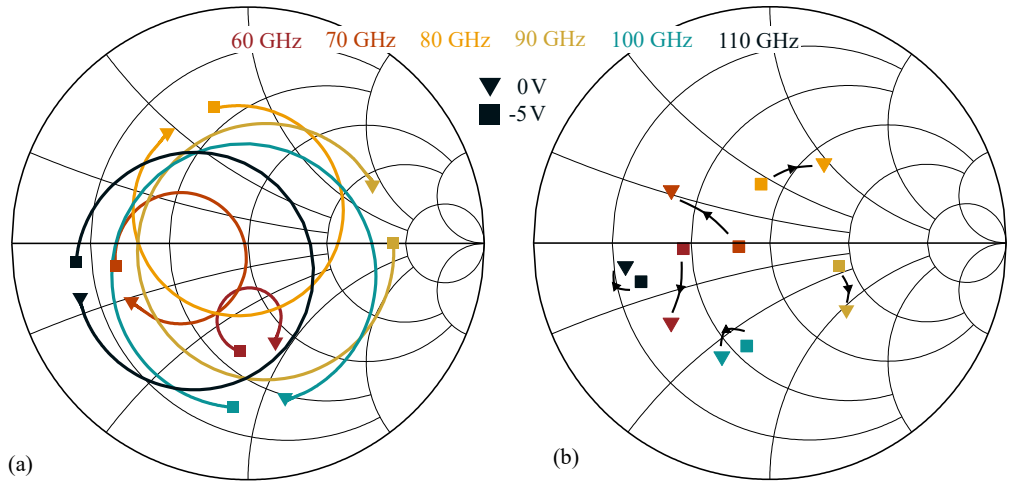


Figure 5.9: (a) Simulated and (b) measured impedance looking into terminated SPDT in tunable state as HEMT gate voltage is swept from -5 V to 0 V for different frequencies.

5.1.2.1 W-Band Power Amplifier with Mismatch Tunability

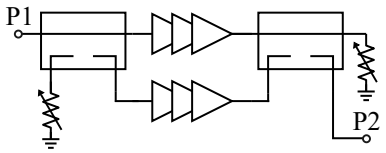
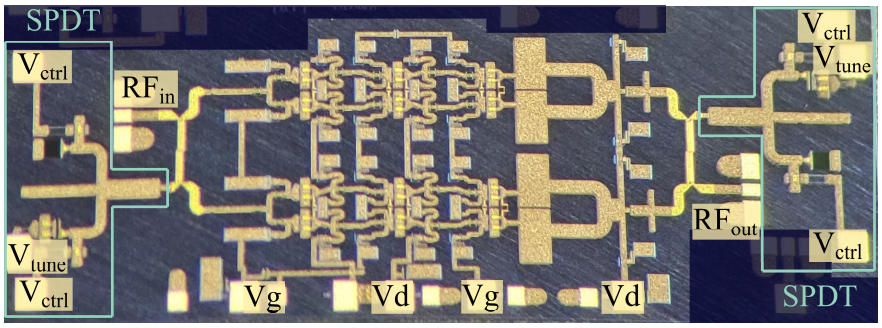


Figure 5.10: Schematic of three stage balanced amplifier with tunable matching.

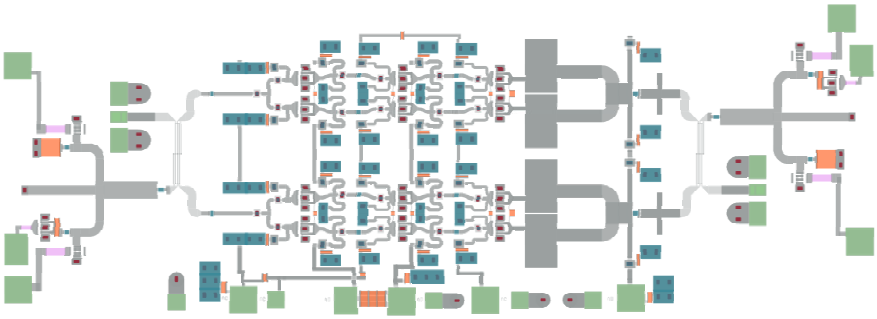
A balanced power amplifier with tunable impedances is also designed onto the reticle. From Fig 5.10, the topology is a three stage balanced PA with tunable impedances placed on the terminated fourth port of the Lange Couplers. The one-port terminated SPDT is employed for this tunable fourth port, with the ability to toggle between a matched and tunable state.

The power amplifier used in this design is adapted from [121] and tuned to accommodate for new DRC rules in the QGaN09 process. The staging ratio, 1:1.5:2 in the original design, is adjusted to 1:1:1 as

a result. A picture of the reticle and layout are displayed in Fig. 5.11 with each of the ports labeled. The SPDT is clearly integreted with the PA at both the input and output Lange terminations.



(a)



(b)

Figure 5.11: (a) Photograph and (b) balanced three-stage amplifier MMIC in QGaN09 two two integrated SPDTs for match tuning. Total size is 4.8 mm × 1.6 mm.

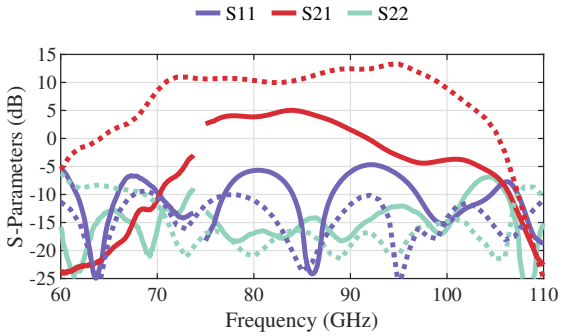


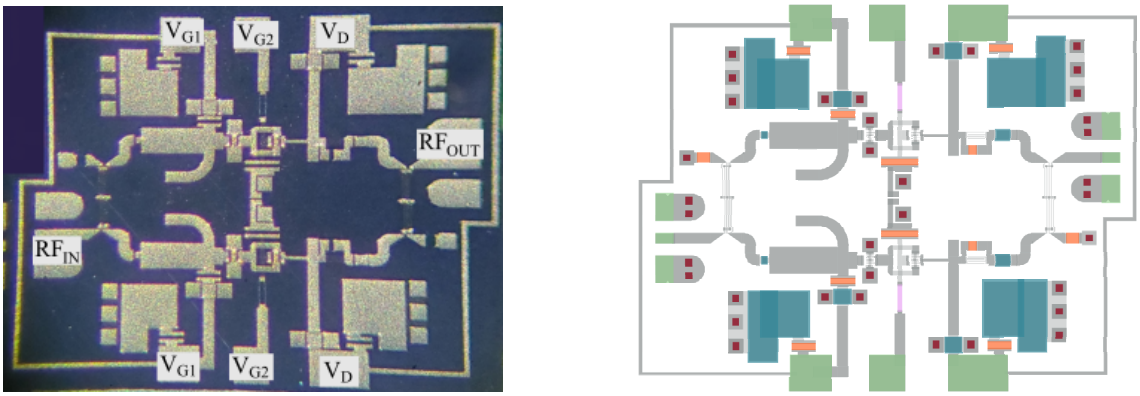
Figure 5.12: Measured (solid) and simulated (dashed) S-Parameters of balanced three-stage amplifier.

Measured and simulated S-Parameters of the QGaN09 balanced amplifier are displayed in Fig. 5.12.

Simulated gain is above 10 dB from 71-99 GHz. Measured gain, however, has a maximum gain of 5 dB at 84 GHz. In both simulation and measurement, the PA is well matched across all of W-band. Tuning the SPDT did not provide any noticeable change in matching. Note: in two previous run in QGaN09, similar severe gain degradation was observed [121]. These results show that the process still requires development, and this work provides useful feedback to Qorvo.

5.2 Active Amplifier-Isolator

Isolators are used in microwave front ends to prevent reflections from damaging or interfering with circuit elements. The design of an isolator requires a nonreciprocal element which can be realized by a ferrite [122] or semiconductor devices, e.g. [123]. Isolators based on time-varying circuits have been demonstrated, primarily in CMOS technologies that can support a large number of switching devices, e.g. [124]. These topologies are difficult to realize in III-V technologies such as GaN and GaAs, which are beneficial due to their greater power handling. Transistor-based isolators using resonant cells have been demonstrated in GaAs at lower frequencies [125].



(a) (b)

Figure 5.13: (a) Photograph of the balanced cascode amplifier MMIC with Lange couplers, using four $4 \times 25\,\mu$m HEMTs. (b) Layout of the circuit with a total size of 2.1 mm $\times$ 1.6 mm.

Traditional MMIC amplifiers can also operate as isolators and be cascaded to form active circulators [126] on chip in place of RF switches [120]. The cascode amplifier topology is suitable for such nonreciprocal devices, due to their inherently large bandwidth and high isolation resulting from a reduction

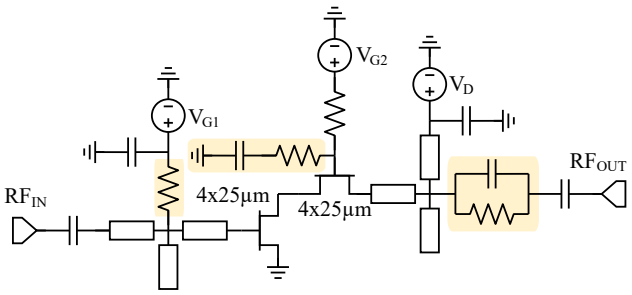


Figure 5.14: Simplified schematic of the unit cascode amplifier. Stability networks are highlighted in yellow.

in the Miller feedback capacitance compared to single-transistor amplifiers [49]. In this section, a balanced cascode amplifier is designed for wideband flat gain and high reverse isolation. The circuit is displayed in Fig. 5.13a with a size of 2.1 mm by 1.6 mm, along with its layout in Fig. 5.13b.

5.2.1 Circuit Topology

The amplifier design presented here is implemented in the HRL T3 40 nm GaN process. The goals for this design are wideband flat gain and high reverse isolation. The gate to drain capacitance of the transistor in common-source amplifiers is significant with increasing frequency, so a cascode topology is selected to increase bandwidth and isolation. Some cascode amplifiers use feedback networks for stability [40] or power compression enhancement [127], but this can lead to a reduction in reverse isolation. The schematic of a unit cascode amplifier is displayed in Fig. 5.14. The unit amplifier contains two $4 \times 25\,\mu$m transistors connected in cascode, with stub matching networks at the input and output. Using foundry models for this process, the nonlinearity of the cascode device cannot be modeled with power fed into the source. As a result, the amplifier is designed for small signal performance. The two gates of the cascode cell are biased independently to allow an equal voltage drop, $V_D/2$, from the drain to source of each transistor. Two such unit amplifiers are then placed in a balanced configuration to improve wideband matching and power handling using the Lange Coupler detailed in [128]. DC routing connecting the two V_{G1} pads and the two V_D pads of the single-ended amplifiers is seen in the layout in Fig. 5.13b and reduces the number of dc probes needed for measurement.

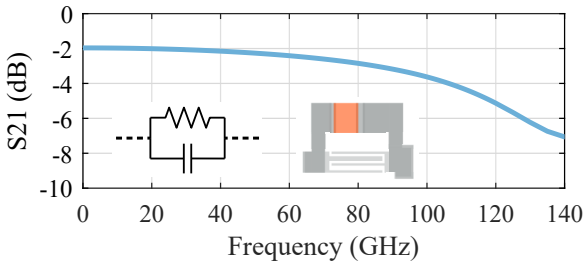


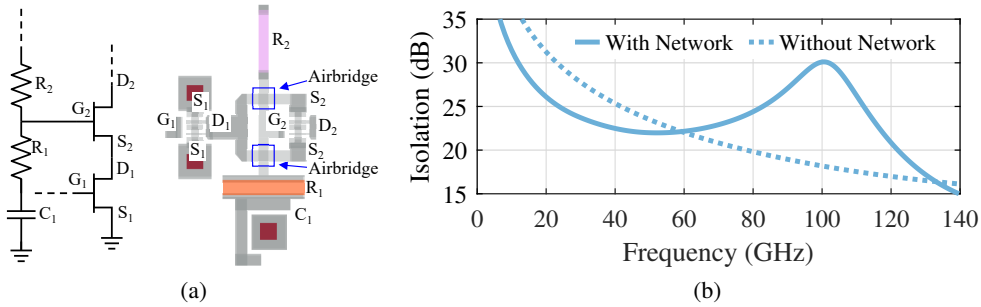
Figure 5.15: Simulated $|S_{21}|$ of output stability network with schematic and layout representations overlayed.

5.2.2 Stability Network Design

Stability is a particular concern in the design of the cascode amplifier due to multiple feedback mechanisms. Low frequency instability is addressed through bias line design. From the layout in Fig. 5.13b, it is seen that large shunt capacitors with a series resistor are placed in the first gate and drain bias network to attenuate low frequencies where instabilities may resonate along the long transmission lines. A small resistor is also placed in series with the first gate path. Additional larger capacitors are used off chip for low frequency stability.

At the output, an $|S_{22}|$ above 0 dB at the high end of W-band indicated instability, so a parallel RC network is inserted. The network's circuit and layout implementation are displayed in Fig. 5.15. The capacitor is realized using interdigitated metal fingers to give a low capacitance and quality factor and add some of the desired loss. A parallel RC typically allows high frequency signals to pass through with less attenuation. However, the long fingers of the interdigitated capacitor add inductance that cause more insertion loss at and above W-band, as seen in Fig. 5.15.

The design of the interconnect between the two transistors, displayed in Fig. 5.16a, is critical to maintaining stability of the amplifier. The configuration of the two devices requires airbridges for a connection from the drain of the first device (D1) to the source of the second (S2), in addition to a separate bias network made up of resistor (R2) for the second device. The second device is highly susceptible to coupling at the gate (G2) as a result of the airbridges. A series resonant structure to minimize the coupling between these two paths is designed using a coupled line capacitor (C1) directly to a via, along with the via inductance.



(a) (b)

Figure 5.16: (a) Schematic and layout representation of interconnect between HEMTs in the cascode pair. (b) Comparison of isolation from drain of HEMT1 (D1) to gate of HEMT2 (G2) with and without resonant network.

A small resistor (R1) is added to attenuate the signal at its resonant frequency. In Fig. 5.16b, the isolation between D1 and G2 for this interconnect network is plotted with and without the resonant network. Without the network included, isolation decreases with increasing frequency as the parasitic capacitance becomes increasingly significant, below 20 dB in W-band. The resonant network adds a peak at 100 GHz to improve isolation by approximately 12 dB at this frequency and maintain D1 to G2 isolation well above 20 dB from dc through W-band. With all of these networks implemented, overall amplifier stability is ensured using linear simulations. Nyquist and k-factor measurements indicate unconditional stability from DC to the third harmonic (330 GHz) for a wide range of impedances at the DC and RF ports. Large signal stability could not be accurately analyzed due to the lack of cascode models in this process.

5.2.3 Measurements

The cascode amplifier is mounted on a gold-plated copper molybdenum (CuMo) carrier, and the dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for further stability. The circuit is probed on a Summit 9000 probe station with 100-μm pitch GSG probes and characterized in small signal from 30 GHz to 110 GHz. An E8364C PNA Network Analyer is used for characterization from 30−50 GHz, while an HP8510C Vector Network Analyzer with V-band and W-band extender heads is employed for characterization at 50−75 and 75−100 GHz, respectively. Small gaps in the measured data of Fig. 5.17 and Fig. 5.18 are in place of the slight discontinuities between these three measurement setups.

5.2.4 Small Signal Measurements

Small-signal characterization of the amplifier is performed at a bias point of $V_{DD} = 12\,\text{V}$ with a drain current of 38 mA. The S-Parameters are plotted in Fig. 5.17, comparing the simulated and measured results. The amplifier has a small-signal gain $S_{21} \approx 7\,\text{dB}$ over a wide frequency range with a 3 dB bandwidth from 46 to 102 GHz. A slight peak of 8 dB is measured around 60 GHz. The circuit is also well matched, with $|S_{11}|$ and $|S_{22}|$ both below -10 dB across almost the entire band.

The small-signal isolation for this active isolator is defined as follows:

$$I = 10\log\left[\frac{P_2/P_1}{P_1/P_2}\right] = 20\log|S_{21}| - 20\log|S_{12}|$$

As seen from Fig. 5.18, the isolation ranges from 32 to 43 dB within this frequency range.

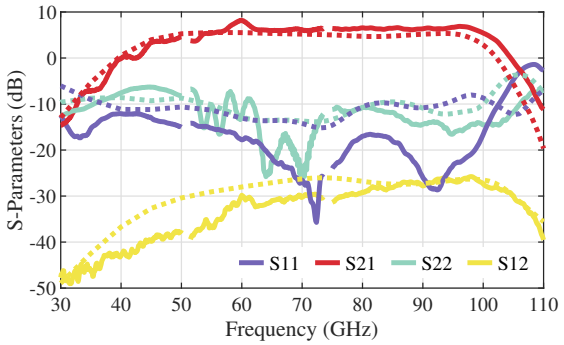


Figure 5.17: Measured (solid) and simulated (dashed) S-parameters of cascode amplifier with 12 V, 38 mA drain current bias.

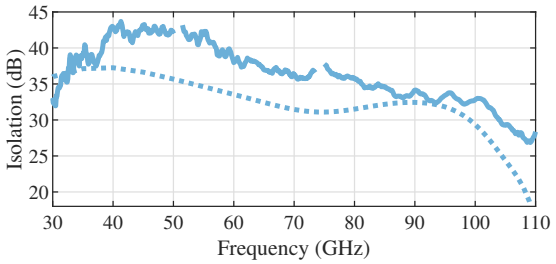


Figure 5.18: Measured (solid) and simulated (dashed) small-signal isolation of the balanced cascode MMIC isolator with gain.

5.2.5 Large Signal Measurements

Large-signal characterization is next performed on the cascode amplifier across W-band. For the large signal setup, a Ka-band source is fed into a Ka-band amplifier. The signal is then upconverted to W-band through a passive frequency multiplier and filtered before it is fed into a W-band amplifier. A small portion of the signal is then coupled off for an input power measurement. At the output, a portion of the signal is coupled off for an output power measurement while the remaining power is dissipated through attenuators. The passive components between the two W-band power meters are measured independently, deembedding between the couplers and the probe tips. This setup unfortunately does not allow for large-signal measurements below 75 GHz. In addition, large-signal isolation could not be measured due to a combination of the limited sensitivity of the W-band W8486A Power Sensors (-30 dBm) and maximum output power of the W-band source.

The input power is swept in 1 dB steps across frequency. Traces of the output power and large signal gain are plotted in Fig. 5.19 at 82 GHz, 89 GHz, and 96 GHz. The amplifier is biased at a slightly higher drain current of 100 mA to compensate for the limited sensitivity of the power sensors. Surprisingly, the large-signal gain peaks just below 10 dB at 89 GHz, almost 3 dB higher than the small-signal gain. This is due to the impedances looking into the devices varying with its nonlinear reactances. As a result, the networks are better matched to the devices around 89 GHz where the gain peaks. These effects could not be accounted for in simulation as explained in Section 4.1. From Fig. 5.19, the 1 dB compression point is measured at approximately 6, 5 and 6 dBm input power for 82, 89 and 96 GHz, respectively. The corresponding output powers at these frequency and power levels are 12.5 dBm, 13.7 dBm, and 11.5 dBm.

We measure compression at 6 dBm of input power, but this includes a gain of at least 7 dB of the first device. Therefore, effectively, the compression is on the order of at least 13 dBm for the second device which could not be modeled during the design phase. To further improve this metric, one might choose a larger device periphery for the cascode transistor, or if possible as in [129], a larger gate length transistor.

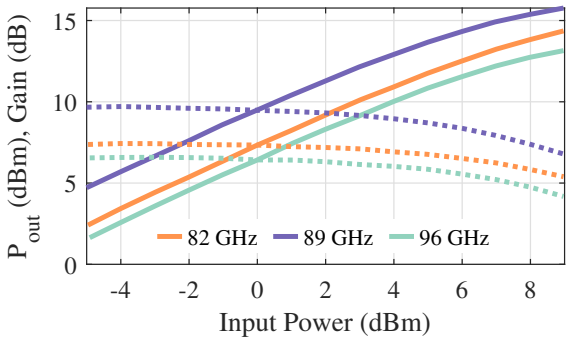


Figure 5.19: Output power (solid) and gain (dashed) of cascode amplifier measured against input power at 82, 89, and 96 GHz. Amplifier is biased at 12 V, 100 mA quiescent drain current.

Table 5.2: Comparison of Solid-State Transistor Isolators

Reference	Technology	Frequency (GHz)	Isolation (dB)	$\lvert S_{21}\rvert$ (dB)	$P_{DC,q}$ (mW)	IP_{1dB} (dBm)	NF (dB)	Area (mm^2)
[130]	200 nm SiGe	5-6	35	-2	2.6	-	13	0.28
[125]	GaAs	7.21−10.39	14.9	-0.2	114.3	15.5	-	1.02
[125]	GaAs	8.07−9.73	31.7	0.3	229	10.2	-	4.42
[131]	180 nm CMOS	24	36.8	-1.8	3.6	9.5	4−6.7	0.29
[132]	65 nm CMOS	1.5 (tunable, 85-110)	45− 46.5	-4.5	9.6− 12.9	10.9	4.53	0.13
[48]	40 nm GaN	46−102	32−43	7	470	6	5.4−10*	3.36

* Simulated

5.2.6 Conclusion

Several wideband circuits that serve as building blocks for duplexers are detailed in this chapter. An SPST and three SPDT designs are first discussed. A wideband cascode amplifier with high reverse isolation is then detailed. A comparison of this circuit with other state-of-the-art published transistor isolators is displayed in Table 5.2. This circuit operates over a much wider bandwidth and at higher frequencies with comparable isolation and noise figure to other designs. The contributions in this chapter are detailed in [30, 48, 120].

Chapter 6

Active Circulator MMICs

Circulators are another form of duplexer, shown in the RF front end in Fig. 1.4, and allow full-duplex operation. A nonreciprocal element provides high isolation in the reverse path, with a desired low loss in the forward path. Microstrip and waveguide W-band circulators have been demonstrated in [133] and [134], respectively, with ferrite resonators which require external bias magnetic fields and are not monolithically integrated. Self-biased ferrite circulators hybridly embedded in a GaN-on-SiC substrate are described in [46, 135]. On-chip active circulators are desirable for higher levels of integration. Integrated-circuit quasi-circulators have been demonstrated at millimeter waves in CMOS [136], SiGe [137], InP [138], and GaAs [139, 140], with limited power handling. The goal of this chapter is to demonstrate a broadband GaN MMIC circulator with high P1dB and a potential of higher power handling and improved linearity.

Circuit implementations in GaN have been proposed or demonstrated at lower frequencies [141–144]. One approach contains three identical amplifiers and co-designed Lange couplers with coupling coefficients that are not necessarily 3 dB. These components are connected in a ring configuration to achieve gain in the forward path and high isolation in the reverse path, as shown in the block diagram in Fig. 6.1. This approach was demonstrated in a GaAs technology at X-band [126] and scaled to W-band frequencies in [128], employing a GaN-on-SiC technology described in [145]. In this chapter, we extend the concept to traveling-wave and cascode topologies, with photos of the two fabricated circulator MMICs displayed in Fig. 6.6.

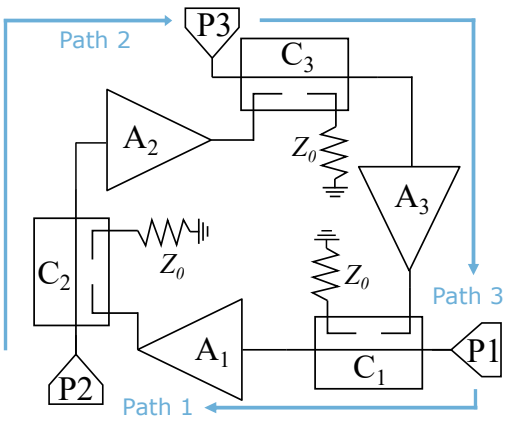


Figure 6.1: Block diagram of active circulator topology. The three couplers have the same coupling ratio in the MMICs presented in this work, and the three amplifiers are also the same. The isolated coupler ports are terminated on-chip in matched loads.

6.1 Active Circulator MMIC Design

The circulator designs presented here are implemented in the HRL T3 40 nm GaN process on a 50 μm SiC substrate. The T3 process achieves an $f_T/f_{\max}$ of 200/400 GHz with a breakdown voltage greater than 40 V. Three metallization layers are used to form transmission lines and air bridges, while capacitors and resistors are formed with silicon nitride (SiN) and tantalum nitride (TaN), respectively.

Most integrated-circuit active circulators use transistors as the non-reciprocal element. The topology chosen for this design contains three identical amplifiers connected in a ring with 90° couplers. The three ports of the circulator are connected to the same ports of three identical Lange couplers. The operation of an active circulator ring topology can be described as follows. Assuming perfectly matched ports, the power from each input is split to two coupled ports. Part of the signal drives one of the amplifiers, while the remainder arrives at the output of the amplifier from the previous port. For example, part of a transmitted signal from Port 1 is amplified by amplifier A_1, while the remainder is coupled through C_1 to the output of A_3. Thus, a low $|S_{12}|$ of each individual amplifier is required for high reverse-path isolation. At the output of A_1, part of the amplified signal is coupled to Port 2 through C_2, while the remainder is dissipated in the load. Amplifier A_2 is connected to the isolated port of C_2. Each subsequent amplifier is connected to the isolated port of the previous coupler.

Transmission to the isolated port is attenuated in two fashions: reverse and forward. For example, an input at Port 1 is isolated in the reverse path to Port 3 through C_1, A_3, and C_3, and in the forward path through C_1, A_1, C_2, A_2, and C_3. In the reverse path, a low $|S_{12}|$ of the amplifier connected to the coupled port is the primary factor, while in the forward path, the isolated port of the output coupler has the greatest impact. To compare the contributions of the two paths to the total isolation, we define the insertion loss between the externally connected coupler port and the input and outputs of the amplifiers as, respectively, L_{T} and L_{C}, while the coupler isolation is L_{i}. Each amplifier is assumed to have the same gain, G, and reverse isolation, L_R. For example, the isolation between Port 1 and Port 3 in the reverse path is:

$$I_{\mathrm{R}} = L_{\mathrm{C}} + L_{\mathrm{R}} + L_{\mathrm{T}}, \tag{6.1}$$

while in the forward path, the isolation is:

$$I_{\mathrm{F}} = L_{\mathrm{T}} - G + L_{\mathrm{i}} - G + L_{\mathrm{C}}. \tag{6.2}$$

The total isolated power, $P_{\mathrm{R}} + P_{\mathrm{F}}$, has equal contributions from both paths when

$$L_{\mathrm{R}} = L_{\mathrm{i}} - 2G. \tag{6.3}$$

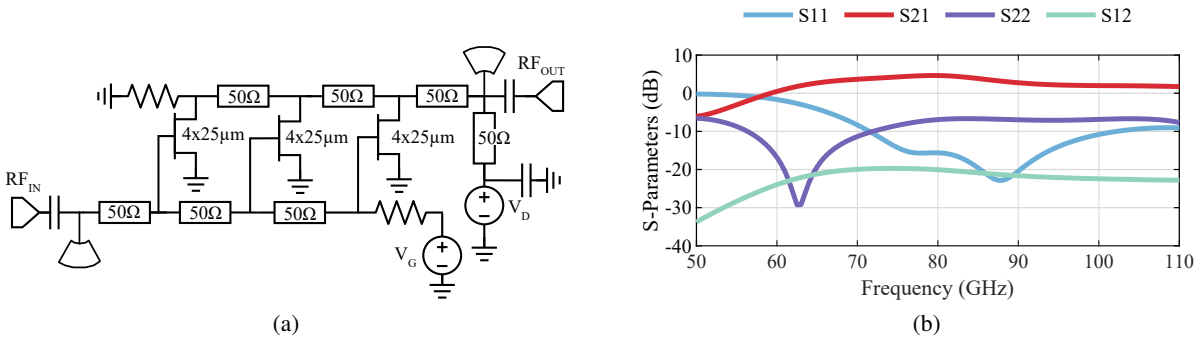
In most cases, one of the two paths will dominate power received in the reverse port. When all three of the amplifiers are turned on, which we refer to as the *Full Circulator Mode* (FCM), forward gain significantly reduces the isolation. To minimize this impact, the circuit can also operate in *Bias-Switched Circulator Mode* (BSCM), whereby the amplifiers in unused paths are biased off. In this case, isolation is dominated by reverse isolation of the amplifier, and the circulator is limited to half-duplex operation.

In principle, the amplifier between the Tx and Rx connected ports is not necessary for operation. However, a key characteristic of this circuit is that it is a "true" circulator, since each path consisting of a coupler C_i and amplifier A_i is theoretically identical. This implies that the antenna, transmit path, or receive path can be connected to any of the ports provided the amplification is in the correct direction. It also allows the circulator to be used in a variety of applications, not limited to antenna interfacing circuits,

e.g. reflection amplifiers [146]. In contrast, the majority of active circulators published to date fall into the category of quasi-circulators which must be connected in a specific configuration.

6.1.1 Amplifier Design

The unit amplifiers used in each branch of the ring are designed with bandwidth and isolation as primary specifications. A traveling-wave topology is selected for the unit amplifier of the first circulator, with a simplified schematic displayed in Fig. 6.2a. The amplifier contains three $4\times25\,\mu$m devices connected with unequal length $50\,\Omega$ transmission lines at the gates and drains. DC blocking capacitors are placed at the input and output of the amplifier. The gate is biased through a resistor and the drain bias line is a transmission line with a shunt capacitor before the pad. A 12 V nominal drain voltage is applied for this process, with the gate bias set for maximum gain in small-signal operation. The input and output matching network layouts for each amplifier are slightly different to enable proper connectivity in a ring. Simulated S-parameters of the unit amplifier are displayed in Fig. 6.2b. The distributed amplifier has $|S_{21}| \approx 5$ dB at 80 GHz with a 3 dB bandwidth from $62-112$ GHz, and $|S_{12}| = 20\pm2$ dB.



(a) (b)

Figure 6.2: (a) Simplified schematic of traveling-wave amplifier used for Circulator 1. The three devices have equal peripheries, while the interconnecting transmission lines have the same impedances but different electrical lengths. (b) Simulated S-parameters of unit distributed amplifier.

The second circulator (Circulator 2) uses the cascode amplifier validated in [48]. The gate to drain capacitance of the transistor in common-source amplifiers is significant with increasing frequency. The cascode cell is a suitable nonreciprocal element for this application, due to its inherently large bandwidth and

high isolation resulting from a reduction in the Miller feedback capacitance compared to single-transistor amplifiers. Some cascode amplifiers use feedback networks for stability [40] or power compression enhancement [127], but this can lead to a reduction in reverse isolation. The schematic of a unit cascode amplifier is shown in Fig. 6.3a. The unit amplifier contains two $4 \times 25\,\mu$m transistors with stub matching networks at the input and output. The foundry model is not designed for nonlinear modeling of a cascode cell. As a result, only small-signal performance is considered. The two gates of the cascode cell are biased independently to allow an equal voltage drop, $V_D/2$, from the drain to source of each transistor. DC routing connecting the gates of each amplifier is achieved using two rings around the circulator, as seen in Fig. 6.6b. The pads of each gate are wire bonded to the ring to reduce the number of dc probes needed for measurement. Each drain is biased individually to enable switching from full- to half-duplex mode of operation. Simulated S-parameters of the unit amplifier are displayed in Fig. 6.3b. The cascode amplifier has a flat gain $|S_{21}| \approx 6\,$dB with a 3 dB bandwidth from $42-98\,$GHz and an $|S_{12}| = 29 \pm 5\,$dB.

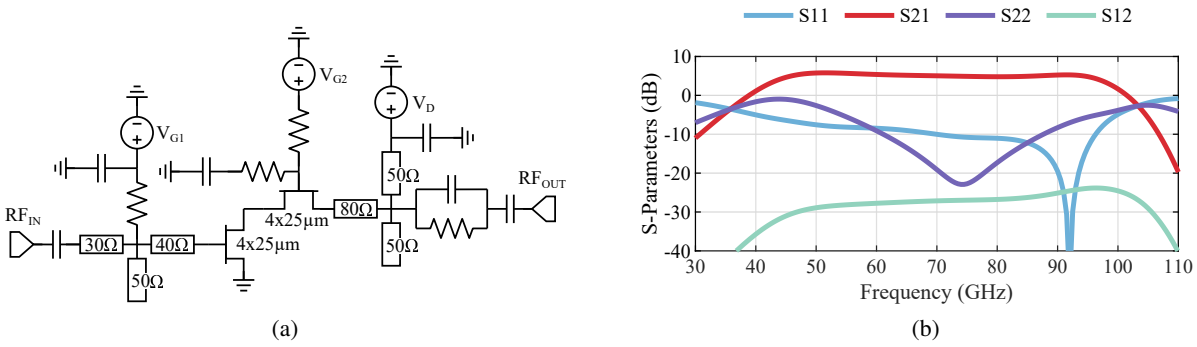


Figure 6.3: (a) Simplified schematic of cascode amplifier used for Circulator 2. (b) Simulated S-parameters of unit cascode amplifier.

6.1.2 Lange Coupler Design

The coupler is a major component of an active circulator ring topology. Lange couplers are advantageous for this application due to their small footprint and wide bandwidth. A MMIC process with at least two metal layers to create air bridges and the ability to place metal traces with narrow spacing for the proper coupling factor are the key requirements for implementing a Lange coupler at millimeter-wave fre-

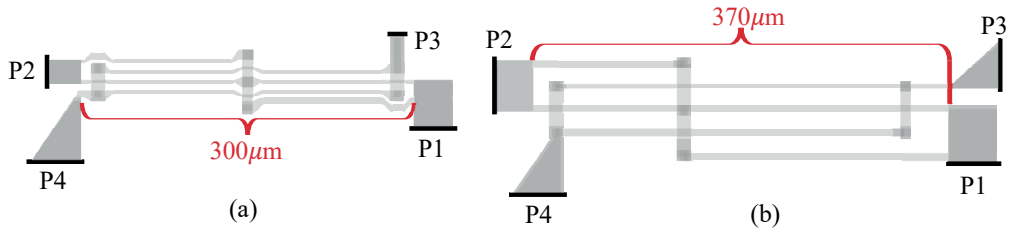


Figure 6.4: Layout depiction of Lange couplers. (a) Uniform 3-dB Lange coupler used in Circulator 1. (b) Nonuniform Lange coupler used in Circulator 2, with a coupling coefficient of 6 dB and transmission coefficient of -1.5 dB.

quencies. Layouts of the two Lange couplers used in these designs are given in Fig. 6.4. Individual coupler test structures are fabricated for independent characterization, with a comparison to simulations shown in Fig. 6.5.

The Lange coupler in Fig. 6.4a is designed for an even 3 dB split between the input and coupled ports. It is observed in Fig. 6.5a that the coupled ports have an increased loss of about $1-2$ dB at the higher end of the band (>90 GHz) as compared to simulation. The measurement of the phase balance involves two separate probe landings on different test Lange couplers, making calibration difficult; nevertheless the measured phase between the two coupled ports ranges from 70° to 85° across the octave bandwidth. Simulated isolation ranges from $24-29$ dB across V and W-band.

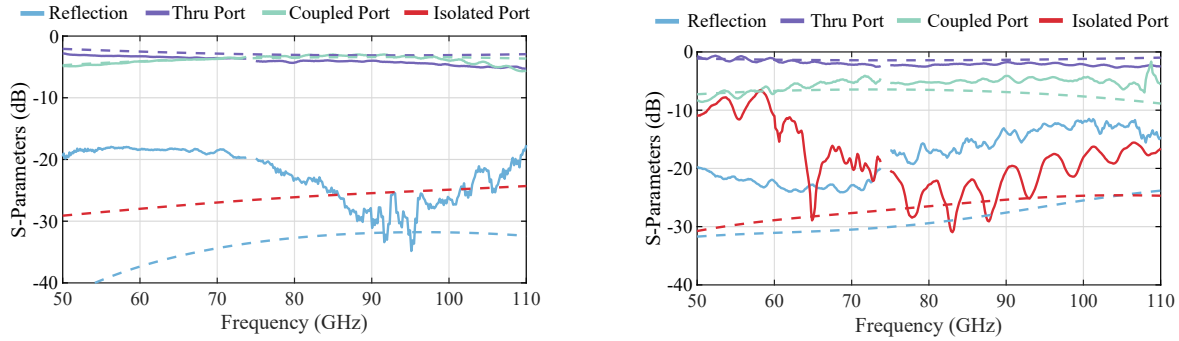


Figure 6.5: Measured (solid) and simulated (dashed) *S*-parameters of (a) uniform and (b) nonuniform Lange couplers. Note that the isolation was not measured in (a) due to limited area for a 3-port breakout structure.

The Lange coupler in Fig. 6.4b is designed as a nonuniform coupler, with less coupling in the forward-path amplifier branch. This reduces the coupler's impact on receiver noise figure. Approximately -1.5 dB of the signal is delivered to the "thru" port (P1 to P2) and -6 dB to the "coupled" port (P1 to P3). Measured and simulated *S*-parameters of the nonuniform Lange coupler are displayed in Fig. 6.5b. The "thru" and "coupled" paths are closer in magnitude than designed in W-Band, but follow simulated values at V-Band. Simulated isolation is 28 ± 3 dB across the band, but the measured isolation is up to 20 dB higher.

By inserting the simulated values at 80 GHz for the distributed amplifier and uniform coupler into (6.1) and (6.2), the predicted reverse and forward isolation for the first circulator are approximately:

$$I_{\mathrm{R}} = 3\,\mathrm{dB} + 20\,\mathrm{dB} + 3\,\mathrm{dB} = 26\,\mathrm{dB} \tag{6.4}$$

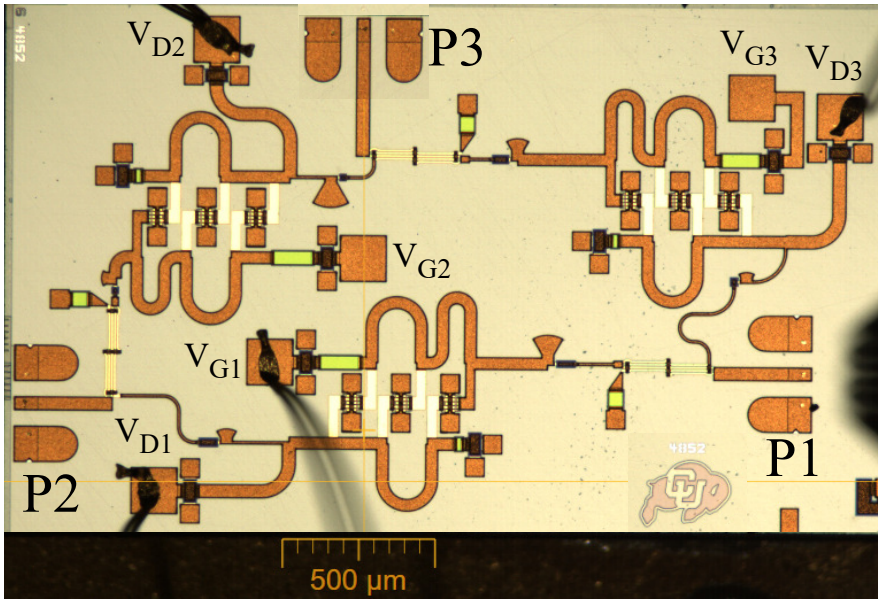
$$I_{\mathrm{F}} = 3\,\mathrm{dB} - 5\,\mathrm{dB} + 26\,\mathrm{dB} - 5\,\mathrm{dB} + 3\,\mathrm{dB} = 22\,\mathrm{dB} \tag{6.5}$$

Similarly, the simulated values of the cascode and nonuniform coupler can predict the isolation. The estimated values at 70 GHz are:

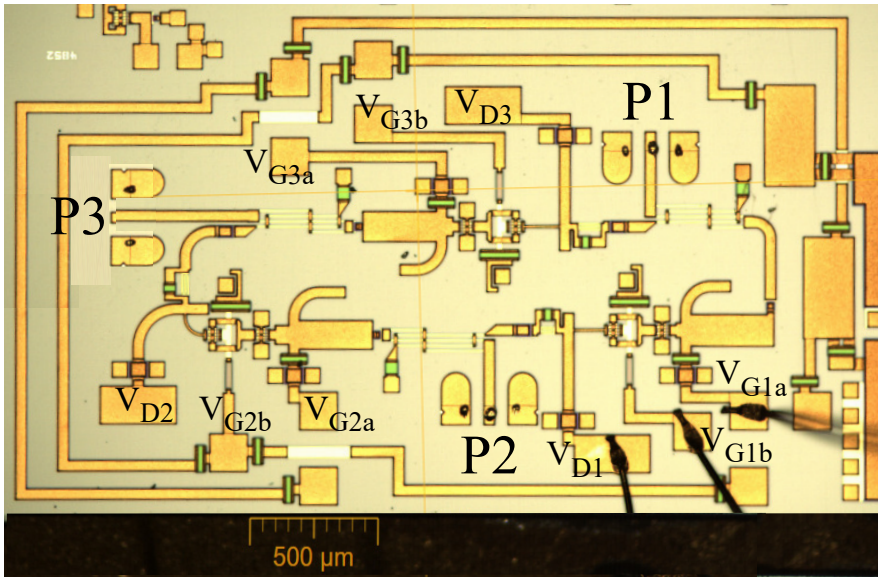
$$I_{\mathrm{R}} = 1.5\,\mathrm{dB} + 27\,\mathrm{dB} + 6\,\mathrm{dB} = 34.5\,\mathrm{dB} \tag{6.6}$$

$$I_{\mathrm{F}} = 1.5\,\mathrm{dB} - 5\,\mathrm{dB} + 28\,\mathrm{dB} - 5\,\mathrm{dB} + 6\,\mathrm{dB} = 25.5\,\mathrm{dB} \tag{6.7}$$

In both circulators, forward isolation is significantly lower than reverse, exacerbated by a reduced coupler isolation in measurement compared to simulation, seen in Fig. 6.5. Overall circulator isolation is limited by the lesser of the two paths, determined whether the quantity L_R from (6.1) or $L_i - 2G$ from (6.2) is greater. From equations (6.4)–(6.7), it is evident that overall isolation is limited by I_F in both circulators. However, bias switching off the unused amplifiers reduces this quantity significantly, leading I_R to dominate overall isolation in BSCM. Bandwidth will also increase in this mode, as amplifier gain and coupler isolation is reduced at the edges of the band.



(a)



(b)

Figure 6.6: Photographs of active circulator MMICs with (a) traveling-wave amplifiers (Circulator 1) and (b) cascode amplifiers (Circulator 2). The overall chip sizes are approximately 2.8 mm × 1.6 mm in (a) and 3.3 mm × 1.9 mm which includes the outer biasing lines in (b).

6.2 Measurements

The two circulator MMICs are characterized in small-signal operation, as well as compression and in terms of noise that they add to a front end. The circulator MMICs are mounted on a gold-plated copper molydenum (CuMo) carrier. The dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for stability. The dc gate pads of the three devices are tied together while the bias of each amplifier is applied independently to enable turning different paths *on* or *off*.

6.2.1 Small-Signal Performance

For small-signal measurements, the circuits are probed on a Summit 9000 probe station with 100-μm pitch GSG probes. Calibration is performed on wafer with a Cascade Microtech W-band impedance standard substrate (ISS). Coefficients are retrieved from the probe manufacturer and the ISS to perform SOLT calibration. The circuits characterized using an HP8510C Vector Network Analyzer with V-band and W-band extender heads.

Small-signal characterization across V- and W-bands for the two circulators is presented. The gates of each amplifier in both circulators are tied together, while only one drain is biased in the forward path in BSCM, and all three together in FCM. Figures 6.7 and 6.9 display the small-signal *S*-parameters for each circulator in one orientation. In reference to Fig. 6.1, *Tx* is connected to Port 1, with Path 1 connecting to the output *Ant* at Port 2. The isolated path is from Port 1 to Port 3 (*Tx*-*Rx*), i.e. Path 3 in reverse. For this orientation, $|S_{11}|$, $|S_{21}|$, and $|S_{12}|$ are plotted across frequency. The insertion loss includes loss of two Lange couplers, measured to be between 1 and 6 dB (Fig. 6.5). Additionally, the amplifiers are biased near pinch off to maximize isolation rather than forward gain, as discussed in Section 6.1. While only one set of forward, reverse, and match *S*-parameters are plotted, a 3×3 scattering matrix describes the performance of this 3-port circuit. The individual path characteristics differ slightly due to differences in matching networks and interconnects that required asymmetric layout for connecting the entire structure in a ring.

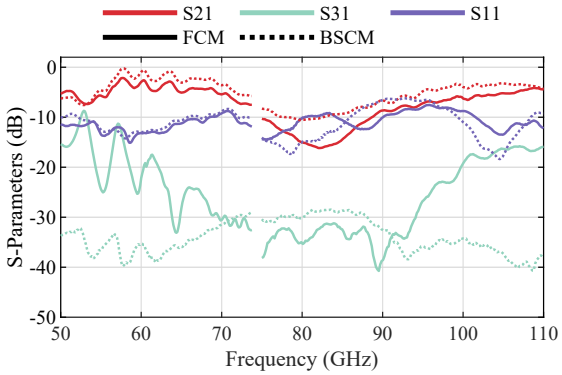


Figure 6.7: Measured small signal characteristics of distributed circulator in FCM and BSCM. The circuit is biased at a 12 V drain voltage with 130 mA drain current.

6.2.1.1 Distributed Circulator

The bandwidth is defined where both the small signal isolation is greater than 15 dB and $|S_{21}|$ is above -10 dB averaged across the three paths. In FCM the circulator is operational from 63–93 GHz. In BSCM, the circulator range of operation is extended significantly from 50–110 GHz, covering all of V- and W-band. Over this frequency range, an average of $|S_{11}| = -10.7$ dB, $|S_{21}| = -6.3$ dB, and $|S_{12}| = -31.1$ dB are measured.

The small-signal isolation for each path is defined as follows:

$$I = 10\log\left[\frac{P_2/P_1}{P_1/P_2}\right] = 20\log|S_{21}| - 20\log|S_{12}| \tag{6.8}$$

The measured and simulated isolation are plotted in Fig. 6.8. When operating in FCM, isolation averaged across the three states ranges from 15 dB to 30 dB between 63–93 GHz. In BSCM, isolation ranges from 19 dB to 30 dB between 50–100 GHz. In comparison, the simulated isolation ranges from 14 dB to 21 dB across the entire band, around 10 dB lower than measured for the BSCM. Discrepancies between measurement and simulation are believed to result from reduced Lange coupler isolation compared to the model.

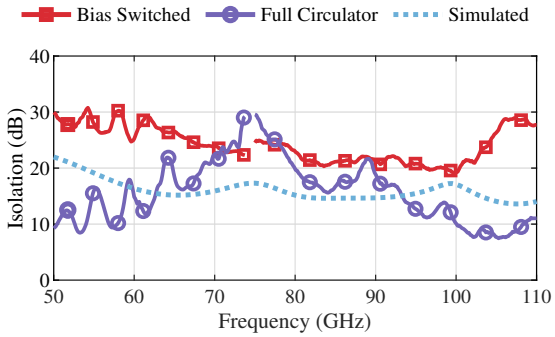


Figure 6.8: Comparison of measured and simulated isolation for Circulator 1. Circulator operation in both BSCM and FCM are plotted. Simulated isolation does not change between the two modes.

6.2.1.2 Cascode Circulator

Small-signal characterization of the cascode circulator is performed at a bias point of $V_{DD} = 12\,\text{V}$ with a drain current of 40 mA. The S-parameters are plotted in Fig. 6.9, comparing the measured results of each path. In the forward path, $|S_{21}| > -11\,\text{dB}$ for each amplifier in the frequency range 45-81 GHz when all amplifiers are on. This range is increased to 45-96 GHz in BSCM. Measured and simulated isolation for the cascode circulator is displayed in Fig. 6.10. In FCM, the isolation ranges from 15-32 dB across the three paths, and is increased to 21-35 dB up to 107 GHz in BSCM.

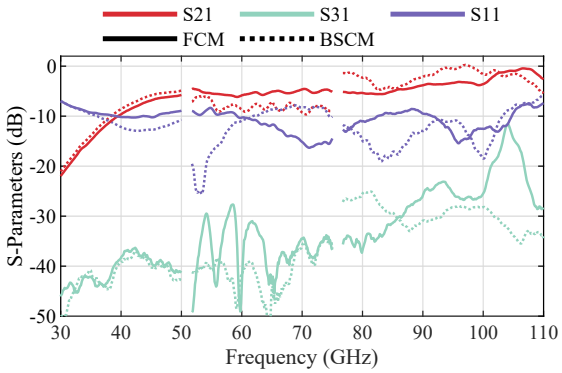


Figure 6.9: Measured small signal characteristics of the cascode circulator in FCM and BSCM. The circuit is biased at a 12 V drain voltage with 40 mA drain current.

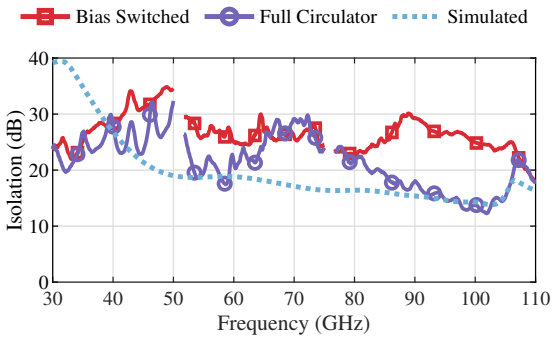


Figure 6.10: Comparison of measured and simulated isolation for Circulator 2. Circulator operation in both BSCM and FCM are plotted. Simulated isolation does not change between the two modes.

For both circulators, isolation and bandwidth are improved in BSCM compared to FCM where the isolation is limited by the forward gain as predicted in Section 6.1. Turning off the unused amplifiers causes the value of the expression in (6.2) to increase, leaving isolation to be dominated by the reverse path.

6.2.2 Large-Signal Performance

In the large-signal setup, a Ka-band source feeds a Ka-band amplifier, and the output is then upconverted to W-band through a passive frequency multiplier and filtered before it is fed into a W-band amplifier. A small portion of the signal is then coupled off for an input power measurement. At the output, a portion of the signal is coupled off for an output power measurement while the remaining power is dissipated through attenuators. The passive components between the two W-band power meters are measured independently and deembedded. This setup unfortunately does not allow for large-signal measurements below 75 GHz. In addition, large-signal isolation could not be measured due to a combination of the limited sensitivity of the W-band W8486A Power Sensors (-30 dBm) and maximum output power of the W-band source.

This characterization is performed through one branch of the circulator in BSCM. Two W-band driver amplifiers are cascaded to generate an input power of 20 dBm at the device plane of Circulator 1. Under these conditions, the circulator remains linear for a majority of the power sweep displayed in Fig. 6.11a. The 1 dB compression point is measured at an input power of 16 dBm, as compared to 20 dBm in simulation. The second circulator requires only one W-band power amplifier for large-signal characterization as it saturates

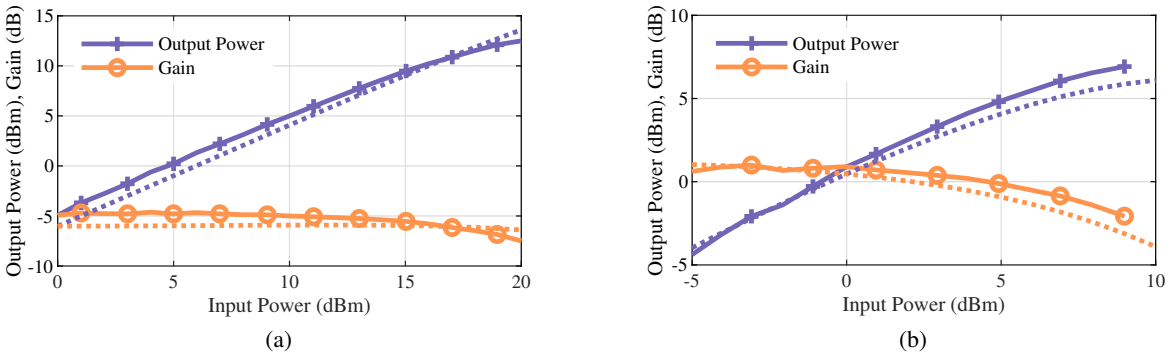


Figure 6.11: Measured (solid) and simulated (dashed) comparison of output power and gain vs input power for (a) distributed amplifier circulator at 92 GHz and (b) cascode amplifier circulator at 101 GHz. For each case, only amplifier 1 is biased at 12 V drain voltage. The distributed amplifier is biased with a quiescent drain current of 40 mA and the cascode amplifier with 50 mA.

at a lower input power. Large-signal gain and output power for the cascode circulator are plotted at 101 GHz in Fig. 6.11b. Measured 1 dB compression point is measured at approximately 5 dBm input power, following the trend predicted by simulation. This could be improved in future designs by increasing the device size of the cascode transistor. Simulations show that the power measured at the source of the cascode device is ≈ 4.5 dB higher than the power measured at the input to the amplifier, leading the authors to believe that it is compressing before the first device.

6.2.3 Noise Characterization

The amplifier in the circulator adds noise to the receive path before the signal reaches an LNA, so the noise figure of the circulator must be taken into consideration. The noise figure of the active circulator is analyzed across the W-band frequency range with a Maury ultra-fast noise parameter measurement system. The WR-10 (75 – 110 GHz) system includes a noise diode, RF switches, a PNA-X with frequency extenders and a noise figure meter, a source tuner, a noise receiver comprised of a commercial LNA and mixer down-converter, and GGB picoprobes. Calibration of the system included an in-situ characterization of the source tuner at a fixed set of impedance states and characterization of the noise receiver chain. Measurements of the active circulator provided noise parameters across the W-band frequency band. The 50 Ω noise figure of the circulator was then calculated from the noise parameters. This rigorous approach to characterizing the

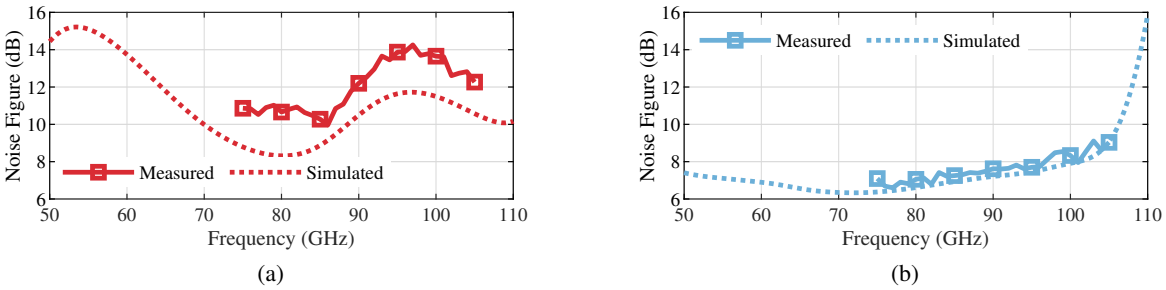


Figure 6.12: Measured (solid) and simulated (dashed) noise figure of each circulator across W-band. For each case, only amplifier 1 is biased at 12 V drain voltage. (a) Distributed circulator with 40 mA drain current. (b) Cascode circulator with 17 mA drain current.

W-band noise figure enabled the very good agreement between measurements and simulations illustrated in Fig. 6.12. Only the forward path amplifier is biased in this measurement (BSCM). The distributed amplifier circulator noise figure in Fig. 6.12a matches the trend predicted by simulations, but is approximately 1-2 dB higher across the band. In comparison, the measured noise figure of the cascode circulator in Fig. 6.12b is within 1 dB of the simulated value. The cascode FET does not have a designated model in this PDK which could explain the discrepancy between Figs. 6.12a and 6.12b. In addition, Circulator 1 includes a uniform 3 dB Lange coupler which degrades the noise figure compared to the nonuniform Lange coupler in Circulator 2 that has a 1.5 dB coupling factor to the cascode amplifier.

6.3 Conclusion

This chapter presents two active MMIC circulators designed in a ring topology consisting of three amplifiers and three Lange couplers. The first circulator employs traveling wave amplifiers and uniform Lange couplers, while the second uses cascode amplifiers to improve reverse isolation and nonuniform Lange couplers to improve noise figure while maintaining the same insertion loss. The first circulator operates from 63–93 GHz in FCM, consuming 1.56 W of dc power, with an average isolation between 15–30 dB. In BSCM, bandwidth is extended to 50–110 GHz with an average isolation between 19–30 dB and insertion loss of 6.3 dB. The second circulator operates from 40–95 GHz in FCM, consuming 0.48 W of dc power, with an average isolation between 15–32 dB and insertion loss above -10 dB averaged across the

Table 6.1: Comparison of State of the Art millimeter Wave Circulators

Reference	Technology	Topology	Frequency (GHz)	Iso (dB)	P_{1dB} (dBm)	NF (dB)
[133]	Ferrite	Microstrip Junction	95.5 - 97.5	>20	-	-
[134]	Ferrite	Waveguide Junction	92-100	>20	-	-
[136]	CMOS	Bidirectional Amplifiers	62-75	18	-	9
[137]	SiGe	Quasi-Circulator	76-80	>16	1	-
[138]	InAlAs/InGaAs/InP	Quasi-Circulator	35-50	30	-	-
[139]	GaAs	Quasi-Circulator	75-85	10-20	-	-
[140]	GaAs	Quasi-Circulator	80.8-89.3	>18	-	-
[126]	GaAs	Amplifier Ring	8-12	20	-	-
[147]	GaN	Quasi-Circulator	75–100	30	-	7
This Work (FCM/BSCM)	**GaN**	**Traveling-Wave Amplifier Ring**	**63–93 / 50–110**	**10–30 / 19–30**	**16**	**10.0**
This Work (FCM/BSCM)	**GaN**	**Cascode Amplifier Ring**	**40–95 / 40–107**	**15–32 / 21–35**	**5**	**6.6**

three paths. In BSCM, bandwidth is extended to 107 GHz with an average isolation between 21–35 dB and $|S_{21}|$ above -10 dB averaged across the three paths. Both circulators are well matched across the entire bandwidth and demonstrate a high degree of linearity with a 1 dB compression points of 16 dBm at 92 GHz and 5 dBm at 101 GHz for the distributed and cascode circulators, respectively.

In summary, two active GaN MMIC millimeter-wave broadband circulators are presented in two reconfigurable operation modes, showing isolation from 50–110 GHz. A comparison to other selected topologies shown in Table 6.1 indicates a wider bandwidth, higher isolation and higher compression level than other demonstrated devices. Due to the high-power handling of GaN and the demonstrated relatively low noise figure in the receive path, integration with a PA in the transmit path and an LNA in the receive path would be interesting. The active circulators discussed in this chapter can be further compared to commercial products having the same frequency of operation. Several ferrite waveguide circulators are offered by companies such as Eravant. The products offered are passive, have lower insertion loss, typically handle power levels >1 W, and have comparable isolation to the circuits presented in this chapter. However, they are far more narrowband in nature and cannot be integrated on chip. For example, the SNW-7638130818-12-C1 E-Band Waveguide Junction Circulator operates from 76-81 GHz with 0.8 dB of insertion loss and 18 dB of

insertion loss. The designs presented here emphasize wideband performance and employ appropriate amplifier topologies with low gain. However, performance metrics such as insertion loss, isolation, and power consumption could be improved with narrowband or multistage amplifier designs. Nonetheless, forward gain is limited by equation 6.2, at least in FCM where the amplifier gain reduces forward isolation. The contributions of this chapter are described in [128, 148, 149].

Chapter 7

Higher Level of Transceiver Millimeter-wave Integration

In this chapter, higher levels of integration in GaN are studied, towards a full transceiver on a chip. The advancement of millimeter-wave GaN process and yield shows promise for successfully integrating multiple components from previous chapters. Generally, silicon processes have demonstrated higher integration levels with the ability to formulate circuits that operate both in the analog and digital domain, e.g. in CMOS [150, 151] or SiGe BiCMOS [97, 152]. However, they suffer from lower output powers. Front end T/R modules assembled from individual chips have also been demonstrated at W-band, e.g. [153–155], requiring multi-chip packaging. Single-chip W-band front ends have been demonstrated as early as the 1990s in GaAs [156, 157], and recently in InP [158]. Integrated GaN modules are now coming into play; several Ka-band GaN front ends have been demonstrated, e.g. [159–161], along with heterodyne W-band receivers [162, 163]. A handful of narrowband GaN transceivers have been published at W-band [164–166]. In this chapter, both full and half-duplex monolithically integrated GaN transceivers are presented covering all or most of W-band.

7.1 Half-Duplex Front End

In this section, a monolithically integrated half-duplex W-band transmit/receive (T/R) front end is discussed. The front end is implemented in the HRL T3 process, described in depth in previous chapters, as well as in [44]. The design of the front end MMIC along with its individual components are discussed in [29, 66, 120], but will be summarized in the following section.

7.1.1 T/R Front End Chip Design

A circuit block diagram of the front end is displayed in Fig. 7.1. The front end is assembled on chip partly with existing components, e.g. a power-combined multi-stage balanced PA with 15–20 dB small signal gain across W-band [29]. A single-pole double-throw (SPDT) switch is slightly modified from [120], providing 17.5–20 dB isolation in the OFF state and 1–2 dB insertion loss in the ON state across W-band. Power handling of the switch is high enough that no compression was observed in simulation or measurement up to 20 dBm input drive in [120]. A driver and three stage LNA are also designed and added to the system. The design of these components are discussed in depth in [66]. In summary, the driver amplifier is designed to 50 Ω at the both input and output, with the same operating bandwidth as the balanced amplifier. Biasing of the driver is also the same as the primary amplifier to reduce the number of dc connections required. The LNA is implemented with three single-ended HEMT stages. The first stage input matching network transforms the 50 Ω impedance from the SPDT to the optimum noise match, while the second two stages are designed to maximize gain.

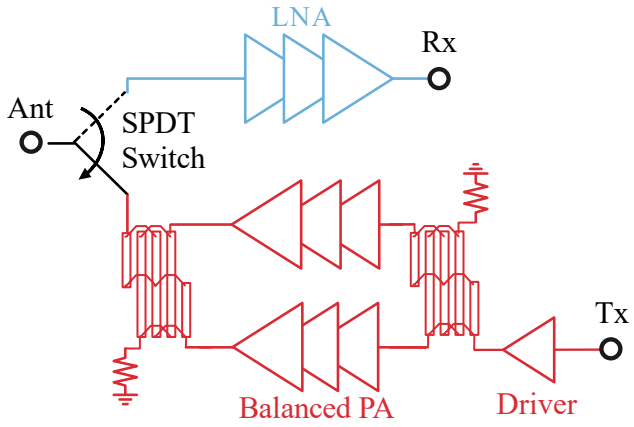


Figure 7.1: Schematic of half duplex integrated front end.

A picture of the die is displayed in Fig. 7.2. The three RF ports are labeled along with the PA, LNA, and SPDT. The MMIC is mounted onto a CuMo carrier along with off chip bypass capacitors. Bond wires are connected to the LNA dc ports. These are tied together off chip to reduce the number of dc inputs.

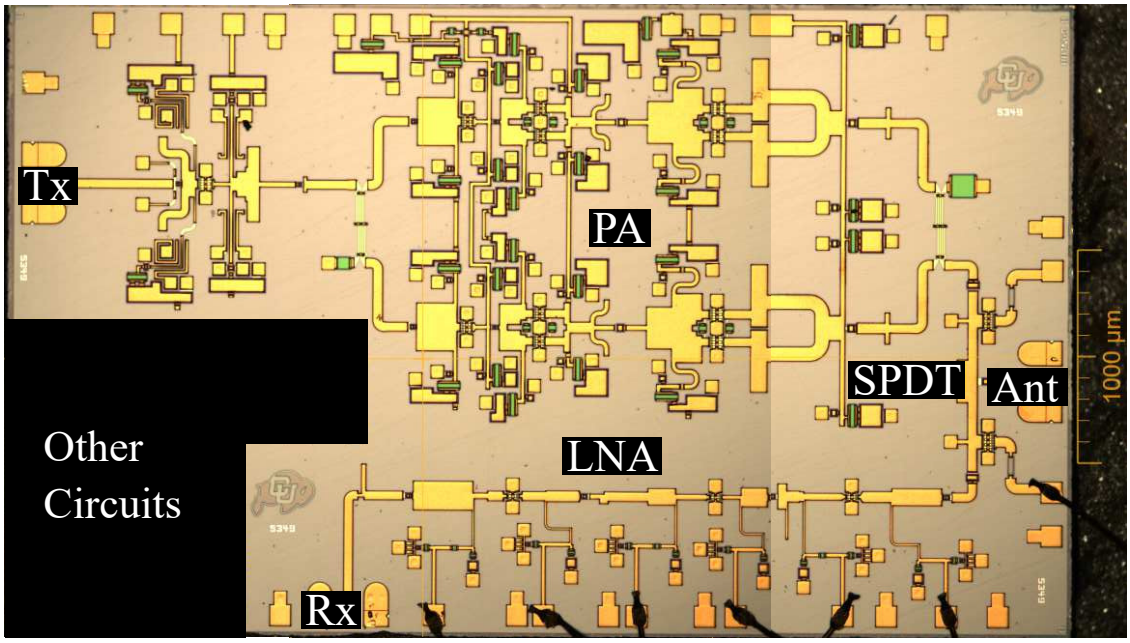


Figure 7.2: Picture of half duplex integrated front end MMIC. The die has dimensions of 5 mm $\times$ 3 mm.

7.1.2 Measurements

An HP8510C VNA with V- and W- band frequency extenders is used for on-wafer small-signal measurements. Two 100 μm GSG probes are used to land onto the MMIC on a Summit 9000 probe station. The front end MMIC is then measured in both transmit and receive operation. Measurement results compared to simulations are shown in Fig. 7.3a for the transmit path and in Fig. 7.3b for the receive path. A measurement discontinuity at 75 GHz arises from two different wave-guide band measurements. In the transmit path, the peak small-signal gain is 25 dB at 75 GHz, sloping down to 19 dB at 108 GHz. The receive path shows a peak small-signal gain of 22 dB at 77 GHz with over 16 dB gain from 70–105 GHz. The measured and simulated $|S_{21}|$ agree within 1.5 dB across the entire W-band. The simulated and measured results in the transmit path deviate more, especially below 70 GHz, since this path was designed to impedance under large-signal conditions.

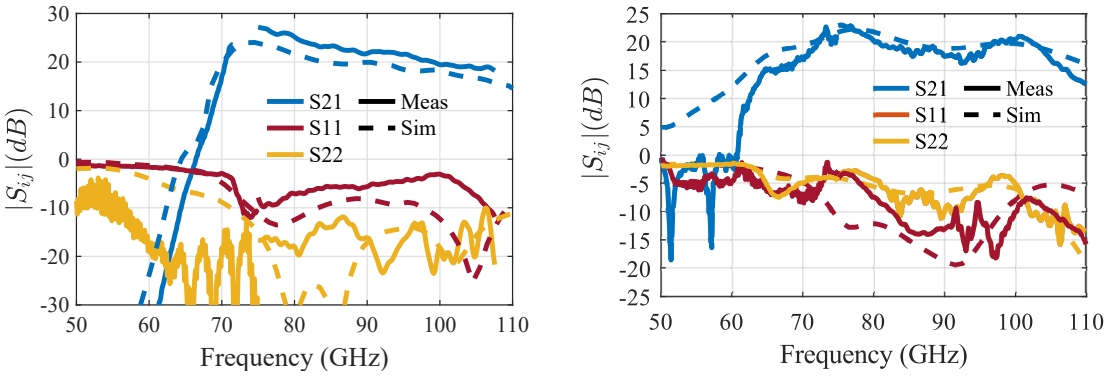
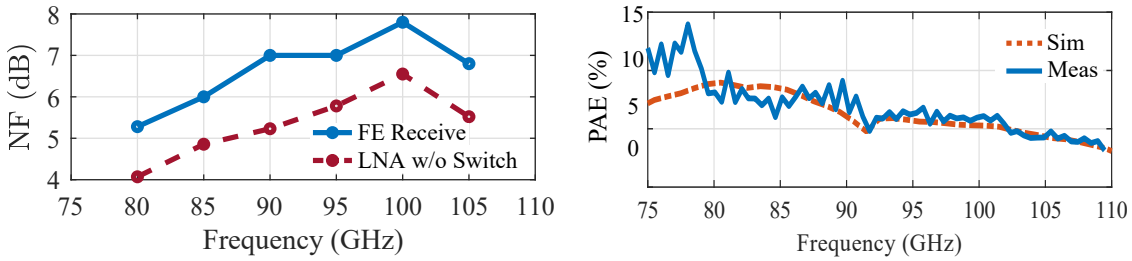


Figure 7.3: Measured (solid) and simulated (dashed) S-Parameters of half duplex front end in (a) receive and (b) transmit mode.

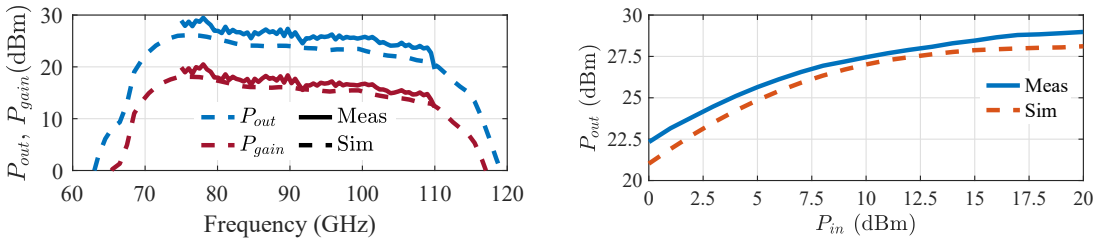
On-wafer 50 Ω noise figure (NF) measurements were collected for the LNA using a custom scalar NF test bench described in depth in [66]. The NF measurements involve calibration with a WR-10 noise diode and receive chain individually. The NF of the LNA is determined by the Friis formula with the transducer gain and NF of the fixtures calculated from their respective S-parameter measurements, while the transducer gain of the LNA is calculated from a calibrated S-parameter measurement. As a result of this complex setup, only measurements at 80, 85, 90, 95, 100 and 105 GHz are conducted. Measured NF of the receive path are shown on Fig. 7.4a along with de-embedded NF of the LNA alone, based on measured switch loss from [120]. The measurements show a minimum NF of 5.2 dB at 80 GHz and a peak NF of 7.8 dB at 100 GHz. These results are consistent with measured noise parameter data of individual millimeter-wave GaN HEMTs [167].



(a) (b)

Figure 7.4: (a) Measured noise figure with and without SPDT. (b) Measured (solid) and simulated (dashed) transmit path PAE.

On-wafer large signal measurements are conducted with a power-calibrated scalar test bench. To reach up to 20 dBm of input power at the DUT, a custom W-band solid-state PA is driven by a QPI-W01820-H4W02 W-band power amplifier. An HP83650A sweeper generates a 25-36.6 GHz CW signal. After this, a Ka-band QPW-18402020-J0 power-amplifier drives a passive QPM-93003W diode tripler followed by a QFL-B4SW00 low-pass filter to provide an up-converted 75–110 GHz CW signal to the W-band test-bench power-amplifiers. W-band power meters are connected to capture scalar measurements, and the passive interconnects are de-embedded using individually measured S-parameters.



(a) (b)

Figure 7.5: (a) Measured and simulated output power and power gain of the front end Tx path with 9 dBm input drive. (b) Measured (solid) and simulated (dashed) output power of the MMIC at the Ant port at 92 GHz with swept input drive.

Two separate large signal measurements are conducted on the transmit branch of the MMIC. The cus-

tom solid-state PA operates in the 90–95 GHz band and is used to conduct single frequency power sweeps at 92 GHz providing 0 to 20 dBm at the plane of the DUT. The QPI-W01820-H4W02 W-band power amplifier operates from 75-110 GHz and is used to measure large-signal performance across the entire W-band at a power of 9 dBm at the DUT. Power added efficiency (PAE) is plotted across frequency in Fig. 7.4, reaching a maximum of 14% at 78 GHz in the transmit path. In Fig. 7.5a, output power and gain are plotted against frequency, with >29 dBm at 75 GHz measured at an input power of 9 dBm, gently sloping down to 24 dBm at 108 GHz. The measurement of the 0–20 dBm power sweep at 92 GHz is shown in Fig. 7.5b.

7.2 Full-Duplex Front End

In-band full-duplex (IBFD) systems which allow for improved spectral efficiency [16], as well as RF convergence [13] [23], allow for maximal use of the electromagnetic spectrum. However this leads to high self-interference that desensitizes the receiver, due to coupling between the transmit (Tx) and receive (Rx) signals. In order to recover the sensitivity of the receiver, self-interference cancellation (SIC) can be implemented. This can be done in the propagation domain, analog domain, and digital domain as discussed in [15]. The level of SIC is determined by the transmit output power, coupling between Tx and Rx, and the receiver noise floor. Typically, a combination of SIC techniques is required for sufficient cancellation.

Analog cancellation networks that improve receiver sensitivity can be implemented in a number of ways, e.g. the commonly used ferrite circulators [122], which require bulky external magnets and are not monolithically integrated. Alternatively, active circulators [128] and quasi-circulators [168] can be implemented on chip. Analog SIC networks have been demonstrated in [169] where multiple couplers are stacked at the antenna port, and [170] which utilizes the terminated port impedance of a single coupler. To allow monolithic integration and avoid power handling limitations due to transistors in the signal path, an analog self-interference cancellation network with three connected Lange couplers and with added tunablity at the isolated port on two of the couplers is presented.

7.2.1 Design

The front end is designed in the HRL T3 process, providing state-of-the-art efficiency and power density in the millimeter wave regime [44, 45]. Referring to Fig. 7.6, a three-stage power amplifier (PA) similar to [29] is integrated with a three-stage low noise amplifier (LNA) and a three-port self-interference cancellation network (SIC) network that connects the Tx and Rx paths to a single antenna port. The design of these three main components is detailed next. The SIC network is also fabricated separately and its performance is characterized.

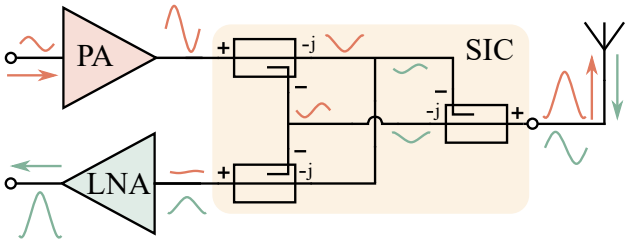


Figure 7.6: Block diagram of IBFD 3-port front end integrated on a single W-band GaN die. The self-interference cancellation (SIC) network suppresses leakage signal from the PA to the LNA by 30 dB.

7.2.1.1 Analog SIC Network

The layout and schematic of the broken out SIC network are displayed in Fig. 7.7. Three identical Lange couplers are interconnected with transmission lines including a cross-over, and two of the isolated coupler ports are terminated in tunable loads while the third isolated port is terminated in a matched resistor. A transmitted signal from Tx is split evenly by hybrid coupler C_1, with a 90° phase offset between the through and coupled ports. Each signal is then split again at a T-junction, and recombined independently by couplers C_2 and C_3. The through and coupled ports from coupler C_1 connect to the same ports of C_2. They combine destructively at Rx and constructively at the isolated port terminated by Z_2. The connection to C_3 however is opposite that of C_2, so the signals combine constructively at the antenna port and destructively at the isolated port of C_3 terminated by Z_0. In principle, the transmitted signal experiences a 3 dB loss between Tx and Ant. In receive mode, this network works in reverse. The signal from the antenna combines constructively at Rx and Tx, and destructively at Z_1 and Z_2. Thus, a 3 dB loss is also experienced between

Ant and Rx. The waves drawn in Fig. 7.6 display the transmit and receive signals with their appropriate phase through the SIC.

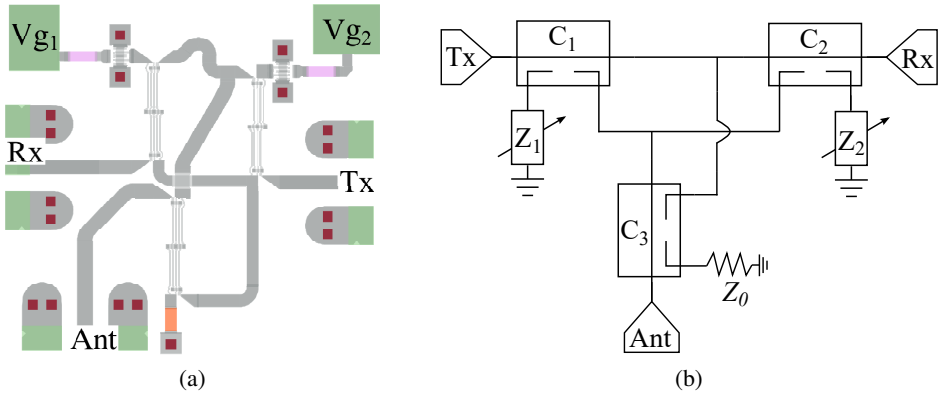


Figure 7.7: (a) Analog SIC network layout with a size of 1.1 mm $\times$ 1.1 mm, and (b) schematic showing the tunable impedances at the coupler isolated ports.

While the Lange couplers are wideband, the bandwidth of the SIC network is limited by the interconnects. Moreover, signals cannot experience the same phase differences without additional meandering of the transmission lines at the nodes between couplers. This challenge is exacerbated at W-band, whereby a 300 μm transmission line is approximately $\lambda/4$ at 90 GHz in the T3 process. To accommodate for proper phasing with unequal routing distances, the length between C_1 and C_3 is approximately twice as long as the connections between C_2 and C_3, as displayed in Fig. 7.7a. The receive path connects to C_2 with a shorter path length, minimizing the impact on noise figure due to loss, while the transmit path connects to C_3.

Tunable loads are added onto the isolated ports of C_1 and C_2 to control the combining phase at the ports and enhance the Tx-Rx isolation over a broader bandwidth. The tunable load is realized using a source grounded HEMT connected at the drain. The gate voltage of a $4 \times 37.5\,\mu$m device is tuned to adjust the impedance seen by the coupler. A plot of the simulated tunable range is displayed in Fig. 7.8. Each trace shows the impedance at a different frequency looking into the drain as gate voltage is swept from -1 V to +0.5 V. When the HEMT is pinched off, it appears purely capacitive. With the gate voltage at approximately +0.2 V, the impedance is purely real across frequency. At this bias point, the impedance is $\approx 30\,\Omega$ and is reasonably well matched to the 50 Ω coupler. Beyond this voltage, the HEMTs appear inductive.

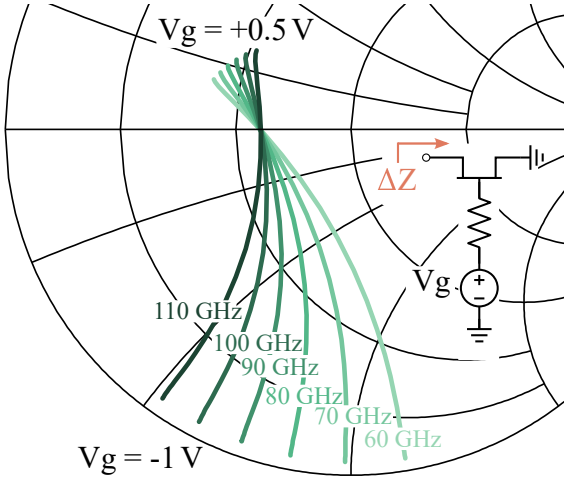
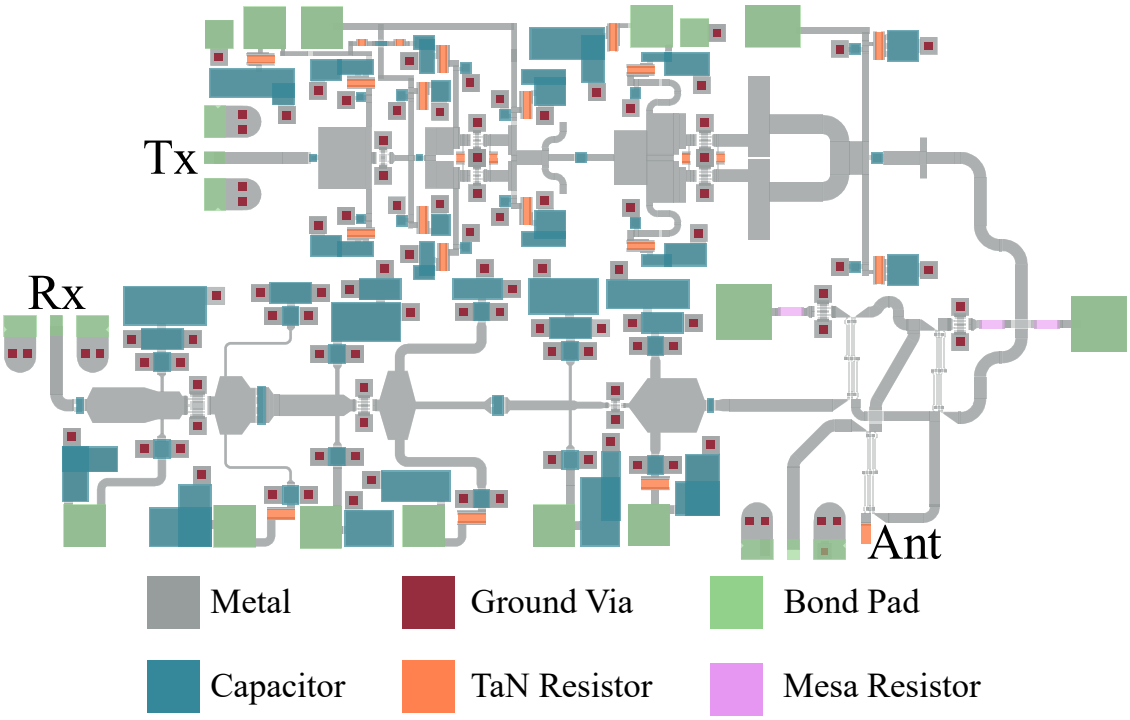


Figure 7.8: Simulated impedance variation across gate bias from -1 V to +0.5 V looking into drain of a $4 \times 37.5\,\mu$m device from 60 to 110 GHz.

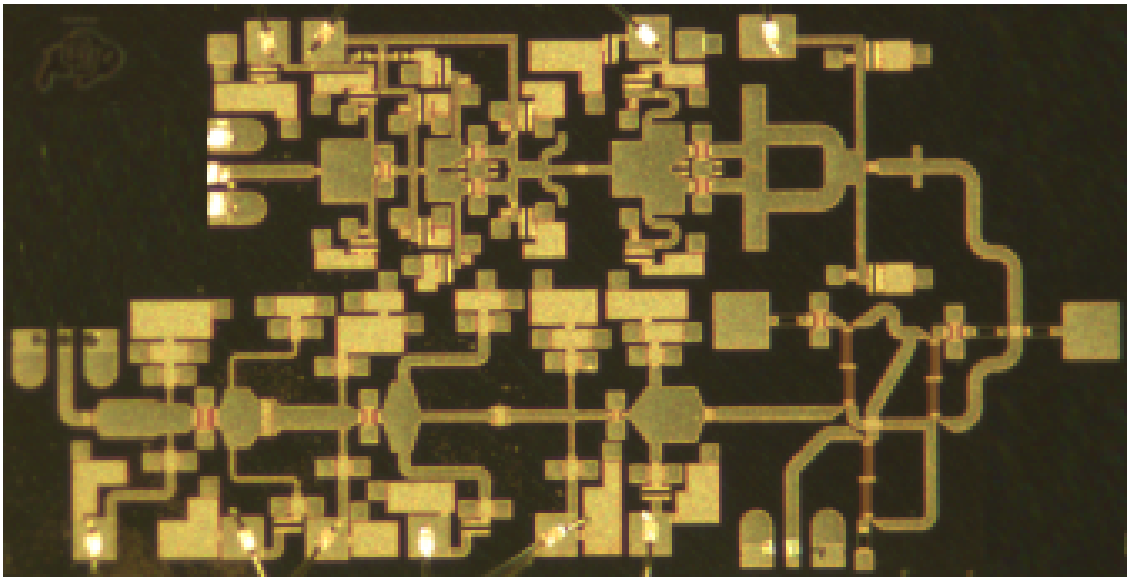
7.2.1.2 Front End Integration

The layout of the full chip is displayed in Fig. 7.9a. The three-stage PA is at the top, with the input denoted by Tx GSG and the output fed to the SIC network, shown at the bottom right where the output/input of the antenna is denoted by Ant GSG. The three-stage LNA is in the bottom left, where the output Rx GSG is rotated for layout considerations. A photograph of the $4 \times 2\,\text{mm}^2$ front end MMIC is displayed in Fig. 7.9b. The reactively-combined PA has over 12 dB of simulated gain from 75 to 110 GHz, and 24 dBm of output power at the 3 dB compression point [103].

Due to the full-duplex implementation, the peak PA output power and minimum SIC is of concern when considering compression of the LNA, which degrades the linearity of the receive chain. A high compression level (high IP3) is a benefit of GaN LNAs [167] further making full Tx-Rx integration advantageous.



(a)



(b)

Figure 7.9: (a) Layout of integrated PA, LNA and SIC network. (b) Photo of the 4 mm $\times$ 2 mm GaN MMIC die.

The 75–100 GHz LNA includes three stages to achieve sufficient receiver gain, accounting for ap-

proximately 3 dB loss in the SIC network. While the decrease in gain can be overcome by additional stages, the noise figure (NF) suffers. To minimize NF of the LNA, all validated device models in the T3 process are analyzed for their minimum noise characteristics. The $2 \times 25\,\mu$m device, which has the smallest NF among the four standard devices, is chosen for the first LNA stage. In stages 2 and 3, the next largest validated devices of $4 \times 37.5\,\mu$m and $6 \times 50\,\mu$m are utilized to maintain linearity. To ensure stability of the LNA, bypass capacitors on the bias line are added along with series resistors in the gate paths. The LNA has a NF ranging from 3.3 dB to 3.8 dB from 75 to 100 GHz, and a simulated input P1dB of 16.5 dBm at the center of the band (87.5 GHz).

7.2.2 Measurements

The front end is mounted on a gold-plated copper molybdenum (CuMo) carrier, and the dc pads are wire-bonded with 1-mil gold bond wire to off-chip capacitors for stability. The circuit is measured on a Summit 9000 probe station with 100-μm pitch GSG probes and characterized in small-signal operation from 75 GHz to 110 GHz using an HP8510C Vector Network Analyzer with W-band extender heads.

7.2.2.1 Analog SIC Network Characterization

The measured small-signal performance of the analog SIC network is shown in Fig. 7.10. Simulations of the SIC network are plotted for the control voltages on the two gates of 0 V. The self-interference cancellation between Tx and Rx is displayed in Fig. 7.10a for several gate voltages on the tunable loads. For each trace, a notch below -30 dB is tunable within the operating frequency of the front end. The interference cancellation is below 12.5 dB for the rest of the band. Gate voltages between 0 and 0.5 V are applied to translate the notch within the frequency range. The combination of voltages applied, as well as the notch bandwidth for each trace is displayed in Table 7.1. Simulation agrees well with measurement, fitting between the magnitude range of all measured traces.

The transmission between Tx-Ant and Ant-Rx is plotted in Fig. 7.10b. The shaded regions represent the range across bias when the voltages applied to two gate pads are changed between 0 V and 0.5 V. As predicted by simulation, the transmit path experiences greater loss due to the longer path length. A maximum

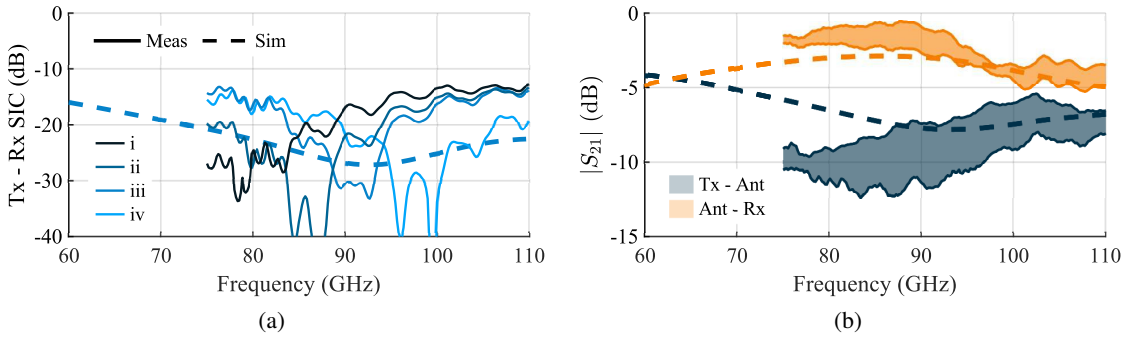


Figure 7.10: Measured (solid) and simulated (dashed) characterization of SIC network. Magnitude of S-Parameters for (a) Tx-Rx self-interference cancellation and (b) $|S_{21}|$ between Tx-Ant and Ant-Rx. For each path, the gate control voltage is varied from 0 to 0.5 V for both paths, showing the extreme values. In the simulations, the control voltage is held at 0 V.

insertion loss difference of 4.6 dB is measured between the two paths at 86 GHz, while they cross at 63 GHz when $|S_{21}| = -4.4$ dB. Simulations agree well with measurements above 90 GHz. Below this frequency, the simulated and measured difference in insertion loss between the two paths diverges.

Table 7.1: Gate bias voltages applied to tunable loads for a SIC notch < 30 dB

Trace	i	ii	iii	iv
V_{g1} (V)	0.5	0.5	0	0.4
V_{g2} (V)	0.25	0.15	0	0
Notch freq (GHz)	78 - 80	84 - 88	89 - 93	95 - 100

7.2.2.2 Full Tx-Rx Chip Characterization

The integrated front end is next measured in transmit and receive modes with the unused path biased off and terminated with an on-chip load. A resistor is included in the layout close to the GSG pad and bonded when needed to the microstrip, but are not shown in the layout for clarity. For each measurement and simulation, shown in Fig. 7.11 with solid and dashed lines, respectively, both tunable loads are biased at 0 V. The transmit path response is displayed in Fig. 7.11a. A small-signal gain ranging from 10.6 to 13.6 dB

is measured across 75 to 100 GHz, up to 5 dB higher compared to simulation. Note that we observe an increase in gain at the higher end of the band at 110 GHz. The measured return loss is less than 5 dB across the band.

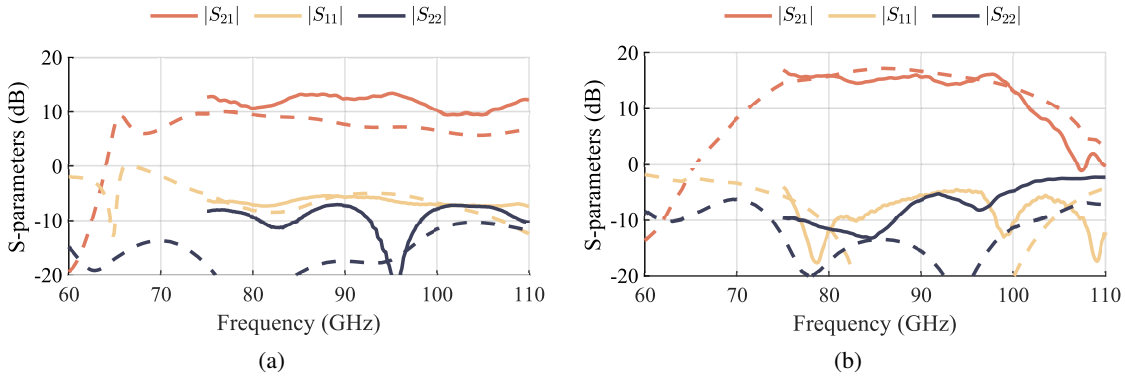


Figure 7.11: Measured (solid) and simulated (dashed) small signal characterization of front end (a) transmit path and (b) receive path.

The measured performance in receive mode is seen in Fig. 7.11b. Both simulations and measurements are performed with gate and drain biases tied together, with a drain voltage of 12 V and a combined drain current of 95 mA. The measurements show a small-signal receive gain of 17 to 14 dB from 75 to 100 GHz, in good agreement with simulation. The noise figure was not measured at this time. Simulations show a noise figure of 7 dB or less across the band for the integrated chip.

Table 7.2: Comparison of millimeter-wave GaN T/R single chip MMICs

Freq. (GHz)	Process Node (nm)	Topology (HD/FD)	Tx P_{out} (dBm)	Rx NF (dB)	Tx/Rx Gain (dB)	Ref.
32-36	60/100	HD	35	3.2	25/30	[160]
37-40	60/100	HD	34-35.5	3-3.5	23-25/14.5	[161]
71-77	130	HD	31.5	5.0	19-20/18-20	[164]
75-86	100	HD	>27	4.5	18-21/19-22	[165]
100-110	120	HD	30	6.0-6.4	11/21-22	[166]
75-110	**40**	**HD**	**29**	**5.2-7.8**	**19-25/16-22**	**This Work**
75-100	**40**	**FD**	**20***	**<7***	**11-14/14-17**	**This Work**

* Simulated Values

7.3 Conclusion

In summary, both full and half duplex W-band transceivers are presented. The circuits are compared to other published GaN T/R front ends in Table 7.2. The half-duplex front end [66, 171] is by far the most wideband of all MMICs, while still providing comparable output power, noise figure, and gain across the band. Meanwhile, the second presented chip is also very wideband and is the only full-duplex W-band GaN front end published to date in [147]. Its specified frequency range will also widen in the near future as V-band has not yet been characterized.

With these millimeter-wave GaN front-ends, opportunities to build and explore new applications are not in short supply. In the near term, future work includes characterizing the noise figure and linearity of the full duplex MMIC, as well as extending measurements to V-band. The MMICs can also be monlithically integrated with phase shifters for phased array applications [111], assembled heterogeneously with other technologies (MECA) [26], packaged into a wave-guide or with antennas [34, 155], or characterized with modulated signals, etc.

Chapter 8

Conclusions and Future Work

8.1 Thesis Results Summary

This thesis presents the design and integration of millimeter-wave circuits for GaN MMICs summarized in Fig 8.1. Specifically, designs covering Ka-band through W-band (27–110 GHz) are discussed. Beginning with element level design, several different circuits are detailed with increasing levels of integration as the chapters progress. After an introduction, bias line design is discussed in depth. This element is a requirement for any active circuit, and is often overlooked. Bias line architectures commonly used for low frequency design are tested for their limitations at high frequencies. From this study, it is determined that alternative methods should be used to optimize millimeter-wave circuits, often integrating bias lines into the design of matching networks.

Conclusions from the bias line element study lead to several chapters on component level design. Ka-band power amplifiers are first presented. Two 150 nm GaN processes are employed to test the scaling of efficiency techniques at Ka-band, such as harmonic termination and dual-drain voltage amplifiers. While the topologies do not boost efficiency as hoped in measurement compared to simulation, the studies provide useful information on the limitations of foundry models at the design frequencies. A comparative study on physics-based HEMT models is also performed on three single-stage amplifiers to test its validity. This analysis will help to improve these models and allow for additional scaling parameters within individual HEMTs for future process design kits.

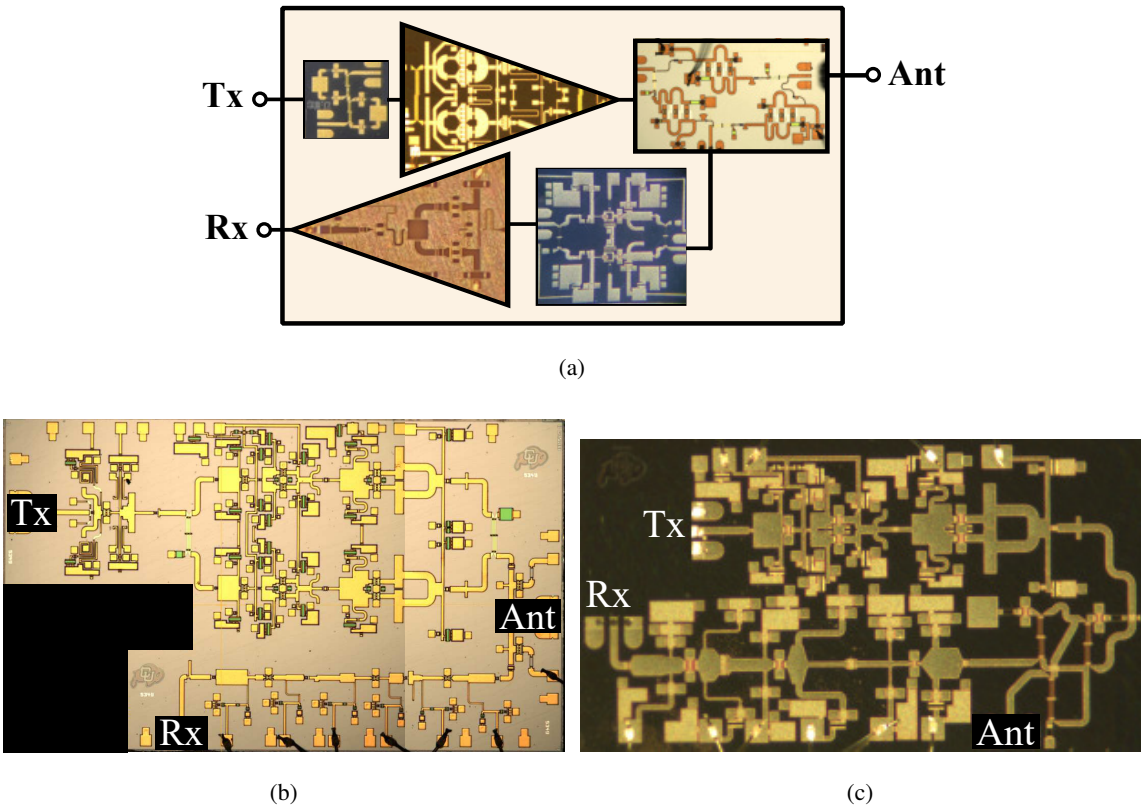


Figure 8.1: Progression of circuit complexity discussed in this thesis. (a) Hypothetical system proposed in Fig. 1.4 using circuits discussed in Chapters 2–6. (b) Half and (c) full duplex single-chip transceivers discussed in Chapter 7.

Many different control circuits are then presented. Wideband continuous reflective phase shifters are designed in the T3 40 nm GaN process covering all of V and W-bands (50-110 GHz). The phase shifters can impose a 90° shift from a single stage Lange coupler with two source-grounded HEMTs providing tunability. Cascading two of these stages provides 180° phase shift. Next, several different switches are presented, with operation across W-band. The primarily SPDT switches are designed in both the T3 and 90 nm Qorvo GaN processes. Finally, a wideband cascode amplifier isolator designed in T3 is presented. This circuit provides gain in the forward path and high reverse isolation from 46–102 GHz.

Subsequent chapters present the integration of components into front end systems. First, two active circulators are discussed. The circulators are designed in T3 and contain three amplifiers connected in a ring with three Lange couplers. The amplifiers contained within are wideband topologies, the first being a

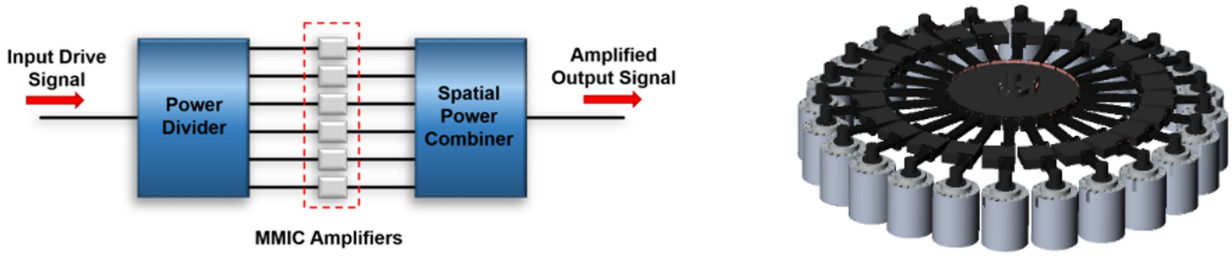
three-HEMT distributed amplifier, and the second being a cascode amplifier adapted from the isolator in the previous chapter. Following this discussion, two transceiver front ends are presented that contain a PA and LNA. The first front end is a half duplex system, integrating one of the SPDTs from the previous chapters. The second front end is a full duplex system, containing a tunable analog cancellation network that composes of three interconnected Lange couplers with two source-grounded HEMTs to tune the cancellation notch. Both front ends operate across W-band and are designed in T3. The first is the most wideband millimeter-wave GaN front end presented to date. The second is the only millimeter-wave full-duplex GaN front end presented to date.

8.2 Future Work

The designs in this thesis have provided a basis for new techniques along with the scalability of established methods to higher frequencies. This, combined with the development in state-of-the art GaN processes, provides many opportunities for improvement.

8.2.1 Spatial Combining of Ka-Band PAs for SatCom

The harmonically terminated output combiner unfortunately did not provide the boost in efficiency at Ka-band that was hoped for. However, the research topic is being revisited in a project funded by JPL for deep-space communications. This method among others will be tested in additional GaN processes not discussed in this chapter to achieve the most efficient PA MMICs possible at Ka-band. The required power for space communications ranges from tens of watts to kilowatts, so power combining will be necessary. Spatial combiners are in development at Ka-band for this effort. Packaging, reliability, and thermal performance will be key considerations for design. A diagram and CAD rendering of a spatial combiner are displayed in Fig. 8.2. These systems with solid-state spatially combined amplifiers allow for graceful degradation over the operation lifetime.



(a) (b)

Figure 8.2: (a) Diagram and (b) CAD rendering of amplifier MMIC spatial combiner [5].

8.2.2 FEP Model Manifold Study

Another topic of interest is improving the physics-based FEP transistor model. The bulk of this effort is limited to the foundry and their modeling partners, i.e. fabricating several different device sizes and validating them under a number of conditions. On the university side, we can insert these models into more complex systems to test the performance. When the first reticle using this model was fabricated, a second reticle of the same size was also assembled. A layout of this reticle is displayed in Fig. 8.3. Contained within the area are several breakout devices, along with a TRL kit and two additional test amplifiers designed at a lower frequency than the three from Chapter 3. The breakout devices are a variety of uniform and nonuniform gates pitches with four different peripheries. Additionally, the manifolds connecting to the gates contain different shapes. A hole can be seen on one of the manifolds with the hope of producing a uniform RF current distribution to each finger. The goal of these test structures is to see if nonuniform gate spacing or manifold manipulation can improve amplifier efficiency, as varying finger pitch may lead to uniform heat dissipation. These tests build upon the work in [172] with some additional variables, and are tested in collaboration with Professor Peter Aaen from the Colorado School of Mines.

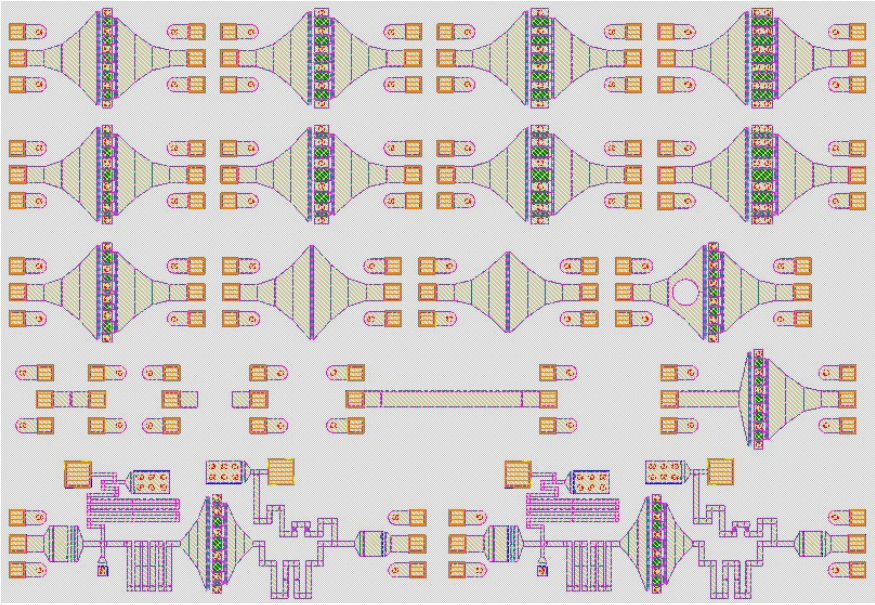
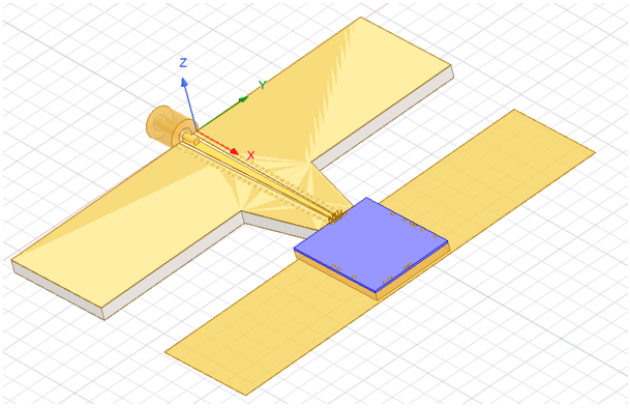


Figure 8.3: Second reticle from GaN Challenge tapeout. Several devices are broken out applying the nonuniform gate spacing FEP capability. Various manifold shapes and sizes are also included for some of the same devices, as well as two additional test amplifiers. Reticle size is 5 mm × 3.5 mm.

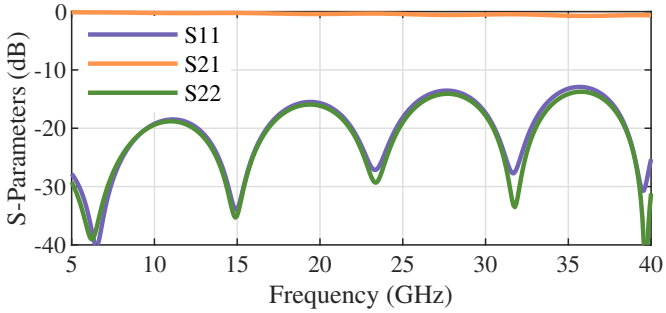
8.2.3 RF Design Challenge Packaging

Next, the four stage power amplifier discussed in Chapter 3 will be packaged for test with coaxial connectors. The design of the package is not trivial for a Ka-band amplifier. This process was performed for the first iteration of this power amplifier. The transition from coaxial to microstrip on the MMIC is first designed in a 3D FEM solver. The system is displayed in Fig. 8.4a. A rectangle the size of the die is drawn in the CAD software with RF GSG and dc pads placed appropriately according to the circuit layout. All pads are drawn close to the edge of the chip to reduce the size of bond wires. Next, a coaxial launcher is drawn using dimensions from a 2.4 mm connector which operates up to 50 GHz. To connect these two 50 Ω terminals, a coplanar waveguide (CPW) transition is drawn on a substrate. Careful attention must be placed on the spacing between ground and signal lines to fit the launcher without shorting it to ground. The spacing must decrease along the substrate to fit to the spacing of the GSG pads on chip. Bond wires, two on each pad, are then drawn connecting from the GSG to the CPW. This entire structure is simulated to capture the 2-port S-Matrix from coaxial to microstrip. A simulation of the structure is displayed in Fig. 8.4b. Return

loss is less than 13 dB and insertion loss is less than 1 dB from 5 GHz up to 40 GHz.



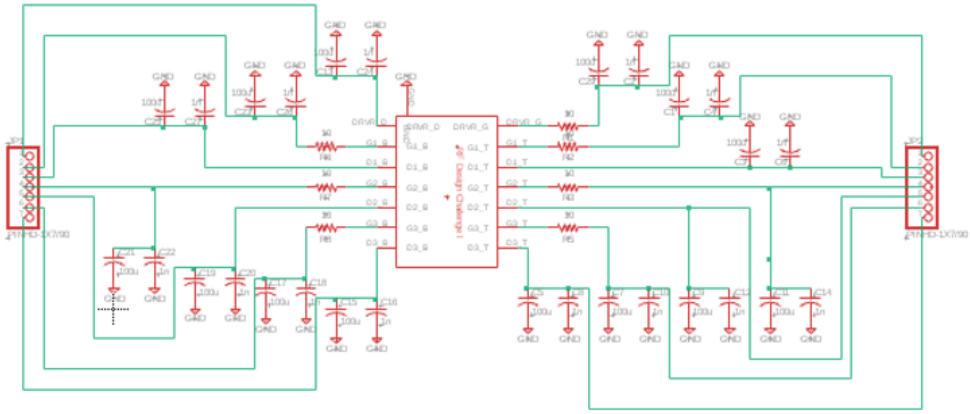
(a)



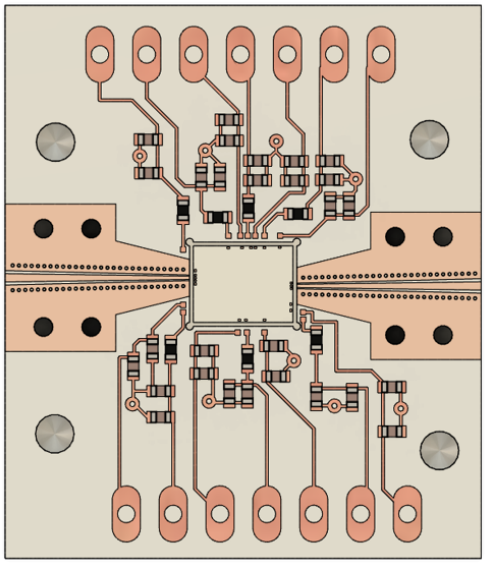
(b)

Figure 8.4: (a) CAD rendering and (b) simulated plot of co-planar waveguide transition.

DC connections to the MMIC are next designed onto the printed circuit board (PCB). A large number of off chip components are added onto the PCB due to stability concerns. For each dc pad, 0.1 pF and 1.0 pF bypass capacitors are added to short low frequency components through filled vias to the ground plane. Additionally, 10 Ω resistors are added in series to the gate paths. Holes are added for dc pin connectors. A schematic of the dc biasing circuit is displayed in Fig. 8.5a. A dc routing layout is drawn and combined with the CPW transitions. A 3D rendering of the entire PCB with surface mount components is displayed in Fig. 8.5b. Holes are also placed in the board so that it can be screwed into an aluminum base.



(a)



(b)

Figure 8.5: (a) Schematic and (b) CAD rendering of bias circuit with CPW transitions.

Five prototypes are assembled using this PCB and the MMICs, displayed in Fig. 8.6. The MMIC is first mounted onto the base using silver epoxy. Next, the PCB is screwed into the base, and bond wires are made from the MMIC onto the PCB. The surface mount components are then placed individually on the PCB with silver epoxy. Finally, the RF and dc connectors are attached with a soldering iron. Unfortunately, these prototypes did not yield measurable results due to instabilities. However, this process will be repeated for the power amplifier in Chapter 3.

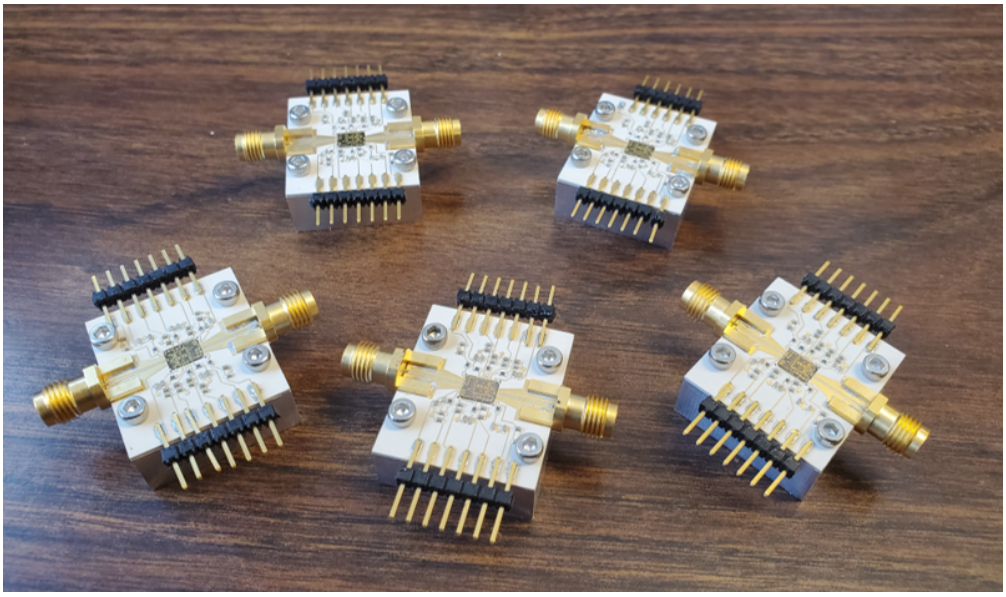


Figure 8.6: Packaged power amplifier prototypes delivered to AFRL.

8.2.4 W-band Rectifiers

Development of the HRL T3 process and the Navy STARRY NITE program has allowed CU Boulder students to design state-of-the-art millimeter wave GaN MMICs with the freedom to explore topologies not yet published at this frequency. One example is the transistor rectifier discussed in [54]. To summarize its operation, a high power signal is incident at the drain of a transistor. Power couples across the gate-to-source capacitance and is completely reflected to drive the gate which is dc biased. This produces a dc output at the drain of the device. A schematic of the topology is displayed in Fig. 8.7. A straightforward method for creating this circuit is to first design a high efficiency amplifier. The gate input is then replaced with a reflective element and the circuit can be tested as a rectifier as mentioned.

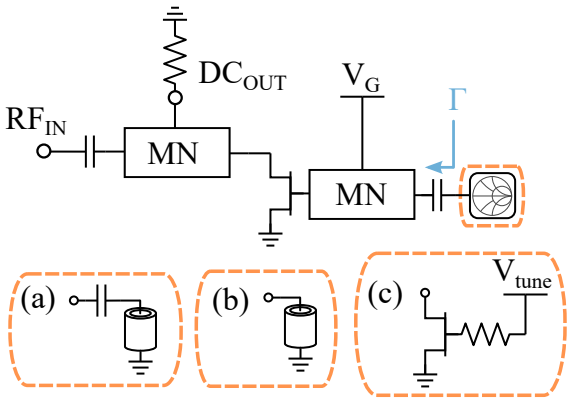
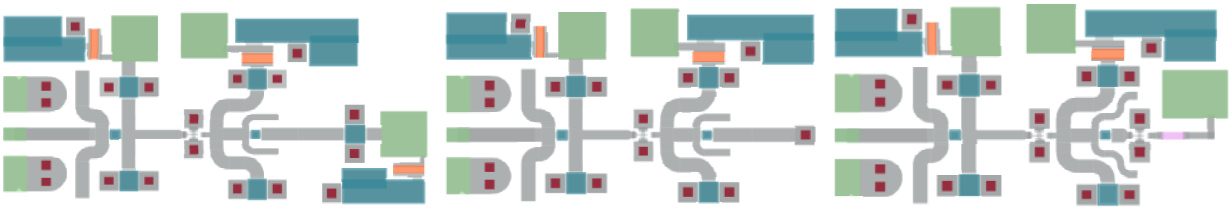


Figure 8.7: Generalized schematic of 90 GHz transistor rectifiers.

Three of these rectifiers are designed in the HRL T3 process using the single stage amplifier mentioned in Chapter 2. The gate terminations of the three rectifiers each contain a different element. The schematic depiction of these elements is displayed in Fig. 8.7, and the layouts in Fig. 8.8. Rectifier 1 in Fig 8.8a contains a resonant shunt capacitor, 2 in Fig. 8.8b a via, and 3 in Fig. 8.8c a source grounded HEMT which can be tuned by changing the gate voltage. The input and output matching networks are tuned slightly to maximize efficiency, $P_{OUT}(DC)/P_{IN}(RF)$.



(a) (b) (c)

Figure 8.8: Layout of three rectifiers designed in T3 process with (a) shunt capacitor, (b) via, and (c) tunable HEMT gate terminations.

A plot of the simulated efficiency for each rectifier is displayed in Fig. 8.9. All three rectifiers have a peak efficiency at 90 GHz of 29 % for rectifier 3 and 25 % for rectifiers 1 and 2. The maximum PAE of the amplifier adjusted for these designs was designed to 90 GHz so agreement between the two topologies matches well in frequency. The smallest modeled device size was selected for this design so that the circuits would saturate at a lower power. For each rectifier, the input power required to maximize efficiency

is between 13-19 dBm, although previous designs have demonstrated lower saturation in measurement as compared to simulation in this PDK [48, 111]. The measurement of these circuits involves the previously used large signal W-band setup from Chapters 4, 5, 6, and 7. Power will be swept over frequency as the output dc power is monitored. Once the frequency of the maximum dc power is found, drive up power sweeps can be performed at that frequency while also adjusting the drain impedance. For future designs, a DC-DC converter can be implemented to present the optimum impedance to the drain [173]. The three rectifier circuits are currently in fabrication and are awaiting testing.

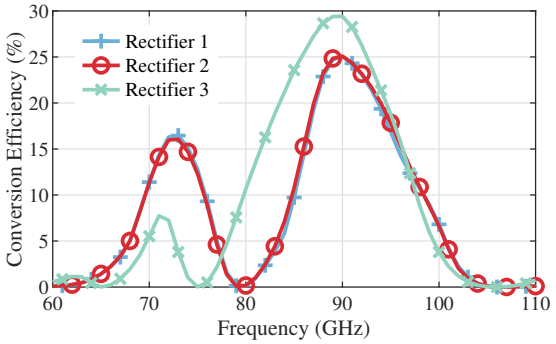


Figure 8.9: Simulated conversion efficiency for three rectifiers.

8.2.5 Integrated Front End and Circulator Topologies

The circuits presented throughout the course of this thesis, among others described in [30] can be combined to form more complex systems. A few of these systems were presented in Chapters 6 and 7. A suggested topology is displayed in Fig. 8.10. This resembles the circulator topology from Chapter 6, but with an additional phase shifter. Depending on the mode of operation (BSCM/FCM), the isolation in the forward or reverse path dominates the overall isolation of the circulator. However, adding a phase shifter in one of the branches adds the capability to combine isolation from both paths out of phase. Only one phase shifter is required since the isolation in either forward or reverse must pass through it. For example, if a signal is placed at P2, it would ideally have an output at P3 and be isolated at P1. The reverse isolated path from P2 to P1 is through Path 1, while the forward isolated path from P2 to P1 is through Path 2 then Path 3. Path 1 contains the phase shifter which can be adjusted to combine the two isolated paths out of phase.

Canceling the two paths also gives the added capability to increase forward gain, which has a negative effect on isolation in the original topology. Additional ways to improve the active circulator topology are to implement different designs for the amplifier paths, e.g. include a PA and LNA.

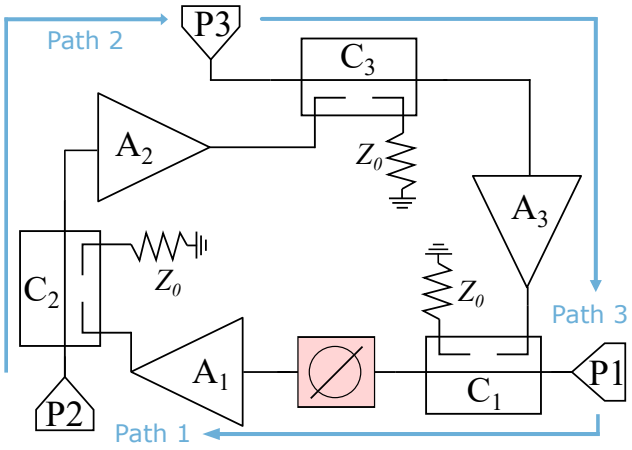


Figure 8.10: Block diagram of active circulator with integrated phase shifter.

The quasi-circulator presented in Chapter 7.2 can also be improved. A negative aspect of this circuit is that 3 dB of the transmitted signal is dissipated in the isolated port of the coupler connected to the LNA. For a large power amplifier with several Watts of output power, this can be significant. The rectifier circuit, once tested and validated, can be combined with the IBFD front end at this terminal to recover some of that power. This concept is displayed in Fig. 8.11, where the rectifier is used to power the LNA.

The applications for these systems are not limited to these suggested topologies. Many others, such as harmonically injected power amplifiers, diplexed power amplifiers, and various power recovery/energy harvesting circuits can be implemented.

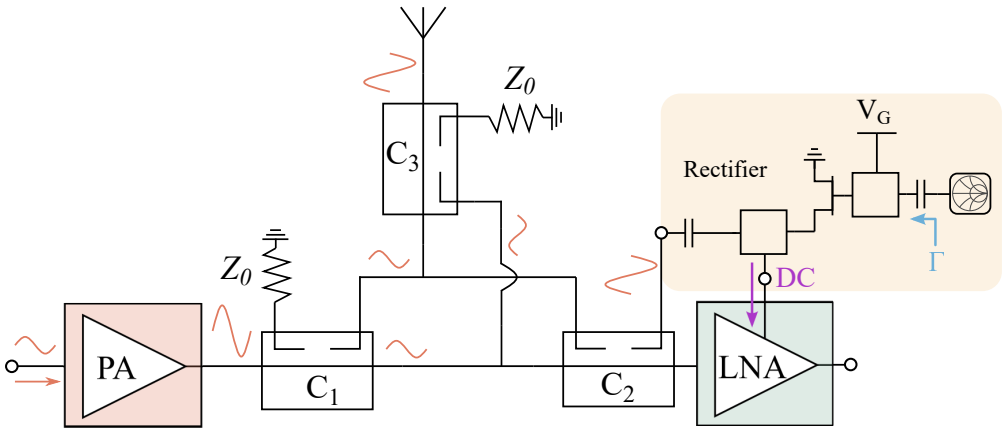


Figure 8.11: Block diagram of IBFD front end with power recovery.

8.3 Summary of Contributions

This thesis has led to several contributions in the area of millimeter wave GaN front end design. They are summarized as follows.

- Chapter 2: This chapter explores the design of different bias networks and their applications to millimeter wave MMIC amplifiers. Low-frequency techniques such as RF chokes, parallel resonant structures, and bypass capacitors are analyzed in both measurement and simulation. It is determined that the scaling of these techniques beyond 30 GHz results in performance degradation. RF signals can be more effectively reflected using microstrip lines with resonant structures such as small shunt capacitors, coupled filters, and radial stubs, while still allowing a path for dc current. Bias lines can also help amplifier stability by isolating the RF path from interference at other frequencies. This is achieved by adding large bypassing capacitors with some attenuation on the die or off chip. Results from this work are published in [67].

- Chapter 3: This chapter explores several different Ka-band amplifier designs in multiple processes. First, two power amplifiers are designed with harmonic terminations integrated into an output combining network. This topology boosted efficiency in simulation, but did not translate to measurements. Ongoing studies with alternative PDKs may lead to improved results. Next, three single-stage amplifiers and one four-stage power amplifier are designed to test the robustness of the FEP

model with finger pitch scaling and comparison to foundry models. In both small and large signal, the FEP model appears over-optimistic in terms of gain and efficiency, as is evident from S-Parameters and large signal characterization. A shift in the target impedance from load pull compared to foundry models is the suspected reason for the shift in frequency in measurement. However, foundry models do not properly predict the input power where compression occurs. Further improvements and studies with the FEP model are ongoing outside of CU Boulder.

- Chapter 4: This chapter presents design, simulation, and measurements of continuous 90° and 180° phase shifters in a reflective topology. Measured results show greater than 90° phase shift across 50–110 GHz with less than 10 dB average loss over a control voltage range of –1 V to +1 V, and a measured 1 dB compression point of 19 dBm at 95 GHz. Cascading two 90° phase shifters results in a 180° phase shifter in which toggling each set of tunable devices independently is shown to improve insertion loss by as much as 15 dB while providing the same phase change. The GaN phase shifters presented here show the largest bandwidth with maintained phase variation up to 180° and with comparable insertion loss and area. The power handling is greater than 22 dBm, limited by our measurement capability, and the phase shifters do not consume any dc power. Results from this work are published in [30, 108, 111]

- Chapter 5: Several wideband circuits that serve as building blocks for duplexers are detailed in this chapter. An SPST and three SPDT designs are first discussed. A wideband cascode amplifier with high reverse isolation is then detailed. The isolator circuit operates over a much wider bandwidth and at higher frequencies with comparable isolation and noise figure to other designs. Results from this work are published in [30, 48, 120].

- Chapter 6: This chapter presents two active MMIC circulators designed in a ring topology consisting of three amplifiers and three Lange couplers. The first circulator employs traveling wave amplifiers and uniform Lange couplers, while the second uses cascode amplifiers to improve reverse isolation and nonuniform Lange couplers to improve noise figure while maintaining the same insertion loss. The two millimeter-wave broadband circulators are presented in two reconfigurable

operation modes, showing isolation from 50–110 GHz. A comparison to other selected topologies indicates a wider bandwidth, higher isolation and higher compression level than other demonstrated devices. Results from this work are published in [128, 148, 149].

- Chapter 7: Both full and half duplex W-band transceivers are presented in this chapter. The half-duplex front end is by far the most wideband of all W-band T/R front ends, while still providing comparable output power, noise figure, and gain across the band. Meanwhile, the second presented chip is also very wideband and is the only full-duplex W-band GaN front end published to date. Its specified frequency range will also widen in the near future as V-band has not yet been characterized. Results from this work are published in [147, 171].

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